GPDK446

(Generic PDK Process)

BASELINE

Process Design Kit (PDK)

Specification Document

Revision 1.1
1.0 Overview

The purpose of this specification document is to describe the technical details of the GPDK446 Generic Process Design Kit (“PDK”) provided by Cadence Design Systems, Inc. (“Cadence”). This PDK was tested for use with Cadence IC 4.4.6 Release. This PDK requires the environmental variable “CDS_Netlisting_Mode” to be set to “Analog”. Training is not provided as part of this PDK. **THIS PDK IS INTENDED TO BE USED FOR DEMOOSTRATION PURPOSES ONLY.**

2.0 Supported Devices

2.1 MOSFETS

- nmos - NMOS transistor
- nmos3 - 3 terminal NMOS transistor with an inherited connection for the Body
- pmos - PMOS transistor
- pmos3 - 3 terminal PMOS transistor with an inherited connection for the Body

2.2 RESISTORS

- nplusres – N+ Diffused Resistor
- polyres – Poly Resistor

2.3 CAPACITORS

- mimcap - metal to metal capacitor
  - CapA = 0.1fF/um²
  - CapP = 0.01fF/um
- nmoscap - NMOS transistor configured as a capacitor

2.4 INDUCTOR

- inductor – Metal 3 Inductor
2.5 BIPOLARS

- vnp - CMOS vertical PNP with substrate collector
  - Fixed emitter area
- npn - Bipolar NPN
  - Variable emitter area
- pnp - Bipolar vertical PNP
  - Variable emitter area

2.6 DIODES

- ndio - N type diode
  - Variable diode length and width
- pdio - P type diode
  - Variable diode length and width
3.0 Views provided

3.1 MOSFETS
- Four terminals (D, G, S, B)
- symbol, spectre, auLvs, auCdl, ivpcell, layout (Pcells)

3.2 RESISTORS
- Three terminals (PLUS, MINUS, B) for diffused resistor
- Two terminals (PLUS, MINUS) for poly resistor
- symbol, spectre, auLvs, auCdl, ivpcell, layout (Pcells)

3.3 CAPACITORS
- Two terminals (PLUS, MINUS) for mimcap
- Three terminals (TOP, BOT, B) for nmoscap
- symbol, spectre, auLvs, auCdl, ivpcell, layout (Pcells)

3.4 INDUCTOR
- Two terminals (PLUS, MINUS)
- symbol, spectre, auLvs, auCdl, ivpcell, layout (Pcells)

3.5 BIPOLARS
- Three terminals (C, B, E)
- symbol, spectre, auLvs, auCdl, ivpcell, layout (Fixed for vnpn, Pcells for npn,pnp)

3.6 DIODES
- Two terminals (PLUS, MINUS)
- symbol, spectre, auLvs, auCdl, ivpcell, layout (Pcells)
4.0 CDF parameters

4.1 MOSFETS

- **Model Name** - Spectre model name (non-editable)
- **l (M)** - gate length in meters
- **Calculate Width Method** - cyclic which control user entry of total Width value or individual finger Width value
- **w (M)** - gate width in meters (non-editable using fingerWidth)
- **Number of Fingers** - Number of poly gate stripes used in layout (w/nf width)
- **Width Per Finger** - Width of each gate stripe (non-editable using totalWidth)
- **Multiplier** - Number of Parallel MOS devices
- **Calc Diff Params** - cyclic which controls the calculation of area and periphery of the source/drain regions for simulation. Default is true which auto calculates the values. If nil, the user can enter the values.

  - **Source diffusion area** - Calculated source diffusion area in square meters
  - **Drain diffusion area** - Calculated drain diffusion area in square meters
  - **Source diffusion periphery** - Calculated source diffusion periphery in meters
  - **Drain diffusion periphery** - Calculated source diffusion periphery in meters

4.2 RESISTORS

- **Resistance** - Resistance value used for simulation
- **w (M)** - resistor width in meters
- **l (M)** - resistor length in meters (non-editable)
- **Number of Series Segments** - Number of series resistor legs used in layout
- **Number of Parallel Segments** - Number of parallel resistor legs used in layout
- **Segment Spacing** - spacing between series or parallel resistor legs
- **Rho** - resistor layer sheet rho (non-editable)
- **Area** - resistor area for parasitics (non-editable)
- **Perim** - resistor perimeter for parasitics (non-editable)
- **Model name** - not used for default specte simulation
4.3 CAPACITORS

- **Capacitance** - capacitance value used in simulation
- **total Capacitance** - Capacitance multiplied times Multiplier (non-editable)
- **l (M)** - capacitor length in meters (non-editable for mimcap)
- **w (M)** - capacitor width in meters (non-editable for mimcap)
- **Multiplier** - Number of devices in layout (non-editable for mimcap)
- **CapA (F/M^2)** - Plate Capacitance (non-editable, units are Farads per Meter Squared)
- **CapP (F/M^2)** - Fringe Capacitance (non-editable, units are Farads per Meter Squared)

The following parameters are for the nmoscap only

- **Spec** - cyclic used to choose capacitor entry method (Capacitance, Cap & l, l & w)
- **Number of Fingers** - Number of poly gate stripes used in layout (w/nf width)
- **Width Per Finger** - Width of each gate stripe (non-editable using totalWidth)
- **Multiplier** - Number of Parallel MOS devices
- **Calc Diff Params** - cyclic which controls the calculation of area and periphery of the source/drain regions for simulation. Default is true which auto calculates the values. If nil, the user can enter the values.

- **Source diffusion area** - Calculated source diffusion area in square meters
- **Drain diffusion area** - Calculated drain diffusion area in square meters
- **Source diffusion periphery** - Calculated source diffusion periphery in meters
- **Drain diffusion periphery** - Calculated source diffusion periphery in meters

4.4 INDUCTOR

- **Inductance (H)** - Inductance in Henry’s based on calculation (non-editable)
- **Number of Turns** - Fixed number of coil turns (1.5, 2.5, 3.5, 4.5, 5.5, 6.5, 7.5, 8.5, 9.5)
- **Inner Radius** - Radius of inner coil (non-editable)
- **Inductor Space** - Space of top metal (non-editable)
- **Inductor Width** - Width of top metal (non-editable)
4.5 BIPOLARS

- Model name - Spectre model name (non-editable)
- Area - Emitter Area (non-editable)
- Emitter width - the width of the emitter, in meters (For npn and pnp only)
- Emitter Size - the length and width of the emitter, in meters (For vpn only)
- Multiplier - Number of Parallel Bipolar devices

4.6 DIODES

- Model name - Spectre model name (non-editable)
- Device Area - Calculated junction area in meters squared (non-editable)
- Multiplier - Number of Parallel Diode devices
- Length (M) - diode length in meters
- Width (M) - diode width in meters
5.0 Component Label Defaults

5.1 MOSFETS
- component parameters: l, w, fingers, m
- operating point: ids, vgs, vds, vth, vdsat
- model: vto, kp, gamma
- instance name prefix: MN, MP

5.2 RESISTORS
- component parameters: r, w, l
- operating point: v i pwr
- model: -
- instance name prefix: R

5.3 CAPACITORS
- component parameters: c, l, w, m
- operating point: -
- model: -
- instance name prefix: C

5.4 INDUCTORS
- component parameters: model, nr, rad
- operating point: -
- model: -
- instance name prefix: L

5.5 BIPOLARS
- component parameters: model, area, m
- operating point: betadc, ic, Vce
- model: bf, is, va
- instance name prefix: Q
5.6 DIODES

- component parameters: model, area, m
- operating point: id, vd, reg
- model: is, rs, n
- instance name prefix: D
6.0 Spectre Models/Netlist Format

Spectre models will be provided with this PDK.

6.1 MOSFETS

- nmos - NMOS Transistor
  MN0 (D G S B) nmos1 w=2u l=180.0n as=1.2e-12 ad=1.2e-12 ps=3.2u
  \[pd=3.2u \quad m=(1)\]

- pmos - PMOS Transistor
  MP0 (D G S B) pmos1 w=2u l=180.0n as=1.2e-12 ad=1.2e-12 ps=3.2u
  \[pd=3.2u \quad m=(1)\]

6.2 RESISTORS

- nplusres - N+ Diffused Resistor
  R0 (PLUS MINUS B) resistor r=1k Area=1.2985e-11 Perim=3.85e-05

- polyres - Poly Resistor
  R1 (PLUS MINUS) resistor r=1k

6.3 CAPACITORS

- mimcap - Metal to Metal Capacitor
  C1 (PLUS MINUS) cap c=1p m=1

- nmoscap - Nmos configured as a Capacitor
  C2 (BOT TOP BOT B) nmos1 w=10u l=10u as=6e-12 ad=6e-12
  \[ps=11.2u \quad pd=11.2u \quad m=(1)\]

6.4 INDUCTOR

- inductor - Metal3 Inductor
  L0 (PLUS MINUS) inductor l=2.625e-09
6.5 BIPOLARS

- **vnpv** - Vertical PNP
  
  Q0 (C B E) vnpv  area=1.69e-12  m=1

- **nnpn** - Bipolar NPN
  
  Q1 (C B E) nnpn  area=3.6e-13  m=1

- **ppnp** - Bipolar PNP
  
  Q0 (C B E) pnp  area=3.6e-13  m=1

6.6 DIODES

- **ndio** - N type diode
  
  D0 (PLUS MINUS) dion  area=1e-12   pj=4e-06  m=1

- **pdio** - P type diode
  
  D1 (PLUS MINUS) diop  area=1e-12   pj=4e-06  m=1
7.0 Techfile Layers

Cadence to provide standard display setup, and will not support desired changes to the display. Customer is free to modify the display.drf file used on-site to achieve any desired display.

Techfile Layers

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</tbody>
</table>
8.0 Virtuoso XL

The standard Cadence Virtuoso XL design flow will be implemented. This includes basic connectivity of connection layers, wells, and substrate, and symbolic contacts. The M factor will be used for device instance multiplier - there will be no conflict with the parameter used in cell operation. Names will be displayed on the layout views to aid in schematic-layout instance correlation. Auto-abuttment of MOSFET devices is supported. Pin permuting of MOSFET and Resistor device is also supported. The skill pcell layouts are compiled into the PDK.

NOTE: Skill pcell source code is not included in the PDK kit.
8.1 SYMBOLIC CONTACTS

- M1_NIMP – Metal 1 to Nimp, Oxide contact
- M1_NWELL – Metal 1 to Nwell contact
- M1_PIMP – Metal 1 to Pimp, Oxide contact
- M1_POLY1 – Metal 1 to Poly contact
- M1_PSUB - Metal1 to Substrate contact
- M2_M1 – Metal 2 to Metal 1 via contact
- M3_M2 – Metal 3 to Metal 2 via contact
- M4_M3 – Metal 4 to Metal 3 via contact
- M5_M4 – Metal 5 to Metal 4 via contact
- M6_M5 – Metal 6 to Metal 5 via contact
9.0 Device Layer Usage

9.1 MOSFETS (pcell layouts)
- nmos - Oxide, Poly, Nimp, Cont, Metal1, WellBody
- pmos - Nwell, Oxide, Poly, Pimp, Cont, Metal1

9.2 RESISTORS (pcell layouts)
- nplusres - Oxide, Nimp, Cont, Metal1, Resdum
- polyres – Poly, Cont, Metal1, Resdum

9.3 CAPACITORS (pcell layouts)
- mimcap - Metal2, CapMetal, Via2, METAL3, Capdum
- nmoscap – Oxide, Poly, Nimp, Cont, Metal1, WellBody, Capdum

9.4 INDUCTOR (pcell layouts)
- inductor - Metal2, Via2, METAL3, INDdummy, IND2dummy

9.5 BIPOLARS (fixed & pcell layout)
- vnp - Nwell, Nimp, Pimp, Oxide, BJTdum, Cont, Metal1 (Fixed)
- npn - Nwell, Pwell, Nburied, Nimp, Pimp, Oxide, NPNdum, Cont, Metal1 (Pcell)
- pnp - Nwell, Pwell, Nburied, Nimp, Pimp, Oxide, PNPdum, Cont, Metal1 (Pcell)

9.6 DIODES (pcell layout)
- ndio - Nimp, Pimp, Oxide, Cont, Metal1, DIOdummy (Pcell)
- pdio - Nwell, Nimp, Pimp, Oxide, Cont, Metal1, DIOdummy (Pcell)
10.0 Dracula Support

No Dracula support will be provided with the exception of creating an auCdl netlist. Listed below is an example of the CDL netlist for each device.

10.1 MOSFETS

- nmos - NMOS transistor
  
  MNM0 D G S B N W=2u L=180.0n M=1.0

- pmos - PMOS transistor
  
  MPM0 D G S B P W=2u L=180.0n M=1.0

10.2 RESISTORS

- nplusres - N+ diffused resistor
  
  RR0 PLUS MINUS 1.5K $[NR]

- polyres - P+ poly resistor
  
  RR4 PLUS MINUS 170.606 $[PR]

10.3 CAPACITORS

- mimcap - Metal capacitor
  
  CC1 PLUS TOP MINUS 1000f $[MC]

- nmoscap - NMOS capacitor
  
  MC1 BOT TOP BOT B N W=10u L=10u M=1

10.4 INDUCTOR

- inductor - Metal3 inductor
  
  QL0 PLUS MINUS inductor

10.5 BIPOLARS

- vpnnp - Vertical PNP
  
  QQ0 gnd! B E PV M=1 $EA=1.69e-12 $W=4e-05 $L=2.5e-06

- npn - Bipolar NPN
  
  QQ1 C B E NP M=1 $EA=3.6e-13

- pnp - Bipolar PNP
  
  QQ2 C B E PN M=1 $EA=3.6e-13
10.6 DIODES

- **vppn** - Vertical PNP
  
  QQ0 PLUS MINUS ndio 1e-12

- **nppn** - Bipolar NPN
  
  QQ1 PLUS MINUS pdio 1e-12
11.0 Diva Decks

Cadence has developed DIVA Antenna, Density, DRC, LVS, and LPE/PRE decks based on the information contained in this specification.

11.1 DIVA DRC

Three separate DIVA DRC rules files have been provided with this PDK and are based on the design rules outlined in Section 12.0 of this document.

The three files are:

- divaDRC.rul - This rule file is for checking the design rules outlined in Sub-Section 12.1 of this document.

The following switches are available in the divaAntenna.rul file:

- Check_CO_Antenna - Perform Contact Antenna checks
- divaANT.rul - This rule file is for checking Antenna rules only (see Sub-Section 12.2 of this document).

The following switches are available in the divaAntenna.rul file:

- Check_CO_Antenna - Perform Contact Antenna checks
- Check_M1_Antenna - Perform Metal 1 Antenna checks
- Check_M2_Antenna - Perform Metal 2 Antenna checks
- Check_M3_Antenna - Perform Metal 3 Antenna checks
- Check_M4_Antenna - Perform Metal 4 Antenna checks
- Check_M5_Antenna - Perform Metal 5 Antenna checks
- Check_M6_Antenna - Perform Metal 6 Antenna checks
- Check_Poly_Antenna - Perform Poly Antenna checks
- Check_V1_Antenna - Perform Via 1 Antenna checks
- Check_V2_Antenna - Perform Via 2 Antenna checks

- divaDEN.rul - This rule file is for checking Density rules only (see Sub-Section 14.3 of this document).

The following switches are available in the divaAntenna.rul file:

- Check_CO_Antenna - Perform Contact Antenna checks
11.2 DIVA LVS

The parameters checked in LVS include:

- MOS Devices - type, length and combination of width, “m” factor
- Resistors - type, width, and value
- Capacitors – type, area and capacitance
- Bipolars – type and area

11.3 DIVA EXTRACT

The DIVA EXTRACT rule decks contains the following switches:

Skip_Soft-Connect_Checks - Do not DRC flag well regions that are connected only through the well. This is valid for both nmos and pmos devices.

CHECK_PARASITIC_C - When switch is set parasitic capacitors will be generated in the extracted view. The standard Cadence flow is used to perform post-layout simulations.

CHECK_PARASITIC_RC - When switch is set parasitic resistors and capacitors will be generated in the extracted view. The standard Cadence flow is used to perform post-layout simulations.

SKIP_MERGE_VIA_ARRAYS - When switch is set all via arrays will NOT be merged into a single object. The default is to merge vias as it leads to smaller device counts.

11.4 DIVA LPE/PRE

The PDK will utilizes the interconnect coefficients listed in Section 15 of this document.

For Capacitance:
- Section 13 - Interconnect Capacitance Table.

For Resistance:
- Section 14 - Sheet Resistance Table.

Note: The resistance extraction is written with a 10 square distribution setting.
12.0 DESIGN RULES

12.1 Layout Guidelines

1A Minimum NWELL width 1.0um
1B Minimum NWELL space 1.0um
2A Minimum OXIDE width 0.4um
2B Minimum OXIDE space 0.3um
2C Minimum NWELL enclosure of OXIDE 0.5um
3A Minimum NIMP width 0.4um
3B Minimum NIMP space 0.4um
3C Minimum NIMP enclosure of OXIDE 0.2um
4A Minimum PIMP width 0.4um
4B Minimum PIMP space 0.4um
4C Minimum PIMP enclosure of OXIDE 0.2um
5A Minimum POLY width 0.18um
5B Minimum POLY space 0.3um
5C Minimum POLY extension beyond OXIDE (poly endcap) 0.2um
5D Minimum OXIDE extension beyond gate POLY 0.4um
5E Minimum Poly to OXIDE spacing 0.2um
6A Minimum and maximum width of CONT 0.2um
6B Minimum CONT space 0.2um
6C Minimum OXIDE enclosure of CONT 0.2um
6D Minimum POLY enclosure of CONT 0.2um
6E Minimum POLY to CONT space 0.2um
7A Minimum METAL1 width 0.3um
7B Minimum METAL1 space 0.3um
7C Minimum METAL1 enclosure of CONT 0.1um
8A Minimum and maximum width of VIA1 0.2um
8B Minimum VIA1 space 0.3um
8C Minimum METAL1 enclosure of VIA1 0.1um
9A Minimum METAL2 width 0.3um
9B Minimum METAL2 space 0.3um
9C Minimum METAL2 enclosure of VIA1 0.1um
10A Minimum and maximum width of VIA2 0.2um
10B Minimum VIA2 space 0.3um
10C Minimum METAL2 enclosure of VIA2 0.1um
11A Minimum METAL3 width 0.3um
11B Minimum METAL3 space 0.3um
11C Minimum METAL3 enclosure of VIA2 0.1um
11D Minimum METAL3 enclosure of VIA2 for metal capacitor 0.1um
12A Minimum CAPMETAL width 0.5um
12B Minimum METAL2 enclosure of CAPMETAL 0.4um
12C Minimum CAPMETAL enclosure of VIA2 0.2um
12D Minimum CAPMETAL enclosure of METAL3 0.3um
13A Maximum distance from a source/drain OXIDE region to the nearest well tie 10um
14A Minimum and maximum width of VIA3 0.2um
14B Minimum VIA3 space 0.3um
14C Minimum METAL3 enclosure of VIA3 0.1um
15A Minimum METAL4 width 0.3um
15B Minimum METAL4 space 0.3um
15C Minimum METAL4 enclosure of VIA3 0.1um
16A Minimum and maximum width of VIA4 0.2um
16B Minimum VIA4 space 0.3um
16C Minimum METAL4 enclosure of VIA4 0.1um
17A Minimum METAL5 width 0.3um
17B Minimum METAL5 space 0.3um
17C Minimum METAL5 enclosure of VIA4 0.1um
18A Minimum and maximum width of VIA5 0.2um
18B Minimum VIA5 space 0.3um
18C Minimum METAL5 enclosure of VIA5 0.1um
19A Minimum METAL6 width 0.3um
19B Minimum METAL6 space 0.3um
19C Minimum METAL6 enclosure of VIA5 0.1um
12.2 Antenna Rules

ANT1 Maximum ratio of field poly area to poly gate area 100
ANT2 Maximum ratio of metal area (METAL1 to METAL6) to poly gate area 200
ANT3 Maximum ratio of contact area to the poly gate area 10
ANT4 Maximum ratio of VIA area (VIA1 and VIA2) to poly gate area 20

12.3 Density Rules

DEN1 Minimum POLY density* 15%
DEN2 Minimum METAL1 density* 25%
DEN3 Minimum METAL2 density* 25%
DEN4 Minimum METAL3 density* 25%
DEN5 Minimum METAL4 density* 25%
DEN6 Minimum METAL5 density* 25%
DEN7 Minimum METAL6 density* 25%

*Density is calculated as Total POLY/METAL area/Chip area
### 13.0 Interconnect Capacitance Table

<table>
<thead>
<tr>
<th>Top Layer</th>
<th>Bottom Layer</th>
<th>Area Capacitance aF/um2</th>
<th>Fringe Capacitance aF/um</th>
<th>Dielectric Thickness</th>
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</thead>
<tbody>
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## 14.0 Coupling Capacitance Table

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### 15.0 Sheet Resistance Table

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