Mm-Wave Phase Shifter and Phase Array IC Design

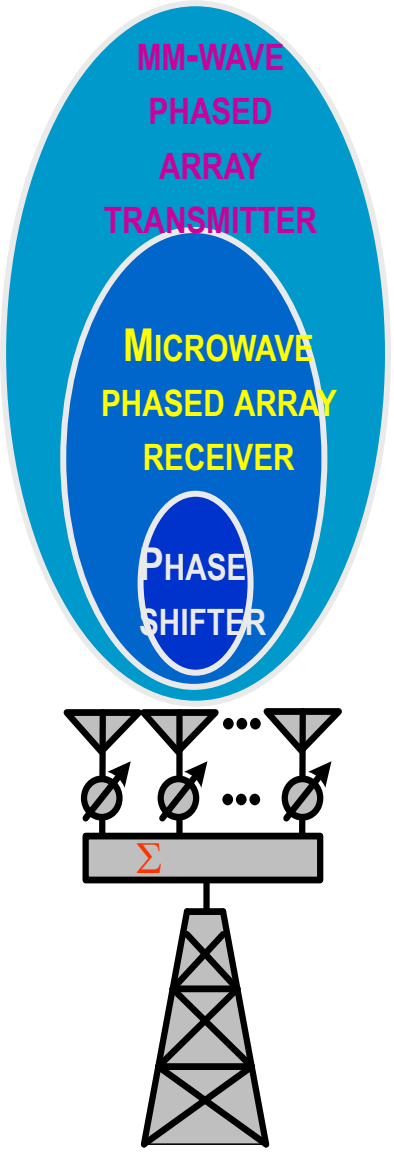
Outline

- Introduction- mm-Wave phase shifter design
- Passive phase shifters
  - Switched transmission line phase shifter
  - The high-pass/low-pass phase shifter
  - Reflection type phase shifter
- Active Phase shifters
  - Vector-Summing Phase Shifter
  - Quadrature all-pass filters
  - 90◦ hybrid coupler
- Conclusion

Outline

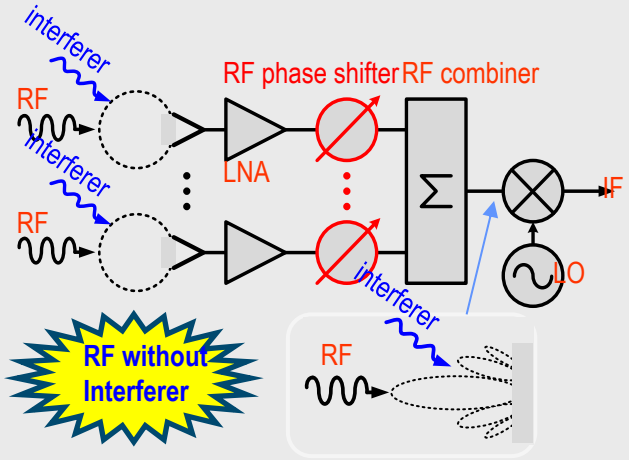
Phased Array IC Design

- Phased array receiver @ 12 GHz
  - IC-design, chip & board level verification
- Phased array transmitter @ 44 GHz
  - IC-design & chip level verification
- Conclusions



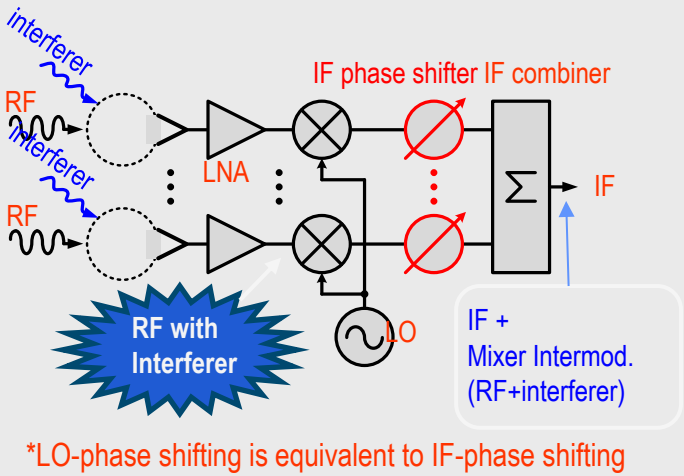
Introduction

RF-SCANNED PHASED ARRAY



- Need 1 mixer (simple)
- Mixer "sees" high directivity pattern
- Widely used (since 1950)

IF (LO)-SCANNED PHASED ARRAY



*LO-phase shifting is equivalent to IF-phase shifting

- Need # N mixers (complex)
- Mixer "sees" low directivity pattern
- Limited applications

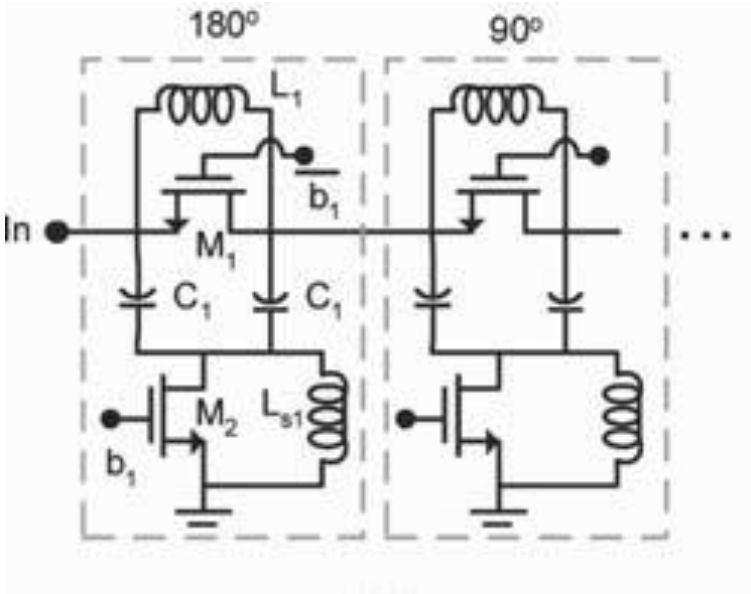
- For on-chip integration, RF phase shifting is much better (lower power, high linearity)
- RF phase shifting architecture meets backward compatibility with existing systems

Passive Phase Shifters

Switched transmission line phase shifter

Multiple, quasi-distributed, transmission-line

Π-sections, combined with MOSFET switches.



This phase shifter has:

- **Good linearity performance.**

The main challenge is:

- **The loss associated with the MOSFET switches.**

Ref: B.W. Min, et al, " Ka-Band BiCMOS 4-Bit Phase Shiftrer with Integrated LNA for Phased Array T/R Modules", IEEE/MTT-S, June, 2007.

Performance:

4 bit phase-shifter implemented in a 0.13μm SiGe BiCMOS technology.

The insertion loss is **13dB** from **30-38GHz**.

Phase error is less than **7°**.

Passive Phase Shifters

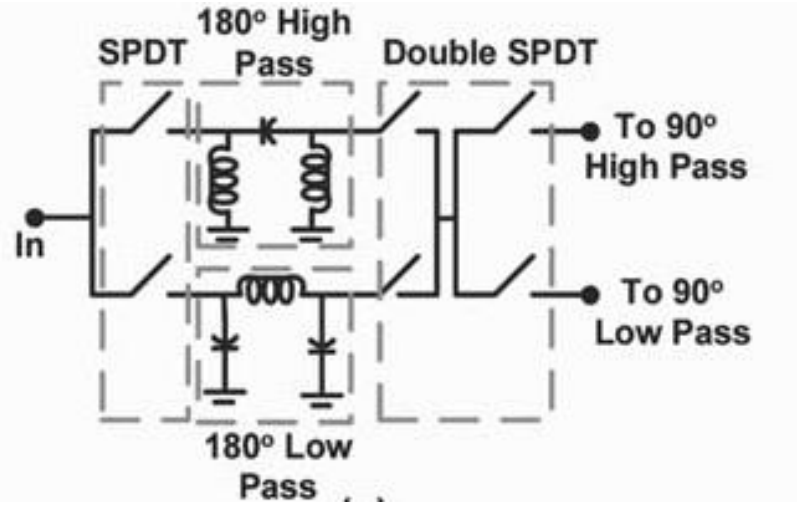
The high-pass/low-pass phase shifter

Phase Shift: Difference between the phase response of a high-pass path and a low-pass path.

- Each individual bit is designed for different phase differences.
- Good Linearity Performance

The challenges:

- Losses in the passive elements and the switches.



Performance:

5 bit phase-shifter implemented in a 200GHz SiGe BiCMOS technology,

the insertion loss is **18dB** from **8-12GHz**.

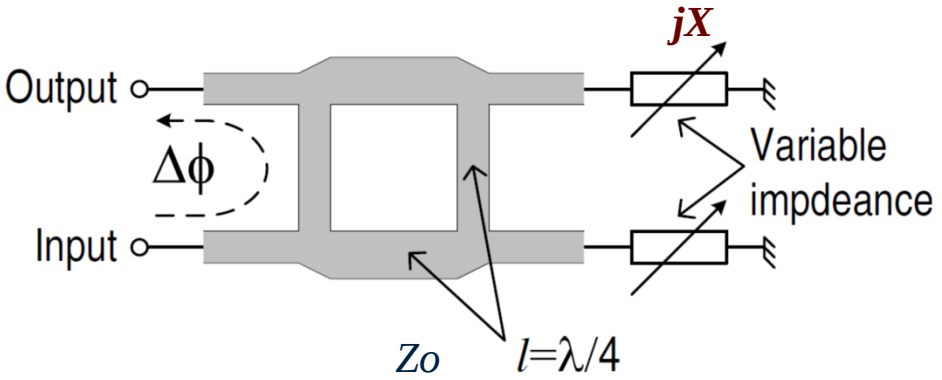
Absolute rms phase error is less than **8°**

M. Morton, et al "Sources of Phase Error and Design Considerations for Silicon-Based Monolithic High Pass/Low-Pass Microwave Phase Shifters," *IEEE Transactions on Microwave Theory and Techniques*, Dec. 2006.

Passive Phase Shifters

Reflection-Type Phase Shifter (RTPS)

- Includes: 4-port directional coupler and purely reflective (imaginary) loads.
- Phase of the output varies by varying the imaginary termination.



C. T. Charles, et al "A 2-GHz Integrated CMOS Reflective-type Phase Shifter with 675◦ Control Range," IEEE International Symposium on Circuits and Systems, May 2006.

The total phase shift: $-\pi/2 - 2\tan^{-1}(Zo/X)$,

Zo is the impedance to which the ports are matched.

- For a total phase variation of 180◦, the termination capacitance must vary from 0 to ∞, cannot be realized with varactor.
- To maximize the achievable phase shift range, higher order terminations are employed, such as series LC networks.

Passive Phase Shifters

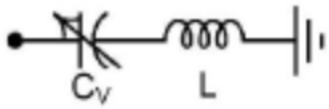
Reflection-Type Phase Shifter (RTPS)

- **Good linearity performance.**

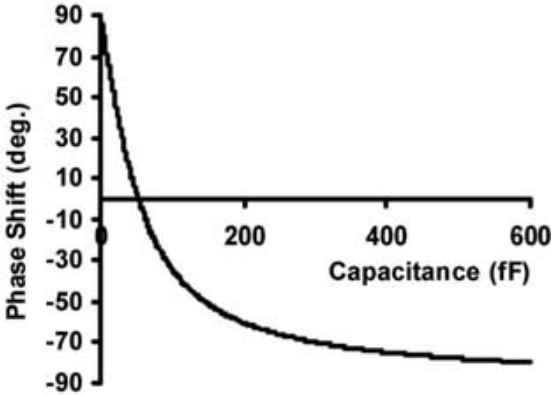
The main challenge is

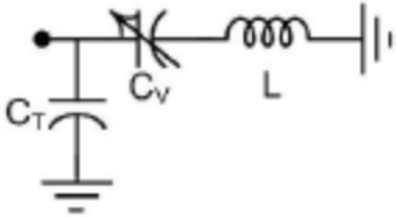
- **Loss Associated by Switch and TLs.**

Varactor



Single resonated load (SRL)





Transformed single resonated load (TSRL),

Performance:

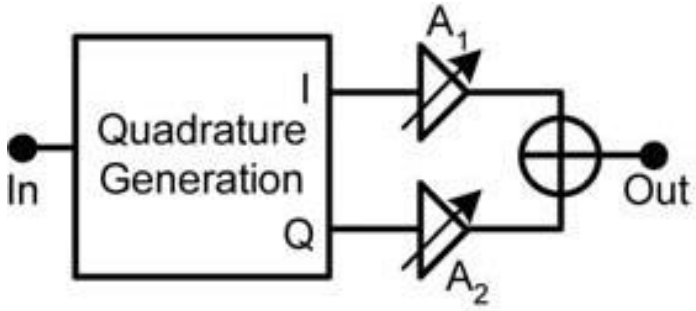
2GHz phase-shifter implemented in a 0.18 um CMOS process, phase change 343º.
The insertion loss is -10dB, and noise figure is 19 dB, for 0-1.8V operation.

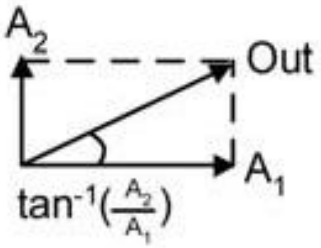
Active Phase Shifters

Vector-Summing Phase Shifter

- Quadrature generation block.
- Variable-gain amplifiers
- Combiner.

Phase of the output is **$\tan^{-1}(A2/A1)$**





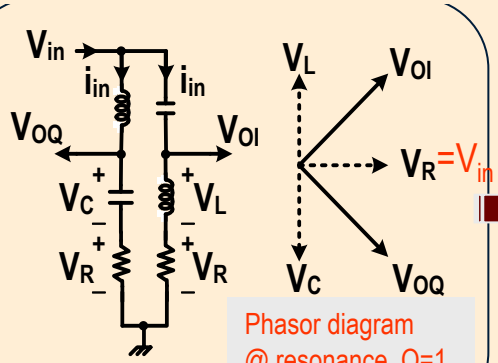
The quadrature generation block can be implemented in a number of ways.

- **Quadrature all-pass filters (QAF).**
- **90◦ hybrid coupler.**

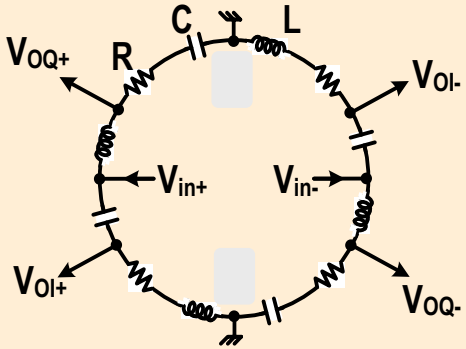
Vector-Summing Phase Shifter (Quadrature all-pass filters)

Passive signal interpolation for quadrature vector synthesis !

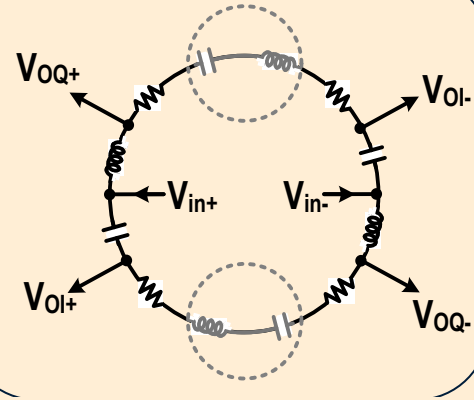
1. Single-ended quadrature generation



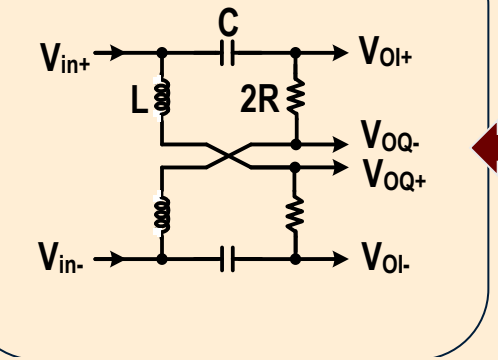
2. Differential configuration



3. Elimination by series resonance



4. Differential Quadrature All-pass Filter (QAF)



NOTE

- Step-1: 3-dB gain @ resonance
- Step-3: bandwidth extension (by removing L-C energy storage pair, de-Q)
- All-pass filter with 3dB NF

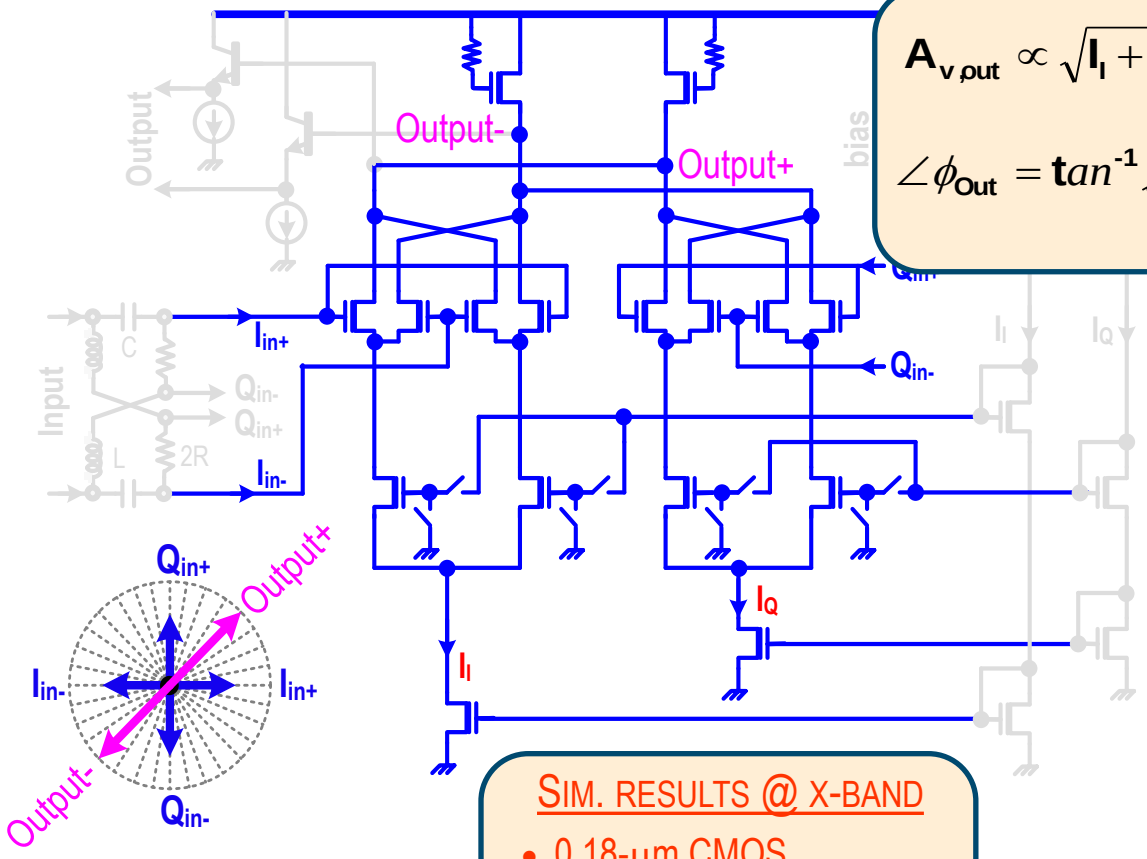
TRANSFER FUNCTION

$$\begin{pmatrix} V_{OI\pm} \\ V_{OQ\pm} \end{pmatrix} = V_{in\pm} \times \left(\underbrace{\frac{s^2 + \frac{2\omega_o}{Q}s - \omega_o^2}{s^2 + \frac{2\omega_o}{Q}s + \omega_o^2}}_{\text{I-path}} \underbrace{\frac{s^2 - \frac{2\omega_o}{Q}s - \omega_o^2}{s^2 + \frac{2\omega_o}{Q}s + \omega_o^2}}_{\text{Q-path}} \right)$$

$$\text{where, } Q = \frac{\omega_o L}{R}, \omega_o = \frac{1}{\sqrt{LC}}$$

Ref: K.-J. Koh etal, "0.13-μm CMOS phase shifters for X-, Ku-, and K-Band Phased Arrays", IEEE JSSC, Nov. 2007

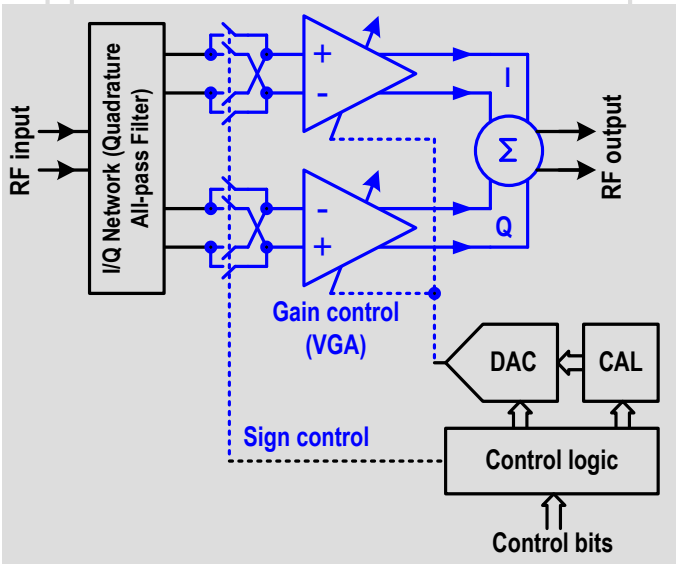
Vector-Summing Phase Shifter (Quadrature all-pass filters)



$$A_{v,out} \propto \sqrt{I_I + I_Q}$$

$$\angle\phi_{Out} = tan^{-1}\sqrt{\frac{I_Q}{I_I}}$$

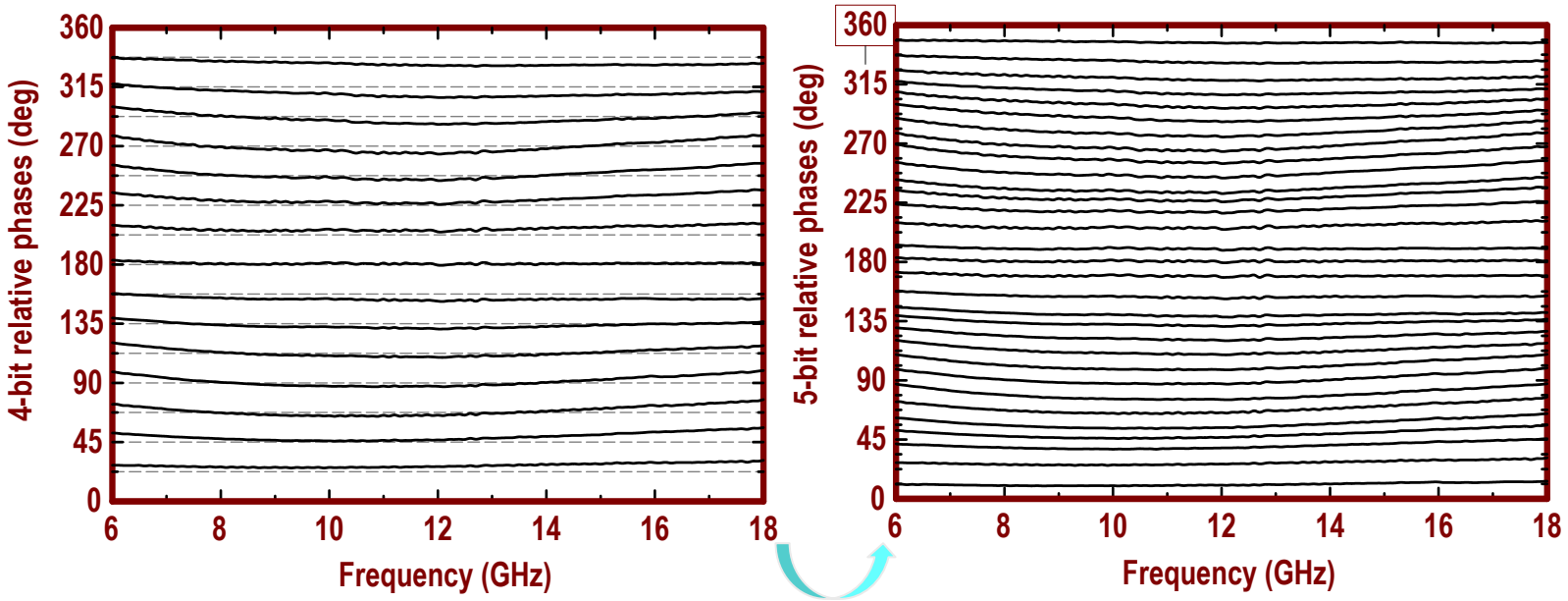
- 2 Gilbert-cells ➡ I/Q VGA
- Active inductor ➡ save area
- Keep I_Q+I_I=constant ➡ constant gain versus phase change



SIM. RESULTS @ X-BAND

- 0.18-µm CMOS
- Gain = 0 dB @12 GHz
- IIP3 = 15 dBm @12 GHz
- I_I+I_Q=2.5 mA, Vdd=3.3 V

ACTIVE PHASE SHIFTER – 4/5-BIT RELATIVE PHASES



After DAC calibration

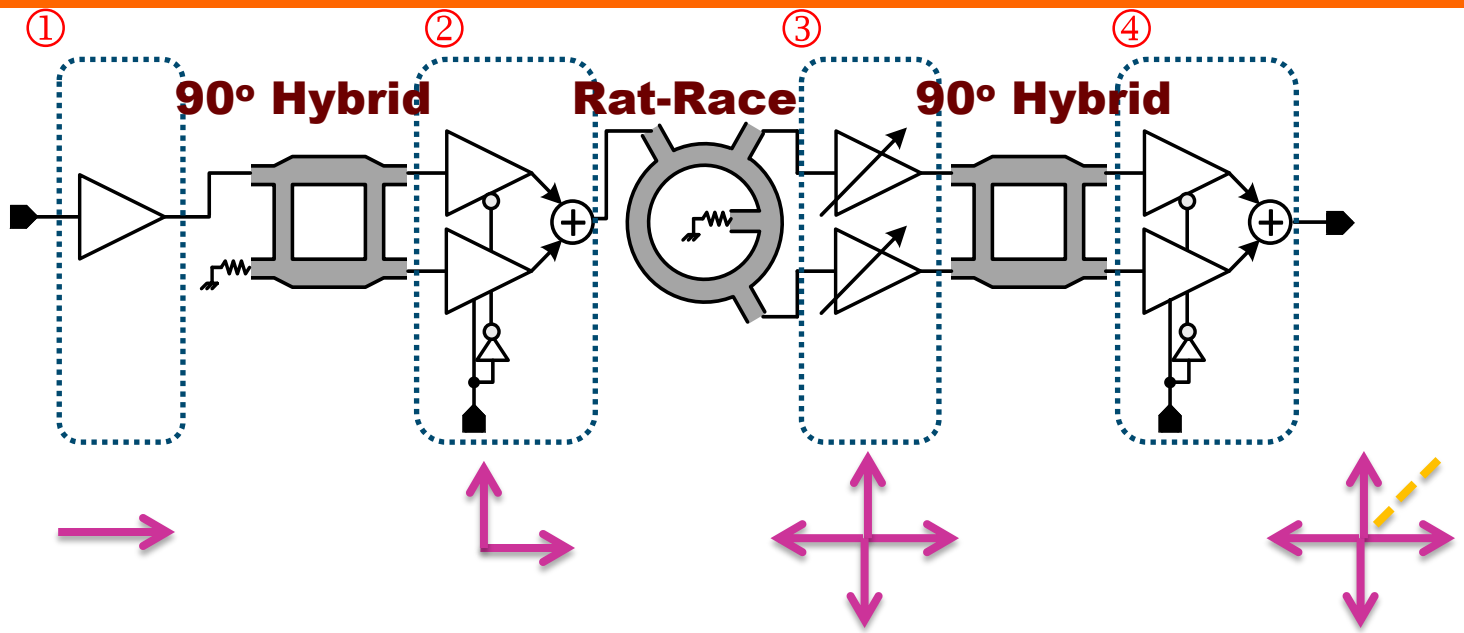
(Relative phases referenced to 0°-bit phase, RMS phase error < 5.6° @6-18 GHz)

NOTE

- Phase interpolation is an independent process of frequency
- Operational BW is limited by the I/Q network, i.e. the accuracy of I/Q network
- Phase can be easily calibrated using a high resolution DAC (not easy in passive design)

First realization of integrated 5-bit active phase shifter in silicon achieving 6-18 GHz coverage (3:1 BW)

Vector-Summing Phase Shifter (90◦ hybrid coupler)



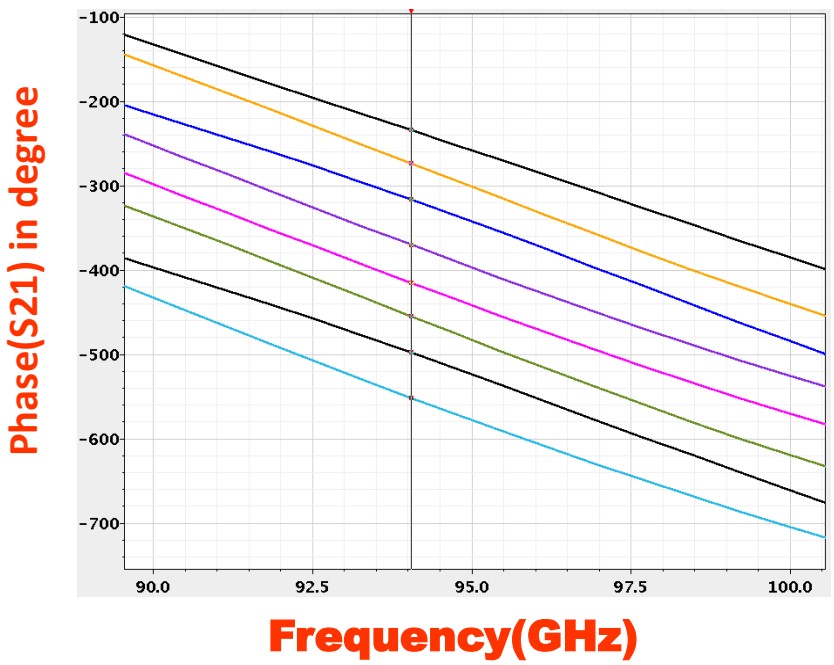
①: **LNA** Compensates for the loss of phase shifter.

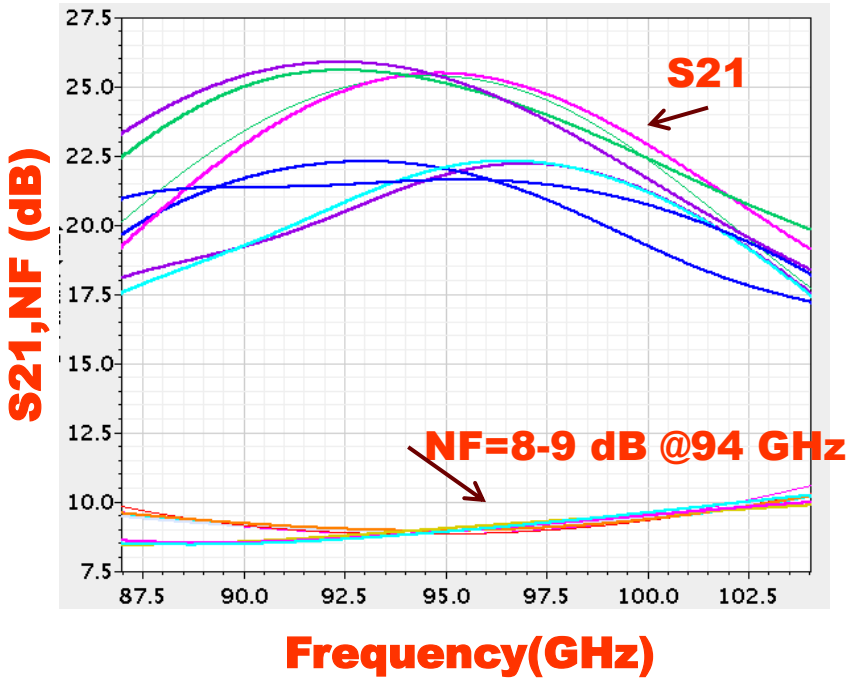
②&④: **Switch Amplifier (functioning as an active switch)**

These switches are used to select the appropriate quadrant that the two orthogonally-phased inputs create the desired phase.

③: **VGA** varies the amplitudes of two orthogonally-phased input signals to get the desired phase within the selected quadrant.

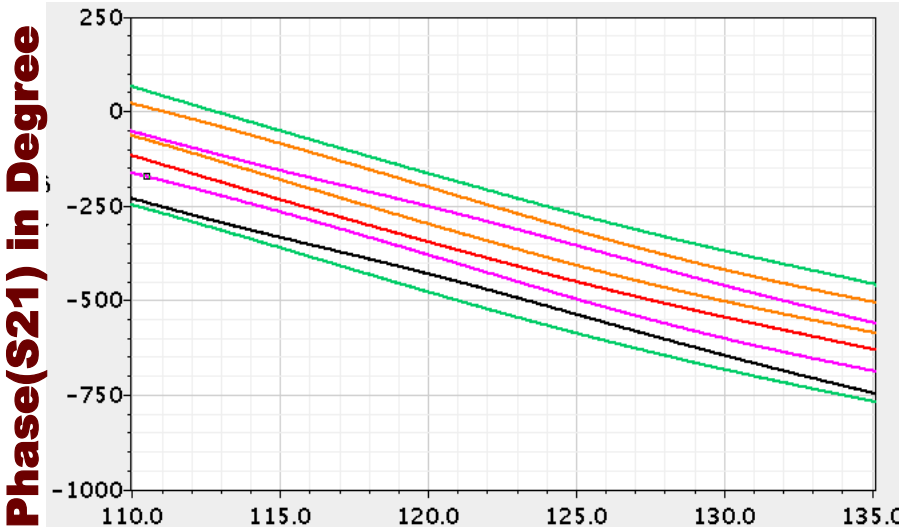
1- 94 GHz Phased Array Front End

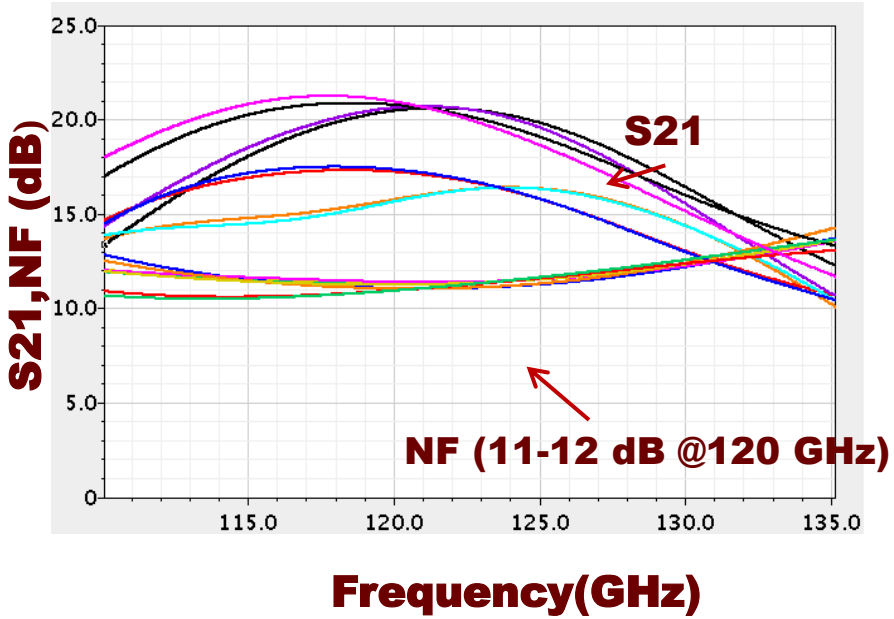




- Continuous 360° phase control (shown only 3-bit control here)
- S21: 21-25 dB @94 GHz
- These gain variation can be offset by adjusting VGA (not shown here)
- NF: 8-9 dB @94 GHz

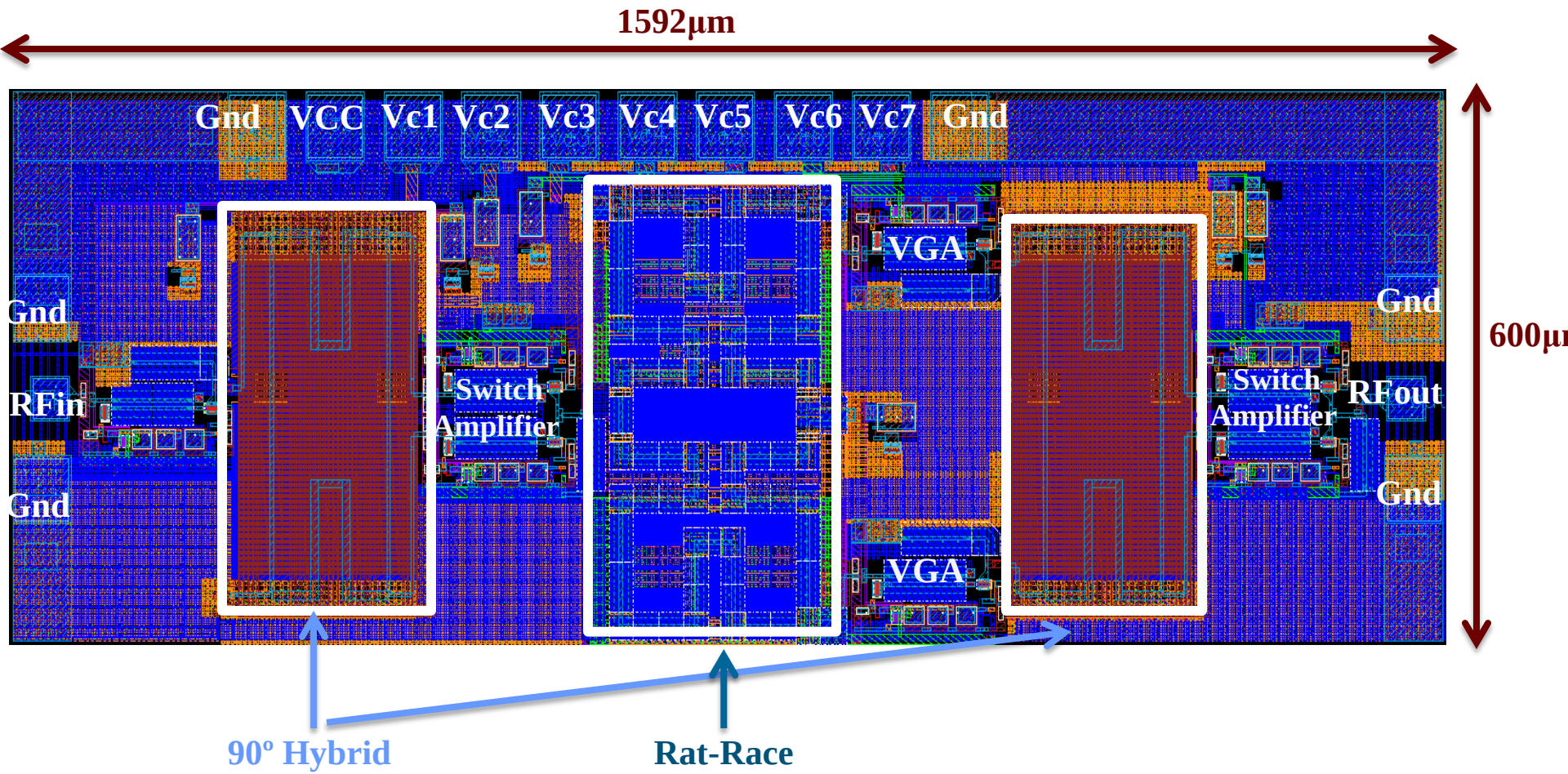
2-120 GHz Phased Array Front End





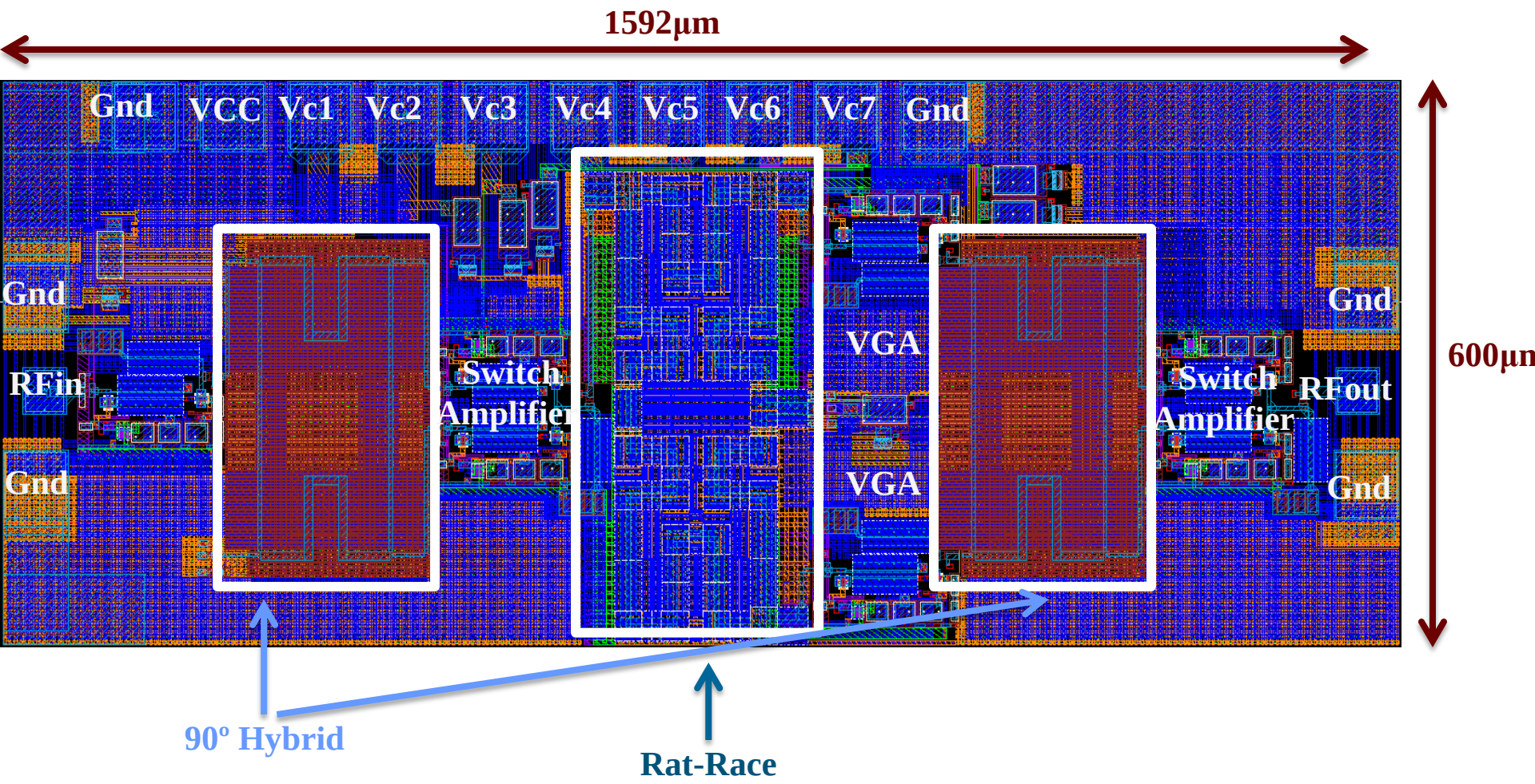
- Continuous 360° phase control (shown only 3-bit control here)
- S21: 16-20 dB @120 GHz
- These gain variation can be offset by adjusting VGA (not shown here)
- NF: 11-12 dB @120GHz

94 GHz Phased Array Front End: Layout



- Supply 2.5 V , Total current 44mA

2. 120 GHz Phased Array Front End: Layout



- Supply 2.5V ,Total Current 37mA

Conclusion

- Passive phase shifters have good linearity performance, but the main challenge is the loss associated with the passive elements and switches.

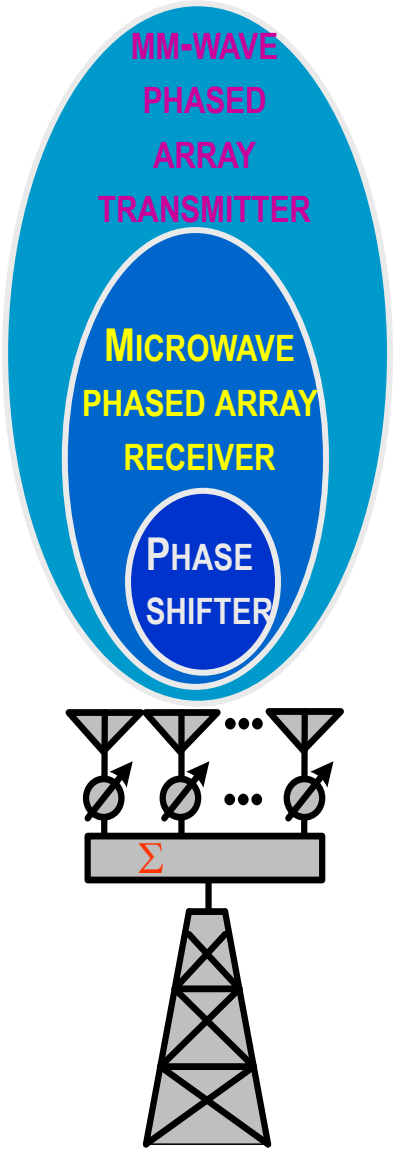
- Their physical sizes make them impractical for integration with multiple arrays in a commercial IC process, especially below K band frequencies (< 30 GHz).

- Active phase shifters can achieve a high integration level with decent gain and accuracy along with a fine digital phase control under a constrained power budget.

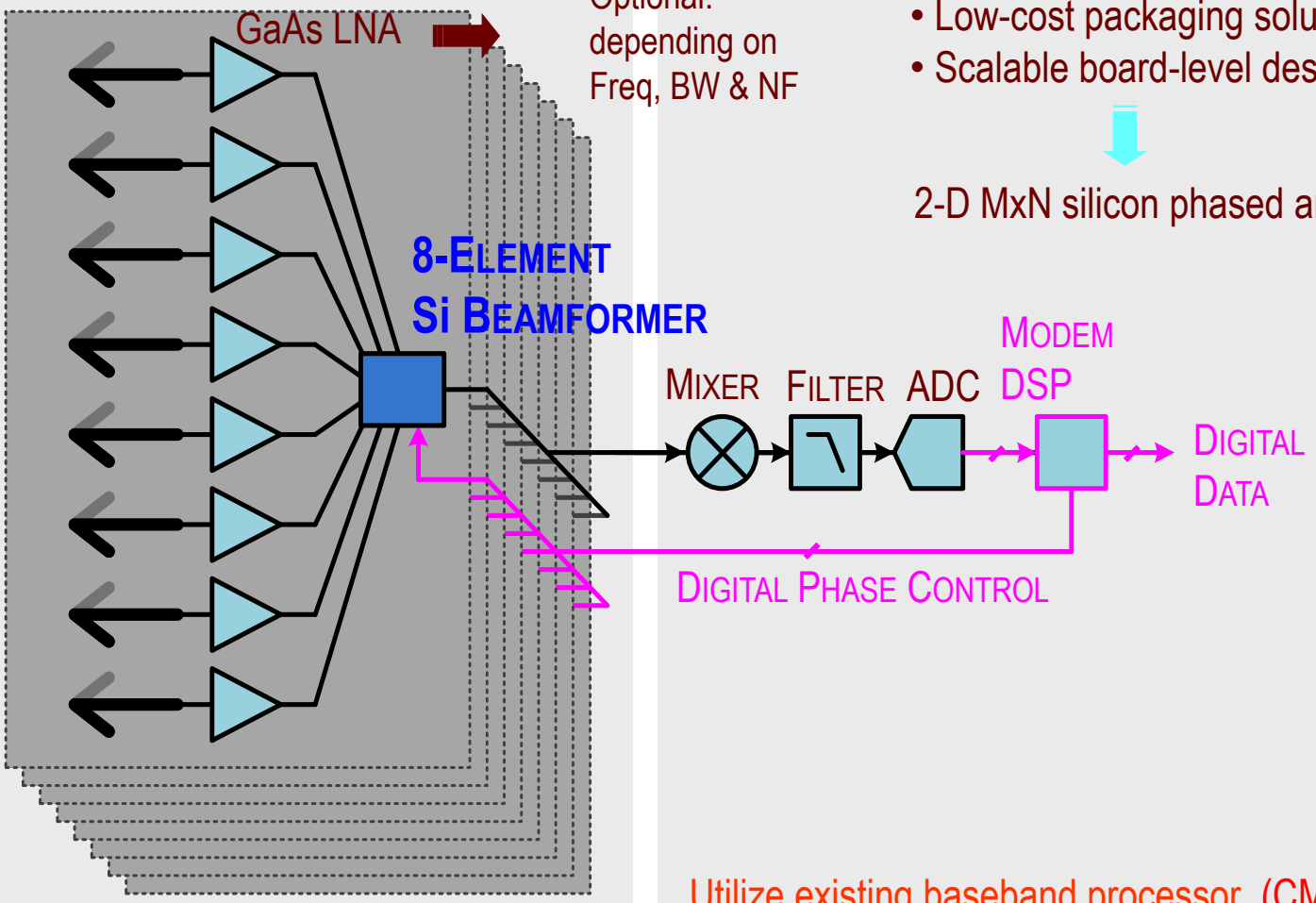
- The most challenging part of realizing active phase shifters is the quadrature generation block which can be implemented by quadrature all-pass filters (at lower frequencies) and a 90◦ hybrid coupler (at higher frequencies).

PHASE ARRAY IC DESIGN

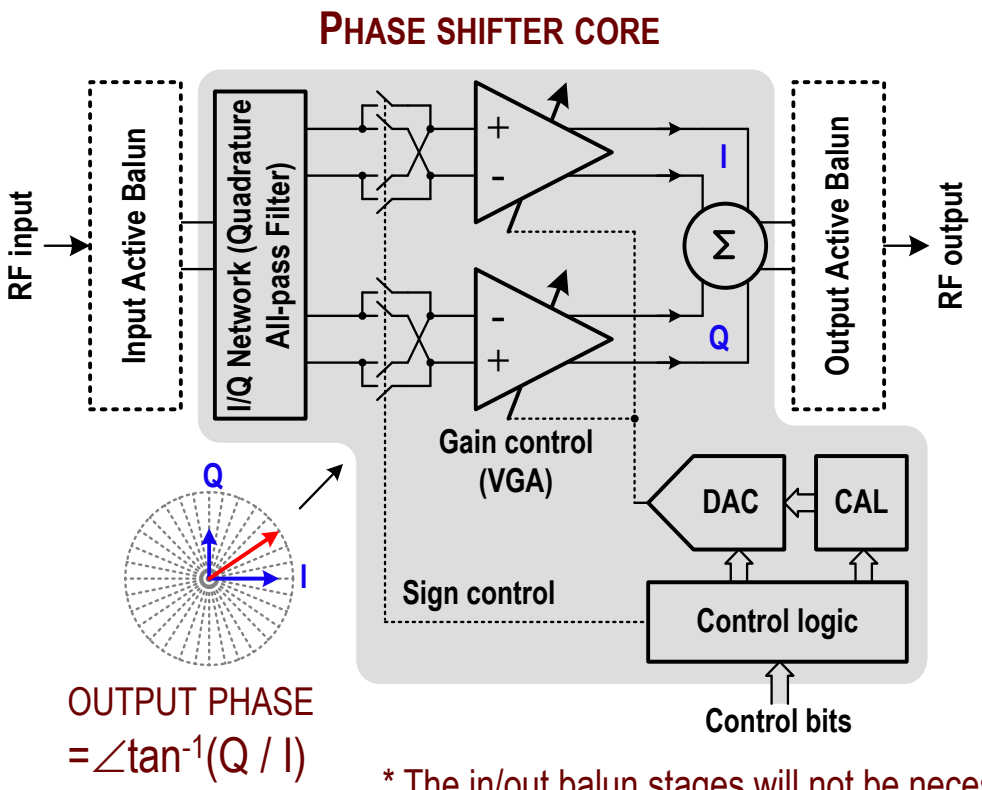
- PHASED ARRAY RECEIVER @ 12 GHZ
  - IC-design, chip & board level verification
- PHASED ARRAY TRANSMITTER @ 44 GHZ
  - IC-design & chip level verification
- CONCLUSIONS



8-ELEMENT PHASED-ARRAY (12 GHz, SCALABLE ARRAY)



8 ELEMENT SI BEAMFORMER: PHASE SHIFTER



OPERATION

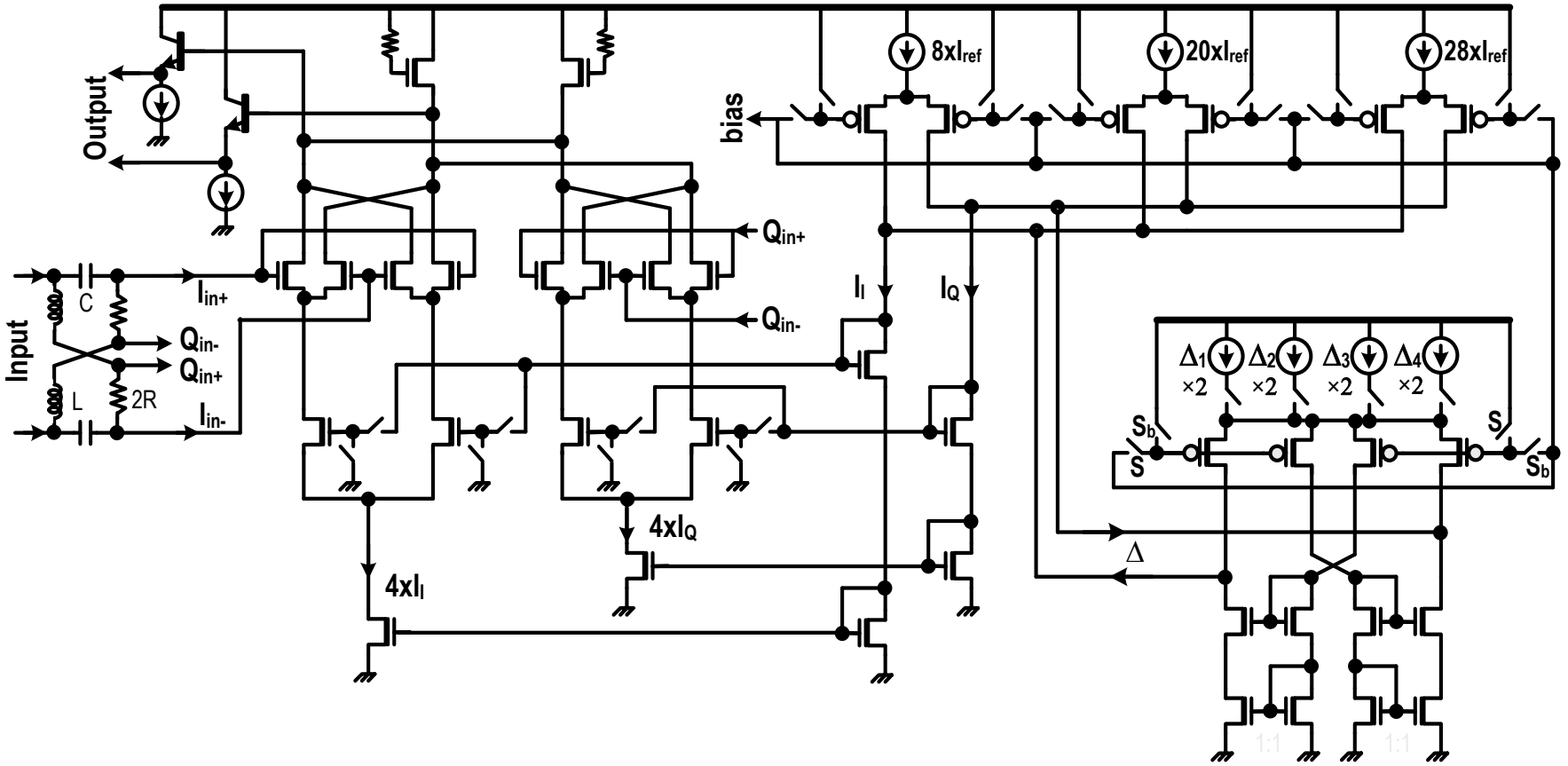
- Balun provides differential signal
- I/Q network splits signal into I & Q vector signals
- VGA controls gain for I & Q path
- I/Q signals are added in V-domain (phase interpolation)
- DAC provides 4-bit phase control
- CAL calibrates DAC to get 5-bit phase resolution

* The in/out balun stages will not be necessary for fully integrated differential systems

Mostly active circuits ➡ **Small chip area & Gain**

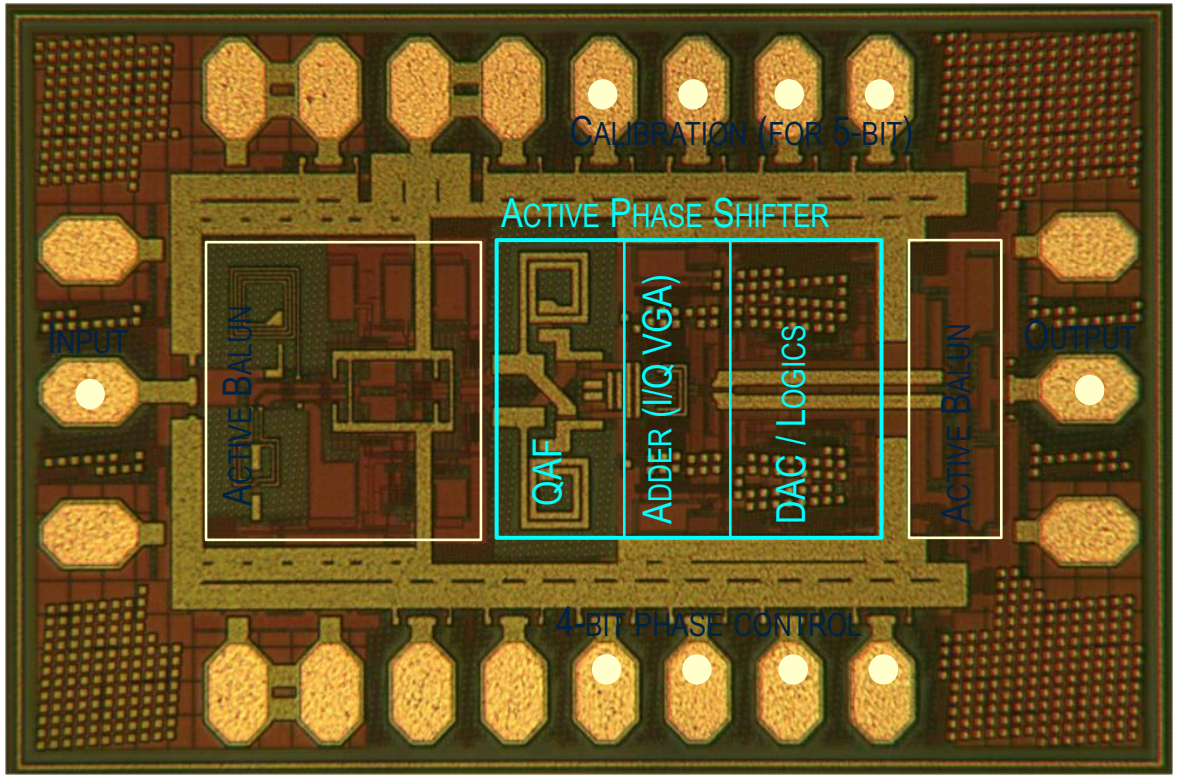
DAC control ➡ **Fine accurate phase control & calibration**

ACTIVE PHASE SHIFTER - SCHEMATIC

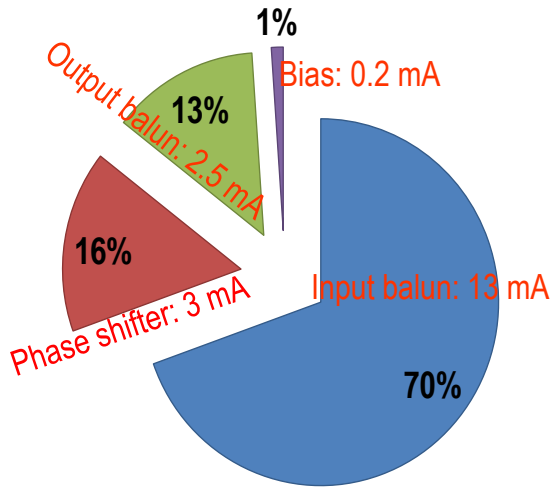


Ref: K.-J. Koh etal, "0.13-μm CMOS phase shifters for X-, Ku-, and K-Band Phased Arrays", IEEE JSSC, Nov. 2007

ACTIVE PHASE SHIFTER – CHIP PHOTO



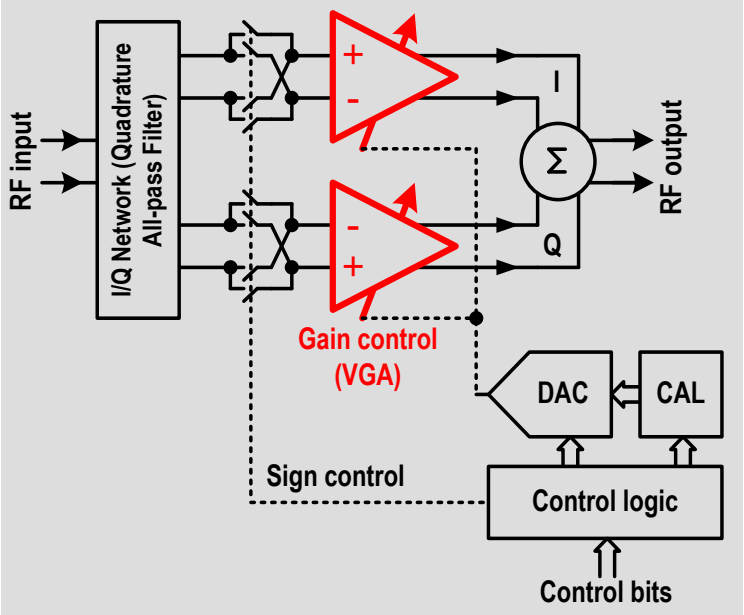
- 0.18-μm SiGe BiCMOS process (Phase shifter: 0.18-μm CMOS)
- Chip size: 1.2 x 0.7 mm^2 (Phase shifter: 0.4 x 0.3 mm^2)
- Total current: 18.7 mA (V_{DD}=3.3 V)

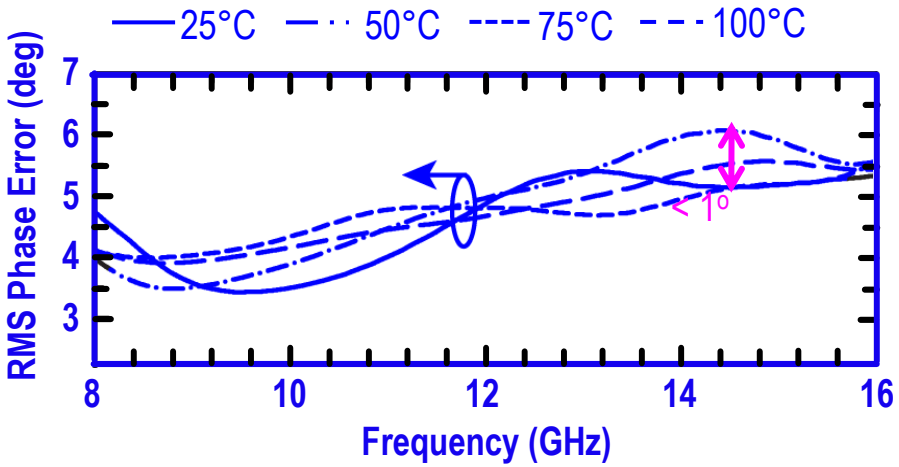


- All pads are ESD protected (HBM rating: 3kV, 2A)

- Supported by "DARPA SMART project" (2006-2008)
- Presented at the DARPA meeting & MTT-s 2010
- Lockheed Martin bought the designs (schematic & layout), 2009

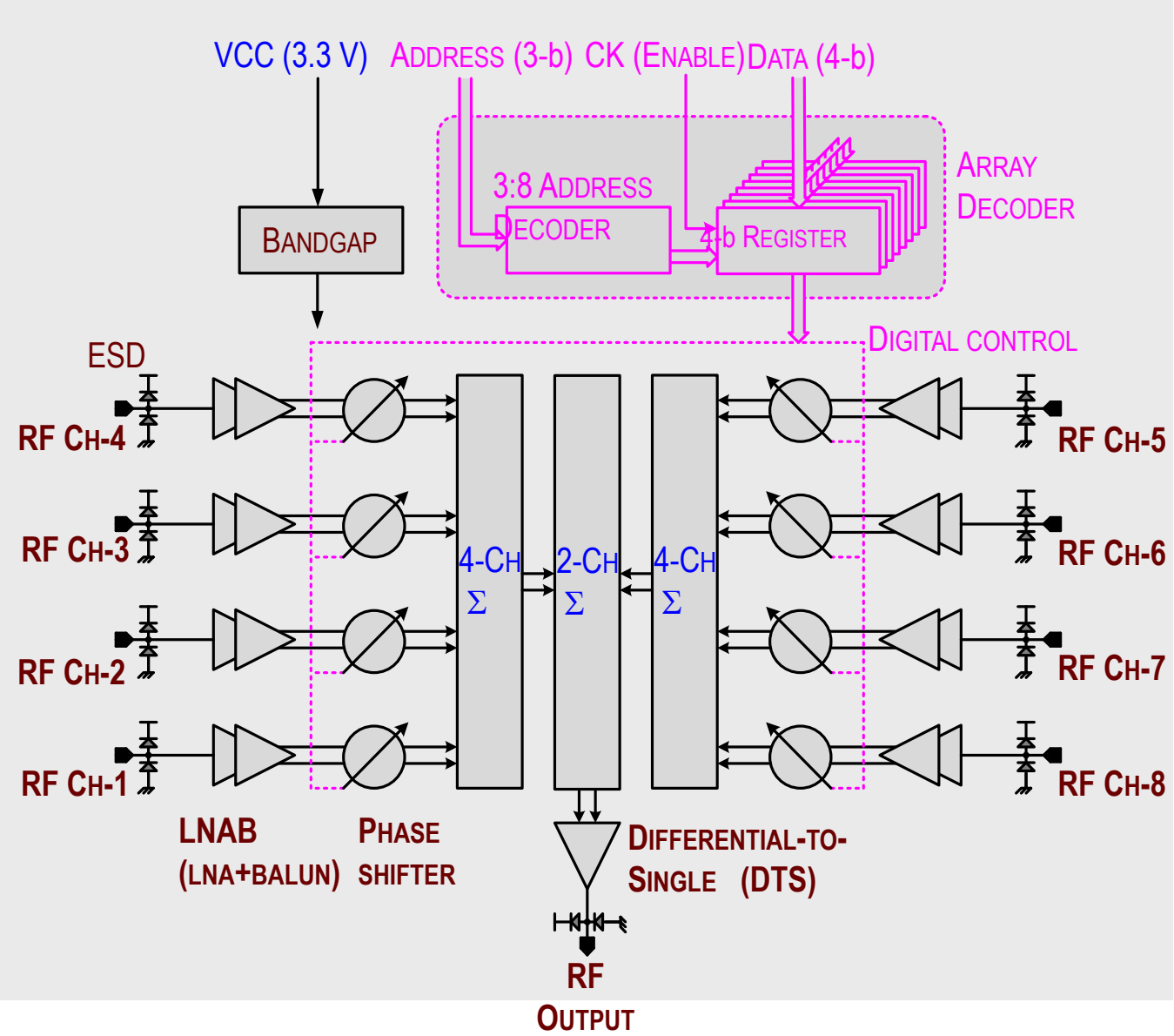
Active phase shifter – temperature measurements





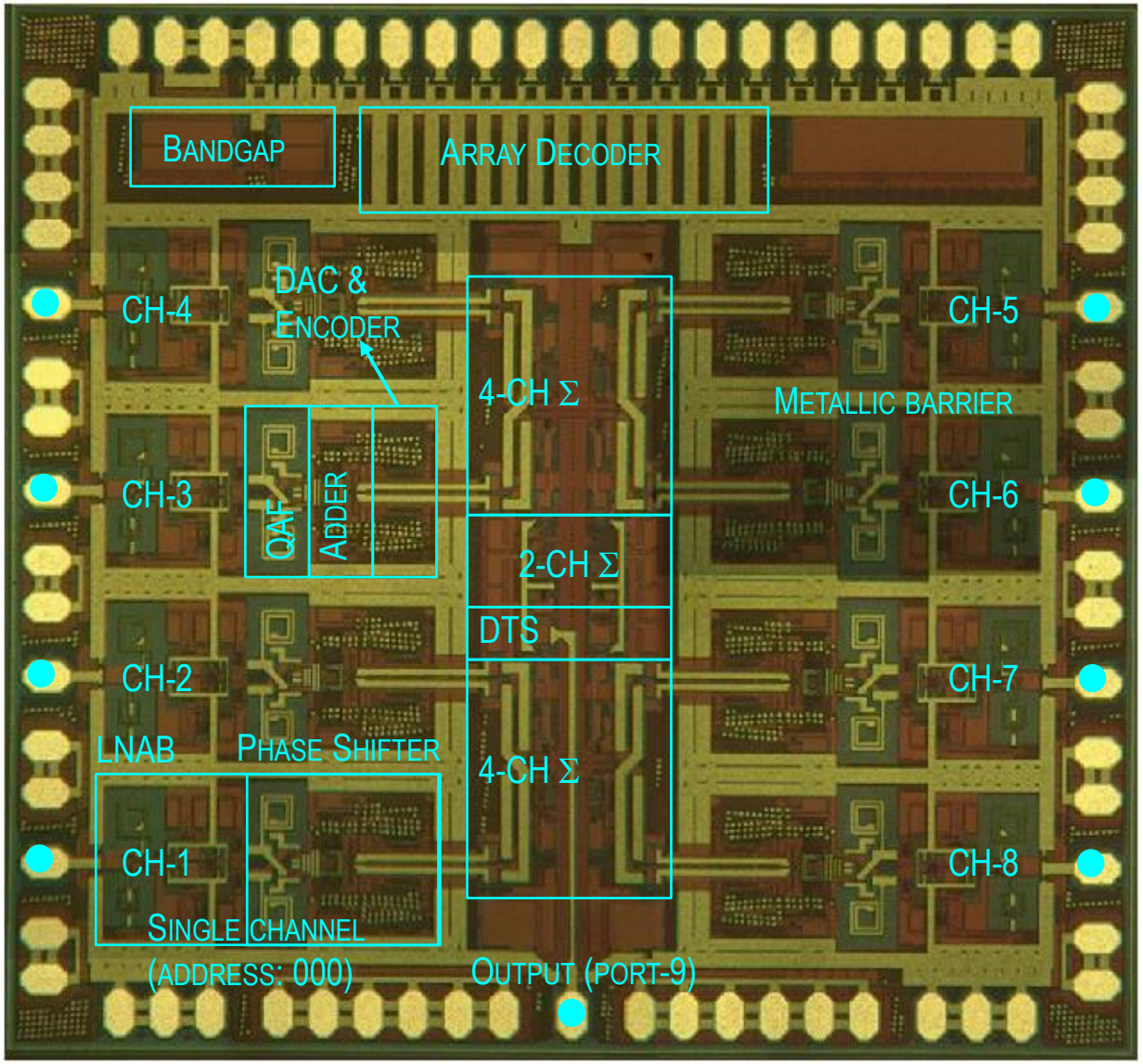
- I & Q paths are biased with a reference PTAT circuit
- Output phase depends on I:Q gain ratio (not absolute gain)
- I & Q amplifiers track each other vs. PVT, resulting in low sensitivity to PVT
- RMS phase error < 6° @ 25°-100° C

8-Element phased-array (12 GHz, architecture)

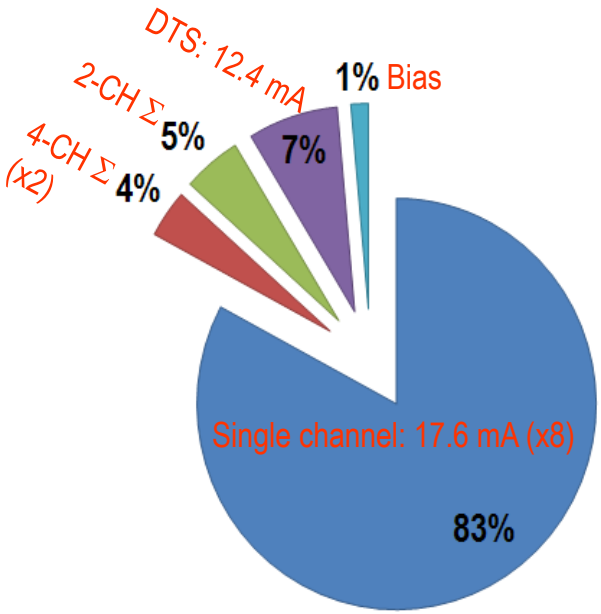


- Integrate 8-CHs in SiGe
- Integrate "RF + Digital"
- 4-bit active phase shifter
- 2-step signal combining (active adders)
- ESD protection (3kV, 2A)

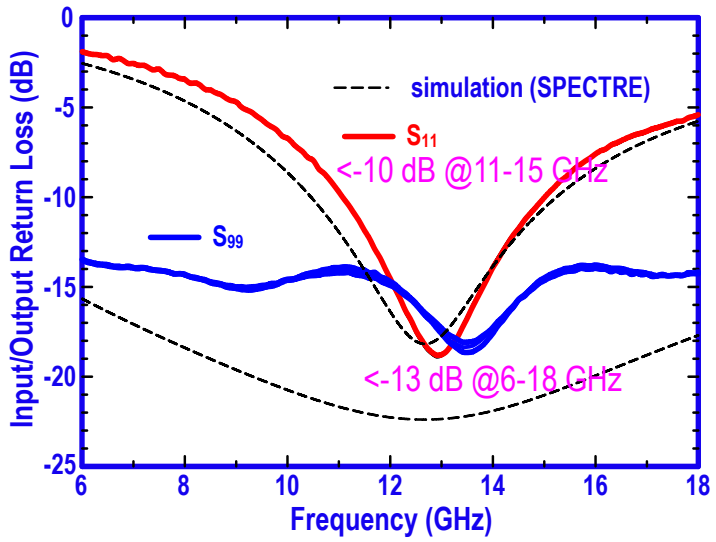
8-Element phased-array (12 GHz, chip photo)

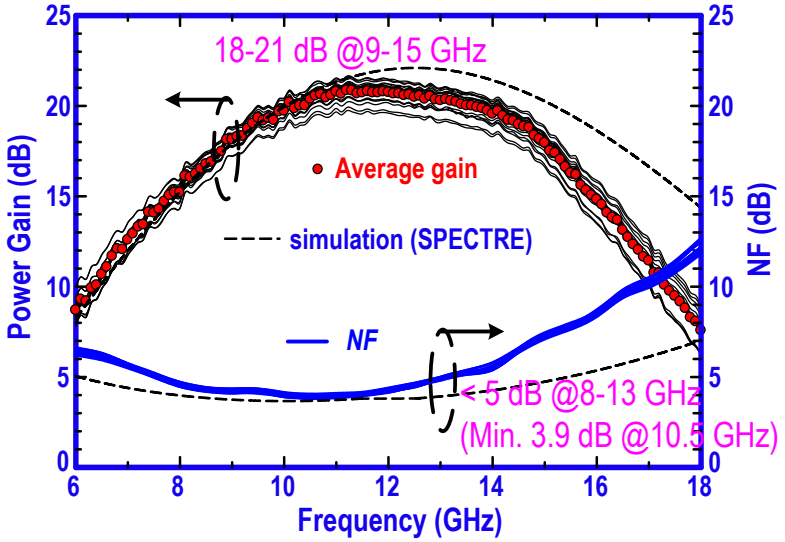


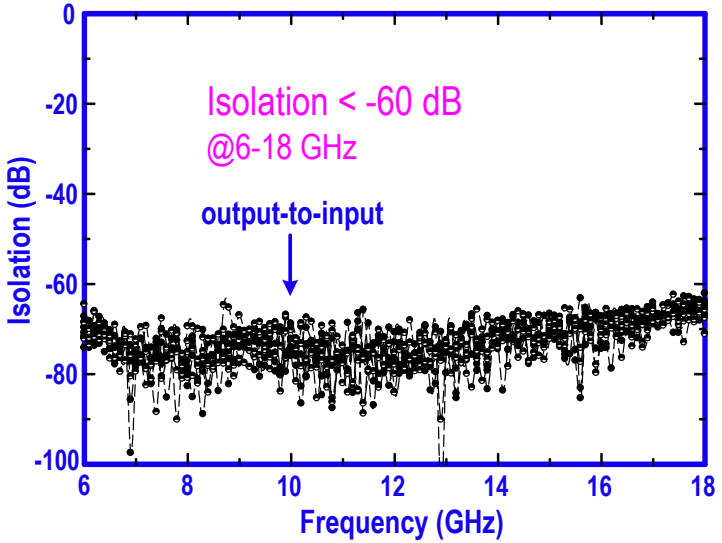
- 0.18-μm SiGe BiCMOS (Jazz SiGe120, 1P6M, f_T=150 GHz)
- Area = 2.2 x 2.4 mm^2
- Near perfect corporate-feed layout (E-length btw any input to output is identical)
- Metallic barrier: max CH-CH isolation
- V_{CC}=3.3 V, I_{total}=170 mA (561 mW, Active-Σ < 10%)

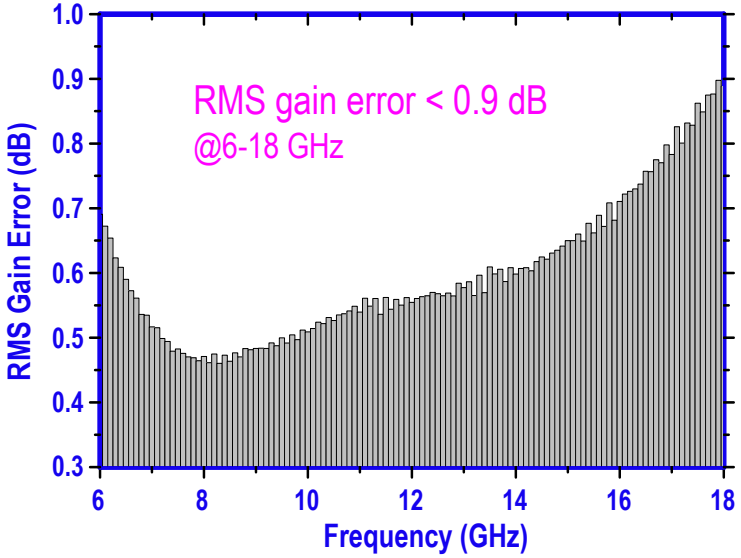


8-ELEMENT PHASED-ARRAY (12 GHZ, GAIN, NF, MATCHING)

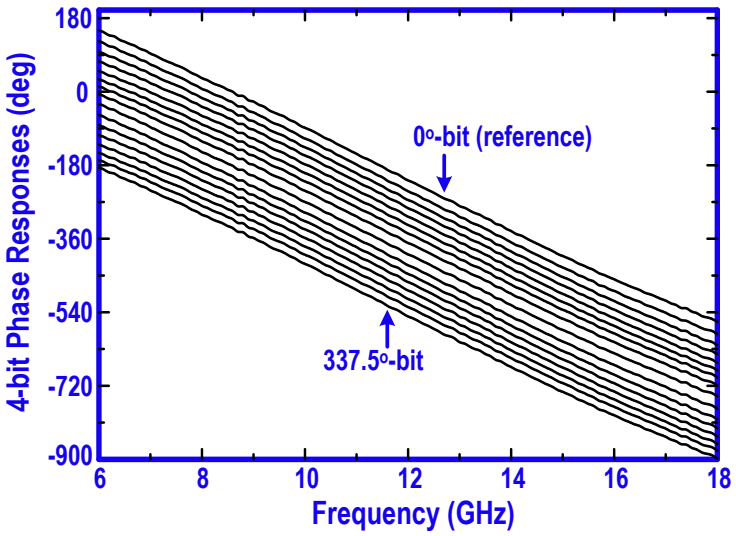


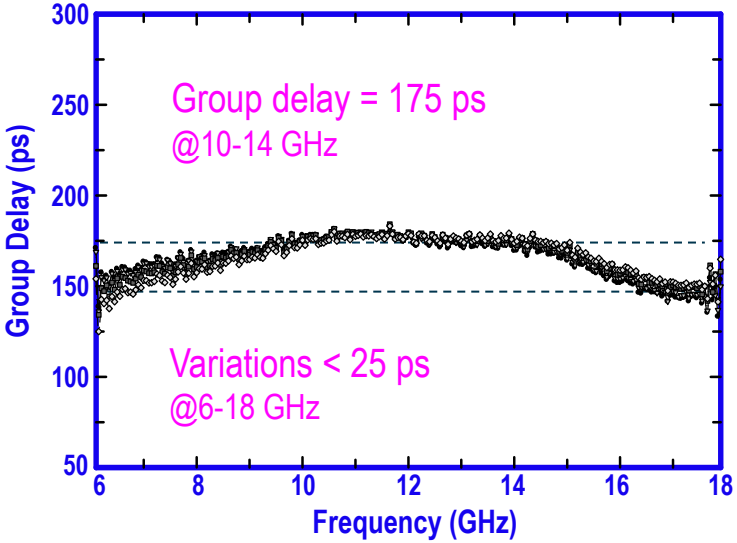


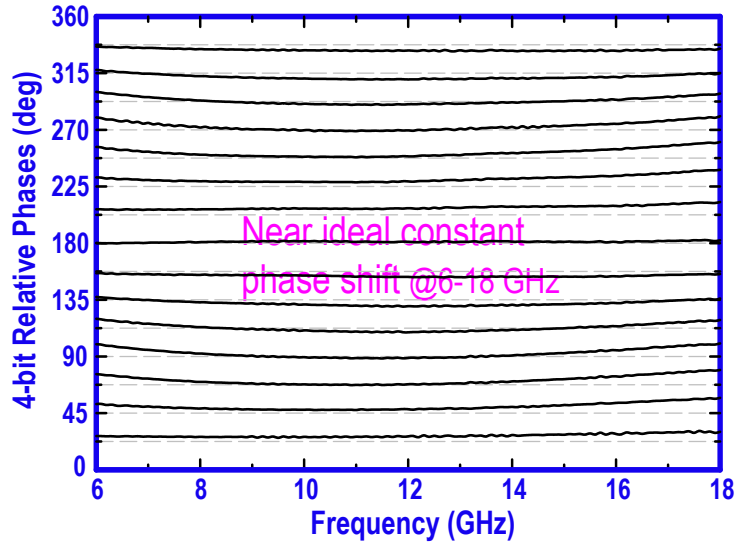


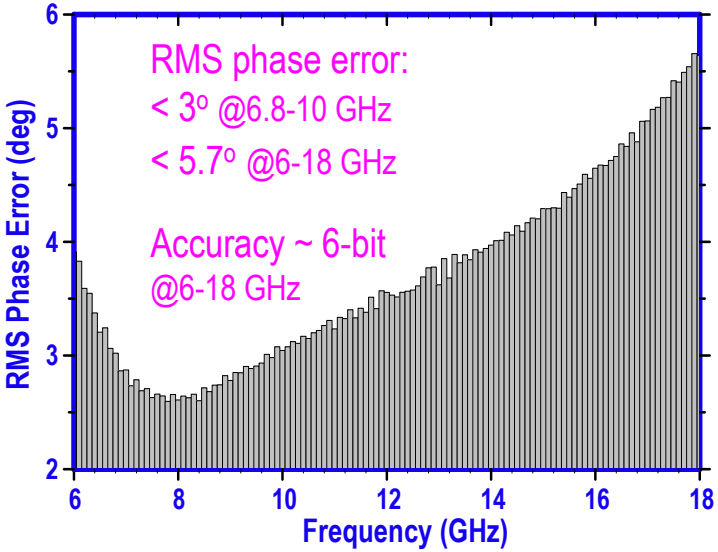


8-ELEMENT PHASED-ARRAY (12 GHZ, PHASE, GROUP DELAY)

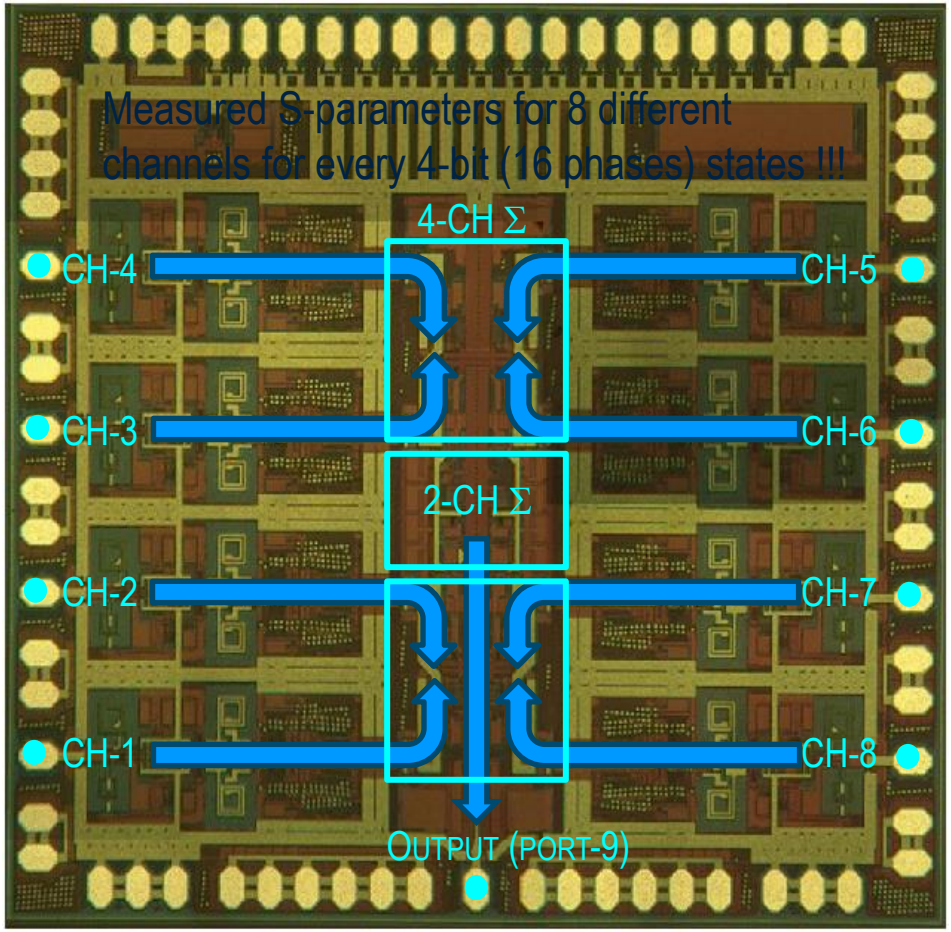


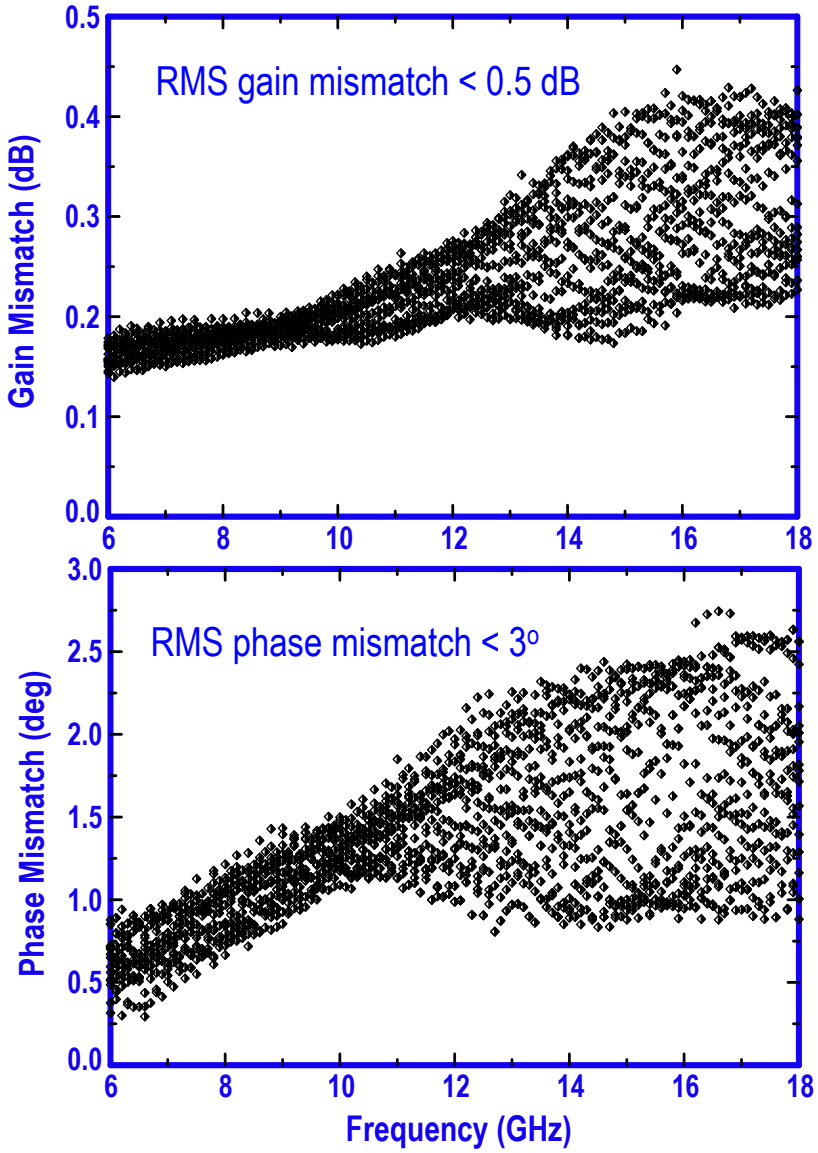






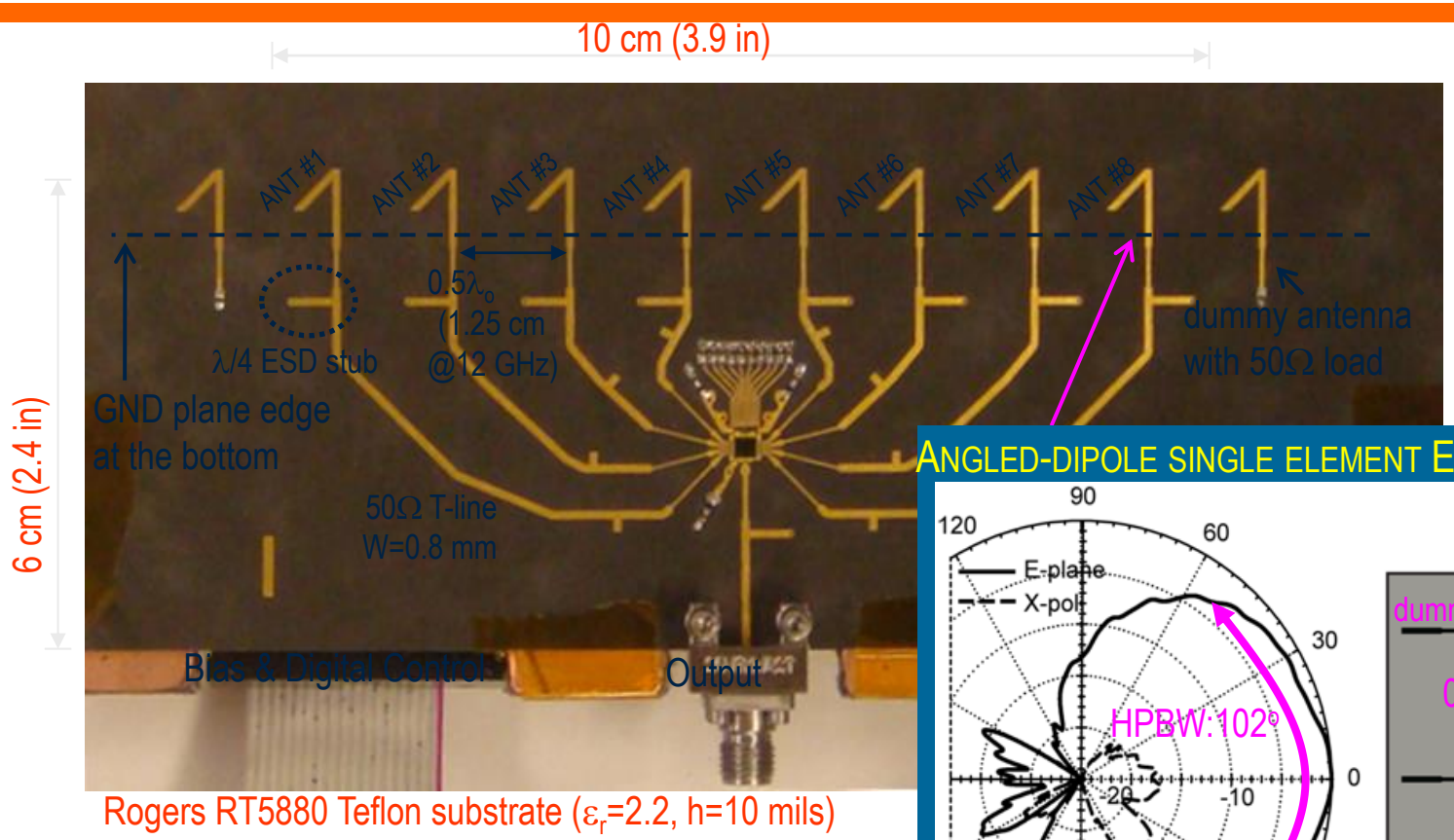
8-Element phased-array (12 GHz, ch-to-ch variation)

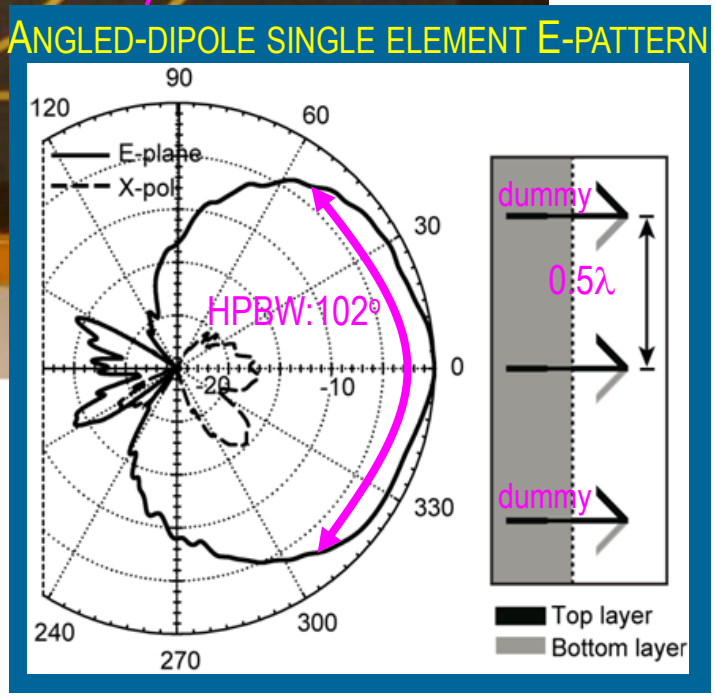




- Comparison of 128 S-Parameters
  = 8 (channels) x 16 (4-bit phases)
- Excellent matching between array elements
  → Major benefit in the on-chip integration

8-ELEMENT PHASED-ARRAY (12 GHZ, CHIP-ON-BOARD, ANGLED-DIPOLE)





ANGLED-DIPOLE ANTENNA:

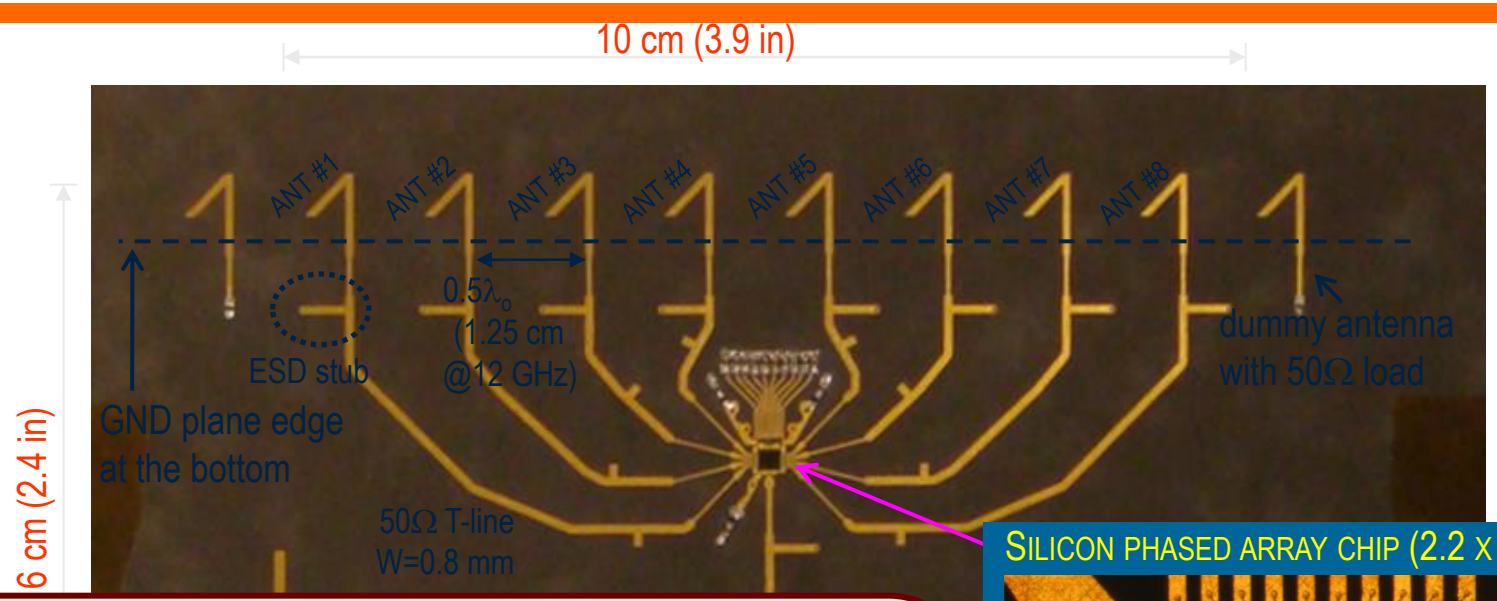
Wider beam width, Lower mutual coupling , Wideband S11

HPBW: 102°, S11<-10 dB @10.5-14 GHz, S21<-17 dB

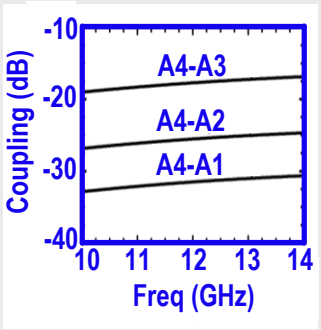
Scan angle: +/- 60° w/ 4dB drop in element factor

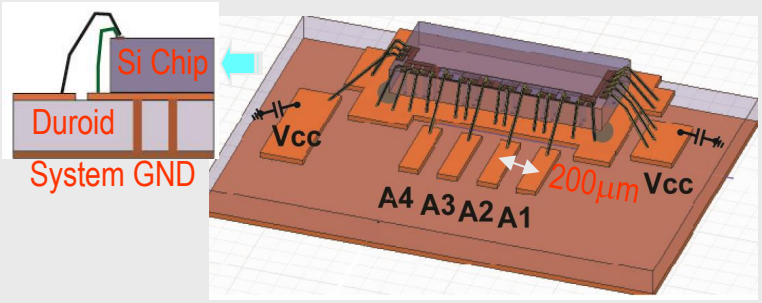
Ref: Y. A. Atesal, B. Cetinoneri, K.-J. Koh, G. M. Rebeiz, "X/Ku-Band 8-Element Phased Arrays Based on Single Silicon Chips", 2010 IMS, May 2010

8-ELEMENT PHASED-ARRAY (12 GHZ, CHIP-ON-BOARD, CHIP MOUNTING)



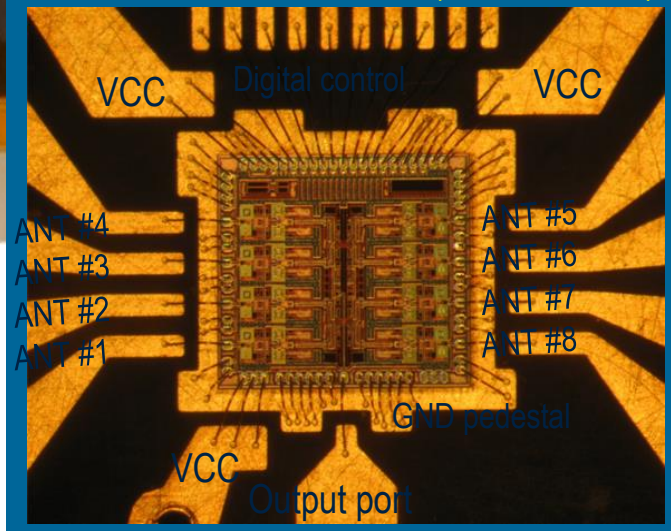
BONDWIRE & COUPLING SIMULATION WITH HFSS





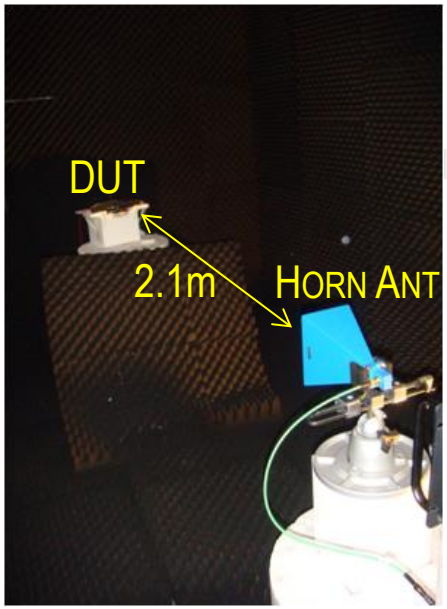
Worst-case coupling < -17 dB, bondwire inductance: 0.5 nH

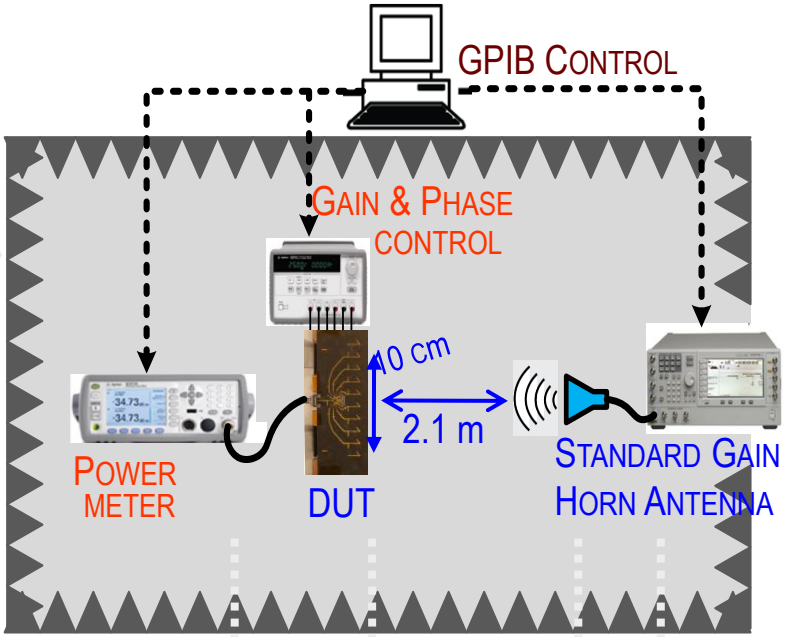
SILICON PHASED ARRAY CHIP (2.2 X 2.4 mm²)



Ref: Y. A. Atesal, B. Cetinoneri, K.-J. Koh, G. M. Rebeiz, "X/Ku-Band 8-Element Phased Arrays Based on Single Silicon Chips", 2010 IMS, May 2010

8-Element phased-array (12 GHz, board measurement setup)





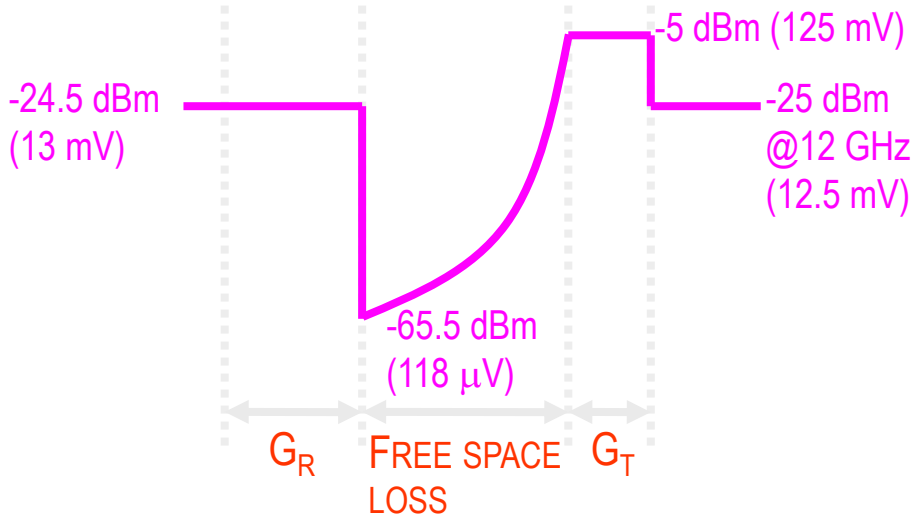
Friis Transmission Equation

$$\frac{P_R}{P_T} = \underbrace{G_T}_{\text{Horn ANT gain}} \times \underbrace{\left(\frac{\lambda}{4\pi \cdot R}\right)^2}_{\text{Free space path loss}} \times \underbrace{G_R}_{\text{Phased array gain}}$$

= 20 dB

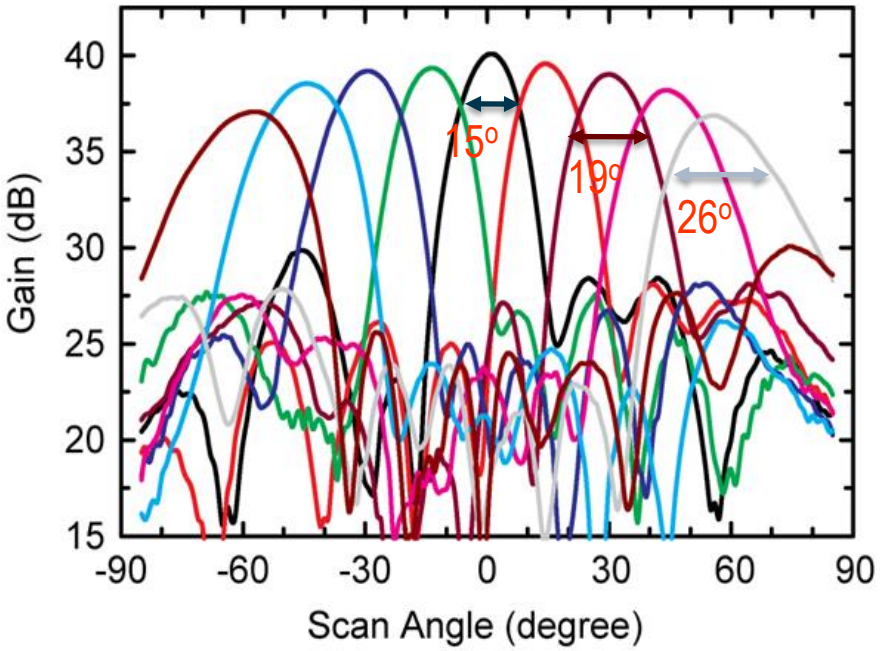
= -60.5 dB
R: 2.1 m
λ: 2.5 cm
@12 GHz

= 41 dB
Channel gain (20 dB)
Array factor (18 dB)
Antenna gain (3 dB)

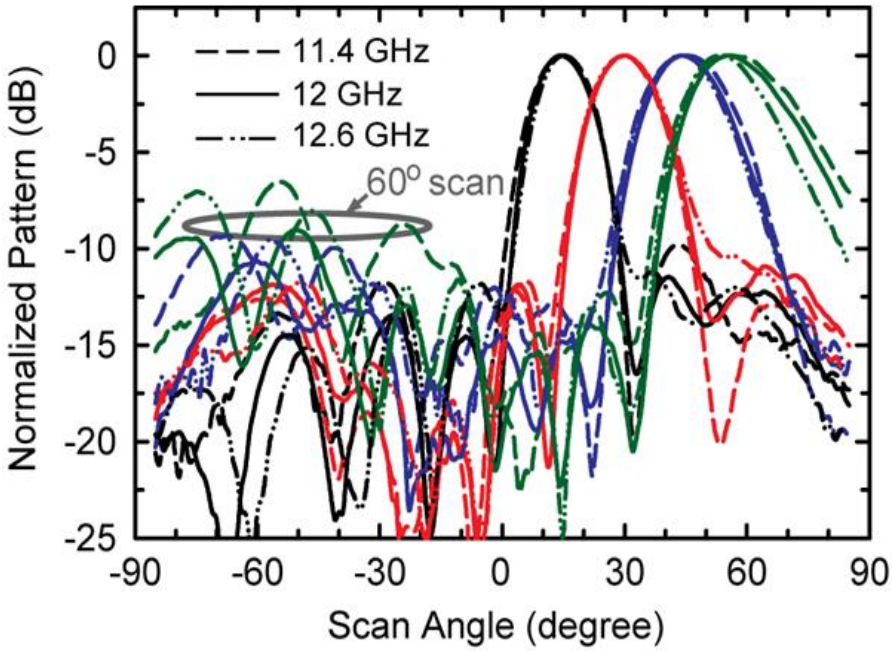


8-Element phased-array Rx (12 GHz, board measurement)

Measured pattern @12 GHz



Measured pattern @11.4-12.6 GHz

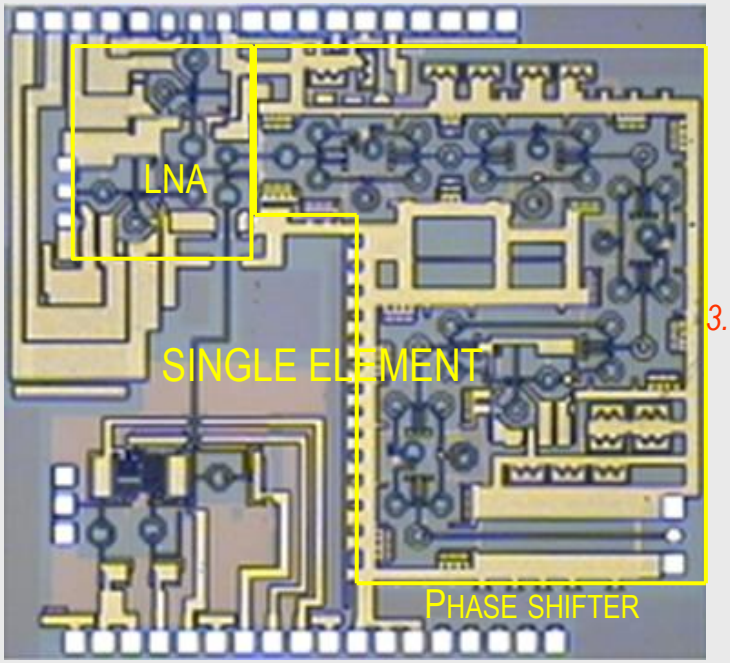


- Scanned from -60° to 60°
- Element factor causes 3-4 dB drop at 60°
- HPBW: 15° @0°-scan, 19° @30°-scan, 26° @60°-scan
- Excellent agreement with simulations

- No-true-time delay on each element
- Slight beam walk @ 60°- scan angle
- Instantaneous BW limited to 11.4-12.6 GHz (Δ=1.2 GHz, 10%)

First system-level (w/ antenna) demo of an X-band array based on a single silicon chip !

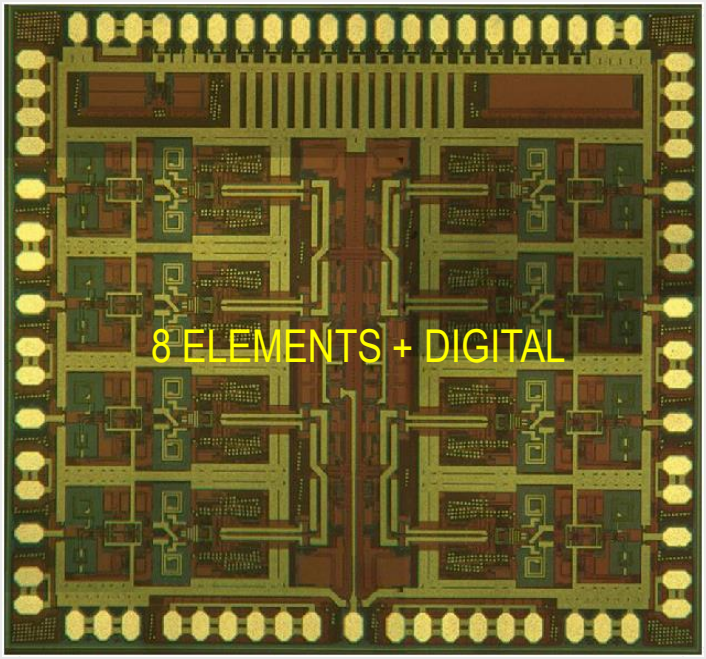
AREA COMPARISON: SINGLE VS 8-ARRAY



3.5 mm

3.8 mm

Ref: Comeau etal (Georgia Tech), "A SiGe Receiver for X-Band T/R Radar Modules", IEEE JSSC, Sept. 2008



2.4 mm

2.2 mm

Ref: K.-J. Koh etal, "An X- and Ku-Band 8-Element Phased-Array Receiver in 0.18-μm SiGe BiCMOS Technology", IEEE JSSC, June 2008

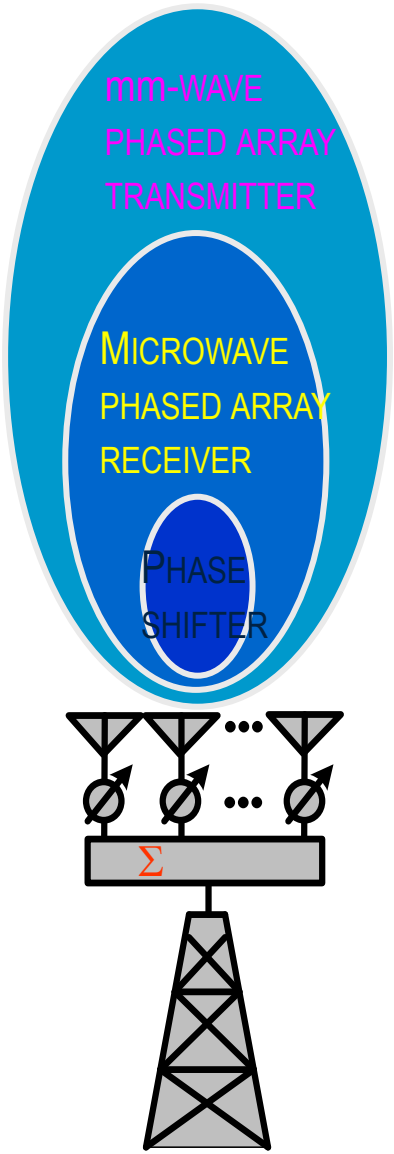
Integration (A=13.3 mm^2):
LNA + Phase shifter + bias c.k.t.
(single element: analog)

COMPARE
(8-element array is 40% size of the passive single-element)

Integration (A=5.3 mm^2):
8 LNAs + 8 Phase shifters + bandgap
(8 elements: analog)
+
Array decoder (digital control)

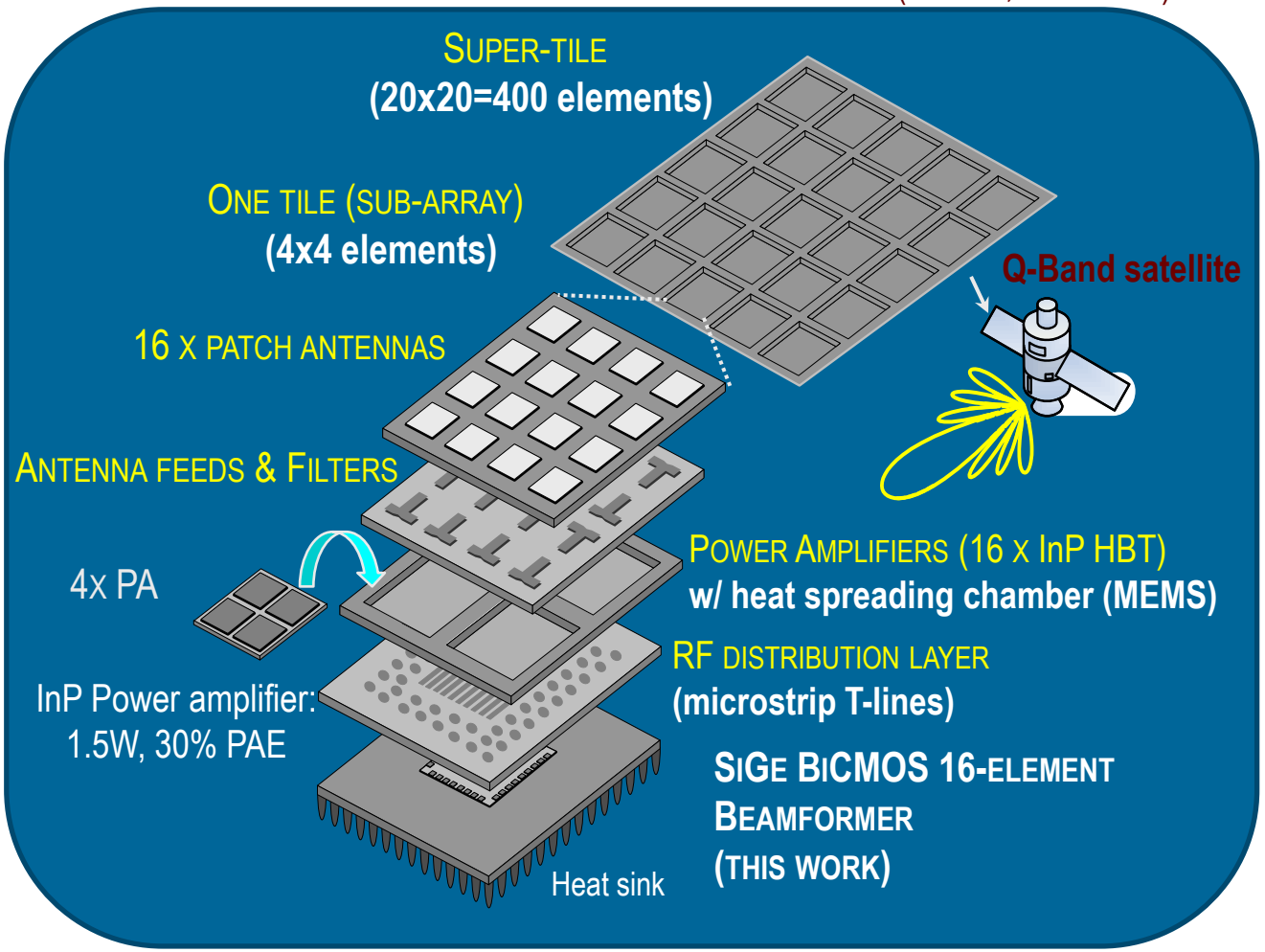
PHASE ARRAY IC DESIGN

- PHASED ARRAY RECEIVER @ 6-18 GHZ
  - IC-design, chip & board level verification
- PHASED ARRAY TRANSMITTER @ 44 GHZ
  - IC-design & chip level verification
- CONCLUSION



16-Element mm-wave phased-array Tx (large array, 3-D integration)

Project: DARPA Scalable Millimeter-wave Array Technology (SMART, 2006-2008)

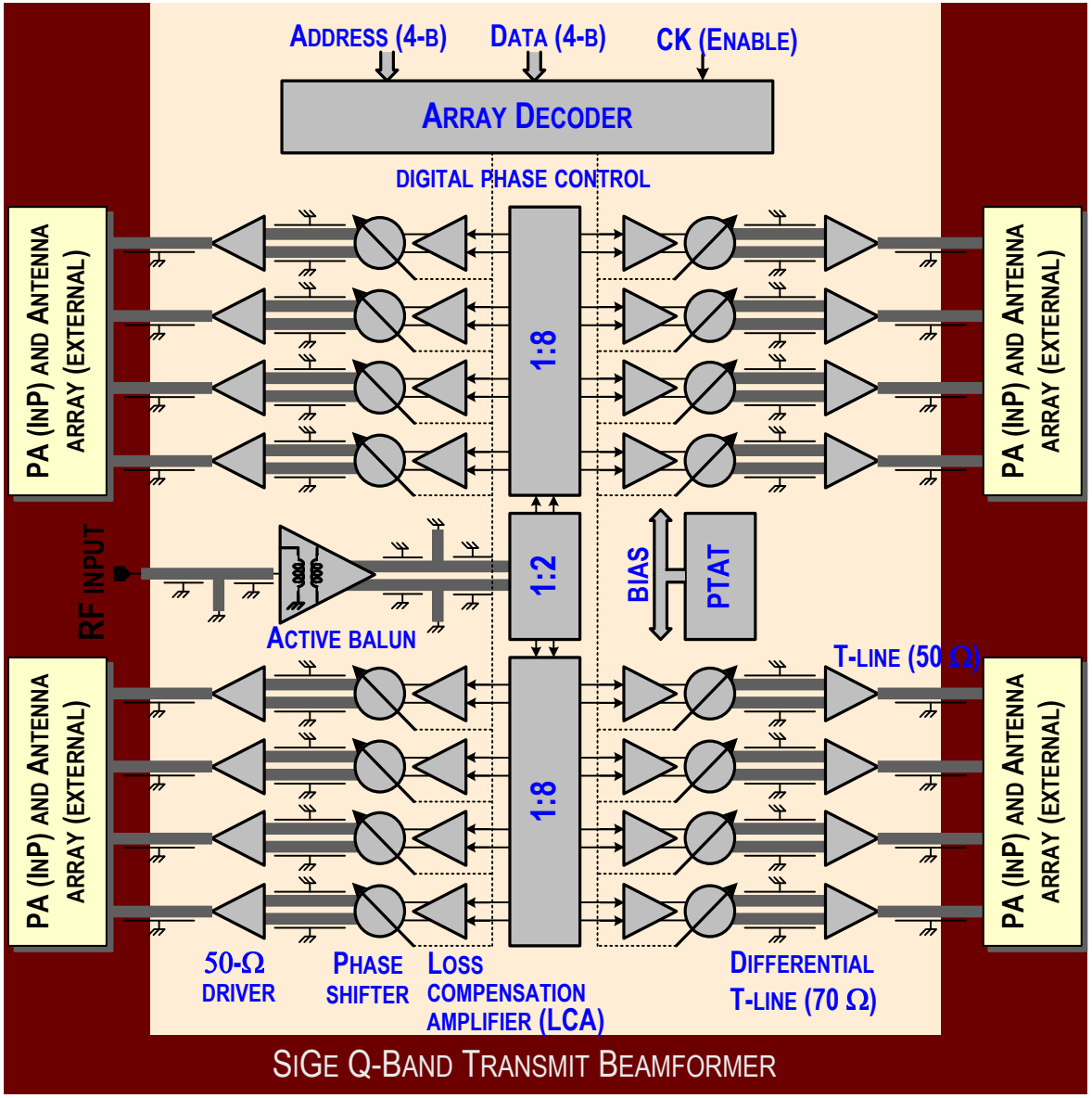


- Q-band satellite comm. (43-45 GHz, $\lambda/2$=3.4 mm)
- Large array: 20x20 elements
- Microstrip antenna size = 3.4x3.4 mm^2
- Integrate 1 sub-array (4x4) in a single package (Area < 3x3 cm^2)

Multi-layered integration in a single package

Tile-based 2-D large array (20x20) construction
One tile (sub-array): 4x4 element, One super-tile: 5x5 tiles

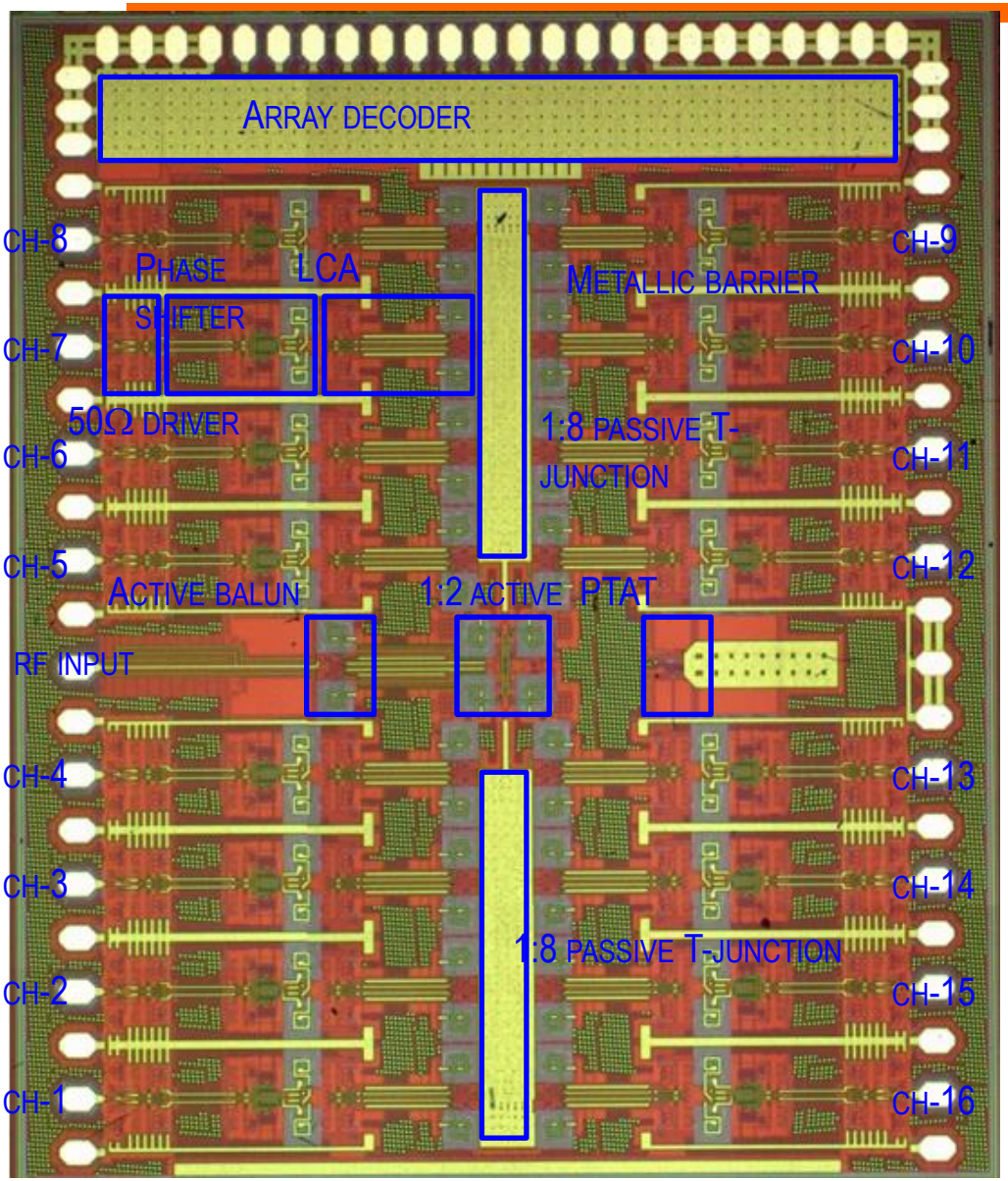
16-Element mm-wave phased-array Tx (44 GHz, architecture)



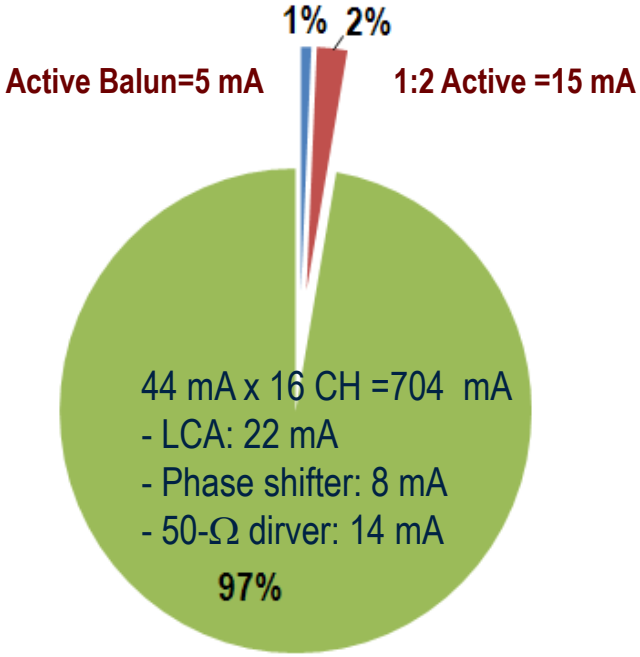
- 44 GHz satellite comm. application
- Integrate 16 elements (4x4)
- Corporate feed architecture
  - Active balun, 1:2 active, 1:8 passive
- Single channel elements
  - LCA: compensate 1:8 division loss
  - 4-bit active phase shifter
  - 50-Ω driver drives external PA
- Array decoder
  - control each channel independently

Ref: K.-J. Koh *etal,* "A Millimeter-wave (40-45 GHz) 16-Element Phased-Array Transmitter in 0.18-μm SiGe BiCMOS Technology", IEEE JSSC, May 2009

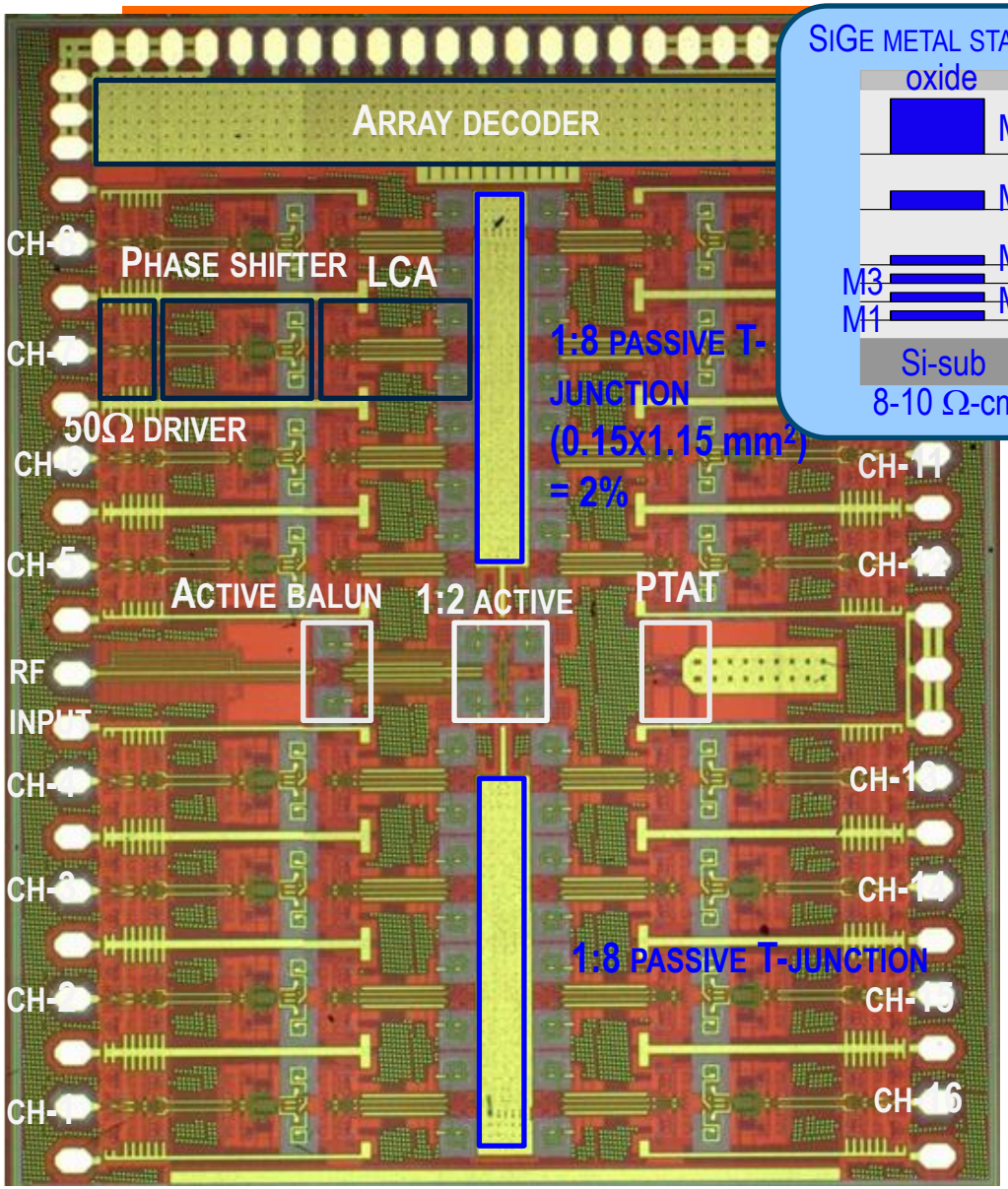
16-Element mm-wave phased-array Tx (44 GHz, chip photo)



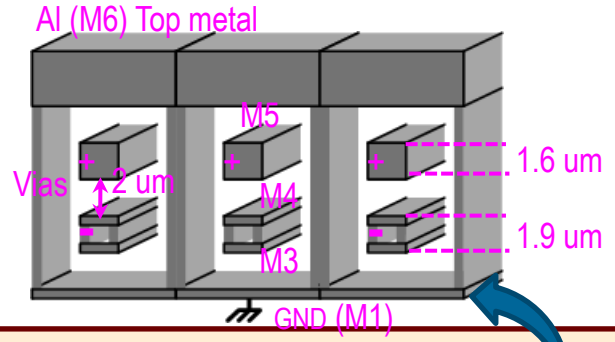
- 0.18-μm SiGe BiCMOS technology
  - 1P6M, f_T=150 GHz
- Size: 2.6 x 3.2 mm^2 (overall)
- Near perfect corporate-feed layout
  - E-length is identical for all channels
- Metallic barrier
  - Grounded via stacks from M1-M6
  - Decrease ch-to-ch coupling
- Current consumption: 724 mA (5 V, 3.6 W)



16-Element mm-wave phased-array Tx (44 GHz, 1:8 T-junction)

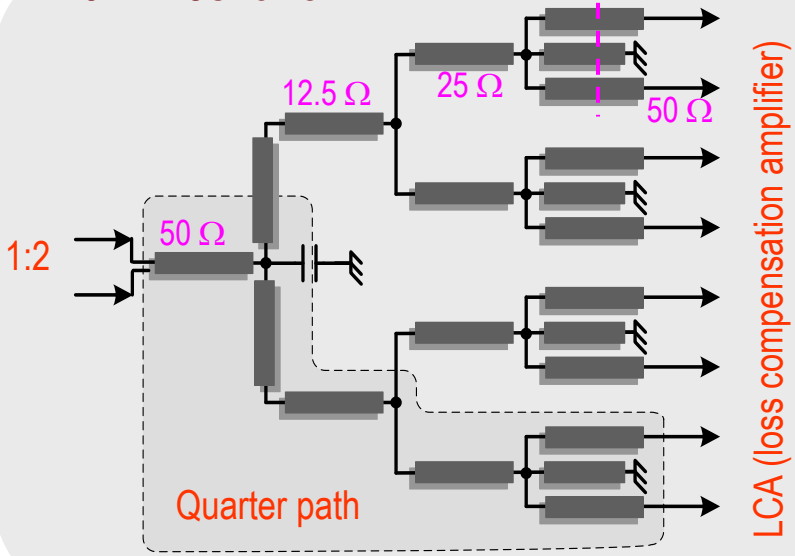


Shielded Broadside-coupled Diff-T-line



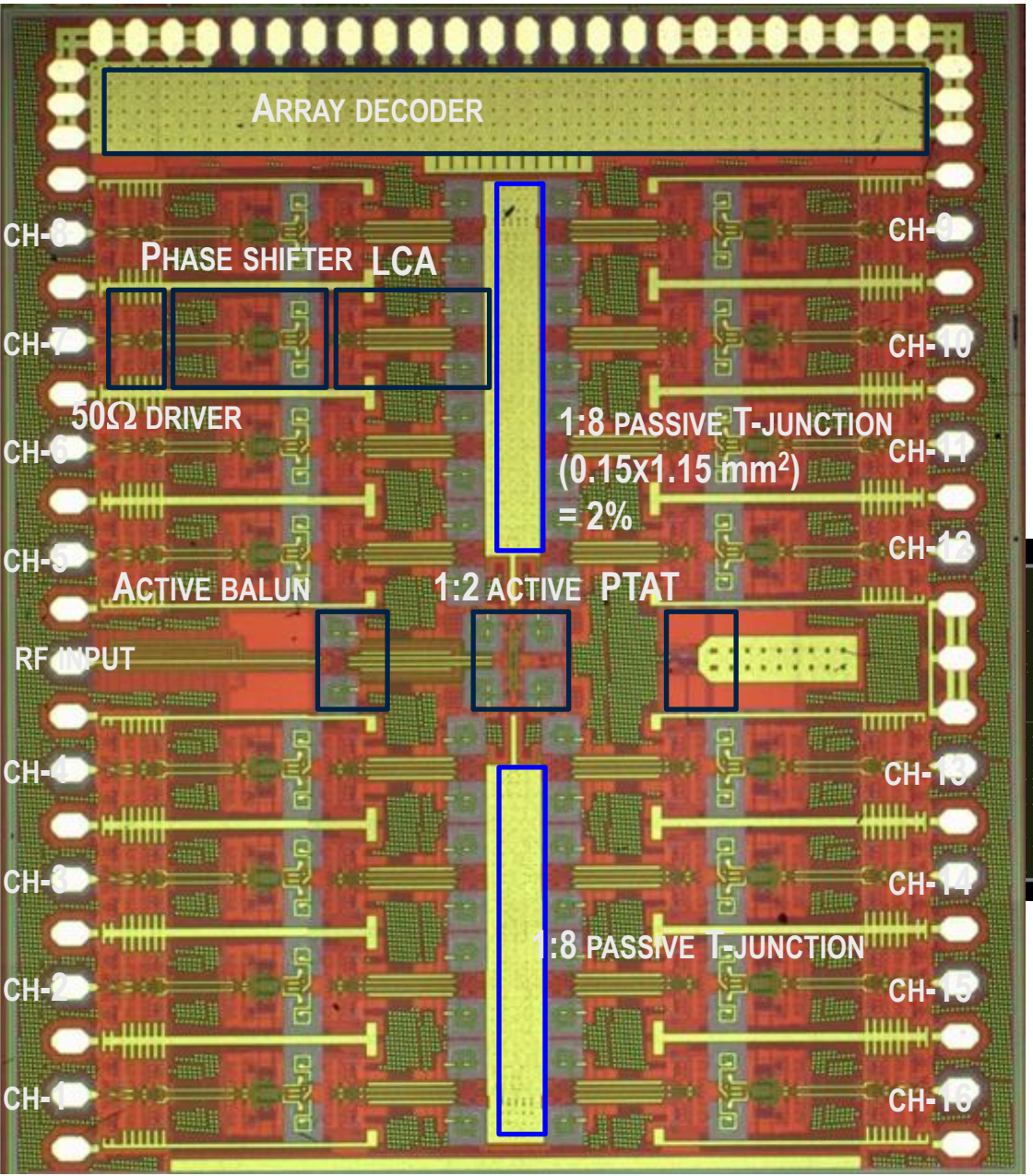
- Perfectly shielded (no coupling btw T-lines)
- Allow compact integration of many diff T-lines

1:8 Tee-Junction Divider

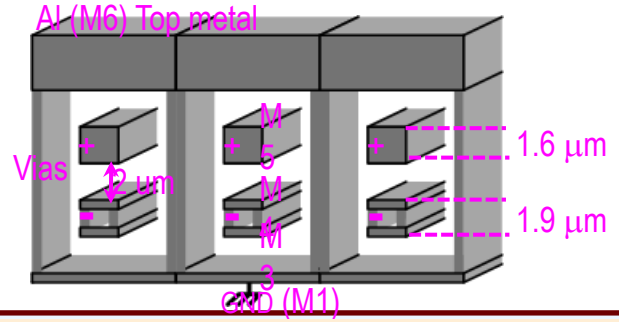


Division loss: 18 dB + parasitic loss (~ 3 dB)

16-Element mm-wave phased-array Tx (44 GHz, coaxial T-line)

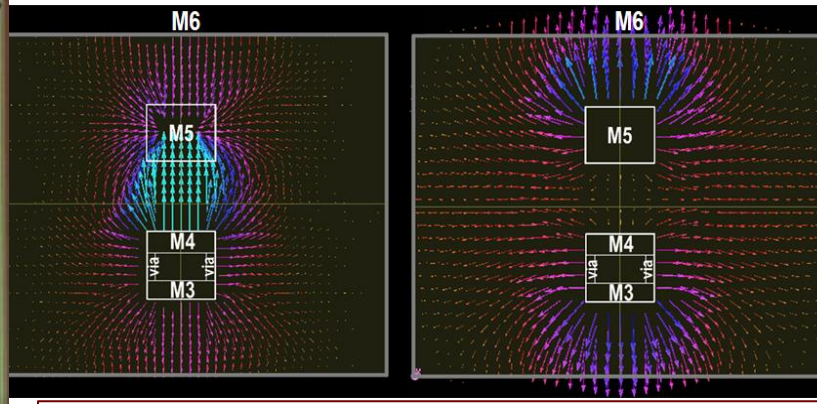


Shielded Broadside-coupled Diff-T-line



- Perfectly shielded (no coupling btw T-lines)
- Allow compact integration of many diff T-lines

Odd-mode E-fields | Even-mode E-fields



- W=3 μm: odd-mode impedance=50 Ω (HFSS sim)
- Most fields (> 95%) are confined btw diff-T lines
- Measured loss: 3 dB / 0.5 mm @45 GHz

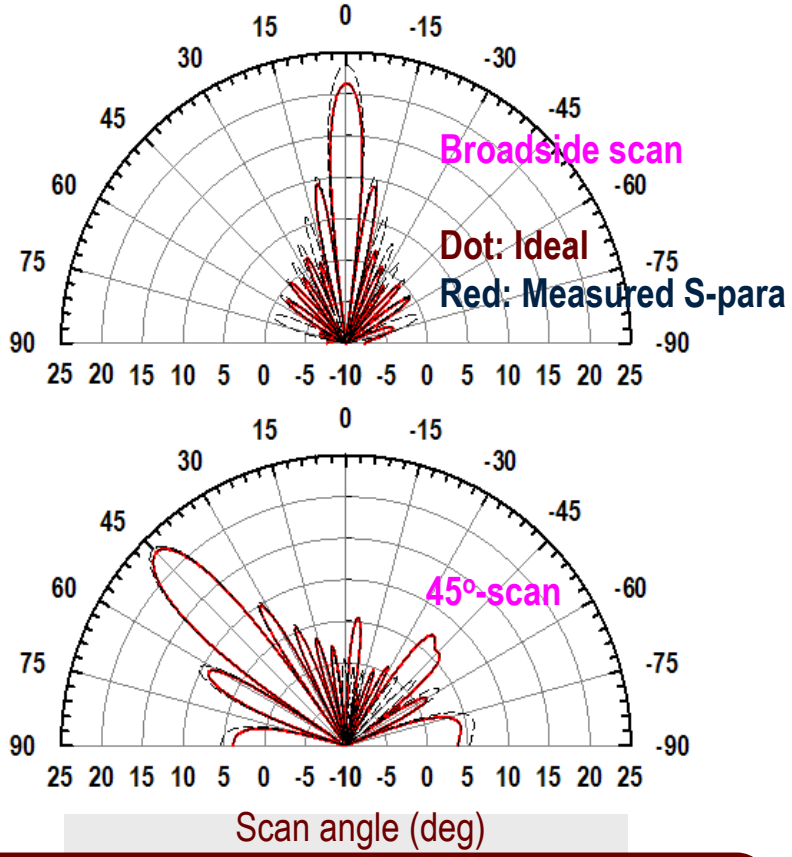
16-Element mm-wave phased-array Tx (44 GHz, measurement)

Parameter	Results
Technology	0.18-μm SiGe BiCMOS (Jazz SiGe120, 1P6M)
Supply voltage	5 V (analog), 3.3 V (digital)
Current consumption	I_{bias}=720 mA (44 mA per channel)
Frequency band	Q-band (3-dB BW: 40-45.5 GHz)
Phase resolution	4-bit (accuracy > 5-bit)
Input return loss	< -10 dB @ 36.6-50 GHz
Output return loss	< -10 dB @ 37.6-50 GHz
Power gain (ave)	12.5 dB @ 42.5 GHz
Maximum output power	-2.5±1.5 dBm @ 42.5 GHz
Phase error (RMS)	< 8.8° @ 30-50 GHz
Gain error (RMS)	< 1.3 dB @ 30-50 GHz
Output P_{1dB}	-5±1.5 dBm @ 42.5 GHz
Phase mismatch (RMS)	< 7° @ 30-50 GHz (between all channels)
Amp. mismatch (RMS)	< 1.8 dB @ 30-50 GHz (between all channels)
Isolation (CH-to-CH)	< -30 dB @ 30-50 GHz
Array factor directivity	12 dB (16-element)
Chip area	2.6 x3.2 mm^2

Single channel

16-array

Beam pattern based on measured S-parameters (16 S-para x 16 channels= 256 S-para)

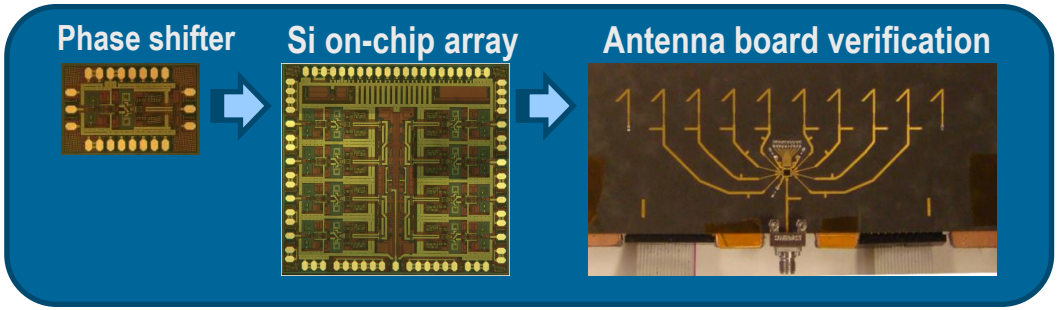


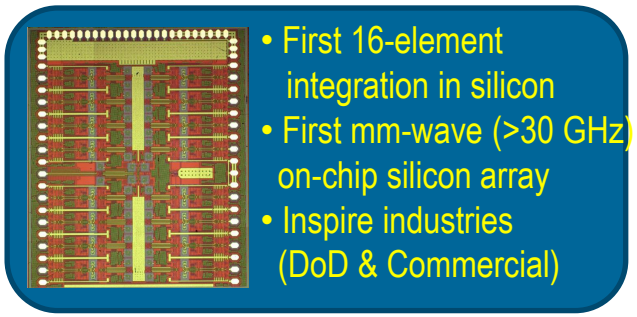
Assumption

- Isotropic radiator, uniform array spacing, d=λ/2
- Ideal 45°-scan: 127.3° (= 360° x d/λ x sin45°)

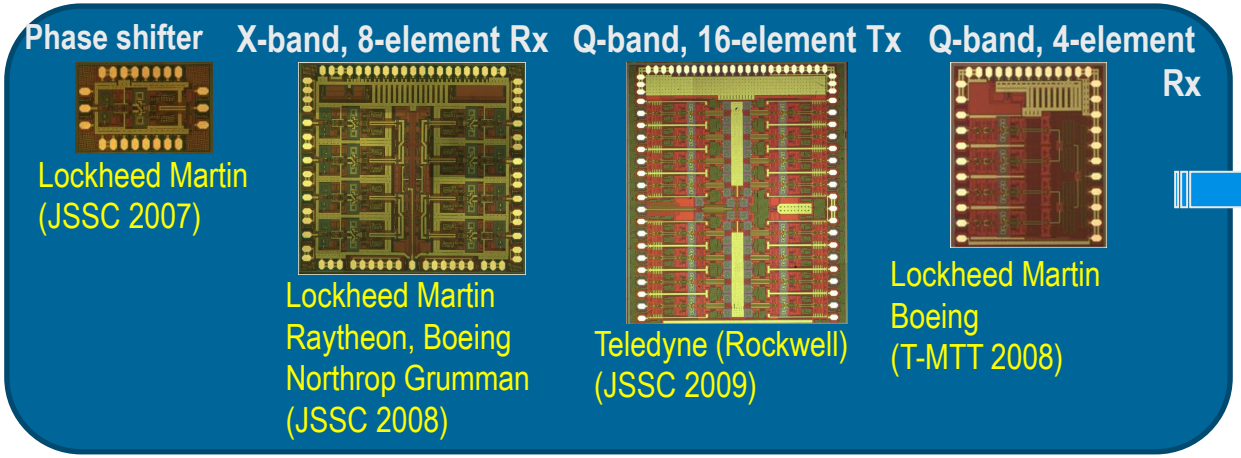
CONCLUSIONS

- Provide a low-cost phased array solution for RF and mm-wave defense & commercial applications
- First implementation of *All-RF (RF-scanning)* Si phased array IC including system-level demonstration





- Successful technology transfers to DoD industries (Boeing, Lockheed Martin, Raytheon, Teledyne, NG)



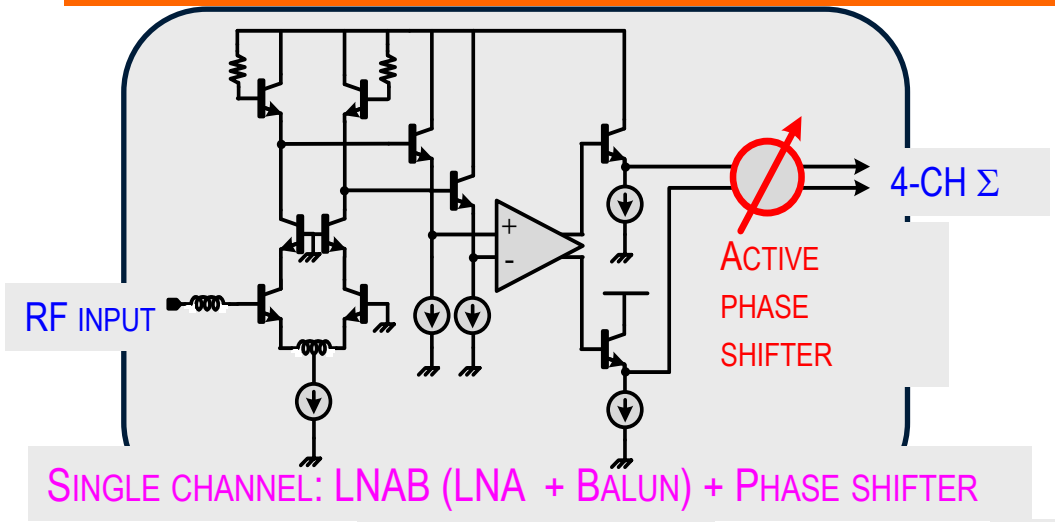
"The Most Significant Achievement in 2008" **DARPA Special "WAR REPORT" to Pentagon**

"Team of The Year Award in 2010" **from Teledyne Scientific Corp (Rockwell)**

- Designs can be extended for high data-rate wireless systems at mm-wave frequencies (60 GHz wireless comm., > 100 GHz high data rate mm-wave comm. …)
- SiBeam, IBM, MTK, Intel … all use now the *All-RF* based phased array architecture.

BACK-UP SLIDES

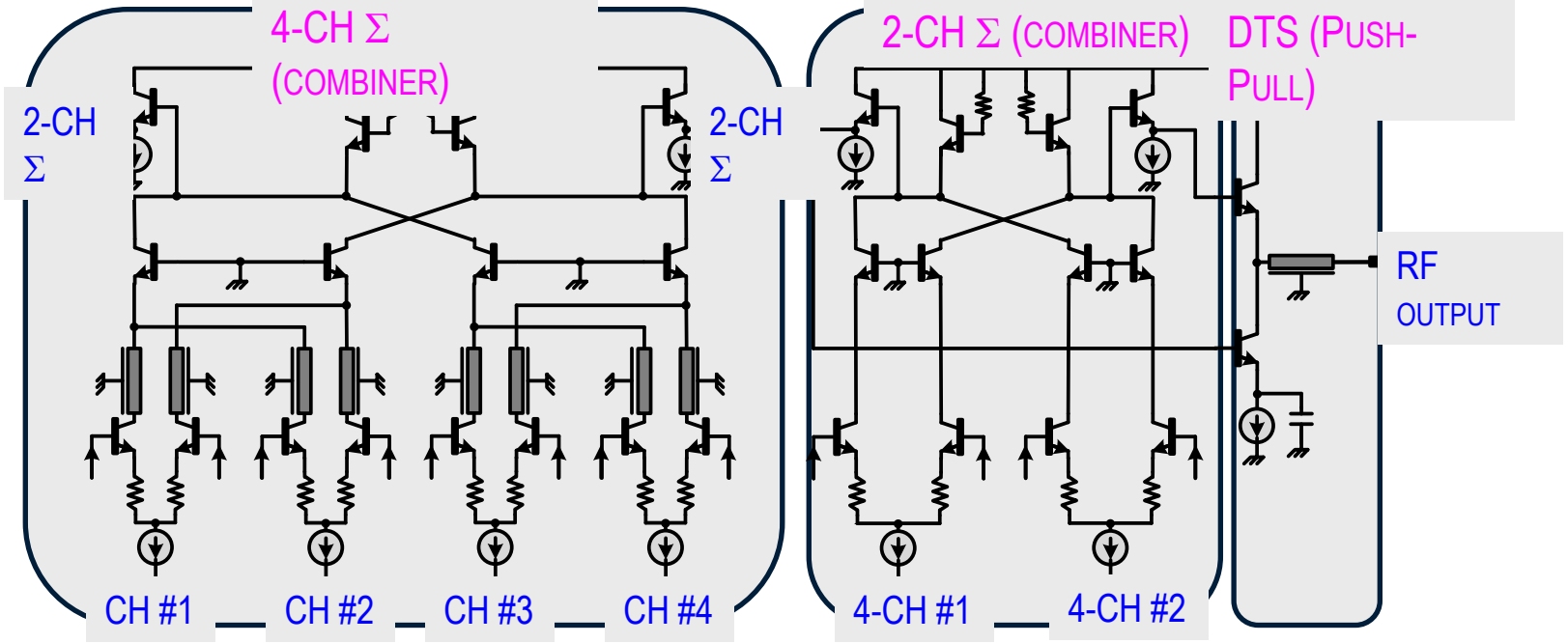
8-ELEMENT PHASED-ARRAY (12 GHZ, SCHEMATICS)



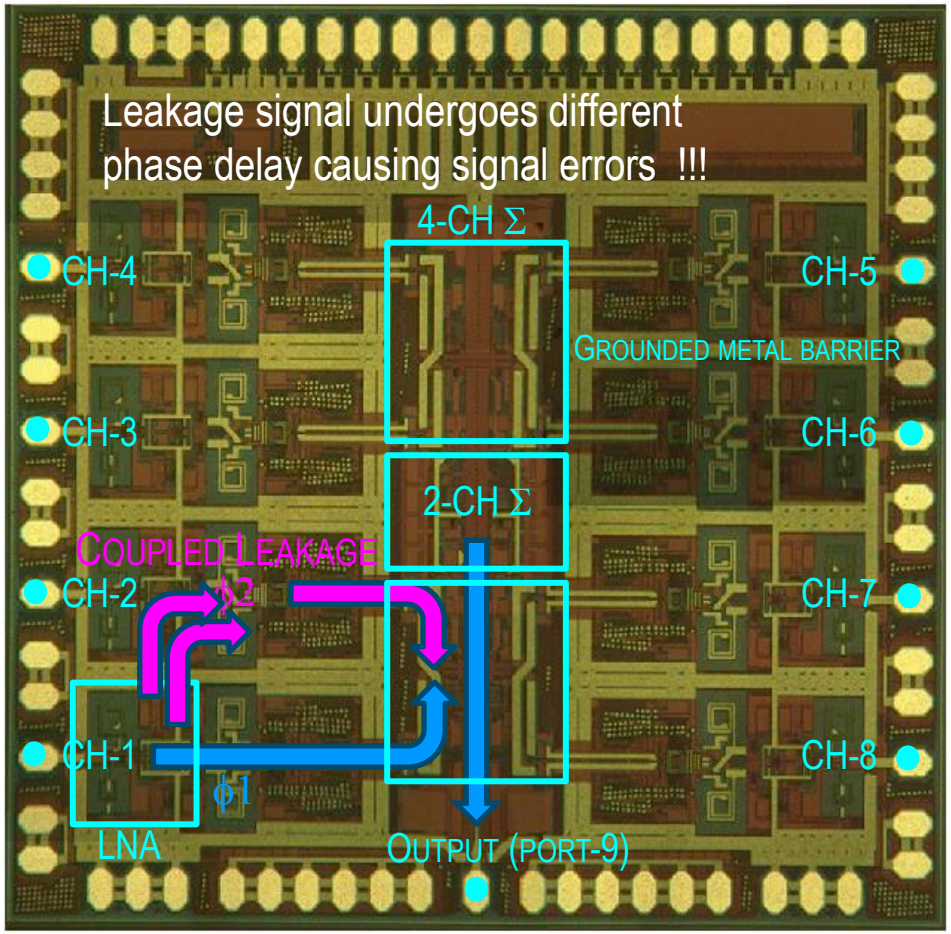
SINGLE CHANNEL: LNAB (LNA + BALUN) + PHASE SHIFTER

- Emitter-coupled diff-pair
- Single-to-differential conversion
- L-C input matching
- 2nd–stage diff amp: CMRR

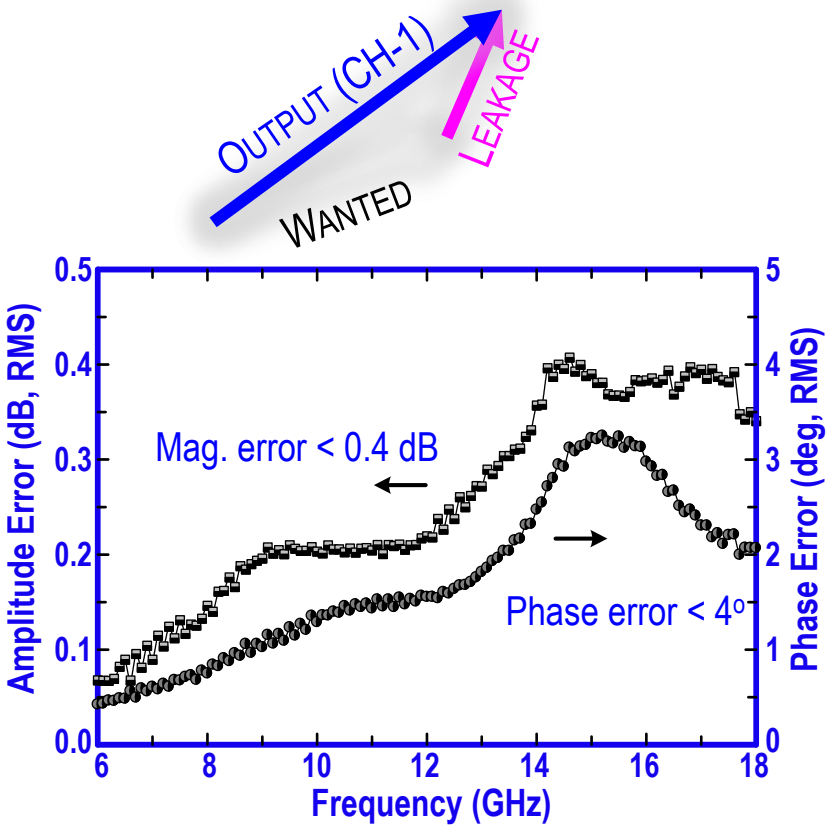
- Signal -Σ in current domain
- Binary fashion signal -Σ
- Wideband signal-Σ
- NMOS-based push-pull



8-ELEMENT PHASED-ARRAY (12 GHZ, CH-TO-CH COUPLING)



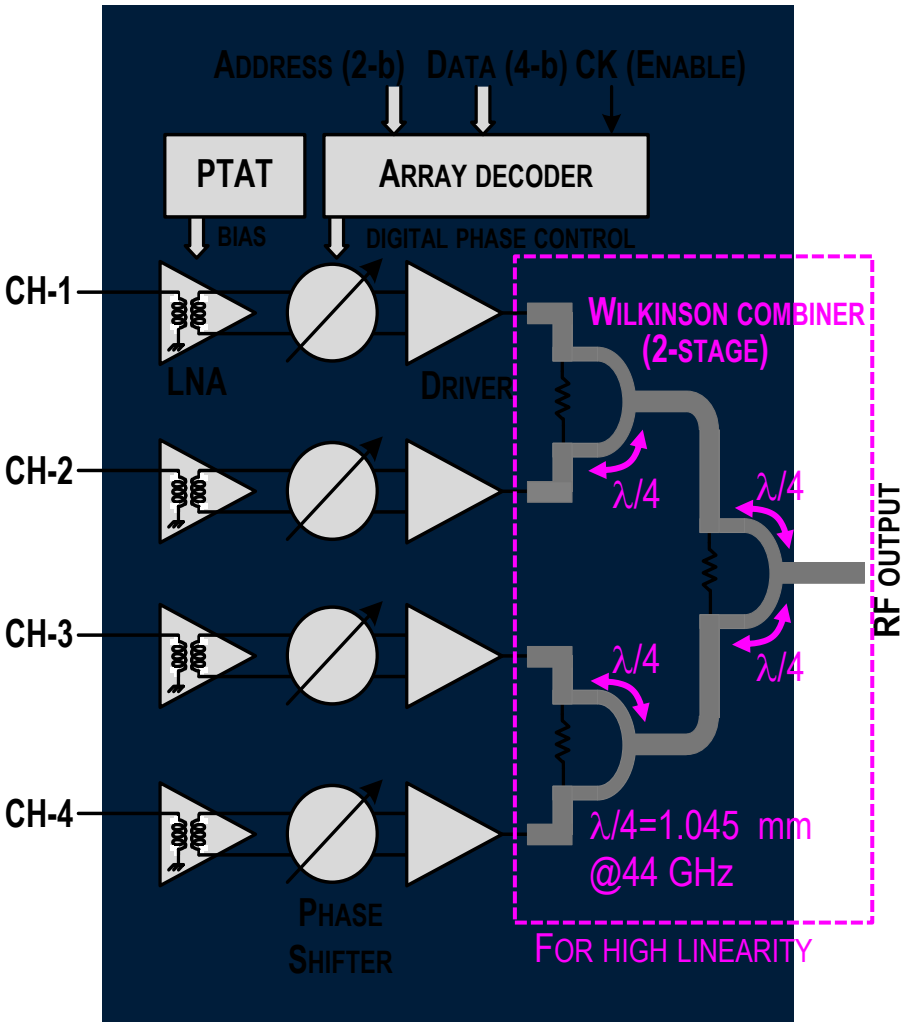
SIGNAL ERROR DUE TO COUPLING
(@ 12 GHZ, GAIN=20 dB)



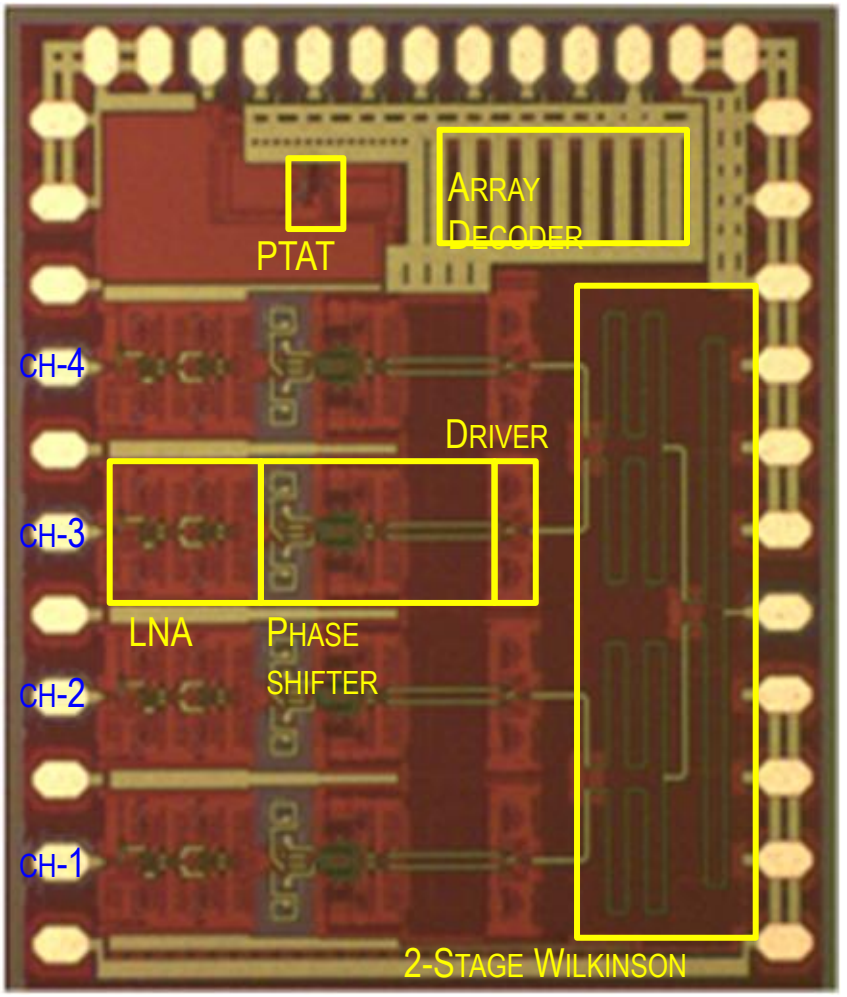
- Coupling causes amplitude & phase errors which could be serious in silicon
- Measured errors are negligible due to high isolation layout, e.g. metallic barrier

4-Element mm-wave phased-array Rx (44 GHz, arch & chip photo)

Phased-array Rx block diagram



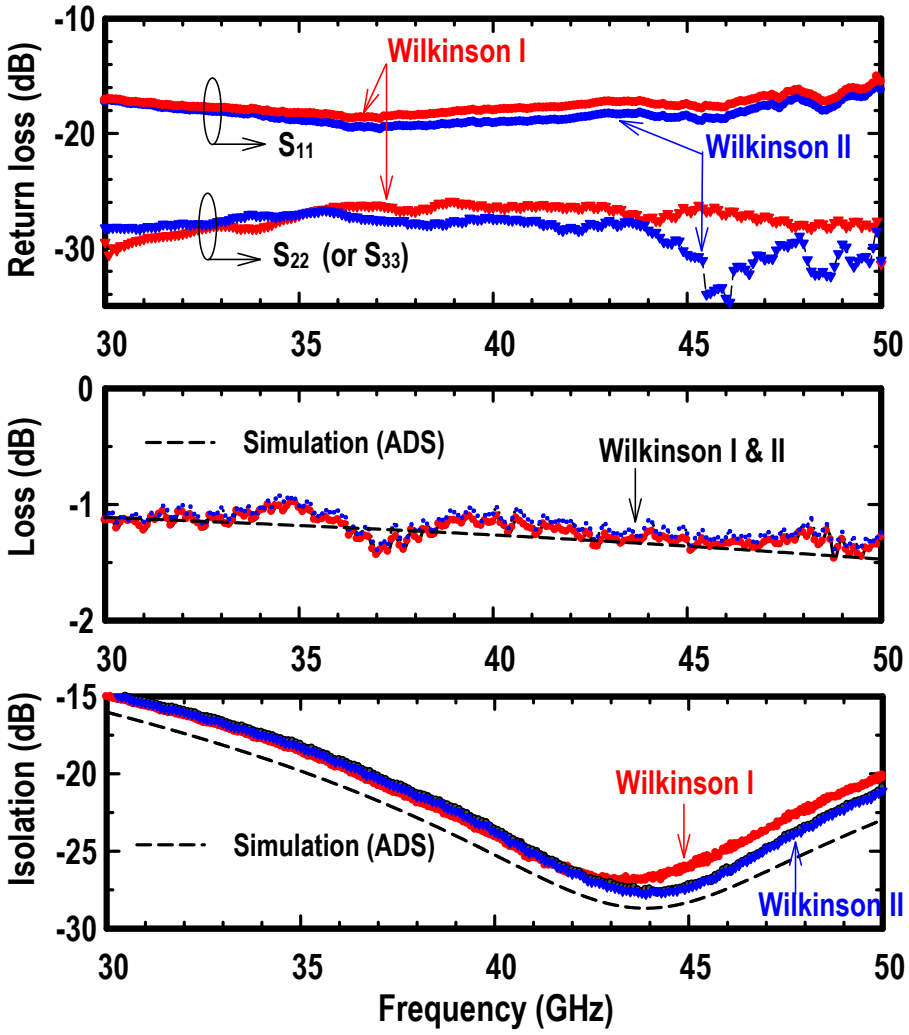
Chip photograph



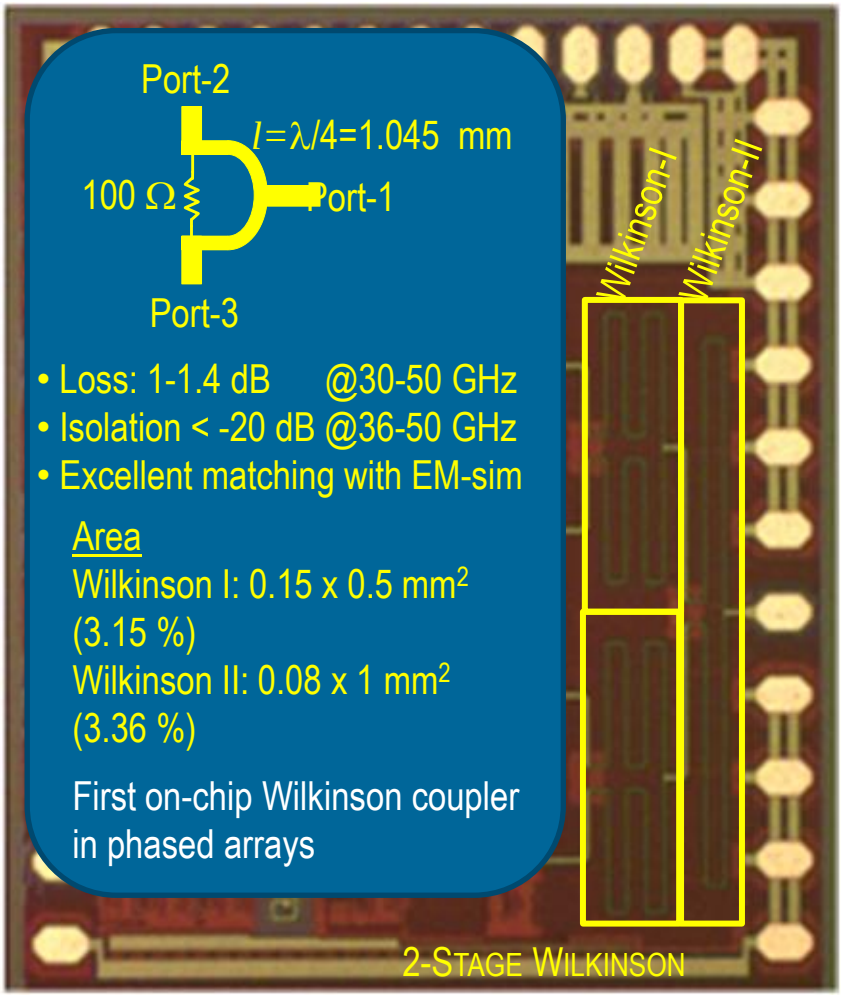
SiGe BiCMOS (f_T=150 GHz), Area=1.4x1.7 mm^2

4-Element mm-wave phased-array Rx (44 GHz, Wilkinson coupler)

Wilkinson coupler measurements



Chip photograph



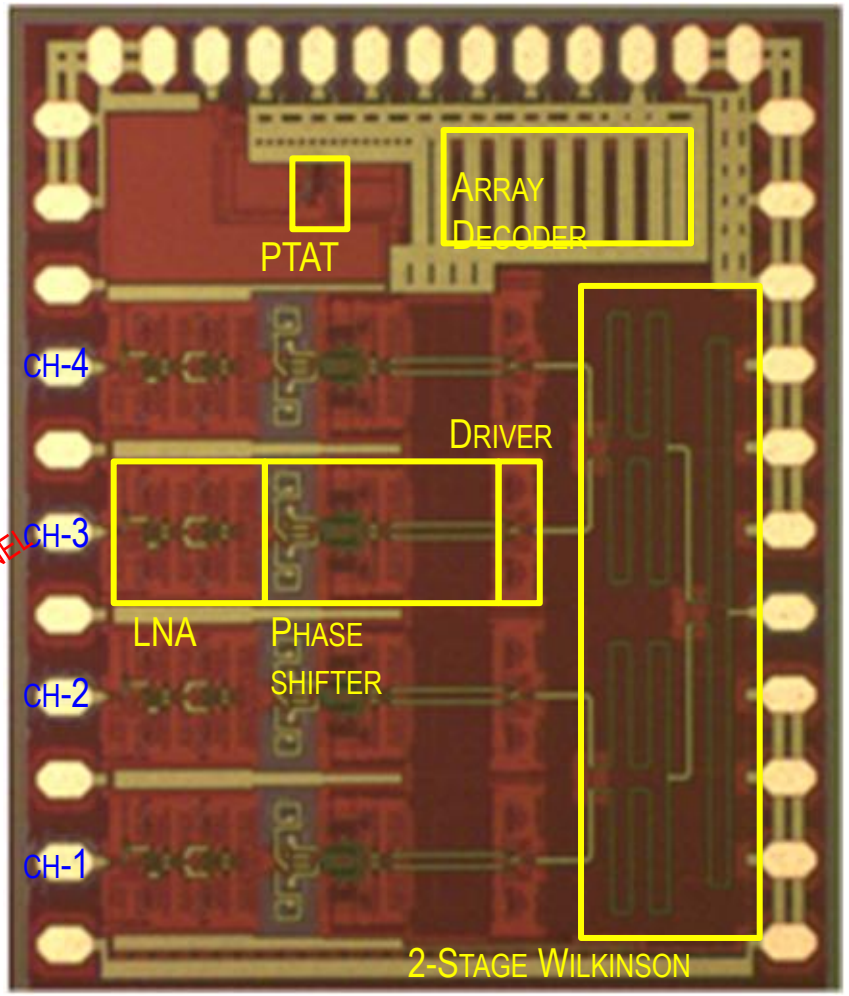
SiGe BiCMOS (f_T=150 GHz), Area=1.4x1.7 mm^2

4-Element mm-wave phased-array Rx (44 GHz, measurement)

Parameter	Results
Technology	0.18-μm SiGe BiCMOS (Jazz SiGe120, 1P6M)
Supply voltage	5 V (analog), 3.3 V (digital)
Current consumption	I_{bias}=118 mA (29 mA per channel)
Frequency band	Q-band (3-dB BW: 32.3-44 GHz)
Phase resolution	4-bit (accuracy > 5-bit)
Input return loss	< -10 dB @ 40-50 GHz
Output return loss	< -10 dB @ 40-50 GHz
Power gain (ave)	10.4 dB @ 38.5 GHz
NF	12.4 dB @ 38.5 GHz
Phase error (RMS)	< 8.7° @ 30-50 GHz
Gain error (RMS)	< 1.2 dB @ 30-50 GHz
IIP3	-13.8±1.5 dBm @ 38.5 GHz
Phase mismatch (RMS)	< 2° @ 30-50 GHz (between all channels)
Amp. mismatch (RMS)	< 0.4 dB @ 30-50 GHz (between all channels)
Isolation (CH-to-CH)	< -35 dB @ 30-50 GHz
Array factor directivity	6 dB (4-element)
Chip area	1.4 x1.7 mm^2

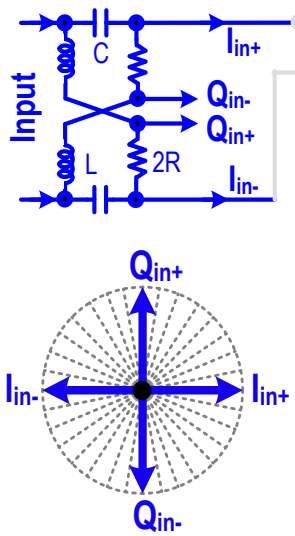
Single channel

4-array



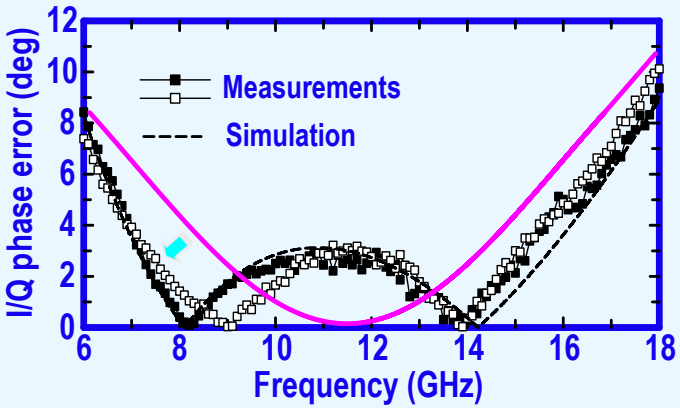
Ref: K.-J. Koh *etal,* "A Q-Band Four-Element Phased-Array Front-End Receiver with Integrated Wilkinson Power Combiners in in 0.18-μm SiGe BiCMOS Technology", IEEE Trans. On MTT, Sept 2008

ACTIVE PHASE SHIFTER - I/Q NETWORK (LOSSLESS)

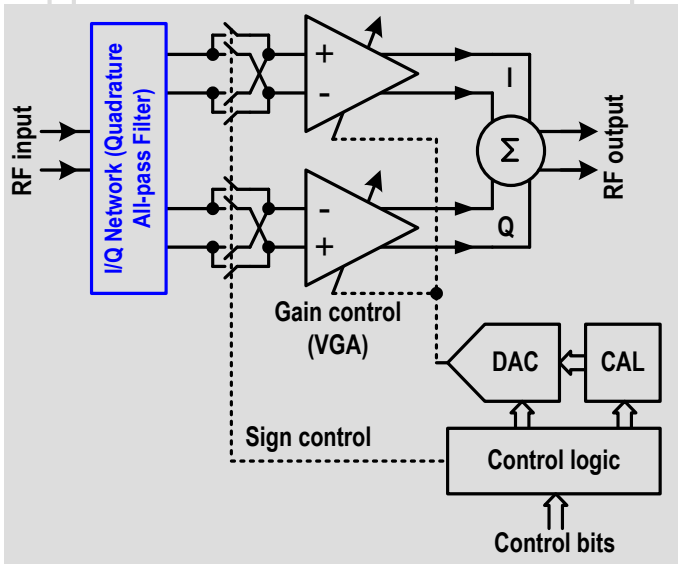


FOR X- & KU-BAND (6-18 GHZ)

- 2R=50 Ω
  L=324 pH
  C=543 fF
  ⇒ f_o=12 GHz
- Optimization of R, L & C
  ⇒ Allow acceptable error around f_o to increase bandwidth

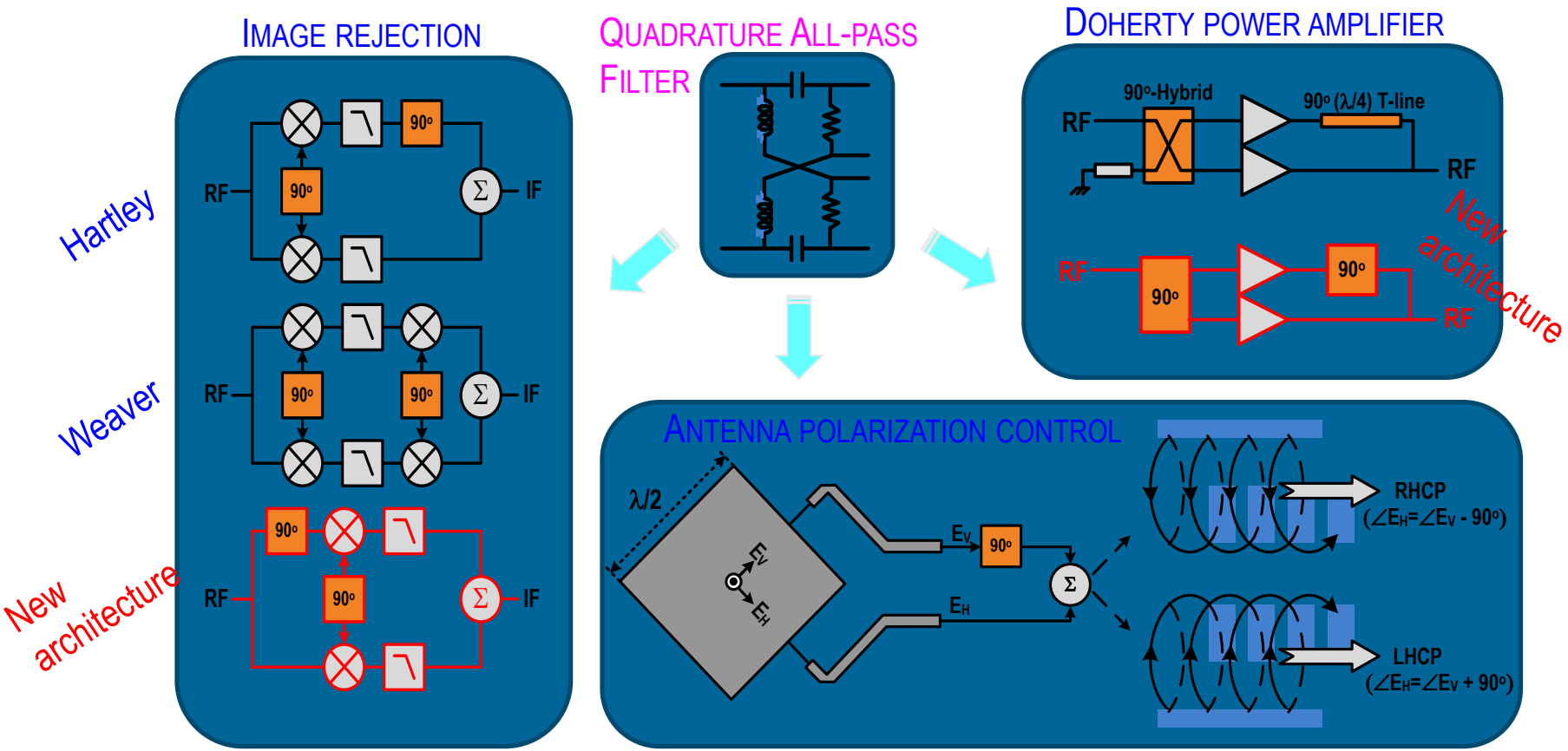


Under 70 fF loading capacitance,
I/Q phase error < 3° @7-15 GHz
I/Q amplitude mismatch < 1.8 dB @7-15 GHz



SOME REMARKS ON I/Q NETWORK

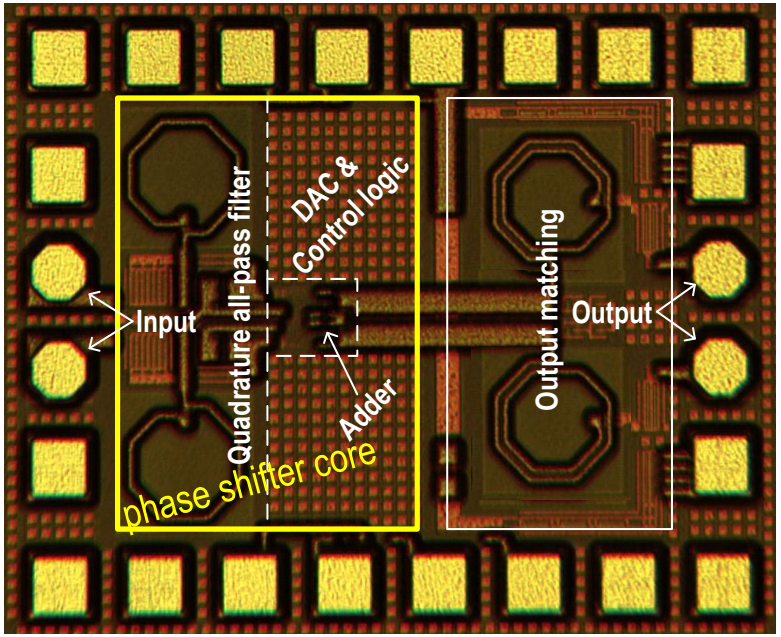
- I/Q network is an indispensable block for comm. system, but rarely used at RF signal path due to loss
- Lossless I/Q network, QAF (3dB gain, 3dB NF, All-Pass), enables many new system configurations



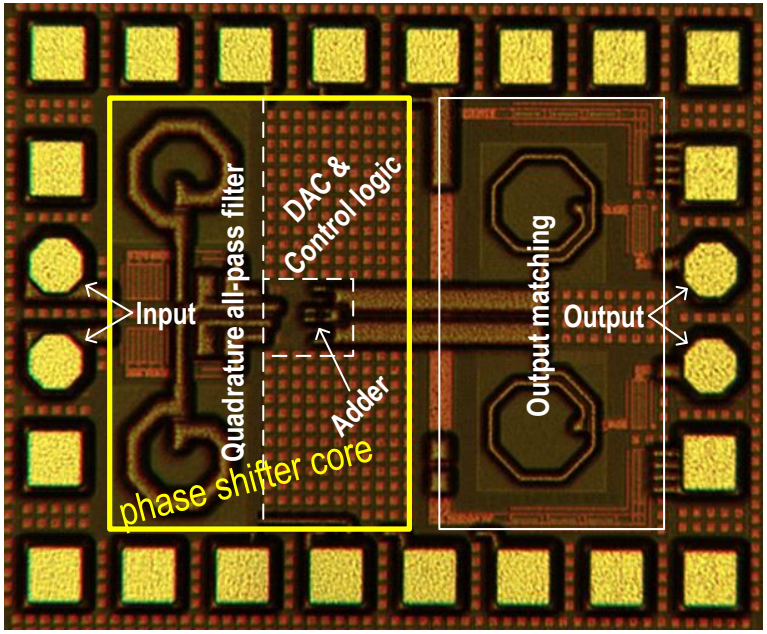
- Versatile and promising building block for future RF & mm-wave phased arrays and comm. systems

0.13-μm CMOS ACTIVE PHASE SHIFTERS

X-BAND (6-18 GHz) DESIGN



KU-BAND (15-26 GHz) DESIGN



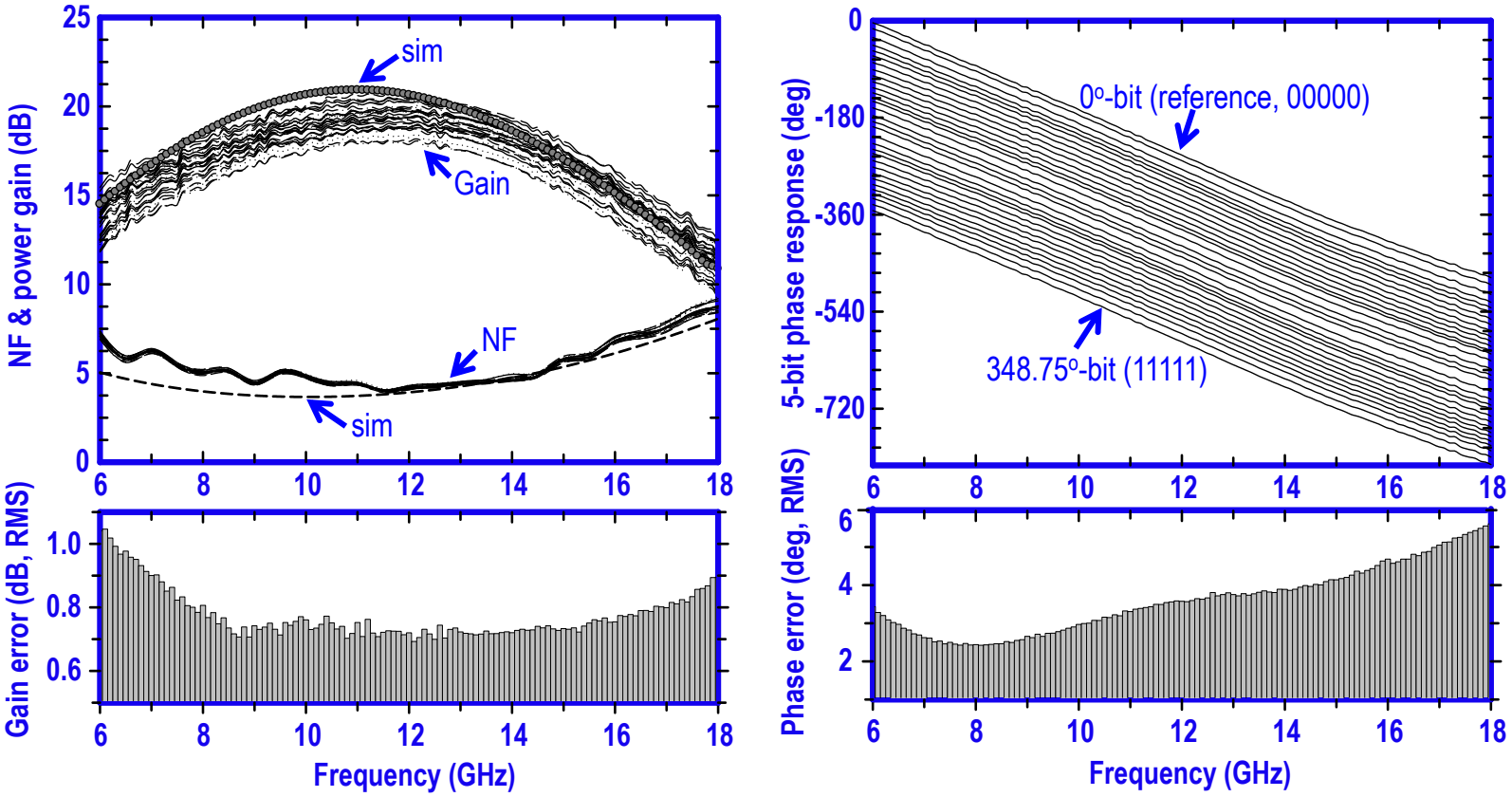
CMOS implementations with same active phase shifter architectures

Phase shifter core size: 0.3 x 0.4 mm^2 (smallest one published)

Ref: K.-J. Koh etal, "0.13-μm CMOS phase shifters for X-, Ku-, and K-Band Phased Arrays", IEEE JSSC, Nov. 2007

- First realization of CMOS active phase shifters (4-bit resolution)
- Supported by Intel "UC Discovery Project" (2006-2007)
- Presented at Intel project review meeting & RFIC 2007

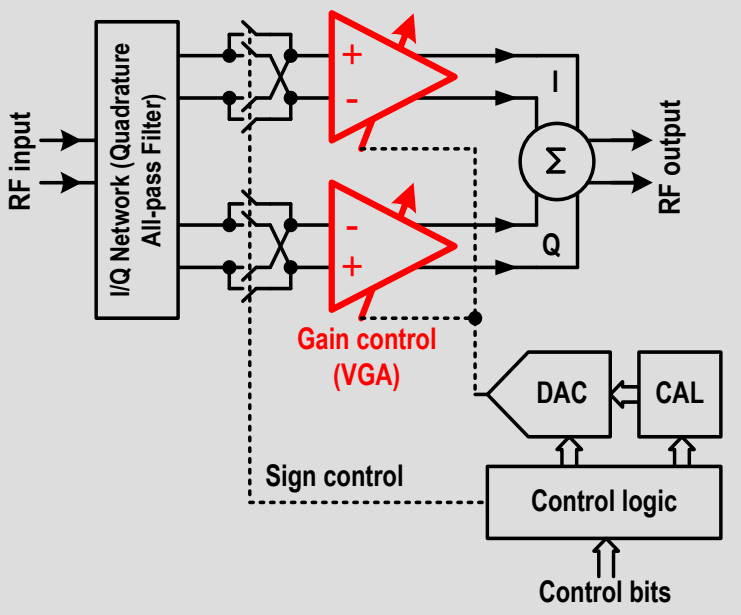
ACTIVE PHASE SHIFTER – MEASUREMENTS

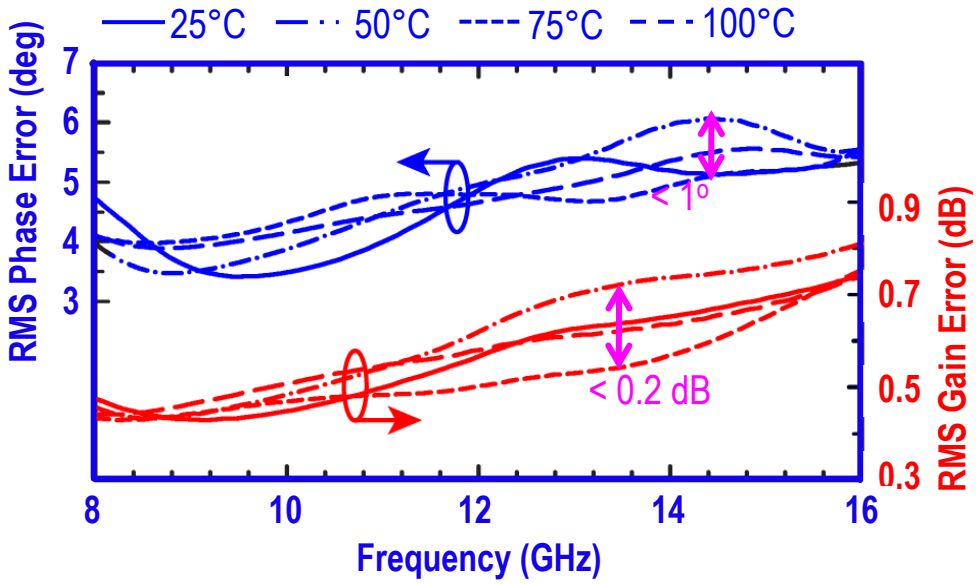


- Gain: 16.5 - 19.5 dB @7.5-15.2 GHz
- Gain error: ≤ 1.1 dB (RMS) @6-18 GHz
- NF: 4 - 5.7 dB @7.5-15.2 GHz
- Phase error: < 5.6° (RMS) @6-18 GHz
- S11 < -10 dB @11-15.5 GHz
- S22 < -10 dB @6-18 GHz

The active phase shifter achieves 6-bit accuracy at 6-18 GHz ($\Delta = 360^o/2^6 = 5.625^o$)

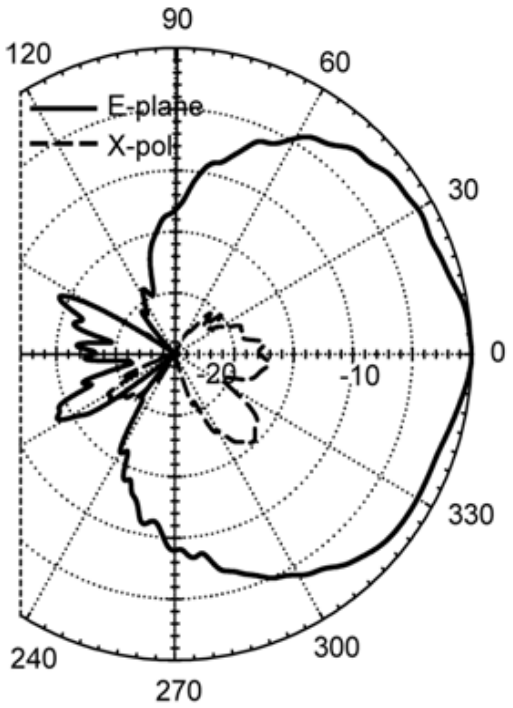
ACTIVE PHASE SHIFTER – TEMPERATURE MEASUREMENTS

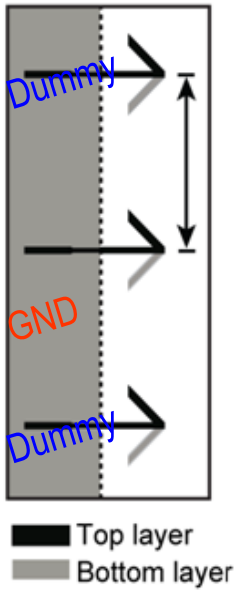




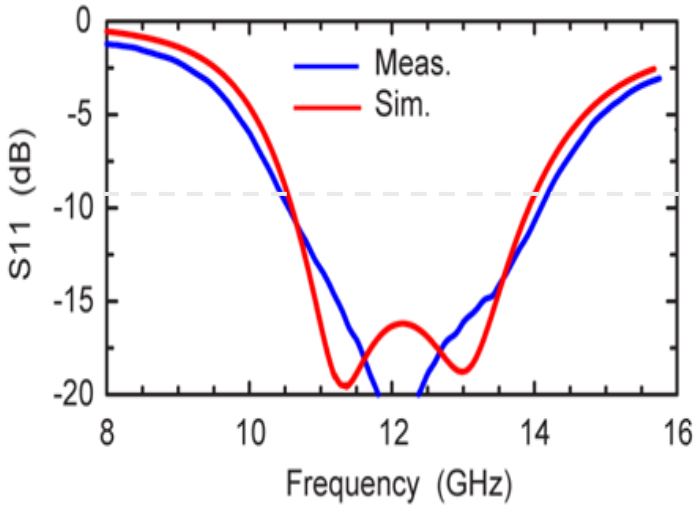
- I & Q paths are biased with a reference PTAT circuit
- RMS phase error < 6° @ 25°-100° C
- RMS gain error < 0.8 dB @ 25°-100° C
- I & Q amplifiers track each other vs. PVT, resulting in low sensitivity to PVT

ANGLED-DIPOLE ANTENNA DESIGN @12 GHZ





0.5 λ_o @ 12 GHz

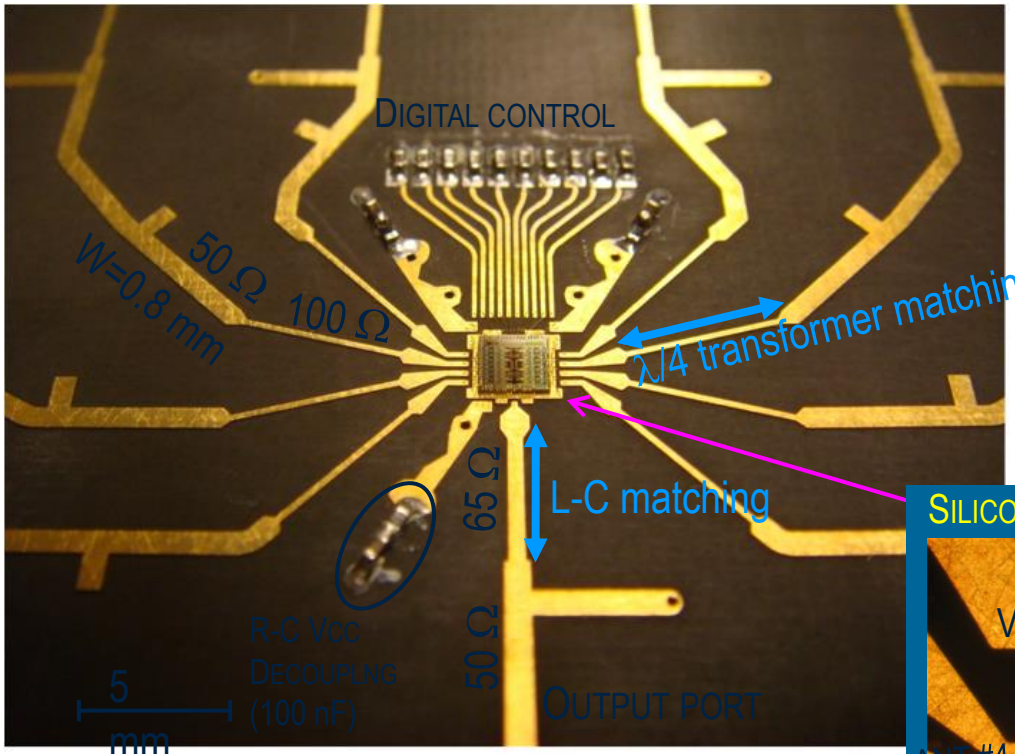


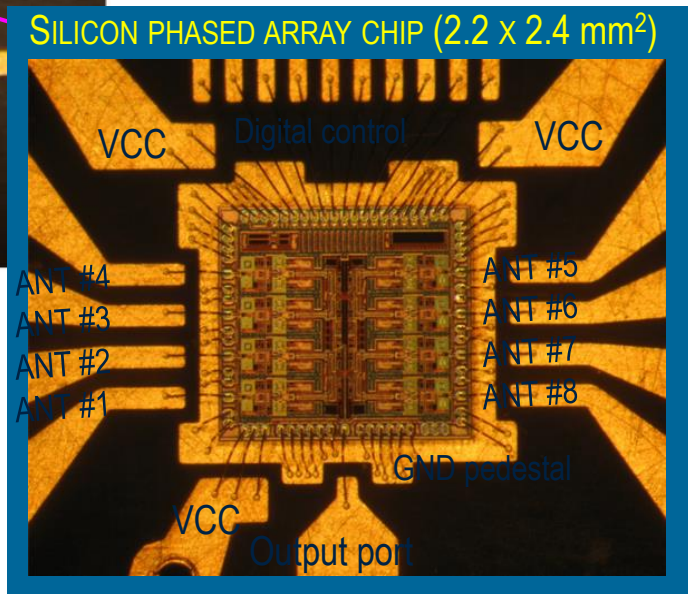
MEASUREMENT

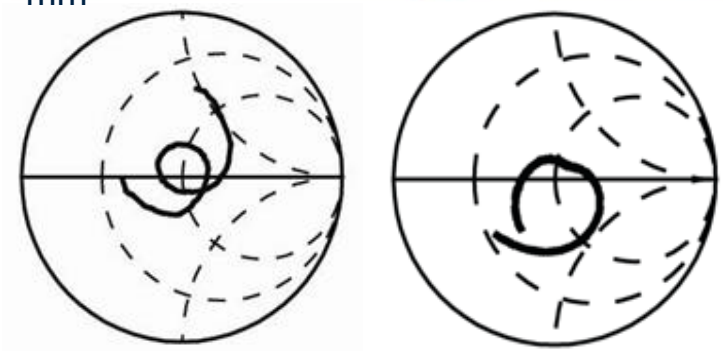
- S_{11} < -10 dB @ 10.5-14 GHz
- 102° HPBW
- 3 dB antenna gain
- Coupling < -17 dB
- Can be used +/- 60° scan with 4dB drop in element factor

Ref: Y. A. Atesal, B. Cetinoneri, K.-J. Koh, G. M. Rebeiz, "X/Ku-Band 8-Element Phased Arrays Based on Single Silicon Chips", 2010 IMS, May 2020

8-ELEMENT PHASED-ARRAY (6-18 GHZ, Z-MATCHING)

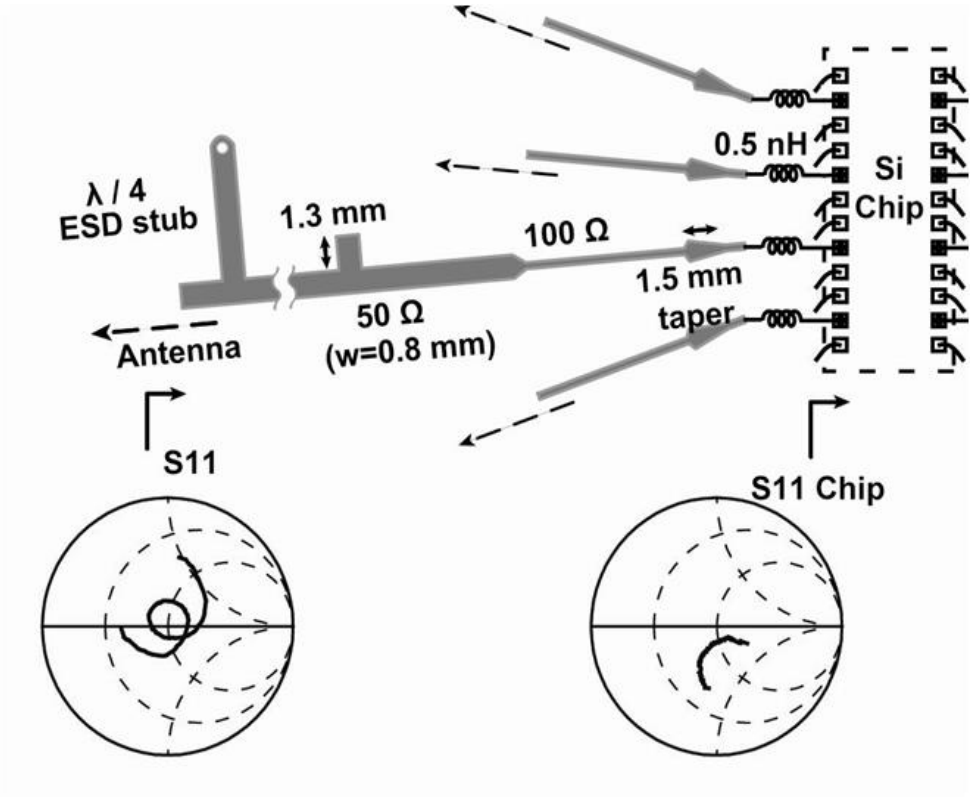




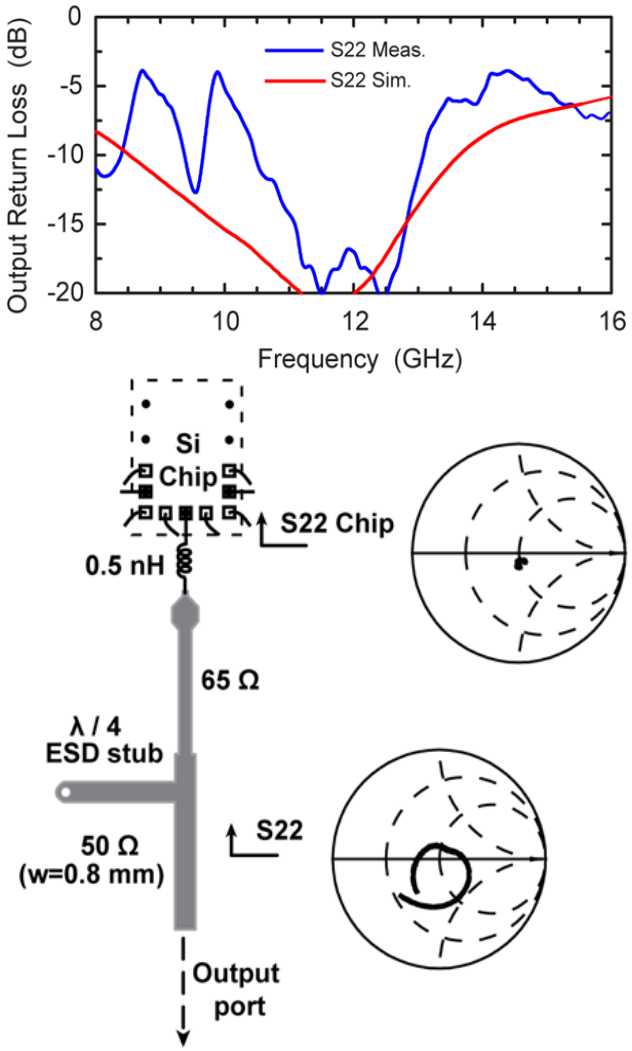


S_{11} < -10 dB @ 10-14 GHz S_{22} < -10 dB @ 8.5-13.5 GHz

8-ELEMENT PHASED-ARRAY (6-18 GHz, BOARD MEASUREMENT)

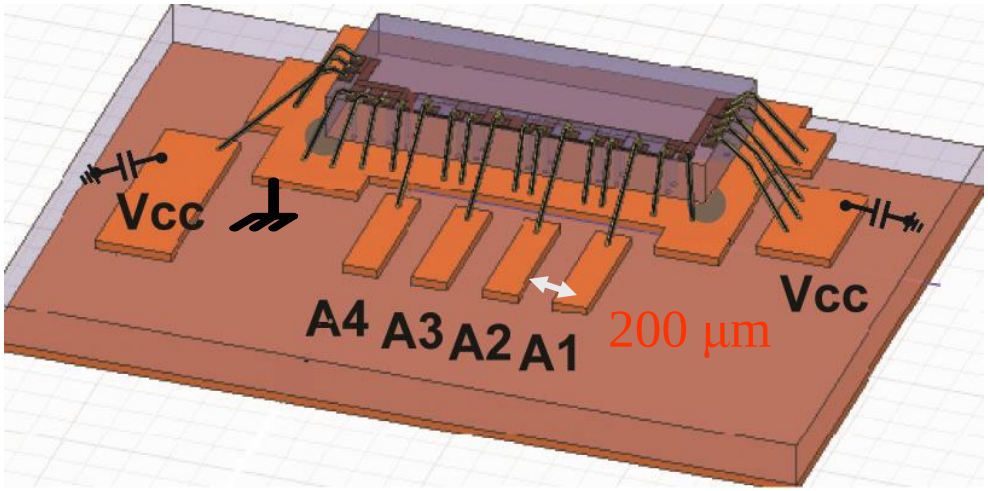


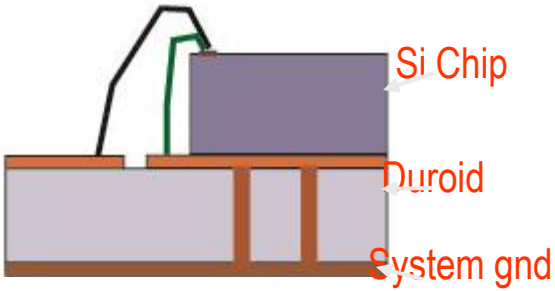
S11 < -10 dB @ 10-14 GHz

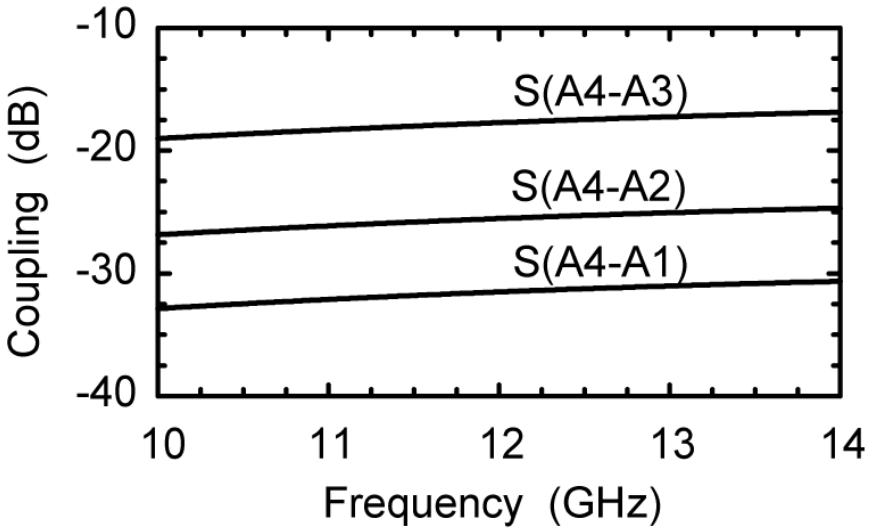


S22 < -10 dB @ 8.5-13.5 GHz

3-D PACKAGE SIMULATION (1)



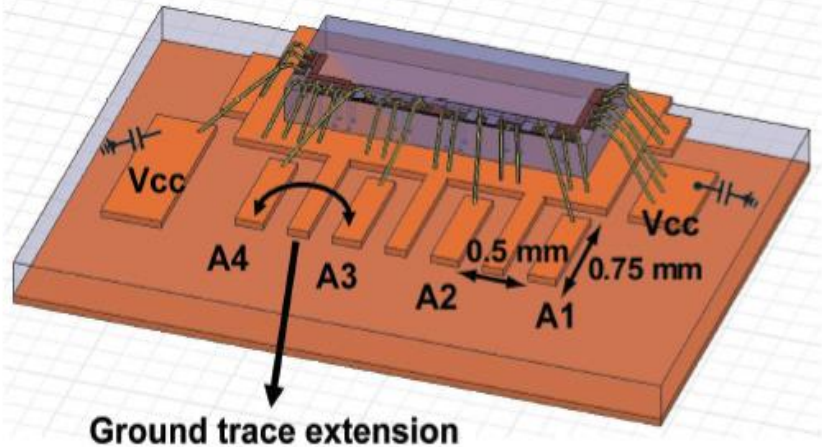




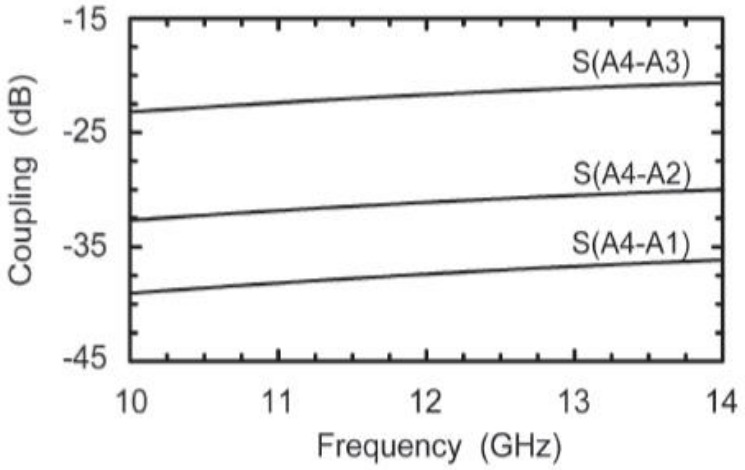
Modeled using HFSS
Coupling between adjacent ports < -17 dB

3-D PACKAGE SIMULATION (2)

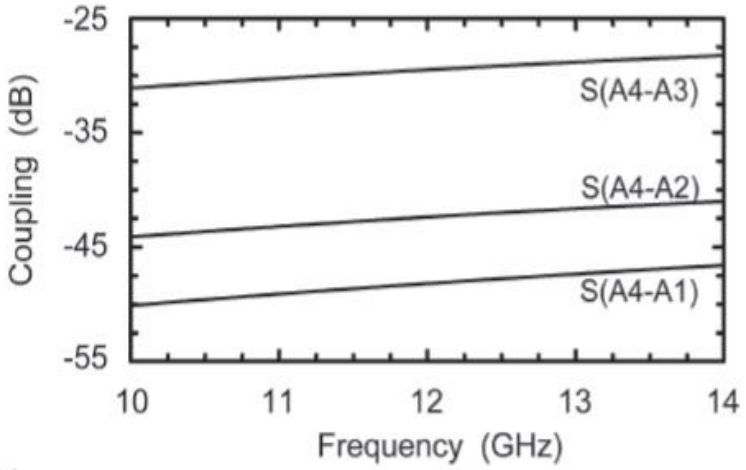
Coupling between adjacent ports is reduced to < -25 dB



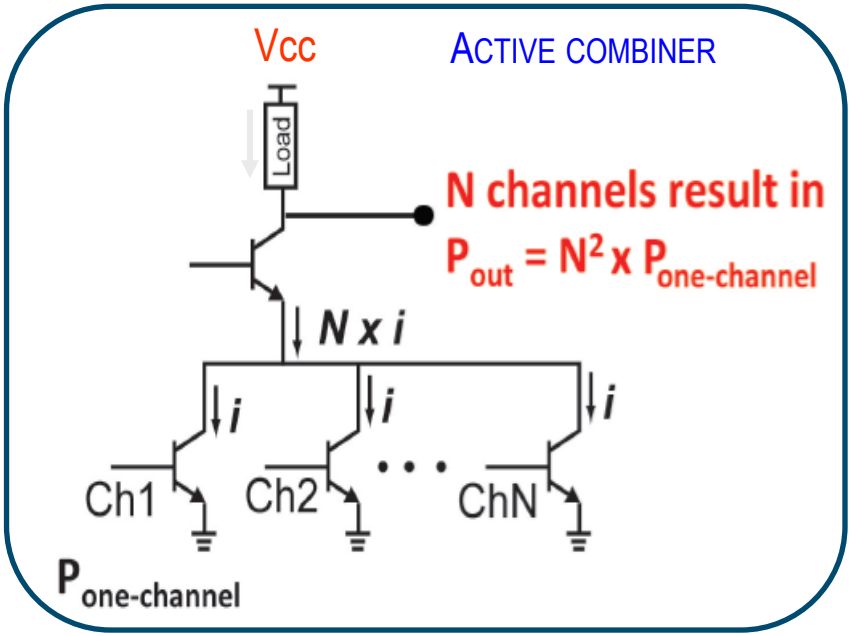
Left open (after 0.75 mm)

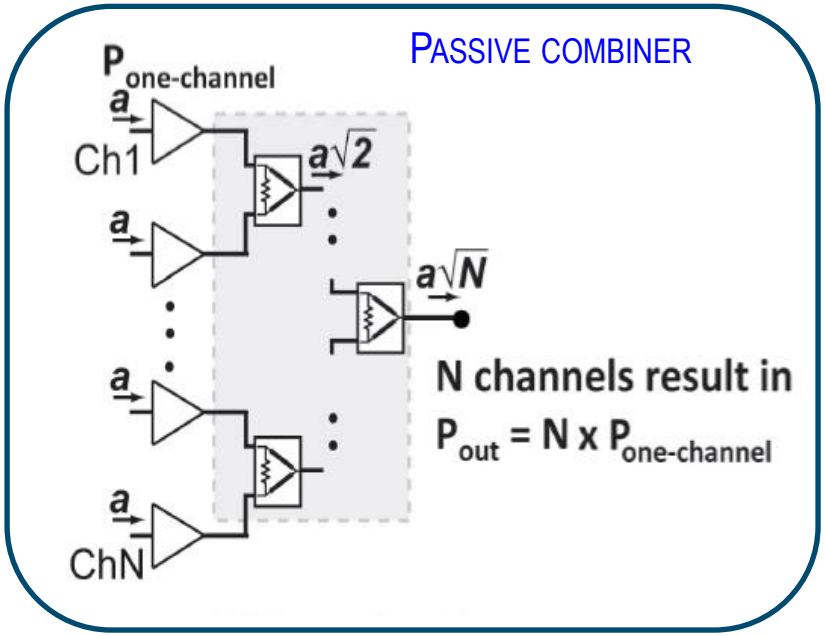


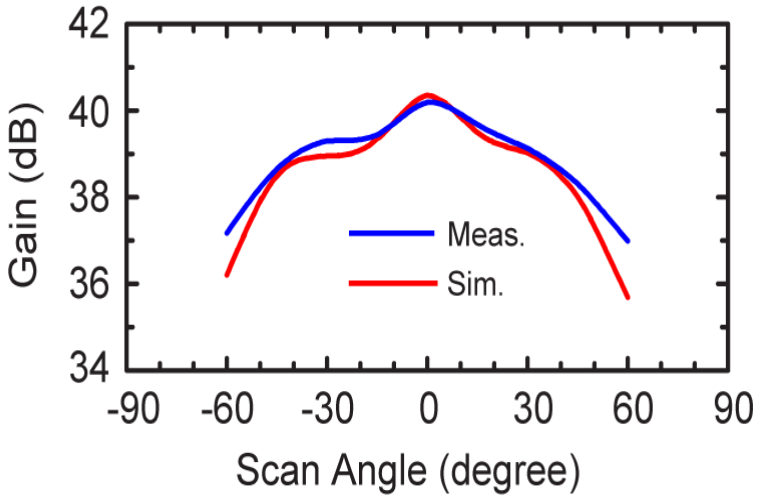
Shorted to the bottom gnd (after 0.75 mm)



ACTIVE COMBINER V.S. PASSIVE COMBINER







20-21 dB channel gain

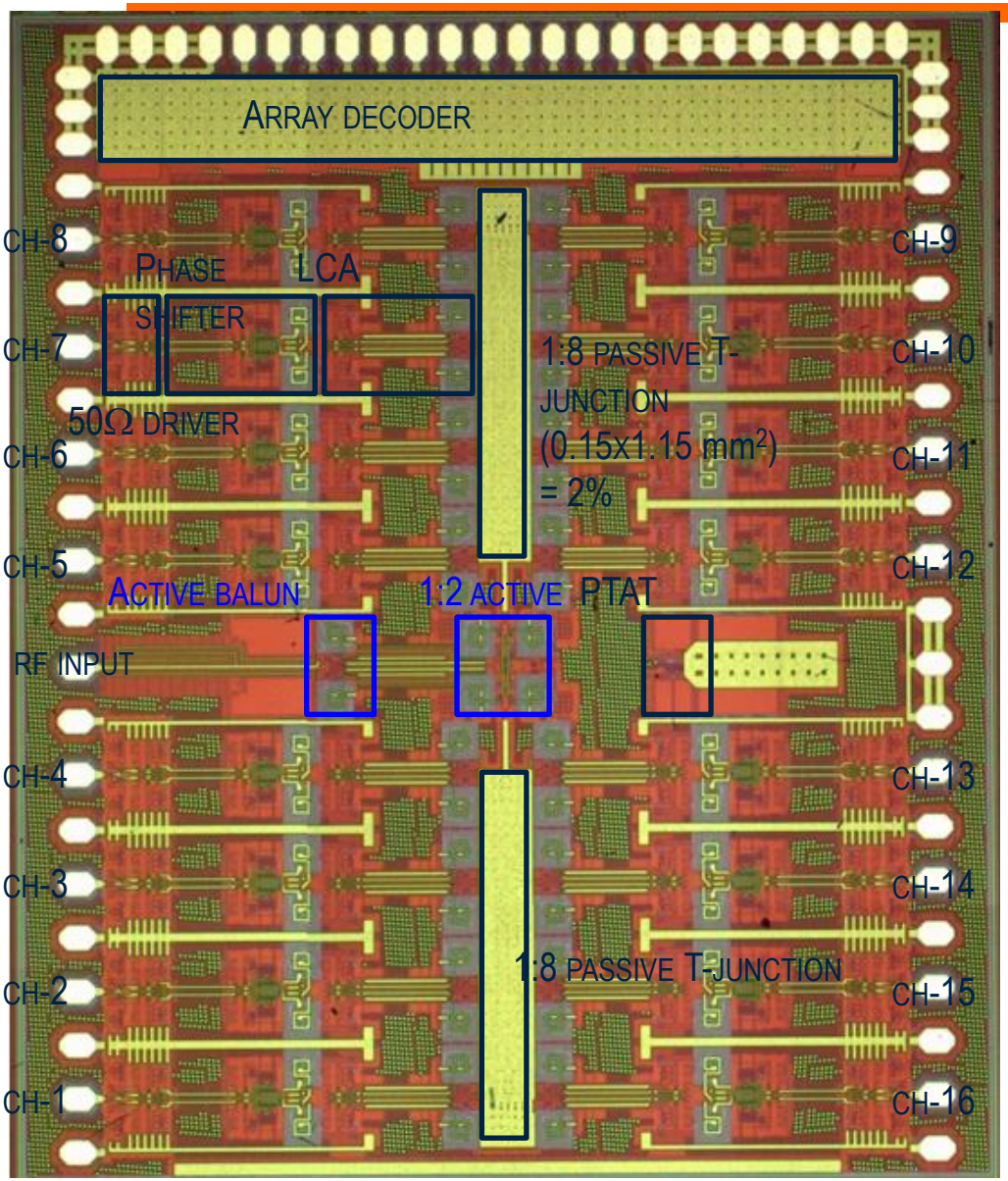
18 dB array gain (αN^2)

~ 3 dB antenna gain

0.7 dB loss due to connector

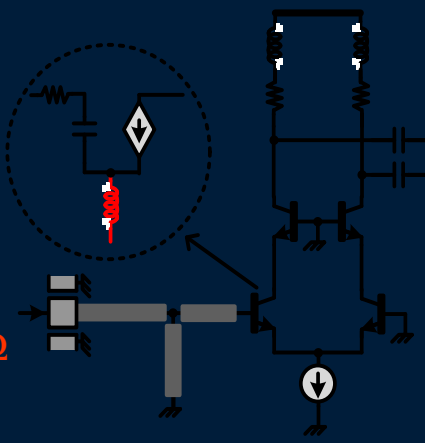
~40 dB overall measured gain

16-Element mm-wave phased-array Tx (44 GHz, schematic)



Active Balun

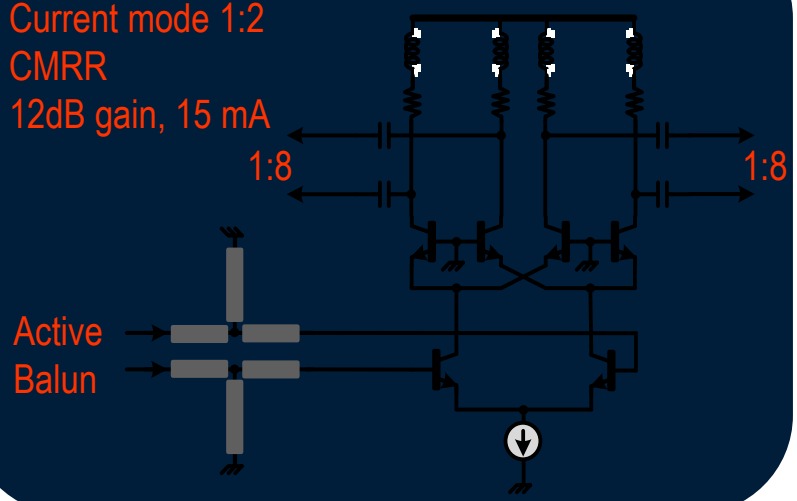
include parasitic L (EM sim)



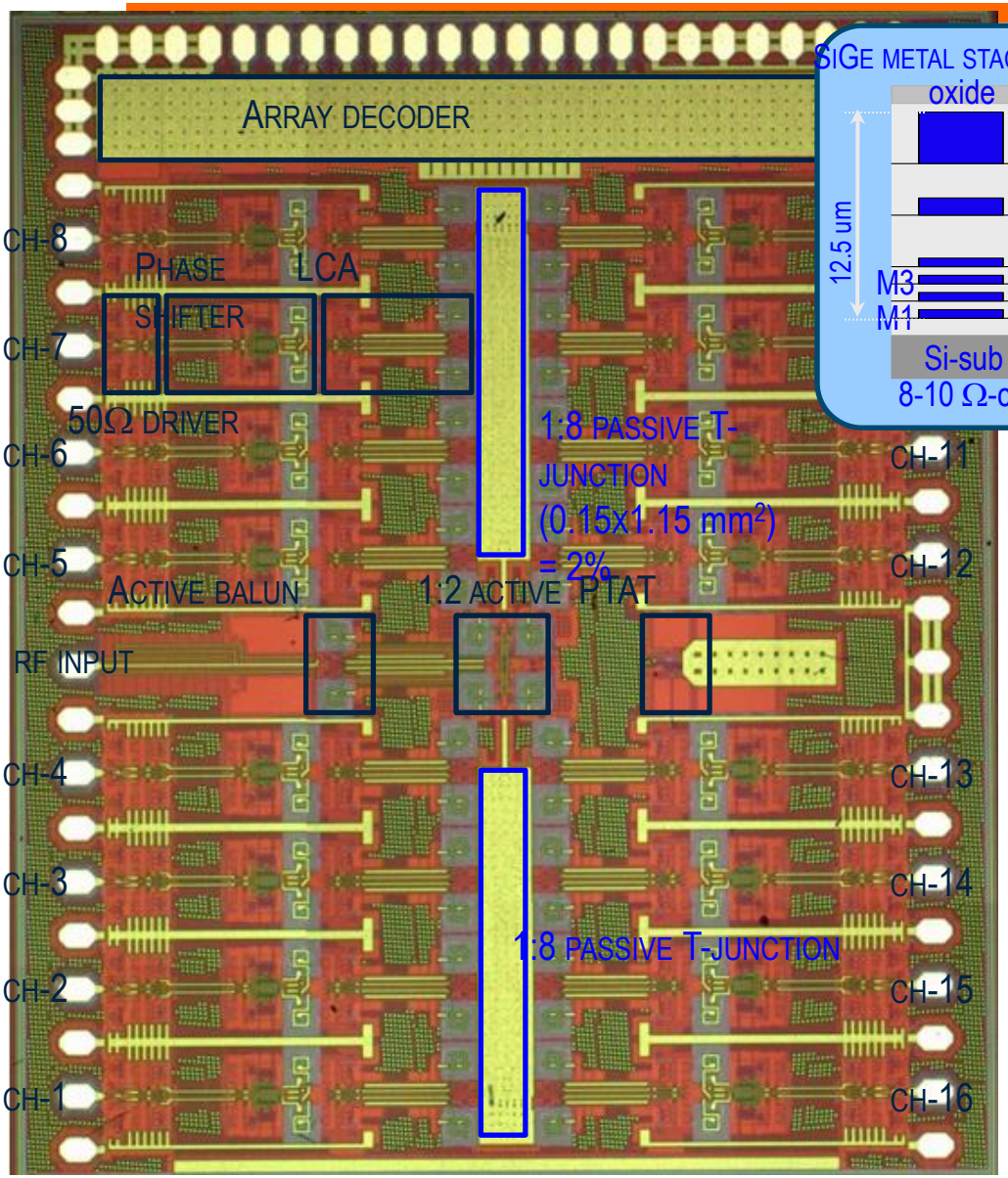
- Emitter-coupling
- Stub-matching: 50Ω
- 6dB gain, 5 mA

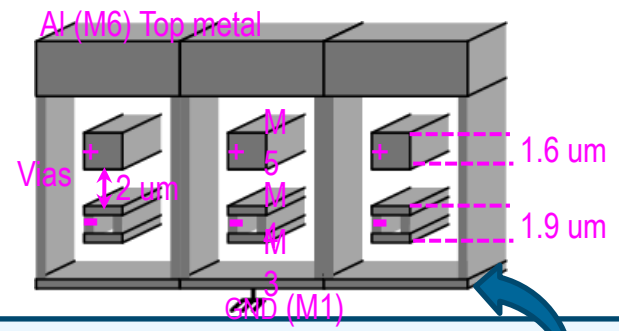
1:2 Active Divider

- Current mode 1:2
- CMRR
- 12dB gain, 15 mA

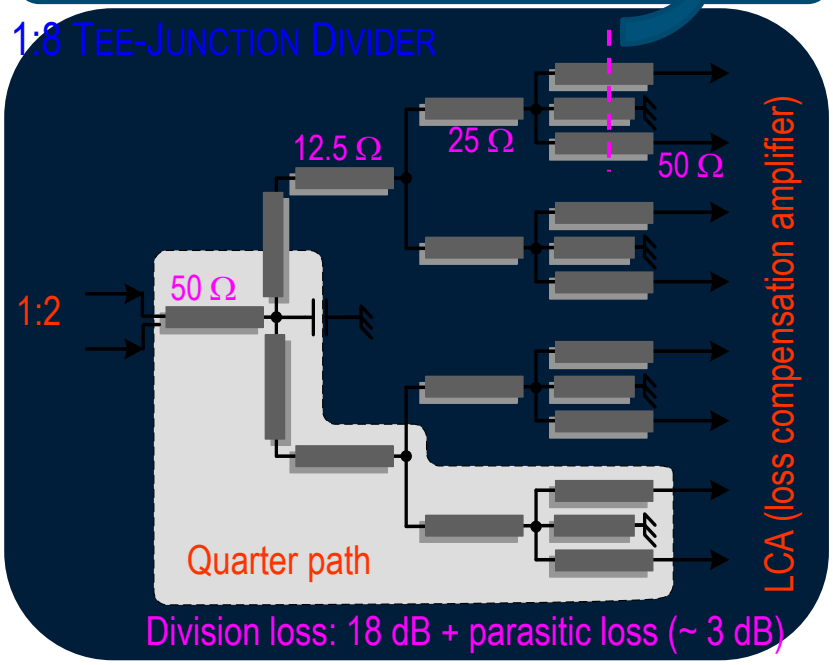


16-ELEMENT mm-WAVE PHASED-ARRAY TX (44 GHz, 1:8 T-JUNCTION)

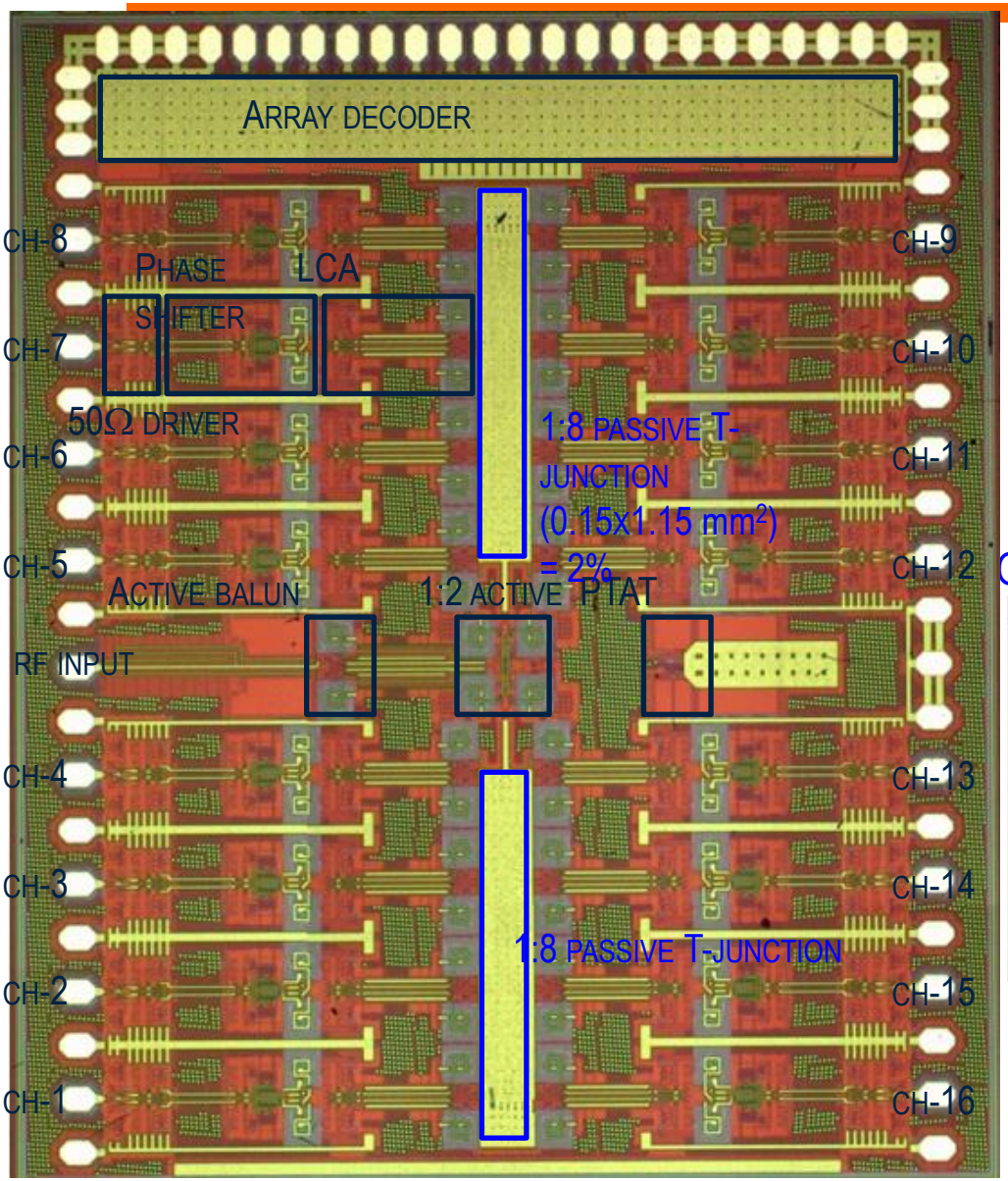




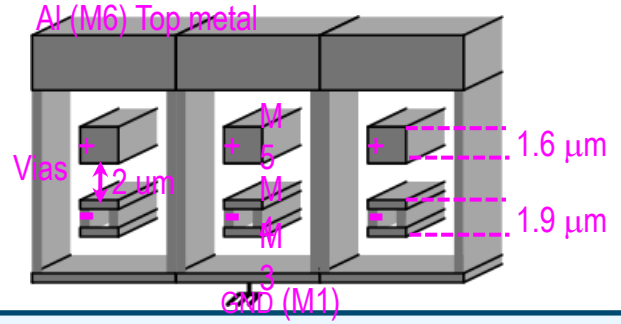
- Perfectly shielded (no coupling btw T-lines)
- Allow compact integration of many diff T-lines



16-ELEMENT mm-WAVE PHASED-ARRAY TX (44 GHz, COAXIAL T-LINE)

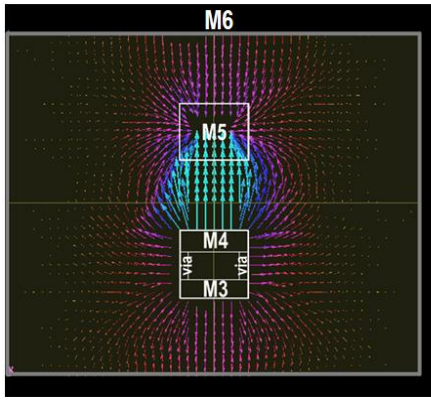


SHIELDED BROADSIDE-COUPLED DIFF-T-LINE

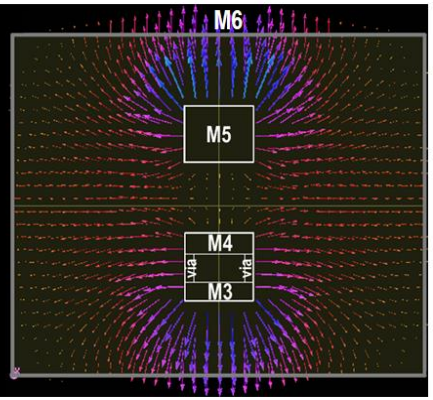


- Perfectly shielded (no coupling btw T-lines)
- Allow compact integration of many diff T-lines

ODD-MODE E-FIELDS

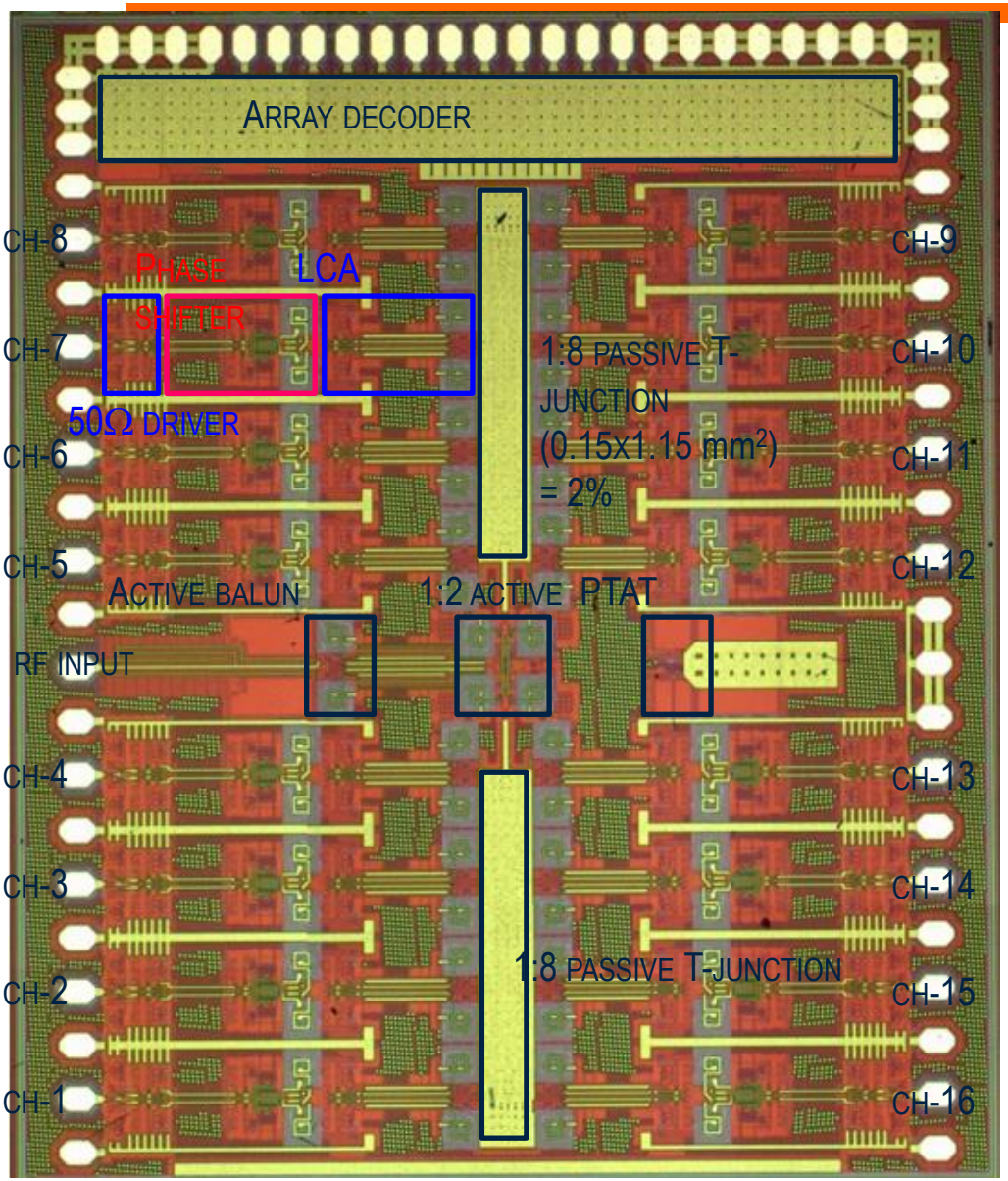


EVEN-MODE E-FIELDS

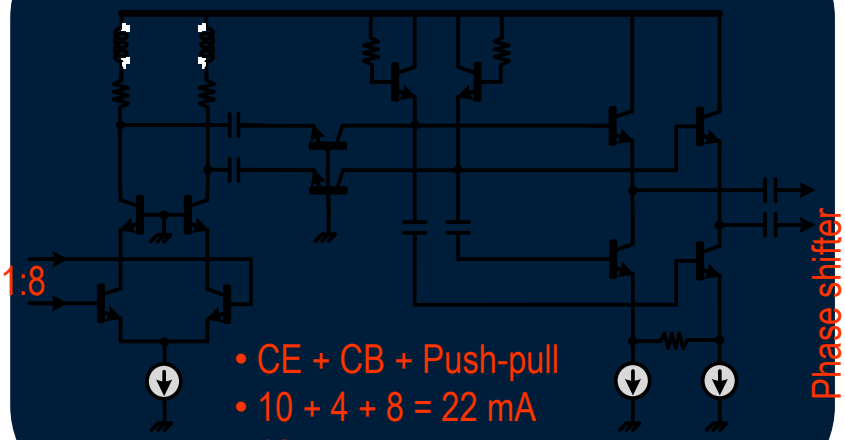


- W=3 µm: odd-mode impedance=50 Ω (HFSS sim)
- Most fields (> 95%) are confined btw diff-T lines
- Measured loss: 3 dB / 0.5 mm @45 GHz

16-Element mm-wave phased-array Tx (44 GHz, schematic)

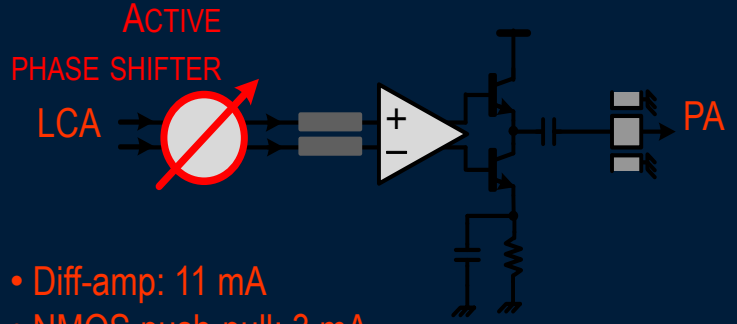


Loss Compensation Amp (LCA)



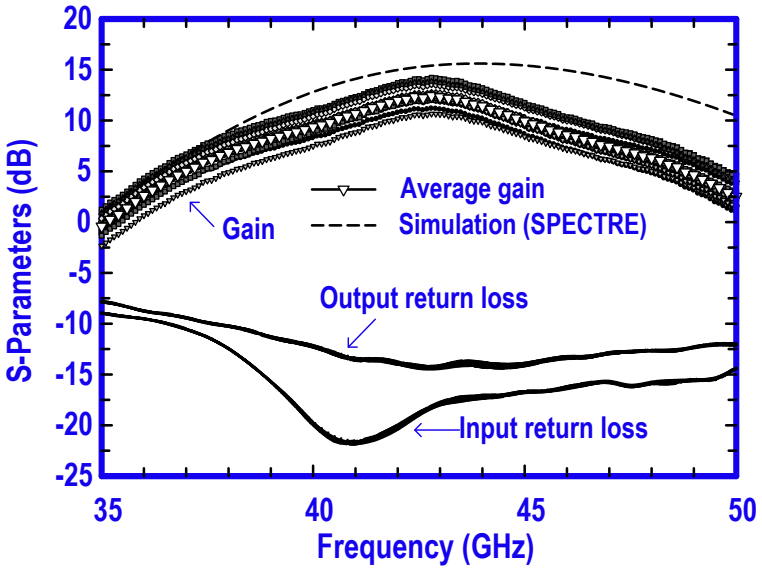
- CE + CB + Push-pull
- 10 + 4 + 8 = 22 mA
- 12 dB gain

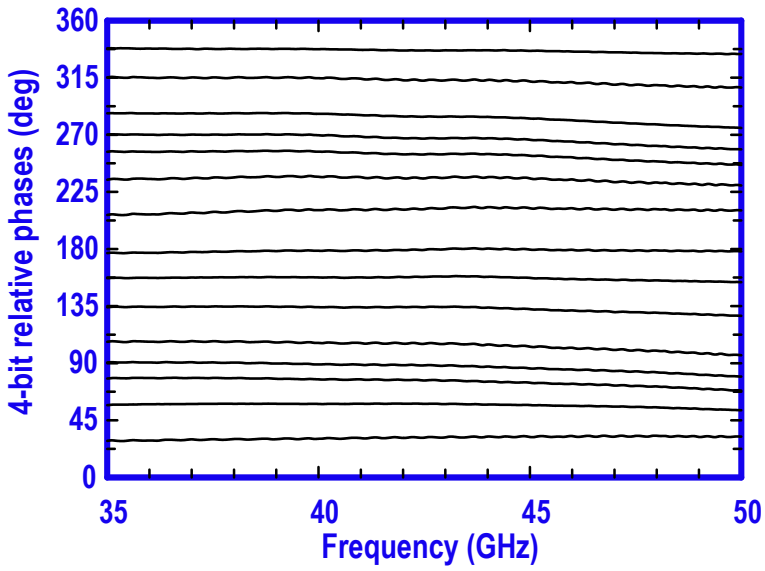
50Ω Driver

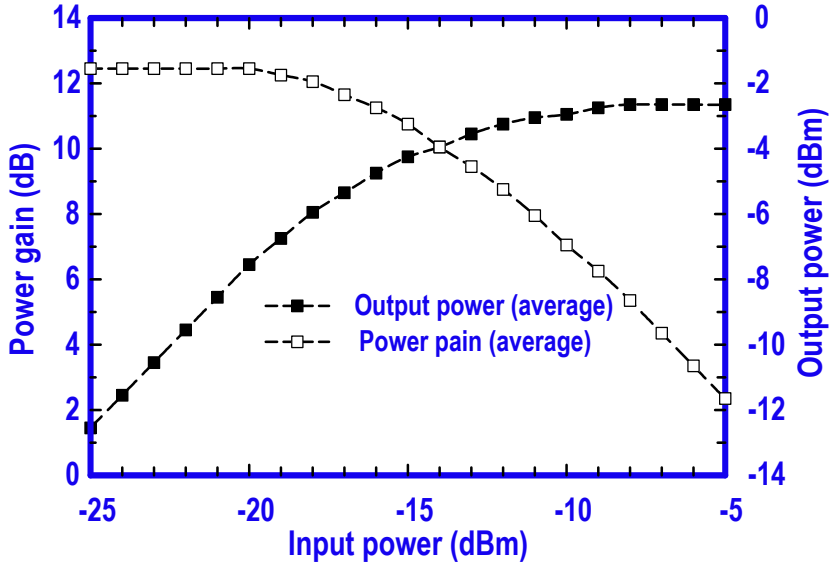


- Diff-amp: 11 mA
- NMOS push-pull: 3 mA
- Wideband 1/gm matching (S11< -10dB, 36-54 GHz)

16-ELEMENT mm-WAVE PHASED-ARRAY TX (44 GHz, MEASUREMENT)



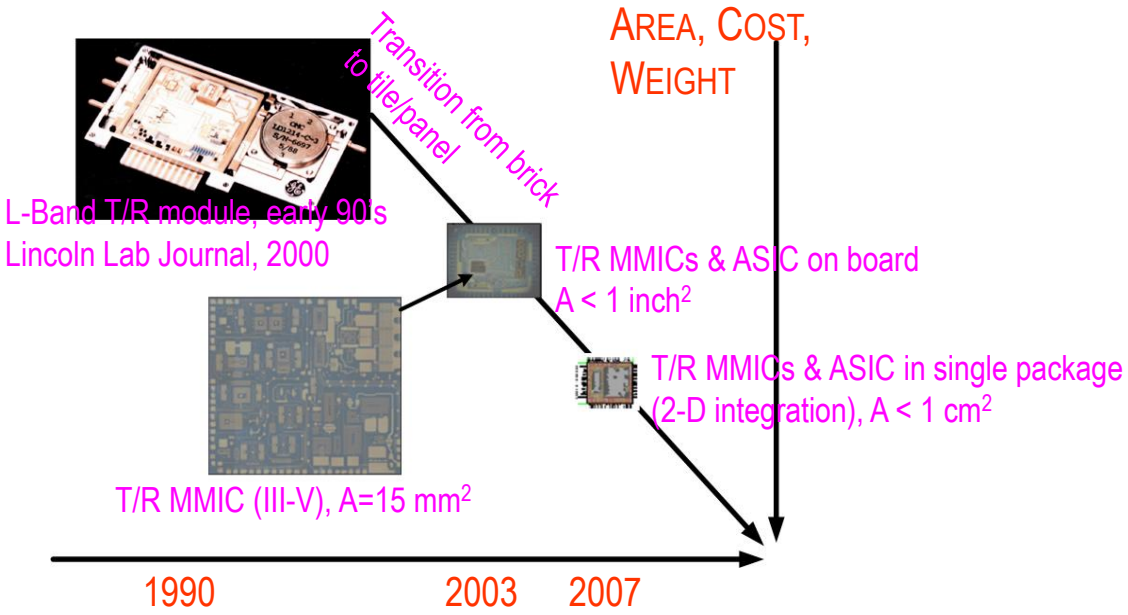




- Power gain: 12.5 dB @42.5 GHz
- RMS gain variation < 1.3 dB @30-50 GHz
- 3-dB BW: 40-45.6 GHz
- S11 < -10 dB @36.6-50 GHz
- S22 < -10 dB @37.6-50 GHz
- RMS phase error < 8.8° @40-50 GHz
- P_{sat}: -2.5 ± 1.5 dBm (for all phase states) @42.5 GHz
- OP_{1dB}: -5 ± 1.5 dBm @42.5 GHz

16-ELEMENT mm-WAVE PHASED-ARRAY TX (CHIP-SET TREND)

EVOLUTION OF PHASED ARRAY CHIP-SET



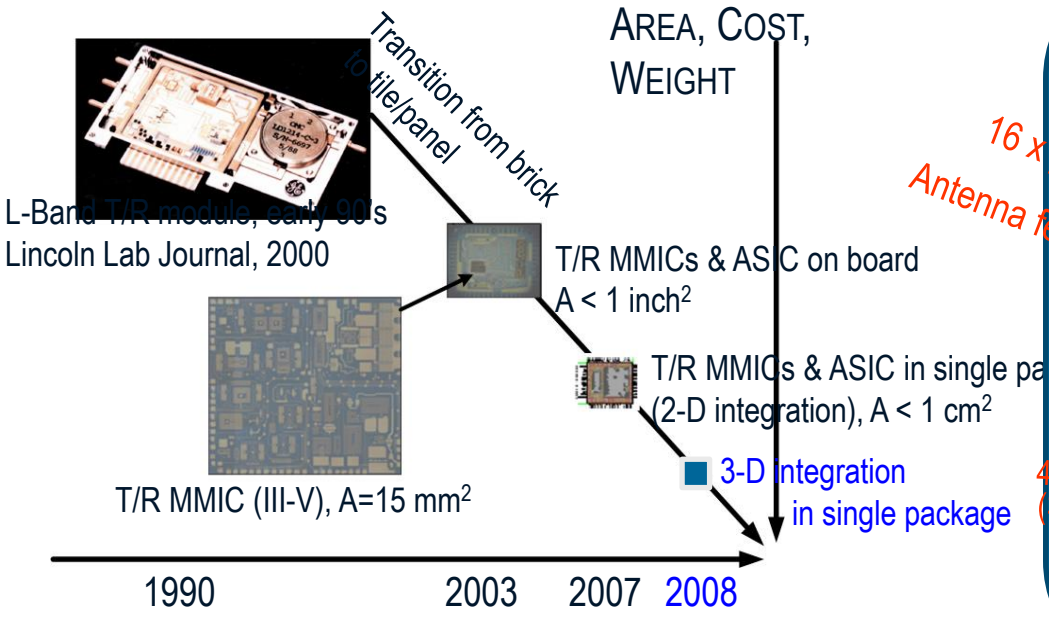
Ref: 2007 Multi-function phased-array RADAR Conference

- CERAMIC BOARD (packaged transistors, switches, phase shifters & AMP)
- CERAMIC BOARD (T/R MMICs & signal processor)
- SINGLE PACKAGE (2-D integration)

CURRENT TECH

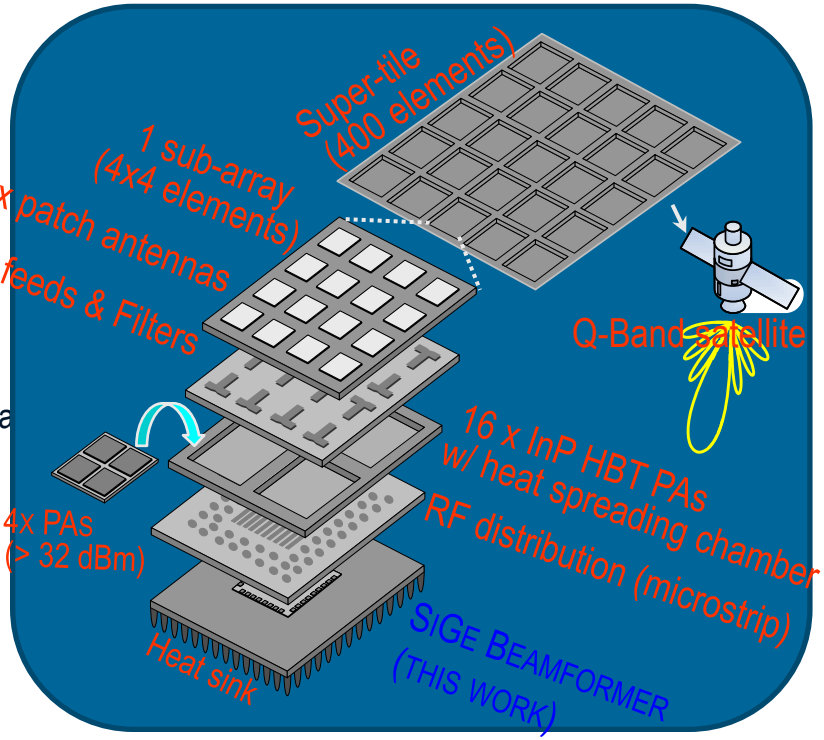
16-ELEMENT mm-WAVE PHASED-ARRAY TX (LARGE ARRAY, 3-D INTEGRATION)

EVOLUTION OF PHASED ARRAY CHIP-SET



Ref: 2007 Multi-function phased-array RADAR Conference

MULTI-LAYER 3-D INTEGRATION



- CERAMIC BOARD (packaged transistors, switches, phase shifters & AMP)
- CERAMIC BOARD (T/R MMICs & signal processor)
- SINGLE PACKAGE (2-D integration)

CURRENT TECH

- SINGLE PACKAGE (3-D integration)

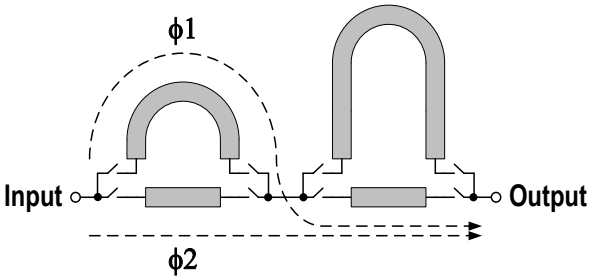
FUTURE TECH

MICS

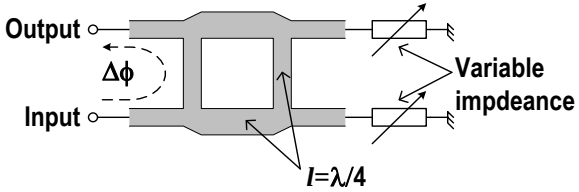
TYPICAL PASSIVE PHASE SHIFTERS (TOPOLOGIES)

T-LINE APPROACHES

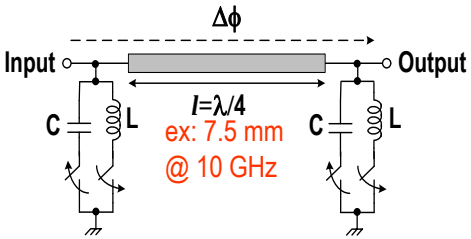
1. Switched T-lines



2. 90° branch-line hybrid coupler

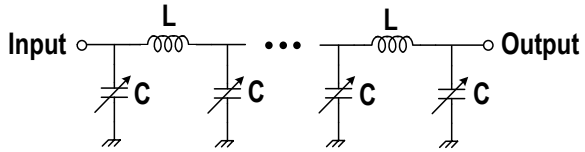


3. Periodic loaded line

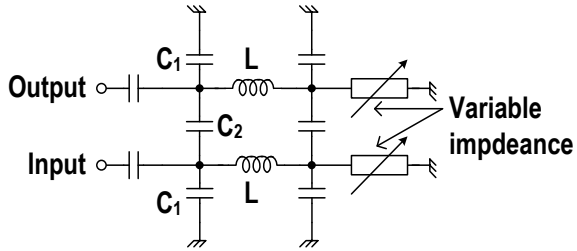


LUMPED PASSIVE APPROACHES

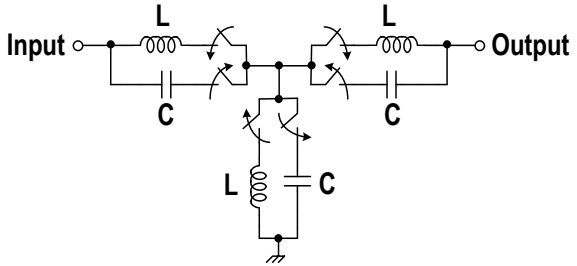
1. Lumped synthetic T-lines



2. Lumped hybrid coupler

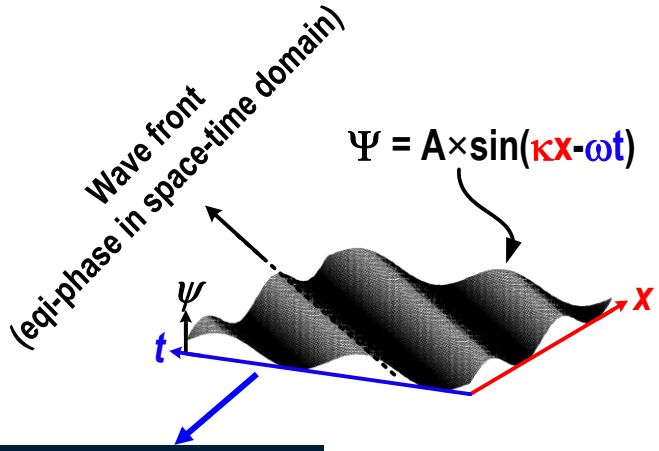


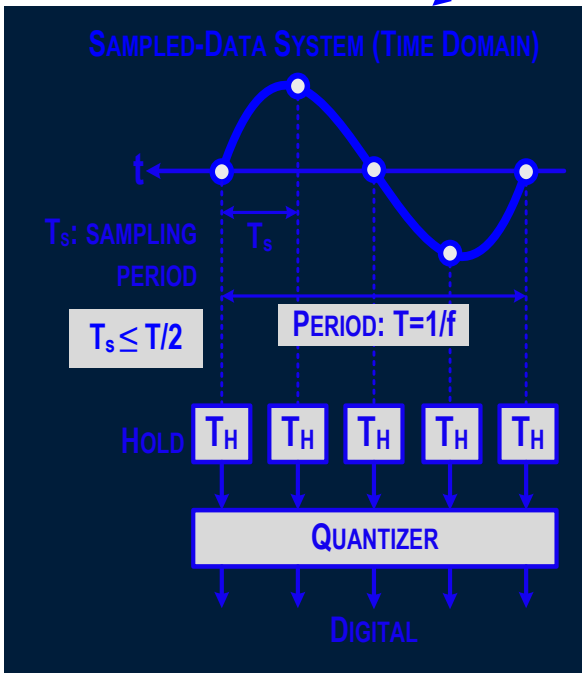
3. LPF / HPF approach



ISSUES: Chip area, Loss, Nonlinear control

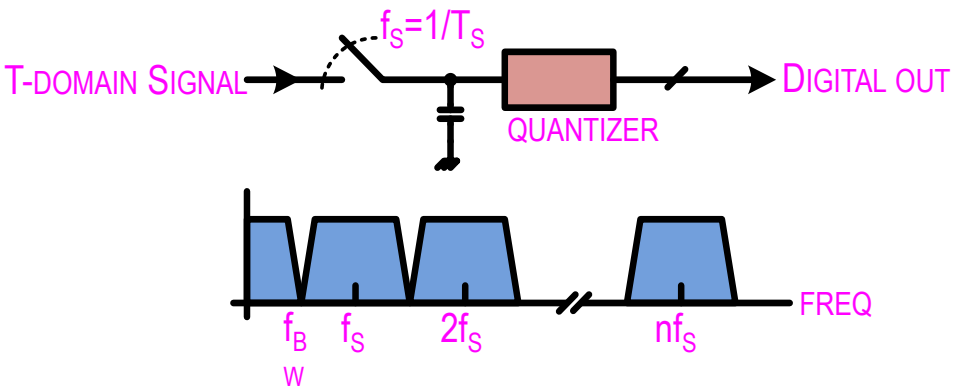
SAMPLING @ TIME-DOMAIN



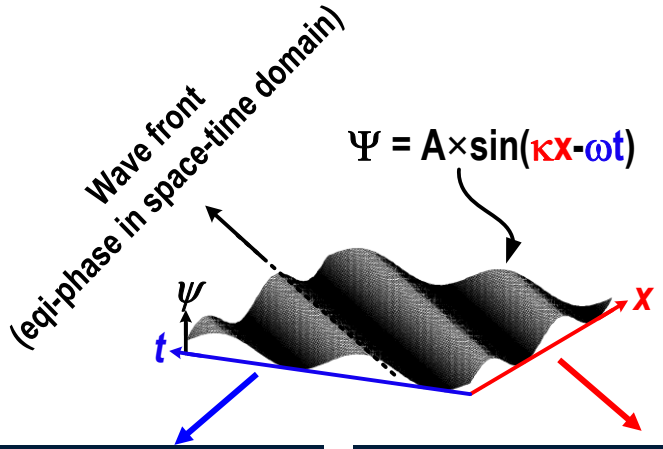


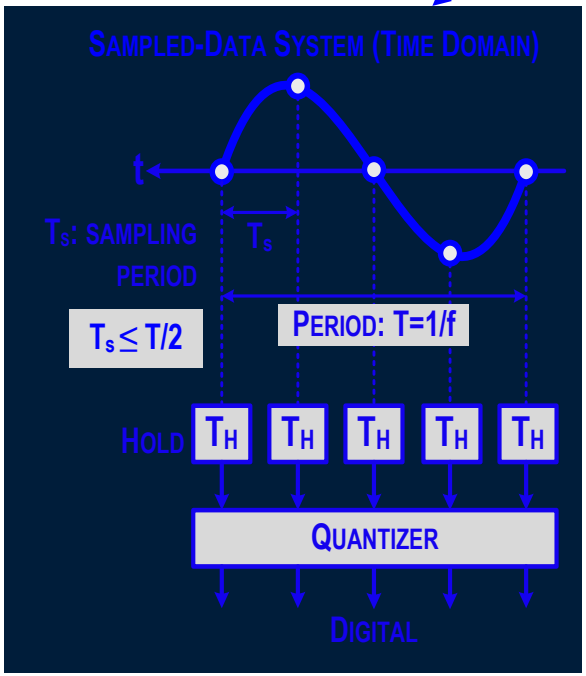
SAMPLE & HOLD (ADC)

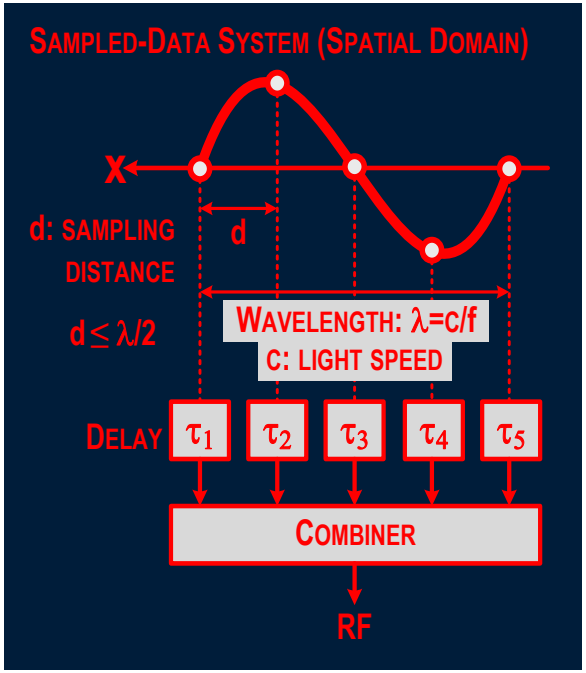
- Time-domain sampling
- T_s < Nyquist rate
  - ↳ Aliasing
- Need hold time, T_H, to quantize



SAMPLING @ SPACE-DOMAIN







SAMPLE & HOLD (ADC)

- Time-domain sampling
- T_s < Nyquist rate
  - ↳ Aliasing
- Need hold time, T_H, to quantize

PHASED-ARRAY (MULTI-ANTENNA)

- Space-domain sampling
- d < Nyquist distance
  - ↳ Aliasing ("Grating lobe")
- Need τ to in-phase ("Select")
  - or to out-of-phase ("Reject")

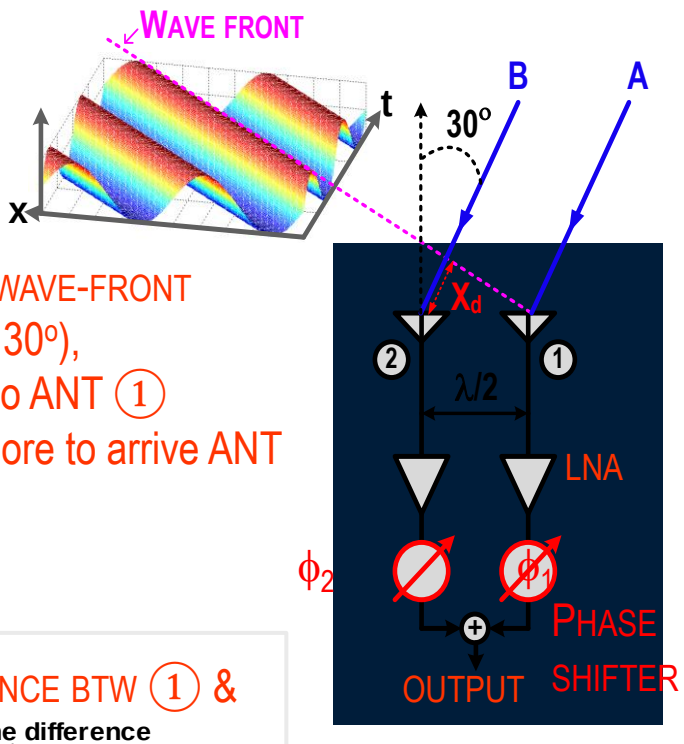
TIME

$$\omega = \frac{2\pi}{T}$$

SPACE

$$k = \frac{2\pi}{\lambda}$$

2-ANTENNA ARRAY (2-POINT SAMPLING, INTUITIVE)



FOR THE SAME WAVE-FRONT (incident angle: 30°),

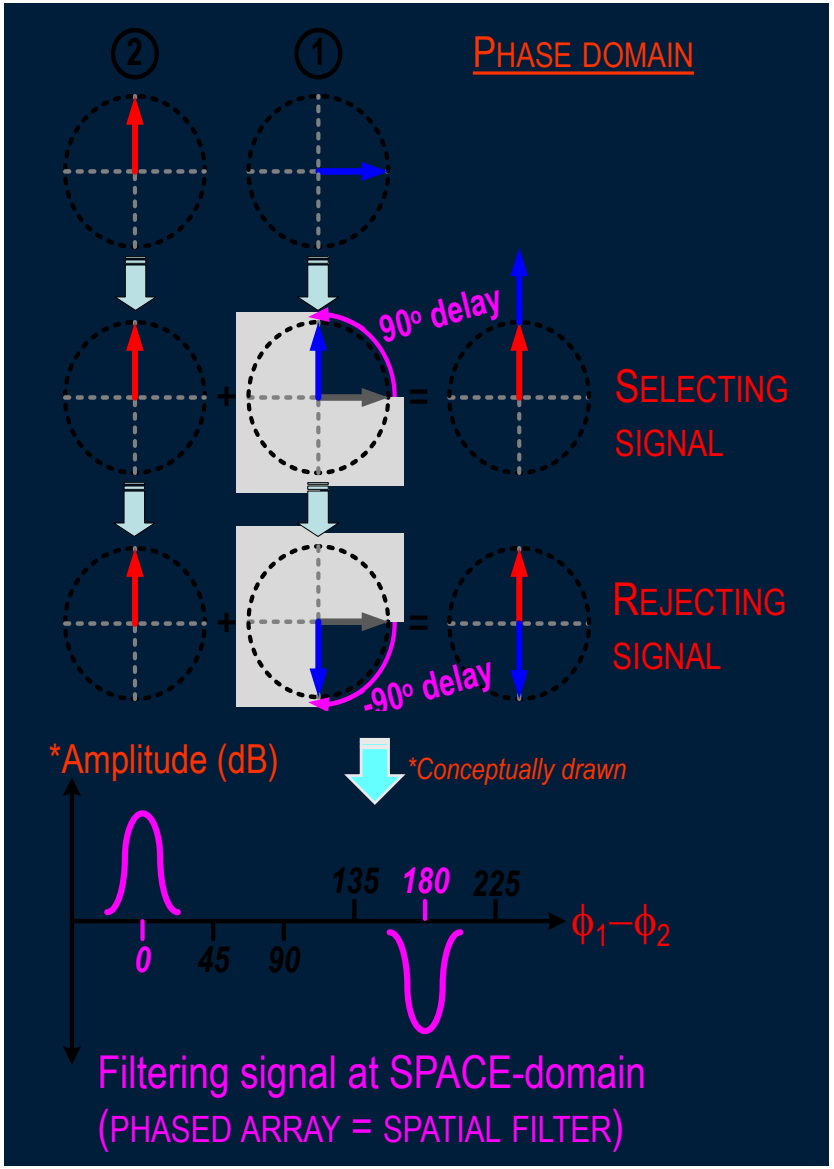
- A arrives first to ANT ①
- B travels X_d more to arrive ANT ②

PHASE DIFFERENCE BTW ① & ②

Arriv altime difference

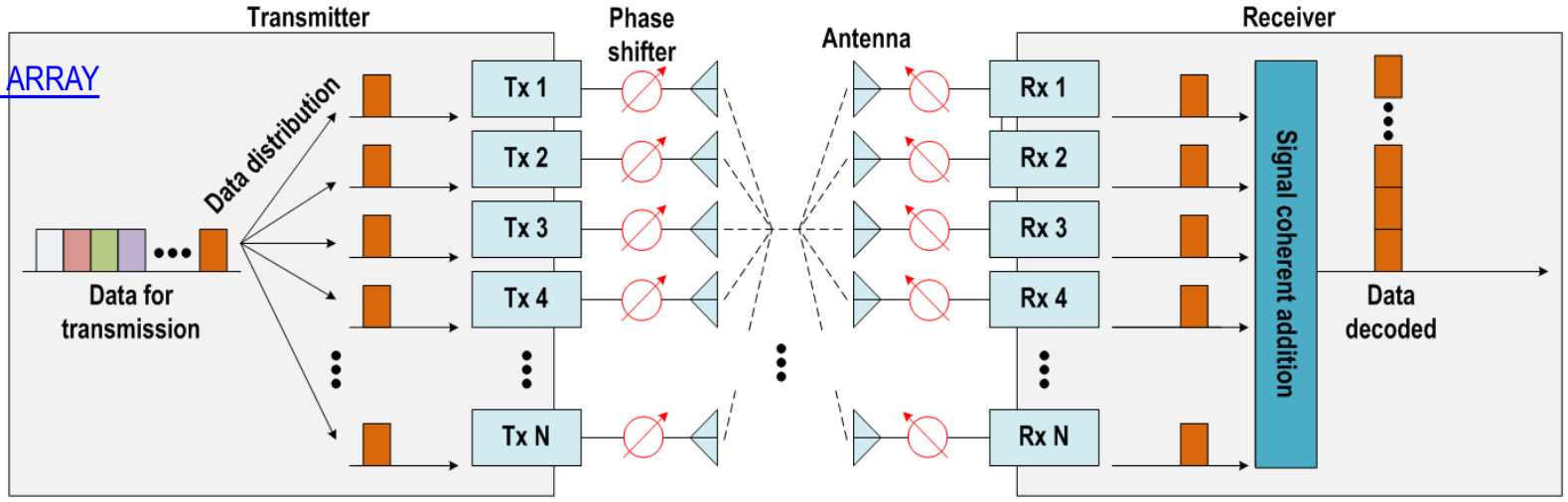
$$\phi_d = \underbrace{\frac{\lambda}{2} \times \sin 30^o}_{\text{Distance } (X_d)=\frac{\lambda}{4}} \times \frac{1}{c} \times 2\pi f$$

$$= \pi \times \sin 30^o = 90^o$$

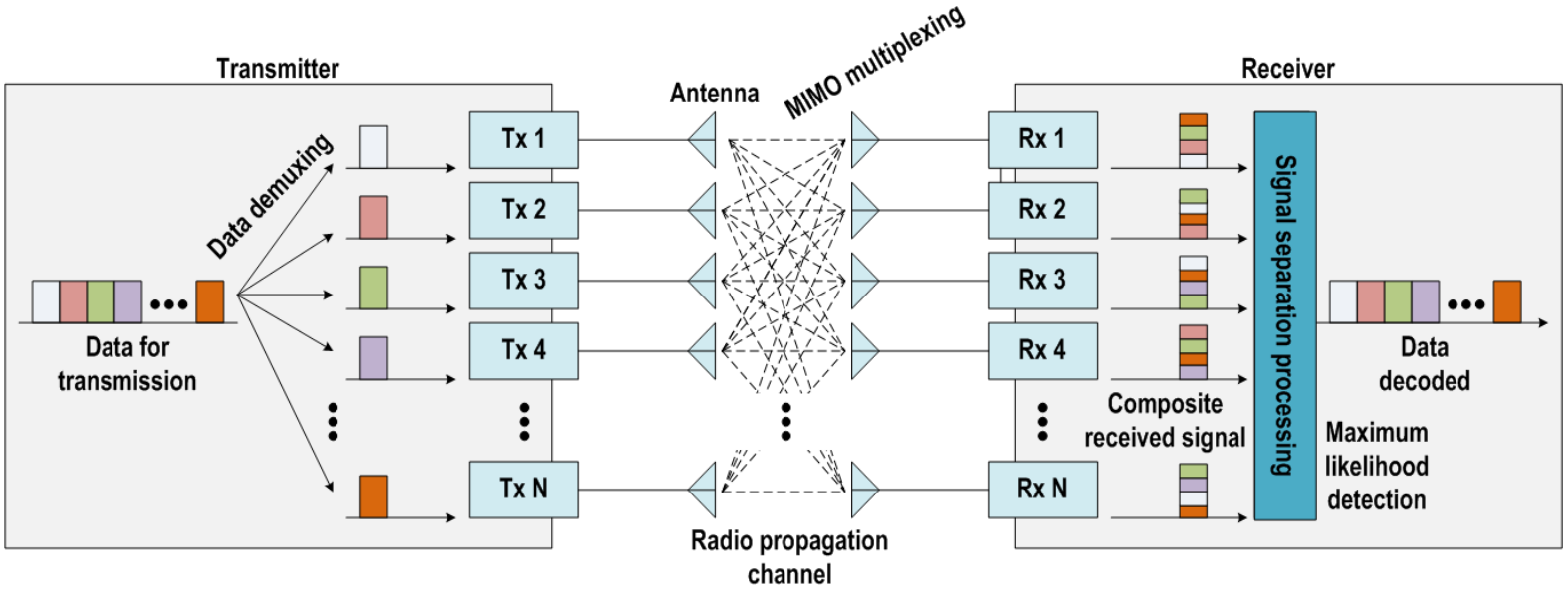


PHASED ARRAY V.S. MIMO (1)

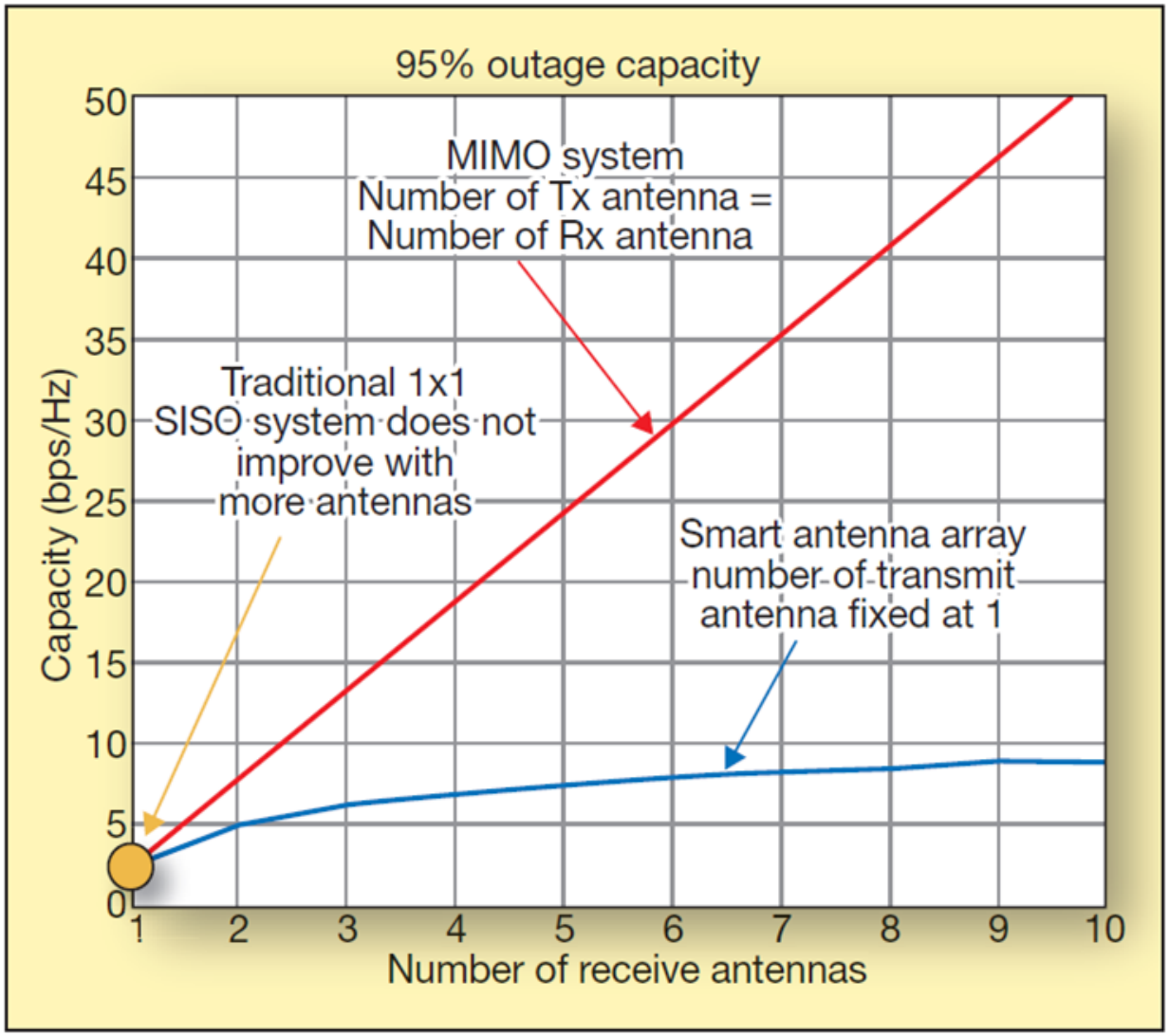
PHASED ARRAY



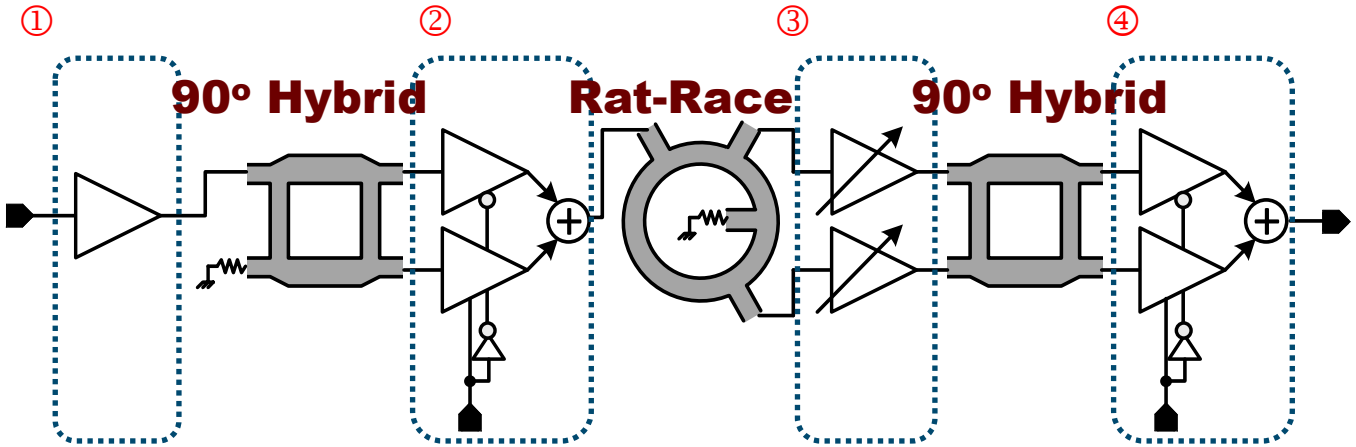
MIMO

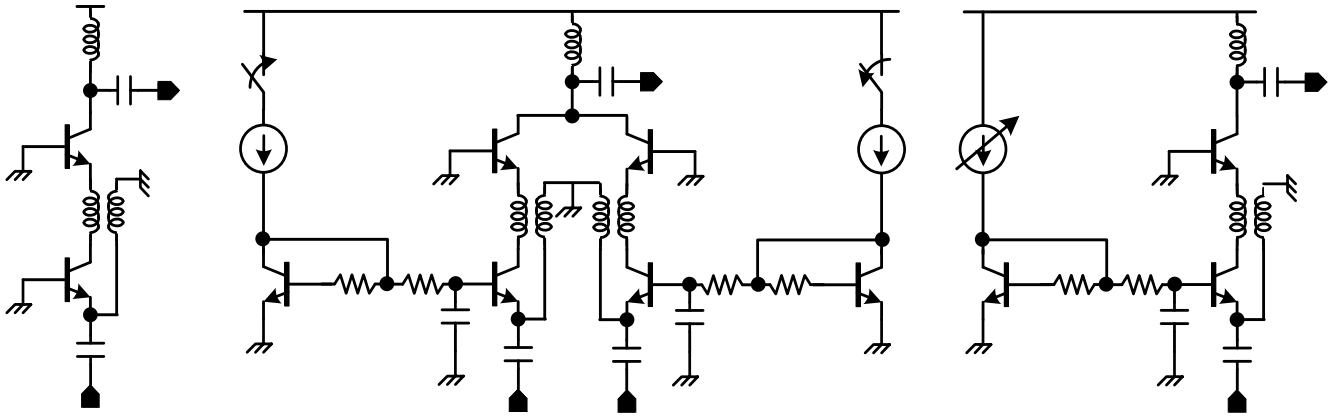


PHASED ARRAY V.S. MIMO (2)



Vector-Summing Phase Shifter (90◦ hybrid coupler)





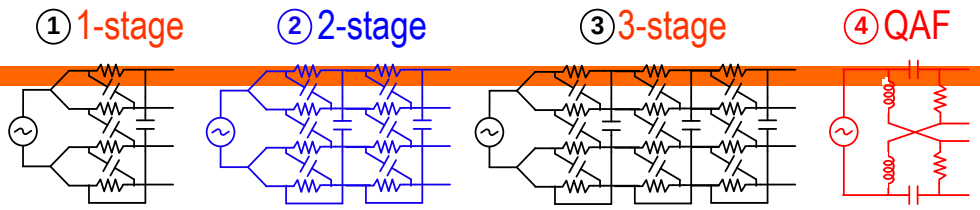
①: LNA

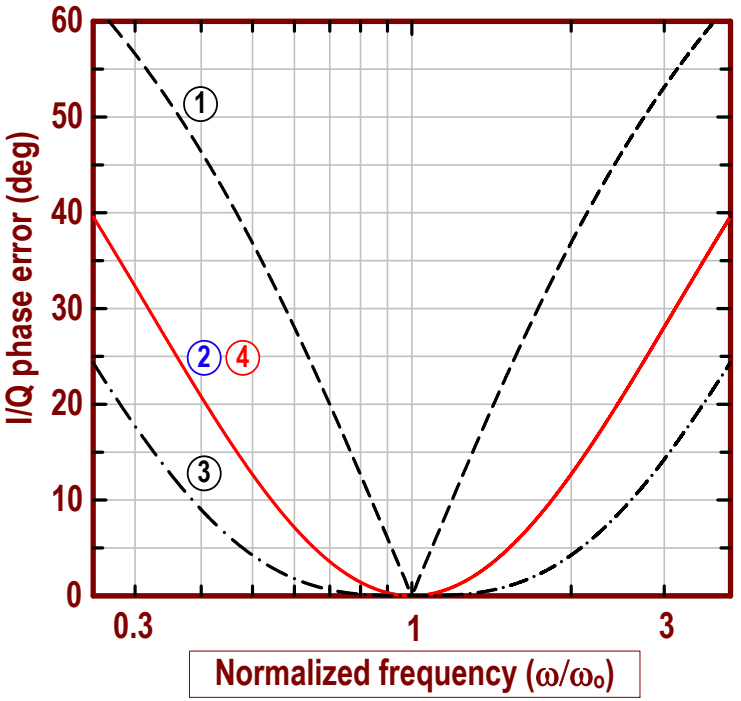
②&④: Switch Amplifier (functioning as an active switch)

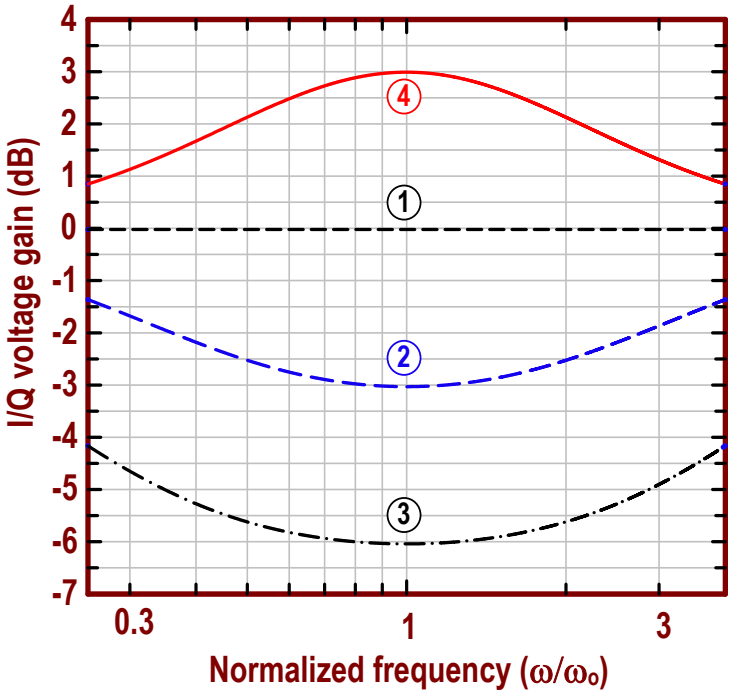
③: VGA

- The operating principle of an active phase shifter is to vary the amplitudes of two orthogonally-phased input signals to get the desired phase at the output.

Vector-Summing Phase Shifter (Quadrature all-pass filters)







- Exactly the same I/Q phase performance as the 2-stage polyphase filter
- 6 dB larger voltage gain than the 2-stage polyphase filter

Phased Arrays versus Timed Arrays