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A 28.5GHz Monolithic Cascode LNA with 70GHz f_T SiGe HBTs

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Abstract:

This paper presents the design and experimental results of a monolithic cascode LNA for 28.5GHz applications using SiGe HBTs. It shows that designing circuits at frequencies beyond $f_T/3$ is possible. The best experimental results are obtained at 26GHz with a 3.3V supply voltage: $|S_{21}|$ = 10.4dB, input and output matching better than –10dB. The measured noise figure is 6.4dB.

1. Introduction

In the last decade, silicon based MMICs have been gradually found place in the low microwave range (2-3GHz), due to lower processing cost than GaAs [1]. At higher frequencies, SiGe HBTs are also finding their place, due to their higher f_T, despite the lower performance of passive components. A reported LNA with *NF* = 3.8dB at 16GHz [2], receiver front-ends at 23GHz with LNA having *NF* = 4.3dB [3] and at 24GHz having *NF*=9.0dB [4] show that SiGe processes are also entering the low millimeter wave band.

This paper presents the design of a 28.5GHz LNA with SiGe HBTs from a 0.25μm BiCMOS process [5]. Although this technology was optimized to operate at a decade lower than the current application, results at 30GHz [6] show its ability to operate also in the lower millimeter wave band, mainly due to reasonable quality factors of the passive components. The target frequency is close to half of the peak f_T (70GHz) of the active devices.

Section 2 presents the LNA design, where the adequate active device and input and output port matching are presented. Section 3 discusses the experimental measurement results and conclusions are made in section 4

2. LNA Design

The LNA was designed for 28.5GHz applications. The technology used was the 0.25μm BiCMOS process from Philips [5]. This process provides SiGe HBTs with peak f_T/f_{max} of 70/100GHz, MIM capacitors and spiral inductors with reasonable *Q*-factor up to a few GHz due to the 3μm thick top metal layer. At high frequencies, close to the low millimeter wave band, it is possible to obtain inductors with *Q*-factors close to 20 [5].

2.1 Active Device

LNA applications require an active device with a low base resistance to have a low minimum noise figure (NF_{min}). The optimum configuration for this purpose is an HBT with double base contact and minimum emitter width (0.5μm). The minimum and maximum emitter lengths for standard devices are 1μm, and 20.7μm.

The optimum current density for minimum noise figure was found, by simulation, to be 0.2mA/μm^2. The optimum current density for G_{MAX} is slightly higher. At 28.5GHz the shortest emitter length provides the lowest NF_{min} (2.9dB) and G_{MAX} (less than 3dB) and an equivalent noise resistance close to 500Ω. An emitter length of 20.7μm provides the highest NF_{min} (3.6dB) and G_{MAX} (9.6dB) and an equivalent noise resistance closer to 50Ω. The cascode configuration uses two devices with the same emitter geometry of 20.7μm. Simulation of this structure showed NF_{min} = 4.5dB and G_{MAX} = 17.9dB at 28.5GHz with 2.4mA collector current. The value of G_{MAX} is close to twice G_{MAX} of each device.

2.2 Input port matching

To have a good input matching with low noise figure two possible solutions were considered: a series feedback

emitter inductor and an LC input matching network as presented in figure 1.

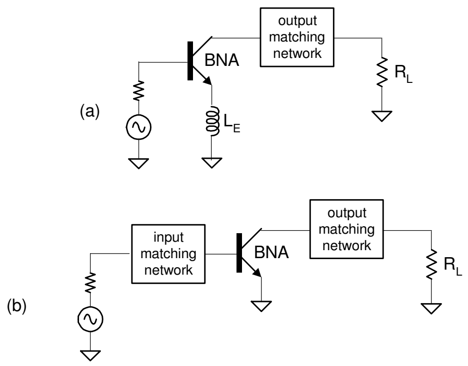

Figure 1: Input port matching: (a) emitter inductor; (b) input matching network.

Including an emitter inductor changes the active device input impedance to near 50Ω without significantly increasing the active device noise figure [7]. Accordingly, no input matching network is needed. Figure 2 shows the noise figure (NF), G_{MAX} and $|S_{11}|$ variation with the emitter inductor value. With 60pH inductor G_{MAX} = 15.7dB, $|S_{11}|$ = –10.2dB and NF = 4.8dB (NF_{min} ≈ 4.6dB). However, this inductor value is too low to implement in the targeted process. A realistic value of 100pH or more improves input matching, while NF is kept in 4.8dB, but decreases G_{MAX} to less than 15dB.

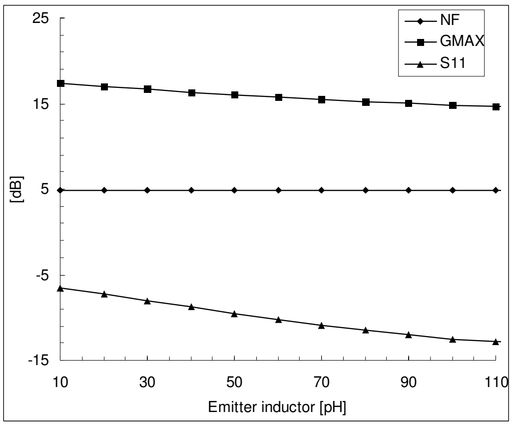

Figure 2: Noise figure (NF), G_{MAX} and $|S_{11}|$ variation with the emitter inductor.

Figure 3 shows the constant noise and available gain circles to evaluate the alternative input matching network for the cascode. A source admittance y_S = 1+j0.8 provides an available gain of 17.5dB (0.4dB lower than G_{MAX}) and a NF of 4.9dB (0.4dB higher than NF_{min}). The input return losses are better than 10dB. The input matching network is obtained by placing a simple 320pH spiral inductor in parallel with the 50Ω source impedance (i.e. y_S = 1+j0.8 @ 28.5GHz). The input port is AC coupled with a 10pF capacitor.

These results show that for similar noise figure and input matching, a higher gain is obtained with these active devices when using input parallel inductor.

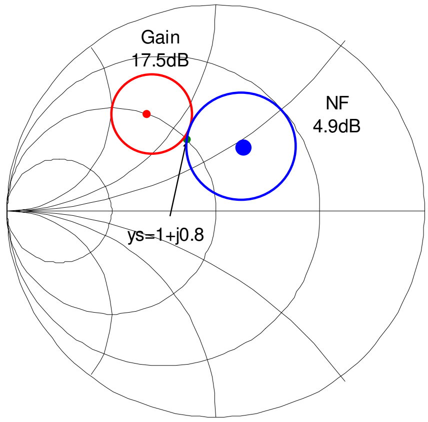

Figure 3: Constant noise and available gain circles for the cascode configuration.

2.3 Output port matching

The LNA with the input and output matching networks is presented in figure 4. Output matching is made by tuning the bias inductor L_O with the capacitive divider C_{O1} and C_{O2}.

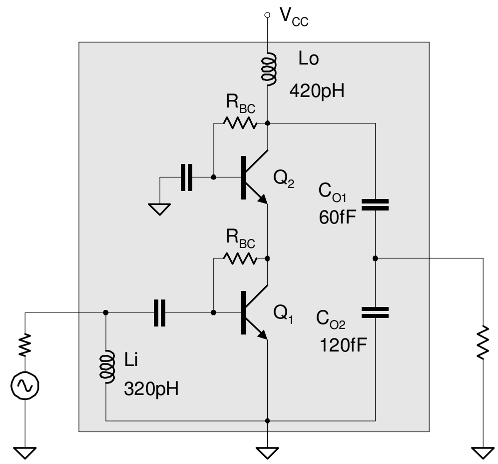

Figure 4: Cascode LNA circuit.

2.4 LNA Simulations

To accurately simulate the LNA, the ideal components of figure 4 circuit were replaced with dedicated process RF components models. The two 40kΩ base-collector resistors R_{BC} were implemented with poly resistors. AC coupling capacitors (input port and Q_2 base grounding) are MIM structures with 2pF (W=25µm, L=16µm for low series resistance). The capacitors in the output matching network are also MIM (two 120fF capacitors in series were used to obtain 60fF).

The 320pH and 420pH inductors were realised as two turn, top-metal only octagonal inductors on a deep trench isolation grid. Their equivalent inductances at DC were 350pH and 500pH, respectively. Both inductors have a quality factor close to 20 at 28.5GHz.

Small-signal simulations of the cascode LNA were performed. The results for S parameters and noise figure are shown in figure 5. The circuit was biased with V_{CC} = 2.7V, I_C = 2.4mA. At 28.5GHz, the LNA shows return losses better than 10dB, $|S_{21}|$ = 12.6dB and NF = 4.9dB.

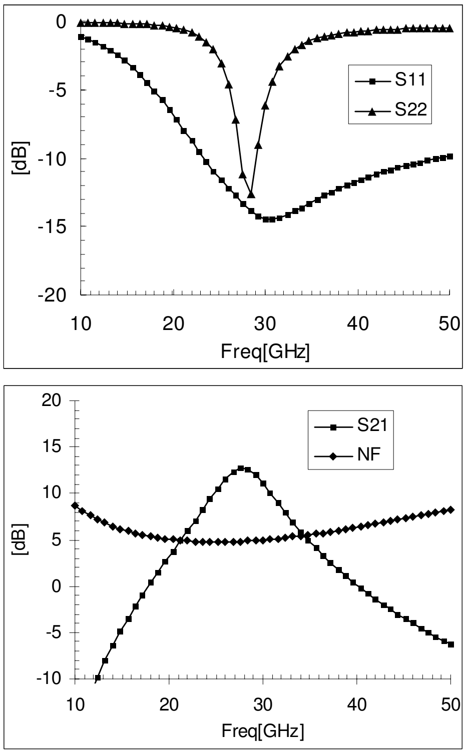

Fig. 5: LNA simulated performance: input and output return losses, gain and noise figure.

Including input and output port pads in the simulation reduces the gain from 12.6dB to 11.4dB. Noise figure is increased from 4.9dB to 5.4dB. Good input and output matching is maintained.

3. Experimental Results

Figure 6 shows the chip photograph of the fabricated LNA prototype. Special care was taken with ground connections, mainly the substrate grounding, by spreading as much metal with p-sub taps as possible. The signal path connections were kept as short as possible to minimise parasitic inductors / transmission lines.

For experimental evaluation, bond pads were added to input and output ports to allow on-wafer probing. They were placed as GSG (Ground-Signal-Ground) RF probes with a pitch from 125µm to 150µm. The total die area is 350µm x 390µm, including pads.

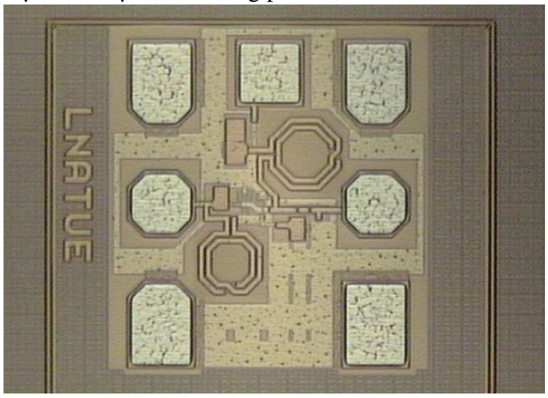

Fig. 6: cascode LNA chip photograph.

The measured bias current of the active devices was lower than expected, due to process spread. To compensate this, the supply voltage was increased to 3.3V to obtain the expected bias current.

Figure 7 shows the comparison between simulated and experimental noise figure. At 26GHz measured NF is 6.4dB with 3.3V. At the highest measured frequency (with 3.3V) the difference to simulated NF is close to 1dB. The NF is almost constant from 23 to 26GHz (the maximum measured frequency due to measurement set limitation) predicting a similar performance at 28.5GHz.

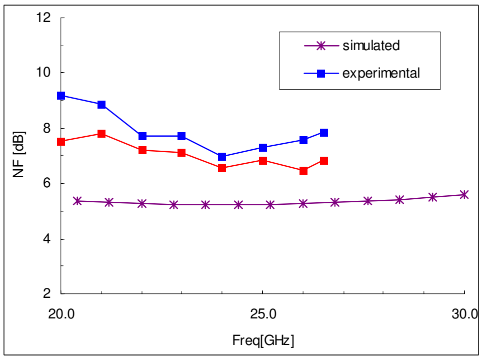

Fig. 7: Noise figure simulated/experimental comparison.

The comparison between measured and simulated S parameters magnitude is presented in figure 8. Simulations were made with a bias voltage of 2.7V, and measurements with 2.7V, 3.0V and 3.3V due to the reduced current at 2.7V, as previously mentioned.

The $|S_{11}|$ parameter has a minimum at 22GHz and it is lower than -10dB at 28.5GHz.

The $|S_{22}|$ parameter has a minimum at 25.4GHz. Although this frequency is different from the expected 28.5GHz, the curve shape is very similar. The cause for this frequency shift can be a higher inductor value than expected and additional parasitic not considered in simulation.

The frequency shift in $|S_{21}|$ parameter is directly related to $|S_{22}|$. It has a measured maximum value of 10.4dB at

25.6GHz, with 3.3V operation. The measured curve shape is also similar to the simulated one, as observed in $|S_{22}|$. At 28.5GHz it presents 5.7dB.

The measured reverse gain, $|S_{12}|$, is in reasonable agreement with the simulated one, considering its low value.

4. CONCLUSIONS

A 28.5GHz monolithic LNA design and experimental results using SiGe HBTs with 70GHz peak f_T was presented.

Experimental results present a minimum noise figure of 6.4dB and $|S_{21}|$ = 10.3dB at 26GHz for 2.4mA at 3.3V. The input and output return losses are not tuned at the target frequency but are better than 10dB. The differences between targeted 285GHz and measured 26GHz peak performance can be associated with the process spread and parasitic effects, which were wrongly considered in simulations.

The results indicate the possibility of using mature SiGe processes at the lower millimeter wave band, like a 0.25μm SiGe-BiCMOS optimized for lower frequency applications.

5. References

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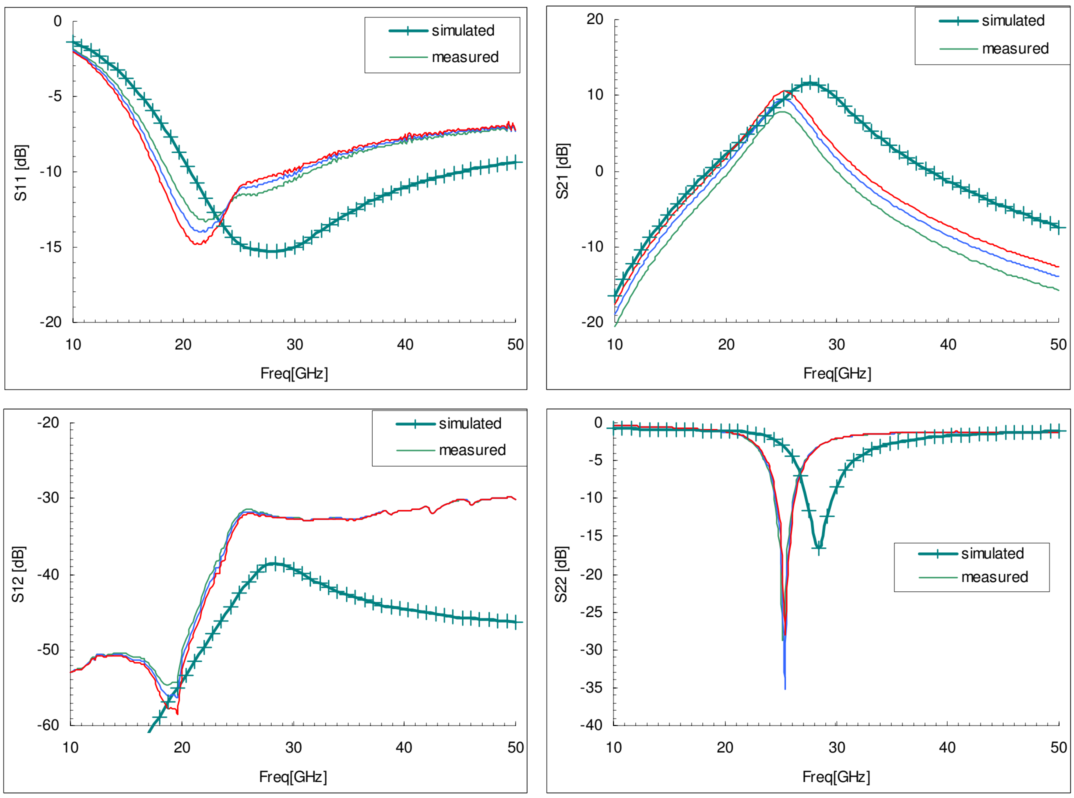

Fig. 8: S parameter simulation/measurement comparison. Top, middle and bottom measured curve is related to 3.3V, 3.0V and 2.7V supply voltage respectively.