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## **Sonnet Verification Kit for TowerJazz SBC18H Process Family Version 1.2**

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## Supported Technologies

This Sonnet verification kit is designed for simulation of passive components such as inductors and transformers in the TowerJazz SBC18H process family including SBC18HA, SBC18HX, SBC18H2 and SBC18H3 amongst others. The definitions for the Sonnet model file of conductivity, permittivity, dielectric and conductor thicknesses are current with the TowerJazz Process Specification NPB-PS-0267 rev17.

The Sonnet files apply to all SBC18H processes with 2.81um thick Al top metal and identical interconnect stackup as SBC18HX. The S-parameter measurements and GDSII layout data for the inductors used in this work were provided by TowerJazz.

Simulation of MIM capacitors is not supported at the present time, because the MIM layers are not included in the stackup.

## Design Flow Overview

The Sonnet EM simulator supports multiple design flows for this technology:

- Sonnet's Integration into Cadence Virtuoso
- Manual GDSII based layout data transfer with technology template file

This document describes the Sonnet template and mapping files that are available.

### ***Cadence Virtuoso & Agilent ADS Interfaces***

The Sonnet interfaces for Cadence Virtuoso and Agilent ADS use a \*.matl file which contain all the material definitions and layer mapping. No other files are required.

File name: SBC18H.matl

### ***GDSII template file and GDSII layer mapping file***

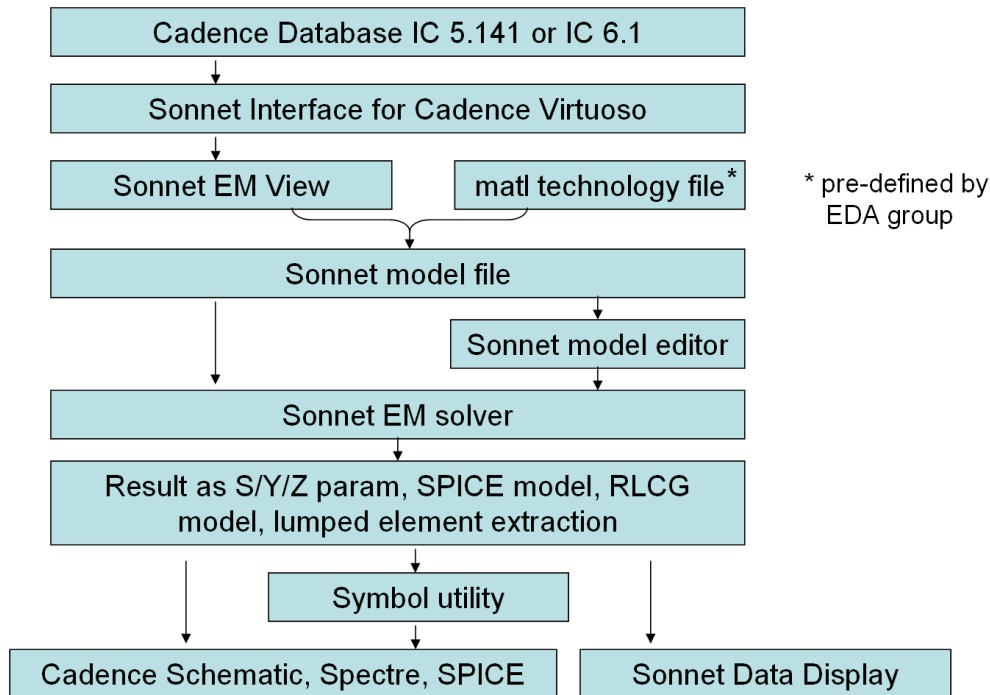
In the Sonnet editor, a "template" project file is used for GDSII import to provide default technology information (layers, materials) and simulation setup (frequencies and analysis settings). It is not required to use a template file, but it makes the analysis setup a lot easier if you do more than one analysis with the same technology.

File name: SBC18H.son

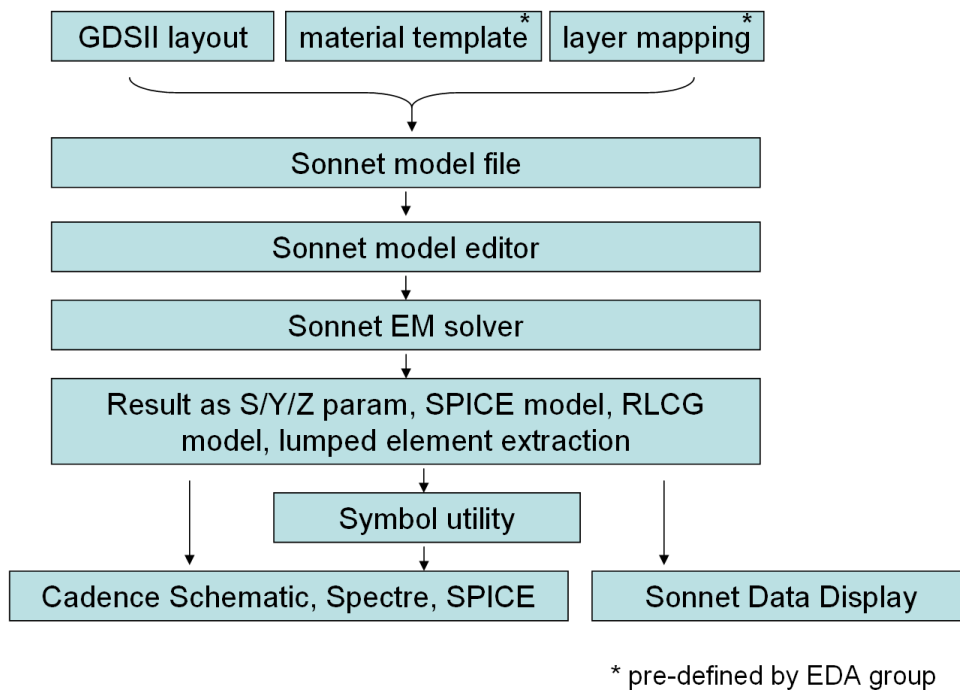
The layer mapping file is used to define how the layers in the GDSII file correspond to the levels in Sonnet. It is also used to assign materials from the template file to each layer.

File names: SBC18H.lay

## Design Flow Sonnet ↔ Cadence



## Design Flow GDSII → Sonnet → Cadence



# Known Limitations

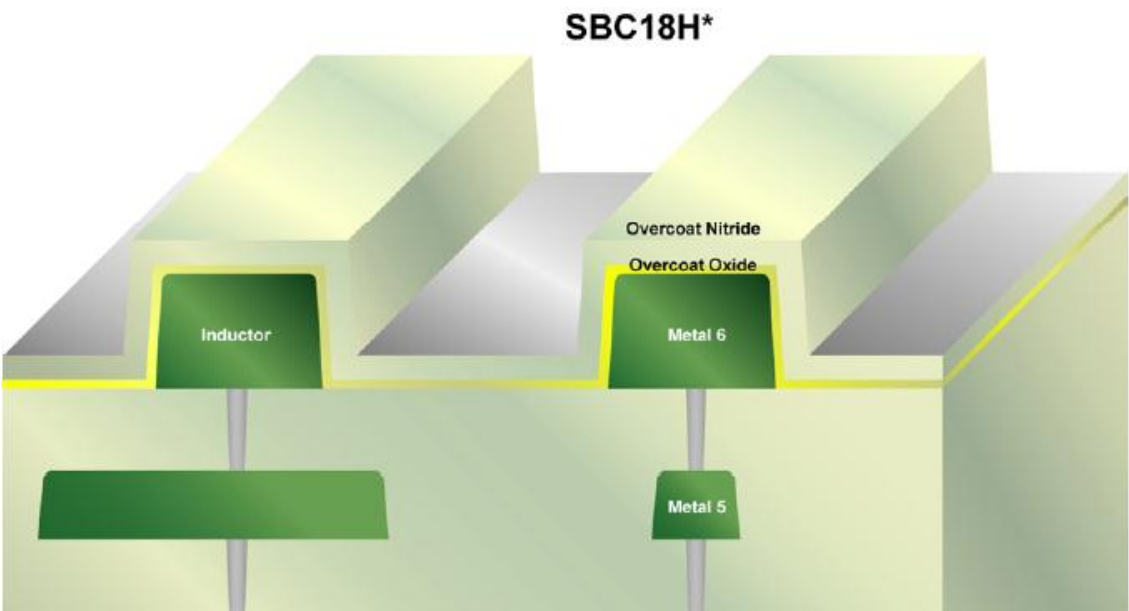
## 1. PWell block assumed

All substrate definitions are only valid for areas where a PWell block is placed. This is hard coded into the substrate definitions. The simulation does not check the presence of the PWell block in your layout.

## 2. Planar approximation

The Sonnet simulator solves the field problem for a planar structure. Whereas most of the back end structure is planarized and can be modelled very accurately, the top layer passivation is a conformal dielectric and the Sonnet model is only approximate.

Actual passivation as documented in the Process Specification NPB-PS-0267 rev17:



Planarized passivation as modeled in this Sonnet Verification Kit:

	2500um			air_above	er=1.00
0	0.6um			nitride_overcoat	er=7.00
1	0.2um			oxide_overcoat	er=4.20
2	2.81um	2.81um	metal6	3.389E7 S/m	at_metal6 er=4.20
3	2um		via5	below_metal6	er=4.20
4	1.59um	1.59um	metal5	3.495E7 S/m	at_metal5 er=4.20
5					

This simplified planar approximation is considered good enough for structure where most of the coupling is to the metal and substrate below, e.g. for wide lines. For metal in the metal6 layer that is closely spaced, the capacitance between the sidewalls is somewhat underestimated by the Sonnet thick metal algorithm, and the higher effective permittivity (due to the oxide over the full height) should partially compensate for that effect. In case of doubt, please check for yourself. One possible check would be to simulate with the minimum and maximum permittivity in this layer, and see how much results change for your actual layout.

We expect that line impedance for coplanar lines on metal6 is not precise, due to the simple planar modeling of the passivation. This effect has not been fully investigated, so we recommend running your own test for these applications.

One idea for a possible workaround, which has not been tested yet, might be the use of anisotropic dielectric properties to represent the differences in effective horizontal and vertical permittivity.

### ***3. Conductor loss over-estimated for very narrow conductors***

By comparing simulations and measurements, it was found that this Sonnet stackup over-estimates the conductor loss for very narrow conductors, resulting in pessimistic values for the Q factor.

This effect was seen for inductors where the line width was about the same as the top metal thickness. For the test cases, the simulated Q<sub>max</sub> for an inductor with 2µm wide lines was 20% below the measured values, whereas inductors with wider lines were simulated much more accurately.

### ***4. Sonnet 13 required because of new via loss model***

This version of the Sonnet Verification Kit is based on the new via metal definition introduced in Sonnet 13, for more accurate via loss modeling. Sonnet 12 can not be used with this version of the Sonnet Verification Kit.

In Sonnet 13, the cross section of a single via is properly included even if it is smaller than the cell size. For merged via arrays, the total metal cross section is calculated and the metal properties for the array are set so that the total DC resistance is maintained.

# Stackup Documentation

## SBC18H

(applies to SBC18HA, SBC18HX, **SBC18H2**, SBC18H3 and others)

	2500um			air_above	er=1.00
0	0.6um			nitride_overcoat	er=7.00
1	0.2um			oxide_overcoat	er=4.20
2	2.81um	2.81um	metal6	3.389E7 S/m	at_metal6 er=4.20
3	2um		via5		below_metal6 er=4.20
4	1.59um	1.59um	metal5	3.495E7 S/m	at_metal5 er=4.20
5	2um		via4		below_metal5 er=4.20
6	0.62um	0.62um	metal4	2.445E7 S/m	at_metal4 er=4.20
7	0.8um		via3		below_metal4 er=4.20
8	0.52um	0.52um	metal3	2.346E7 S/m	at_metal3 er=4.20
9	0.8um		via2		below_metal3 er=4.20
10	0.52um	0.52um	metal2	2.346E7 S/m	at_metal2 er=4.20
11	0.8um		via1		below_metal2 er=4.20
12	0.52um	0.52um	metal1	2.346E7 S/m	at_metal1 er=4.20
13	0.86um		contact		below_metal1 er=4.10
14	0.28um	0.28um	act	64.935E4 S/m	STI er=4.20
15	0.6um			sigma=200.000 S/m	EPI er=11.90
16	370um			sigma=12.500 S/m	Si er=11.90

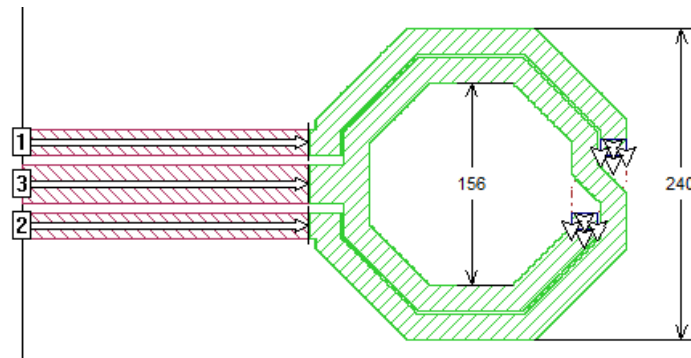
GND

## Inductor Examples

To help you with modelling your own inductors, the *examples* directory gives a few examples for stand-alone inductors based on TowerJazz measurement. In addition, one inductor example with feed lines and pads is included, and compared to the “raw” measurement of that “full” layout.

### ***D11: DIFF\_IND240x20x2p0***

This inductor example is a differential inductor with 2 turns, 20μm line width, 2μm gap with and 240μm outer dimension. Sonnet model file: D11\_inductoronly.son



The model was created from a GDSII file, using the GDSII template file SBCI8H.son and the layer mapping file SBCI8H.lay. The via simplification option was switched on, so that vias were automatically merged during the GDSII import.

Box wall ports are used to feed the inductor, and the reference plane is shifted to the edge of the inductor. Ports 1 and 2 are connected to the outer terminals, port 3 is connected to the center tap. The Sonnet simulation box size is ~3x the inductor diameter, to minimize the coupling between the inductor and the Sonnet simulation box.

Below is the comparison of the differential inductance between port 1 and 2, with port 3 as a virtual ground. In the measurement, the center tap was grounded to the feed line ground, so that the measured data file is a two port file:

measured\_D11\_inductoronly\_centertapshorted.s2p

The differential inductance plot shows the **total** inductance, not ½ inductance as in some TowerJazz documents. The equation used for the differential inductance plot is:

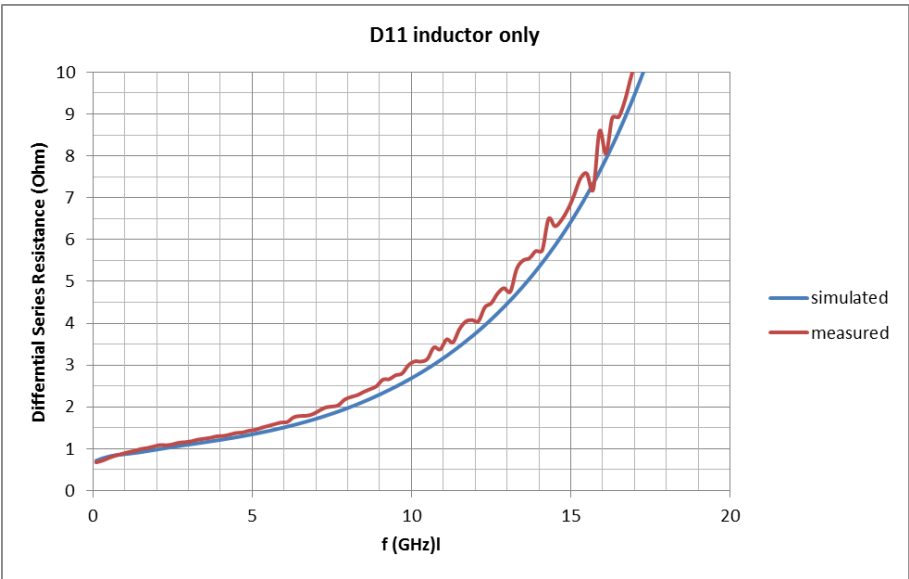
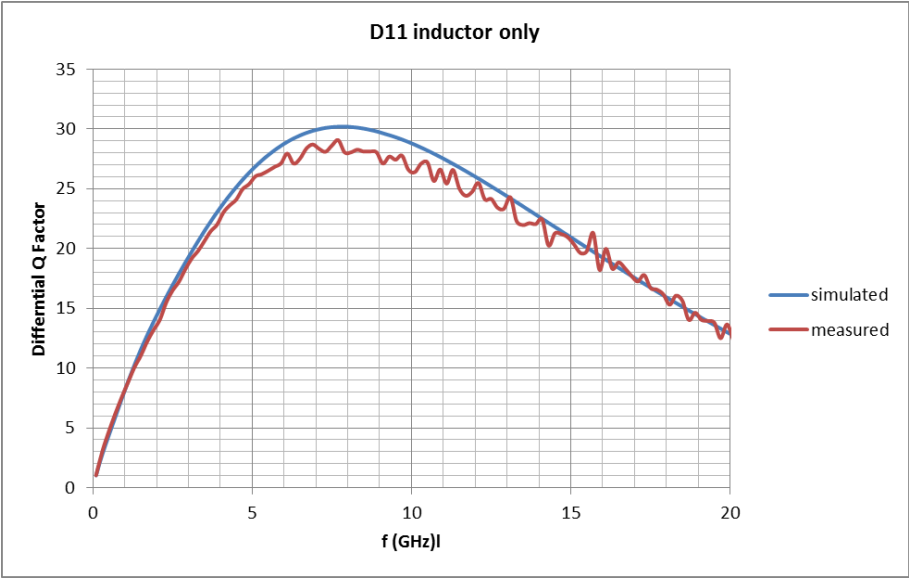
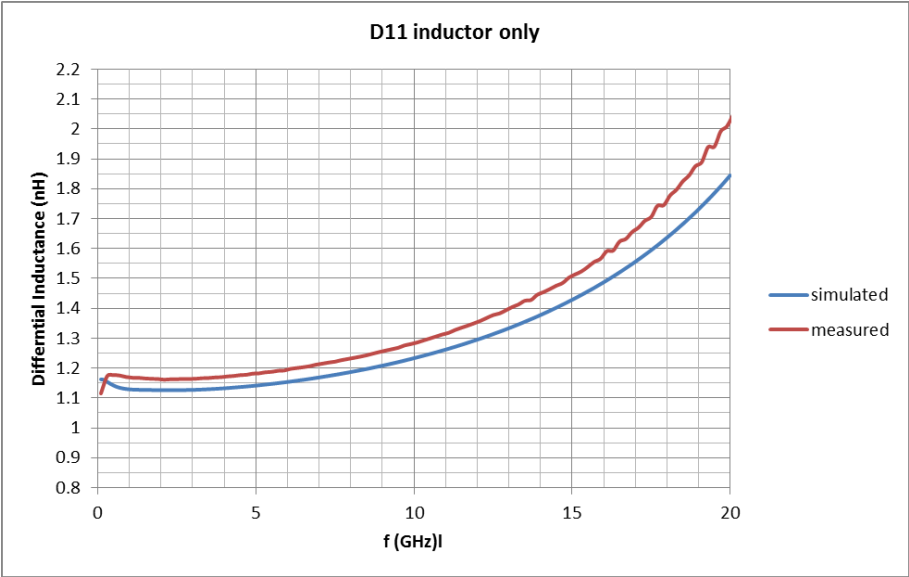
$$L_{diff,total} = \text{Imag} \{Z_{11} + Z_{22} - Z_{12} - Z_{21}\} / \omega$$

The differential mode Q factor is calculated using this equation:

$$Q_{diff} = \text{Imag} \{Z_{11} + Z_{22} - Z_{12} - Z_{21}\} / \text{Real} \{Z_{11} + Z_{22} - Z_{12} - Z_{21}\}$$

The differential mode series resistance is calculated using this equation:

$$R_{diff,total} = \text{Real} \{Z_{11} + Z_{22} - Z_{12} - Z_{21}\}$$



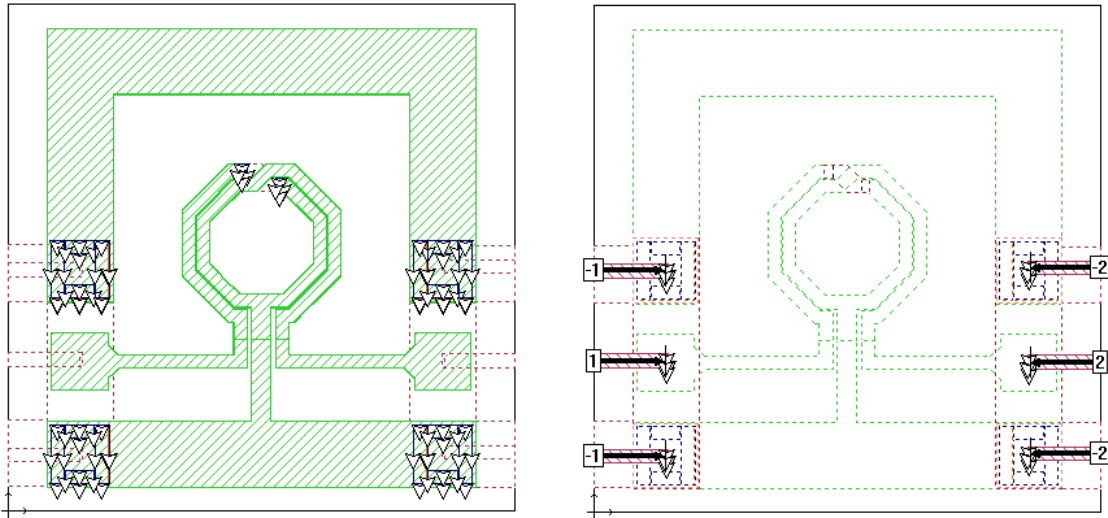


### ***D11: DIFF\_IND240x20x2p0 with feedlines and pads***

To exclude possible influences from the de-embedding of feedlines and pads, the comparison to measured data was also performed on the full layout. This eliminates any error that might be introduced by measurement de-embedding.

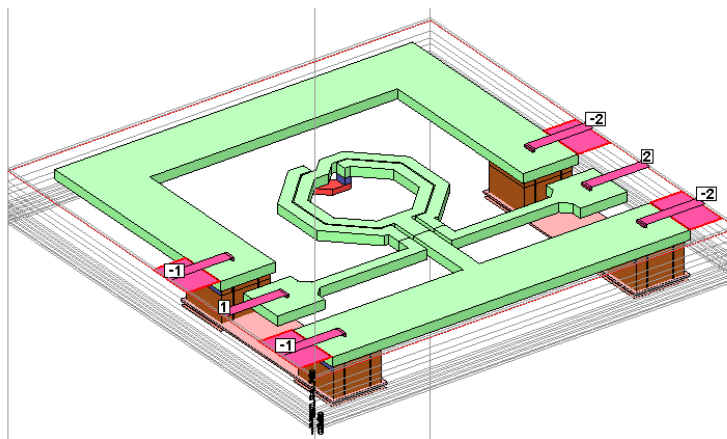
The Sonnet model file in the examples directory is D11\_with\_pads.son and the measurement raw data file is measured\_D11\_withpads\_centertapshorted.s2p.

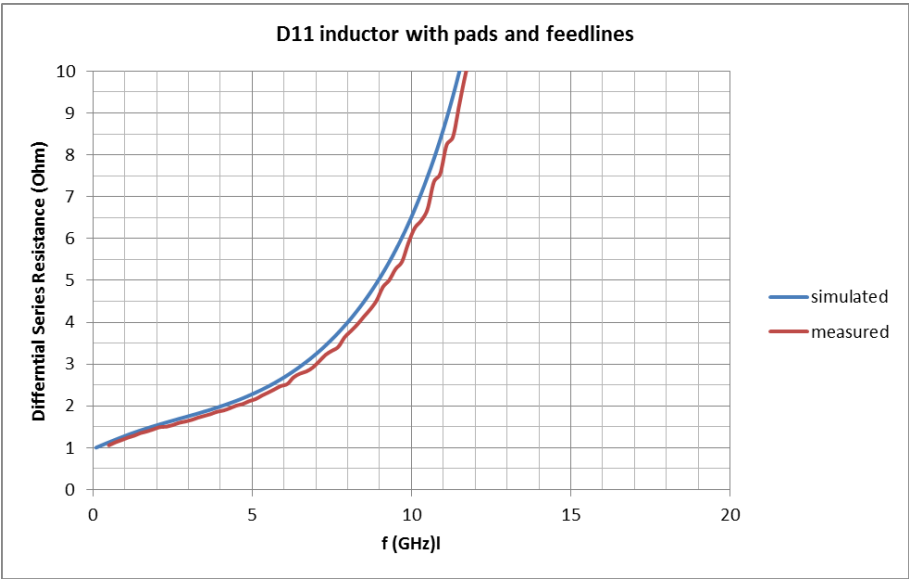
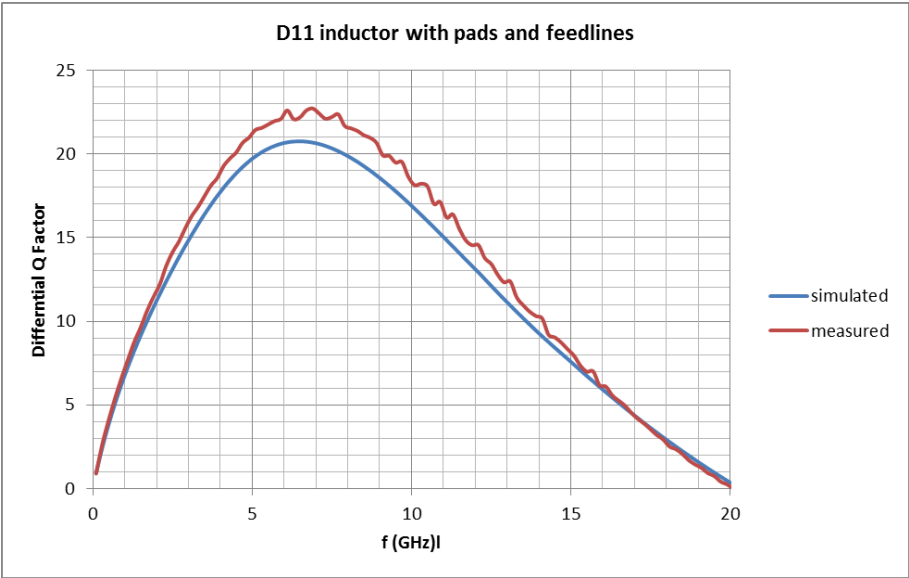
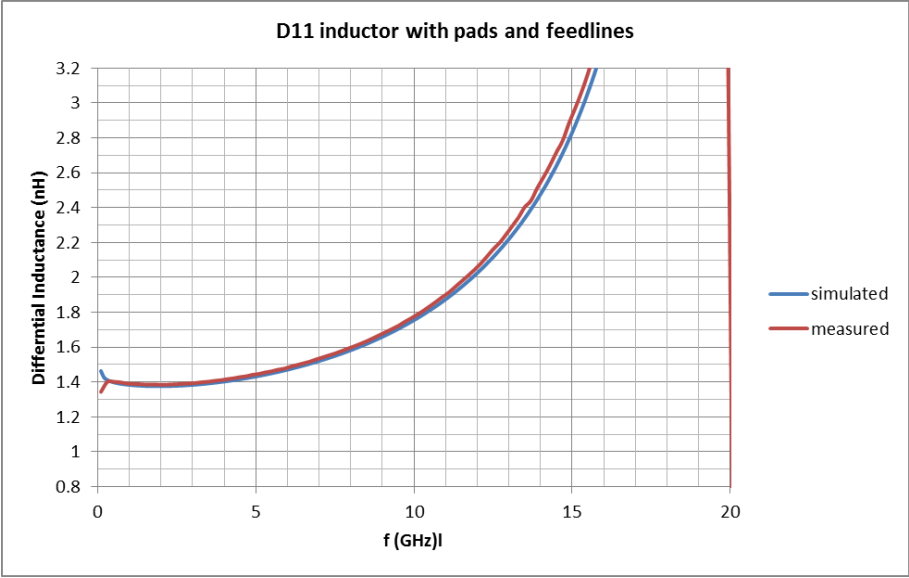
In measurement and simulation, the center tap is shorted to the feed line ground.



The wafer probe feed is modelled with box wall ports in -/+/- configuration, to create co-planar mode excitation and termination. The feedlines are placed at Sonnet level 0, above the passivation, and the reference shift is applied to the middle of the pads. There, the feedlines are connected to the pads with vias.

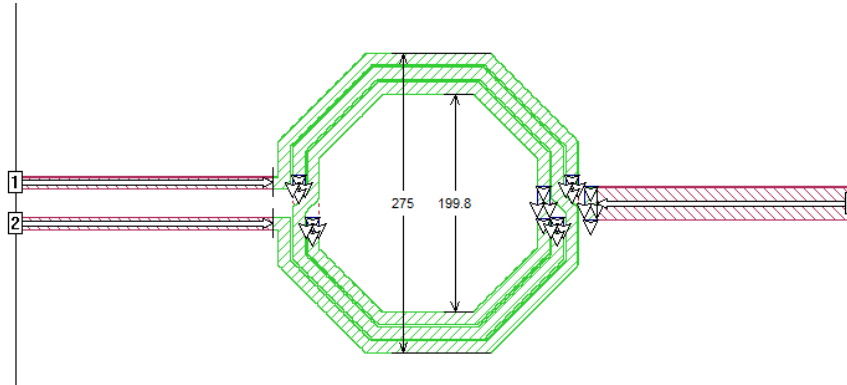
This is not exact, because the Sonnet reference shift algorithm assumes a constant cross section from the port up to the reference plane. To minimize the error, metal was placed under the “ground” feed lines between the ground frame and the Sonnet box.





### **D22: DIFF\_IND275x11.2x3p0**

This inductor example is a differential inductor with 3 turns, 11.2µm line width, 3µm gap with and 275µm outer dimension. Sonnet model file: D22\_inductoronly.son



The model was created from a GDSII file, using the GDSII template file SBC18H.son and the layer mapping file SBC18H.lay. The via simplification option was switched on, so that vias were automatically merged during the GDSII import.

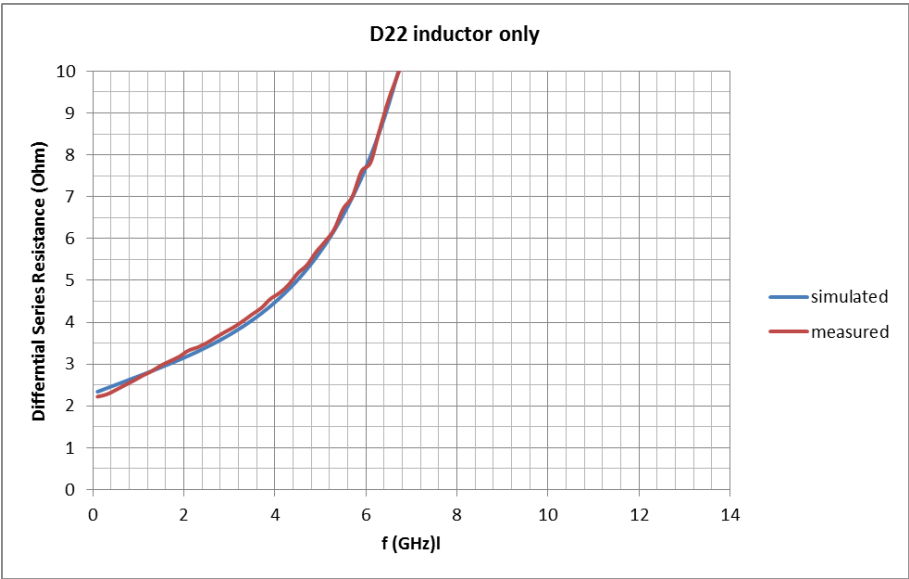
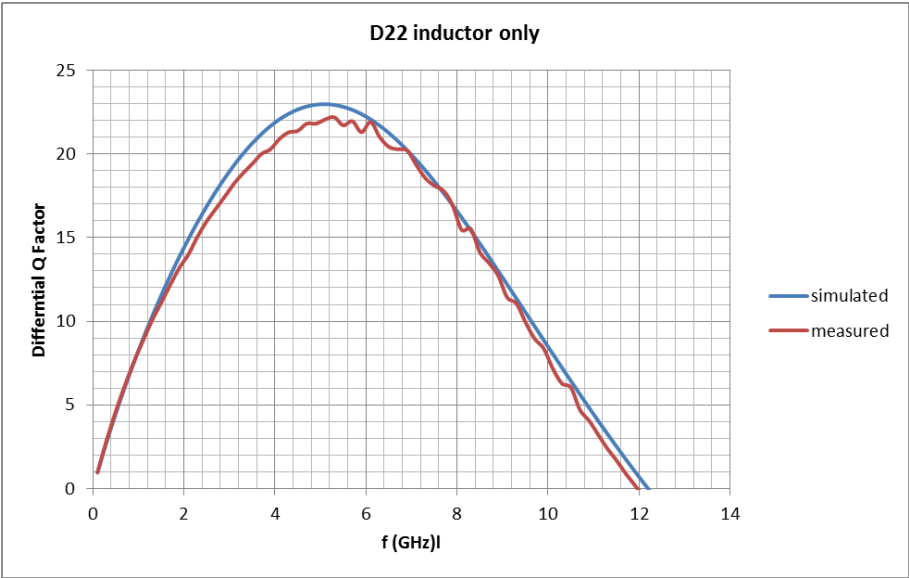
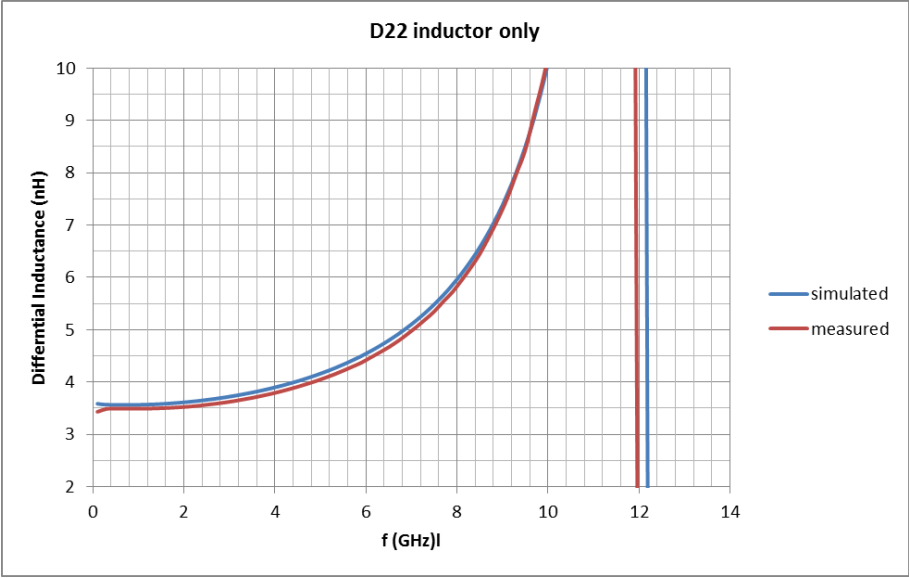
Box wall ports are used to feed the inductor, and the reference plane is shifted to the edge of the inductor. Ports 1 and 2 are connected to the outer terminals, port 3 is connected to the center tap. The Sonnet simulation box size is ~3x the inductor diameter, to minimize the coupling between the inductor and the Sonnet simulation box.

Below is the comparison of the differential inductance between port 1 and 2, with port 3 as a virtual ground. In the measurement, the center tap was grounded to the feed line ground, so that the measured data file is a two port file: measured\_D22\_inductoronly\_centertapshorted.s2p

The differential inductance plot shows the **total** inductance, not 1/2 inductance as in some TowerJazz documents. The equation used for the differential inductance plot is:  
$$L_{diff, total} = \text{Imag} \{Z_{11} + Z_{22} - Z_{12} - Z_{21}\} / \omega$$

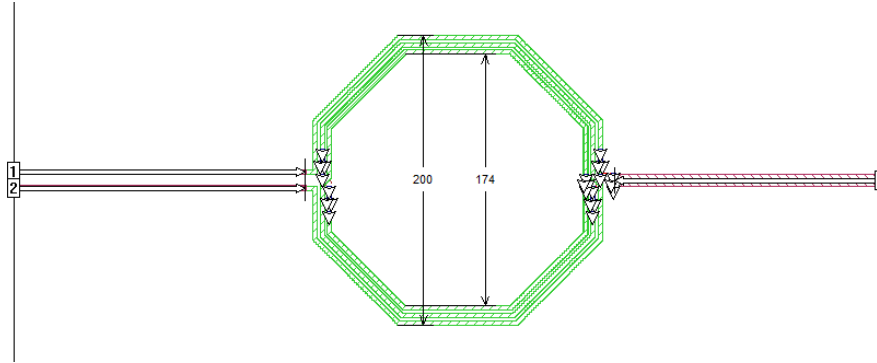
The differential mode Q factor is calculated using this equation:  
$$Q_{diff} = \text{Imag} \{Z_{11} + Z_{22} - Z_{12} - Z_{21}\} / \text{Real} \{Z_{11} + Z_{22} - Z_{12} - Z_{21}\}$$

The differential mode series resistance is calculated using this equation:  
$$R_{diff, total} = \text{Real} \{Z_{11} + Z_{22} - Z_{12} - Z_{21}\}$$



### **D26: DIFF\_IND200x3x3p0**

This inductor is an example for the over-estimated conductor loss when very narrow lines are simulated with the default stackup files. The device under test is a differential inductor with 3 turns, 3μm line width, 3μm gap with and 200μm outer dimension. Sonnet model file: D26\_inductoronly.son



**First, the inductor is simulated with the standard stackup that is provided with this Sonnet Verification Kit. This results in a over-estimate of loss, because the calculation of side wall currents in the skin effect region are less accurate for very narrow lines. Then, it is shown how to overcome this issue with tweaked metal properties.**

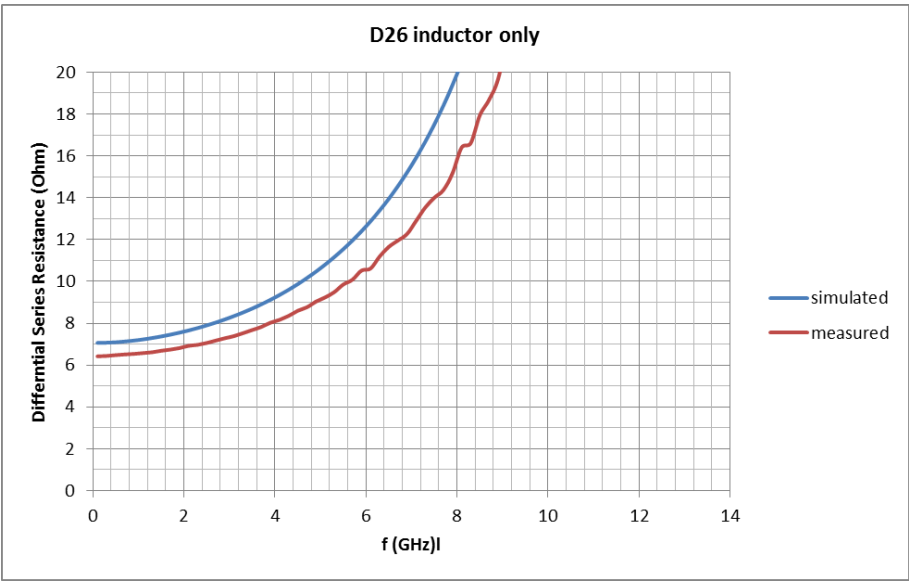
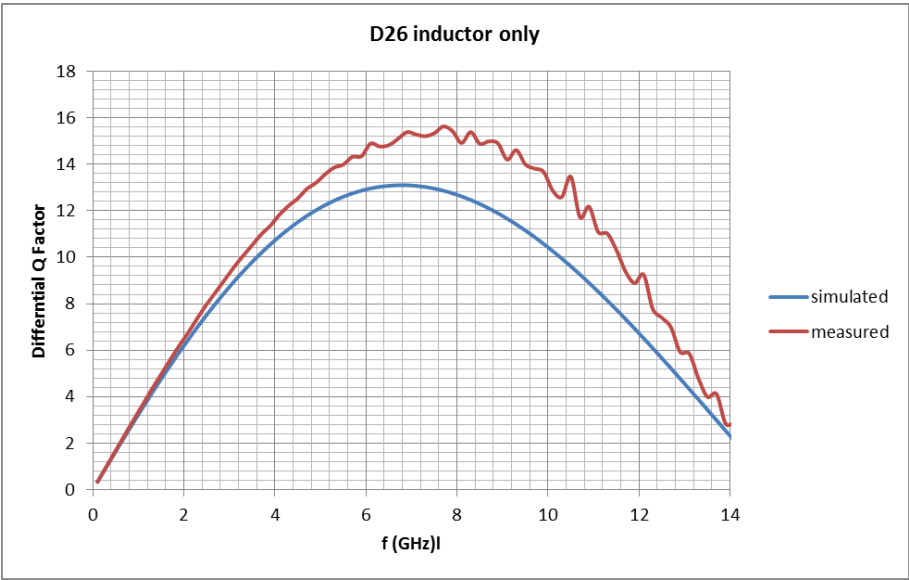
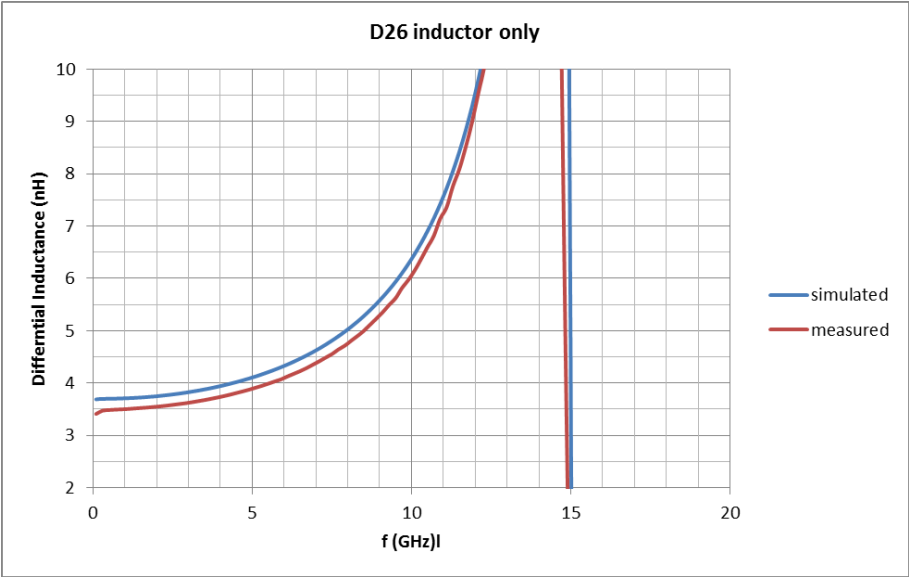
Box wall ports are used to feed the inductor, and the reference plane is shifted to the edge of the inductor. Ports 1 and 2 are connected to the outer terminals, port 3 is connected to the center tap. The Sonnet simulation box size is ~3x the inductor diameter, to minimize the coupling between the inductor and the Sonnet simulation box.

Below is the comparison of the differential inductance between port 1 and 2, with port 3 as a virtual ground. In the measurement, the center tap was grounded to the feed line ground, so that the measured data file is a two port file: measured\_D26\_inductoronly\_centertapshorted.s2p

The differential inductance plot shows the **total** inductance, not 1/2 inductance as in some TowerJazz documents. The equation used for the differential inductance plot is:  
$$L_{diff, total} = \text{Imag} \{Z_{11} + Z_{22} - Z_{12} - Z_{21}\} / \omega$$

The differential mode Q factor is calculated using this equation:  
$$Q_{diff} = \text{Imag} \{Z_{11} + Z_{22} - Z_{12} - Z_{21}\} / \text{Real} \{Z_{11} + Z_{22} - Z_{12} - Z_{21}\}$$

The differential mode series resistance is calculated using this equation:  
$$R_{diff, total} = \text{Real} \{Z_{11} + Z_{22} - Z_{12} - Z_{21}\}$$



### Metal definition tweak for very narrow lines

The bad agreement for D26 results from under-estimated currents on the sidewalls of the narrow conductor. Below are the results for a model that was manually modified with a tweaked metal definition, where the skin effect resistance was reduced by a factor of two, to account for the almost square conductor cross section. With this tweak, we assume that the skin currents on the side walls are about the same as the skin currents on the top and bottom side of the conductor.

Sonnet model file: D26\_inductoronly\_tweakedMetal.son

Sonnet thick metal modelling uses a built-in model that covers the range from DC to skin effects, so we have to use the generic metal model with RDC/RRF and create the thick metal model from two stacked thin metals. This is only shown for demonstration, and not recommended for normal use.

**Don't to try use this tweak unless you understand exactly what you are doing and what the limitations and assumptions are!**

Metal definition for each of the two parallel metal sheets:

The image shows two windows from the Sonnet software. The top window is titled "Planar Metal Editor-D26\_inductoronly\_tweakedMetal.son". It contains the following fields:

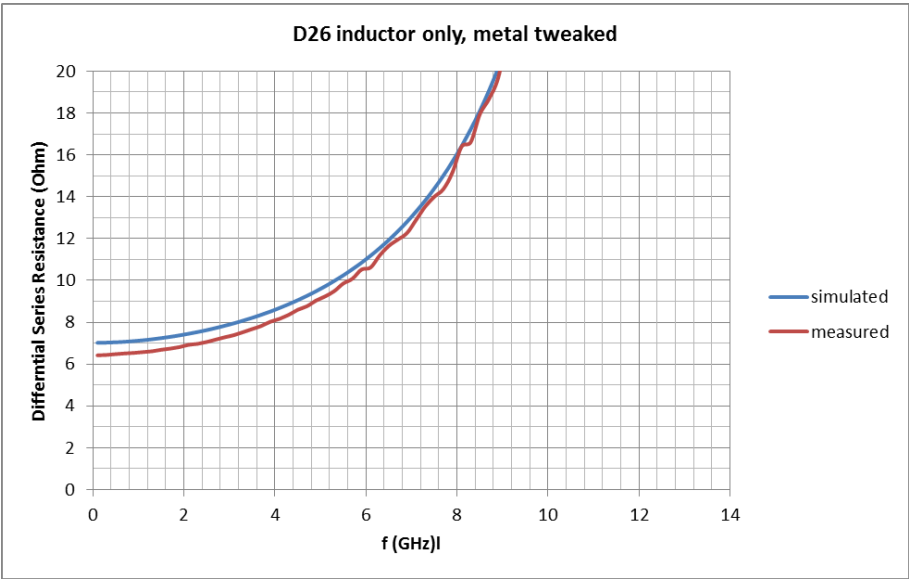
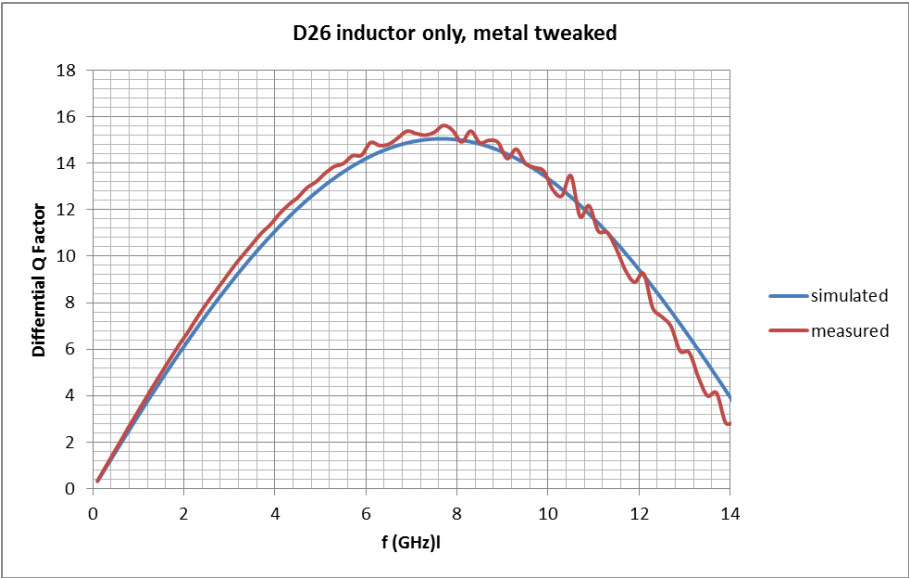
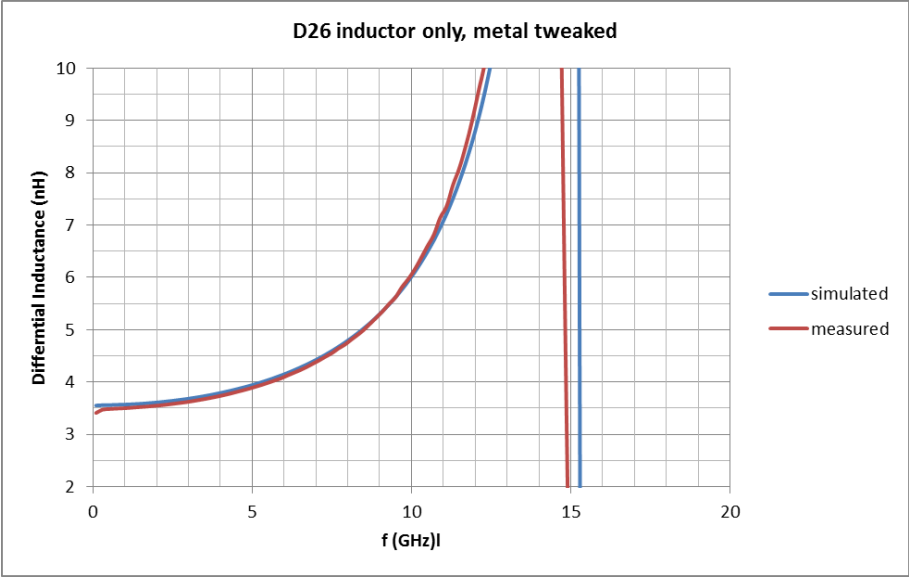
- Name:** Metal6\_half
- Pattern:** A small grid icon.
- Model:** Rdc/Rrf (selected from a dropdown)
- Rdc:** 0.021 ohms/sq
- Rrf:** 3.41e-7\*Rrf\_factor (with a "See Help \*" link)

The bottom window is titled "Variable List-D26\_inductoronly\_tweakedMetal.son". It contains a table with the following data:

Used	Variable	Value	Description
	Rrf_factor	0.5	Metal Rrf

As you can see in the results below, the metal with tweaked side wall currents is not only more accurate for Q factor, it is also more accurate for series inductance.

**Note that this tweak to the metal model is only valid for metal cross section where the width is about the same as the metal thickness.**





# Sonnet Interface to Cadence Virtuoso

Sonnet offers an interface that links into Cadence Virtuoso, and can read layouts directly from the Cadence database.

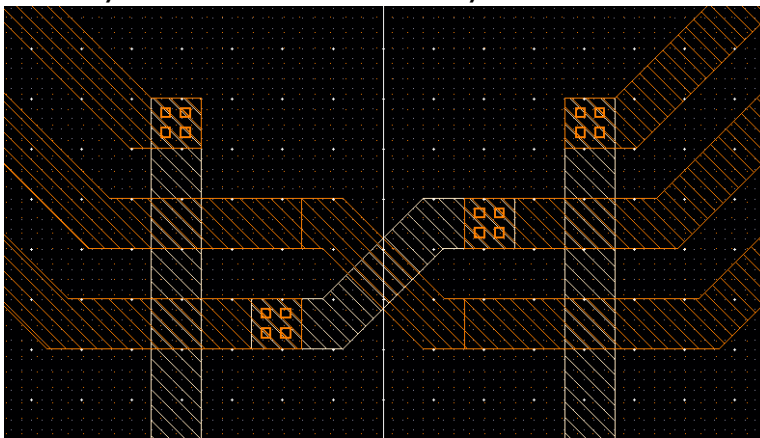
<http://muehlhaus.com/wp-content/uploads/2011/08/Using-Sonnet-in-a-Cadence-RFIC-Design-Flow.pdf>

Below is some additional information for use of the Sonnet Cadence integration.

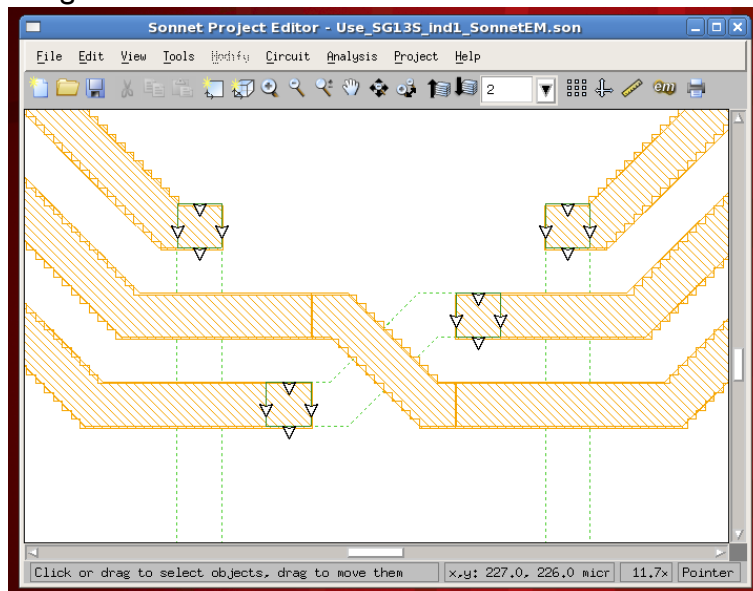
## *Via merging*

Since Sonnet release 13, Sonnet's Cadence interface will automatically merge via arrays when the "Simply Via Array" option is enabled. This creates simulation friendly via boundaries and adjusts the via metal properties to give the correct series resistance.

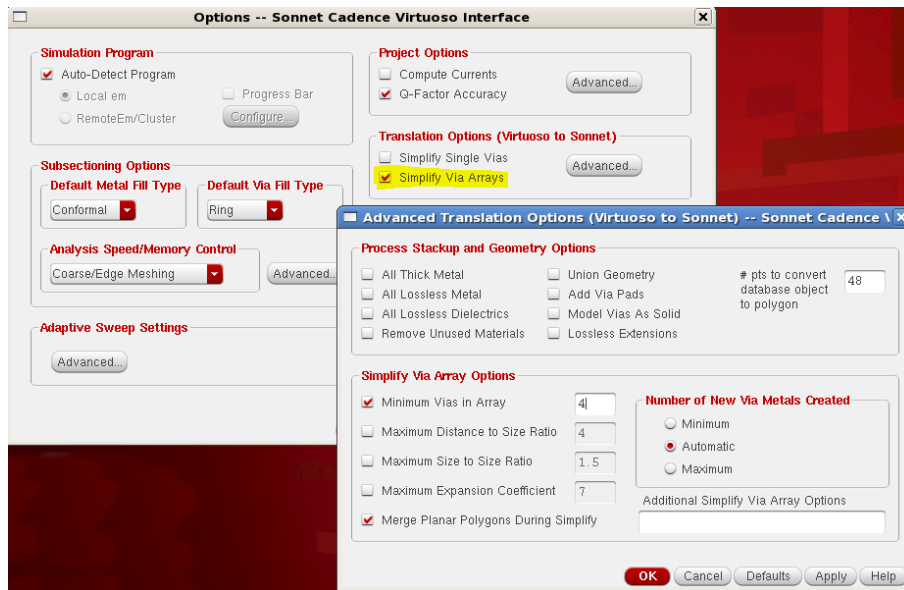
Via arrays as seen in the Cadence layout and Cadence EM view:



## Merged vias in the Sonnet model



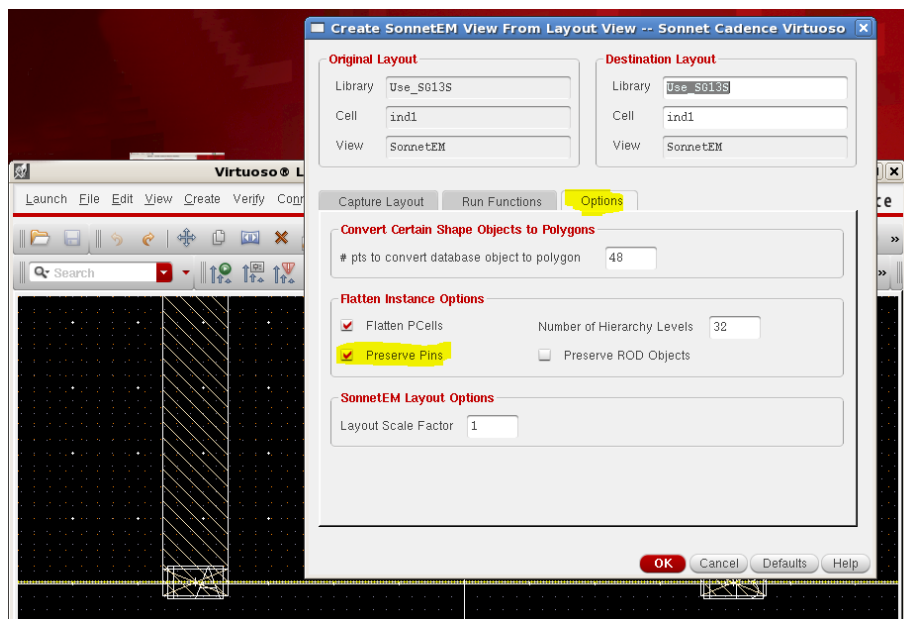
You can use the default via merge settings with inductor pcells, with no need for manual changes.



### ***Cadence pin to Sonnet port conversion***

The Sonnet interface can automatically detect Cadence shape pins and convert them to Sonnet ports. If you want include pins from the layout view, instead of adding them manually in the Sonnet EM view, use the "Preserve Pins" option.

This setting is **disabled** by default. You can save this setting by saving the "State" in the Sonnet interface application, or you can also modify the defaults according to your own preferences, as described in `$SONNET_DIR/sonnet_virtuoso_dk/ virtuoso.txt`



## Legal note

All files have been created with care, but the authors do not warrant that the simulation results obtained with the files and information from this verification kit is accurate. You may only use the files and information from this verification kit at your own risk.

Autor: Volker Mühlhaus  
Dr. Mühlhaus Consulting & Software GmbH  
[www.muehlhaus.com](http://www.muehlhaus.com)

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## Technology file modifications

- VI.2 31. August 2012 (Mü)  
Changed file names from SBCI8H2 to SBCI8H and updated documentation
- VI.1 22 August 2012 (Mü)  
More example files added
- v1.0 27. March 2012 (Mü)  
Initial version of this Sonnet Verification Kit