Use Jazz 0.18-µm CMOS devices, model "nfet" and "pfet" for active transistors. For all passive components, you can use ideal model in "analoglib". Set NMOS and PMOS sizes as shown in the figure.

Q-1) Through DC simulation, set R_B and V_B so that total bias current in the differential paths is 2 mA (1mA per each path) and all the transistors can operate in saturation mode (10 pt).

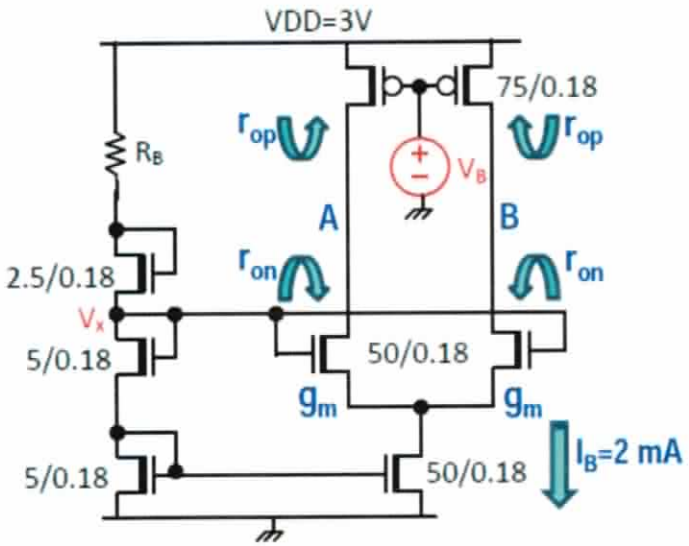

Figure 1: Q-1

Solution:

The schematic for the circuit shown in Figure 1 is shown in Figure 2. Now, let us choose the R_B to be 3.5KΩ, and sweep the V_B from 0V to 3V. Figure 2 shows the current I_{D2} as function of V_B. It is noticed that the current I_{D2} is equal to 1 mA when V_B is equal to 2.44V. This voltage value is updated and the circuit was re-simulated to check the condition for all transistors. It was found that all transistors were in saturation and the current in each path was 1mA.

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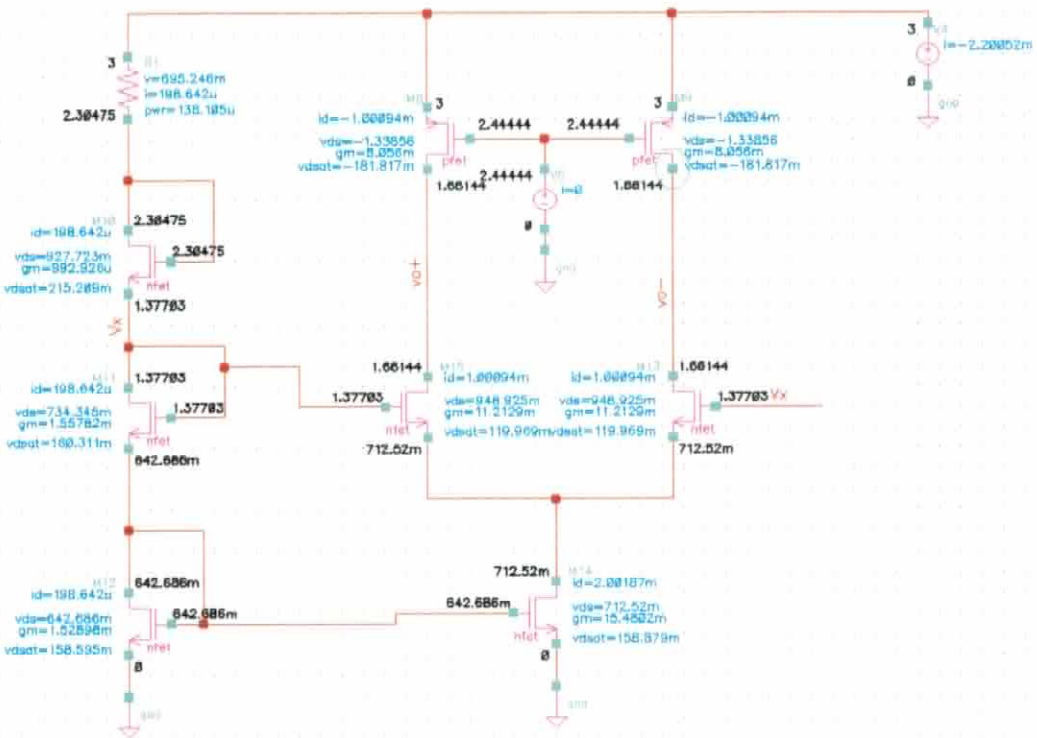

Figure 1: Q-1

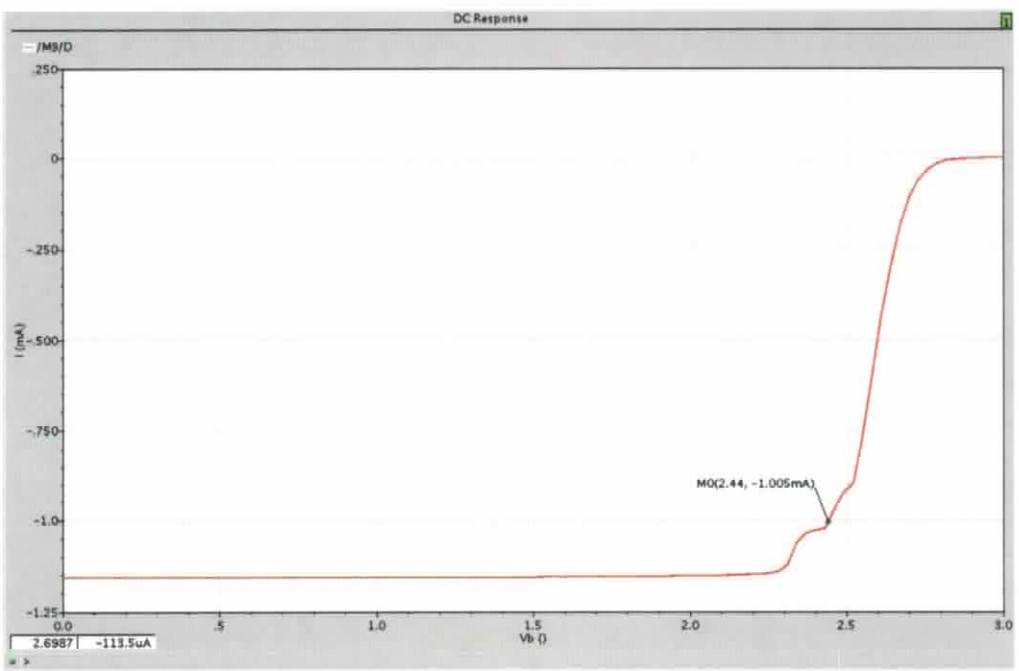

Figure 2: V_B versus I_{D2}

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Q-2) Once you set an appropriate V_B, you can check all small signal parameters out (basically the simulator will display the small signal parameters). What are the output impedance of NMOS (r_{on}) and PMOS (r_{op})? What is g_m of NMOS?

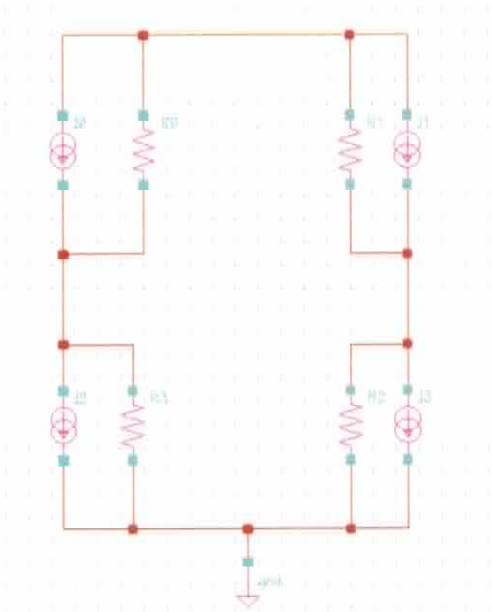
Solution:

$$r_{on} = \frac{1}{g_{ds}} = \frac{1}{571.168\,u} = 1750.8\Omega$$
$$r_{op} = \frac{1}{g_{ds}} = \frac{1}{181.979\,u} = 5495.14\Omega$$
$$g_{mn} = 11.213\,mS$$
$$g_{mp} = 8.056\,mS$$

Q-3) From Q-1 you can notice that DC voltage of drain nodes of NMOS and PMOS (node-A and node-B) will be very sensitive to VB. Explain the reason why (5 pt).

Solution:

To explain the reason for the nodes A and B being sensitive to Vb, let us have a look at the equivalent circuit is shown in figure :



The PMOS transistors work as current sources with r_o being their output impedance. The same thing is correct for the NMOS transistors. If Vb is slightly increased, the current generated by PMOS transistor also increases. If there is mismatching between the PMOS and NMOS current sources, the extra current generated by PMOS transistor goes to the output resistor of the NMOS transistors which increases the voltage at the nodes A and B. this voltage increase limits the maximum allowable swing voltage.

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Use bias voltages you set in the previous step (Step-(1)), and apply DC bias voltages to NMOS and PMOS as shown in the figure below (Vx and VB to NMOS and PMOS, respectively). Set CL as CL=10 pF (note: CL could represent a loading capacitance from next stage).

Q-4) Apply input signal ($\pm\frac{1}{2}V_s$) using "vsin" source, and plot output differential gain ($A_v = \frac{V_{o+}-V_{o-}}{V_s}$) versus frequency in dB-scale (5 pt)

Solution:

The schematic design of the differential amplifier is shown in figure 3. The output and input differential voltages are shown in figure 4. The maximum output voltage is almost 150 mV when the applied differential input voltage is 10 mV. Therefore, the voltage gain is 15 as shown in figure 5. The voltage gain in dB is 23.46 dB as shown in figure 6.

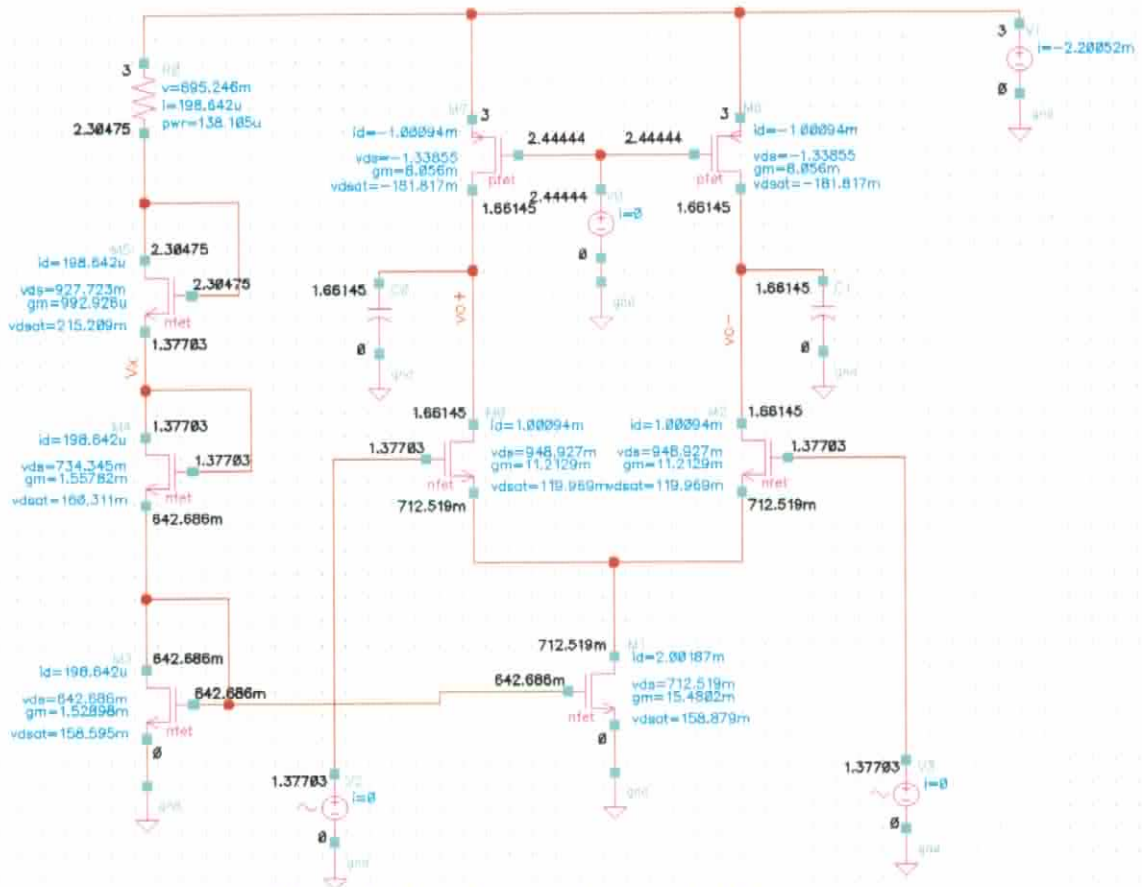

Figure 3: the schematic design of Q-4

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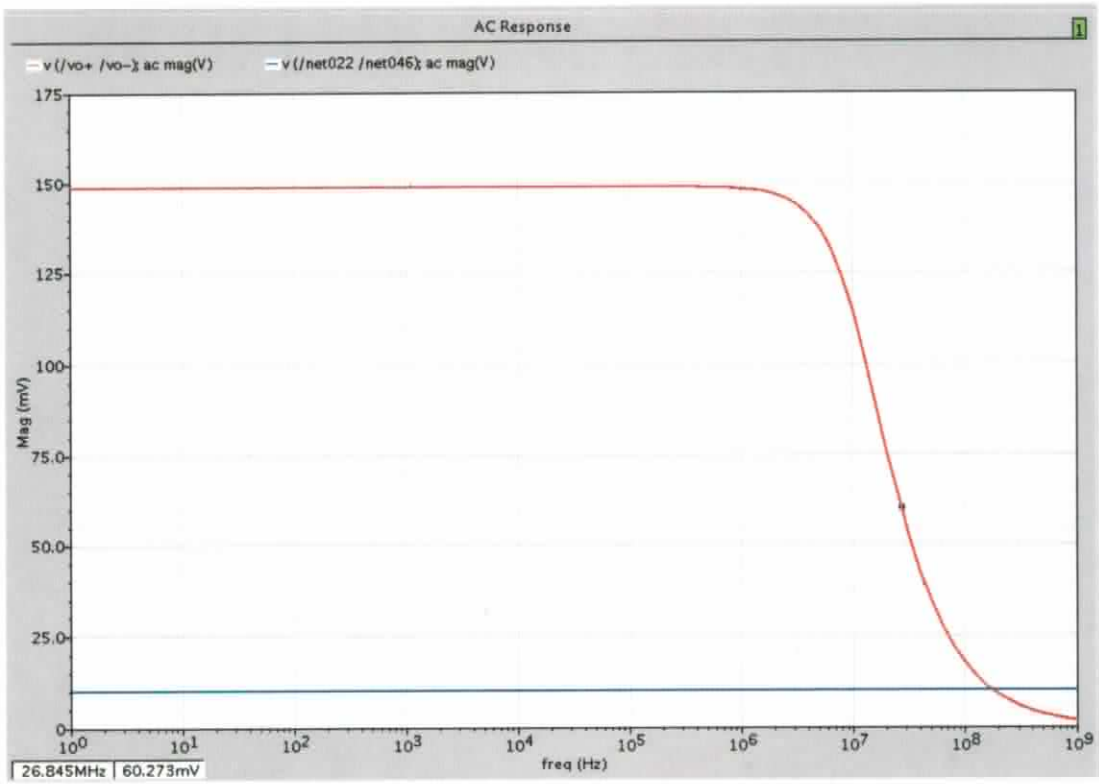

Figure 4: the output and the input differential voltages

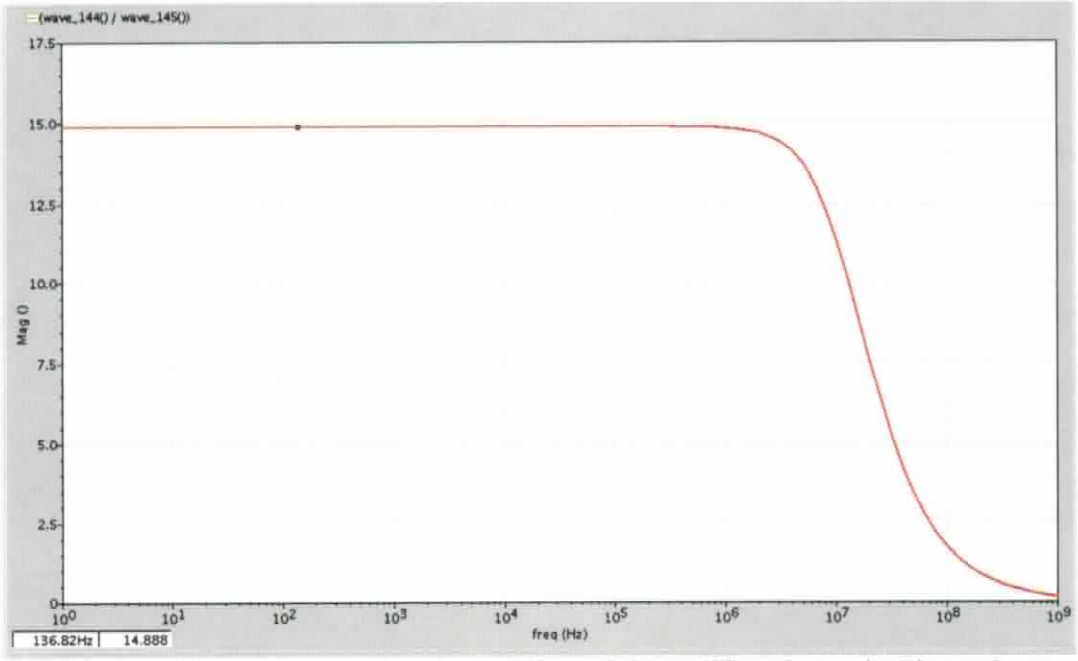

Figure 5: the voltage gain of the differential amplifier shown in Figure 3

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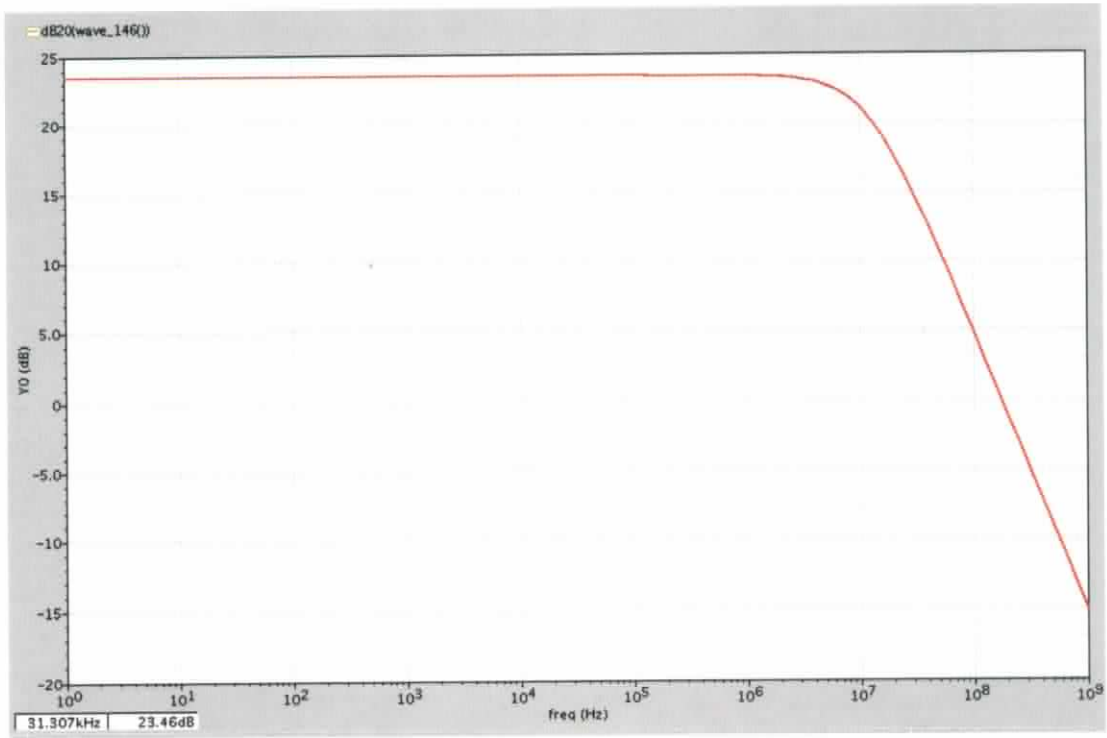

Figure 6: the voltage gain in dB of the differential amplifier shown in Figure 3

Q-5) Estimate the differential gain based on small signal parameters (r_{on}, r_{op} and g_m) you find in the DC simulation in Step-(1) , and compare the simulation result in Q-4 with your estimation (5pt).

Solution

The differential gain is:

$$A_v = g_m(r_{on}//r_{op})$$

Since $r_{on} = 1750.8\Omega$, $r_{op} = 5495.14\Omega$, *and* $g_{mn} = 11.213\ mS$, then:

$$A_v = 11.213 \times 10^{-3} \times \frac{1750.8 \times 5495.14}{1750.8 + 5495.14} = 14.9$$

$$A_v(dB) = 20\log(14.9) = 23.46\ dB$$

These results perfectly match the simulation results.

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Q-6) From the result in Q-4, you can confirm that the differential amplifier is one-pole system. Calculate the pole frequency (3-dB BW) based on small signal parameters and compare your calculation with the simulation result (5 pt).

Solution:

The pole frequency of the differential amplifier can be derived as:

$$A_v = g_m(r_{on}//r_{op}) \times \frac{1}{1 + r_{on}//r_{op} \times sC_T} = g_m(r_{on}//r_{op}) \times \frac{1}{1 + \frac{s}{\omega_p}}$$

$$\tau_p = \frac{r_{on}r_{op}}{r_{on} + r_{op}} \times C_T$$

The total capacitance seen at each output node is:

$$C_T = C_{GD1}\left(1 + \frac{1}{|A_v|}\right) + C_{GD2} + C_L$$

$$\tau_p = \frac{1750.8 \times 5495.14}{1750.8 + 5495.14} \times \left(17.207\ fF \times \left(1 + \frac{1}{14.9}\right) + 22.8545\ fF + 10pF\right) = 13.333\ n\ sec$$

$$\omega_p = 75.00341\ Mrad/sec$$

$$f_p = 11.94\ MHz$$

The calculated pole frequency is equal to the simulation result which is 11.9 MHz.

Q-7) Apply input signal ($\pm\frac{1}{2}V_s$) using "vsin" source, and plot output gain ($A_v = \frac{V_o}{V_s}$) versus frequency in dB-scale. While single-ended output, gain should be about the same as in Q-4, and explain why? (5pt).

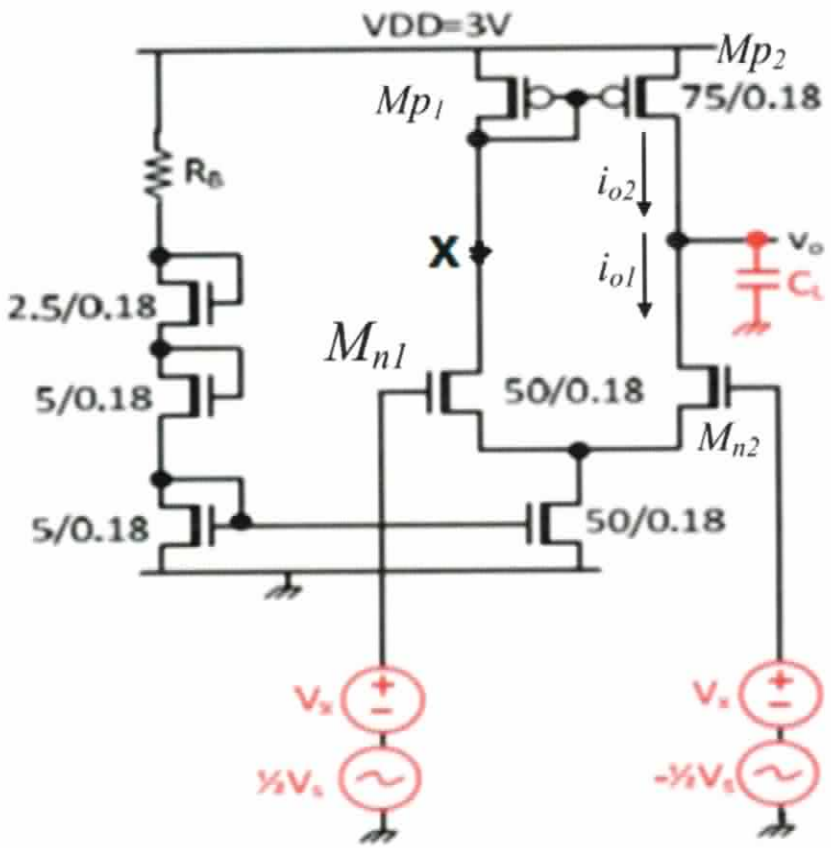


Figure 7: Q-7

Solution:

The schematic design of Figure 7 is shown in Figure 8,. The output differential voltage of the design is shown in Figure 8. It is noticed that the gain of this circuit with single-ended output is equal to the gain of the circuit shown in Figure 3 with differential output. This is achieved by copying the input drain current from the right to the left side where the magnitudes of the two input signals add. For this purpose, the input of the current mirror is connected to the right output and the output of the current mirror is connected to the left output of the differential amplifier. The current mirror inverts the right collector current and tries to pass it through the left transistor that produces the left collector current. In the middle point between the two left transistors, the two signal currents are subtracted. In this case, (differential signal), they are equal and opposite.

If we ignore the parasitic capacitance for a moment, the voltage at node X can be presented as:

$$V_X = i_{o1} \times \frac{1}{g_{mp1}}$$

This voltage is the gate to source voltage of M_{p2}. Therefore the current i_{o2} is :

$$i_{o2} = -g_{mp2} V_X = -g_{mp2} \times i_{o1} \times \frac{1}{g_{mp1}}$$

Since g_{mp1} is equal to g_{mp2}, the current is :

$$i_{o2} = -i_{o1}$$

The output voltage for

$$V_o = i_{oT} \times (r_{op} // r_{on} // \frac{1}{sC_{gs}}) = (i_{o1} - (-i_{o1})) \times (r_{op} // r_{on} // \frac{1}{sC_{gs}})$$

$$V_o = 2i_{o1} \times (r_{op} // r_{on} // \frac{1}{sC_{gs}})$$

$$i_{o1} = \frac{1}{2} g_{mn1} V_x$$

$$V_o = g_{mn1} V_x \times (r_{op} // r_{on} // \frac{1}{sC_{gs}})$$

$$A_v = \frac{V_o}{V_x} = g_{mn1} \times (r_{op} // r_{on} // \frac{1}{sC_{gs}})$$

Therefore the gain of this single-ended output circuit is equal to the gain of differential output circuit shown in figure 3.

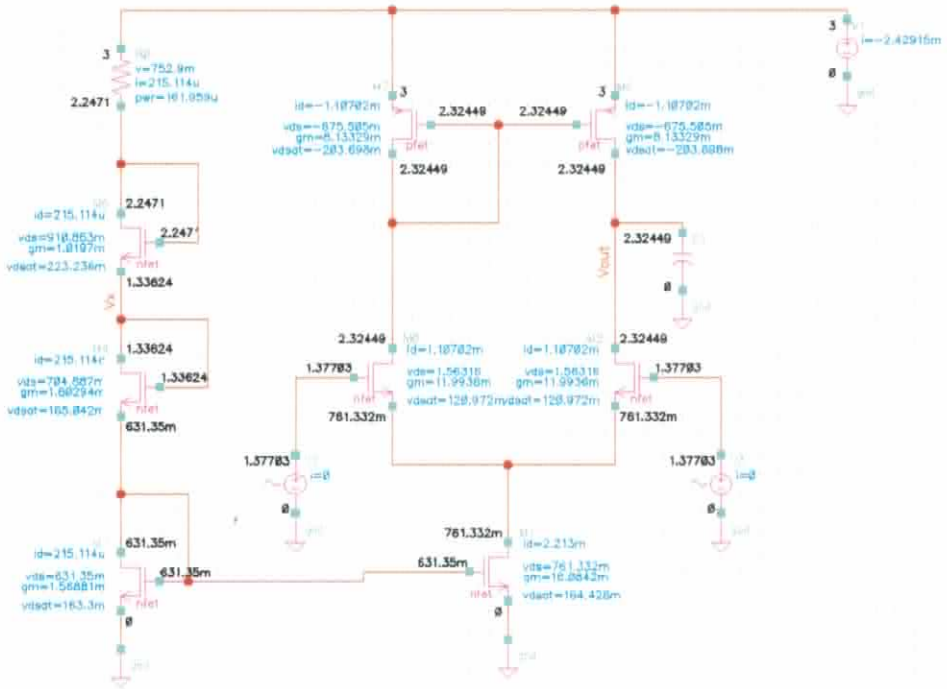


Figure 8: The schematic design of Q-7

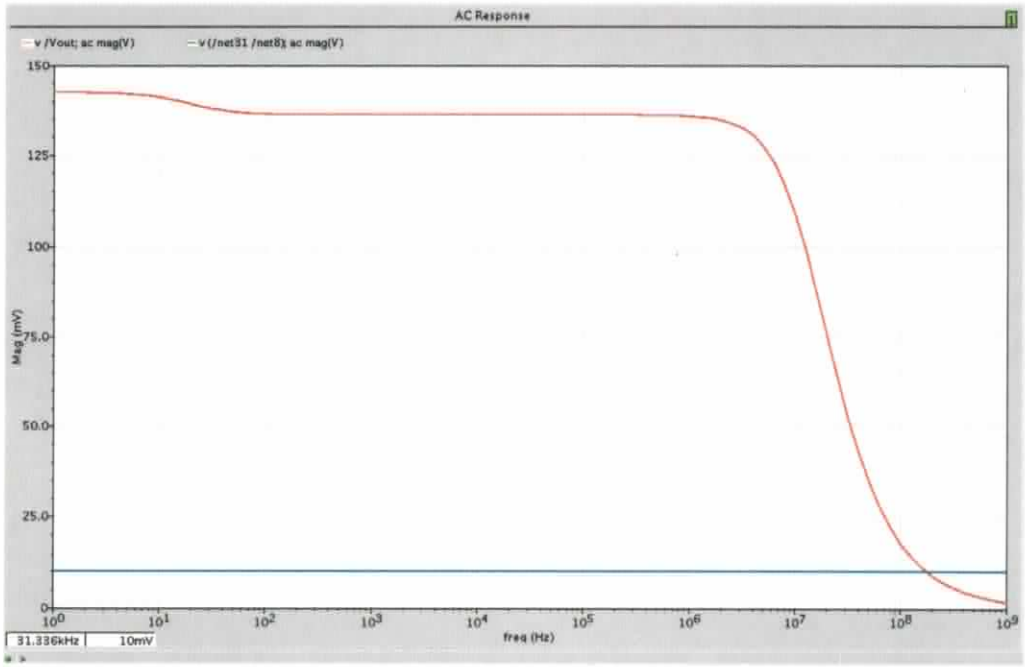


Figure 9: The output voltage and the input voltage versus frequency.

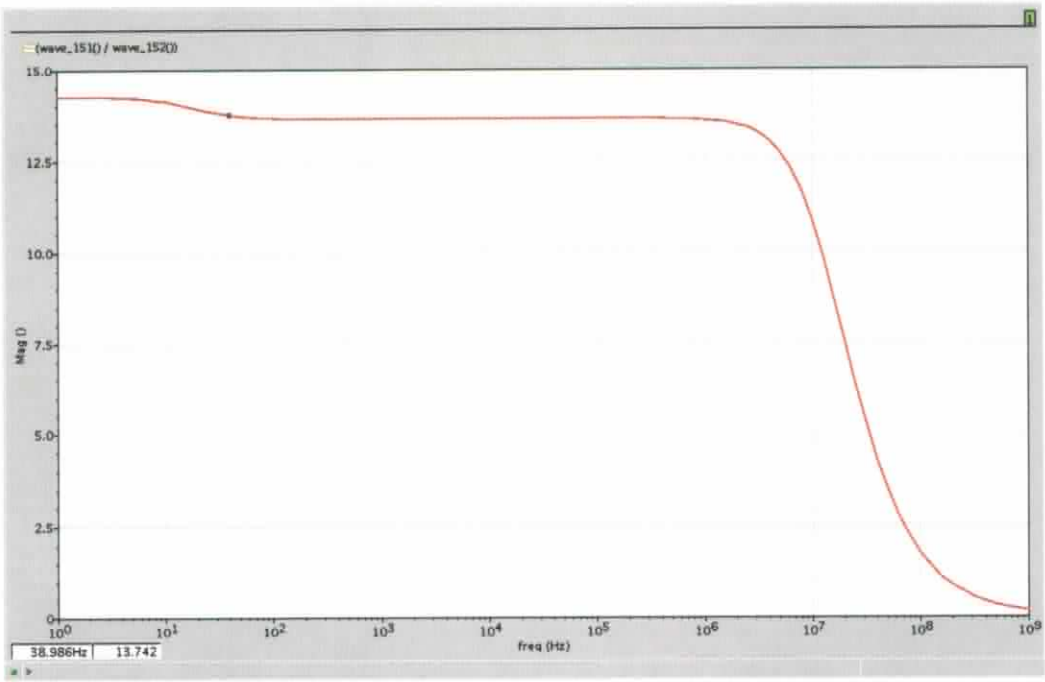


Figure 10: the voltage gain for the circuit shown in figure 8.

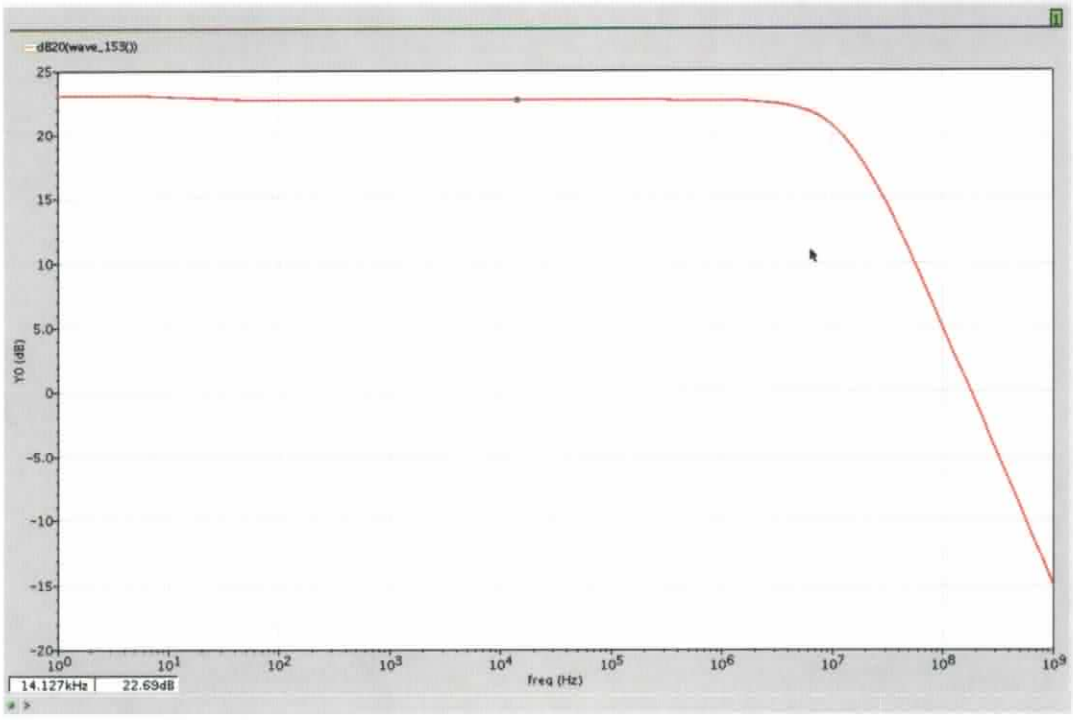


Figure 11: the voltage gain in dB for the circuit shown in figure 8.

Q-8) From the result in Q-7, you should observe that this amplifier is second-order system (2-poles and 1-zero). Calculate the dominant, non-dominant poles and zero frequencies. Compare your calculations with the simulation results (20 pt). *Hint: You can approximate that each node contribute a pole ("one-pole one-node " approximation).*

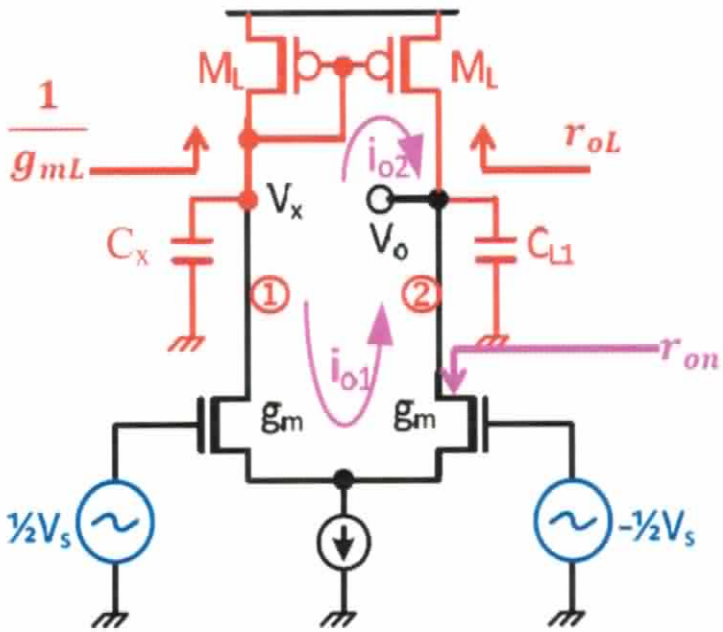


Figure 12: Q-8

Solution:

$$V_X = i_{o1} \times \left(\frac{1}{g_{mL}} // \frac{1}{s\,C_x} \right)$$

Where the C_x is the parasitic capacitance at the node V_x.

$$V_X = i_{o1} \frac{1}{g_{mL}} \times \left(\frac{1}{1 + \frac{s}{\omega_{px}}} \right)$$

$$\omega_{px} = \frac{g_{mL}}{C_x}$$

This voltage is the gate to source voltage of M_L . Therefore the current i_{o2} is :

$$i_{o2} = g_{mL} V_X = g_{mL} \times i_{o1} \frac{1}{g_{mL}} \times \left(\frac{1}{1 + \frac{s}{\omega_{px}}} \right) = i_{o1} \left(\frac{1}{1 + \frac{s}{\omega_{px}}} \right)$$

$$V_o = i_{oT} \times (r_{op} // r_{on} // \frac{1}{sC_{gs}}) = (i_{o1} + i_{o2}) \times (r_{op} // r_{on} // \frac{1}{sC_{gs}})$$

$$= \frac{r_{op} r_{on}}{r_{op} + r_{on}} \left(i_{o1} + i_{o1} \left(\frac{1}{1 + \frac{s}{\omega_{px}}} \right) \right) \times \left(\frac{1}{1 + \frac{s}{\omega_{p2}}} \right)$$

Where $\omega_{p2} = \frac{1}{\frac{r_{op} r_{on}}{r_{op} + r_{on}} C_T}$

$$V_o = i_{o1} \frac{r_{op} r_{on}}{r_{op} + r_{on}} \left(1 + \left(\frac{1}{1 + \frac{s}{\omega_{px}}} \right) \right) \times \left(\frac{1}{1 + \frac{s}{\omega_{p2}}} \right)$$

$$V_o = i_{o1} \frac{r_{op} r_{on}}{r_{op} + r_{on}} \left(\frac{1 + \frac{s}{\omega_{px}}}{1 + \frac{s}{\omega_{px}}} + \left(\frac{1}{1 + \frac{s}{\omega_{px}}} \right) \right) \times \left(\frac{1}{1 + \frac{s}{\omega_{p2}}} \right)$$

$$V_o = \frac{i_{o1} \frac{r_{op} r_{on}}{r_{op} + r_{on}}}{\left(1 + \frac{s}{\omega_{px}} \right) \left(1 + \frac{s}{\omega_{p2}} \right)} \left(2 + \frac{s}{\omega_{px}} \right)$$

$$V_o = 2 i_{o1} \frac{r_{op} r_{on}}{r_{op} + r_{on}} \frac{\left(1 + \frac{s}{\omega_z} \right)}{\left(1 + \frac{s}{\omega_{px}} \right) \left(1 + \frac{s}{\omega_{p2}} \right)}$$

$$\omega_z = 2 \omega_{px}$$

The dominant pole:

$$\tau_{p2} = \frac{r_{on} r_{op}}{r_{on} + r_{op}} \times C_T$$

The total capacitance seen at the output node is:

$$C_T = C_{GD2}(Miller) + C_{GDML2}(Miller) + C_{L1} + C_{DB2} + C_{DBML2}$$

$$C_{GD2}(Miller) = C_{GD2} \times \left(\frac{1}{2} + \mathrm{g}_m \times \frac{r_{on}r_{op}}{r_{on} + r_{op}}\right) = 14.071\ fF \times 15.0 = 211.1\ fF$$

$$C_{GDML2}(Miller) = C_{GDML2} \times \left(\frac{1}{2}\frac{\mathrm{g}_m}{\mathrm{g}_{mL}} + \frac{1}{\mathrm{g}_m \times \frac{r_{on}r_{op}}{r_{on} + r_{op}}}\right) = 26.2629\ fF \times 0.81 = 21.2\ fF$$

$$C_T = 211.1\ fF + 21.2\ fF + 10.0\ pF + 64.287\ pF + 88.707\ pF = 10.7682\ pF$$

$$\tau_p = \frac{1859.3 \times 3560.0}{1859.3 + 3560.0} \times 10.7682\ pF = 12.685\ n\ sec$$

$$\omega_p = 78.84\ Mrad/sec$$

$$f_{p2} = 12.55\ MHz$$

The non-dominant pole:

$$\omega_{px} = \frac{\mathrm{g}_{mL}}{C_x}$$

Where

$$C_x = 2C_{GSML} + C_{GDML2}(Miller) + C_{GD1}(Miller) + C_{DB1} + C_{DBML1}$$

$$C_{GD1}(Miller) = C_{GD1} \times \left(\frac{1}{2} + \frac{\mathrm{g}_m}{\mathrm{g}_{mL}}\right) = 14.071\ fF \times 2 = 28.14\ fF$$

$$C_{GDML2}(Miller) = C_{GDML2} \times \left(\frac{1}{2}\frac{\mathrm{g}_m}{\mathrm{g}_{mL}} + \mathrm{g}_m \times \frac{r_{on}r_{op}}{r_{on} + r_{op}}\right) = 26.2629\ fF \times 15.4 = 404.12\ fF$$

$$C_x = 2 \times 74.844\ fF + 404.12\ fF + 28.14\ fF + 64.287\ fF + 88.707\ fF = 734.942\ fF$$

$$\omega_{px} = \frac{8.132\ mS}{734.942\ fF} = 11.065\ G\ rad/sec$$

$$f_{px} = 1.761GHz$$

$$f_z = 2 \times 1.761GHz = 3.522GHz$$

Let's cascoding NMOS and PMOS. You might need to tweak RB slightly from previous value so that the differential amplifier has the same bias current of 2 mA total. Set CL as CL=10 pF (note: CL could represent a loading capacitance from next stage).

Q-9) Apply input signal ($\pm\frac{1}{2}V_s$) using "vsin" source, and plot output gain ($A_v = \frac{V_o}{V_s}$) versus frequency in dB-scale (5 pt).

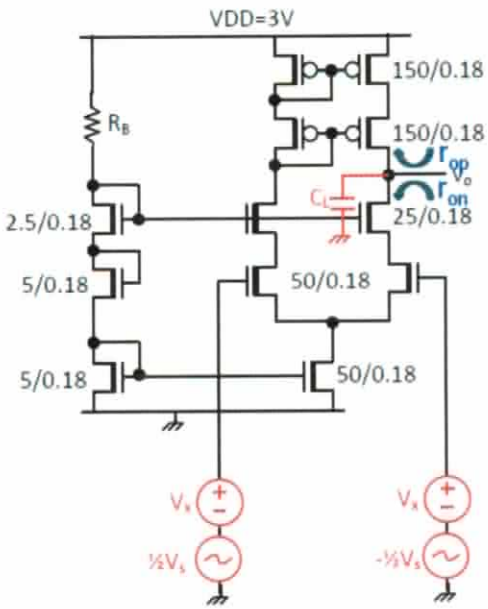


Figure 13: Q-9

Solution:

The schematic design of the circuit show in figure 13 is illustrated in figure 14. The output and input differential voltages are shown in figure 15. The maximum output voltage is almost 1.23 V when the applied differential input voltage is 10 mV. Therefore, the voltage gain is 123.21 as shown in figure 16. The voltage gain in dB is 41.812 dB as shown in figure 17.

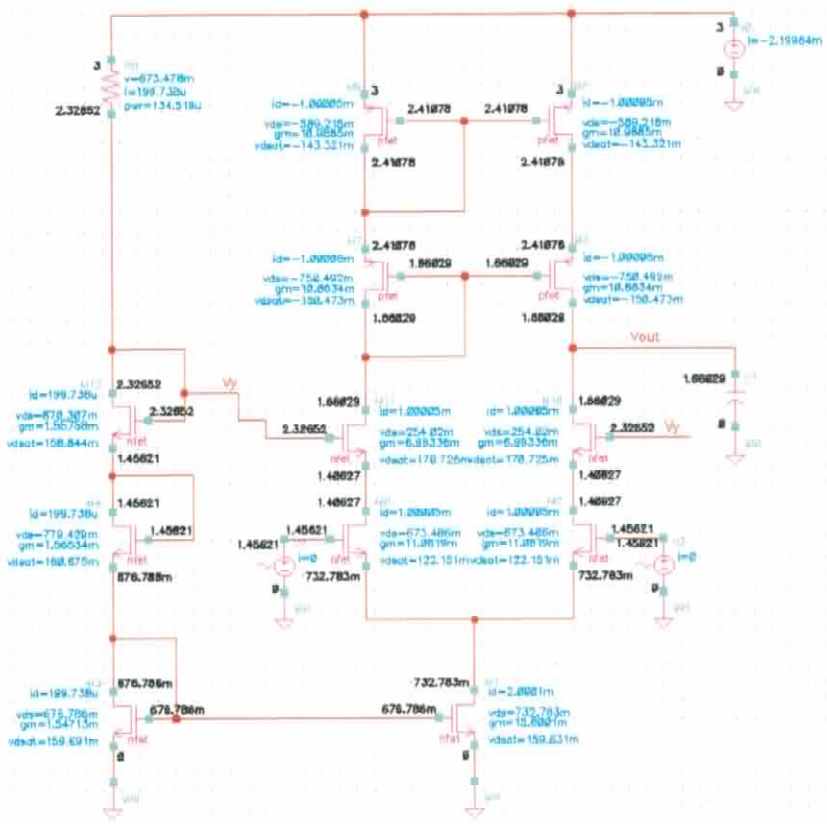


Figure 14: the schematic design of Q-9.

Figure 15: The output voltage and the input voltage versus frequency.

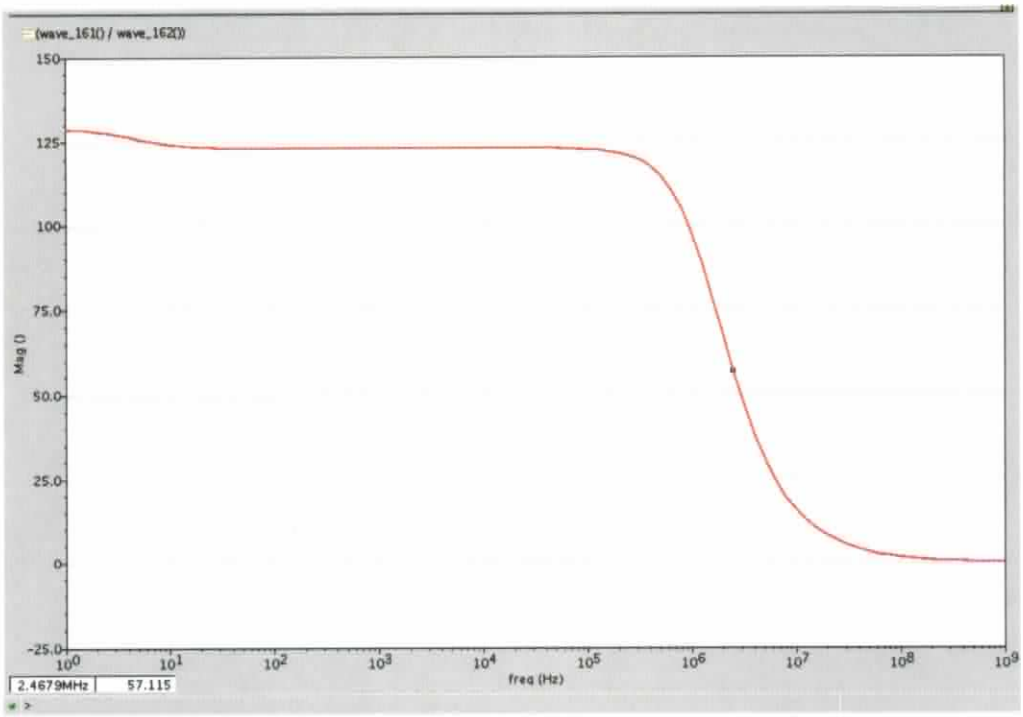


Figure 16: the voltage gain for the circuit shown in figure 14.

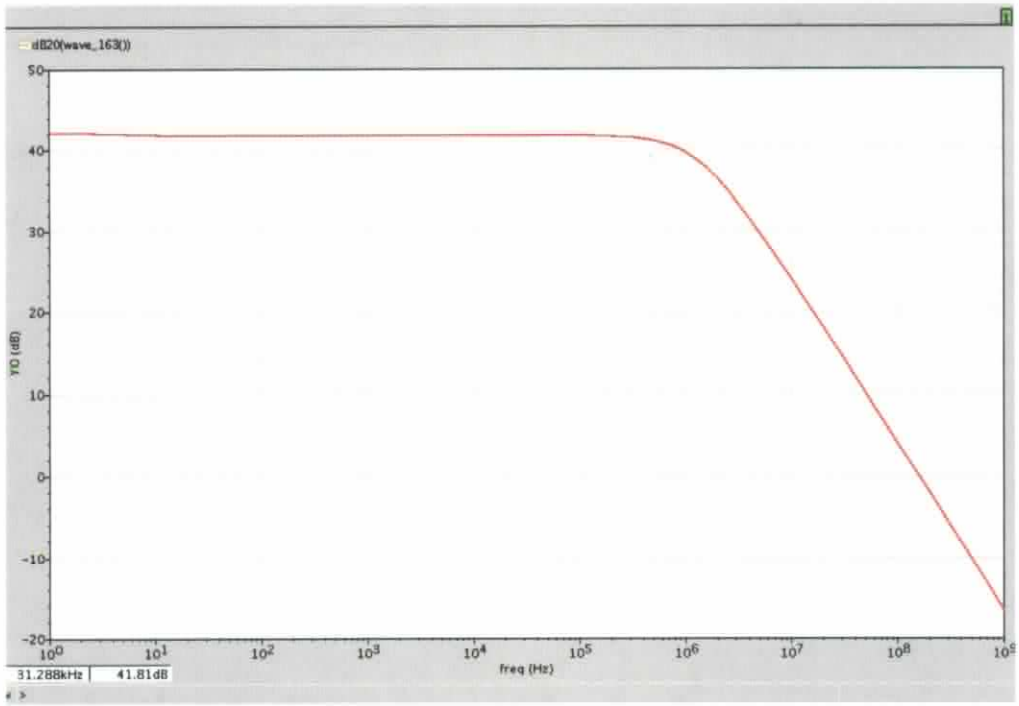


Figure 10: the voltage gain in dB for the circuit shown in figure 14.

Q-10) Calculate r_{on} , r_{op} and output resistance r_{on} // r_{op} Calculate output gain and compare your calculation with the simulated result (15 pt).

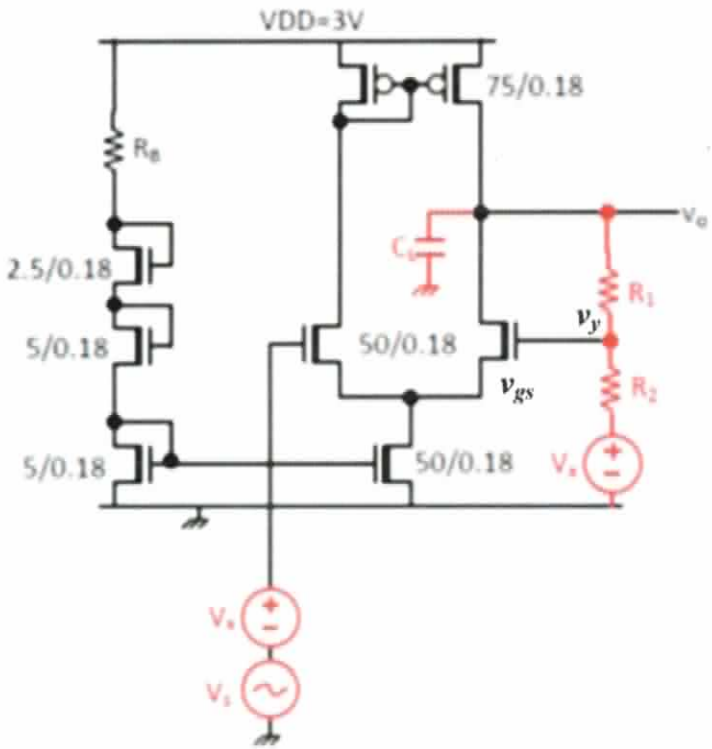
Solution:

$$r_{op} \approx r_{op1} + r_{op2} + r_{op1}(g_{mp2}r_{op2})$$
$$= 3023.04 + 3076.16 + 3023.04 \times 10.8634 \times 10^{-3} \times 3076.16 = 107.12\ K\Omega$$
$$r_{on} \approx r_{on1} + r_{on2} + r_{on1}(g_{mp2}r_{on2})$$
$$= 1502.23 + 967.214 + 1502.23 \times 6.9933 \times 10^{-3} \times 967.214 = 12.634\ K\Omega$$
$$r_{on}//r_{op} = 11.3015\ K\Omega$$
$$A_v = g_m(r_{on}//r_{op}) = 11.082 \times 10^{-3} \times 11.3015\ K\Omega = 125.2$$
$$A_v = 41.95\ dB$$

The calculated gain is very close to the simulated gain.

Use the same DC conditions as in Step-(3), and apply feedback resistors, R1 and R2. Set CL as CL=10 pF (note: CL could represent a loading capacitance from next stage).

Q-11) Use virtual grounding concept and calculate R_1 and R_2 so that the gain ($A_v = \frac{V_o}{V_s} = \frac{1}{f}$) can be 6 dB (5pt).



Solution:

To use virtual ground concept, consider v_{gs} =0. The leads to v_y =v_s.
Therefore, current path from the output to the ground, and it can be calculated as:

$$i_y = \frac{v_s}{R_2}$$

$$v_o = v_s + \frac{R_1}{R_2} v_s$$

$$A_v = \frac{V_o}{V_s} = 1 + \frac{R_1}{R_2}$$

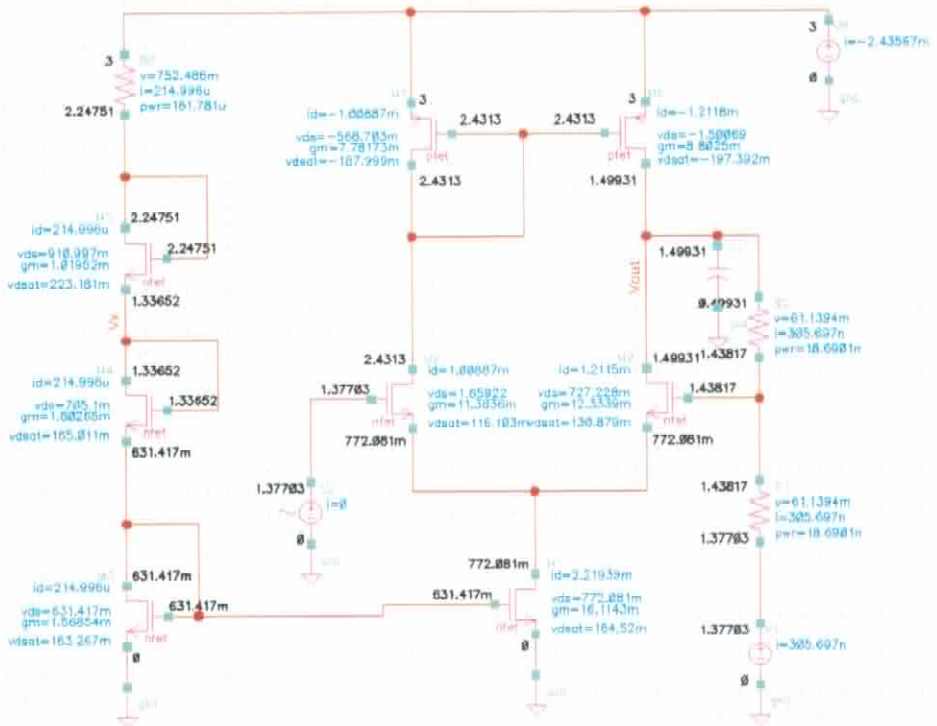
$$A_v = 6\,dB \rightarrow A_v = 2.0$$

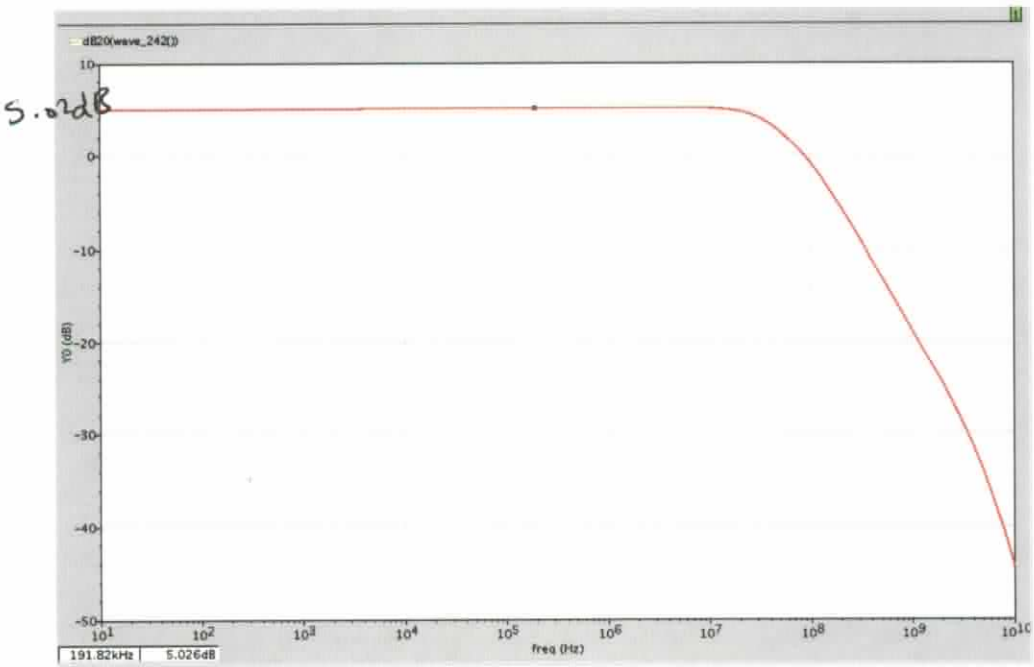
$$1 + \frac{R_1}{R_2} = 2$$

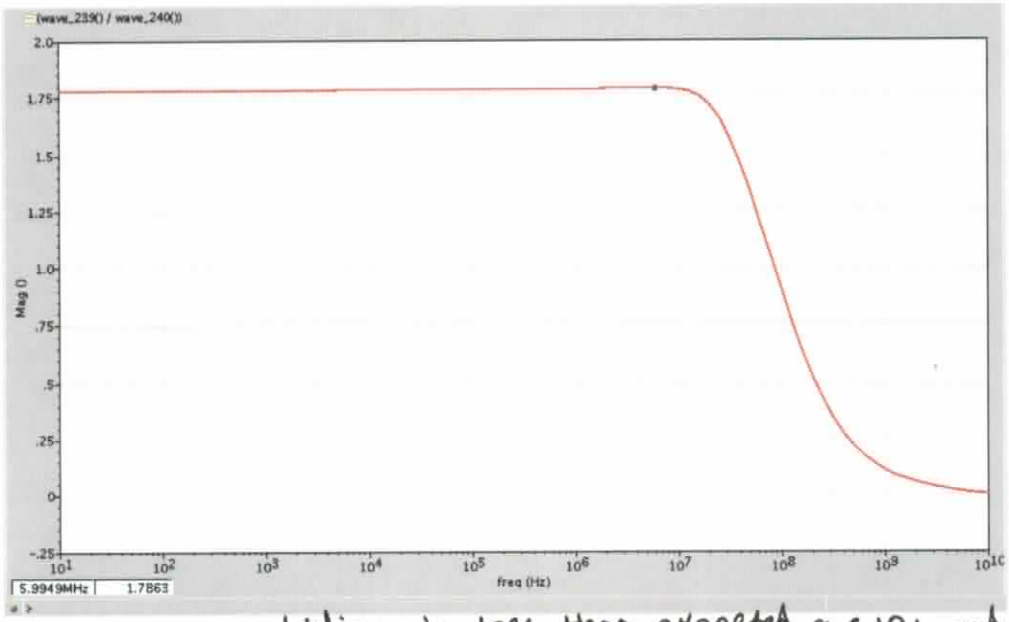
$$R_1 = R_2$$

Let us choose the resistors to be 200KΩ.

Q-12) Simulate your design and plot gain curve versus frequency (5 pt). Note: your simulated gain might be smaller than the target 6dB (why?)







The gain of the amplifier is less than expected a 6dB!, and this is because of small loop gain. That is why we should include the correction factor ($\frac{T}{T+1}$) to the virtual ground gain. If the loop gain is infinite, then the virtual ground gain will be ~~eq~~ the ~~the~~ exact gain of the Amp.

Use the same DC conditions as in Step-(3), and set feedback resistors, R1 and R2, as you designed in the previous step. Set CL as CL=10 pF (note: CL could represent a loading capacitance from next stage).

Q-13) Calculate and simulate feedback loop gain ($T = \frac{V_{to}}{V_t}$) (10 pt).

Note: Your loop gain (T) might not be large enough in this design, and there could be some error in the overall closed-loop gain $\left(= \frac{1}{f}\right)$which is calculated based on virtual grounding technique. To get an exact gain, you can multiply a correction factor ($= \frac{T}{1+T}$) , to the gain based on virtual grounding technique. To improve loop gain, cascoding design is preferable.

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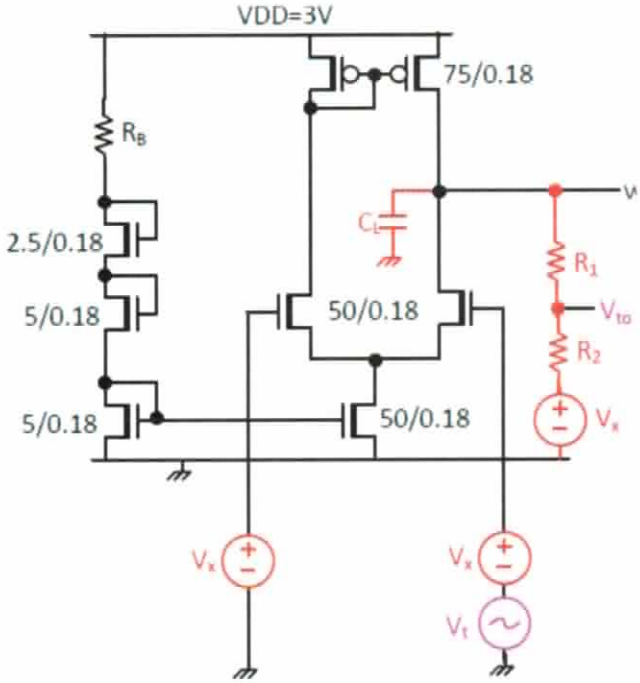
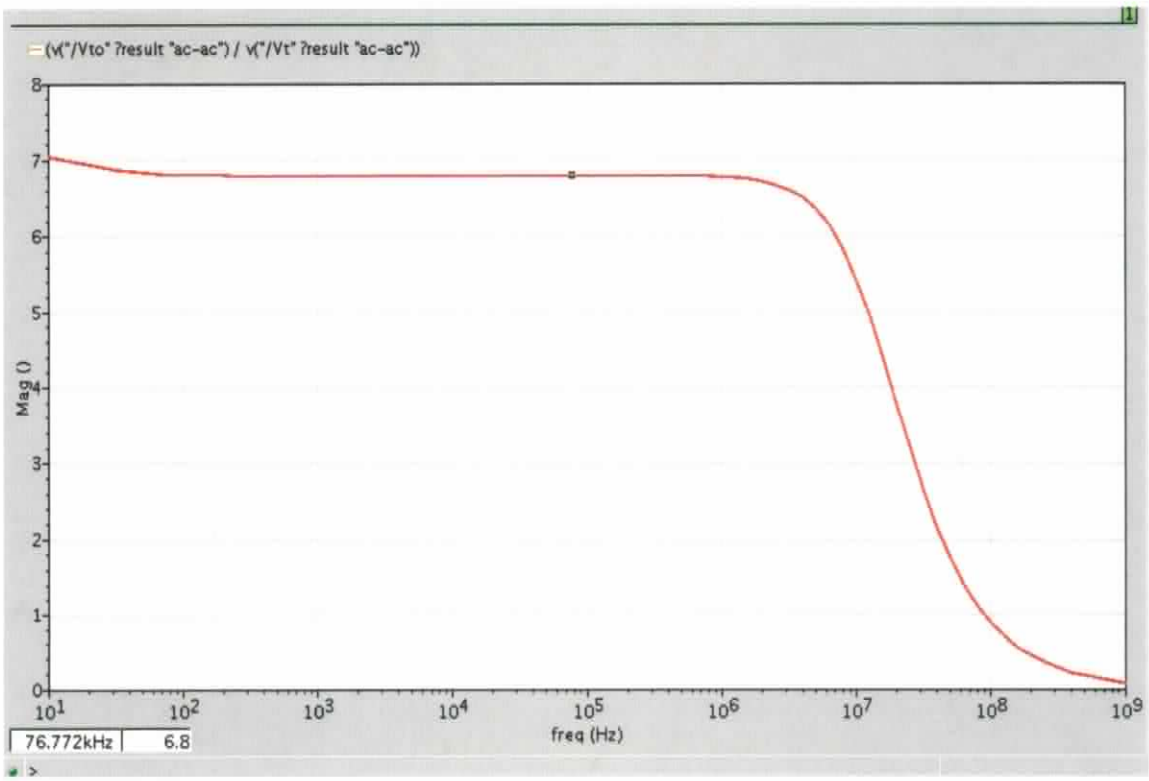

VDD=3V
75/0.18
R_B
2.5/0.18
5/0.18
5/0.18
50/0.18
50/0.18
C_L
R_1
V_{to}
R_2
V_x
V_x
V_x
V_t


(v("/Vto" ?result "ac-ac") / v("/Vt" ?result "ac-ac"))
Mag ()
freq (Hz)
76.772kHz
6.8

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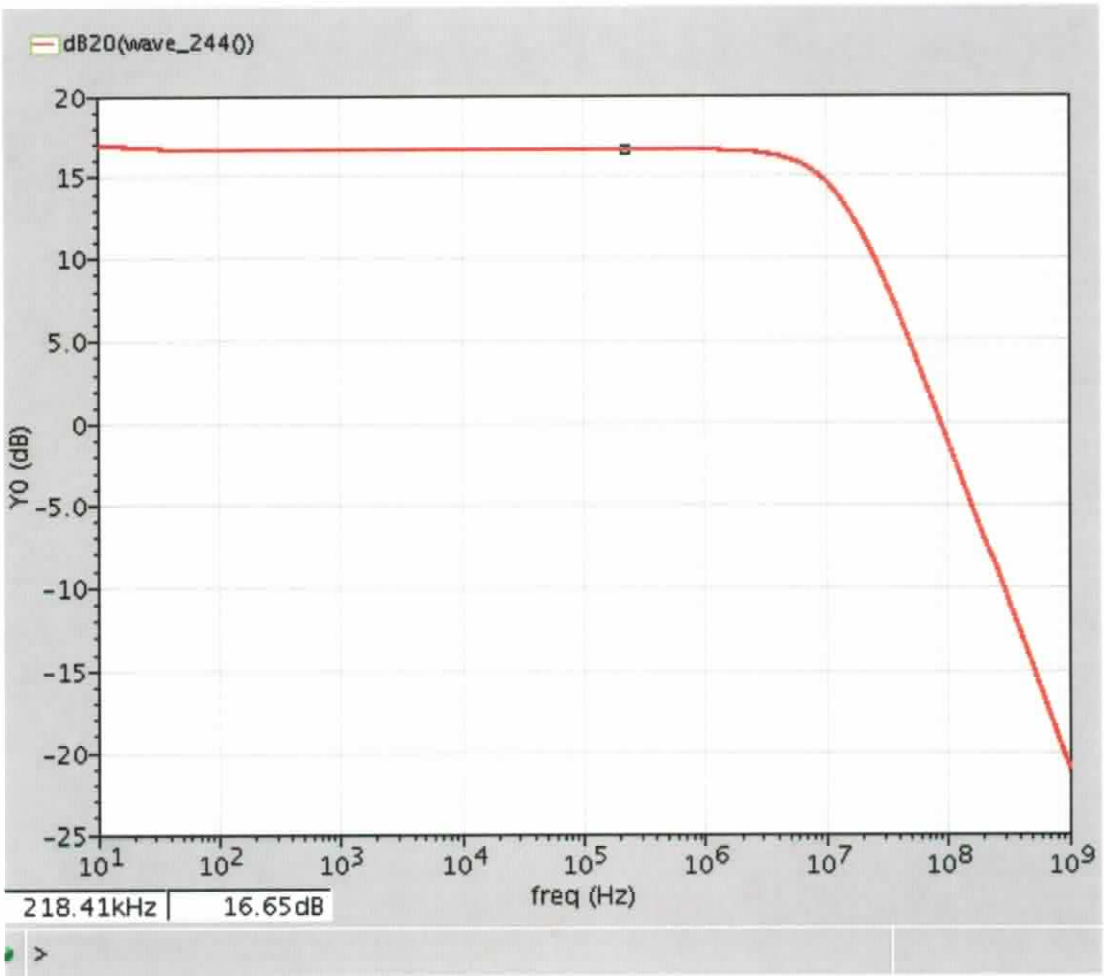

The loop gain can be calculated as the following:

$$T = \frac{v_o}{v_t} \times \frac{v_{ot}}{v_o} =$$

$$\frac{v_o}{v_t} = gm \times \left(r_{op}//r_{on}//(R_1 + R_2)\right) = 11.99 \times 10^{-3}(3566.84//1859.81//400k) = 14.624$$

$$\frac{v_{ot}}{v_o} = \frac{R_2}{R_1 + R_2} = 0.5$$

$$T = \frac{v_o}{v_t} \times \frac{v_{ot}}{v_o} = 14.624 \times 0.5 = 7.312 \quad \rightarrow T = 17.28$$

The calculated loop gain is almost the same as the simulated one.

The gain of the amplifier:

$$Av = \left(\frac{R_1}{R_2} + 1\right) \frac{T}{T+1} = 5.1 \text{ dB}$$

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