CMOS-SOI-MEMS Transistor (TeraMOS) for Terahertz Imaging

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Abstract **— This study presents a new sensor for Terahertz Imaging, dubbed here as TeraMOS, which is based on several leading technologies: CMOS-SOI (Silicon on Insulator), MEMS (Micro Electro Mechanical Systems) and Terahertz Photonics. The paper focuses on the electrical characterization of CMOS-SOI "virgin" (unreleased) transistors fabricated in the IBM 0.18µm RF CMOS-SOI advanced process. By applying MEMS post processing to thermally isolate the transistors, the resulting CMOS-SOI-MEMS transistors become highly sensitive active bolometers - the TeraMOS sensors. The measured Temperature Coefficient of Current (TCC) as a function of temperature, gate voltage and drain current is presented. A new suggested figure of merit for the TeraMOS sensors is defined by $TCC^2 \cdot I$ and measured values of it are presented.**

Index Terms **— CMOS, MOS transistors, Silicon-on-Insulator (SOI), Temperature Coefficient of Current (TCC), Terahertz sensors.**

I. State of the Art and the TeraMOS Motivation

High performance, low-cost passive imaging at approximately 0.5-1.5 THz has well-established benefits but has been little explored because current state of the art sensors, which are based on bolometers, are not sufficiently sensitive, unless we deal with superconducting bolometers operating at ~4K. There is low but adequate radiation from terrestrial bodies at 300K to allow passive remote sensing as well as high-resolution images of hidden objects covered under clothing or other materials, provided that higher sensitive sensors will be available. Applications include concealed weapon detection, surveillance cameras, astronomy, non-destructive material testing, as well as ample bio and medical applications. For example, THz imaging can distinguish between normal skin tissue and tumors even when a trained dermatologist cannot.

This study presents a new sensor, dubbed here as TeraMOS, which is based on several leading technologies: CMOS-SOI (Silicon on Insulator), MEMS (Micro Electro Mechanical Systems) and Terahertz Photonics. By introducing a completely new type of THz sensors, which may be directly integrated with the on-chip CMOS-SOI readout circuitry, we expect to achieve a breakthrough in performance and cost of THz passive imaging systems. The low cost is emphasized here because this will allow the deployment of a large number of such focal plane array (FPA) imagers in point-of-care medical clinics (dermatologists for example) as well as in crowded places, providing highly efficient response to terrorists' threats.

II. TeraMOS Principle of Operation and Performance

The new proposed TeraMOS sensor [1],[2] is a thermally isolated micromachined (released) CMOS transistor operating at subthreshold, as shown schematically in Fig.1.

The TeraMOS is a thermal sensor, similar to a bolometer, but with inherent advantages since it is an *active device* and is fabricated in a well established and matured CMOS technology. Incident blackbody THz radiation heats the transistors by approximately $\Delta T(t) = \eta P_0 / G_{th}\left(1 - e^{-t/\tau}\right)$. The temperature increase induces an increase in the transistor current, which is detected by the readout. In order to correspond to a video format, $\tau_{th} = C_{th} / G_{th}$ of ~20-70msec is required. Since a low G_{th} is essential for achieving enough sensitivity, a corresponding reduction of C_{th} is also needed (see below).

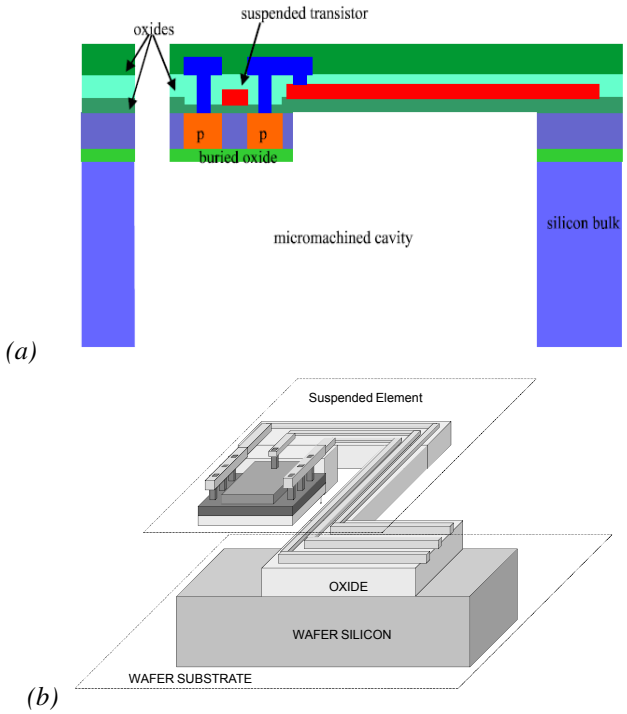

Fig.1. A schematic view of the TeraMOS sensor that can be obtained in a standard CMOS-SOI process after post-CMOS MEMS processing; (a) a schematic cross section of a suspended (released) transistor (b) a perspective view

The use of such a transistor as the sensing element for IR radiation was previously proposed and dubbed as TMOS [3], and the advantages and performance of this "active bolometer" are reported in [4]-[7]. An optical image of a pixel with a suspended (released) TMOS after MEMS post-CMOS processing is reported in [5]. The micromachined, thermally isolated transistor is connected to the silicon chip by a holding arm, which provides the electrical contacts and the thermal isolation. The thinned transistor (few microns thick) is suspended in vacuum to reduce its thermal conductivity G_{th}.

The available signal for passive imaging in the Terahertz region is lower by approximately two orders of magnitude compared to the IR signal. Furthermore, the pixel dimension of the TeraMOS is of the order of the wavelength, ranging between 200μm-600μm, in contrast to the IR wavelength of 8-14μm. Hence, the TeraMOS sensors introduce several unique challenges compared to the TMOS sensors.

Fig. 2 exhibits the design of the TeraMOS sensor with a perforated platform, constructed according to the principles of the Technion invention. The absorbing platform (brown color) has dimensions $A \times B$ while the TeraMOS sensor is $a \times b$ (the blue square).

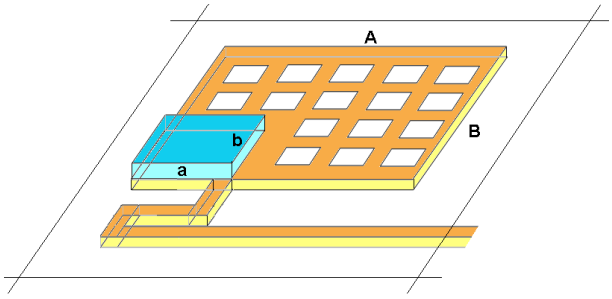

Fig. 2. Illustration of a typical pixel of the TeraMOS. The pixel is comprised of a perforated platform and a sensing transistor positioned in a corner

The perforated platform (membrane) absorbs the radiation by direct coupling: a "$\lambda/4$" Salisbury screen absorber is implemented with the use of a separate backside reflector die, in addition to the TeraMOS FPA die. In this design, the transistor is connected in a diode-like configuration – the gate and drain are shortened and the source and bulk are shortened. This configuration reduces the width of the holding arm to the possible minimum provided by the technology, so that low thermal conductivity and better fill factor are obtained; three terminal devices have also been designed, but will not be discussed in the current paper. The platform is etched to minimize the pixel's thermal mass, which needs to be very low. The sensing transistor's dimensions are significantly smaller than those of the membrane. This is due to the fact that, since the transistor must include in addition to active silicon the polysilicon gate and the metallic contacts, once released it will be much ticker than the rest. By contrast, the platform cross section is based just on the buried oxide and active silicon.

In order to meet the required signal to noise of the TeraMOS sensor, an advanced CMOS-SOI technology is needed. Furthermore, it is possible that unlike the TMOS sensor, the TeraMOS will need to be cooled down to 77K.

This paper presents preliminary experimental results of the CMOS-SOI transistors, fabricated using the IBM 0.18μm RF CMOS-SOI process [8], which are designed to perform as TeraMOS sensors after additional MEMS post processing.

III. TCC – The Temperature Coefficient of Current of the IBM CMOS-SOI Transistors

The temperature coefficient of current, TCC, is defined as the percentage change of current per degree ($TCC = (dI_{DS}/dT)/I_{DS}$). In the case of TeraMOS transistors, TCC is a significant figure-of-merit, corresponding to the TCR (temperature coefficient of resistance) of bolometers. The temperature coefficient of current (TCC) of CMOS-SOI transistors in the three major regions of operation -linear, saturation and subthreshold was studied analytically and experimentally in [4]. It was shown that at subthreshold the TCC is highest. This is expected since in this operation region the channel conduction is mainly governed by diffusion, which is a thermal process with a strong exponential dependence on temperature, while in the other regions the conduction is governed by drift. For long-channel transistors, the current in the subthreshold region is given by [9]:

$$I_{DS} = \mu^* C_{ox} \left(\frac{W}{L}\right)\left(\frac{kT}{q}\right)^2 (n-1) e^{\frac{q}{nkT}(V_{GS}-V_T)}\left(1-e^{-\frac{q}{kT}V_{DS}}\right) \quad (1)$$

where $n = 1+(C_s + C_{it})/C_{ox}$ and C_s, C_{it} and C_{ox} are the semiconductor, fast surface states, and oxide capacitance respectively; W and L are the gate's width and length of the MOSFET.

By neglecting the drain-source voltage term, which is correct for values higher than a few kT/q, neglecting the changes of n with the temperature, and differentiating with respect to the temperature, assuming for simplicity that $(d\mu/dT)/\mu \cong -1/T$, we obtain at subthreshold for long-channel transistors:

$$TCC = \frac{1}{T} - \frac{q}{nkT^2}(V_{GS}-V_T) - \frac{q}{nkT}\frac{dV_T}{dT} \quad (2)$$

The analysis presented here ignores short channel effects and the temperature dependence of n. In order to obtain a simple simulation tool that can predict the thermal effects of the IBM CMOS-SOI 0.18μm process [8] , we have used expression (2) with a correction introduced by the experimental values for dV_T/dT and $n(T)$. As expected for n-channel MOSFETs, dV_T/dT is negative, with a typical value of -1mV/K. The linearly fitted n is $n(T) \approx 1.47 + 0.001 \cdot T[^\circ C]$.

The current-voltage characteristics of the as-processed ("virgin") transistor were extensively measured as a function of temperature. The measurements were performed with an automatic prober system with hot chuck, and a high temperature probe card. The devices were measured in the temperature range of 20°C-70°C with 2°C steps.

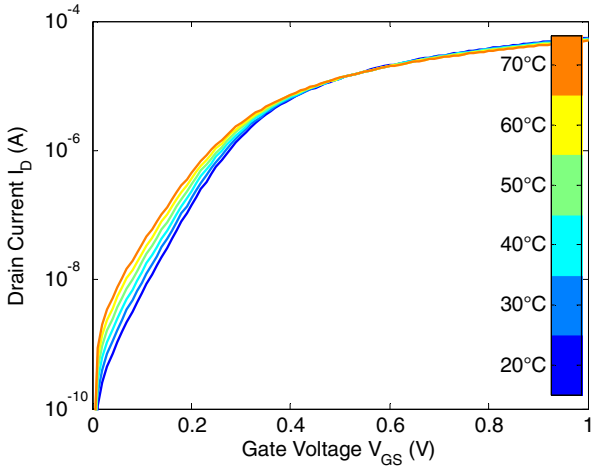

Fig. 3. Measured current-voltage characteristics, compared for several temperatures. The "virgin" (as-processed) n-channel transistor has W/L=5µm/0.5µm

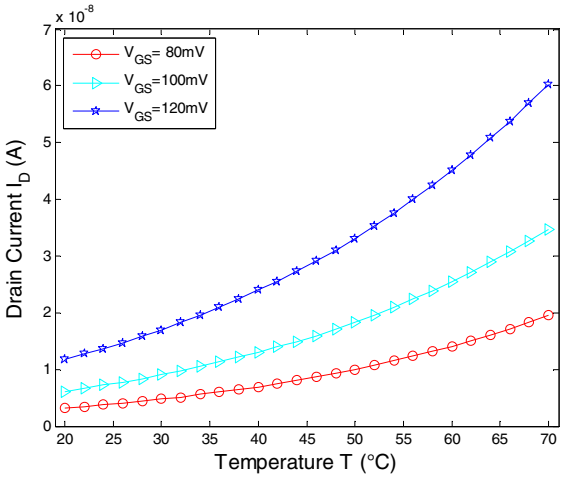

Fig. 4. Measured drain current as a function of the temperature of the "virgin" transistor W/L=5µm /0.5µm

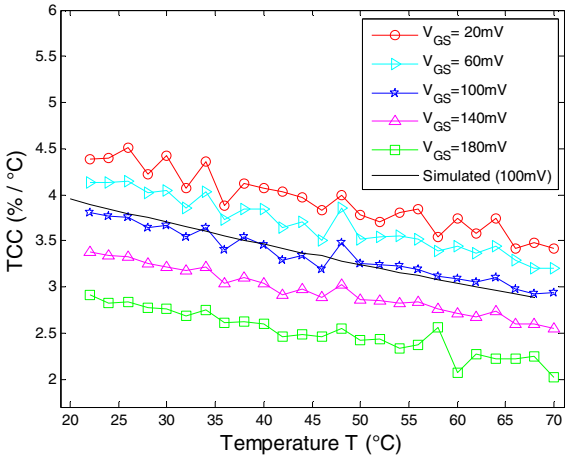

Fig. 5. Measured TCC as a function of temperature for different gate voltage values for the transistor W/L=5µm /0.5µm

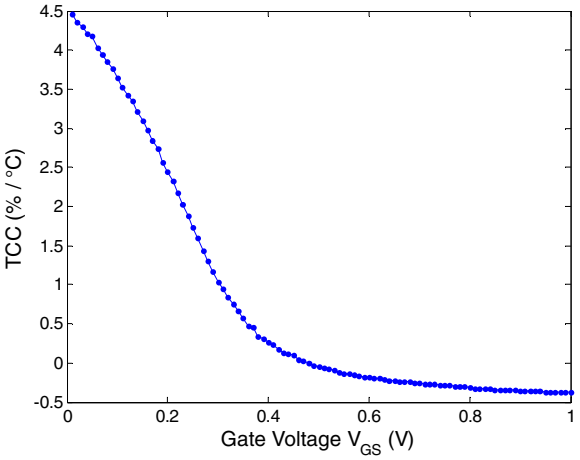

Fig. 6. Measured TCC as a function of gate voltage for the "virgin" transistor W/L=5µm /0.5µm at 32°C

At each temperature, gate and drain voltage sweeps were conducted in the range of 0-1V, at steps of 0.02V. Fig. 3 exhibits the measured data for a typical transistor. The measurements yield $n(T)$ as well as the experimental value for dV_T / dT.

The measured current versus temperature for gate voltages corresponding to subthreshold is shown in Fig. 4.

Fig. 5 exhibits the measured TCC as a function of temperature for the "virgin" TeraMOS transistor with W/L=5µm/0.5µm, prior to the MEMS post processing. The simulated TCC, according to (2), is also shown. A typical TCC of the order of 4% is obtained at deep subthreshold. A higher TCC of 10% was previously obtained in another silicon process for higher threshold voltage transistors which allow for a deeper subthreshold domain. The temperature sensitivity of the TCC for the IBM CMOS-SOI transistors is about 0.01 %/°C^2. This moderate and known change in TCC allows for easy temperature gain compensation.

The TCC is also plotted against the gate voltage Vgs (Fig. 6) and drain-source current I_{DS} (Fig. 7) at a fixed temperature. These graphs show that TCC improves as the transistors enter deeper subthreshold.

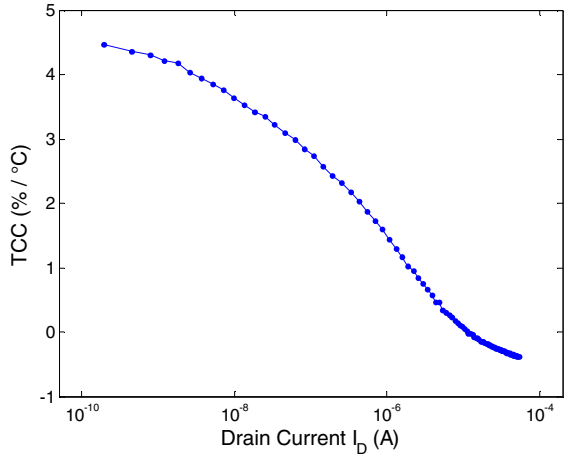

Fig. 7. Measured TCC as a function of the drain-source current I_{DS} for the "virgin" transistor W/L=5µm /0.5µm at 32°C

IV. Optimizing the Operation Point of the TeraMOS

Although the TCC is an important parameter to characterize the thermal response of the transistors, different figures of merit may be needed to determine the optimal operation point of the TeraMOS transistors. We hereby suggest the figure of merit expressed by $TCC^2 \cdot I_{DS}$ - namely the product of the square of the TCC and the DC current.

The Noise Equivalent Power (NEP), which is the smallest signal that the sensor can detect, is expressed by $NEP = \sqrt{i_n^2} / R_i$ [W] where the current responsivity is given by $R_i = TCC \cdot I_{DS} \cdot \eta / G_{th}$ [A/W]. TCC is the Temperature Coefficient of Current, I_{DS} is the DC current at the operation point, G_{th} is the thermal conductivity and η is the absorption efficiency; $\sqrt{i_n^2}$ is the RMS value of the current noise, namely the standard deviation of the detector current where all the noise sources are taken into account.

The contributions to the sensor's noise come from the electrical noise sources and the fundamental thermal fluctuation noise. The current noise (namely the statistical variance of the detector current) of a TeraMOS in the subthreshold region, neglecting the thermal radiation noise, can be written as a sum of temperature fluctuation noise, shot noise and 1/f noise:

$$\overline{i_n^2} = \frac{kT_0^2 \cdot TCC^2 \cdot I_{DS}^2}{\tau_{th} \cdot G_{th}} + 2qI_{DS}B + K_f I_{DS}^2 \ln\left(\frac{f_2}{f_1}\right) \quad (3)$$

where k is Boltzmann's constant, T_0 is the average temperature, τ_{th} is the thermal time constant, G_{th} is the thermal conductivity of the structure, I_{DS} is the DC current through the TeraMOS transistor. K_f is the technological 1/f noise parameter, which depends on the transistor operation region as well as on the transistor channel area W·L [10]. f_2 and f_1 are the frequencies corresponding to the electrical bandwidth of the measurement and the video format rate.

Accordingly, the noise equivalent power (NEP) can be expressed by:

$$NEP = \sqrt{\frac{kT^2 G_{th}}{\eta^2 \tau_{th}} + \frac{2qG_{th}^2 B}{(TCC)^2 \eta^2 I_{DS}} + \frac{K_f G_{th}^2 \ln\frac{f_2}{f_1}}{(TCC)^2 \eta^2}}) \quad (4)$$

The 1/f noise can be reduced by well-known circuit methods like correlated double sampling. The temperature noise may be reduced either by reducing the thermal conductivity or the temperature. If we expect the shot noise to be largely dominant over the other sources, it is easily seen from (4) that the optimal operation point is the gate voltage that yields the maximal $TCC^2 \cdot I_{DS}$.

Fig. 8 exhibits the measured $TCC^2 \cdot I_{DS}$ as a function of gate voltage for several "virgin" transistors with different W/L ratios. The graph clearly indicates that, for each transistor, there is an optimal operation point near subthreshold, where the new figure of merit, based on the product of the square of the TCC and the DC operation current, reaches a maximum. This maximum is observed near the threshold voltage of the transistors.

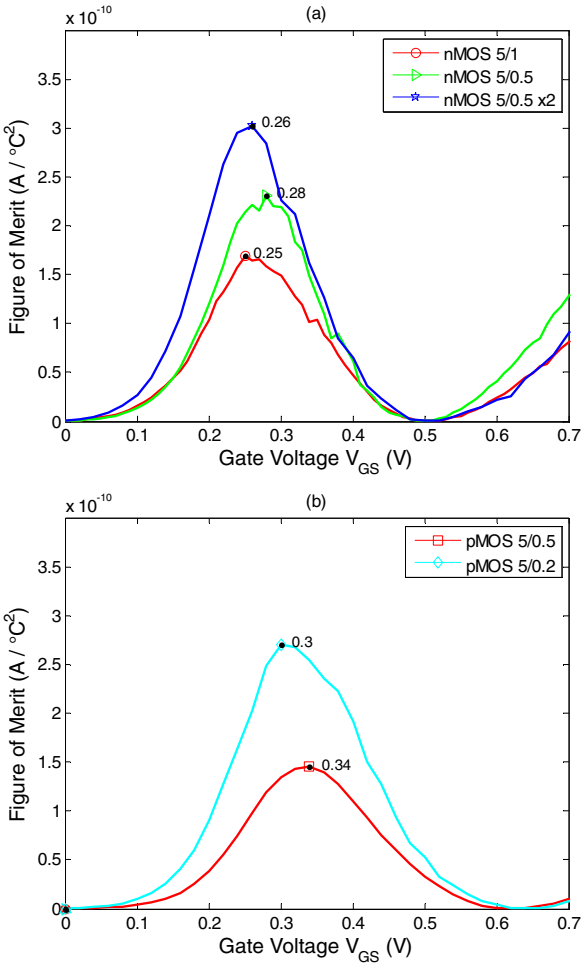

Fig. 8. (a) and (b): the chosen figure of merit for TeraMOS transistors with various form factors W/L as a function of Vgs at 34°C

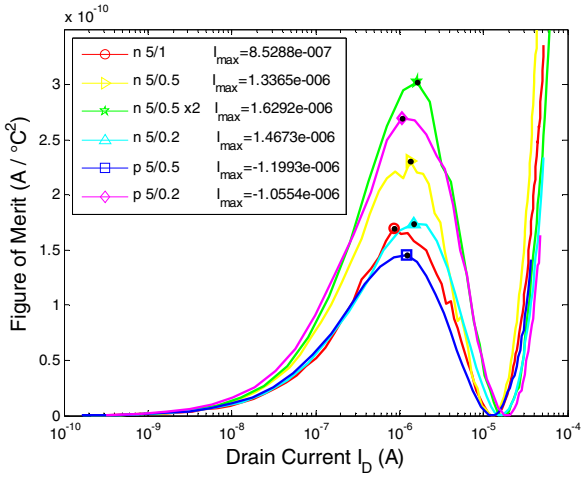

Fig. 9. The chosen figure of merit for TeraMOS transistors with various form factors as a function of I_{DS} at 34°C

Fig. 9 exhibits the chosen figure of merit at the maximal point as a function of the transistor DC current. It is easily seen that, by increasing the operation current through the choice of larger W/L, the figure of merit improves. However, by increasing the DC current, also the self heating of the transistors is increased – even for these virgin, unreleased transistors. This affects the value of the threshold voltage,

which is reduced as the temperature is increased (dV_T / dT of n-MOS is negative). Hence, the different transistors of Fig. 8, each with a different W/L and a different drain current at the maximum, exhibit an optimal work point at different gate voltages. It also follows that larger transistors have a larger figure of merit because their TCC is higher when their gate bias shifts away from Vt into deeper subthreshold. According to Fig. 9, the chosen figure of merit, for currents close to 10^{-6}A, is $TCC^2 \cdot I_{DS} \cong 3 \cdot 10^{-10}$.

The transistor's self heating is estimated for pulses by $\Delta T \cong \left(I_{DS} \cdot V_{DS} \cdot t_{measure}\right) / C_{th}$, and for steady state operation by $\Delta T \cong \left(I_{DS} \cdot V_{DS}\right) / G_{th}$. The thermal capacitance C_{th} is assumed to be $4 \cdot 10^{-10}$ J/K and $t_{measure}$ is determined by the measurement bandwidth. Thus, a bandwidth of 30Hz and $G_{th} \cong 3 \cdot 10^{-8}$ W/K, for a current of 1μA and drain voltage around 0.1V, yields a temperature increase of the order of ~4K, which is adequate.

V. Expected Electro-Optical Performance

The NEP, estimated with equation (4) for the case of a dominant shot noise and assuming that we can reach a thermal conductivity of $G_{th} \cong 3 \cdot 10^{-8}$ W/K, absorption efficiency of $\eta = 0.85$, noise bandwidth B=30Hz, bias current $I_{DS} \cong 1\mu A$ and $TCC^2 \cdot I_{DS} \cong 3 \cdot 10^{-10}$ A/°C^2, is about 6pW at room temperature.

The NEP together with the pixel area and Fill Factor determine the expected NETD - Noise Equivalent Temperature Difference. The NETD is expressed by:

$$\left(NETD\right) = \left(NEP\right) \cdot \frac{\left(4 f_{\#}^2 + 1\right)}{A_D FF \frac{d}{dT}\left(P\right)_{\lambda_1 - \lambda_2}} \tag{4}$$

Assuming $\left(dP / dT\right)\Big|_{0.5-1.5THz} = 1 \cdot 10^{-7} W / cm^2 K$, FF (Fill Factor) of the order of 0.85, f-number $f_{\#} = 1$ and pixel size of the order of $(200\mu m)^2$, and assuming that we can reach the above given NEP of 6 pWatt, pixels may exhibit NETD of less than 1 degree.

VI. Summary

The present study focuses on the electrical characterization of "virgin" (unreleased) transistors fabricated in the IBM 0.18μm RF CMOS-SOI process.

The novel concept of a thermally isolated MOS transistor (TeraMOS) for Terahertz sensing is presented. The main novel features of the TeraMOS are the following: the use of a MOS transistor, *operating at subthreshold*, as an *active device* for terahertz sensing and the implementation of the TeraMOS in standard CMOS-SOI, followed by MEMS post processing. Operation at subthreshold is preferred since the conduction mechanism at subthreshold is based on diffusion, which is very sensitive to temperature variations. We have defined a figure of merit given by $TCC^2 \cdot I_{DS}$ which obtains larger values as the operating current is increased till reaching a maximal value after which it falls back again. However, higher currents induce self heating which may require pulsed operation posing a tradeoff between the operation DC current and the measurement bandwidth. At subthreshold, the TCC is higher and a lower noise is contributed by the MOS transistor. SOI technology is proposed for TeraMOS detectors since thermal isolation by MEMS is achieved much easier than with regular CMOS technology, due to the fact that in CMOS-SOI the oxide provides an etch stop for the backside removal of the substrate by DRIE -Deep Reactive Ion Etching.

A significant additional research is needed to demonstrate the feasibility of the TeraMOS sensors, the highest challenge being the un-cooled operation for passive THz imaging at normal video rates.

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