SiGe Heterojunction Bipolar Transistors and Circuits Toward Terahertz Communication Applications

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***Abstract*—The relatively less exploited terahertz band possesses great potential for a variety of important applications, including communication applications that would benefit from the enormous bandwidth within the terahertz spectrum. This paper overviews an approach toward terahertz applications based on SiGe heterojunction bipolar transistor (HBT) technology, focusing on broad-band communication applications. The design, characteristics, and reliability of SiGe HBTs exhibiting record f_T of 375 GHz and associated $f_{\max}$ of 210 GHz are presented. The impact of device optimization on noise characteristics is described for both low-frequency and broad-band noise. Circuit implementations of SiGe technologies are demonstrated with selected circuit blocks for broad-band communication systems, including a 3.9-ps emitter coupled logic ring oscillator, a 100-GHz frequency divider, 40-GHz voltage-controlled oscillator, and a 70-Gb/s 4:1 multiplexer. With no visible limitation for further enhancement of device speed at hand, the march toward terahertz band with Si-based technology will continue for the foreseeable future.**

***Index Terms*—BiCMOS integrated circuits, communication systems, heterojunction bipolar transistors (HBTs), high-speed integrated circuits.**

I. Introduction

SEMICONDUCTOR devices have enjoyed enormous success in two separate ranges of the electromagnetic spectrum: the dc-to-microwave band and the optical band, exploiting their versatile electrical and optical characteristics, respectively. Located roughly between these two bands is the terahertz range. Compared to its neighboring bands that abound in applications and have been explored extensively, this portion of the spectrum has been relatively less exploited, mainly because it lacks suitable devices to properly handle the signals in this range. The terahertz band covers a number of important applications such as medical and biological imaging [1], radio astronomy [2], upper atmosphere study [3], plasma diagnostics [4], and, most recently, broad-band communication systems that would benefit from virtually infinite bandwidth with terahertz spectrum. Therefore, the extension of the application spectrum of semiconductor devices into this range is of growing importance and interest. There exist two possible approaches for such extension of the application front. One is the upward penetration from electrical operation, which is limited by the control over spatial carrier transport for reduced transit times. The other is the downward penetration from optical operation, which is limited by the control over carrier transitions across narrowly located energy states for reduced photon energies. This paper presents one of such efforts based on the first approach, which is basically an effort to increase the bandwidth of devices, primarily for broad-band communication applications.

A few types of semiconductor diodes, in fact, have already been widely used in terahertz applications. GaAs Schottky barrier diodes have been a key component in terahertz heterodyne receivers, serving as a mixer for down-conversion of terahertz to gigahertz signals [5], [6]. Impact avalanche transit time (IMPATT) and Gunn diodes [7] have been employed as power generators in terahertz transmitters and local oscillators in terahertz receivers, usually combined with frequency multipliers based on GaAs Schottky barrier varactors. However, in order to implement complex and sophisticated signal-processing functions on integrated systems by switching and amplification action, it is imperative to employ active semiconductor devices: *transistors*. There have been continuous and extensive efforts to improve the operation frequency of transistors, as illustrated in Fig. 1, which shows the evolution of the best-achieved cutoff frequency f_T (frequency where the current gain becomes unity) for various transistor types over recent years [8]–[24]. As manifested by the trend, the best performing devices today are now penetrating into the hundreds of gigahertz range, indicating the impending terahertz era of transistors. It should be noted that, in terms of another measure of device speed, maximum oscillation frequency $f_{\max}$ (frequency where the power gain becomes unity), the possibility of terahertz operation of transistors has already been demonstrated based on a rather exotic structure of transferred substrate [25].

It is notable from Fig. 1 that Si-based devices, which have long been considered slower than III–V devices, have exhibited quite a remarkable speed enhancement in recent years. As a matter of fact, Si-based bipolar transistors have begun to outperform their III–V counterpart heterojunction bipolar transistors (HBTs) in terms of f_T, owing to the latest performance improvement, as will be detailed in this paper. Over the past

Manuscript received May 5, 2003. This work was supported in part by the Defense Advanced Research Projects Agency under SPAWAR Contract N66001-02-C-8014.

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Digital Object Identifier 10.1109/TMTT.2004.835984

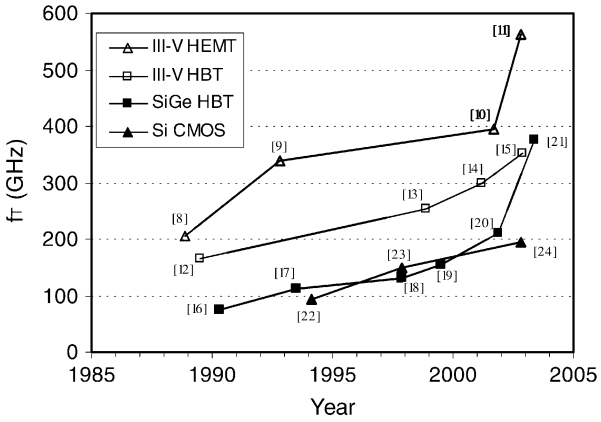

Fig. 1. Trend of the best-achieved f_T for various transistors. The numbers indicate corresponding reference.

decade, Si-based bipolar transistors have experienced a significant speed enhancement with the advent of Si-based bandgap engineering, which was enabled by the growth of high-quality SiGe alloy films on Si substrate. By incorporating epitaxial SiGe alloy to the base layer, the transit time across the base was significantly reduced due to the quasi-electric field established across the base with graded bandgap. In addition, the reduced bandgap in the base greatly improved the emitter efficiency, allowing heavier base doping concentration and, thus, narrower base width without punch-through, resulting in a further reduction of the base transit time. As a result, SiGe HBTs typically exhibit significantly higher f_T than the traditional Si homojunction bipolar transistors.

These enabling factors for speed improvement, however, do not fully explain the observed comparable or even superior performance recently achieved by SiGe HBTs compared to that of III–V HBTs. The benefits of the bandgap engineering listed above apply exactly to III–V devices as well and, furthermore, III–V devices benefit from the well-known material advantages such as higher mobility and more pronounced ballistic carrier transport [26], [27]. In fact, the principal advantage of Si devices comes from its extremely aggressive scaling and extensively optimized structure, which are enabled by the state-of-the-art Si technology. The availability of deep submicrometer lithography, precise anisotropic etch, planar structures, high-quality thermal oxide, and silicidation for low contact resistance all contribute to the realization of such aggressively scaled complex device structures. With the operation speed on par, Si-based devices enjoy an additional set of advantages such as CMOS compatibility, large wafer size, and large-scale integration with high yield, all contributing to a strong cost efficiency.

Another noticeable trend from Fig. 1 is the impressive performance improvement by CMOS, which, until recently, has not been seriously considered as a leading contender for RF applications. There is no doubt that CMOS technology enjoys advantages in cost and integration level. However, CMOS devices are still inferior to bipolar transistors in many of the key performance parameters required for successful analog and RF applications. Although the operation speed of CMOS benefits from continued lithography scaling, performance currently lags behind bipolar transistors. The transconductance and output impedance, essential for sufficient voltage gain required for various circuit blocks, also favor bipolar transistors due to its exponential current–voltage relation and graded bandgap in the base. The vertical nature of the bipolar structure results in superior $1/f$ noise and device matching performance. Bipolar transistors tend to exhibit better linearity as well, which is critical for low noise and power amplifiers. These factors limit the current RF application of CMOS to applications where the benefits of a high level of integration predominate.

This paper portrays the state-of-the-art SiGe HBT devices and circuits based on the most recently achieved data. In Section II, the SiGe HBT structure and the latest dc and RF performance results are presented, followed by the description of noise performance in Section III. Issues regarding avalanche breakdown and increasing current density are discussed in Section IV along with stress test results. Selected examples on circuit demonstration of SiGe HBT technology are exhibited in Section V, and this paper is concluded in Section VI.

II. SiGe HBT Structure and Performance

A. Overview of Commercial SiGe HBT Technology Evolution

After the first demonstration in 1987 [28], SiGe HBT technology progressed through a decade of incubation period in research laboratories until the world's first commercial SiGe BiCMOS technology was introduced in 1996 [29]. This 0.5-μm BiCMOS technology offers SiGe HBTs exhibiting f_T and $f_{\max}$ of 47 and 65 GHz, respectively. This was followed by 0.25-μm BiCMOS technology with similar HBT performance, but with enhanced CMOS offering [30]. While both of these early technologies were suitable for applications at less than 5 GHz, the subsequent 0.18-μm technology was intended for increased frequency operation such as 40-Gb/s wireline communication applications, with f_T and $f_{\max}$ both exceeding 100 GHz [31], [32]. The speed enhancement was primarily achieved through vertical and lateral scaling, resulting in the reduction of transit time and parasitic resistance and capacitance. Continuing scaling and structural innovation led to a 200-GHz technology based on a 0.13-μm lithographical node [33]. The latest vertical scaling effort with a 0.13-μm node was marked by a record f_T higher than 350 GHz [21], [34], the details of which are the major subject of this section. The key parameters from each technology generation are summarized in Table I along with the corresponding lithographical node.

B. Device Structure

A schematic cross section of the 375-GHz SiGe HBT, fabricated with fully CMOS-compatible processes on 200-mm Si wafers, is illustrated in Fig. 2. The process starts with the formation of a heavily arsenic-doped subcollector buried layer formed by ion implantation, on top of which a lightly doped epitaxial layer is grown that serves as the collector region. Deep and shallow trenches provide device isolation without the use of mesa etching generally employed in III–V HBTs, leading to a planar topography and dense layout. A highly doped collector pedestal region is subsequently formed by a selective implantation into the collector layer. This selectively implanted collector (SIC) provides a narrow base–collector depletion

TABLE I
COMPARISON OF KEY PERFORMANCE PARAMETERS FOR SiGe TECHNOLOGIES FROM IBM. THE EXPERIMENTAL TECHNOLOGY (EXP. TECH.) IS UNDER DEVELOPMENT AND THE DATA THUS FAR ACHIEVED ARE LISTED

	5HP	6HP	7HP	8HP	Exp. Tech
Lithographic node [μm]	0.5	0.25	0.18	0.13	0.13
f_T [GHz]	47	47	120	210	375
f_{max} [GHz]	65	65	100	285	210
Beta	100	100	350	300	3500
BV_{CEO} [V]	3.4	3.4	1.8	1.7	1.4
BV_{CBO} [V]	10.5	10.5	6.5	5.5	5.0
J_C @$f_{T,peak}$ [mA/μm²]	1.5	1.5	8	12	20

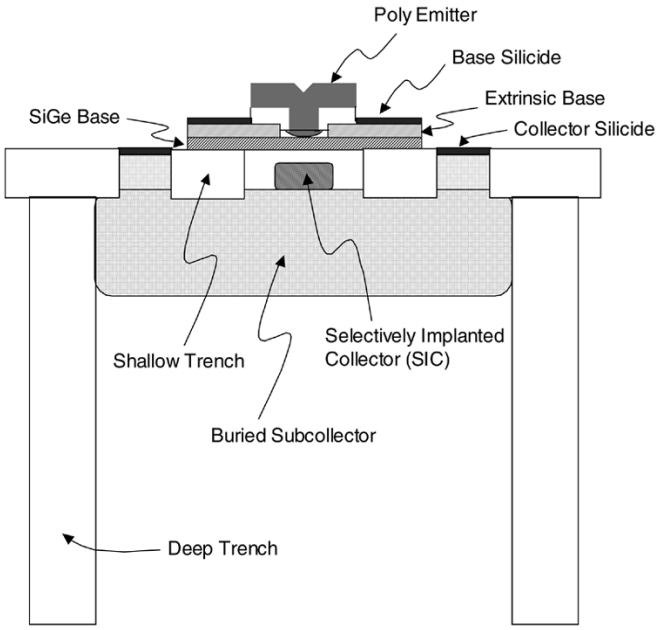

Fig. 2. Schematic cross-section of the 375-GHz SiGe HBT.

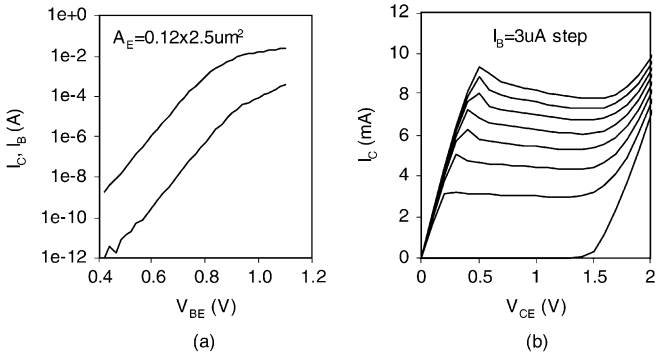

Fig. 3. (a) Gummel plots and (b) forced-I_B output characteristics of the SiGe HBT with the $A_E = 0.12 \times 2.5\ \mu\text{m}^2$ device.

width and high collector current density along with minimized extrinsic base–collector capacitance. This eliminates the need for some exotic approaches such as collector undercut [35] or ion-implant damaging of extrinsic collector [36] often employed for epitaxial III–V HBTs. Bandgap engineering applies to a boron-doped ultrahigh vacuum chemical vapor deposition (UHVCVD)-grown SiGe base layer, where graded Ge composition is incorporated for speed enhancement by a built-in quasi-electric field and improved emitter efficiency. A self-aligned raised extrinsic base decouples extrinsic base resistance and base–collector overlap capacitance, providing a great flexibility in structure optimization for parasitic reduction. A heavily phosphorus-doped T-shaped poly emitter allows narrow emitter stripes close to ∼0.1 μm without causing a significant increase in emitter resistance. Contact resistance for the base and collector is minimized with the silicidation of an extrinsic base and collector. The completed devices are wired by Cu-based multilevel back end of the line (BEOL) process, which provides low resistance and favorable electromigration characteristics for interconnect lines, and also allows a great flexibility in the implementation of various passive components such as thin-film resistors, metal–insulator–metal capacitors, high-Q inductors, and transmission lines.

C. DC and RF Characteristics

DC characteristics of the device with an emitter size of $A_E = 0.12 \times 2.5\ \mu\text{m}^2$ are shown in Fig. 3. The Gummel plots show the near-ideal characteristics of both the collector and base current without a signature of base leakage down to $V_{\text{BE}} = 0.4$ V. The ideality factor is 1.05 and 1.08 for the collector and base, respectively. The near-unity base ideality factor is an indication of the excellent control of surface and interface states. This can be attributed to the planar structure and high-quality Si-oxide interface. The peak dc current gain is approximately 3500. The gain can be adjusted by modulating the emitter–base junction depth. Common-emitter forced-I_B output characteristics exhibit BV_{CEO} (collector-to-emitter BV with base opened) of ∼1.4 V. Reduction of the current gain is expected to increase BV_{CEO}. BV_{CBO} (collector-to-base BV with emitter opened), which is usually larger than BV_{CEO} owing to the absence of the positive feedback that causes faster avalanche current build-up, is measured to be ∼5 V. Note that

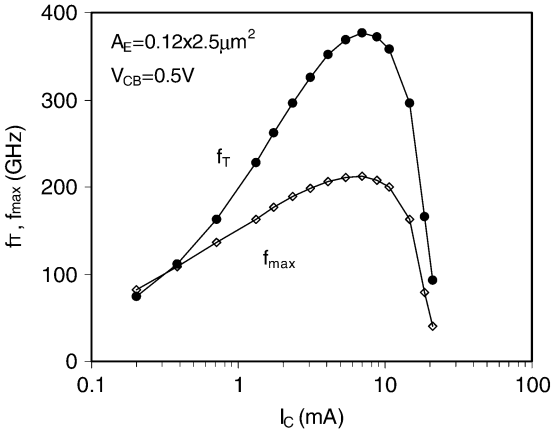

Fig. 4. f_T and $f_{\max}$ of the SiGe HBT extracted from h_{21} and U, respectively, from 40 GHz with -20 dB/dec rolloff. $T = 25\ ^\circ$C.

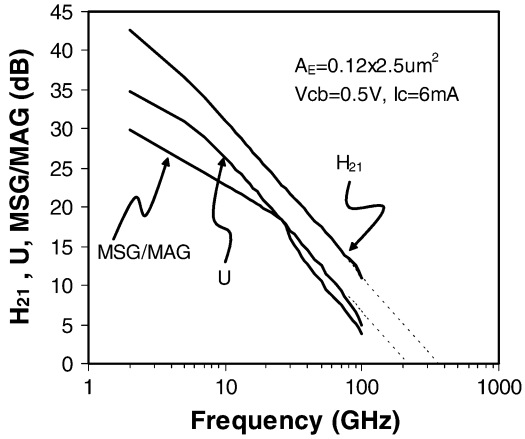

Fig. 5. h_{21}, U, and MSG/MAG measured up to 100 GHz, shown along with -20-dB/dec line for extrapolation.

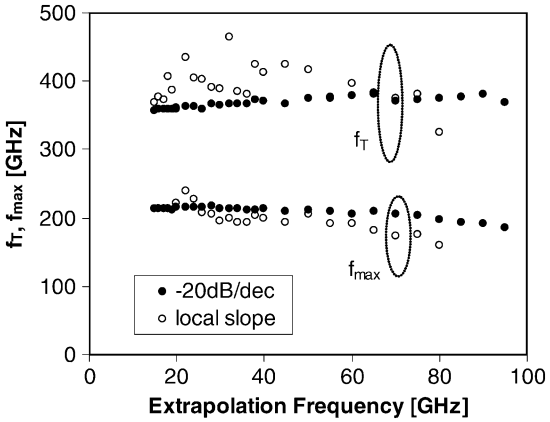

Fig. 6. Comparison of f_T and $f_{\max}$ obtained with -20-dB/dec slope and local slope, shown as a function of frequency from which the extrapolation was made.

$\mathrm{BV_{CEO}}$ is not the upper limit of allowed voltage across the emitter and collector in most practical operations. Instead, such a limit is rather given by $\mathrm{BV_{CBO}}$, as is discussed in more detail in Section IV.

Fig. 4 plots f_T and $f_{\max}$ of the device ($A_E = 0.12{\times}2.5\ \mu\mathrm{m}^2$) as a function of collector current ($V_{\mathrm{CB}} = 0.5$ V fixed), which were extracted by the extrapolation of the current gain h_{21} and Mason's unilateral power gain U, respectively, from 40 GHz with a slope of -20 dB/dec. The peak values of f_T and $f_{\max}$ are 375 and 210 GHz, respectively. To the authors' best knowledge, the f_T of 375 GHz is the highest reported value to date for any Si-based transistors. The significant improvement in f_T was achieved through a vertical scaling in both base and collector layers, which lead to a significant reduction in transit times. The vertical scaling, however, was accompanied by the increase in base resistance R_B and collector-to-base capacitance C_{CB}, resulting in rather moderate value of $f_{\max}$ compared to f_T. Nevertheless, further improvement of $f_{\max}$ can be achieved through structural modification and additional layout optimization leading to R_B and C_{CB} reduction. Moreover, the achieved high f_T provides an opportunity to trade part of its value in favor of $f_{\max}$ for applications where $f_{\max}$ plays an important role.

The accuracy of the extrapolated values of f_T and $f_{\max}$ was verified by a careful examination of the raw data from which the parameter values were extracted. Fig. 5 illustrates h_{21}, U, and maximum stable gain (MSG)/maximum available gain (MAG) obtained from S-parameters measured up to $f = 100$ GHz with an HP8510 network analyzer. The gain curves are quite well behaved, closely following a -20-dB/dec slope over a wide range of frequency, as expected by the single-pole approximation. Fig. 6 plots f_T and $f_{\max}$ of the device as a function of the frequency from which the extrapolation was made, with two different slopes assumed for the extrapolation: local slope around each frequency point and fixed slope of -20 dB/dec. As indicated from the plot, f_T and $f_{\max}$ values exhibit obvious dependence on the extrapolation frequency, even with the apparently well-behaved gain curves, as well as on the rolloff slope assumed. This implies that there exist no unique values of f_T and $f_{\max}$ for a given set of S-parameters over the frequency. A way to avoid this ambiguity is a direct quotation of the gain values at frequency points of interest, as provided in Table II for selected frequencies. This approach is relevant for practical purpose as well since the gain value at a frequency of interest is more useful for the circuit designers than the extrapolated upper limit of the operation frequency.

TABLE II
VARIOUS GAINS AT SELECTED FREQUENCIES OF INTEREST

	20GHz	40GHz	60GHz
h_{21} [dB]	25.1	19.3	16.0
U [dB]	20.7	14.5	10.7
MSG/MAG [dB]	19.7	12.7	8.8

D. Device Layout, Dimensions, and Bias Impacts

The effect of the layout configuration on RF performance is illustrated in Fig. 7. The schematics for the three layout variants of collector–base–emitter (CBE), collector–base–emitter–base (CBEB), and collector–base–emitter–base–collector (CBEBC) are also provided. The nomenclature represents the relative order of electrode contacts. Si-based devices have traditionally adopted the compact CBE configuration since the contact and spreading resistance are not performance-limiting factors because of the availability of silicide. As the Si devices enter

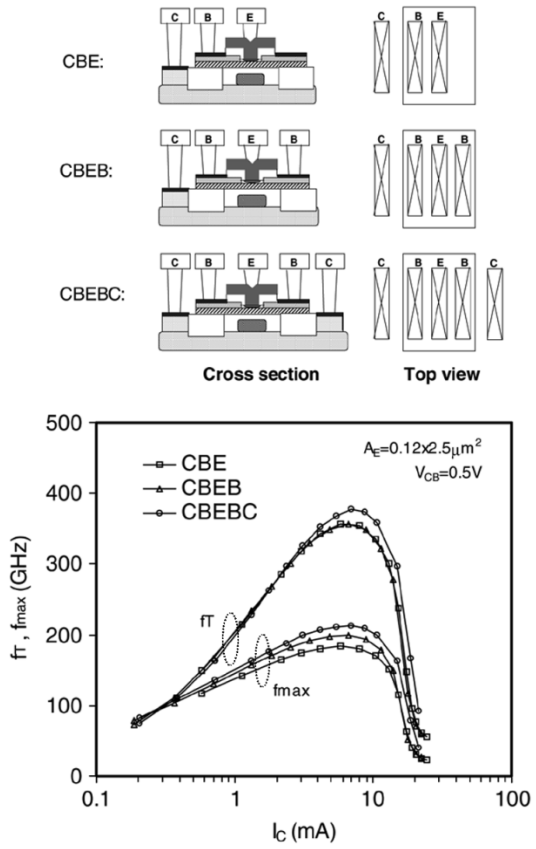

Fig. 7. Schematic of the three configurations employed—CBE, CBEB, and CBEBC—and its impact on f_T and $f_{\max}$.

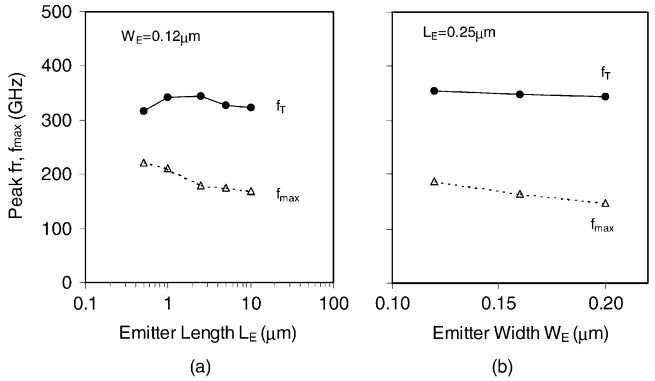

Fig. 8. Dependence of f_T and $f_{\max}$ on lateral dimension. (a) Dependence on emitter length L_E. (b) Dependence on emitter width W_E.

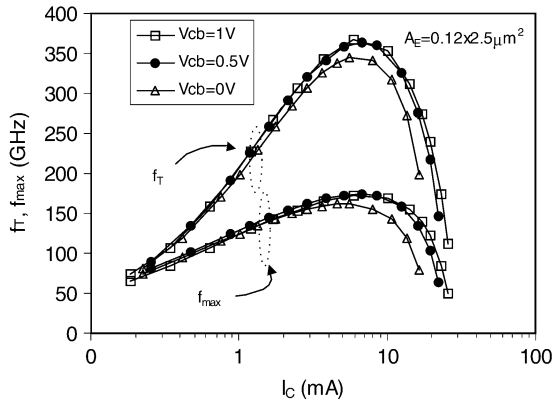

Fig. 9. Dependence of f_T and $f_{\max}$ on collector-to-base bias $V_{\rm CB}$.

the 100-GHz operation regime, however, the effect of parasitic resistance becomes more significant and all the layout options now need to be considered for any performance enhancement. Measurement shows that, compared to the CBE case, the CBEB configuration improves $f_{\max}$ due to the reduction of the R_B component along the silicided region, while imposing little effect on f_T. On the other hand, CBEBC leads to the increase in both f_T and $f_{\max}$, which can be ascribed to R_C reduction and the symmetric spread of injected electrons at the collector region that effectively delays the onset of the Kirk effect and results in a charging time reduction.

The dependence of peak f_T and $f_{\max}$ on emitter length L_E and width W_E is depicted in Fig. 8 for CBE devices. The most evident trend for the L_E dependence is the increase of $f_{\max}$ with decreasing L_E, which can be ascribed to the decreasing R_B with the shorter base current path to the opposite side of emitter finger along the silicided extrinsic base. f_T shows a weaker dependence on L_E compared with $f_{\max}$, but it exhibits a moderate optimum point near $L_E = 2.5$ μm. This can be attributed to the competing scaling behavior of the resistance (R_E and R_C) and capacitance ($C_{\rm CB}$) with L_E variation with an apparent balance occurring around that point. The reduction of f_T for smaller L_E is further accelerated by the increased peripheral component of injected electrons, which travels a longer path to the collector, thus resulting in a longer transit time. The impact of W_E modulation is also more pronounced on $f_{\max}$ than f_T, exhibiting a substantial increase of $f_{\max}$ with W_E reduction. This is the result of the reduced base spreading resistance underneath the emitter opening. The negligible dependence of peak f_T on W_E variation indicates the balance established between reduced $C_{\rm CB}$ and $C_{\rm EB}$ and increased R_C and R_E with the scaling leaving the RC delay mostly unchanged.

Fig. 9 shows the dependence of f_T and $f_{\max}$ on base–collector bias $V_{\rm CB}$. No significant change in f_T and $f_{\max}$ is observed for the given range of $V_{\rm CB}$, except for a slight degradation for both parameters near $V_{\rm CB} = 0$ V. Increased $V_{\rm CB}$ tends to widen the base–collector depletion layer and narrow the neutral base width, leading to increased transit time across the B-C depletion layer ($\tau_{\rm CSCL}$), but reduced transit time across the base (τ_B). It is accompanied by $C_{\rm CB}$ reduction and R_B increase as well. The observed weak dependence of f_T and $f_{\max}$ on $V_{\rm CB}$ indicates that combined effects of these trends are mostly balanced out, while the increased R_B and $\tau_{\rm CSCL}$ begin to dominate with $V_{\rm CB}$ approaching 0 V. The weak dependence also suggests that the increased self-heating with $V_{\rm CB}$ increase does not result in visible performance degradation for the given range of $V_{\rm CB}$.

III. Noise Performance and Contributing Factors

The performance of wireless systems depends critically on the control of noise. In a communications system, for example, signal-to-noise ratio sets the limit on receiver sensitivity for a desired data and bit error rate. The ability of an imaging system to resolve small or low-contrast features is similarly tied to noise level. Such noise can arise from a variety of sources within a circuit. Considering a direct-conversion receiver, for example,

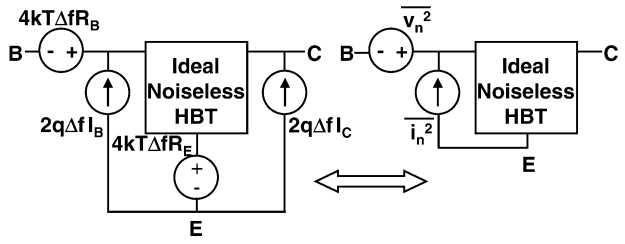

Fig. 10. Basic noise model for an HBT, consisting of a noiseless device plus thermal and shot noise sources.

an input signal from the antenna passes through both a low-noise amplifier (LNA) and mixer, each of which add both broadband (e.g., thermal and shot) and low-frequency (e.g., $1/f$, also known as flicker) noise. Furthermore, the second port of the mixer is fed by an oscillator, which generates a signal containing noise of its own, particularly phase noise stemming from transistor $1/f$ noise. Finally, as the down-converted signal is sampled and processed digitally, the high-speed switching of the baseband logic can inject noise into the substrate, where it can feed back into the signal path at any preceding stage.

To be suitable for implementing such high-frequency systems, a technology must, therefore, provide active devices capable of processing a signal while injecting as little noise into the signal path as possible and should provide the designer with a means of isolating the noise-sensitive from the noise-generating circuit blocks.

The magnitude of noise in a bipolar transistor is a function of frequency. As frequency increases, noise first falls in an approximately $1/f$ fashion, before flattening out for an interval and finally rising once again. Low-frequency flicker or $1/f$ noise is dominated by carrier number fluctuation as these carriers are trapped and released from interface defects. Higher frequency noise may be understood in terms of the simple model drawn in Fig. 10 in which we represent a noisy HBT as a noiseless device to which we connect four external noise sources: two thermal noise voltages due to R_B at the input (base) and R_E at the emitter, a shot noise current proportional to I_B at the input, and a shot noise source proportional to I_C at the output (collector). For $g_m \gg g_d$ (as is typical), the impact of R_E thermal noise is equivalent to that of R_B, allowing the two thermal noise voltage sources to be replaced by a single source at the base with an associate resistance of $(R_B + R_E) \approx R_B$ for $R_B \gg R_E$. Shifting the I_C shot noise to an equivalent input noise source allows for a more direct comparison between noise magnitude and signal level. In doing so, this source is effectively reduced by the gain of the device. At frequencies well below f_T, gain is high and noise is dominated by the input terminal noise sources and, thus, relatively independent of frequency. As frequency rises, however, gain begins to drop and the impact of I_C shot noise at the device input terminal grows.

The noise properties of an active device can be represented by four noise parameters: minimum noise figure $(F_{\min})$, noise resistance (R_n), and the real and imaginary components of the source impedance match for lowest $F_{\min}$ (Γ_{opt}). By assuming a simple common-emitter compact model for the HBT in our noise model, we arrive at an approximate expression for $F_{\min}$

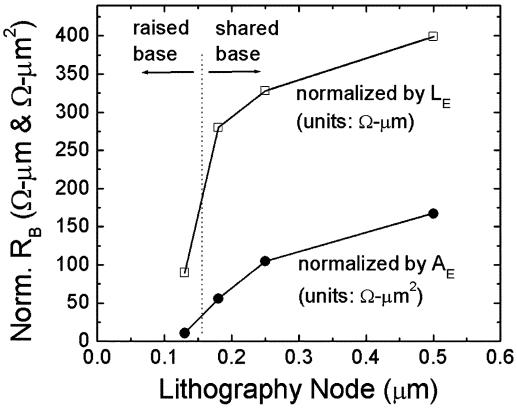

Fig. 11. Base resistance R_B (normalized by both emitter length and area) versus lithography node for four generations of IBM SiGe HBT technology.

in terms of both device parameters and biasing conditions [37] as follows:

$$F_{\min} = 1 + \frac{1}{\beta} + \sqrt{2\frac{qI_C}{kT}R_B\left(\frac{f^2}{f_T^2} + \frac{1}{\beta}\right) + \frac{1}{\beta}}. \quad (1)$$

$F_{\min}$ is impacted directly by the value of R_B (a simplification of $R_B + R_E$ under the assumption that $R_B \gg R_E$) regardless of frequency and bias. Thus, driving toward lower base resistance must be one key goal in the scaling of a low-noise bipolar technology. As previously mentioned, R_B reduction can be achieved through lateral scaling, as well as structure improvements such as the move from a shared-base to a raised base scheme. Fig. 11 plots R_B (normalized against both emitter length and area) versus lithographic node across four generations of IBM SiGe BiCMOS technology, illustrating a 15%–18% per generation decrease in length-normalized R_B due to lateral scaling through and including the 0.18-μm (120 GHz f_T) generation, followed by a much larger 68% drop in R_B with the move to an *in-situ* doped raised base scheme in the 0.13-μm (200 GHz f_T) generation [38]. These improvements are even more dramatic if emitter area is held constant and are a key source of continued noise performance improvement with each SiGe HBT generation.

At low frequencies $(f^2/f_T^2 \ll 1/\beta)$, the frequency-dependent term drops out and $F_{\min}$ becomes relatively insensitive to f_T. In this regime, there are diminishing returns with f_T scaling, although some noise improvement is possible through increased β. As frequency increases further, however, $F_{\min}$ begins to rise linearly, with a slope dependent on the value of f_T. The higher the frequency, the more significant the role of high f_T in maintaining low noise.

Although I_C and f_T appear in the ratio I_C/f_T^2 in (1), f_T is itself a function of I_C. RC delay dominates transit time at low currents and f_T rises with I_C. Under this condition, the ratio reduces to a $1/I_C$ dependence and $F_{\min}$ falls with increasing current. At higher current, however, f_T flattens toward a peak, and the ratio becomes directly proportional to I_C. These two competing trends give rise to a value of I_C at which $F_{\min}$ is minimized, as illustrated in Fig. 12. The optimum value of I_C is typically not near peak f_T, but rather at 1%–20% of this value. Scaling for best noise performance should, therefore, emphasize

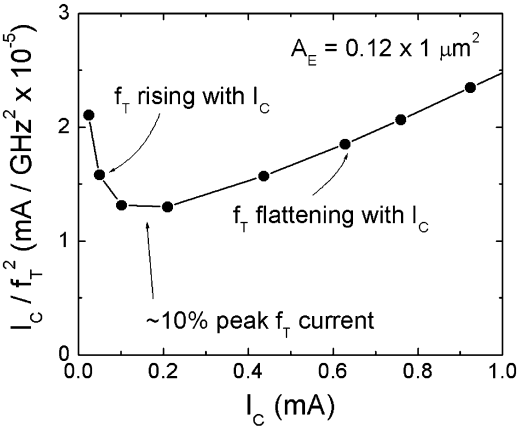

Fig. 12. I_C/f_T^2 versus I_C for a 0.12×1 μm^2 200-GHz SiGe HBT, illustrating the competing trends that result in minimum noise figure occurring below peak f_T current.

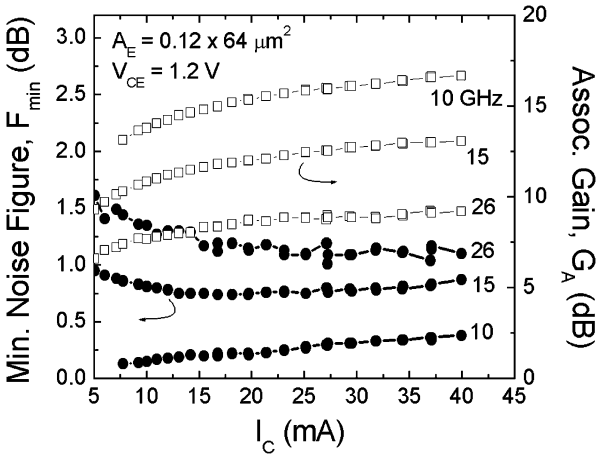

Fig. 13. Minimum noise figure ($F_{\min}$) and associated gain (G_A) versus I_C for a 0.12×64 μm^2 200-GHz SiGe HBT for 10, 15, and 26 GHz at $V_{\rm CE} = 1.2$ V.

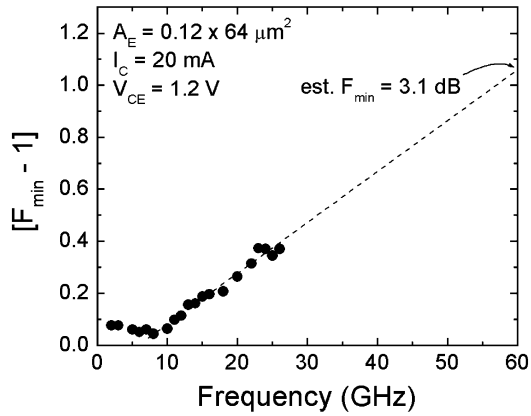

Fig. 14. $[F_{\min} - 1]$ (on a linear scale) versus frequency for a 0.12×64 μm^2 200-GHz SiGe HBT, indicating estimated performance at 60 GHz based on linear extrapolation.

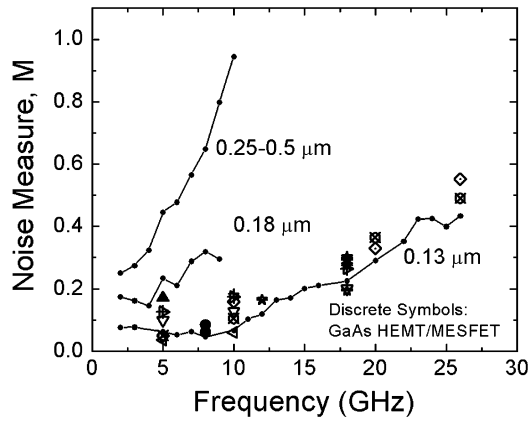

Fig. 15. Noise measure (M) versus frequency for SiGe HBTs across generations, with comparison against GaAs FETs, illustrating performance enhancement due to both f_T and R_B improvement.

improved low-current f_T, which may be achieved by reducing $C_{\rm BE}$ and $C_{\rm CB}$, as well as by lateral scaling to reduce I_C at a given current density. This approach is in contrast with the increase in peak f_T through transit time reduction and Kirk effect pushout typically sought for applications such as wired/optical networking.

Improvement in both R_B and f_T with each SiGe HBT generation has led to a steady improvement in broad-band noise performance. This performance may be explored in more detail by focusing on IBM's pre-production 0.13-μm 200-GHz technology [38] and using data taken up to the 26-GHz limit of the ATN electronic tuner noise figure system, concentrating on the higher frequencies of greater interest in emerging wireless applications. Fig. 13 plots $F_{\min}$ and associated gain (G_A) versus I_C at 10, 15, and 26 GHz for a $V_{\rm CE}$ value of 1.2 V. The figure illustrates that $F_{\min}$ achieves a value below 0.4 dB at 10 GHz, with a corresponding G_A greater than 17 dB. At 26 GHz, $F_{\min}$ has risen to only slightly above 1 dB, with G_A in excess of 9 dB. Still higher gains are possible by increasing I_C beyond our measured values.

Although we have not yet measured noise performance beyond 26 GHz, we note the well-behaved nature of $[F_{\min} - 1]$ versus frequency, as illustrated in Fig. 14 on a linear scale. At frequencies beyond 7–10 GHz, $F_{\min}$ grows quite linearly with frequency, permitting a reasonable extrapolation to higher frequencies. Confining our extrapolation to within 2.5$\times$ of the highest measured frequencies, we can estimate a value of $F_{\min}$ at 60 GHz of 3.1 dB, which is sufficient performance for exploring the emerging wireless applications such as networking and automotive radar in this part of the spectrum.

Low $F_{\min}$ is less useful if not accompanied by sufficient gain. Noise measure (M) combines both $F_{\min}$ and G_A into a composite quantity $(F_{\min} - 1)/(1 - 1/G_A)$ that tracks $F_{\min}$ for $G_A \gg 1$, but self-degrades if gain drops. Using this method, we consider M versus frequency for three generations of IBM SiGe HBT technology in Fig. 15 [39]. This figure also includes data from the specification sheets of commercially produced GaAs high electron-mobility transistor (HEMT) and MESFET devices, generally considered the standard for good low-noise behavior [40]–[47]. At 10 GHz, we note a tenfold improvement in noise measure in moving from the 0.5- to 0.13-μm generation. We also note that the 0.13-μm generation achieves values of noise measure on par with those of production GaAs devices, suggesting that a silicon technology can serve the same

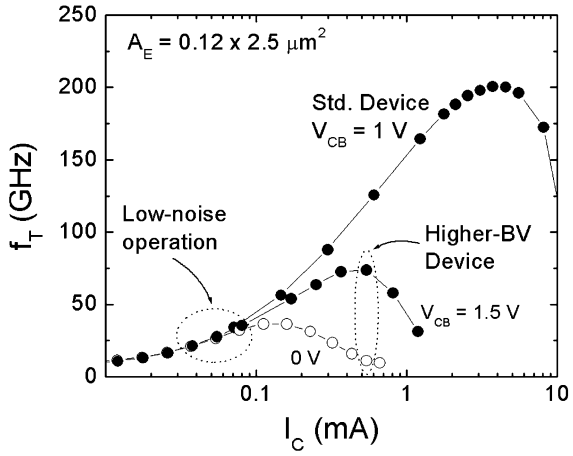

Fig. 16. f_T versus I_C for two 0.12×2.5 μm^2 200-GHz SiGe HBTs, comparing a standard device with a modified-collector higher-breakdown variant.

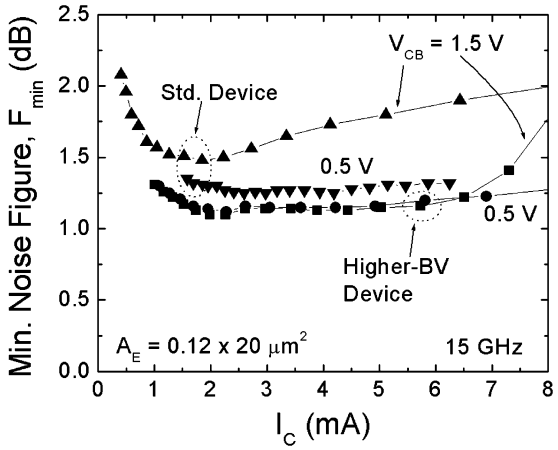

Fig. 17. $F_{\min}$ versus I_C at $V_{\rm CB} = 0.5$ and 1.5 V and 15 GHz for standard and higher-breakdown 0.12×20 μm^2 SiGe HBTs, comparing impact of avalanche on the noise properties.

low-noise applications while providing the additional benefits of low cost and high integration potential.

The ability to easily provide the designer with multiple HBT variants within the device library of a silicon technology enables another means of achieving reduced noise. One potential variant is a device with a reduced collector doping in order to provide for a higher breakdown voltage (BV). Fig. 16 compares f_T versus I_C for both a standard-offering and higher-breakdown 0.13-μm-generation HBT [48]. We note that reducing the collector doping lowers peak f_T by reducing the collector density at the onset of the Kirk effect. Peak f_T and associated I_C also become more sensitive to $V_{\rm CB}$. However, low-current f_T, more relevant for low-noise performance, is affected much less by collector doping. At the same time, the higher breakdown device experiences less avalanche current multiplication at higher $V_{\rm CB}$, reducing avalanche noise at such voltages. Fig. 17 illustrates this benefit, plotting $F_{\min}$ versus I_C at 15 GHz for both standard and higher breakdown HBT variants at $V_{\rm CB}$ values of 0.5 and 1.5 V. Both devices display similar behavior at $V_{\rm CB} = 0.5$ V. At 1.5 V, however, the standard device shows a degraded noise figure, while the higher breakdown device experiences little change. The ability of the higher breakdown device to operate at higher $V_{\rm CB}$ can provide the designer with added flexibility of low-noise operation combined with large headroom.

Minimum noise figure, greatest gain, and highest linearity are not, in general, obtained at the same source impedance tuning. In developing an LNA, for example, a designer may need to seek a compromise in source impedance, striking a favorable balance between these three figures-of-merit. A technology in which noise figure increases slowly as the source is tuned away from the optimum impedance, therefore, provides greatest flexibility in obtaining this balance. The rate of noise figure increase with mismatch is characterized by the noise resistance (R_n) of the device. Fig. 18 plots R_n versus I_C for a 200-GHz HBT of 7.7-μm^2 emitter area and at frequency values of 10, 15, 20, and 26 GHz. For I_C above 15 mA, we note that R_n remains below 4 Ω for all measured frequencies. This is among the lowest values we have observed and fosters great ease in implementing a source match.

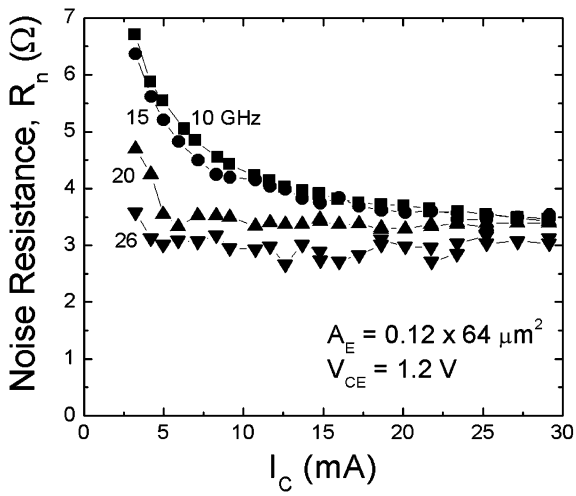

Fig. 18. Noise resistance R_n versus I_C at $V_{\rm CE} = 1.2$ V for a 0.12×64 μm^2 200-GHz SiGe HBT.

Although a low-frequency phenomenon, $1/f$ or flicker noise can have direct impact on performance in high-frequency wireless applications. Flicker noise contributes to phase noise in voltage-controlled oscillators (VCOs), which is then shifted into the channel band by the action of the mixer. In a direct-conversion receiver architecture, $1/f$ noise may also combine directly with the baseband signal. The severity of $1/f$ noise is directly proportional to trap density in the regions of the device through which the majority of carriers flow. As a vertical device, most carrier flow in the SiGe HBT is through high-quality bulk material and away from silicon surfaces. High-quality oxide passivation reduces trap density in those surfaces that do exist. Thus, the device enjoys a very low level of $1/f$ noise compared with III–V devices, in which good surface passivation does not exist, or with lateral devices such as field-effect transistors (FETs) in which most of the carrier flow is in close proximity to an interface. To illustrate this behavior, we plot I_C noise versus frequency in Fig. 19 for a 0.18-μm-generation 120-GHz SiGe HBT [49]. As frequency increases from dc, we observe the expected falloff in noise, with the flicker noise eventually dropping below the level of the background broad-band noise. For the device

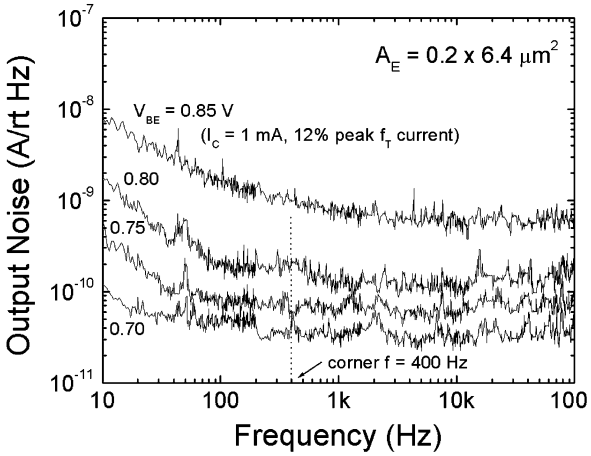

Fig. 19. Output noise versus frequency at various $V_{\rm BE}$ for a $0.2 \times 6.4\ \mu{\rm m}^2$ 120-GHz SiGe HBT.

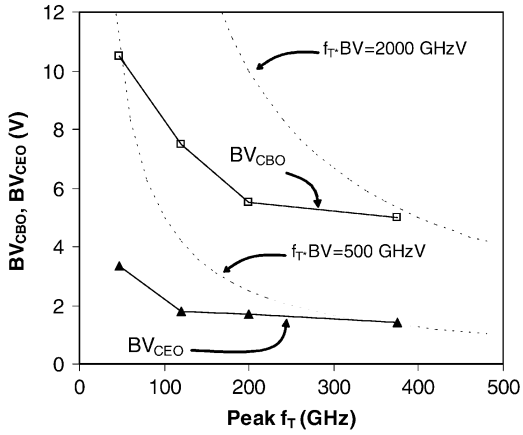

Fig. 20. Trend of $\rm BV_{CEO}$ and $\rm BV_{CBO}$ with increasing f_T. Both BVs show a signature of saturation. Shown as a dotted line is the constant f_T BV product contour.

shown, this "corner frequency" is less than 1 kHz and is 1–3 orders of magnitude smaller compared with competing FET devices. Thus, the SiGe HBT is a natural choice for the design of oscillators requiring very low phase noise.

IV. Avalanche, Current Density, and Stress Test

Scaling has been the key enabler for the device speed enhancement, but it also brings about issues regarding device operation constraints and reliability. The increase of the electric field at the base–collector junction leads to increased avalanche effects and reduced BVs. The increase in collector doping concentration is usually accompanied by increased operation current density. This section addresses these issues, along with the stress test results.

A. Avalanche and Device Operation Limit

The trend of BVs of SiGe HBTs with increasing device speed is shown in Fig. 20, taken from four generations of IBM SiGe technology. Both $\rm BV_{CEO}$ and $\rm BV_{CBO}$ continue to decrease with increasing f_T, but they show a signature of saturation as f_T enters the multihundred-gigahertz regime. Also plotted as a dotted line is the constant f_T BV product contour, which indicates the increase of the product with the generation. As mentioned briefly earlier, $\rm BV_{CEO}$ does not serve as the upper limit of voltage allowed across collector and emitter. This limit is rather given by $\rm BV_{CBO}$, which is typically a few times larger than $\rm BV_{CEO}$, as shown in Fig. 20. To explore the practical voltage limit of bipolar transistors, it will be helpful to review a detailed picture of the avalanche mechanism occurring in the device.

When avalanche multiplication takes place in the reverse biased base–collector junction, the generated holes drift toward the base. Once in the base region, a hole may take either of two courses: it may exit the device through the base contact without further reaction or recombine with an electron and trigger additional injection of electrons from emitter into base, which is basically the current amplification action. The injected electrons will contribute to the increased avalanche multiplication and cause a further increase of electron injection from the emitter, forming a positive feedback loop. The strength of the positive feedback, which modulates the BVs, increases with increasing external impedance seen by the base electrode since the avalanche-generated holes are increasingly forced to stay within the device with larger base impedance. Therefore, the configuration of base connection, which affects the base impedance, has a direct impact on the BV. Note that this positive feedback in breakdown is a unique feature for bipolar transistors that is not found in FETs or diodes. The difference lies in the fact that the breakdown path in bipolar transistors traverses through two p-n junctions and, more importantly, one of the junctions often remains forward-biased, enabling current amplification. Open-base configuration corresponds to infinite external impedance and maximized positive feedback, rendering the corresponding BV $\rm BV_{CEO}$ to be the smallest BV across collector and emitter. However, this configuration is rarely found in most practical circuit applications, and this explains why $\rm BV_{CEO}$ does not frequently serve as the voltage limit. The opposite extreme happens with base shorted to emitter, where the external impedance is effectively zero and the positive feedback is absent, leading to the corresponding BV $\rm BV_{CES}$ largest and equivalent to $\rm BV_{CBO}$. Lying in between is the configuration in which base is connected to emitter through a resistance, in which the corresponding BV ($\rm BV_{CER}$) falls between $\rm BV_{CEO}$ is $\rm BV_{CES}$, the specific value dictated by the resistance value. This is the most realistic case and its dependence on external resistance is illustrated in Fig. 21 for 0.18-μm-generation 120-GHz SiGe HBTs, clearly showing the feasibility of device operation well above $\rm BV_{CEO}$.

Although the junction breakdown is the most common avalanche-originated mechanism that affects the operation region of devices, there is another phenomenon related to the avalanche that may also limit the operation of bipolar transistors. The phenomenon, which is called the "pinch-in" effect, refers to a situation in which the vertical current path in the intrinsic device is abruptly squeezed into the very center of the device when $V_{\rm CB}$ exceeds a certain point [50]. When the device is biased with a common-base forced-emitter current configuration, the direction of base current is reversed when the avalanche-generated hole current becomes larger than the

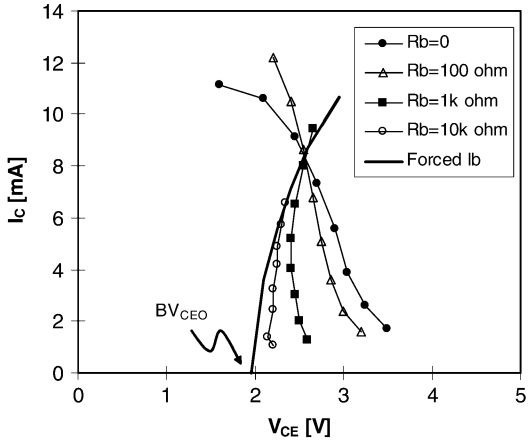

Fig. 21. Breakdown points with forced-I_B configuration and forced-$V_{\rm BE}$ configuration with various resistance values connected to base in series.

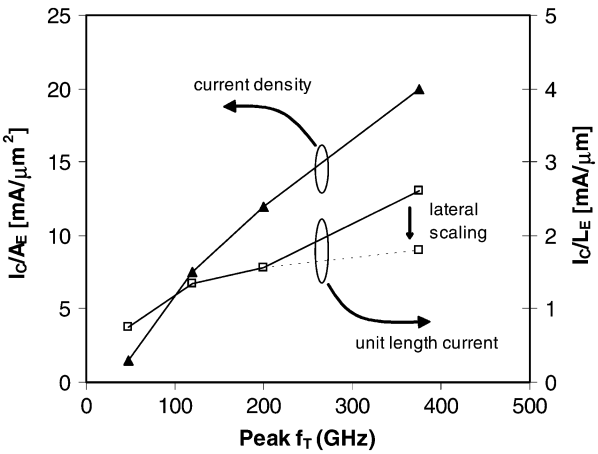

Fig. 22. Trend of collector current density (I_C/A_E) and unit length current (I_C/L_E) with f_T. Unit length current increases more slowly than current density with increasing device speed. The dotted line shows the unit length current predicted with appropriate lateral scaling for the $f_T = 375$ GHz point.

current supplied from outside. As the reverse base current becomes sufficiently large as the device enters the deep avalanche region, emitter crowding effect takes place due to the lateral voltage drop across the base layer. Since the current direction is reversed, the voltage drop occurs from the center to the edge of the active area, opposite of normal operation conditions, resulting in the current crowded at the center of the device instead of the edge of the emitter. This pinch-in mechanism tends to occur in an abrupt fashion and causes a sudden drop of I_C and $V_{\rm BE}$, altering the bias condition of the device. Hence, the pinch-in may potentially limit the voltage allowed across the emitter and collector for the forced-I_C configuration, necessitating an accurate modeling of the phenomenon [51].

B. Current Density and Device Stability

The trend of current density with speed enhancement is shown in Fig. 22, along with the trend of unit length current. The increasing current density may have implications on device robustness, self-heating, and electromigration. Its effect on device robustness is often associated with the stability of a thin oxide layer frequently employed at the poly/mono interface, and also with the integrity of Si–Si and Si-dopant bonding of the device. The interfacial oxide was historically employed as an effort to increase the current gain, but as sufficient current gain is now available with the SiGe base, the necessity of such oxide layer is diminished. In fact, devices without the oxide have emerged as a viable option [52], rendering the oxide-related reliability issues less relevant. The stability of dopant atoms under high current density has been a concern for III–V-based devices, as recombination-enhanced dopant diffusion has been a major degradation mechanism for those devices [53]. In addition, the high defect density frequently found in III–V devices is susceptible to high current density, resulting in defect propagation and defect cluster growth. On the contrary, Si-based devices generally benefit from more stable dopant bonding and lower defect density and, therefore, they are less vulnerable to such integrity issues associated with high current density. It is notable that the collector current density of the fastest Si-based bipolar transistor is still much smaller than the channel current density of typical Si CMOS devices (Table III), implying the margin in the current density increase for Si-based bipolar transistors in terms of bulk Si integrity.

As scaling increases current density, the stability of the interconnect lines that feed current to the HBT may be limited by electromigration. While layout solutions such as vertical strapping of metal lines and multiple collector contacts are often sufficient to prevent the electromigration, new wiring materials or exploitation of the short line effect [54], [55] may be required at the highest current densities. Fortunately, the lateral scaling that often accompanies the vertical scaling helps to alleviate the electromigration issue. The current capacity of metal feeding lines is, in most cases, given by the current per unit length of the emitter finger, which decreases with decreasing emitter width for a fixed current density (current per emitter area). As the emitter width tends to decrease over the technology generations, the current per emitter length exhibits slower increase than the current density, as is clearly shown in Fig. 22. Note from the plot that lateral scaling for the $f_T = 375$ GHz case would lead to a near-flat trend of the unit length current (shown as a dotted line).

A more pronounced self-heating effect is expected with increasing current density. Excessive junction temperature rise may promote device performance degradation and, more importantly, aggravate the electromigration as the current capacity of metal lines decreases exponentially with increasing temperature. Hence, it is increasingly necessary to consider thermal resistance $(R_{\rm th})$ reduction as one of the factors to be considered in device structure optimization. Since deep trench (DT) significantly impedes heat dissipation from the device, the most effective way to reduce $R_{\rm th}$ of bipolar transistors is to modify DT structures such as DT-enclosure area enlargement or DT depth reduction [56]. The lateral scaling of the device also helps to suppress the junction temperature rise as $R_{\rm th}$ decreases with decreasing emitter width for a fixed emitter area [57].

C. Stress Test

Bipolar transistors are operated in the forward active mode for most of their operating time and, therefore, the reliability of the device under forward mode operation should be carefully analyzed to meet the required lifetime for a given application.

TABLE III
CURRENT DENSITY AND UNIT LENGTH CURRENT FOR VARIOUS DEVICES

Device Type	Conducting cross-section width (μm)	Current density for peak f_T (mA/μm²)	Unit length current (mA/μm)
SiGe HBT [21]	0.12	20	2.4
InP HBT [15]	0.8	7	5.6
Si MOSFET	~ 0.01	~70	~0.7

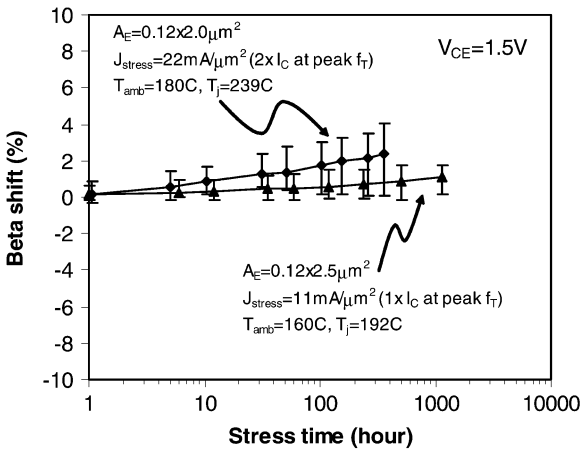

Fig. 23. Current gain shift under forward-mode stress, compared for the stress current of $1\times$ and $2\times$ of I_C at peak f_T.

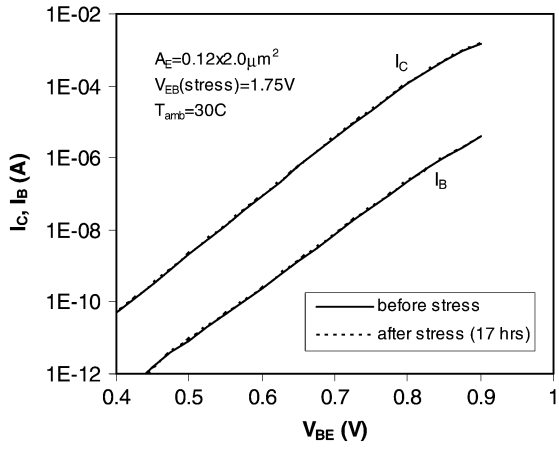

Fig. 24. Gummel plots before and after reverse-mode stress. No noticeable change is observed.

Typically observed degradations under forward mode operation include: 1) emitter and base current increase in high-$V_{\rm BE}$ range due to the reduction in emitter resistance often associated with emitter poly/mono interface stability [58]–[60]; 2) base current decrease in the mid-$V_{\rm BE}$ range due to hydrogen passivation of emitter poly boundaries and poly/mono interface [59]–[61]; and 3) base leakage current increase in the low-$V_{\rm BE}$ range related to avalanche-generated hot carriers or Auger recombination [62], [63]. Most of these degradations are aggravated with increased current density and, hence, the device reliability under raised operation current density should be addressed with accelerated current stress. Elevated ambient temperature is often adopted to further accelerate the stress test, as it also promotes many of the degradation mechanisms. In this study, accelerated long-term stresses have been performed on 0.13-μm-generation 200-GHz SiGe HBTs, and the results are shown in Fig. 23. Two different conditions were employed and compared, which are: 1) nominal current density of 11 mA/μm^2 (where peak f_T occurs) at the elevated ambient temperature $T_{\rm amb}$ of 160 °C (junction temperature $T_j = 192$ °C) and 2) twice the nominal current density (22 mA/μm^2) at $T_{\rm amb} = 180$ °C ($T_j = 239$ °C). Under $1\times$ nominal current stress, current gain shift is tightly confined within 2% shift up to 1140 h. The device exhibits little degradation even with the $2\times$ nominal current density, as evidenced by the current gain shift of less than 4% up to 350 h. The results are an indication of the robustness of the device against the increased current density.

In some applications, such as power control circuits, the base–emitter junction may be switched between forward and reverse bias. With reverse bias, a relatively high electric field is established laterally across the peripheral emitter–base junction. Once electron–hole pairs are generated by either thermal emission from traps or tunneling [64], the carriers are accelerated within the high-field region and become hot. If an Si–oxide interface is located in proximity to that region, as is often the case for typical bipolar structures, the hot carriers generate traps by breaking weak interfacial bonds. The increased trap density enhances the carrier recombination rate and, as a result, base current is increased and current gain is reduced in the low-$V_{\rm BE}$ region. Although the base leakage current does not result in significant change in most RF characteristics, it may degrade some parameters such as noise. In order to investigate the stability of the device under the reverse-bias condition, 200-GHz SiGe HBTs with $A_E = 0.12 \times 2.5$ μm^2 were stressed with a reverse emitter–base bias of $V_{EB} = 1.75$ V for 17 h at $T = 30$ °C. Note that $\rm BV_{EBO}$ (emitter-to-base BV with collector opened) of the device is 3.5 V. Gummel plots of the stressed device were taken before and after the stress, and one observes no noticeable increase in base current at the low-$V_{\rm BE}$ region (Fig. 24). This can be attributed to the fairly small oxide interface area along the emitter perimeter of the device, as well as the favorable field configuration in that region.

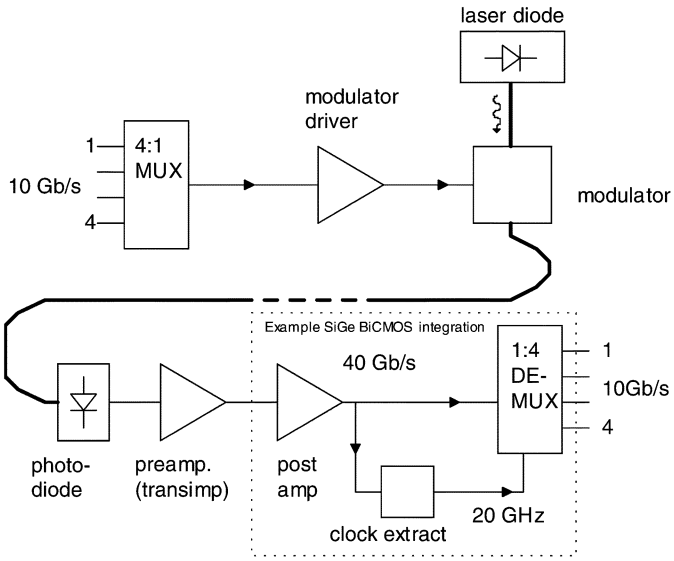

Fig. 25. Block diagram of 40-Gb/s implementation.

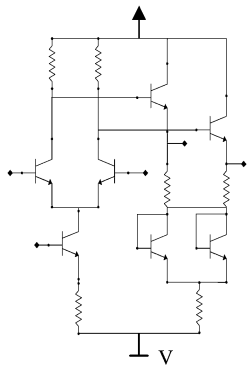

Fig. 26. Schematic of a single stage in the ECL ring oscillator.

V. High-Speed Circuits

SiGe HBT technology on a silicon platform enables a rich set of active and passive devices and, hence, provides the circuit designers with a unique set of advantages compared to the possible implementations in other material systems. Large-scale integration is possible because of the high yields available for active devices. Furthermore, designs in silicon enjoy the benefits of scaling with each generation, leading to improvements in devices both in the front end and BEOL. The wiring needs for microprocessors and application-specific integrated circuits (ASICs) have resulted in very routine planar BEOL with 7+ levels of metal. Such planar back-end schemes integrate low-K dielectrics with Cu metallization with optional add-on thick dielectric module. This has, in turn, led to significant progress in enabling high-Q inductors on silicon substrates. 1.1-nH inductors with Q values as high as 28 (at 3.5 GHz) are offered in production SiGe technologies [65]. Even higher Q can be expected as technology implementation become feasible with higher resistivity substrates [66].

Multigigabit serial communication has benefited from the improved HBT power-speed characteristics resulting from scaling the devices every generation. Fig. 25 shows a block diagram of a typical circuit implementation. These systems employ both high-speed digital and wide-bandwidth analog components that are required to be robust (over voltages and temperature) and are designed to meet stringent jitter and bit error rate specifications. One of the advantages of the SiGe HBT technology is the possibility of integrated solutions in both transmit and receive paths. Integration becomes even more attractive from a cost and complexity standpoint if interfaces at slower 2.5-Gb/s rates and skew compensation are required. Integrated transmit and receive chipsets for 10-Gb/s Ethernet and optical communication (OC-192) have been demonstrated in the 0.5-μm SiGe generation [67], [68]. With the availability of higher speed HBT devices in the 0.18-μm generation, designs for 40-Gb/s application space have also been reported [69], [70]. Integrated transmit chips with 4:1 multiplexers (MUXs) integrated with a clock multiplication unit and receivers with a 1:4 demultiplexer (DeMUX) integrated with limiting amplifier and clock-data recovery (CDR) units for OC-768 implementation are also beginning to appear in the 0.18-μm technology [71]. Scaling the SiGe HBT device into the 0.13-μm node opens up the possibility of implementing these 40-Gb/s systems with greater design latitude at possibly much lower power.

This section describes results from ring oscillators, frequency dividers, VCOs, and MUXs that have been demonstrated in IBM's 0.18- (120 GHz f_T) and 0.13-μm (200 GHz f_T) generation SiGe technology.

A. Ring Oscillator

Delay in the emitter coupled logic (ECL) bipolar ring-oscillators circuits is representative of the raw performance that can be expected from an unloaded gate. While these are simple circuits, they can also be very useful in benchmarking the technology and identifying potential device design tradeoffs to enable higher bandwidth and speed in more complex circuits. Previous studies have shown that the delay in the ring stage [ECL or current mode logic (CML)] is related to the charging times of the various resistive and capacitive parasitics of the gate [72]. Some of the parasitic elements like R_B and $C_{\rm CB}$ have been shown to affect gate delay relatively more than others. We have used the ring oscillators to rapidly evaluate the effect of minimization of components of various parasitics on circuits as the HBT device is scaled both laterally and vertically [73], [74].

The circuits were fabricated during various stages of scaling with devices having $f_{\max}$ ranging from 90 to 340 GHz (extracted from Mason's unilateral power gain U). The rings employ a basic ECL gate (schematic in Fig. 26) designed for an output swing of $\sim$300 mV (single ended) at the peak f_T current with a $\sim$100-Ω resistor used as a load. A $-$3.6-V nominal power supply was used. Fig. 27 compares the stage delay for three different transistor designs. Minimum delay in the 0.13-μm generation is reduced to 4.3 from 8.8 ps in early stages of the 0.18-μm technology. A further reduction of minimum delay to 3.9 ps is achieved when the $f_{\max}$ in the 0.13-μm technology is improved to 338 GHz. From this figure, it can also be observed that minimum delay occurs at current density lower than the peak f_T

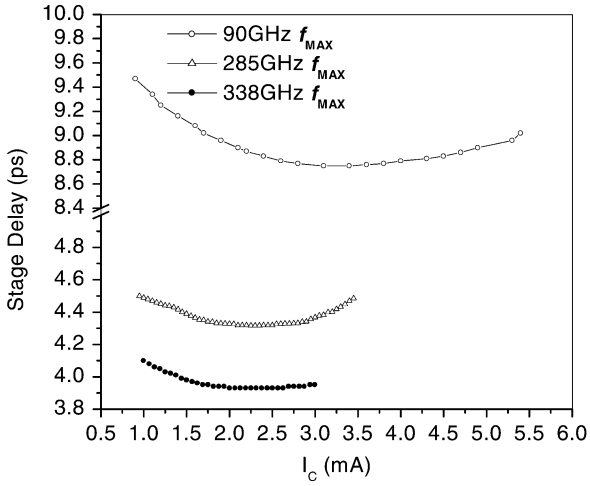

Fig. 27. ECL stage delay comparison for ring oscillators fabricated in 90-, 285-, and 338-GHz $f_{\max}$ SiGe technologies.

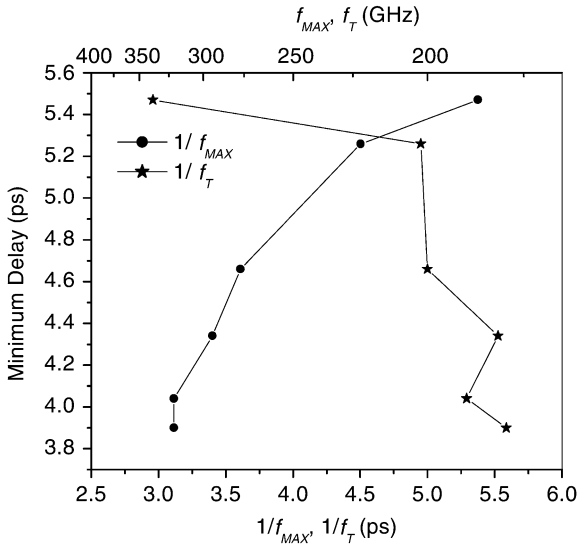

Fig. 28. Minimum delay versus f_T and $f_{\max}$ in the 0.13-μm technology.

current, indicating that biasing such circuits at the peak f_T current density would be suboptimal from a power-speed tradeoff.

There is an inherent f_T and $f_{\max}$ tradeoff during device scaling. The impact of this tradeoff is shown in Fig. 28, where the minimum ring oscillator delay is shown as a function of various f_T and $f_{\max}$ design points. It is seen that minimum delay is more correlated to $f_{\max}$ than it is to f_T. In this plot, the voltage swing is $\sim$230 mV for all design points and all the rings use a 100-Ω resistor. Such a dependence of ring delay on $f_{\max}$ is not surprising since all other factors like load resistance and emitter–base diffusion capacitance are very similar in all the designs, as a result, delay predominantly depends on the $R_BC_{\rm CB}$ product. As the device scaling continues toward achieving f_T and $f_{\max} \sim 400$ GHz, it is instructive to understand the components of the minimum stage delay. These components have been analyzed using model-based analysis and are shown in Fig. 29 for a ring with a stage delay of 3.9 ps (C_T refers to the total effective capacitance charged by the resistor). From the analysis, it appears that $\sim$45% of the delay is associated

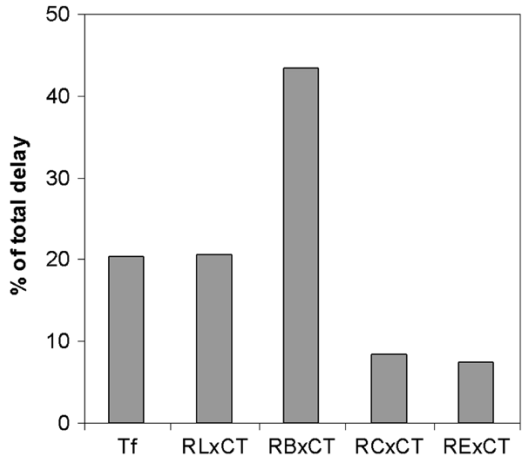

Fig. 29. Delay components for a 3.9-ps ring oscillator estimated by model-based simulations.

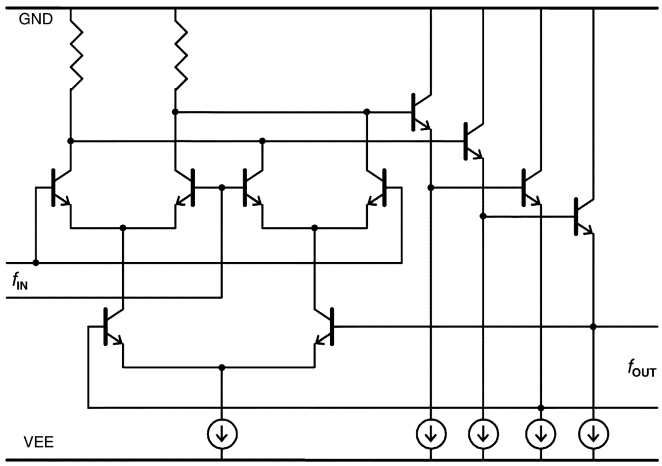

Fig. 30. Schematic of the dynamic divider core.

with the $R_BC_{\rm CB}$ product in the device, $\sim$20% is transit time related, and $\sim$20% resulting from the delay associated with charging of the parasitic capacitance via the load resistors. As the technology is scaled further with more improvements in R_B and $C_{\rm CB}$ and transit time, the ring oscillator delay is expected to reduce even further.

B. Frequency Dividers

Frequency dividers are key building blocks in communication circuits. They are used in high-speed MUX, DeMUX, and phase-locked loop (PLL) circuits. The static divider based on a toggle flip-flop can be used to determine the maximum clocking frequency in such circuits. Dynamic dividers are used in aforementioned applications when either higher speed of operation or lower power consumption (compared to a static divider) is desired. Static and dynamic frequency dividers have been made in both the 0.18- and 0.13-μm SiGe generations [75]. Identical circuit topology has been used in both generations to facilitate comparisons. The static divider is a conventional two-latch toggle flip-flop, while the dynamic divider uses regenerative frequency division (schematic in Fig. 30). The dividers were designed for a $-$3.6-V nominal supply.

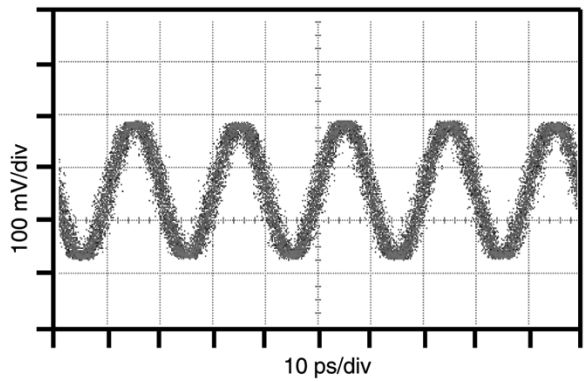

Fig. 31. Output 50-GHz signal of the dynamic divider at 100-GHz input.

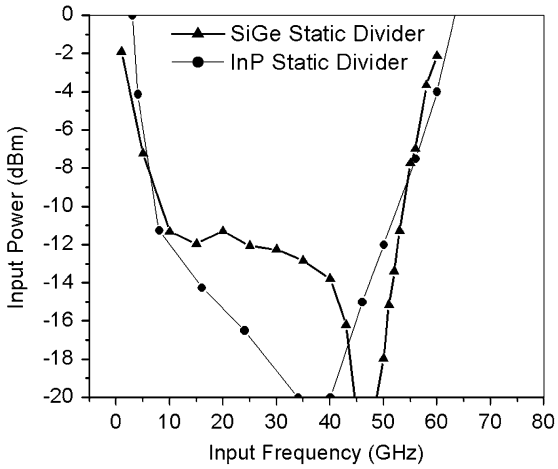

Fig. 32. Input sensitivity of SiGe static divider. InP-based divider from [75] shown for comparison.

The 0.13-μm SiGe dividers were tested in packaged form at room temperature. Fig. 31 shows the 50-GHz output of the dynamic divider at 100-GHz input clock frequency. The output voltage swing is 260 mVpp (single ended). The exact value of the input power of the 100-GHz signal applied to the divider is not known, but is estimated to be from 0 to +4 dBm. At the input frequencies in the 30–50-GHz range, the dynamic divider required only −7 dBm of input clock power and provided a 500-mVpp output (single ended). Above 60 GHz, the minimum input power of the clock signal was in the 0- to +4-dBm range. However, applying 0 dBm of the input clock power, divided output signals for input frequencies down to 14 GHz can be seen. The 0.13-μm SiGe static divider was operational from 2 to 62 GHz (tested with a sinusoidal input signal). Fig. 32 shows the sensitivity of the input signal of the SiGe static divider and compares it to static divider based on an AlInAs–InGaAs HBT [76]. For the SiGe static divider, −1 dBm of input power was required for 62-GHz operation. For a similar power supply voltage of −3.6 V, the tail current in the SiGe divider is 2.8 mA compared to 9 mA in the AlInAs–InGaAs based divider. Speed can be traded off for power in these circuits, and this is shown in Fig. 33, where divider operation at 30 GHz is demonstrated at 380-μA tail current. This corresponds to $\sim$7$\times$ lower current

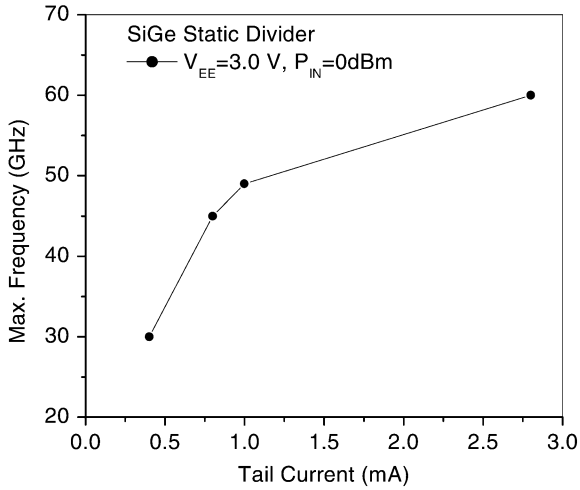

Fig. 33. Maximum input frequency of static dividers versus bias (tail) current in 0.13-μm SiGe technology.

compared to the static dividers made in the 0.18-μm SiGe generation (described below).

The static dividers in 0.18-μm technology were tested on-wafer at room temperature using high-speed picoprobes. Table IV summarizes the measured performance parameters of the dividers. "ECLi" in this table refers to a designs using inductive peaking. Static dividers self-oscillate when no external clock signal is applied (floating inputs). The frequency of this oscillation is an important parameter ($f_{\rm SO}$ in this table) and it is directly related to the maximum speed that can be achieved by a static divider. Comparing the self-oscillation and maximum speed data for the 0.13- and 0.18-μm SiGe ECL static dividers, we observe approximately a 2$\times$ increase in performance, which is in rough correspondence with a 2$\times$ increase in f_T and $f_{\rm max}$. Bandwidth at the 0.18-μm node can be increased further to 41 GHz with the use of inductive peaking.

C. VCOs for Clock Implementation in OC-768

Standards such as OC-768 (for 40-Gb/s optical communication systems) demand very low jitter in the transmitted and received data. Robust (noise immunity from supply and control noise) low phase-noise VCO designs are critical in achieving the jitter budget in these 40-Gb/s applications. SiGe BiCMOS technology enables both FET and bipolar based *LC*-VCO implementations. Low-loss *LC* tank circuits are formed using an inductor in the top metal level and with either junction and/or MOS varactors. The half rate architecture for 40 Gb/s needs $\sim$20-GHz VCO with precise quadrature phases. Both bipolar and FET-based implementation of such *LC* VCOs with digitally selectable bands have been realized with the 0.18-μm SiGe technology [71]. In the receiver block, the half-rate quadrature VCO is built with two coupled CMOS *LC* VCOs (schematic shown in Fig. 34), each one employing two back-to-back cross-coupled inverters to form the negative resistance required for oscillation. The VCO operates in 16 digitally controlled overlapping frequency bands, allowing the VCO gain within the loop to be small, thus reducing its noise sensitivity and improving loop phase-noise performance. The frequency tuning range in

TABLE IV
COMPARISON OF STATIC AND DYNAMIC FREQUENCY DIVIDERS IN 0.18- AND 0.13-μm SiGe TECHNOLOGY.

	0.13 μm SiGe		0.18 μm SiGe	
	Dynamic ECL	Static ECL	Static ECL	Static ECLi
V_{EE} [V]	-3.8	-3.8	-3.6	-3.6
f_{SO} [GHZ]	none	24	9	18
f_{CLK} [GHZ]	100	62	33	41

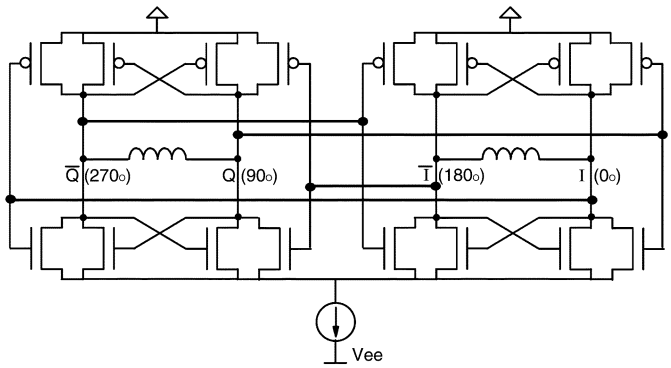

Fig. 34. Schematic of a quadrature LC VCO.

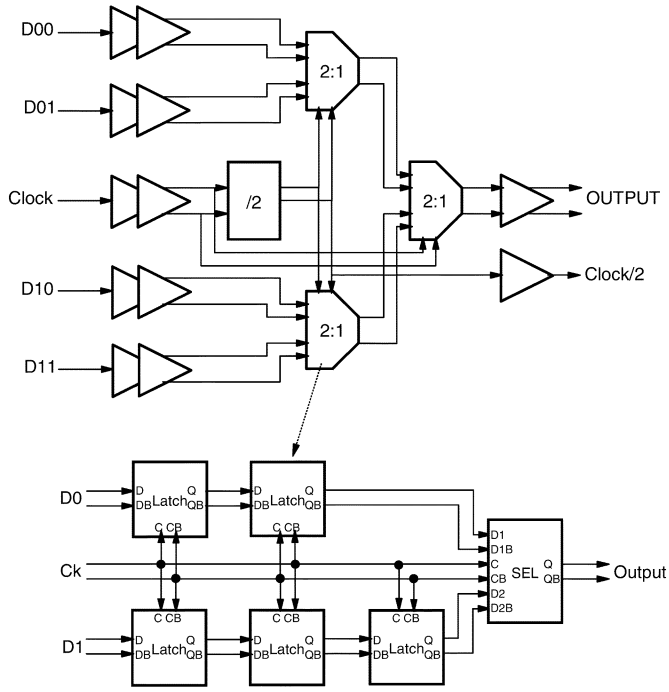

Fig. 35. Simplified block diagram of the 4:1 MUX circuit.

each band, however, is large enough to cover temperature and supply voltage variations without requiring crossover into an adjacent band. The measured total tuning range for the coupled VCO in the PLL is ~2.3 GHz. Within a typical band, the tuning range is 800 MHz with temperature and supply voltage sensitivity less than 1.9 MHz/°C and 133 MHz/V, respectively. The free-running VCO phase noise at 21.5 GHz was measured to be −103 dBc/Hz at a 1-MHz offset from the carrier. The current flowing in each VCO tank is ~9 mA. The transmit chip uses a bipolar *LC* VCO, which employs a positive feedback cross-coupled differential pair to generate the negative resistance required for oscillation. This VCO, like the VCO in the receiver, operates in 16 digitally controlled overlapping frequency bands. The measured total frequency tuning range of the VCO is ~1.8 GHz. For a typical tuning range in a given band of 600 MHz, temperature and supply voltage sensitivity are less than 3.5 MHz/°C and 190 MHz/V, respectively. The free-running VCO phase noise at 21.5 GHz was measured to be −100 dBc/Hz at a 1-MHz offset from the carrier. The current flowing in the tank is ~6 mA.

D. MUX

Time-division digital multiplexing is a central operation in communication systems. The device and layout parasitic are critical to obtaining low jitter and clock phase margin in the circuit. The MUX circuit block diagram is shown in Fig. 35. It uses a tree architecture with a recursive series of 2:1 MUX stages. The logic family chosen for this design is emitter-coupled logic, which offers sufficient performance while enabling the use of supply voltages in the −3.3-V range. Single-ended internal signal swing levels were chosen to be 300 mV throughout the design, providing adequate signal-to-noise ratio without demanding a larger supply voltage.

The MUX integrated circuit, implemented with the 0.18-μm SiGe technology, takes four parallel single-ended data at its input and uses a half-rate clock frequency, e.g., 20 GHz for 40-Gb/s operation [70]. This clock is internally divided by two with a static divider (built with a toggle flip-flop) in order to latch the four parallel data inputs and perform the first multiplexing operation. On-chip clock distribution was carefully done in order to avoid excessive ringing or damping due to layout parasitics, especially layout parasitic inductance because of the high fan-out on the clock (six for each MUX). Operation of the circuit was verified up to 70 Gb/s with $2^{31}-1$ pseudorandom bit sequence (PRBS) data inputs. At 60 Gb/s and −3.6-V supply, the Q-factor (defined as the ratio of the eye diagram mean amplitude to the noise on high and low levels) of the eye-diagram is approximately 7.1. Fig. 36 shows the eye diagram at 60 Gb/s at room temperature and at 100 °C chip temperature. Consistent operation has been seen when varying the

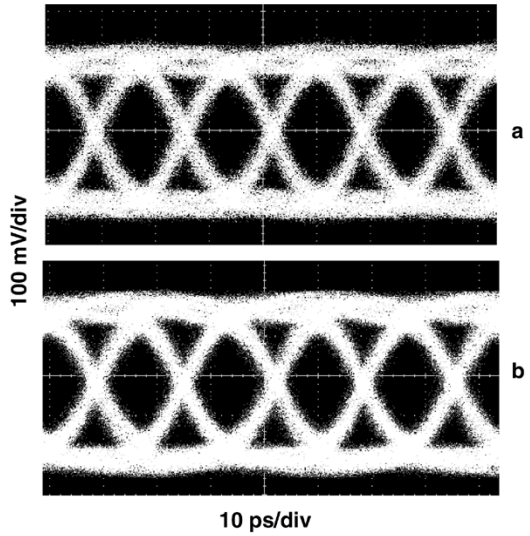

Fig. 36. 60-Gb/s output eye-diagram of the 4:1 MUX at −3.6-V supply voltage. (a) At room temperature. (b) At 100 °C chip temperature.

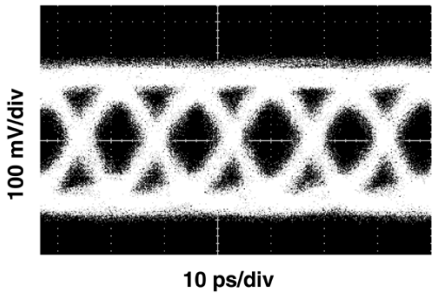

Fig. 37. 70-Gb/s output eye-diagram of the 4:1 MUX at −3.7-V supply voltage.

supply voltage from −3.3 to −3.6 V. Fig. 37 shows the eye diagram at 70 Gb/s and −3.7-V supply voltage with a Q-factor better than 5.6.

VI. Conclusion

The relentless device scaling supported by the state-of-the-art Si technology, along with the availability of Si-based bandgap engineering with the advent of high-quality SiGe alloy films, have led to SiGe HBTs exhibiting record f_T of 375 GHz and associated $f_{\max}$ of 210 GHz. Innovative structure modifications such as a raised extrinsic base have significantly contributed to base resistance reduction, leading to the minimum noise figure $F_{\min}$ of below 0.4 dB at 10 GHz. Reliability analysis has proven the device robustness against the increased current density and avalanche multiplication that stemmed from the device scaling. The multihundred-gigahertz SiGe HBTs have successfully been applied to various circuit blocks for broad-band communication applications, leading to a 3.9-ps delay ECL ring oscillator, 100-GHz frequency divider, 70-Gb/s 4:1 MUX, etc. With no obvious roadblock to further device speed enhancement, the march toward the terahertz band with Si technology will continue for the foreseeable future, opening enormous opportunities for terahertz-band applications.

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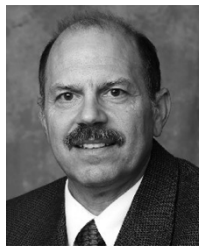

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