A −189 dBc/Hz $\mathrm{FOM_T}$ Wide Tuning Range Ka-band VCO Using Tunable Negative Capacitance and Inductance Redistribution

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***Abstract* — An ultra wideband LC voltage-controlled oscillator (LC-VCO) operating in the Ka-band with equally spaced sub-band coarse tuning characteristics is proposed and characterized. A tunable negative capacitance (TNC) circuit technique is used to cancel the fixed capacitance in the LC-tank to extend the tuning range (TR). A digitally-switched varactor coarse tuning structure with an inductance redistribution technique is utilized to reduce VCO gain (K_V) and retain uniform spacing between tuning curves. The proposed VCO structure and a baseline VCO are fabricated in a 130 nm CMOS process. Compared to the reference VCO, the proposed VCO achieves a 34% increase in TR with maximum K_V of 450 MHz/V. The measured worst-case phase noise is −100.1 dBc/Hz at 1 MHz offset across the TR from 30.5 GHz to 39.6 GHz. The power dissipation of the VCO core is 11 mW from a 1.2 V supply. The TNC-based VCO achieves a $\mathrm{FOM_T}$ of −189 dBc/Hz, which is the highest reported at the Ka-band.**

I. Introduction

As future wireless and wireline systems continue to push the available bandwidth and shift towards mm-wave frequencies, RF CMOS is expected to remain the predominant technology of choice. This is mainly driven by the continued scaling of digital CMOS technology in accordance with Moore's law, which has greatly benefited RF and Analog circuits in terms of higher transistor f_T, improved device matching and lower noise. Unfortunately, this trend is not perpetuated easily in designing mm-wave VCOs, as designers are confronted with key challenges that limit performance and yield. In designing low frequency LC-VCOs, wide tuning range (TR) and low phase noise can be obtained by employing a parallel combination of course-tuned switched capacitors and fine-tuned MOS varactors. However, as the design shifts to mm-wave frequencies, issues such as low Q-factor of the MOS varactor, higher losses incurred in the switched-capacitor elements and parasitic capacitances from the transistors and varactor, result in a sharp degradation in the resonator Q and limited TR. To counter these issues, inductive mode control techniques [1] or distributed transmission line structures [2] has been proposed and demonstrated a wide TR at the expense of increased phase noise or power consumption. In [3], push-push frequency doubler is validated to double the VCO frequency without degrading the wide TR of the original low frequency VCO. Due to the low efficiency of harmonic generation, the push-push VCO consumes high power. By utilizing a negative capacitance (NC) circuit, an increase in VCO TR is demonstrated in [4]. However, this structure is only applicable to bottom-based VCOs. Compared to top-biased VCOs, they are characterized by lower phase noise performance.

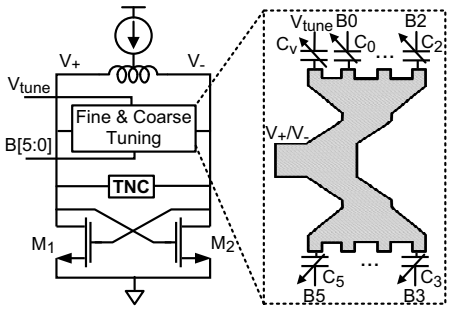
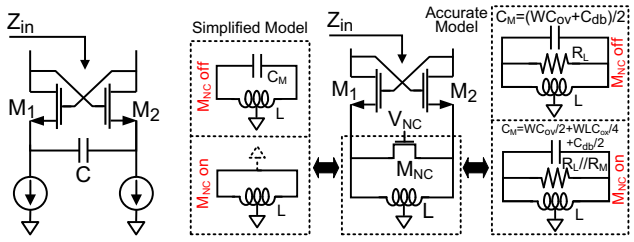


Fig. 1. An LC-VCO with TNC and inductance redistribution.

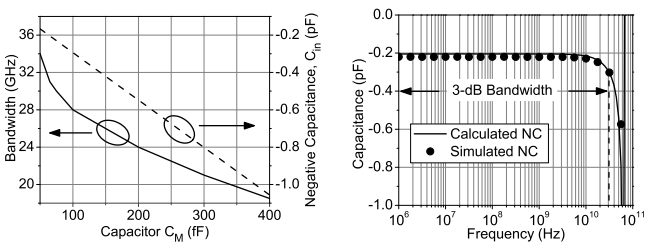
In this paper, we propose a tunable negative capacitance (TNC) technique to extend the TR of top-biased mm-wave VCOs with minimal impact on phase noise, power consumption or die area. We further present a feed structure to connect a large network of coarse-tuning capacitors while providing uniform spacing between tuning curves. Fig. 1 illustrates a conceptual structure of the implemented VCO in 130 nm CMOS. To the best of the authors' knowledge, this is the first CMOS VCO that achieves a low VCO gain (K_V) of 450 MHz/V and TR of 26% at 35 GHz with a record figure-of-merit-with-tuning ($\mathrm{FOM_T}$) of −189 dBc/Hz.

The paper is organized as follows: Section II analyzes the NC structure as part of the LC-VCO. The limitations of conventional VCO feed structures are analyzed in section III, along with the proposed feed structure. Section IV presents measurement results followed by a conclusion in Section V.



(a) (b)

Fig. 2. (a) An NC circuit with a cross-coupled pair with biases at the bottom. (b) The proposed NC structure and the equivalent circuit when M_{NC} is off.



(a) (b)

Fig. 3. (a) The scalable NC and corresponding bandwidth of Fig. 2(b). (b) NC of Fig. 2(b) when $C_M = 65$ fF.

II. TNC VCO Design and Operation Principle

A. NC Circuits

An ultra wideband NC circuit can be realized using a negative-g_m cross-coupled pair (M_1 and M_2) and a capacitor between the source pair [4], as shown in Fig. 2(a). The single-ended input capacitance is expressed as

$$C_{in}(\omega) = -2 \cdot \frac{g_m^2 C + \omega^2 C C_{gs}^2}{g_m^2 - \omega^2 C_{gs}(C_{gs}+C)}. \quad (1)$$

C_{in} is negative when $\omega^2 < g_m^2/C_{gs}(C_{gs}+C)$. The single-ended parallel resistance is given by

$$R_{//}(\omega) = -\frac{g_m^2 + \omega^2(C_{gs}+2C)^2}{4\omega^2 g_m C(C_{gs}+C)}. \quad (2)$$

Note that at high frequencies, $R_{//}$ is approximately equal to $-1/g_m$ when $C > C_{gs}$, implying minimal degradation in the negative resistance of the cross-coupled pair.

While this structure lends itself to bottom-biased VCOs, combining it with a top-biased VCO is difficult since the NC circuit in Fig. 2(a) is biased at the bottom. To counter this, an inductor is added in parallel with a digitally-switched MOS transistor (M_{NC}), as shown in Fig. 2(b). Off and on capacitance of M_{NC} is utilized to generate TNC. The inductor L is designed to have high impedance up to the desired frequency range while providing a constant DC current to bias the cross-coupled pair. To illustrate the circuit operation, a simplified model in Fig. 2(b) is analyzed. When M_{NC} is off, the input impedance is calculated as

$$Z_{in} = -\frac{X + 2/sL}{2(g_m - sC_{gs})(sC_M + 1/sL) - 4sC_{gd}X - 8C_{gd}/L} \quad (3)$$

where $X = s(C_{gs}+2C_M)+g_m$. At low frequencies, to a first order approximation, $C_{in} = -2C_M + 4C_{gd}$. Therefore, the input NC is scalable with C_M, as shown in Fig. 3(a). The bandwidth is given by $g_m/2\pi(1+2C_M/C_{gs})C_{gs}$ and can be extended to tens of GHz depending on the transistor f_T and the value of C_M, as depicted in Fig. 3(a). To verify the result, the NC circuit in Fig. 2(b) is designed and the simulated C_{in} is consistent with the simulation (Fig. 3(b)). When M_{NC} is on, Z_{in} has only a real part of $-1/g_m$ to a first order approximation and does not contribute any NC.

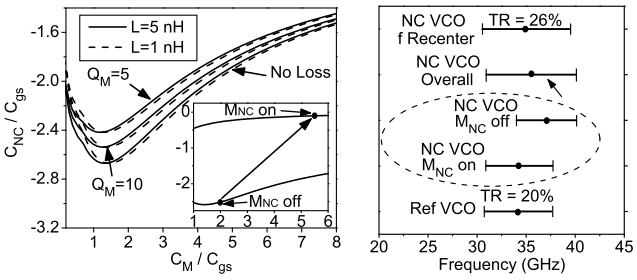
B. Top-biased TNC LC-VCO

The above section illustrates the NC principle within the bandwidth of operation. However, in the proposed design, since the VCO operates above the 3-dB bandwidth of the NC circuit, an accurate model including the losses and parasitic capacitance of an on-state M_{NC} is used (Fig. 2(b)). Assuming the fixed capacitance of the cross-coupled pair is C_{cc} ($C_{cc} = 2C_{gs} + 4C_{gd}$), the amount of canceled parallel capacitance C_{NC}, which is defined as $C_{NC} = C_{in} - C_{cc}$, can be derived from (3) as

$$\frac{C_{NC}}{C_{gs}} = -\frac{2H[1-(1+2H)(f/f_T)^2 - 4K(1+K)]}{(1+2K)^2 + (1+2H)^2(f/f_T)^2} + \frac{4C_{gd} - C_{cc}}{C_{gs}} \quad (4)$$

where $H = C_M/C_{gs} - 1/4\pi^2 f^2 L C_{gs}$, $K = (H/Q_M)(f/f_T)$. Fig. 4(a) shows C_{NC} for different Q_M and L. When M_{NC} is off, C_M equals $(WC_{ov}+C_{db})/2$. Since the resistance of M_{NC} is high, Q_M is dominated by the inductor loss R_L. When the switch is on, C_M is $WC_{ov}/2 + WLC_{ox}/4 + C_{db}/2$. The total loss is $R_L // R_M$, where R_M is the on-state differential resistance of M_{NC}. The inset in Fig. 4(a) depicts the change of C_{NC} as M_{NC} turns from off to on. A wide TR of C_{NC} from $-2.5C_{gs}$ to $-0.1C_{gs}$ is achieved. Note that C_{in} is kept at $-1/g_m$ at both on and off states.

To demonstrate the TR improvement, a top-biased VCO (Fig. 1) is designed without TNC, serving as a reference VCO. The reference VCO covers a TR of 6.8 GHz around 35 GHz. Adding the TNC element in Fig. 2(b) to the VCO and switching M_{NC} extends the frequency TR by 31% and increases the frequency of operation, as shown in Fig. 4(b). To maintain the same center frequency, the capacitors in the coarse tuning structure are resized. It is worth noting that while extending the TR of the VCO, the TNC does not incur additional power consumption or degradation in its phase noise.



(a) (b)

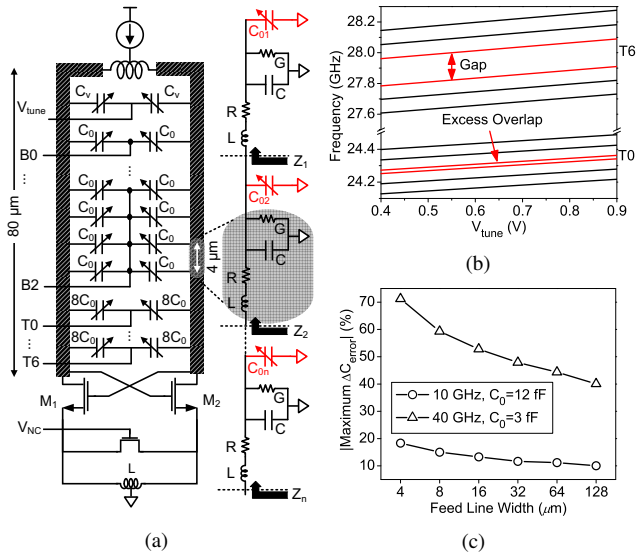
Fig. 4. (a) C_{NC} vs. C_M for different Q_M and L. The inset shows C_{NC} in the top-biased VCO changes as M_{NC} turns on and off. (b) TR extension from the ref. VCO to the TNC VCO.

III. Coarse Tuning VCO With Inductance Redistribution

In order to reduce the AM-PM noise conversion and hence the overall phase noise of the VCO, digital coarse-tuning is often employed to lower the K_V. A coarse tuning structure typically utilizes a binary-weighted switched-capacitor (C-DAC) array to reduce the number of capacitors and simplify the tuning control logic. However, for higher number of coarse tuning bits, a segmented or thermometer-weighted C-DAC is preferred to ensure monotonicity across the TR. To connect across such a large number of C-DAC elements, a long feed line is required. This comes at the expense of large parasitic inductance. Since the capacitance step per digital word (C_{step}) at mm-wave frequencies is in the order of fFs, the parasitic inductance significantly alters the effective capacitance of the varactor bank, leading to non-uniform f_{step}. The following subsections further explain the limitations of conventional feed structures and detail the proposed solution.

A. Conventional Capacitor Bank Structure

A 6-bit C-DAC is implemented as 50 % segmented, i.e. thermometer code is employed for the 3 most significant bits (T0-T6), while the other 3-bits are binary coded (B0-B2), as shown in Fig. 5(a). The feed line structure is modeled using Sonnet EM simulator. By switching T3-T6, a higher capacitance is added to/subtracted from the tank, resulting in a large frequency gap, as illustrated in Fig. 5(b). Since bits T3-T6 are close to the cross-coupled pair, they have more impact on changing the effective capacitance. Conversely, bits T0-T2 which are farther away from the cross-coupled pair have minimal impact on changing the tank capacitance. Therefore, switching T0-T2 results in an excess overlap between tuning curves, as shown in Fig. 5(b). Without considering these routing parasitics, neither gaps nor excess overlaps would exist across the TR.



(a) (b) (c)

Fig. 5. (a) The conventional capacitor bank. (b) Frequency tuning curves of the conventional structure. (c) Maximum ΔC_{error} vs. the feed line width at 10 GHz and 40 GHz.

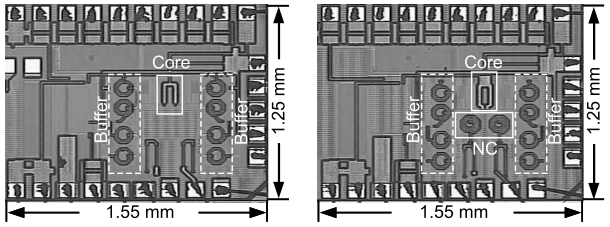
Since the distance between two successive capacitors is 4 μm, which is smaller than one-twelfth of the wavelength in the Ka-band, this segment is modeled by a lumped RLCG model (Fig. 5(a)). To demonstrate the impact of the line inductance on the effective capacitance, two segments of the line are considered. Neglecting the resistive losses and mutual coupling, the effective capacitance is given by

$$C_{\mathit{eff}}(\omega) = \frac{C_{X1} + C_{X2} - \omega^2 L C_{X1} C_{X2}}{\omega^4 L^2 C_{X1} C_{X2} - \omega^2 L (C_{X1} + 2C_{X2}) + 1} \tag{5}$$

where $C_{X1} = C_{01} + C$ and $C_{X2} = C_{02} + C$. For $L = 0$, C_{eff} is reduced to $C_{X1} + C_{X2}$. However, the inductance of the feed line introduces error to the effective capacitance by adding the capacitances in a non-uniform way. The error in C_{step}, $\Delta C_{\text{error}} = C_{\text{step}}/C_{\text{step,ideal}} - 1$, can be reduced by decreasing the line inductance. As depicted in Fig. 5(c), the line inductance affects the effective capacitance significantly at high frequencies. While increasing the width of the routing trace reduces its inductance and ΔC_{error}, the capacitance increases reducing the frequency and TR.

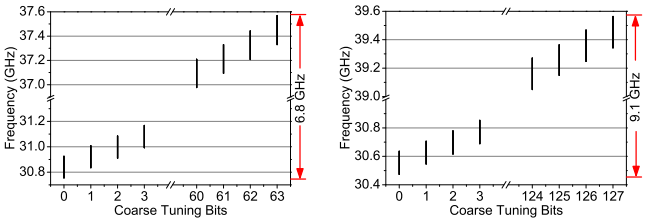
B. Tree Structure

As shown in Fig. 1, the proposed tree feed structure is realized with equal routing inductance between the g_m devices and each capacitor in the tuning structure, resulting in minimal variation in f_{step}. Each branch of the tree has a unit varactor (C_0) controlled by the binary bits and $8C_0$ controlled by the thermometer bits. The tree structure uses a wide line to minimize its resistive losses and inductance. The tree structure is also modeled using



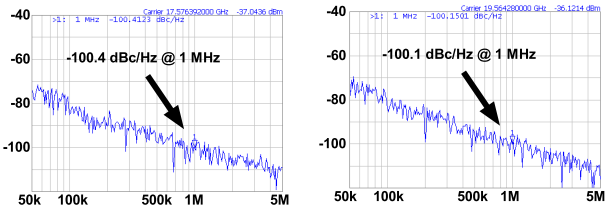
(a) (b)

Fig. 6. Micrograph of (a) the ref. VCO and (b) the TNC VCO.



(a) (b)

Fig. 7. Measured tuning curves of (a) the ref. VCO and (b) the TNC VCO.



(a) (b)

Fig. 8. Measured phase noise of (a) the ref. VCO at 37.58 GHz, (b) the TNC VCO at 39.56 GHz.

Sonnet EM simulator. The TR is simulated to be uniform without any gaps from 30.8 GHz to 37.6 GHz.

IV. Measurement Results

Two inductance redistributed VCOs with/without TNC are fabricated in a standard eight metal 130 nm CMOS process with each VCO occupying an area of 1.25×1.25 mm^2, as shown in Fig. 6. The VCO cores occupy areas of 200×250 μm^2 and 180×250 μm^2, respectively. The chips are wire-bonded on a printed circuit board, which provides all DC and RF connections. Fig. 7 shows the tuning curves of the two VCOs measured by an Agilent E4440A spectrum analyzer with an additional down conversion mixer to extend the measurement frequency range up to 40 GHz. As expected, the TNC VCO covers a wide TR from 30.5 GHz to 39.6 GHz with uniform f_{step}. Compared to the reference VCO, the TR of the TNC VCO increases from 6.8 GHz to 9.1 GHz. The phase noise, averaged over 100 measurements, is captured using an Agilent E5052B signal source analyzer and shown in Fig. 8. At 1 MHz offset, the phase noise of the reference VCO ranges from -102.8 to -100.4 dBc/Hz across the TR. With TNC, the phase noise is from -102.7 to -100.1 dBc/Hz. The VCO core draws 9 mA of current from a 1.2 V power supply. To evaluate the TR of the two VCOs along with phase noise, FOM$_{\text{T}}$ [2] is utilized:

$$\text{FOM}_{\text{T}} = L\{\Delta f\} - 20\log\left(\frac{f_0}{\Delta f}\cdot\frac{\text{TR}}{10}\right) + 10\log\left(\frac{P}{1\,\text{mW}}\right). \quad (6)$$

Table I summarizes the comparison to other state-of-the-art VCOs. The proposed TNC VCO achieves the highest FOM$_{\text{T}}$ among VCOs with similar center frequency.

V. Conclusion

A wide TR TNC-based LC-VCO with the inductance re-distribution technique operating in the Ka-band is proposed, designed and fabricated in a standard 130 nm CMOS process. The implementation of the TNC is demonstrated to extend the TR of the 35 GHz VCO to 9.1 GHz with minimal impact on phase noise and power consumption. By applying a tree coarse tuning structure, the frequency sub-bands are equally spaced with a maximum K_V of 450 MHz/V and a FOM$_{\text{T}}$ of -189 dBc/Hz.

TABLE I
Performance Summary of Wide TR mm-wave LC-VCOs

Reference	Process	Freq (GHz)	TR (%)	Phase Noise (dBc/Hz)	Power (mW)	FOM$_{\text{T}}$
[1]	65nm CMOS	42.1	43	-89.5@1MHz	5.8	-187
[2]	180nm CMOS	40	20	-100@1MHz	27	-184
[3]	65nm CMOS	77	15	-88@1MHz	190	-166
[4]	130nm CMOS	40	27	-95@1MHz	12	-185
Ref VCO	130nm CMOS	34.2	20	-100.4@1MHz	11	-187
TNC VCO	130nm CMOS	35	26	-100.1@1MHz	11	-189

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