# A Compact Millimeter-Wave Energy Transmission System for Wireless Applications

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***Abstract* — A compact energy transmission system in 40nm standard CMOS is presented. The system consists of a 60GHz VCO followed by a quad-core power amplifier as transmitter and an RF-to-DC converter as receiver. The total power delivered by the quad-core PA to its four 50Ω loads is 24.6dBm. The receiver is a complementary cross-coupled rectifier with a measured efficiency of 28% while supplying 1mA of current. The system can support amplitude and frequency modulations and beam-forming capabilities for wireless applications with minimal front-end complexities.**

***Index Terms* — Energy transmission, mm-wave power amplifier, mm-wave VCO, power harvesting, millimeter wave integrated circuits, and 60GHz ISM band.**

## I. Introduction

Demand for seamless mobility and sensor fusion into a number of new products requires compact and efficient power sources. Battery is a size, cost, and performance bottleneck for many handheld systems and sensors. For modern wireless systems there is a growing interest in compact and efficient wireless power and data transmission. Power harvesting using mm-wave frequencies, and within the 60GHz ISM band in particular, has the following distinct advantages. Highly directive antenna arrays can be realized with compact footprints. In addition, the allowed EIRP level in this band is larger than in other bands, which is especially beneficial for energy transmission systems. Also comparably higher path loss at farther distances in this band limits the potential interference of this system to coexisting wireless systems.

The proposed energy transmission system is an alternative technology for NFC applications with significant size and potential bandwidth advantages. It uses the 60GHz ISM band and with a small footprint transfers a high level of energy from the transmitter to the receiver. The system also provides AM and FM modulations and beam-forming capabilities with minimal front-end complexities. The solution includes a 60GHz VCO followed by a quad-core power amplifier as transmitter (Figure 1). Each of the four cores of the 60GHz quad-core PA generates 18.6dBm power at its 50Ω load; therefore, the quad-core PA can deliver a total power of 24.6dBm to a four-feed antenna array. This is, to the best of our knowledge, the highest reported power level delivered to the antenna at mm-wave frequencies in CMOS. The receiver consists of a complementary cross-coupled rectifier to convert the received RF power to DC with a measured efficiency of 28% while supplying 1mA of current (Figure 2). The system was implemented in 40nm bulk CMOS technology with 1.2V power supply at the transmitter side.

## II. Transmitter Architecture

As shown in Figure 1 the quad-core PA has a binary-tree architecture in which the output signal of each stage fans out to two symmetric paths in order to alleviate the voltage reliability concerns. Figure 1 depicts the schematic diagrams of the VCO and the first stage of each PA core. Each core chain has 5 cascaded tuned amplifiers. All the stages are common-source NMOS differential pairs loaded with transformers. All devices are 1μm/40nm low $V_T$ NMOS transistors with different multiple counts as specified in Figure 1. The floating-source cross-coupling neutralizing devices are used to improve the stability by eliminating the drain-to-gate capacitances of the differential pairs devices to create unilateral amplifiers in the price of increasing the effective drain parasitic capacitances due to doubling the junction capacitances.

The VCO consumes 54mA and covers from 61.64 to 62.08GHz using accumulation varactors. This analog frequency tuning can be used for frequency modulation. The binary-tree architecture requires the secondary coils of the transformers of the VCO and the first three stages of each PA core to have two different ends to split the output power while preserving the impedance matching conditions (Figure 2). Each stage has a switched-capacitor tank to adjust the tuning frequency. The second stage of each PA core has two sets of out-of-phased outputs to offer two distinct capabilities to the system: 14º beam-forming range which is possible due to $0^0$ to $180^0$ phase-shifting combinations for the four outputs of the quad-core PA and AM modulation by combining different weights of the out-of-phased outputs. Stage 4 and stage 5 of each PA core consist of 16 amplifiers. A transformer-based power combiner with a compact layout and a reasonable loss of

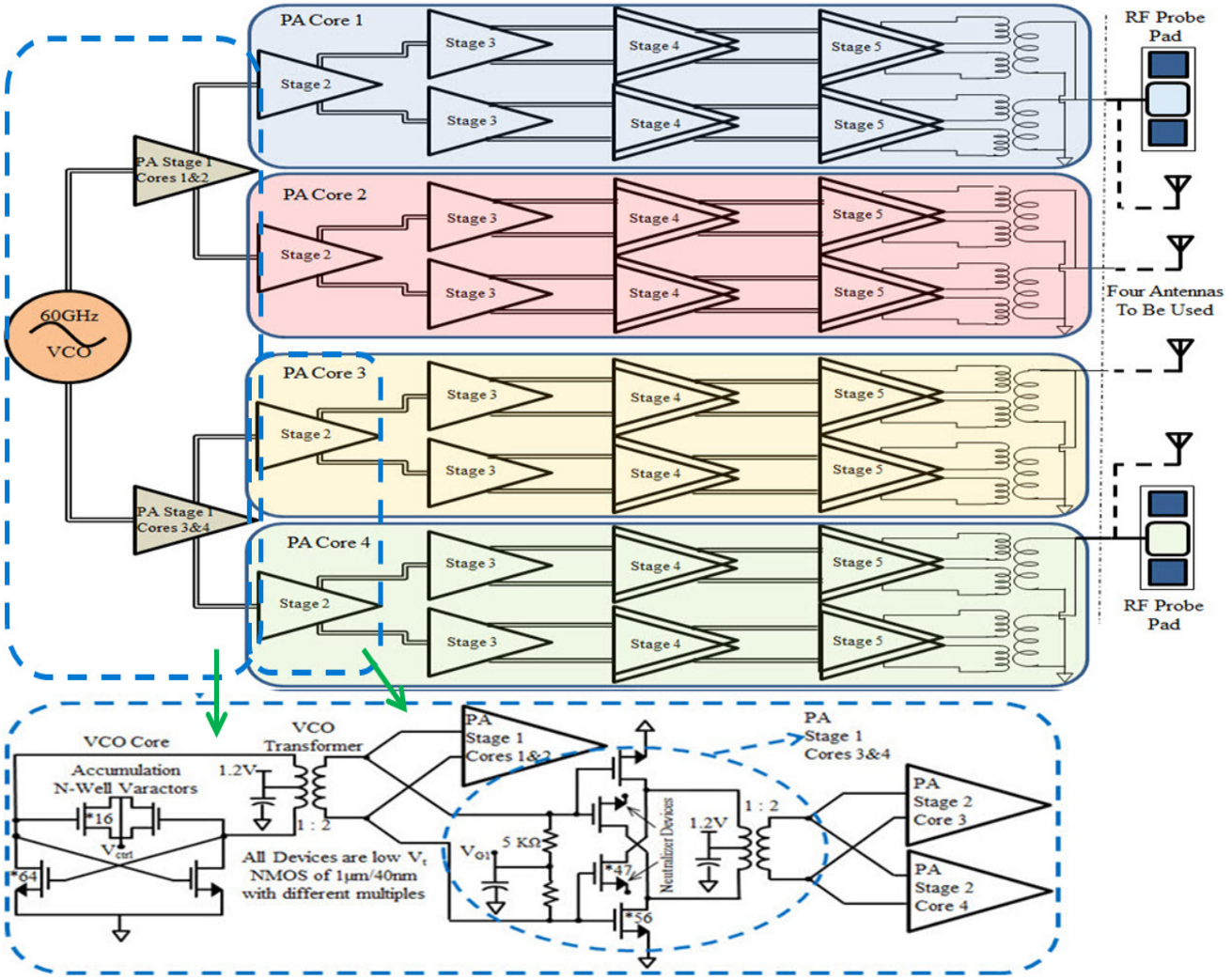


Figure 1: Block diagram of the power transmitter and the schematic diagrams of the VCO and the first stage of core 3 and 4 of the PA.

2dB is used at the very end of each of the four PA cores chains. The complete transmitter, the receiver, and the stand-alone single-core and quad-core PAs have been separately fabricated and measured (Figure 5).

A single 60GHz patch antenna on a substrate with a relative permittivity of 3 would only occupy 1.5mm×1.5mm ($\lambda_g/2$x$\lambda_g/2$). Having an element separation of 2.5mm ($\lambda_{air}/2$), a 4×4 phased-array antenna would occupy 10mm×10mm area. Compared to a typical NFC coil with the size of 30mm×40mm this system has a remarkable size advantage and also the ground plane underneath the antenna array makes it much less susceptible to the degradation by nearby conductive surfaces. Using the Friis transmission equation (Figure 2) the required PA output power can be calculated. With an element peak gain of about 5dBi, the phased-array patch antenna would have a peak gain of 15dBi, assuming 2dB routing loss. The total link loss is estimated to be 15dB at 4cm distance, which is the operating range of the NFC.

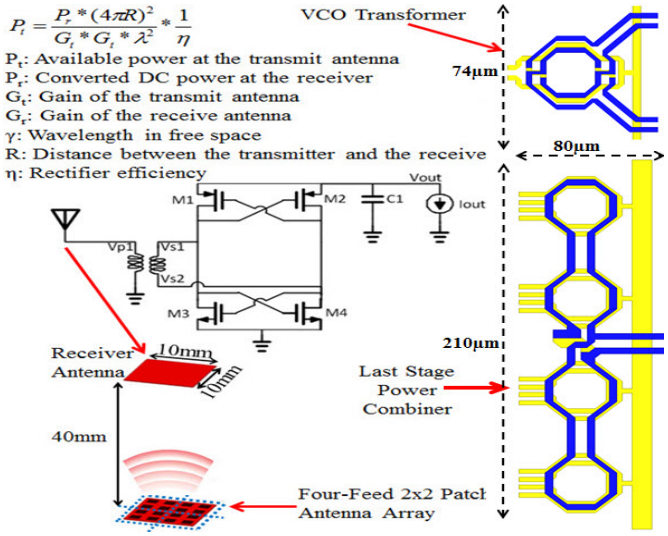


Figure 2: The patch antennas, the schematic of rectifier, and the layouts of VCO transformer and the last stage power combiner.

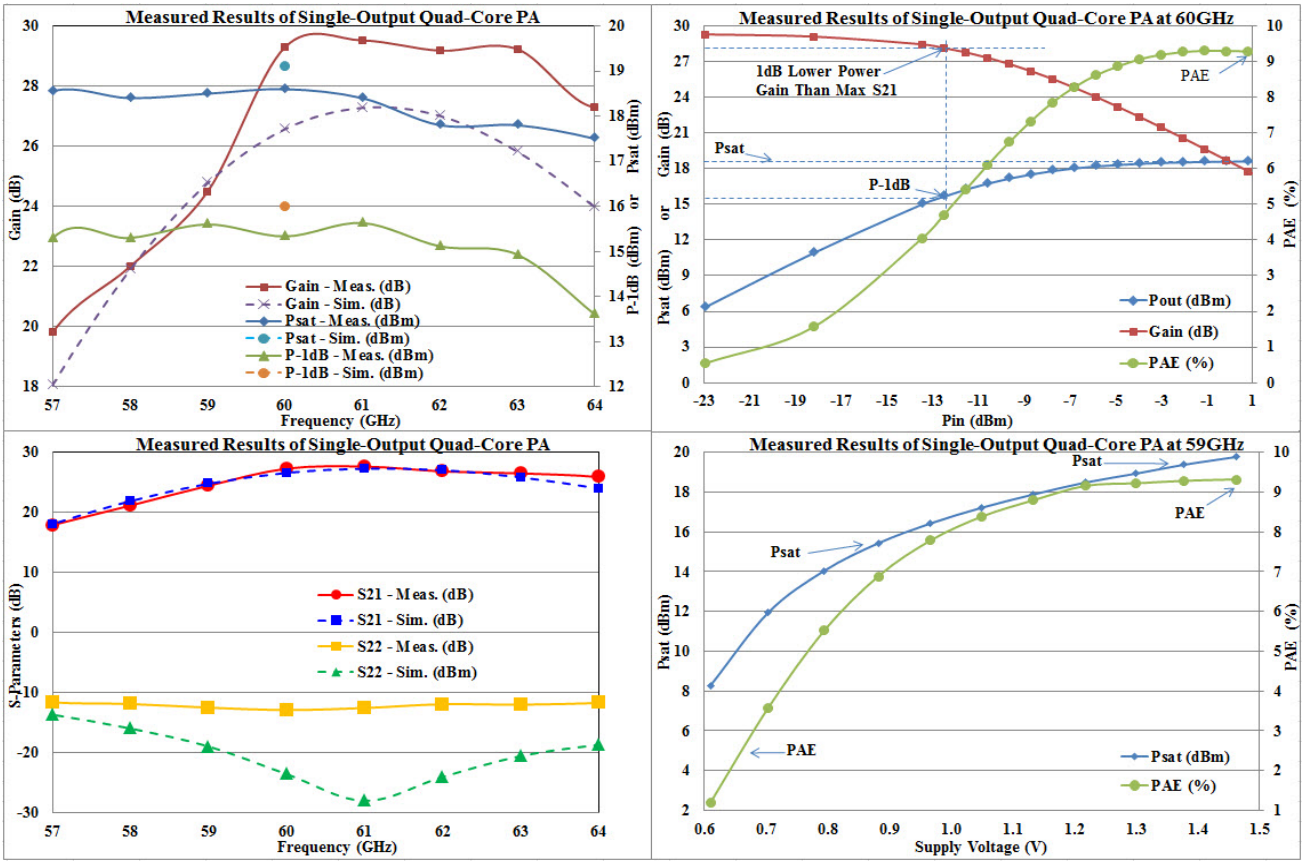


Figure 3: Measurement and simulation results of one of the four outputs of the quad-core PA.

Figure 3 presents the measurement results of key specifications of one of the four outputs of the quad-core PA and compares them with the simulation results. Table I summarizes these results and proves the achievement of the required specifications. Table II compares the measurement results of this work with those of the other published mm-wave CMOS PAs [2-5]. The measurement setup at the probe station is shown in Figure 6.

TABLE I: Measurement results

| Specification | Measurement Results of One Output of the Quad-Core PA | Projected Performance of the Combined-Output Quad-Core PA |
|---|---|---|
| Supply Voltage (V) | 1.2 | 1.2 |
| Current Consumption (A) | 0.625 | 2.5 |
| Bias Voltage of Stage 1 (V) | 0.6 | 0.6 |
| Bias Voltage of Stage 2 (V) | 0.55 | 0.55 |
| Bias Voltage of Stage 3 (V) | 0.62 | 0.62 |
| Bias Voltage of Stage 4 (V) | 0.85 | 0.85 |
| Bias Voltage of Stage 5 (V) | 0.92 | 0.92 |
| Linear Power Gain (dB) | 29.5 | 35.5 |
| Saturated Power Gain (dB) | 12.5 | 18.5 |
| $P_{1dB}$ (dBm) | 15.6 | 21.6 |
| $P_{SAT}$ (dBm) | 18.6 | 24.6 |
| PAE (%) | 9.2 | 9.2 |
| Area (μm * μm) | 550 * 350 | 850 * 550 |
| $P_{SAT}$ / Area (mW/mm$^2$) | 376 | 490 |

The DC current consumption of the quad-core PA is approximately 2.5A. A network of power and ground grids are deployed to minimize the IR-drop using the thick top metal layer and the RDL layer with equal resistances of 15mΩ/Sq. The effective resistance of the grid is less than 20mΩ not to introduce any significant drawback for efficiency, gain, or $P_{SAT}$. The local current densities should also be controlled to prevent the circuitry to get damaged and to meet the specified electro-migration and thermo-migration limits of the technology.

TABLE II: PA Results Comparison

| REF# / Specification | This Work | | [2] | [3] | | [4] | | [5] |
|---|---|---|---|---|---|---|---|---|
| | One Output | Four Outputs | | | | | | |
| CMOS Technology | **40nm** | **40nm** | 65nm | 65nm | 65nm | 65nm | 65nm | 90nm |
| Supply Voltage (V) | **1.2** | **1.2** | 1 | 0.9 | 1 | 1.2 | 1.8 | 1.2 |
| Current Consumption (A) | **0.625** | **2.5** | 0.48 | 0.49 | 0.53 | 0.77 | 1.0 | 0.6 |
| Combiner Loss (dB) | **0** | **1** | 0.63 | 1 | 1 | 1 | 1.0 | 1.1 |
| S21 (dB) | **29.5** | **35.5** | 20.3 | 18.9 | 19.2 | 14.3 | 15.5 | 20.6 |
| $P_{1dB}$ (dBm) | **15.6** | **21.6** | 15 | 13 | 15.1 | 11 | 11.5 | 18.2 |
| $P_{SAT}$ (dBm) | **18.6** | **24.6** | 18.6 | 16.8 | 17.7 | 16.6 | 18.1 | 19.9 |
| PAE (%) | **9.2** | **9.2** | 15.1 | 10.8 | 11.1 | 4.9 | 3.6 | 14.2 |
| Area (μm * μm) | **0.19** | **0.47** | 0.28 | 0.83 | 0.83 | 0.46 | 0.5 | 1.7 |
| $P_{SAT}$ / Area (mW/mm$^2$) | **376** | **490** | 256 | 59 | 72.3 | 99 | 140 | 58.7 |

## III. RECEIVER DESIGN

The receiver consists of an RF to DC power convertor. To serve this purpose, at lower frequencies rectifier architectures such as voltage multipliers are used [1]. The performance of such architectures degrades when mA-current is drawn from them. In this work a differentially driven complementary cross-coupled oscillator was used to rectify the received signal from the antenna [6]. The 1:2 transformer increases the impedance level such that the loading of the antenna on the resonant tank of the rectifier is minimal. When biased as an oscillator, the oscillation frequency is measured to be 60.5GHz resulting in a high rectifying efficiency at this frequency. The bigger the $C_1$ in Figure 2 is the more energy the rectifier can store, in the price of slower response for the system when used for supplying wireless communication circuitry. The efficiency is a nonlinear function of the received input power at the antenna and the load current. If needed, the rectifier can demodulate AM signals. Figure 4 shows the measurement results of the receiver and its de-modulated outputs when fed with 60GHz AM modulated signal with 200kHz modulation rate and 25% modulation depth.

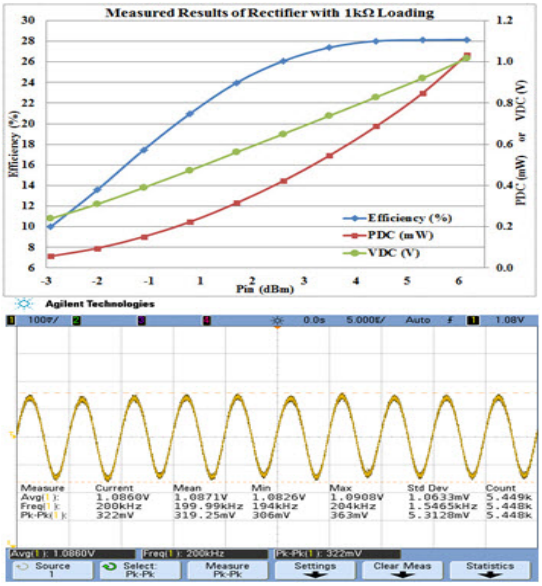


Figure 4: Receiver measurement results.

## IV. CONCLUSION

The 60GHz ISM band is a promising host for compact solutions for energy transmission and wireless communication. Both the receiver and the transmitter described in this work achieve acceptable performances compared with those of the other alternative technologies for energy transmission. The proposed quad-core PA demonstrates a remarkable high power delivery at 60GHz. The system supports AM and FM modulations and beam-forming capabilities with minimal front-end complexities.

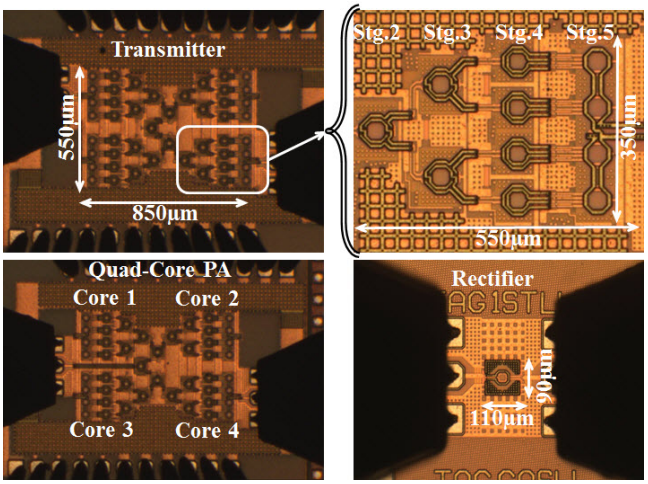


Figure 5: Die micrograph of the complete transmitter, the stand-alone PA core, the stand-alone quad-core PA, and the receiver.

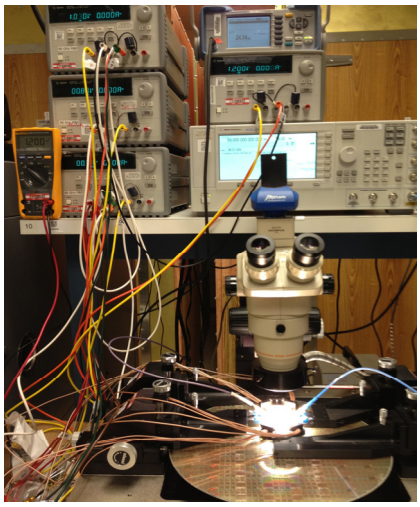

Figure 6: Measurement setup at the probe station.

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