A 135-170 GHz Power Amplifier in an advanced SiGe HBT technology

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***Abstract*— High-power, broadband power amplifiers (PA) operating in the D-band (110-170 GHz) are essential towards implementation of broadband frequency multiplier chains at sub-mmWave frequencies. In this paper we present the design of a 3-stage power amplifier (PA) with 3-dB bandwidth of 35 GHz (135-170 GHz) and implemented in 130 nm SiGe BiCMOS technology. A staggered tuning approach where the peak gain of the individual or group of individual stages are tuned at offset frequencies is used for broadband operation. In the 135-170 GHz, the small signal gain for the PA is 14-17 dB and the saturated output power (P_{sat}) varies from 5-8 dBm and the output referred 1 dB compression point (P_{1dB}) varies from 1-6 dBm over this frequency range. The nominal dc power consumption of this PA is 320 mW with peak PAE of 1.6%. To our best knowledge, this is the highest bandwidth reported for silicon PAs in the D band.**

***Index Terms*— Power amplifiers, D-band, 110-170 GHz, MMICs, Millimeter-wave integrated circuits, SiGe HBT, transmitter components, imaging.**

I. Introduction

PAs operating in the D-band form an essential component for realisation of multiplier chains at sub-mmWave frequencies. For multiplier chains, high output power and broadband operation of PA is essential. For typical implementation, PAs with reasonable gain can be implemented upto f_{max}/3 [1], [2]. In general operation at D-band enables several applications and the frequency band around 160 GHz is particularly interesting for 3D imaging, multi-Gbps wireless communications, radio astronomy and remote sensing [3]. On the receiver side, broadband low noise amplifier (LNAs) operating from 70-155 GHz with 25 dB gain and 3 dB bandwidth of 67 GHz have been reported in [4]. The recent advancement in silicon technologies have resulted in SiGe HBTs with f_{max} approaching 500 GHz [5]. This has enabled silicon PAs in the D-band with output power in excess of 10 dBm. At frequencies above 100 GHz, PA design is confronted with challenges like low output resistance and physical dimensions of the required tuning elements. In [6], a detailed discussion on the implications and origin of these challenges is presented along with the results of a narrowband 160 GHz PA with output power in excess of 10 dBm.

Multiplier chains implemented in silicon technologies and targeted for imaging applications above 300 GHz have been reported in [7] with output power of -3 dBm at 325 GHz. This was implemented by driving a frequency doubler with a narrow band PA at 160 GHz. In [8], output power of -17 dBm have been reported at 825 GHz where a PA at 165 GHz was used to drive a differential amplifier to generate the 5th harmonic. In these implementations, the narrowband PA limits the overall bandwidth of the multiplier chain.

PA with high bandwidth enables multi-Gbps communication systems and broadband frequency multiplier chains. This paper presents the design of a broadband 3-stage pseudo-differential PA with 3-dB bandwidth of 35 GHz (135-170 GHz) and implemented in 130 nm SiGe HBT technology with f_T/f_{max} of 300/450 GHz [9]. The design is based on the differential cascode topology described in [6]. In the 135-170 GHz, the small signal gain for the PA is 14-17 dB and the saturated output power (P_{sat}) varies from 5-8 dBm while P_{1dB} varies from 1-6 dBm. This paper is organized into 3 sections. Section 2 presents the circuit architecture for the PA and Section 3 presents the measurement results.

II. Circuit architecture

Fig.1 shows the schematic for the PA. For this implementation, differential topology is chosen due to the advantages like ability to drive on-chip differential antennas and multiplier circuits. Also, differential operation results in a virtual ground at the base of the common-base stage of the cascode amplifier and relaxes the need for extensive decoupling capacitors. For the HBTs T1-T4, the emitter area is 0.12x0.96 μm^2. For this technology, the back-end of the line offers 7 metalisation layers with 2 low loss thick metal layers.

The basic design principle for this circuit invloves tuning the peak gain frequencies for individual or group of individual stages at an offset frequency so as to make the overall power transfer broadband. In this design, a 3-stage topology is used with similar transistor sizes for all the 3 stages. The first two stages (Stage 1 and Stage 2) were

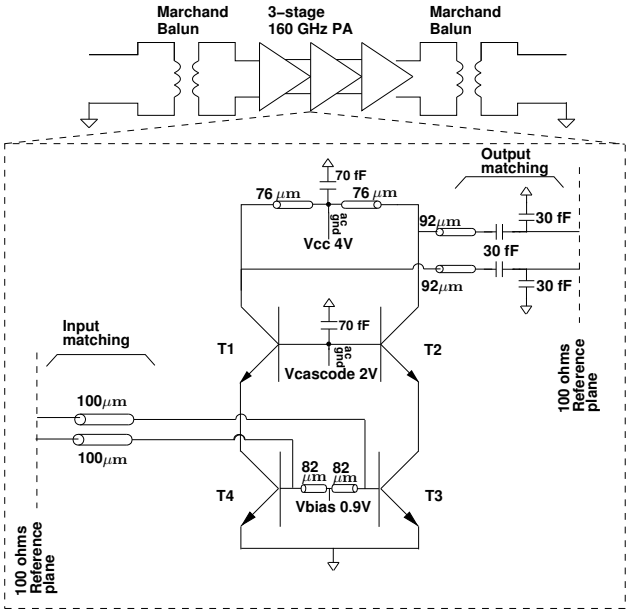


Fig. 1. Circuit schematic for a single stage of the PA. The emitter area for the HBTs T1-T4 is 0.12x0.96 μm^2. The transmission lines used in this design is based on side-shielded microstrip lines.

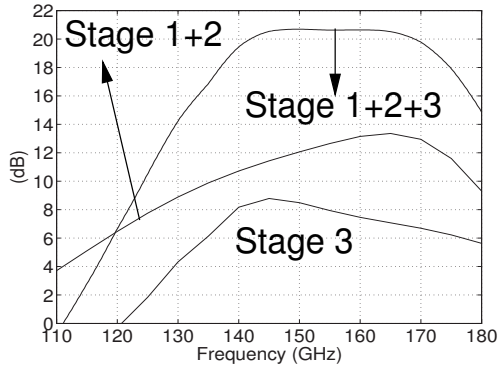


Fig. 2. Simulated small signal gain versus frequency for the different stages of the PA.

tuned to a higher frequency while the output matching for the last stage (Stage 3) was such that the peak gain frequency for Stage 3 is lower compared to Stage 1 and Stage 2. Fig. 2 shows the simulated gain for the different stages of the PA. The peak gain frequency for Stage 1 and Stage 2 is at 165 GHz while the peak gain for Stage 3 is at 145 GHz. This makes the overall gain broadband. The drop in gain with increase in frequency was accounted for by having two stages (Stage 1 and 2) tuned to the higher freqeuncy band (165 GHz). Fig. 3 shows the chip micrograph for the PA and the total chip area including the pads is 1.2x0.48 mm^2.

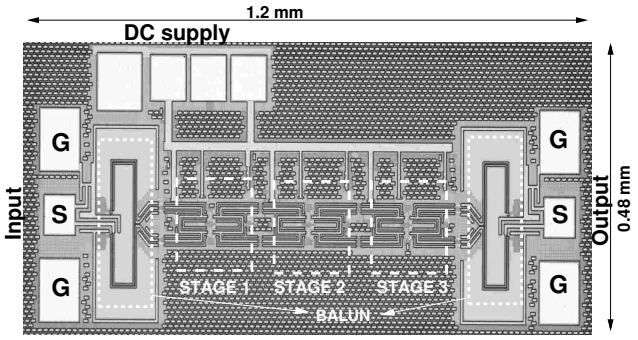


Fig. 3. Chip micrograph of the PA. The total chip area including the pads is 1.2x0.48 mm^2.

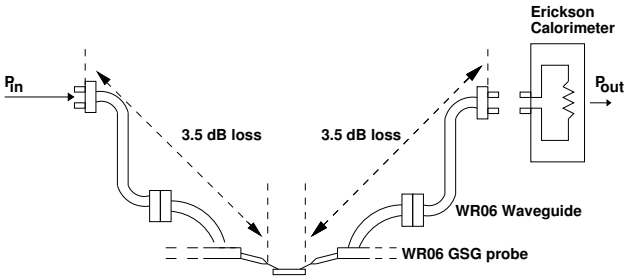
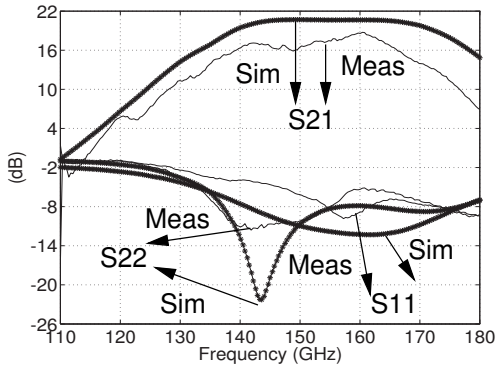


Fig. 4. Measurement setup for the large signal characterisation of the PA where one port is driven by the VNA extension module while the other port is connected to the power meter. For the small signal characterisation both the ports are driven by the VNA and is not shown in the figure.

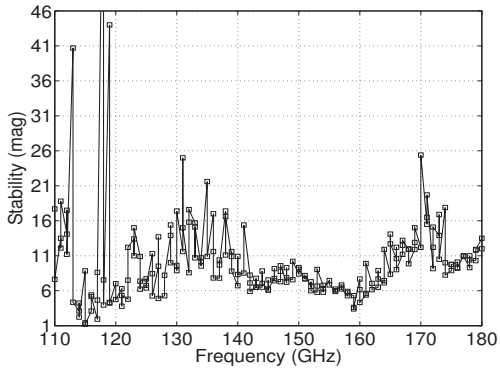
In this design side-shielded microstrip lines were used as inductive loads and for matching. A 3D electromagnetic simulator was used for modeling the passives. The use of side-shielded line minimises parasitic coupling between the different components or stages. The reduction in parasitic coupling between different components allows the use of scalable models for good simulation accuracy. This reduces simulation time and complexity as compared to unshielded lines where extensive EM simulation is required for accurate prediction of different parasitic effects. The signal line for the microstrip lines was implemented in the topmost metal layer with the ground plane in the third metal from the top. The use of such side-shielded lines have been reported in [10] and its modeling has been discussed extensively in [11].

III. Measurement results

The PA was characterised on wafer using using the setup shown in Fig. 4. For measurements, GSG WR-06-waveguide probes were used. For small and large signal measurements, Vector network analyser (VNA) extension modules operating in the D-band were used. The measured insertion loss due to the probe and waveguide is approximately 3.5 dB.

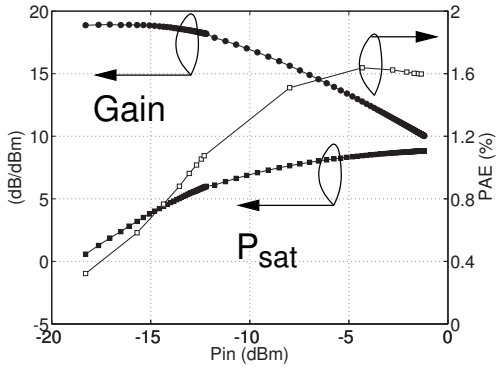


(a)

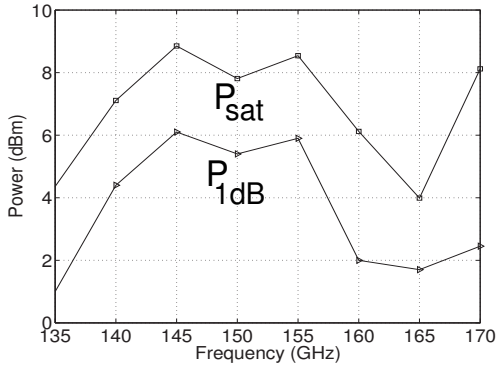


(b)

Fig. 5. Small signal model-hardware correlation of the PA. (a) Comparison between simulated and measured sparameters. (b) Measured Rollett's stability factor (K-factor).



(a)



(b)

Fig. 6. Large signal characterisation of the PA. (a) P_{sat}, Gain and PAE at 145 GHz. (b) P_{sat} and P_{1dB} from 135-170 GHz.

Fig. 5 shows the comparison between the simulated and measured small signal paramters S11, S22 and S21. For simulations, VBIC model [12] was used for the HBT and electromagnetic simulated models of the balun and the input/output pads have been included. The 3-dB bandwidth for the PA is 35 GHz with 14-17 dB gain from 135-170 GHz and the measured reverse isolation is below -40 dB. Due to modelling inaccuracies, discrepancy of 3-5 dB between simulated and measurement is seen for the measured S21 over this frequency range. The measured S21 is greater than 10 dB over a 45 GHz range from 130-175 GHz and the PA is unconditionally stable over this frequency range.

For large signal characterisation, power measurement was done using an Erickson calorimeter [13]. The mm-wave source modules, driven by the VNA, were first calibrated to account for their non-linear behavior. Additionally, an external amplifier was used at the output of the mmWave source modules to drive the PA into compression for P_{sat} measurement. Fig. 6 shows the result for the large signal characterisation of the PA. At 145 GHz, the P_{sat} is in excess of 8 dBm with 10 dB gain at compression. The measured P_{sat} varies from 5-8 dBm while the P_{1dB} varies from 1-6 dBm over the 135-170 GHz band. In the frequency range of 155-165 GHz, a drop of P_{sat} is seen and this corresponds to the drop in input drive from the source module and the external amplifier. The nominal dc power consumption for this PA is 320 mW and the peak PAE at 145 GHz is 1.6%.

IV. Conclusion

Power generation at sub-mmWave frequencies require frequency multiplier chains. The implementation of broadband frequency multiplier chains at sub-mmWave frequencies (300 GHz and above) is limited by the bandwidth of the PAs operating in the D-band. A bandwidth of 20 GHz for a PA operating at 160 GHz translates to an overall bandwidth of 60 and 100 GHz after x3 and x5 multiplication. At frequencies above 100 GHz, designing broadband PAs with high gain and output power is challenging and typical implementations are narrowband in nature. In this paper, a 3-stage differential PA operating in the D band and implemented in advanced SiGe HBT technology with

TABLE I
COMPARISON OF SILICON PAS IN THE D-BAND

Freq [GHz]	Tech [nm]	Mode[1]	Stages	P_{sat}[dBm]	GT_{max}[dB]	3 dB BW	f_T/f_{max}	Ref
135-170	SiGe 130	Differential	3	5-8	17	35	300/450	This work
155	SiGe 130	Single	5	8	35	less than 10	300/400	[14]
160	SiGe 130	Differential	3	10	32	12	300/400	[6]
140	SiGe 130	Single	5	-1	18	18	230/290	[15]
130	SiGe 130	Single/Differential	3	7.7	24.3	20	250/300	[16]
160-170	SiGe 130	Single	5	0 at 165	15 at 165	-	270/340	[17]
150	CMOS 65	Single	3	6.3	8.2	27	180/280	[18]

f_T/f_{max} of 300/450 GHz is presented. The PA is based on a staggered tuning approach where individual or group of individual stages are tuned at offset frequencies to make the overall power transfer broadband. The small signal gain for this PA is between 14-17 dB over a bandwidth of 35 GHz (135-170) with reverse isolation lower than -40 dB. The measured saturated output power (P_{sat}) varies from 5-8 dBm and P_{1dB} varies from 1-6 dBm over the 135-170 GHz band. The nominal dc power consumption for this PA is 320 mW and the peak PAE is 1.6% at 145 GHz. Table 1 compares the result of this work with state of the art silicon PAs operating in similar frequency range. To our best knowledge, this is the highest bandwidth reported for silicon PAs operating at 160 GHz.

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