An FM Demodulator Operating Across 2-10GHz IF

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***Abstract*— An FM demodulator operating across 8GHz IF bandwidth for application in low-power, wideband heterodyne receivers is presented. A 4-stage ring oscillator is frequency modulated by a wideband input. Locking to 1/4th the input frequency, it divides the FM deviation by four, thereby reducing the energy required for wideband demodulation to 0.75nJ/bit. Autocorrelation of the quadrature-phased outputs using a new low-power folded CMOS mixer is capable of detecting FM up to 400Mb/s over 2–10GHz IF. The inductorless 65nm CMOS prototype circuit occupies 0.17mm^2 and dissipates 3mW from 1.2V.**

***Index Terms*— FM demodulator, injection locking, auto-correlation, FM deviation, low-power, wideband.**

I. INTRODUCTION

Portable receivers for low-cost, high-speed data links should be compact, fully-integrated and consume minimal DC power. Simple modulation schemes, such as wideband FSK, are currently of interest for wireless local- and personal-area communication, where low-complexity receivers capable of robust data transfers at rates up to 1Gbit/s are required [1]. Down-conversion and demodulation of Gbit/s data streams at baseband has proven difficult with conventional circuit techniques within a reasonable power constraint [2],[3]. Demodulation at IF, using a heterodyne approach, simplifies the implementation of a wideband receiver, thereby saving power and chip area. Low-complexity FM receivers [1], (simplified block-diagram in Fig. 1a) are efficient and compact when processing data rates on the order of 100kbits/s. However, their wideband performance for data rates approaching 1Gbit/s is limited, as the power consumption increases in proportion to the increase in data rate.

In this work, a wideband, low power FM demodulator based on injection locking is demonstrated that operates across 2-10GHz ($\Delta f/fc$=1.4), while consuming 0.75nJ/bit at 4Mbps data rate. Simulations predict that the circuit is capable of demodulating data at rates up to 400Mb/s (i.e., 7.5pJ/bit). Experimental verification to date is limited to 4Mbps by the signal source bandwidth available for characterization. The total power consumption of the demodulator is 3mW from a 1.2V supply. A block diagram of the demodulator is shown in Fig. 1b and is discussed in detail in Section II. This integrated frequency/phase demodulator is capable of operating over a fractional bandwidth $\Delta f/fc$ greater than one, and is the first IC demonstration of division of FM deviation, and of a multi-GHz-IF low-power demodulator.

Section II is a discussion on division of the FM deviation and subsequent demodulation, section III deals with design aspects of the circuit blocks, and measurement results are presented in Section IV. Section V is a summary of the work.

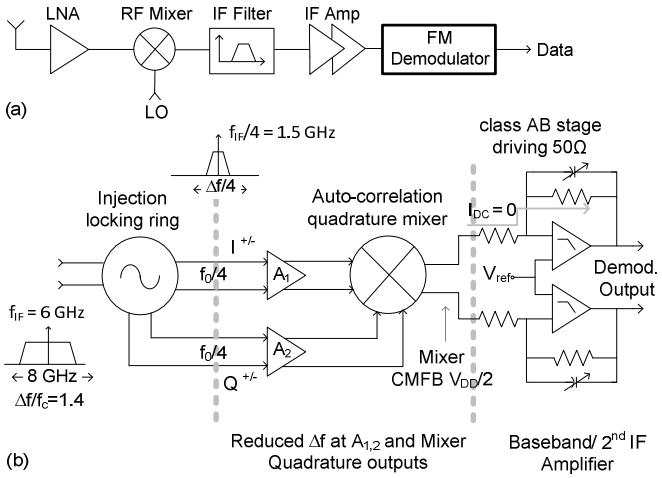


Figure 1: (a) Heterodyne receiver with demodulation at IF [1], (b) the presented wideband injection-locking IF demodulator.

II. LOCKED-IN DEVIATION DIVISION & FM DEMODULATION

Ring oscillators perform frequency division when injection locked. Multiphase injection is known to widen the locking range of these dividers, while 4-stage oscillators requiring anti-phased signals fit seamlessly into differential circuit chains. Inherently compact inductorless implementations are widely used for quadrature-phased LO division, and can even operate over two frequency octaves in the low GHz region [4]. When driven by a wideband FM signal, an injection-locked oscillator behaves like an adaptive filter, tracking the frequency having maximum power. The remarkable ability of these circuits to lock to FM signals and divide the input signal bandwidth has remained an unexplored circuit technique for wideband demodulation.

Injection locking creates a bandpass filter for signal and noise, and can work at input SNR values approaching ~0dB. An analytical treatment of noise in injection-locked FM receivers is presented in [5]. It is important to note that while the locked oscillator reduces FM deviation by virtue of division, the modulation frequency remains unaltered [5]. The operating bandwidth is reduced by the division factor (of 4 here), which appreciably eases the bandwidth/power consumption trade-off in following stages. Quadrature phases inherent in the ring topology can be multiplied, and subsequently low-pass filtered, to perform demodulation based on autocorrelation. This avoids the need for wideband phase shifters and complex frequency plans for I/Q generation.

The benefits of this approach to demodulation are: insensitivity to noise (since noise is uncorrelated), wideband operation, non-susceptibility to AM, and it does not impose a harmonic distortion requirement on the preceding IF amplifier.

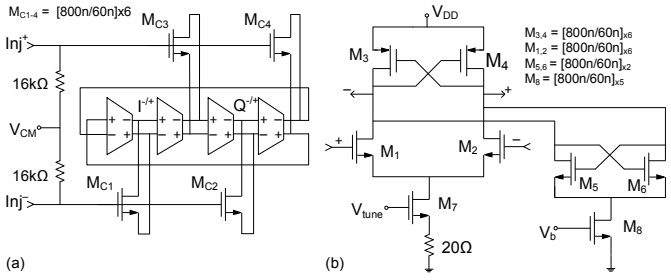


Figure 2: (a) Injection-locked four-stage ring oscillator, and (b) implementation of each stage.

However, the high input drive required for injection locking and its susceptibility to interferers must be addressed. Both these problems are alleviated by applying the technique at IF rather than RF, where potential blockers can be filtered by the preceding stages. The design of the wideband IF amplifier is necessary for signal gain, while the impact of interferers is considerably reduced by the directivity of mm-wave antennas.

A block diagram of the proposed IF demodulator for heterodyne receiver applications is shown in Fig. 1b. Quadrature outputs from the injection-locked input stage are interfaced through buffers $A_{1,2}$ to the autocorrelation mixer. The power consumption of the interface buffers and mixer are reduced considerably by the rail-to-rail output provided by the ring oscillator, and reduction of the input bandwidth by FM division (shown in fig. 1b). The low-frequency demodulated output from the mixer is buffered for 50Ω measurement using class-AB operational amplifiers in shunt feedback. The ratio of the feedback and input resistances sets the voltage gain to 6, while the common-mode output of the mixer and amplifier is set to $V_{DD}/2$ using V_{ref}, thereby ensuring DC isolation.

III. CIRCUIT DESIGN AND PERFORMANCE OUTLINE

Circuit design aspects of the building blocks of the FM demodulator shown in Fig. 1b are discussed in this section.

A. 4-stage injection-locked ring oscillator

The four-stage divide-by-4 ring oscillator shown in Fig. 2a constitutes the input stage. It is differentially injection locked to the wideband input signal through gain stages M_{C1-4}. Each stage of the ring is a differential amplifier with a cross-coupled PMOS load as shown in Fig. 2b. The cross-coupled PMOS load provides local positive feedback and ensures that the outputs charge and discharge rapidly. The transistors are sized (values indicated in the figure) for: the operating frequency band, minimum power consumption and maximum locking range when operated from 1.2V. Cross-coupled NMOS transistors $M_{5,6}$ provide additional negative resistance in an event of startup failure, controlled by V_b. Coupling transistors M_{C1-4} across the output of each stage are sized for maximum gain to enlarge the locking range, and therefore mitigate the impact of V_b on the output frequency. Frequency tuning is implemented at the tail node, where M_7 is operated in triode as a variable resistor controlled by V_{tune}. The oscillator has a 67% tuning range from 900MHz to 1.8GHz. The ring oscillator draws between 350 to 500μA per stage, depending

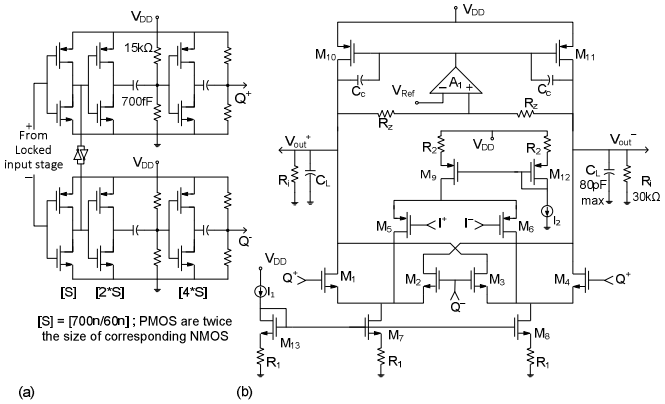


Figure 3: (a) Interface buffers $A_{1,2}$, (b) the folded CMOS autocorrelation mixer with a CMFB loop to set the output DC.

on V_{tune}. DC voltage V_{CM} ensures that transistors M_{C1-4} remain in saturation (with respect to the amplitude driving their gate) to provide maximum gain. Its optimal value cannot, however, be determined *a priori* and is therefore obtained iteratively. Frequency sensitivity is maximum at the oscillator's free-running f_0, but can also be controlled with V_{CM} [4]. In this work, all measurements are made with V_{CM} set to 0.6V. Adequate drive and bias at the input of M_{C1-4} further ensures that the oscillator does not fall out of lock, which would distort the demodulated waveform. The injection-locking stage was also characterized as a stand-alone IC in order to study its frequency response to wide-band signals. These data are presented and discussed in Section IV.

In an FM signal, the modulating frequency (f_m) is typically orders of magnitude below the carrier, and does not affect the frequency tracking ability of the locked-in ring oscillator. A data-rate (i.e., twice f_m) limitation is imposed by the assumption that the carrier is much higher than f_m for an autocorrelation demodulator, as shown analytically in [6]. Simulations suggest that the presented injection-locked demodulator can detect FM signals coherently when the carrier is 1 order of magnitude higher than the modulating signal. This limits the maximum data-rate to ~400Mbps at the 2GHz band edge, and > 1Gbit/s between 8 and 10GHz.

B. Folded CMOS mixer and interface & output amplifiers

The schematic of the new folded mixer topology is shown in Fig. 3b. Mixers operating from low supply voltages encounter headroom limitations, and the tail current is often sacrificed at the expense of bias regulation and common-mode performance. This mixer has complimentary transistors at its ports. The switching quad consists of M_{1-4}, while PMOS transistors $M_{5,6}$ form the RF port. The PMOS device widths are twice that of the NMOS quad transistors to ensure equal loading in the I and Q paths. I_2 determines the current in $M_{5,6}$, while I_1 sets their difference to be equally distributed between M_{1-4}. In this way, there is accurate control over the circuit's biasing. The simulated common-mode suppression from 0.5 to 2.5GHz (the intended band of operation, since the 2-10GHz IF input is divided by 4 by the ILO) varies from 40-50dB at either port. The mixer conversion gain is limited by the output impedance of tail current sources $M_{7,8,9}$, and a 75Ω

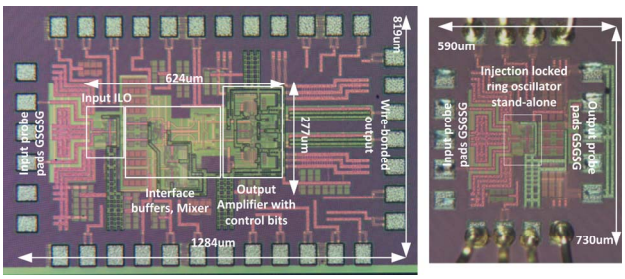
degeneration resistance is employed at each source node to increase their output impedances. The injection-locked stage provides rail-to-rail swing that allows the mixer to be designed for low power consumption. Measurements have been made with both I_1 and I_2 set to 150µA. The output is set to 0.6V-DC using common-mode feedback. The CMFB amplifier is a standard NMOS folded-cascode amplifier that consumes 30µA. Compensation capacitance C_c stabilizes the CMFB loop, for a maximum load capacitance of 80pF. The mixer load is set by the input resistor of the feedback network of the output stage (see Fig. 1), and is 30kΩ. The minimum current in transistors $M_{1\text{-}4}$ to ensure a stable CMFB loop is 25µA each.

Interface buffers $A_{1,2}$ between the oscillator output and the autocorrelation mixer are shown in Fig. 3a, along with device sizes. It consists of a 3-inverter fan-out. Cross-coupled inverters between the differential paths preserve inverse phases, while the output DC level is set by a resistive divider. The inter-stage network has a 40MHz high-pass characteristic and does not attenuate the propagating signal.

The output amplifiers provide low-pass filtering in addition to the mixer load and can be made integral to the process of demodulation. Class-AB operational amplifiers drive the 50Ω load efficiently. The amplifiers' quiescent current is 800µA.

IV. MEASUREMENT RESULTS AND DISCUSSION

The micrograph of the demodulator prototype implemented in 65nm CMOS is shown in Fig. 4a. The core area is 624×277µm^2. The chip was mounted on a custom test-board for measurement. All DC inputs are wire bonded, while the RF input and output probed on die. A micrograph of the input ring oscillator characterized stand-alone is shown in Fig. 4b.



(a) IF Demodulator 0.17mm^2 (b) Input stage only

Figure 4: Chip micrographs.

The spectrum of the free running oscillator at its band edges of 900MHz and 1.8GHz is shown in Fig. 5. The measured tuning range is 67% around 1.35GHz.

The 2-10GHz bandwidth has been measured in bands of 1GHz. National Instruments arbitrary-waveform generator cards to synthesize linearly-modulated analog FM signals of 1GHz bandwidth that drive off-chip up-conversion I/Q modulators to obtain a wideband signal at the desired carrier. The modulation frequency limit of the AWG is 100kHz to 2MHz, thereby limiting the validation to 4Mbps (note that the simulated data-rate limit of the circuit is 400Mbps).

Fig. 6 is a measurement validation of the concept, where

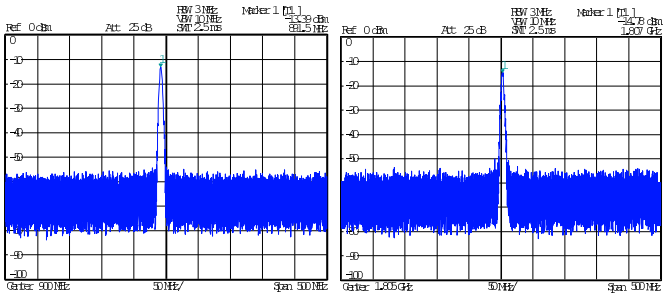


Figure 5: Frequency spectrum of the free-running oscillators at band edges – 900MHz to 1.8GHz. Tuning range equals 66.7%.

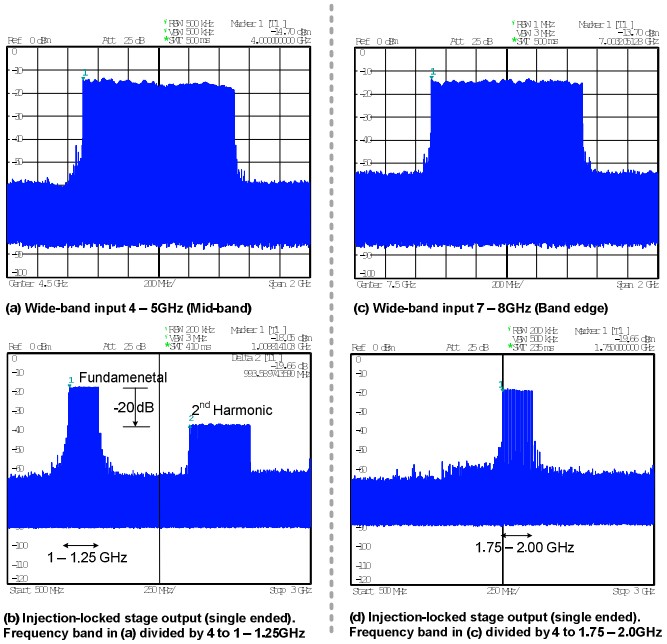


Figure 6: Division of the frequency spectrum at the middle and edge of the band. The 1GHz input signal is divided down by a factor of 4, while retaining the modulating frequency.

1GHz bandwidth signal applied to the input gets divided down by a factor of 4 to 250MHz. These are the frequency responses at mid-band (4-5GHz) and the edge of the band (7-8GHz). The output is single ended, however, in both cases the second harmonic suppression is ~20dB, which indicates that the oscillator is within its locking range. Locking limits are determined by the oscillator's f_0, and the amplitude driving trans-conductance stages $M_{C1\text{-}4}$.

Fig. 7 shows the measured locking performance of the 4-stage ring oscillator, with V_{CM} set to 0.6V. The gate-drive requirement measured at different frequencies is shown in Fig. 7a when the oscillator's f_0 is at band edges and mid-band. The 2-10GHz band coverage requires a 240m$V_{p\text{-}p}$ input drive when frequency tuning is performed. Locking range measured for different input amplitudes at f_0 of 1.5GHz (6GHz/4) is shown in Fig. 7b. At ~400m$V_{p\text{-}p}$ input, the entire 2-10GHz band can be divided down to 0.5–2.5GHz, without changing either V_{CM} or the oscillator's center frequency, and subsequently demodulated by the low power mixer.

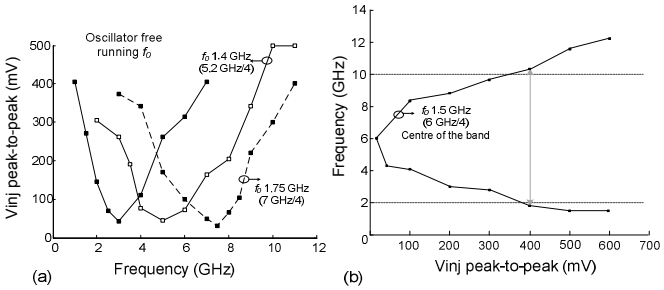


Figure 7: (a) $V_{p\text{-}p}$ input for locking at different frequencies (b) locking frequency range for different input $V_{p\text{-}p}$.

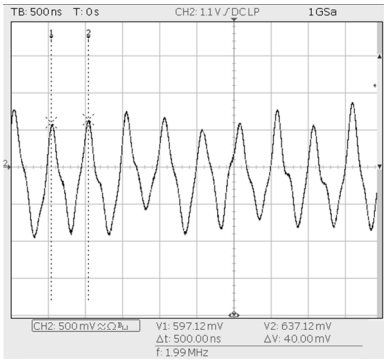


Figure 8: Demodulated 2MHz triangular wave for 7-8GHz input.

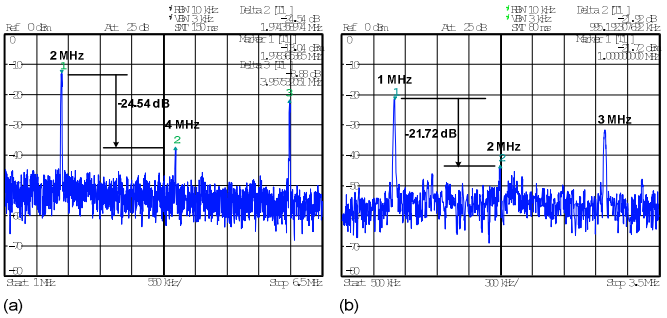


Figure 9: Demodulated output spectrum (a) 7-8GHz input modulated by 2MHz triangular signal, (b) 2-3GHz with 1MHz modulation.

The demodulated output is shown in Fig. 8. The input RF band in this case is at 7–8GHz, V_{CM} is 0.6V and f_0 is 1.5GHz. The modulating signal was set to 2MHz (a limitation of the wideband generator), and a triangular wave is used to obtain a flat RF power spectrum. The demodulated waveform is a 2MHz triangular wave, with the second-harmonic component suppressed by ~24dB, as seen from Fig. 9a. The peak-to-peak swing is ~1V. Fig. 9b shows, the demodulated output for the low-band case of 2–3GHz and a f_m of 1MHz. Note that the output power at frequencies lower than 10MHz is attenuated by AC coupling at the spectrum analyzer input.

Table I summarizes the performance of recently reported FM/FSK receivers and dedicated IF demodulators [7], [8], [9]. The comparison is restricted to measured values (constrained by test equipment limitations), though data rates in excess of 400Mb/s have been simulated. The developed low-power IF demodulator in 65nm CMOS achieves excellent wideband performance, operating at a fractional bandwidth of 1.4 while dissipating just 3mW from 1.2V.

TABLE I Comparison with recent publications

	Tech.	Mod.	Bandwidth (GHz) [$\Delta f/f_0$]	Data Rate (Mb/s)	P_{diss} (μW)	Energy per bit (nJ)
[7]	0.13um CMOS	FM/ FSK	19.2-21.8 [0.08]	1500	7200*	0.0048
[8]	65nm CMOS	FSK	4 – 5 [0.22]	0.100	2200	2.2
[9]	90nm CMOS	FSK	0.9– 0.928 [0.028]	5	380	0.076
This work	65nm CMOS	Analog FM	2 – 10 [1.34]	4	3000	0.75
*demodulator core power dissipation						

V. CONCLUSION

An FM demodulator is presented in which a 4-stage ring oscillator is frequency modulated by a wideband input, locking it to 1/4th the input frequency. The locked-in oscillator reduces the FM deviation by a factor of 4, and provides quadrature outputs to the folded CMOS autocorrelation mixer, for coherent FM demodulation. This is the first IC demonstration of a multi-GHz-IF low-power demodulator for wideband heterodyne receivers. A stand-alone IC prototype in 65nm CMOS verifies the wideband locking behavior of the 4-stage ring oscillator along with division of FM deviation. Measurements at 4Mbit/s data rate demonstrates demodulator operation from 2-10GHz, i.e., a fractional bandwidth of 1.34, at 0.75nJ/bit.

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