

V-Band Dual-Conversion Down-Converter With Low-Doped N-Well Schottky Diode in 0.18 μm CMOS Process

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Abstract — In this paper, a V-band dual-conversion down-converter with a silicon-based Schottky diode using low-doped N-well for DC and RF characteristics optimization is demonstrated in standard 0.18 μm CMOS technology. A triple-balanced subharmonic Schottky diode microwave mixer and a double-balanced resistive analog mixer are employed as the first conversion mixer and the second conversion mixer, respectively. As a result, the conversion gain is about -1 dB in the range of 45~64 GHz. The noise figure is about 20 dB, IP_{1dB} is about -5 dBm and IIP3 is about 5 dBm. The total power consumption is 92.4 mW at 2.5 V supply voltage.

Index Terms — Schottky diode, dual-conversion, down-converter, subharmonic mixer.

I. INTRODUCTION

Millimeter-wave transceivers have been widely developed due to the unlicensed band around 60 GHz. Nowadays, a millimeter-wave transceiver is usually demonstrated in the advanced CMOS technologies [1]-[3] and the expensive research and development cost of the advanced CMOS process prevents the 60 GHz transceiver from entering the commercial market. In 2005, K. K. O. et al [4] employed Schottky diodes to implement millimeter wave detectors in the low-cost 0.18 μm CMOS process [5]. A Silicon-based Schottky diode has cut-off frequency of several hundred GHz and thus opens up a new scenario for applying low-cost CMOS process to millimeter-wave applications [6].

This paper demonstrates a V-band dual-conversion down-converter with low-doped N-well Schottky diode in standard 0.18 μm CMOS process. The threshold voltage adjustment optional mask which blocks the n-implant to form a medium threshold voltage PMOS is used to form the low-doped N-well Schottky diode. The resulting low-doped N-type Schottky diode possesses a good ideality factor and small leakage current; the high cut-off frequency and low turn-on voltage of a silicon Schottky diode device result in the diode mixer with low conversion loss and low LO pumping power.

The V-band dual-conversion subharmonic down-converter can be established using anti-parallel Schottky diode pairs. In this paper, the low-doped N-well Schottky diode technology is discussed in detail. A triple-balanced configuration is employed to improve the isolation of the subharmonic diode mixer.

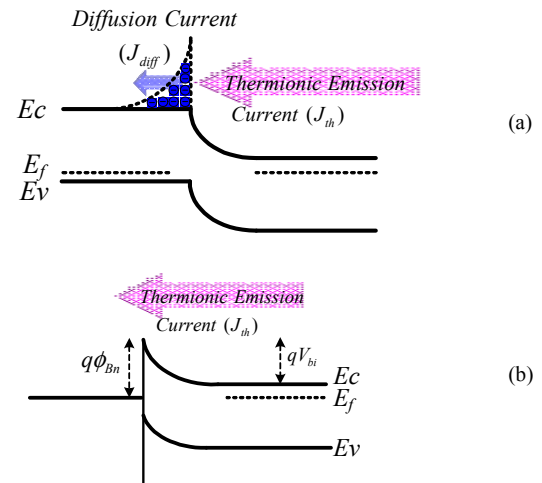


Fig. 1. Current transport mechanism and charge storage effect in PN junction and Schottky diodes (a) p⁺n junction diode and (b) N-type Schottky diode.

$$J_{th} = \frac{4\pi q m^* k^2}{h^3} T^2 e^{-\frac{q\phi_{Bn}}{kT}} \left(e^{\frac{qV}{kT}} - 1 \right) \quad (1)$$

$$= q \frac{v_{th}}{4} \left(N_D e^{-\frac{qV_{bi}}{kT}} \right) \left(e^{\frac{qV}{kT}} - 1 \right)$$

$$J_{diff} = \left(\frac{q D_n n_i^2}{L_n N_A} \right) \left(e^{\frac{qV}{kT}} - 1 \right)$$

$$\left\{ \frac{J_{th}}{J_{diff}} = \frac{q \frac{v_{th}}{4} \left(N_D e^{-\frac{qV_{bi}}{kT}} \right)}{\frac{q D_n n_i^2}{L_n N_A}} = \frac{v_{th}}{4} \frac{L_n}{\tau_n} \right.$$

Typical case :

$$v_{th} = 10^7 \text{ cm / s,}$$

$$L_n = 10^{-4} \text{ cm, } \tau_n = 10^{-6} \text{ s}$$

$$J_{th} \sim 10^5 J_{diff}$$

II. SILICON SCHOTTKY DIODE IN FOUNDRY CMOS PROCESS

The band diagrams of a p^+n junction and a metal-n Schottky junction with the same doping density in n-type region are shown in Fig. 1(a) and Fig. 1(b), respectively. Apparently, a Schottky diode is different from a pn junction at two aspects. A Schottky diode has no minority carrier storage effect and thus possesses a much higher frequency response [4][5]. The current transport mechanism of a Schottky diode is dominant by the thermionic current while the current transport mechanism in a pn junction is dominant by the diffusion current. The thermionic current is much larger than the diffusion current as shown in equation (1). Thus, the turn-on voltage of a Schottky diode is lower than that of a p^+n junction and a Schottky diode with low turn-on voltage facilitates the LO power design. No extra photo mask is needed to form the Schottky diode. In the 0.18- μm CMOS, two types of metal-n Schottky diodes can be formed because an optional mask blocks PMOS threshold voltage adjustment implant in the n well region. The measured I-V curves are shown in Fig. 2(a). The doping densities are obtained from the C-V measurement data by plotting $1/C^2$ -V curve as shown in Fig. 2(b). The doping density corresponding to the medium PMOS is on the order of $2 \times 10^{17} \text{ cm}^{-3}$ while that corresponding to the nominal PMOS is on the order of $2 \times 10^{18} \text{ cm}^{-3}$. The Schottky diode with the lower doping density has less reverse leakage current, good ideal factor and is employed in this paper.

III. 60 GHz DUAL-CONVERSION DOWN-CONVERTER WITH TRIPLE-BALANCED SCHOTTKY DIODE MIXER

A V-band dual-conversion down-converter is composed of a triple-balanced subharmonic diode mixer, IF_1 low-noise buffer, double-balanced resistive mixers and shunt-shunt feedback wideband IF_2 amplifiers as shown in Fig. 3. The V-band dual-conversion down-converter uses a triple-balanced diode mixer as the first conversion mixer. Following the diode mixer, an IF_1 low noise buffer is employed to suppress the noise figure from the subsequent second conversion resistive mixer. The IF_1 is set to be 10 GHz. The selection of IF_1 frequency is a trade-off between the image rejection and noise figure. Then, a double-balanced resistive mixer down-converts 10 GHz (IF_1) signal to 1 GHz bandwidth baseband signal (IF_2). The 1 GHz baseband bandwidth corresponds to 2 GHz RF channel bandwidth. Following the resistive mixer, shunt-shunt feedback wideband amplifiers are realized as IF_2 buffer amplifiers to compensate the resistive mixer loss. Moreover, precise quadrature output signals are obtained by using a two-stage polyphase filter at the LO port of the second stage resistive mixer.

The combination of the triple-balanced and anti-parallel configurations makes the subharmonic Schottky diode mixer with good isolation for each port. The triple-balanced Schottky diode mixer uses Marchand balun at RF input port to create differential input signals and trifilar transformer at LO_1 port to create a pair of differential signals to the anti-parallel diode pairs. Moreover, the IF differential output signals are taken from the center tap of the trifilar transformer. To obtain wider bandwidth and precisely balanced signal, the Marchand balun and trifilar transformer are based on slotted bottom metal to improve return loss and shield lossy substrate. Furthermore, the low-doped N-well Schottky diodes are placed at the center of trifilar transformer to reduce layout complexity.

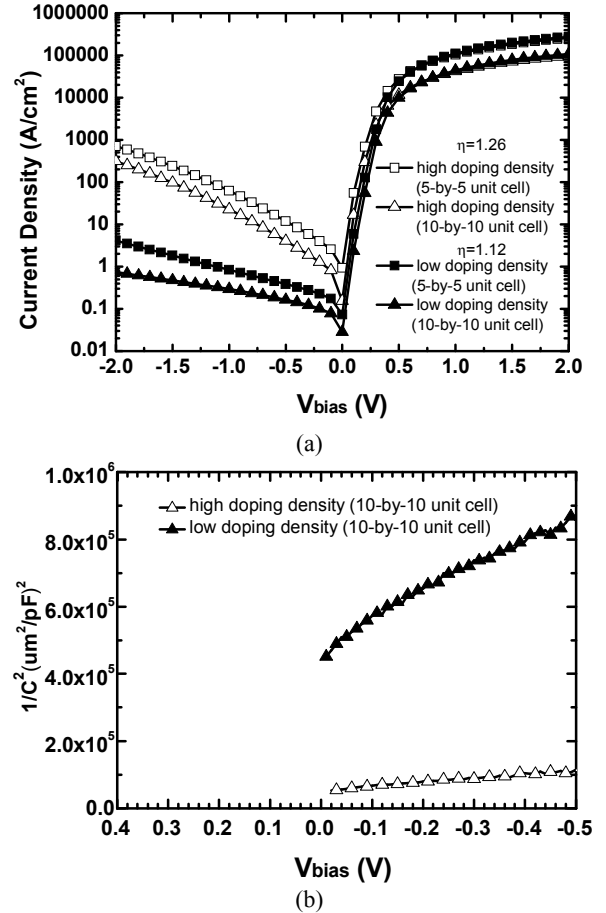


Fig. 2. Comparisons of the measured (a) I-V and (b) $1/C^2$ -V curves for the Schottky diodes with/without the optional mask in 0.18- μm foundry CMOS technology.

A 10 GHz differential low-noise buffer consisting of two common-source amplifiers (M_1 , M_2 , M_3 , and M_4) is placed between the microwave diode mixer and the analog resistive mixer. The source degenerated inductors, interstage matching inductor and RF chokes are entwined

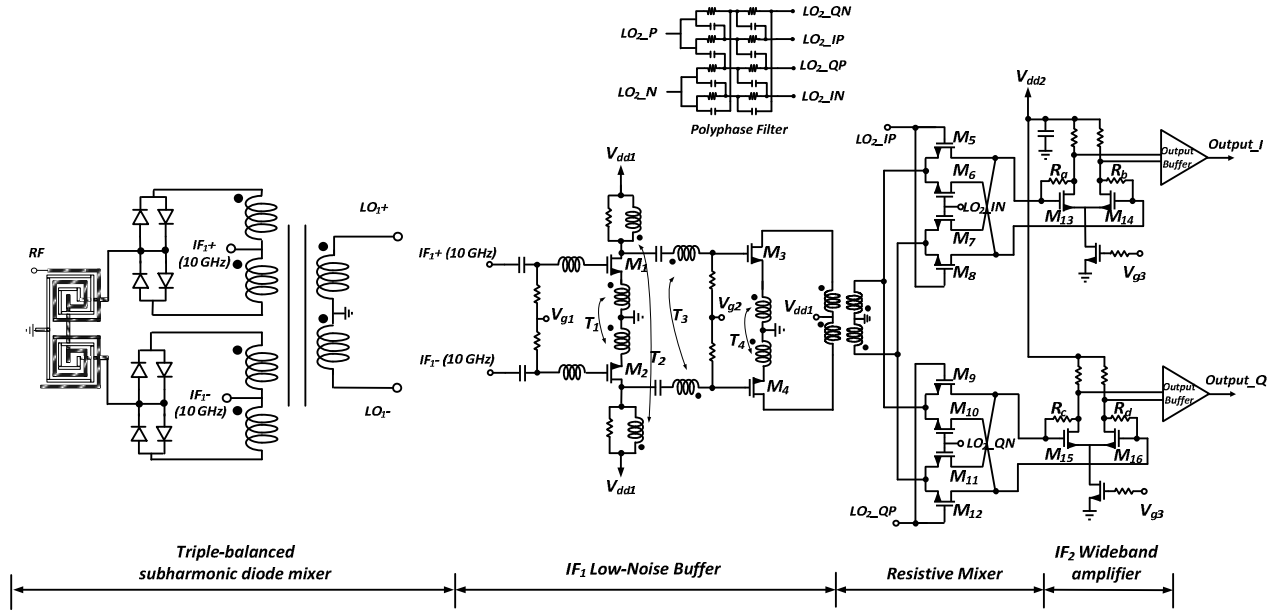


Fig. 3. Schematic of a V-band dual-conversion down-converter with triple-balanced subharmonic Schottky diode mixer.

as transformers (T_1 , T_2 , T_3 , and T_4) to reduce chip area. The second down-conversion double-balanced resistive mixer (M_5 , M_6 , M_7 , M_8 , M_9 , M_{10} , M_{11} , and M_{12}) has a two-stage polyphase filter to create precise quadrature signals. Finally, IF_2 wideband differential amplifiers (M_{13} , M_{14} , M_{15} , and M_{16}) with 3-K Ohm shunt-shunt feedback resistors (R_a , R_b , R_c , and R_d) are employed as transimpedance amplifiers.

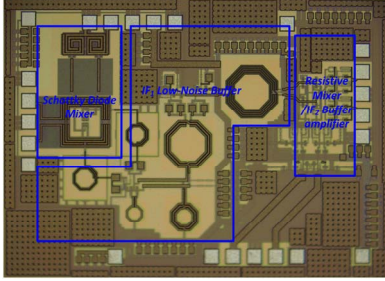


Fig. 4. Die photo of the V-band dual-conversion down-converter.

IV. MEASUREMENT RESULTS

The total power consumption is 92.4 mW at 2.5 V supply voltage and the die size is $1.8 \times 1.3 \text{ mm}^2$ as shown in Fig. 4. Due to the low-doped n-type Schottky diode, the LO_1 pumping power only requires 6-dBm to achieve fully switching and achieves -1-dB conversion gain as shown in Fig. 5. The conversion gain is around -1-dB in the frequency range of 45~64 GHz when the IF is fixed at 0.5 GHz. Moreover, the IP_{1dB} is about -5 dBm, IIP3 is about 5 dBm and noise figure is about 20 dB as shown in Fig. 6. The IF 3-dB bandwidth is 1.5-GHz as shown in Fig. 7, and noise figure with respect to the IF frequency is around 20 dB as shown in Fig. 8. Due to the triple-balanced configuration of diode mixer, the LO_1 -to-RF isolation is better than 20 dB and $2LO_1$ -to-RF isolation is

better than 50 dB in the LO_1 frequency range, respectively, as shown in Fig. 9. Finally, a poly-phase filter creates precise output quadrature signal waveforms as shown in Fig. 10.

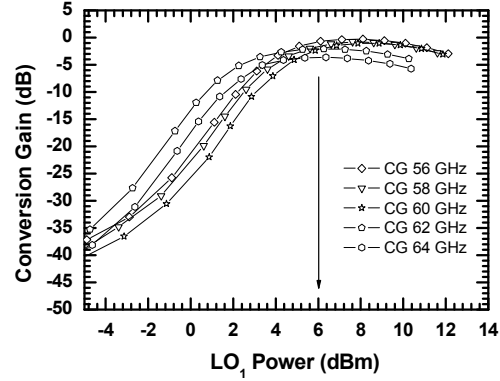


Fig. 5. Conversion gain with respect to LO_1 power when $IF_1 = 0.5$ GHz.

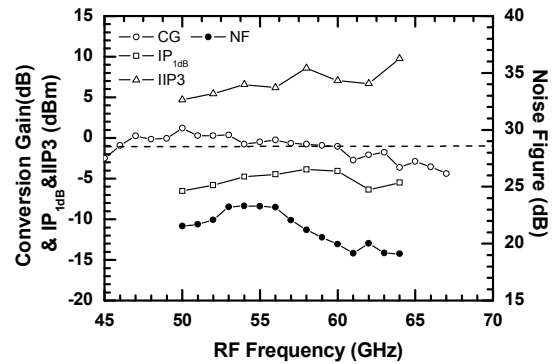


Fig. 6. Conversion gain, IP_{1dB} , IIP3 and noise figure with respect to RF frequency when LO_1 power = 6 dBm and $IF_1 = 0.5$ GHz.

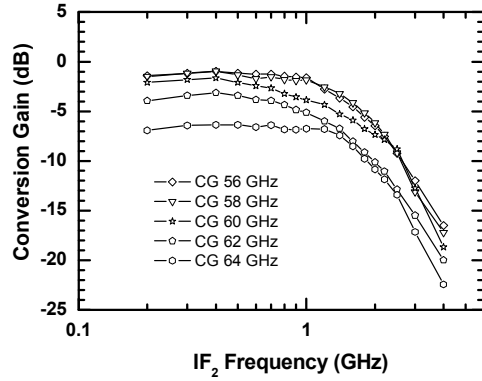


Fig. 7. Conversion gain with respect to IF_2 frequency when LO_1 power= 6 dBm.

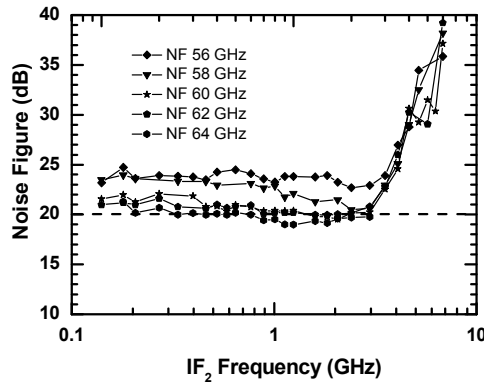


Fig. 8. Noise Figure with respect to IF_2 frequency when LO_1 power= 6 dBm.

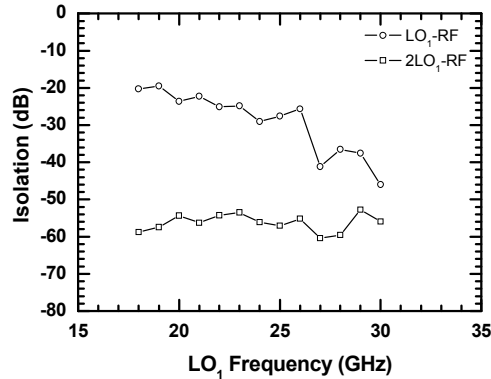


Fig. 9. Isolation with respect to LO_1 frequency of the V-band dual-conversion down-converter.

V. CONCLUSION

In this paper, a low-doped N-well Schottky diode has been used to realize a V-band dual-conversion down-converter in low-cost 0.18- μ m CMOS technology. The measured result shows LO_1 pumping power only requires

6-dBm to achieve fully switching and achieves -1-dB conversion gain and 20-dB noise figure. The N-type Schottky diode with low doping density is suitable to realize 60 GHz down-converter.

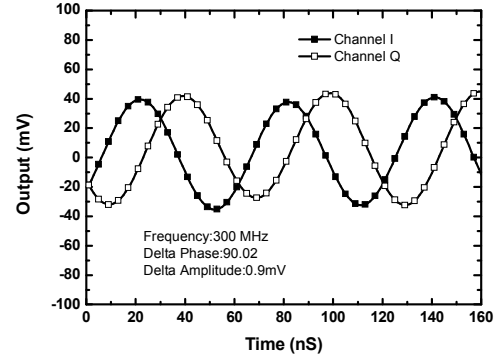


Fig. 10. Output waveform of the V-band dual-conversion down-converter.

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REFERENCES

- [1] C. H. Doan, S. Emami, A. M. Niknejad, and R. W. Brodersen, "Millimeter-wave CMOS design," *IEEE J. Solid-State Circuits*, vol. 40, no. 1, pp. 144-155, Jan. 2005.
- [2] S. K. Reynolds, B. A. Floyd, U. R. Pfeiffer, T. Beukema, J. Grzyb, C. Haymes, B. Gaucher, and M. Soyuer, "A silicon 60-GHz receiver and transmitter chipset for broadband communications," *IEEE J. Solid-State Circuits*, vol. 41, no.12, pp. 2820-2831, Dec. 2006.
- [3] S. Emami, R. F. Wiser, E. Ali, M. G. Forbes, M. Q. Fordon, X. Guan, S. Lo, P. T. McElwee, J. Parker, J. R. Tani, J. M. Gilbert, and C. H. Doan, "A 60-GHz CMOS phase-array transceiver pair for multi-Gb/s wireless communications," *IEEE ISSCC Dig. Tech. Papers*, pp.164-166, Feb. 2011.
- [4] S. Sankaran, and K. K. O, "Schottky barrier diodes for millimeter-wave detection in a foundry CMOS process," *IEEE Electron Device Lett.*, vol. 26, no. 7, pp 492-494, Jul. 2005.
- [5] S. Sankaran and K. K. O., " Schottky diode with cut-off frequency of 400 GHz fabricated in 0.18 μ m CMOS. " *IEE Electron. Lett.*, vol. 41, no. 8, pp. 506-508, Apr. 2005.
- [6] H.-J. Wei, C. C. Meng, T.-W. Wang, T.-L. Lo, and C.-L. Wang, " 60-GHz dual-conversion down/up- converters using Schottky diode in 0.18 μ m foundry CMOS technology," *IEEE Trans. Microw. Theory Tech.*, vol. 60, no. 6, pp. 1684-1698, June 2012.