A Ka-Band Doherty Power Amplifier with 25.1 dBm Output Power, 38% Peak PAE and 27% Back-Off PAE

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Abstract — We present the design and development of the first fully integrated, two stage Doherty power amplifier (DPA) in the Ka-Band. The DPA is fabricated in a 0.15-µm GaAs pseudomorphic high electron mobility transistor (pHEMT) process. At 26.4 GHz, the amplifier achieves measured small signal gain of 10.3 dB, output power at 1-dB compression point (P_{1dB}) of 25.1 dBm, peak power added efficiency (PAE) of 38%, and PAE of 27% at 6 dB back-off power. To the best of the author's knowledge, this Doherty circuit is the first fully integrated millimeter-wave amplifier that achieves the highest power and a recorded 27% PAE at 6-dB back-off and each unit amplifier has 2 stages.

Index Terms — Millimeter wave integrated circuits, Power amplifiers, Gallium arsenide, Millimeter wave devices, MIMICs.

I. Introduction

The demand for mobile data has seen tremendous growth in recent years. As this demand grows, the spectrum in use for mobile data traffic (i.e., below 6 GHz) is becoming increasingly crowded. The current 4G systems including the long-term evolution (LTE) that uses advanced technologies such as Orthogonal Frequency Division Multiplex, Multiple Input Multiple Output, etc. are reaching theoretical limits in terms of bit-per-second/Hz/cell. The limited capacity of this spectrum as well as the potential for higher data rates has generated interest among many companies and research institutions to develop mobile broadband systems beyond X-band into the millimeter-wave (mm-wave) spectrum (i.e., the 14-300 GHz spectrum) [1].

Beamforming is a key technology for millimeter-wave mobile broadband transceivers and reduces the peak power requirements. However, the low efficiency of mm-wave power amplifiers remains the main challenge. Commercially available PA's at mm-wave frequencies exhibit around 5% to 10% PAE at 6-dB back-off power [2]-[3]. Deploying hundreds of these amplifiers in a transmitting beamforming system create major thermal management issues. Likewise, at the mobile device level, the 5% to 10% PAE at 6-dB back-off power is quite low for battery operation.

A Doherty amplifier is a popular architecture to maintain high efficiency at 6-dB back-off power for wireless applications below 6 GHz [4]. Several DPA's have been reported in the mm-wave regime but have low power, low efficiency and a single-stage unit cell amplifier (except for [5] which employs 5 cascode stages). [5]-[8] have reported multiple DPAs built in CMOS, SOI and GaAs operating in mm-wave frequencies up to 76 GHz. The highest efficiency at 6-dB back off is limited to 17% without linearization technique [8], and 23% using post-distortion linearization [7]. In addition, the highest power was the GaAs HEMT DPA that has saturated power of 21.8 dBm [8].

In this paper, we present the design and development of a fully integrated Doherty power amplifier in the Ka-Band, fabricated in a 0.15-μm GaAs pHEMT process. An identical unit cell amplifier is used as the main and peaking amplifiers, and this unit cell amplifier was also fabricated as a standalone block to highlight the efficiency improvement of the DPA. An on-chip asymmetric Wilkinson power divider is used at the input and an on-chip tee junction, a $\lambda/4$ inverter, and an offset line are implemented at the output. The proposed Ka-band Doherty power amplifier achieves measured P_{1dB} of 25.1 dBm and PAE of 27% at 6-dB back-off power. To the best of the author's knowledge, this fully integrated Ka-Band Doherty amplifier achieves the highest PAE at 6-dB power back-off compared to reported millimeter wave PAs.

II. Circuit Design

The DPA has a "main" or "carrier" amplifier arranged in a power combining configuration with the "peaking" or "auxiliary" amplifier The main amplifier is ideally biased in class B for a load Z_L and the auxiliary is biased in class C with both amplifiers delivering the same peak power. The main amplifier is always on and the auxiliary amplifier turns on when the input power reaches a certain level. The varying signal level of the auxiliary amplifier and the $\lambda/4$ inverter allow the main amplifier to see a load from Z_L to $2Z_L$ from the total peak power till the auxiliary PA is off, respectively. Hence, the Doherty amplifier can ideally maintain the same peak efficiency at a certain back-off power.

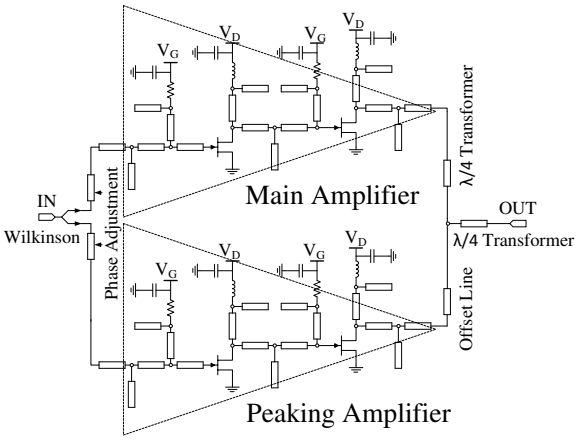

Fig. 1. Schematic diagram of the millimeter-wave Doherty architecture.

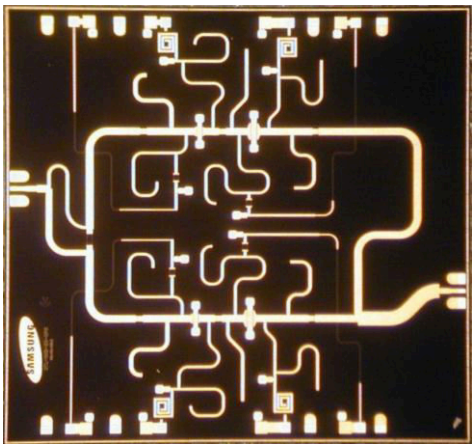

Fig. 2. Chip photograph of Doherty power amplifier. Chip size is 5 mm x 5 mm.

The DPA presented here accomplishes this active load modulation using identical unit cell amplifiers as the main and peaking amplifiers. The unit cell amplifier is a two stage amplifier. In the main amplifier, the driver stage is biased in class AB and the power stage is biased in class C. This is the same bias condition used to test the unit cell PA as a standalone block. The peaking amplifier is biased in a class C configuration, with the gate voltage tuned to a specific value so that the amplifier will turn on at 6 dB back-off power. Through the use of quarter-wave transformers and the added current of the peaking amplifier, the load at the output of the main amplifier is successfully modulated over a 6 dB output power range, keeping it in a compressed, high efficiency state over the range. A 50 Ω characteristic impedance transmission line is used at the output of the peaking amplifier to transform the output impedance to a high value when the amplifier is off. This prevents power leakage from the main amplifier in low power operation. The remaining transmission lines on the input are designed to match the phase of the main and peaking amplifiers at the output, to ensure the output signals add constructively. A 90 degree hybrid coupler is traditionally used in the Doherty architecture, however, the 90 degree shift is not strictly necessary for Doherty operation. Through simulation we found that the relative phase differences between the main and peaking amplifiers were more easily matched with a Wilkinson splitter. The input Wilkinson splitter was designed to asymmetrically split the power between the main and peaking amplifier, with more power being delivered to the peaking amplifier to allow it to fully turn on and modulate the load seen by the main amplifier to 50 Ω. A chip photograph of the DPA is shown in Figure 2.

The unit cell amplifier used in the Doherty architecture as the main is a two stage design that consists of a class AB driver stage and a class B power stage. The power stage device gate periphery was selected based on nonlinear load-pull simulations and sample data from the foundry to provide the desired output power and efficiency. The driver stage device gate periphery was selected to provide an adequate power margin so that it does not compress before driving the power stage into compression. The power and driver stage device peripheries were selected as 600 μm and 300 μm, respectively. The auxiliary amplifier has 2 stages with similar design to the main one but is biased in class C.

The power amplifier design used open microstrip stubs and shorted microstrip stubs (realized through quarter-wave chokes) for all matching networks. In 0.15-μm GaAs pHEMT processes, stability can be a major issue due to the large gain at low frequencies. A multiband reject filter was designed and implemented in the DC path using spiral inductors on the drain and series resistors on the gate as well as bypass MIM capacitors to ensure stable operation for all frequencies. All passive structures were simulated using Momentum electromagnetic simulator software [9]. The complete PA non-linear simulation was done using Agilent Advanced Design Systems.

III. Measured Results

Both the DPA and the unit cell power amplifier were measured using on-wafer probing and on-die TRL calibration. The DPA bias conditions were tuned for optimal performance and we report the measured results for two different bias conditions. In the "Bias A" condition, the two stages of the main amplifier were biased at a drain voltage of 6 V and 5 V in the driver stage

and power stage, respectively, and drain currents of 17 mA and 10 mA in the driver stage and power stage, respectively. This is the deep class AB and class B biasing discussed previously and is the same biasing configuration used in testing the individual unit cell power amplifier. The two stage peaking amplifier was biased at a drain voltage of 6.7 V and 6.6 V in the driver and power stage, respectively, and the gate voltage of each stage was tuned to -1.45 V to control the power level at which the peaking amplifier turns on. The higher drain voltage in the peaking amplifier allows it to fully turn on and modulate the load at high output powers. Fig. 3 demonstrates the measured PAE, gain and output power using the Bias A condition.

In the "Bias B" condition, all drain voltages were set to 5 V and the drain currents of the main amplifier were 14 mA and 10 mA in the driver stage and power stage, respectively. The gate of each stage in the peaking amplifier was set to -1.2 V. Fig. 4 demonstrates the measured PAE, gain and output power using the Bias B condition.

In the Bias B condition, the DPA achieves an OP_{1dB} better than 25 dBm from 26 to 26.4 GHz. Over the same frequency band, the peak PAE is 37-38%, and the PAE at 6 dB back-off ranges from 23% to 27%. The peak performance of the DPA is at 26.4 GHz, with an OP_{1dB} of 25.1 dBm, a peak PAE of 38%, and a PAE at 6 dB back-off of 27%. A plot of the measured S-parameters is shown in Figure 5 for the Bias B condition.

Figure 6 shows a plot of the PAE of the unit cell amplifier and the DPA as a function of back-off power (from OP_{1dB}) for both bias conditions. It can be seen that in comparison to the unit cell, the DPA achieves a slightly lower maximum PAE because the load is not fully modulated to the ideal 50 Ω as in the unit cell PA. However, it improves the PAE at 6 dB back-off by 8%. The efficiency improvement is consistent throughout the entire 6 dB power range.

Figure 7 shows a plot of the drain current as a function of input power for the main amplifier and the peaking amplifier for both bias conditions. This helps to illustrate when the peaking amplifier begins to turn on and modulate the load of the main amplifier. It is apparent from the plot that the peaking amplifier begins to turn on at an input power of ~13 dBm (Bias A). From Figure 3, we observe that this is the same power level where the PAE begins to increase again due to the load modulation effect of the peaking amplifier. We also observe from Figures 3 and 7 that the DPA has reached output power saturation at an input power of 16 dBm, before the peaking amplifier is fully turned on and operating at the same drain current as the main amplifier. As the input power is increased from 16 dBm and the drain current in the peaking amplifier increases, there is very little increase in the output power of the DPA. This behavior suggests that the main amplifier and peaking amplifier outputs may have a phase mismatch problem at high power which causes them to add somewhat destructively at the tee junction. This can be easily resolved by adjusting the lengths of the transmission lines on the inputs, and could increase the OP_{1dB} and extend the power range over which the amplifier operates with high efficiency.

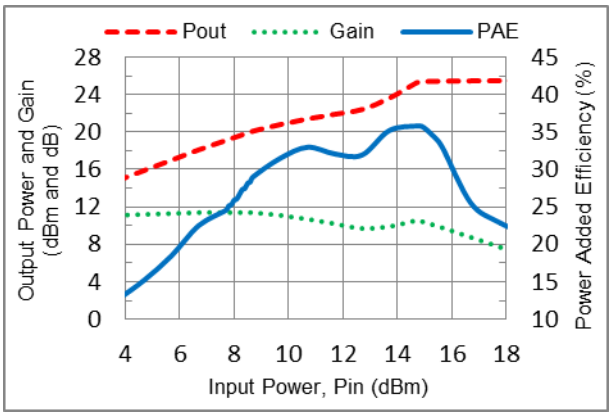

Fig. 3. Measured PAE, gain and output power of DPA at 26.4 GHz. Bias A: Vd_{1main} = 6V, Vd_{2main} = 5V, Vd_{1peak} = 6.7V, Vd_{2peak} = 6.6V, Id_{1main} = 17mA, Id_{2main} = 10mA, Vg_{peak} = -1.45V.

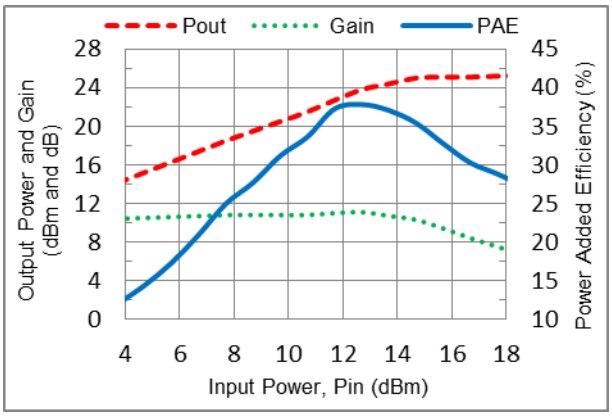

Fig. 4. Measured PAE, gain and output power of DPA at 26.4 GHz. Bias B: Vd = 5V, Id_{1main} = 14mA, Id_{2main} = 10 mA, Vg_{peak} = -1.2V.

IV. Conclusion

We demonstrate a fully integrated Doherty power amplifier for millimeter-wave mobile broadband systems. The DPA is designed in a 0.15-μm GaAs pHEMT process with the main and auxiliary amplifiers having 2 stages. Our DPA achieves a measured output power of 25.1 dBm.

Our experimental results demonstrate that the PAE at 6-dB back-off power is 27%, the highest reported to date for a power amplifier in a Ka-band.

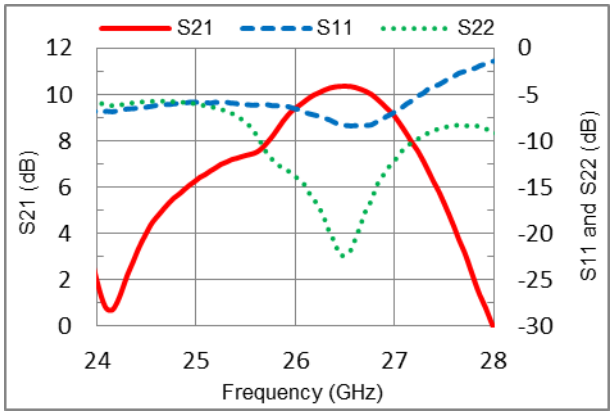

Fig. 5. Measured S-parameters of Doherty power amplifier (Bias B).

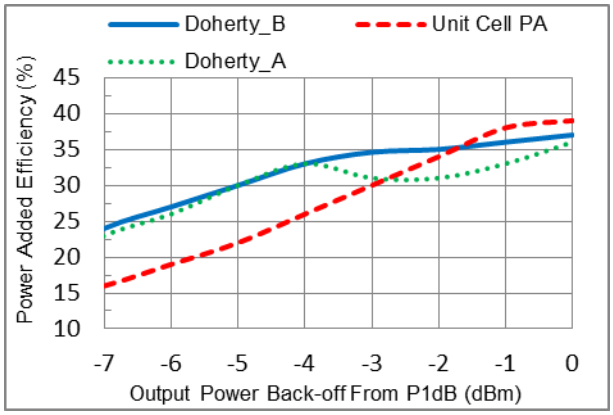

Fig. 6. Measured PAE of DPA and unit cell power amplifiers at 26.4 GHz under both bias conditions (Bias A and B).

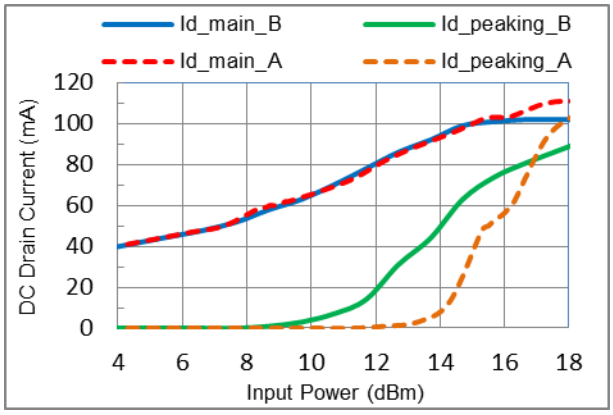

Fig. 7. Measured Drain current of main and peaking amplifiers under both bias conditions (Bias A and B).

TABLE I
COMPARISON TO PREVIOUS RESULTS

Process	45nm CMOS SOI	130nm CMOS	90nm CMOS	GaAs HEMT	**GaAs HEMT**
Ref.	[8]	[5]	[6]	[7]	**This Work**
Freq (GHz)	42	60	71-76	42	**26.4**
Supply (V)	2.5	1.6	1.7	5	**5**
Psat (dBm)	18	7.8	11.7	21.8	**25.3**
Peak PAE (%)	23	3	30.6	25	**38**
Back-off PAE (%)	17	1.5	15.6	23	**27**
Gain (dB)	7	13.5	4.7	7	**10.3**

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