HF Mismatch Characterization and Modeling of Bipolar Transistors for RFIC Design

Tzung-Yin Lee and Yuh-Yue Chen
Skyworks Solutions, Inc. 5221 California Avenue, Irvine, CA 92617

***Abstract* — This paper presents a methodology to characterize and model BJT's mismatch behavior for RFIC design. A measurement technique based on the conventional S-parameter measurement is developed to measure the mismatch behavior at high frequencies (HFs). First, besides the typical de-embedding, the bondpad mismatch is subtracted statistically from the capacitance mismatch measurement. Second, a semi-empirical methodology using physical parameters, such as window CD and vertical doping, is developed to model the measured AC mismatch behavior for transistors of different size. Finally, a systematic procedure is proposed to extract the mismatch parameters, which can be used in the SPICE Monte-Carlo mismatch simulation. The proposed mismatch modeling methodology is validated on an industrial 0.35μm RF BiCMOS process. The proposed model fits the mismatch characteristics of the key AC parameters, such as C_{BE}, C_{BC}, and f_T at different current densities. The model also scales well with geometry for the transistors with sizes useful for RFIC application.**

***Index Terms* — Bipolar modeling, mismatch modeling, RF circuit design.**

I. Introduction

Fast commoditization of low-cost, high-performance wireless application has driven higher-level integration RFICs. Direct conversion architecture has been widely employed to achieve the desired level of integration. However, generating balanced IQ signals at RF is a typical challenge in the realization of such a direct conversion transceiver [1]. Mismatch is often the main mechanism limiting the precision of such balanced IQ generation.

In the past, BJT mismatch characterization and modeling has been focused on key DC parameters such as I_C and current gain β [2][3]. While modeling of the DC mismatch parameters is sufficient for most analog and mixed-signal applications, it can't predict fully the phenomenon observed in some of the contemporary RF circuitry. For instance, the LO leakage of a direct conversion transmitter operating at multi-GHz ranges is usually underestimated with only DC mismatch parameters.

This paper presents a mismatch modeling methodology to include the key AC parameters, such as C_{BE}, C_{BC}, and f_T, for the high-speed bipolar transistors used in RFIC. It is based on the conventional S-parameter technique to measure the AC parameter mismatch at high frequencies. The following sections describe the measurement, modeling, extraction, and validation for AC mismatch for the BJTs used in RFIC design.

II. Devices and Measurements

The mismatch measurement is performed on matching transistor pairs from a 0.35μm RF BiCMOS process [4]. The f_T peaks of the high-speed vertical NPN BJTs are about 27 GHz at V_{CE}=1V (BVCEO~3.6V). The f_Ts of the transistors peak around the collector current densities J_C~400μA/μm at V_{CE}=1V. As the BJTs in the process are specifically designed for RF applications, the widths of the transistors are limited to a few discrete values, i.e. 0.4, 0.65, 0.9, and 1.15μm. Transistors of a matching pair are laid out in close geometrical proximity with their own ground-signal-ground (GSG) pads for the measurement.

A 4-port S-parameter measurement is an intuitive choice to measure a matching pair. However, besides being more efficient, it provides no substantial advantage over a simple 2-port measurement in mismatch characterization. A 4-port s-parameter measurement requires special probe and calibration. Its result has the same uncertainty as in that of the simple two-port measurement. Therefore, a simple two-port S-parameter technique with an accurate calibration procedure is used for all the HF capacitance and f_T measurements.

The measurement is performed on a Cascade wafer probe station with auto probing so that consistent probing can be achieved over multiple dies. All the S-parameter data are de-embedded with the open measurements. The short de-embedding is omitted, as the parasitic inductance and resistance of the pads introduces insignificant difference to the f_T and capacitance measurements. The short de-embedding can introduce more numerical fluctuation in the data.

Two factors, i.e. the probe resistance and pad capacitance mismatch, need to be carefully dealt with in the AC mismatch characterization, regardless it is obtained from a 2- or 4-port s-parameter measurement. According to simulation, the impact of a limited amount of probe resistance difference, e.g. within 1Ω, to the accuracy of the f_T and capacitance measurement is insignificant. It is because the capacitance is derived from the current, i.e. the imaginary part of the y-parameters, and f_T is also essentially a current gain measurement.

The pad capacitance mismatch is inevitably included in the capacitance mismatch characterization. Although the pad capacitances are calibrated out by the open de-embedding, the mismatch of the GSG pad capacitance

remains in the measurement result [5]. To subtract the pad mismatch from the total capacitance mismatch, we assume it is statistically uncorrelated with the transistor mismatch. It is a good assumption because the pad and transistor are manufactured with totally different steps in the process. Therefore, the transistor mismatch component can be extracted by statistically subtracting the pad mismatch component from the raw measured result. For the case of C_{BE}, the actual mismatch can be extracted as

$$\sigma C_{BE} = \sqrt{\sigma C_{BE(raw)}^{\ 2} + \sigma C_{pads}^{\ 2}} \qquad \text{Eq. (1)}$$

The subtraction of pad mismatch as with Eq. (1) is only needed for the parameters derived from y11 and y22, i.e. C_{BE} and C_{CS}. The mismatch of C_{BC} is not over accounted by the pad mismatch, as it is derived from y12.

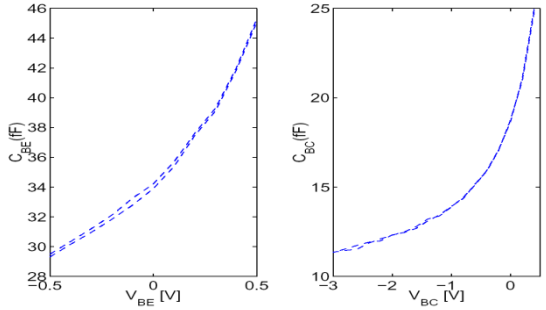

Figure 1 Measured C_{BE} and C_{BC} of a pair of transistors.

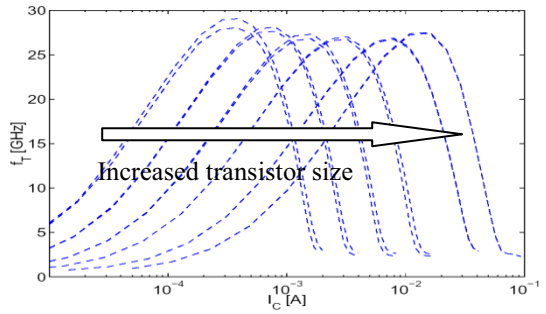

Figure 2 Measured f_T of pairs of transistors of various sizes.

Figure 1 shows the measured C_{BE} and C_{BC} of a pair of transistors. The C_{BE} and C_{BC} mismatch of the transistor pair can be extracted from the plot for the particular die. The measurement is repeated for the transistor pairs of different sizes and on multiple dies of multiple wafers. The standard deviation can then be calculated from the mismatch data collected from all these dies and be represented as a function of the transistor sizes.

Figure 2 shows the measured f_T of transistor pairs of various sizes. As shown in the figure, the f_T mismatch is strongly dependent on the transistor sizes. Also the mismatch of f_T is a function of the bias. The bias dependence of the f_T mismatch can be predicted with the proposed model discussed in the next section.

III. Mismatch Model

The scaling behavior of the device mismatch can be viewed as composition of random and systematic components [6]. The random part decreases with the inverse square root of the area, while the systematic part, such as a process gradient, can increase with the area [6]. Physically speaking, mismatch is caused by the non-uniformity of a process and the lithographic variation. For example, the 1-sigma values of the B-E junction capacitance mismatch σC_{BE}, of a pair of BJTs can be expressed as

$$\sigma C_{BE} = \frac{\sigma L_E}{L_E} + \frac{\sigma W_E}{W_E} + 0.5\frac{\sigma D_{base}}{AE^{\alpha D_{base}}} \qquad \text{Eq. (2)}$$

where L_E, W_E, and AE are the length, width, and area of the emitter window, σL_E and σW_E are the 1-sigma values of the mismatch in L_E and W_E, σD_{base} is the 1-sigma value of the base doping mismatch, and αD_{base} is the area-dependence coefficient of the base doping profile mismatch.

Note that the first two and the third terms in Eq. (2) have different dependence on the device area. Therefore this semi-empirical equation allows a flexible modeling of the mismatch area dependence. For a mismatch behavior exhibiting a very significant process gradient [6], another term modeling the systematic mismatch, which increases with the device area, can also be added to the end of this equation. However, as this behavior is not very obvious in the process characterized here, the systematic mismatch term is omitted here.

Analogous to that of C_{BE}, the 1-sigma values of the B-C junction capacitance mismatch σC_{BC}, of a pair of BJTs can be expressed as

$$\sigma C_{BC} = \frac{\sigma L_C}{L_C} + \frac{\sigma W_C}{W_C} + 0.5\frac{\sigma D_{coll}}{AC^{\alpha D_{coll}}} \qquad \text{Eq. (3)}$$

where L_C, W_C , and AC are the length, width, and area of the B-C junction, σL_C and σW_C are the 1-sigma values of the mismatch in L_C and W_C, σD_{coll} is the 1-sigma value of the collector doping mismatch, and αD_{coll} is the area-dependence coefficient of the collector doping concentration mismatch.

The above equations account for only the mismatch of the junction capacitance. In reality, the total capacitance of B-E and B-C junctions should also include the extrinsic and parasitic components such as the capacitance over the emitter spacers, the extrinsic B-C junction, and the field oxide. However, for the sake of simplicity, these components are implicitly lumped into the mismatch equations of the intrinsic junction capacitances.

The proposed C_{BE} and C_{BC} mismatch model can be implemented on top of the HICUM model [7], i.e. applying the mismatch Eq. (2) and Eq. (3) to the related HICUM parameters as perturbation. The amounts of the perturbation are randomly generated in a Monte-Carlo process with the independent random variables of σL_E , σW_E, etc.

The above equations are semi-empirical, but can maintain correlation between the mismatch of different electrical parameters. This is achieved by sharing common parameters, such as the variations in window CDs and vertical doping profiles, in their mismatch equations. For instance, σD_{coll} influences not only the mismatch of C_{BC}, but also the high-current roll-off behavior of β and f_T, which is modeled with the parameter ***RCi0*** in HICUM.

$$\sigma RCi0 = \frac{\sigma L_A}{L_A} + \frac{\sigma W_A}{W_A} + \frac{\sigma D_{coll}}{AC^{\alpha D_{coll}}} \qquad \text{Eq. (4)}$$

Similarly the mismatch equations of I_C and I_B also share the same emitter window parameters as they are expressed as

$$\sigma I_C = \frac{\sigma L_E}{L_E} + \frac{\sigma W_E}{W_E} - \frac{\sigma D_{base}}{AE^{\alpha D_{base}}} - \frac{\sigma T_{base}}{AE^{\alpha T_{base}}} \qquad \text{Eq. (5)}$$

$$\sigma I_B = \frac{\sigma L_E}{L_E} + \frac{\sigma W_E}{W_E} - \frac{\sigma S_{emit}}{AE^{\alpha S_{emit}}} \qquad \text{Eq. (6)}$$

where σT_{base} and αT_{base} are the 1-sigma value and the area-dependence coefficient of the base thickness mismatch, and σS_{emit} and αS_{emit} are the 1-sigma value and the area-dependence coefficient of the emitter surface recombination velocity mismatch.

The mismatch of the transit time parameter ***TF*** is modeled as

$$\sigma T_F = \xi_{TF} \frac{\sigma T_{base}}{AE^{\alpha T_{base}}} \qquad \text{Eq. (7)}$$

where ξ_{TF} is an empirical parameter to adjust the mismatch of ***TF***. While σT_{base} and αT_{base} are shared by both the I_C and ***TF*** mismatches, ξ_{TF} is needed to decouple the mismatches of these two electrical parameters. It can also be explained by the fact that ***TF*** is a function of not only the base thickness but also the base doping gradient or even the band gap engineering.

IV. Characterization and Extraction Results

The characterization results are collected on 56 dies of 7 wafers from the same lot. No significant statistical difference in the measured results is observed due to the different sample sizes. The standard deviation of the mismatch is calculated from all the available measurements. No measurement point is dropped to alter the statistical representation shown here. The results are presented in such a sequence that the extraction procedure of the mismatch parameters is revealed.

The base-line (without mismatch) model parameters are extracted with a scalable modeling methodology described in [8]. The mismatch simulation is performed with Cadence Spectre statistical (Monte-Carlo) analysis. 0 shows the mismatch behavior of C_{BE} at V_{BE}=0V. Symbols represent the 3-sigma value of the C_{BE} mismatch results collected from 56 dies of 7 wafers and the line represents the model prediction. The vertical bars represent the spread if the 3-sigma values are calculated individually for each wafer.

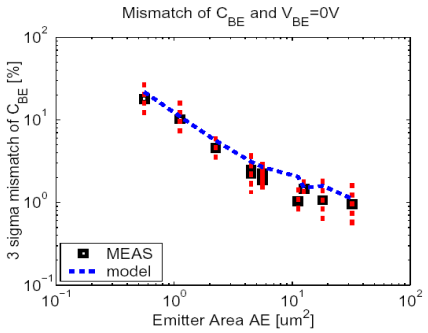

Figure 3 Mismatch results of C_{BE} at V_{BE}=0V.

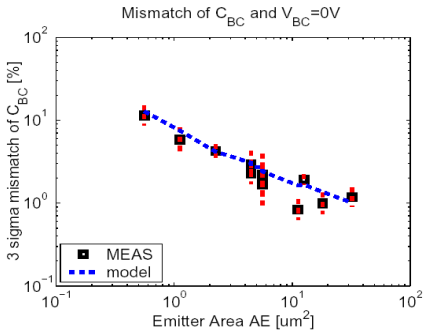

Figure 4 Mismatch results of C_{BC} at V_{BC}=0V.

As shown in Figure 3, the C_{BE} mismatch behavior can be sectioned into two regions: the strong A_E-dependent region for small transistors and the less A_E-dependent region for big transistors. Physically speaking, the mismatch behavior for small transistors is dominated by the lithographic control. Therefore, this section can be described by the first two terms in Eq. (2). Assuming σL_E ~= σW_E, their values can be extracted from the mismatch behavior of the small transistors. The mismatch behavior of the big transistors, i.e. the next section, can be described by the 3rd term in Eq. (2). Therefore σD_{base} and αD_{base} can be extracted from there.

The assumption of σL_E ~= σW_E is usually valid, since the emitter window length and width mismatches are resulted from the same origin while the proximity effect does not significantly influence the mismatch in either the length or width of the emitter window.

Figure 4 shows the 3-sigma mismatch of C_{BC} at V_{BC}=0V. Similar to the C_{BE} mismatch parameter extraction, the lithography mismatch variables σL_C and σW_C can be extracted from the mismatch behavior of the small transistors, while σD_{coll} and αD_{coll} can be estimated from the mismatch behavior of big transistors.

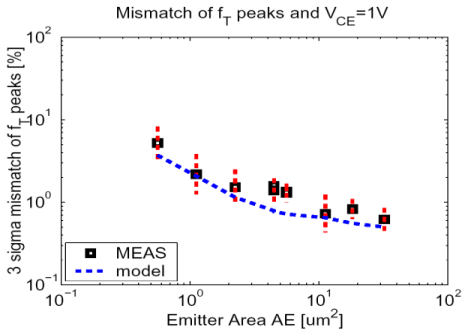

Figure 5 Mismatch results of f_T peaks and V_{CE}=1.0V.

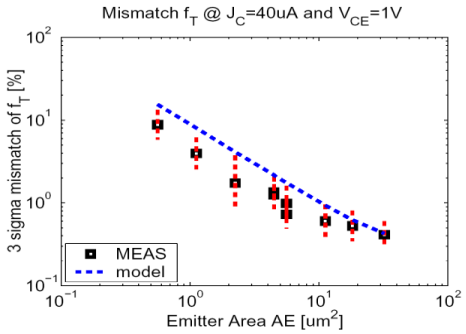

Figure 6 Mismatch results of f_T at J_C=40μA/μm^2 and V_{CE}=1.0V.

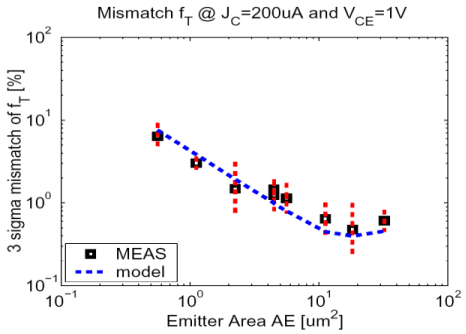

Figure 7 Mismatch results of fT at JC=200μA/μm^2 and VCE=1.0V.

From the I_C and I_B mismatch characteristics, the mismatch parameters related to the base doping and thickness D_{base} and T_{base} in Eq. (5) and the emitter surface velocity S_{emmit} in Eq. (6) can be estimated.

Given the mismatch characteristics of I_C, I_B, C_{BE} and C_{BC} are properly fitted with the mismatch parameters extracted from the above steps, the final mismatch parameter ξ_{TF} in Eq. (7) can be estimated from the mismatch characteristics of the f_T peaks.

Figure 5 shows the 3-sigma mismatch of f_T peaks, while Figure 6 and Figure 7 show the mismatch characteristics of f_T at low (40μm/μm^2) and medium (200μm/μm^2) collector current densities. As shown in these figures, the f_T mismatch characteristics at various collector current densities can be properly predicted with the model, even though the parameters are extracted from either other mismatch characteristics or bias regions.

V. Summary

We presented the mismatch behavior of the key AC parameters of the high-speed BJTs in a 0.35μm RF BiCMOS process. The characterization is performed with a HF S-parameter technique. A semi-empirical model using physical parameters is proposed to predict the mismatch behavior of the transistors. Finally the mismatch parameters are extracted through a systematic procedure, showing the proposed model is capable of simultaneously predicting the mismatch of the key DC and AC parameters for RFIC design.

References

[1] B. Razavi, "Design considerations for direct-conversion receivers", IEEE Transactions on Circuits and Systems II, Volume 44, June 1997, p.428-435.

[2] H.-Y. To and M. Ismail, "Mismatch modeling and characterization of bipolar transistors for statistical CAD", IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications, Volume 43, July 1996, p. 608-610.

[3] P. Drennan, C. McAndrew, and J. Bates, "A comprehensive vertical BJT mismatch model", Proc. of 1998 IEEE BCTM, p.83-86.

[4] Racanelli M, et. al., "BC35: a 0.35 μm, 30 GHz production RF BiCMOS technology", Proc. of Bipolar/BiCMOS Circuits and Technology Meeting, p.125-128, 1999.

[5] A. Perrotin, D. Gloria, S. Danaie, F. Pourchon, M. Laurens, "High frequency mismatch characterization on 170GHz HBT NPN bipolar device," IEEE International Conference on Microelectronic Test Structures (ICMTS), 2006, p. 169-172.

[6] P. Drennan, "Device Mismatch in BiCMOS technologies", Proc. of 2003 IEEE BCTM, p.104-111.

[7] M. Schroter, "HICUM -- A scalable physics-based compact bipolar transistor model," Dec. 2000.

[8] T.-Y. Lee and M. Schroter, "A Scalable Model Generation Methodology of Bipolar Transistors for RFIC Design", Proc. of Bipolar/BiCMOS Circuits and Technology Meeting, p. 171-174, 2001.