# A 283 GHz low power heterodyne receiver with on-chip local oscillator in 65 nm CMOS process

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***Abstract* — A Fully integrated 283 GHz heterodyne receiver in 65 nm CMOS process is presented in this paper. The circuit includes a resistive differential mixer, an intermediate frequency amplifier and a 282 GHz sub-harmonic injection locked oscillator. The on-chip oscillator generates a 94 GHz fundamental tone but exploits a 282 GHz third harmonic. An injection signal of 47 GHz (one sixth of the RF frequency) is used to lock the oscillator on a reference. The receiver measured conversion gain is -6 dB for a DC power consumption of 97.6 mW. Simulated noise figure is 38 dB. The chip size is 820 µm x 780 µm including matching networks and DC/RF pads.**

***Index Terms* — mmW, Heterodyne receiver, Sub-harmonic injection locked oscillator, THz, sub-THz, CMOS.**

## I. Introduction

Sub-micron CMOS technologies have evolved enough in terms of cut-off frequencies that the design of purely based CMOS mmW/sub-mmW systems is actually possible. In comparison of classics high frequency processes like SiGe or III-V, CMOS processes have lower cut-off frequencies and breakdown voltages [1], but offer the advantage of high level of integration, maturity and low-cost. For instance, the lack of power at sub-THz frequencies of standard CMOS technologies must be compensated by advancements in the field of design.

With the arrival of the industrial-scientific-medical (ISM) band at 245 GHz in Europe [2], there will be a high demand of sub-THz chip-sets for different applications such as mmW imaging for security or biomedical purposes, high data transfer and compact range radar. The main application of the heterodyne receiver presented in this work is sub-THz imaging. In [3] the advantage of heterodyne image detectors is presented in comparison to direct detectors which could be translated in terms of imagers as a better output signal-to-noise ratio.

So far, many research groups have been working towards fully integrated sub-THz CMOS systems such as high power sources [1], high frequency direct power detectors [3]; recently, the first CMOS transceiver at 260 GHz was reported in [4]. This announces the beginning of a journey of "beyond ft/fmax" CMOS design which must face the large amount of advantages of advanced processes like SiGe or III-V. In this paper, a heterodyne receiver is the main focus.

## II. Circuit Design

### *A. System architecture*

The simplified architecture of the 283 GHz heterodyne receiver is presented in figure 1. A 282 GHz sub-harmonic injection locked oscillator is used as a local frequency reference. The front end mixer uses a passive structure which allows down converting mixing far beyond CMOS cut-off frequencies. The down converted signal is then amplified at the end of the front end by a three stage differential to single ended amplifier.

Because of the low ft/fmax (155/200 GHz) of the used CMOS process, a low noise amplifier is absent at the RF input which deteriorates considerably the receiver noise figure, since the first component of the front-end is passive. In order to overcome this issue, the local oscillator must generate enough amplitude to decrease consistently the passive mixer conversion loss and thus the noise figure.

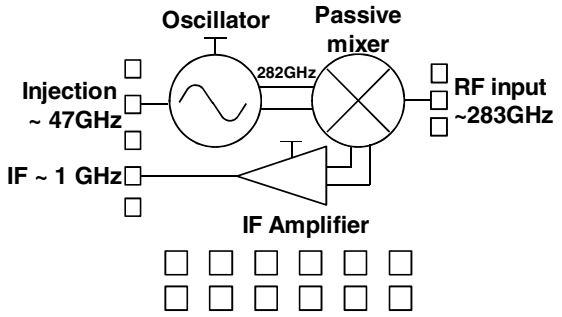


Fig. 1. Basic diagram of the 283 GHz CMOS heterodyne receiver. The system includes: a passive mixer, a sub-harmonic injection locked oscillator and an intermediate frequency amplifier.

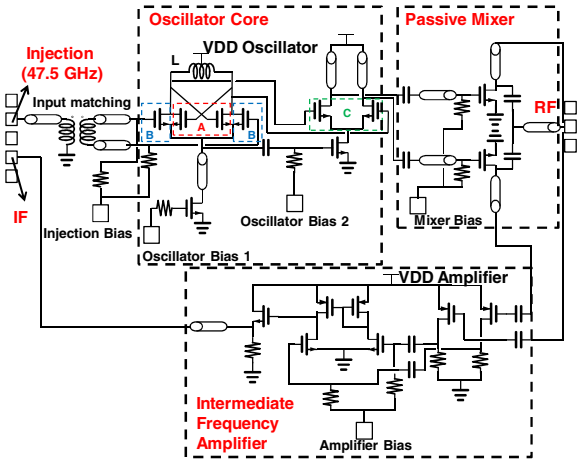


Fig. 2. Transistor level schematic of the heterodyne receiver. Oscillator, passive mixer and IF amplifier.

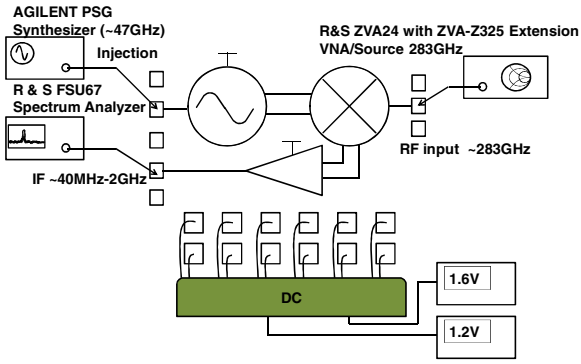


Fig. 3. Test setup: AGILENT PSG as injection source, R&S FSU67 for IF analysis and a VNA R&S ZVA-Z325 as RF source and RF port S11 measurements.

### *B. Oscillator*

The transistor level schematic is presented in figure 2. The oscillator architecture is based on the LC tank push-push structure which offers a differential fundamental output and a single second harmonic signal. An active differential mixer is added in order to multiply the fundamental and the second harmonic signals. As a result the oscillator is able to generate a differential third harmonic output frequency. In this paper a 94 GHz fundamental frequency is chosen in order to obtain a third harmonic of 282 GHz.

The oscillator offers a tuning range of 4.8 GHz and can be locked by a half fundamental frequency injection signal (one sixth of the output frequency) all along the tuning range. The integrated injection system stabilizes the oscillation frequency and fixes the phase noise on the injection source near the carrier. The tuning range is achieved by changing the bias voltage of the oscillator core current source (Oscillator Bias 1).

In the oscillator core schematic, three transistor pairs can be observed; *A* is the cross-coupled pair that acts as a negative resistance in order to compensate the resonator losses, *B* is the injection transistor pair and *C* corresponds to the active mixer transistor pair. These three couples of transistors add enough parallel capacitance to the inductance L so that varactors or capacitors are not needed. Since the fundamental oscillation frequency depends mostly on the three transistor pairs and the inductance, accuracy of the transistors capacitance extraction (intrinsic and access) is extremely important, as well as the electromagnetic high frequency behavior of the inductance L.

Because of the differential nature of the chosen oscillator architecture, the injection signal must be differential as well; for that, a balun transformer in the 47 GHz injection input is designed. Inductive components used for the resonator and matching networks are thin film micro-strip lines modelled using ANSYS HFSS full wave simulations. Injection balun and RF pads models are generated using AGILENT MOMENTUM. MOM capacitor models were provided by the design kit library.

### *C. Passive mixer*

At lower frequencies passive mixers are mostly used because of their high linearity [5], low conversion loss and absence of power consumption. Nevertheless, at sub-THz frequencies, this kind of mixers is used to multiply signals far beyond CMOS ft/fmax allowing the THz design on low cut-off frequencies CMOS processes. The high linearity advantage is kept but the conversion loss increases with frequency.

The passive resistive-mixer used in this circuit is presented in figure 2. This structure was chosen because of the single ended RF input and the differential connections on IF and LO ports that adapt perfectly to the oscillator output and the IF amplifier input. The used architecture was presented by [6]. Simulations results show better than 20 dB LO to IF isolation and 23 dB of LO to RF isolation. For better transistor high frequency accuracy, the NQS (Non-quasi static) option is used in the BSIM3 transistor model provided by the STMicroelectronics design kit.

### *D. Intermediate frequency amplifier*

The transistor level schematic of the IF amplifier is shown in figure 2. This component has three stages; the first one is a common source pMOS differential wide band

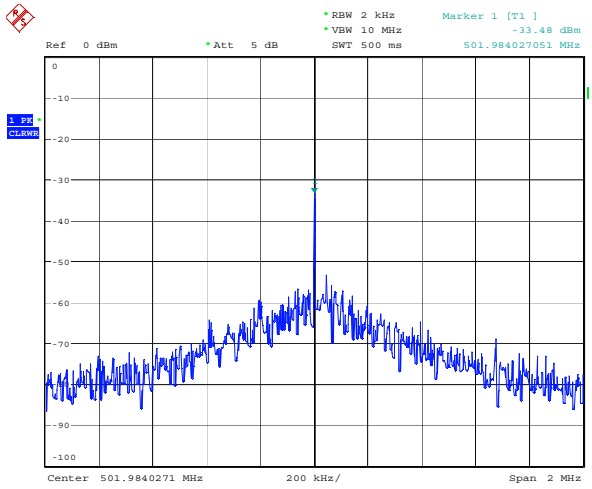


Fig. 4. Measured IF output spectrum at 500 MHz for a RF frequency of 282.3 GHz and a LO frequency of 281.8 GHz.

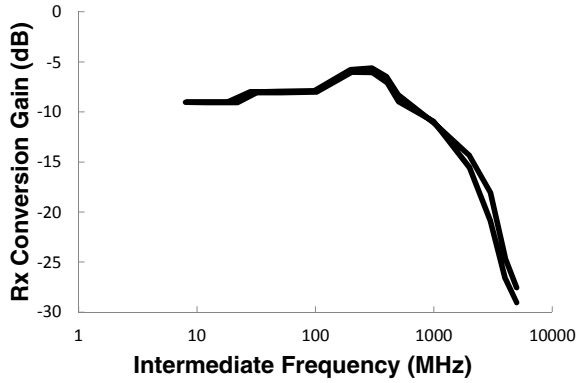


Fig. 5. Receiver conversion gain vs. IF frequency for a fixed LO frequency (lower and upper side bands).

stage, the second one is a differential to single ended nMOS high gain stage and the last one is a source follower for output 50 Ω matching. The amplifier is designed to operate from 40 MHz to 2 GHz IF band.

## III. Measurements

The test setup is depicted in figure 3. An Agilent PSG synthesizer is used as 47 GHz injection source. A VNA R&SZVA24 with a ZVA-Z325 extension is used as the 283 GHz RF source and the RF port S11 measurements. An R&S FSU67 spectrum analyzer is used to measure the IF signal frequency and power.

Figure 4 shows a snapshot of the down converted spectrum of the IF signal around 500 MHz when the LO frequency is locked ($F_{RF}$ = 282.3 GHz, $F_{LO}$=281.8 GHz). The receiver entire front-end achieves low conversion loss even beyond cut off frequencies as showed in figure 5.

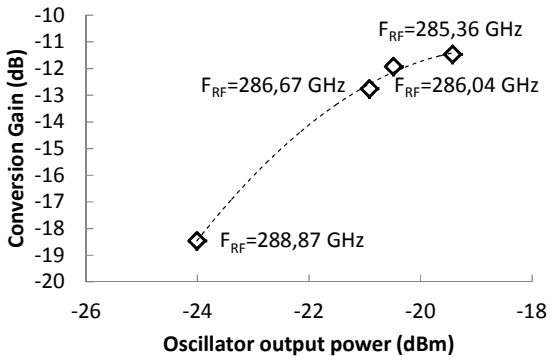


Fig. 6. Measured Rx conversion gain versus oscillator output power for 1 GHz constant IF frequency ($F_{LO}$=$F_{RF}$-1 GHz). Oscillator measured data on stand-alone circuit.

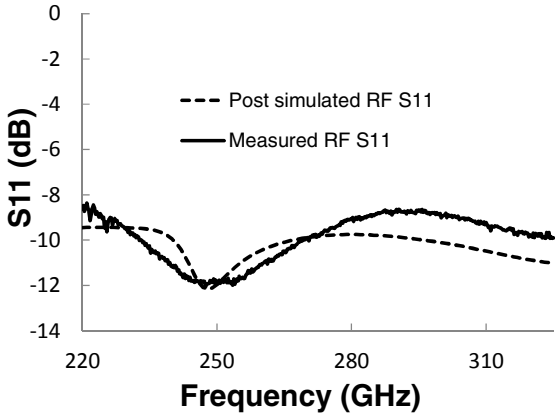


Fig. 7. Measured and post-simulated S11 of the RF input.

The circuit has high symmetry between lower and upper side bands. The RF frequency was tuned from 277.44 GHz to 287.44 GHz with a fixed LO frequency of 282.44 GHz. A maximum of -6 dB conversion gain is achieved for the passive mixer and intermediate frequency amplifier. The LO power must be high enough in order to increase the passive mixer conversion gain and reduce the noise figure: indeed, figure 6 shows a direct correlation between LO power and conversion gain of the complete front-end for fixed IF frequency of 1 GHz. For this graph, the oscillator output power was measured on a stand-alone circuit versus the oscillation frequency and correlated to receiver conversion gain measurements for 1 GHz IF. In figure 7 are depicted the post-simulated and measured S11 of the RF input; measured data provides enough feed-back to adjust and validate the different passive modelling approaches. Figure 8 shows the measured phase noise on the down-converted IF signal at 254 MHz ($F_{RF}$=283.67 GHz). The graph highlights also the measured phase noise of the locking reference source extrapolated with a factor

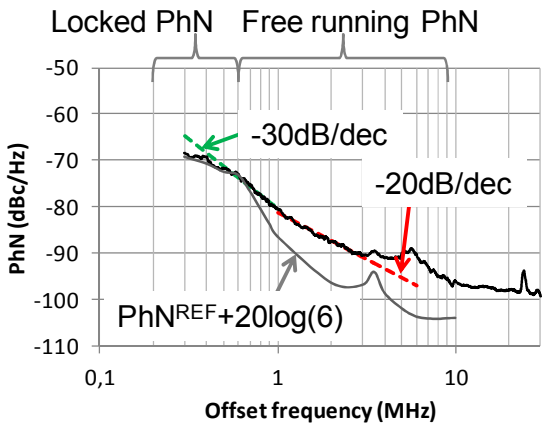


Fig. 8. Measured phase noise at IF frequency (254 MHz) after down-conversion with 283.67 GHz RF input signal. Grey line: measured source reference phase noise (47.236 GHz) extrapolated to 283.416 GHz.

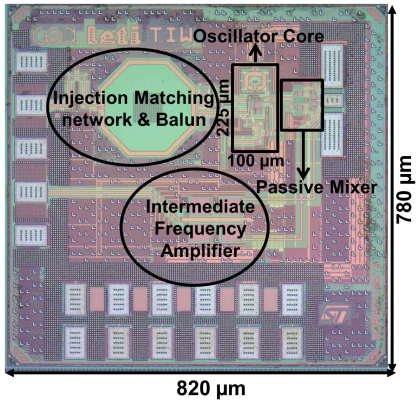


Fig. 9. Chip micrograph.

of six: $PhN^{ref}$+20log(6). The oscillator free running phase noise is -82 dBc/Hz at 1 MHz offset. Figure 9 depicts a micrograph of the heterodyne receiver chip.

## IV. Conclusion

A 283 GHz heterodyne receiver with on-chip local oscillator has been designed and fabricated in a standard 65 nm CMOS process. A maximum conversion gain of -6 dB has been measured for an intermediate frequency of 300 MHz with a simulated single side band NF of 38 dB. The local oscillator is sub-harmonically locked with a 47 GHz frequency reference fixing the LO frequency. The main advantage of this circuit, if compared with the state of the art sub-THz heterodyne receivers, is the low DC power consumption as well as the sub-harmonically injection locked oscillator (cf. Table I).

TABLE I
State of the Art of Sub-THz Silicon Receivers

| References | [2] | [4] | [7] | [7] | **This Work** |
|---|---|---|---|---|---|
| Process | 130nm SiGe HBT | 65 nm CMOS | 130nm SiGe HBT | 130nm SiGe HBT | **65 nm CMOS** |
| Frequency (GHz) | 245 | 260 | 220 | 320 | **283** |
| Conversion Gain (dB) | 21 | 19 (sim.) | 16 | -14 | **-6** |
| $P_{DC}$ (mW) | 358 | 485 | 216 | 3072 | **97.6** |
| NF ssb (dB) | 33 | 19 (sim.) | 18 | 36 | **38 (sim.)** |
| Locking | YES Divider | NA | YES | YES multiplier | **YES Sub-harmonic** |
| Level of Integration | LNA Mixer LO | Mixer LO-chain Demodulator IF-buffer | LNA Mixer | Mixer LO-chain | **Mixer, LO IF-amp** |


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## References


[1] O. Momeni, and E. Afshari, "High Power Terahertz and Millimeter-Wave Oscillator Design: A Systematic Approach," *IEEE Journal of Solid-State Circuits,* pp. 583–597, vol. 46, no 3, March 2011.

[2] Y. Mao, K. Schmalz, J. Borngraber, and J.C. Scheytt, "245-GHz LNA, Mixer, and Subharmonic Receiver in SiGe Technology," *IEEE Transactions on Microwave Theory and Techniques*, pp. 1-11, vol. 60, no 12, 2012.

[3] U.R. Pfeiffer, and E. Ojefors, "Terahertz imaging with CMOS/BiCMOS process technologies," *Proceedings of the ESSCIRC,* pp. 52–60, 2010.

[4] J.-D. Park, S. Kang, S.V. Thyagarajan, E. Alon, and A.M. Niknejad, "A 260 GHz fully integrated CMOS transceiver for wireless chip-to-chip communication," *IEEE Symposium on VLSI Circuits (VLSIC)*, pp. 48-49, 2012.

[5] F. Ellinger, "26.5-30-GHz Resistive Mixer in 90-nm VLSI SOI CMOS Technology With High Linearity for WLAN," *IEEE Transactions on Microwave Theory and Techniques*, vol. 53, no 8, pp. 2559–2565, 2005.

[6] M. Varonen, M. Karkkainen, and K.A.I. Halonen, "V-band balanced resistive mixer in 65-nm CMOS," *Proceedings of the ESSCIRC.* pp. 360–363, 2007.

[7] E. Ojefors, B. Heinemann, and U.R. Pfeiffer, "Subharmonic 220- and 320-GHz SiGe HBT Receiver Front-Ends," *IEEE Transactions on Microwave Theory and Techniques*, vol. 60, no 5, pp. 1397-1404, 2012.