# A Low Power Miniaturized 1.95mm$^2$ Fully Integrated Transceiver with fastPLL Mode for IEEE 802.15.4 / Bluetooth Smart and Proprietary 2.4GHz Applications

Franz Pengg, David Barras, Martin Kucera, Nicola Scolari and Alexandre Vouilloz
CSEM, Neuchâtel, Switzerland

***Abstract* — This paper presents an ultra-low power miniaturized single chip transceiver operating in the ISM band at 2.4GHz. Targeting low power and minimum die size, while excluding RF-options and minimizing the count of external components for low-cost, asks for appropriate architectural choices to obtain high performance. Fast PLL locking and immediate RX-TX turn-around minimize the consumption overhead at wake-up and turn-around. With a die size of only 1.95mm$^2$ in a 90nm standard digital CMOS technology, the receiver achieves a sensitivity of -94.5dBm (1Mbps, BER 10E-3) while consuming only 7.1mA and the transmitter consumes 9.2mA for 0dBm output power. The base-band is compliant with the IEEE 802.15.4 standard, the Bluetooth Smart standard (former Bluetooth low energy BLE) and can be configured for proprietary standards at 2.4GHz, with data-rates up to 3Mbps.**

***Index Terms* — Wireless communication, IEEE 802.15.4, Bluetooth smart, BLE, low power CMOS transceiver.**

## I. Introduction

Low cost, small size and minimum count of external components are of paramount importance for a wide range of applications using radio transceivers for wireless interconnectivity. At the same time, minimum power consumption together with high performance with respect to link-budget, data-rate, start-up and turn-around latencies as well as receiver linearity remain key-parameters. Since a couple of years, advances in the domain of low power, high performance transceivers have been published, with excellent results in terms of current consumption [4-7], sensitivity and transmitter efficiency [3,4,6,7], or integration complexity [1-4].

This paper presents a high performance, ultra-low power fully integrated radio transceiver solution for the 2.4GHz ISM band compliant with Bluetooth Smart (former Bluetooth low energy BLE) and IEEE 802.15.4 standards, with a size of only 1.27x1.54mm$^2$ (including the seal-ring, see die micro-photograph in Fig. 1) in a standard digital 90nm CMOS technology and requiring only a minimum of external components (a 48MHz XTAL and supply decoupling). To our knowledge, this is the first complete transceiver to be published, that combines the above mentioned features of high performance, low power, small size, low cost and complete integration.

## II. Transceiver Architecture

Fig. 1 presents a block diagram of the transceiver and shows the die micro-photograph. Receiver and transmitter present a common 50Ω differential RF-port to the external antenna-interface. Alternatively, a single-ended RF-frontend implementation (not shown) reduces the interface to a single RF-pad with on-chip 50Ω impedance matching. Together with a SCR-type (silicon controlled rectifier) ESD protected RF-pad this RF interface is very robust against ESD discharge (measured >4kV HBM).

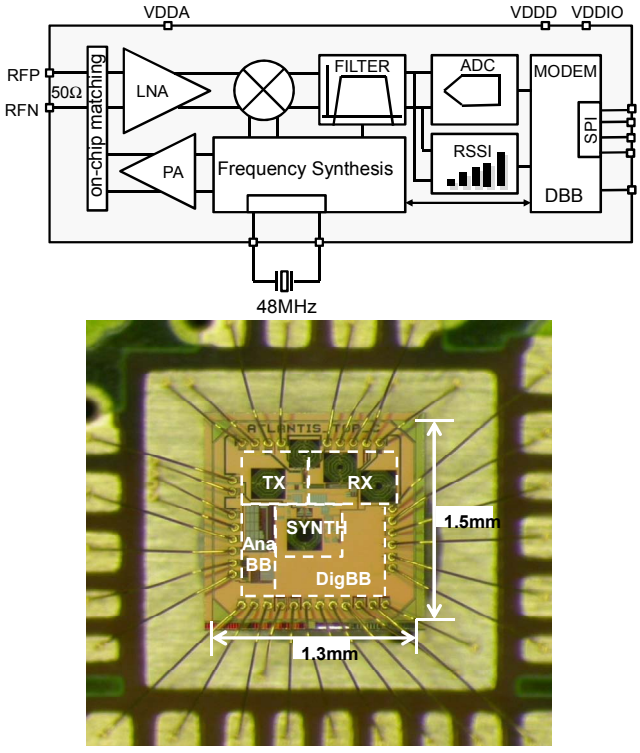


Fig. 1. Block diagram and die photograph of the miniaturized 1.95mm$^2$ fully integrated transceiver.

### A. Receiver

The receiver signal path, shown in Fig. 2, is designed for high performance and low power consumption. High

performance is obtained by generating a voltage gain as high as 32dB in the LNA through high-Q resonances using optimized integrated inductances. Two steps of 6dB gain control are included at the level of the LNA.

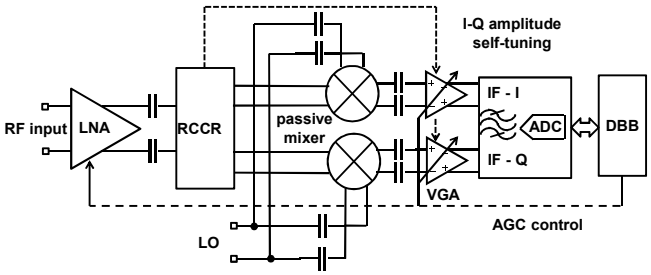


Fig. 2. Block diagram of the receiver signal path.

One of the architectural choices leading to low power consumption is the way to combine the receiver RF-signal path and the frequency synthesizer [3]. In this work, a single-stage passive RCCR polyphase filter in the RF-signal path generates the quadrature signals required for image rejection in the down-conversion to a low intermediate frequency (low-IF), while avoiding the necessity of quadrature signals in the LO-path. A passive down-conversion mixer minimizes the current consumption without compromising linearity. The total current consumption of the RF signal path, from antenna input to down-conversion mixer, amounts to only 2.2mA from 1.2V. A variable gain amplifier (VGA) at IF generates an additional 20dB of voltage gain and provides four 6-dB steps of gain control. Furthermore, by construction, the VGA compensates for the signal amplitude mismatch in the I- and Q-channels, which generally occurs due to process variations impairing the polyphase filter frequency precision. The overall I-Q amplitude mismatch is limited to less than +/-0.5dB, as confirmed by the measurement shown in Fig. 3.

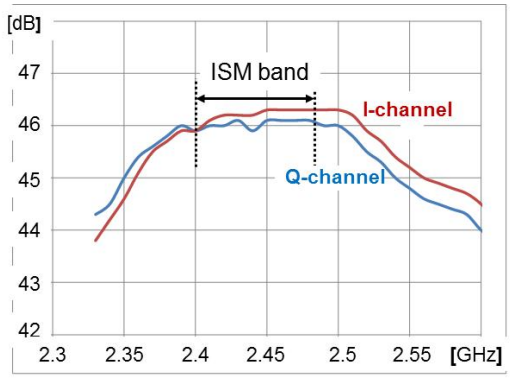


Fig. 3. Measured I- and Q-channel voltage gain over input frequency.

A highly configurable 5th-order polyphase gm-C channel filter followed by a 4-bit PhaseADC [4] completes analog baseband. A RSSI (received signal strength indicator) with 72dB dynamic range in steps of 3dB senses channel activity and signal strength for the automatic gain control (AGC). The latter has a range of 36dB by setting the gain in LNA and VGA with an additional 6dB through current reduction in the RF front-end. Linearity is guaranteed through good co-channel rejection (-10dB) and a flexible AGC strategy. The total current consumption of the analog IF signal path (VGA, filter, PhaseADC, RSSI) amounts to 1.8mA. Bit error rate (BER) measurements for a 1Mbps GFSK signal at different temperatures (-40°,+25°,+85°) and supply voltages (1.2V +/-10%) are shown in Fig. 4. Reduced frontend-gain causes sensitivity loss at high temperatures.

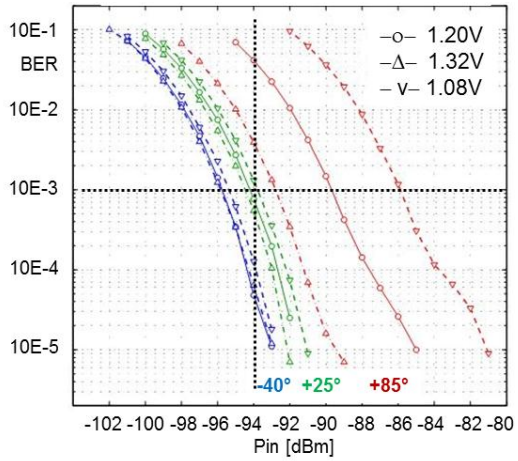


Fig. 4. Measured sensitivity for 1Mbps with varied supply voltage (1.2V +- 10%) and temperature (-40°,+25°,+85°).

### *B. Transmitter*

The transmitter power amplifier stage, shown in Fig. 5, comprises a push-pull preamplifier-buffer as interface to the VCO, a cascoded output stage and a resonant interface between the two amplifying stages.

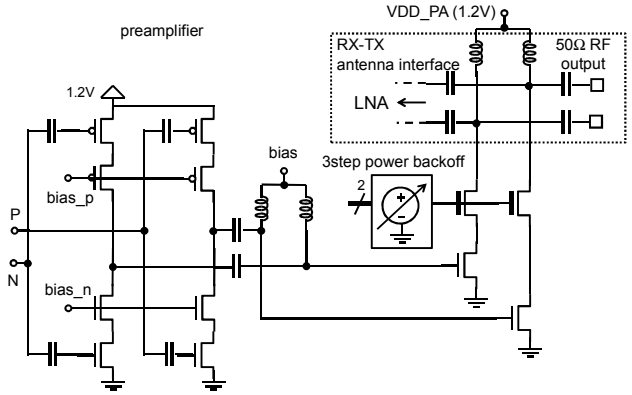


Fig. 5. TX preamplifier and output stage.

Three 3-dB steps of power back-off are available by controlling the cascode bias voltage together with an additional -12dB power back-off obtained by significantly reducing the conduction angle of the switches in the output stage. Fig. 6 shows the measured TX output spectrum and the eye-diagram for a 1Mbps GFSK signal ( =0.5, BT=0.5) after matched filtering.

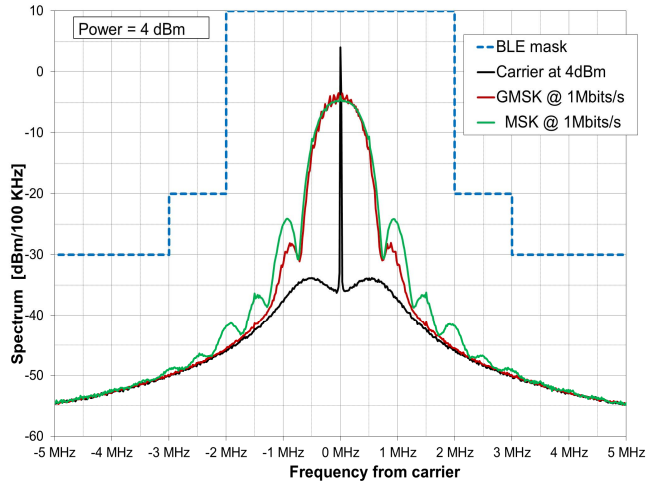


Fig. 6. 1Mbps GFSK (η=0.5, BT=0.5) transmitter output spectrum (including the Bluetooth-smart mask) and eye diagram.

## III. Frequency Synthesizer

The frequency synthesizer comprises a 2.4GHz complementary VCO, a fractional-N divider, a zero to 3rd order configurable MASH, PFD (phase-frequency discriminator), LPF (loop filter) and a 48MHz XTAL frequency reference. Running the dynamic divider directly at the LO-frequency (2.4GHz) without fixed pre-division by $N_{fix}$ avoids the degradation by $20\log(N_{fix})$ [dB] of the phase-noise performance. In RX-mode, the VCO directly drives the switches of the passive mixer, hence requires no additional buffering. In TX-mode, direct modulation of the RF-signal is achieved by introducing a fastPLL-mode. This architectural choice has the big advantage of simplicity and robustness, without need for calibration. The very fast transmitter start-up of only 5µs allows a drastic reduction of the current consumption overhead in applications where duty-cycling is used to limit the average power consumption of the transceiver. The fastPLL-mode can also be made available in the RX start-up procedure to accelerate the locking of the PLL in RX-mode. The data rate can be boosted to 3Mbps (TX up to 4Mbps) for special applications with proprietary protocols. A further advantage of the synthesizer architectural choice is the immediate RX-TX turn-around since, in both modes, the VCO oscillates at practically the same frequency for a given channel.

Fig. 7 highlights the fast RX and TX start-up performance in terms of current integrated over time (41nC over 5µs corresponds to 8.2mA instantaneous current drain which causes only 41µA current consumption overhead when averaged over 1ms TX activity).

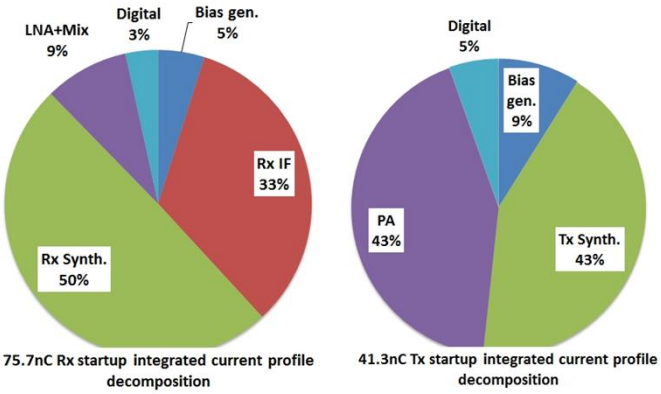


Fig. 7. Receiver and transmitter startup integrated current consumption decomposition.

## IV. Digital Baseband

The integrated digital base-band (DBB) includes the full physical layer with some additional features of the physical link layer, covering Bluetooth Smart and IEEE 802.15.4 standards and, due to its flexibility and programmability, lends itself to a wide range of proprietary protocols. A finite state machine (FSM) handles optimized receiver and transmitter start-up and turn-around. A configurable AGC allows for an optimized sensitivity-linearity tradeoff for input signals up to 0dBm and higher. The DBB further includes a FSK modem with programmable pulse shape and modulation index, data-rate programmable from 62.5kbps to 4Mbps, IEEE

TABLE I
TRANSCEIVER PERFORMANCE AND COMPARISON WITH OTHER EXISTING WORK

| | [3]* | [6]** | [7]*** | This Work |
|---|---|---|---|---|
| Standards | IEEE802.15.4 | IEEE802.15.4<br>IEEE802.15.6 | BLE<br>IEEE802.15.4<br>IEEE802.15.6 | BLE<br>IEEE802.15.4<br>proprietary |
| Max data rate | 2Mbps | 2Mbps | 2Mbps | 3Mbps |
| Technology/size | 180nm/5.8mm$^2$ | 130nm/5.9mm$^2$ | 90nm/3.6mm$^2$ | 90nm/1.95mm$^2$ |
| Supply voltage | 1.8V | 1.0V/1.5V(PA) | 1.2V | 1.2V |
| External RF components | N | Y<br>RX-TX separated | Y<br>RX-TX separated | N |
| RX current | 14.7mA | 4.8mA | N/A | 7.1mA |
| TX current (@ power) | 16mA (3dBm) | 8.9mA (0dBm) | 4.5mA (-1dBm) | 9.2mA (0dBm) |
| PLL settling RX/TX | 40us | N/A | 40us | 15us/5us |
| RX NF | 6dB | 5.7dB | N/A | 5.5dB |
| RX IIP3 | -16dBm | N/A | N/A | -33dBm |
| RX sensitivity | -101dBm | -94dBm | N/A | -94.5dBm |
| TX max output | 3dBm | 5dBm | N/A | 4dBm |

*** Full transceiver, RX sensitivity with processing gain**
**** Transceiver without digital base-band, RX consumption without ADC**
***** Transmitter only, without digital base-band, chip-size including other circuit parts**

802.15.4 chip encoding and decoding, Manchester coding, packet handling, CRC and a high speed SPI interface.

## VII. CONCLUSION

A miniaturized low-power transceiver with minimum count of external components has been presented. Despite the trade-offs incurred by the choice of low-cost and small size, the transceiver performance compares very favorably to works published so far, as shown in Table I, while being fully integrated with a surface of only 1.95mm$^2$ (including seal-ring) in a 90nm standard digital 1PM6 technology, requiring only a 48MHz XTAL and supply decoupling as external components.

## ACKNOWLEDGEMENT

The authors wish to thank the back-end group at CSEM for their precious support in layout, tape-out and preparation of the measurement setups.

## REFERENCES

[1] P. Choi, et al., "An Experimental Coin-Sized Radio for Extremely Low-Power WPAN (802.15.4) Applications at 2.4GHz," IEEE Journal of Solid-State Circuits, vol 38, no. 12, pp. 2258-2268, Dec., 2003.

[2] P. Dal Fabbro, et al., "A 0.8V 2.4GHz 1Mb/s GFSK RF Transceiver with On-Chip DC-DC Converter in a Standard 0.18µm CMOS Technology," Proc. IEEE European Solid-State Circuits Conference (ESSCIRC), 2010, pp. 458-461.

[3] W. Kluge, et al., "A Fully Integrated 2.4-GHz IEEE 802.15.4 – Compliant Transceiver for ZigBee Applications," IEEE Journal of Solid-State Circuits, vol 41, no. 12, pp. 2767-2775, Dec., 2006.

[4] E. Le Roux, et al., "A 1V RF SoC with an 863 to 928 MHz 400kb/s Radio and a 32b Dual-MAC DSP Core for Wireless Sensor and Body Networks," IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers (ISSCC'10), pp. 464-466, Feb., 2010.

[5] M. Vidojkovic, et al., "A 2.4GHz ULP OOK Single-Chip Transceiver for Healthcare Applications," IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers (ISSCC'11), pp. 458-460, Feb. 2011.

[6] A. Wong, et al., "A 1V 5mA Multimode IEEE 802.15.6/Bluetooth Low-Energy WBAN Transceiver for Biotelemetry Applications," IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers (ISSCC'12), pp. 300-302, Feb. 2012.

[7] Y.-H. Liu, "A 2.7nJ/b Multi-Standard 2.3/2.4GHz Polar Transmitter for Wireless Sensor Networks," IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers (ISSCC'12), pp. 448-450, Feb. 2012.