A 53-to-73GHz Power Amplifier with 74.5mW/um^2 Output Power Density by 2D Differential Power Combining in 65nm CMOS

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***Abstract* — Towards wide bandwidth and high output power density for 60GHz PA design in 65nm CMOS, this paper introduces a 2D differential power combining network by metamaterial-based zero-phase-shifter. Simultaneous distributed amplification and power combining can be achieved with improved performances in both power density and bandwidth. The PA measurement results show 13.2 dB gain, 8.7% PAE, 13dBm P1dB, and 20GHz bandwidth (53 to 73GHz) within an area of 0.268mm^2.**

***Index Terms* — 65nm CMOS, metamaterial-based zero-phase-shifter, millimeter-wave PA, power combining.**

I. Introduction

The primary design challenge for CMOS power amplifier (PA) at 60GHz is the limited output power performance. Low supply and breakdown voltage, and lossy substrate of deeply scaled CMOS technologies severely constrain the achievable output power by one single transistor. Apart from the output power performance, bandwidth is another important Figure-of-Merit (FOM) because wideband performance is normally required to cover the wide spectrum along with large PVT variations for designs at 60GHz.

Power combining is one commonly deployed technique to improve PA output power and PAE at 60GHz. However, the output power density (output power per area) by traditional power combining techniques is normally limited due to their 1D nature [1-4]. One 2D power combining by electrical funnel is introduced in [5] but with large size, low PAE and difficulty of matching. Moreover, wideband performance cannot be supported by the traditional power combining methods. At the same time, though distributed amplification is effective to achieve wide bandwidth, traditional distributed amplifiers suffer from low PAE due to un-optimized power performance for transistors in different distributed stages as well as power wastage from resistive terminations. One single-ended dual-fed distributed amplifier (SEDFDA) is introduced in [6] to improve PAE and power gain, but it requires phase-shift of $\pm n\pi$ (n=0,1,2...) to be maintained on gate and drain lines. Since traditional T-line introduces phase-shift proportional to its length, only positive phase-shift such as π can be achieved which is too bulky and lossy for on-chip implementation.

A 2D power combining network was introduced in [7] to realize power combining and wideband amplification simultaneously. With the use of composite right/left handed (CRLH) T-line, a real Zero-Phase-Shifter (ZPS) is designed by 65nm CMOS at 60GHz [7] with a zero-phase matching. As CRLH T-line size is scaled at 60GHz, the ZPS structure becomes more compact and less lossy enough for feasible on-chip implementation. However, due to the single-ended topology with large matching network deployed, the benefit to achieve wideband and high output power density was still not fully demonstrated.

In this paper, we introduce a differential 2D power combining network for 60GHz PA design in 65nm CMOS with demonstrated wide bandwidth and high output power density. Compact differential ZPS structure and 2D power combining network are designed to realize simultaneous power combining and wideband amplification. Transformer matching and neutralization capacitor are also deployed to further improve PA performance. The rest of the paper is organized as follows. The differential ZPS is designed and analyzed in Section II. In Section III, the differential 2D power combining network is then proposed with circuit implementation details. The according differential 60GHz PA prototype is presented in Section IV, with measured results showing improved performance compared with [1-4,7]. Section V draws the conclusion.

II Differential Zero-Phase-Shifter

Figure 1 shows an equivalent circuit for unit-cell of CRLH T-line. CRLH T-line can achieve the zero-phase-shift by combining two parts of phase-shifts in opposite directions. The first part is from the traditional right-handed T-line portion (*Ls* and *Cp*); and the second part is from the left-handed metamaterial portion (*Lp* and *Cs*):

$$\beta = \beta_R + \beta_L = \omega\sqrt{L_S C_p} - \omega\sqrt{L_p C_s} = 0. \qquad (1)$$

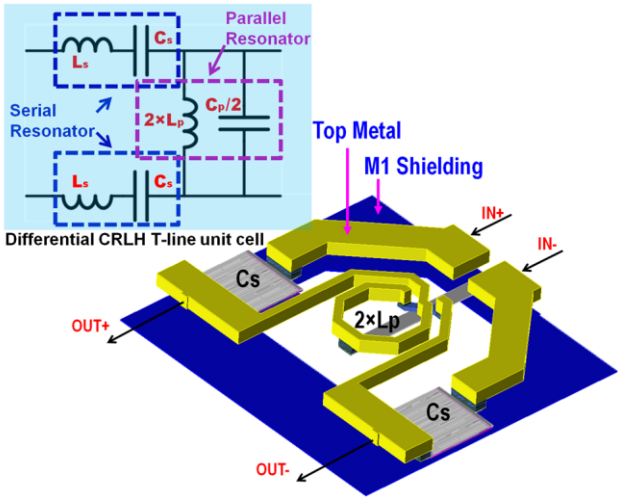

Fig. 1. Equivalent circuit and layout diagrams for one unit-cell of differential CRLH T-line based zero-phase-shifter.

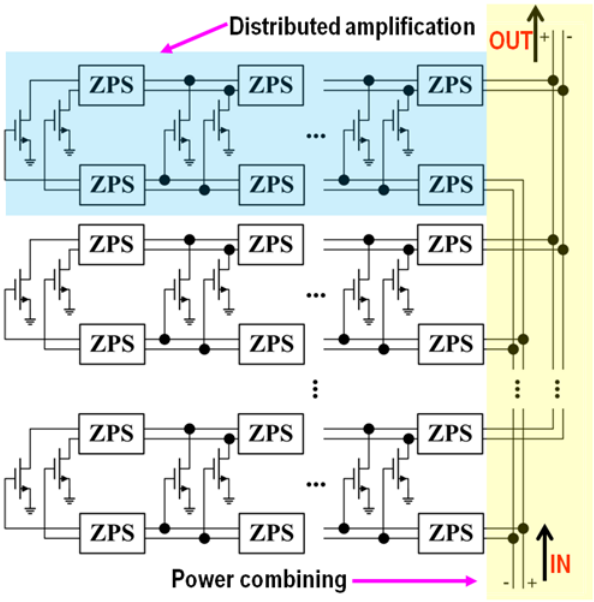

Fig. 2. New differential 2D power combining network by ZPS for both in-phase distributed amplification and in-phase transformer combining.

where β is phase-shift constant. Note here all components (*Ls, Lp, Cs, Cp*) are normalized to unit-cell length. Since CRLH T-line's phase-shift does not depend on its physical length, compact area and low loss can be achieved.

However, it is unknown how to design differential ZPS for wideband and high-density power combining. In this paper, one differential ZPS is implemented with circuit and layout diagrams shown in Fig. 1. The serial capacitor *Cs* is realized with inter-digital capacitors for compact size. M1 shielding is used to improve *Cs* quality factor. The parallel inductor *Lp* is implemented by a loop inductor. Thick top metal is used to minimize ohm and substrate loss. M1 shielding is used around the inductor to reduce the loss in return ground and also to improve isolation. All parasitic from *Cs*, *Lp* and connections form the right-handed T-line portion (*Ls* and *Cp*). Connection lines and M1 shielding are used to adjust *Ls* and *Cp* values for a zero-phase-shift at the targeted frequency ω.

Note that due to the differential design, the parallel inductor for the two differential branches can be merged together with reduced area and improved isolation. In addition, due to virtual ground on the central tap of the merged inductor, de-coupling capacitor is removed with further reduced area.

III Differential 2D Power Combining

With the use of differential CRLH T-line based ZPS, one differential 2D power combining network can be realized as shown in Fig. 2. It leverages *serial power combining* from SEDFDA with in-phase distributed amplification for wide bandwidth; but also *parallel power combining* from transformer with in-phase power combining. Note that the 2D power combining allows more transistors to be combined within a compact area, which ensures a wideband and high-density power combining for 60GHz PA designs.

Note that the single-ended topology in [7] results in large matching network with low power density. In this paper, the differential topology is adopted with benefits of reduced area due to merged parallel inductors and the elimination of de-coupling capacitors. Moreover, loss is also reduced due to confined EM field and nullified parasitic at virtual ground in the differential topology. In addition, the differential topology also allows easy implementation of techniques such as transformer matching and neutralization capacitor. Transformer matching provides DC isolation with easy biasing and compact area. Neutralization capacitor improves stabilization, simplifies matching, and also boosts gain with minimized external loss.

There are, however, two design challenges for the proposed differential topology. First, for a differential implementation, it is desired to design the circuit as symmetric as possible. An asymmetric implementation would cause mismatch in the differential signals and degrade the pre-mentioned benefits. However, since transistor pairs, differential ZPS, and differential input and output terminals are all connected together, it is almost impossible to have a fully symmetric implementation. Second, the input and output terminals in Fig. 2 are on the same side of the power combining network. This would

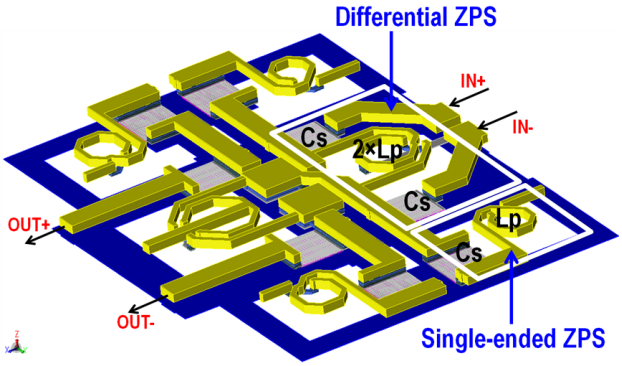

Fig. 3. The proposed layout for differential 2D power combining network.

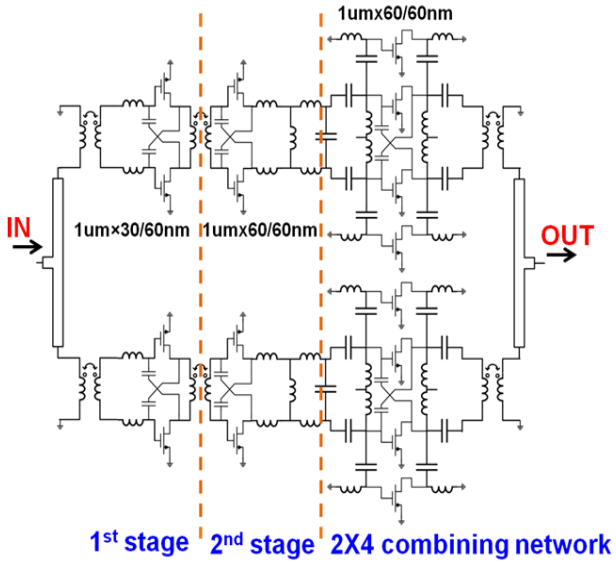

Fig. 4. Schematic of 3-stage differential PA with differential 2×4 distributed power combining network.

lead to long overlapped interconnection, which severely increases parasitic and degrades performance.

To solve the abovementioned problems, one novel differential 2D power combining network topology is proposed in Fig. 3. For each differential gate-line and drain-line, the differential ZPS is implemented in the first distributed stage only. The differential signals then flow into separate directions to 2 single-ended ZPSs on both sides. In this way, the differential topology can be maintained highly symmetrical, while input and output terminals are placed on opposite sides of the power combining network. Though some of the ZPSs are realized single-ended, the whole topology is still differential, allowing techniques such as transformer matching and neutralization capacitor for compact matching and stabilization.

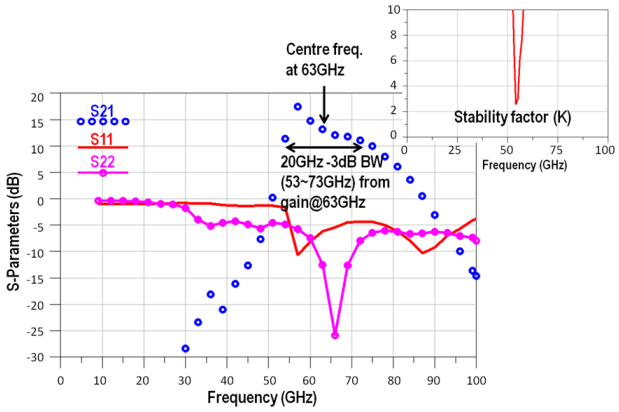

Fig. 5. The measured S parameters of PA and its stability factor with center frequency (63GHz) under 1V supply.

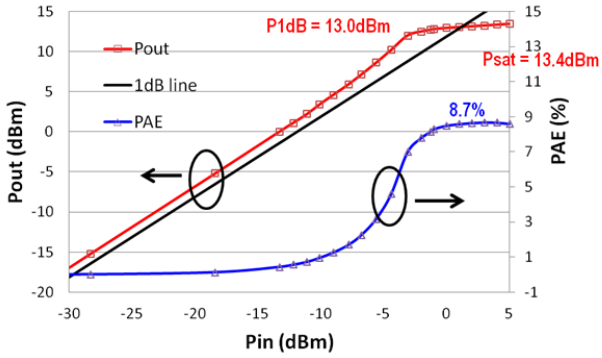

Fig. 6. The measured output power and PAE of PA at center frequency (63GHz) under 1V supply.

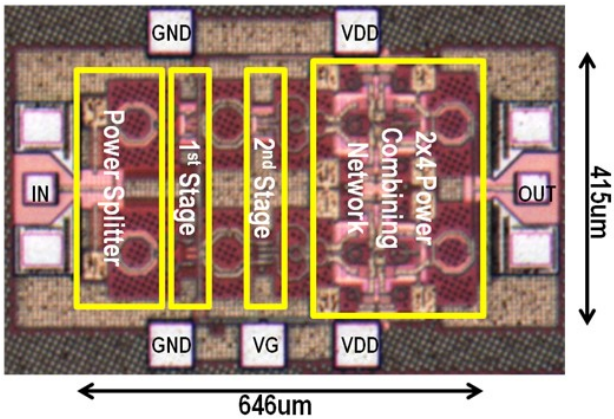

Fig. 7. Die micrograph of PA with 2D power combining network by zero-phase-shifter.

IV. PA Design Aspects and Measurement Results

As shown in Fig. 4, one 3-stage PA is implemented with the central frequency at 63GHz in 65nm CMOS from Global Foundries 1P8M RF CMOS process. The first 2

stages work as drivers; and a 2×4 distributed power combining array is in the 3rd stage, which has 2 power-combining braches with each branch being a differential 2-stage distributed PA. Each transistor is in a common-source (CS) topology with size of 30×1um/60nm for the first stage; and 60x1um/60nm for second and third stages. With a biasing current of 14mA, the simulated f_{max} for the 60um transistor is 231GHz. The parasitic capacitances from transistor gate and drain are absorbed in ZPS design to realize the distributed amplification. After adjusted in-phase by ZPS, all horizontal distributed amplification branches are further vertically combined by transformers. Under the differential structure, transformers are adopted for inter-stage matching. Moreover, the stabilization is realized by compact neutralization capacitors.

The design is verified by EM simulation (ADS-Momentum) before fabrication. Figure 7 shows the chip micrograph with active area of 0.268 mm^2. It is measured on CASCADE Microtech Elite-300 probe station and Agilent PNA-X (N5247A) with frequency-sweep up to 110GHz. Measurement is done at the center frequency (63GHz) with pads de-embedded. Figure 5 shows the measured S parameters with an open-short de-embedding performed. One can observe that the power gain S21 is 13.2dB at 63GHz with the 3dB bandwidth of 20GHz (53 to 73GHz). The PA is unconditionally stable over entire measured frequency range from DC to 100GHz. Figure 6 shows the measured power performance at 63GHz. Output power P1dB of 13dBm and PAE of 8.7% are achieved with 1V supply. The output power can be further improved with more branches combined compactly.

Table I summarizes the proposed PA with comparison to the state-of-art CMOS PAs at 60GHz with power combining. Three FOMs are utilized for comparison. Firstly, FOM1 (P1dB/Area) is used to compare the output power density. Moreover, FOM2 (Gain×P1dB×f^2×PAE) from ITRS 2005 and FOM3 (Gain×P1dB×f^2×PAE× BW/Area) with further considerations of bandwidth and area are deployed to compare the overall performance. The proposed PA achieves FOM1 of 74.5 dBm·mm^{-2}, FOM2 of 130.6 W·GHz^2, and FOM3 of 9744 W·GHz^3·mm^{-2}, which demonstrates a wideband and high-density power combining, and provides the state-of-art performance for all three FOMs.

TABLE I
COMPARISON OF STATE-OF-ART 60GHZ CMOS PAS

	[2]	[3]	[4]	[1]	[7]	This Work
Process(nm)	65	65	65	90	65	65
Supply (V)	1.2	2.2	1	1	1.2	1
Gain (dB)	14.3	10.8	15.4	8.2	8.3	13.2
P1dB (dBm)	11	11.8	2.5	10.1	9.7	13
Psat (dBm)	16.6	14.8	11.5	11.6	11	13.4
Peak PAE (%)	4.9	7.1	11	11.5	7.1	8.7
BW-3dB (GHz)	15	9	8	13.5	16	20
Area (mm^2)	0.46	0.3	0.053	0.6	0.27	0.268
FOM1 (mW·mm^{-2})	27.3	50.5	33.6	17.1	34.6	**74.5**
FOM2 (W·GHz^2)	59.8	46.5	24.4	28.0	16.1	**130.6**
FOM3 (W·GHz^3·mm^{-2})	1945	1395	3686	630	956	**9744**

FOM1 = P1dB/Area
FOM2 = Gain×P1dB×f^2×PAE (ITRS 2005)
FOM3 = Gain×P1dB×f^2×PAE×BW/Area

V. CONCLUSION

In this paper, a differential 2D power combining network is proposed for wide bandwidth and high output power density (output power per area) of 60GHz PA designed in 65nm CMOS. With the use of differential metamaterial-based zero-phase-shifter (ZPS), measurement results have demonstrated high combining power density (74.5mW·mm^{-2}) and wide bandwidth (53-to-73GHz), simultaneously.

ACKNOWLEDGEMENT

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