

245 GHz subharmonic receivers in SiGe

Yanfei Mao¹, K. Schmalz¹, J. Borngräber¹, J.C. Scheytt², C. Meliani¹

¹IHP, Im Technologiepark 25, Frankfurt (Oder), Germany, mao@ihp-microelectronics.com

²System & Circuit Technology, University Paderborn, Germany

Abstract — Two subharmonic receivers for 245 GHz spectroscopy sensor applications in the 245 GHz ISM band have been proposed. One receiver consists of an 2nd APDP (antiparallel diode pair) passive SHM (subharmonic mixer), a 120 GHz push-push VCO with 1/64 divider, and a 120 GHz PA (power amplifier). The other consists of a single-ended four-stage CB (common base) LNA, an 2nd APDP passive SHM, an IF amplifier, a 120 GHz push-push VCO with 1/64 divider, and a 120 GHz PA. The receivers are fabricated in a SiGe:C BiCMOS technology with $f_T/f_{max}=300/500$ GHz. The measured conversion gain are -17 dB resp. 10.6 dB at 245 GHz with 3-dB bandwidths of 13 GHz resp. 14 GHz, and the single-side band noise figure are 17 dB resp. 20 dB; the two receivers dissipates a power of 213 mW and 312 mW, respectively.

Index Terms — 245 GHz, APDP, VCO, subharmonic receivers.

I. INTRODUCTION

Two subharmonic receivers for 245 GHz spectroscopy sensor applications are presented in this paper. The requirement for the 245 GHz receivers are low power, wide bandwidth, high linearity and high integration level with integrated LO signals for easy implementation at PCB level design with an external PLL in future.

In [1] a fully differential 220 GHz integrated receiver front-end without VCO has been demonstrated in SiGe technology. Both the LNA and the mixer are implemented with differential signaling. Although differential signaling is more robust to common-mode noise, it comes at the expense of higher power and more complicated LO distributions. In order to reduce power dissipation, in [2] a single-ended 245 GHz subharmonic receiver comprising of a four stage common base 245 GHz LNA and a 4th sub harmonic 245 GHz transconductance mixer, IF amplifier

and 60 GHz VCO is realized. The receiver in [2] accomplishes high gain and low power, however exhibits a high noise figure due to the 4th sub harmonic index.

In order to achieve high gain, low power, high linearity and low noise figure, two subharmonic receivers based on a 2nd APDP passive subharmonic mixer and a 120 GHz VCO were studied in this work.

II. CIRCUIT DESIGN

Two receivers based on a 2nd APDP passive subharmonic mixer and a 120 GHz VCO are designed and measured for the 245 GHz ISM band. Receiver I consists of a 2nd APDP passive SHM and a 120 GHz VCO-PA chain which provides the local oscillator signals for the mixer. As shown by the rectangle of figure 1, LNA and IF amplifier are not included in receiver I. Receiver II consists of a 4 stage common base LNA, 2nd APDP passive SHM, IF amplifier, and a 120 GHz VCO-PA chain, as shown in figure 1.

In order to obtain a thorough understanding of the gain distribution of the two subharmonic receivers, the CB LNA, 2nd passive SHM, 120 GHz VCO, 120 GHz VCO-PA chain were designed and tested both as separate components as well as in their fully integrated configurations in receiver I and receiver II.

In the following sections, the details of these circuit designs and the two complete receiver designs are presented.

A. CB LNA

CB topology is chosen for each stage for its wide bandwidth, high gain and high isolation at the operating frequency.[2]

Figure 2 shows the schematic of one stage of the four-stage CB LNA. Vcb provides the base bias for the common base transistor through diode-connected transistor D1 and resistor R1. Transmission lines TLsh not only provide the dc ground for the emitters of the transistors but as well work together with the TLser and Metal-Insulator-Metal (MIM) capacitors Cn (n=1-4) to form the input and inter-stage impedance matching network. Transmission lines TLload are inductive loads for each common base stage. Cbyp provides the ac ground for the base connection and the dc supply. Bondpad

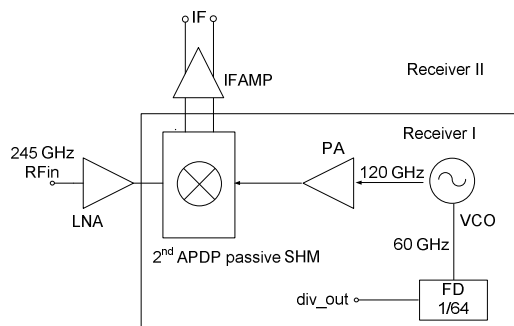


Fig. 1. Topology of two subharmonic receivers

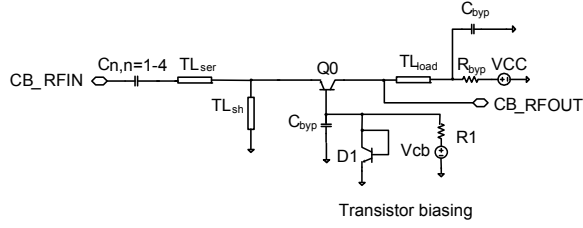


Fig. 2. One stage of the CB LNA

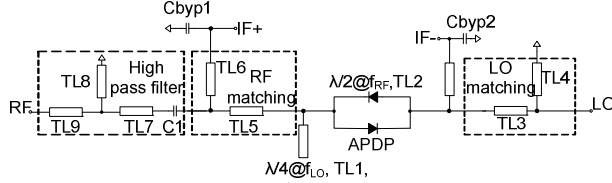


Fig. 3. Schematic of the 2nd APDP passive SHM

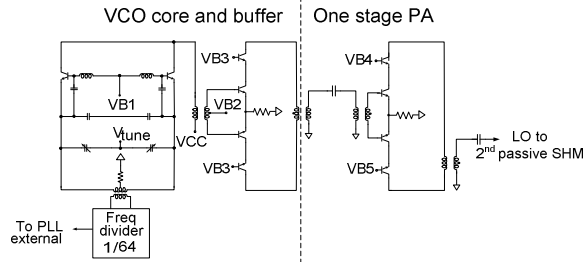


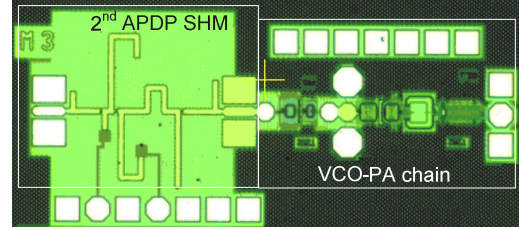
Fig. 4. Schematic of the VCO-PA chain

capacitances are included in both the input and output matching networks.

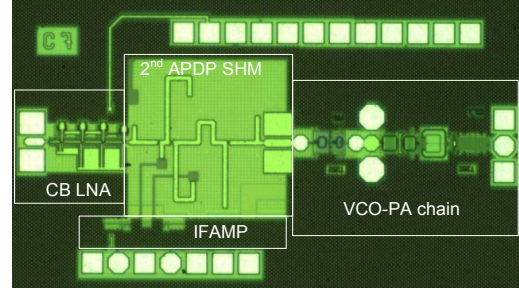
B. 2nd APDP passive SHM

Figure 3 shows the schematic of the passive sub harmonic mixer. [4] An anti-parallel diode pair is the mixing core of the passive sub-harmonic mixer. At RF port, TL1, an open quarter wave length shunt stub at LO, forms the grounding for LO signals and open for RF signals, so that the diodes are terminated with a short-circuit at LO signals but RF signals are not affected. Similarly, at LO port, TL2, a ground half wave length shunt stub at RF, forms the grounding for RF signals and open for LO signals. Transmission line TL3 and TL4 form the LO matching network. Transmission line TL5 and TL6 form the RF matching network. A high pass filter is designed at the input of the RF port, which comprises of transmission lines TL7, TL8, TL9 and capacitor C1. [3] The high pass filter not only provides good rejection at IF frequency, preventing IF leakage to the RF port and allowing RF signals passing through, but as well resonates out the input capacitance. The components used in this network are electrically small enough at IF to be essentially transparent at IF frequency and IF signals are extracted differentially from both sides of the APDP through the bypass capacitors C_{byp1} and C_{byp2} .

As shown in figure 1, in receiver II, a two stage common emitter differential IF amplifier is following after the SHM. The final stage of the IF amplifier utilizes 50



(a)



(b)

Fig. 5. Chip photos: (a) Receiver I (b) Receiver II

Ohm resistors as differential loads for output matching. Between the first stage and second stage, differential emitter followers are utilized as buffer stage. In order to increase the bandwidth of the IF amplifier, no dc decoupling capacitors are introduced between the stages.

C. VCO-PA chain

The oscillator has to provide a 120 GHz single-ended signal to the 2nd APDP passive SHM. To fulfill all requirements in terms of tuning range, power and reliability, a push-push oscillator topology was chosen. With this topology, it is possible to provide a signal path with relatively low fundamental frequency f_0 of 60 GHz to the frequency divider and to provide the 120 GHz signal via a buffer to the 120 GHz PA. The PA uses one-stage differential-cascode, transformer-coupled topology[5]. The schematic of the 120 GHz VCO-PA chain is shown in figure 4.

Both receivers I and II utilize the VCO-PA chain to provide LO signals for the 2nd APDP SHM.

III. LAYOUT DESIGN

Chip photos of the receiver I and II are shown in figure 5(a) and 5(b) respectively. Chip size of receiver I is $1.6 \times 0.7 \text{ mm}^2$. On the left are the RF input GSG pad; on the top are the dc pads for VCO-PA chain; at the bottom are the GSGSG IF output pads and two redundant dc pads. Chip size of receiver II is $1.9 \times 1.0 \text{ mm}^2$. Pad configurations are the same as in receiver I except that on the top dc pads for CB LNA and IF amplifier are included. Metal shielding is adopted for the pad design.

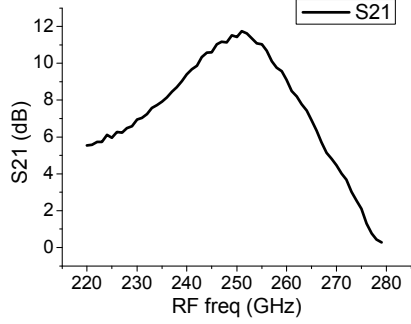


Fig. 6. S21 of the CB LNA

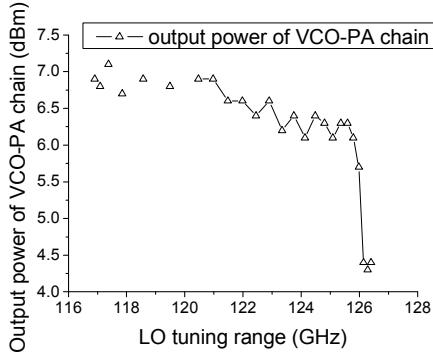


Fig. 7. Output power of VCO-PA chain versus LO tuning range

IV. SIMULATION AND MEASUREMENT RESULTS

Receiver I was measured applying 4 V PA supply voltage with current of 31 mA and 3.3 V 120 GHz VCO supply voltage with current of 27 mA. The total chip dissipates 213 mW. Receiver II was measured applying 2.1 V CB LNA base bias voltage with current of 2.5 mA, 2 V CB LNA supply voltage with current of 24.8 mA, 2.5 V IF amplifier supply voltage with current of 17.9 mA, 4 V PA supply voltage with current of 31 mA and 3.3 V 120 GHz VCO supply voltage with current of 27 mA. The total chip dissipates 312 mW. Measurement setup configuration is the same as in [2].

The CB LNA, 120 GHz VCO, 120 GHz VCO-PA chain were also designed as separate components. The CB LNA has a 3-dB bandwidth extending from 237 GHz to 261 GHz. Gain of 11 dB is achieved at 243 GHz as shown in figure 6 and the simulated NF is 12 dB. Input return loss of CB LNA is below -4 dB throughout the bandwidth. The VCO-frequency changes from 116.9 GHz to 126.4 GHz by increasing the tuning voltage V_{tune} from 0 V to 3 V. An output power of about -1 dBm is measured at 122 GHz, and phase noise of -92dBc/Hz at 1 MHz offset is measured at 1.5 V with a corresponding LO frequency of 122 GHz. Further more, in order to give a clear description of the interface between VCO-PA chain and 2nd APDP passive SHM, figure 7 presents the output

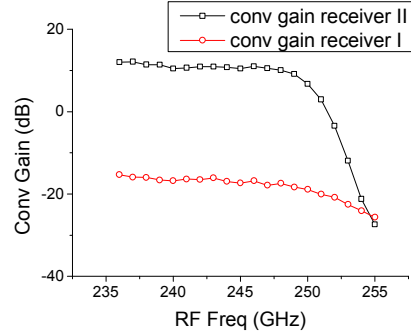


Fig. 8. Conversion gain of receivers I, II versus RF frequency with fixed IF frequency of 1 GHz

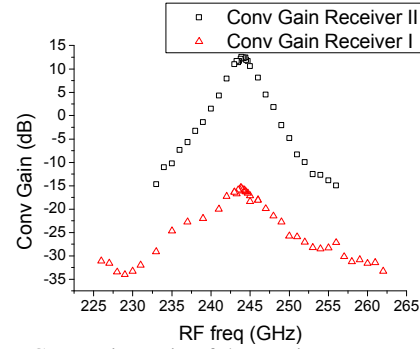


Fig. 9. Conversion gain of the receivers I, II versus RF frequency with fixed LO frequency of 244 GHz

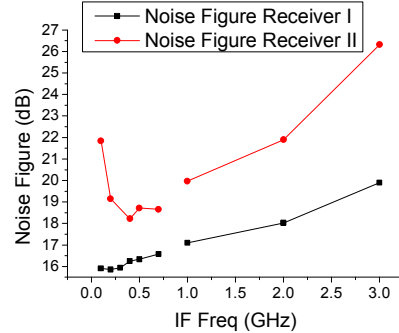


Fig. 10. Noise figure of receivers I, II versus IF frequency power of the VCO-PA chain versus tuning frequency range. 6.5 dBm output power is obtained at 122 GHz.

Figure 8 shows the conversion gain of the receiver with fixed VCO tuning voltage V_{tune} of 1.3 V with corresponding VCO-frequency at 122 GHz, when the input RF frequency is swept. Receiver II achieves 12.5 dB peak-conversion gain when RF frequency is approaching LO frequency 244 GHz with the 3-dB RF frequency bandwidth extending from 242.5 GHz to 245.5 GHz. Receiver I achieves conversion loss of 16 dB when RF frequency is approaching 244 GHz, with the 3-dB RF frequency bandwidth extending from 241.5 GHz to 246.5 GHz. The limited IF bandwidth is due to the filtering of bypass capacitors C_{byp1} and C_{byp2} (2 pF) in the 2nd passive SHM. The IF amplifier contributes 17.5 dB gain in receiver II, which is calculated from the difference

TABLE I
COMPARISON STATE OF ART

	RF (GHz)	ft/fmax (GHz)	Integration level	Conv. Gain (dB)	Power Dissipation (mW)	Input 1 dB CP (dBm)	NF (dB)
[1]	220	280/435	LNA, Mixer	16	216	-	18
[2]	245	300/500	CB LNA, 60 GHz VCO, IFAMP 4 th transconductance SHM	21	358/158 (with/ without VCO)	-37	32
Receiver I	245	300/500	120 GHz VCO-PA, 2 nd APDP passive SHM	-17	213/0 (with/ without VCO)	0	17
Receiver II	245	300/500	CB LNA, 120 GHz VCO-PA, IFAMP, 2 nd APDP passive SHM	10.6	312/99.6 (with/ without VCO)	-9	20

between the conversion gain of the two receivers and then subtraction of the LNA gain.

Figure 9 presents the conversion gain of the receiver versus RF frequency with tuning voltage from 0 V to 3 V and fixed IF frequency 1 GHz. The input RF frequency is swept from 236 GHz to 255 GHz while keeping the IF frequency constant. Receiver II achieves 3-dB RF frequency bandwidth extending from 236 GHz to 249 GHz, with a 13 GHz 3-dB bandwidth. Receiver I achieves 3-dB RF frequency bandwidth extending from 236 GHz to 250 GHz, with a 14 GHz 3-dB bandwidth. Conversion gain of the two receivers drop when RF frequency goes up.

For receiver II, with LO frequency 122 GHz, IF frequency at 1 GHz, corresponding RF frequency is 245 GHz, a -143.4 dBm/Hz output noise power is obtained. With 10.6 dB conversion gain, this corresponds to a 20 dB single-side-band (SSB) NF. For receiver I, noise figure equals to the conversion loss of the receiver because it is passive circuit. Therefore NF of 17 dB is achieved at IF frequency of 1 GHz. Figure 10 presents and compares the noise figure of the two receivers. At RF frequency as high as 245 GHz, when CB LNA couldn't suppress the noise from its subsequent circuits, the receiver I without LNA even achieves better noise performance than receiver II.

Simulated input 1 dB compression point of receiver I and II are 0 dBm and -9 dBm respectively. The maximum RF output power at 245 GHz in the measurement setup [2] is limited to -15 dBm. Further measurements on linearity will be carried out in future.

Table I gives a performance comparison between the receivers of this work and state of the art. Comparing receiver II in this work with that in [1], receiver II has higher integrated level (with VCO), a bit smaller conversion gain, comparable noise figure, but much smaller power consumption which is only half of the receiver in [1]. Receiver I in this work consumes no power (excluding LO generation power consumption) and exhibits better noise figure as well as extreme high input

linearity (0 dBm than in [1],[2], while exhibiting smaller conversion gain.

VI. CONCLUSIONS

Subharmonic receivers for spectroscopy applications at 245 GHz have been presented. The two receivers I and II have high integration level with on-chip LO generation, achieve conversion gain -17 dB and 10.6 dB at 245 GHz with 3-dB bandwidth of 13 GHz and 14 GHz. The single-side band noise figure are 17 dB and 20 dB respectively. The two receivers dissipates extreme low power of 0 mW and 99.6 mW excluding LO generation power consumption. Receiver I without LNA and IF amplifier achieves even better noise figure and much higher input linearity than receiver II and state of the art [1][2].

ACKNOWLEDGEMENT

The authors thank the IHP pilot line staff for excellent fabrication of the chip.

REFERENCES

- [1] E. Öjefors, B. Heinemann, U. R. Pfeiffer, "A 220GHz subharmonic receiver frond end in a SiGe HBT technology," IEEE RFIC, pp.1-4, 2011.
- [2] Mao, Y., Schmalz, K., Borngräber, J., Scheytt, J. C., "245-GHz LNA, Mixer, and Subharmonic Receiver in SiGe Technology," IEEE Trans. Microwave Theory & Tech., vol. pp, no. 99, pp.1 -11, 2012.
- [3] Chapman, M.W., Raman, S., "A 60-GHz uniplanar MMIC 4× subharmonic mixer" IEEE Trans. Microwave Theory & Tech., vol.50, no.11, pp.2580 -2588, 2002.
- [4] Yaoming Sun, Scheytt, C.J., "A 122 GHz Sub-Harmonic Mixer With a Modified APDP Topology for IC Integration", IEEE Microwave and Wireless Components Letters, vol.21, no.12, pp.679 -681, 2011.
- [5] Schmalz, K., Borngräber, J., Heinemann, B., Rucker, H., Scheytt, J.C., "A 245 GHz transmitter in SiGe technology", IEEE RFIC pp. 195- 198, 2012.