A Low-Q Resonant Tank Phase Modulator for Outphasing Transmitters

Gilad Yahalom and Joel L. Dawson

Microsystems Technology Laboratories, Massachusetts Institute of Technology, Cambridge, MA 02139

***Abstract* — A new design concept is proposed for a phase modulator for outphasing transmitter architectures, utilizing the phase shifting capabilities of a resonant tank and the ability to separately control the circuit properties via its components. A prototype in 65-nm CMOS achieves 12 bits of resolution, with a fast settling time of less than five carrier cycles to within 1°. The circuit is also tested as a stand-alone transmitter showing an EVM of less than 5% for 8-PSK modulation at maximum data rate, meeting the FCC requirements for operation at the medical implant communication services (MICS) band.**

***Index Terms* — CMOS integrated circuits, phase modulation, phase shifters, radiofrequency integrated circuits.**

I. Introduction

Recent work on supply-modulated outphasing architectures (such as multi-level linear amplification with non-linear components (ML-LINC) [1], and, more recently, asymmetric multi-level outphasing (AMO) [2]) has proven to be a promising step toward breaking the linearity/efficiency trade-off in radio frequency (RF) power amplifiers (PAs). Phase modulators (PMs) are critical components of these systems. The most important performance metrics for phase modulators in AMO systems are speed and resolution.

The need for speed in the PM arises from the expanded bandwidth of an amplitude/phase representation relative to an I/Q representation [3]. If the system is to maintain a given oversampling rate, the sampling speed and settling time requirement of the PM are correspondingly more severe. In addition, the resolution requirements of the PM are set by the symbol constellation, EVM requirements and ACPR requirements of the relevant standard.

In this paper a new design is presented to achieve the desired fast and accurate phase shifting required for such systems. The proposed design relies on the phase shifting properties of low-Q resonant passive structures [4]. Measurements of a proof-of-concept test chip are described and discussed.

II. Architecture

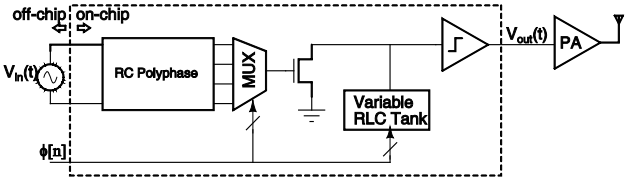


Fig. 1. Block diagram of proposed phase modulator

The proposed topology of the PM architecture is shown in Fig. 1. A differential RF signal is separated into four quadrants via a 2-stage RC polyphase filter. One of the phases is selected and phase shifted by a desired amount through the use of a varying switched capacitor bank acting as part of a resonant RLC tank load for a source amplifier. The signal is then amplitude limited and passed on to the switching PA.

In order to achieve the desired phase modulation of the signal, the impedance properties of the RLC tank are exploited. The impedance of the tank is given by

$$Z_{RLC} = R \parallel j\omega L \parallel \frac{1}{j\omega C} = \frac{R}{\sqrt{1+R^2\left(\omega C-\frac{1}{\omega L}\right)^2}} e^{-j\tan^{-1}\left(R\left(\omega C-\frac{1}{\omega L}\right)\right)}. \quad (1)$$

It may be seen that by varying the value of the capacitor between $C_{min}=C_0(1-1/Q_0)$ and $C_{max}=C_0(1+1/Q_0)$, the phase shift of the carrier signal can be varied by the desired amount across a span of 90°. C_0 is a midpoint capacitance value resonating with the inductor at a center frequency of $\omega_c=1/\sqrt{C_0 L}$ and $Q_0=\omega_c R C_0$ is the quality factor at that midpoint capacitance and frequency value. Operating the system at the carrier frequency ω_c and treating the capacitor as the variable component, the resulting phase relationship between input and output can be written as

$$\angle\left(\frac{v_{\text{out}}}{v_{\text{in}}}\right)=\tan^{-1}\left(\omega_c RC_0\left(\frac{C}{C_0}-1\right)\right). \qquad (2)$$

From (2) another key aspect of this system can be observed. To first order, the phase range and the center frequency can be set independently. Varying the fixed capacitance of the tank, so as to set the median varying capacitor value (corresponding to the middle code word in a single quadrant) to C_0 will ensure that the output phase function is (anti-)symmetric, regardless of the resistor value. Furthermore, changing the resistor value will change the effective quality factor. Increasing the quality factor increases the phase coverage of a single quadrant, allowing to stretch it beyond 90°, or shrink it below it. These properties enable adopting a straightforward, non-iterative procedure for component trimming. In order to tune the tank and set it to the desired center frequency the static tank capacitance C_0 is chosen to resonate with the inductor L. Following, a proper phase coverage can be ensured by setting the resistor value R.

The quality factor of the resonant tank will also determine the ``steepness'' of its response, therefore requiring a smaller change in absolute capacitance value to cover the entire quadrant. For this system there is no need for high frequency selectivity. Therefore a relatively low quality factor value may be used to obtain a better phase resolution for a given capacitor step size. Thus the given name for the proposed phase modulation technique is ``Low-Q Resonant Tank Phase Modulator''.

Given that the system is a second order system, it is a straightforward matter to estimate its settling time given the capacitance change of the tank. The system response will be dominated by its attenuation and damping factors, and specifically for the discussed parallel RLC tank, the settling time constant will be $\tau=2RC$. Therefore the worst-case time required to settle, for example, to within 1° of the desired phase (corresponding to 0.3% of the full range) will occur for the maximum capacitance value and will require a period of roughly

$$\begin{aligned} t_{s,0.3\%} &\approx 6\tau_{\max}=12RC_{\max} \\ &=\frac{12}{\omega_c}\omega_c RC_0\left(1+\frac{1}{Q_0}\right)\approx 2\left(1+Q_0\right)T_c. \end{aligned} \qquad (3)$$

Where the previously given definitions of Q_0 and $C_{\max}$ were used for appropriate substitutions, as well as the definition $\omega_c=2\pi/T_c$. Recalling that the system requires a low quality factor for its operation yields a short settling time of a few carrier cycles.

III. Circuit Design

A. Switched Capacitor Bank

To implement the varying capacitance value, a switched capacitor cell element was used consisting of a MIM capacitor (C_{MIM}) in series with an NMOS switch to enable the toggling of the tank's effective capacitance. The NMOS parasitic drain capacitance (C_{par}) will lower the overall effective capacitance that each cell provides.

The circuit consists of a fixed capacitance (which needs to be controlled) and a varying capacitance which will generate the desired phase modulation. Both of these functions were implemented via a binary weighted array of such capacitor elements. Where a 10-bit array, consisting of 1023 elements was used for the varying capacitance, and a 5-bit, 31 element array was used to implement the function of the fixed capacitor bank.

Each capacitor element in the array represents an effective capacitance depending on the control voltage, which opens or closes the NMOS switch. When the control signal is high an effective ``on'' capacitance may be designated as $C_{\text{on}}=C_{\text{MIM}}$, and when the control signal is low the total capacitance of each element will be $C_{\text{off}}=C_{\text{MIM}}C_{\text{par}}/(C_{\text{MIM}}+C_{\text{par}})$. Thus, given a digital control code word n, and the maximal available code $N=2^b-1$, where b is the number of code word bits, the total bank capacitance will be

$$\begin{aligned} C_{tot} &= nC_{on}+\left(N-n\right)C_{off} \\ &= n\left(C_{on}-C_{off}\right)+NC_{off}. \end{aligned} \qquad (4)$$

An effective LSB capacitance can be identified as $C_{\text{LSB}}=C_{\text{on}}-C_{\text{off}}$, as well as a constant offset capacitance $C_{\text{offset}}=NC_{\text{off}}$.

Any parasitic capacitance, or variation in the intentional MIM capacitor results in both a constant capacitance offset and a change of the desired LSB value. The change in the LSB and resulting capacitance range may be mitigated by the resistor value as explained earlier. The offset can be absorbed into the tank's fixed capacitance and be compensated by varying the fixed capacitor bank value. The use of an additional fixed capacitance bank also allows to compensate for variations in the inductor size, changing the tank's resonance frequency.

B. Active Resistor

As The value required for the resistor element of the tank is fairly small to achieve the desired low-Q behavior and to avoid high sensitivity to the component values. If in addition some tuning ability is desired to this value, then there are some limitations imposed on the

implementation. Using an actual passive resistor may be limited by the accuracy of the process as well as by switch parasitics for trimming capabilities. Therefore the resistive element was chosen to be implemented as an active device, by connecting an operational transconductance amplifier (OTA) with a unity gain negative feedback loop as shown in Fig. 2a.

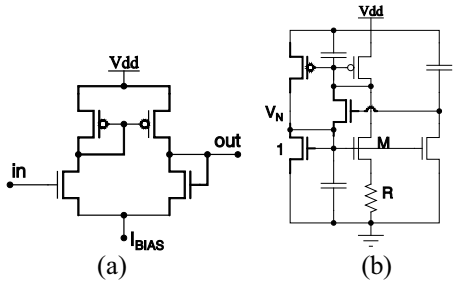


Fig. 2. (a) OTA and (b) current reference schematic

To supply the required current bias for the OTA, as well as provide a method for scaling the resistor value, a Constant-g_m current source [5] is used along with a trimmable current mirror. The schematic of the current source reference is shown in Fig. 2b.

The current reference circuit also includes startup circuitry to ensure the settling of the circuit nodes to their correct steady state values. The reference is proportional to absolute temperature (PTAT), and therefore, provides a constant g_m value for all of the devices referenced to it, independent of temperature change.

C. RC Polyphase Filter

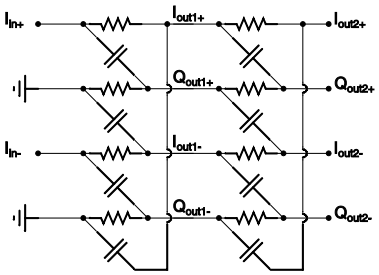


Fig. 3. RC polyphase filter schematic

A schematic showing the polyphase filter design is shown in Fig. 3. A two stage polyphase filter was chosen as opposed to one-stage in order to reduce the sensitivity to frequency variation at the cost of an additional amplitude loss of three dB at the output [6].

In order to avoid asymmetrical loading of the polyphase filter by the common source amplifier stage, a unity gain, source follower amplifier was implemented following a quadrature select analog MUX. This approach allowed for the relevant output to be loaded by a small capacitance and thus not varying and affecting its output greatly.

IV. Measured Results

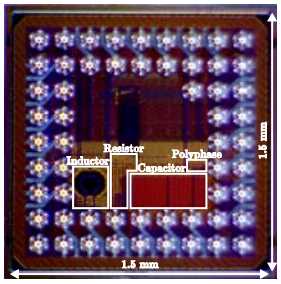


Fig. 4. Chip micrograph

In order to demonstrate the properties described above, a test chip was fabricated in 65-nm CMOS which implements this design (Fig. 4). The active area occupies 0.22 mm^2. The PM was extensively tested in static scenarios as well as high data transfer rate to demonstrate the accurate and fast operation of the circuit and its fast settling time.

The measurements described below were carried out with the PM acting as a stand-alone system operating at the medical implant communication services (MICS) band of 413-419 MHz commissioned by the FCC for low power transceivers communicating with medical implants. Though this usage scenario is not the ultimate purpose of the proposed circuit, where it should be incorporated in an outphasing architecture, it serves well to demonstrate the performance of the circuit in a well defined testing environment. The measurements which follow use the demodulated complex value of the output waveform (and in particular, the phase value) to analyze the behavior of the circuit.

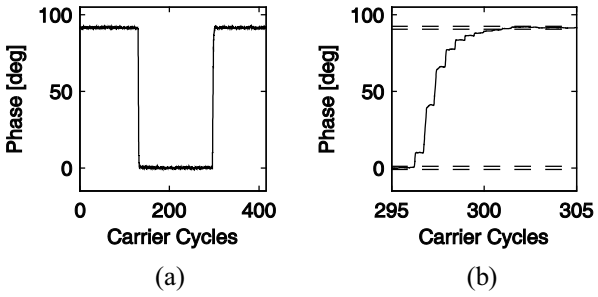


Fig. 5. (a) Phase step settling time and (b) zoom-in

To test the settling time performance of the circuit, a repetitive pattern was transmitted causing a phase change of 90°, being the largest step size. A demodulated signal

step response and a zoomed-in view are shown in Fig. 5a and Fig. 5b respectively. The ±1° limits are marked around the start and end phases in dashed lines.

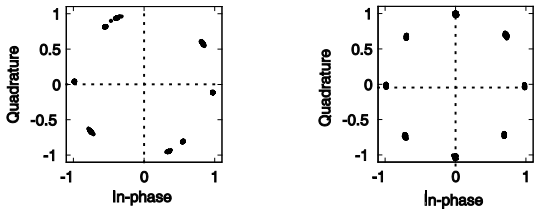
It can be seen that the system indeed has a fast settling time, which is in excellent agreement with (3) at about 5 carrier cycles for settling to 1° of the final value. This speed allows to highly oversample the transmitted signal if desired in order to improve the output spectrum.

To demonstrate the linearity of the proposed PM several experiments were conducted transmitting various modulated data at different rates going up to 80 MSamples/s, one fifth of the carrier frequency which was shown to be roughly the settling time. For each modulation scheme, a random set of symbols was transmitted with and without pre-distortion to compensate for the ``arctangent'' nature of the system's output.

The EVM of these experiments was calculated and a summary of the results is listed in Table 1 for the pre-distorted samples and the values for the samples without pre-distortion given *in parentheses*. Sample constellation diagrams are also shown in Fig. 6.

TABLE I EVM MEASUREMENT SUMMARY

Constellation	Sample Rate [MSample/s]	RMS EVM [%]
QPSK	10	1.39 ***(5.12)***
	80	4.39 ***(7.33)***
8-PSK	10	1.61 ***(20.54)***
	80	2.81 ***(19.08)***



(a) (b)

Fig. 6. EVM measurements for 8-PSK modulation at 40 MSamples/s (a) Without and (b) with pre-distortion

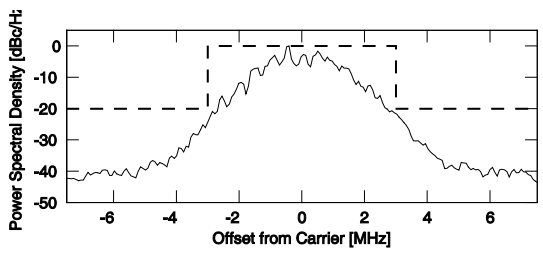


Fig. 7. 8-PSK modulation output PSD overlaid with MICS mask, x8 Oversampling, 15 MSamples/s

The MICS spectral mask alongside with the power spectral density of the output of the circuit is plotted in Fig. 7. The plot corresponds to transmission at a rate of 15 MSamples/s with an oversampling ratio of eight and utilizing 8-PSK modulation and no pulse shaping.

V. Conclusion

An approach to achieve fast, high precision phase modulation for use in an outphasing transmitter was presented. The switching of the capacitive load of a low-Q resonant tank shows promise as being simple to implement and meeting the requirements for use in such outphasing systems.

A proof-of-concept test-chip implementing the proposed PM was fabricated in 65 nm CMOS and tested to verify performance. It was shown to operate at speeds up to one fifth of the carrier frequency. The PM was tested as a stand-alone transmitter and shown to maintain good linearity of less than 5% EVM while modulating data using QPSK and 8-PSK. The output spectrum was shown to comply with requirements for broadcasting in the MICS bands and achieving data rates of up to 15 MSamples/s.

Acknowledgement

The authors would like to thank the TSMC University Shuttle Program for the fabrication of this design.

References

[1] Y.C. Chen, K.Y. Jheng, A.Y. Wu, H.W. Tsao, and B. Tzeng, "Multilevel LINC system design for wireless transmitters," *International Symposium on VLSI Design, Automation and Test*, pp. 1-4, April 2007.

[2] P. A. Godoy, S. Chung, T. W. Barton, D. J. Perreault, and J. L. Dawson, "A 2.4-GHz, 27-dBm asymmetric multilevel outphasing power amplifier in 65-nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 10, pp. 2372-2384, October 2012.

[3] F. Wang, D. Kimball, J. Popp, A. Yang, D. Lie, P. Asbeck, and L. Larson, "Wideband envelope elimination and restoration power amplifier with high efficiency wideband envelope amplifier for WLAN 802.11g applications," *IEEE International Microwave Symposium Digest*, June 2005.

[4] H. Hayashi and M. Mauraguchi, "An MMIC active phase shifter using a variable resonant circuit [and MESFETs]," *IEEE Transactions on Microwave Theory and Techniques*, vol. 47, no. 10, pp. 2021 –2026, October 1999.

[5] S. Mandal, S. Arfin, and R. Sarpeshkar, "Fast startup CMOS current references," *IEEE International Symposium on Circuits and Systems*, May 2006.

[6] J. Xie, A. Do, K. Yeo, and C. Boon, "Analysis and design of RC polyphase network for quadrature signal generation in the 2.45 GHz ISM band," *International Symposium on Integrated Circuits*, pp. 430-433, September.