A 240 GHz Direct Conversion IQ Receiver in 0.13 μm SiGe BiCMOS Technology

Mohamed Elkhouly*, Yanfie Mao*, Srdjan Glisic*, Chafik Meliani*, Frank Ellinger†
and J. Christoph Scheytt‡

* IHP, Frankfurt (Oder), Germany
Email: elkhouly@ihp-microelectronics.com
†Chair of circuit design and network theory, Dresden University of Technology, Dresden, Germany
‡Heinz Nixdorf Institut, University of Paderborn, Paderborn, Germany

***Abstract*—A 240 GHz direct conversion IQ receiver manufactured in 0.13 μm SiGe BiCMOS technology with f_T/f_{max} of 300/500 GHz is presented. The receiver consists of a four stage LNA, an active power divider, an LO IQ generation network, and direct down-conversion fundamental mixers. The integrated IQ receiver yields a conversion gain of 18 dB, an 18 dB simulated DSB NF, and a 3 dB bandwidth of 25 GHz. The required 245 GHz LO power is in the order of - 10 dBm. The receiver exhibits an IQ amplitude and phase imbalance of 1 dB and 3° respectively. It draws 135 mA from the 3.5 V supply and 20 mA from 2 V.**

***Index Terms*—Sub-THz, Direct-Conversion, IQ Receiver, 240 GHz .**

I. Introduction

The continuous scaling of silicon technologies in both CMOS and SiGe BiCMOS leads to an increase of performance metrics as of the transistors as in [1]. During the last few years, the number of publications reporting circuits and systems operating in the sub-THz frequency band from 160-320 GHz has increased steadily [2]–[4]. They target applications such as security scanning, active and passive imaging, space radiometry and high speed wireless communications. The use of frequencies beyond 200 GHz can improve the resolution of imaging systems, while the communication systems benefit from the large available bandwidth around the high frequency carrier. Most of the reported receivers utilize sub-harmonic mixers to relax the LO requirements in terms of frequency of oscillation and output power as in [2] and [5]. Recently a high power 245 GHz source based on VCO and a frequency doubler has been reported in [6]. The use of such sources will facilitate the design of direct conversion fundamental mixers at sub-THz frequencies.

This paper presents the design of a direct conversion wideband IQ receiver based on fundamental down-conversion mixers. Section II describes the receiver architecture, while the third section elaborates the design of the receiver circuits. The measurement results of the chip are presented in section IV. Finally the conclusion is provided.

II. Receiver Architecture

Fig. 1 shows the direct conversion receiver architecture. The input signal is amplified through an LNA. The LNA is based on a modified version of the circuit published in [5]. The output of the LNA is divided into two branches by utilizing an active power splitter. The use of the active power divider compensates the power division losses, this will reduce the noise figure of the receiver. On chip Marchand Baluns are employed to convert the single ended signal into differential ones required by the down-conversion mixer. The 240 GHz LO signal is provided from the signal generator to the receiver chip. Due to the limited output power of the signal generator at 240 GHz, an amplifier identical to the LNA is used to increase signal level. This amplifier will be removed in the final version, in which the LO chain will be integrated. The LO IQ signals are generated through the $90°$ hybrid coupler as shown in Fig. 1. The outputs of the hybrid coupler are converted to differential signals by the means of the Marchand Baluns. LO buffers are integrated to increase the power level at the mixer input, and to minimize the conversion loss of the direct conversion fundamental mixers. VGAs and wide-band amplifiers are used to amplify the IQ baseband signals.

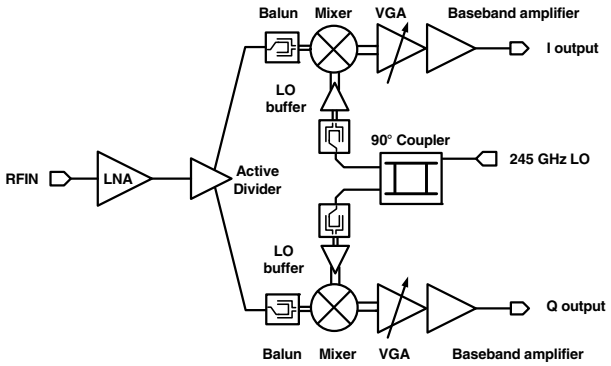

Fig. 1. Architecture of the 240 GHz direct conversion receiver.

III. Receiver Circuits Design

A. Passive Components

As shown in Fig. 1, the receiver contains different passive microwave structures such as Marchand baluns and Branch-line coupler. The Marchand baluns are utilized to convert single ended signal into differential ones required by the down-conversion mixers. The Marchand balun is based on microstrip coupled lines. The microstrip lines have been implemented on the topmost metal layer of the process. The substrate height is around 9.8 μm and the topmost metal thickness is 3 μm. The dimensions of the microstrip coupled lines with even

and odd mode characteristic impedances of 100 Ω and 25 Ω respectively, are 6.5 μm width and 2 μm spacing. The simulated insertion loss of the Marchand balun is less than 1.5 dB from 220 to 260 GHz. The Branch-line coupler is used to generate the LO IQ signals. It has been designed using microstrip lines implemented on the highest metal layer. The 50 Ω microstrip line width is 16 μm. The simulated amplitude and phase imbalance of the coupler are less than 1.5 dB and 3°, respectively.

B. Active Power Divider

The active power splitter is used to compensate the inherent losses of the power division. It also provides RF gain in the receiver, which reduces the noise contribution of the subsequent stages; especially the down-conversion mixer. The schematic of the active power divider is shown in Fig. 2. It is based on a cascode amplifier, where the common base transistor is spitted into two identical transistors. This results in identical current division. The common emitter transistor is biased with I_C for maximum f_T. L-section matching networks are employed to match the input and output impedances to the 50 Ω transmission lines. The simulated gain of the power divider is around 3 dB per branch, and it draws 14 mA from the 3.5 V supply.

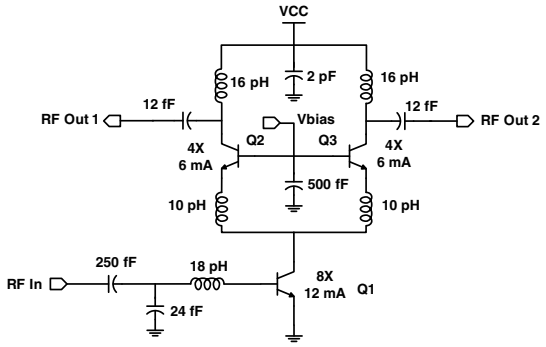

Fig. 2. Schematic of the 240 GHz active power divider.

C. Down Conversion Mixer & LO Buffer

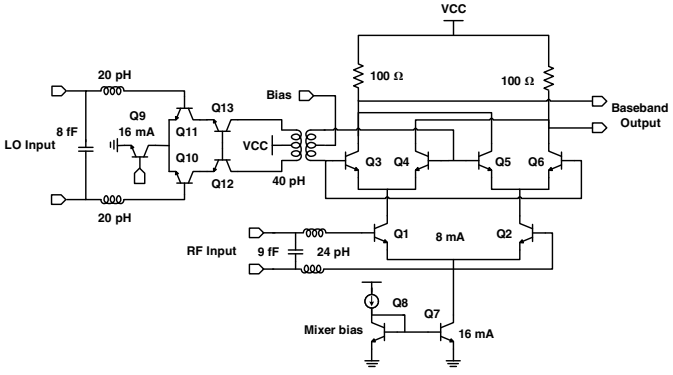

Fig. 3. Detailed schematic of the mixer and LO buffer.

Fig. 3 depicts the detailed schematic of the down-conversion mixer and the LO buffer. This is a fundamental direct-conversion mixer based on Gilbert cell topology. The RF input is fed to the main differential pair Q1 and Q2, they are biased with 8 mA collector current for maximum f_T. In normal cases minimum size transistors are employed in the switching quad Q3-Q6 to increase the switching speed as in [2]. But in this design the switching quad sizes are chosen to be the same size of the Q1 & Q2. This will assure that the HBT is not loaded with much higher current than its peak f_T bias, hence preserving the speed of the HBT in the entire switching cycle. On the other hand, the required LO signal in order to achieve full switching will increase. To address this problem an LO buffer is integrated with the down-conversion mixer core as illustrated in Fig. 3. The LO buffer is a cascode differential amplifier. The transistors Q10-Q13 are biased with I_C for peak f_T. The input impedance of the buffer is matched to the 100 Ω output impedance of the Balun. The output of the buffer is matched to the input impedance of the mixer's switching quad Q3-Q6 to maximize the gain of the buffer hence, reducing the conversion loss of the mixer. The mixer exhibits a simulated conversion gain of -7 dB and a DSB NF of 20 dB. It draws 16 mA from 3.5 V supply. The buffer also draws 16 mA from 3.5 V supply.

D. VGA & Baseband wide-band amplifier

The variable gain amplifiers are utilized to control the gain of the receiver IQ branches. The VGA schematic is shown in Fig. 4 (a). It consists of two emitter followers employed as buffer stage between the mixer and VGA core. The core of the VGA is a resistive loaded differential amplifier, which is linearized through 50 Ω to enhance receiver 1 dB compression point. The output of the VGA is fed to a wide-band differential amplifier depicted in Fig. 4 (b). It consists of a resistive loaded differential amplifier followed by a pair of emitter followers. Minimum size transistors are used in the first amplifier stage and the emitter followers to minimize the power consumption.

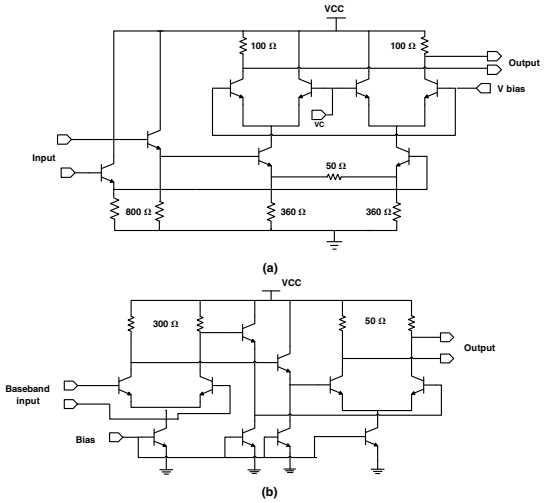

Fig. 4. (a) Schematic of the VGA (b) schematic of the baseband amplifier.

300 Ω resistors are used as loads for the amplifier, they serve as compromise between the gain and the bandwidth of the amplifier. The final stage of the wide-band amplifier is a differential amplifier with 50 Ω resistor loads to archive wide-band matching. The transistors are chosen to be 4 times the minimum size to maximize the swing of the output signal. This wide-band matching amplifier can be eliminated when the chip is integrated with the analog to digital converter. Both VGA and the wide-band amplifier draw 25 mA from the 3.5 V supply. They exhibits 20 dB of gain and 30 GHz of 3 dB bandwidth.

IV. Measurements Results

The IQ receiver has been implemented in 0.13 μm SiGe BiCMOS technology, offering 7 metal layers and a npn HBT with f_T/f_{max} of 300/500 GHz presented in [1]. The chip area is 2.3 x 1 mm^2. The chip draws a 135 mA from the 3.5 V supply and a 20 mA from the 2 V supply. Fig. 5 shows the chip micrograph of the IQ receiver. The test setup used to measure the chip consists of a ZVA-325 frequency converter, which is used as RF signal source and an AMC-280 amplifier multiplier chain from VDI which is used as LO source. Both converters are calibrated at the probe wave guide interface using Erickson calorimeter. The probes insertion losses have been calculated by using the probe S-parameter files, provided by Cascasde Inc. The RF signal source provides a maximum RF power of -25 dBm to the probe tips. Custom probes are used to provide the DC supplies and carry the wide-band IF outputs from the chip. A spectrum analyzer is used to measure the output IF signal and to characterize conversion gain and 1 dB compression point, while a real time scope is used to measure IQ amplitude and phase imbalance. To measure the frequency response of the receiver, the RF frequency was swept from 225 to 265 GHz and the LO frequency was fixed at 245 GHz. The IF output power was measured using the spectrum analyzer, then the conversion gain has been calculated and plotted in Fig.6. The receiver has a gain of 18 dB and a 3 dB bandwidth of 25 GHz. Fig. 7 shows the measured and simulated conversion gain versus LO frequency sweep. The measured conversion gain shows some discrepancy from simulated results, this is due to frequency down shift in the LO IQ generation network and LO buffers. Both RF and LO frequencies were fixed at 246 GHz and 245 GHz respectively.

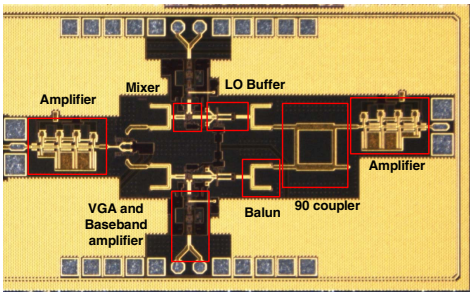

Fig. 5. Chip micrograph of the 240 GHz IQ receiver.

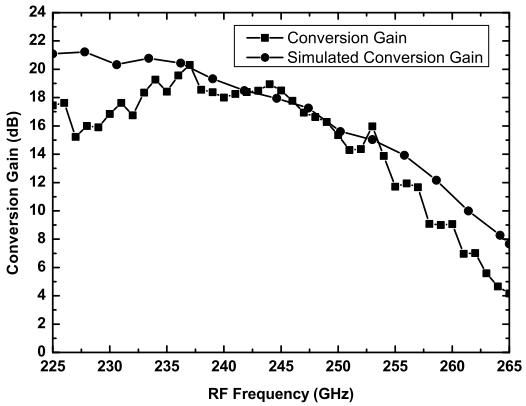

Fig. 6. Measured and Simulated conversion gain vs. RF frequency sweep.

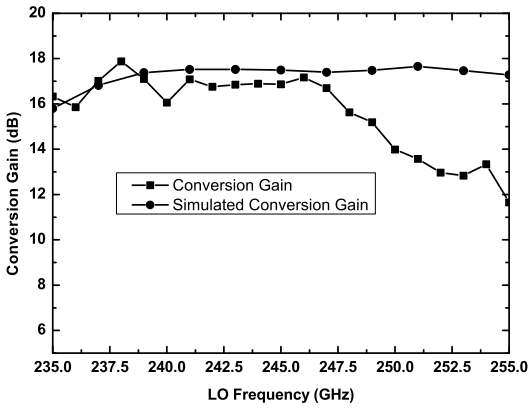

Fig. 7. Measured and simulated conversion gain vs. LO frequency sweep.

Then the RF input power was swept from -56 to - 27 dBm, the measured IF output power and the conversion gain are plotted in Fig.8. The measured gain of the receiver is 18 dB and the output 1 dB compression point is - 27 dBm. The measured maximum IF output power was found to be - 10 dBm. The conversion gain versus LO power was measured and the results are plotted in Fig.9. One can see that there is difference between the measured and simulated conversion gain in the low LO power. This discrepancy can be result of limited accuracy of LO power calibration. In addition to the difference of the insertion loss of the IQ generation network. The control voltage was swept from 2.8 to 3.4 V and the conversion gain was measured. The receiver exhibits 36 dB of gain control. The measured and simulated conversion gain versus control voltage are plotted in Fig. 10. The amplitude and phase IQ imbalance were measured using the wide-band real time scope. The RF and LO frequencies were 246 GHz and 245 GHz respectively, which results in 1 GHz IF output. The receiver shows amplitude imbalance of 1 dB and 3° of phase imbalance between the I & Q outputs.

TABLE I
COMPARISON OF THE RECENTLY PUBLISHED INTEGRATED TRANSCEIVERS ABOVE 160 GHZ.

Ref.	Technology	Architecture	Con. Gain (dB)	LO Freq. (GHz)	Frequency (GHz)	NF (dB)	DC (mW)	Area (mm^2)
[2]	0.13 μm SiGe	Subharmonic Receiver	16	110	200-230	18	216	0.66
[3]	0.25 μm SiGe	Subharmonic Receiver with VCO	35	80	150-160	8	490	0.9
[4]	65 nm CMOS	OOK Transceiver	19	60	253-267	19	458	2
This work	0.13 μm SiGe	Direct Conversion IQ RX	18	245	225-265	18	512	2.1

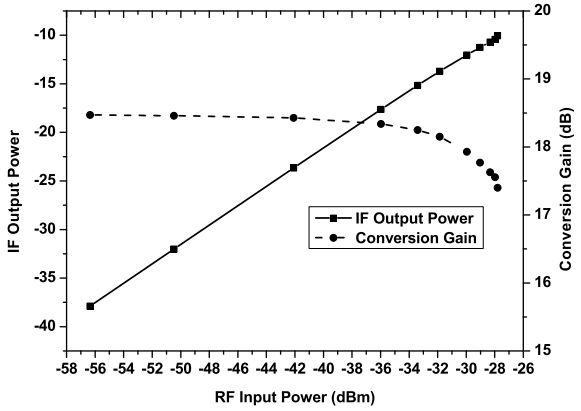

Fig. 8. Measured conversion gain and IF output power vs. RF input power sweep.

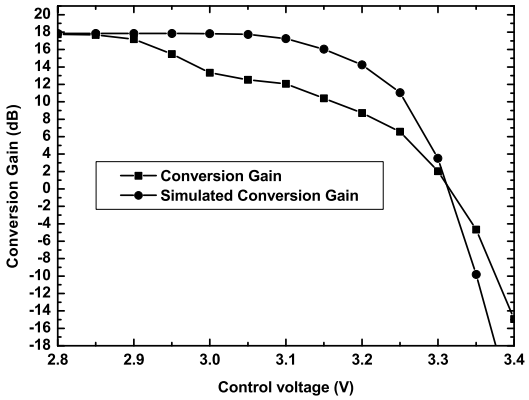

Fig. 10. Measured and simulated gain control of the IQ receiver.

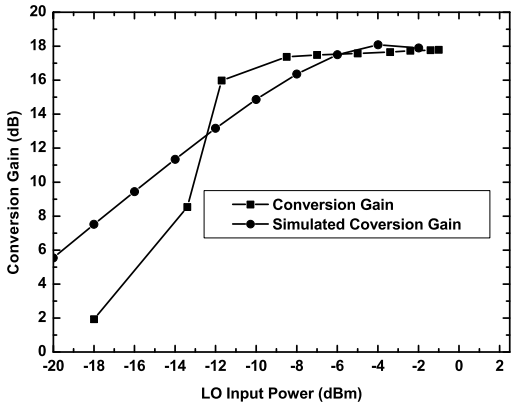

Fig. 9. Measured and simulated conversion gain with respect to LO power.

Table.I shows a comparison between the presented receiver and the recently published sub-THz receivers. One can see that the conversion gain and the noise figure of the presented receiver are comparable to the sub-harmonic topology. It is not straight forward to compare the different receivers because they exhibit different architectures and integration level.

V. CONCLUSION

A direct conversion 240 GHz IQ receiver has been demonstrated in 0.13 μm SiGe BiCMOS technology. The use of low loss IQ generation network along side with LO buffers enabled the implementation of 240 GHz direct conversion fundamental mixer. To the authors best knowledge this is the first fundamental IQ receiver above 180 GHz. The presented receiver exhibits an 18 dB of conversion gain and a 3 dB bandwidth of 25 GHz. It shows excellent amplitude an phase imbalance of 0.5 dB and 3° respectively. By the means of gain control, the receiver shows a dynamic range of more than 36 dB. Those performance metrics, make it ideal for high speed communication with data rate exceeding 20 Gbps.

REFERENCES

[1] B. Heinemann, et. al., "SiGe HBT technology with ft/fmax of 300GHz/500GHz and 2.0 ps CML gate delay," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, 2010.

[2] E. Ojefors, B. Heinemann, and U. R. Pfeiffer, "Subharmonic 220- and 320-GHz sige HBT receiver front-ends," *IEEE Trans. Microw. Theory Tech.*, vol. 60, no. 5, pp. 1397–1404, 2012.

[3] Y. Zhao, E. Ojefors, K. Aufinger, T. F. Meister, and U. R. Pfeiffer, "A 160-GHz subharmonic transmitter and receiver chipset in an SiGe HBT technology," *IEEE Trans. Microw. Theory Tech.*, to be published, early Access.

[4] J.-D. Park, S. Kang, S. V. Thyagarajan, E. Alon, and A. M. Niknejad, "A 260 GHz fully integrated CMOS transceiver for wireless chip-to-chip communication," in *Proc. Symp. VLSI Circuits (VLSIC)*, 2012, pp. 48–49.

[5] Y. Mao, K. Schmalz, J. Borngraber, and J. C. Scheytt, "A 245 GHz CB LNA and SHM mixer in SiGe technology," in *Proc. IEEE 12th Topical Meeting Silicon Monolithic Integrated Circuits in RF Systems (SiRF)*, 2012, pp. 5–8.

[6] K. Schmalz, J. Borngraber, B. Heinemann, H. Rucker, and J. C. Scheytt, "A 245 GHz transmitter in SiGe technology," in *Proc. IEEE Radio Frequency Integrated Circuits Symp. (RFIC)*, 2012, pp. 195–198.