

Subject: **SUBSTRATE ISOLATION CHARACTERIZATION REPORT FOR JAZZ BiCMOS PROCESS**

Introduction

The problem of crosstalk in analog mixed-signal integrated circuits is caused by undesired noise signals generated by digital circuitry that travel through conductive substrates. This noise potentially affects the performance of the analog circuit and therefore, isolation structures are required to alleviate its damaging effects.

This report discusses the substrate isolation (or crosstalk) characterization performed on Jazz SCB18 and SBC35 process wafers with various substrate resistivities. The A0020 and A0023 test chips used for this characterization contained various substrate crosstalk reduction structures such as silicon on insulator substrate (SOI), deep N well (DNwell), P+ guard ring contact, N well guard ring contact, deep trench. The frequency characteristics of substrate isolation structures are a function of their vertical and lateral constructions. The vertical construction parameters include substrate resistivity, wafer thickness, DNwell, and substrate backside contact inductance. The lateral construction parameters include the isolation structures between the two circuit blocks, such as P+ guard ring contact, N well guard ring contact, and deep trench.

Characterization Data Summary and General Guideline for Substrate Isolation

The results of the isolation characterization are provided as a set of techniques for substrate crosstalk reduction:

- a). Adding P+ or N+ guard ring contacts to the noisy circuit block is the most efficient technique to reduce substrate crosstalk. The P+ guard ring contact can effectively eliminate the surface noise current flow at low cost.
- b). Triple well (DNwell) isolation provides even higher isolation from crosstalk and is also insensitive to substrate resistivity. However, the triple well process increases the process complexity and cost.
- c). Using the P+ guard ring contact to surround the circuit block to be isolated.
- d). Due to its lower sheet resistivity, the N+/Nwell guard ring provides higher isolation than P+/Pwell guard ring at frequencies larger than 0.5GHz. The P+/Pwell guard ring

provides better isolation at low frequencies due to the lack of a P+/Pwell to P substrate PN junction.

e). SOI process improves isolation slightly.

f). Deep trench improves isolation slightly.

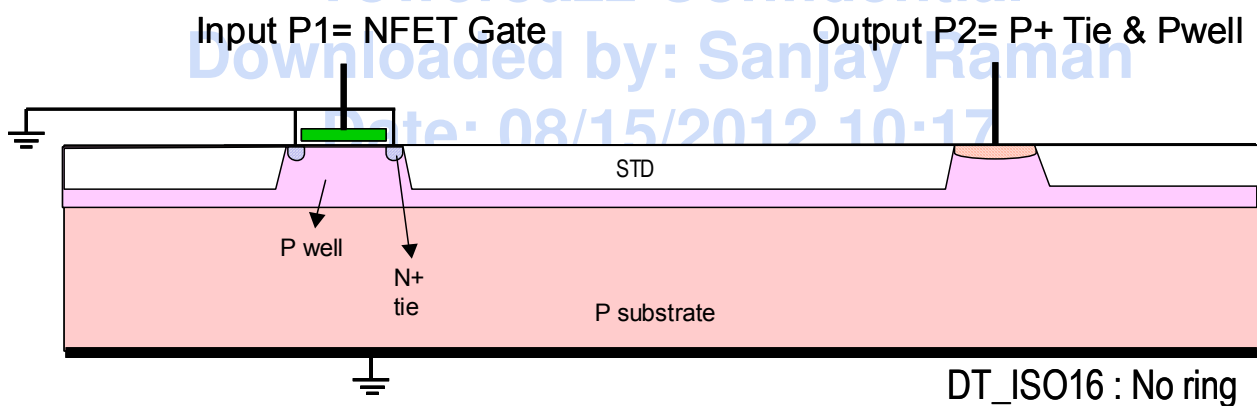
g). High resistivity substrate can provide better isolation. However, the P+ guard ring contact structure only slightly increased isolation for high resistivity substrate.

Test Structures

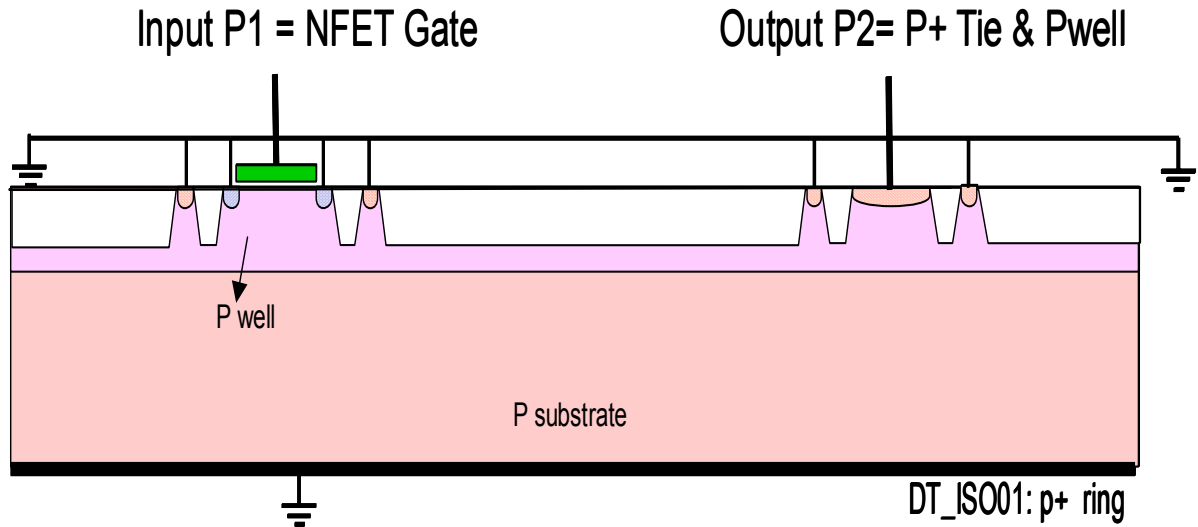
Following are the illustrations of the test structures:

- Source signal is applied to a 50um x 50um NFET gate with source/drain tied to ground
- Sense signal is obtained from 50um x 50um p+ tie to pwell
- Distance between source FET active and sense p+ active = 100um
- Distance between source/sense active to inner p+ substrate tie = 10um
- Standard GSG pad configuration

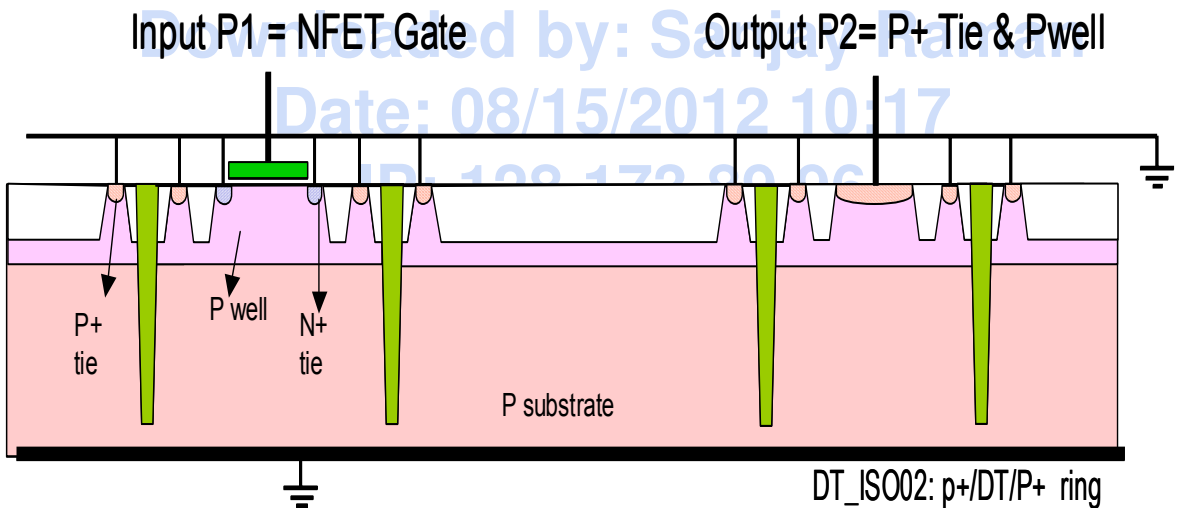
1). No isolation ring between input and output



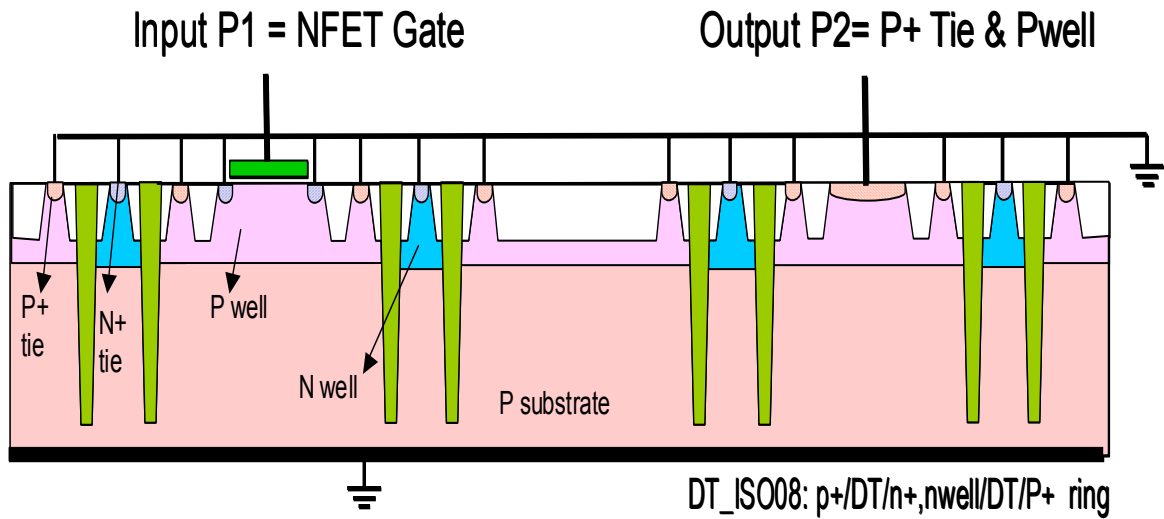
2). P+ guard ring surrounding input and output.



3). P+ guard ring/Deep trench/ P+ guard ring surrounding input and output.

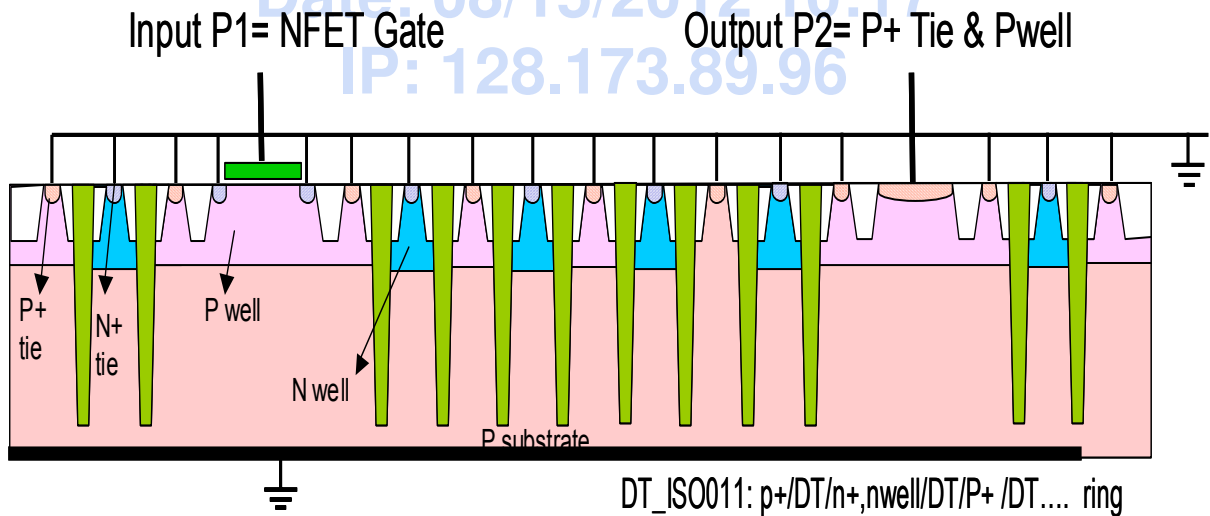


4). Double P+ guard ring/Deep trench/ P+ guard ring surrounding input and output



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5). Filled P+ guard ring/Deep trench/ P+ guard ring between input and output



Measurement Data Summary.

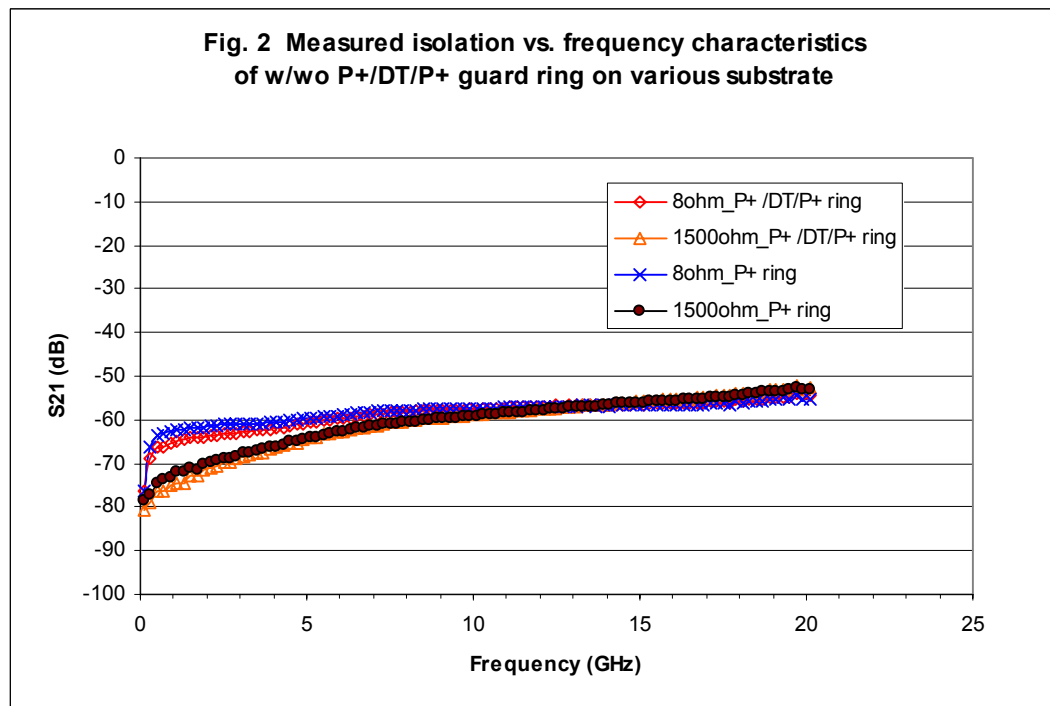
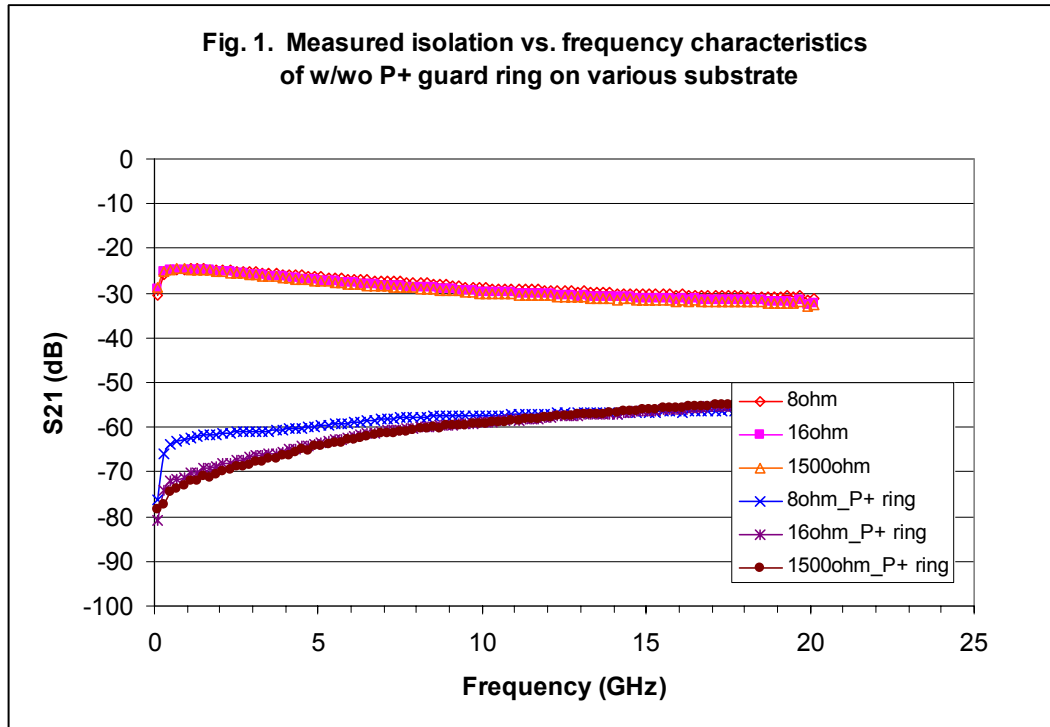


Fig. 3. Measured isolation vs. frequency characteristics of w/wo filled P+/DT/P+ guard ring on various substrate

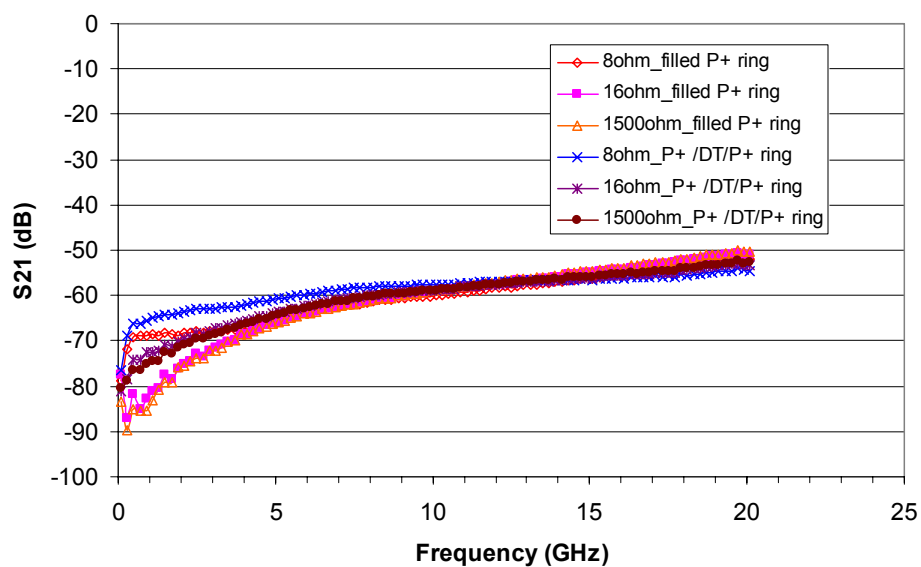
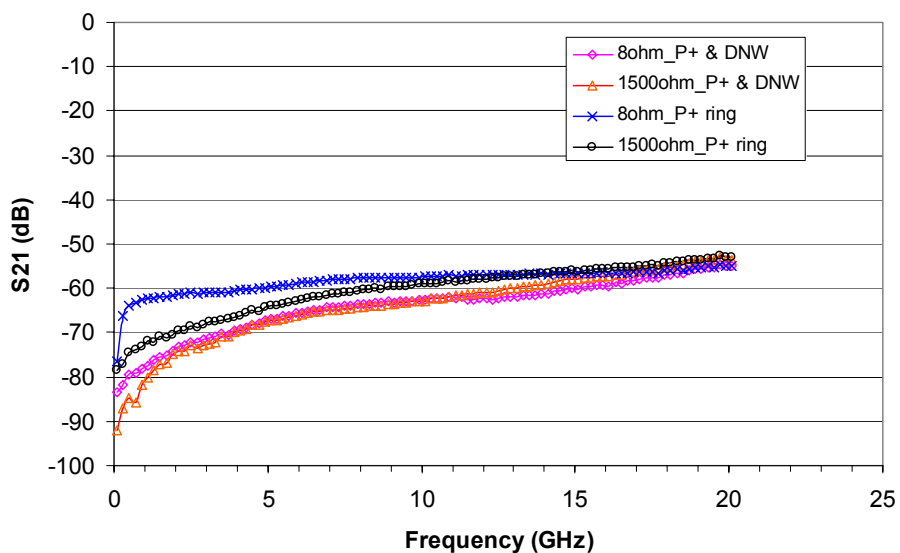
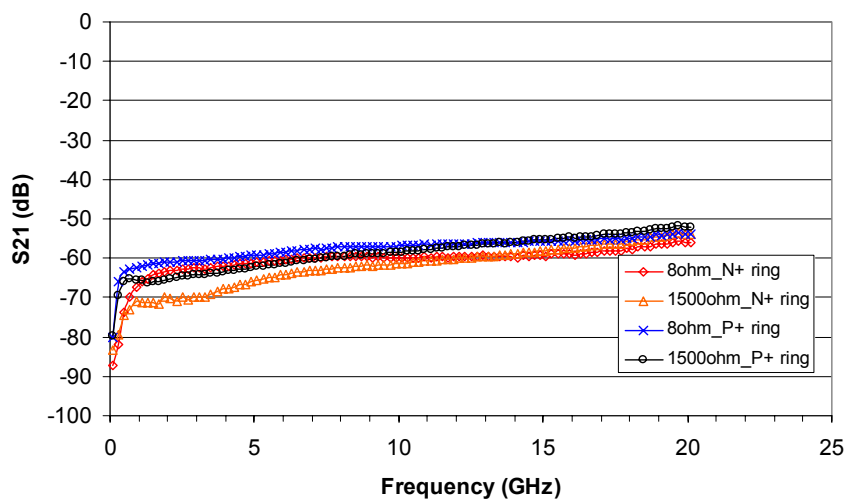


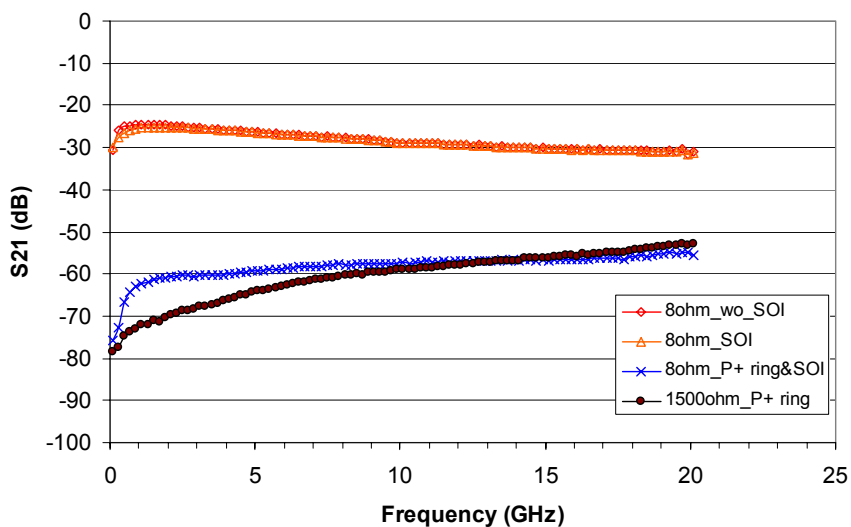
Fig. 4. Measured isolation vs. frequency characteristics of w/wo DNWell on various substrate



**Fig. 5. Measured isolation vs. frequency characteristics
comparson of N+ and P+ guard ring on various substrate**



**Fig. 6. Measured isolation vs. frequency characteristics
of w/wo SOI and w/wo P+ ring**





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