

Jazz Semiconductor

SBC18 Design Manual

SBC18HA/ SBC18HX/ SBC18HK/ SBC18HXL/ SBC18HKL/ **SBC18H2/**
SBC18H2A/ SBC18H3/ SBC18H3A/ SBC18PT/ SBC18PTD/ SBC18PTH/
SBC18QB/ SBC18QPA/ SBC18QTD/ SBC18QTE/ SBC18QTR/ SBC18QTL/
SBC18QW/ SBC18MW/ SBC18MWD/ SBC18MV

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Revision Number	Revision Description	Date
01	Initial release under the QSI document management system: document number NPB PS-0288. For information regarding previous revisions, please contact the document authors.	09/26/02
02	Added Component List and Description to introduction section. Updated all npn model verification plots in section 4.2.	12/20/02
03	3.4 Added RF CMOS Ft vs. Id Plots 4.2 Updated model verification data to reflect npn model changes 5.4 Added PNP model verification plots 6.2 Updated model verification data to reflect inductor model changes 7.3 Added Varactor model verification plots 8.2 Updated model verification data to reflect resistor model changes 9.1 Added Capacitor verification plots	03/24/03
04	Merged with document NPB PS-0289, NPB PS-0290, NPB PS-0309, and NPB PS-0387 to add SBC18PT, SBC18QTD, SBC18QTR, SBC18QW and SBC18MW processes, respectively. Obsoleted documents NPB PS-0289, NPB PS-0290, NPB PS-0309, and NPB PS-0387. Added SBC18HXL, SBC18PTX, SBC18QTL, SBC18MWD processes. 1 Added SBC18 device list table 1 Updated Model list and description table 4.4 Updated list of NPNs offered 4.5 Added NPN Mismatch Data 4.5 Updated NPN Noise figure plots 9.1 Added SBC18 capacitor type table 5.2 Added vertical PNP model 7.2 Expanded P+/Nwell varactor documentation	07/21/03
05	Added SBC18MV process 2.5.1 Corrected low voltage CMOS gate length values in table 7 5.1.2 Added vertical and lateral pnp temperature verification plots 7.1.4 Added Buried Layer and P+/Nwell varactor model scalability plots 7.1.-2 Updated table 1 and 2 to reflect recent Espec adjustments 8.2.2 Added resistor flicker noise sub section 8.2.1 Added additional TiN resistor mismatch plot 9.2 Updated poly capacitor CV curve plots 10.1-2 Updated Schottky Diode sub circuit and IV model verification plots.	10/07/03

06	<p>Completely re-wrote CMOS chapters 2 and 3 to account for new scalable model.</p> <p>Completely re-wrote Varactor chapter 7, including documentation for new MOS varactor available to SBC18HX, SBC18HXL, and SBC18PTX.</p> <p>Expanded corner model sections of each device chapter</p> <p>Added ndiode and pdiode documentation to diode chapter 10.</p>	06/22/04
07	<p>Added section on Statistical NPN Model, reformatted NPN plots.</p> <p>Added Balun Model chapter.</p> <p>Added substrate ring resistance and RF noise model documentation to Chapter 3: RF CMOS Model.</p> <p>Added Appendix A: Additional Model Consideration. This section documents supplemental statistical, corner, and parasitic extraction model behavior.</p> <p>Added device cross sections to each chapter.</p> <p>Updated sub-circuit schematics for all devices.</p> <p>Updated Inductor chapter to be valid for Toolbox 1.4 including new model verification plots.</p> <p>Updated Resistor, Varactor, Capacitor, Inductor, VPNP, and Diode chapters to be more uniform.</p> <p>Added more detailed mismatch sections to Resistor and Capacitor chapters.</p> <p>Added metal option layout descriptions for varactors.</p> <p>Added sbc18hk and sbc18pth process variants to table 1.1</p>	05/27/05
08	<p>Updated device availability list in Chapter 1</p> <p>Added documentation for sbc18ha and sbc18qb processes</p> <p>Updated FET 1/f noise plots to reflect new bsim based models</p> <p>Updated NPN corner and stat model documentation to reflect improved models</p> <p>Improved NPN cross sections</p> <p>Added "known issues" section to NPN chapter</p> <p>Updated Inductor documentation to JIT3, including octagonal models and shields</p> <p>Improved plot quality for resistors, varactors, pnps, capacitors, and diodes</p> <p>Updated junction varactor plots and espec table to reflect model improvements</p> <p>Added improved pc model scalability plots</p> <p>Added Chapter on X-Sigma and Statistical Models</p> <p>Added Chapter on Deep Nwell support</p>	03/31/06

09	<p>Added documentation for sbc18h2 and sbc18hkl processes</p> <p>Added chapter 5: 200GHz SiGe bipolar model (sbc18h2 only)</p> <p>Updated cross sections for capacitor, buried layer varactor, junction varactor, lateral pnp, vertical pnp, and resistor devices.</p> <p>Replaced "Layout Parasitics" section with a unified Appendix chapter. New chapter contains layout parasitics content, Ft simulation test benches, and sbc18h2 device name table.</p> <p>Updated diode device descriptions in Chapter 11 to be consistent with design environment.</p> <p>Updated corner and statistical model tables in CMOS chapter based on new E-specs. and models for narrow channel FETs. No change to NOM model.</p> <p>Updated y-parameter model playbacks in RF CMOS chapter from v6.0 release</p> <p>Design manual release for sbc18 model version 6.1. Please refer to the change history section at the end of each device chapter for a complete listing of model updates.</p>	05/02/07
10	<p>Fixed chapter numbering error for chapters 8 and beyond</p> <p>Fixed incorrect document number on some page footers</p> <p>Added SBC18PTD and SBC18QTE processes</p> <p>Updated NPN Ft and BVceo values, Section 4.1.</p> <p>Updated high speed NPN technology support list, Section 4.1.</p>	05/05/08
11	<p>Rewrote summary of the CMOS Verification Plots</p> <p>In CMOS chapter, updated corner and statistical model tables based on new E-specs, and regenerated the release model quality assurance plots.</p> <p>Restructured the NPN section (Chapter 4) to better align it and the 200GHz NPN section rewriting the descriptions and generating all new plots and tables for the updated models and E-specs.</p> <p>In chapter 5, updated characterization plots, corner and statistical model tables, and the emitter length dependence plot for the low voltage 200GHz NPN.</p> <p>Design manual release for sbc18 model version 6.2 and 6.2a. Please refer to the change history section at the end of each device chapter for a complete listing of model updates.</p> <p>Updated x-sigma corner and statistical model table in Chapter 13.</p>	02/06/09
12	<p>In Section 1.1, corrected capacitor device and model names, added missing H2 device names, clarified npn devices, added differentiation between the 3 and 4 terminal fet devices, removed the asterisk from the passgate devices, corrected capacitor comment on hard-coded.</p> <p>In Section 10.1, corrected table to include rtin_m1.</p> <p>In Section 11.1, corrected table to state that the 5.6fF stacked cap is between M3-M5 and also included a 2fF cap between M4-M5.</p>	12/15/09

13	Added high-frequency chapter, sbc18h3 chapter, 5V fet section to MOSFET chapter, and High-performance PNP section in the PNP chapter. Edited MIM chapter to reflect most recent model. Edited device names to match the most recent gte-based kit.	8/17/11
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1.0 Introduction

This document is intended to serve as a design guide for SBC18, the TowerJazz 0.18um SiGe BiCMOS process family. Please refer to the following SBC18 core technology documents for additional information about the SBC18 process definitions and its variants:

NPB PS-0179	Design Rules
NPB PS-0237	Electrical Specifications
NPB PS-0402	Digital Design Manual
NPB PS-0411	ESD Design Manual
NPB PS-0542	Design Application Note for SBC18H2
NPB PS-1017	Design Application Note for the SBC18H3 Process

The SBC18 models were verified using Cadence Spectre. Hspice, ADS, and ELDO simulators are also supported in selected processes. Table 1.2 lists the devices available to each SBC18 process variant

TABLE 1.1 SBC18 device list

Devices	HA	HX L	HX	HK	HK L	H2	H2A	H3	H3 A	PT	PT H	PT D	QB	QT D	QT E	QT R	QT L	QP A	QW	MW	MW D	MV
3.3V FETs	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
5V FETs																		X				
1.8V FETs	X	X	X	X	X	X	X	X	X	X	X	X	X					X				
High Speed NPN w/ DT	X	X	X												X							
Standard NPN w/ DT	X	X	X	X	X									X	X	X	X				X	
High Voltage NPN w/ DT	X	X	X	X	X									X	X	X	X				X	
Standard NPN w/o DT										X	X	X	X						X	X		X
High Voltage NPN w/o DT										X	X	X	X						X	X		X
8V NPN w/o DT																		X				
200GHz NPN w/ DT (H2)						X	X															
Standard NPN w/ DT (H2)						X	X															
High Speed NPN w/ DT (H3)								X	X													
Standard NPN w/ DT (H3)								X	X													
Lateral PNP	X	X	X	X	X		X	X	X	X	X	X	X	X	X	X	X		X	X	X	X
Vertical PNP	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		X	X	X	X
High Performance PNP												X										
Low Value Poly Resistor	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
High Value Poly Resistor	X					X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Salicided Poly Resistor	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
TiN Resistor	X	X	X	X	X	X	X	X	X							X		X				
Nwell Resistor	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		X	X	X	X
Varactor (ni)																			X	X		
Varactor (buried layer)	X	X	X				X			X	X	X		X	X	X	X				X	X
Varactor (MOS)	X	X	X	X	X	X	X	X	X	X	X	X	X					X				
1fF MIM Cap		X	X	X	X																	
2fF MIM Cap						X	X		X	X	X	X	X	X	X	X	X	X	X	X	X	X

TABLE 1.1 SBC18 device list

Devices	HA	HXL	HXL	HK	HKL	H2	H2A	H3	H3A	PT	PTH	PTD	QB	QTD	QTE	QTR	QTL	QPA	QW	MW	MWD	MV
4fF Stack MIM Cap							X		X	X	X	X	X						X			
2.8fF MIM Cap	X							X		X												
5.6fF Stack MIM Cap	X							X														
Schottky Diode	X	X			X		X	X	X			X				X						
Deep Nwell	X	X			X	X	X	X			X	X					X	X				

1.1 SBC18 Model List and Description

For a complete listing of sbc18 process variant devices please refer to the Jazz Design Kit “Virtual Components Website available through the Cadence **CIW** -> **Technology Component Info (VCSC Web)**, or by navigating to [\\$RDS_ROOT/amslibs/cds_default/cdsware/html/index.html](#)

SiGe NPNs:

- npn (nnp, 4-terminal, sub-circuit model name based on geometry)
- type “L” is for HS (High-speed) with $BV_{CEO}=2.2V$ (In SBC18H2 type “L” is for Low Voltage with $BV_{CEO}=1.9V$ and in SBC18H3 type “L” is for Low Voltage with $BV_{CEO} = 1.6V$). In the legacy PDKs this device starts with “D”.
- type “M” is for STD (Standard) with $BV_{CEO}=3.2V$ (In SBC18H2 and H3 type “M” is for Medium Voltage with $BV_{CEO}=3.5V$). In the legacy PDKs this device starts with “L”.
- type “H” is for HV (High Voltage) with $BV_{CEO}=6.0V$. This device is not available in SBC18H2 or SBC18H3.

FETs:

- nfet (analog nfet, thin oxide, 4-terminal, implicit bulk terminal, sub-circuit model nfets)
- nfet_4 (analog nfet, thin oxide, 4-terminal, explicit bulk terminal, sub-circuit model nfets)
- pfet [pfet⁺] (analog pfet, thin oxide, 4-terminal, implicit bulk terminal, sub-circuit model pfets)
- pfet_4 (analog pfet, thin oxide, 4-terminal, explicit bulk terminal, sub-circuit model pfets)
- nfet3p3 (analog nfet, 3.3V thick oxide, 4-terminal, implicit bulk terminal, sub-circuit model n3p3fets)
- nfet3p3_4 (analog nfet, 3.3V thick oxide, 4-terminal, explicit bulk terminal, sub-circuit model n3p3fets)
- pfet3p3 (analog pfet, 3.3V thick oxide, 4-terminal, implicit bulk terminal, sub-circuit model p3p3fets)
- pfet3p3_4 (analog pfet, 3.3V thick oxide, 4-terminal, explicit bulk terminal, sub-circuit model p3p3fets)
- nfet5p0 (analog nfet, 5V thick oxide, 4-terminal, implicit bulk terminal, sub-circuit model n5p0fets)
- nfet5p0_4 (analog nfet, 5V thick oxide, 4-terminal, explicit bulk terminal, sub-circuit model n5p0fets)
- pfet5p0 (analog pfet, 5V thick oxide, 4-terminal, implicit bulk terminal, sub-circuit model p5p0fets)
- pfet5p0_4 (analog pfet, 5V thick oxide, 4-terminal, explicit bulk terminal, sub-circuit model p5p0fets)

- nfet_rf (RF nfet, thin oxide, 4-terminal, sub-circuit model nfet_rf)
- pfet_rf (RF pfet, thin oxide, 4-terminal, sub-circuit model pfet_rf)
- nfet3p3_rf (RF n3p3fet, 3.3V thick oxide, 4-terminal, sub-circuit model n5p0fet_rf)
- pfet3p3_rf (RF p3p3fet, 3.3V thick oxide, 4-terminal, sub-circuit model p5p0fet_rf)
- nfet5p0_rf (RF n3p3fet, 5V thick oxide, 4-terminal, sub-circuit model n5p0fet_rf)
- pfet5p0_rf (RF p3p3fet, 5V thick oxide, 4-terminal, sub-circuit model p5p0fet_rf)

Junction Diodes:

- dn (n+/sub junction diode, thin oxide, 2-terminal, primitive model ndiode)
- dp (p+/well junction diode, thin oxide, 2-terminal, primitive model pdiode)
- dnwell (nwell/substrate diode, 2-terminal, primitive model nwdiode)
- dn3p3 (n+/sub junction diode, thick oxide, 2-terminal, primitive model n3p3diode)
- dp3p3 (p+/well junction diode, thick oxide, 2-terminal, primitive model p3p3diode)
- dschottky (Schottky diode devices, primitive model schottky)
- diso (Deep Nwell/Nwell to isolated Pwell diode, model dnw_pwell)
- ddnw (Deep Nwell to P substrate diode, model dnw_psub)
- dpin (PiN diode, model dpin)

Resistors:

- rnwell (nwell resistor, 3-terminal, sub-circuit model rw3t)
- rppoly_lo (low value unsalicated poly resistor, 3-terminal, sub-circuit model rpp3t)
- rppoly_hi (high value unsalicated poly resistor, 3-terminal, sub-circuit model rpp3t)
- rppoly_sal (salicated poly resistor, 3-terminal, sub-circuit model rps)
- rtin (TiNitride resistor, 3-terminal, sub-circuit model rtin)

Capacitors:

- cpoly (poly cap over well, thin oxide, 3-terminal, sub-circuit model pc)
- cpoly3p3 (poly cap over well, 3.3V thick oxide, 3-terminal, sub-circuit model pc3p3)
- cpoly5p0 (poly cap over well, 5V thick oxide, 3-terminal, sub-circuit model pc5p0)
- cmim (1fF/um² mim capacitor over substrate, 3-terminal, sub-circuit model c3t_mim)
- cmim2 (2fF/um² mim capacitor over substrate, 3-terminal, sub-circuit model c3t_mim2)
- cmim2_2 (2fF/um² mim capacitor over substrate, 2-terminal, sub-circuit model c2t_mim2)
- cmim3 (2.8fF/um² mim capacitor over substrate, 3-terminal, sub-circuit model c3t_mim3)

- cmim3_2 (2.8fF/um² mim capacitor over substrate, 2-terminal, sub-circuit model c2t_mim3)
- cmim3_m3 (2.8fF/um² mim capacitor over substrate on metal-3, 3-terminal, sub-circuit model c3t_mim3)
- cmimw23_m3_2 (2.8fF/um² mim capacitor over substrate on metal-3, 2-terminal, sub-circuit model c2t_mim3)
- cmim_2 (1fF/um² mim capacitor over substrate, 2-terminal, sub-circuit model c2t_mim)
- cmimw2_4 (2fF/um² mim capacitor over well, 4-terminal with explicit well terminal, sub-circuit model c4t_mimw2)
- cmimw3_4 (2.8fF/um² mim capacitor over well, 4-terminal with explicit well terminal, sub-circuit model c4t_mimw3)
- cmimw3_m3_4 (2.8fF/um² mim capacitor on over well on metal-3, 4-terminal with explicit well terminal, sub-circuit model c4t_mimw3)
- cmimw_4 (1fF/um² mim capacitor over well, 4-terminal with explicit well terminal, sub-circuit model c4t_mimw)
- csmim4 (4fF/um² stacked mim capacitor over substrate, 3-terminal, sub circuit model c3t_smim6)
- csmimw4_4 (4fF/um² stacked mim capacitor over nwell, 4-terminal with explicit well terminal, sub circuit model c4t_smim6)
- csmim6 (5.6fF/um² stacked mim capacitor over substrate, 3-terminal, sub circuit model c3t_smim6)
- csmimw6_4 (5.6fF/um² stacked mim capacitor over nwell, 4-terminal with explicit well terminal, sub circuit model c4t_smim6)

PNPs:

- vpnnp: vertical npnp (25x25), pnpb (11x11), pnpd (5.4x5.4), pnpd (3x3) (3-terminal, primitive model)
- vpnphp (high performance vertical pnp, 4-terminal)
- lpnp (lateral pnp transistor, sub-circuit model pnpl)

Varactors:

- var_bl (implanted varactor, 3-terminal, sub-circuit model rfvar_bl)
- var_mos (MOS varactor 1.8V gate, 3-terminal, sub-circuit model mosvar_1p8)

Inductors:

- ind (top metal square inductor, 3-terminal, sub-circuit model ind_[1,3,5]u)
- ind_diff (top metal differential square inductor, 4-terminal, sub-circuit model inddiff_[1,3,5]u)
- ind_oct (top metal octagonal inductor, 3-terminal, sub-circuit model ind_[1,3,5]u)
- ind_diff_oct (top metal differential octagonal inductor, 4-terminal, sub-circuit model inddiff_[1,3,5]u)

Baluns:

- balun (balun device, 6-terminal, sub-circuit model dependent on process variant)
- balun_xfmr (balun in transformer configuration, 4-terminal, sub-circuit model dependent on process variant)

Fuse:

- fuse (metal fuse, 2-terminal, sub-circuit resistor model fuse)
- efuse (poly fuse, 2-terminal, sub-circuit resistor model efuse)

ESD FETs

- nfet_esd (esd nfet with well resistor and guard ring, schematic based)***
- pfet_esd (esd pfet with guard ring, schematic based)***
- n3p3fet_esd (esd n3p3fet with well resistor and guard ring, schematic based)
- p3p3fet_esd (esd p3p3fet with guard ring, schematic based)***

***For ESD guidelines please refer to document NPB PS-0411

1.2 Model Availability

The following model types are available for each SBC18 device:

TABLE 1.2 Model availability table for SBC18 variants

Device	DC	AC	RF	Noise	Corner	Statistical	Mismatch
CMOS	x	x	x	x	x	x	x
NPN	x	x	x	x	x	x	x
Lateral PNP	x	x		x	x	x	
Vertical PNP	x	x			x	x	
High Performance PNP	x	x	x		x	x	
Unsalicided Poly Resistor (low and high value)	x	x	x	x	x	x	x
Salicided Poly Resistor	x	x	x		x	x	x
Metal (TiN) Resistor	x	x	x		x	x	x
Nwell Resistor	x	x			x	x	
MIM Capacitors		x	x		x	x	x
Poly Capacitor		x			x	x	
Buried Layer Varactor	x	x	x		x	x	
P+/Nwell Varactor	x	x	x		x	x	
MOS Varactor	x	x	x		x	x	
Junction Diodes	x	x			x	x	
Schottky Diode	x	x	x		x	x	
Inductors	x	x	x		x	x	x

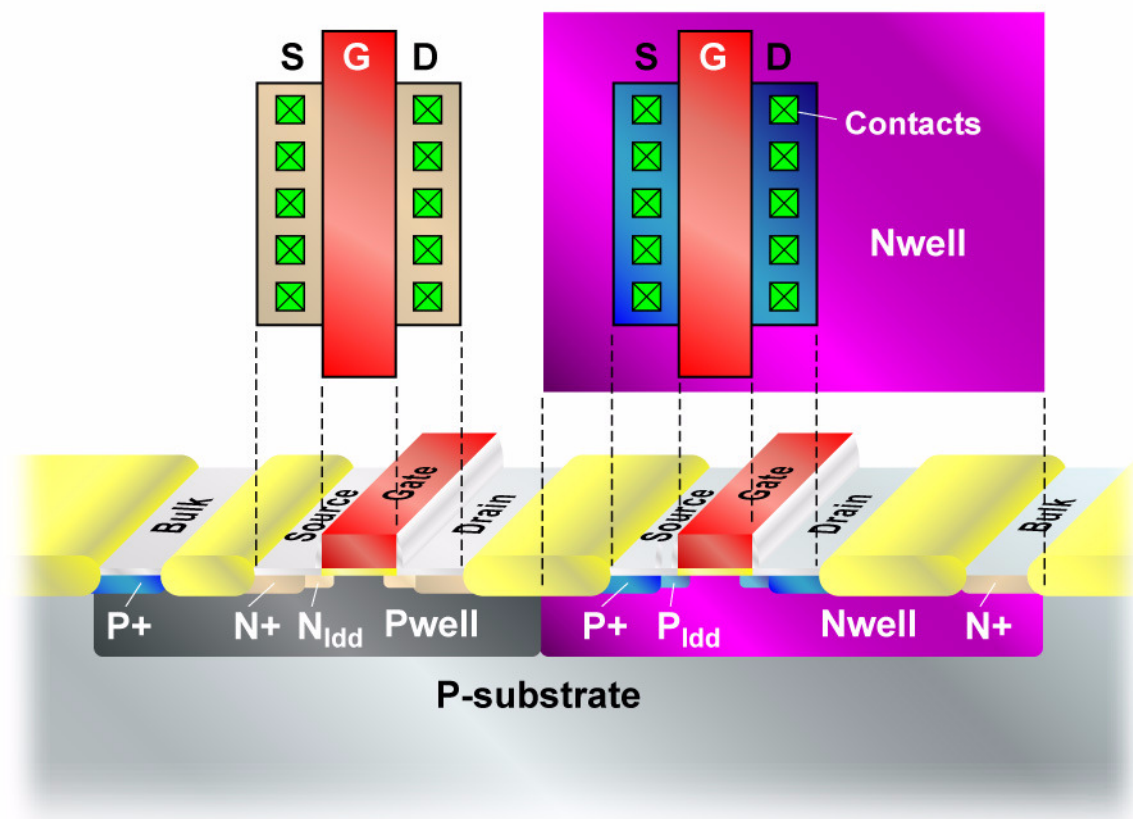
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2.0 MOS MODEL

2.1 Device Description

The SBC18 process supports two different mixed-signal (MS) models. The first model relates to the thin gate-oxide FETs with a maximum operation voltage of 1.8v. The second model relates to the thick gate-oxide FETs with a maximum operation voltage of 3.3V (5.0V for sbc18qpa). The cross section and top view of a typical SBC18 1.8v CMOS section is illustrated in Figure 2.1.

FIGURE 2.1 NFET and PFET cross section and top view



2.2 Model description

TABLE 2.1 Model summary for Fets

Property	1.8v Fets	3.3v FETs	5.0v FETs
Design Kit Cell Name	nfet, pfet	n3p3fet/nfet3p3, p3p3fet/pfet3p3	nfet5p0, pfet5p0
Temperature Range	-40 to 125°C	-40 to 125°C	-40 to 125°C
Channel Length	0.18µm ≤ L ≤ 100µm	0.36µm ≤ L ≤ 100µm for NFET 0.30µm ≤ L ≤ 100µm for PFET	0.60µm ≤ L ≤ 150µm
Channel Width	0.22µm ≤ W ≤ 250µm	0.40µm ≤ W ≤ 250µm	0.60µm ≤ W ≤ 250µm
No. of fingers	1 ≤ NF ≤ 100	1 ≤ NF ≤ 100	1 ≤ NF ≤ 100
Bias Range	Vgs : 0 ~ 1.8V, Vds : 0 ~ 1.8V, Vbs : 0 ~ 1.8V	Vgs : 0 ~ 3.3V, Vds : 0 ~ 3.3V, Vbs : 0 ~ 3.3V	Vgs : 0 ~ 5.0V, Vds : 0 ~ 5.0V, Vbs : 0 ~ 5.0V

Using these models outside of the specified ranges may generate simulation errors.

2.3 Scalable model

A completely scalable BSIM3v3 model was used to fit devices of all geometries. A limited set of model parameters were made geometry dependent to improve model accuracy, as per the equation inside BSIM3v3:

$$P = P0 + \frac{LP}{L_{eff}} + \frac{WP}{W_{eff}} + \frac{PP}{(L_{eff} \times W_{eff})} \quad (\text{EQ 1})$$

where P is the effective parameter value, with P0, LP, WP, and PP defining the geometric dependencies of the parameter.

A scalable model is highly desirable as it maintains the “physical” nature of the model. Parameters such as DVT0, that define the short channel threshold voltage behavior of a MOSFET, are physically extracted. In contrast to the scalable modeling approach, the “binned” model methodology divides the channel length and width space into multiple “bins” and model parameter sets for each of the bins are independently extracted. Eq. 1 is used to make the model parameters continuous across bin boundaries. Parameters such as DVT0 have no physical meaning. A significant advantage of the scalable model approach is in the corner and statistical modeling. These models are generated by changing process specific model parameters such as mobility and channel length, and are intuitively more accurate if the original model was physically extracted.

A PSP model option is also available via the Jazz model selection form. In general, the PSP model provides a more accurate description of the measured data, but due to its relatively new introduction the BSIM option continues to be the default model for the SBC18 design kit. As such, all subsequent model validation plots refer to the model playbacks using the BSIM option.

2.3.1 “Golden” die selection

A rigorous Quality Assurance (QA) methodology was used to select the “golden” die on which detailed measurements are performed and the model parameters extracted. Electrical specifications (E-spec) such as threshold voltage, saturation current, body constant were measured over multiple die to select the die closest to the E-spec of the technology. The geometry dependence of these parameters was also plotted to ensure a clean set of measurements. The following checklist encompasses the measured data QA:

TABLE 2.2 Measured data QA checklist

Critical parameters (Idsat for the small and short device, Vth for the 4 corners large, narrow, short, and small) vs. Electrical Specifications within 5%
Plot Vth vs. Length and Width
Plot Vth vs. Temperature for large device
Plot Idsat vs. Length and Width
Plot Idsat vs. Temperature for short channel device
Plot Body constant vs. Length and Width
Plot Body constant vs. Temperature
Plot subthreshold slope (ST) vs. L and W

Any inconsistencies observed during the QA procedure results in either the deletion of the relevant measured data point or a physical re-measurement of that parameter or sweep.

2.3.2 Thin gate-oxide model parameter extraction devices:

Thin gate-oxide device were measured using the Agilent IC-CAP characterization and modeling software.

Table 2.3 on page 19 lists the devices that were measured at 25C, 125C and -40C.

TABLE 2.3 List of sizes of the measured thin-oxide N and P FETs

W=10u	L=0.18, 0.2, 0.22, 0.25, 0.3, 0.4, 0.6, 1, 2, 10um	Large W, Scale channel length
L=10um	W=0.22,0.3,0.4,0.6,1, 2u	Large L, Scale channel width
W=0.22um	L=0.18, 0.2um	Small devices
L=0.18um	W=0.3,0.4um	Minimum L, scale channel width

Table 2.4 on page 19 lists the various characteristics measured for each of the FETs listed in Table 2.3 on page 19.

TABLE 2.4 List of measured characteristics for thin-oxide FETs

Characteristic	Type	V _{DS} (V)	V _{GS} (V)	V _{BS} (V)
Id Vs. Vgs	Threshold -Linear	0.05	-0.5 to 1.8, 50mV steps	0 to -1.5, in -0.3V steps
Id Vs. Vgs	Threshold -Saturation	1.8	-0.2 to 1.8, 50mV steps	0 to -1.5, in -0.3V steps
Id Vs. Vds	Output	0 to 1.8V, 50mV steps	0.6 to 1.8V, 0.3 V steps	0
Id Vs. Vds	Output with back bias	0 to 1.8V, 50mV steps	0.6 to 1.8V, 0.3 V steps	-1.5

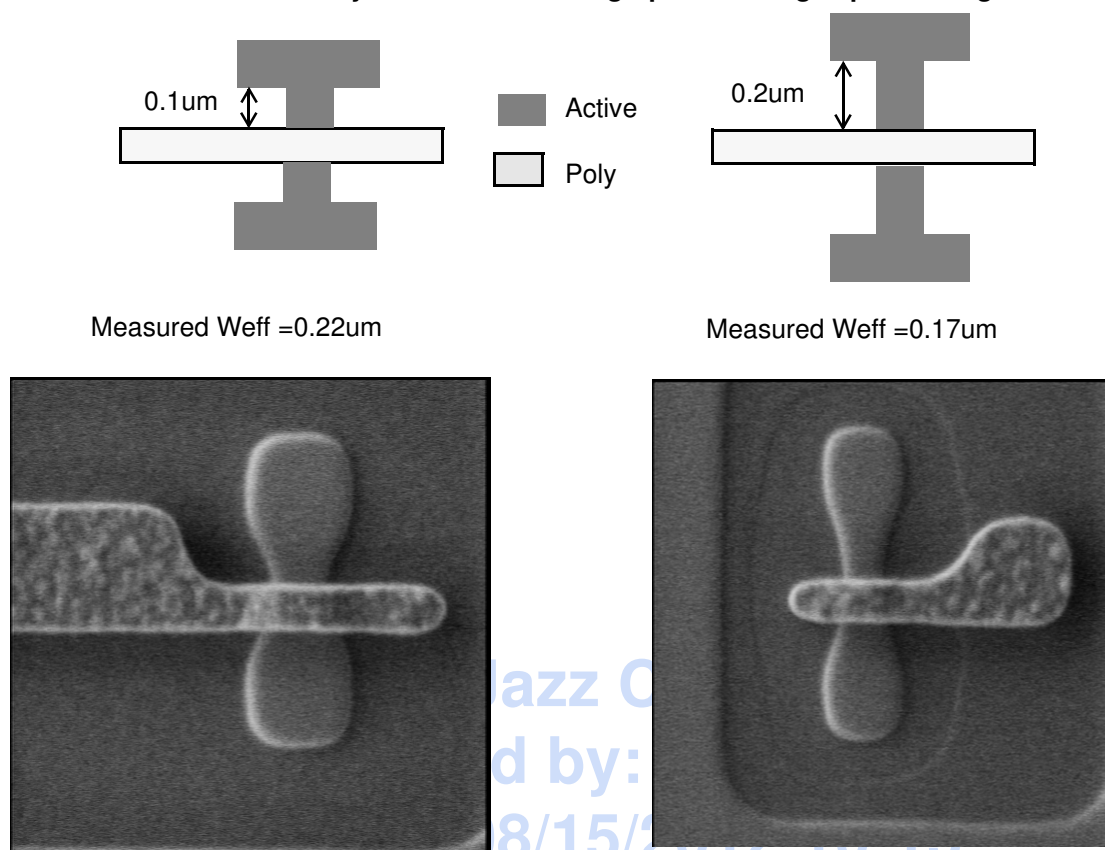
2.3.3 Dog-bone effect for thin gate-oxide devices

The SBC18 design rules allow a minimum drawn standard FET width of 0.22μm. FETs with W smaller than 0.42μm require a dog-bone layout to make contact with the source/drain regions. The effective width of the narrow FETs (W < 0.42μm) increases as a result of the dog-bone layout. This effect is dominant for small channel lengths (L < 0.6μm). To account for the increase in Weff, ΔW was gradually reduced for dog-boned FETs for small channel lengths by using the BSIM3v3 parameters WL and WW in Eq. 2:

$$\Delta W = WINT + \frac{WL}{L^{WLN}} + \frac{WW}{W^{WLN}} + \frac{WWL}{L^{WLN} \times W^{WLN}} \quad (\text{EQ 2})$$

SEM micrographs of the small device (W/L=0.22/0.18um) with varying active-shoulder edge to gate-poly edge spacing are shown in Figure 2.2. The impact of shrinking the gate-poly edge to active edge spacing from 0.2μm to the minimum design rule can be clearly seen in the measured Weff values that increase from 0.17μm to 0.22μm. This can result in a large spread in the measured values of the saturation current (Idsat) for these devices. These are captured in the corner E-specs of this parameter for the small devices.

No dog-bone layout is required for thick-oxide FETs, even with minimum channel width of 0.4μm.

FIGURE 2.2 Schematic of layout and SEM micrographs showing impact of dog-bone on Weff.**2.3.4 Thick gate-oxide (3.3V) model parameter extraction devices:****TABLE 2.5** List of sizes of the measured thick-oxide (3.3V) N & P FETs

NFET		
W=10um	L=0.36, 0.38, 0.42, 0.5, 0.6, 0.8, 1, 2, 10um	Large W, Scale channel length
L=10um	W=0.4, 0.5, 0.6, 1, 2um	Large L, Scale channel width
W=0.4um	L=0.36, 0.38, 0.42um	Small devices
L=0.36um	W=0.5, 0.6um	Minimum L, scale channel width
PFET		
W=10um	L=0.3, 0.32, 0.36, 0.42, 0.5, 0.6, 0.8, 1, 2, 10um	Large W, Scale channel length
L=10um	W=0.4, 0.5, 0.6, 0.8, 2um	Large L, Scale channel width
W=0.4um	L=0.32, 0.36um	Small devices
L=0.3um	W=0.5, 0.6um	Minimum L, scale channel width

Thick gate-oxide device were measured using the Agilent IC-CAP characterization and modeling software. Table 2.5 on page 20 lists the devices that were measured at 25C, 125C and -40C. Table 2.6 on page 21 lists the various characteristics measured for each of the FETs listed in Table 2.3 on page 19.

TABLE 2.6 List of measured characteristics for thick-oxide (3.3V) FETs

Characteristic	Type	V_{DS} (V)	V_{GS} (V)	V_{BS} (V)
Id Vs. Vgs	Threshold - Linear	0.05	0 to 3.3, 100mV steps	0 to -3, in -0.6V steps
Id Vs. Vgs	Threshold - Saturation	3.3	0 to 3.3, 100mV steps	0 to -3, in -0.6V steps
Id Vs. Vds	Output	0 to 3.3V, 100mV steps	0.55 to 3.3V, 0.55 V steps	0
Id Vs. Vds	Output with back bias	0 to 3.3V, 100mV steps	0.55 to 3.3V, 0.55 V steps	-3

2.3.5 Thick gate-oxide (5.0V) model parameter extraction devices:

TABLE 2.7 List of sizes of the measured thick-oxide (5.5V) N & P FETs

NFET		
W=10um	L= 0.6, 0.7, 0.8, 0.9, 1.4, 1.9, 9.9 um	Large W, Scale channel length
L=9.9um	W = 0.6, 0.8, 1.2, 2, 10 um	Large L, Scale channel width
W x L	0.6 x 0.7, 0.7 x 0.7 um	Small Devices
L=0.6um	W = 10 um	Minimum L, scale channel width
PFET		
W=10um	L= 0.6, 0.7, 0.8, 0.9, 1, 1.5, 2, 10 um	Large W, Scale channel length
L=10um	W = 0.6, 0.8, 1, 1.2, 2, 10 um	Large L, Scale channel width
W x L	0.6 x 0.6, 0.7 x 0.8, 0.8 x 0.6 um	Small devices
L=0.6um	W = 0.6, 0.8, 1.2, 10	Minimum L, scale channel width

Thick gate-oxide device were measured using the Agilent IC-CAP characterization and modeling software. Table 2.7 on page 21 lists the devices that were measured at 25C, 125C and -40C. Table 2.8 on page 21 lists the various characteristics measured for each of the FETs listed in Table 2.3 on page 19.

TABLE 2.8 List of measured characteristics for thick-oxide (5.5V) FETs

Characteristic	Type	V_{DS} (V)	V_{GS} (V)	V_{BS} (V)
Id Vs. Vgs	Threshold - Linear	0.05	0 to 5, 50mV steps	0 to -4, in -0.8V steps
Id Vs. Vgs	Threshold - Saturation	5	0 to 5, 50mV steps	0 to -4, in -0.8V steps
Id Vs. Vds	Output	0 to 5V, 50mV steps	1 to 5V, 1 V steps	0
Id Vs. Vds	Output with back bias	0 to 5V, 50mV steps	1 to 5V, 1 V steps	-4

2.4 Parameter Extraction

2.4.1 IV parameters

BSIM3v3.2 model parameters were physically extracted using BSIM3 Modeling Package [1, 2]. Local optimization of selected parameters to the appropriate regions of the measured device characteristics was performed to better fit the measured data. RMS fitting errors were typically less than 1% on the I_D - V_{DS} curves and less than 3% on the g_{out} - V_{DS} curves. Maximum fitting errors were typically less than 3% on the I_D - V_{DS} curves and less than 15% on the g_{out} - V_{DS} curves. RMS fitting errors were typically less than 1% on the I_D - V_{GS} curves and less than 2% on the g_m - V_{GS} curves. Maximum fitting errors were typically less than 3% on the I_D - V_{GS} curves and less than 5% on the g_m - V_{GS} curves.

The temperature dependence of the model parameters was captured by using the relevant BSIM3v3 parameters to fit the measured data at -40C and 125C. The large channel threshold voltage in the linear and saturation regions, high field and back bias dependent mobility, the short channel threshold voltage and saturation currents, and the temperature dependence of the series drain/source resistances were fit to the measured data.

2.4.2 Capacitance parameters

Junction capacitances were measured for bottom, field sidewall, and channel sidewall intensive structures. This capacitance was characterized for biases ranging from a small forward bias (0.2v) to a reverse bias equal to 1.8v for the thin-oxide devices and 3.3v for the thick-oxide devices. The measured values were separated into bottom (CJ), field sidewall (CJSW) and channel sidewall components (CJSWG) parameters by simultaneously solving the 3 equations.

The gate oxide capacitance was measured on two large area test structures. The first structure is a MOS capacitor and allows the accumulation and depletion region CV parameters to be extracted. The second structure is a MOS transistor which allows the inversion region CV parameters to be extracted. The gate capacitance was fitted by using CAPMOD=3 model in BSIM3v3.2. This model takes into account quantum mechanical and poly depletion effects. The maximum error in fitting the intrinsic gate capacitances in inversion was less than 3%.

The gate-to-source/drain overlap capacitances and their bias dependencies were measured on very wide multi-finger FETs with 0.18 μ m (for standard devices) or 0.36 μ m (for thick gate-oxide devices) channel lengths. The gate overlap capacitance is a function of both the gate to source/drain bias, and the substrate bias. Only the gate to source/drain bias dependence is currently modeled in BSIM3v3.2.

The accuracy of the extracted capacitance parameters for the thin and thick-oxide FETs was verified by matching the measured delay times of a set of 10 ring-oscillators for each device type. The measured and simulated

delay/stage for various ring-oscillator configurations are shown for the low and high voltage FETs in Table 2.9 on page 23.

TABLE 2.9 Ring oscillator delay/stage.

Transistor	Ring Osc. load	Measured delay/stage (ps)	Simulated delay/stage (ps)
1p8v	No load	44.6	43.5
	2x N-gate	142.0	149.6
	5x N-gate	177.3	183.9
	2x P-gate	153.9	152.9
	5x P-gate	179.8	194.6
3p3v	No load	82.3	80.5
	2x N-gate	204.3	203.0
	5x N-gate	238.6	239.0
	2x P-gate	179.3	202.8
	5x P-gate	244.4	246.3

The model parameter set fitted to the measurements is referred to as the “measured” case.

2.5 CMOS Verification Plots

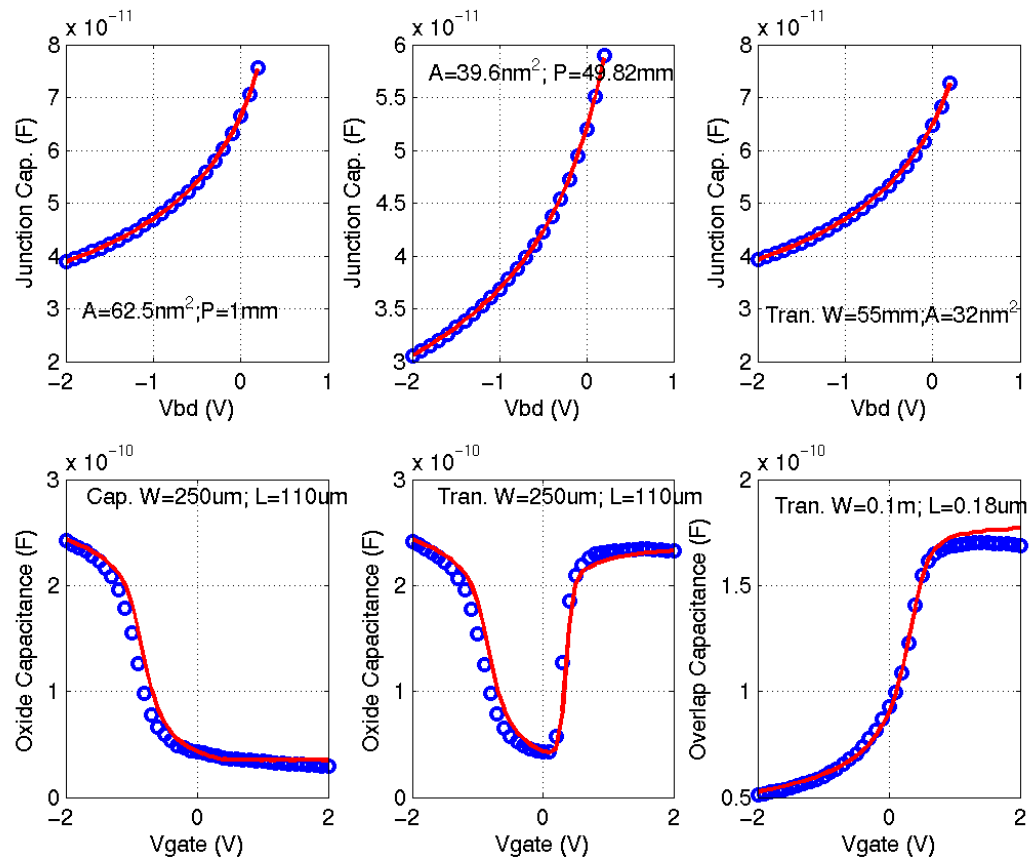
The simulated IV and CV characteristics of the various MOSFETs are compared with the measured data in Figures 2.3 through 2.78. The device description is included in the figure caption and has the format of “max_operating_voltage_fetType_WxL_plotType_temperature”. For e.g. 1p8v_nfet_10x0p18_idvg_25C refers to the Idrain Vs. Vgate characteristic at 25C of a thin oxide NFET with W=10μm and L=0.18μm.

There are 6 different CV plots showing the MOSFET capacitances. The top 3 plots are for junction capacitance from area, perimeter, and perimeter-under-gate intensive structures. The bottom-left plot is for the oxide capacitance from a pure MOS capacitor, where as the bottom-middle plot is the oxide capacitance in a large area MOSFET. Finally, the bottom-right plot is for a large channel width transistor with the bulk floating and captures the overlap capacitance from gate to source/drain.

The IV plots show the threshold and output characteristics of the MOSFET. There are 2 plots to show how the threshold voltage changes with width (top plot) and length (bottom plot) for various body to source voltages ranging from 0V to 1.5V. There are also a set of 6 threshold curve plots, for Id vs. Vgs. in the linear region (top-left), Id vs. Vgs in the saturation region (top-middle), and sub-threshold Id vs. Vgs (top-right). The transconductance in the linear region (bottom left), transconductance in the saturation region (middle-right), and the substrate current vs. gate bias in saturation are shown in the second row. The output curves are a set of 4 plots: Id vs. Vds (top-left), Id vs. Vds with back-bias (top-right), and gds vs. Vds (bottom-left), and gds vs. Vds with back-bias (bottom-right).

Finally, the blue-circles are the measured data, and solid red lines are the BSIM model prediction.

FIGURE 2.3 1p8_nfet_cv_25C



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FIGURE 2.4 1p8v_nfet_vtVsL_25C

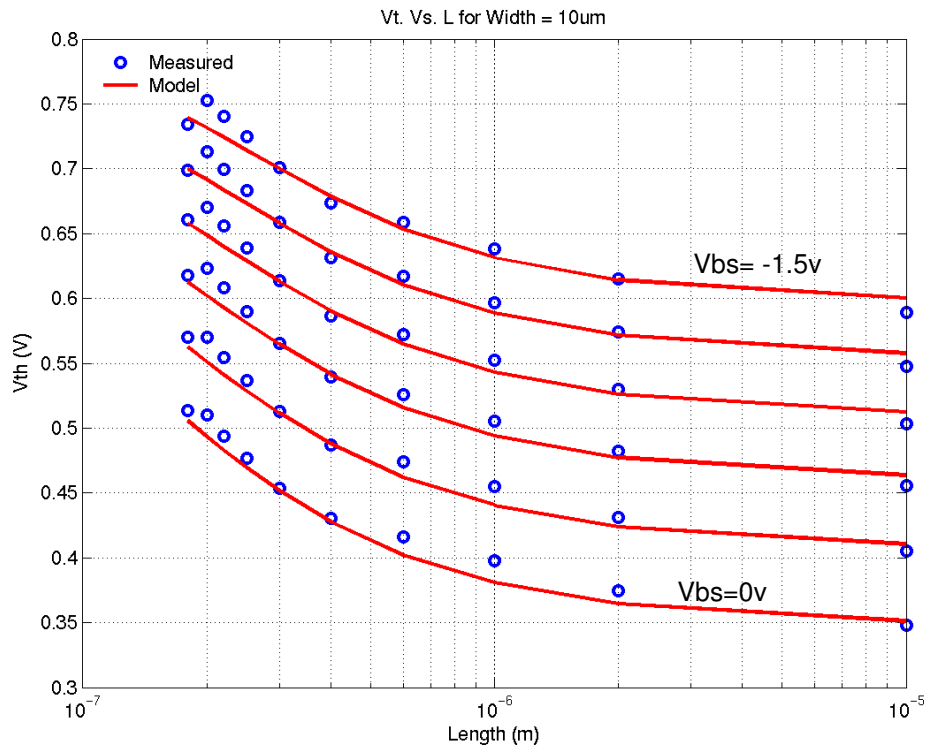


FIGURE 2.5 1p8v_nfet_vtVsW_25C

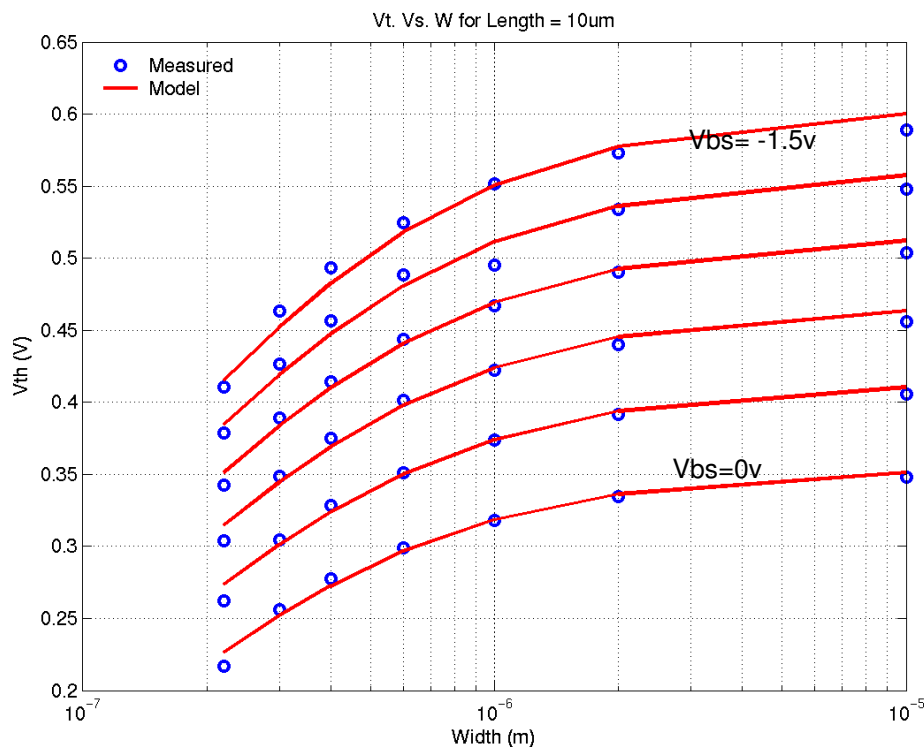


FIGURE 2.6 1p8v_nfet_10x10_idvg_25C

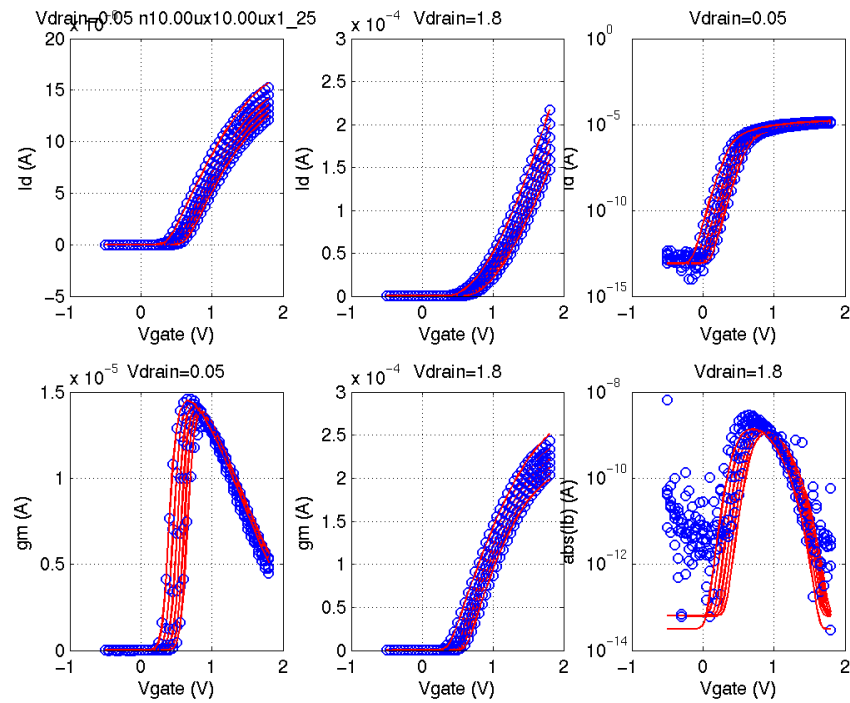


FIGURE 2.7 1p8v_nfet_10x10_idvd_25C

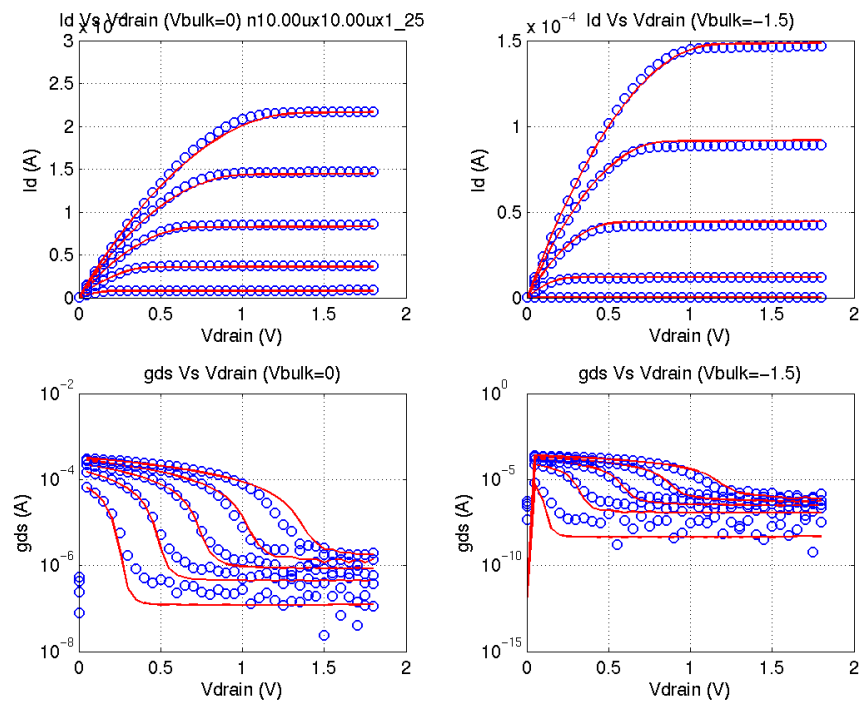


FIGURE 2.8 1p8v_nfet_10x0p18_idvg_25C

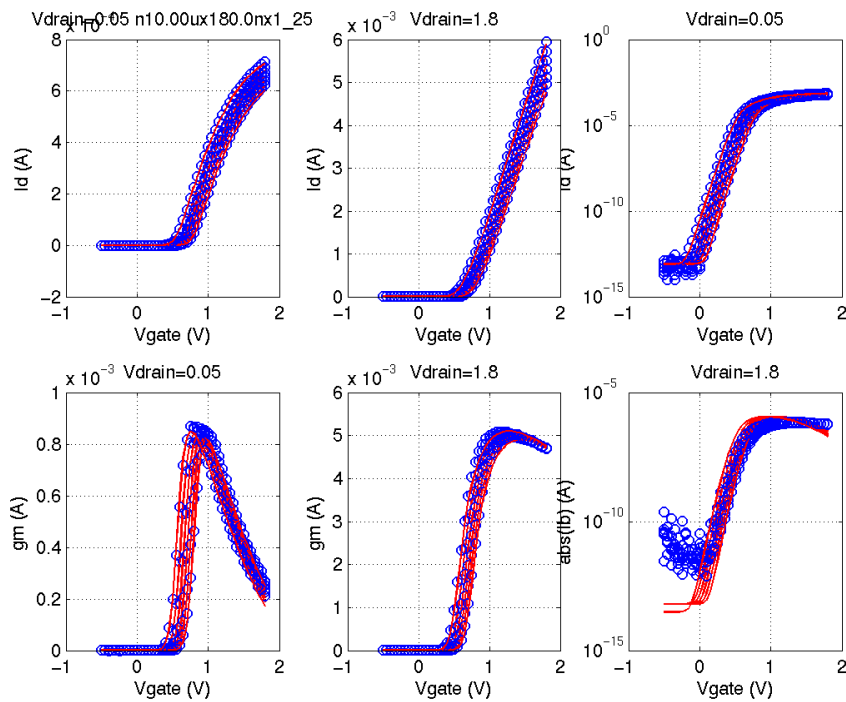


FIGURE 2.9 1p8v_nfet_10x0p18_idvg_25C

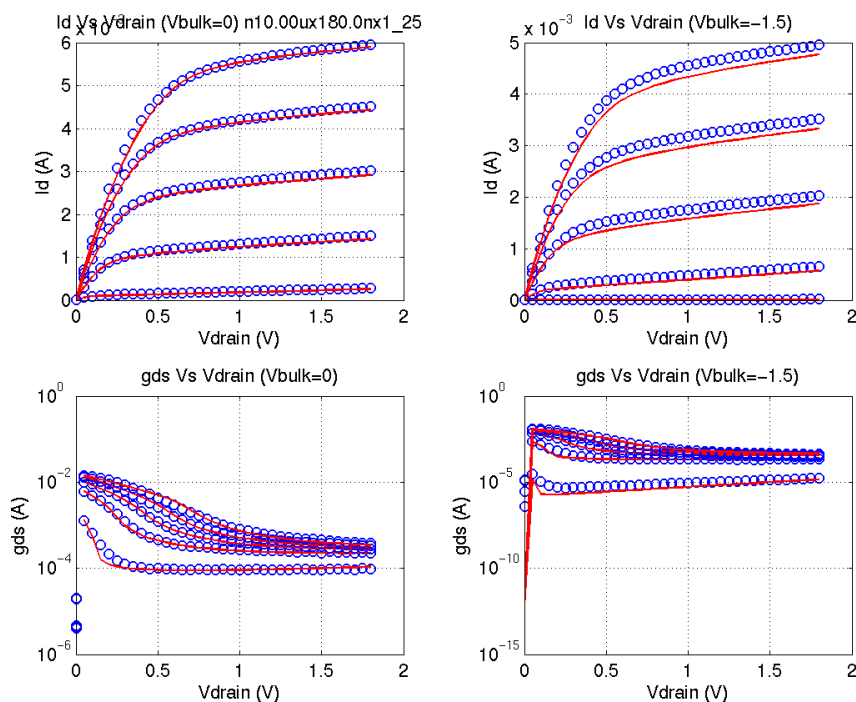


FIGURE 2.10 1p8v_nfet_0p22x10_idvg_25C

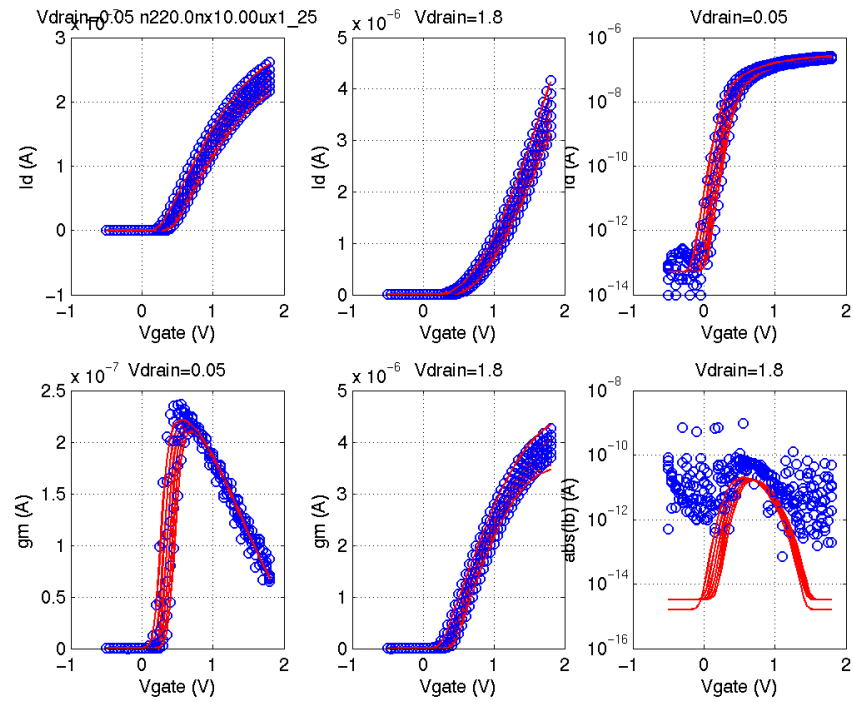


FIGURE 2.11 1p8v_nfet_0p22x10_idvd_25C

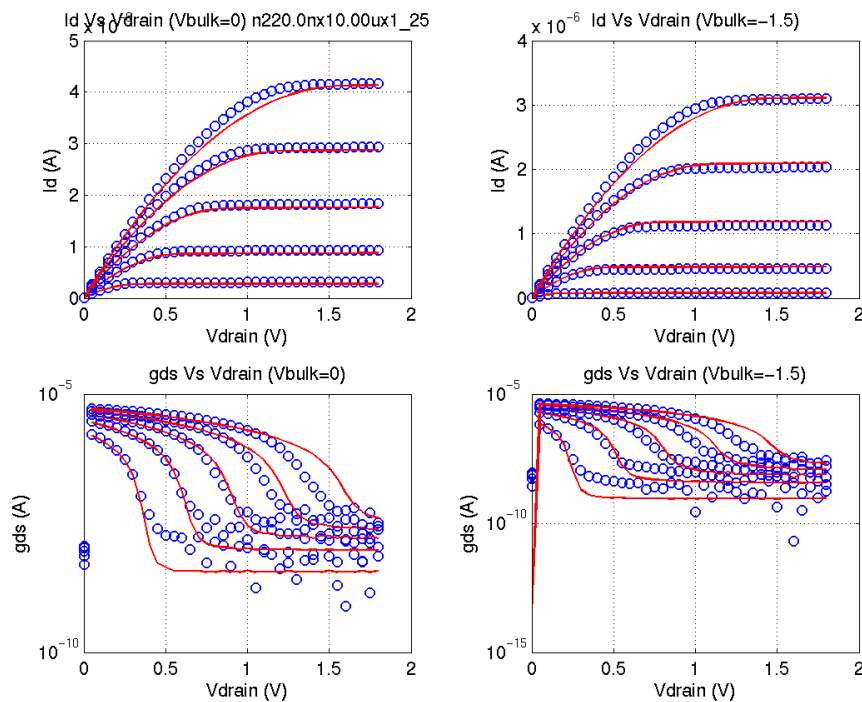


FIGURE 2.12 1p8v_nfet_0p22x0p18_idvg_25C - isolated “non-dogbonned” structure

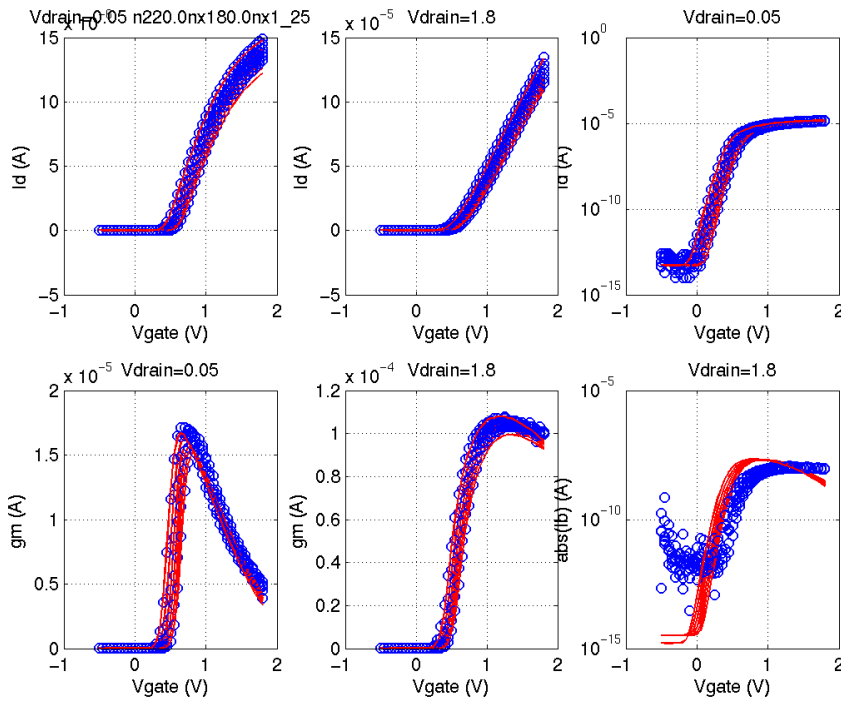


FIGURE 2.13 1p8v_nfet_0p22x0p18_idvd_25C - isolated “non-dogbonned” structure

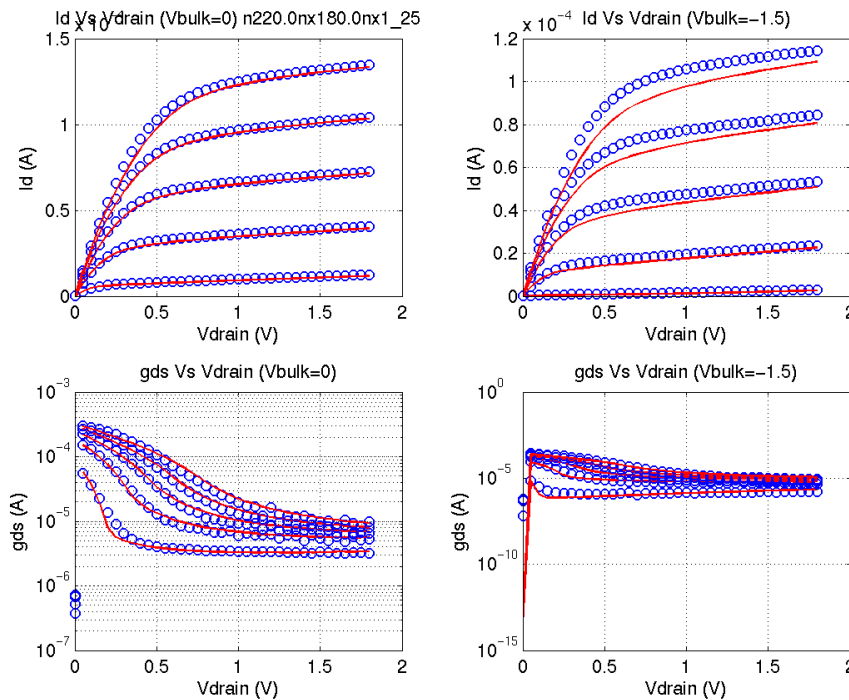


FIGURE 2.14 1p8v_nfet_0p4x0p18_idvg_25C

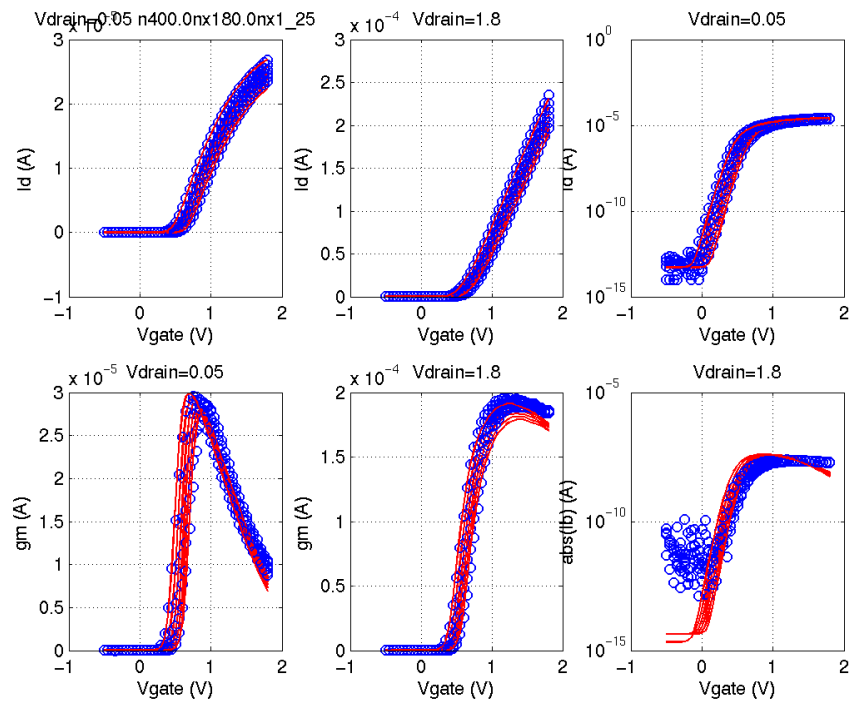


FIGURE 2.15 1p8v_nfet_0p4x0p18_idvd_25C

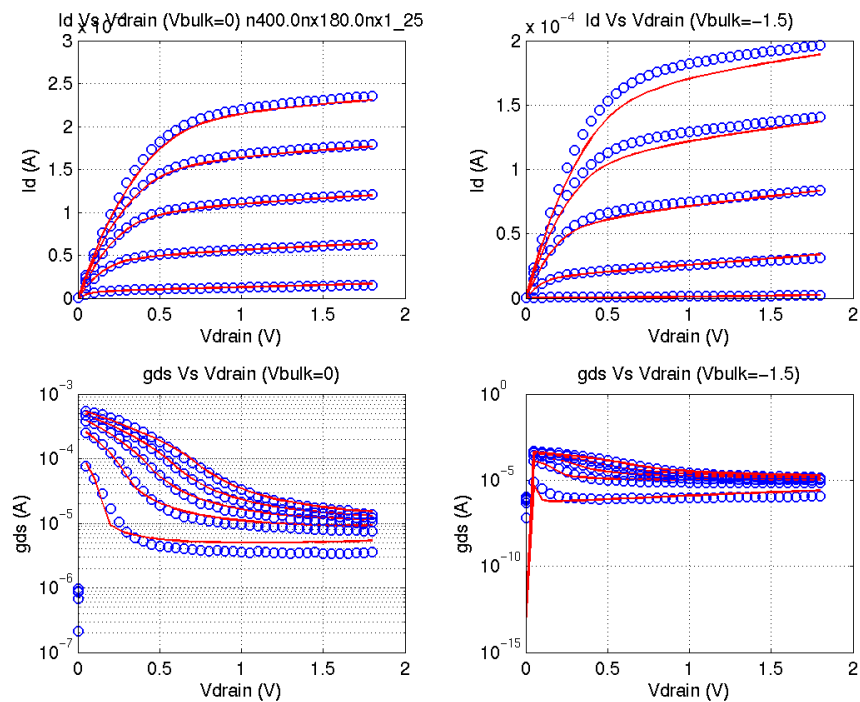


FIGURE 2.16 1p8v_nfet_10x0p25_idvg_25C

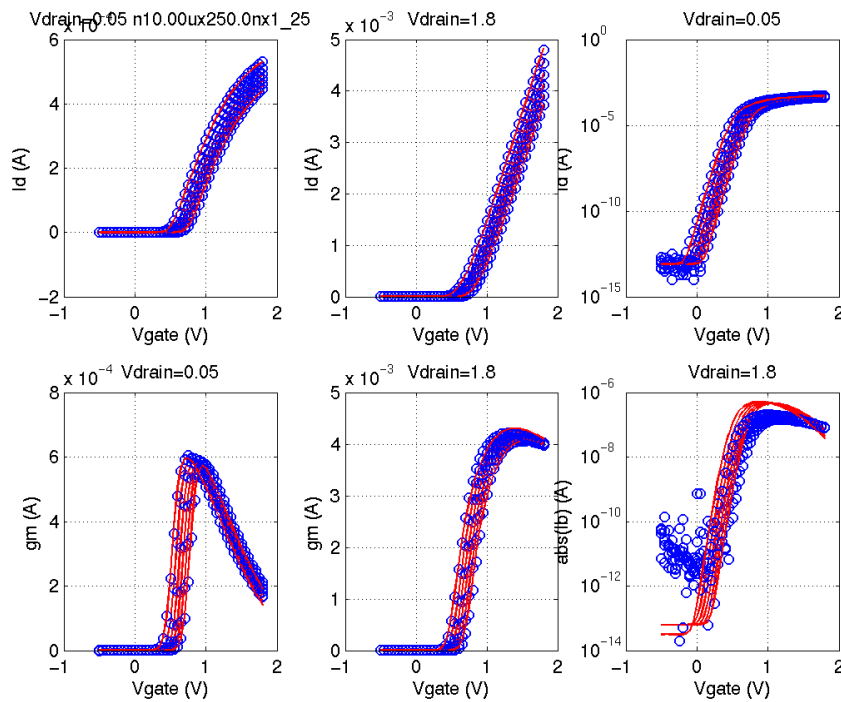


FIGURE 2.17 1p8v_nfet_10x0p25_idvd_25C

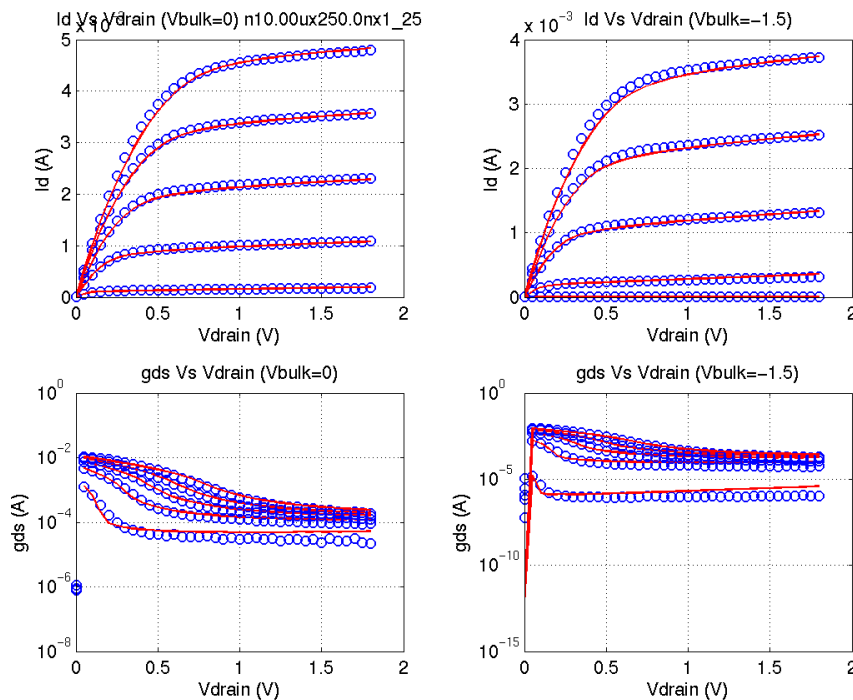


FIGURE 2.18 1p8v_nfet_10x0p18_idvg_-40C

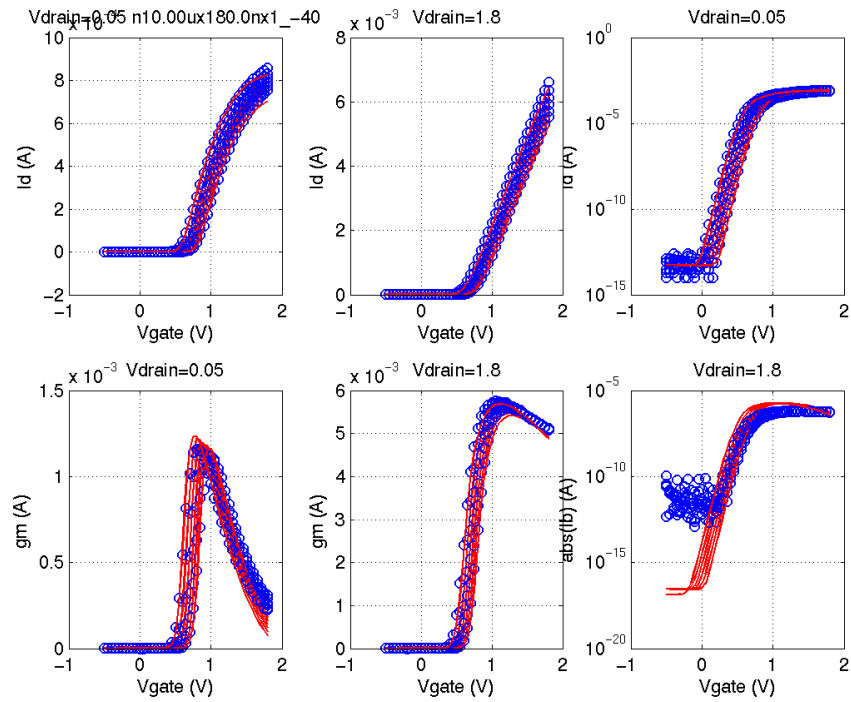


FIGURE 2.19 1p8v_nfet_10x0p18_idvd_-40C

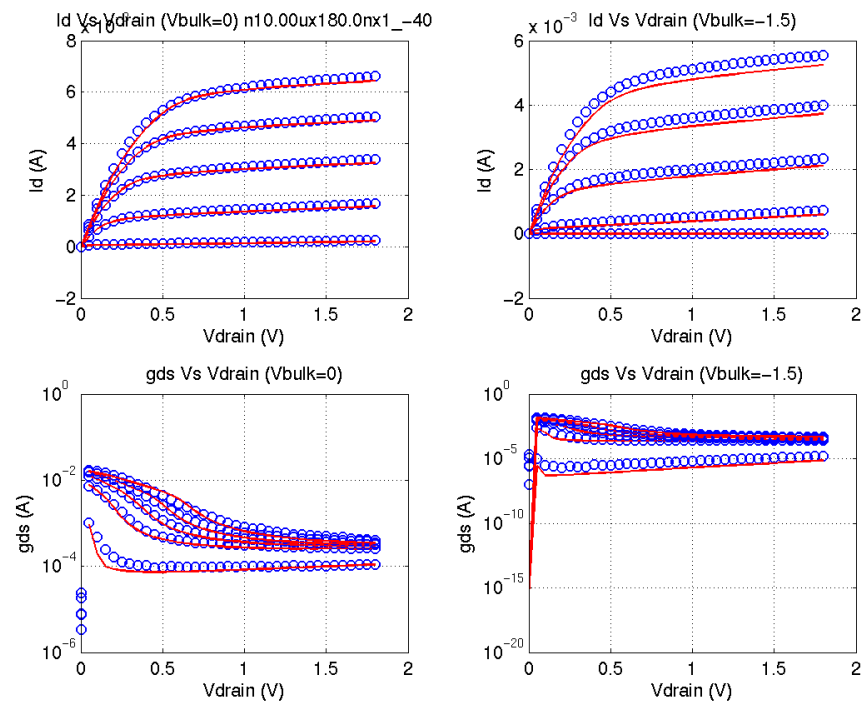


FIGURE 2.20 1p8v_nfet_10x0p18_idvg_125C

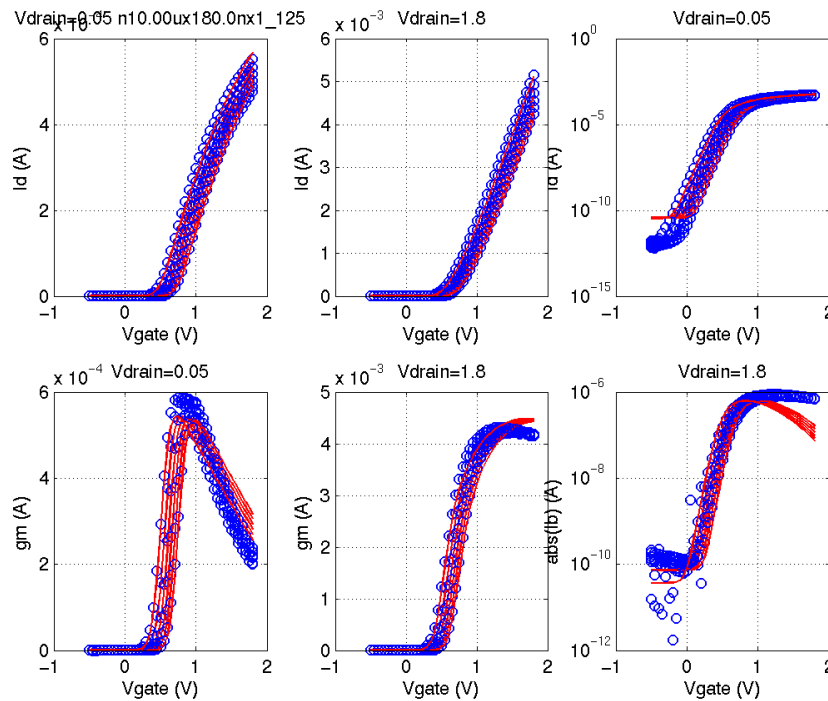


FIGURE 2.21 1p8v_nfet_10x0p18_idvd_125C

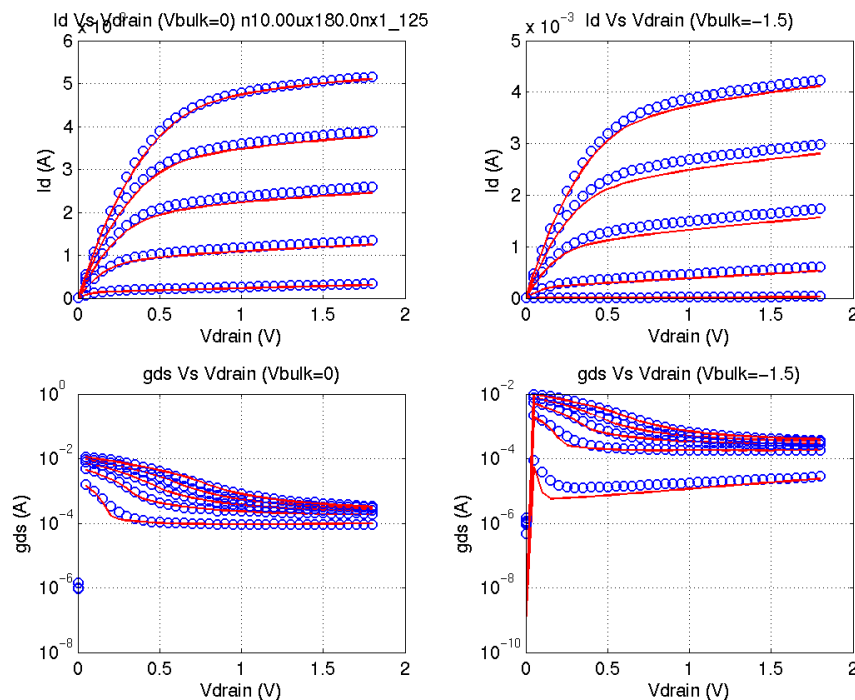
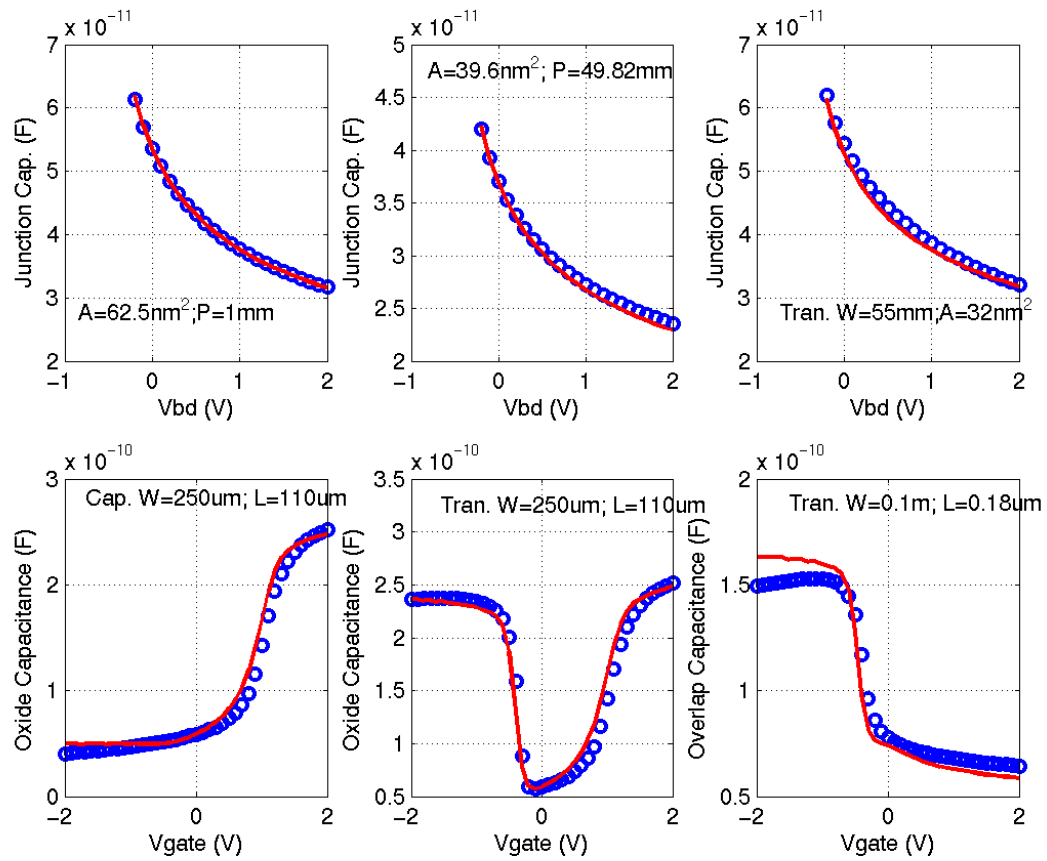


FIGURE 2.22 1p8_pfet_cv_25C



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FIGURE 2.23 1p8v_pfet_vtVsL_25C

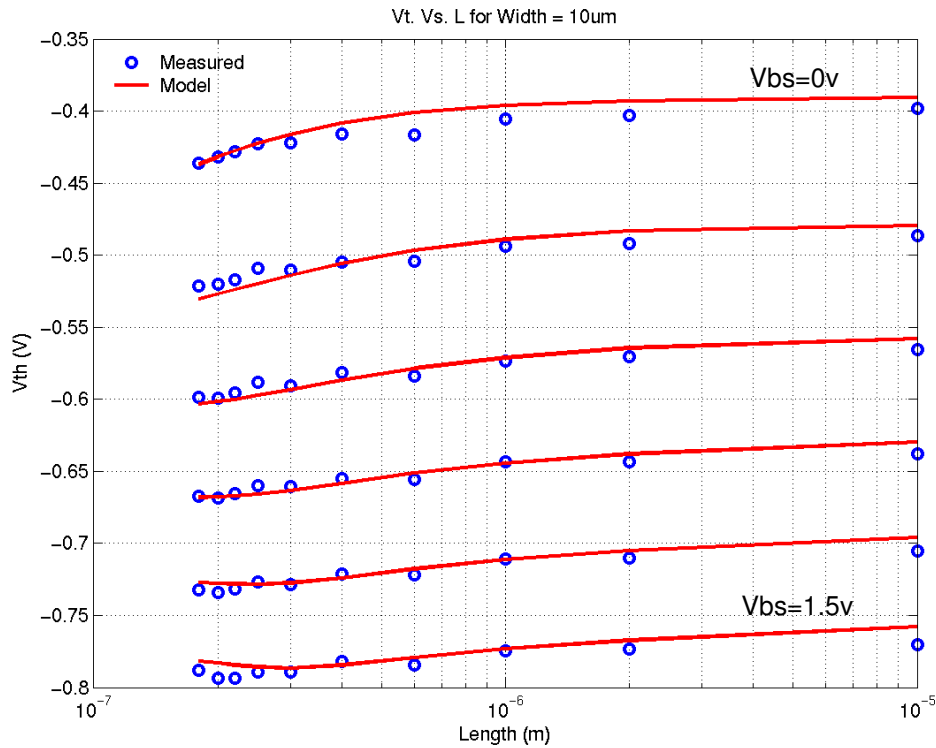


FIGURE 2.24 1p8v_pfet_vtVsW_25C

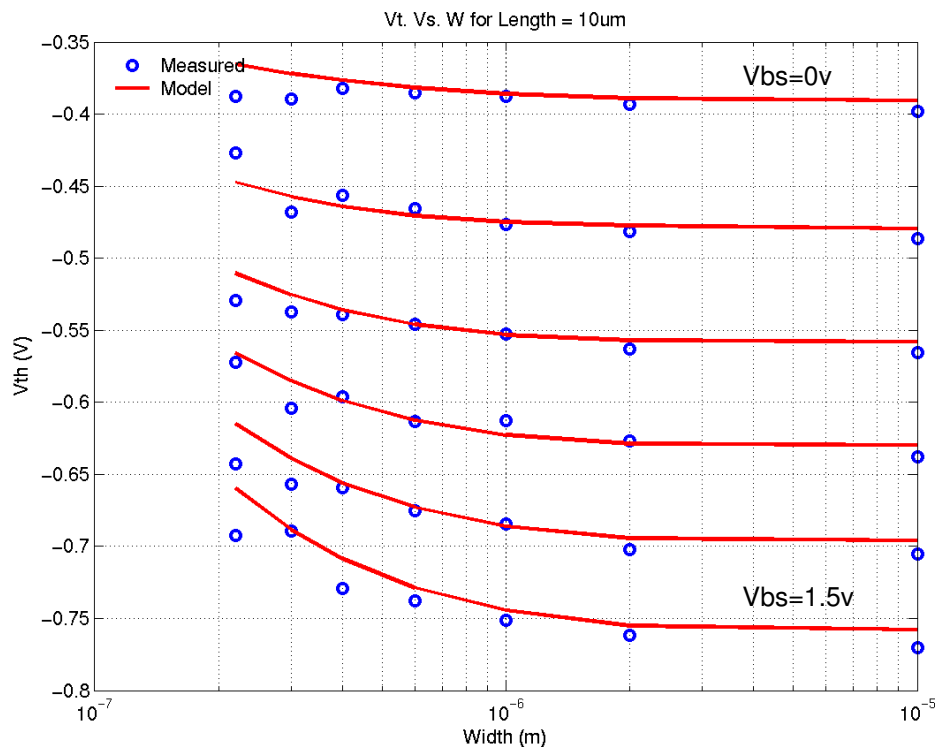


FIGURE 2.25 1p8v_pfet_10x10_idvg_25C

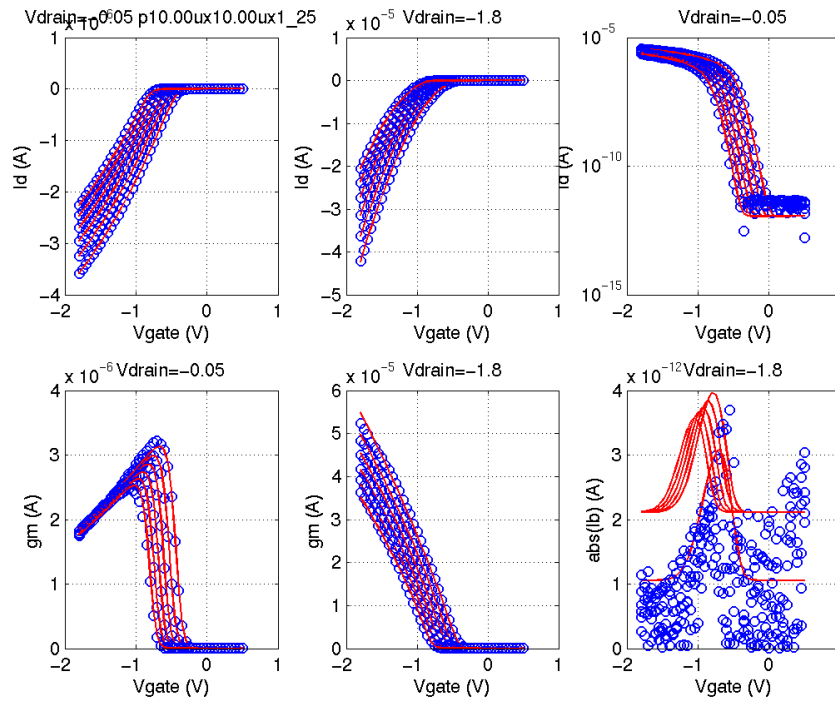


FIGURE 2.26 1p8v_pfet_10x10_idvd_25C

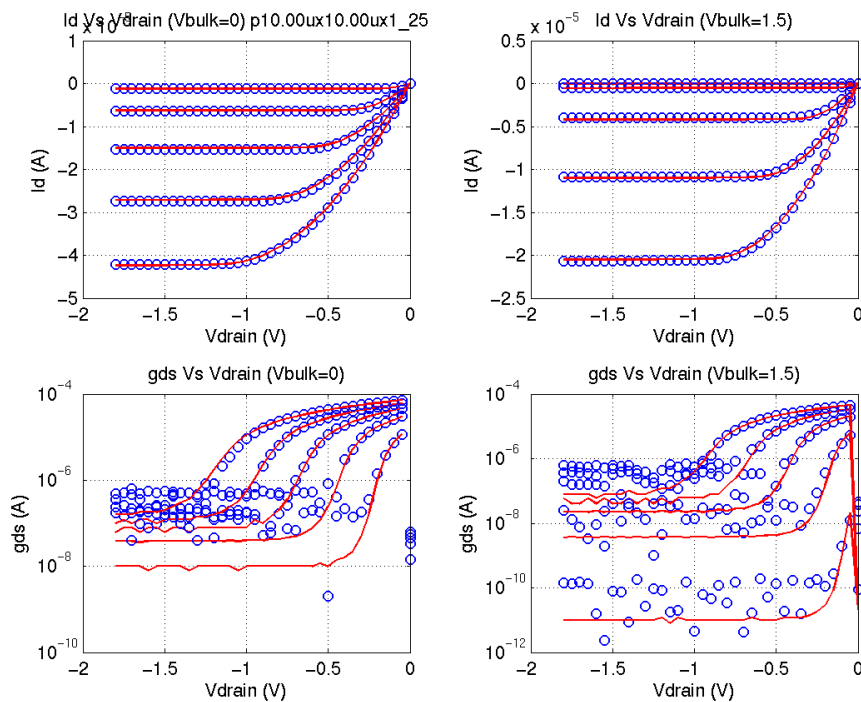


FIGURE 2.27 1p8v_pfet_10x0p18_idvg_25C

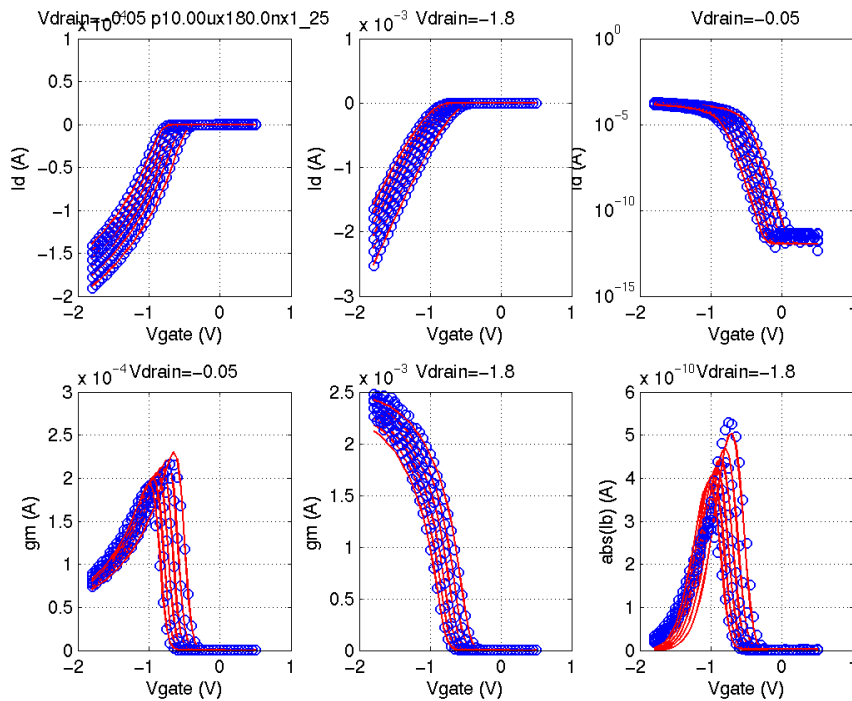


FIGURE 2.28 1p8v_pfet_10x0p18_idvd_25C

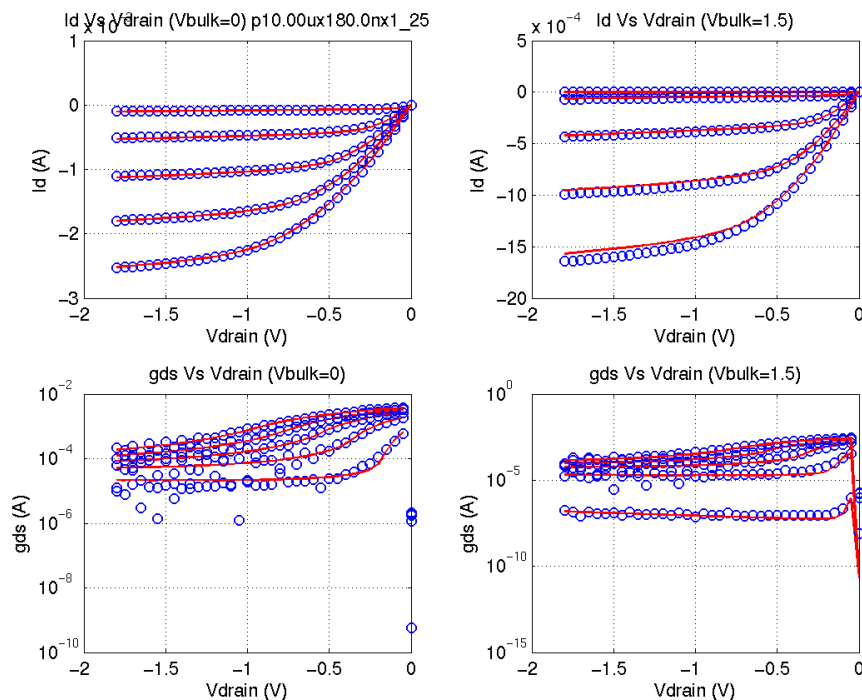


FIGURE 2.29 1p8v_pfet_0p22x10_idvg_25C

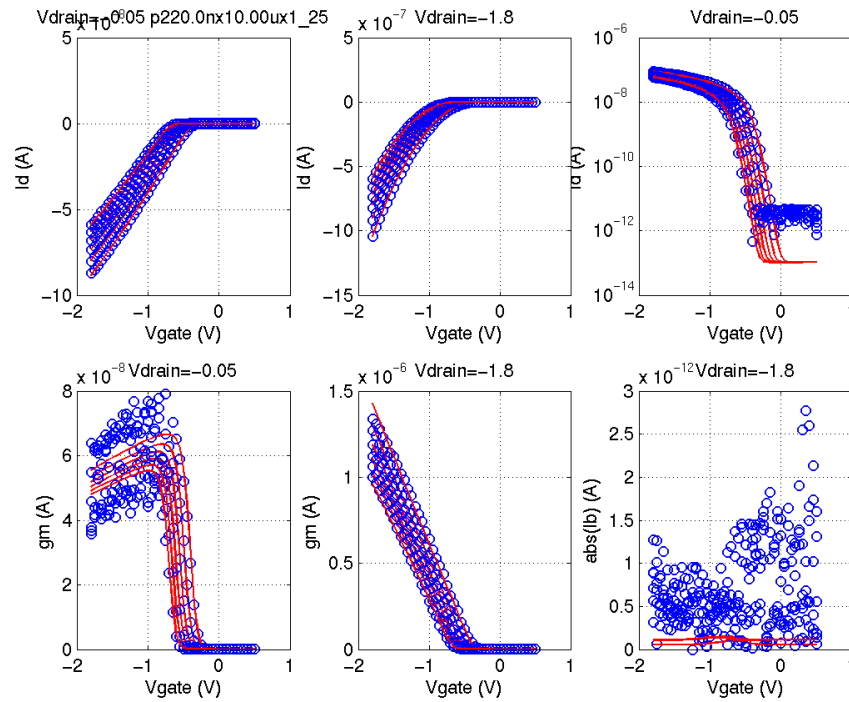


FIGURE 2.30 1p8v_pfet_0p22x10_idvd_25C

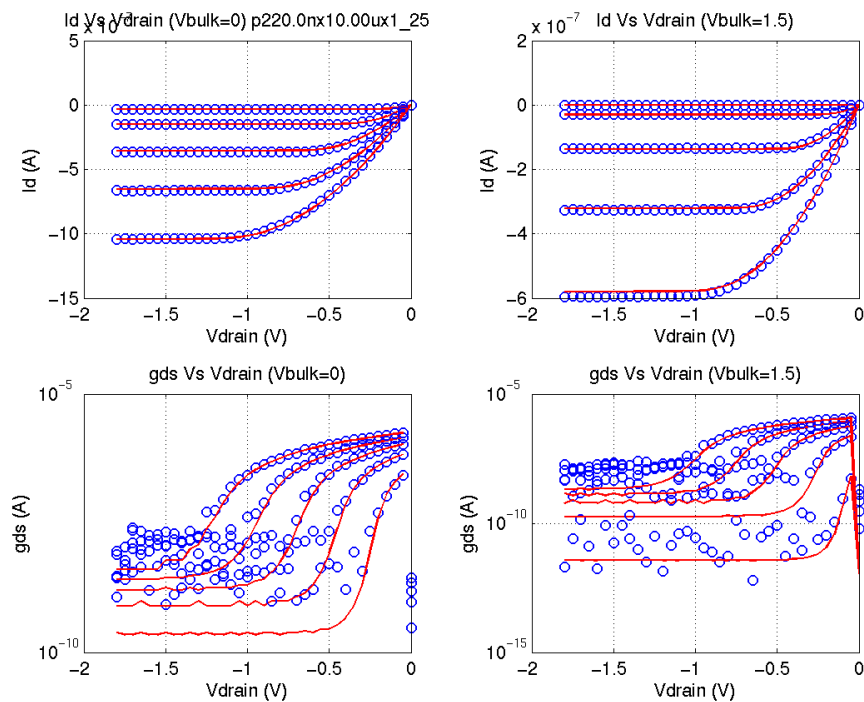


FIGURE 2.31 1p8v_pfet_0p22x0p18_idvg_25C - isolated “non-dogbonned” structure

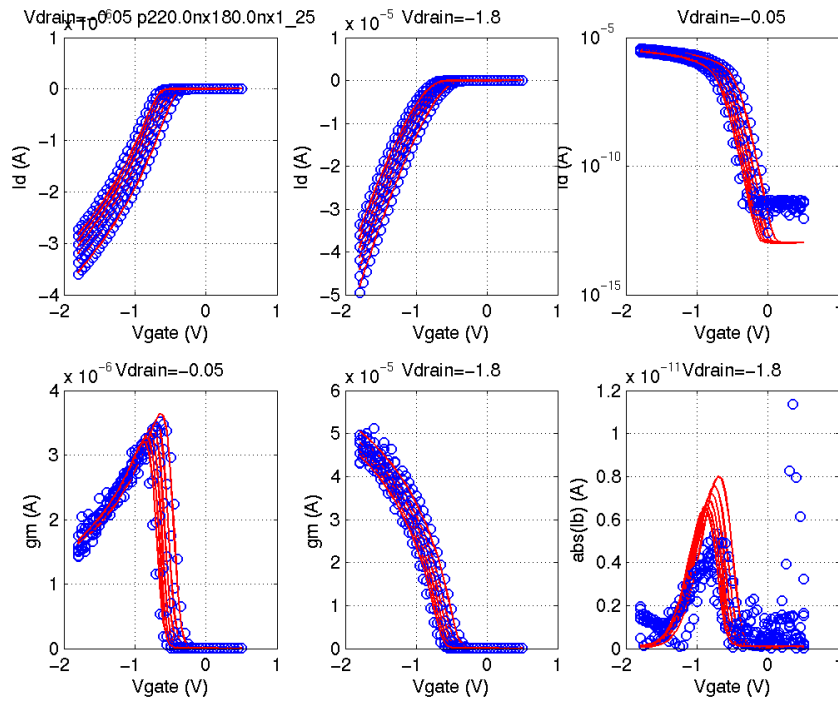


FIGURE 2.32 1p8v_pfet_0p22x0p18_idvd_25C - isolated “non-dogbonned” structure

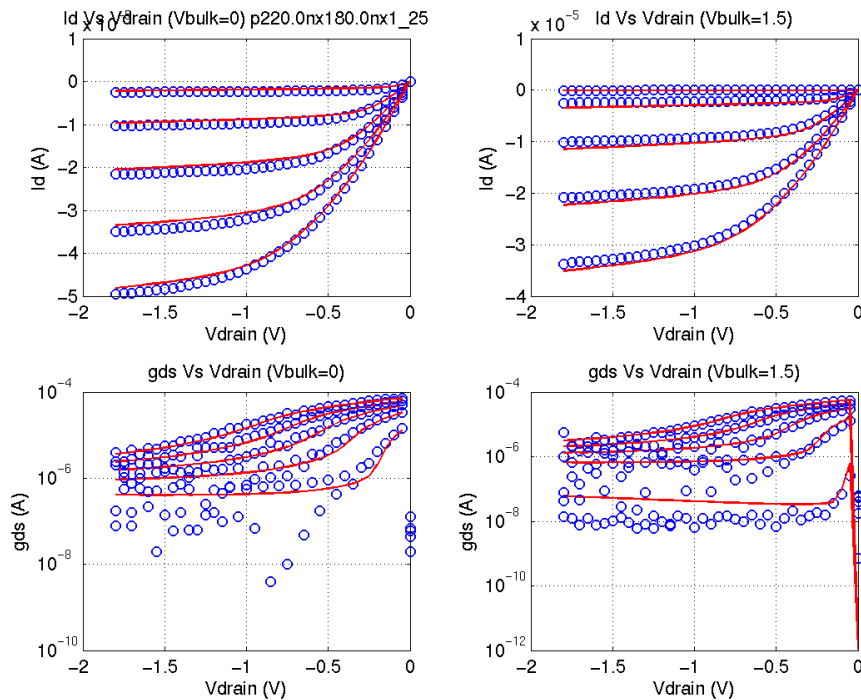


FIGURE 2.33 1p8v_pfet_0p4x0p18_idvg_25C

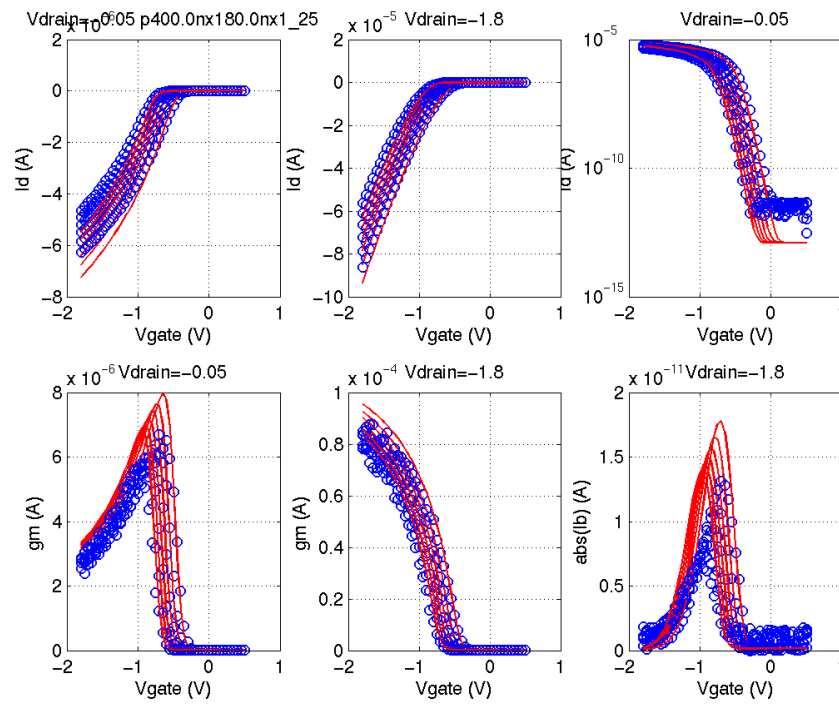


FIGURE 2.34 1p8v_pfet_0p4x0p18_idvd_25C

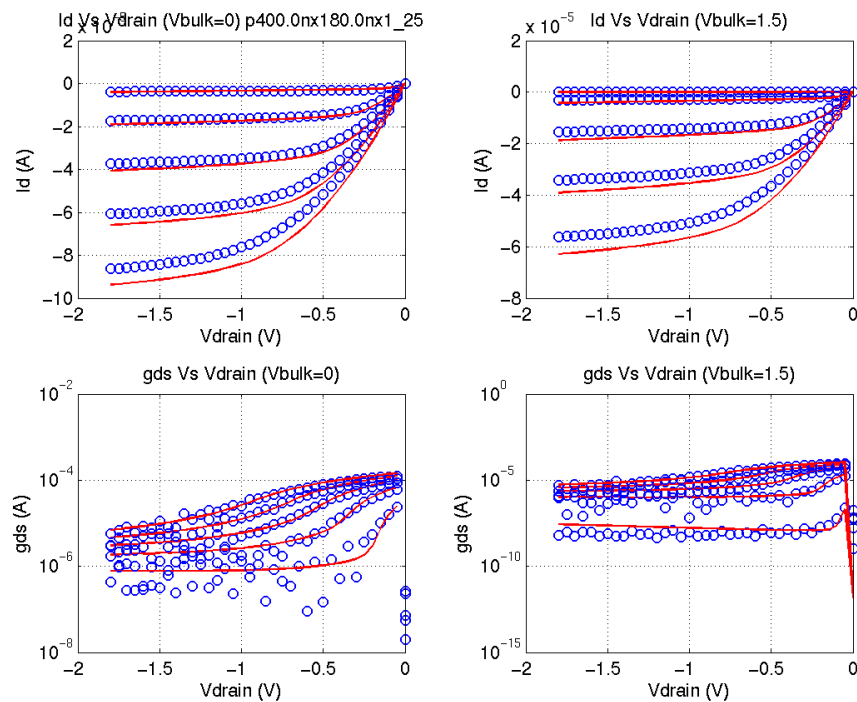


FIGURE 2.35 1p8v_pfet_10x0p25_idvg_25C

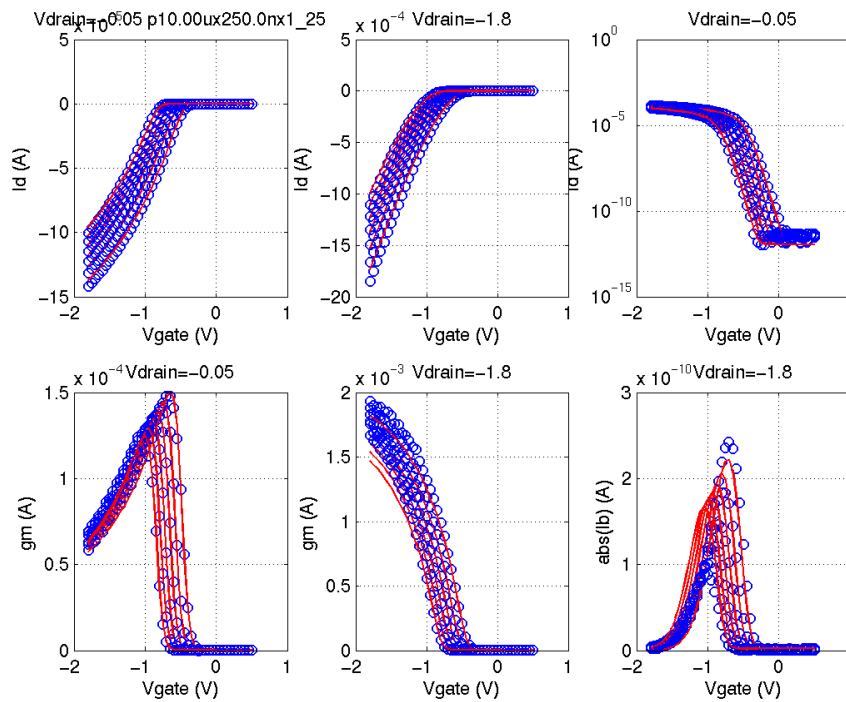


FIGURE 2.36 1p8v_pfet_10x0p25_idvd_25C

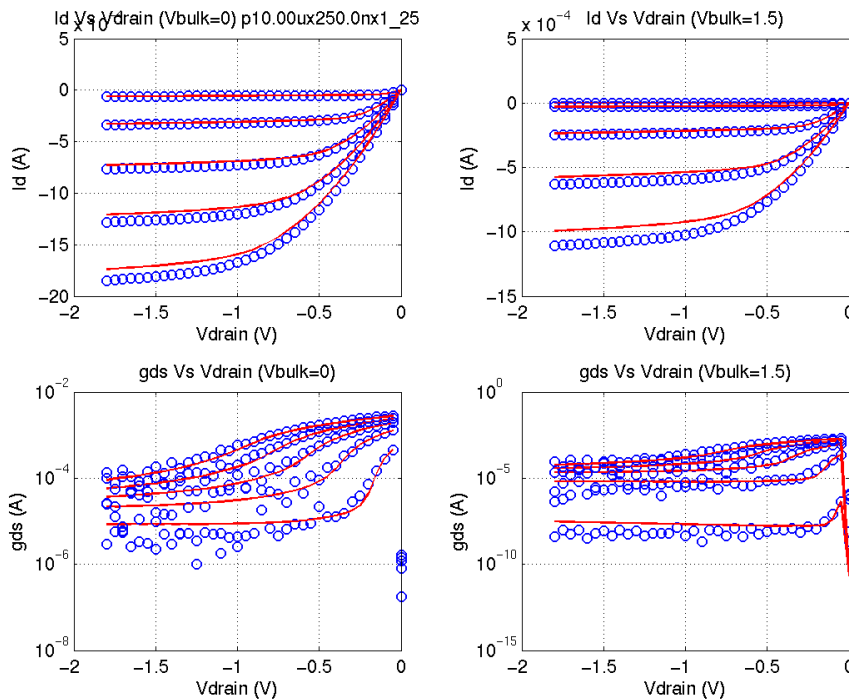


FIGURE 2.37 1p8v_pfet_10x0p18_idvg_-40C

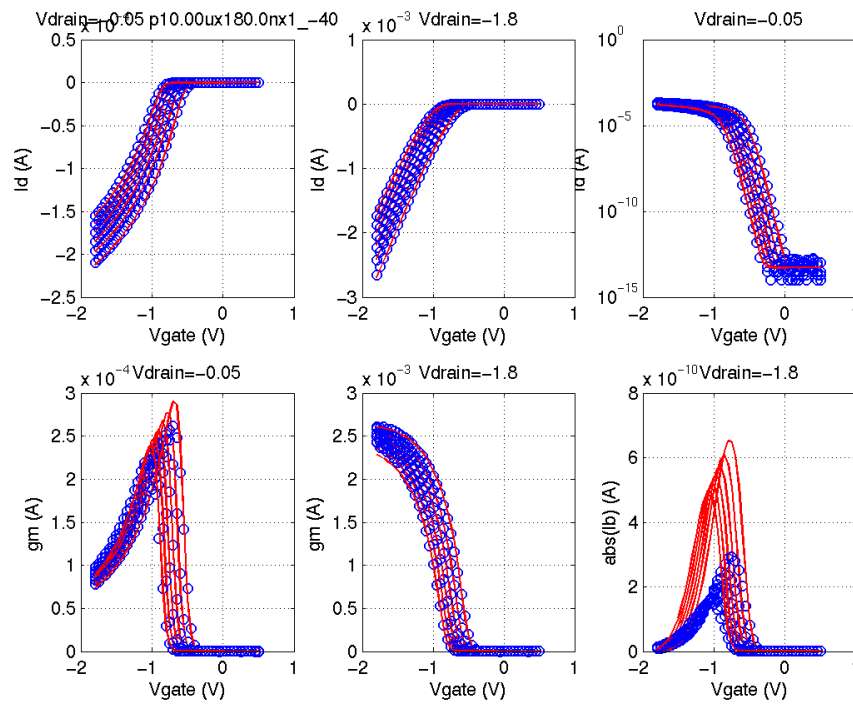


FIGURE 2.38 1p8v_pfet_10x0p18_idvd_-40C

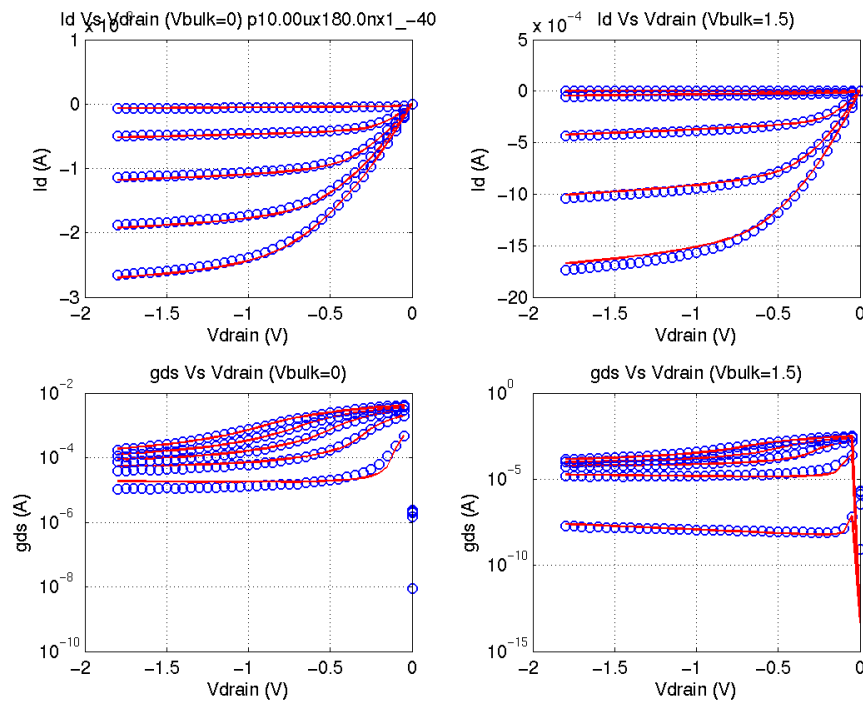


FIGURE 2.39 1p8v_pfet_10x0p18_idvg_125C

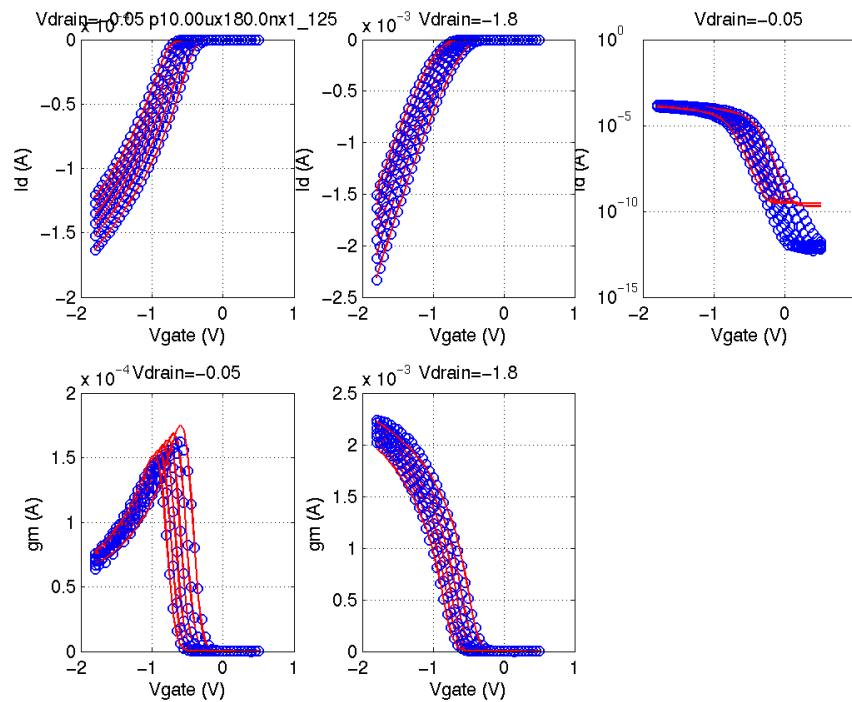


FIGURE 2.40 1p8v_pfet_10x0p18_idvd_125C

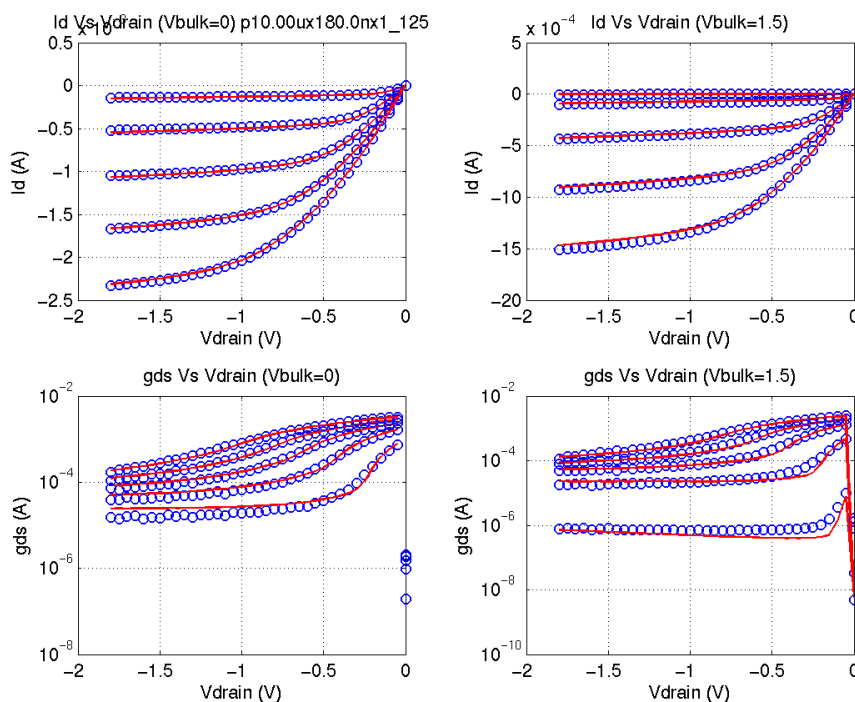
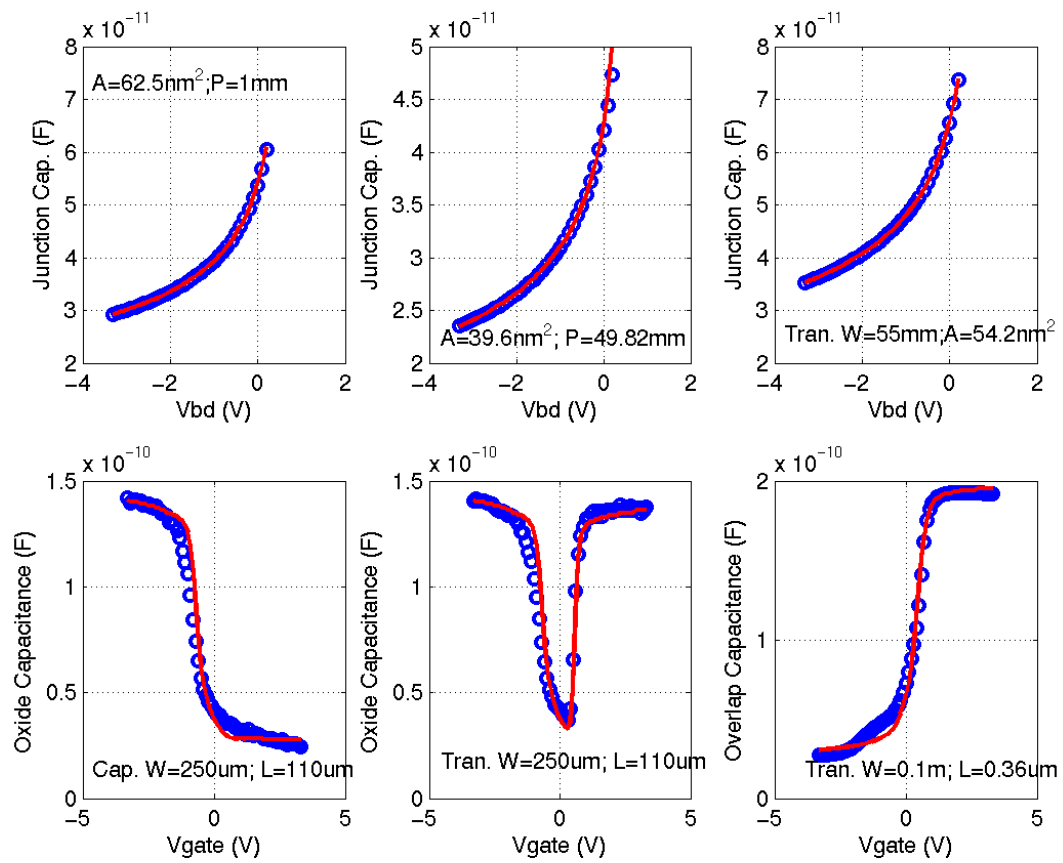


FIGURE 2.41 3p3_nfet_cv_25C



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FIGURE 2.42 3p3v_nfet_vtVsL_25C

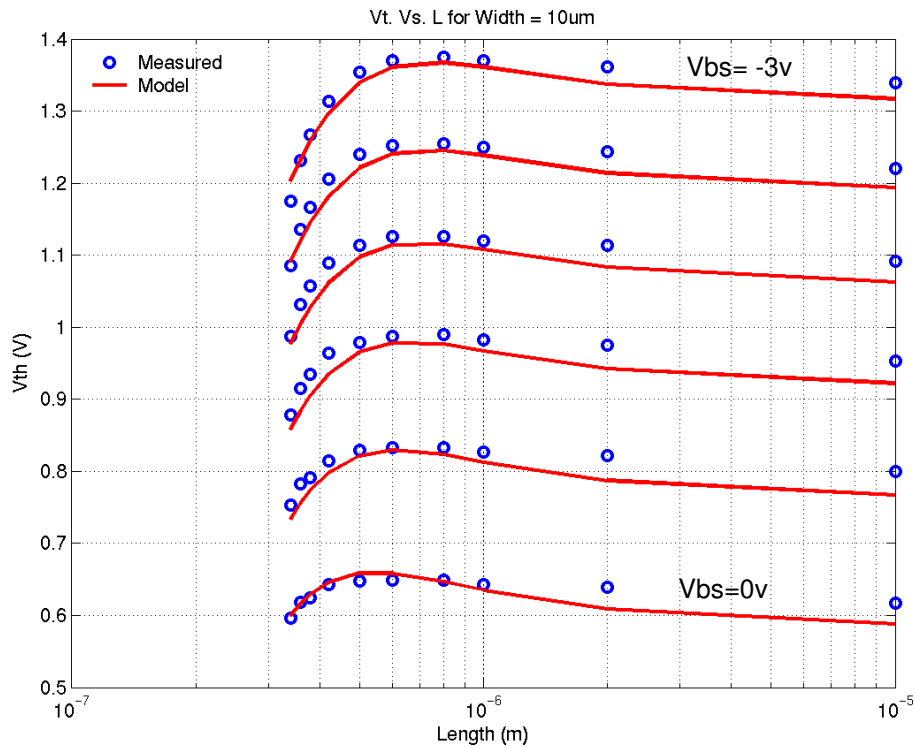


FIGURE 2.43 3p3v_nfet_vtVsW_25C

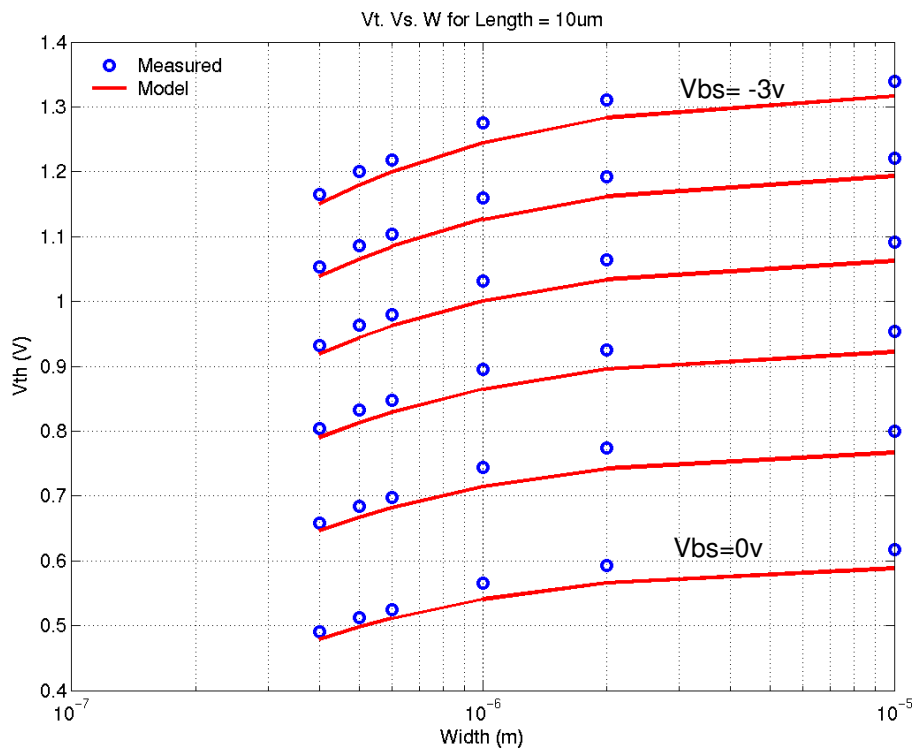


FIGURE 2.44 3p3v_nfet_10x10_idvg_25C

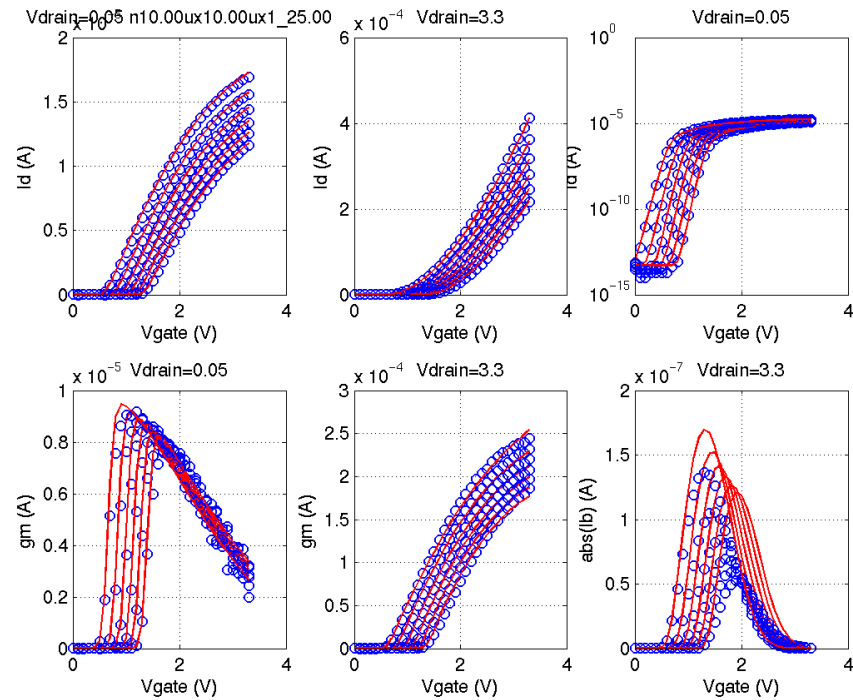


FIGURE 2.45 3p3v_nfet_10x10_idvd_25C

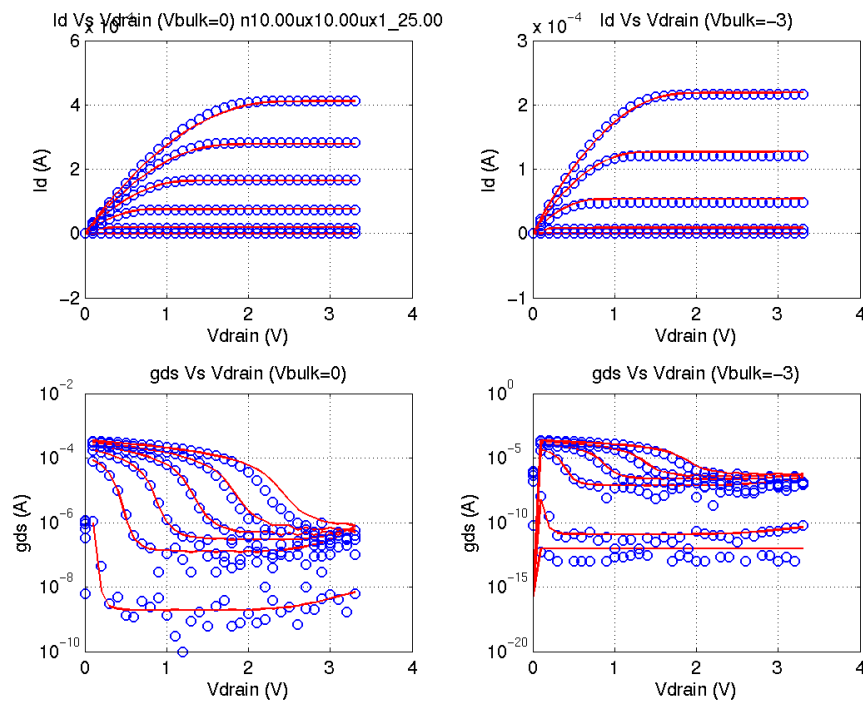


FIGURE 2.46 3p3v_nfet_10x0p36_idvg_25C

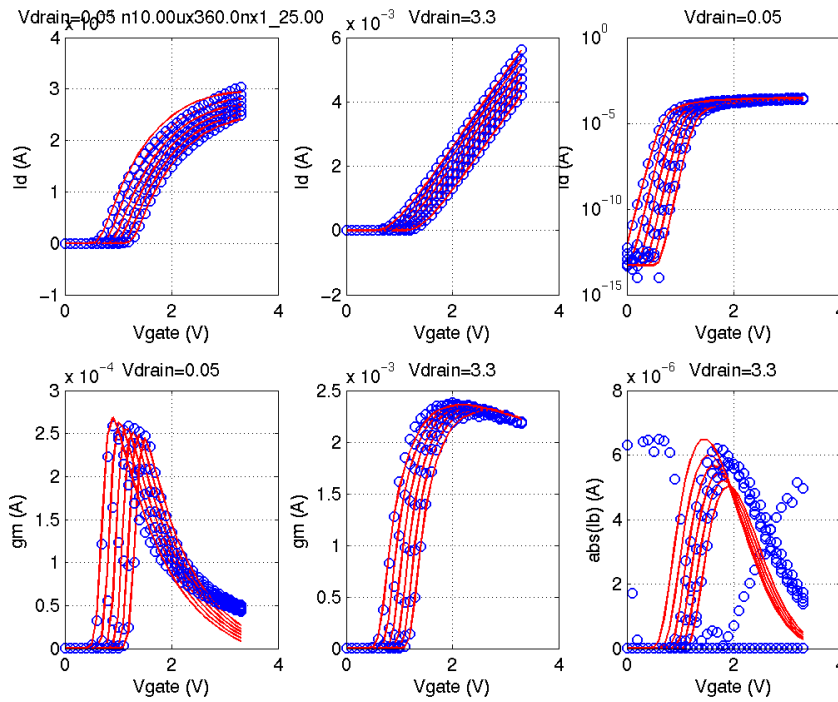


FIGURE 2.47 3p3v_nfet_10x0p36_idvd_25C

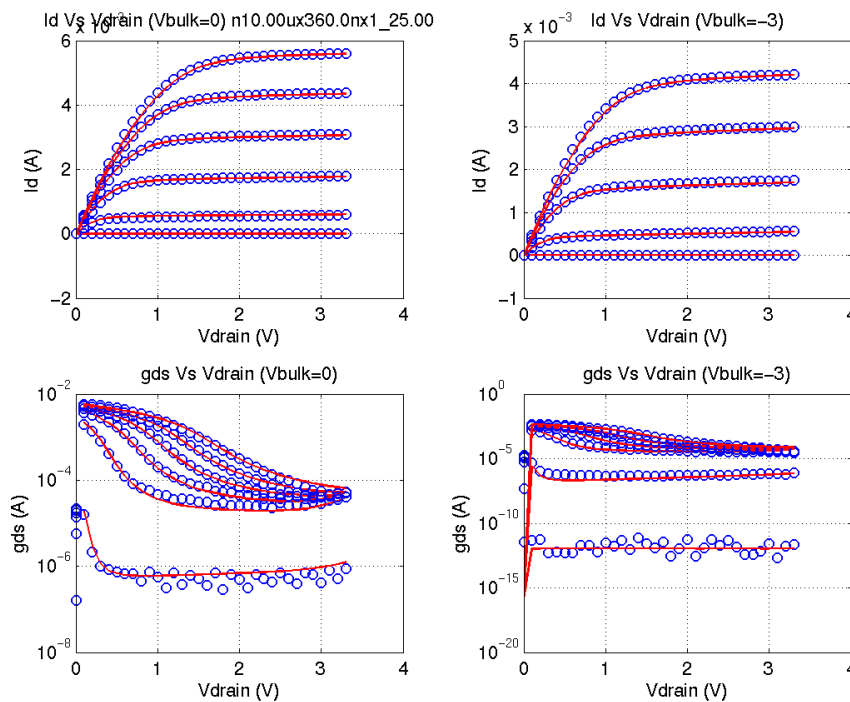


FIGURE 2.48 3p3v_nfet_0p4x10_idvg_25C

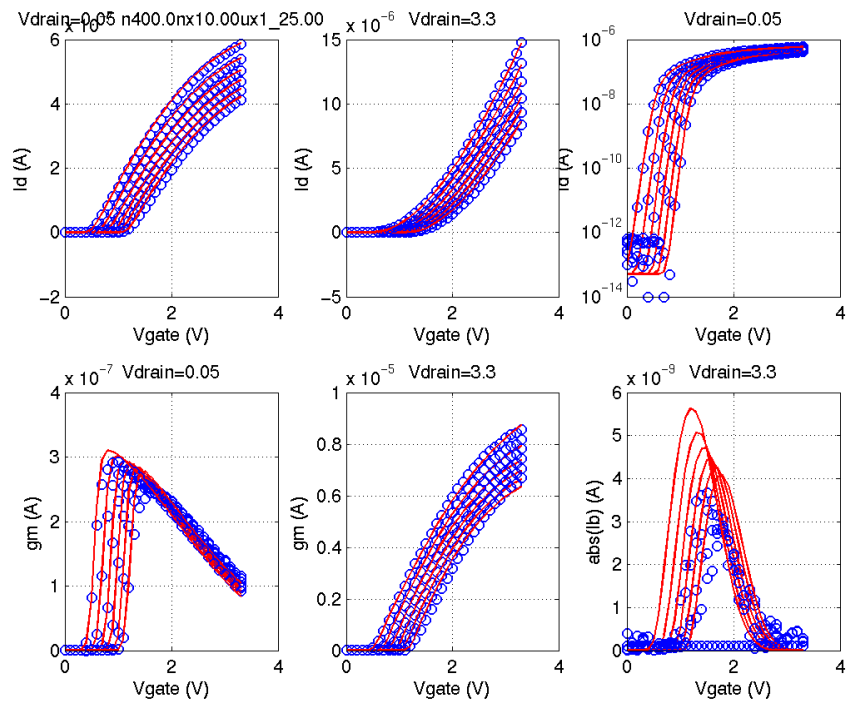


FIGURE 2.49 3p3v_nfet_0p4x10_idvd_25C

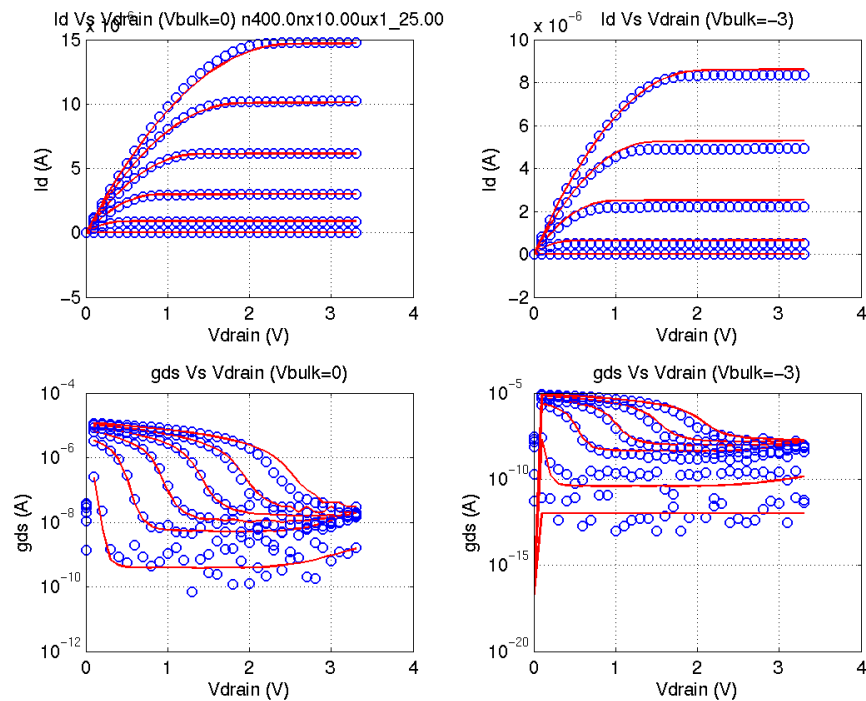


FIGURE 2.50 3p3v_nfet_0p4x0p36_idvg_25C

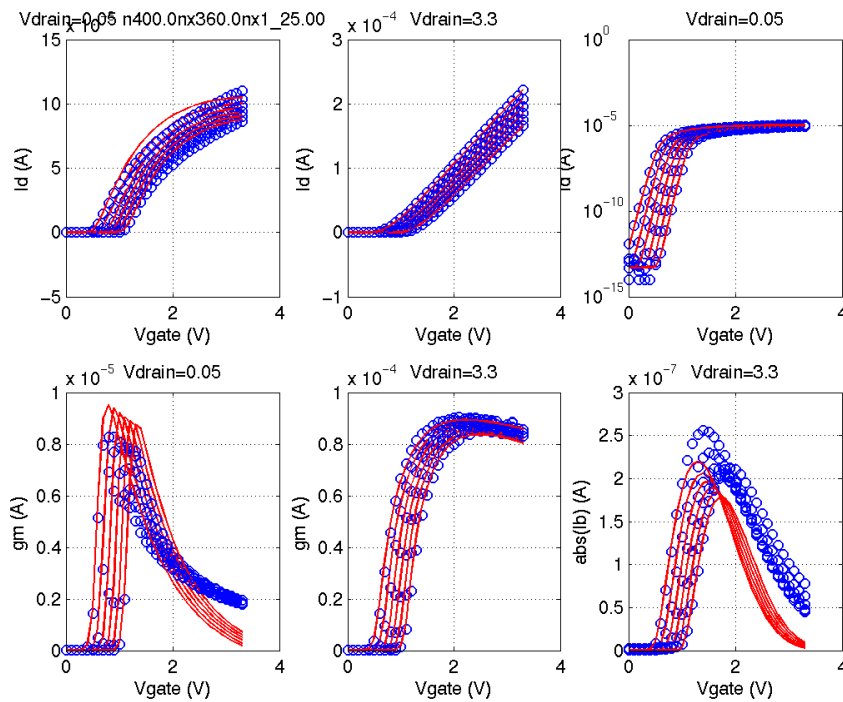


FIGURE 2.51 3p3v_nfet_0p4x0p36_idvd_25C

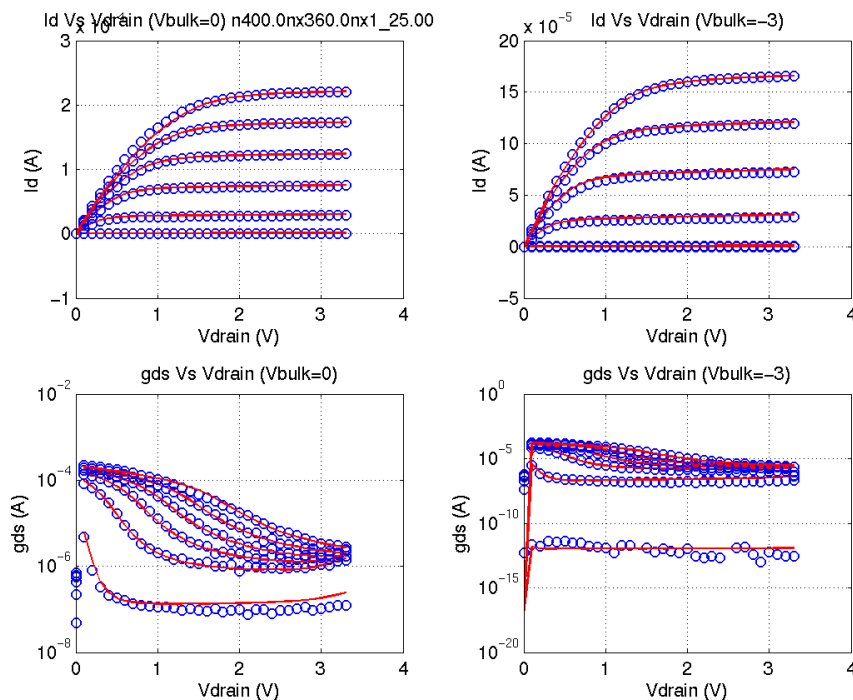


FIGURE 2.52 3p3v_nfet_0p6x0p36_idvg_25C

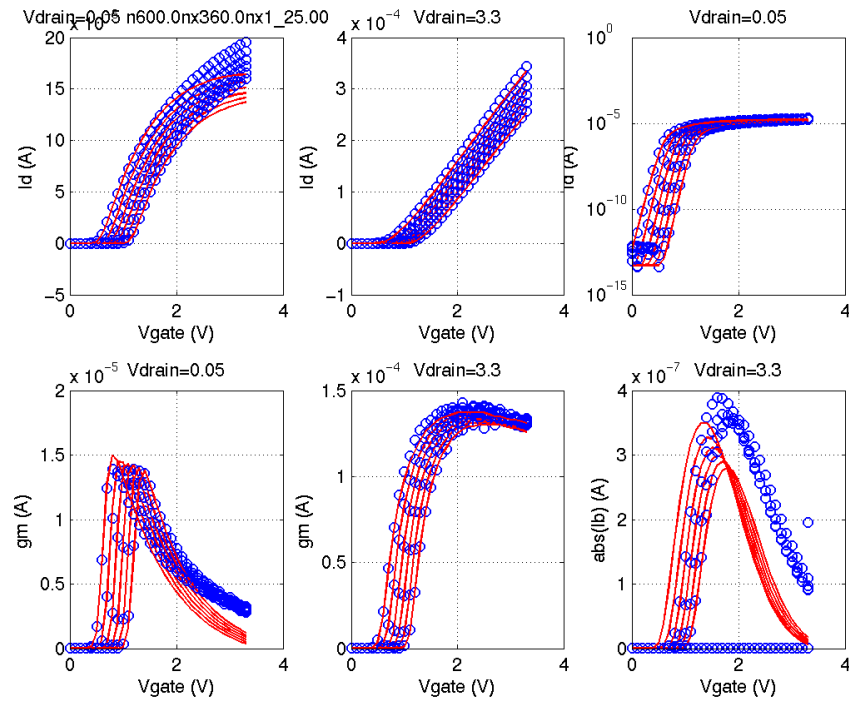


FIGURE 2.53 3p3v_nfet_0p6x0p36_idvd_25C

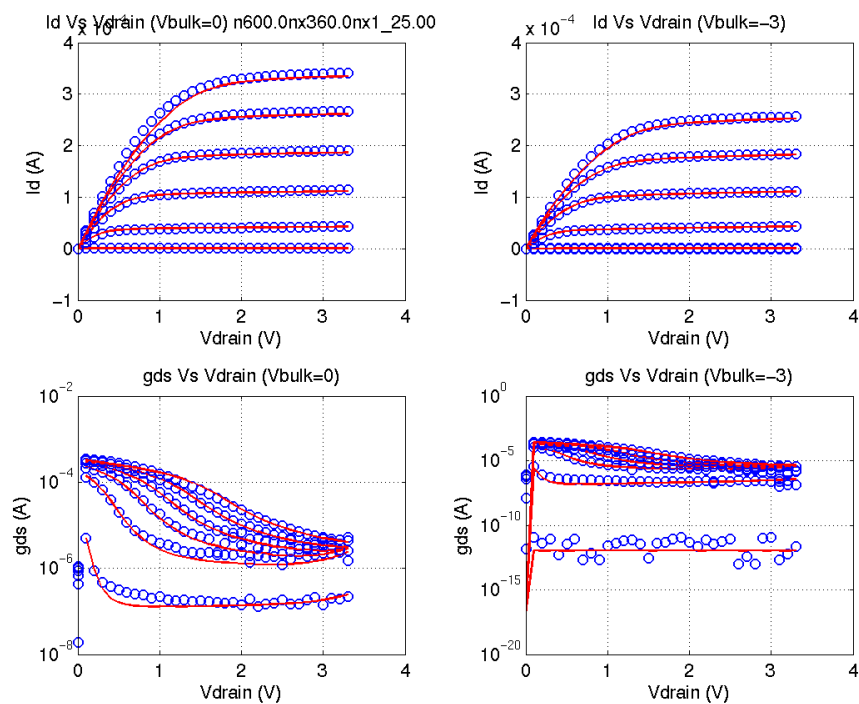


FIGURE 2.54 3p3v_nfet_10x0p6_idvg_25C

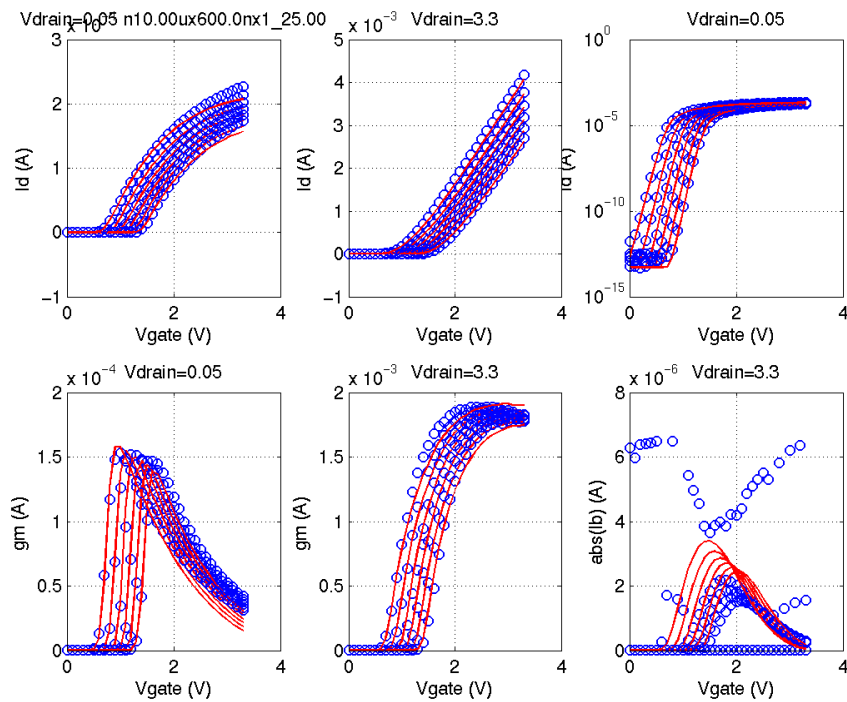


FIGURE 2.55 3p3v_nfet_10x0p6_idvd_25C

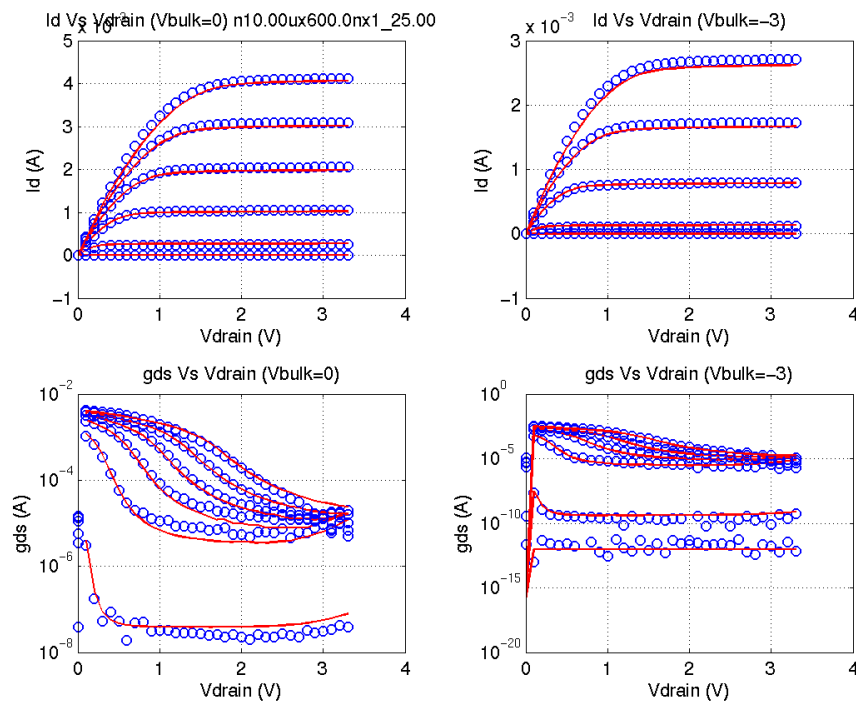


FIGURE 2.56 3p3v_nfet_10x0p36_idvg_-40C

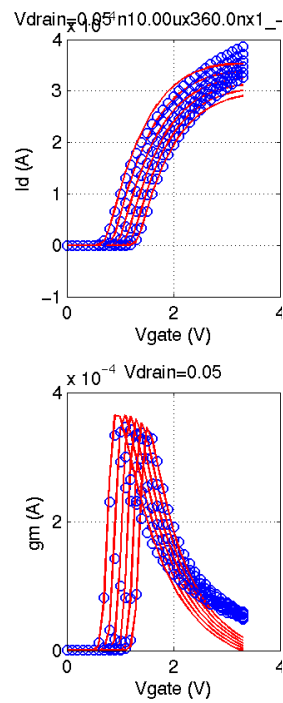


FIGURE 2.57 3p3v_nfet_10x0p36_idvd_-40C

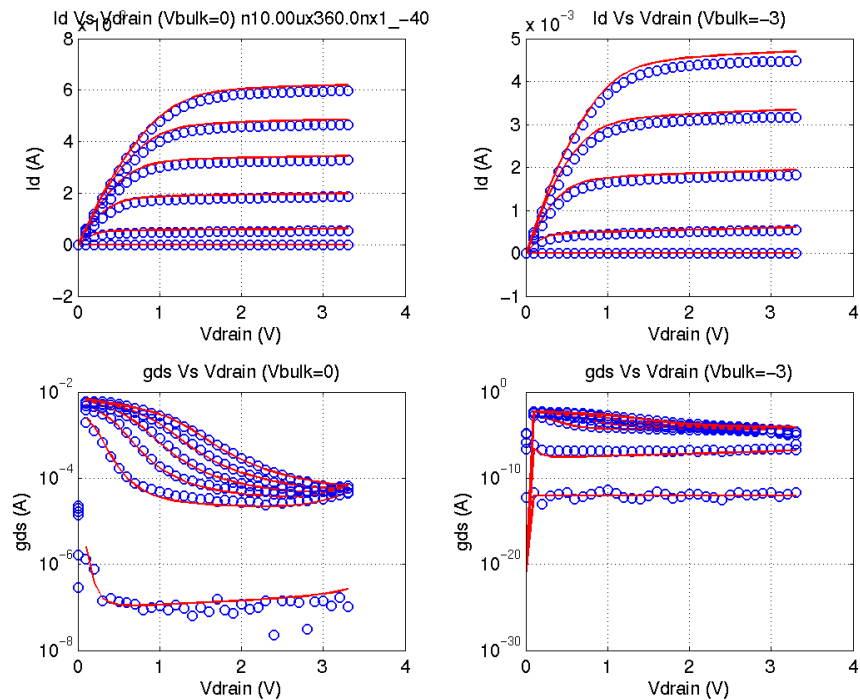


FIGURE 2.58 3p3v_nfet_10x0p36_idvg_125C

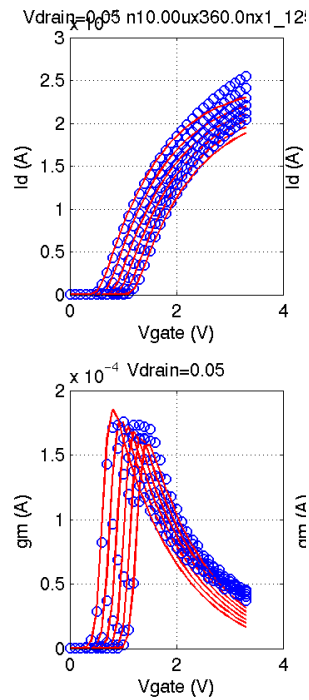


FIGURE 2.59 3p3v_nfet_10x0p36_idvd_125C

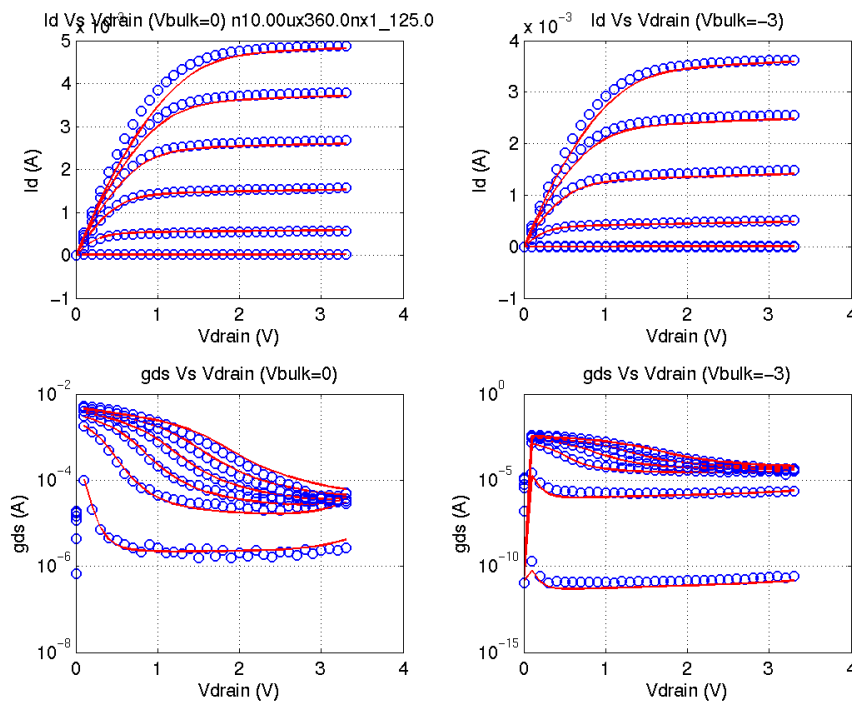
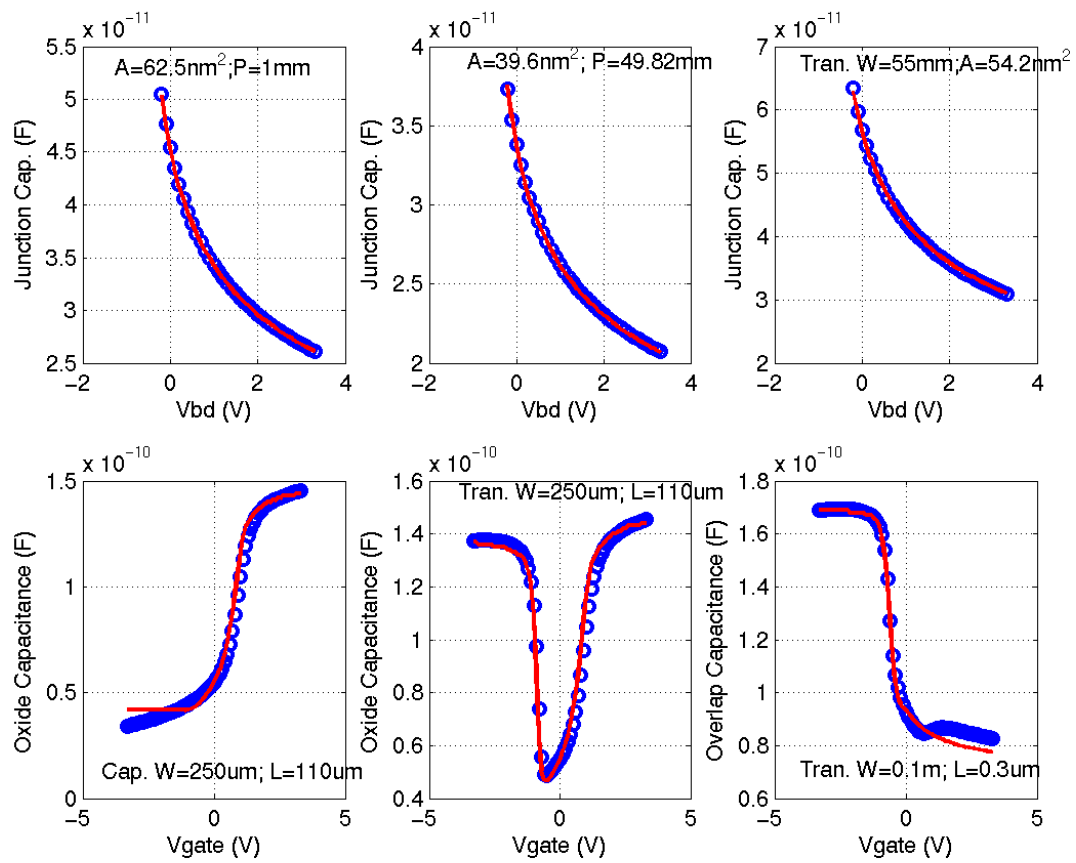


FIGURE 2.60 3p3_pfet_cv_25C



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FIGURE 2.61 3p3v_pfet_vtVsL_25C

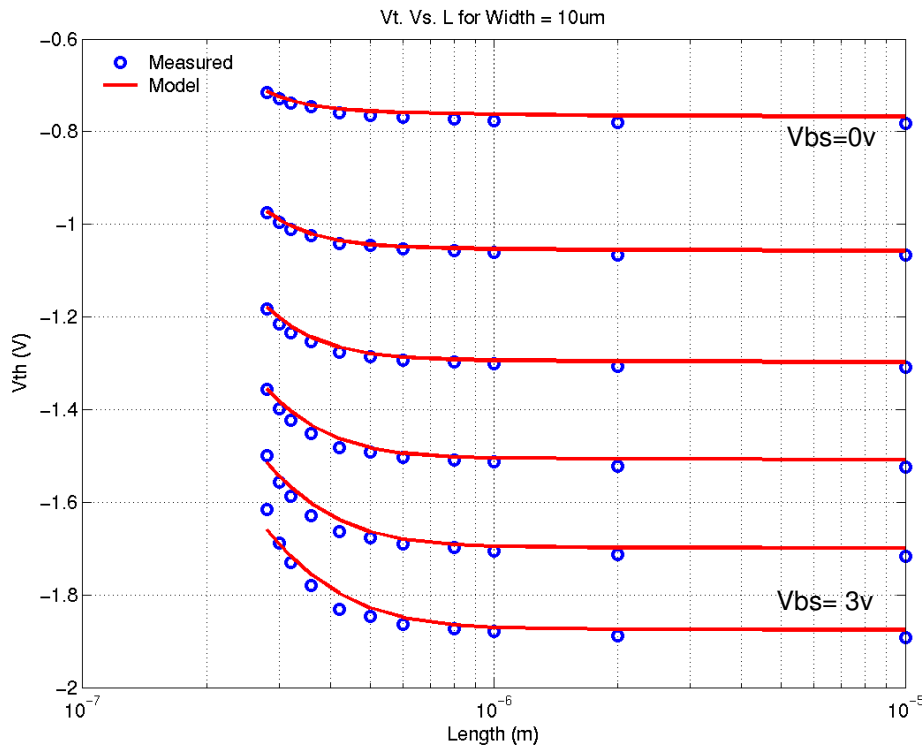


FIGURE 2.62 3p3v_pfet_vtVsW_25C

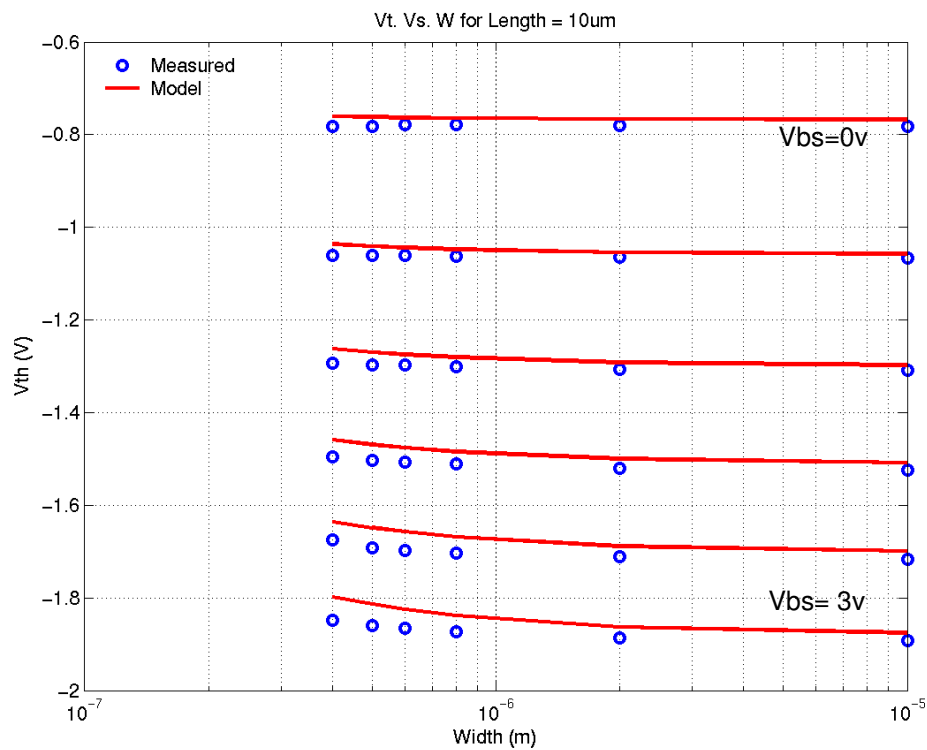


FIGURE 2.63 3p3v_pfet_10x10_idvg_25C

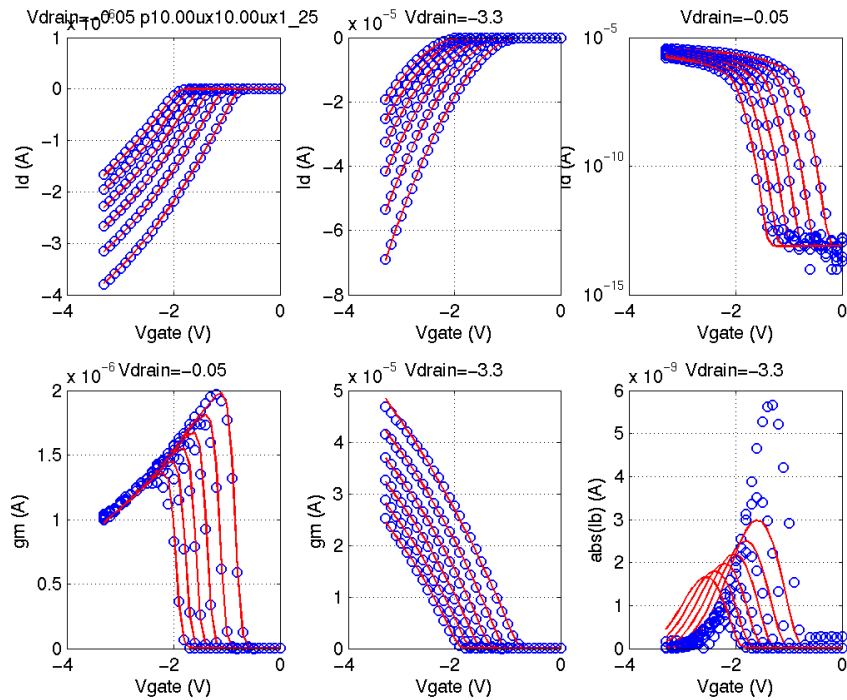


FIGURE 2.64 3p3v_pfet_10x10_idvd_25C

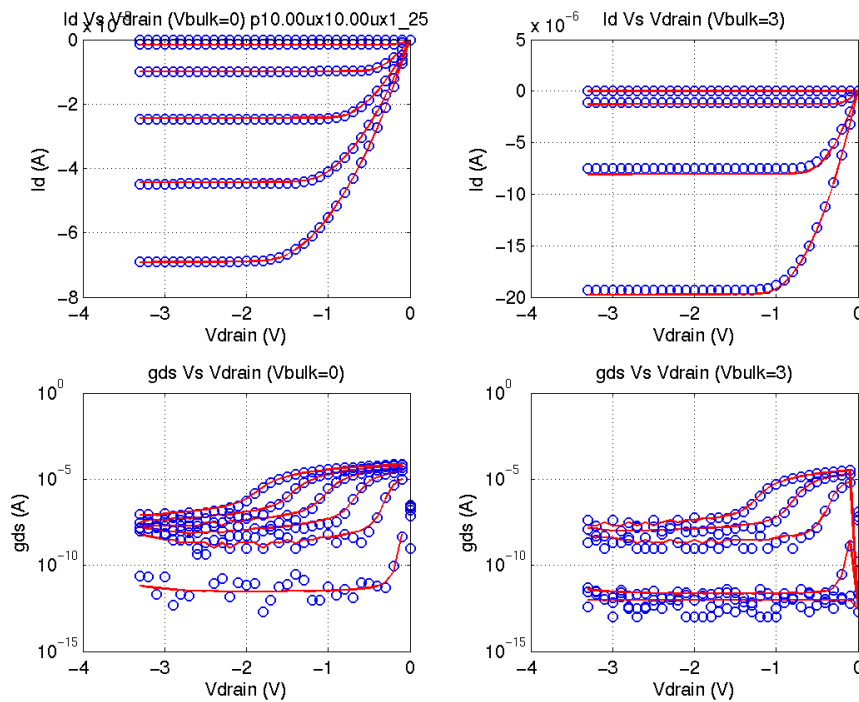


FIGURE 2.65 3p3v_pfet_10x0p3_idvg_25C

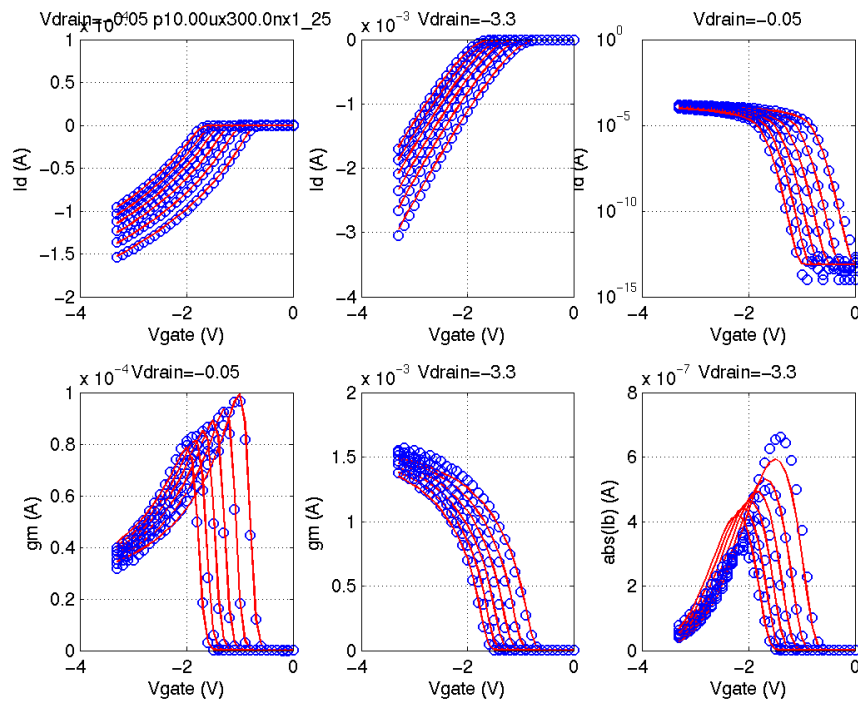


FIGURE 2.66 3p3v_pfet_10x0p3_idvd_25C

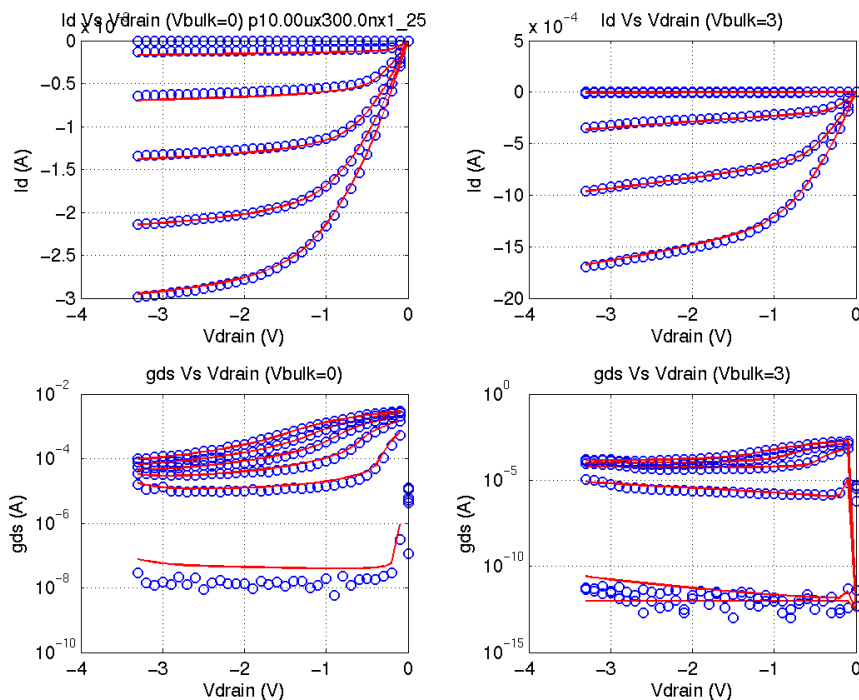


FIGURE 2.67 3p3v_pfet_0p4x10_idvg_25C

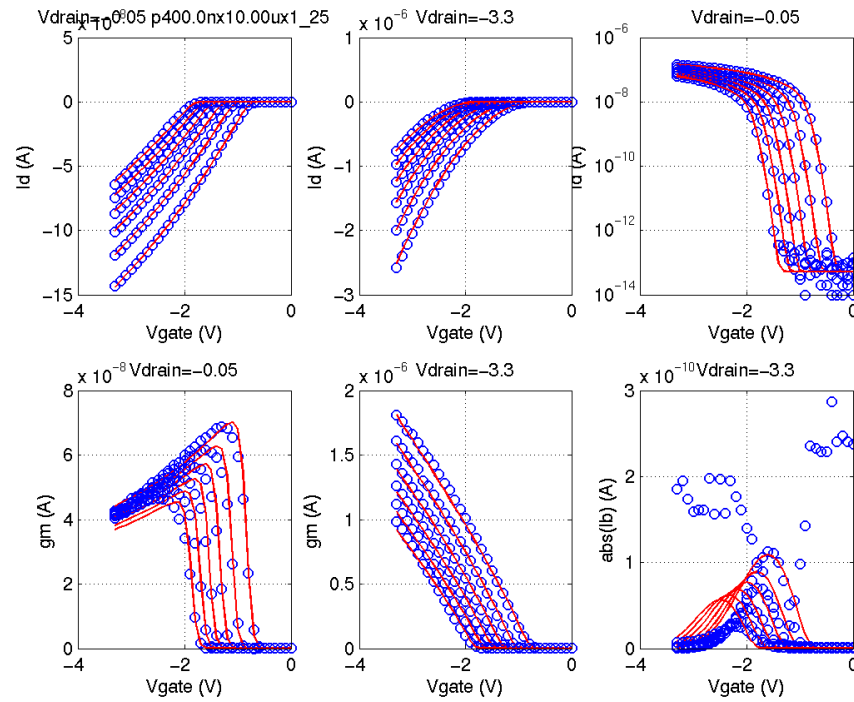


FIGURE 2.68 3p3v_pfet_0p4x10_idvd_25C

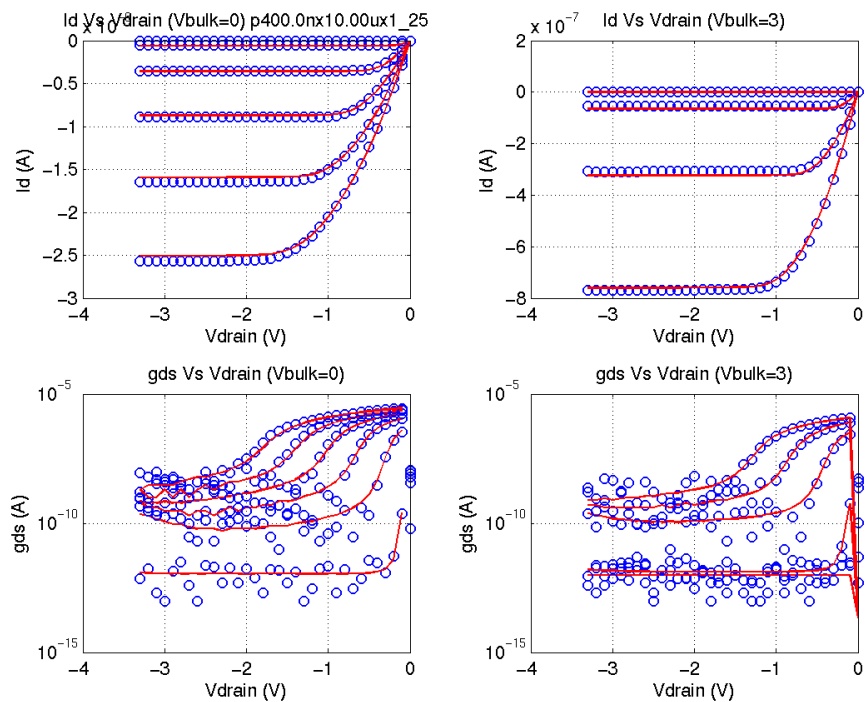


FIGURE 2.69 3p3v_pfet_0p4x0p3_idvg_25C

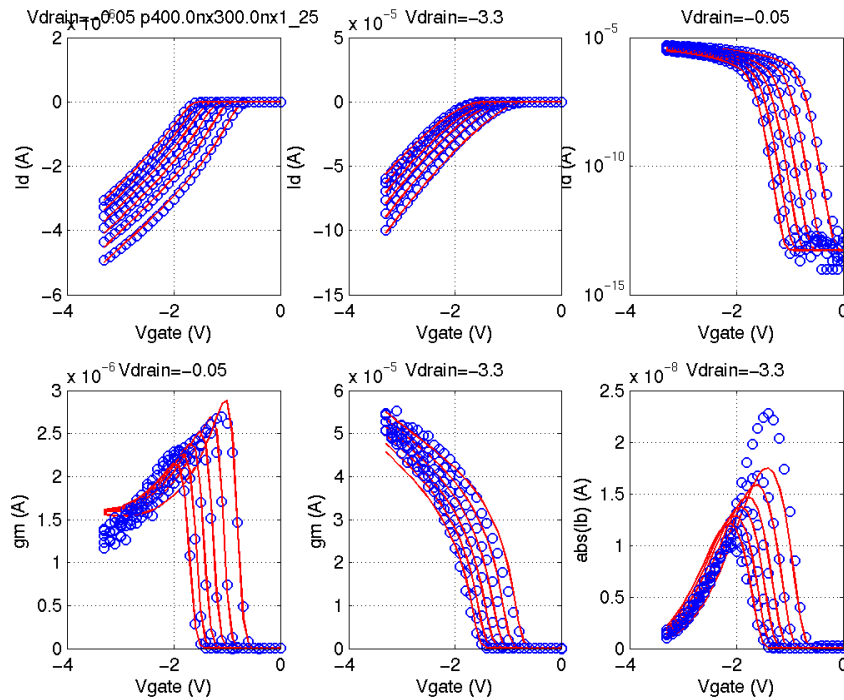


FIGURE 2.70 3p3v_pfet_0p4x0p3_idvd_25C

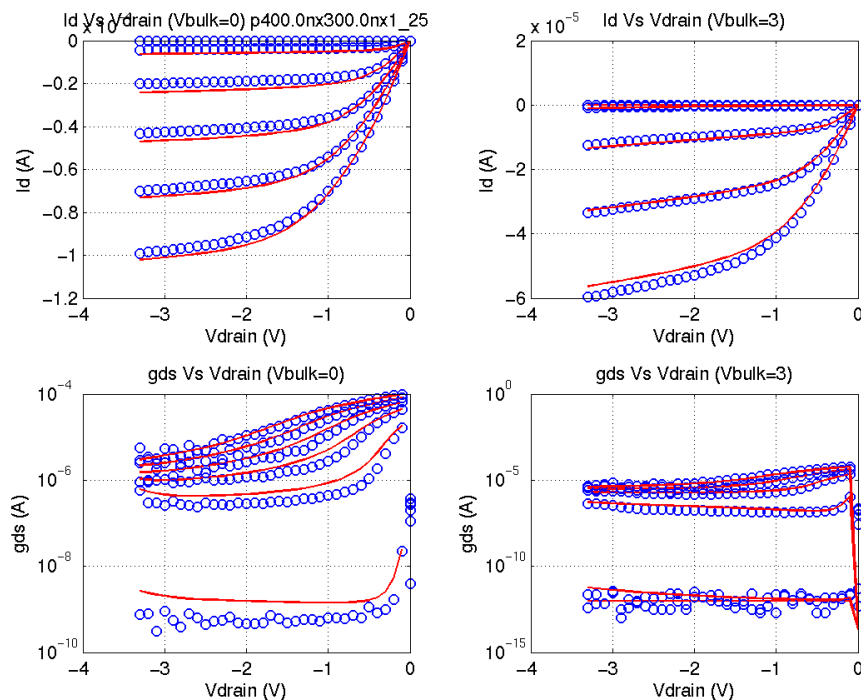


FIGURE 2.71 3p3v_pfet_0p6x0p3_idvg_25C

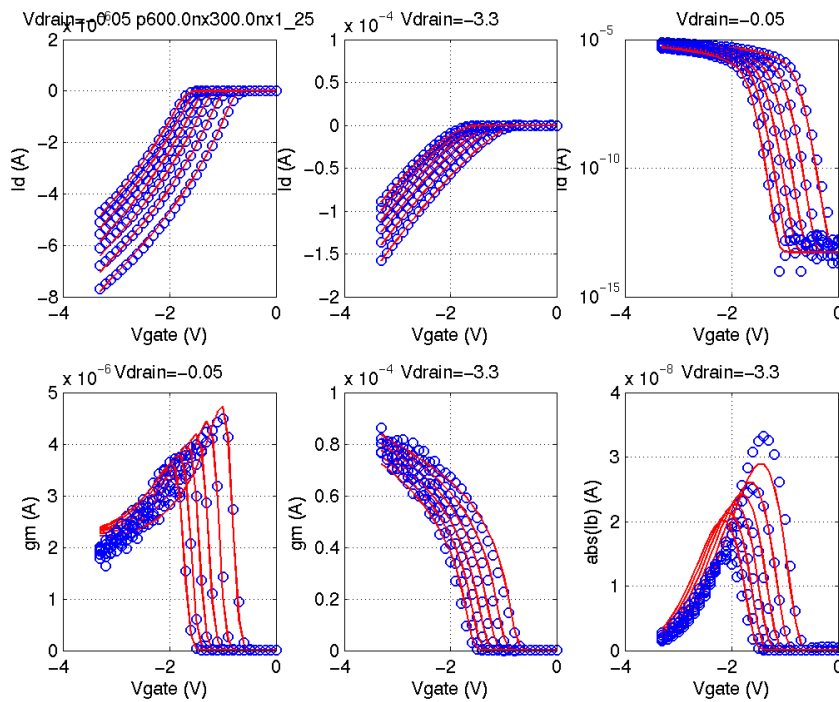


FIGURE 2.72 3p3v_pfet_0p6x0p3_idvd_25C

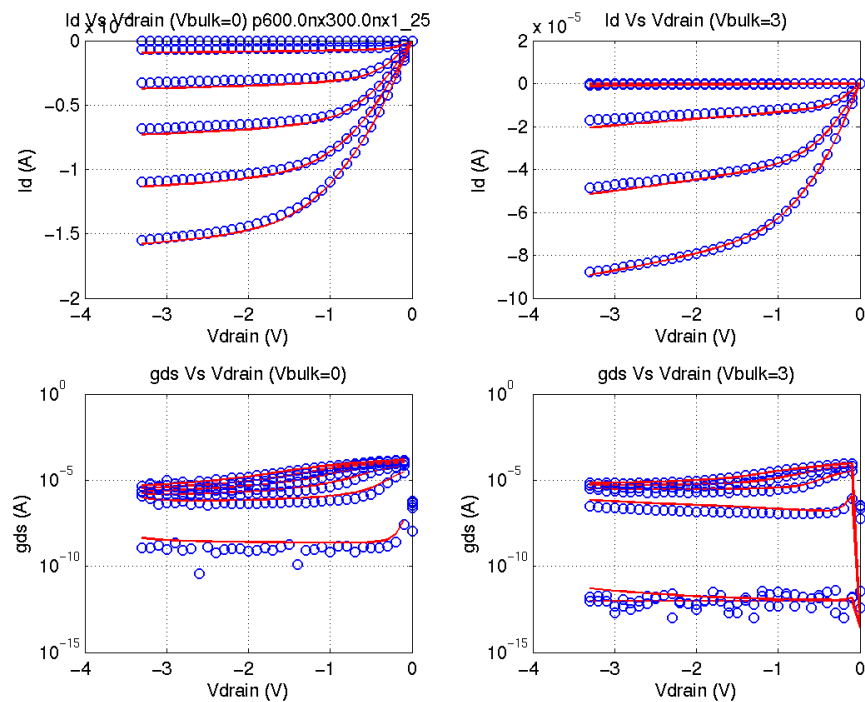


FIGURE 2.73 3p3v_pfet_10x0p6_idvg_25C

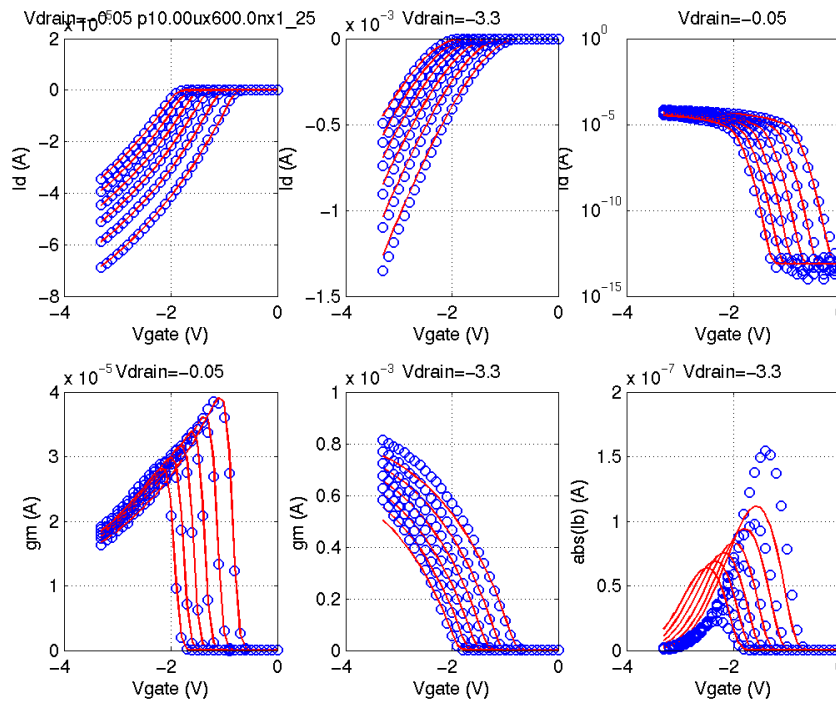


FIGURE 2.74 3p3v_pfet_10x0p6_idvd_25C

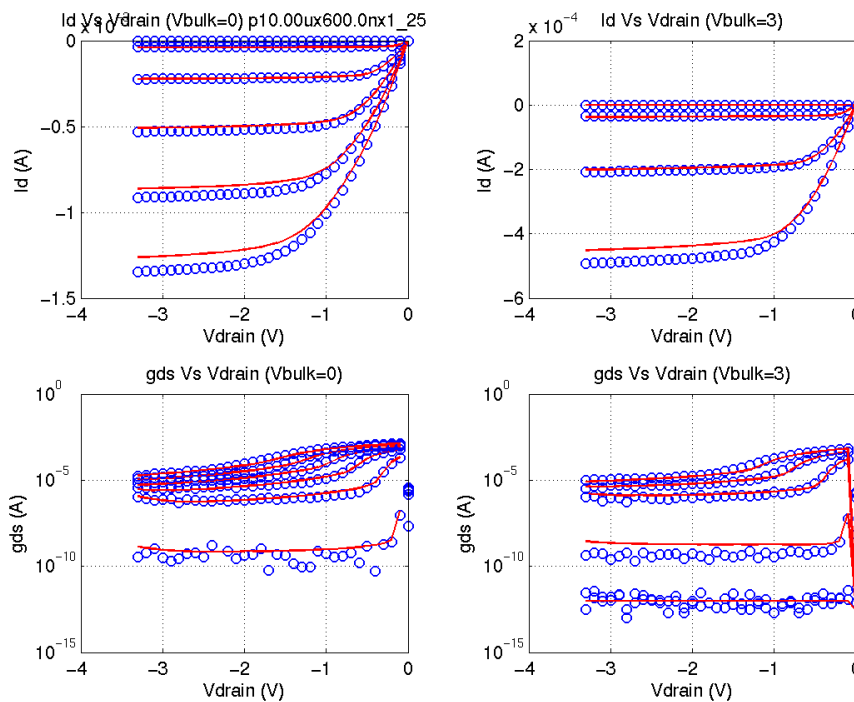


FIGURE 2.75 3p3v_pfet_10x0p3_idvg_-40C

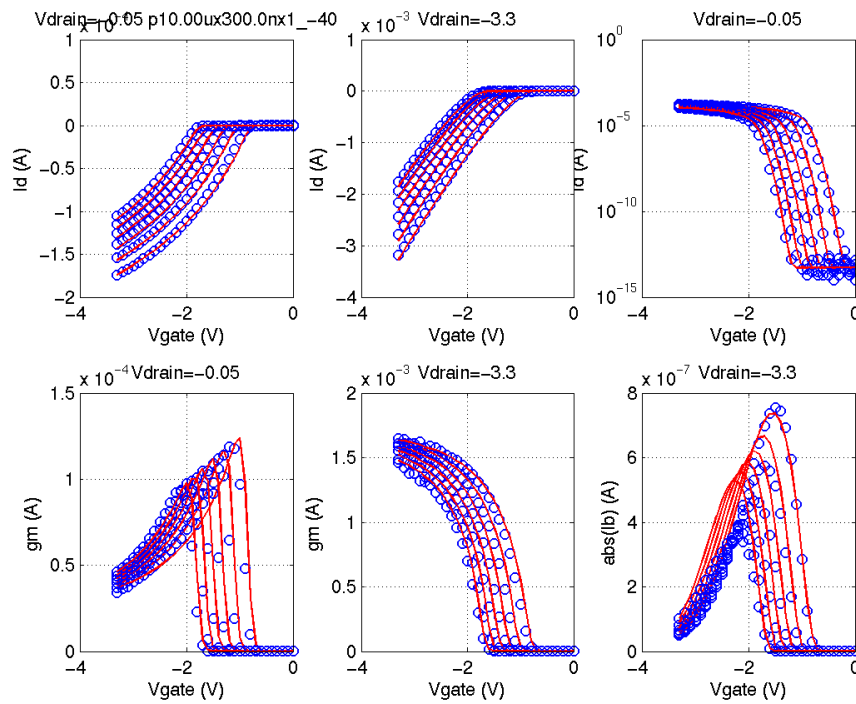


FIGURE 2.76 3p3v_pfet_10x0p3_idvd_-40C

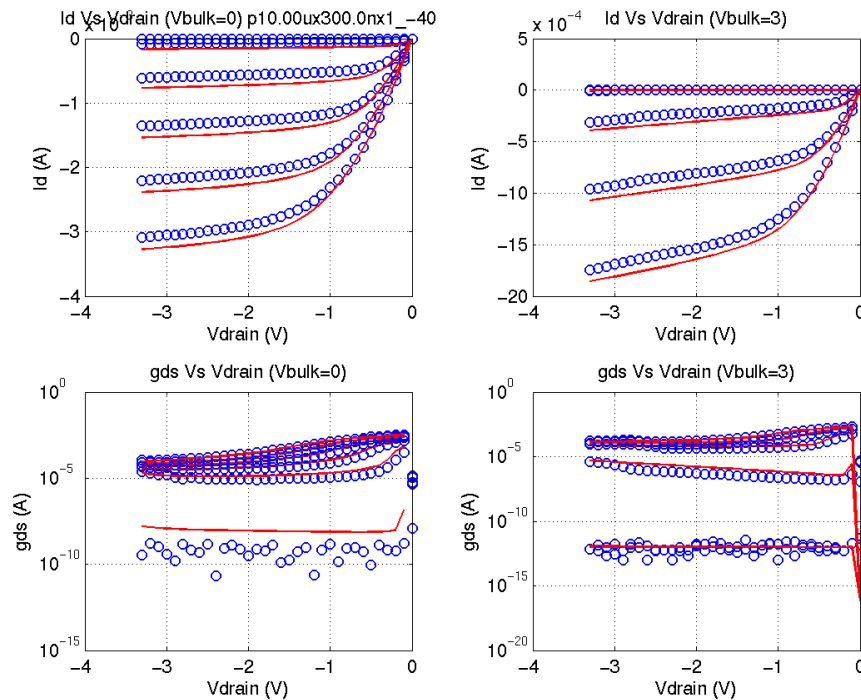


FIGURE 2.77 3p3v_pfet_10x0p3_idvg_125C

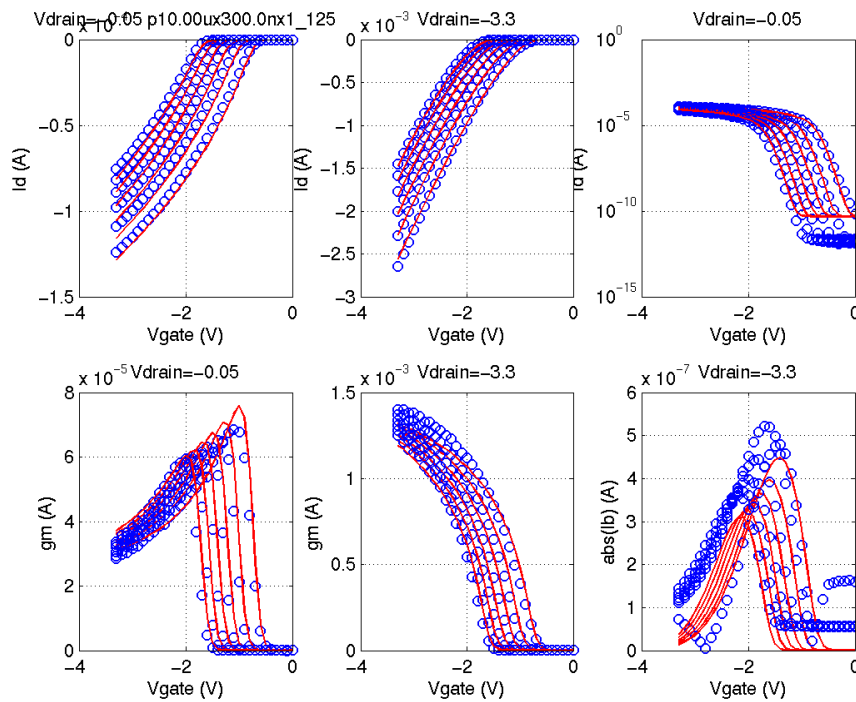


FIGURE 2.78 3p3v_pfet_10x0p3_idvd_125C

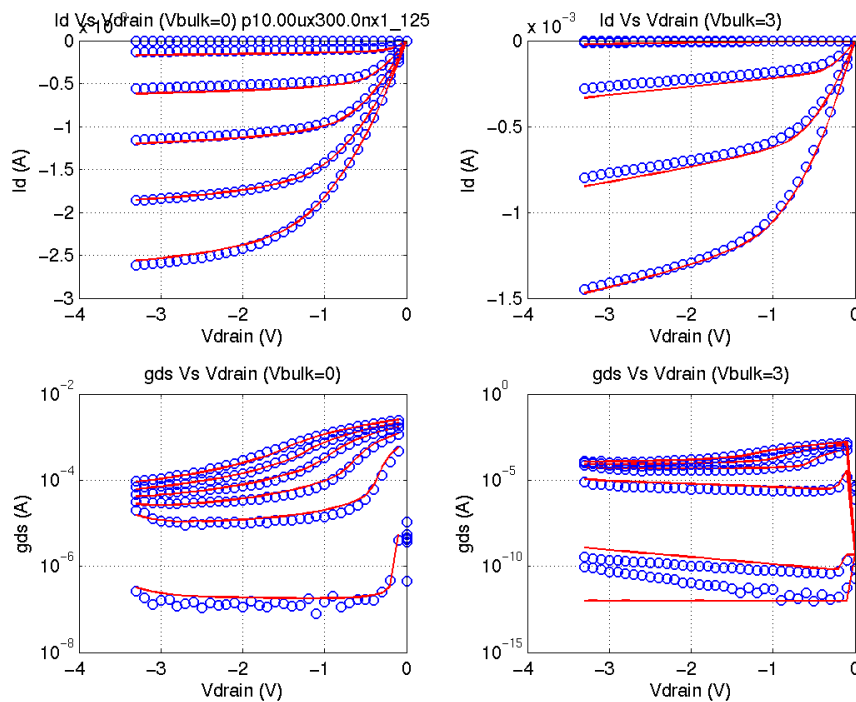


FIGURE 2.79 5p0_NFET_cv

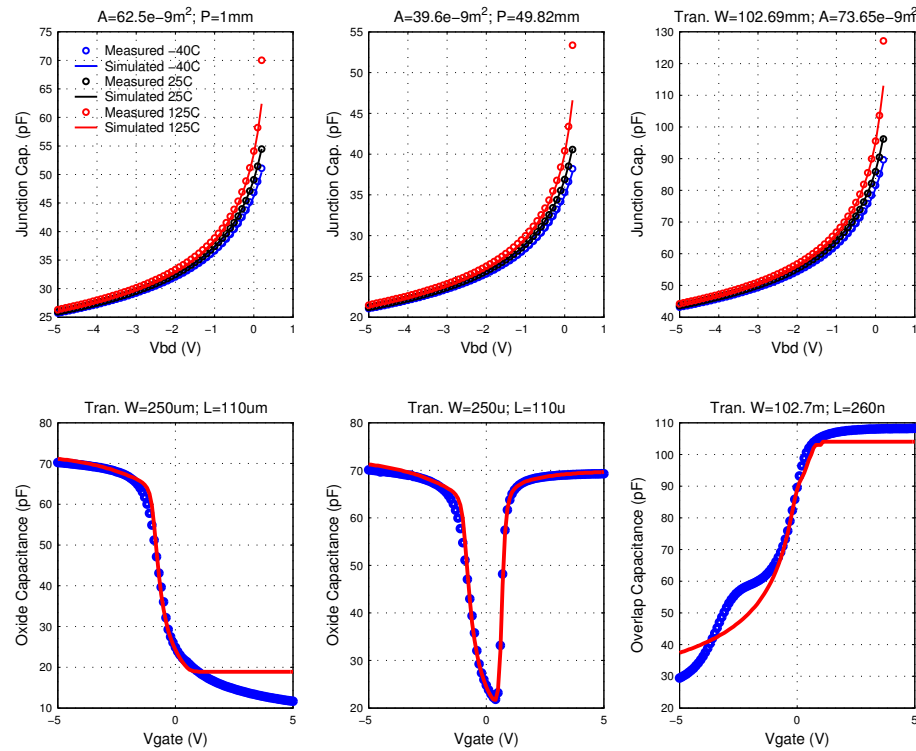


FIGURE 2.80 5p0_NFET_vtVsL_25C

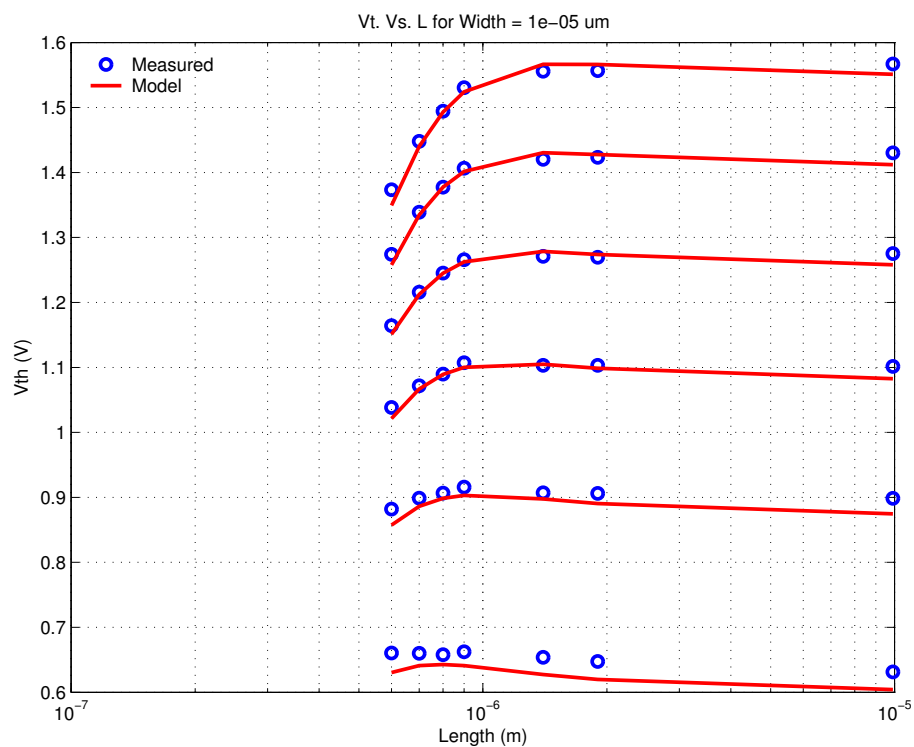


FIGURE 2.81 5p0_NFET_vtVsW_25C

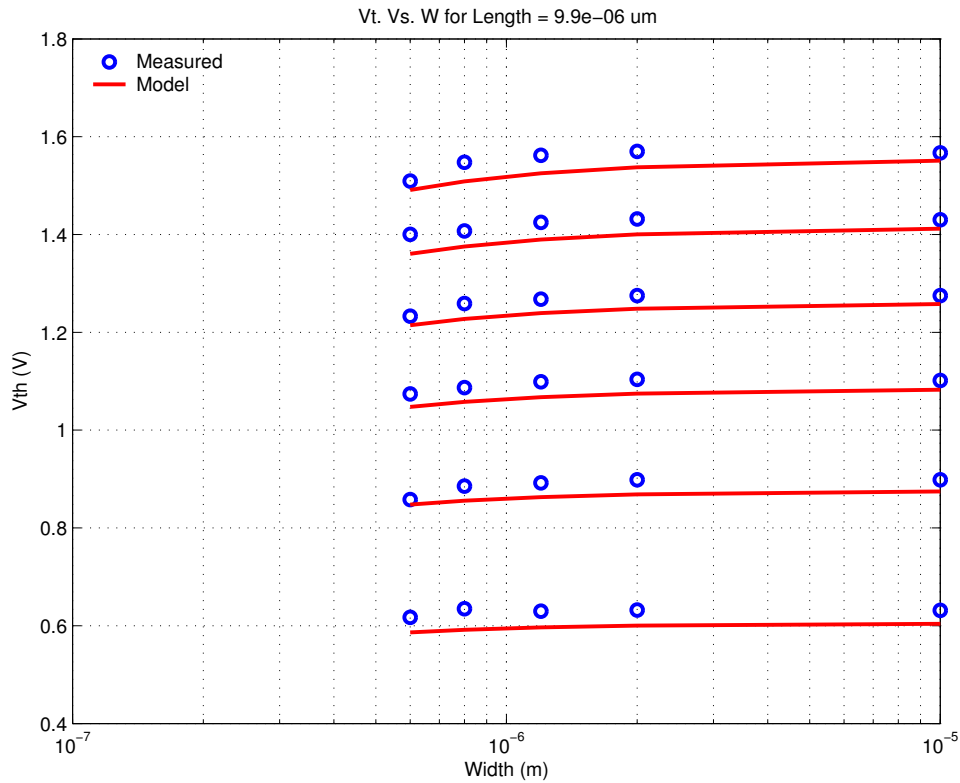


FIGURE 2.82 5p0_NFET_10x9p9_idvd_25C

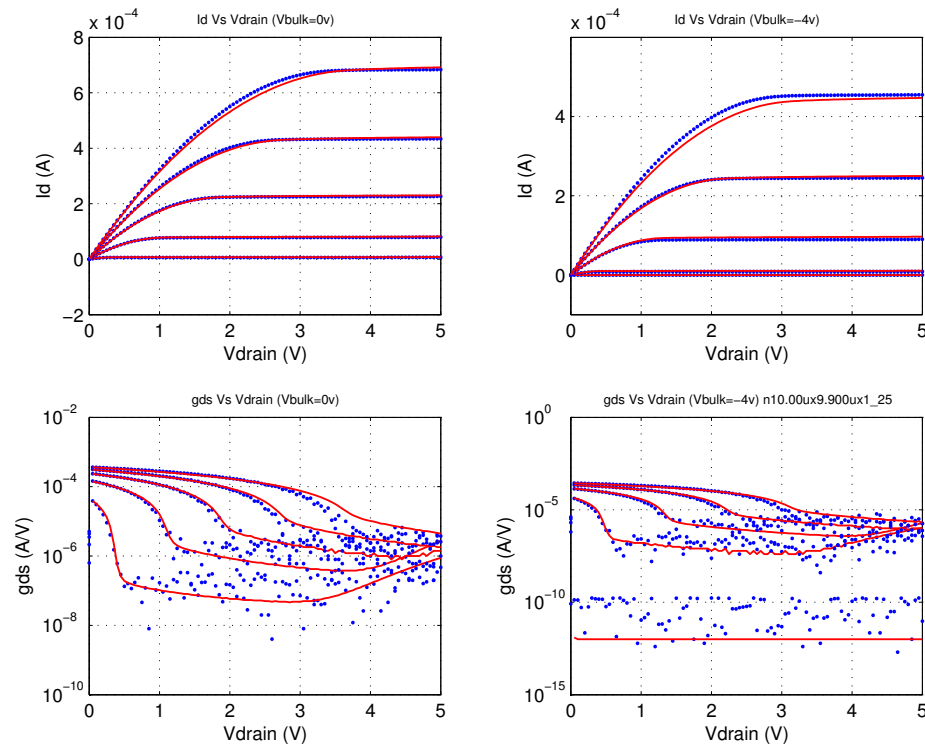


FIGURE 2.83 5p0_NFET_10x9p9_idvg_25C

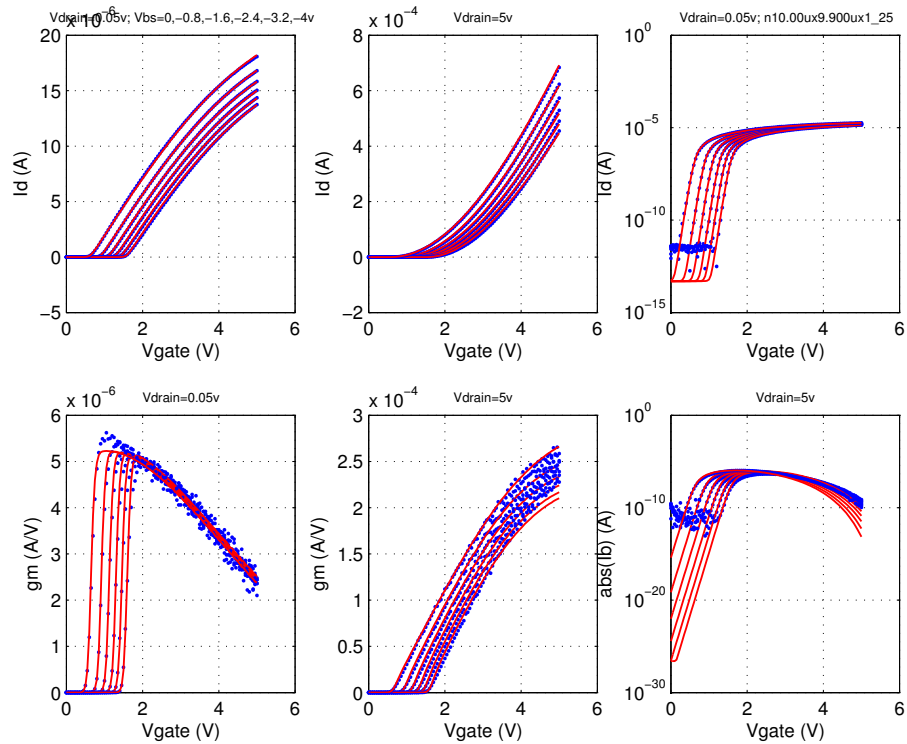


FIGURE 2.84 5p0_NFET_10x0p6_idvd_25C

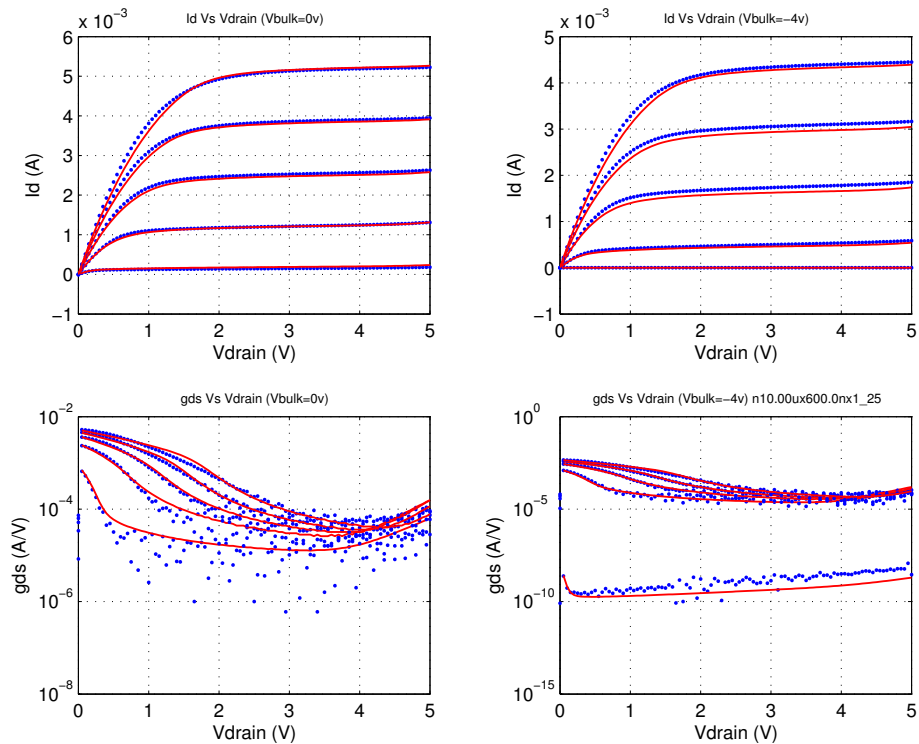


FIGURE 2.85 5p0_NFET_10x0p6_idvg_25C

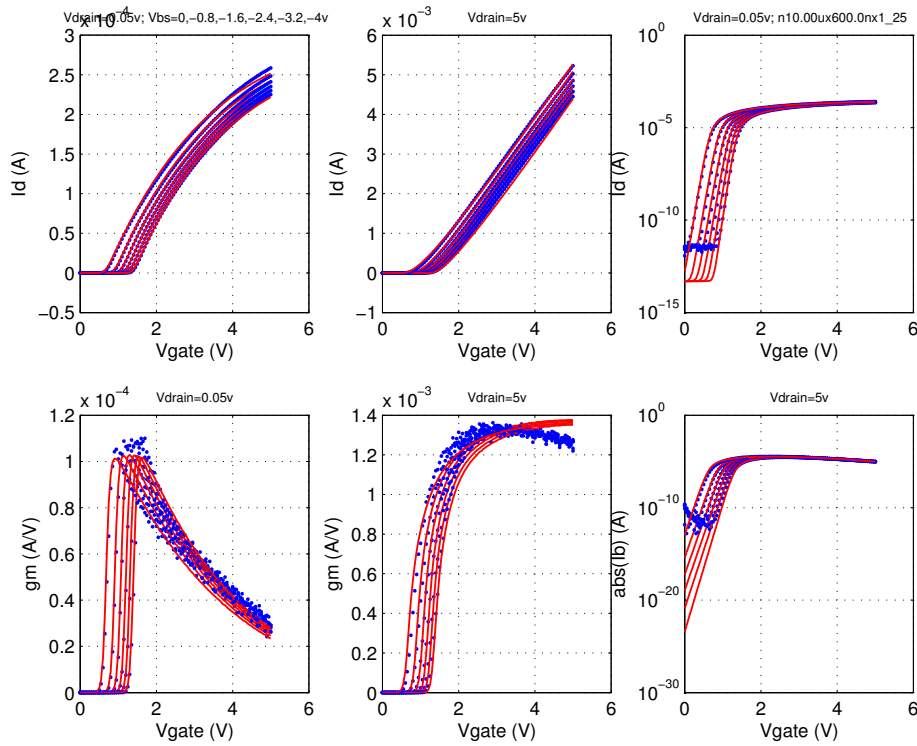


FIGURE 2.86 5p0_NFET_0p6x9p9_idvd_25C

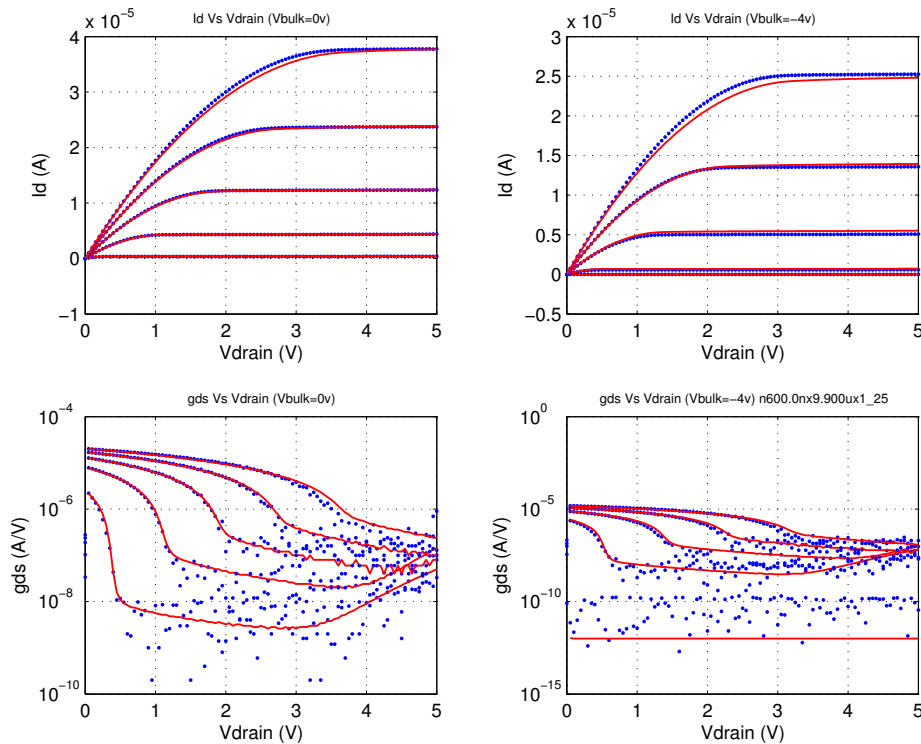


FIGURE 2.87 5p0_NFET_0p6x9p9_idvg_25C

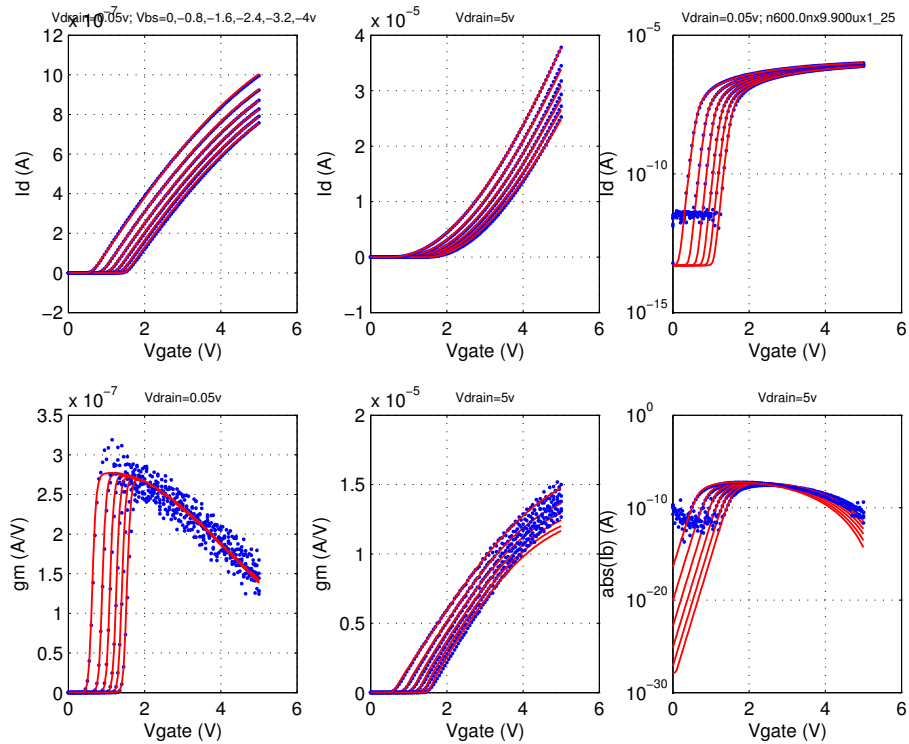


FIGURE 2.88 5p0_NFET_0p6x0p7_idvd_25C

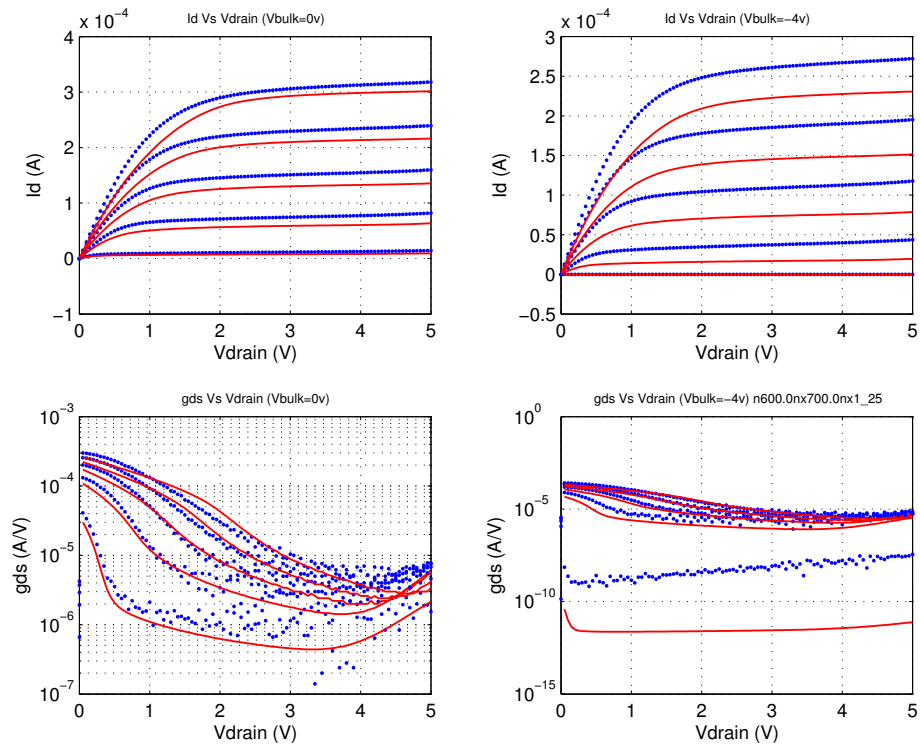


FIGURE 2.89 5p0_NFET_0p6x0p7_idvg_25C

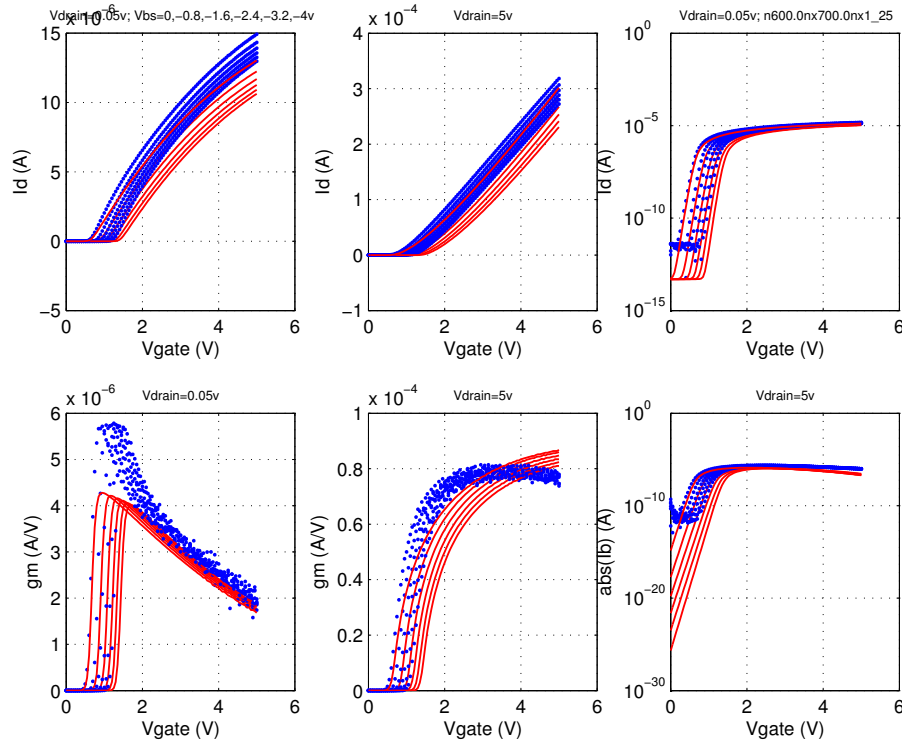


FIGURE 2.90 5p0_NFET_0p7x0p7_idvd_25C

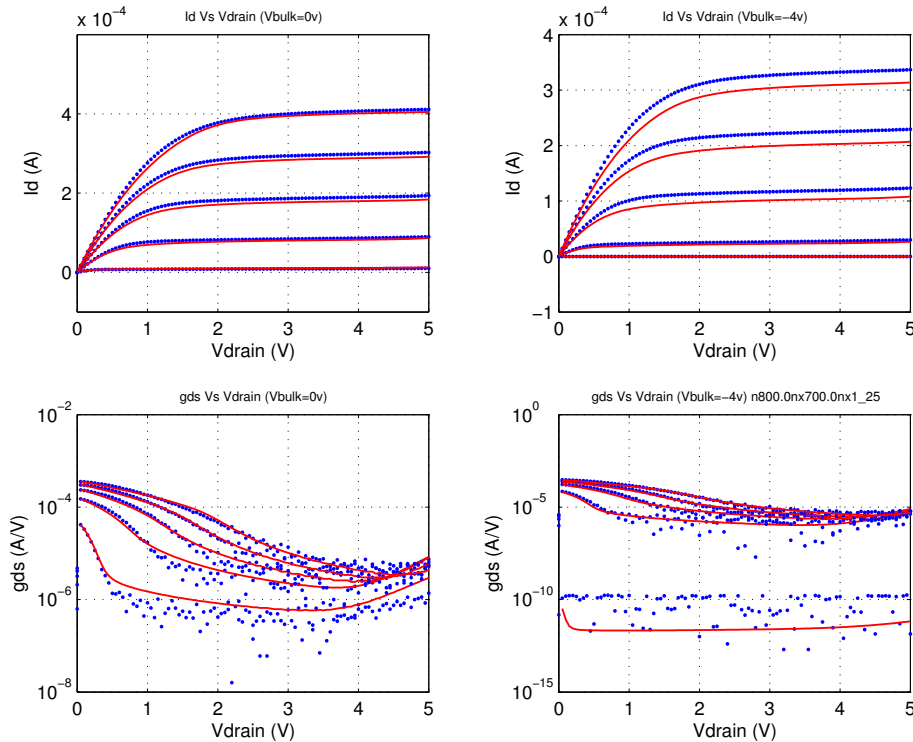


FIGURE 2.91 5p0_NFET_0p7x0p7_idvg_25C

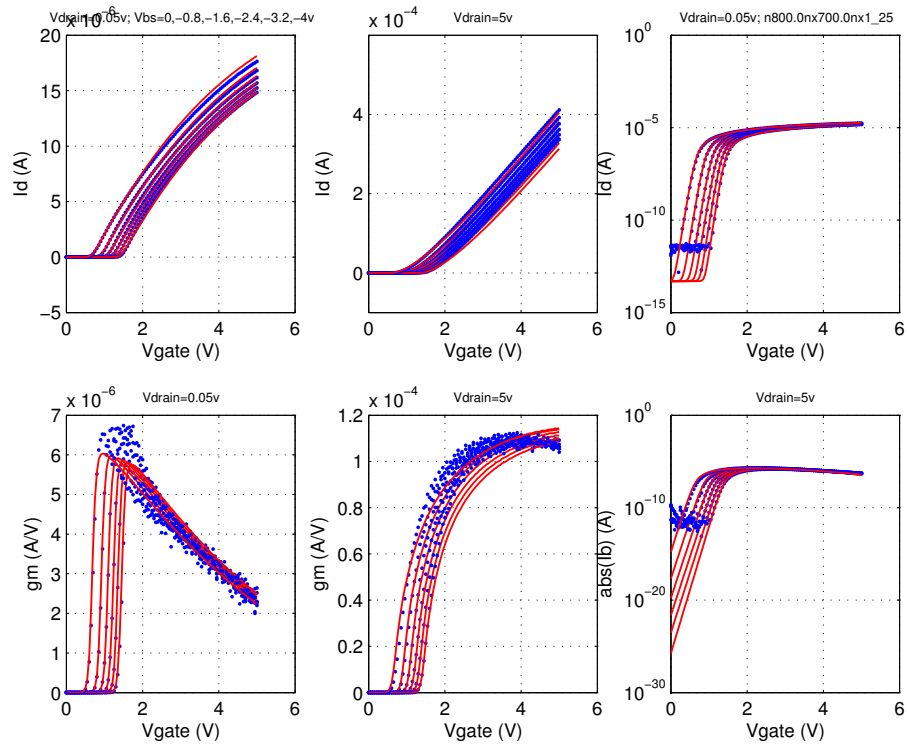


FIGURE 2.92 5p0_NFET_10x0p8_idvd_25C

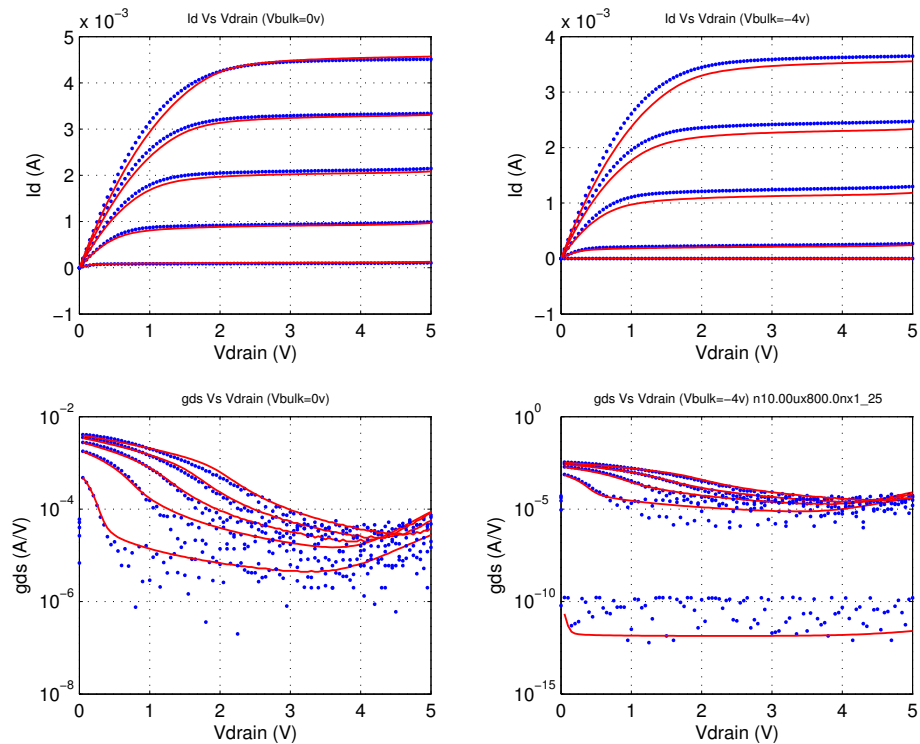


FIGURE 2.93 5p0_NFET_10x0p8_idvg_25C

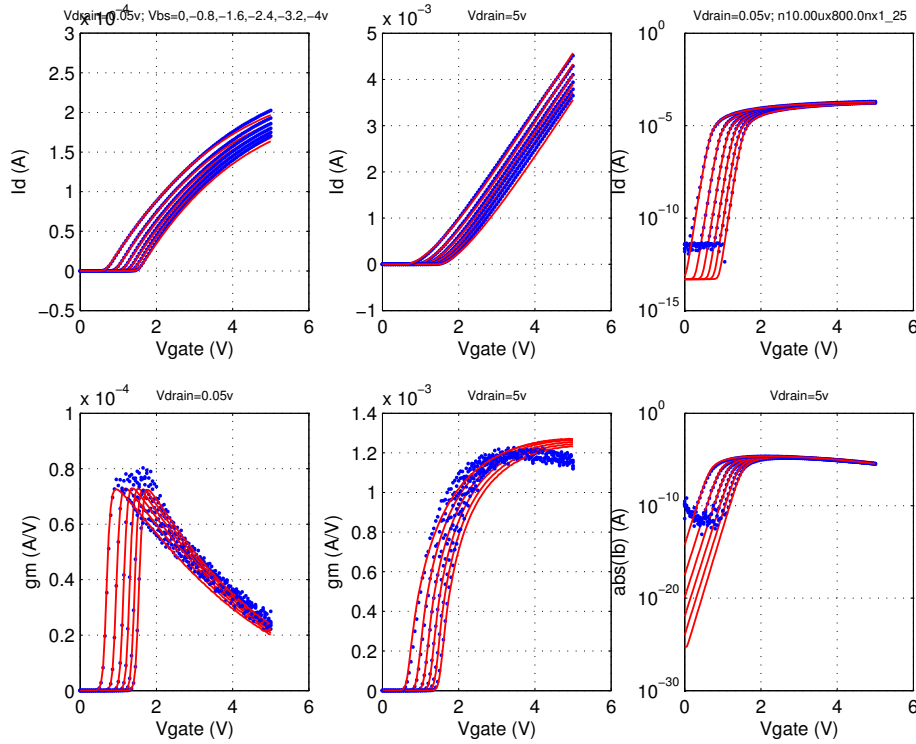


FIGURE 2.94 5p0_NFET_10x0p6_idvd_-40C

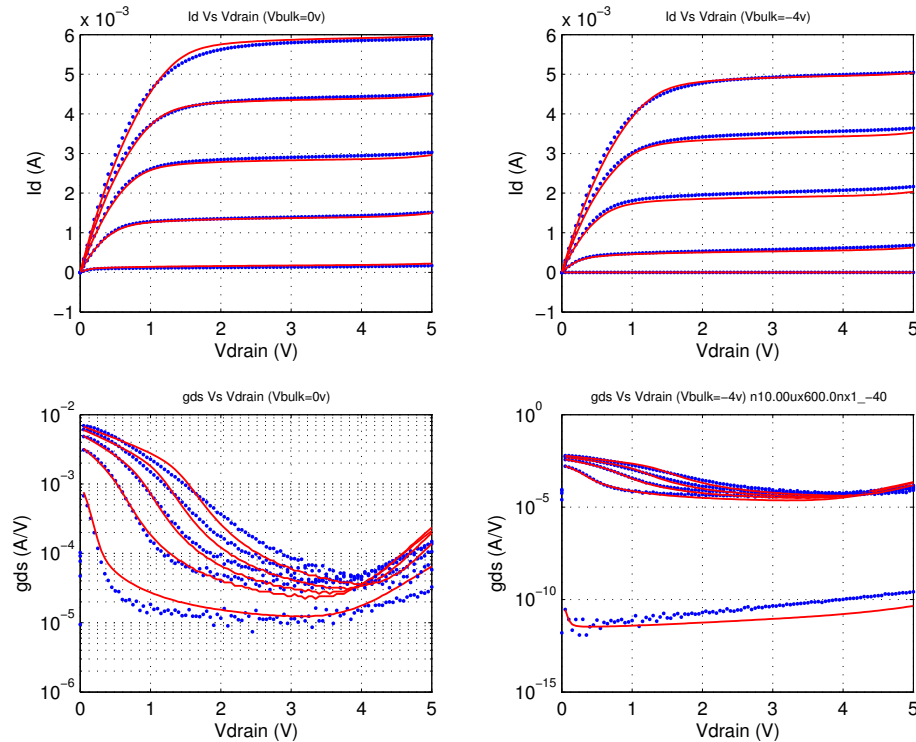


FIGURE 2.95 5p0_NFET_10x0p6_idvg_-40C

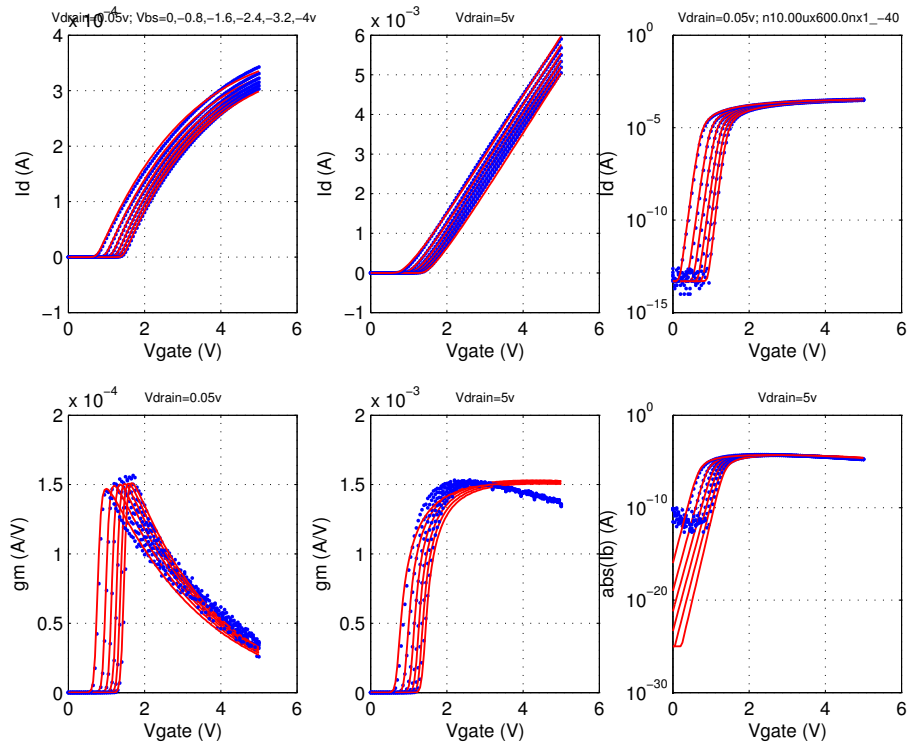


FIGURE 2.96 5p0_NFET_10x0p6_idvd_125C

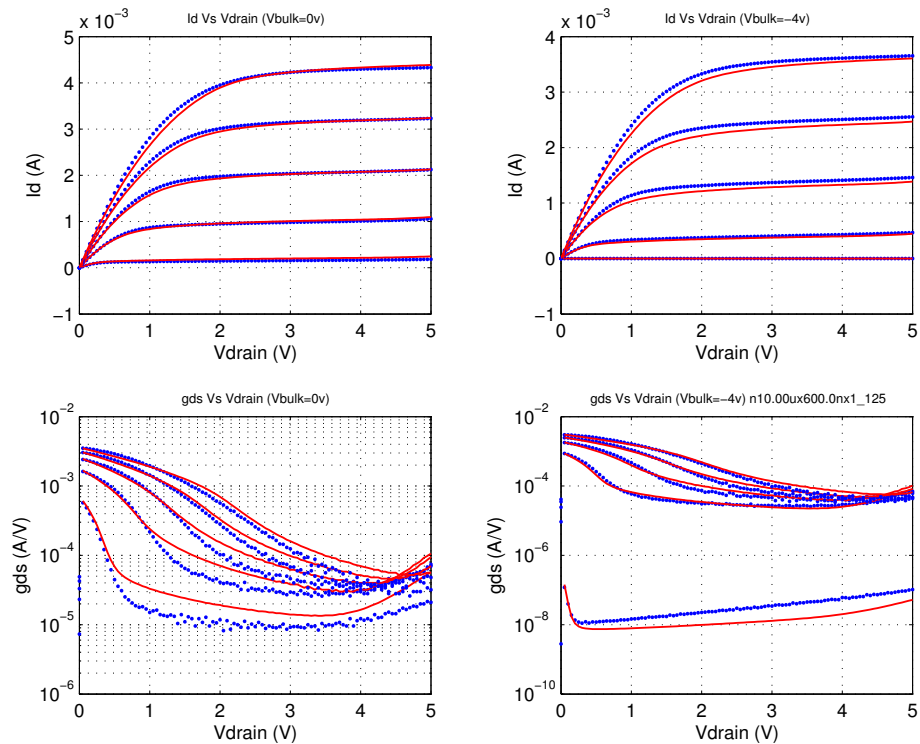


FIGURE 2.97 5p0_NFET_10x0p6_idvg_125C

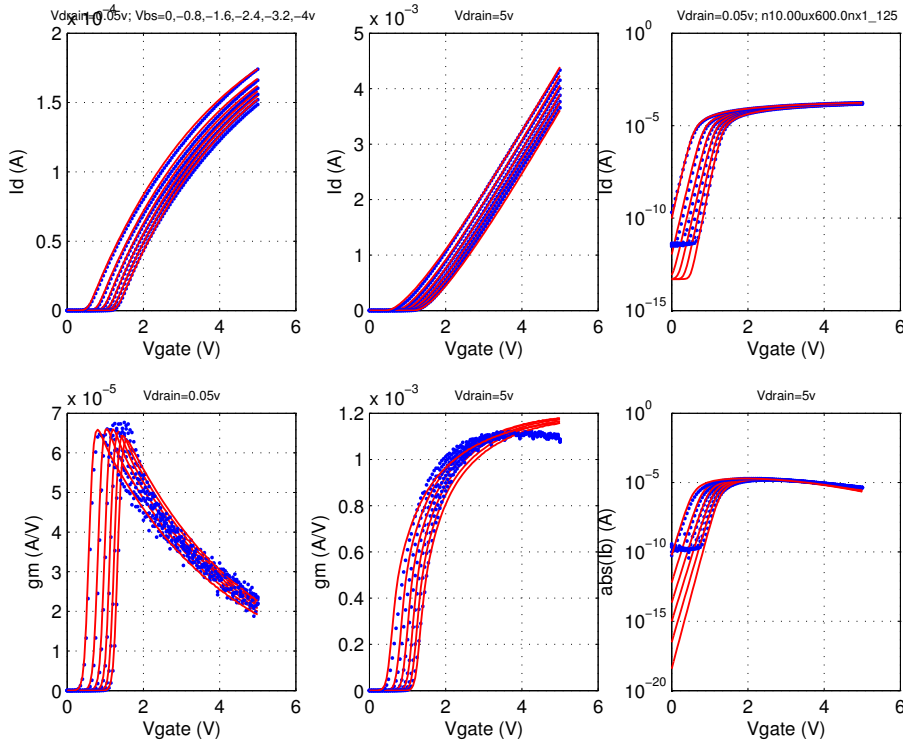


FIGURE 2.98 5p0_PFET_cv

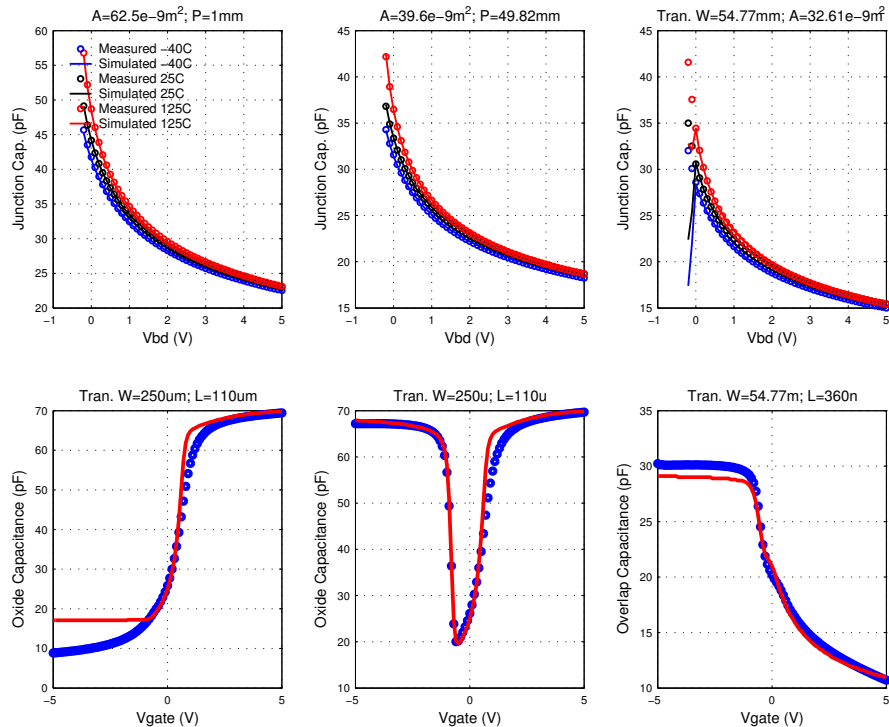


FIGURE 2.99 5p0_PFET_vtVsL_25C

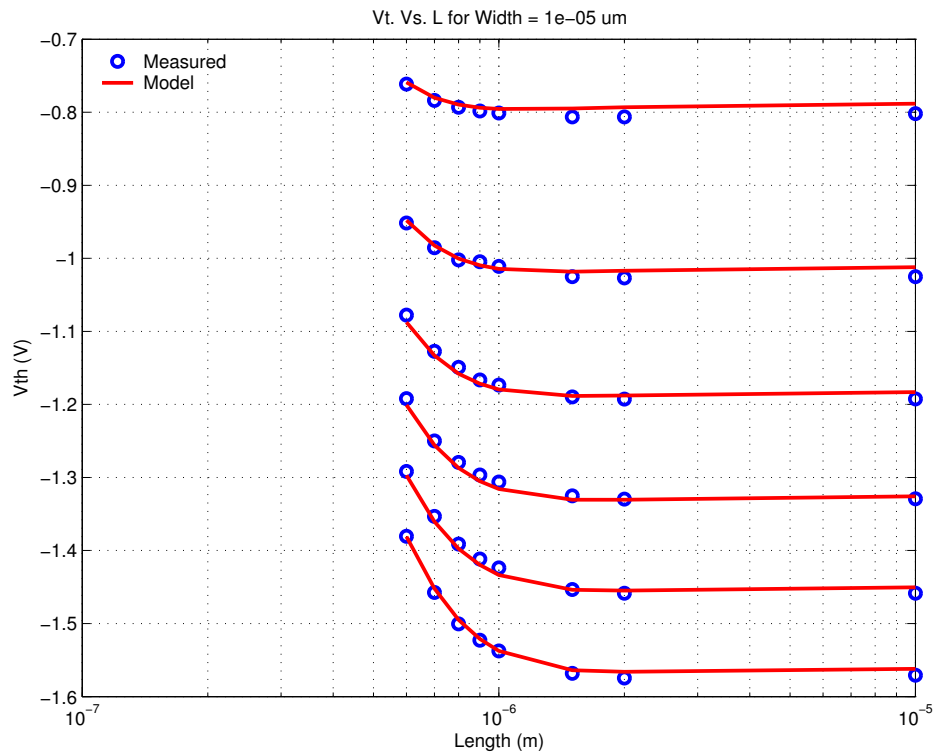


FIGURE 2.100 5p0_PFET_vtVsW_25C

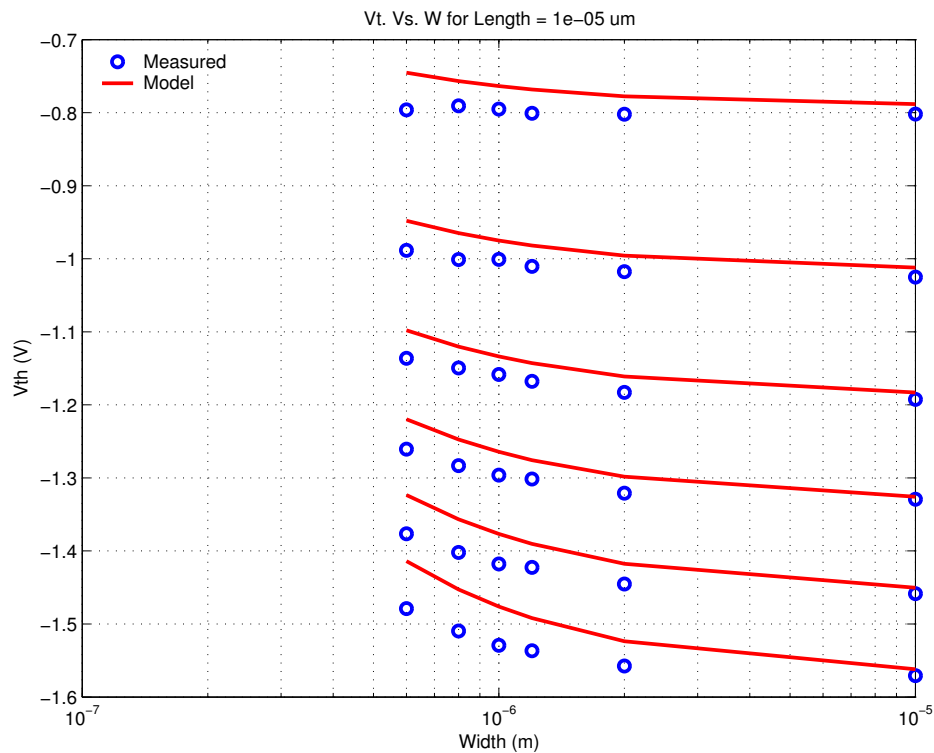


FIGURE 2.101 5p0_PFET_10x10_idvd_25C

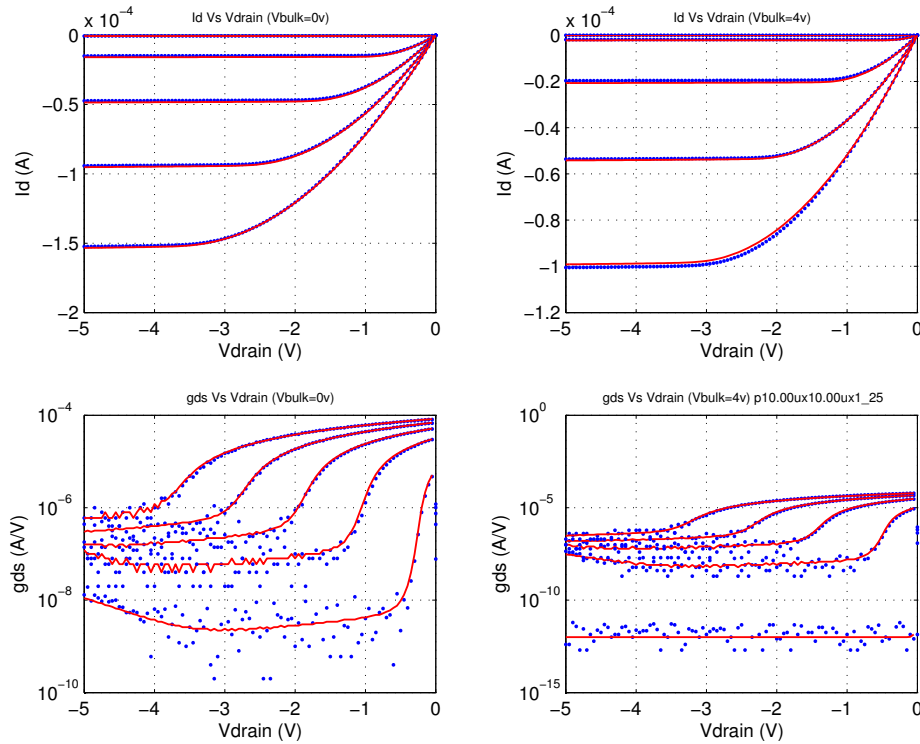


FIGURE 2.102 5p0_PFET_10x10_idvg_25C

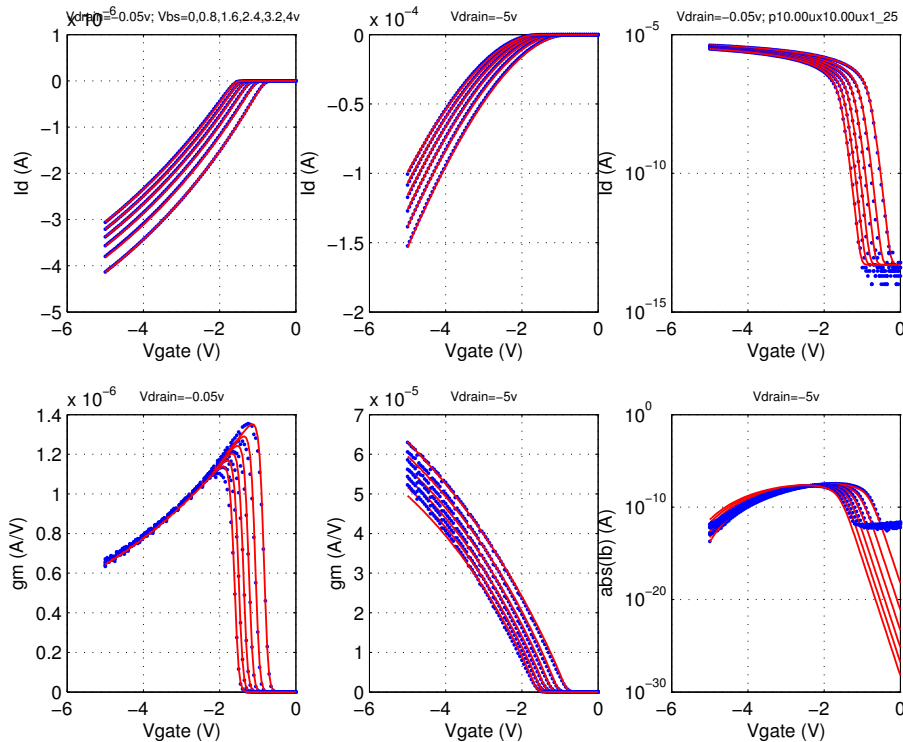


FIGURE 2.103 5p0_PFET_10x0p6_idvd_25C

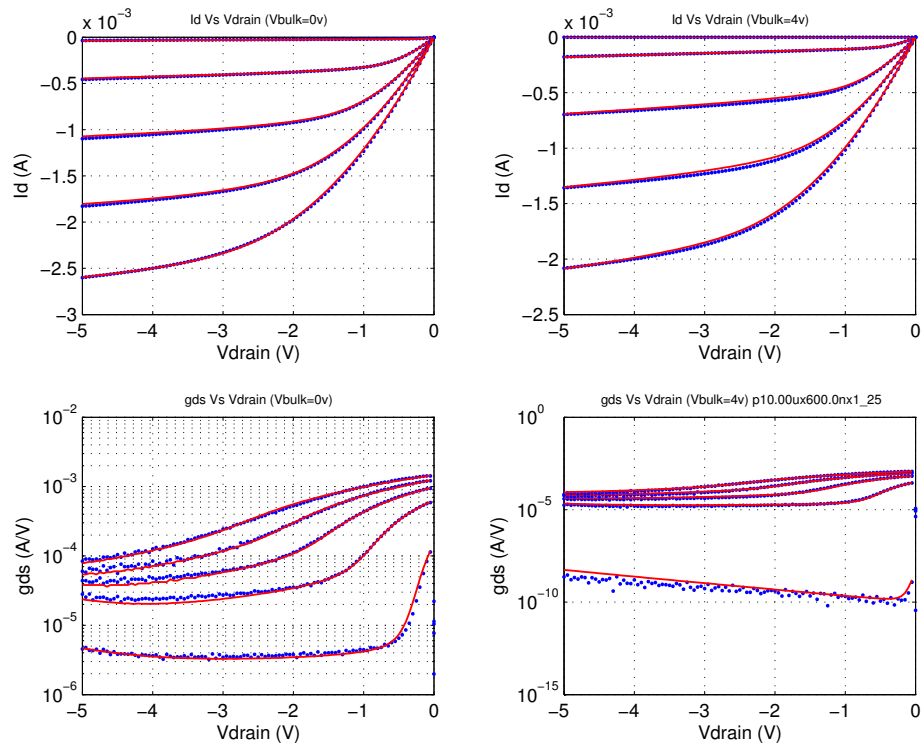


FIGURE 2.104 5p0_PFET_10x0p6_idvg_25C

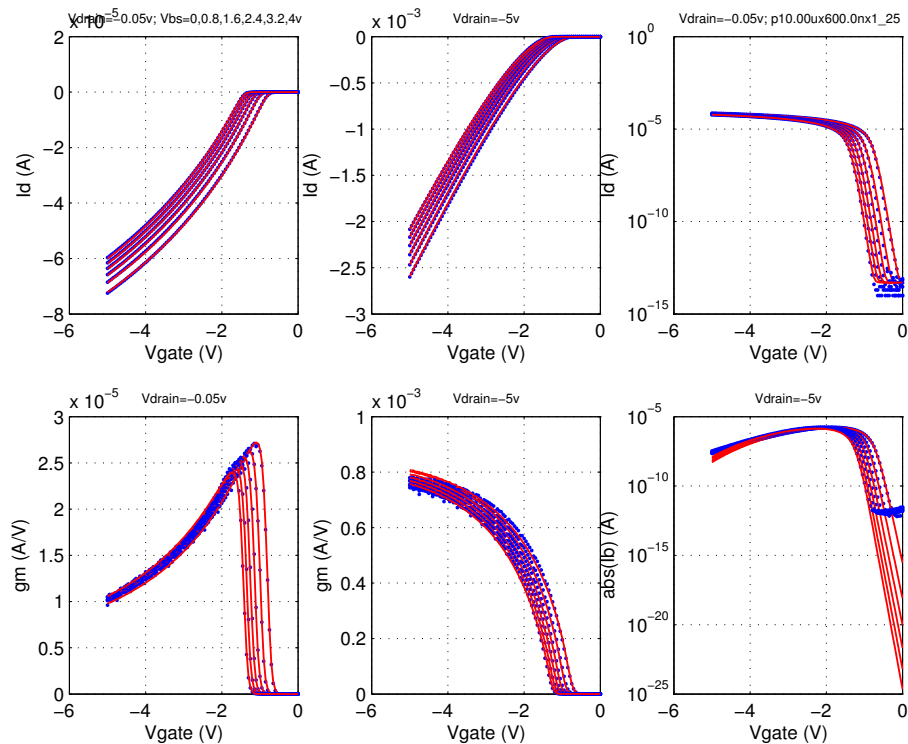


FIGURE 2.105 5p0_PFET_0p6x10_idvd_25C

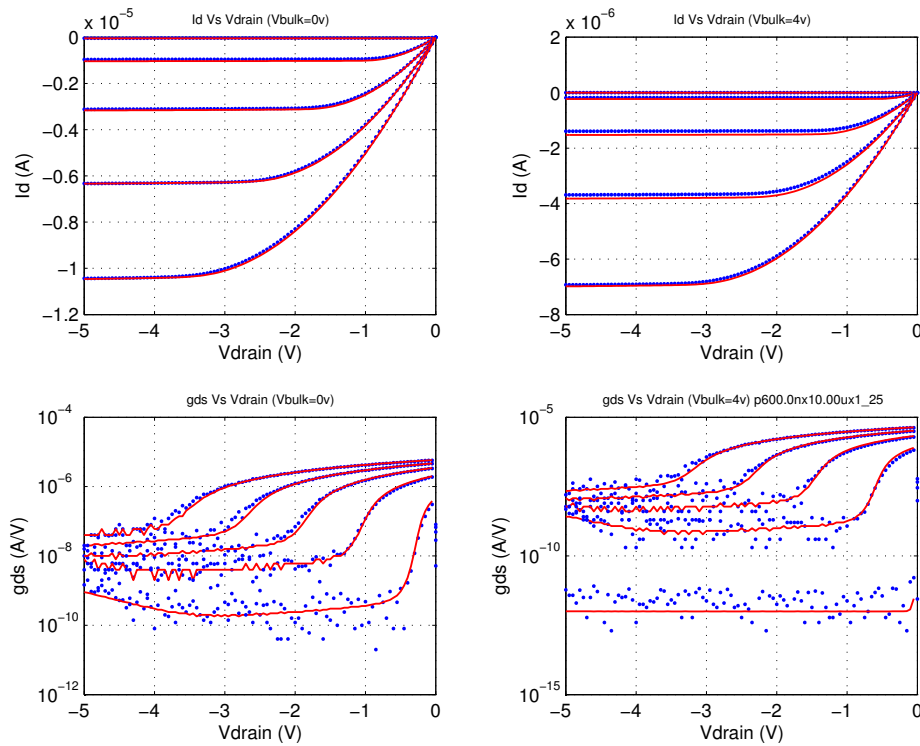


FIGURE 2.106 5p0_PFET_0p6x10_idvg_25C

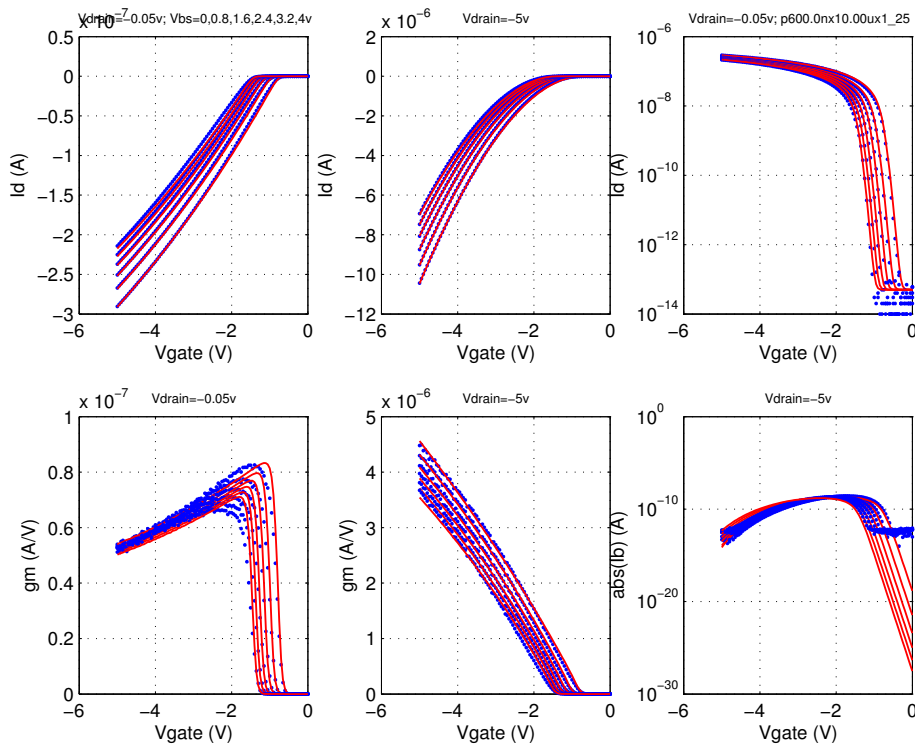


FIGURE 2.107 5p0_PFET_0p6x0p6_idvd_25C

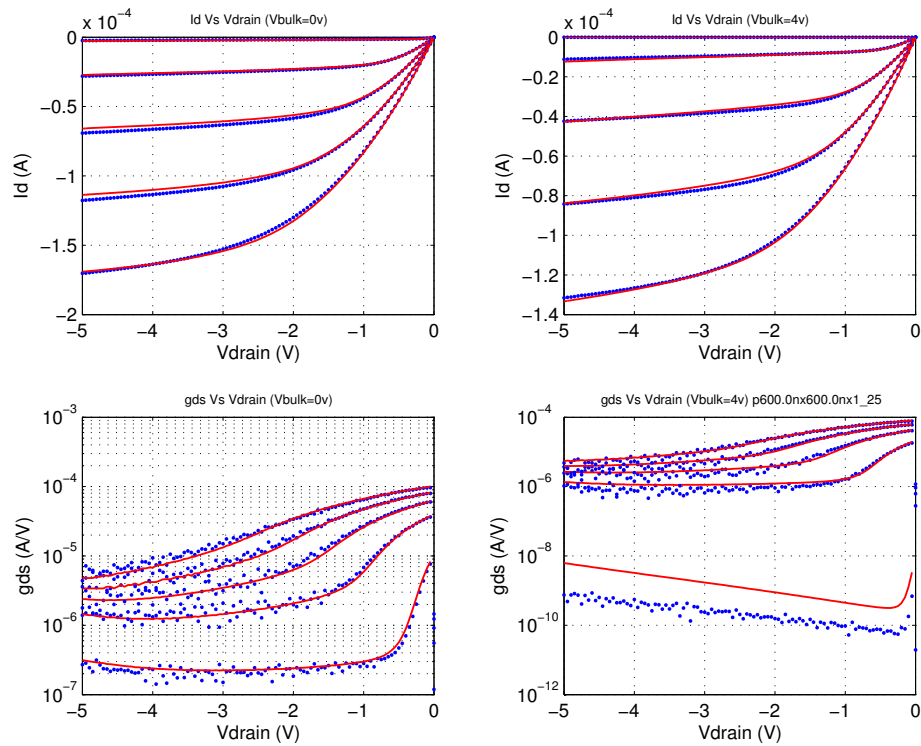


FIGURE 2.108 5p0_PFET_0p6x0p6_idvg_25C

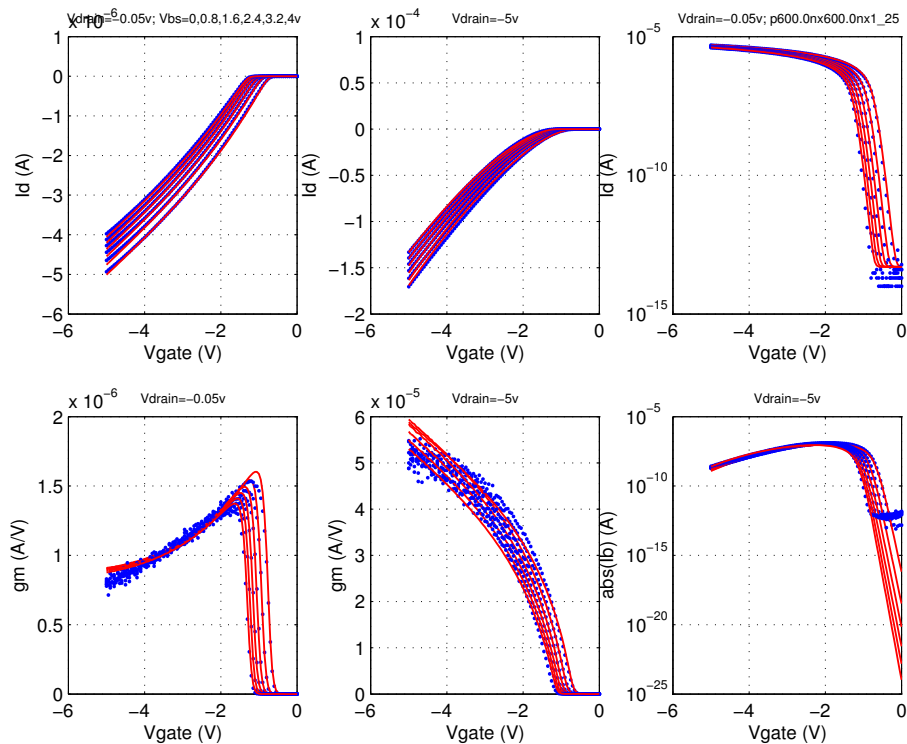


FIGURE 2.109 5p0_PFET_0p7x0p8_idvd_25C

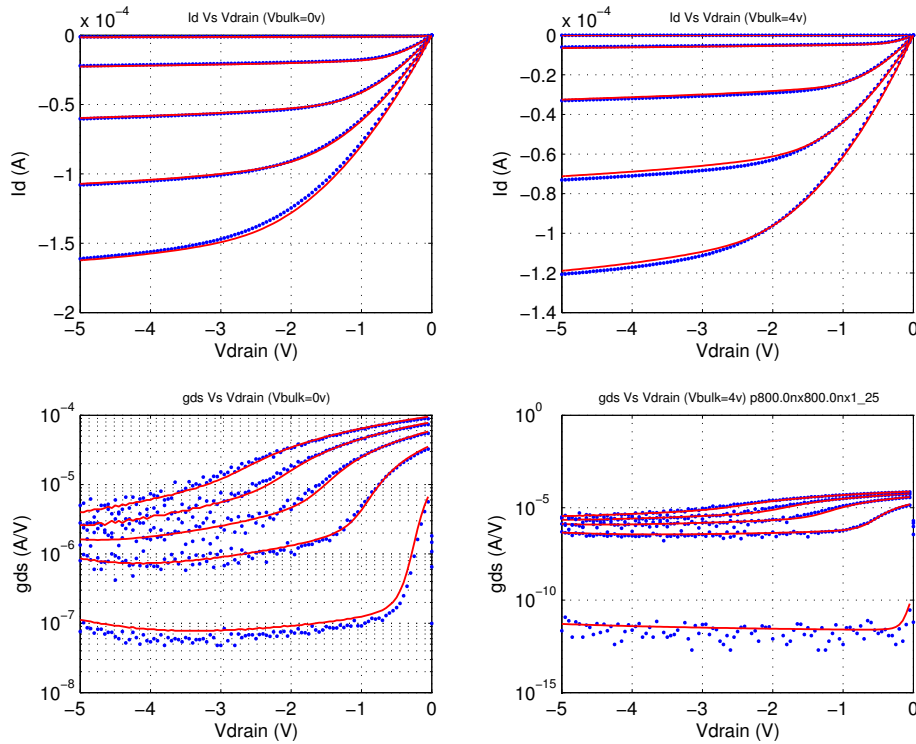


FIGURE 2.110 5p0_PFET_0p7x0p8_idvg_25C

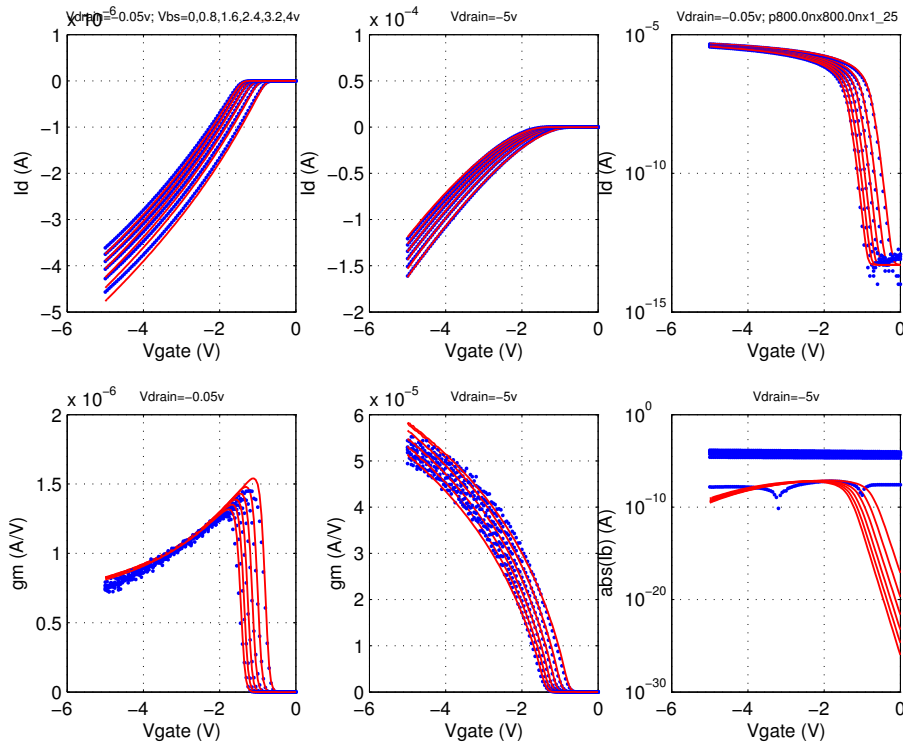


FIGURE 2.111 5p0_PFET_10x0p8_idvd_25C

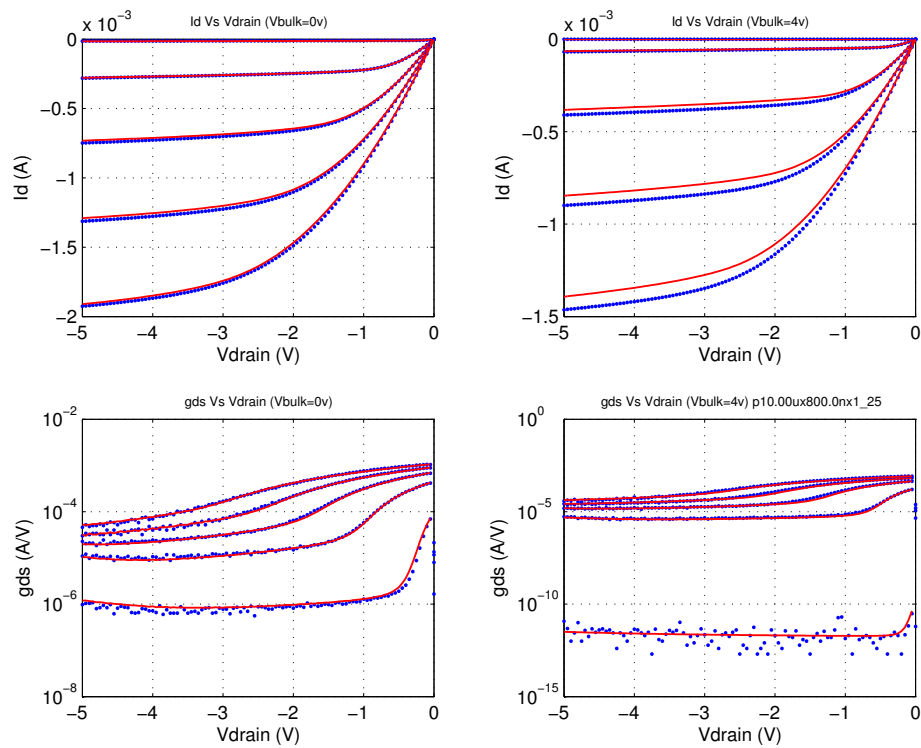


FIGURE 2.112 5p0_PFET_10x0p8_idvg_25C

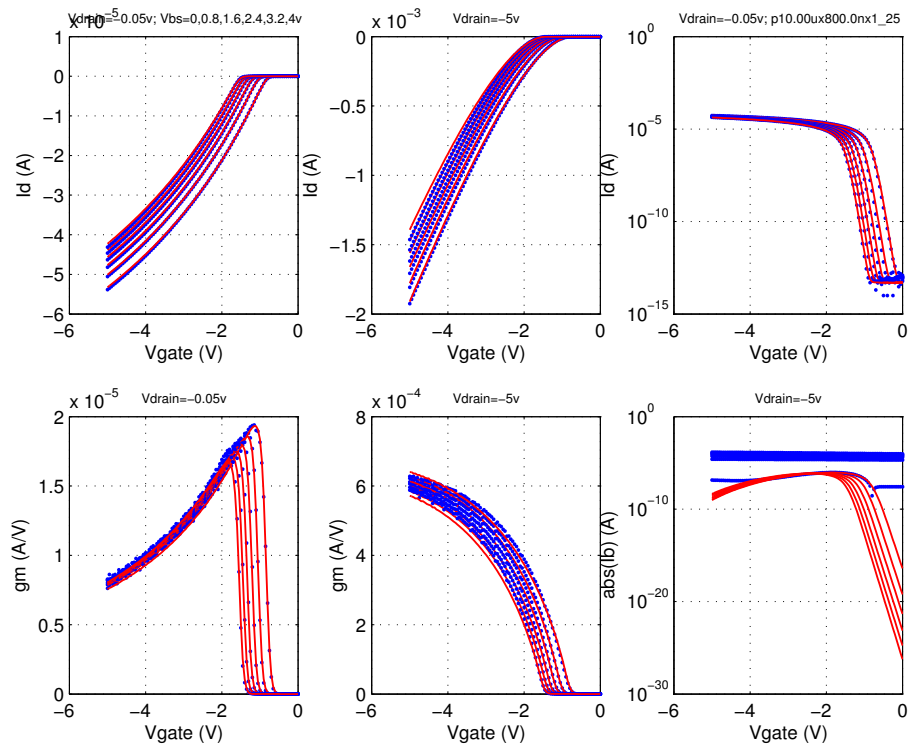


FIGURE 2.113 5p0_PFET_10x0p6_idvd_-40C

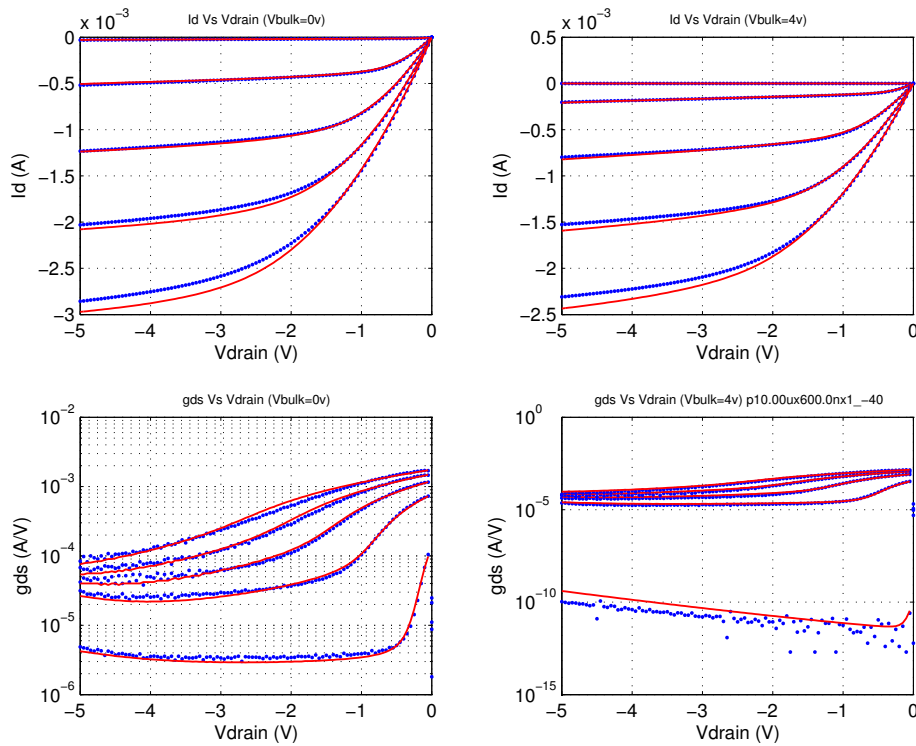


FIGURE 2.114 5p0_PFET_10x0p6_idvg_-40C

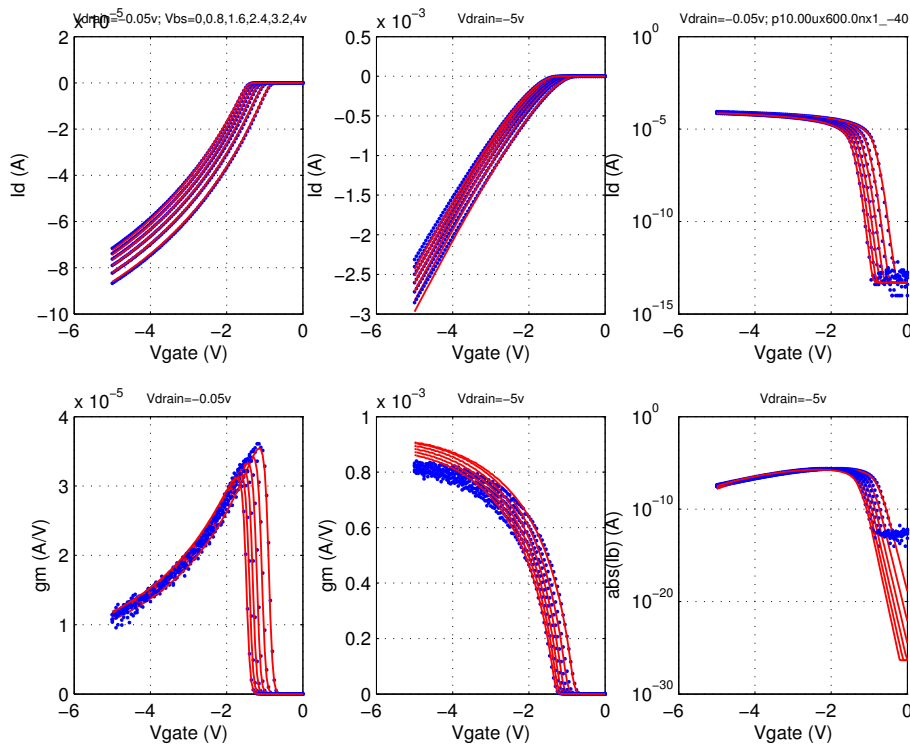


FIGURE 2.115 5p0_PFET_10x0p6_idvd_125C

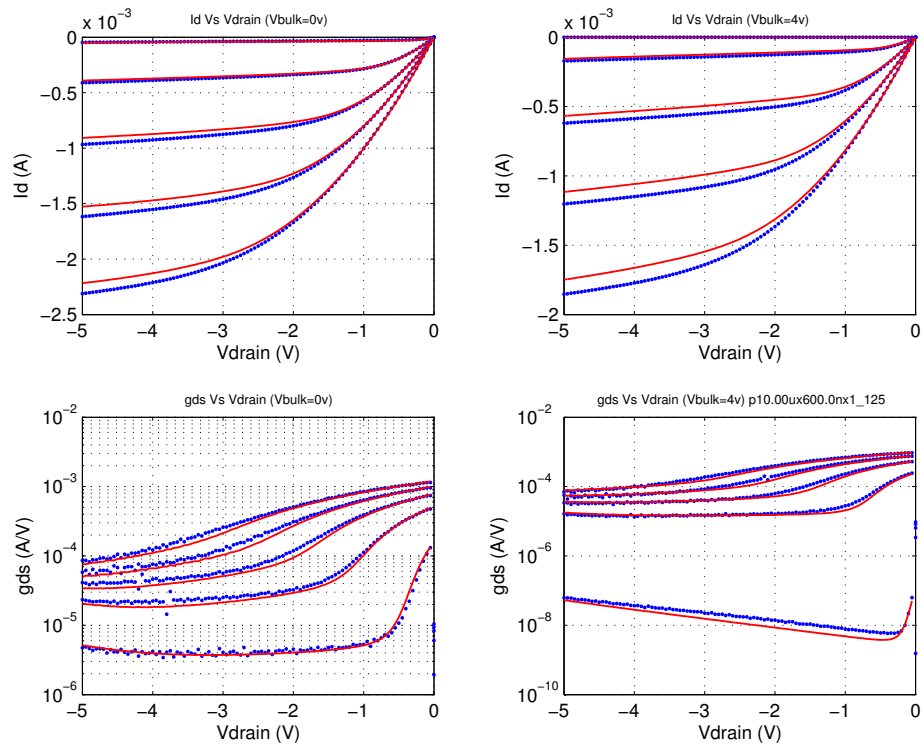
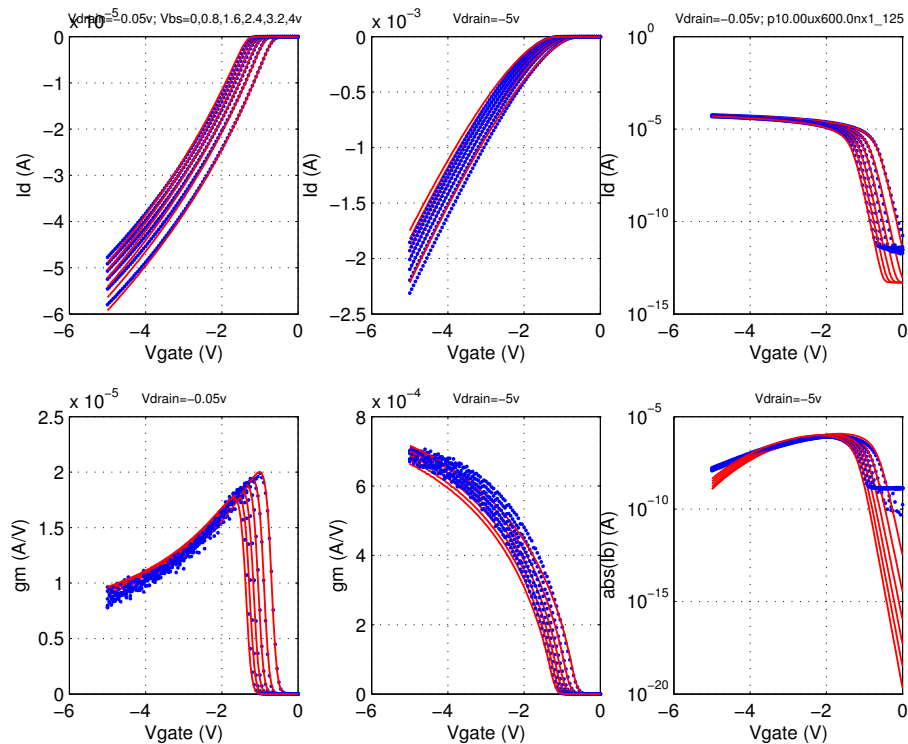


FIGURE 2.116 5p0_PFET_10x0p6_idvg_125C



2.6 Statistical and corner models

Statistical models are generated by specifying 1- σ variations of appropriate model parameters. These variances are generated via a physically based and robust mathematical approach called the “Backward Propagation of Variance (BPV). [3]” The BPV approach is defined by Eq. 3:

$$\sigma_{e_i}^2 = \sum_k \left(\frac{\partial e_i}{\partial p_k} \right)^2 \cdot \sigma_{p_k}^2 \quad (\text{EQ 3})$$

where σ_{e_i} is the standard deviation of the i^{th} Electrical Specification (E-spec), $\frac{\partial e_i}{\partial p_k}$ is the partial derivative of the E-spec w.r.t. to the k^{th} model parameter, and σ_{p_k} is the standard deviation of the model parameter that being solved for. The E-specs for this technology are extracted from Process Control Monitoring (PCM) data and are defined in Jazz document NPB-PS-0267 titled “Electrical Parameters of the SBC18 Processes.” This process is termed as the backward propagation of variance, as it takes measurements in variances (E-specs) of important electrical quantities and then calculates the variances in the model process parameters that are necessary to fit the spread in the measured data, rather than taking the measured variations in the model process parameters and forward propagating them to predict the variations in σ_e . Conventional statistical modeling approaches are typically forward propagated, and do not guarantee consistency between model and E-spec corners and miss the real goal of statistical modeling.

The set of partial derivatives on the RHS of Eq. 3 represent the sensitivity matrix of the extracted model, and are directly evaluated using a circuit simulator such as Spectre. These derivatives can depend on the Δp_k values chosen to approximate δp_k . A global optimizer is used to minimize any error associated with the sensitivity matrix evaluation. The maximum deviation between the E-spec. and simulator prediction for the SLOW, NOM, and FAST corners is 1/2- σ , where 6- σ is the total range from the minimum to the maximum value of the E-spec. Typically, this corresponds to < 2% deviation of the model prediction w.r.t the E-spec. Statistical model predictions for the various flavors of FETs in this technology are shown in Tables 2.13 through 2.16.

The statistical model allows un-correlated variations in oxide thickness, flat-band voltage (from oxide-charge and gate work-function), and channel doping as per Eq. 4 and Eq. 5 to impact threshold voltage (BSIM3v3 parameter VTH0). Additionally, the channel doping and oxide thickness are used for the body effect (BSIM3v3 parameter K1) evaluation as per Eq. 6 and Eq. 7.

$$VTH0 = VFB + 2 \frac{kT}{q} \ln \frac{N_{ch}}{n_i} + \frac{T_{ox}}{E_{ox}} \sqrt{2q \cdot E_{si} \cdot N_{ch} \cdot 2 \frac{kT}{q} \ln \frac{N_{ch}}{n_i}} \quad (\text{EQ 4})$$

$$\Delta VTH0 = \Delta VFB + \frac{\partial}{\partial N_{ch}} VTH0 \cdot \Delta N_{ch} + \frac{\partial}{\partial T_{ox}} VTH0 \cdot \Delta T_{ox} \quad (\text{EQ 5})$$

$$K1 = \frac{T_{ox}}{E_{ox}} \cdot \sqrt{2q \cdot E_{si} \cdot N_{ch}} \quad (\text{EQ 6})$$

$$\Delta K1 = \frac{\partial}{\partial N_{ch}} K1 \cdot \Delta N_{ch} + \frac{\partial}{\partial T_{ox}} K1 \cdot \Delta T_{ox} \quad (\text{EQ 7})$$

The geometry dependence of the threshold voltage and body constant is captured by specifying un-correlated variations in the relevant BSIM3v3 parameters such as K3 (narrow width Vth), K3B (body effect in narrow device), DVT0 (short channel Vth), and DVT2 (body effect of short channel device).

The global variation in active dimensions (active_cd) is propagated into the W_{eff} calculation of FETs to be consistent with other active or passive devices in the circuit. Similarly, global process variations in the gate poly length (poly_cd) are propagated into L_{eff} calculations. Additionally, the L_{eff} depends on the variation in the lateral spread of the LDD (Lightly Doped Drain) under the gate. Oxide thickness and L_{eff} variations are physically propagated into overlap capacitance variation.

The extraction of statistical variations of model parameters is preceded by “Centering” process of the “measured” case. This is described in Section 2.6.1.

2.6.1 Centering within the BPV Framework

The measured case was “centered” to the E-specs of threshold voltage, body constant, and saturation currents for the devices listed in the E-specs. This is an important part of the model release methodology and generates a nominal model that is aligned to the nominal E-specs of the technology.

The centering is performed using the statistical modeling approach defined in the beginning of Section 2.6 by modifying Eq. 3 as:

$$\Delta e_i = \sum_k \frac{\partial e_i}{\partial p_k} \cdot \Delta p_k \quad (\text{EQ 8})$$

where Δe_i is the difference between the measured case prediction of the E-spec and nominal E-spec, $\frac{\partial e_i}{\partial p_k}$ is the partial derivative of the e-spec w.r.t the relevant model parameter, and Δp_k is the shift in the model parameter needed to center the measured case to the E-spec. Typical shift in model parameters required to center the measured case are less than 1%, and represent a statistically valid and unique set of shifts in model parameters that are perfectly aligned with the “nominal” process targets of the Fab. It should be noted that these E-specs are targets that the fab continually tries to match, with the results being regularly reported in the form of CPK charts.

2.6.2 Corner model generation

Corner models are generated via an approach identical to the centering model methodology described in Section 2.6.1 on page 84. The E-spec corners are used to calculate the E-spec delta on the LHS of Eq. 8, which is then solved for the required model parameter shift on the RHS. The maximum allowable deviation between the E-spec. and the model prediction is $1/2\text{-}\sigma$, where $6\text{-}\sigma$ is the total range from the minimum to the

maximum value of the E-spec. Typically, this corresponds to < 2% deviation of the model prediction w.r.t the E-spec.

The variation in junction area capacitance C_J is +/-5% in corner cases. The junction sidewall capacitance C_{JSW} and gate edge sidewall capacitance C_{JSWG} are skewed for the corner cases by +/- 10% for both FET and diode models.

Conventional corner modeling approaches are typically forward propagated, where measured model parameter deltas (Δp_k in Eq. 8) are used to predict spreads in key electrical properties of the FETs and do not guarantee consistency between corner models and E-spec corners. The extracted corner model parameters for thin and thick oxide FETs are shown in Tables 2.10 and 2.11, respectively.

See Section 15.0 for further explanation of the device interdependencies in the corner models and use of the X-Sigma corner models.

TABLE 2.10 Corner model parameters for thin-oxide FETs

BSIM3v3 Parameter	Description	NFET			PFET		
		SLOW	NOM	FAST	SLOW	NOM	FAST
cgdl (F/m)	High Vgs D-S ovlp.	2.88E-10	2.99E-10	3.23E-10	1.46E-10	1.50E-10	1.56E-10
cgdo (F/m)	G-D ovlp. cap.	1.18E-10	1.22E-10	1.31E-10	2.13E-10	2.20E-10	2.28E-10
cgsi (F/m)	High Vgs G-S ovlp.	2.88E-10	2.99E-10	3.23E-10	1.46E-10	1.50E-10	1.56E-10
cgso (F/m)	G-S ovlp. cap.	1.18E-10	1.22E-10	1.31E-10	2.13E-10	2.20E-10	2.28E-10
cj (F/m ²)	Bottom junc. cap	1.10E-03	1.06E-03	1.02E-03	8.95E-04	8.57E-04	8.18E-04
cjsw (F/m)	Sidewall junc. cap.	2.07E-10	2.01E-10	1.94E-10	6.27E-11	6.00E-11	5.73E-11
cjswg (F/m)	Sidewall under gate junc. cap.	5.80E-10	5.61E-10	5.41E-10	5.01E-10	4.80E-10	4.58E-10
dlc (m)	ΔL for cap. model	3.43E-08	3.74E-08	4.09E-08	3.57E-08	3.99E-08	4.42E-08
dlcig (m)	S-D overlap L for lgs and lgd	7.95E-09	1.11E-08	1.46E-08	3.57E-08	3.99E-08	4.42E-08
dvt0	First Narrow W co-efficient	-1.31E+00	1.53E+00	4.02E+00	3.91E-01	1.10E+00	1.44E+00
dvt2 (1/V)	Body effect in short channel	NA	NA	NA	-3.25E-02	-7.08E-02	-2.68E-01
dwc (m)	ΔW for cap. model	6.14E-08	3.85E-08	1.61E-08	2.32E-08	9.74E-09	-2.91E-09
k1 (V ^{1/2})	Body constant	3.83E-01	3.61E-01	3.40E-01	6.83E-01	6.37E-01	5.92E-01
k3	Narrow W co-efficient	-7.94E+00	-1.39E+01	-1.98E+01	-8.41E-01	-2.03E+00	-3.90E+00
k3b (1/V)	Body effect of K3	3.80E-02	3.16E+00	6.18E+00	1.10E+00	3.44E+00	4.26E+00
lint (m)	ΔL	7.95E-09	1.11E-08	1.46E-08	3.57E-08	3.99E-08	4.42E-08
rdsw (Ω -mm)	D-S series resistance	3.85E+01	3.80E+01	3.62E+01	1.09E+03	1.09E+03	1.08E+03
tox (m)	Oxide thickness	3.95E-09	3.85E-09	3.75E-09	3.86E-09	3.76E-09	3.66E-09
toxm (m)	Tox value at param. extraction	3.95E-09	3.85E-09	3.75E-09	3.86E-09	3.76E-09	3.66E-09
u0 (cm ² /Vs)	Low field mobility	2.73E+02	2.89E+02	3.05E+02	9.00E+01	9.13E+01	9.26E+01
vbox (V)	Oxide breakdown threshold	1.18E+01	1.16E+01	1.12E+01	1.16E+01	1.13E+01	1.10E+01
vth0 (V)	Long channel threshold	3.91E-01	3.53E-01	3.14E-01	-4.64E-01	-4.05E-01	-3.47E-01
wint (m)	ΔW	6.14E-08	3.85E-08	1.61E-08	2.32E-08	9.74E-09	-2.91E-09

TABLE 2.11 Corner model parameters for thick-oxide (3.3V) FETs

BSIM3v3 Parameter	Description	N3P3FET			P3P3FET		
		SLOW	NOM	FAST	SLOW	NOM	FAST
cgdl (F/m)	High Vgs D-S ovlp.	1.65E-10	2.10E-10	2.57E-10	1.07E-10	1.12E-10	1.18E-10
cgdo (F/m)	G-D ovlp. cap.	8.26E-11	1.05E-10	1.29E-10	2.43E-10	2.55E-10	2.68E-10
cgsi (F/m)	High Vgs G-S ovlp.	1.65E-10	2.10E-10	2.57E-10	1.07E-10	1.12E-10	1.18E-10
cgso (F/m)	G-S ovlp. cap.	8.26E-11	1.05E-10	1.29E-10	2.43E-10	2.55E-10	2.68E-10
cj (F/m ²)	Bottom junc. cap.	9.58E-04	8.59E-04	7.61E-04	7.48E-04	7.24E-04	7.01E-04
cjsw (F/m)	Sidewall junc. cap.	1.92E-10	1.72E-10	1.52E-10	1.07E-10	1.03E-10	1.00E-10
cjswg (F/m)	Sidewall under gate junc. cap.	3.87E-10	3.47E-10	3.07E-10	3.30E-10	3.19E-10	3.09E-10
dlc (m)	ΔL for cap. model	3.16E-08	4.41E-08	5.65E-08	6.93E-08	7.47E-08	8.02E-08
dlcig (m)	S-D overlap L for lgs and lgd	3.16E-08	4.41E-08	5.65E-08	5.83E-08	6.37E-08	6.92E-08
dvt0	First Narrow W co-efficient	7.60E+00	8.10E+00	9.07E+00	5.76E-01	2.17E+00	3.78E+00
dvt2 (1/V)	Body effect in short channel	1.11E-01	9.19E-02	6.84E-02	-1.20E-01	-8.41E-02	-6.60E-02
dwc (m)	ΔW for Cap. model	1.85E-08	1.10E-08	4.56E-09	-2.47E-09	-1.42E-08	-2.57E-08
k1 (V ^{1/2})	Body constant	5.53E-01	4.82E-01	4.16E-01	9.81E-01	9.24E-01	8.71E-01
k3	Narrow W co-efficient	NA	NA	NA	-3.18E+00	-3.22E+00	-3.63E+00
k3b (1/V)	Body effect of K3	NA	NA	NA	8.71E-01	1.18E+00	2.39E+00
lint (m)	ΔL	3.16E-08	4.41E-08	5.65E-08	5.83E-08	6.37E-08	6.92E-08
rdsw (Ω -mm)	D-S series resistance	7.41E+02	6.22E+02	5.03E+02	2.13E+03	2.08E+03	2.03E+03
tox (m)	Oxide thickness	6.89E-09	6.71E-09	6.53E-09	6.89E-09	6.71E-09	6.53E-09
toxm (m)	Tox value at param. extraction	6.89E-09	6.71E-09	6.53E-09	6.89E-09	6.71E-09	6.53E-09
u0 (cm ² /Vs)	Low field mobility	3.74E+02	3.84E+02	3.93E+02	9.23E+01	9.83E+01	1.04E+02
vth0 (V)	Long channel threshold	6.58E-01	6.10E-01	5.62E-01	-8.58E-01	-7.89E-01	-7.21E-01
wint (m)	ΔW	1.85E-08	1.10E-08	4.56E-09	-2.47E-09	-1.42E-08	-2.57E-08

TABLE 2.12 Corner model parameters for thick-oxide (5.0V) FETs

BSIM3v3 Parameter	Description	NFET			PFET		
		SLOW	NOM	FAST	SLOW	NOM	FAST
tox (m)	Oxide thickness	1.42E-08	1.34E-08	1.26E-08	1.45E-08	1.37E-08	1.29E-08
vth0 (V)	Long channel threshold	7.28E-01	6.31E-01	5.33E-01	-9.09E-01	-8.12E-01	-7.15E-01
cgsi (F/m)	High Vgs G-S ovlp.	4.00E-10	4.00E-10	4.00E-10	1.52E-10	1.52E-10	1.52E-10
cgdl (F/m)	High Vgs D-S ovlp.	4.00E-10	4.00E-10	4.00E-10	1.52E-10	1.52E-10	1.52E-10
cgso (F/m)	G-S ovlp. cap.	4.93E-11	4.93E-11	4.93E-11	4.50E-11	4.50E-11	4.50E-11
cgdo (F/m)	G-D ovlp. cap.	4.93E-11	4.93E-11	4.93E-11	4.50E-11	4.50E-11	4.50E-11
nlx (m)	Short channel Vt	8.87E-08	8.87E-08	8.87E-08	2.32E-10	2.32E-10	2.32E-10
lint (m)	ΔL	3.27E-08	7.13E-08	1.04E-07	7.37E-08	8.75E-08	9.98E-08
k1 (V ^{1/2})	Body constant	8.61E-01	7.52E-01	6.44E-01	7.50E-01	6.40E-01	5.30E-01
k3	Narrow width co-efficient	-2.35	-2.73	-2.96	-1.14	-1.23	-1.34
k3b (1/V)	Body effect of K3	5.37E-01	5.74E-01	6.66	1.55	1.72	1.94
cjsw (F/m)	Sidewall junc. cap.	1.29E-10	1.18E-10	1.06E-10	1.21E-10	1.10E-10	9.86E-11
cjswg (F/m)	Sidewall under gate junc. cap.	3.03E-10	2.75E-10	2.48E-10	1.53E-10	1.39E-10	1.25E-10
cj (F/m ²)	Bottom junc. cap	8.62E-04	7.83E-04	7.05E-04	7.75E-04	7.05E-04	6.34E-04

TABLE 2.12 Corner model parameters for thick-oxide (5.0V) FETs

BSIM3v3 Parameter	Description	NFET			PFET		
		SLOW	NOM	FAST	SLOW	NOM	FAST
u0 (cm ² /Vs)	Low field mobility	3.79E+02	3.98E+02	4.12E+02	1.20E+02	1.31E+02	1.41E+02
rdsw (Ω-μm)	Drain/source series resistance	4.42E+02	4.42E+02	4.42E+02	1.89E+03	1.89E+03	1.89E+03
wint (m)	ΔW	6.46E-08	3.81E-08	2.54E-08	2.12E-08	1.48E-09	-2.11E-08
dvt2 (1/V)	Body effect in short channel	-1.27E-02	-4.42E-02	-1.04E-01	4.32E-02	-2.46E-02	-9.27E-02

2.6.3 Statistical model usage guidelines

In contrast to the corner models, the statistical models allow “multi-directional” variability in model parameters. For a sufficient number of monte-carlo runs these simulation results converge to the measured (E-spec.) 3-σ variation in key MOSFET device properties (such as I_{dsat} , V_{th}) and in most cases represent a more accurate prediction (over corner models) of expected impact of process variations on circuit-level figures of merit. The statistical model is currently supported only in Spectre, which provides the needed framework for statistical modeling. The “process-only” variation option should be selected when setting up statistical model run. This represents the expected functional yield (non-defect related) that can be expected for the particular design split. The “numruns” (number of runs) in monte-carlo analysis is an important parameter that controls the accuracy of the statistical model prediction. For single transistor level simulations of V_{th} , I_{dsat} , and body constant a value of a 100 runs gives reasonably stable results. The user should check the mean value of the circuit-level figure of merit that is being simulated and compare it to nominal simulation and decide whether to increase or decrease this value.

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2.6.4 Statistical and corner model tables

TABLE 2.13 1.8v NFET corner and statistical model predictions

Device	WxL(μm)	Espec Name (unit)	Slow			Nom			Fast		
			Espec	Corner	Stat	Espec	Corner	Stat	Espec	Corner	Stat
small	0.22x0.18	vt (V)	0.510	0.512	0.483	0.390	0.388	0.390	0.270	0.282	0.297
small	0.22x0.18	idsat (mA)	0.080	0.087	0.082	0.140	0.141	0.141	0.200	0.207	0.200
small	0.22x0.18	kb ($\text{V}^{0.5}$)	0.370	0.455	0.419	0.270	0.306	0.310	0.170	0.191	0.201
short	10x0.18	vt (V)	0.570	0.568	0.570	0.490	0.490	0.491	0.410	0.412	0.412
short	10x0.18	idsat (mA)	5.100	5.099	4.960	6.000	5.999	5.960	6.900	7.020	6.960
short	10x0.18	kb ($\text{V}^{0.5}$)	0.390	0.392	0.418	0.320	0.323	0.326	0.250	0.256	0.234
large	10x10	vt (V)	0.390	0.390	0.392	0.350	0.350	0.351	0.310	0.310	0.310
large	10x10	beta ($\mu\text{A}/\text{V}^2$)	130.00	129.90	131.0	143.00	142.90	144.0	156.00	156.90	157.0
large	10x10	kb ($\text{V}^{0.5}$)	0.360	0.362	0.357	0.340	0.340	0.340	0.320	0.319	0.323
narrow	0.22x10	vt (V)	0.290	0.297	0.299	0.220	0.220	0.220	0.150	0.156	0.141
narrow	0.22x10	kb ($\text{V}^{0.5}$)	0.350	0.360	0.343	0.280	0.279	0.278	0.210	0.217	0.213

TABLE 2.14 1.8v PFET corner and statistical model predictions

Device	WxL(μm)	Espec Name (unit)	Slow			Nom			Fast		
			Espec	Corner	Stat	Espec	Corner	Stat	Espec	Corner	Stat
small	0.22x0.18	vt (V)	-0.510	-0.510	-0.510	-0.390	-0.411	-0.409	-0.270	-0.311	-0.308
small	0.22x0.18	idsat (mA)	-0.040	-0.042	-0.037	-0.060	-0.060	-0.060	-0.080	-0.082	-0.084
small	0.22x0.18	kb ($\text{V}^{0.5}$)	0.550	0.552	0.532	0.430	0.412	0.407	0.310	0.300	0.282
short	10x0.18	vt (V)	-0.520	-0.517	-0.510	-0.440	-0.435	-0.434	-0.360	-0.358	-0.357
short	10x0.18	idsat (mA)	-2.100	-2.110	-2.040	-2.550	-2.549	-2.540	-3.000	-3.048	-3.040
short	10x0.18	kb ($\text{V}^{0.5}$)	0.590	0.594	0.611	0.510	0.524	0.526	0.430	0.421	0.441
large	10x10	vt (V)	-0.460	-0.460	-0.461	-0.400	-0.400	-0.399	-0.340	-0.340	-0.337
large	10x10	beta ($\mu\text{A}/\text{V}^2$)	30.000	30.080	30.30	32.00	32.000	32.20	34.00	34.080	34.10
large	10x10	kb ($\text{V}^{0.5}$)	0.570	0.571	0.571	0.530	0.530	0.529	0.490	0.491	0.487
narrow	0.22x10	vt (V)	-0.460	-0.458	-0.460	-0.390	-0.380	-0.378	-0.320	-0.298	-0.296
narrow	0.22x10	kb ($\text{V}^{0.5}$)	0.540	0.555	0.534	0.440	0.450	0.443	0.340	0.402	0.352

TABLE 2.15 3.3v NFET corner and statistical model predictions

Device	WxL(μm)	Espec Name (unit)	Slow			Nom			Fast		
			Espec	Corner	Stat	Espec	Corner	Stat	Espec	Corner	Stat
small	0.6x0.36	idsat (mA)	0.285	0.311	0.309	0.360	0.373	0.374	0.435	0.454	0.439
short	10x0.36	vt (V)	0.700	0.695	0.702	0.600	0.604	0.605	0.500	0.492	0.508
short	10x0.36	idsat (mA)	5.000	4.705	4.620	6.000	5.589	5.600	7.000	6.742	6.580
short	10x0.36	kb ($\text{V}^{0.5}$)	0.620	0.616	0.614	0.520	0.524	0.517	0.420	0.411	0.420
large	10x10	vt (V)	0.660	0.660	0.671	0.610	0.610	0.609	0.560	0.560	0.547
large	10x10	beta ($\mu\text{A}/\text{V}^2$)	85.000	89.220	89.900	90.000	95.050	95.70	95.000	101.20	102.0
large	10x10	kb ($\text{V}^{0.5}$)	0.700	0.641	0.631	0.640	0.580	0.579	0.580	0.521	0.527

TABLE 2.16 3.3v PFET corner and statistical model predictions

Device	WxL(μm)	Espec Name (unit)	Slow			Nom			Fast		
			Espec	Corner	Stat	Espec	Corner	Stat	Espec	Corner	Stat
small	0.6x0.3	idsat (mA)	-0.130	-0.135	-0.136	-0.180	-0.165	-0.165	-0.230	-0.200	-0.194
short	10x0.3	vt (V)	-0.840	-0.836	-0.823	-0.740	-0.740	-0.740	-0.640	-0.636	-0.657
short	10x0.3	idsat (mA)	-2.400	-2.434	-2.440	-2.900	-2.900	-2.900	-3.400	-3.438	-3.360
short	10x0.3	kb ($V^{0.5}$)	0.940	0.946	0.970	0.840	0.844	0.844	0.740	0.741	0.718
large	10x10	vt (V)	-0.860	-0.860	-0.860	-0.790	-0.790	-0.788	-0.720	-0.720	-0.716
large	10x10	beta ($\mu\text{A}/V^2$)	17.500	17.580	17.80	19.50	19.510	19.80	21.50	21.580	21.800
large	10x10	kb ($V^{0.5}$)	0.960	0.961	0.958	0.910	0.910	0.906	0.860	0.861	0.854

TABLE 2.17 5.0v Thick-oxide NFET corner and statistical model predictions

Device	WxL(μm)	Espec Name (unit)	Slow			Nom			Fast		
			Espec	Corner	Stat	Espec	Corner	Stat	Espec	Corner	Stat
large	10x10 ¹	beta ² ($\mu\text{A}/V^2$)	47	47.02	47.1	53	53.08	53.2	59	59	59.4
large	10x10 ¹	kb ² ($V^{0.5}$)	0.77	0.77	0.766	0.67	0.669	0.668	0.57	0.57	0.57
large	10x10 ¹	vt ² (V)	0.74	0.74	0.735	0.64	0.64	0.64	0.54	0.54	0.545
small	0.6x0.7	idsat ² (mA)	0.25	0.251	0.248	0.33	0.333	0.334	0.41	0.413	0.42
short	10x0.6	idsat ¹ (mA)	4.4	4.417	4.47	5.2	5.199	5.21	6	6.014	5.95
short	10x0.6	kb ² ($V^{0.5}$)	0.64	0.641	0.65	0.52	0.519	0.515	0.4	0.402	0.38
short	10x0.6	vt ¹ (V)	0.75	0.755	0.756	0.65	0.652	0.649	0.55	0.555	0.542

TABLE 2.18 5.0v Thick-oxide PFET corner and statistical model predictions

Device	WxL(μm)	Espec Name (unit)	Slow			Nom			Fast		
			Espec	Corner	Stat	Espec	Corner	Stat	Espec	Corner	Stat
large	10x10	beta ² ($\mu\text{A}/V^2$)	11	11.05	11	13	13	13	15	15.06	15
large	10x10	kb ² ($V^{0.5}$)	0.64	0.64	0.641	0.54	0.54	0.54	0.44	0.44	0.439
large	10x10	vt ² (V)	-0.91	-0.91	-0.912	-0.81	-0.81	-0.811	-0.71	-0.71	-0.711
small	0.6x0.6	idsat ² (mA)	-0.125	-0.127	-0.122	-0.17	-0.168	-0.168	-0.215	-0.218	-0.215
short	10x0.6	idsat ¹ (mA)	-2.1	-2.118	-2.08	-2.6	-2.601	-2.6	-3.1	-3.117	-3.12
short	10x0.6	kb ² ($V^{0.5}$)	0.59	0.591	0.585	0.44	0.44	0.437	0.29	0.29	0.289
short	10x0.6	vt ¹ (V)	-0.87	-0.869	-0.874	-0.77	-0.77	-0.77	-0.67	-0.67	-0.666

2.7 Mismatch models

2.7.1 Measurements

The measurement setup is composed of a HP4156 Semiconductor Parameter Analyzer, Keithley 707 switch matrix with 7172 low current matrix cards, and Signatone S485 semi-automatic prober with hot chuck. The test is a two step process. In the first step, the average thresholds of the two transistors in the FET pair are measured via the maximum transconductance method. In the second step, the gate is biased at $V_{gs} = V_{gst} =$

$V_t + 0.1, 0.3, 0.5$ and the currents in each transistor measured for multiple drain biases ($V_{ds} = 0.2, 0.6, 1.4$). The mismatch current is then evaluated via Eq. 9:

$$\Delta I_d = 100 \times \frac{I_{d2} - I_{d1}}{I_{d1}} \quad (\text{EQ 9})$$

The mismatch current represents the error between the currents in a simple current mirror. The transistors in the mismatch test-structures are typically $\sim 10\mu\text{m}$ apart, representing a worst-case mismatch for most analog layouts, where the transistors in the matched pair can be laid-out in closer proximity to each other.

A detailed description of MOSFET mismatch characterization methodology and results are available in Jazz Semiconductor document NPB PS-0392 titled “Analog Characterization Report for SBC18.”

2.7.2 Mismatch modeling

The mismatch between neighboring FETs is a representation of the local variation of process parameters such as oxide thickness, channel doping, oxide charge, gate work-function, channel length and width. The basic equations used to model such variations are identical to what was described in the section “Statistical and corner models” on page 83. To match the measured data, these variations are made geometry dependent as per Eq. 10:

$$\sigma_{local}(X) = \frac{\sigma_X}{\sqrt{W_{eff} \cdot L_{eff}}} \quad (\text{EQ 10})$$

where X is the channel doping N_{ch} , low field mobility U_0 , flat-band voltage V_{FB} , or oxide thickness T_{ox} .

The impact of local lithographic variations is captured via Eq. 11 and Eq. 12:

$$\sigma_{local}(\Delta W) = \frac{\sigma(\Delta W)}{\sqrt{L_{eff}}} \quad (\text{EQ 11})$$

$$\sigma_{local}(\Delta L) = \frac{\sigma(\Delta L)}{\sqrt{W_{eff}}} \quad (\text{EQ 12})$$

whereby a narrower device can be expected to have larger channel length variations, and a shorter device can be expected to have larger channel width variations.

The local variation in these 6 parameters is extracted via a nonlinear least squares global optimization method to best fit the measured data.

2.7.3 Mismatch model usage guidelines

The mismatch model is available in Spectre, which provides the necessary framework to model the local mismatch between transistors. It is implemented inside the “sub-circuit” definition of the FETs allowing for “instance to instance” variations in the process parameters. The “variations” variable inside Spectre should be set equal to “mismatch.” Typically, ~ 100 monte-carlo runs are sufficient to accurately simulate the local-mis-

match between the FETs. The user should, however, increase the “numruns” variable inside Spectre until the improvement in the simulated results is small.

2.7.4 Mismatch model comparison with measurements

Figure 2.117 through Figure 2.120 compare the mismatch model prediction with the measured data for the 3- σ ΔI_d mismatch between a pair of neighboring transistors for low and high voltage N and PFETs. The discrete points are the measured data, while the solid lines represent simulated data.

FIGURE 2.117 1p8_nfet mismatch model vs. measurements

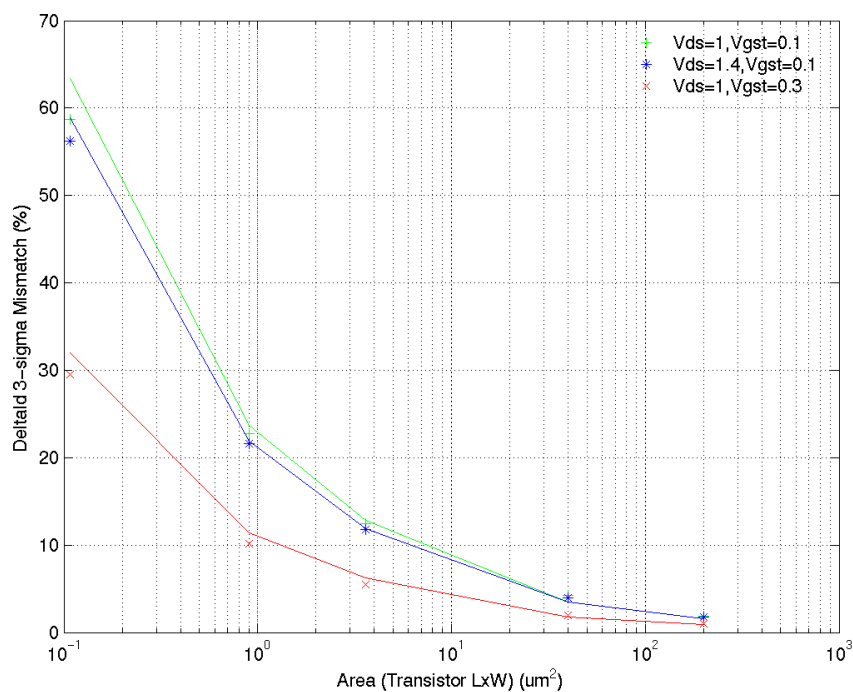


FIGURE 2.118 1p8_pfet mismatch model vs. measurements

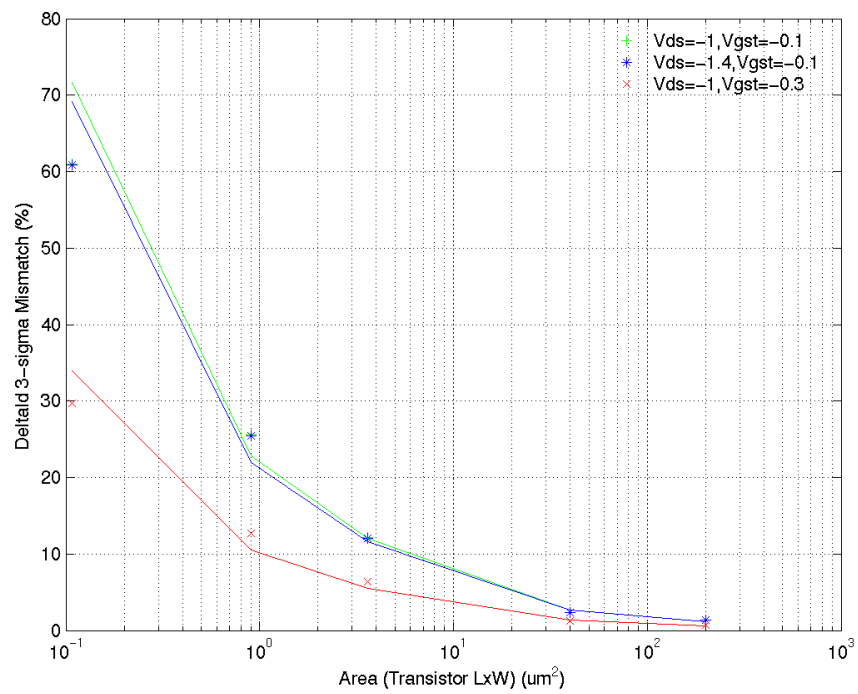


FIGURE 2.119 3p3_nfet mismatch model vs. measurements

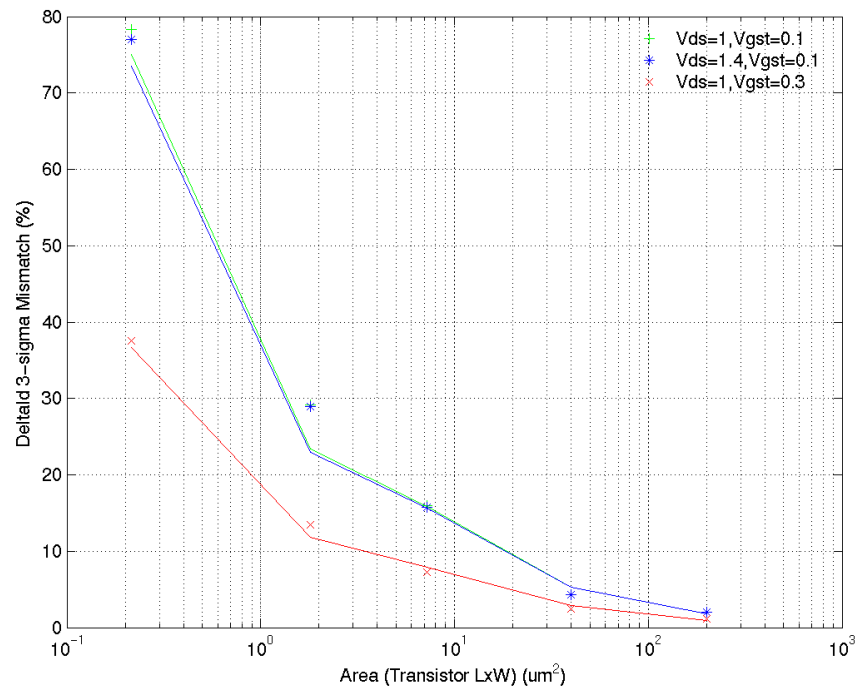


FIGURE 2.120 3p3_pfet mismatch model vs. measurements

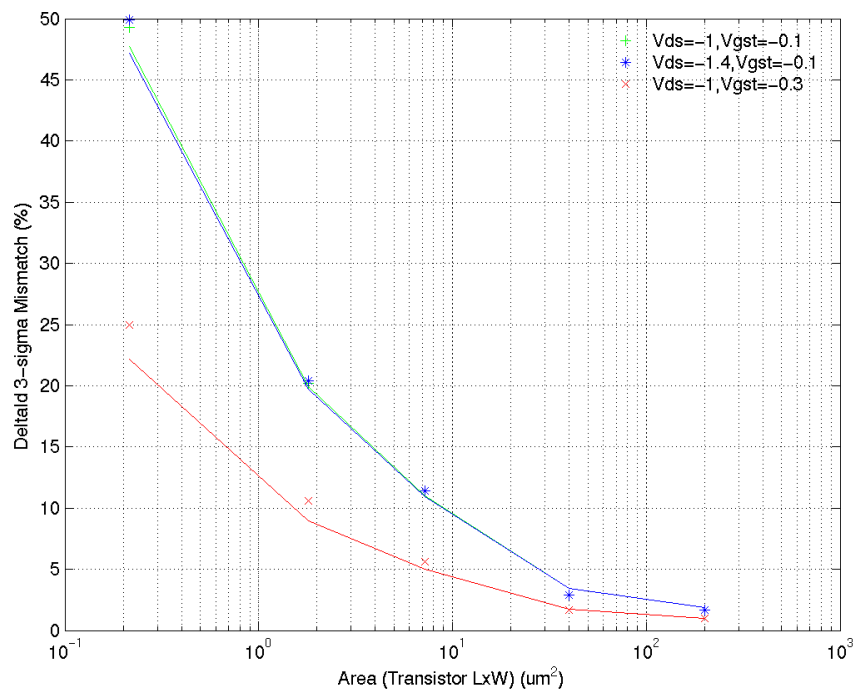


FIGURE 2.121 5V_NFET mismatch model vs. measurements

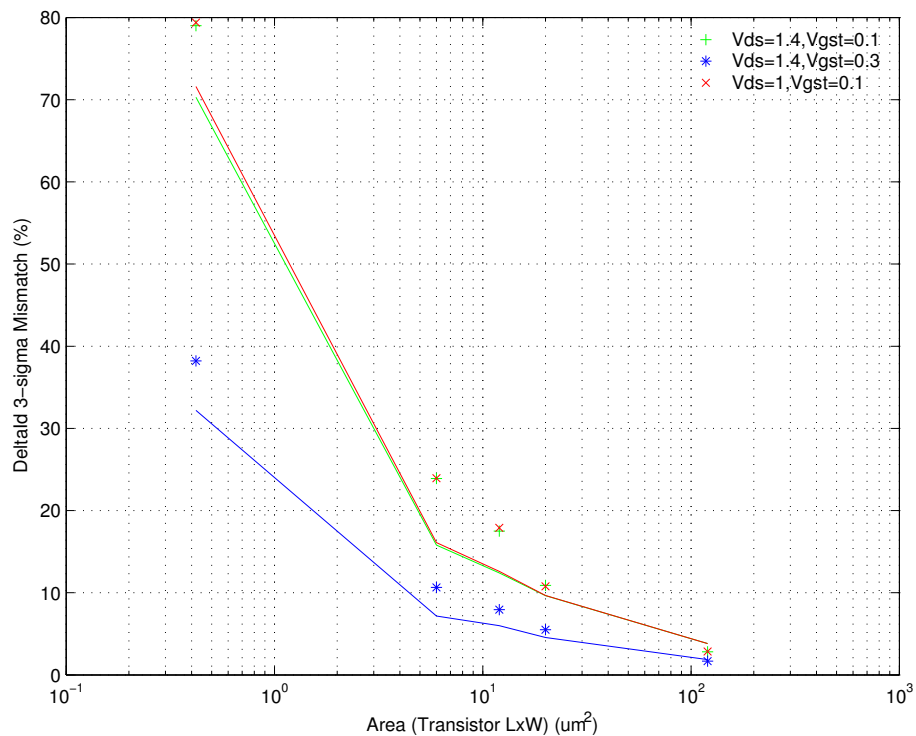
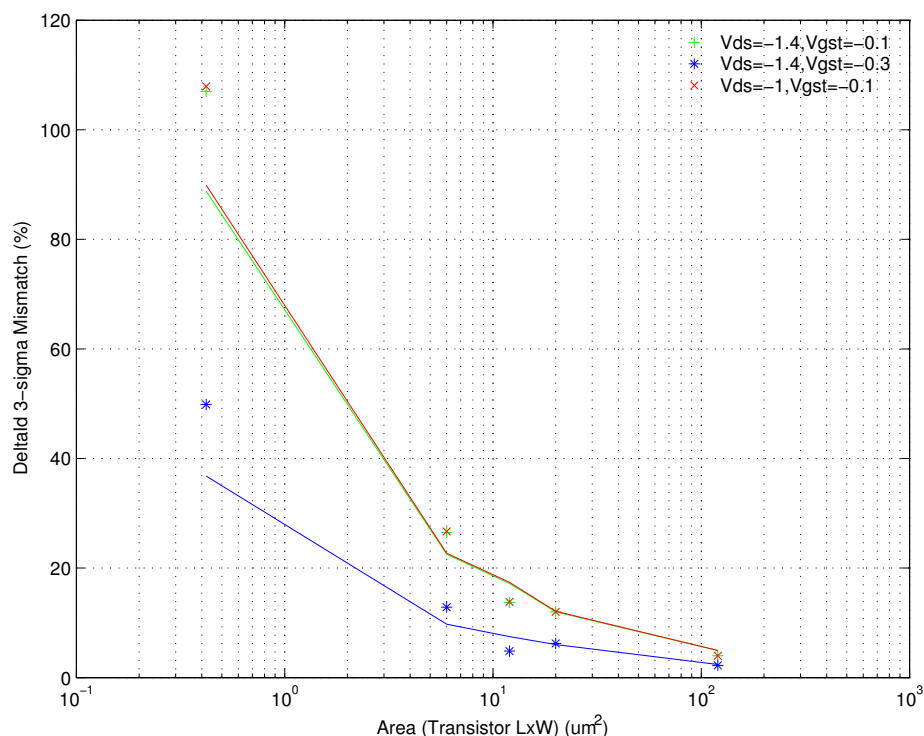


FIGURE 2.122 5V_PFET mismatch model vs. measurements



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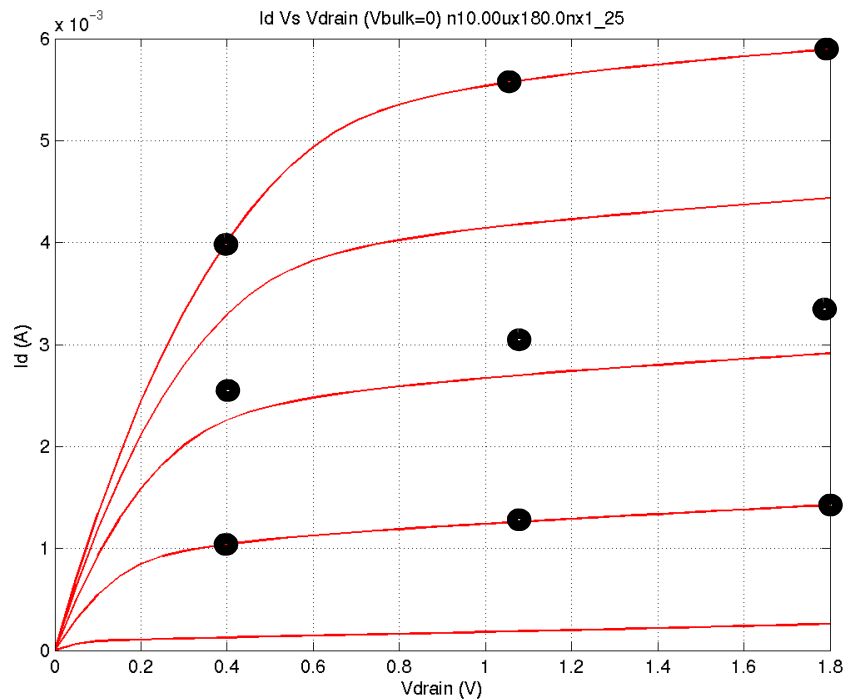
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2.8 Flicker Noise

2.8.1 Measurement

Flicker noise ($1/f$ noise) was measured using the BTA9812A noise analyzer system in conjunction with the HP35670A dynamic signal analyzer using an on-wafer probe-station. BTA's Noisepro software was used to automate the measurements. Precautions were taken to electrically isolate the DUT and the RF-transistor (Ground-Signal-Ground) layouts were used to minimize on-wafer ground loops that can corrupt the measurements. Multi-die measurements with the MOSFET biased in saturation were performed to select the worst-case noise site. Measurements were then performed at 9 different biases. The bias points, encompassing both the linear and saturation regions of the FET, are illustrated in Figure 2.123.

FIGURE 2.123 1.8V FET bias point example at which flicker noise measurements were performed



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2.8.2 Flicker noise modeling

Starting with model rev 6.0, the unified BSIM3v3 flicker noise model is supported. This model provides increased flexibility to match the bias dependence of the flicker noise. The BSIM3v3 flicker noise model parameters NOIA, NOIB, and NOIC are extracted. Flicker noise measurements are compared with the model predictions in Figures 2.124 through 2.135 for the 1.8v and 3.3v N and P-FET devices.

FIGURE 2.124 1.8v_n1x10x0p18_flicker model vs. measurements

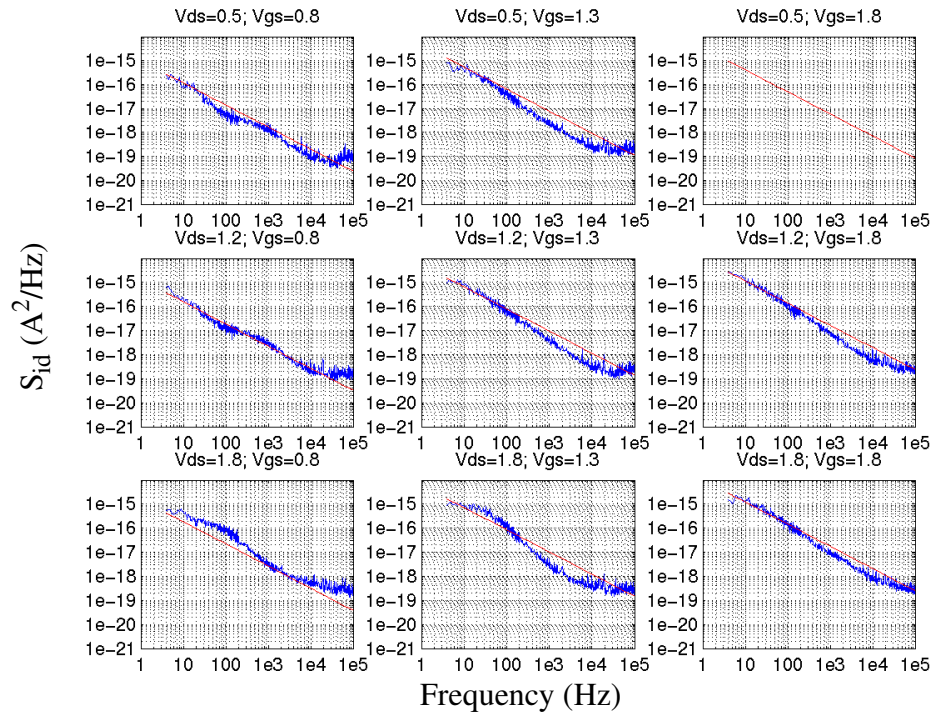


FIGURE 2.125 1.8v_n1x10x0p3_flicker model vs. measurements

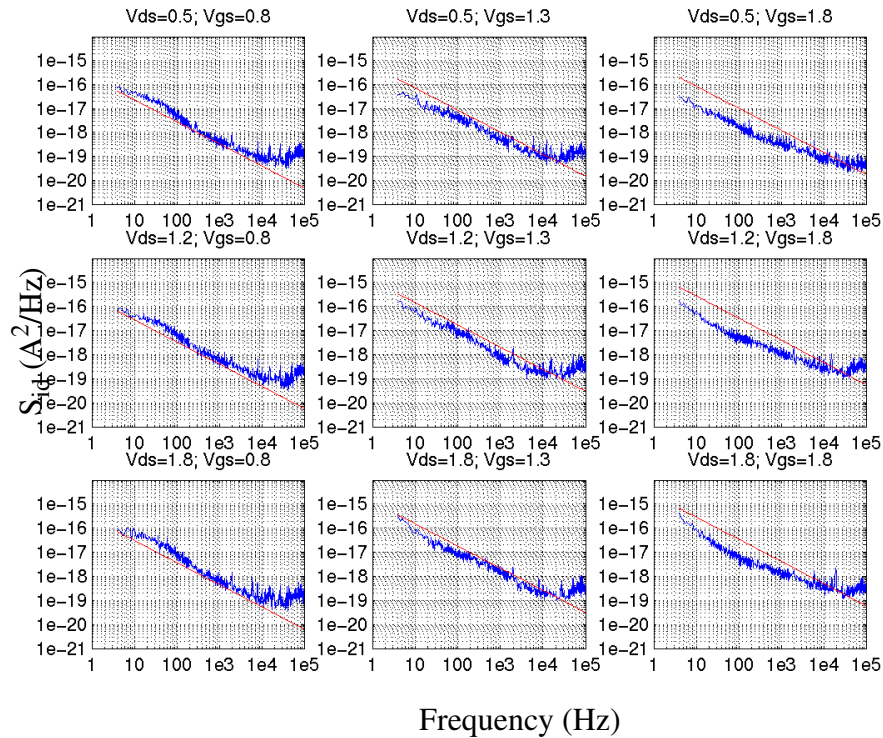


FIGURE 2.126 1.8v_n1x2x0p18_flicker model vs. measurements

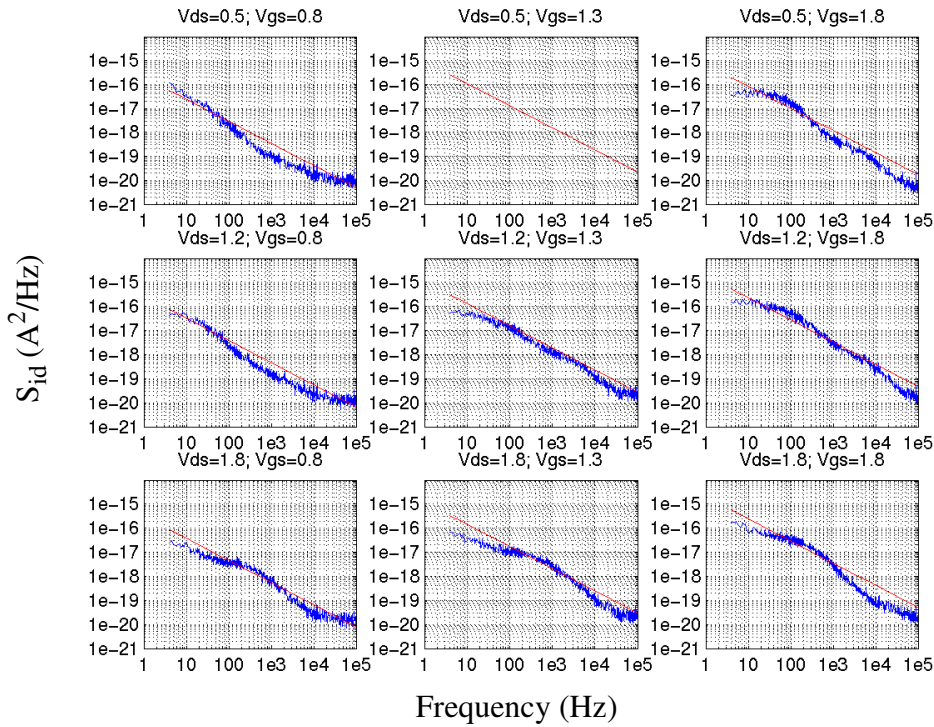


FIGURE 2.127 1.8v_p1x10x0p18_flicker model vs. measurements

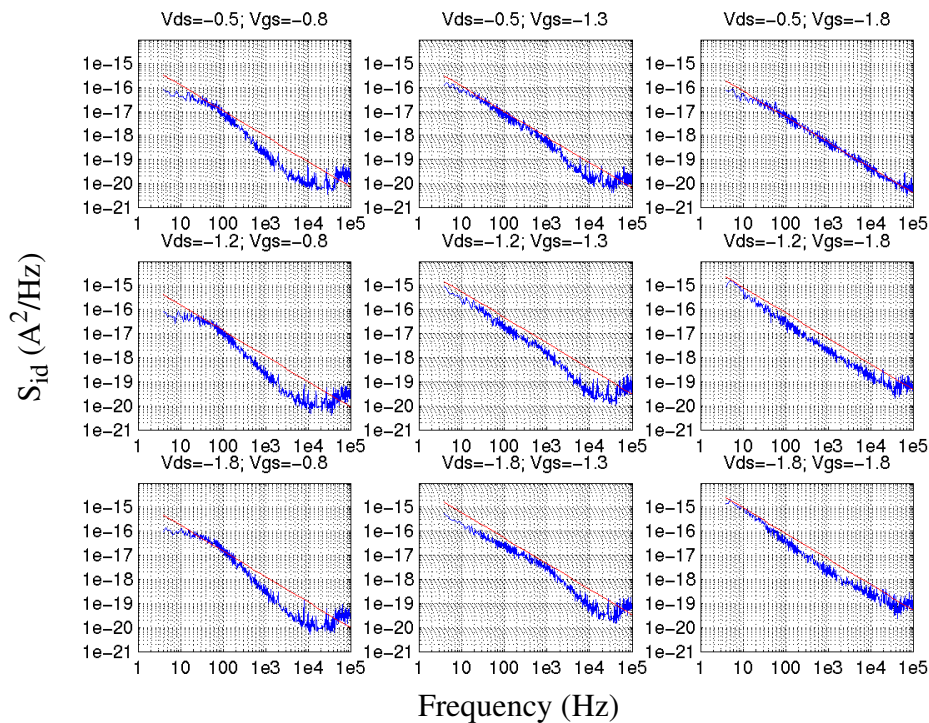


FIGURE 2.128 1.8v_p1x10x0p3_flicker model vs. measurements

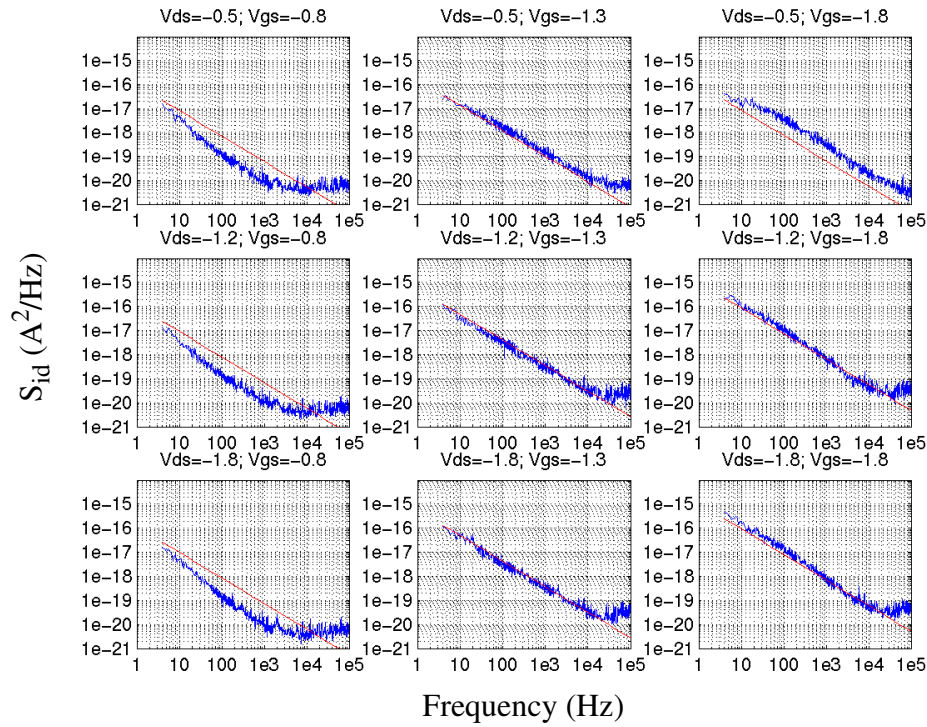


FIGURE 2.129 1.8v_p1x2x0p18_flicker model vs. measurements

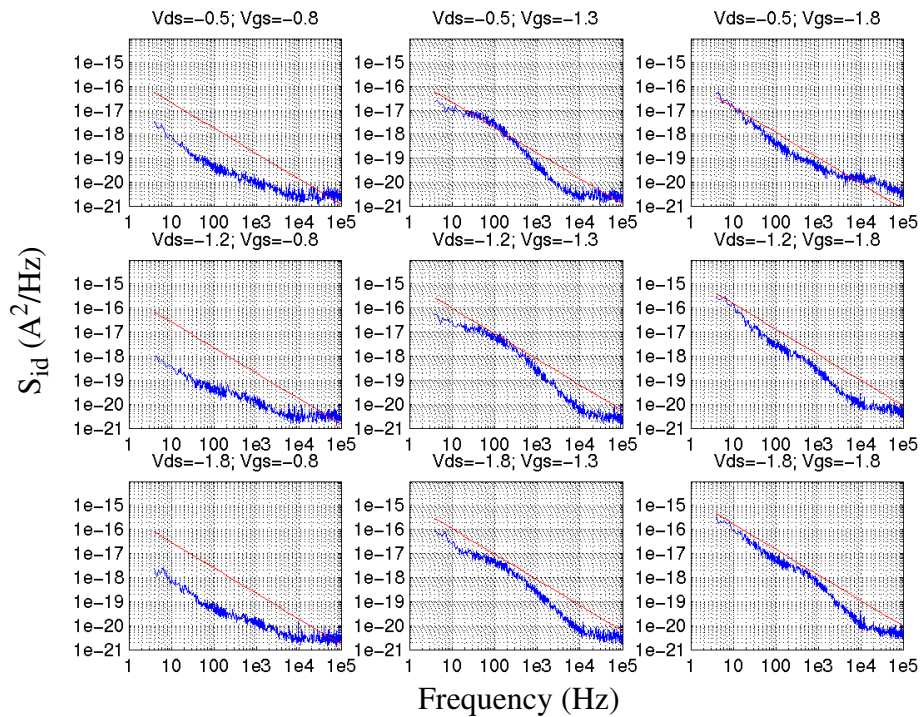


FIGURE 2.130 3.3v_n1x10x0p36_flicker model vs. measurements

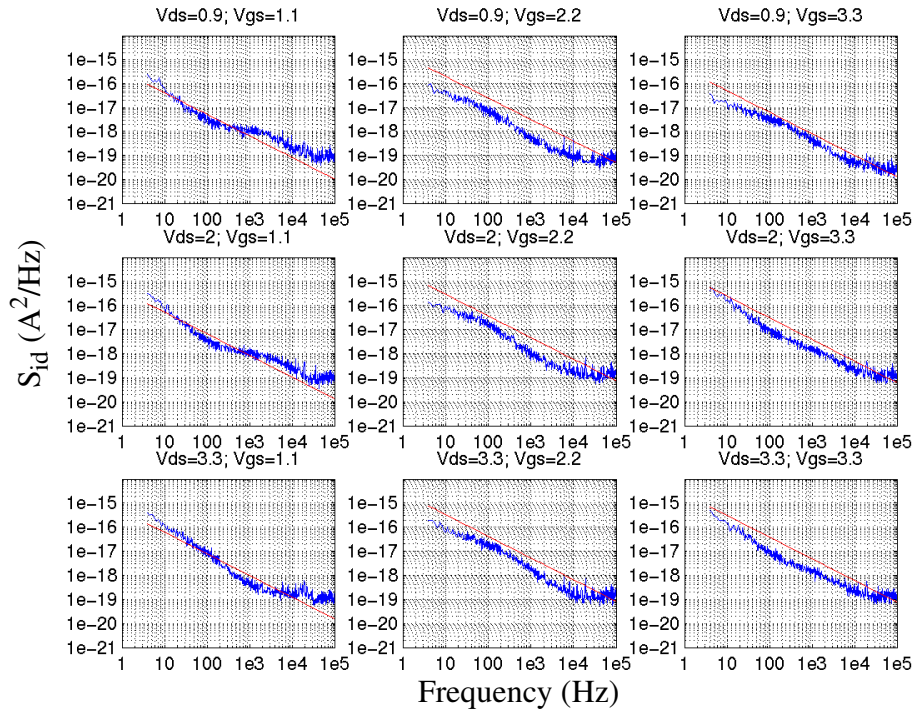


FIGURE 2.131 3.3v_n1x10x0p6_flicker model vs. measurements

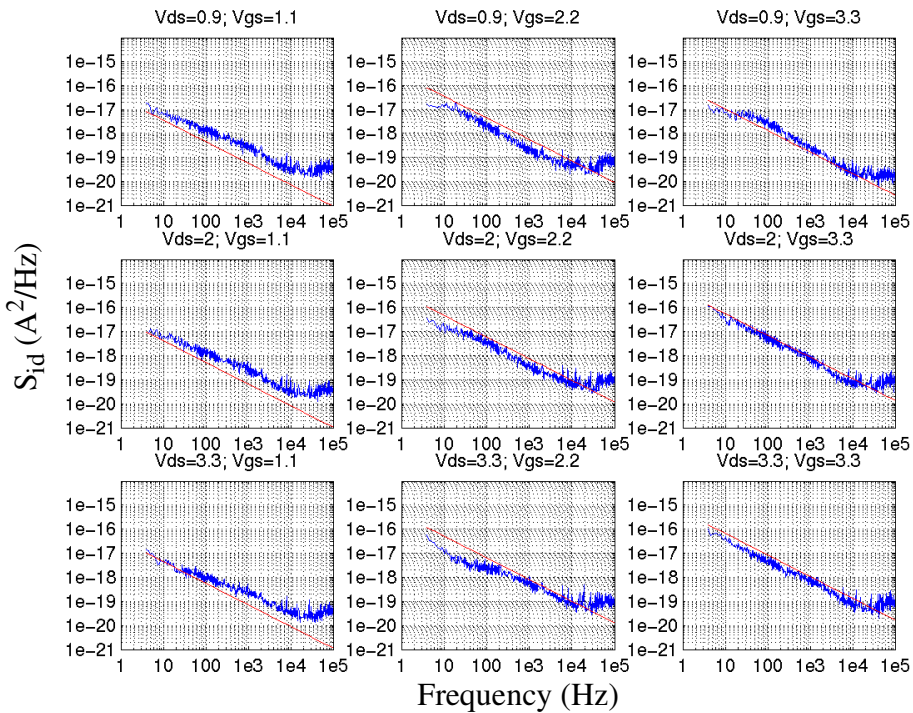


FIGURE 2.132 3.3v_n1x2x0p36_flicker model vs. measurements

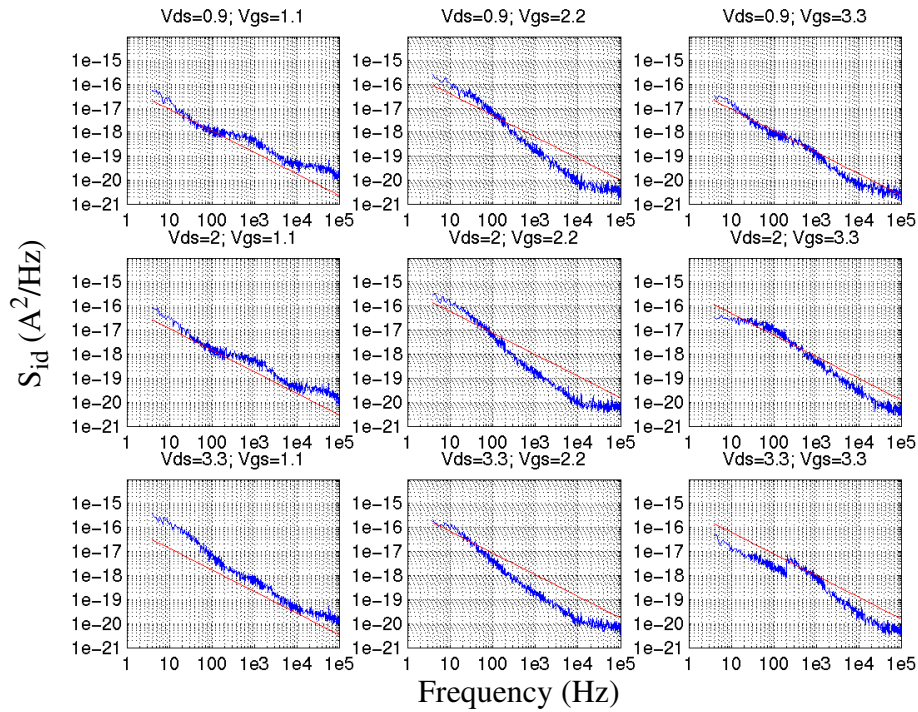


FIGURE 2.133 3.3v_p1x10x0p36_flicker model vs. measurements

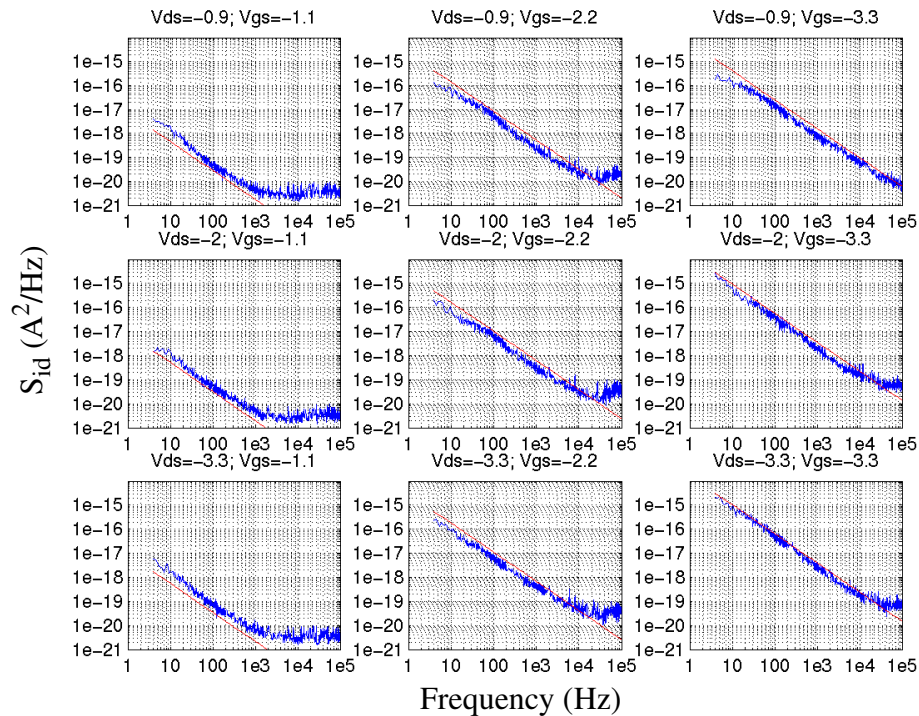


FIGURE 2.134 3.3v_p1x10x0p6_flicker model vs. measurements

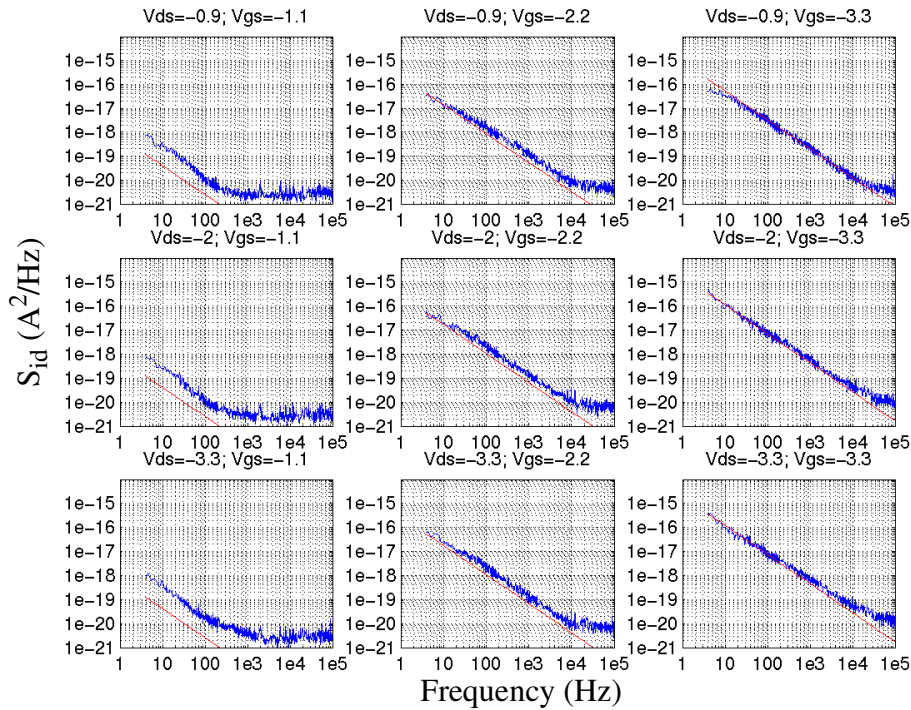


FIGURE 2.135 3.3v_p1x2x0p36_flicker model vs. measurements

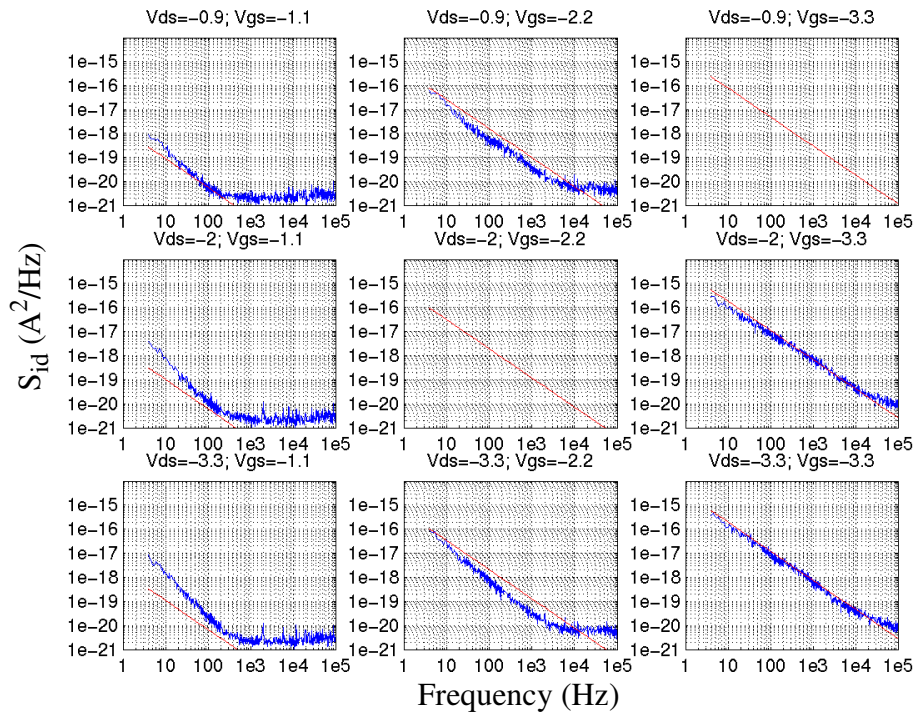
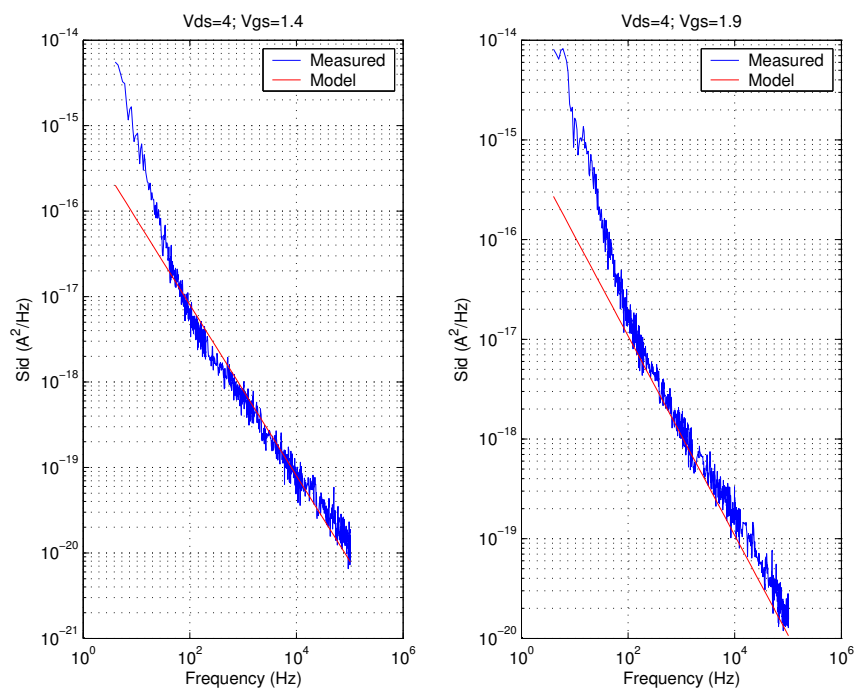
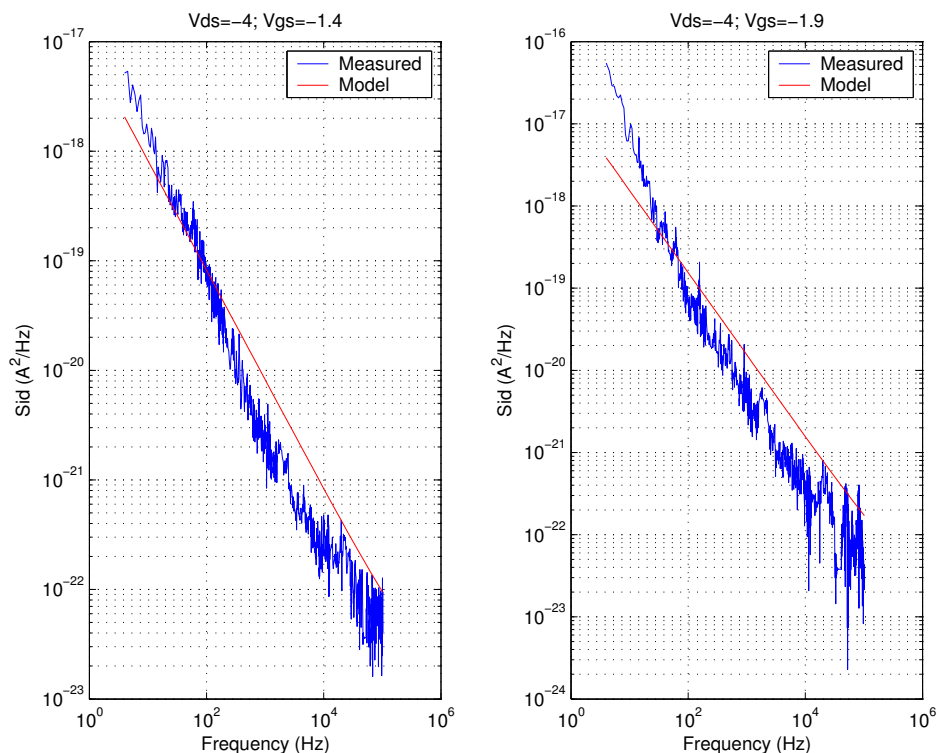


FIGURE 2.136 5V NFET Flicker Noise; NFxWxL = 1x25 μ m x 0.6 μ mFIGURE 2.137 5V PFET Flicker Noise; NFxWxL = 1x25 μ m x 0.6 μ m

2.9 Released model Quality Assurance (QA)

A rigorous QA procedure is executed before any new model release. The geometry dependence of 9 key device parameters is examined for any non-physical behavior for all 3 cases: Nominal, Fast, and Slow. These parameters are listed in Table 2.19 on page 103.

TABLE 2.19 MOSFET electrical parameter list examined as part of model release QA

Parameter	Description
v_t (V)	Threshold voltage in the linear region
k_b ($V^{0.5}$)	Body constant
i_{dsat} (mA)	Drain current at $V_{gs}=V_{ds}=V_{dd}$
st (mV/dec.)	Sub-threshold slope in the linear region evaluated at $V_{gs}=V_t/5$
β ($\mu A/V^2$)	Extracted from the max. g_m as: $1e6 \cdot (g_{m_max}/2 \cdot \text{abs}(v_d))$, where $\text{abs}(v_d)=0.05$ V is the drain voltage to bias the trans. in the linear region
g_{ds} (mhos)	Output conductance in the saturation region evaluated at $V_{gs}=V_{ds}=V_{dd}$
L_{eff} (μm)	Electrical channel length
W_{eff} (μm)	Electrical channel width
i_{off} (A)	Off-state leakage current at $V_{gs}=0$, $V_{ds}=V_{dd}$

Figures 2.138 through 2.141 illustrate the geometry dependence of these 9 parameters for the thin and thick-oxide N and P-FETs. For each device 4 plots are generated as per Table 2.20 on page 103. The right-hand most column in the table references the location of the plot. For e.g. the thin oxide NFET, electrical parameter vs. channel length for the $10\mu m$ wide device is on the top-right of Figure 2.138.

TABLE 2.20 MOSFET channel lengths and widths included as part of QA procedure

Variable dimension	Fixed dimension	Location on plots (Figure 2.138 through Figure 2.141)
Channel length (min. design rule $< L < 10\mu m$)	Channel width = $10\mu m$	Top-left
Channel length (min. design rule $< L < 10\mu m$)	Channel width = Min. design rule	Top-right
Channel width (min. design rule $< W < 10\mu m$)	Channel length = $10\mu m$	Bottom-left
Channel width (min. design rule $< W < 10\mu m$)	Channel length = Min. design rule	Bottom-right

FIGURE 2.138 1p8_nfet_qa_plots

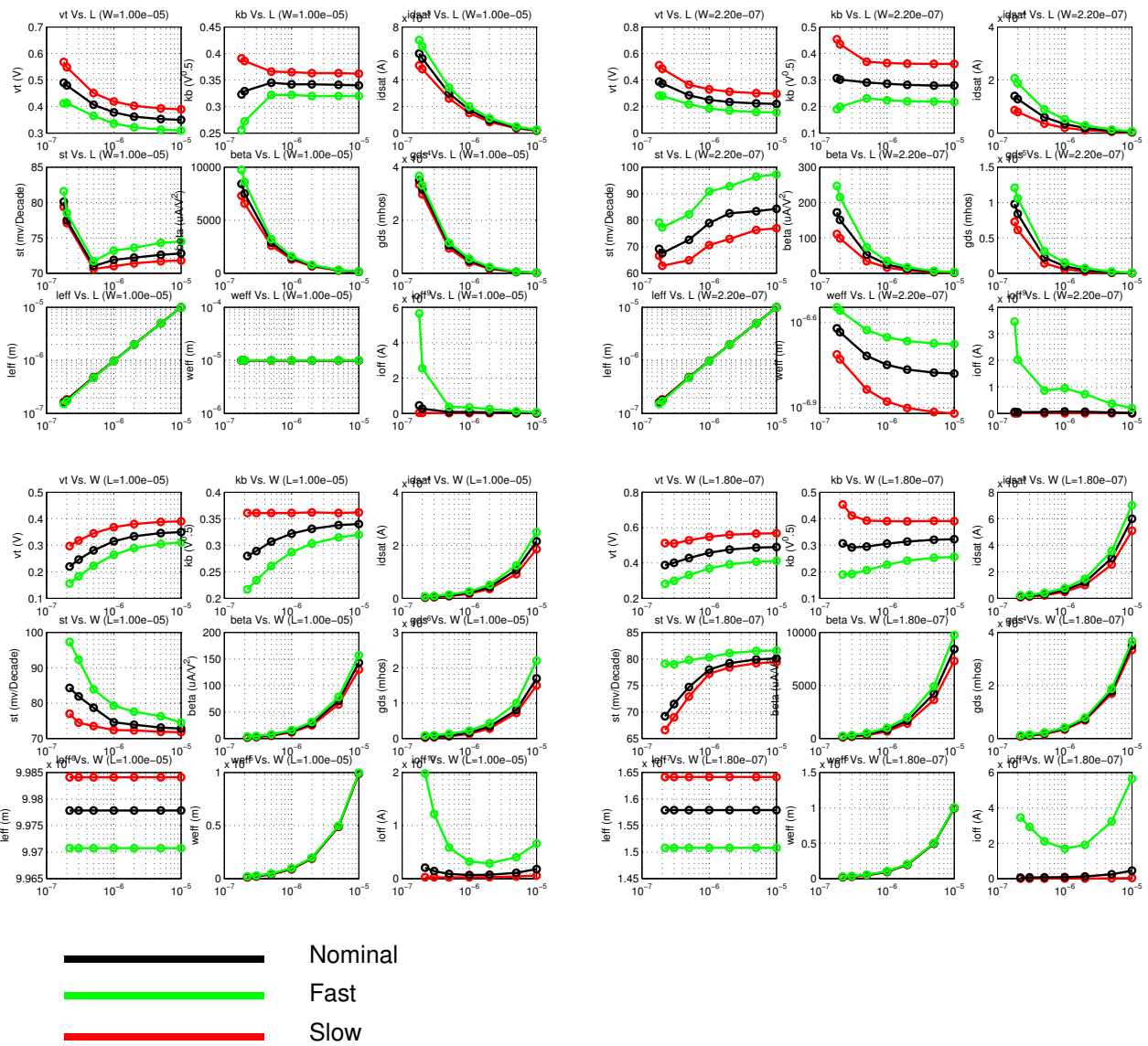


FIGURE 2.139 1p8_pfet_qa_plots

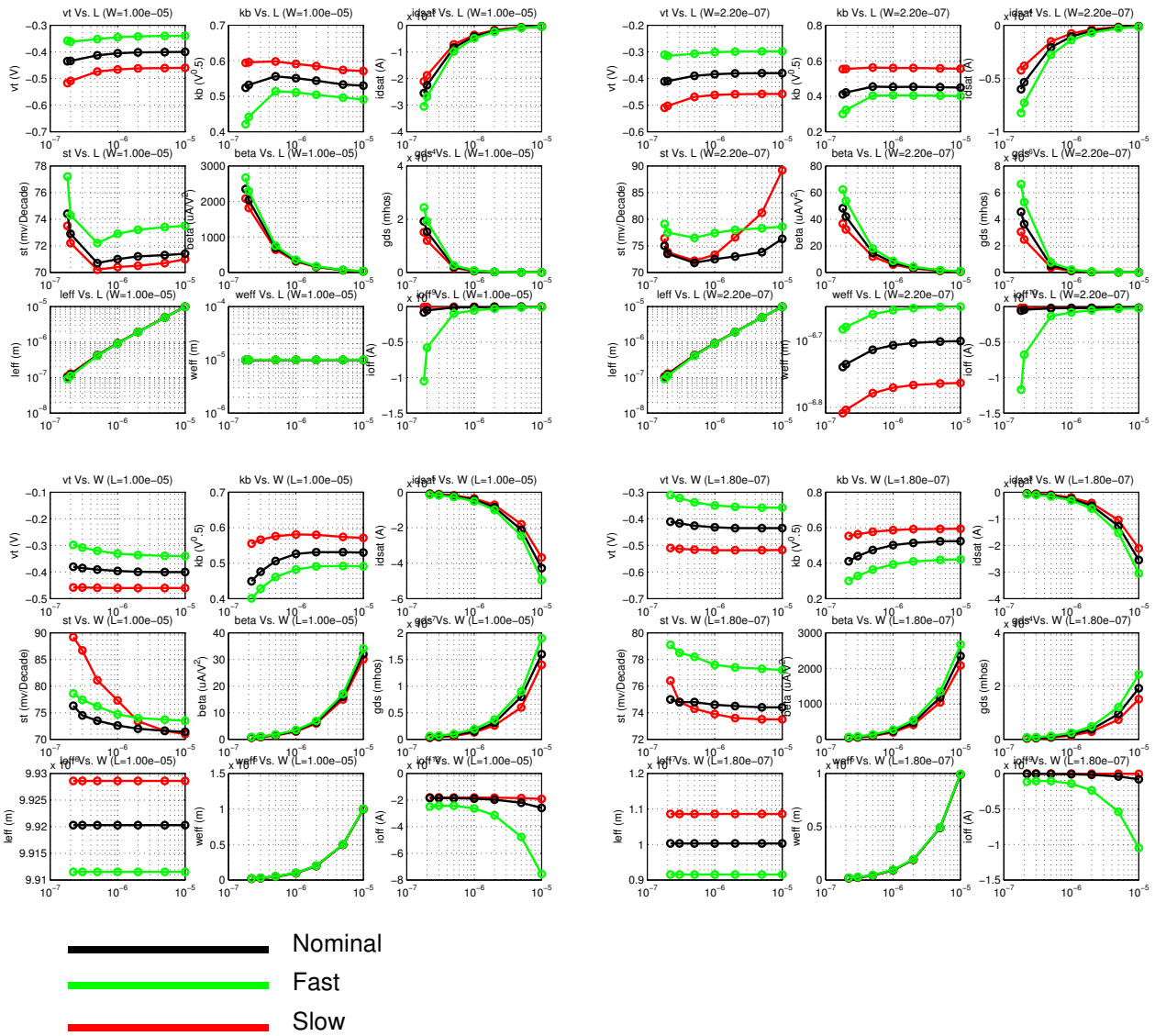


FIGURE 2.140 3p3_nfet_qa_plots

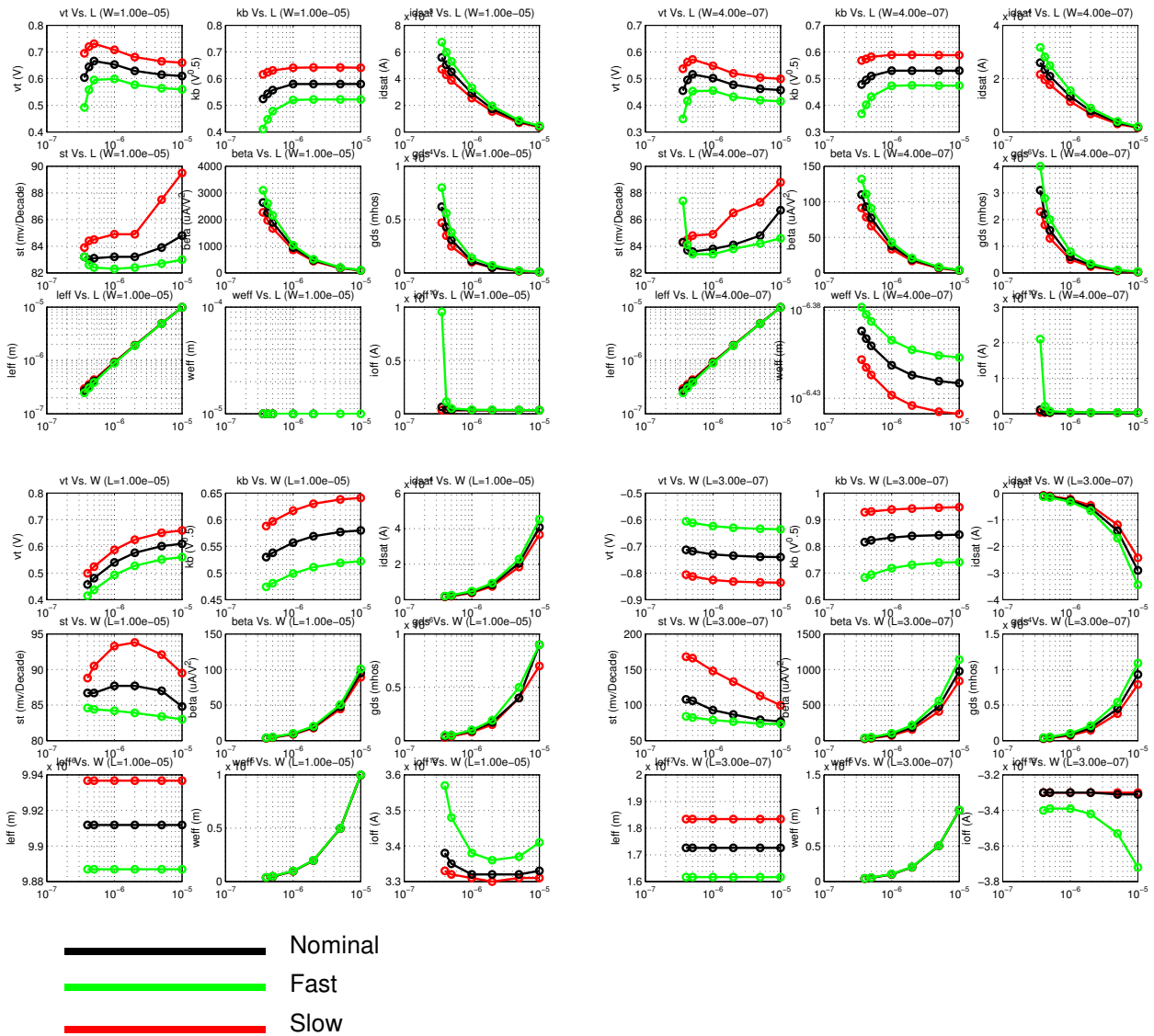


FIGURE 2.141 3p3_pfet_qa_plots

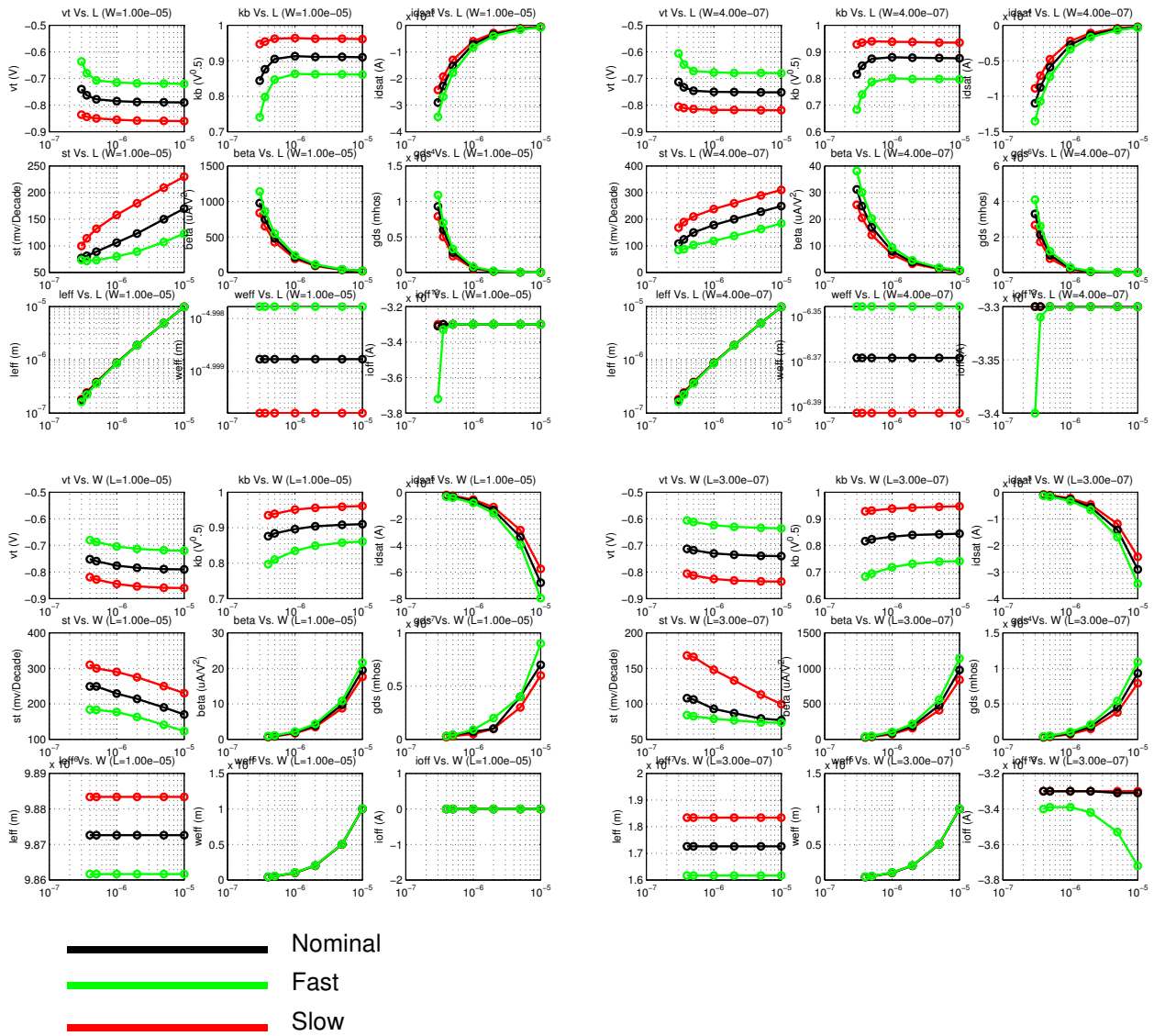


FIGURE 2.142 5V_NFET_qa_plots

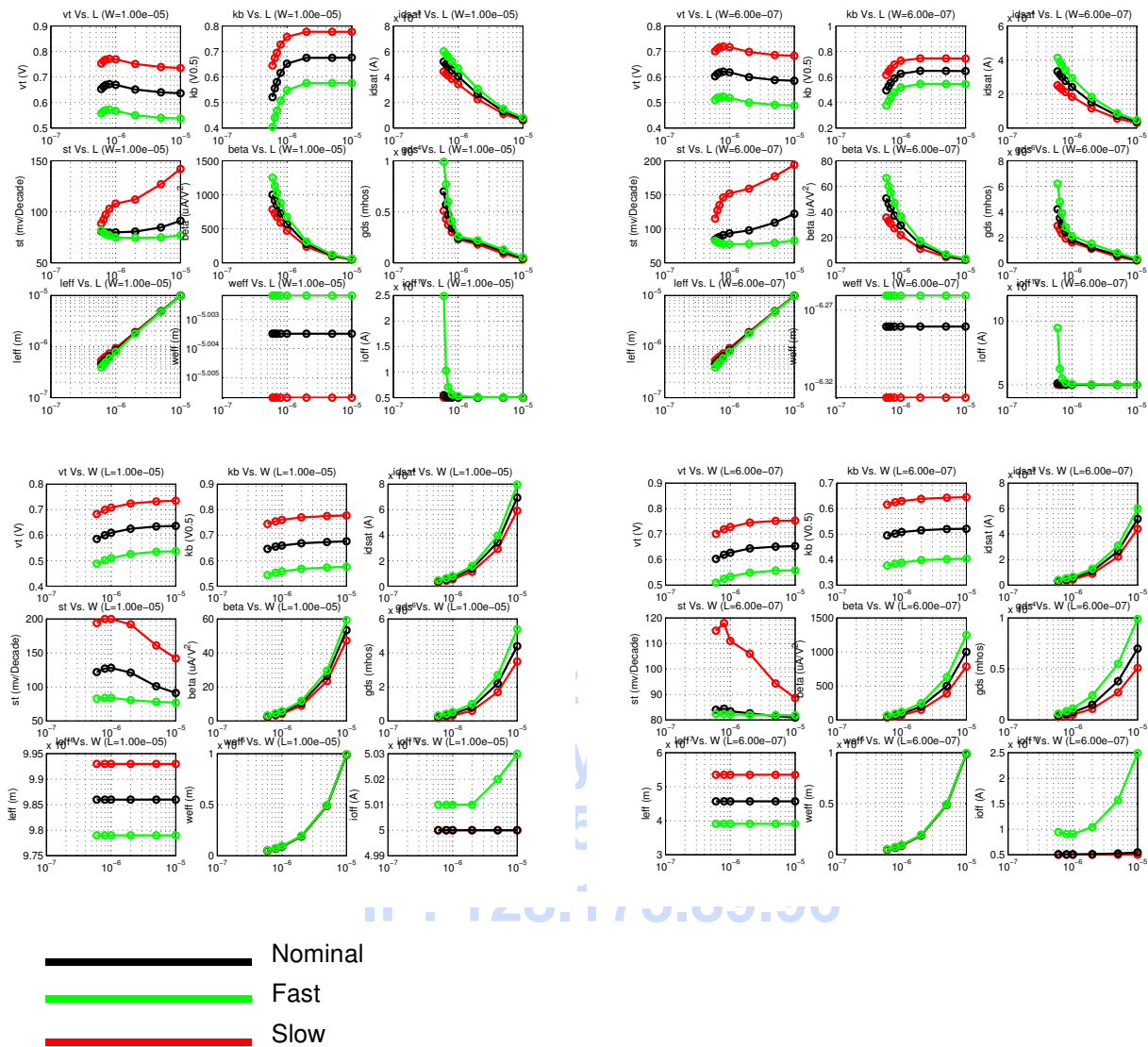
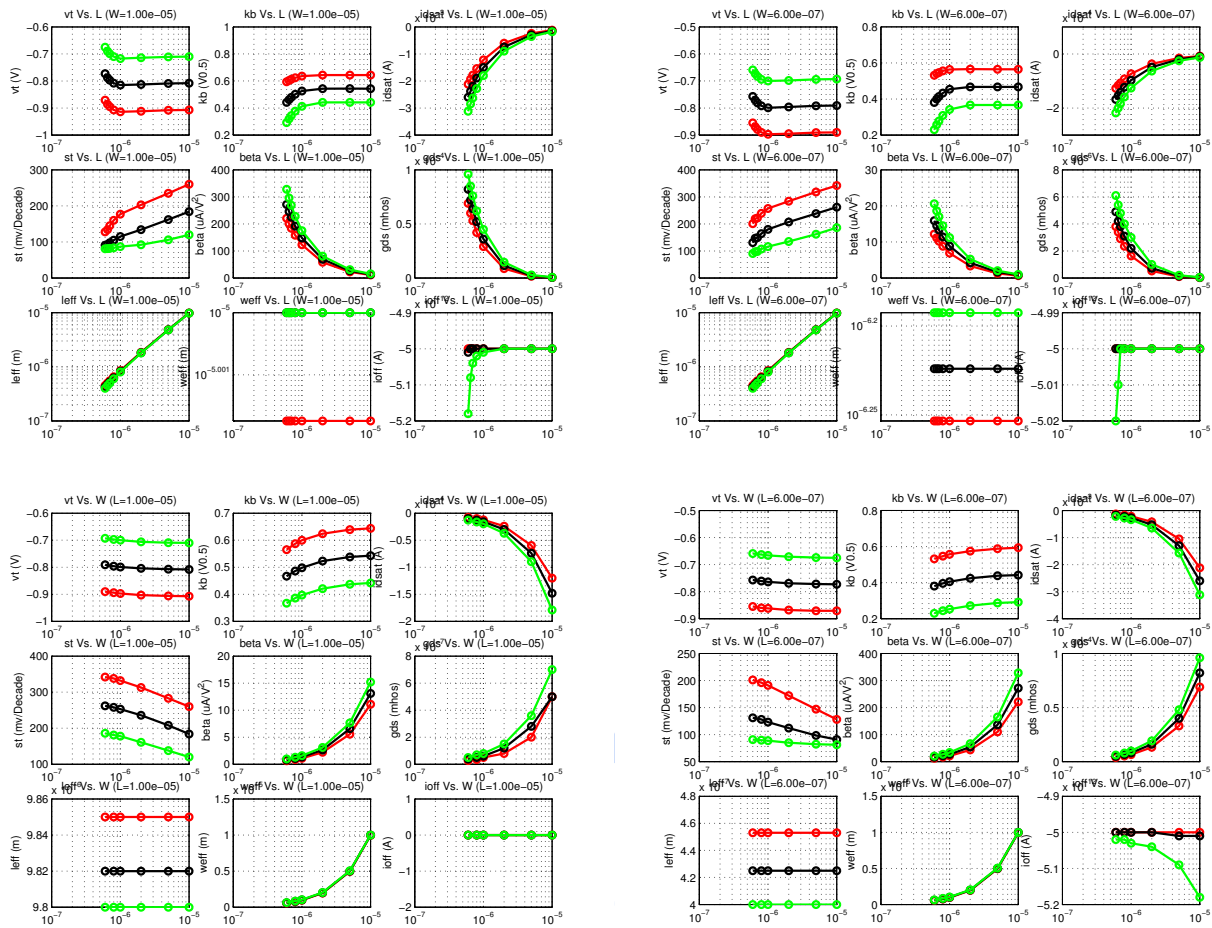


FIGURE 2.143 5V_PFET_qa_plots



— Nominal
— Fast
— Slow

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2.10 Model Update History

TABLE 2.21 Mixed-signal model specific updates in model release version 4.9

v4.9 update	Devices	Reason	Impact on user
Noimod changed from 2 to 1	All 1.8v and 3.3v FETs	Better off-state prediction of RF thermal noise	Reduced (1/10 - 1/200x) noise for $V_g \sim 0v$. 10-20% change in the on-state ($V_g > V_t$)
Change forward biased diode IV model parameters	All 1.8v and 3.3v FETs and diodes	Corrected un-physical diode ideality factors	Better prediction of forward biased current. Possible improvement in convergence in some simulations
Added parameter hdiff	All 1.8v and 3.3v FETs	Allows approximate calculation of as, ad, ps, pd (area and perimeter of source and drain) when primitive model (e.g. nfet) is used directly	No impact if as, ad, ps, pd are specified by user or if sub-circuit wrappers around primitives (nfets, pfets, ...) are used
Added ACM=12, CAP-CALCM=1 in HSPICE and ADS	All 1.8v and 3.3v FETs	Junction capacitance calculations are now compatible across simulators (Spectre, Hspice, ADS)	Increased junction capacitance for Hspice and ADS simulations in v4.9 (over v4.8)

TABLE 2.22 Mixed-signal model specific updates in model release version 5.0

v5.0 update	Devices	Reason	Impact on user
Corner/Statistical model oxide thicknesses	All 1.8v and 3.3v FETs	Updated to match new E-spec. w/ tighter variation	No change in NOMINAL model. Reduced corner/statistical model variation in gate oxide capacitance: 1.8v FETs corner model: v4.9 +/- 1Å; v5.0 +/- 1Å 1.8v FETs stat. model: v4.9 +/- 3Å; v5.0 +/- 1.5Å 3.3v FETs corner model: v4.9 +/- 2Å; v5.0 +/- 1.8Å 3.3v FETs stat. model: v4.9 +/- 6Å; v5.0 +/- 3Å
Corner and stat. parameters added to model process variation on drain/source series resistance	All 1.8v and 3.3v FETs	More physical corner and statistical models	No change in NOMINAL model. Larger gm variation in corner and statistical models for short channel FETs
Corner and stat. parameters added to model process variation on gate-source and gate-drain overlap capacitances	All 1.8v and 3.3v FETs	Corner and statistical models for overlap capacitance in v4.9 did not capture oxide thickness and ΔL variation	No change in NOMINAL model. Larger gate-source and gate-drain overlap capacitance variation in corner and statistical models
Statistical correlation added to FASTSLOW and SLOW-FAST corners	All 1.8v and 3.3v FETs	Improved correlation matching between N and PFETs	Reduced oxide thickness, ΔL , and ΔW variation when simulating with the FASTSLOW and SLOW-FAST corners

TABLE 2.23 Mixed-signal model specific updates in model release version 6.0

v6.0 update	Devices	Reason	Impact on user
X-Sigma Corner Model Support	All 1.8v and 3.3v FETs	Allow for process variation settings different than conventional +/- 3 sigma-corner models	Added flexibility in corner simulation
Switch to unified BSIM3 flicker noise model	All 1.8v and 3.3v FETs	More accurate modeling of flicker noise bias dependence	Change from gm based model which over predicted noise at low Vgs. Noise sensitive circuits at low Vgs should match silicon better.
Add "multiplicity" to mismatch model	All FETs	Mismatch should improve with multiple devices	Correct modeling of transistor mismatch for m>1

TABLE 2.24 Mixed-signal model specific updates in model release version 6.2

v6.2[a-d] update	Devices	Reason	Impact on user
Re-centered NOM, SLOW, and FAST corners and statistical models to new E-specs	All FETs	Reflects most recent Fab data	In general, a tighter process variation in key E-specs such as V_t , I_{dsat} and Body effect for large geometry devices, while the process variation for smaller geometry devices is relatively unchanged.
Various minor syntactical bug-fixes	Various FETs	Certain sections such as monte-carlo or x-sigma were not simulating	Ability to run certain monte-carlo and x-sigma analysis
Updated flicker noise model parameters	QLD FETs	Replaced default BSIM model with more realistic numbers	Improved noise simulations

TABLE 2.25 Mixed-signal model specific updates in model release version 6.3

v6.3 update	Devices	Reason	Impact on user
Re-formatted models to align with "GTE" formatted Cadence PDKs. Schematic and post-layout instance names are now the same	All CMOS FETs	Added ability to simulate mismatch in post-layout simulations	No impact if using models via Cadence PDK. Capability to simulate mismatch in post-layout views.

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2.11 References

1. BSIM3 Modeling Package, Agilent 85194E, "http://www.admos.de/uploads/media/bsim3_datasheet_02.pdf"
2. T. Gneiting, "A Unified Environment for the Modeling of Ultra Deep Submicron MOS Transistors," Nanotech 2003 Conference
3. Colin C. McAndrew, "Statistical Circuit Modeling," SISPAD 98

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3.0 RF CMOS MODEL

3.1 Model list and description

The SBC18 process supports two different RF models. The first model relates to the thin gate-oxide FETs with a maximum operation voltage of 1.8v. The second model relates to the thick gate-oxide FETs with a maximum operation voltage of 3.3V.

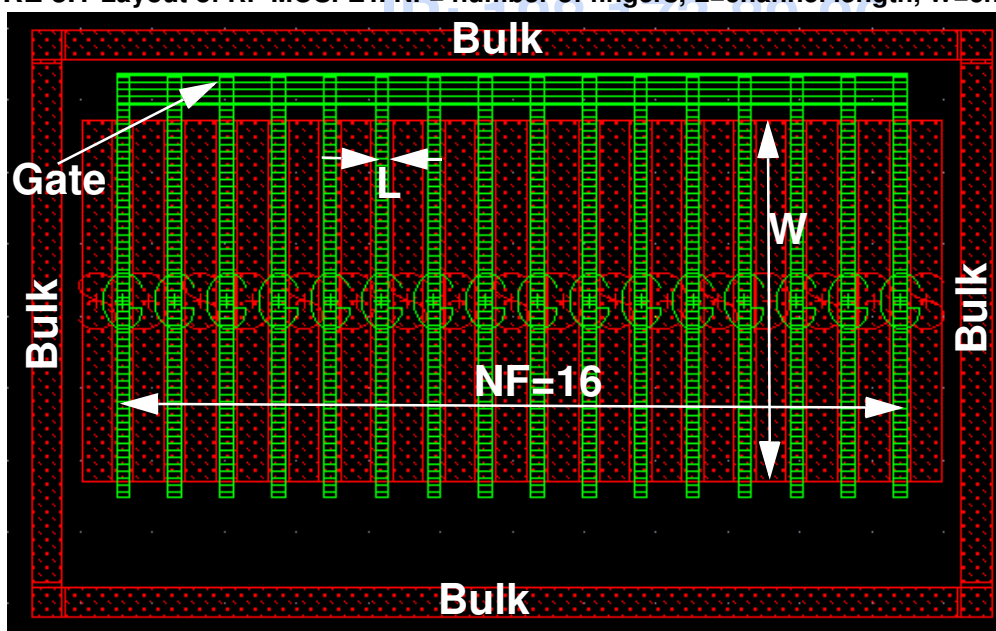
TABLE 3.1 FET model summary for 1.8 and 3.3v FETs

Property	1.8v RF FETs	3.3v RF FETs
Design Kit Cell Name	nfet_rf, pfet_rf	n3p3fet_rf/nfet3p3_rf, p3p3fet_rf/pfet3p3_rf
Temperature Range	25°C	25°C
Channel Length	0.18μm ≤ L ≤ 0.5μm	0.36μm ≤ L ≤ 0.5μm NFET 0.3μm ≤ L ≤ 0.5μm PFET
Channel Width	2μm ≤ W ≤ 10μm	2μm ≤ W ≤ 10μm
No. of fingers	1 ≤ NF ≤ 100	1 ≤ NF ≤ 100
Bias Range	Vgs : 0 ~ 1.8V, Vds : 0 ~ 1.8V, Vbs : 0 ~ 1.8V	Vgs : 0 ~ 3.3V, Vds : 0 ~ 3.3V, Vbs : 0 ~ 3V

Using these models outside of the specified ranges may generate simulation errors. The RF model is based on the core MS model which has been validated over for temperatures valid from -40 to 125°C. Though no RF model validation is performed at temperatures other than 25°C, the RF model should provide a reasonable estimate of RF properties when simulated at temperatures in -40 to 125°C range.

3.2 Layout

FIGURE 3.1 Layout of RF MOSFET. NF= number of fingers, L=channel length, W=channel width



The top view of a RF MOSFET is shown in Figure Figure 3.1 with the key design parameters (NF, L, and W). Note that the total width of the RF MOSFETs is equal to NF*W. RF transistors are typically laid out as multi-finger devices to minimize gate resistance and parasitic junction effects. These improvements translate into higher cutoff (f_t) and maximum oscillation frequencies (f_{max}) as well as lower device noise. The gate resistance can further be improved by contacting the gate on multiple sides as per Eq. 1.

$$R_g = W \cdot \frac{R_{polySheet}}{NF \cdot 3 \cdot L \cdot N_{gc}^2} + \frac{\rho_c}{NF \cdot W \cdot L} \quad (EQ 1)$$

where $R_{polySheet}$ is the silicided poly sheet resistance, N_{gc} is the number of sides that the gate is contacted from, and ρ_c is the contact resistance per unit area between the silicide and the polysilicon gate, and represents an additional component of the gate resistance, dominant for narrow widths ($< 3\mu m$). The factor 3 is due to the distributed nature of this resistance at high frequencies. Only a single sided gate contact is supported in the p-cell ($N_{gc}=1$), and is consistent with the layout shown in Figure 3.1. The various components of the gate resistance in a RF FET are shown in Figure 3.2. The model includes the gate resistance intrinsic to the FET. The interconnect (metal wiring to the intrinsic FET) resistance is not shown in Figure 3.2. The interconnect resistance can be an important component of the gate resistance, and should be included in the post-extraction simulation of the FETs.

Like the gate resistance, the substrate resistance is also layout dependent. The default model for both the 1.8v and 3.3v RF FETs is for a ring of substrate contacts around the active FET, and corresponds to the “lbrt” Tap Style (Left, Right, Top, and Bottom), as shown in Figure 3.3. The 2-sided substrate model is also available corresponding to the “lr” Tap Style (Left and Right). The use of a ringed substrate can significantly reduce the “roll-up” in drain-source conductance g_{ds} (or reduction of output resistance r_o) at high frequencies (Figure 3.4). One-sided contacts or two-sided contacts on the top and bottom are supported by the p-cell, and default to a “lr” Tap Style in the model. The use of Tap Styles other than “lr” or “lbrt” may result in reduced accuracy of the simulations.

FIGURE 3.2 Components of the gate resistance in a RF-FET

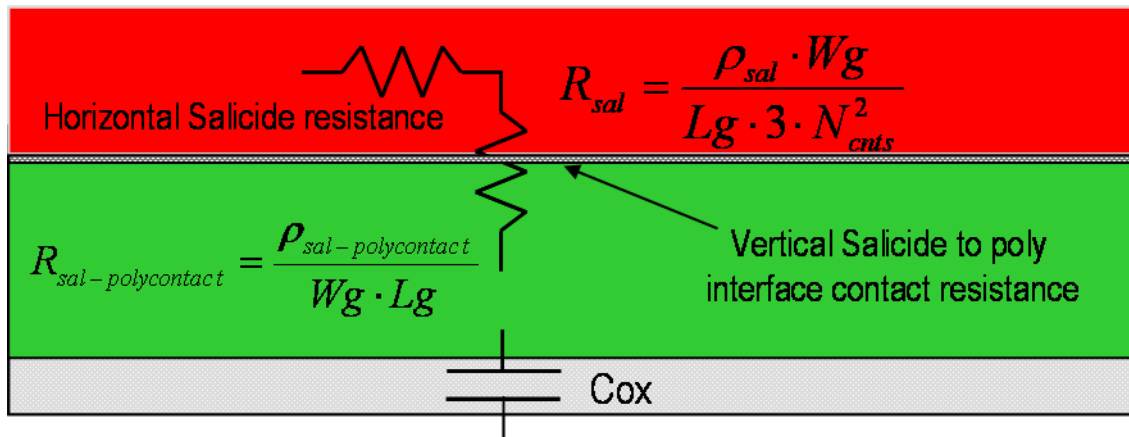


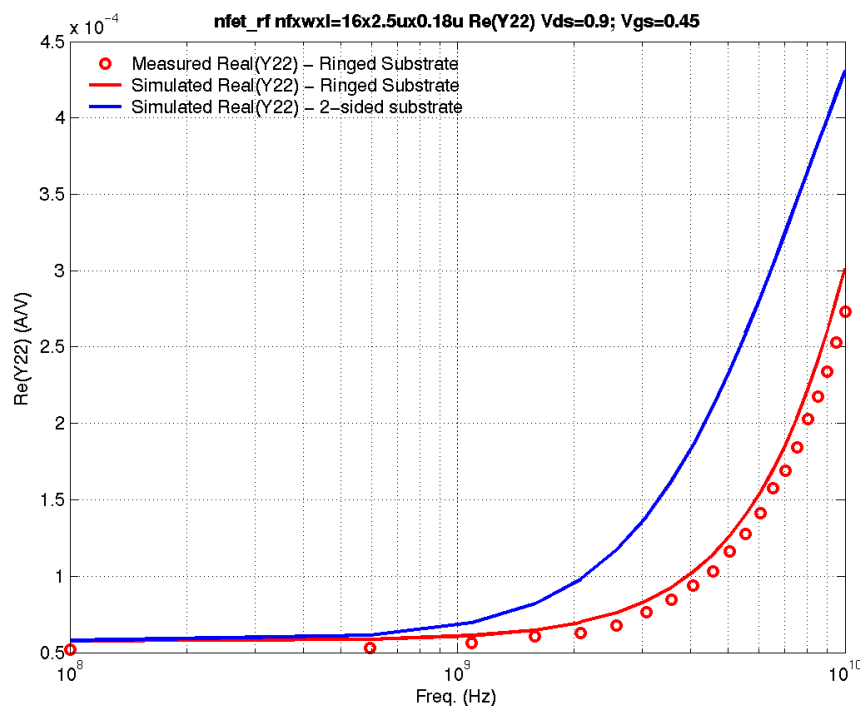
FIGURE 3.3 CDF selection options for 1.8v RF FETs

Model Name	nfet_rf
Substrate Node	sub
Count	1
Width (finger)	10u M
Length	180.0n M
Number of Fingers	1
Number of Slices	1
Current	0 A
Simulation parameters update	
High Freq Noise Opt	0
Bulk	lbrt

High Frequency Noise Opt: (1.8v RF NFET only) is turned off by default. Set to "1" to simulate excess high frequency noise (Section 3.7)

Bulk: Default model is consistent with the "lbrt" option. This corresponds to a 4-sided "ring" of substrate contacts. The model also supports the "lr" or 2-sided (Left and Right) option.

FIGURE 3.4 Impact of "ringed-substrate" on the output conductance



3.3 Measurements

Transistors with multiple widths, channel lengths and number of fingers were measured to extract a model that is scalable over the design space. Measurements were made on Ground-Signal-Ground test-structures with a 150 μm pitch between the pads. The list of transistors measured for the thin and thick-oxide FETs is shown in Table 3.2 on page 116.

TABLE 3.2 List of devices measured for RF model extraction

Thin oxide (N and P FETs)			Thick oxide (N and P FETs)		
NF	W (μm)	L (μm)	NF	W (μm)	L (μm)
10	10	0.18, 0.22, 0.3, 0.38, 0.5	10	10	0.36, 0.42, 0.5, 0.6, 0.7
10	2,5	0.18	10	2,5	0.36
11,5,4,3,1	10	0.18	11,5,4,3,1	10	0.36
			10	4	0.3 (PFET only)

The s-parameters of the RF MOSFETs, were measured on HP 8510C network analyzer. The frequency was swept from 0.1 to 10GHz. The list of biases for the thin and thick-oxide FETs is shown in Table 3.3 on page 116.

TABLE 3.3 List of biases at which s-parameters were measured for the thin and thick-oxide FETs

Thin oxide		Thick oxide	
Vgs (V)	Vds (V)	Vgs (V)	Vds (V)
0	0,0.45,0.9,1.35,1.8	0	0,0.825,1.65,2.475,3.3
0.45	0,0.45,0.9,1.35,1.8	0.825	0,0.825,1.65,2.475,3.3
0.9	0,0.45,0.9,1.35,1.8	1.65	0,0.825,1.65,2.475,3.3
1.35	0,0.45,0.9,1.35,1.8	2.475	0,0.825,1.65,2.475,3.3
1.8	0,0.45,0.9,1.35,1.8	3.3	0,0.825,1.65,2.475,3.3

3.4 Modeling

The BSIM3v3 MOSFET model described in the chapter 2.0 is valid at low frequencies (< 200MHz). At higher frequencies, the coupling between the source and drain through the bulk and the distributed resistance and capacitance effects require the gate, substrate and source/drain coupling networks to be explicitly included. The core mixed-signal (MS) model can be extended for use at high frequencies by adding parasitic resistances and capacitances as shown in Figure 3.5. The gate resistance R_g is modeled via Eq. 1 and has a direct impact on the input admittance [1]:

$$Re(Y_{11}) \sim R_g \cdot Im(Y_{11})^2 \quad (\text{EQ 2})$$

where $Im(Y_{11}) \sim \omega \cdot C_{gate}$.

The substrate network includes 3 resistances in a T-network. R_{db} which models the drain-bulk coupling, and R_{sb} which models the source-bulk coupling are given by:

$$R_{sb} = R_{sbSheet} \times \frac{L}{(2 \times W \times NF)} \quad (\text{EQ 3})$$

$$R_{db} = R_{dbSheet} \times \frac{L}{(2 \times W \times NF)} \quad (\text{EQ 4})$$

where $R_{sbSheet} = R_{dbSheet}$, is the sheet resistance of the region that couples the ac signal from the source to the drain, and is fit to the measured data. The third resistor in the T-network represents the bulk resistance and is modeled by splitting it into 2 components given by Eqs. 5 and 6:

$$R_{dsbv} = R_{dsbSheet} \times \frac{(W/2 + W_{act2act} + W_{act2con})}{2 \times (L + 2 \times (W_{con2gate} + W_{con} + W_{act2con})) \times NF} \quad (\text{EQ 5})$$

where, R_{dsbv} is the vertical component of substrate resistance to the top and bottom taps, $R_{dsbSheet}$ is the sheet resistance of the well and is extracted from the measured s-parameter data, $W_{act2act}$ is the distance between the active regions of the FET and substrate contacts ($=1.16\mu\text{m}$), $W_{act2con}$ is the minimum design rule for the active to contact ($=0.1\mu\text{m}$), $W_{con2gate}$ is the distance between contact and gate, and W_{con} is the width of the contact.

$$R_{dsbh} = R_{dsbSheet} \times \frac{(L/2 + W_{con2gate} + W_{con} + W_{act2con} + W_{sti} + W_{act2con})}{2 \times W} \quad (\text{EQ 6})$$

where R_{dsbh} is the horizontal component of the substrate resistance to the left and right taps, and W_{sti} is the width of the isolation. R_{dsbh} is calculated for the two outermost fingers of the RF FET, as the contribution from the inner fingers has negligible impact on this resistance for layouts with $NF > 4$. The substrate resistance of the RF FETs is either:

$$R_{dsb} = R_{dsbh} \quad (\text{EQ 7})$$

for a 2-sided substrate contact (corresponding to Tap Style “lr” in Figure 3.3), or

$$R_{dsb} = R_{dsbh} \parallel R_{dsbv} \quad (\text{EQ 8})$$

for a 4-sided “ringed” substrate contact (corresponding to Tap Style “lbrt” in Figure 3.3).

Collectively the substrate network (R_{sub}) impacts the output impedance:

$$R_{sub} \sim Re(Y_{22})/(\omega^2 \cdot C_{db}) \quad (\text{EQ 9})$$

The transmission parameter from gate to drain:

$$Y_{12} \sim -j\omega C_{gd} - \omega^2 \cdot C_{gd} \cdot C_{gg} \cdot R_g \quad (\text{EQ 10})$$

where C_{gd} is the overlap capacitance extracted at low-frequency as described in Section 2.4.2 on page 22.

The drain resistance impacts the reverse transmission parameter from drain to gate:

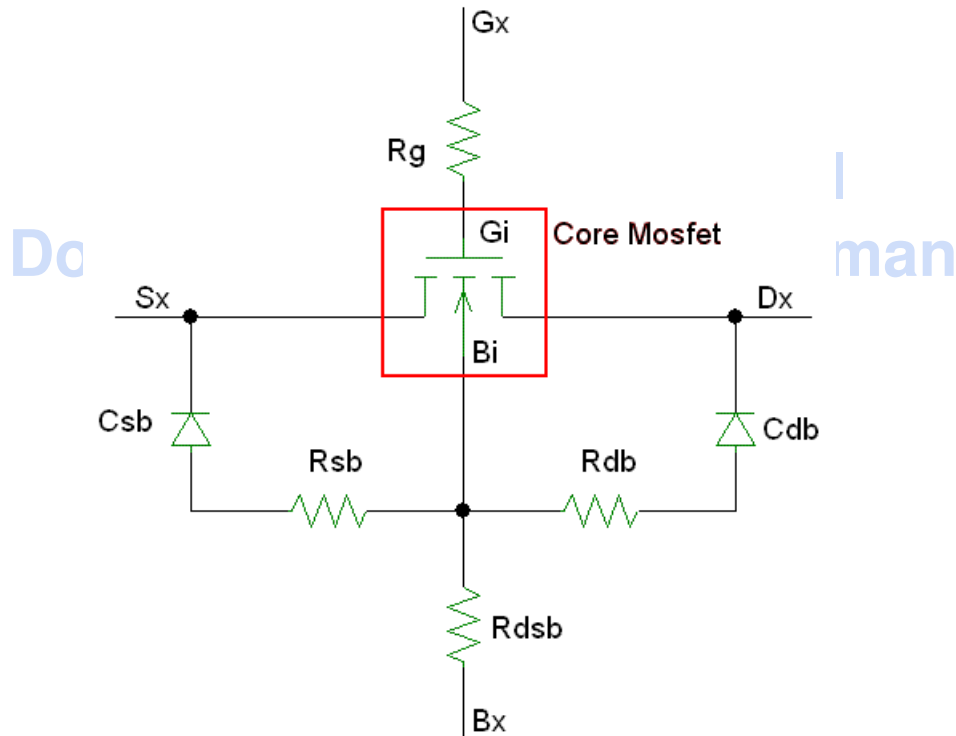
$$Y_{21} \sim -j\omega C_{gd} - \omega^2 \cdot (C_{gd}^2 \cdot R_d + C_{gd} \cdot C_{gg} \cdot R_g) \quad (\text{EQ 11})$$

The drain and source resistances and their associated gate-bias dependencies are included in the core MS model and are not explicitly modeled in the sub-circuit. Modeling these resistors as extrinsic lumped elements in the sub-circuit results in inaccurate predictions of g_m and g_{ds} ; essential in both ac and noise simulations.

The area (C_j) and perimeter components (C_{jsw} , C_{jswg}) of the junction capacitance are pulled out (i.e. set to 0) from core mixed-signal model and placed as external diodes in the sub-circuit (C_{db} , C_{sb}) to model the capacitive coupling of the drain-bulk and source-bulk junctions.

A PSP model option, that includes the modeling of non-quasi-static effects, is also available via the Jazz model selection form. In general, the PSP model provides a more accurate description of the measured data, but due to its relatively new introduction the BSIM option continues to be the default model for the SBC18 design kit. As such, all subsequent model validation plots refer to the model playbacks using the BSIM option.

FIGURE 3.5 Sub-circuit used to model the 1.8 and 3.3v RF FETs



3.5 Corner and statistical models

The core MS corner and statistical model parameters in the RF sub-circuit extension are identical to what was described in Section 2.6 on page 83, and are valid at higher frequencies. In addition, the gate resistance is changed by $\pm 24\%$ for the SLOW/FAST corner cases. Similarly, a $\pm 24\%$ variation is used to model the 3σ variation of this parameter in the statistical models. The 3σ variation of the silicided poly sheet resistance is consistent with E-specs specified for silicided poly resistors in Table 9.1.

3.6 Y-parameter Playbacks

The simulated y-parameters and the cut-off frequency (f_t) of the various MOSFETs are compared with the measured data in Figures 3.6 through 3.25. The plots are for multiple biases which include the linear and saturation regimes. The device description is included in the figure caption using the notation:

max_operating_voltage_fetType_NFxWxL. Y-parameters are shown since they lend better meaning to the device performance than s-parameters.

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Date: 08/15/2012 10:15
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FIGURE 3.6 1p8_nfet_10x5x0p18

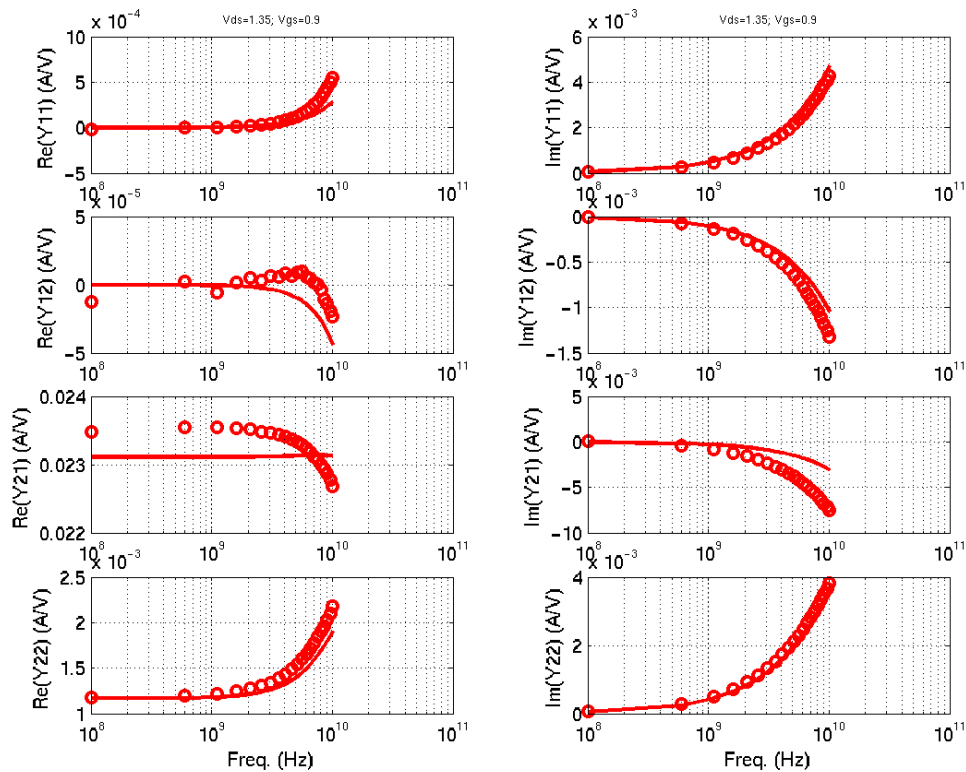
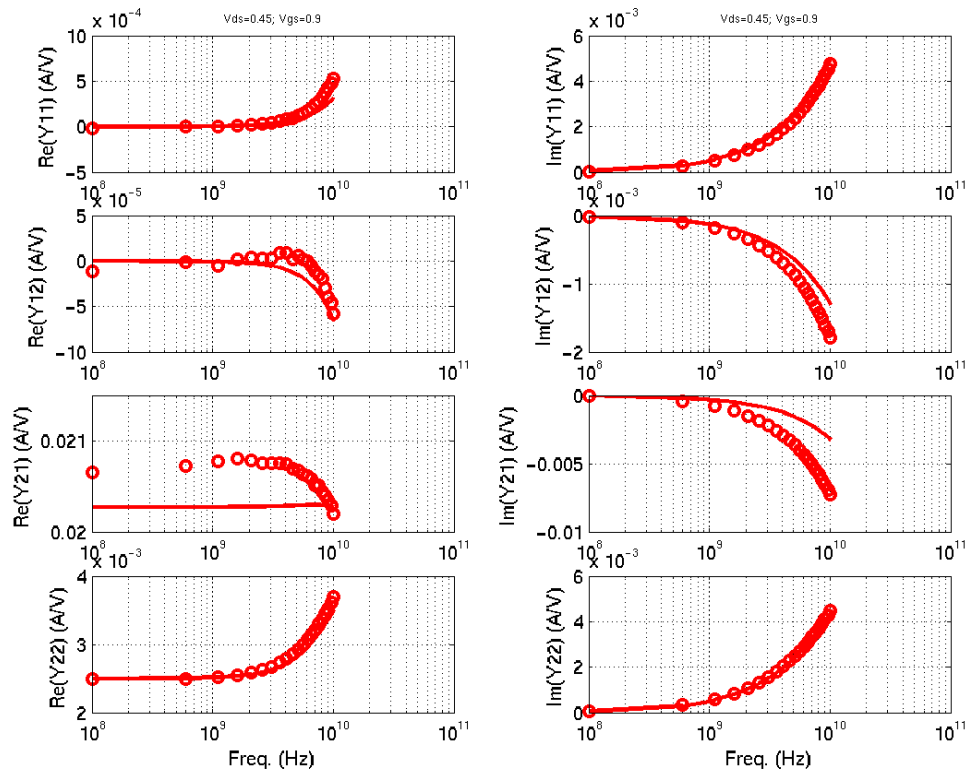


FIGURE 3.7 1p8_nfet_10x2x0p18

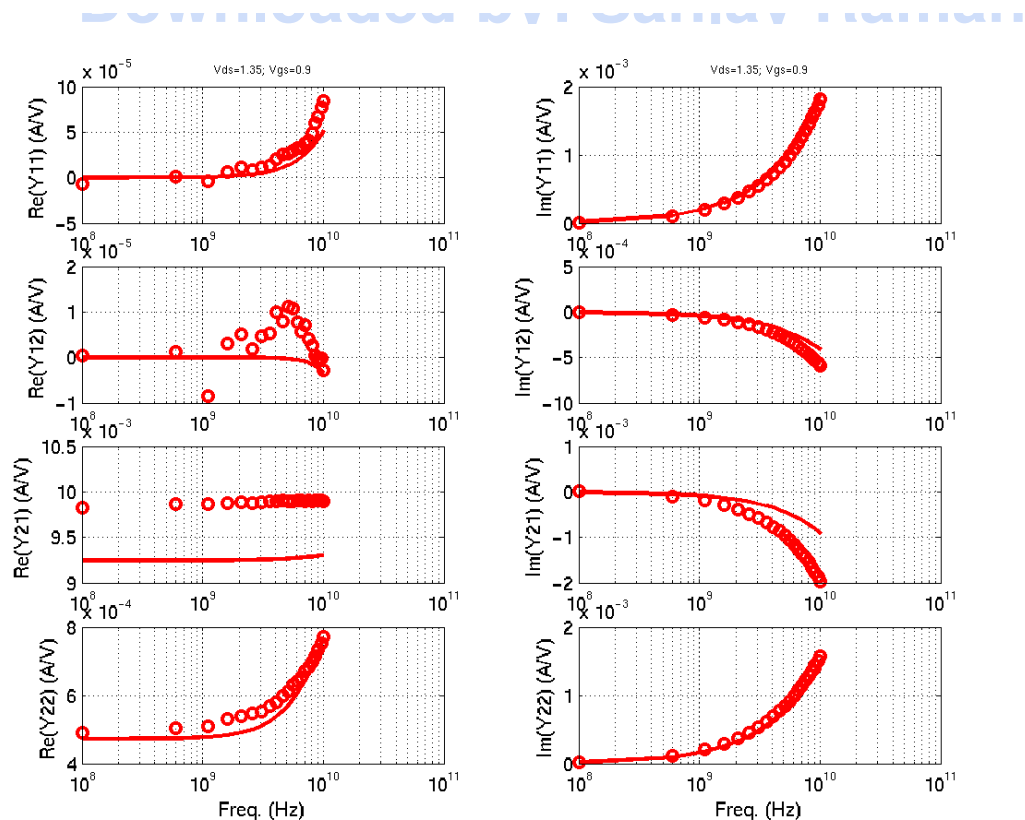
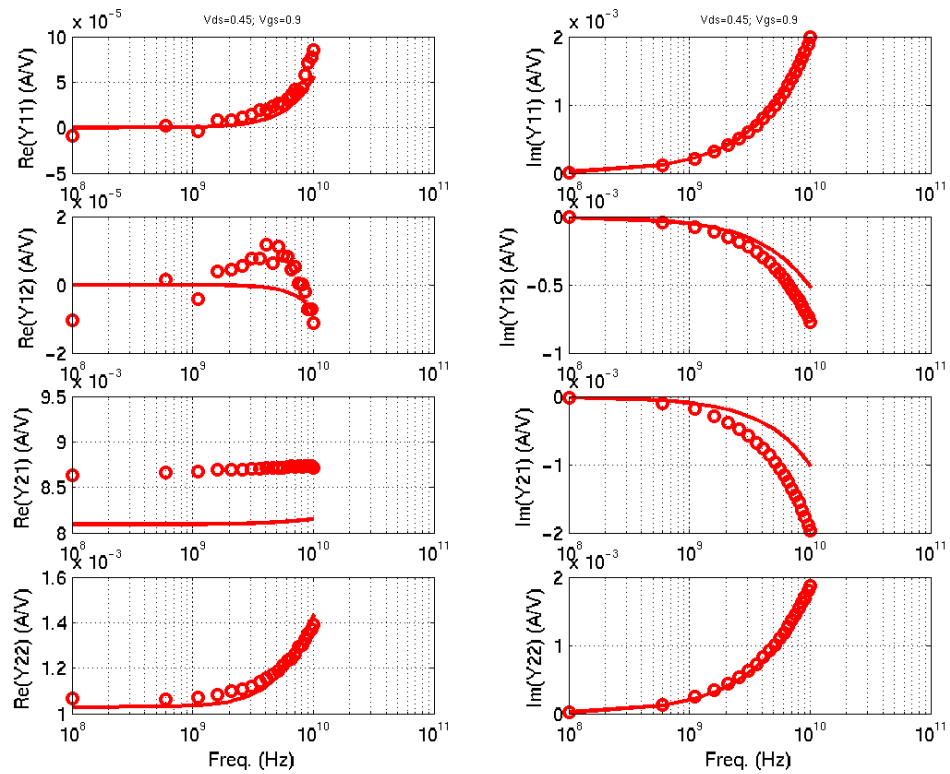


FIGURE 3.8 1p8_nfet_10x10x0p22

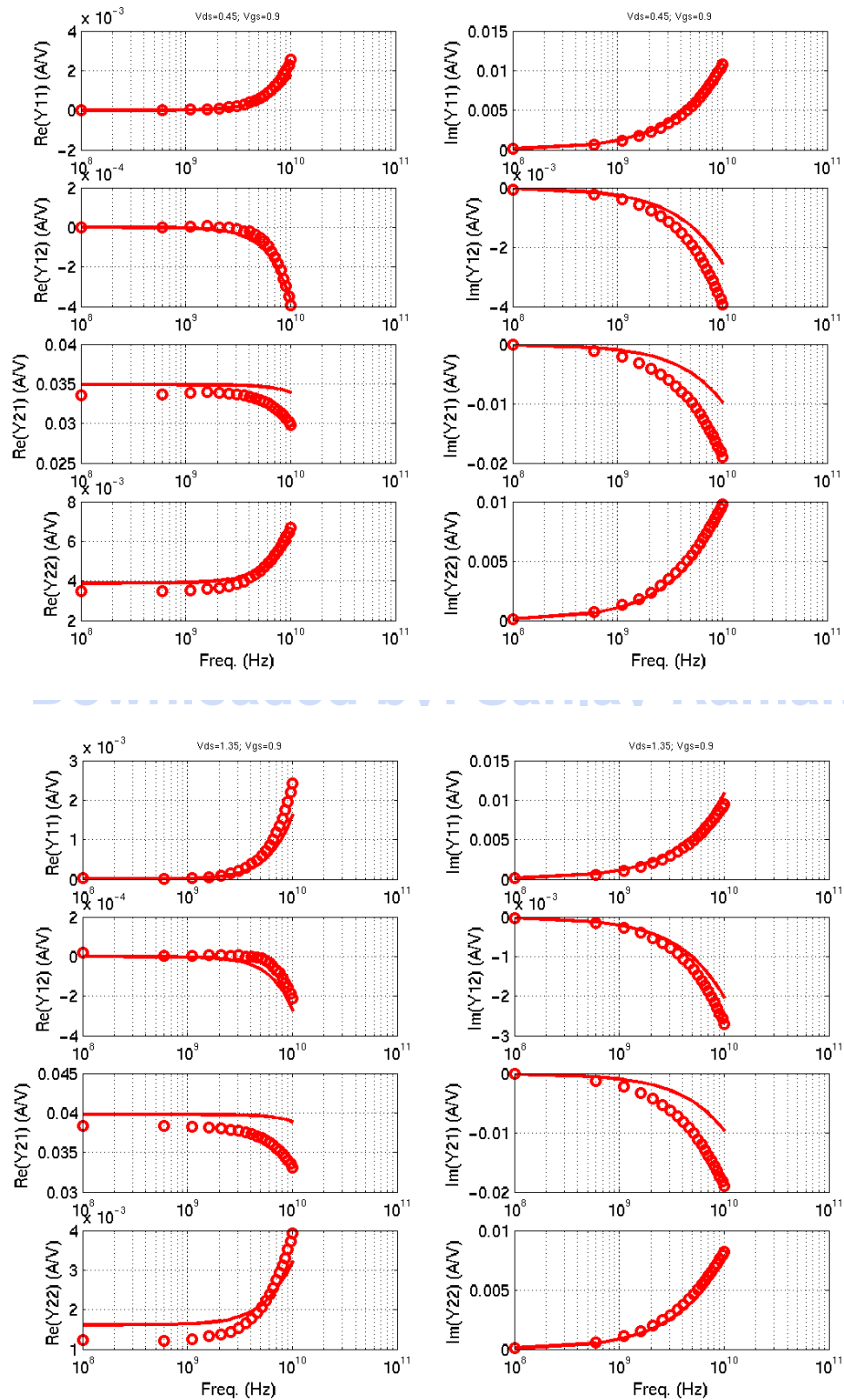


FIGURE 3.9 1p8_nfet_5x10x0p18

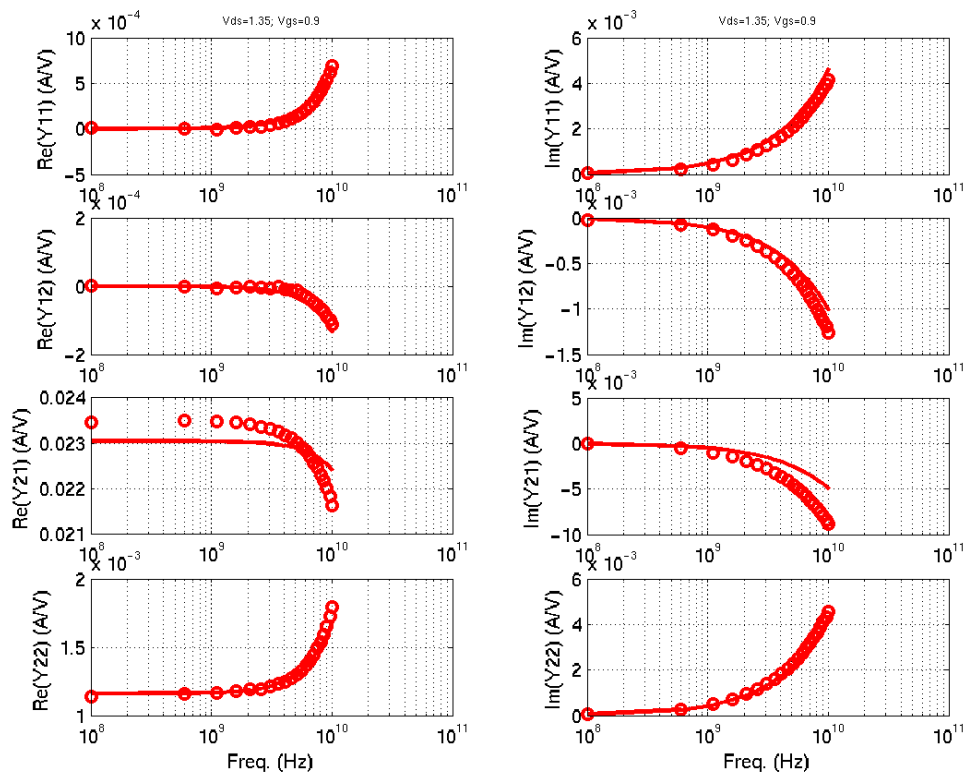
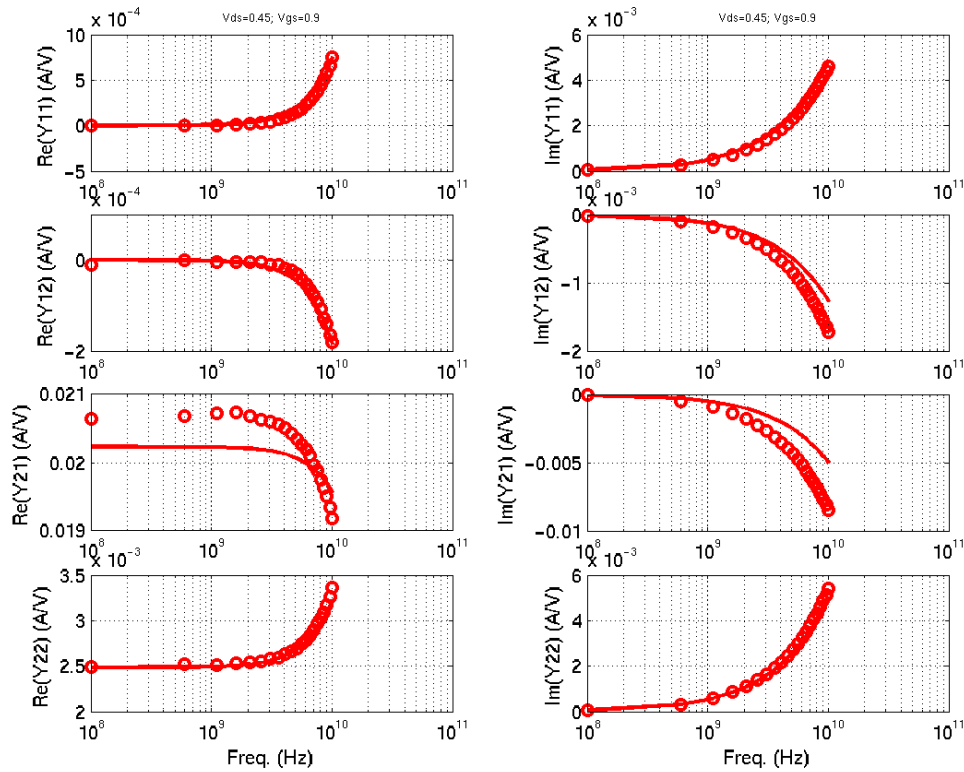


FIGURE 3.10 1p8_nfet_10x2x0p18_ftVsId_vds_1.35

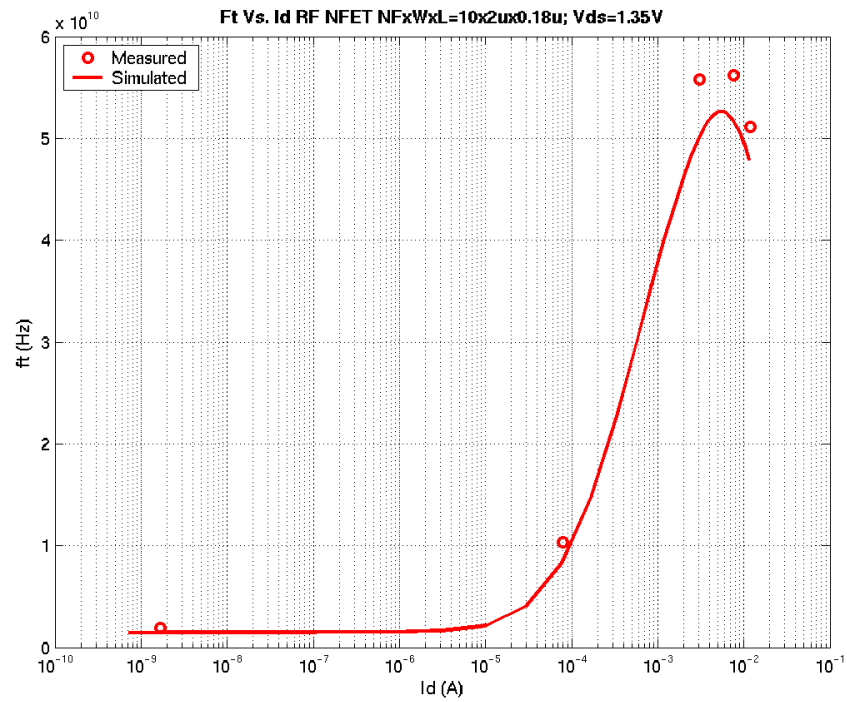


FIGURE 3.11 1p8_pfet_10x2x0p18_ftVsId_vds_-1.35

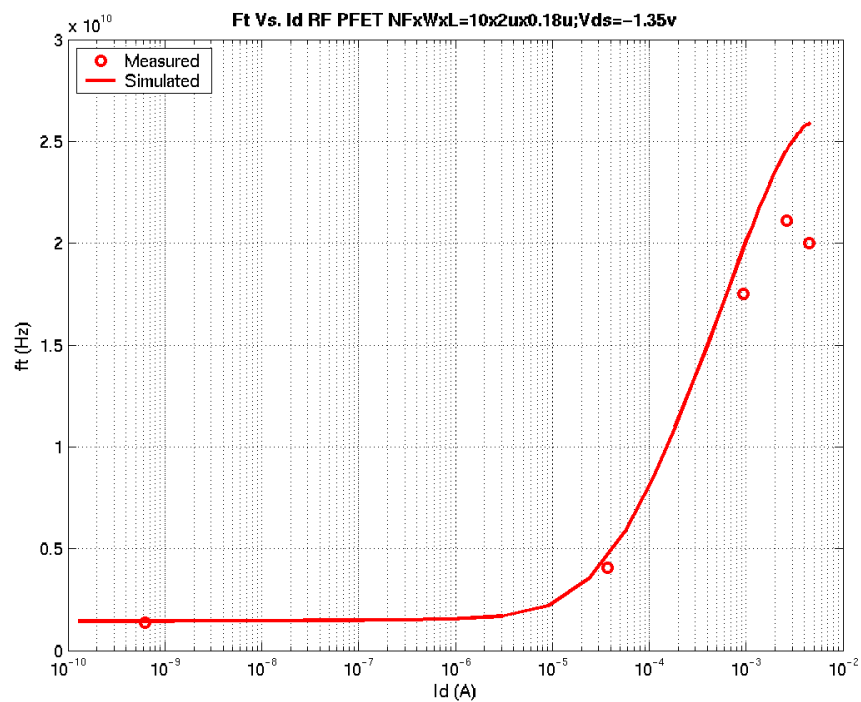


FIGURE 3.12 1p8_pfet_10x5x0p18

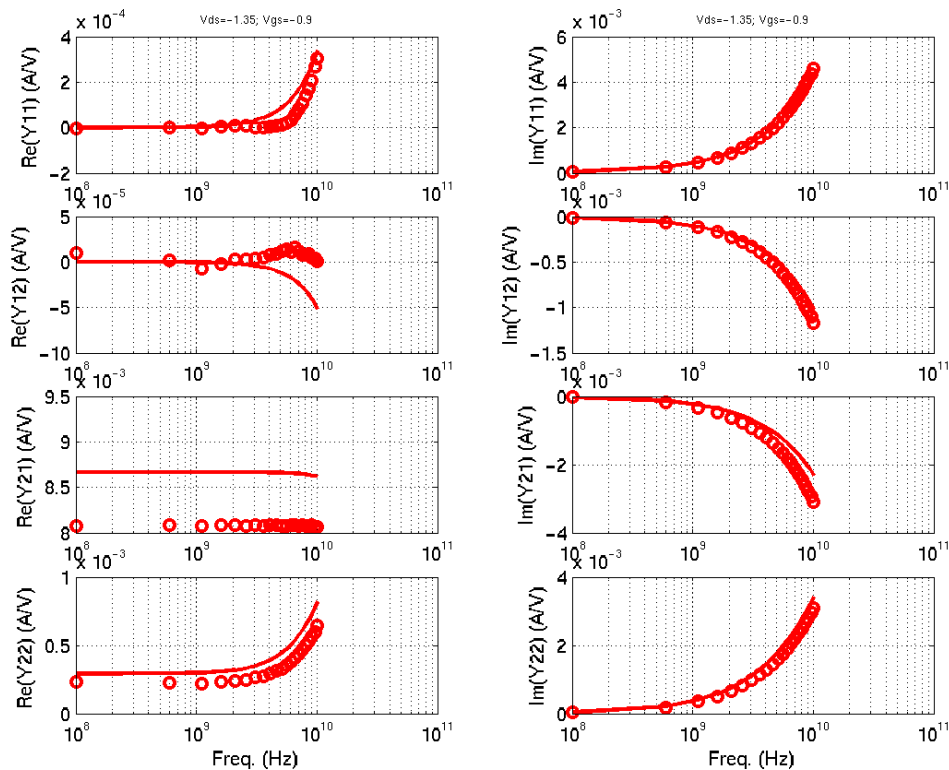
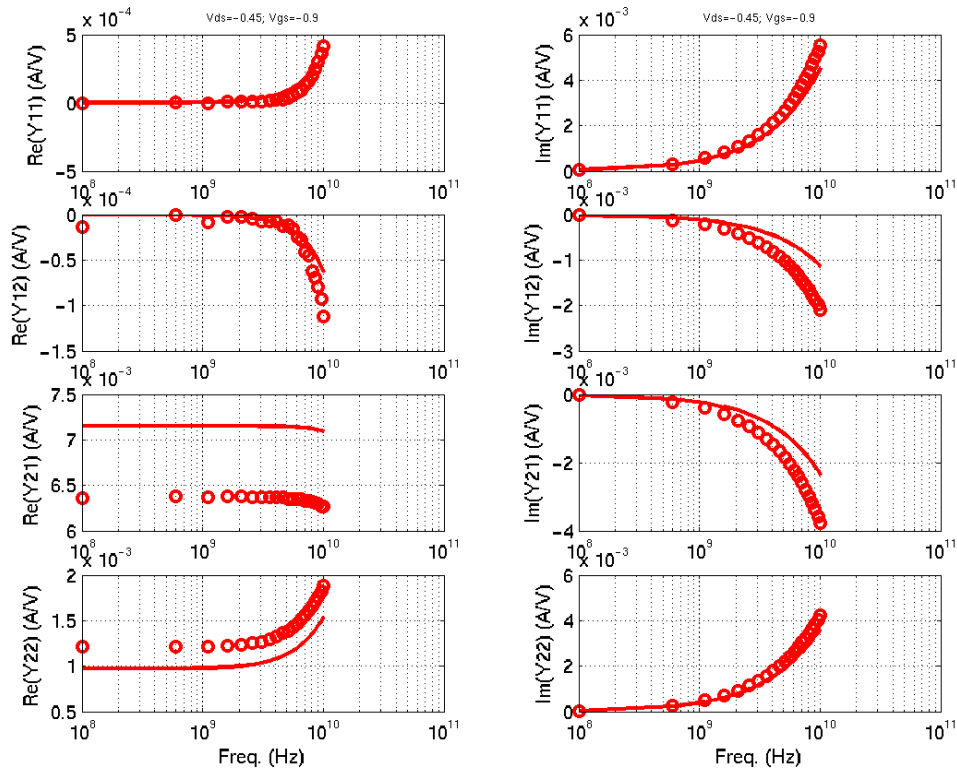


FIGURE 3.13 1p8_pfet_10x2x0p18

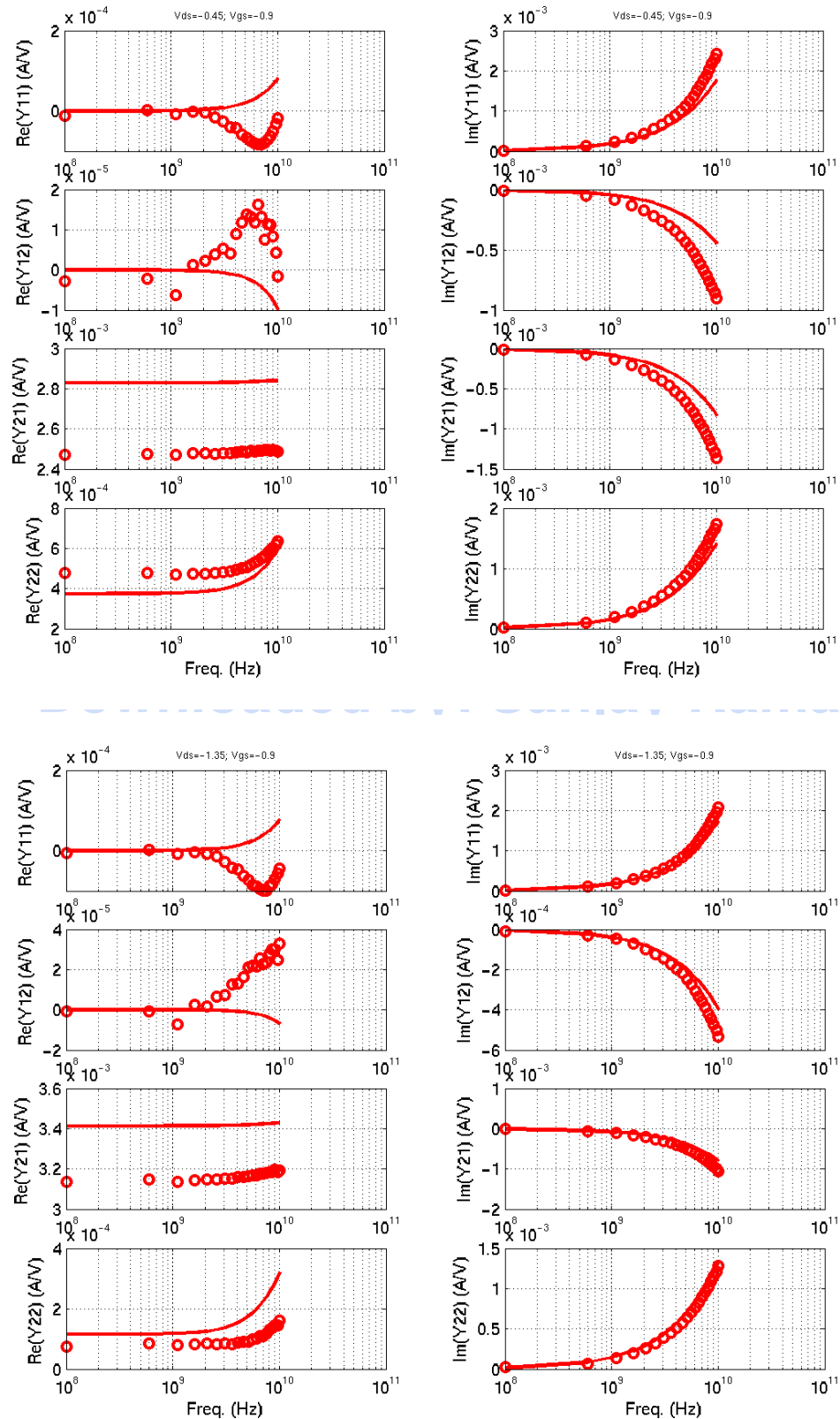


FIGURE 3.14 1p8_pfet_10x10x0p22

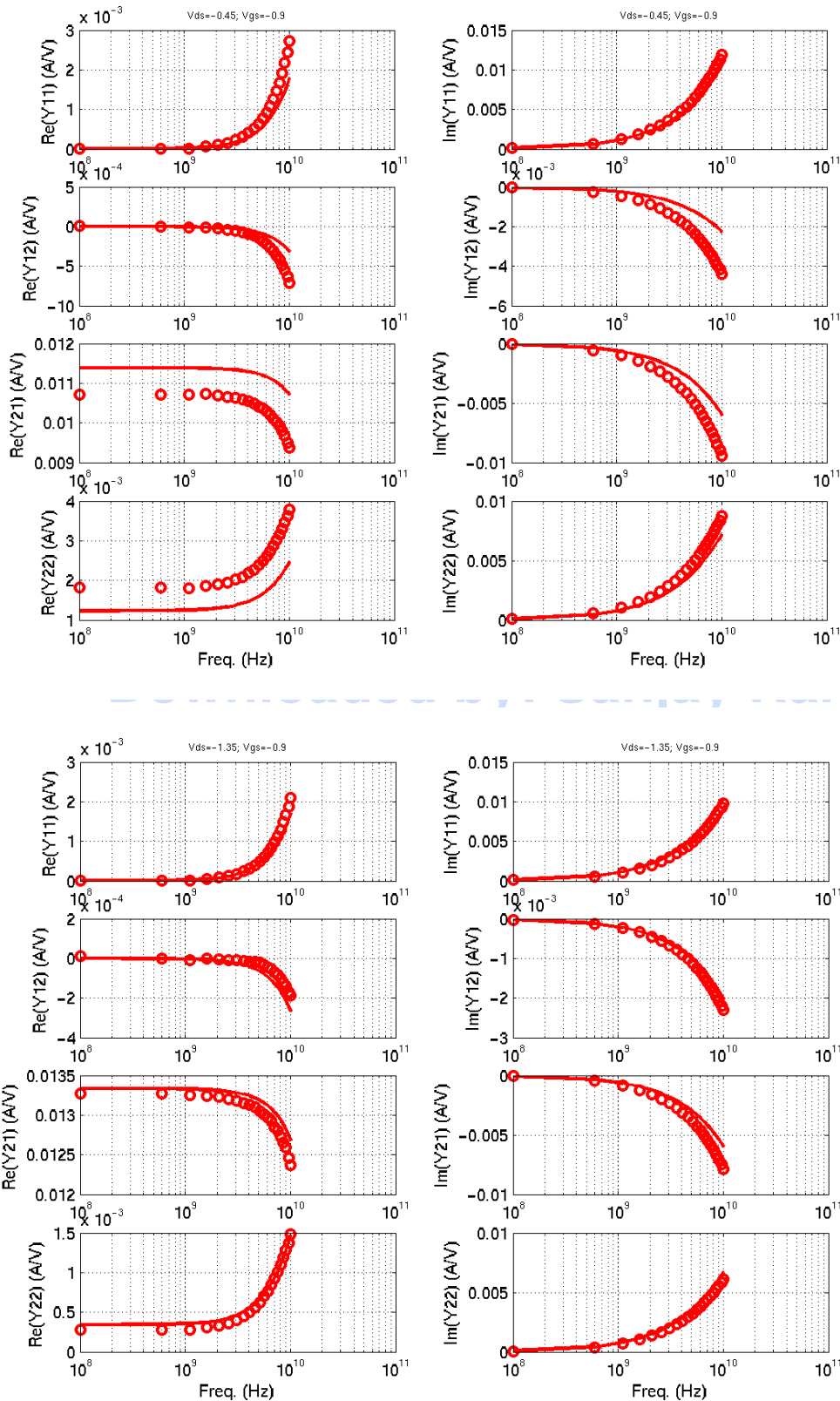


FIGURE 3.15 1p8_pfet_5x10x0p18

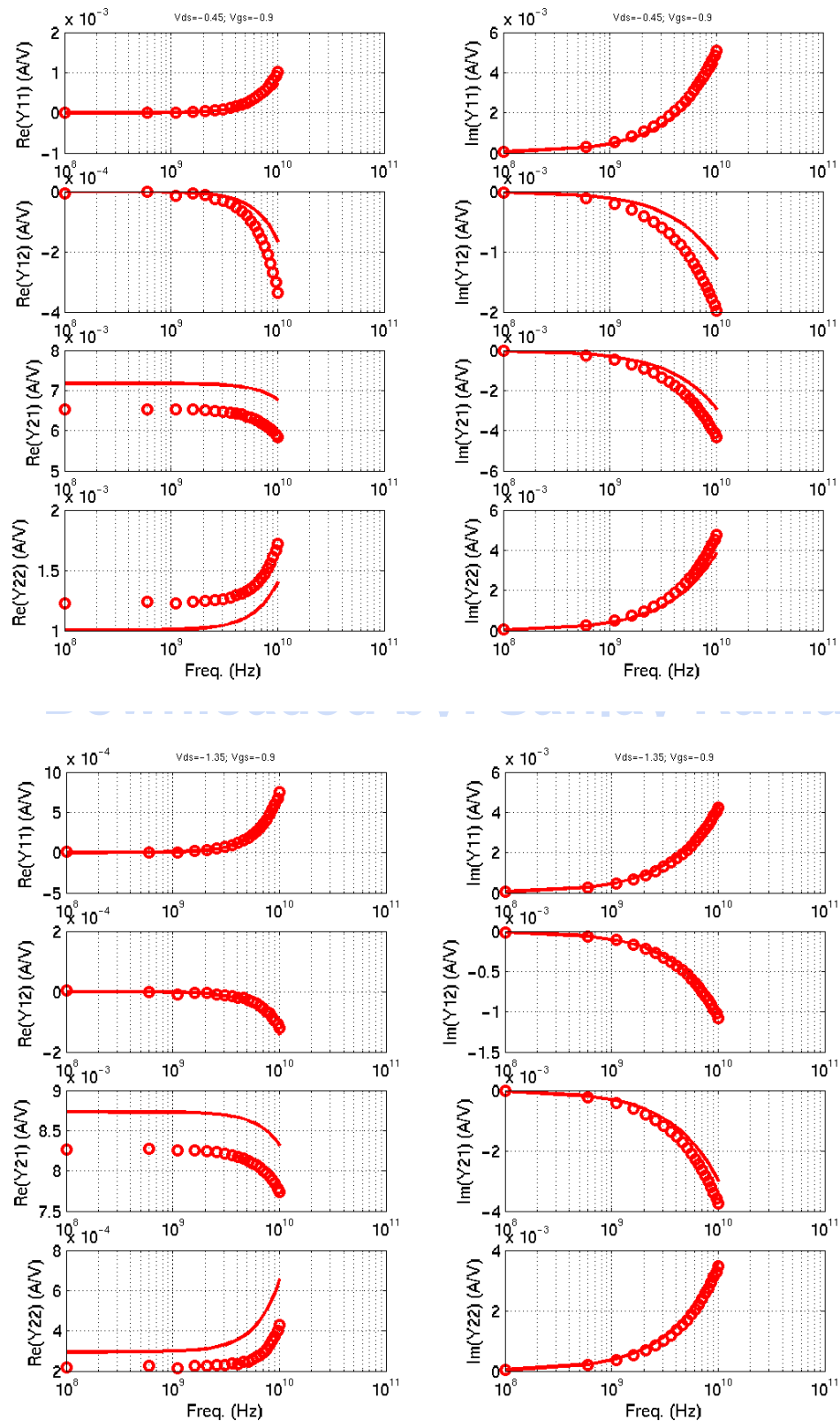


FIGURE 3.16 3p3_nfet_10x5x0p36

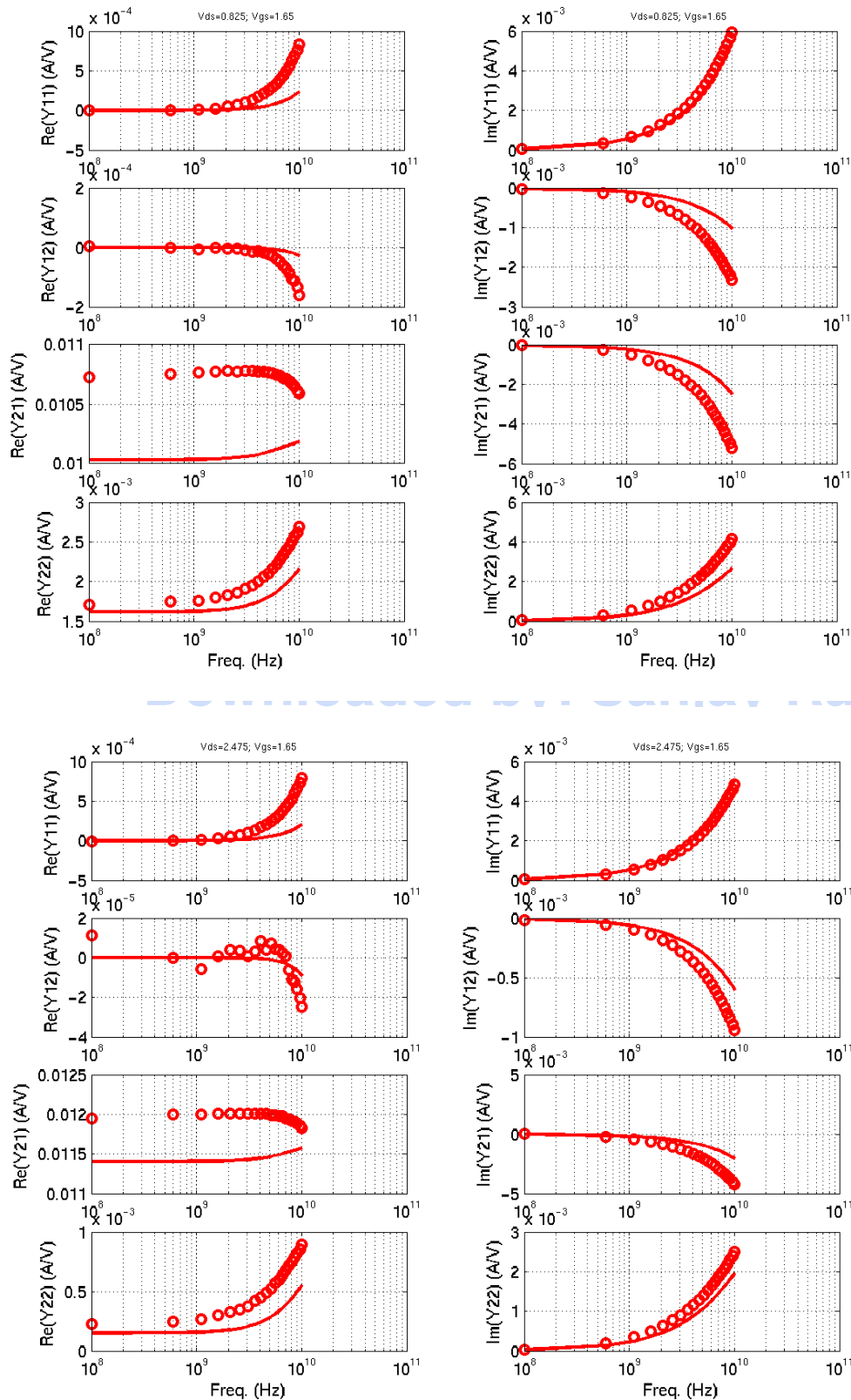


FIGURE 3.17 3p3_nfet_10x2x0p36

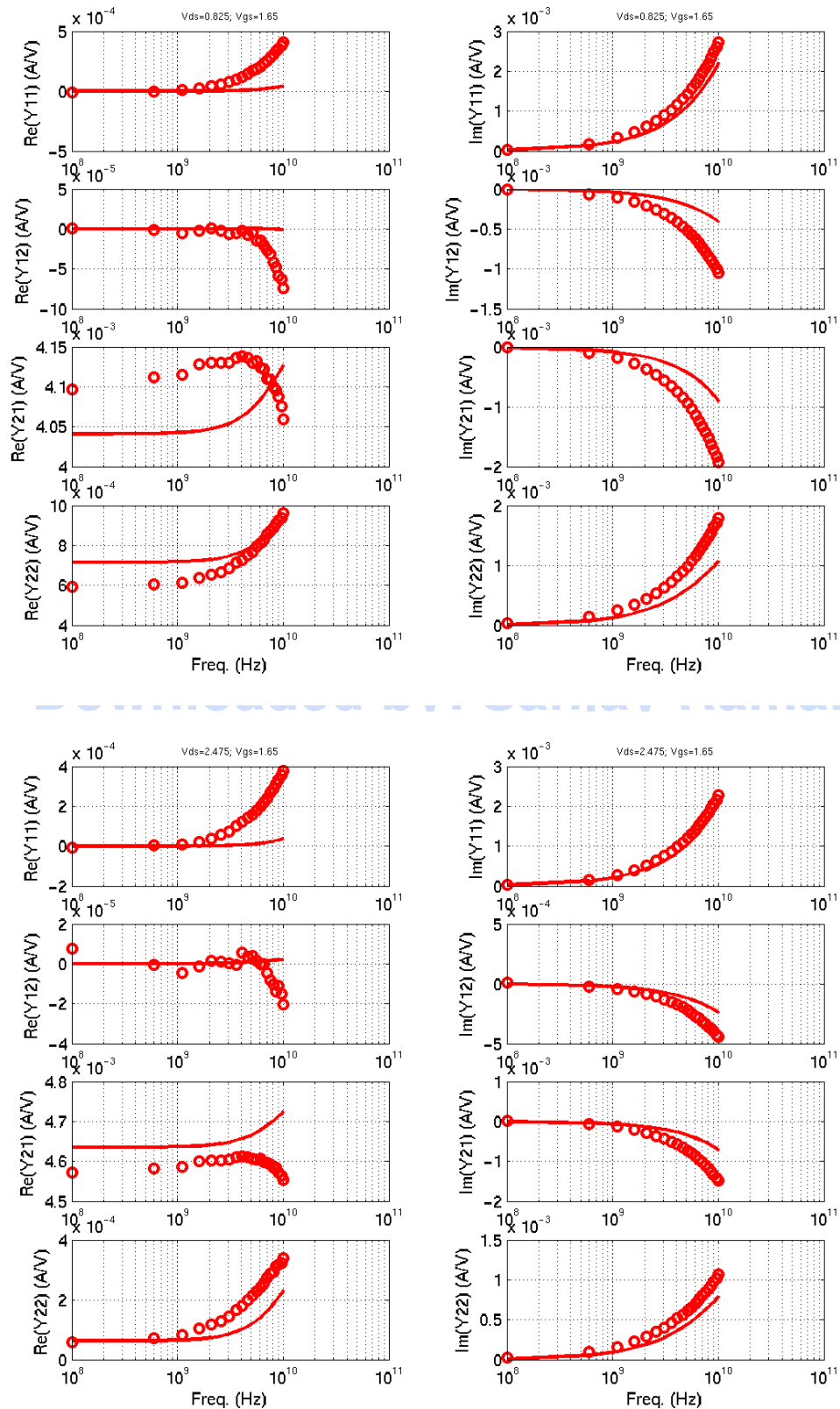


FIGURE 3.18 3p3_nfet_10x10x0p42

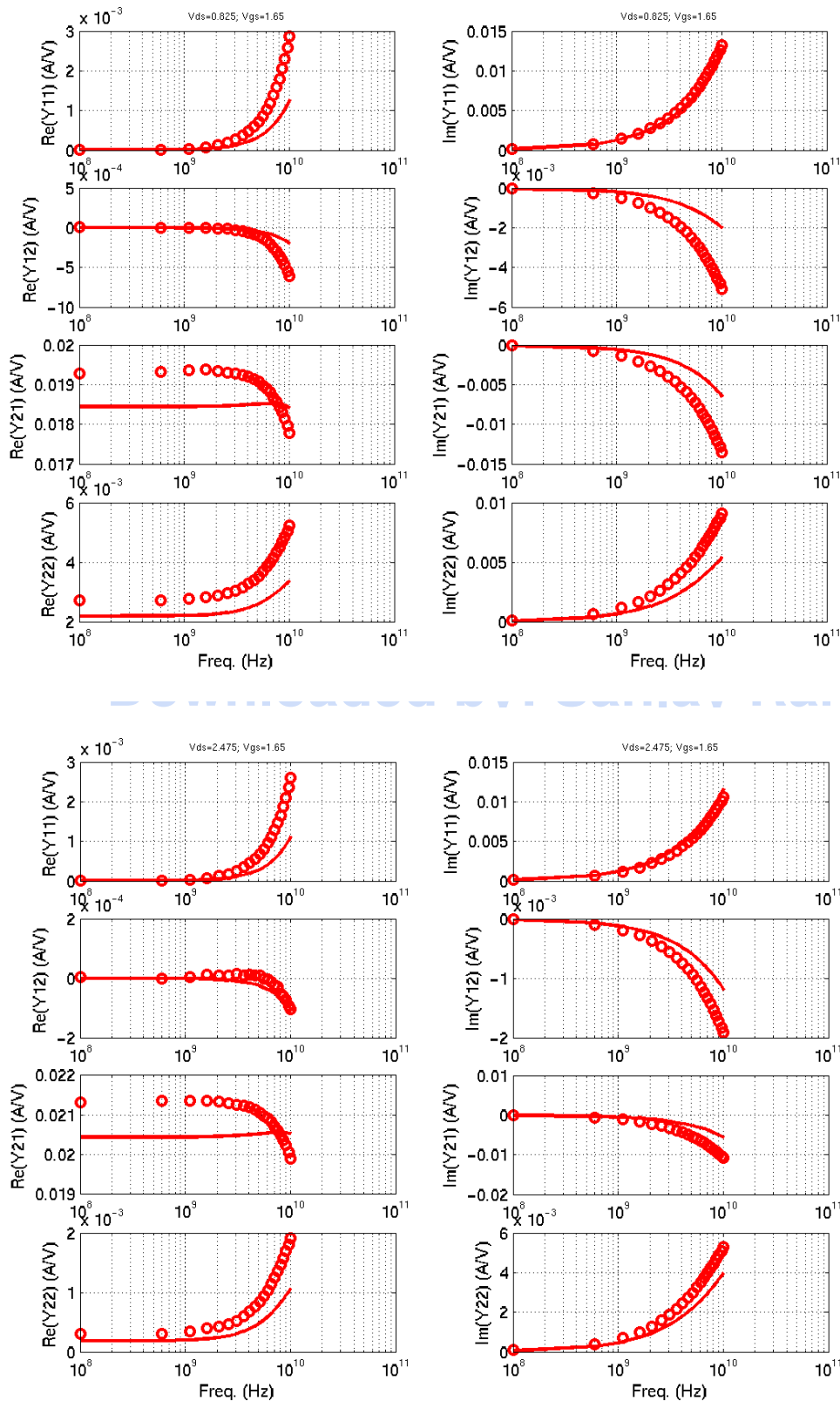


FIGURE 3.19 3p3_nfet_5x10x0p36

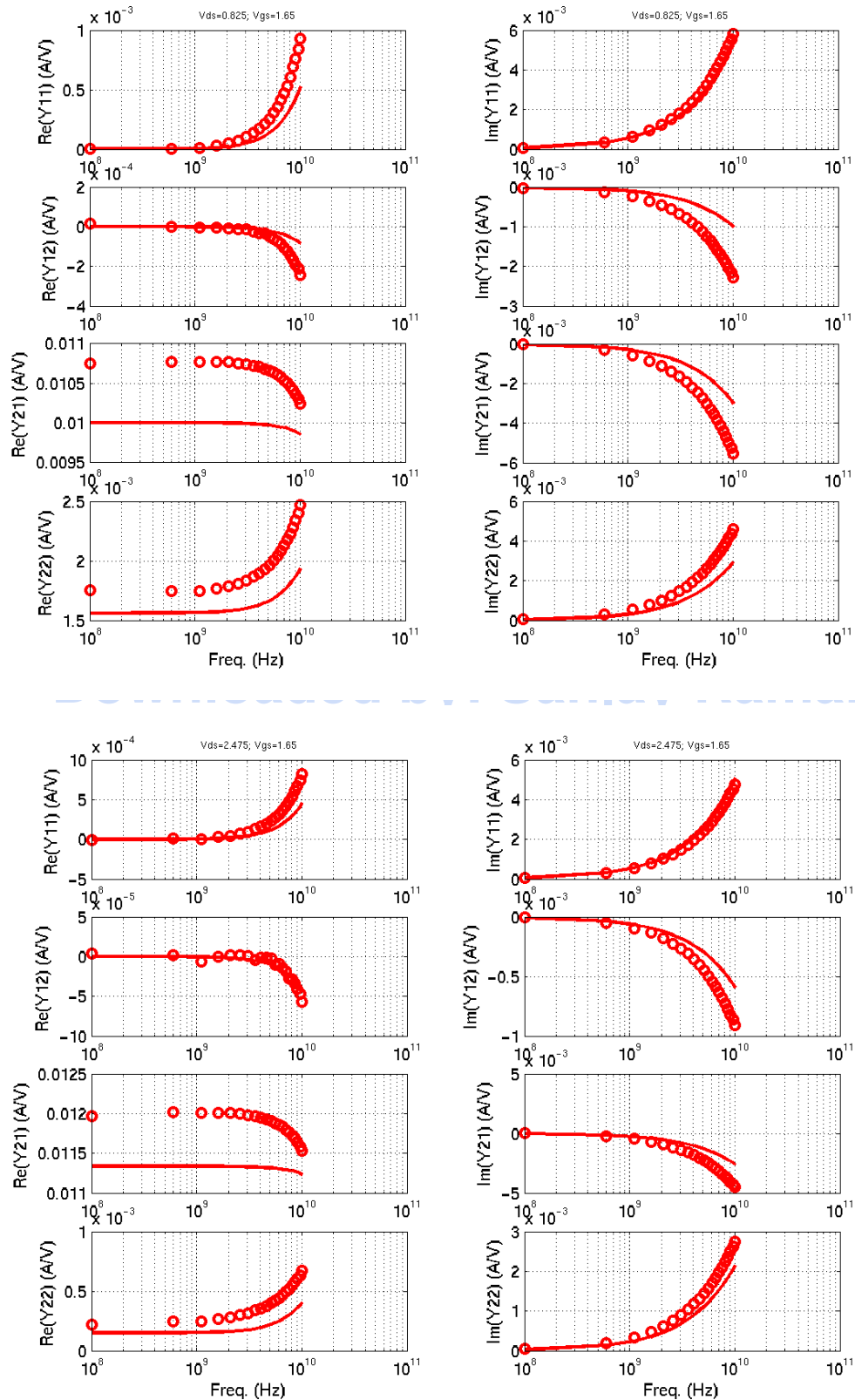


FIGURE 3.20 3p3_nfet_10x5x0p36_ftVsId_vds_2.475

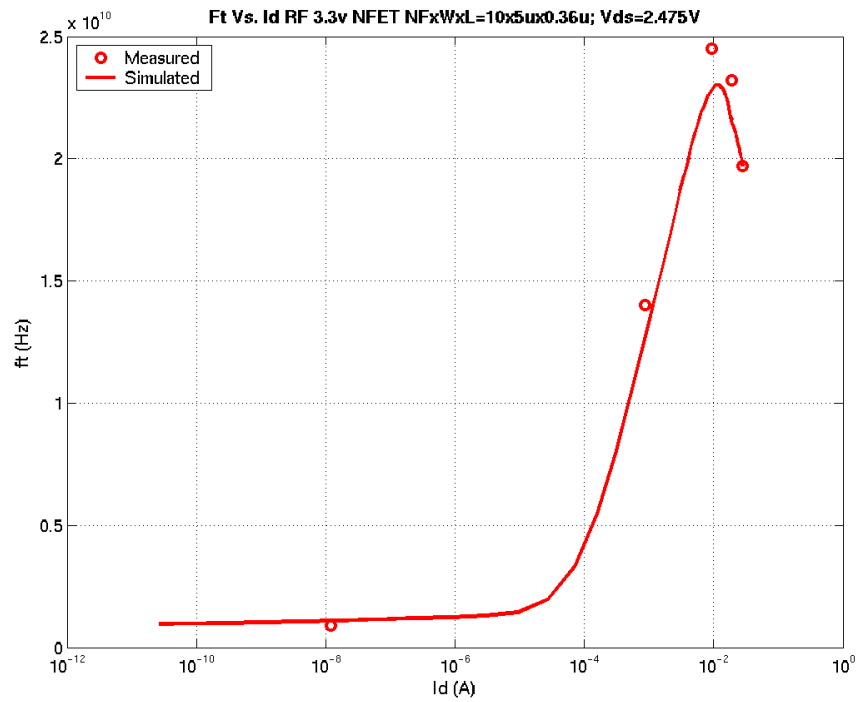


FIGURE 3.21 3p3_pfet_10x4x0p3_ftVsId_vds_-2.475

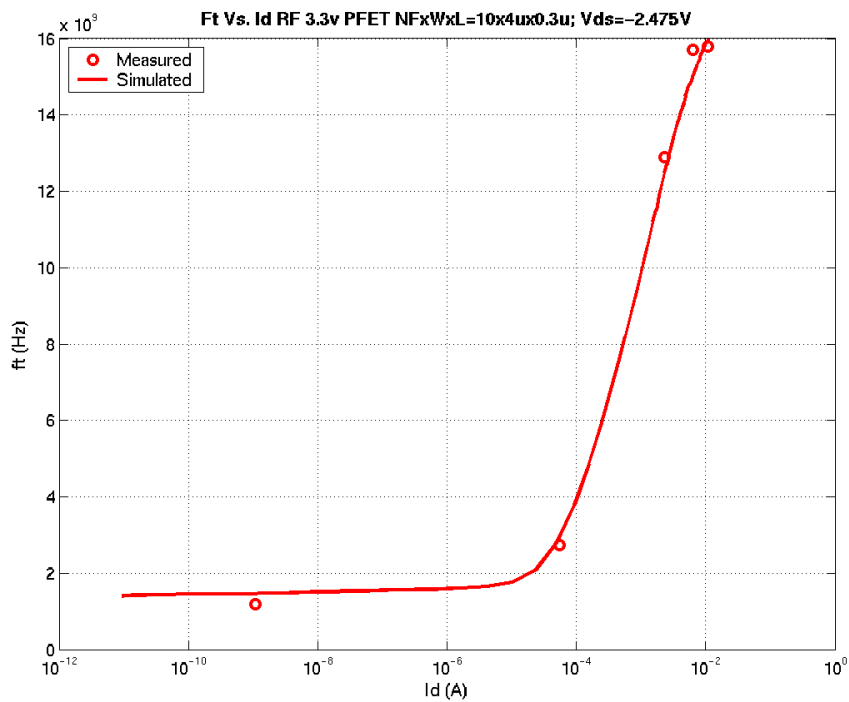


FIGURE 3.22 3p3_pfet_10x5x0p36

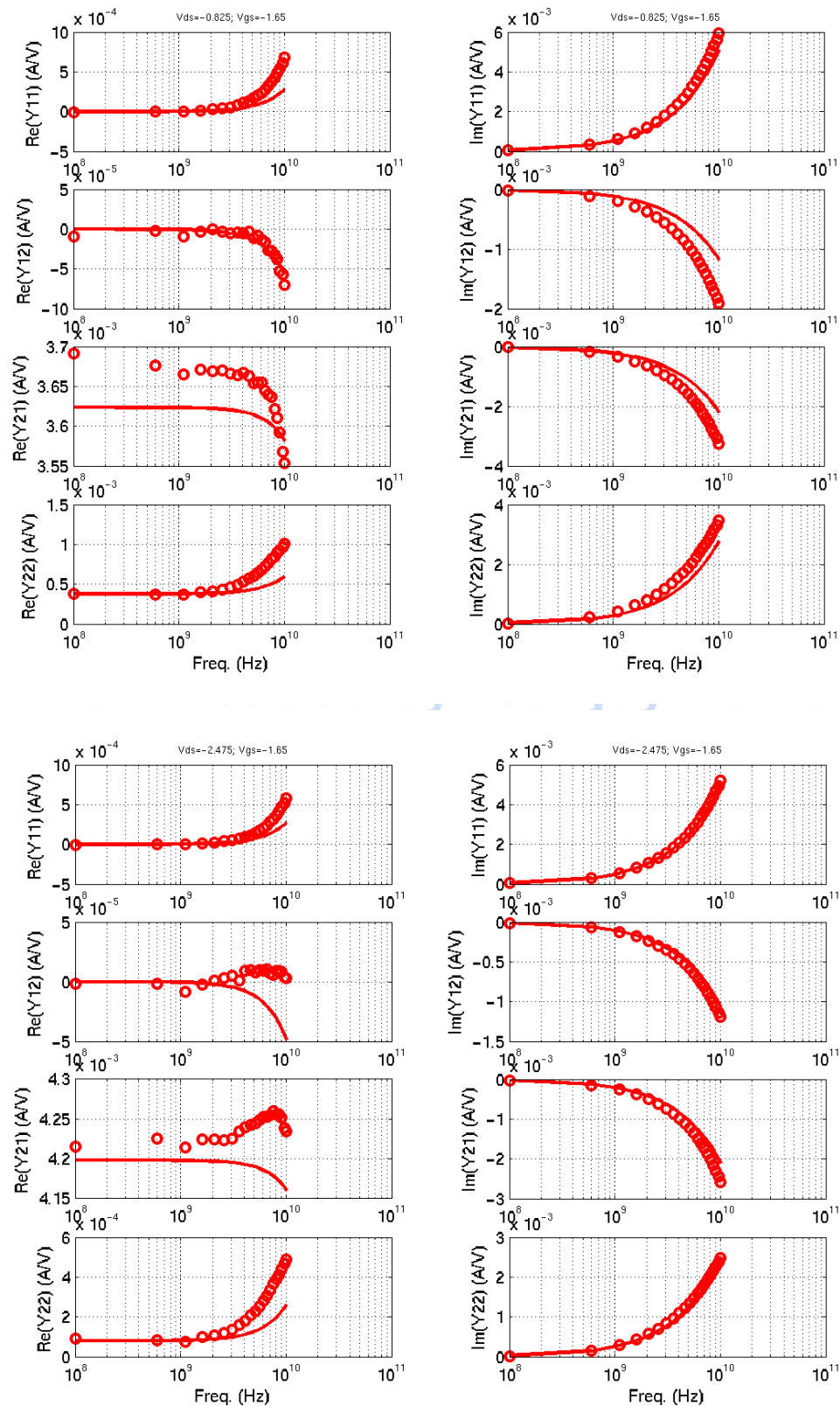


FIGURE 3.23 3p3_pfet_10x2x0p36

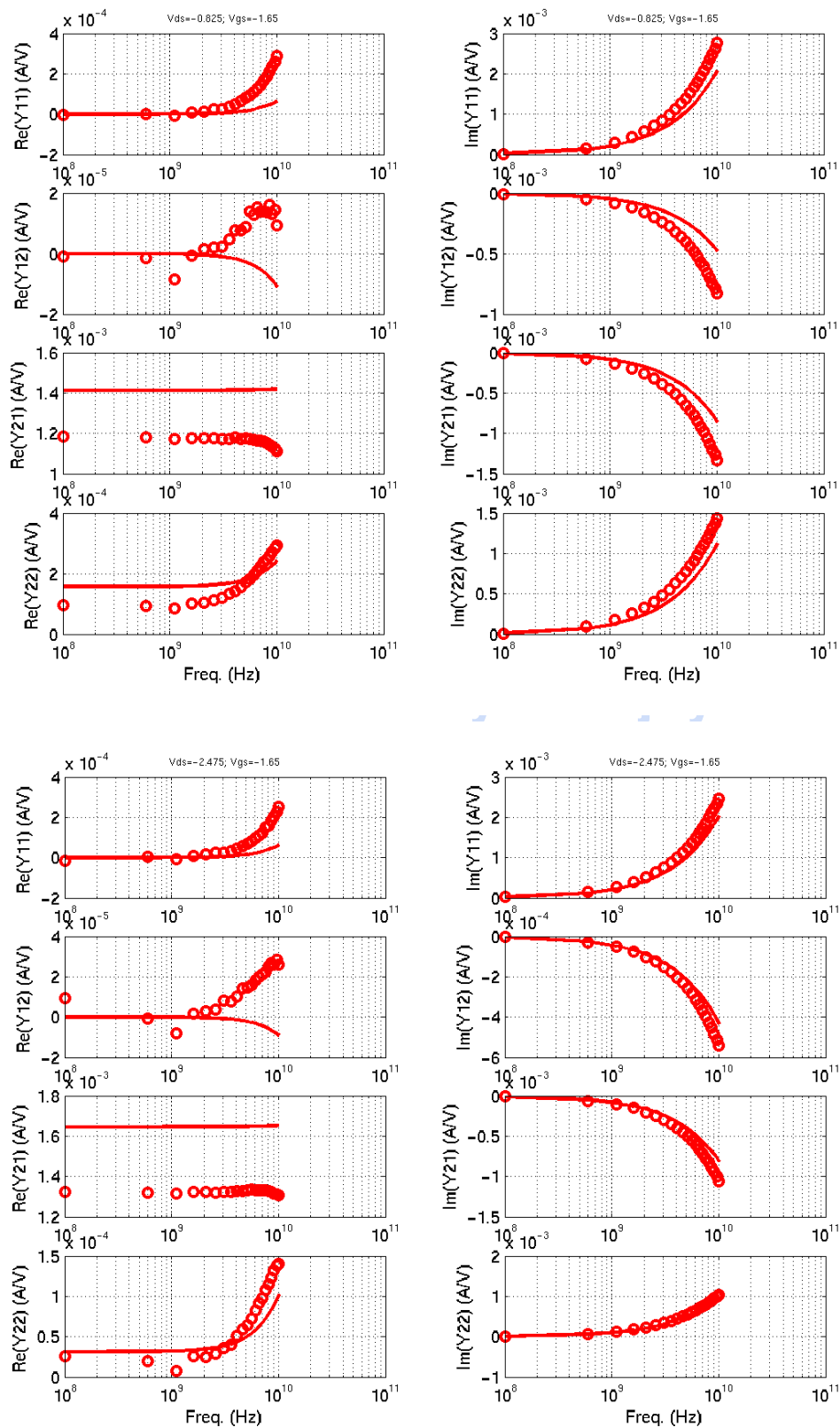


FIGURE 3.24 3p3_pfet_10x4x0p3

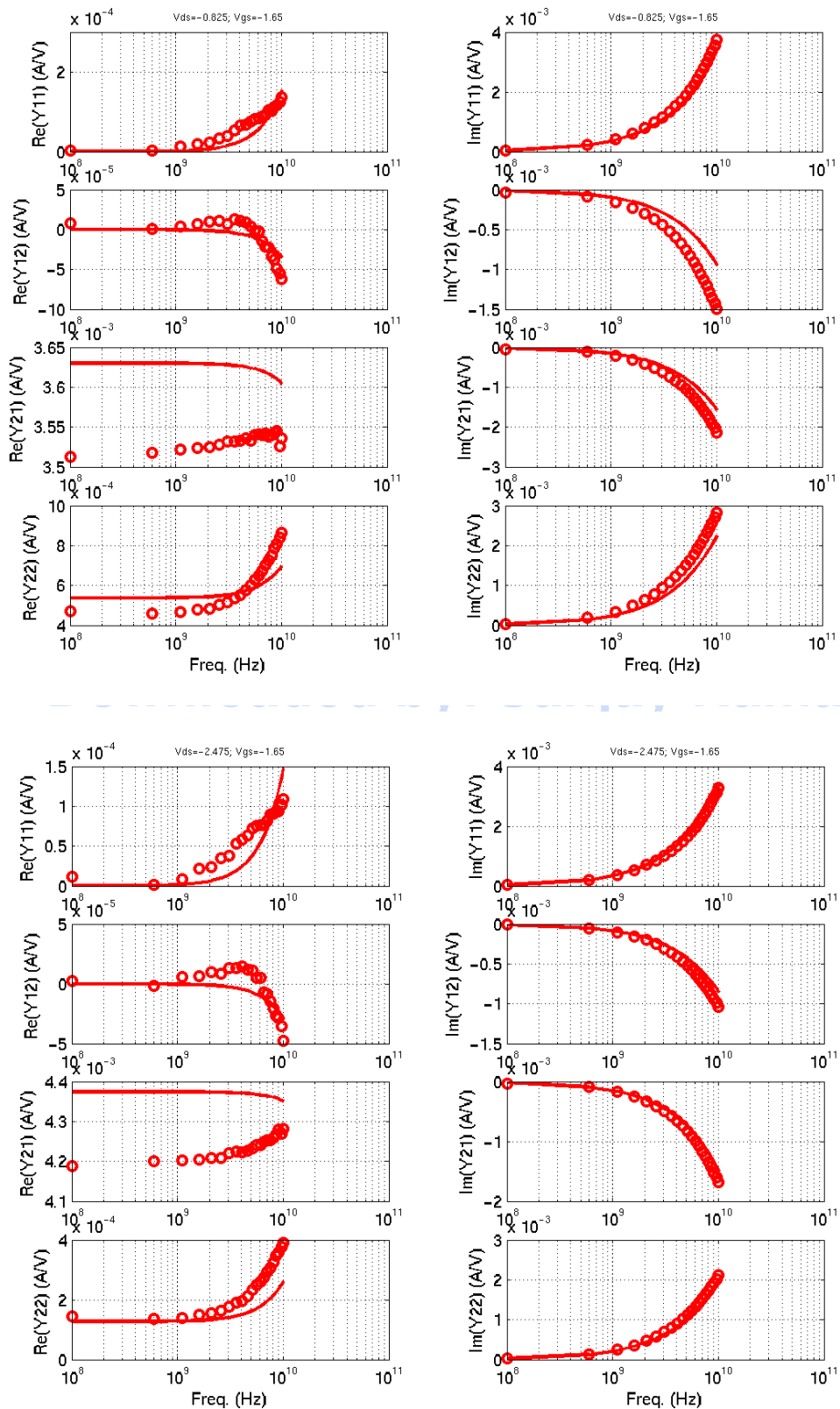
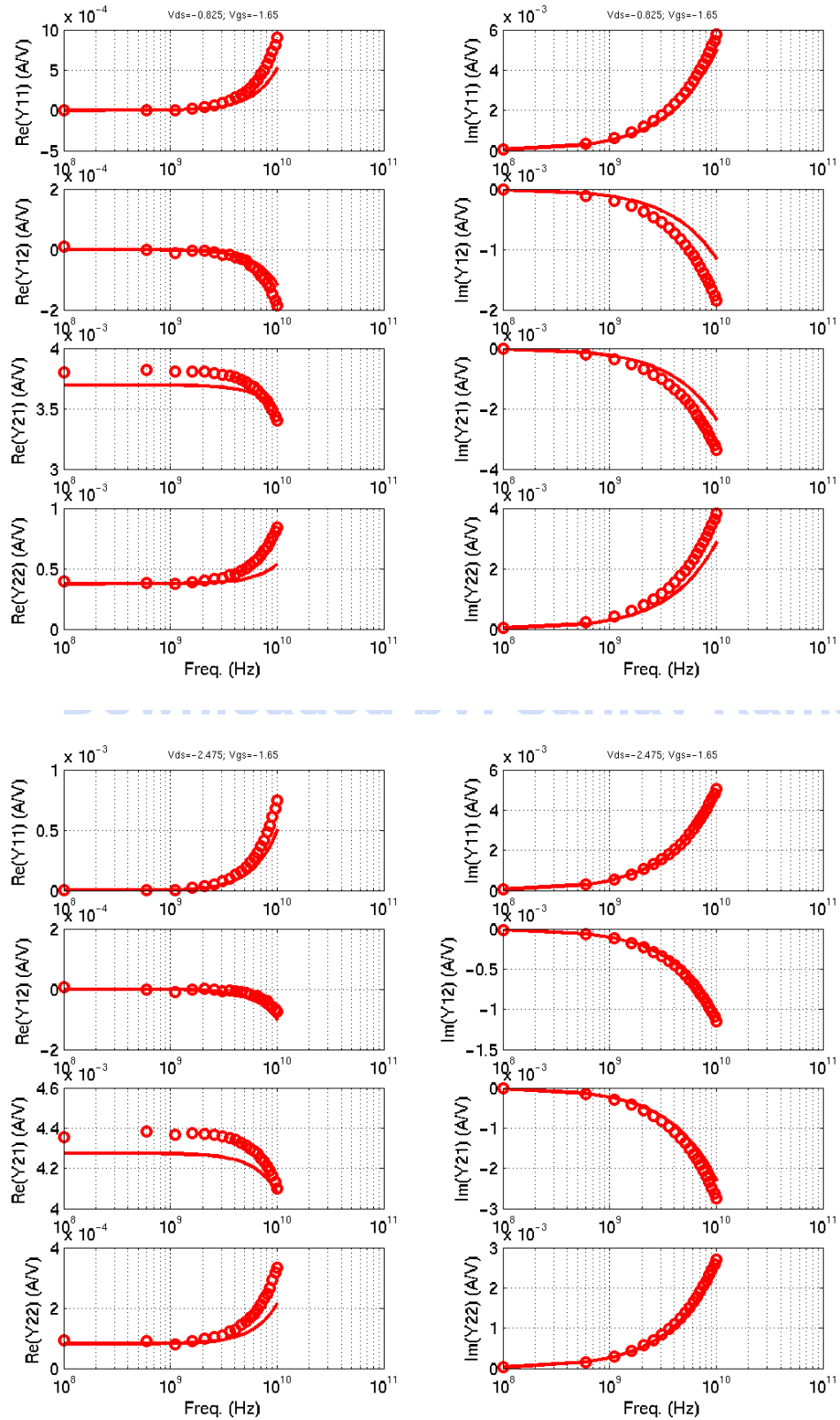


FIGURE 3.25 3p3_pfet_5x10x0p36



3.7 High frequency Noise Modeling

3.7.1 Excess thermal noise in short channel devices

Excess thermal noise, not captured by the BSIM3v3 model, has been observed in short channel devices [2]. There are 2 components to this excess noise: 1. Excess thermal noise in the channel, that manifests itself as noise in the output drain current, and 2. Channel thermal noise induced gate noise that is important at high frequencies (>2 GHz). The default BSIM3v3 model underestimates (1) for velocity saturated short channel devices and does not model (2).

3.7.2 Modeling

From v6.2 onwards, the BSIM high-frequency noise model option is not supported, even though the CDF option has not been removed. It is recommended the PSP model option (available via the Jazz Model Selection Form) be used, when accurate high-frequency noise modeling is needed.

3.8 Model Update History

3.8.1 Version 4.9

TABLE 3.4 RF model specific updates in model release version 4.9

v4.9 update	Devices	Reason	Impact on user
Noimod changed from 2 to 1	All 1.8v and 3.3v FETs	Better off-state prediction of RF thermal noise	Reduced (1/10 - 1/200x) noise for $V_g \sim 0v$. 10-20% change in the on-state ($V_g > V_t$)
Change forward biased diode IV model parameters	All 1.8v and 3.3v FETs and diodes	Corrected un-physical diode ideality factors	Better prediction of forward biased current. Possible improvement in convergence in some simulations
RF substrate network changed from II to T	1.8v RF NFET and PFET	Better fit to measured y-parameters (Y22)	Small change in Y22
RF gate resistance	1.8v RF NFET and PFET	Better fit to $Re(Y_{11})$	Reduced R_{gate} - impact on $Re(Y_{11})$ and gate noise

3.8.2 Version 5.0

TABLE 3.5 RF FET model specific updates in model release version 5.0

v5.0 update	Devices	Reason	Impact on user
Corner/Statistical model oxide thicknesses	All 1.8v and 3.3v RF FETs	Updated to match new E-spec. with tighter variation	No change in NOMINAL model. Reduced corner/statistical model variation in gate oxide capacitance: 1.8v FETs corner model: v4.9 +/- 1Å; v5.0 +/- 1Å 1.8v FETs stat. model: v4.9 +/- 3Å; v5.0 +/- 1.5Å 3.3v FETs corner model: v4.9 +/- 2Å; v5.0 +/- 1.8Å 3.3v FETs stat. model: v4.9 +/- 6Å; v5.0 +/- 3Å
Corner and stat. parameters added to model process variation on drain/source series resistance	All 1.8v and 3.3v RF FETs	More physical corner and statistical models	No change in NOMINAL model. Larger gm variation in corner and statistical models for short channel FETs
Corner and stat. parameters added to model process variation on gate-source and gate-drain overlap capacitances	All 1.8v and 3.3v RF FETs	Corner and statistical models for overlap capacitance in v4.9 did not capture oxide thickness and ΔL variation	No change in NOMINAL model. Larger gate-source and gate-drain overlap capacitance variation in corner and statistical models
Statistical correlation added to FASTSLOW and SLOW-FAST corners	All 1.8v and 3.3v RF FETs	Improved correlation matching between N and PFETs	Reduced oxide thickness, ΔL, and ΔW variation when simulating with the FASTSLOW and SLOW-FAST corners
RF substrate network changed from II to T	3.3v RF NFET and PFET	Better fit to measured y-parameters (Y22). Both 2-sided and 4-sided ("ringed") substrate contacts are now supported for all 1.8v and 3.3v RF FETs	Small change in Y22
Added silicide-polysilicon contact resistance to the gate resistance	All 1.8v and 3.3v RF FETs	Silicide-polysilicon gate resistance is a significant component of gate resistance for narrow width (<3μm) RF FETs with 2-sided gate contacts	Increased gate resistance seen in Re(Y11), especially for narrow FETs (W<3μm) with 2-sided gate contact layouts

3.8.3 Version 6.0

TABLE 3.6 RF FET model specific updates in model release version 6.0

v6.0 update	Devices	Reason	Impact on user
X-Sigma corner model support	All RF FETs	Allow for process variation settings different than conventional +/- 3 sigma corner models	Added flexibility in corner simulation
Fixed junction capacitance partitioning between area and perimeter	All 1.8v and 3.3v RF FETs	Previous versions used an empirical fit. New partitioning scheme aligns RF and MS model	Minimal change in total junction capacitance
Switch to unified BSIM3 flicker noise model	All 1.8v and 3.3v RF FETs	More accurate modeling of flicker noise bias dependence	Change from gm based model which over predicted noise at low Vgs. Noise sensitive circuits at low Vgs should match silicon better.
High-frequency noise modeling	1.8v RF NFET	Model excess noise for short channel devices, not covered by BSIM3 thermal noise model	More accurate noise when HF Noise option selected
Add "multiplicity" to mismatch model	All FETs	Mismatch should improve with multiple devices	Correct modeling of transistor mismatch for m>1

3.8.4 Version 6.2

TABLE 3.7 RF FET model specific updates in model release version 6.2

v6.2 update	Devices	Reason	Impact on user
Re-centered FET models to new E-specs	All FETs	Refects most recent Fab data	For more information, please see Section 2.10 in the "MOS MODEL" chapter.
Updated substrate resistance	All RF FETs	More accurate model to hardware correlation.	Minor change in substrate resistance.

3.8.5 Version 6.3

TABLE 3.8 Mixed-signal model specific updates in model release version 6.3

v6.3 update	Devices	Reason	Impact on user
Re-formatted models to align with "GTE" formatted Cadence PDKs. Schematic and post-layout instance names are now the same	All RF CMOS FETs	Added ability to simulate mismatch in post-layout simulations	No impact if using models via Cadence PDK. Capability to simulate mismatch in post-layout views.

3.9 References

1. Steve Hung-Min Jen, Christian C. Enz, David R. Pehlke, Michael Schroter, and Bing J. Sheu, "Accurate Modeling and Parameter Extraction for MOS Transistors Valid up to 10 GHz," IEEE Trans. on Elec. Dev., Vol. 46, No. 11, November 1999.
2. Chih-Hung Chen, M. Jamal Deen, Yuhua Cheng, and Mishel Matloubian, "Extraction of the Induced Gate Noise, Channel Noise, and Their Correlation in Submicron MOSFETs from RF Noise Measurements," IEEE Trans. on Elec. Dev., Vol. 48, No. 12, December 2001.

4.0 SiGe Bipolar Model

4.1 Device Description

The SBC18 process offers 3 NPN device types, digital (high speed), low voltage (standard) and high voltage, differentiated by BV_{CEO} and F_t targets listed in Table 4.1. The digital device is only available in select variants (e.g. SBC18HX, SBC18HXL, SBC18HA, SBC18QTE). A cross section of a digital or low voltage NPN device is shown in Figure 4.1, where the differentiating factor between the device types is the collector implant. The high voltage device by contrast does not receive a collector implant, and its cross section is shown in Figure 4.2. The layout of an NPN with a 1 emitter, 2 base, 1 collector configuration is shown in Figure 4.3. Layout configurations are further described in Section 4.2.

TABLE 4.1 SBC18 NPN Specification by BV_{CEO} (when V_{bc} is 1 Volt) and F_t

NPN	BV_{CEO} (V)	F_t (GHz)	Design Kit Name	Model Name
low voltage	2.2	155	nnp	ln[1,2][1,2,3][1,2]_hicum
medium voltage	3.5	78	nnp	m[n,m,w][1,2,3,4][1,2,3,4,5][1,2]_hicum
high voltage	6 or 8	38 or 30	nnp	[h,p][n,m,w][1,2,3,4][1,2,3,4,5][1,2]_hicum

FIGURE 4.1 Cross Section of a digital or low voltage NPN

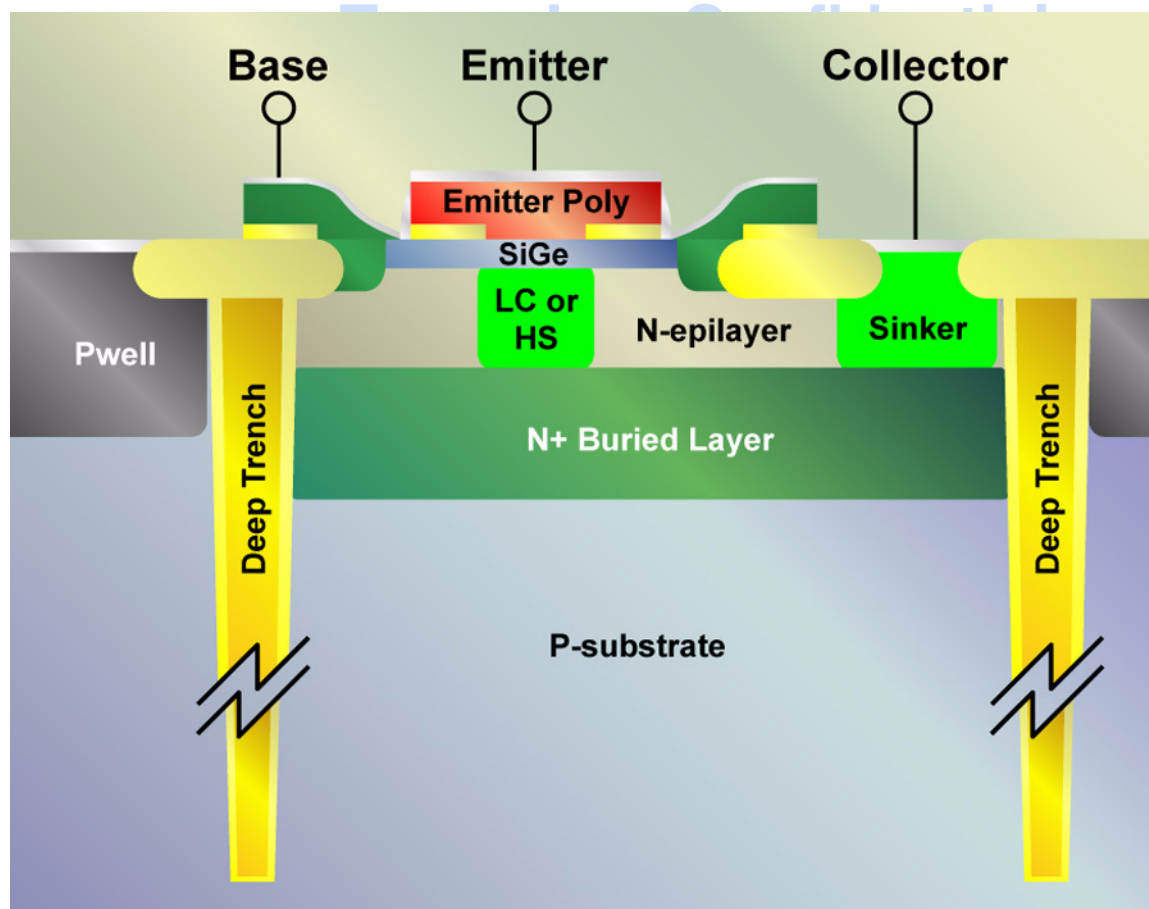


FIGURE 4.2 Cross Section of high voltage NPN

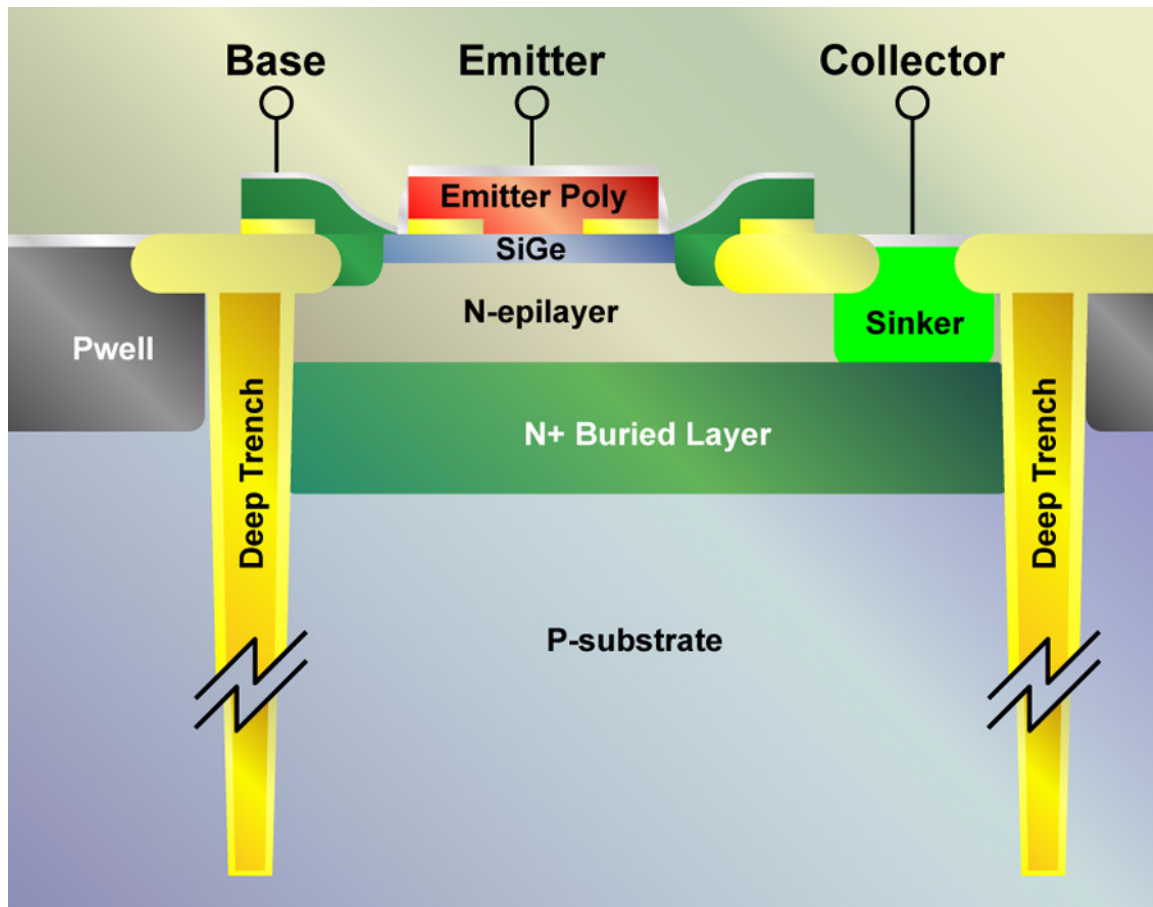
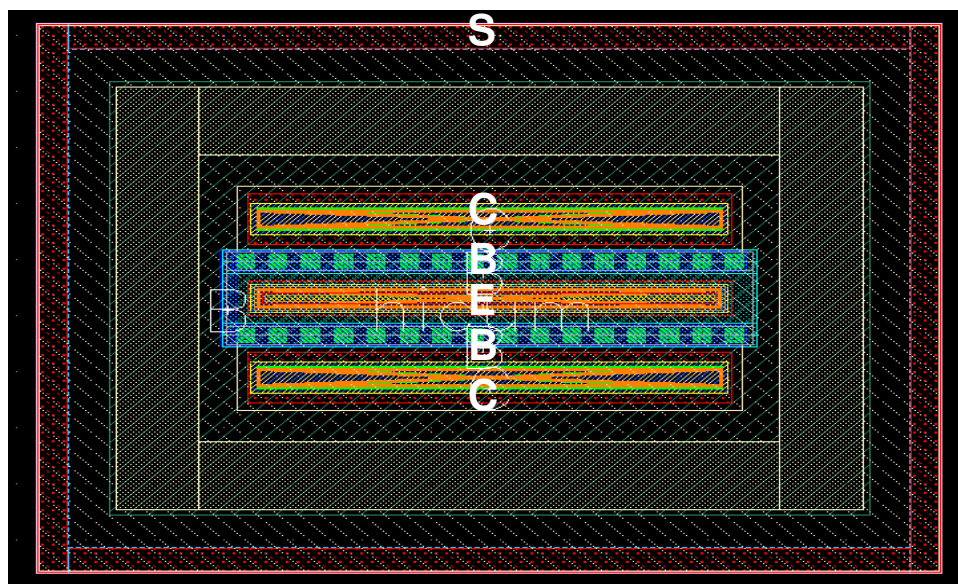


FIGURE 4.3 Layout of NPN: 1 Emitter, 2 Base, and 2 Collector configuration



4.2 Naming Convention and list of NPNs offered

Table 4.2 provides a detailed description of the NPN configurations and parameter ranges.

Emitters Lengths: Scalable, see Table 4.2 for length range.

Emitters Widths: Three different emitter widths (0.2, 0.6, and 0.9um) are supported.

Multiple device instances vs. multiple emitter fingers: use of multiple emitter fingers instead of multiple device instances generally results in more efficient footprint and lower parasitic capacitance. The trade-off is collector resistance.

TABLE 4.2 SBC18 NPN Configurations

Configuration	Device Type: l=low voltage m=medium voltage	Emitter Width n=0.2; m=0.6; w=0.9um	Emitter Length (μm)	No. of Emitters	No. of Bases	No. of Collectors
121	l, m, h	n, m, w	0.76-10.16	1	2	1
122	l, m, h	n, m, w	0.76-10.16	1	2	2
232	l, m, h	n, m, w	0.76-10.16	2	3	2
342	l, m, h	n, m, w	0.76-10.16	3	4	2
452	l, m, h	n, m, w	0.76-10.16	4	5	2

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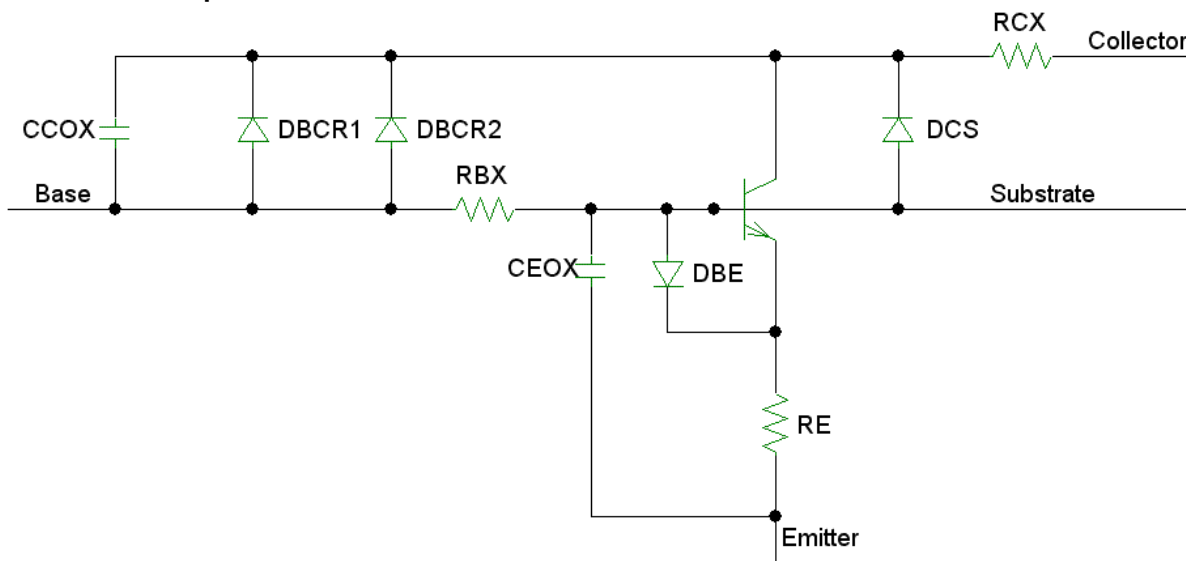
4.3 Model Description

Separate Spice Gummel Poon Model (SGPM) and HICUM models are generated for the various combinations of emitter width and finger combinations mentioned in Table 4.2. The emitter length can be varied within the grid spacing and within the boundaries listed in Table 4.2. Separate models are extracted for the various combinations of emitter width and finger configuration described in Table 4.2.

4.3.1 Spice Gummel Poon Model

SGPM is the most well known, stable and robust bipolar transistor model. The SGPM is readily available in all commercial simulators. However, several physical effects of modern day NPNs are not included in the model. Thus, a sub-circuit based SGPM is provided to improve the modeling accuracy and capture the transistor's scalability. The sub-circuit diagram is shown in Figure 4.4. The SGPM is intended to be accurate at the low current and high V_{bc} region. **Additionally, the SGPM has poor models (no models in some cases) for f_T voltage dependence, f_T roll off at high current, beta roll off at the high correct current, Base-Collector breakdown, Base-Emitter tunneling current, and self-heating.**

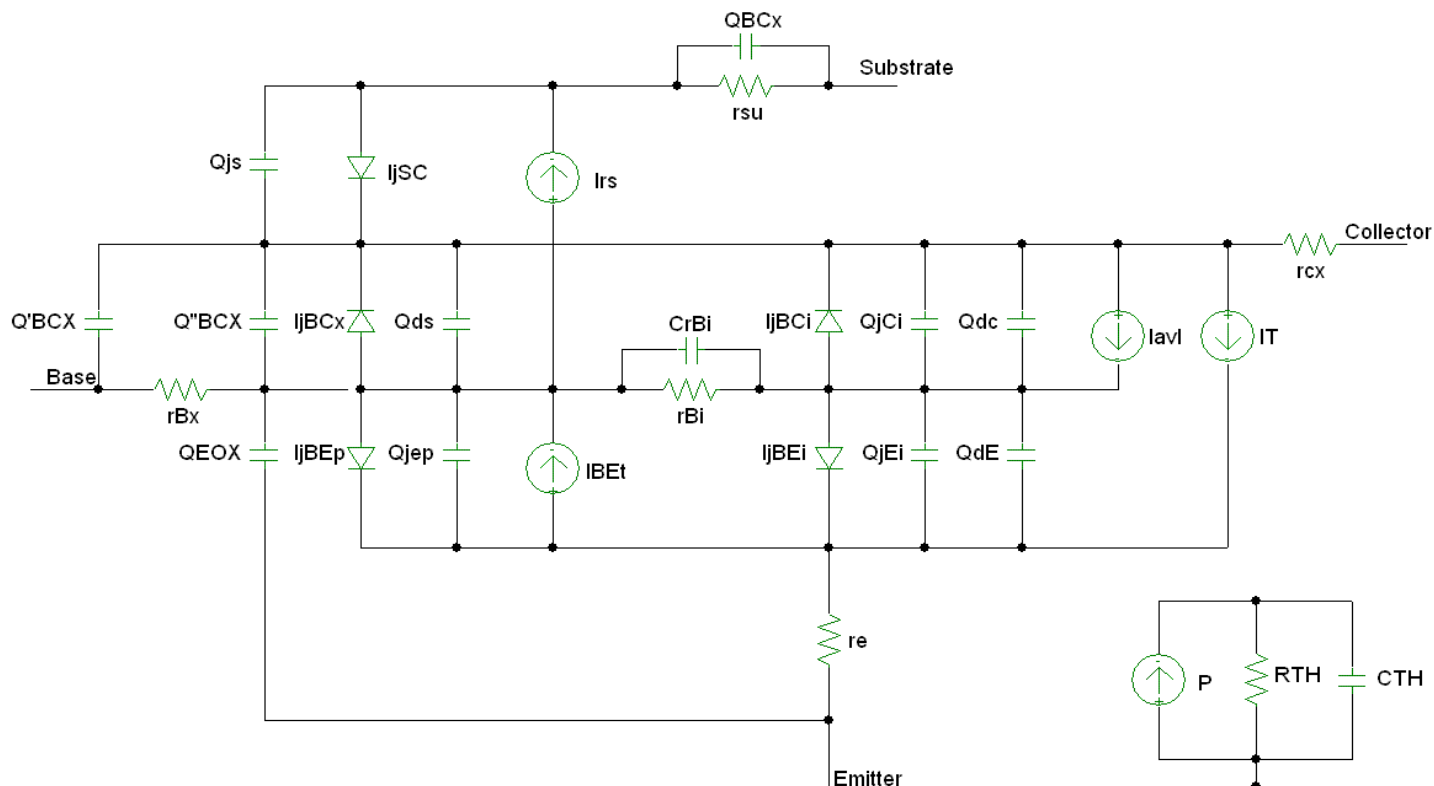
FIGURE 4.4 Equivalent Circuit of SGPM



4.3.2 HICUM Model

The HICUM model was introduced to overcome the shortcomings of the SGPM (Standard Gummel-Poon Model). The name of HICUM is derived from “High Current Model”. HICUM was initially developed with special emphasis on the modeling of the high current region, very important for many high-speed applications. Compared with SGPM, HICUM is based on an extended and generalized integral charge control relationship, and approaches the transistor dynamic behaviors in a more physical way. Its equivalent circuit diagram is shown in Figure 4.5. For more detailed information about HICUM, please refer to HICUM official web page (http://www.iee.et.tu-dresden.de/iee/eb/hic_new/hic_start.html).

FIGURE 4.5 Equivalent Circuit of HICUM



4.4 Model Extraction and Verification

The NPN models are extracted based on DC, CV, and RF measurements over a wide geometry and bias range.

The first set of plots (Figures 4.6 through 4.38) display the characterization plots for the digital (high speed) NPN. The second set of plots (Figures 4.39 through 4.89) display the characterization plots for the low voltage (standard) NPN. The last set of plots (Figures 4.90 through 4.140) display the characterization plots for the high voltage NPN. All of the plots show both the SGPM (red dashed line) and HICUM (solid red line) models against the data. Multiple devices in parallel are characterized for smaller emitter lengths to reduce de-embedding errors. The device type and size are encoded in the figure caption as “Voltage LxWxM_Configuration.” Thus a HV 0.2x1x10_122 caption refers to a high voltage NPN with a width (W) of 0.2μm, a length (L) of 1μm, with 10 devices in parallel (M) and a 122 emitter/base/collector finger configuration.

4.4.1 High Speed (Digital) NPN Verification Plots

FIGURE 4.6 Gummel Plot HS 0.2x0.76x10_122

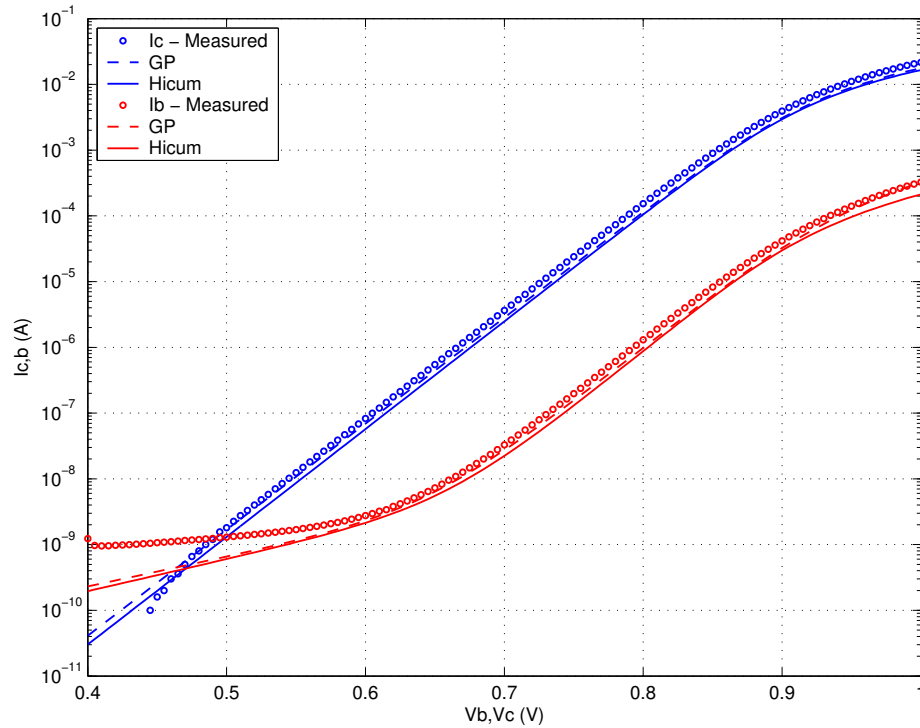


FIGURE 4.7 Beta vs. I_c : HS 0.2x0.76x10_122

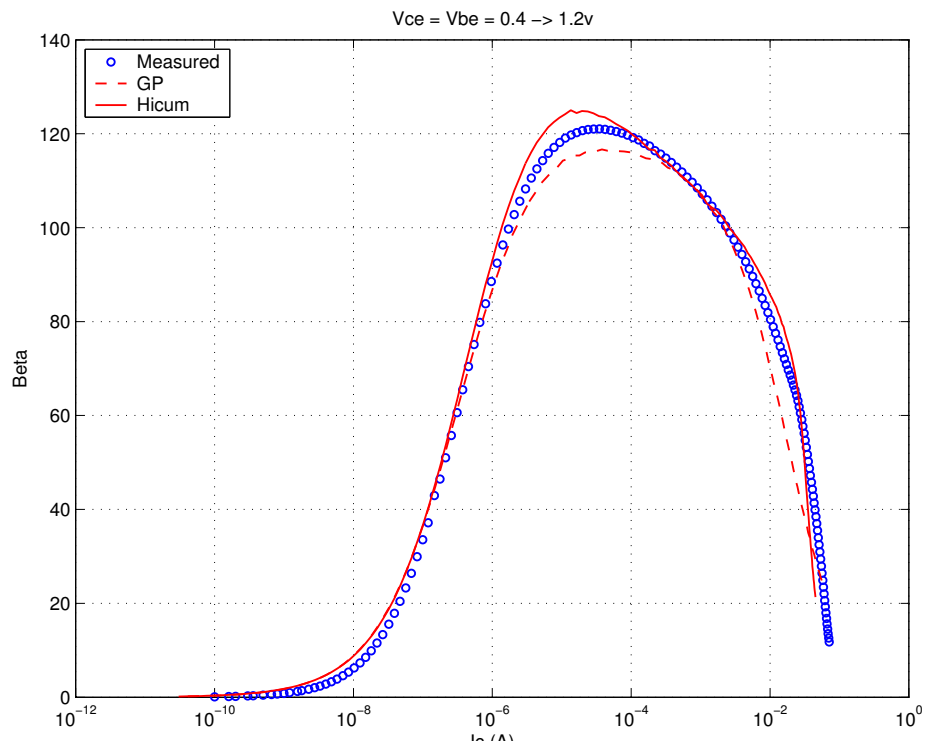
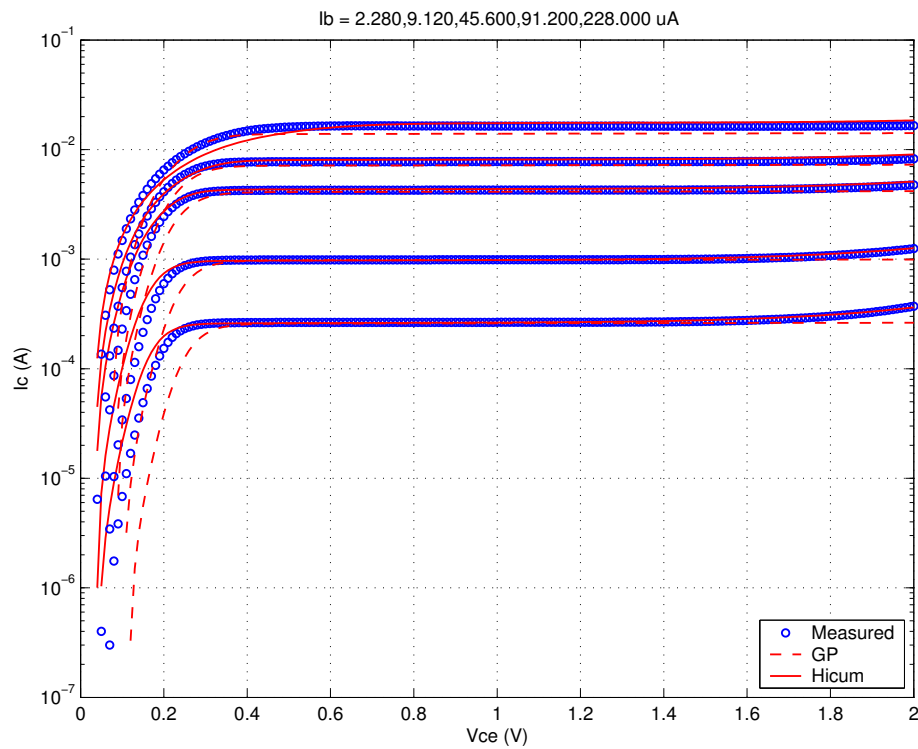


FIGURE 4.8 I_C vs. V_{CE} at constant I_B : HS 0.2x0.76x10_122



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FIGURE 4.9 Gummel Plot HS 0.2x4.52x1_122

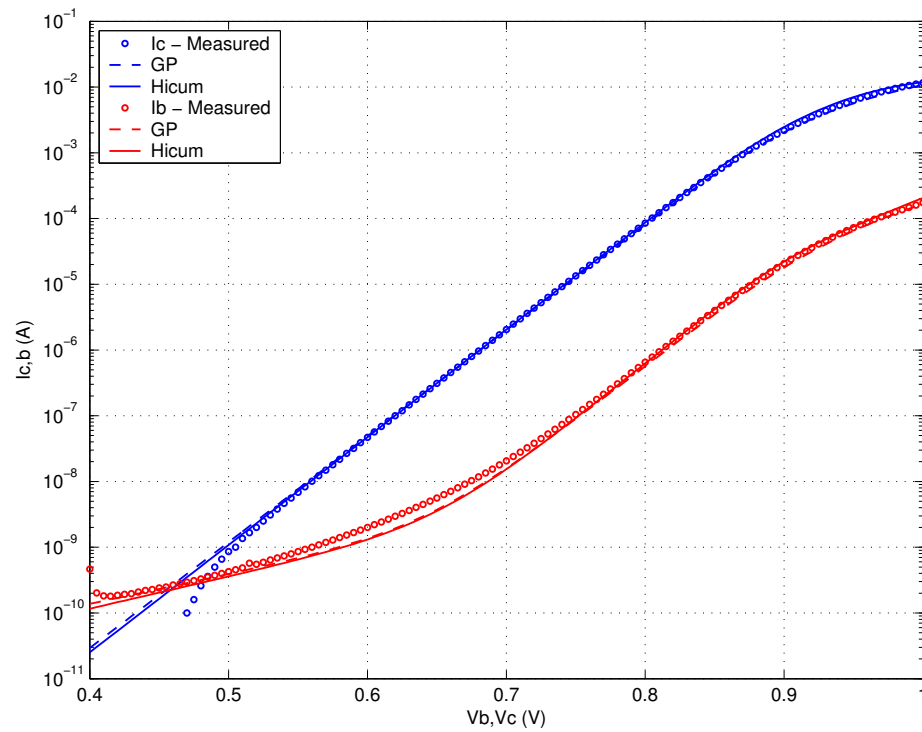
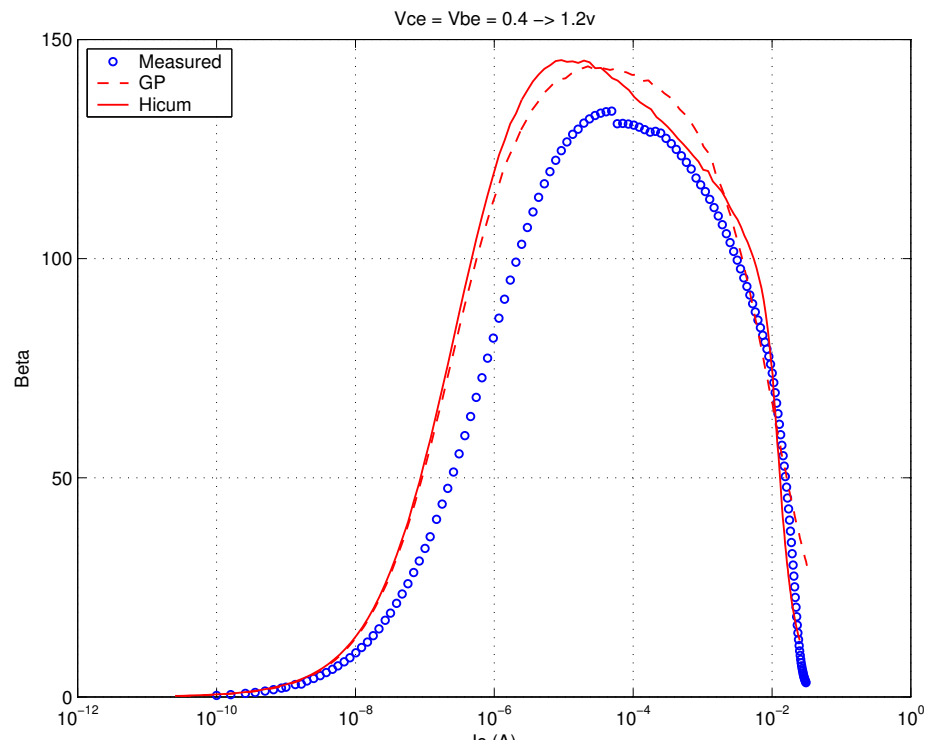
FIGURE 4.10 Beta vs. I_c : HS 0.2x4.52x1_122

FIGURE 4.11 I_C vs. V_{CE} at constant I_B : HS 0.2x4.52x1_122

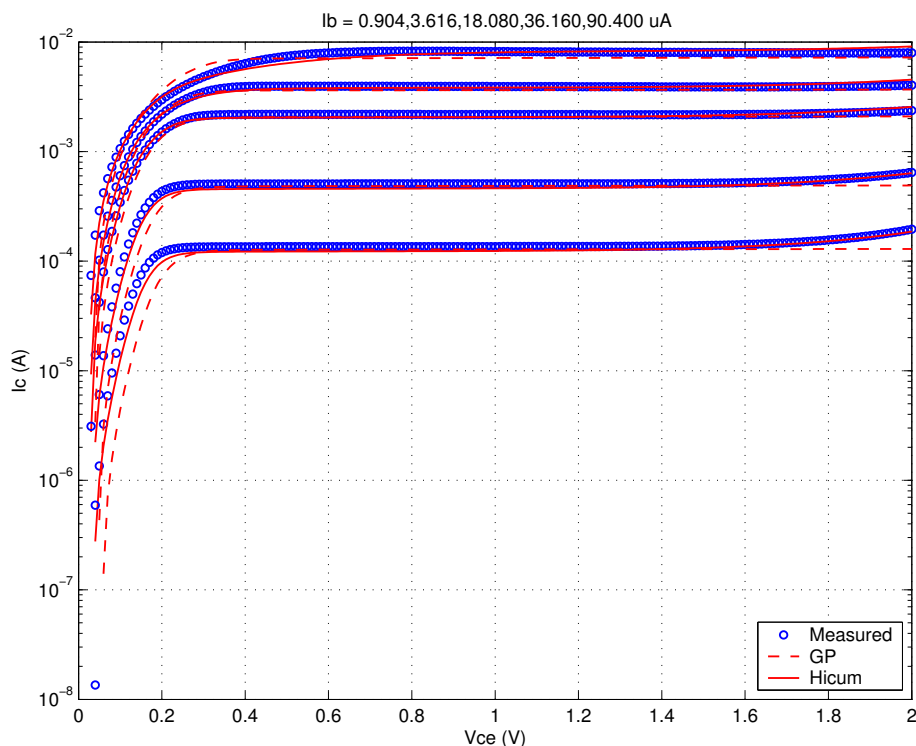


FIGURE 4.12 f_T vs. I_C : HS 0.2x4.52x1_122

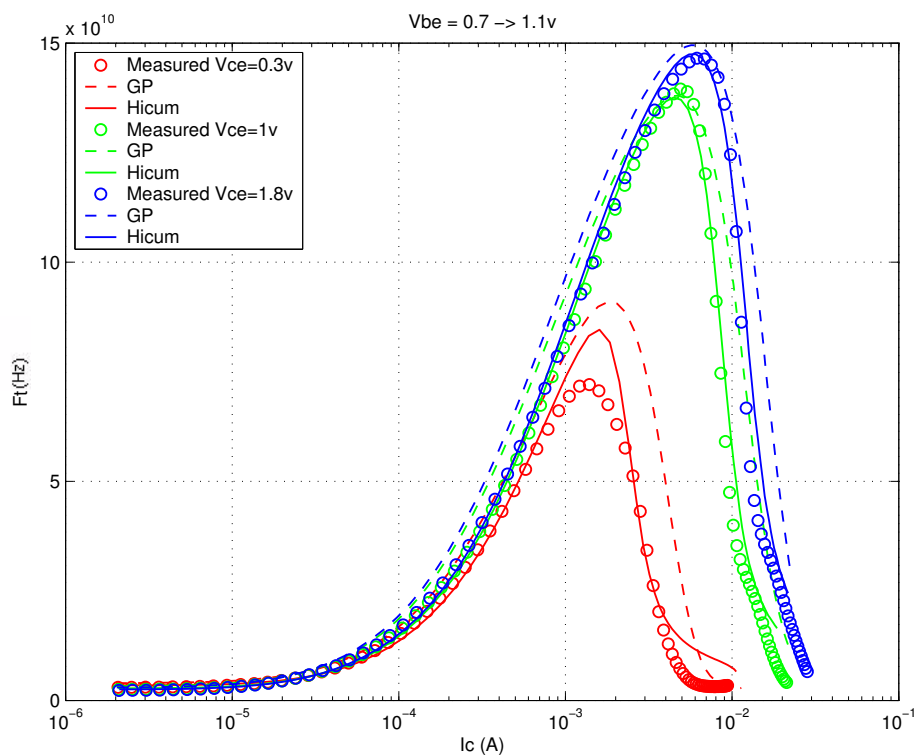
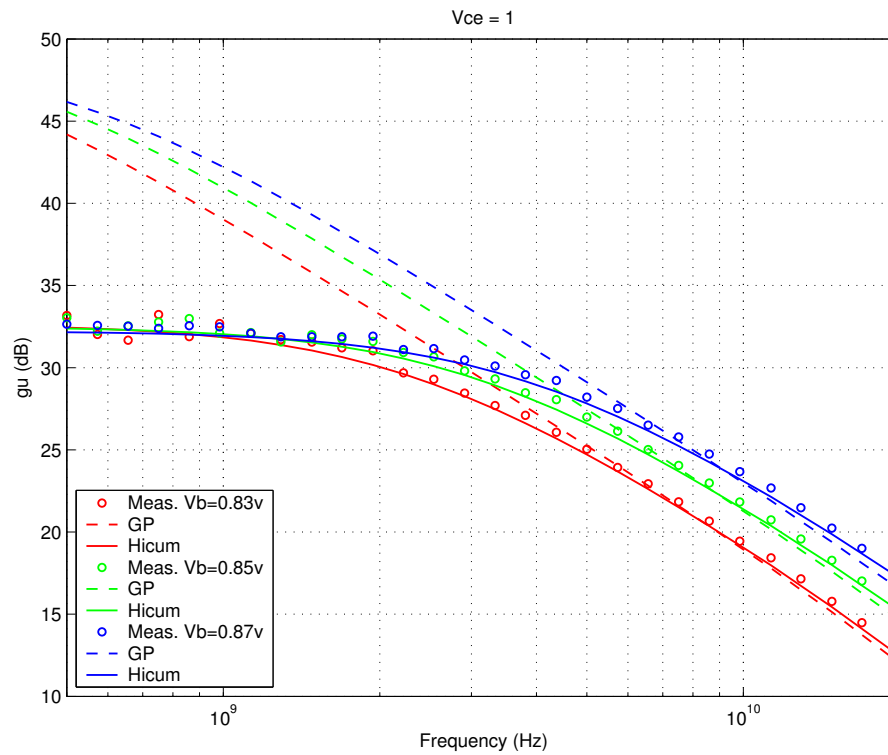


FIGURE 4.13 Power Gain vs. Freq: HS 0.2x4.52x1_122



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FIGURE 4.14 Y-parameters vs. FREQ: HS 0.2x4.52x1_122

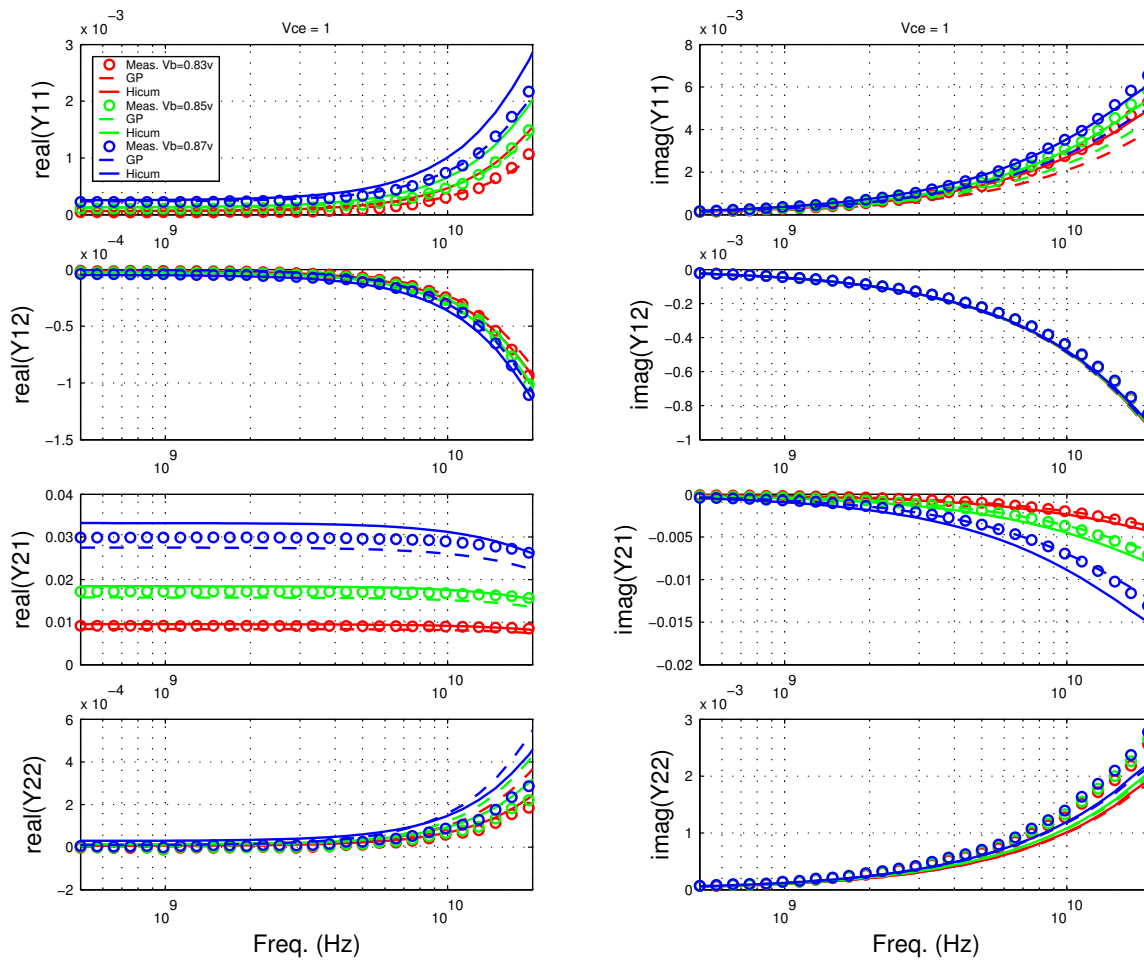


FIGURE 4.15 Gummel Plot HS 0.2x10.16x1_122

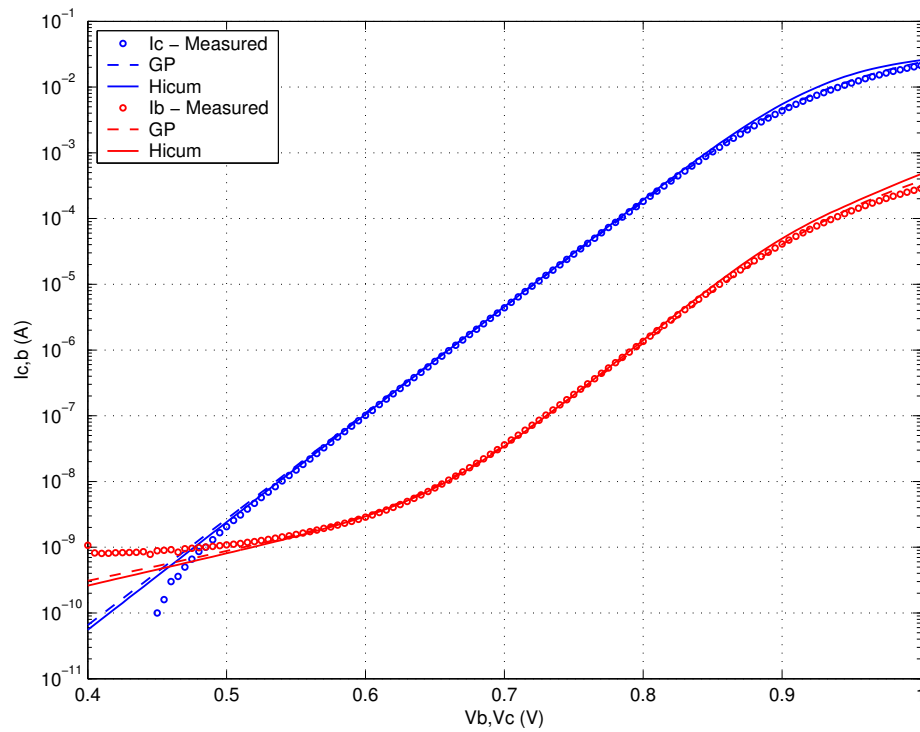
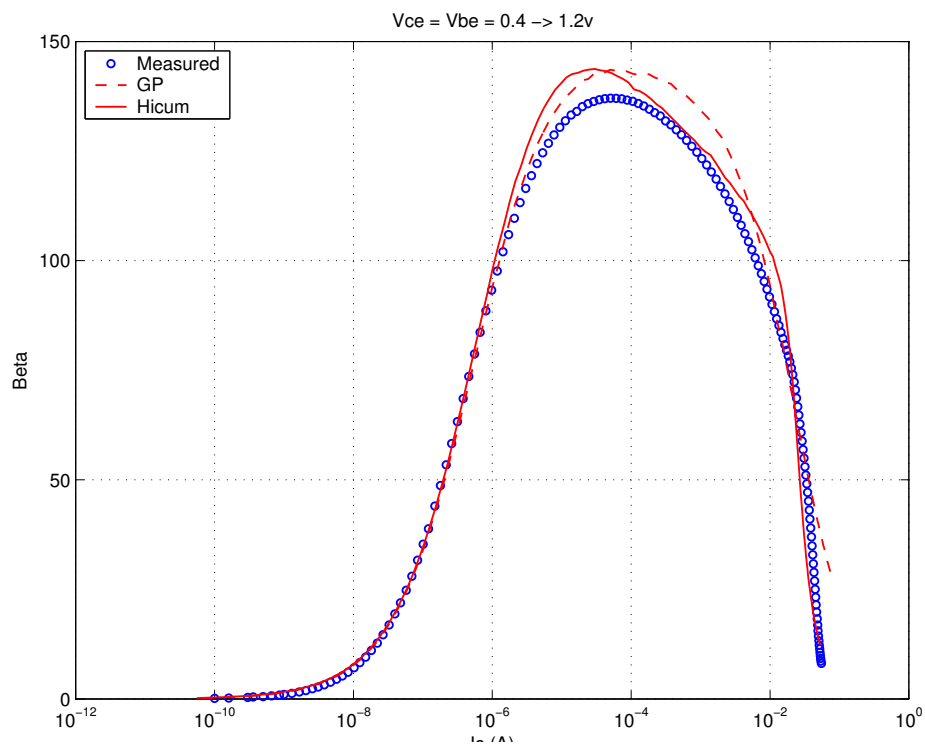
FIGURE 4.16 Beta vs. I_c : HS 0.2x10.16x1_122

FIGURE 4.17 I_C vs. V_{CE} at constant I_B : HS 0.2x10.16x1_122

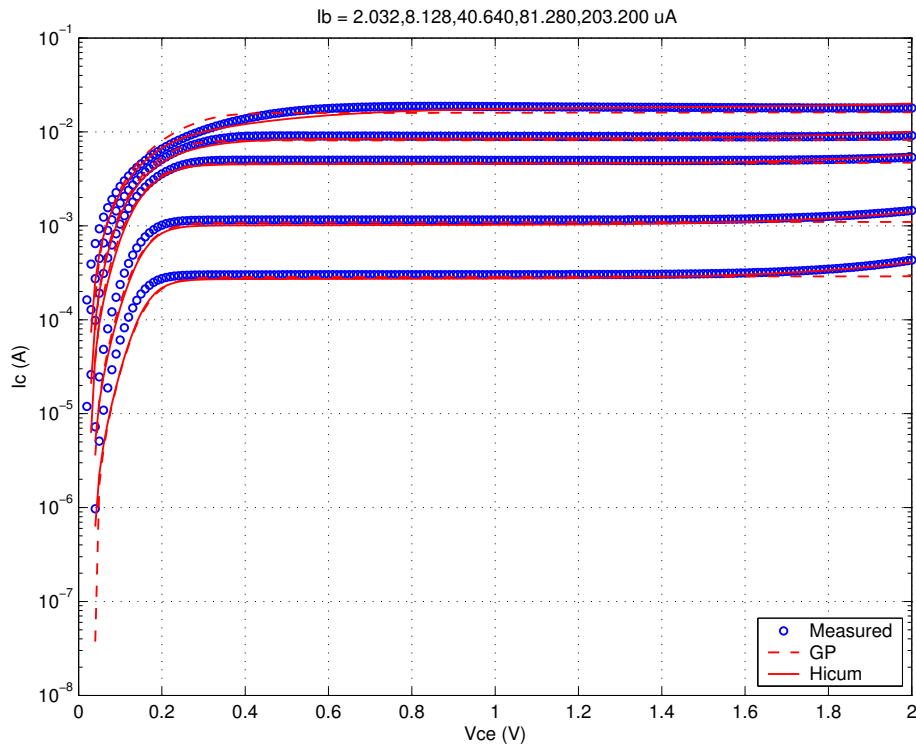


FIGURE 4.18 f_T vs. I_C : HS 0.2x10.16x1_122

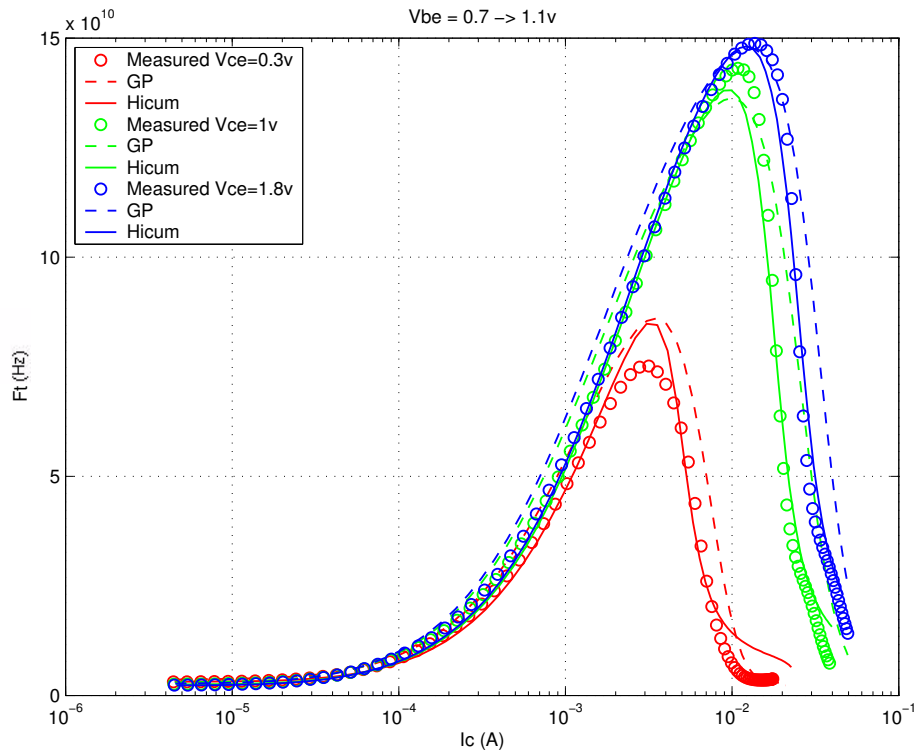
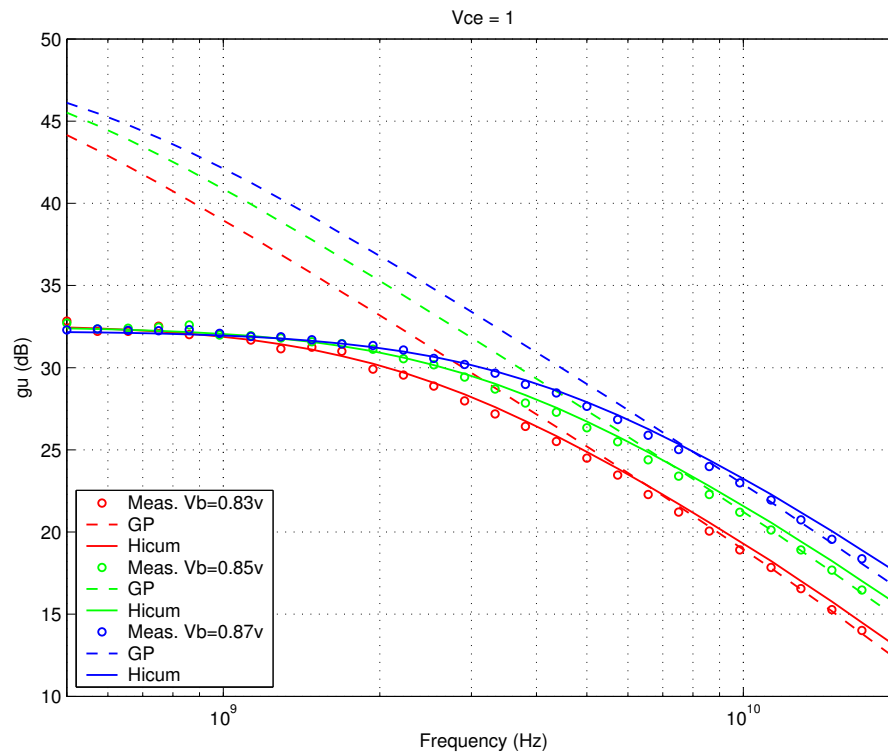


FIGURE 4.19 Power Gain vs. Freq: HS 0.2x10.16x1_122



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FIGURE 4.20 Y-parameters vs. FREQ: HS 0.2x10.16x1_122

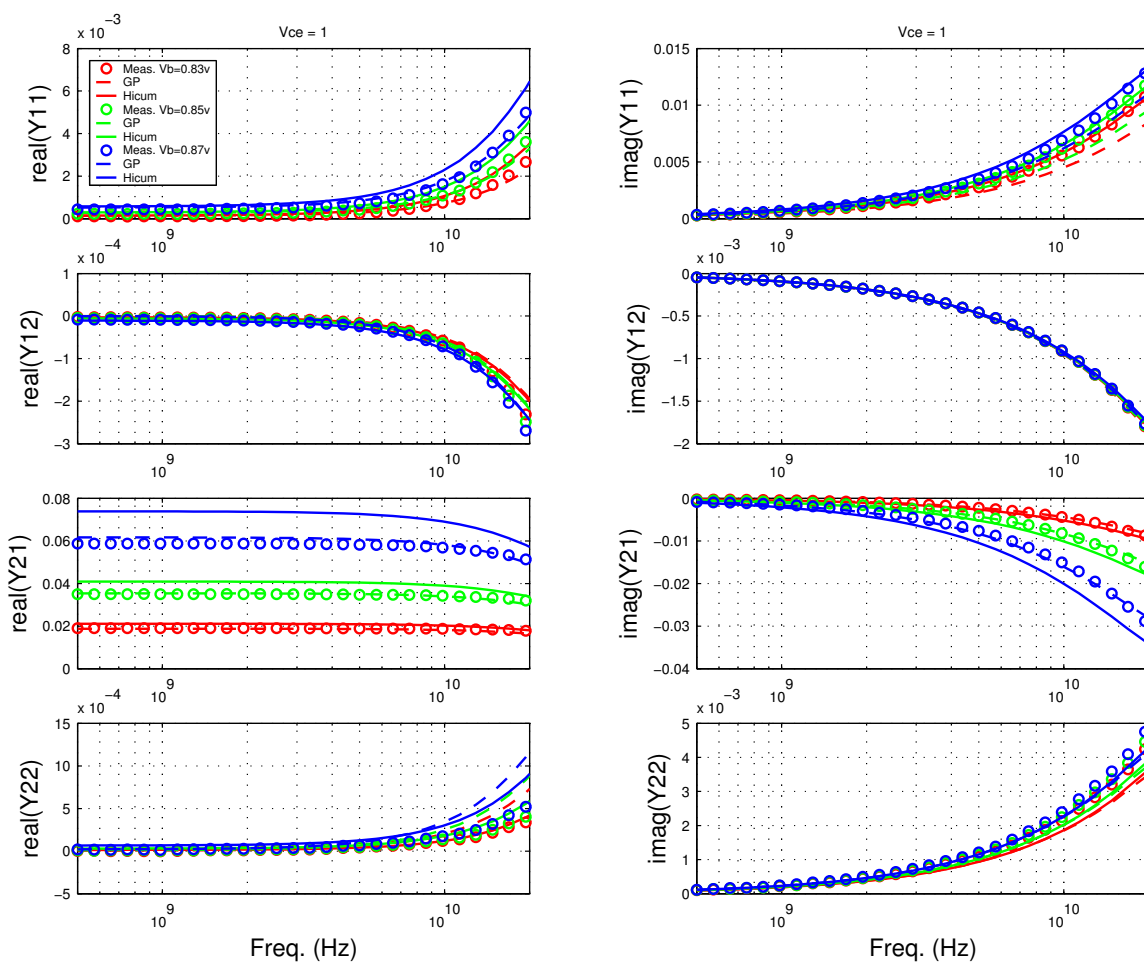


FIGURE 4.21 Gummel Plot HS 0.2x2.64x1_232

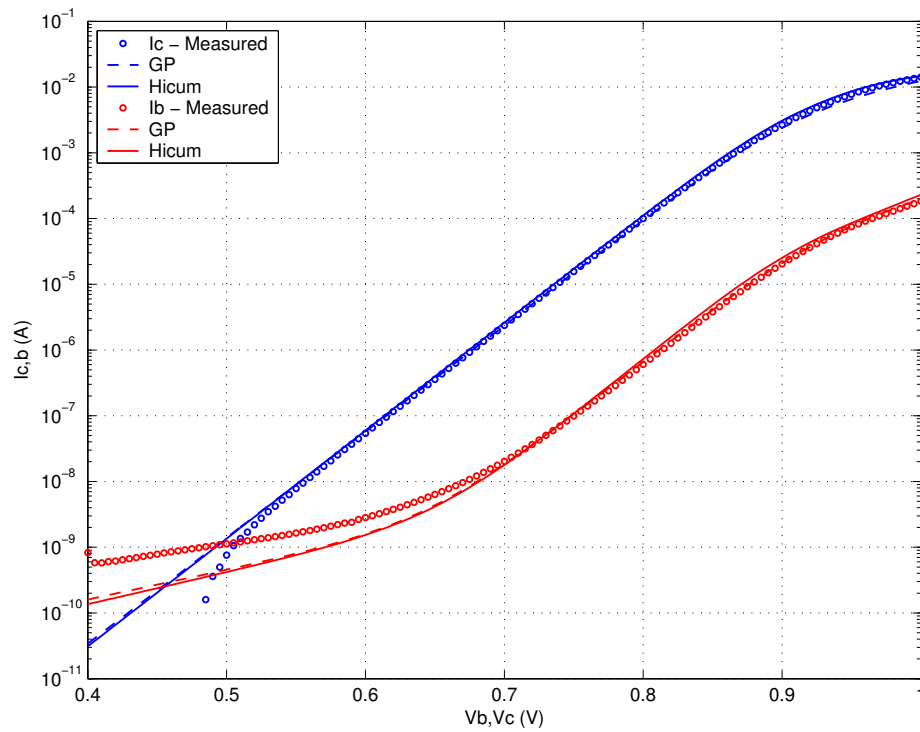
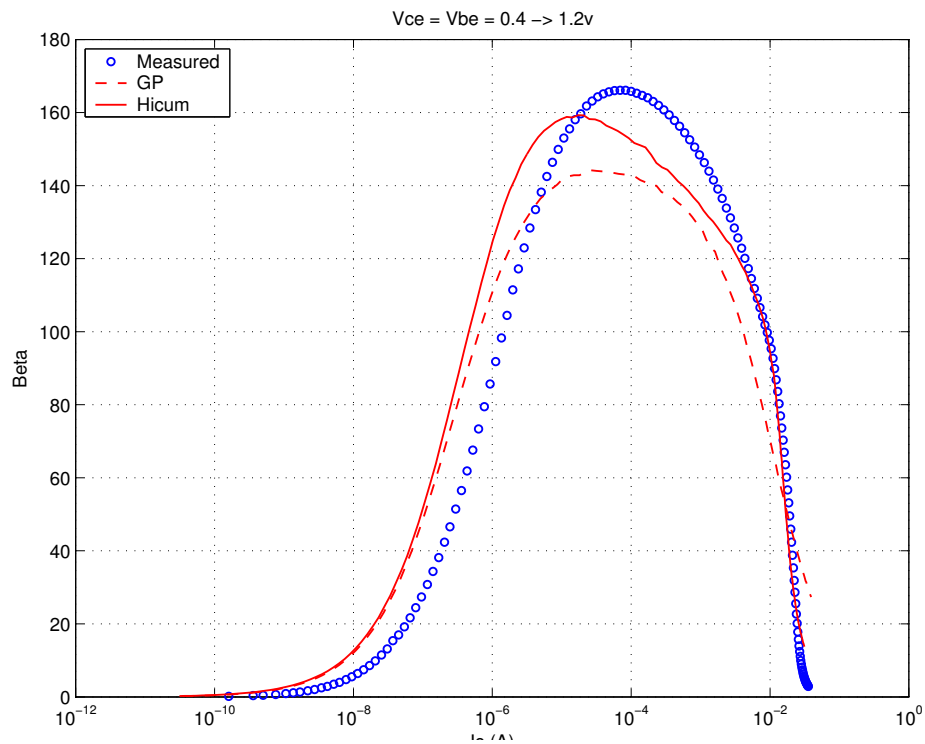
FIGURE 4.22 Beta vs. I_c : HS 0.2x2.64x1_232

FIGURE 4.23 I_C vs. V_{CE} at constant I_B : HS 0.2x2.64x1_232

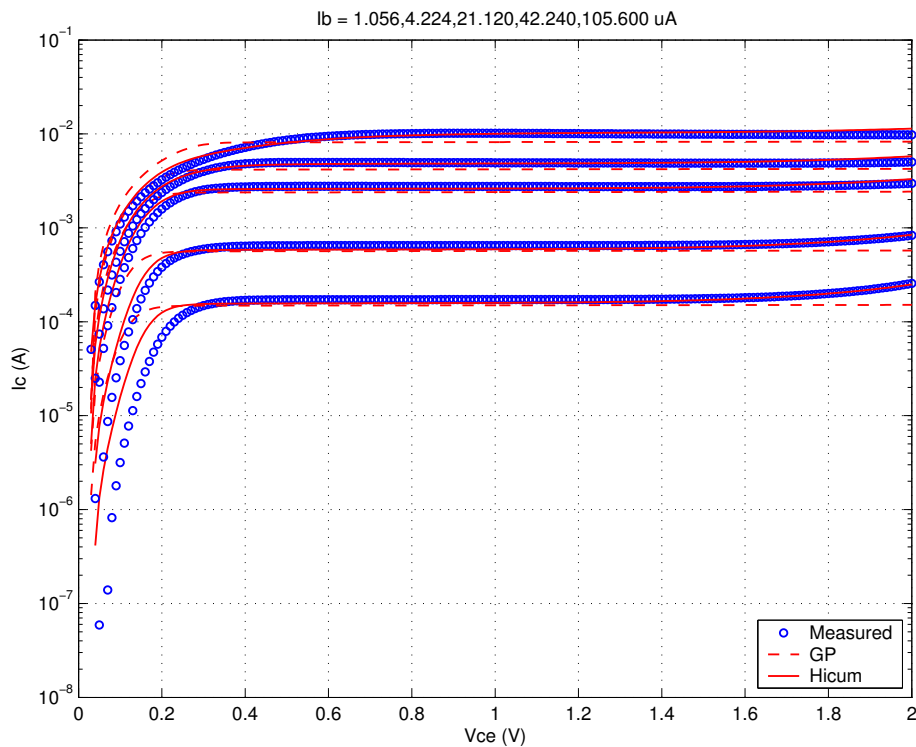


FIGURE 4.24 f_T vs. I_C : HS 0.2x2.64x1_232

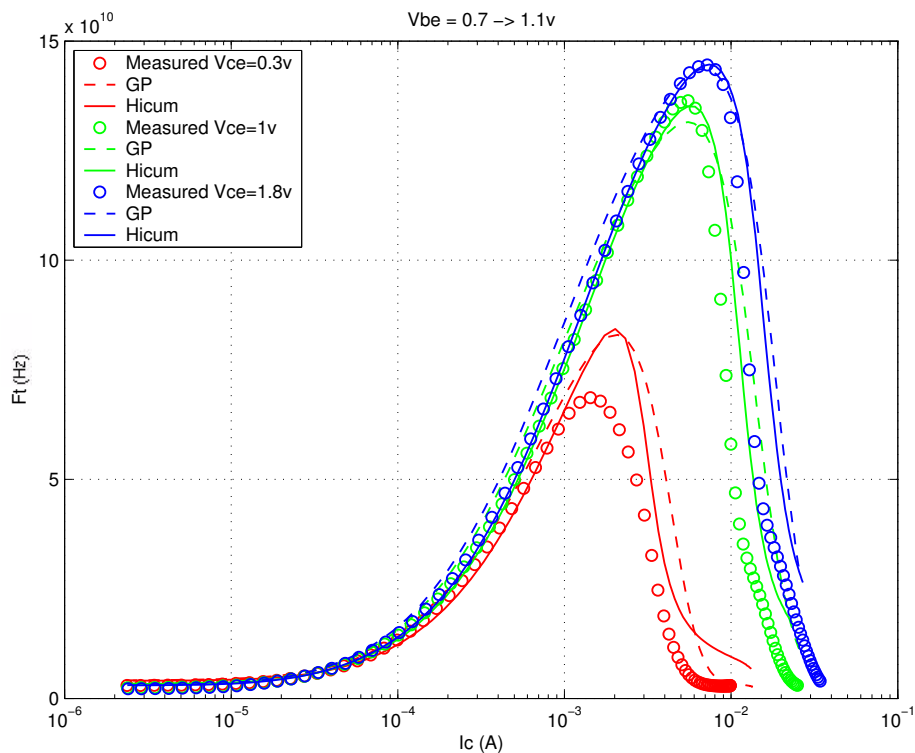
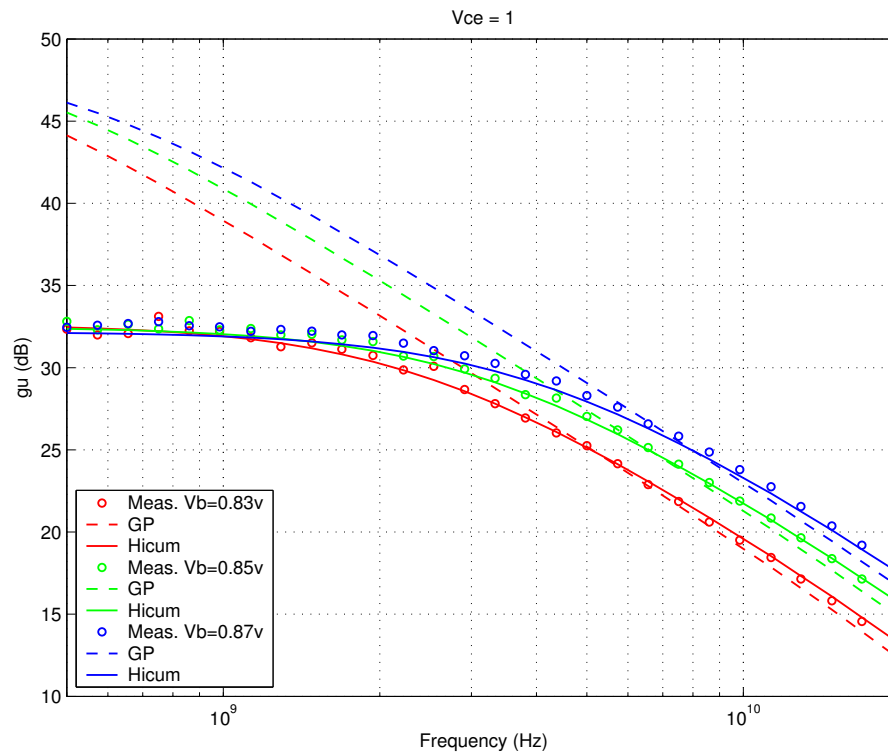


FIGURE 4.25 Power Gain vs. Freq: HS 0.2x2.64x1_232



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FIGURE 4.26 Y-parameters vs. FREQ: HS 0.2x2.64x1_232

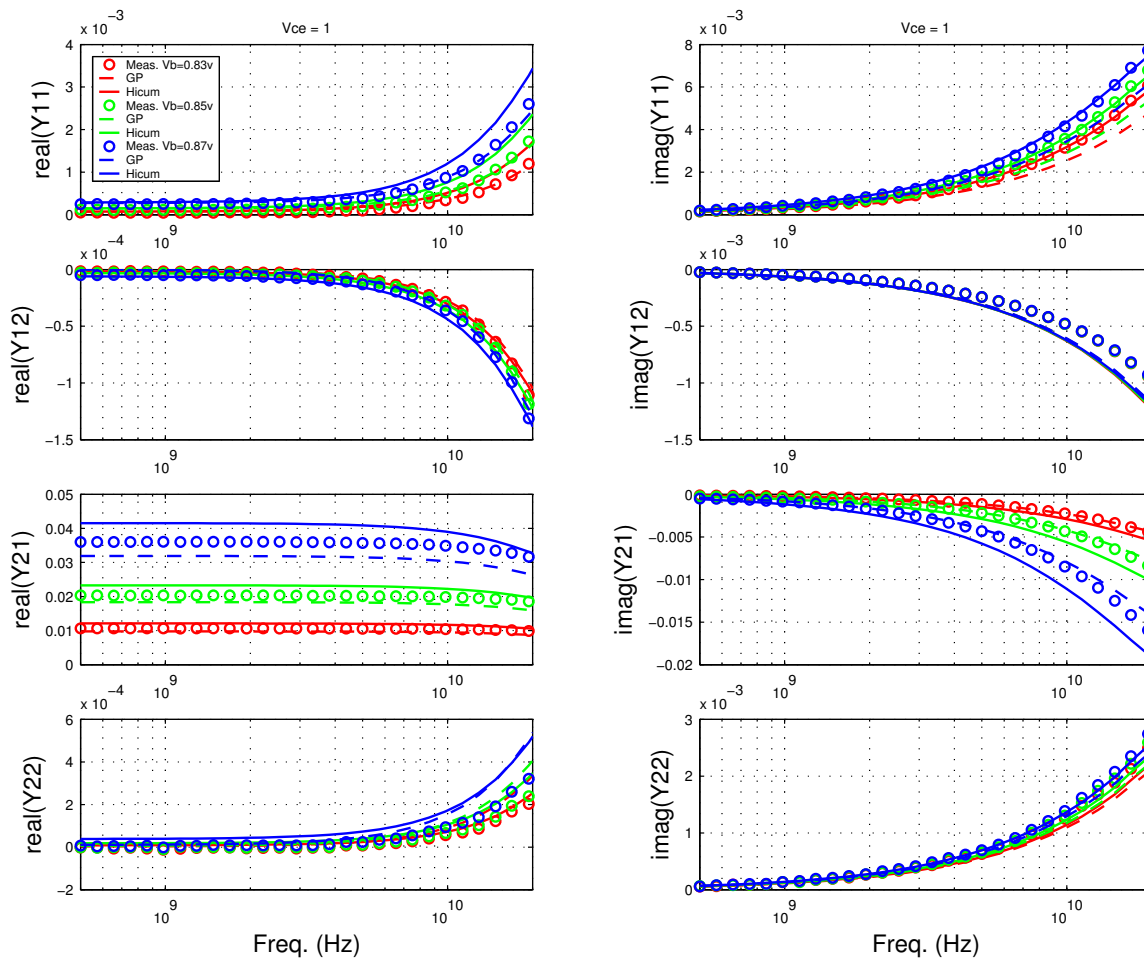


FIGURE 4.27 Gummel Plot HS 0.2x4.52x1_232

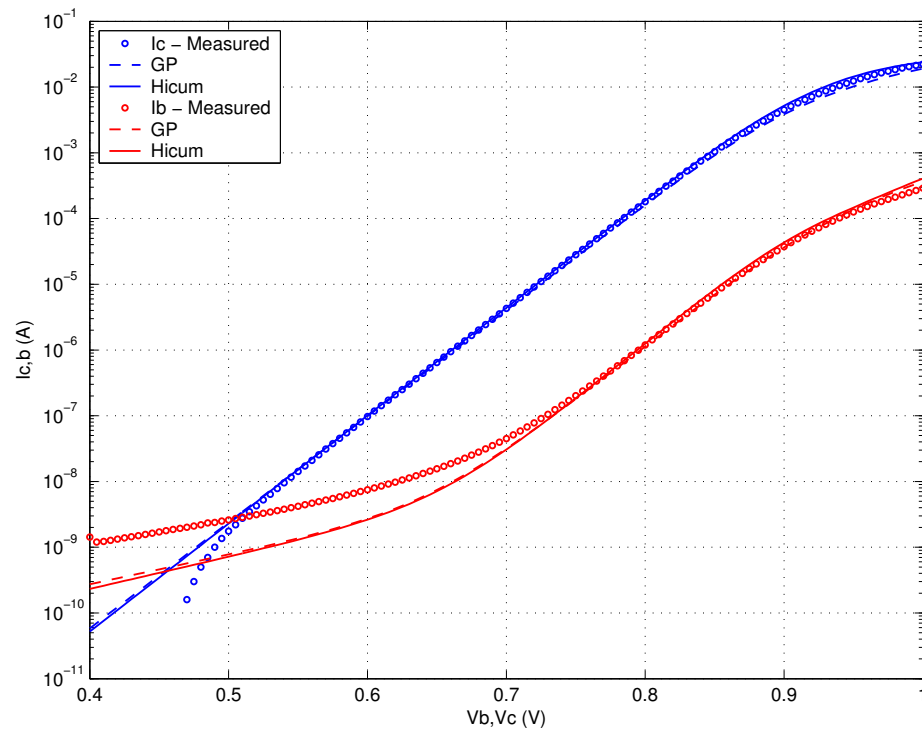
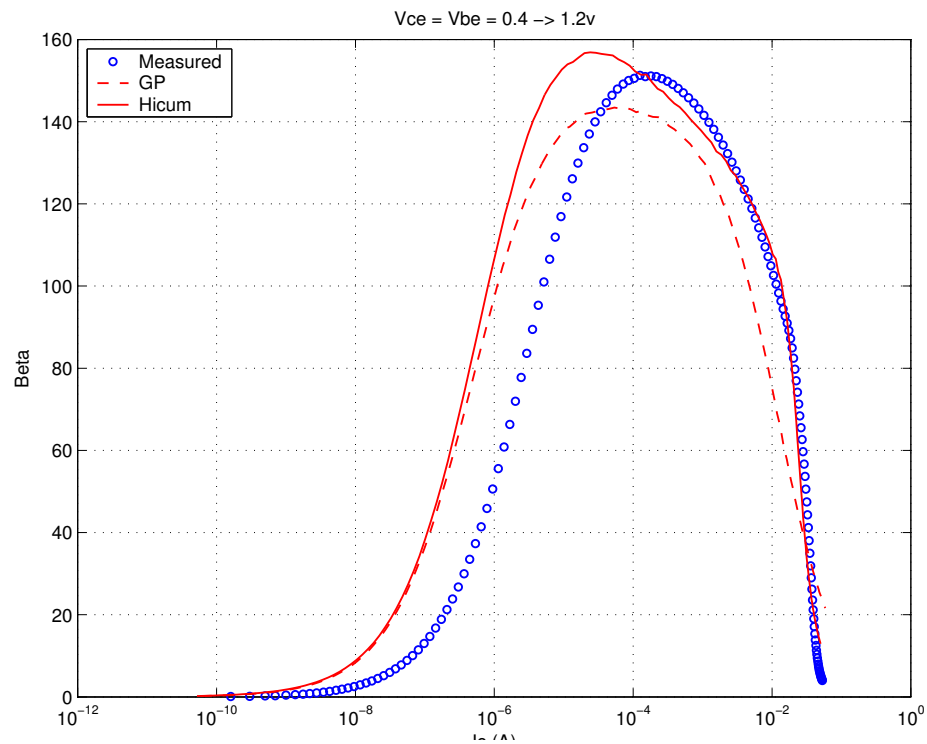
FIGURE 4.28 Beta vs. I_c : HS 0.2x4.52x1_232

FIGURE 4.29 I_C vs. V_{CE} at constant I_B : HS 0.2x4.52x1_232

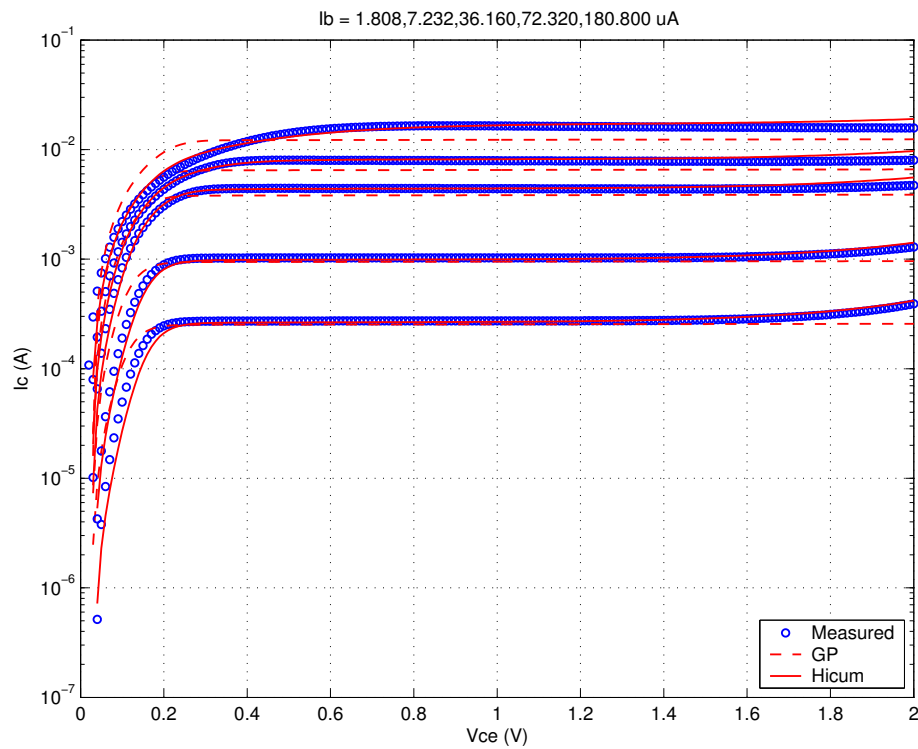


FIGURE 4.30 f_T vs. I_C : HS 0.2x4.52x1_232

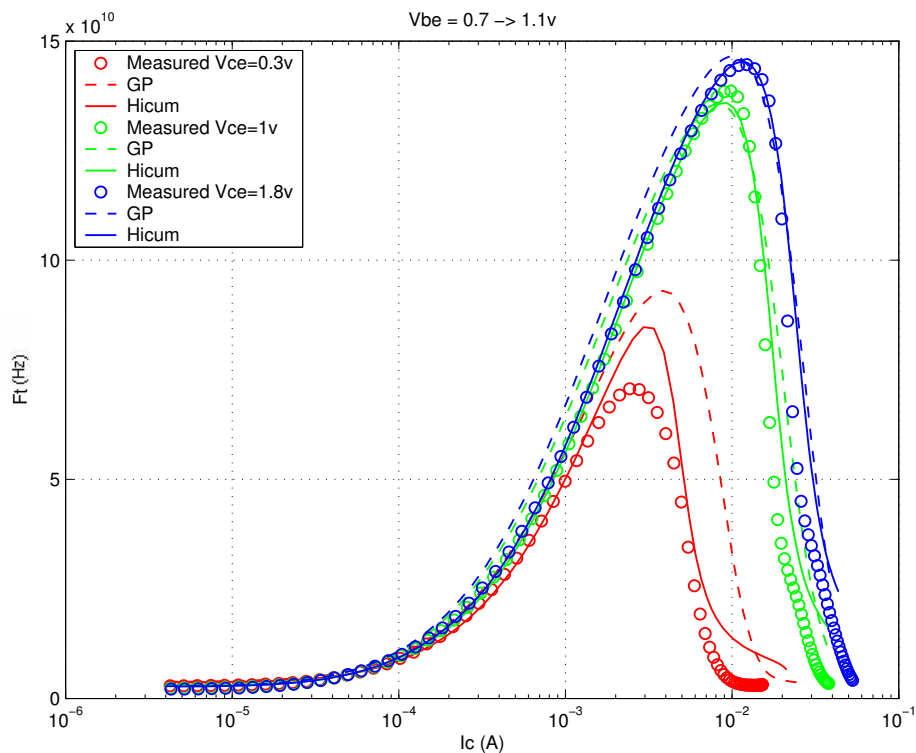
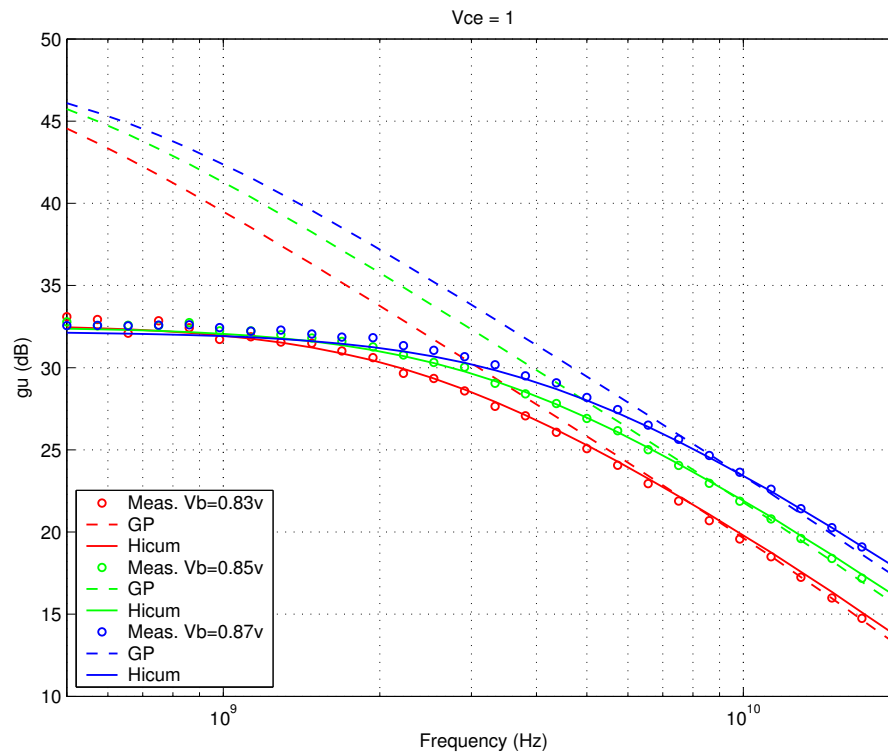


FIGURE 4.31 Power Gain vs. Freq: HS 0.2x4.52x1_232



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FIGURE 4.32 Y-parameters vs. FREQ: HS 0.2x4.52x1_232

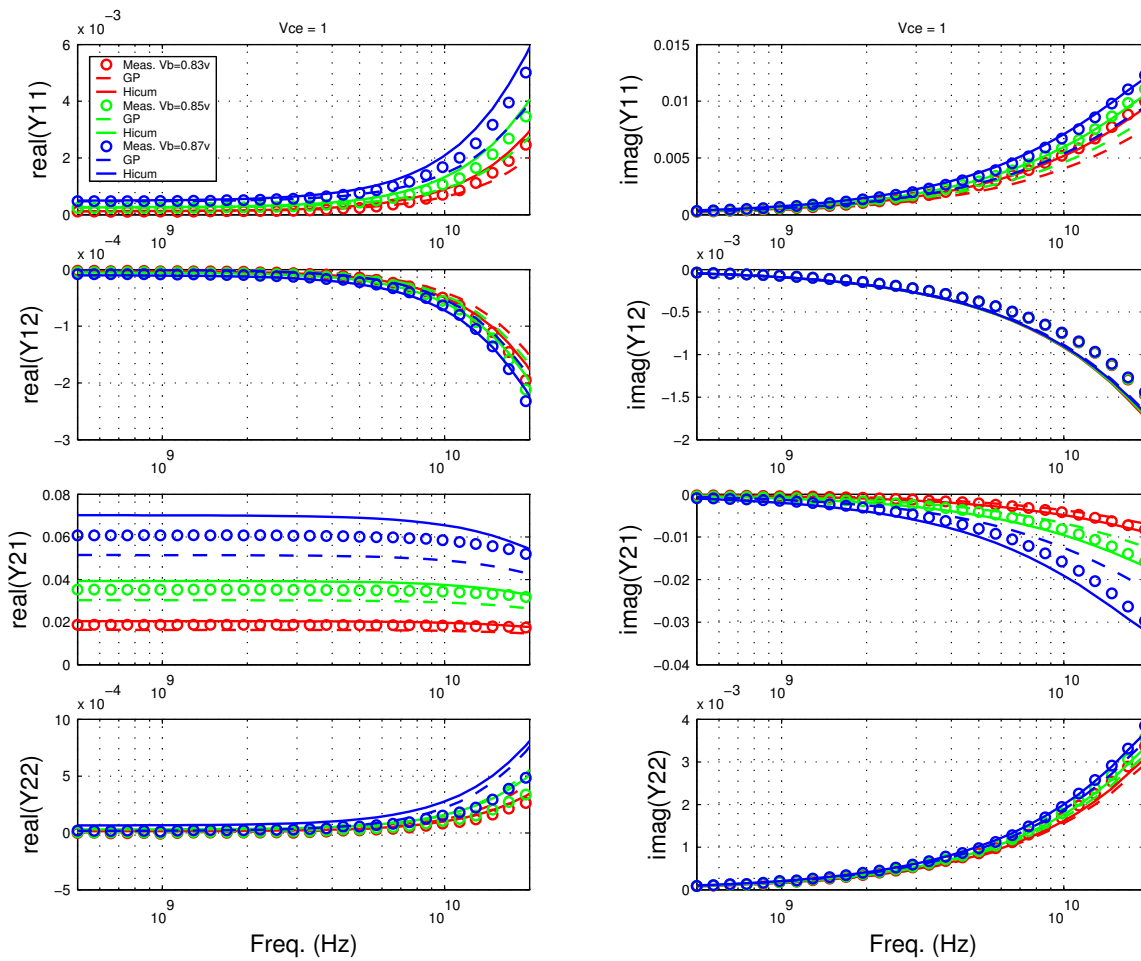


FIGURE 4.33 Gummel Plot HS 0.2x10.16x1_232

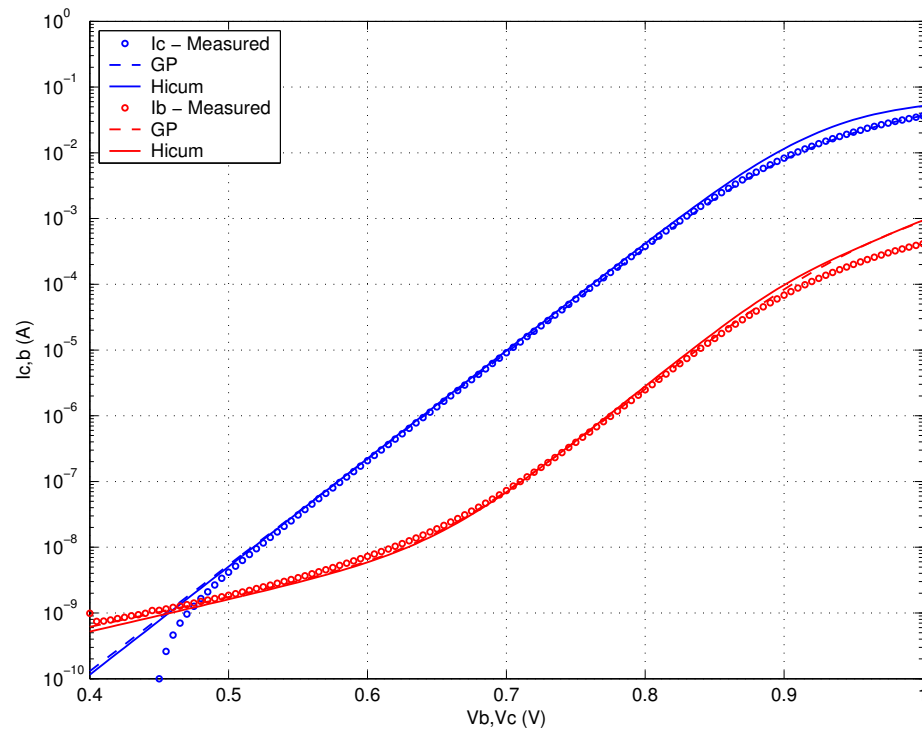
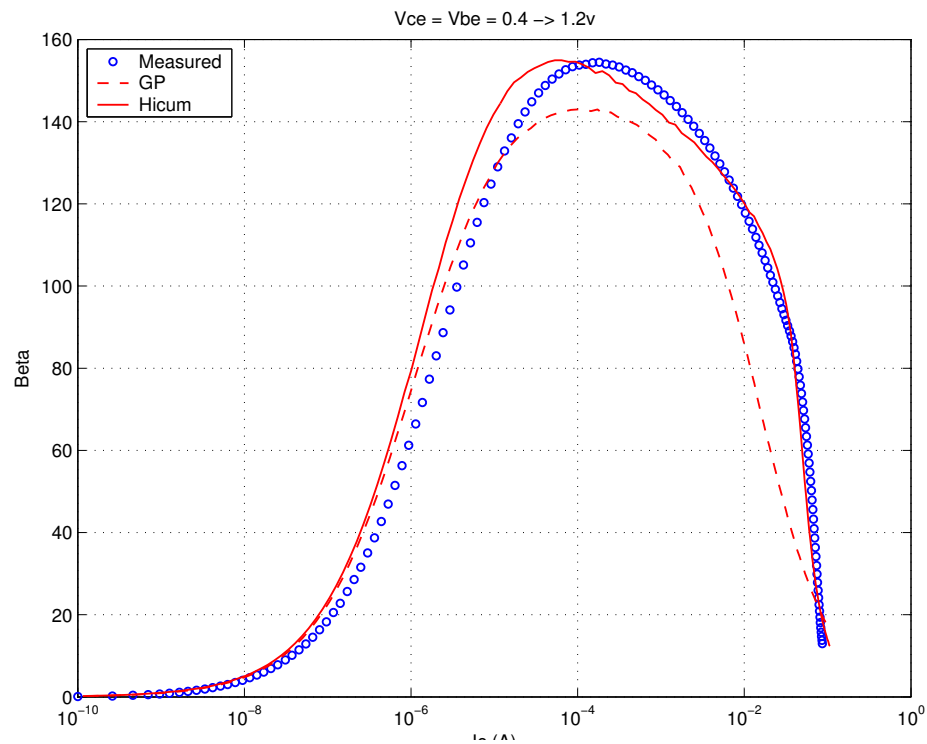
FIGURE 4.34 Beta vs. I_c : HS 0.2x10.16x1_232

FIGURE 4.35 I_C vs. V_{CE} at constant I_B : HS 0.2x10.16x1_232

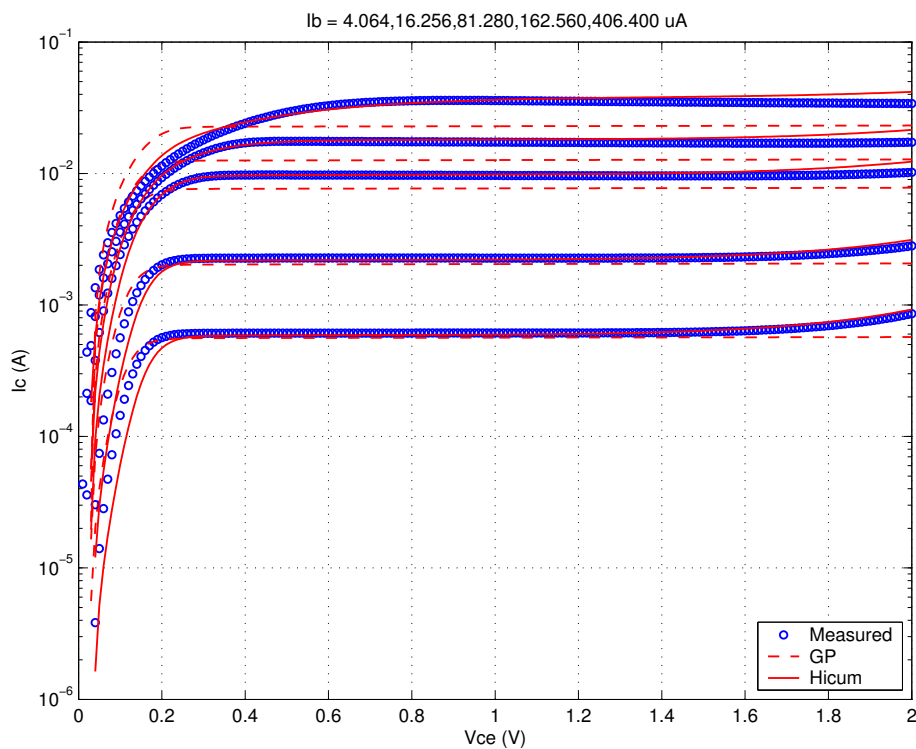


FIGURE 4.36 f_T vs. I_C : HS 0.2x10.16x1_232

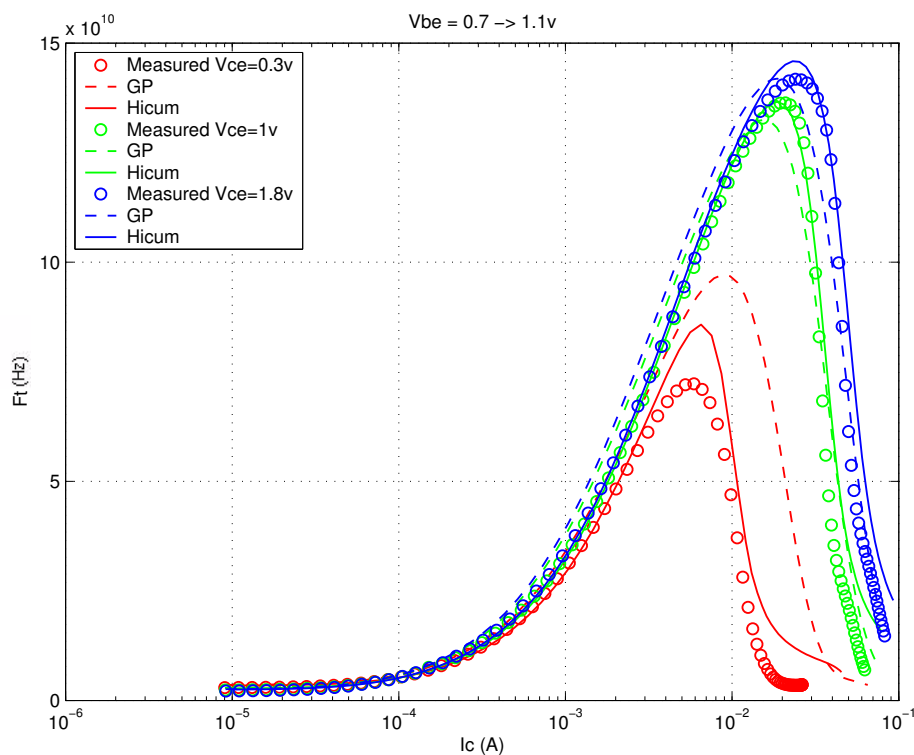
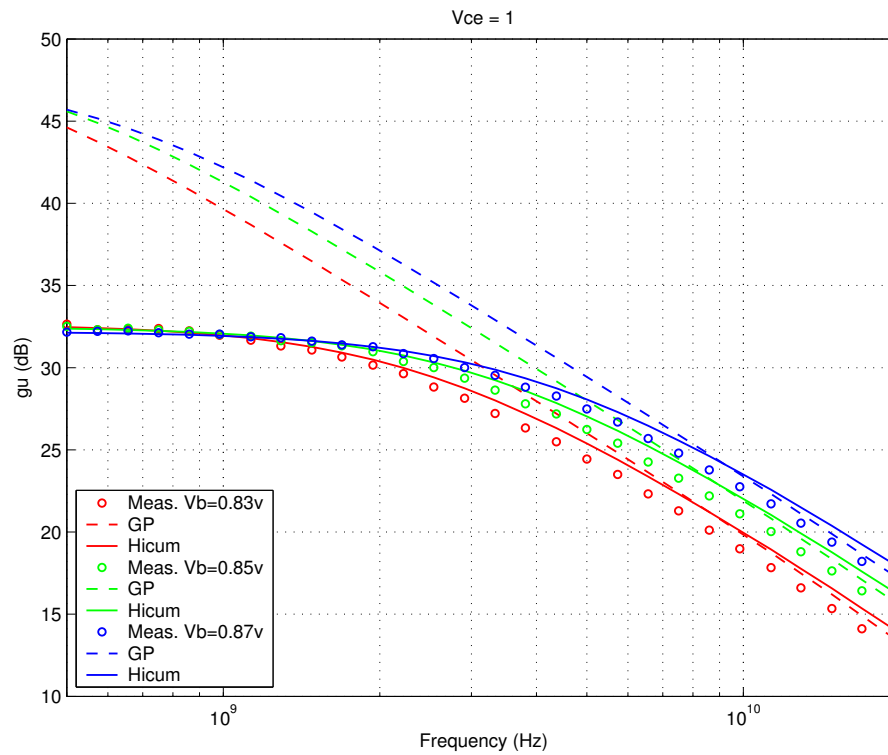


FIGURE 4.37 Power Gain vs. Freq: HS 0.2x10.16x1_232

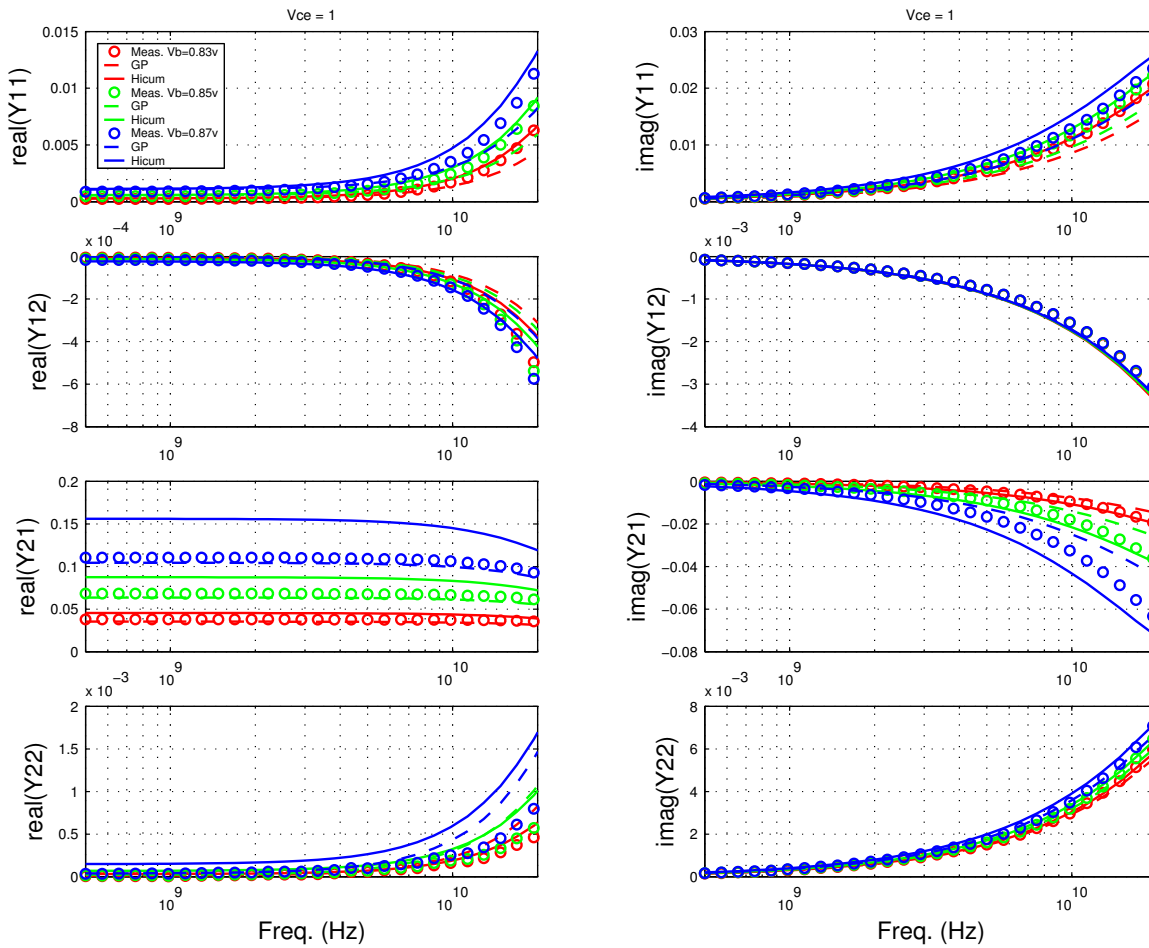


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FIGURE 4.38 Y-parameters vs. FREQ: HS 0.2x10.16x1_232



4.4.2 Low Voltage (Standard) NPN Verification Plots

FIGURE 4.39 Gummel Plot LV 0.2x0.76x10_122

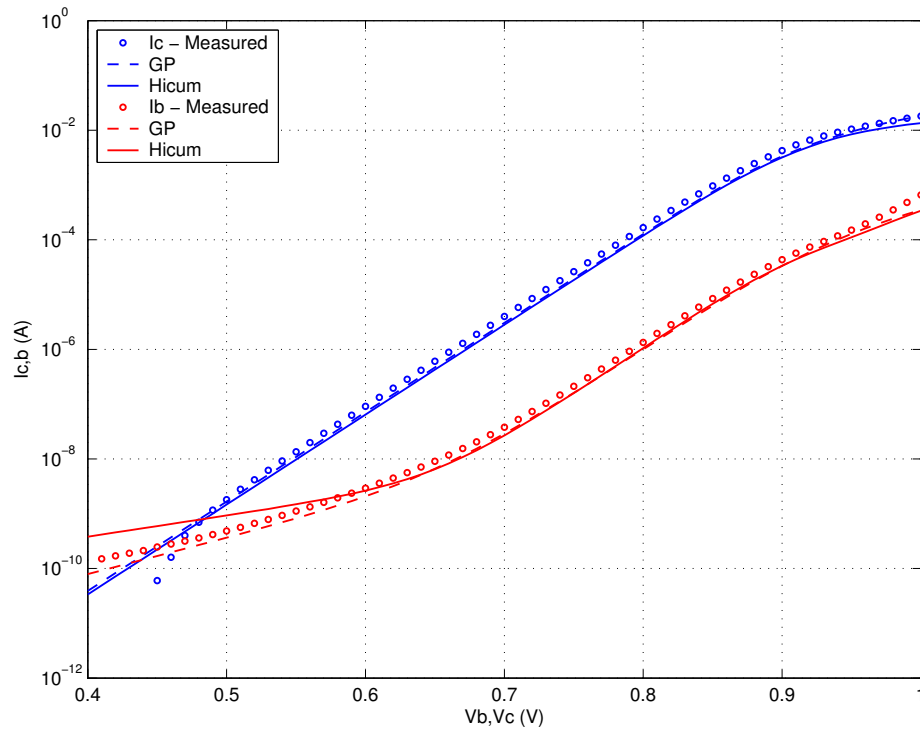


FIGURE 4.40 Beta vs. I_c : LV 0.2x0.76x10_122

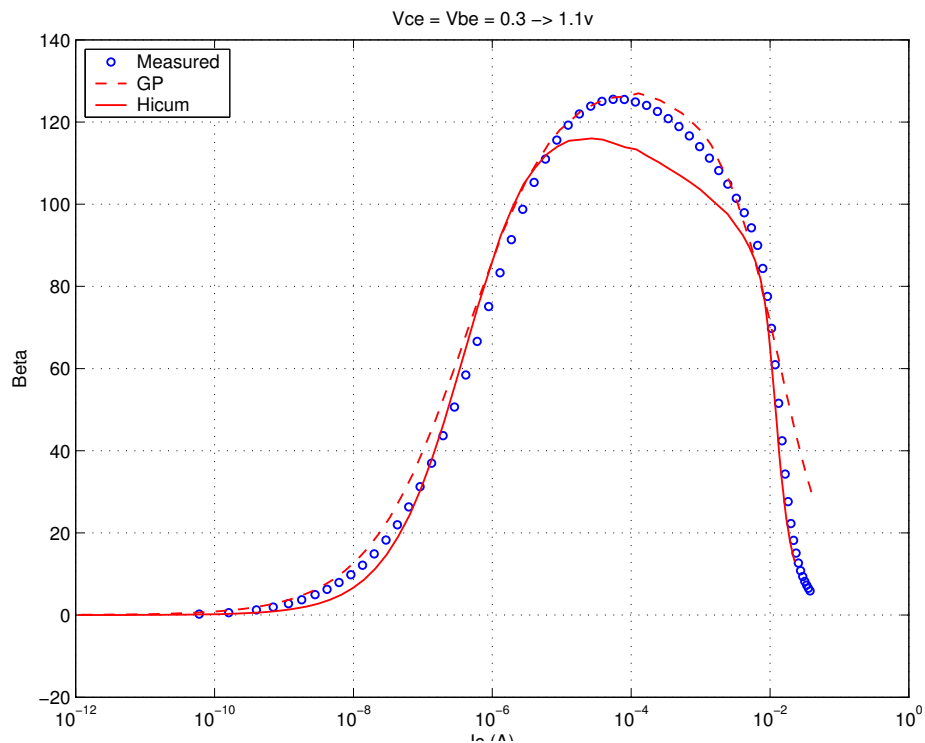
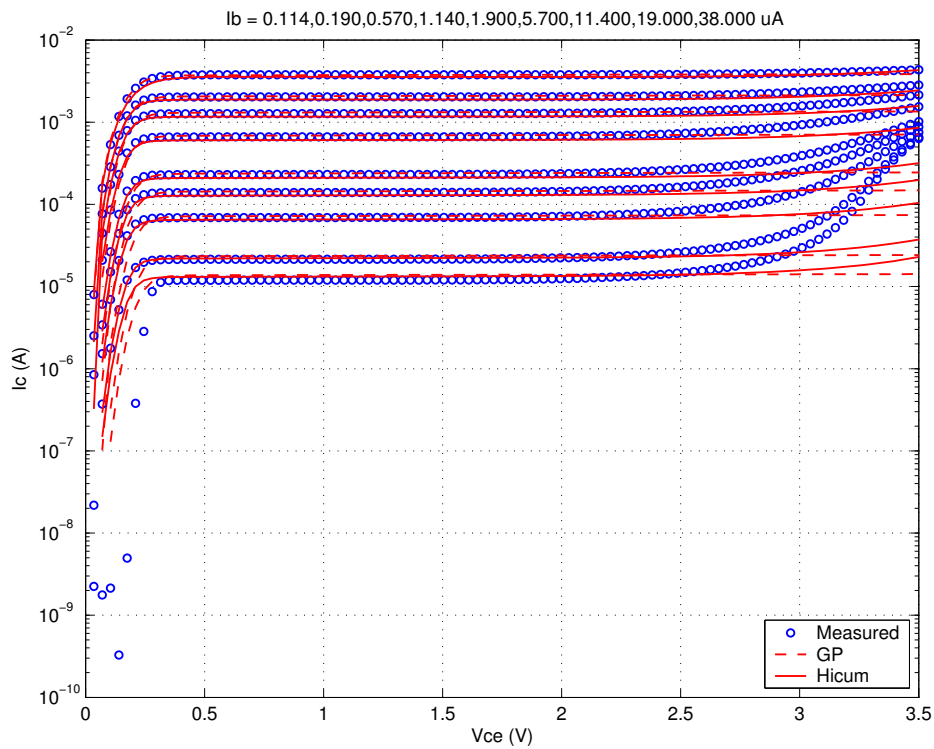


FIGURE 4.41 I_C vs. V_{CE} at constant I_B : LV 0.2x0.76x10_122



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FIGURE 4.42 Gummel Plot LV 0.2x4.52x1_122

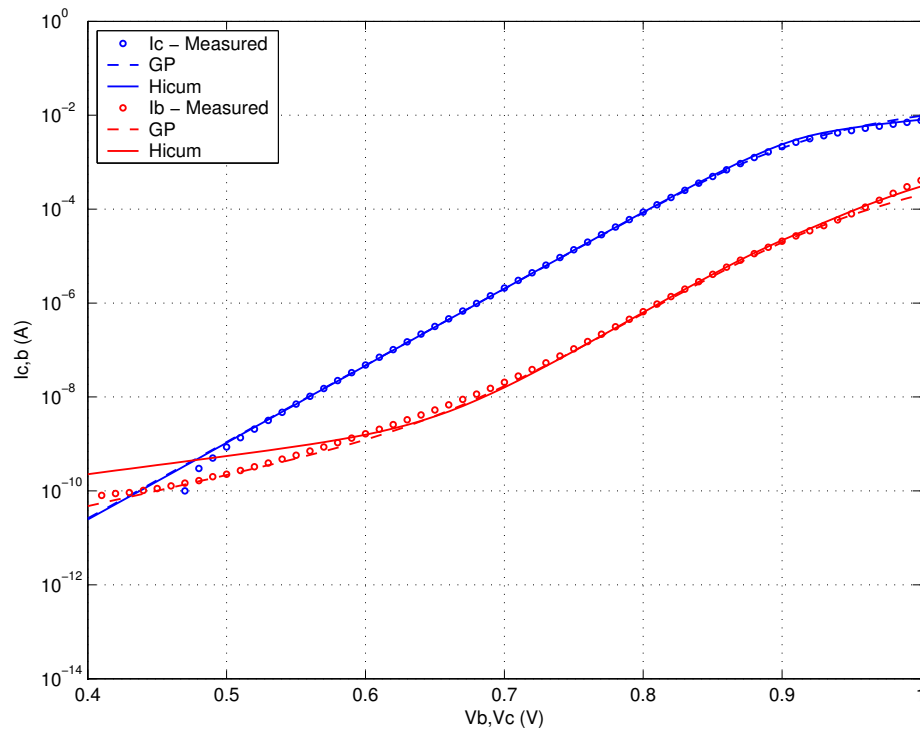
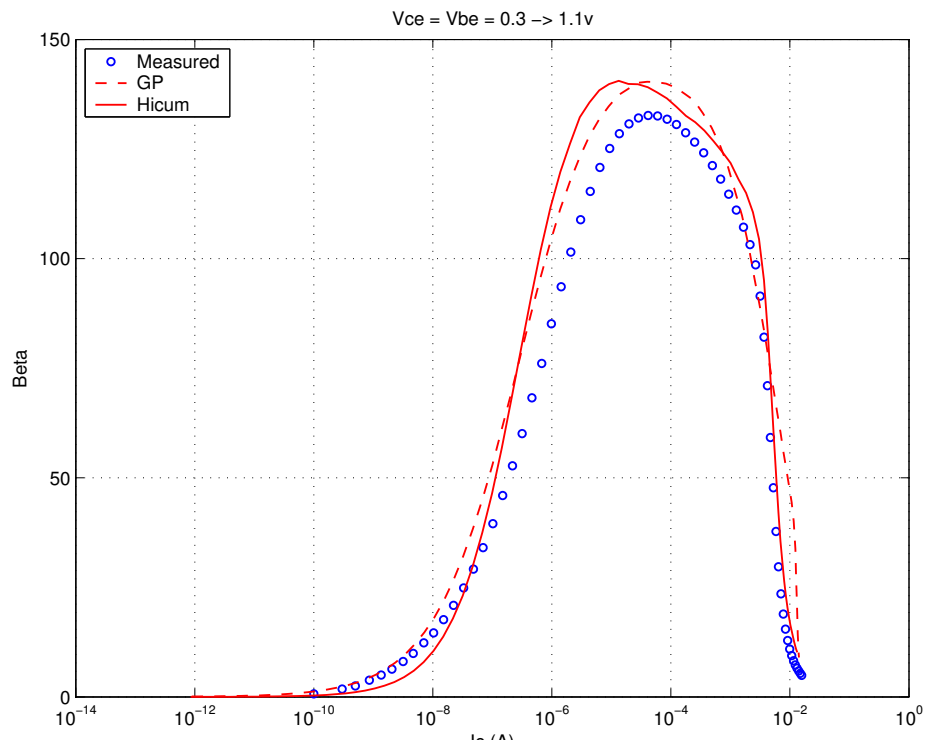
FIGURE 4.43 Beta vs. I_c : LV 0.2x4.52x1_122

FIGURE 4.44 IC vs. VCE at constant IB: LV 0.2x4.52x1_122

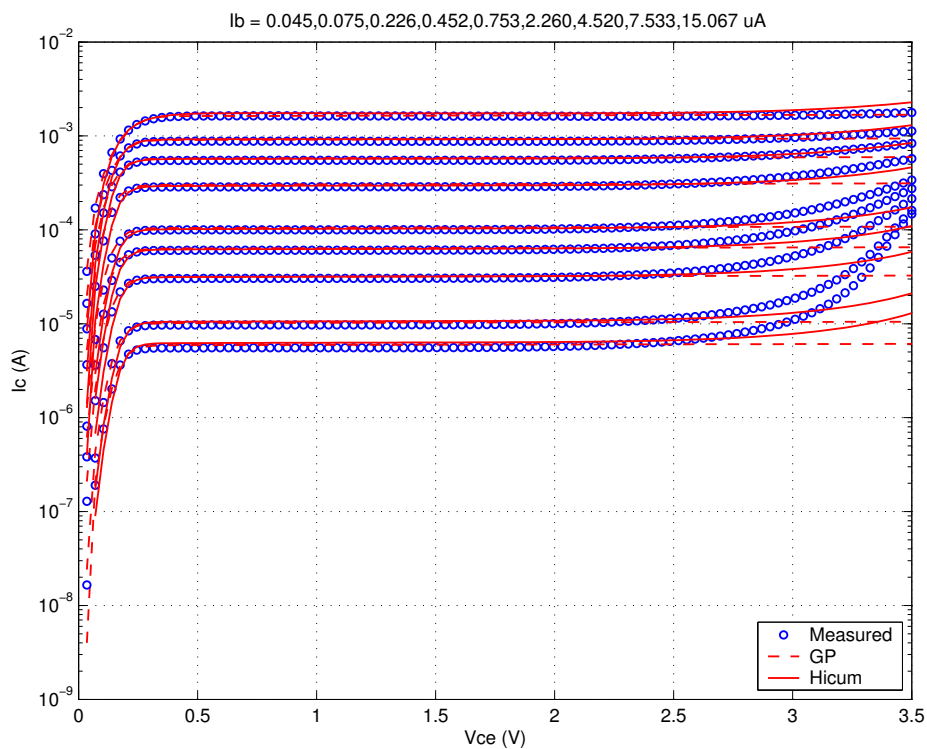


FIGURE 4.45 FT vs. IC: LV 0.2x4.52x1_122

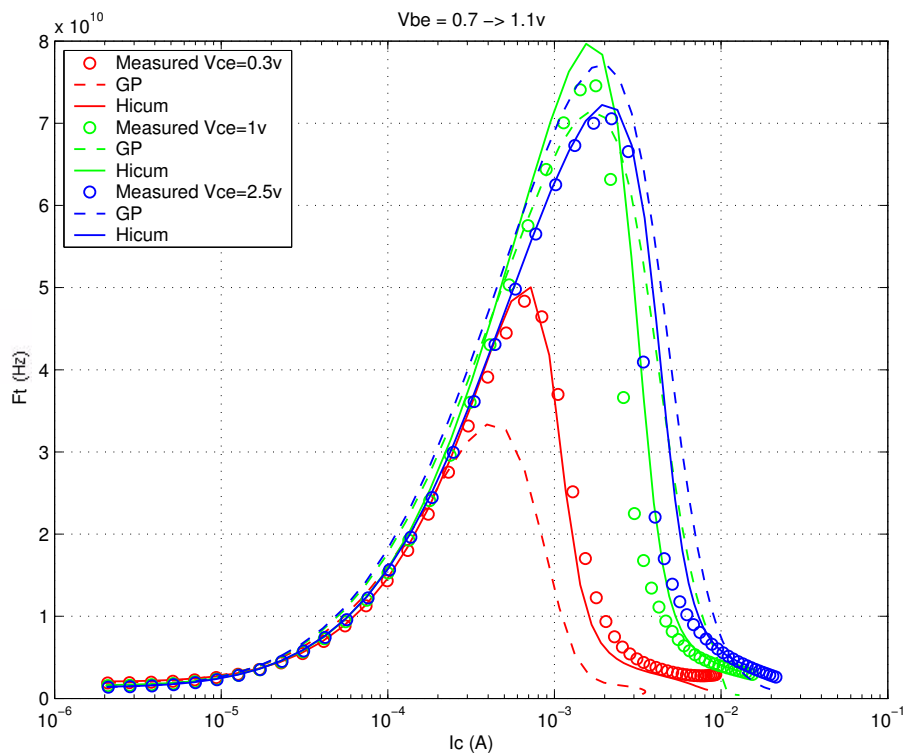
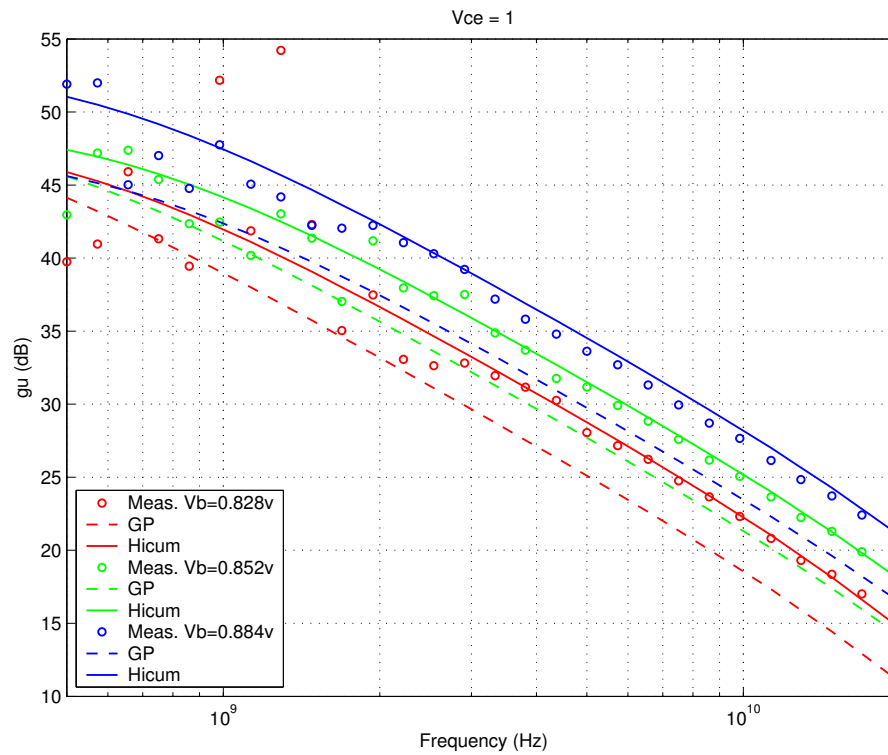


FIGURE 4.46 Power Gain vs. Freq: LV 0.2x4.52x1_122



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FIGURE 4.47 Y-parameters vs. FREQ: LV 0.2x4.52x1_122

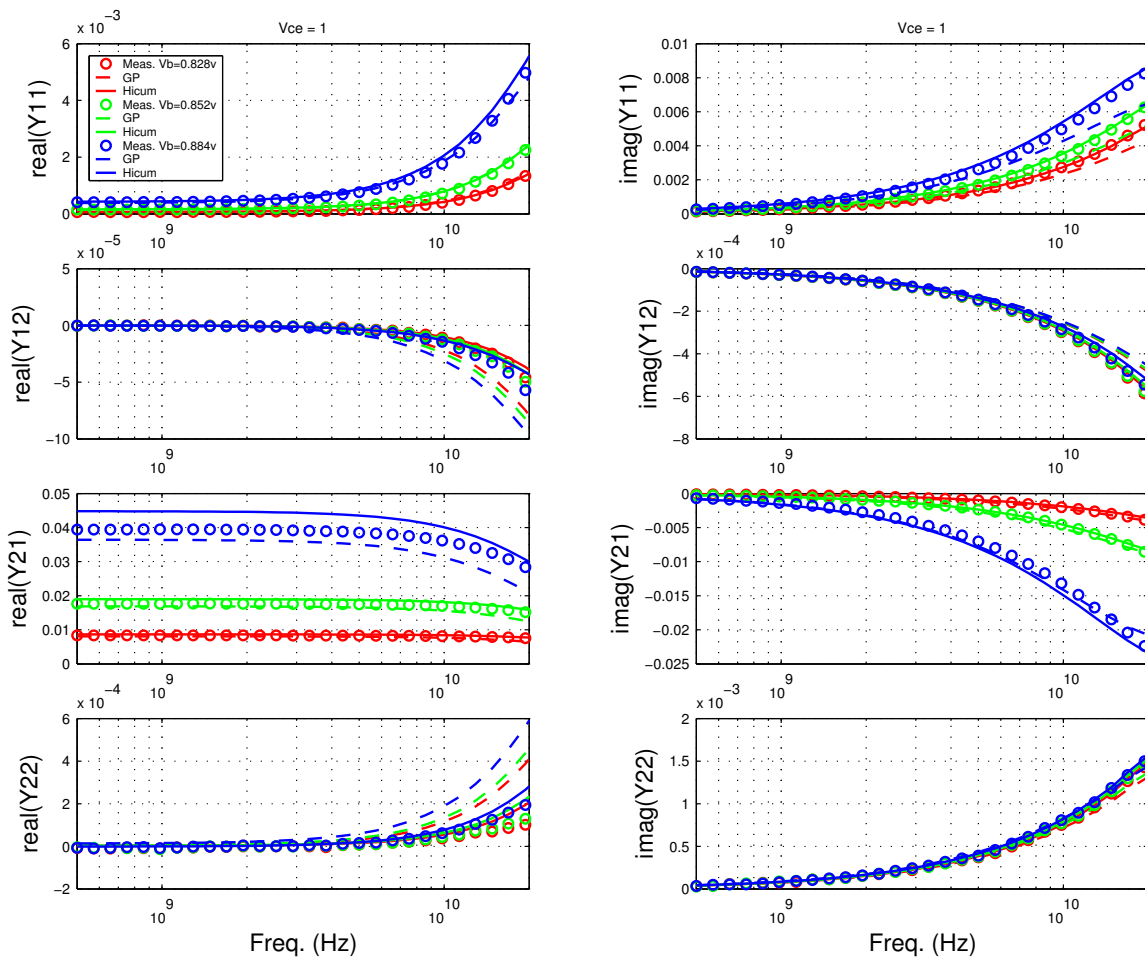


FIGURE 4.48 Gummel Plot LV 0.2x10.16x1_122

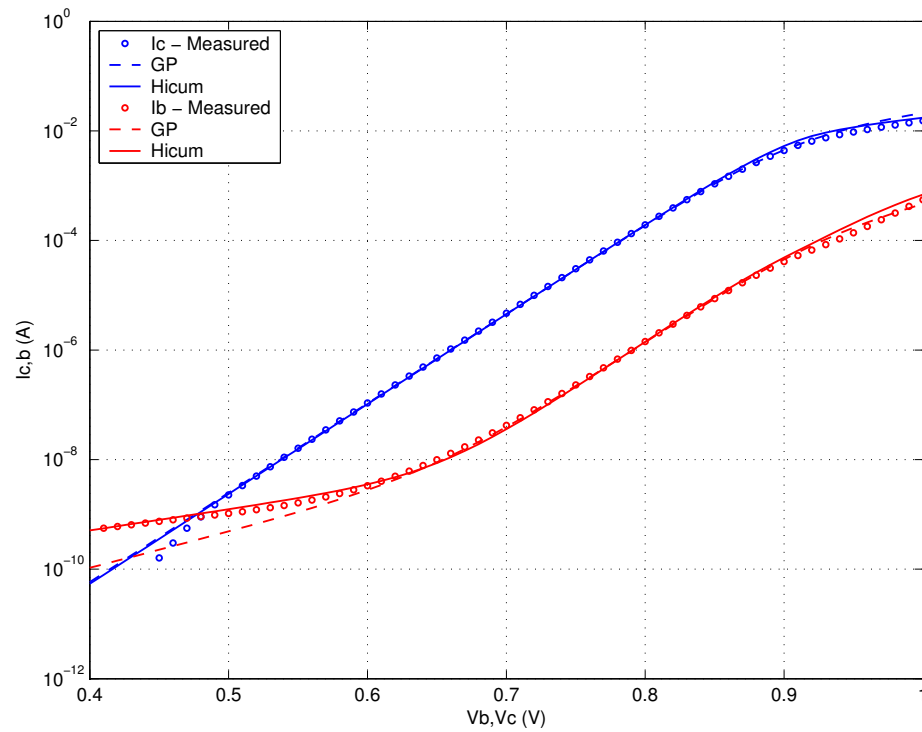
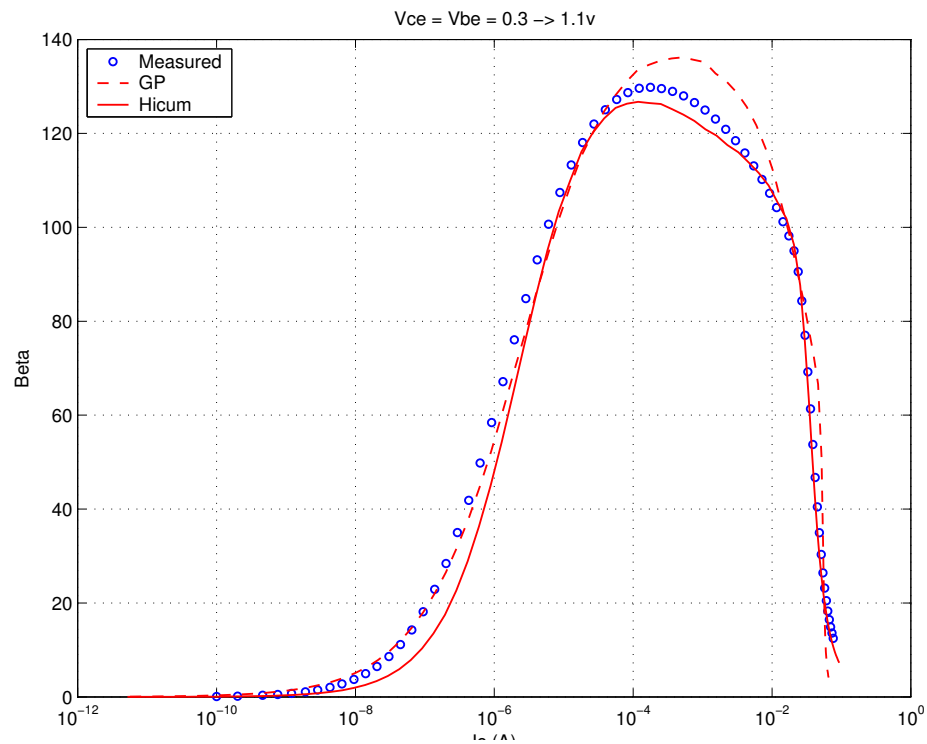
FIGURE 4.49 Beta vs. I_c : LV 0.2x10.16x1_122

FIGURE 4.50 I_C vs. V_{CE} at constant I_B : LV 0.2x10.16x1_122

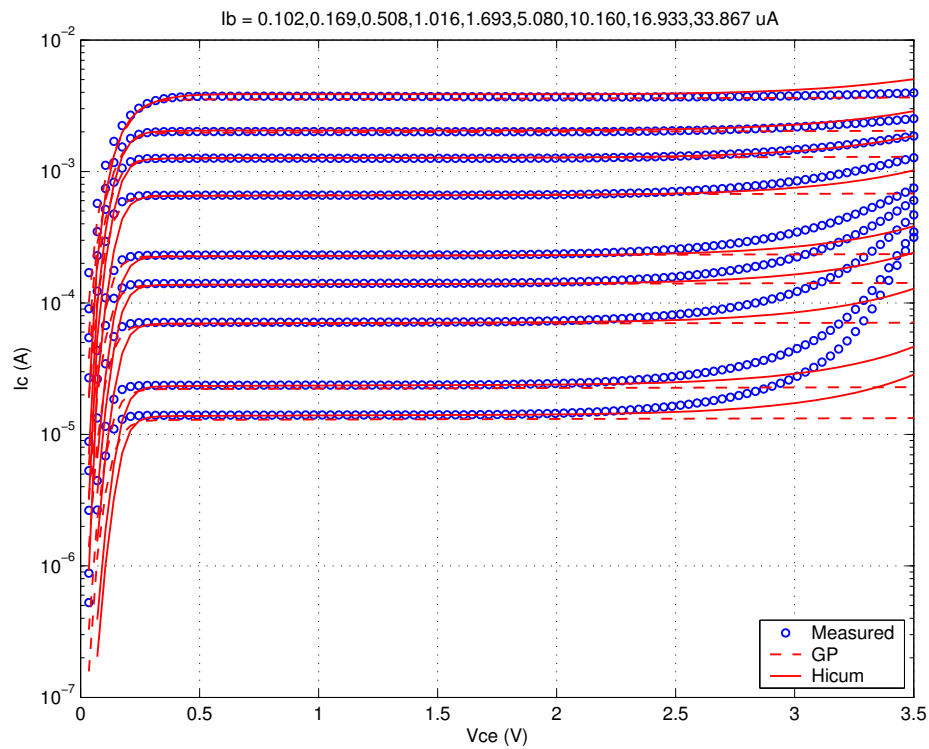


FIGURE 4.51 f_T vs. I_C : LV 0.2x10.16x1_122

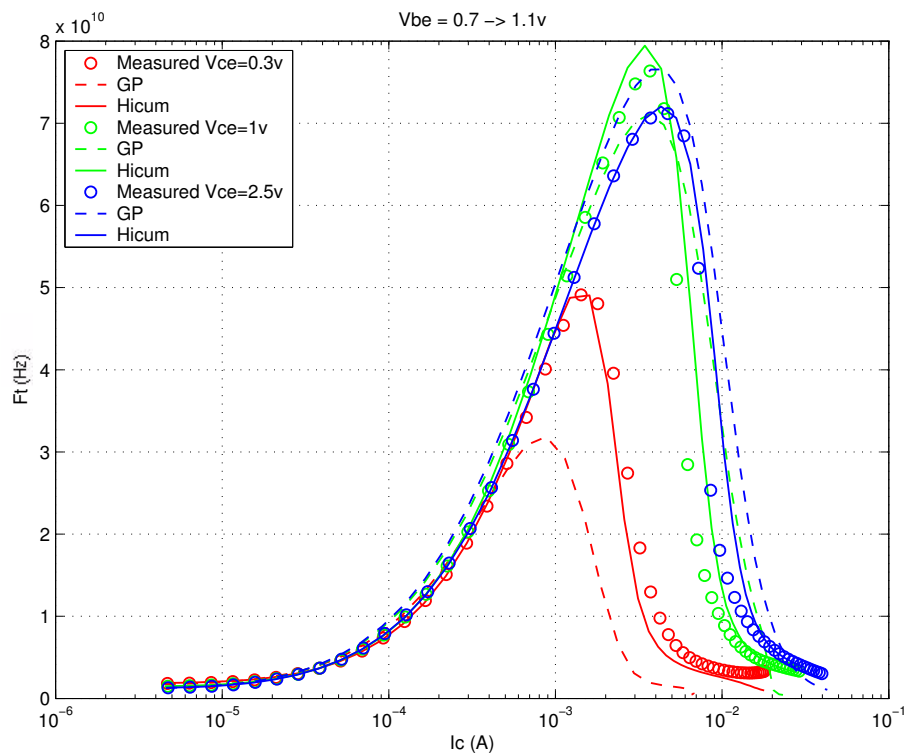
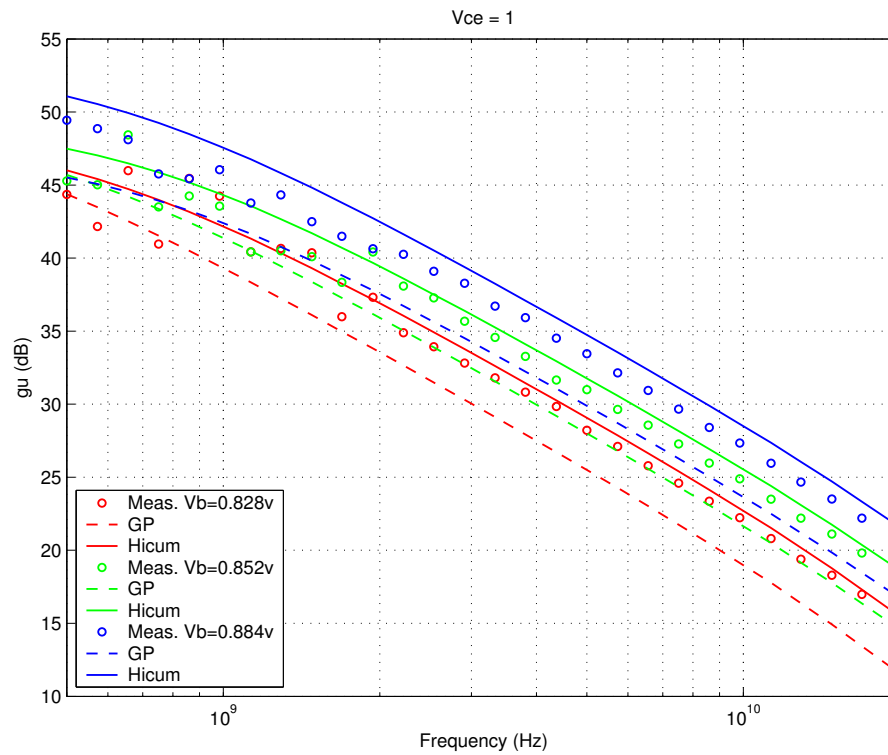


FIGURE 4.52 Power Gain vs. Freq: LV 0.2x10.16x1_122



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FIGURE 4.53 Y-parameters vs. FREQ: LV 0.2x10.16x1_122

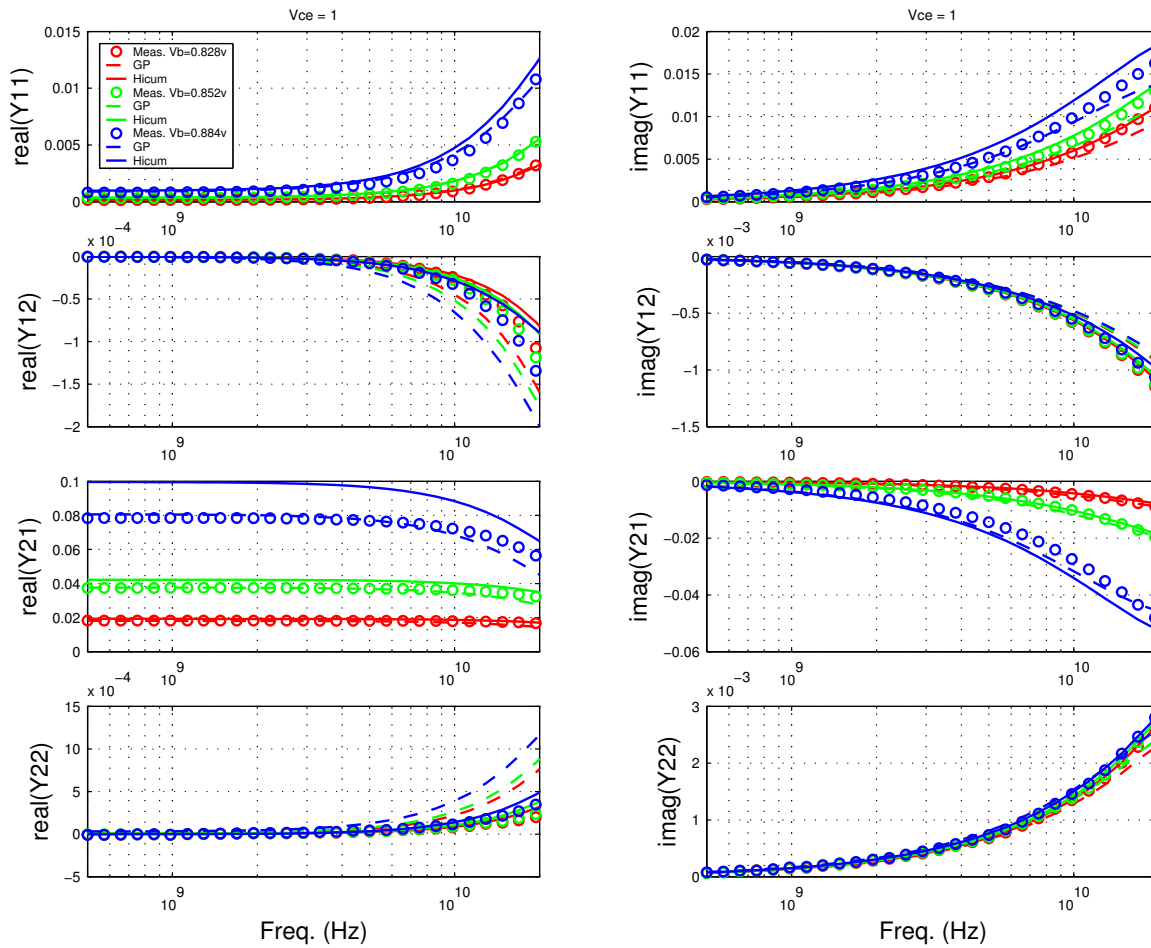
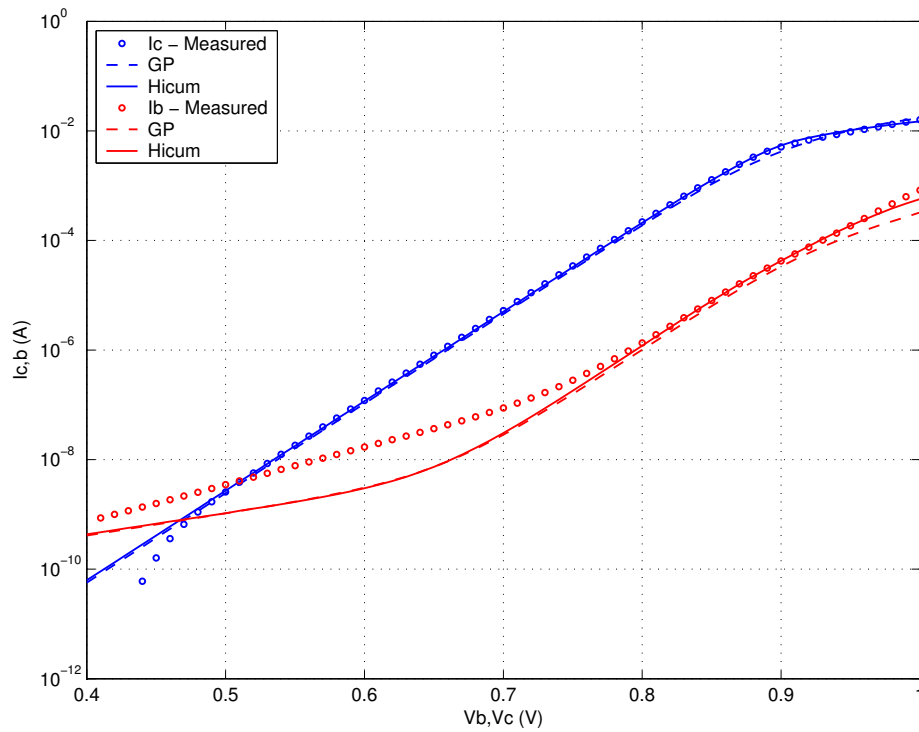


FIGURE 4.54 Gummel Plot LV 0.6x4.52x1_122



Note: Discrepancy at low voltages due to die-specific increase in non-ideal base current

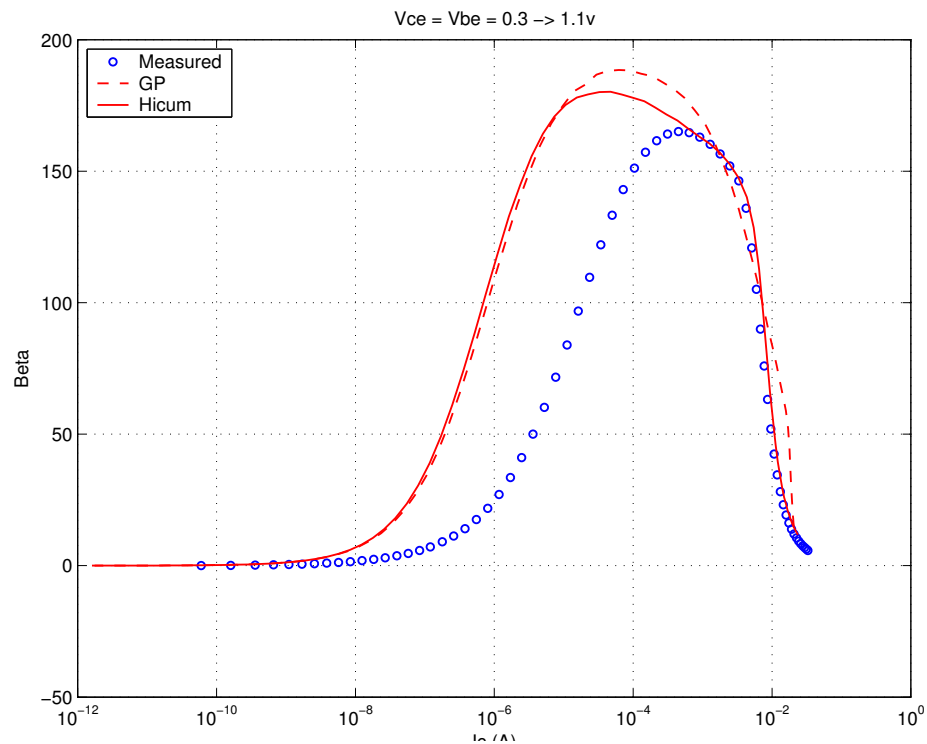
FIGURE 4.55 Beta vs. I_c : LV 0.6x4.52x1_122

FIGURE 4.56 IC vs. VCE at constant IB: LV 0.6x4.52x1_122

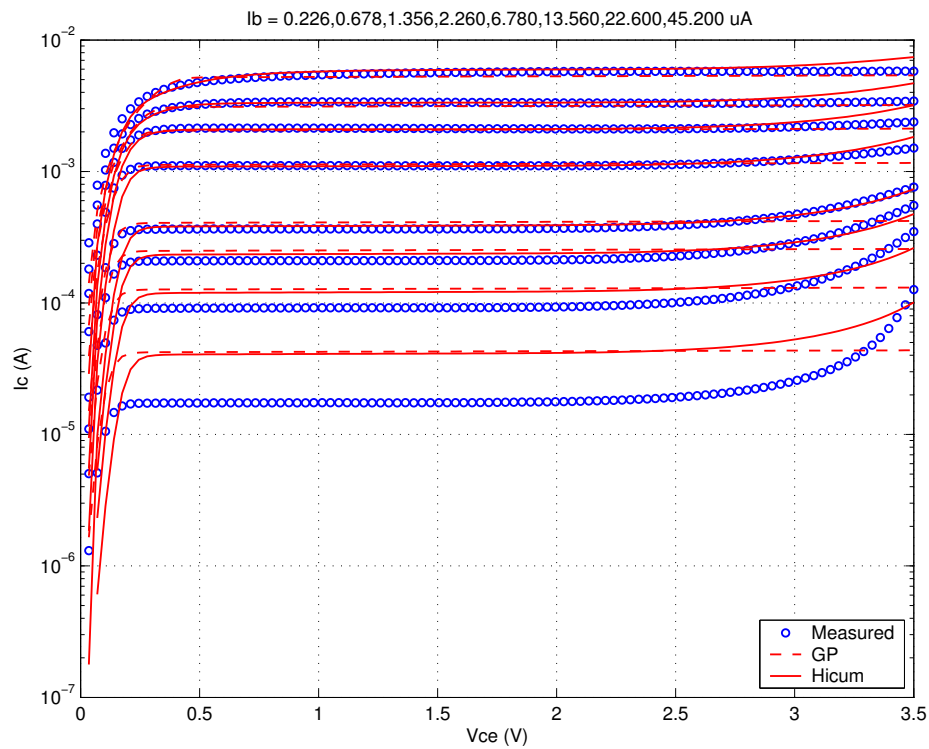


FIGURE 4.57 FT vs. IC: LV 0.6x4.52x1_122

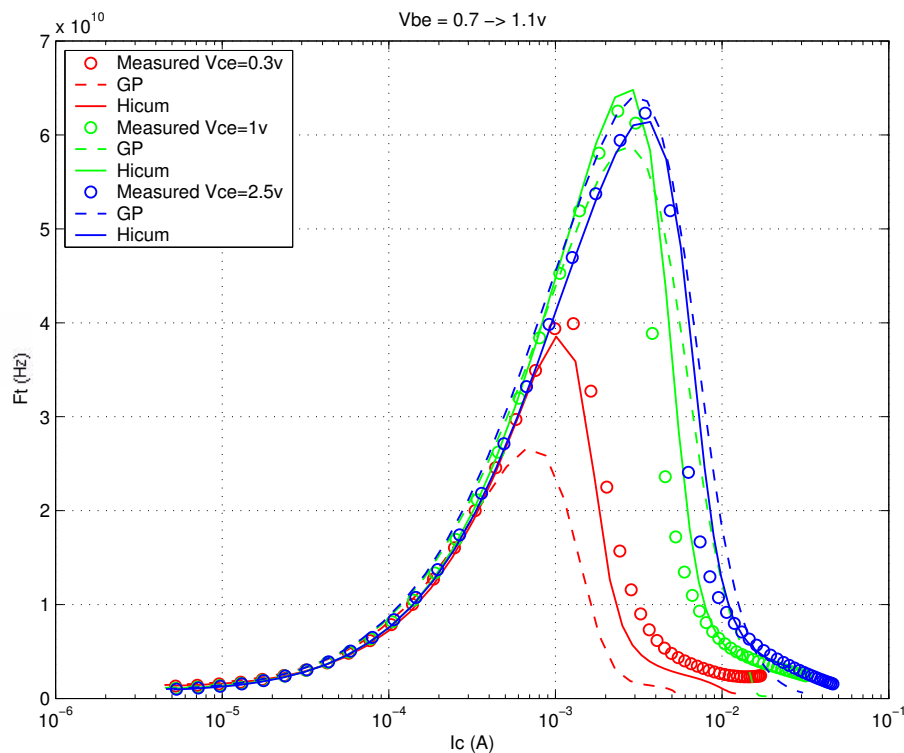
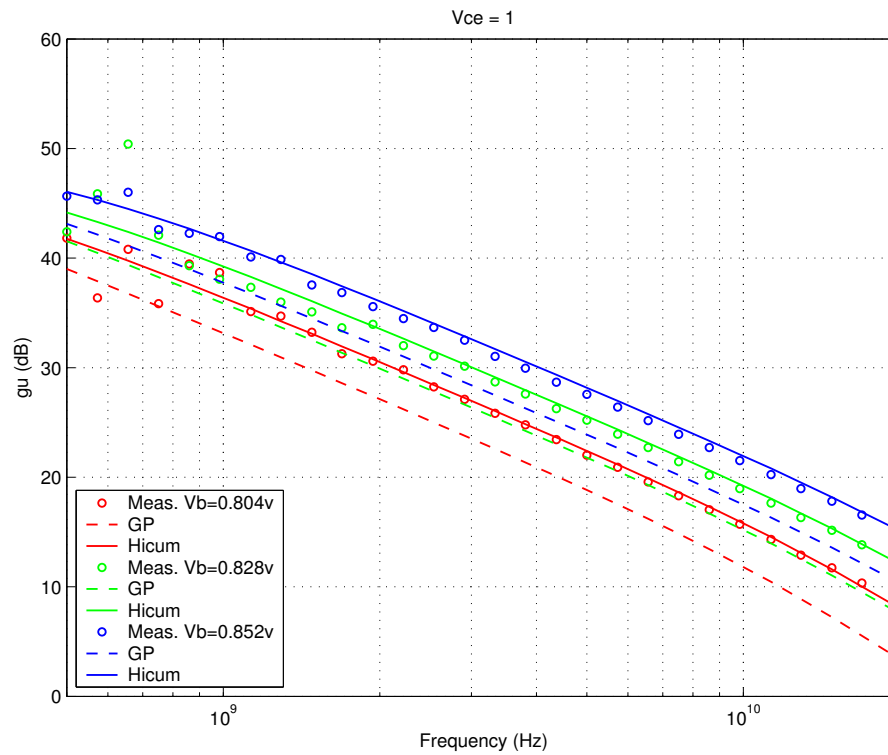


FIGURE 4.58 Power Gain vs. Freq: LV 0.6x4.52x1_122



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FIGURE 4.59 Y-parameters vs. FREQ: LV 0.6x4.52x1_122

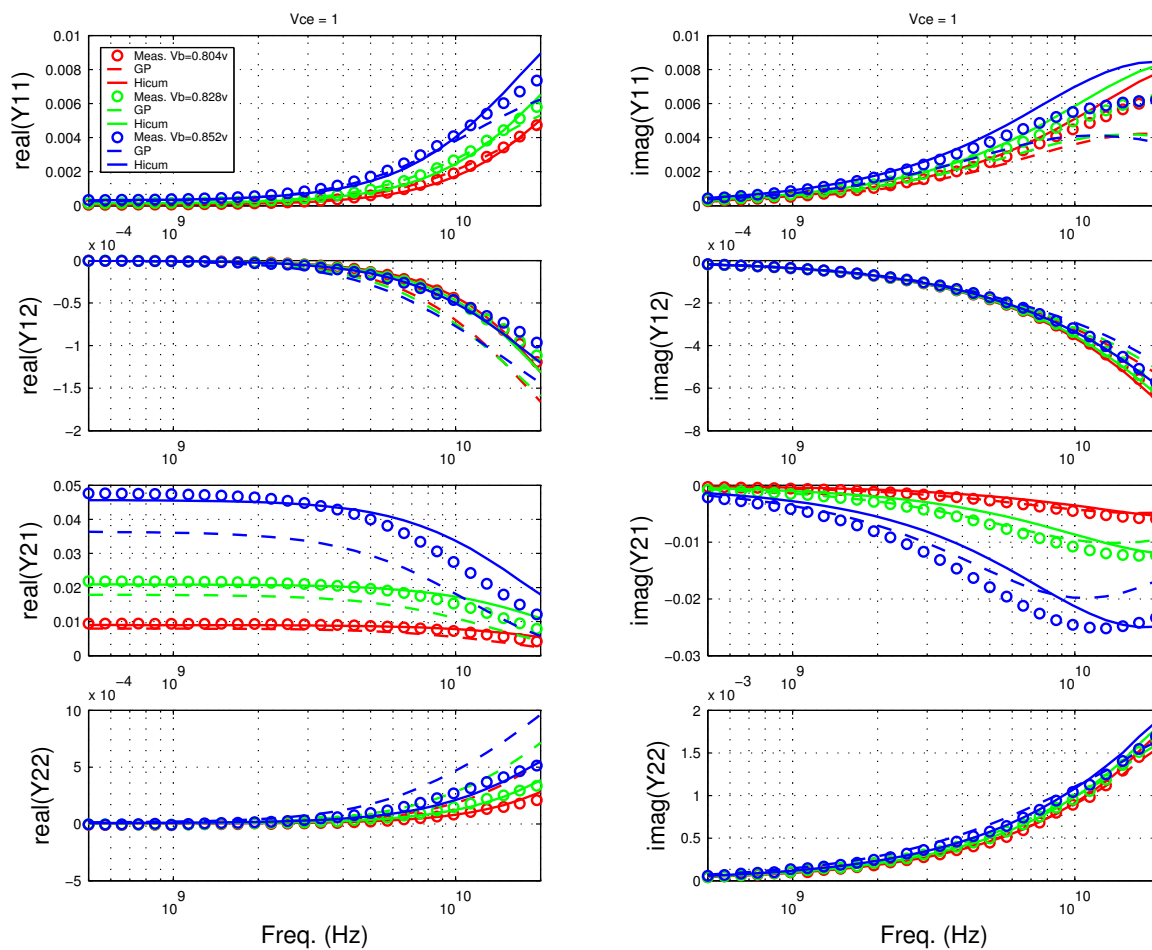


FIGURE 4.60 Gummel Plot LV 0.6x10.16x1_122

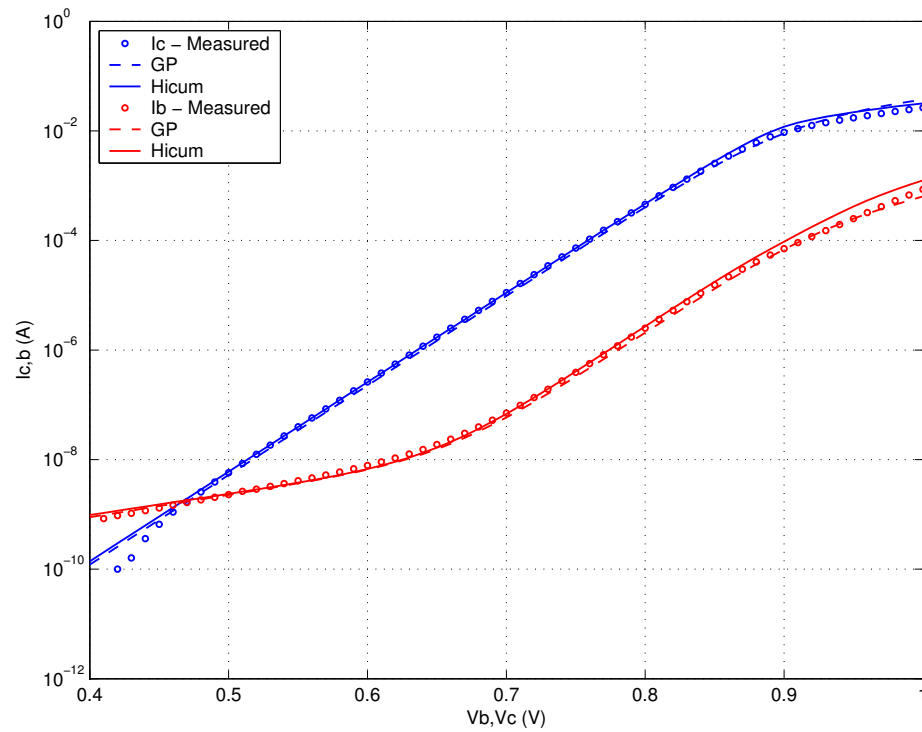
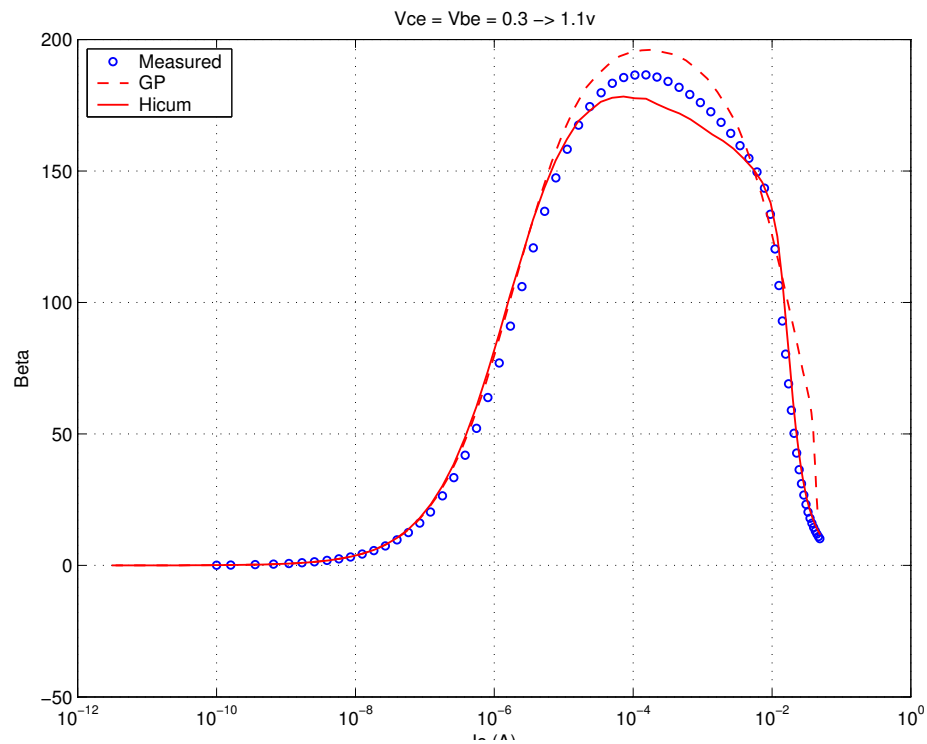
FIGURE 4.61 Beta vs. I_c : LV 0.6x10.16x1_122

FIGURE 4.62 IC vs. VCE at constant IB: LV 0.6x10.16x1_122

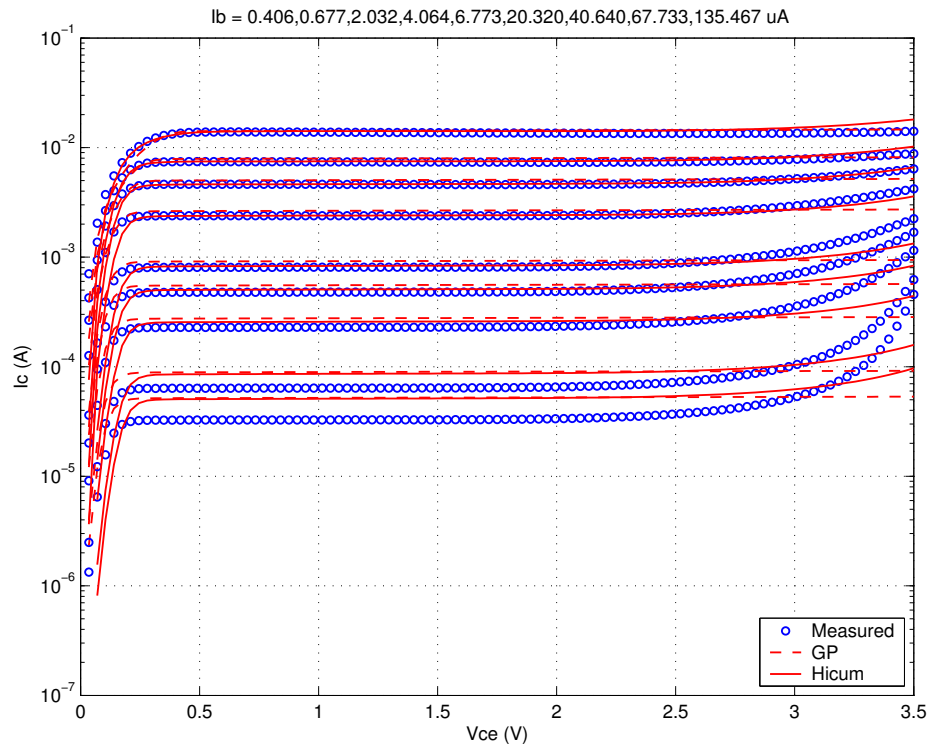


FIGURE 4.63 FT vs. IC: LV 0.6x10.16x1_122

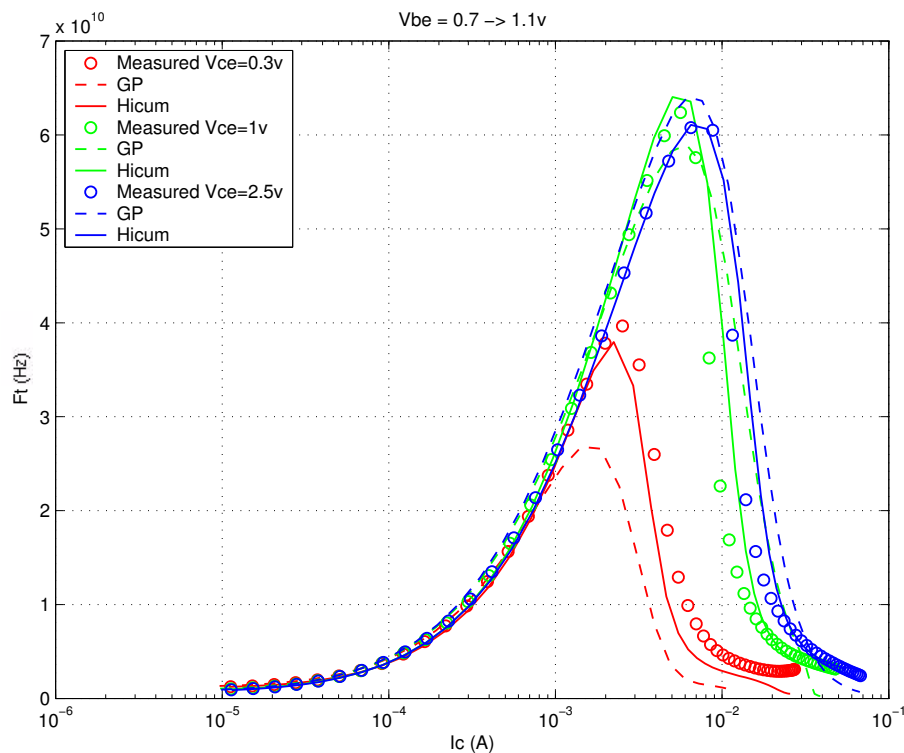
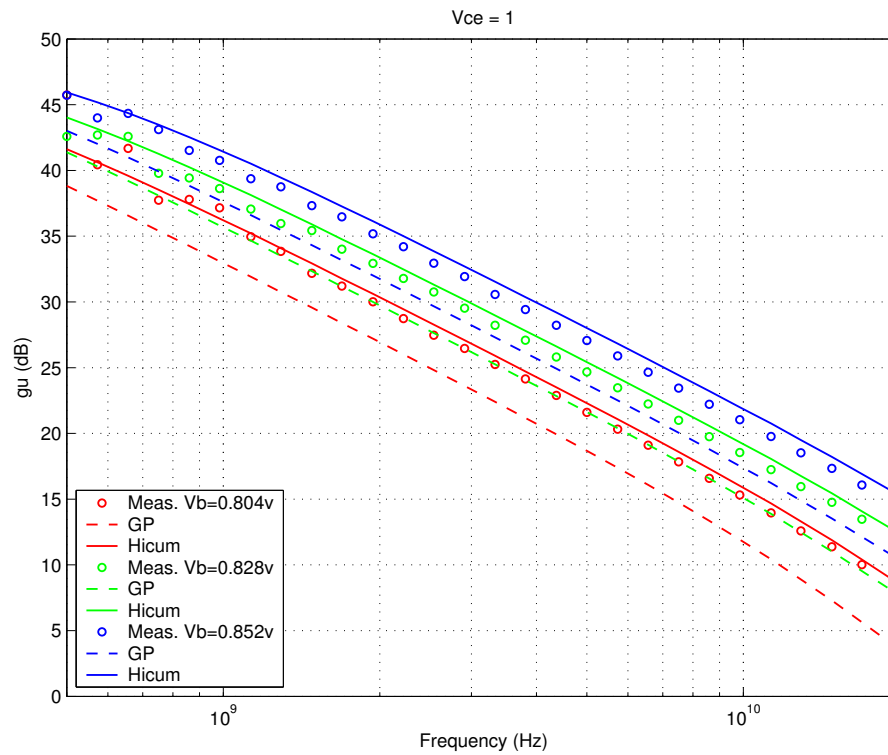


FIGURE 4.64 Power Gain vs. Freq: LV 0.6x10.16x1_122



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FIGURE 4.65 Y-parameters vs. FREQ: LV 0.6x10.16x1_122

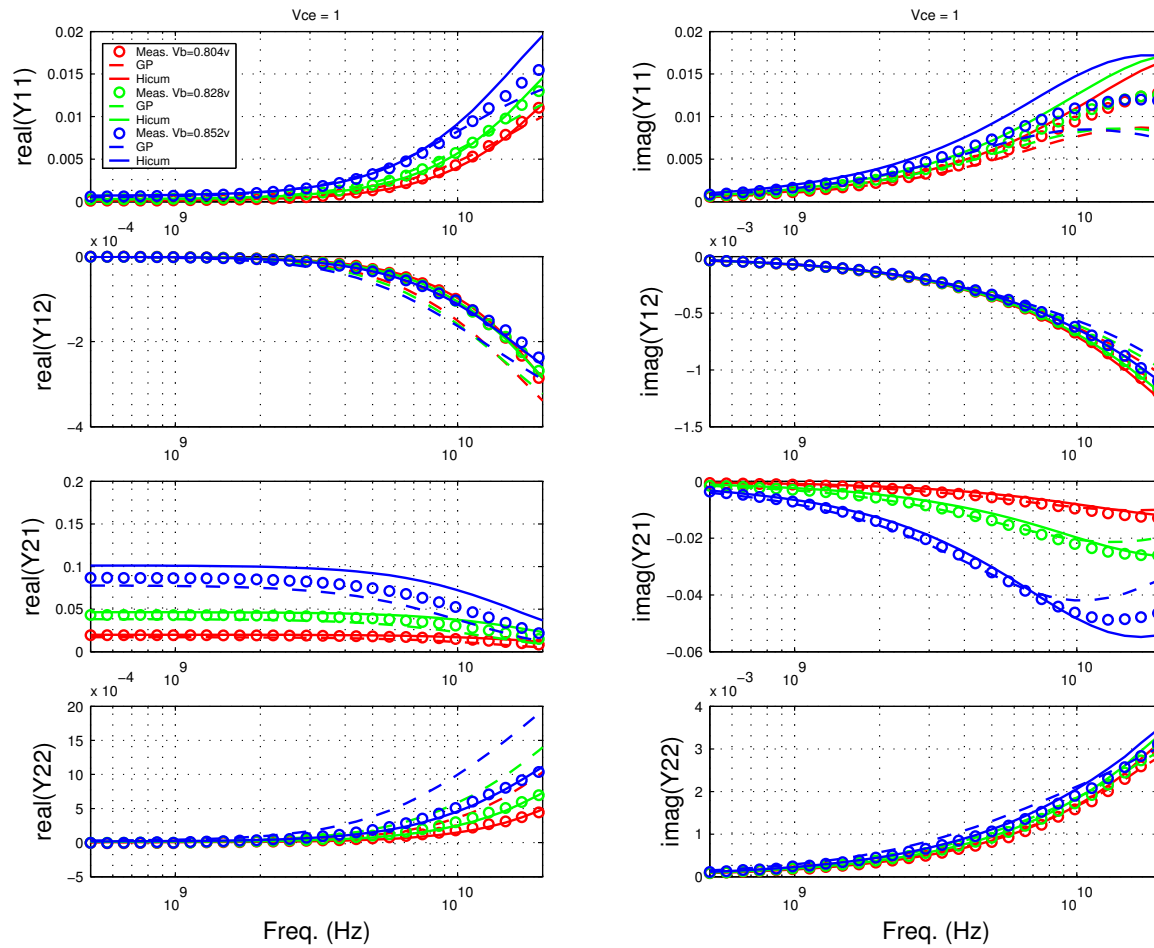


FIGURE 4.66 Gummel Plot LV 0.9x4.52x1_122

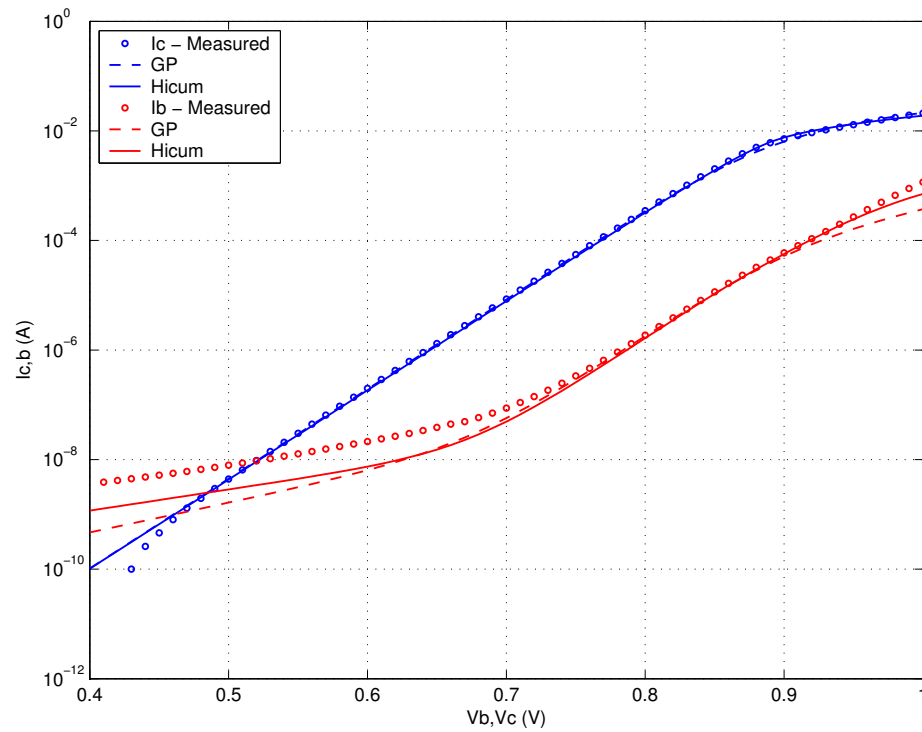
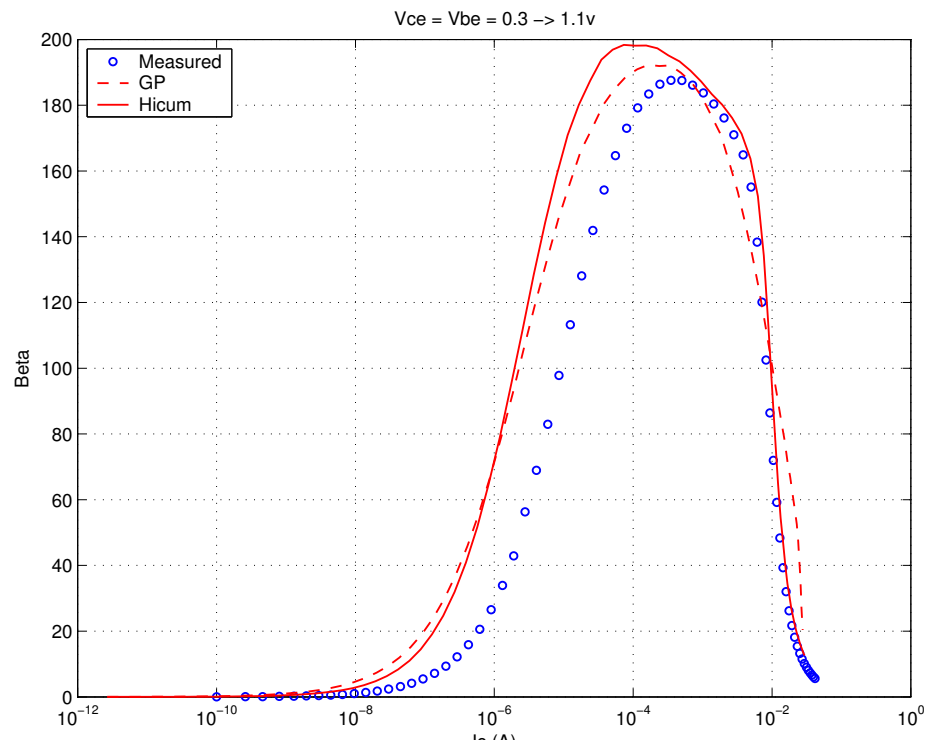
FIGURE 4.67 Beta vs. I_c : LV 0.9x4.52x1_122

FIGURE 4.68 IC vs. VCE at constant IB: LV 0.9x4.52x1_122

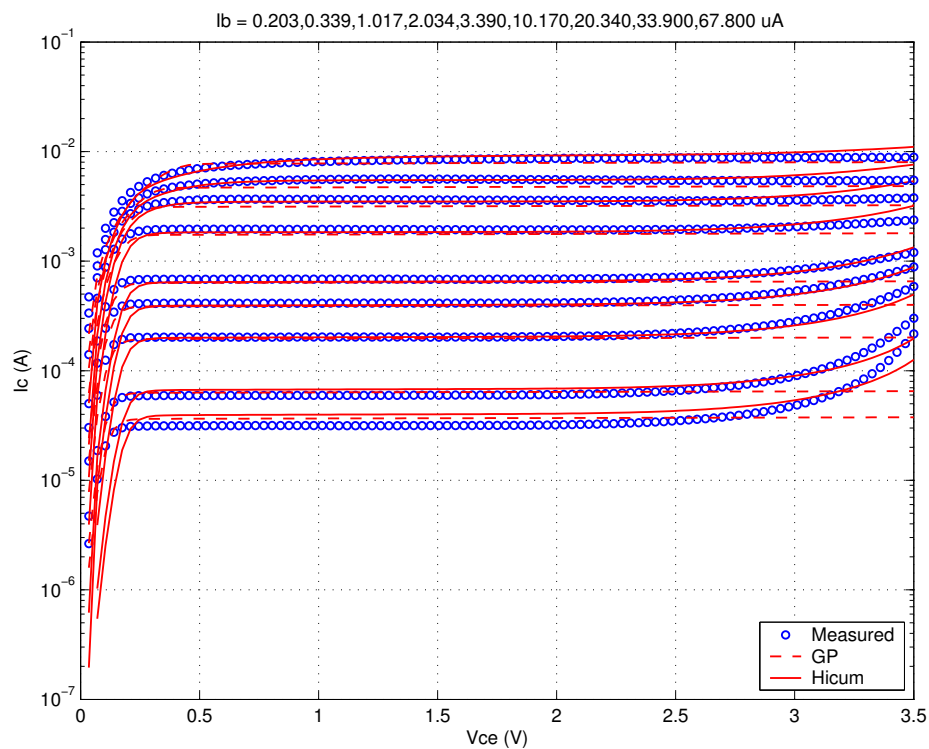


FIGURE 4.69 FT vs. IC: LV 0.9x4.52x1_122

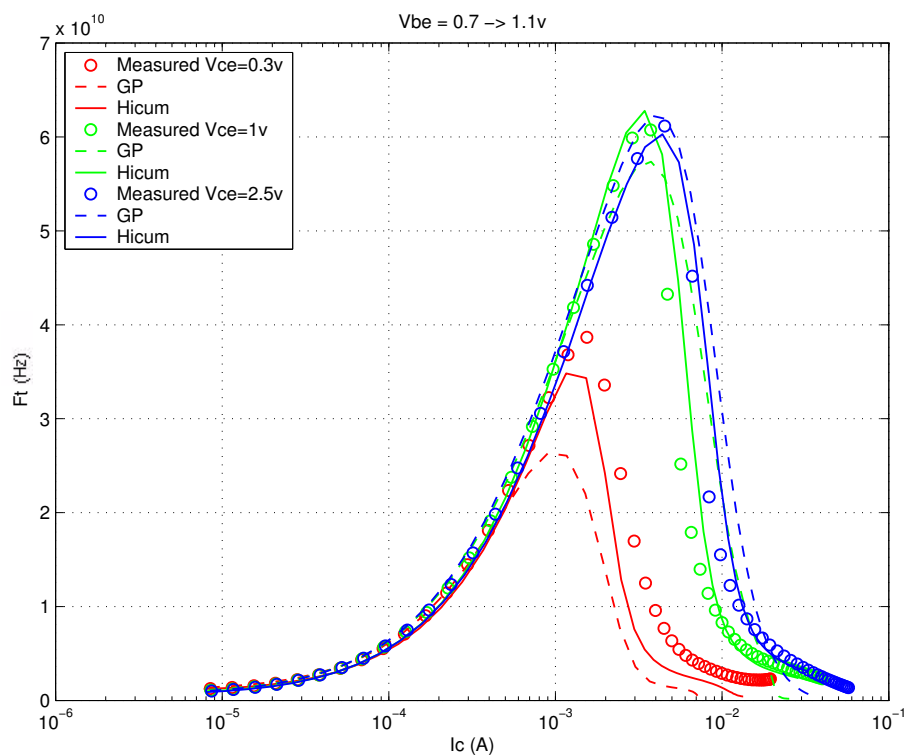
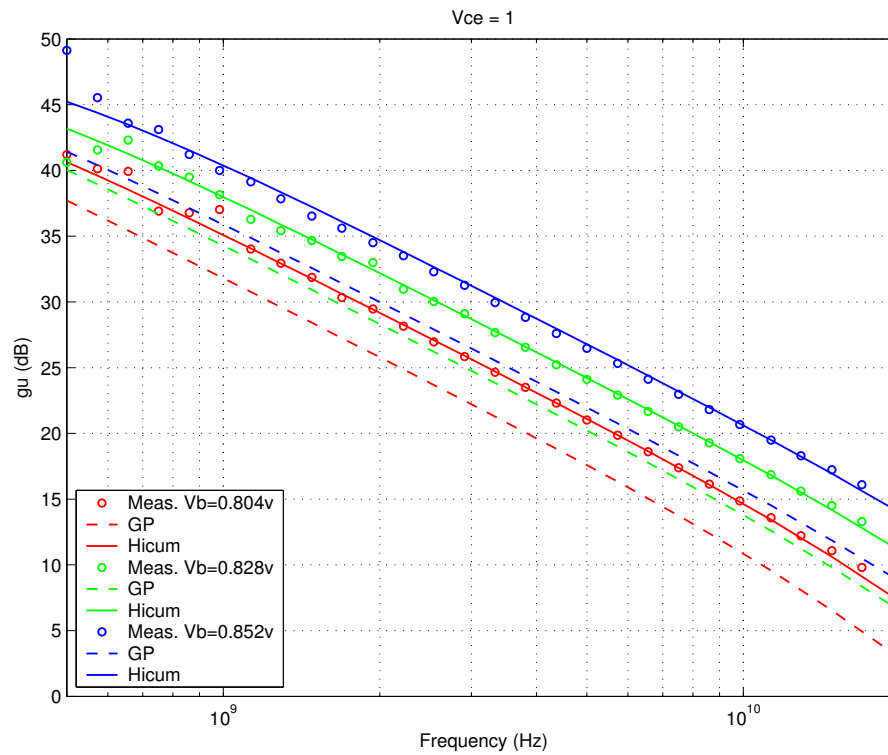


FIGURE 4.70 Power Gain vs. Freq: LV 0.9x4.52x1_122



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FIGURE 4.71 Y-parameters vs. FREQ: LV 0.9x4.52x1_122

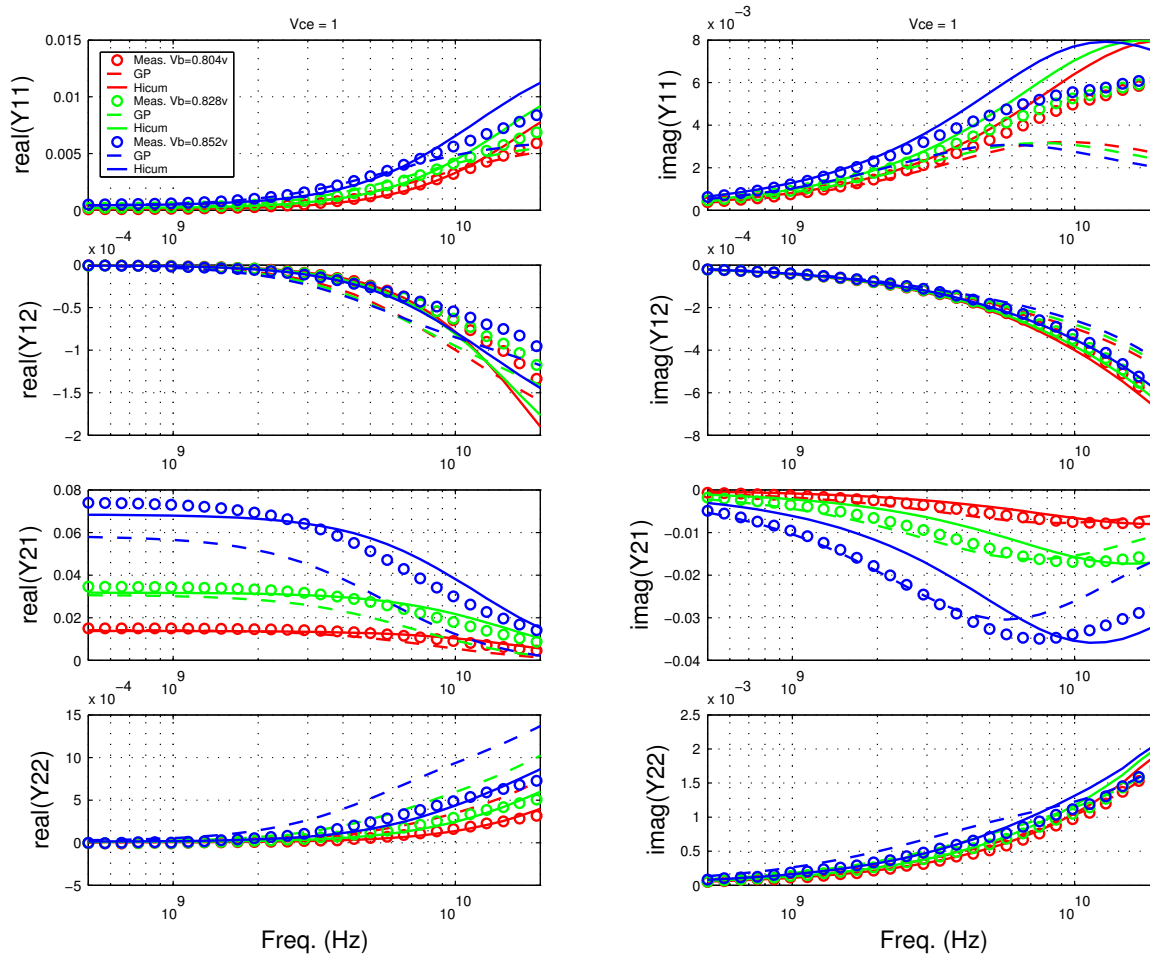


FIGURE 4.72 Gummel Plot LV 0.9x10.16x1_122

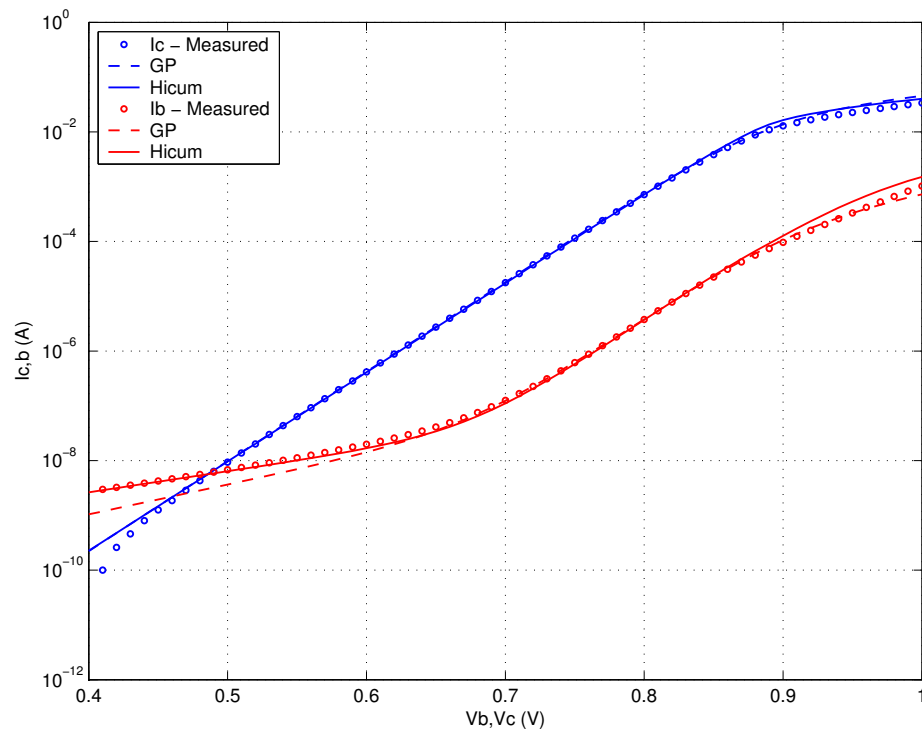
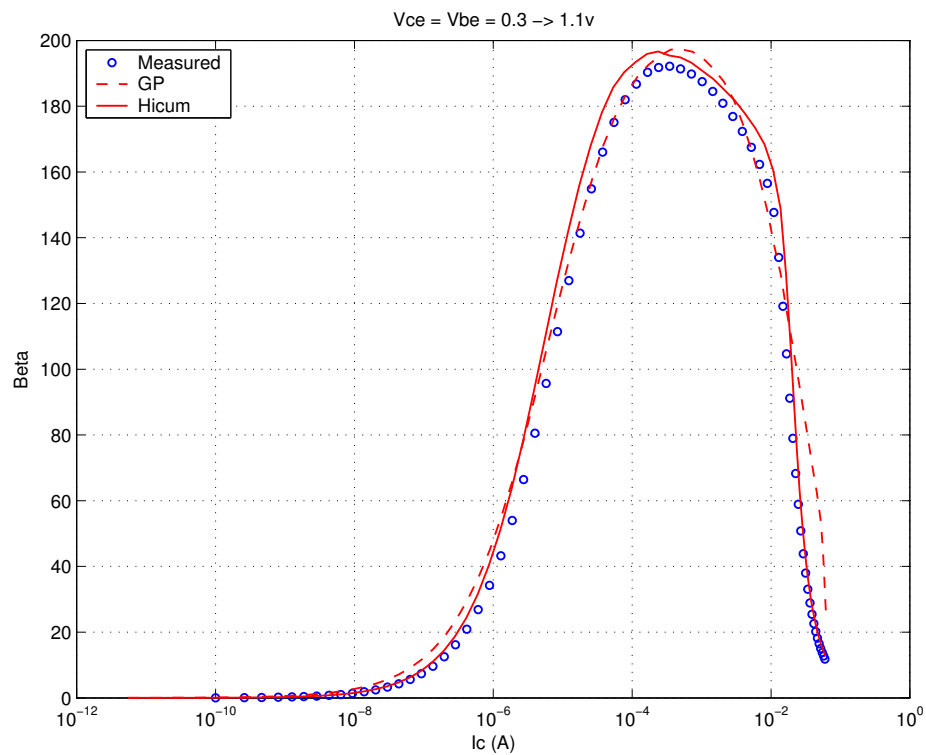
FIGURE 4.73 Beta vs. I_c : LV 0.9x10.16x1_122

FIGURE 4.74 IC vs. VCE at constant IB: LV 0.9x10.16x1_122

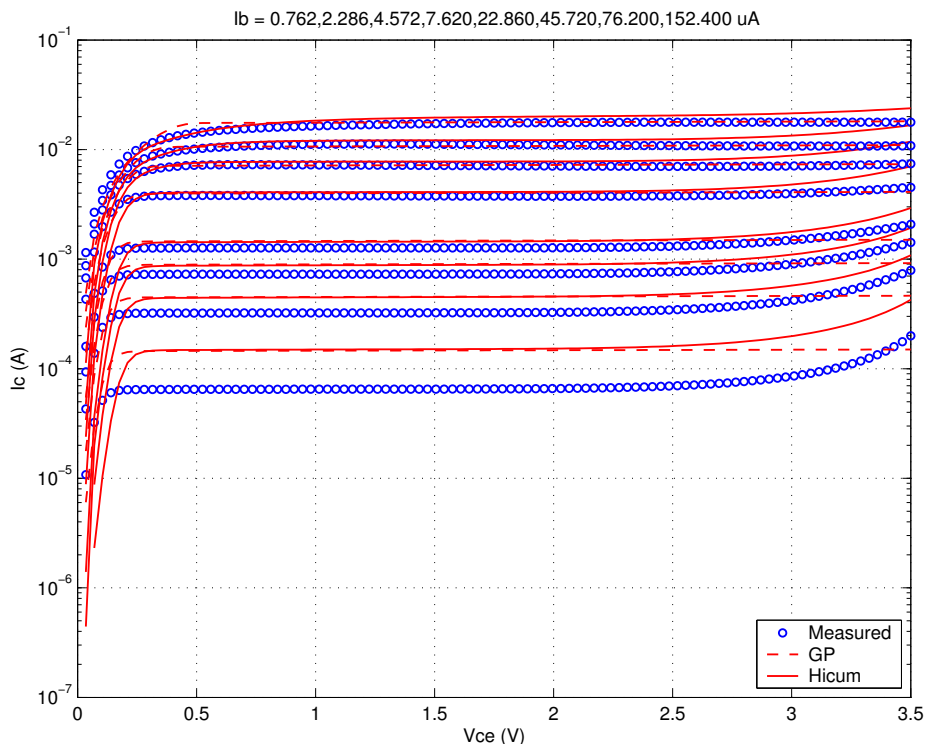


FIGURE 4.75 FT vs. IC: LV 0.9x10.16x1_122

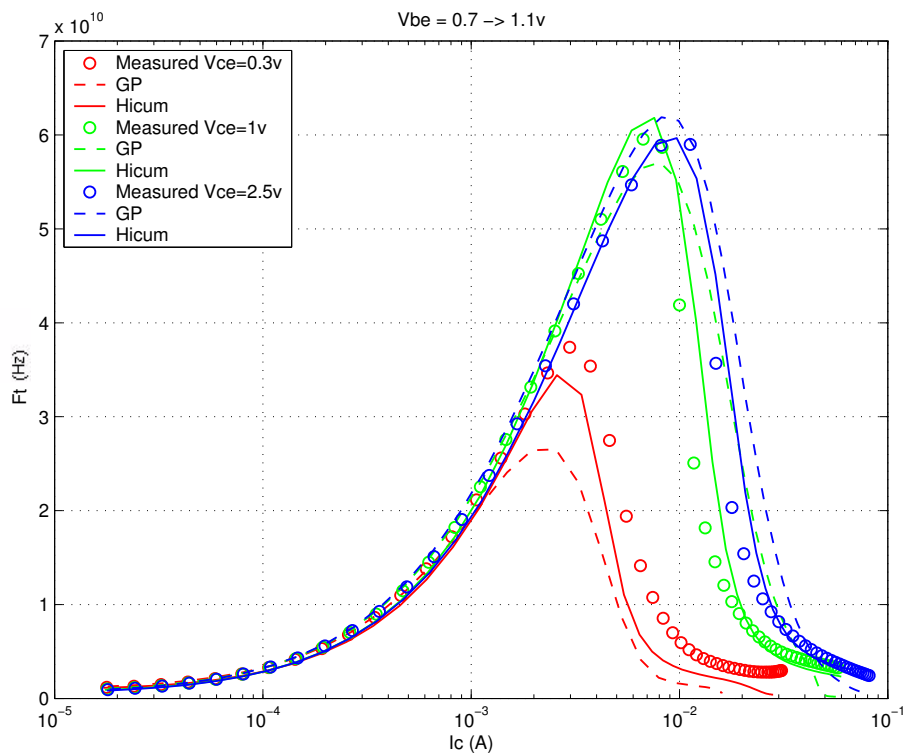
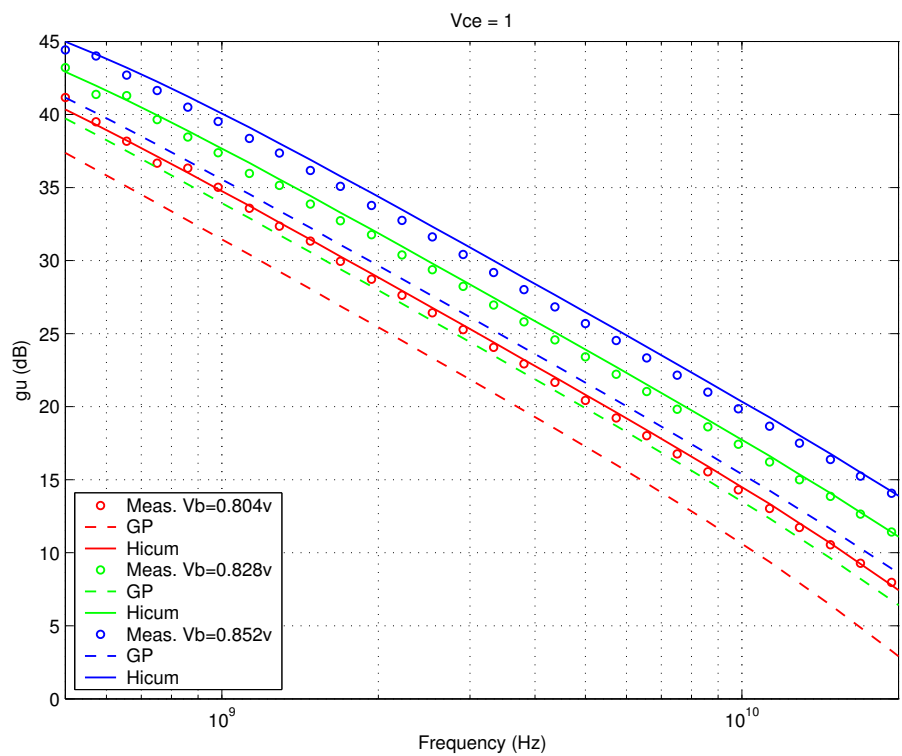


FIGURE 4.76 Power Gain vs. Freq: LV 0.9x10.16x1_122



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FIGURE 4.77 Y-parameters vs. FREQ: LV 0.9x10.16x1_122

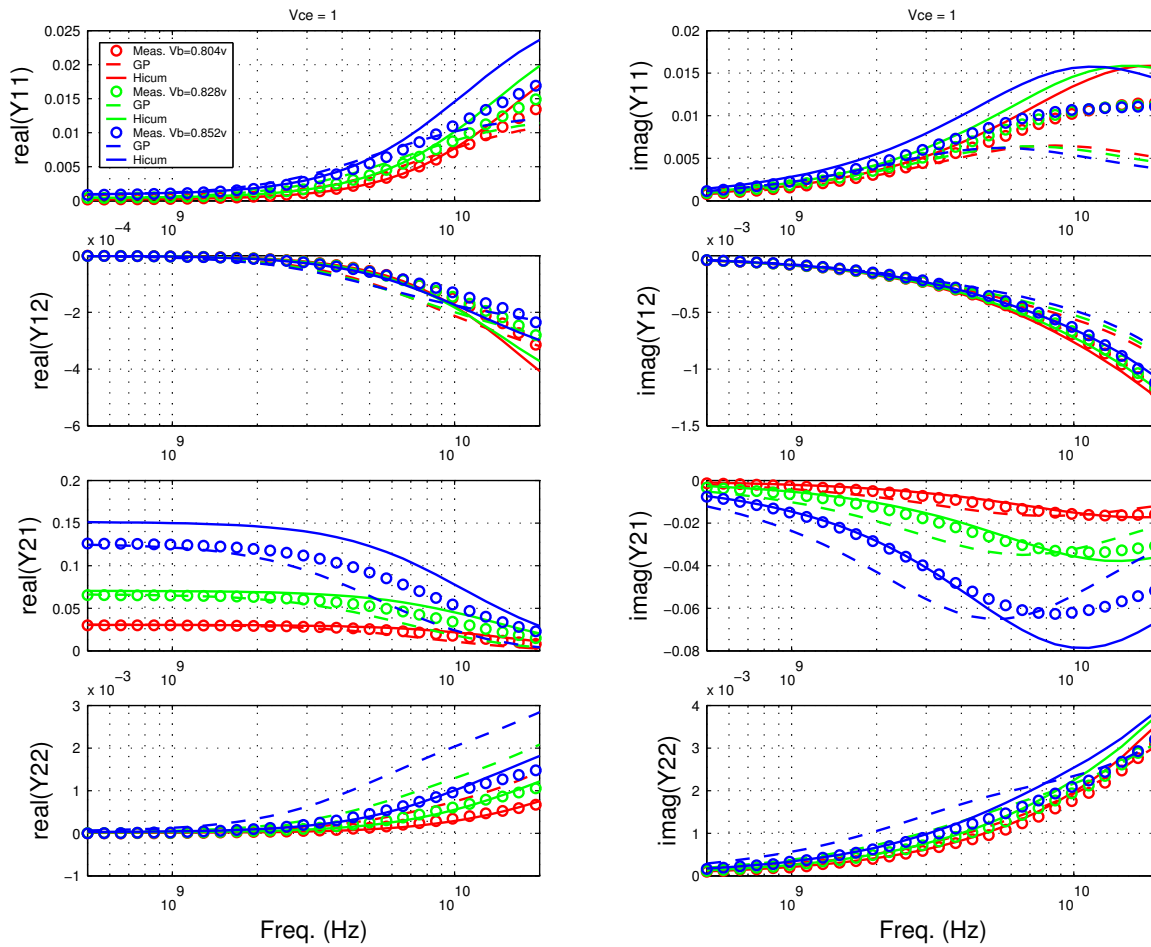


FIGURE 4.78 Gummel Plot: LV 0.2x10.16x1_452

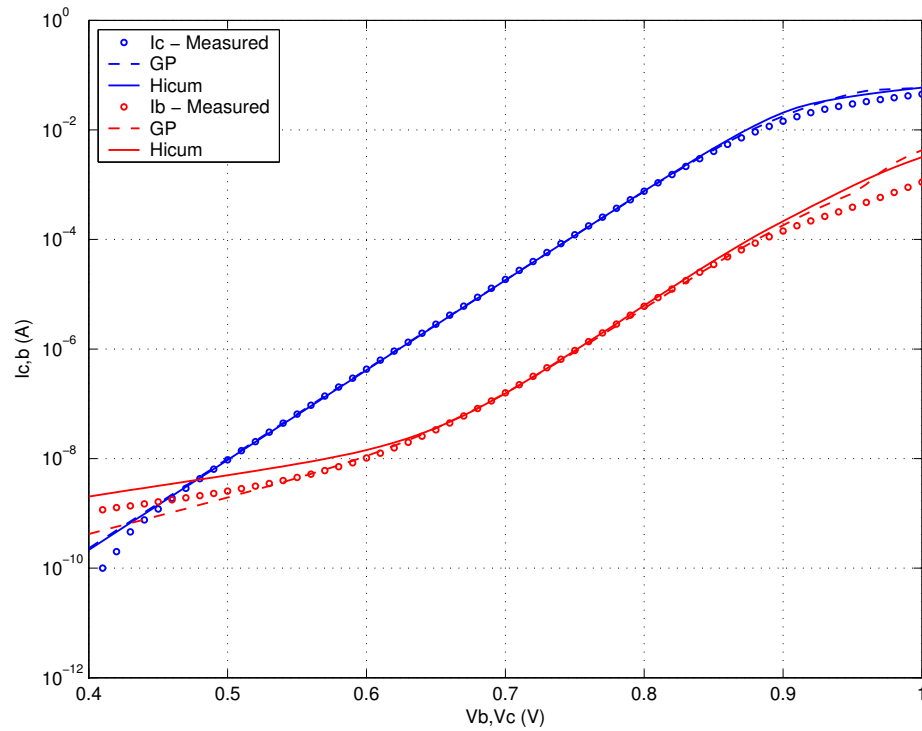
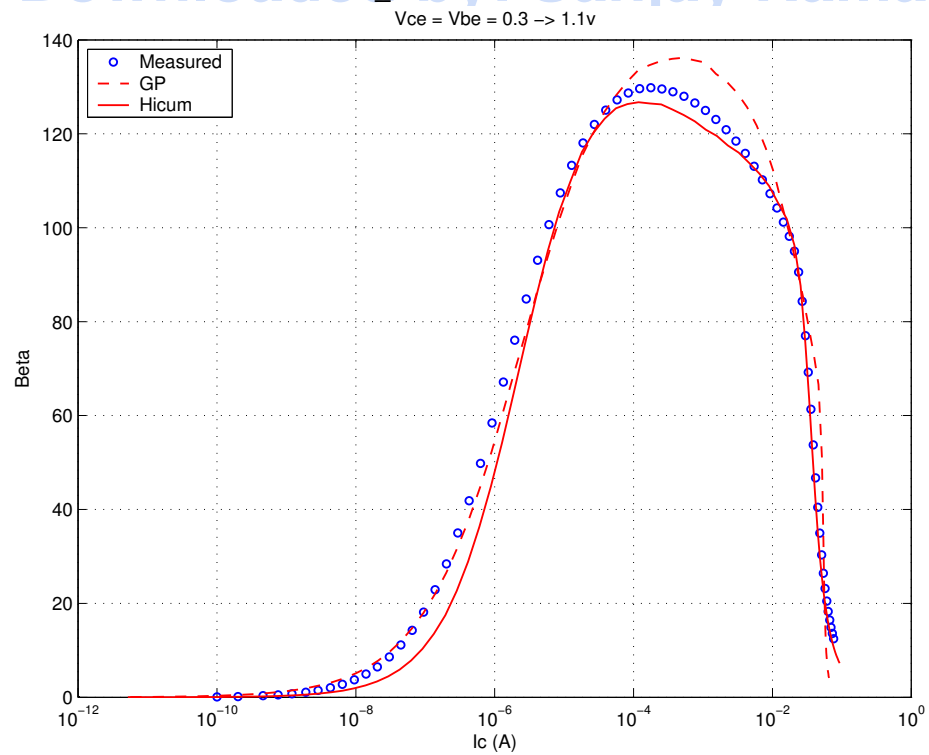
FIGURE 4.79 Beta vs. I_c : LV 0.2x10.16x1_452

FIGURE 4.80 IC vs. VCE at constant IB: LV 0.2x10.16x1_452

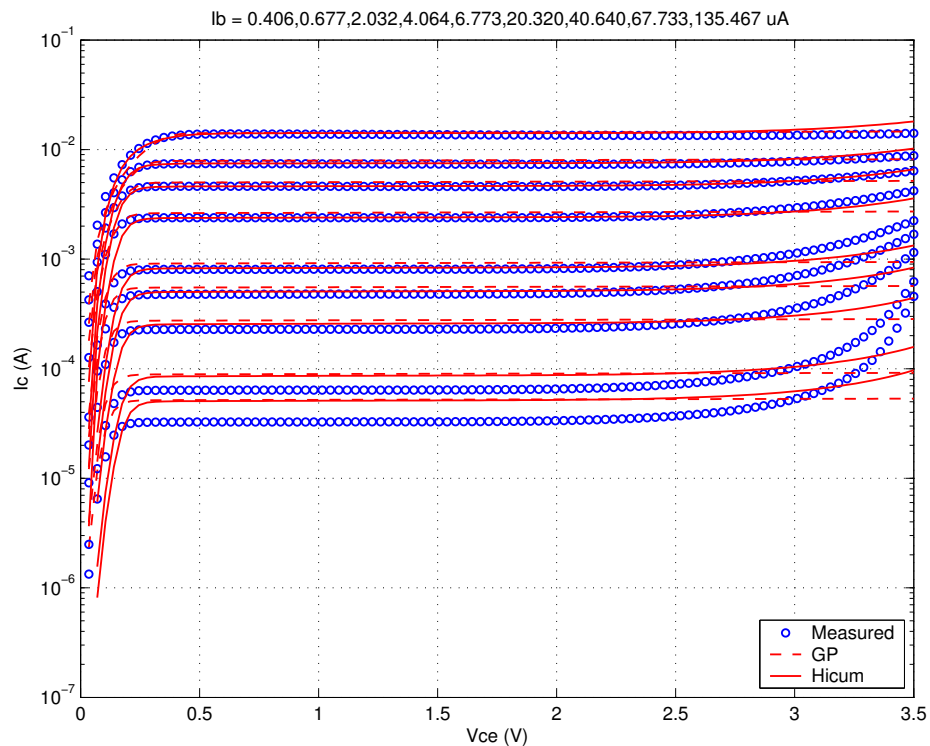


FIGURE 4.81 FT vs. IC: LV 0.2x10.16x1_452

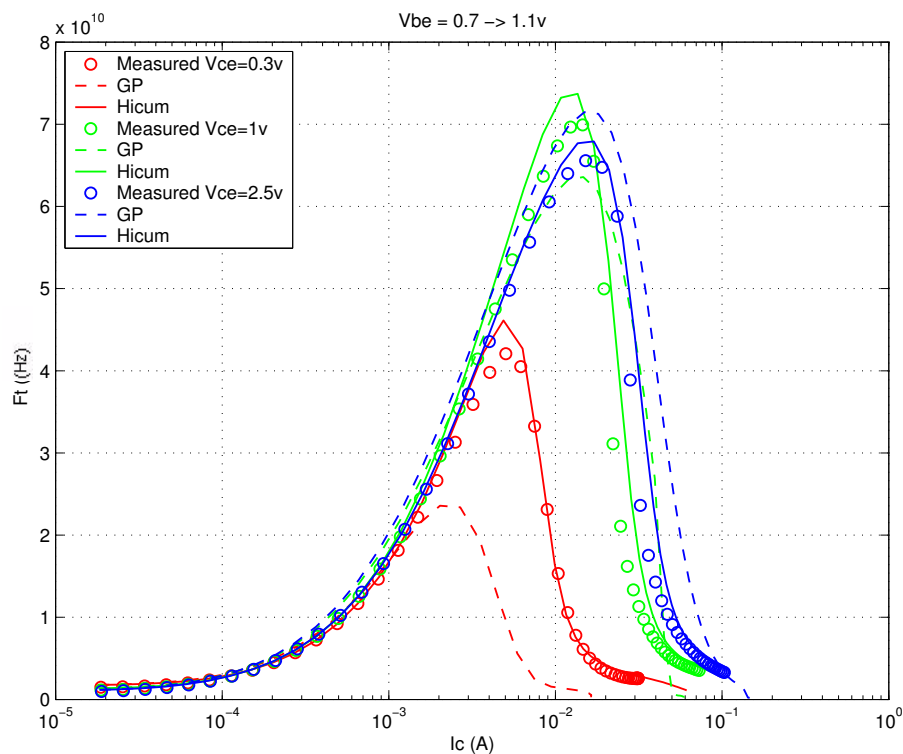
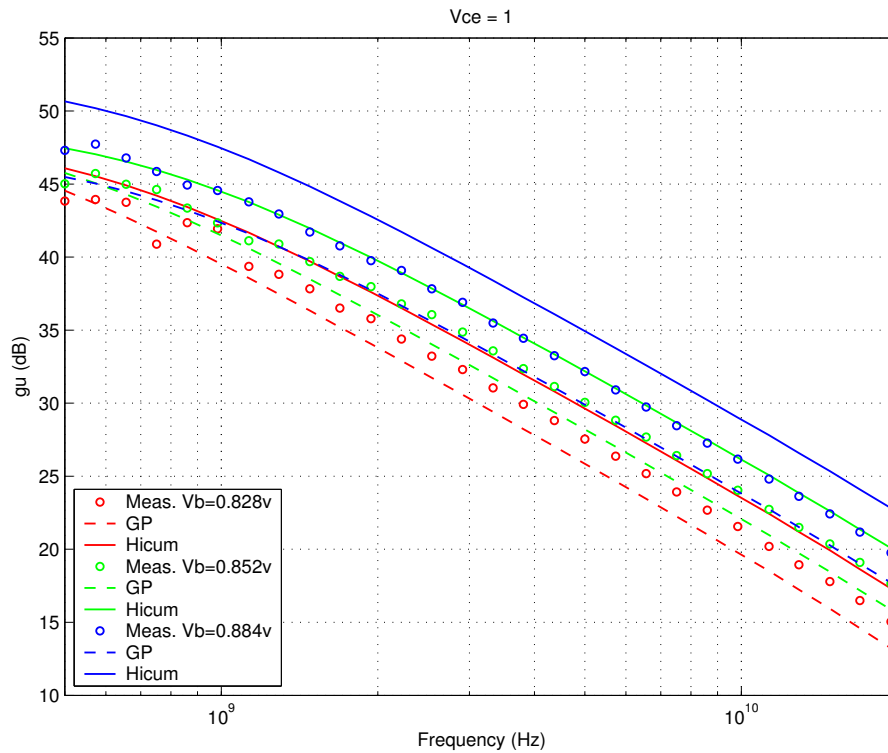


FIGURE 4.82 Power Gain vs. Freq: LV 0.2x10.16x1_452



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FIGURE 4.83 Y-parameters vs. FREQ: LV 0.2x10.16x1_452

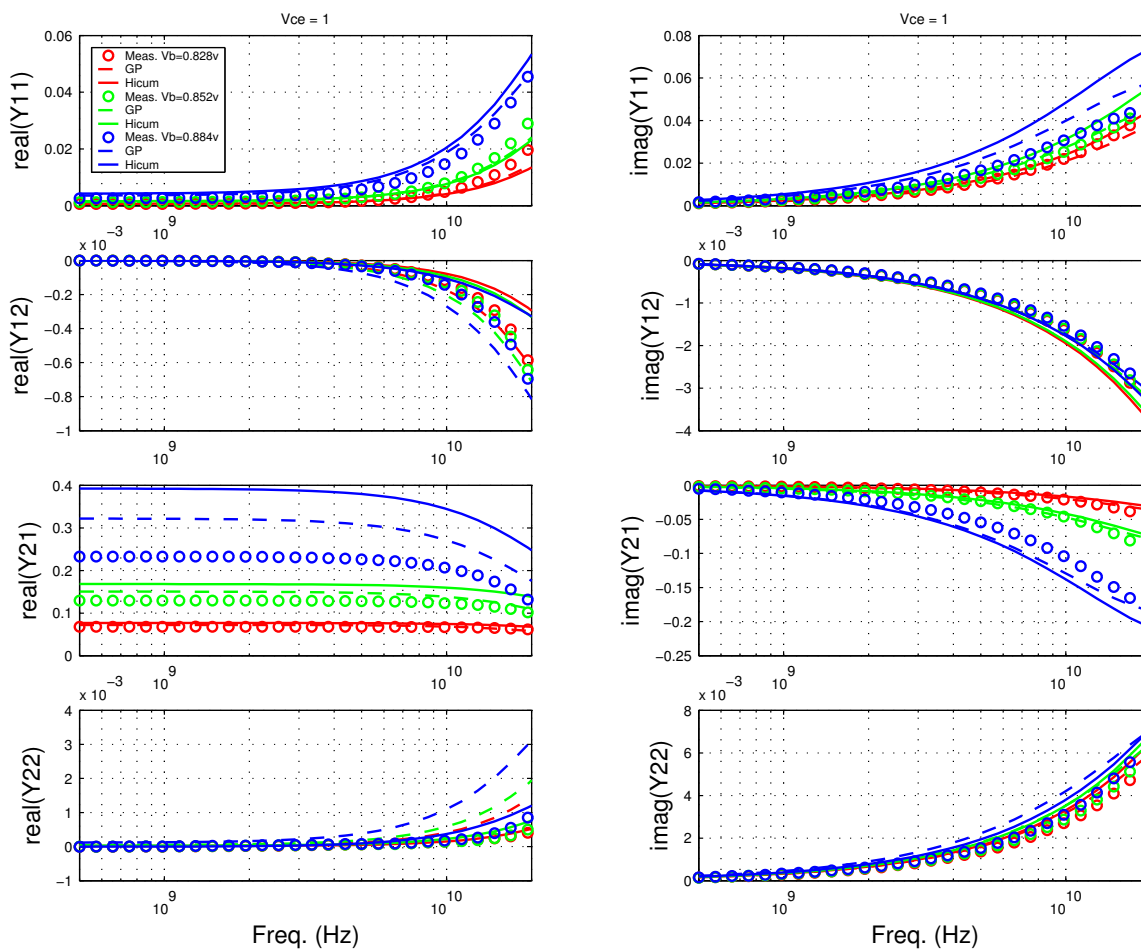


FIGURE 4.84 Gummel Plot LV 0.9x10.16x1_452

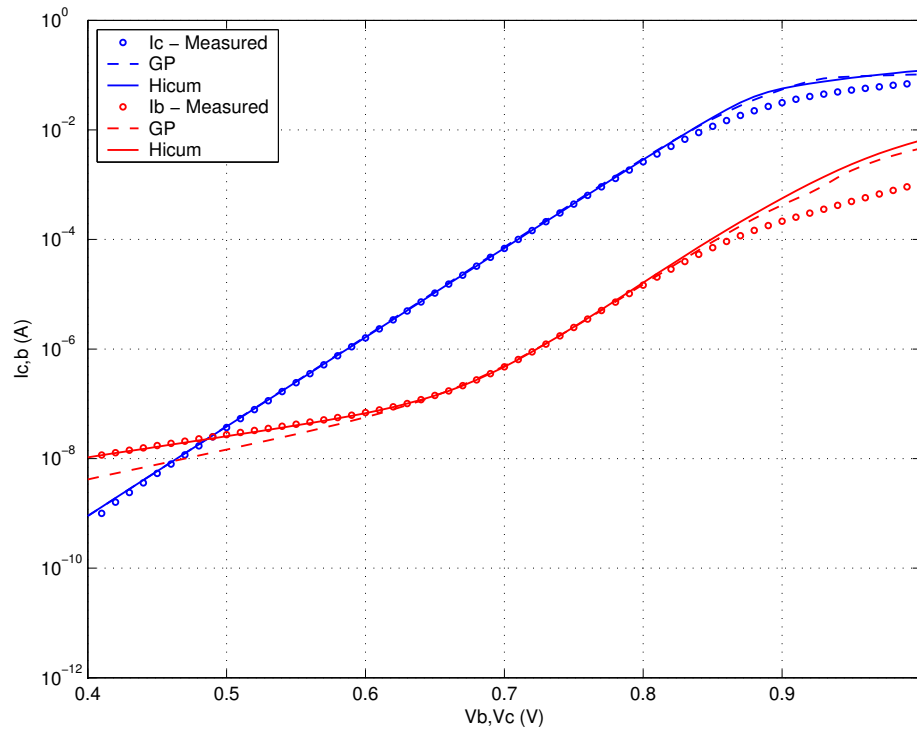
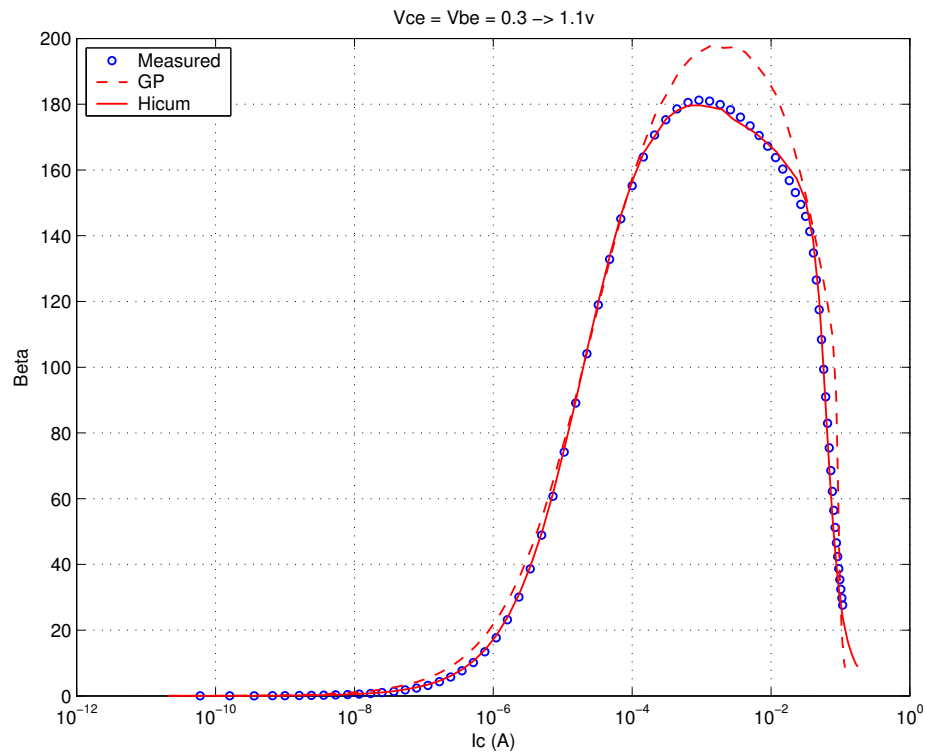
FIGURE 4.85 Beta vs. I_c : LV 0.9x10.16x1_452

FIGURE 4.86 IC vs. VCE at constant IB: LV 0.9x10.16x1_452

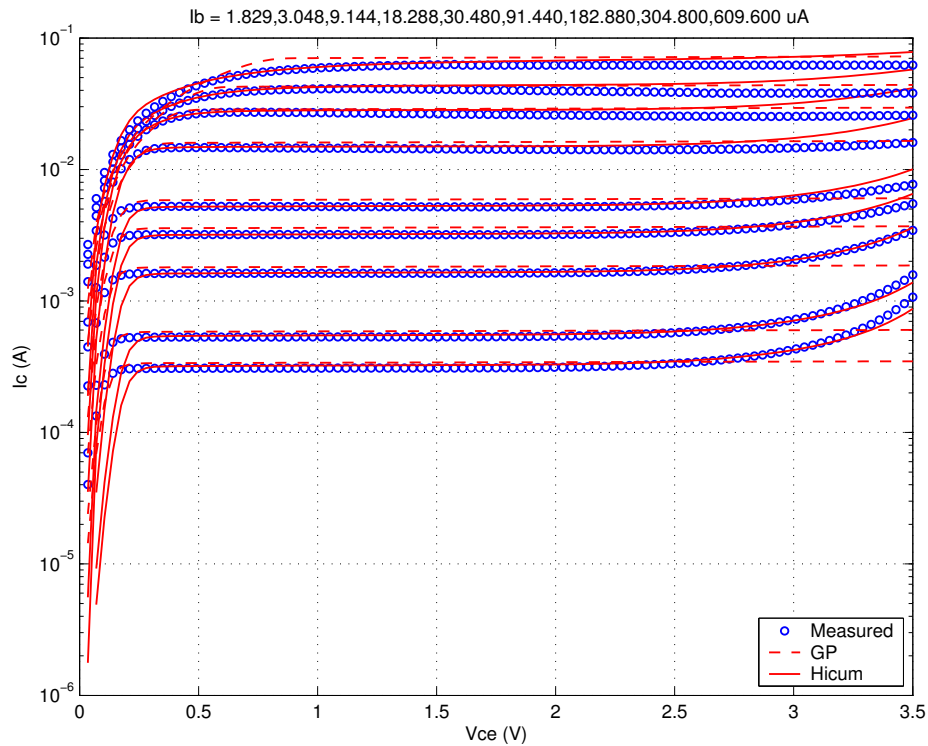


FIGURE 4.87 FT vs. IC: LV 0.9x10.16x1_452

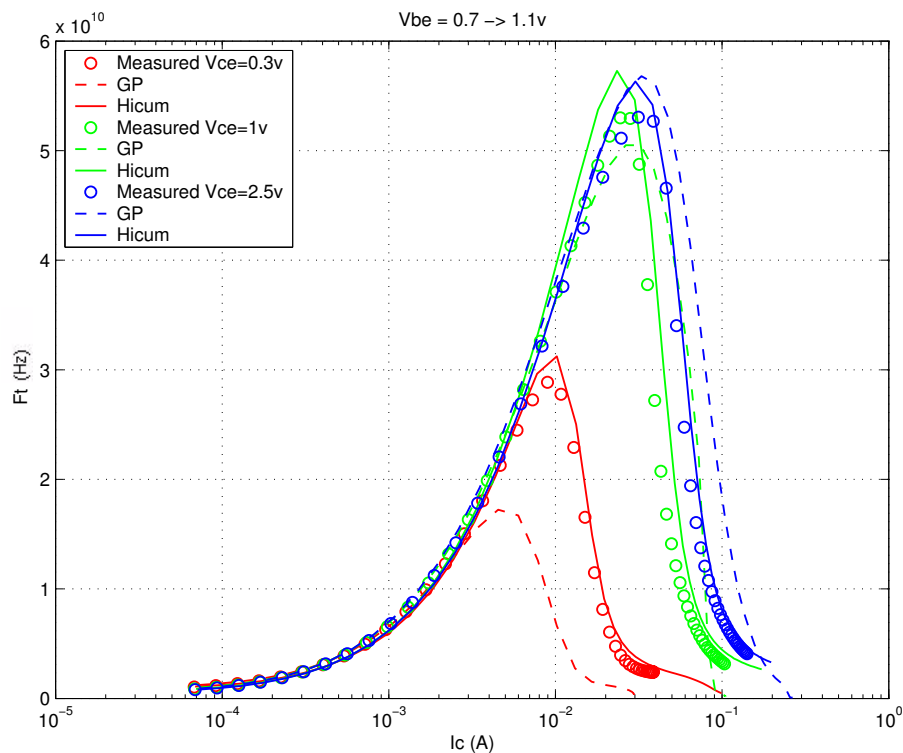
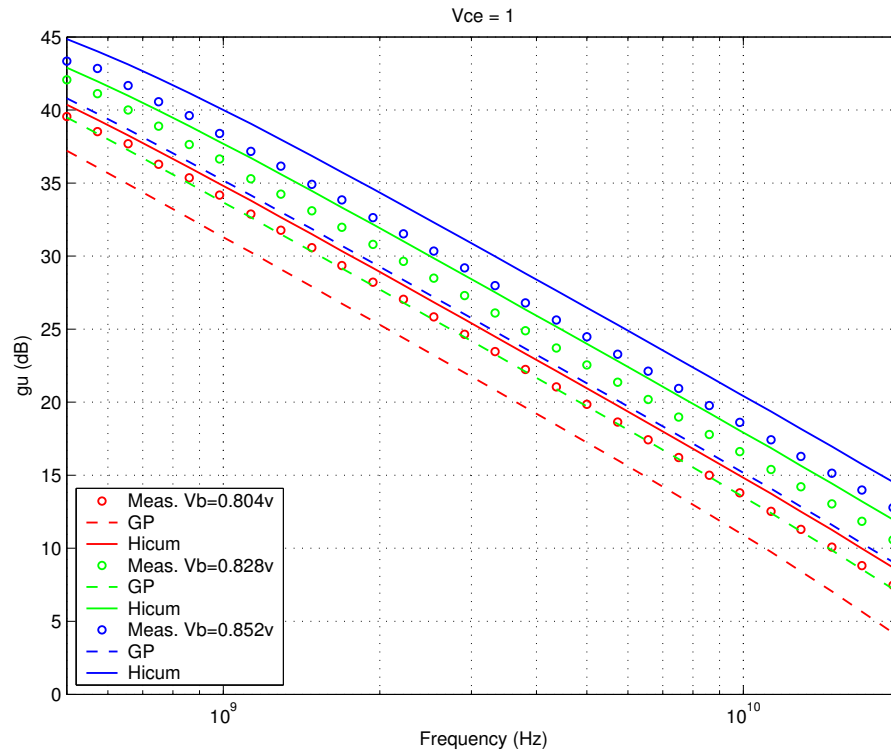
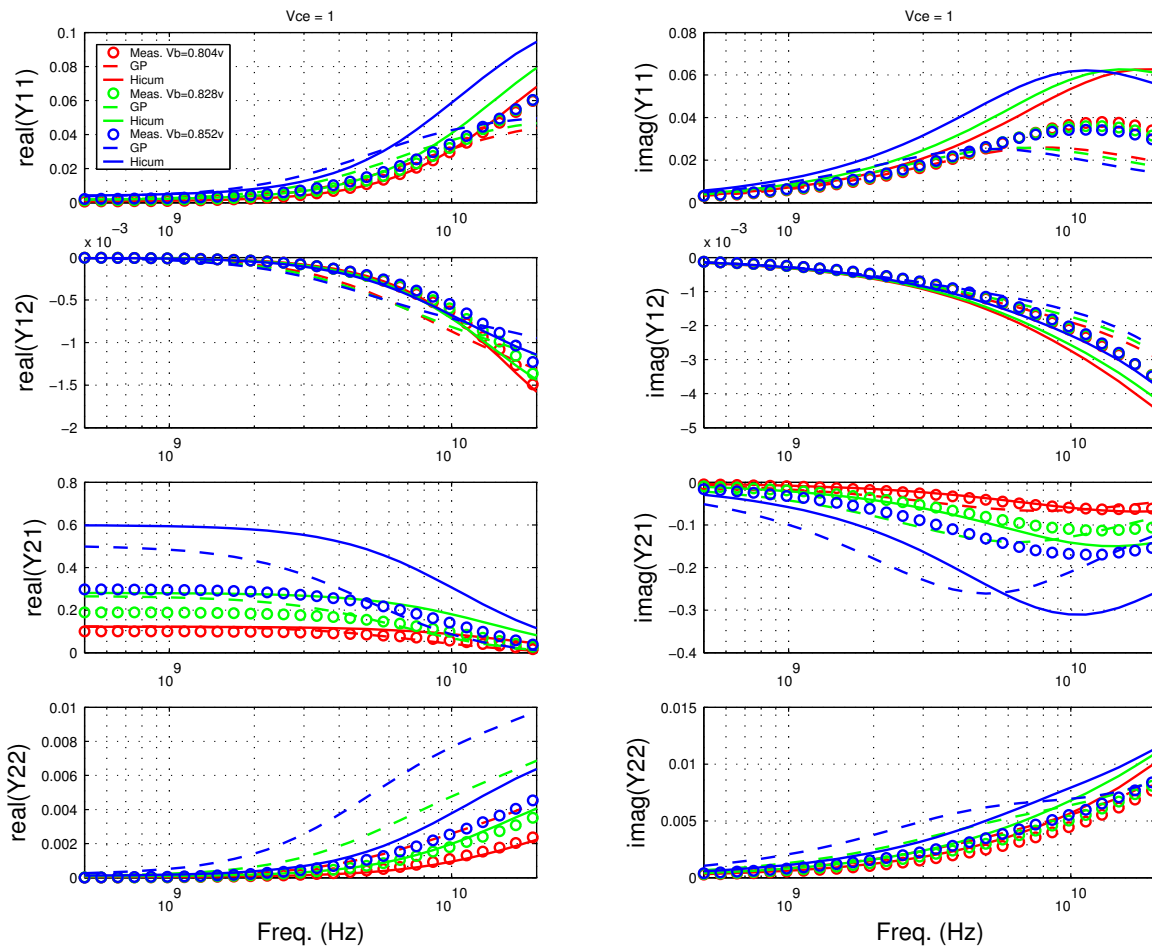


FIGURE 4.88 Power Gain vs. Freq: LV 0.9x10.16x1_452



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FIGURE 4.89 Y-parameters vs. FREQ: LV 0.9x10.16x1_452



4.4.3 High Voltage NPN Verification Plots

FIGURE 4.90 Gummel Plot HV 0.2x0.76x1_122

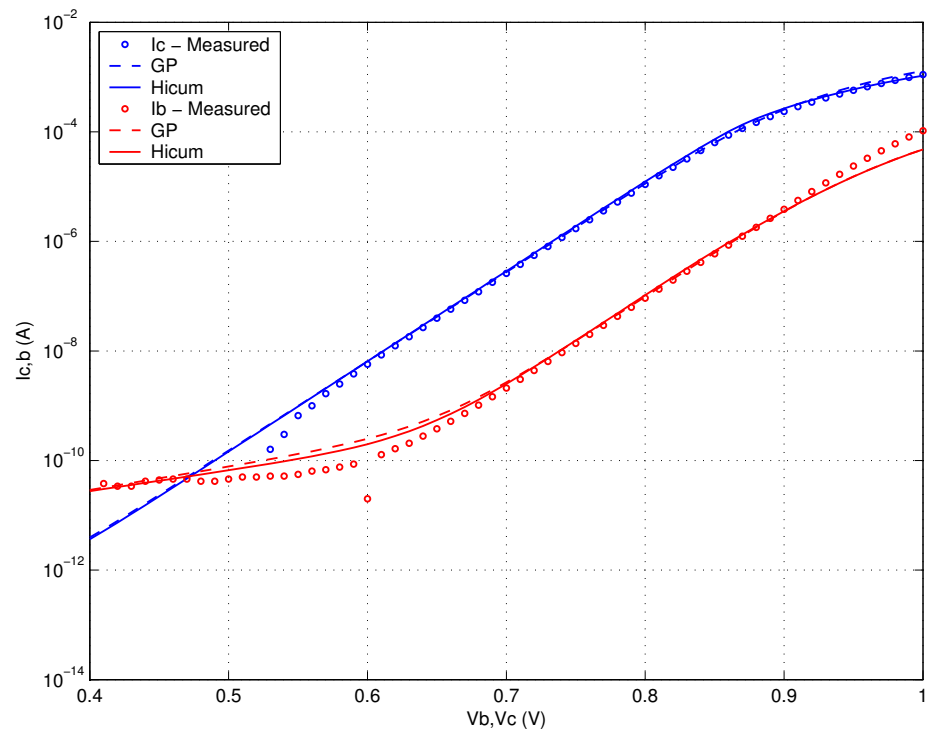


FIGURE 4.91 Beta vs. I_c : HV 0.2x0.76x1_122

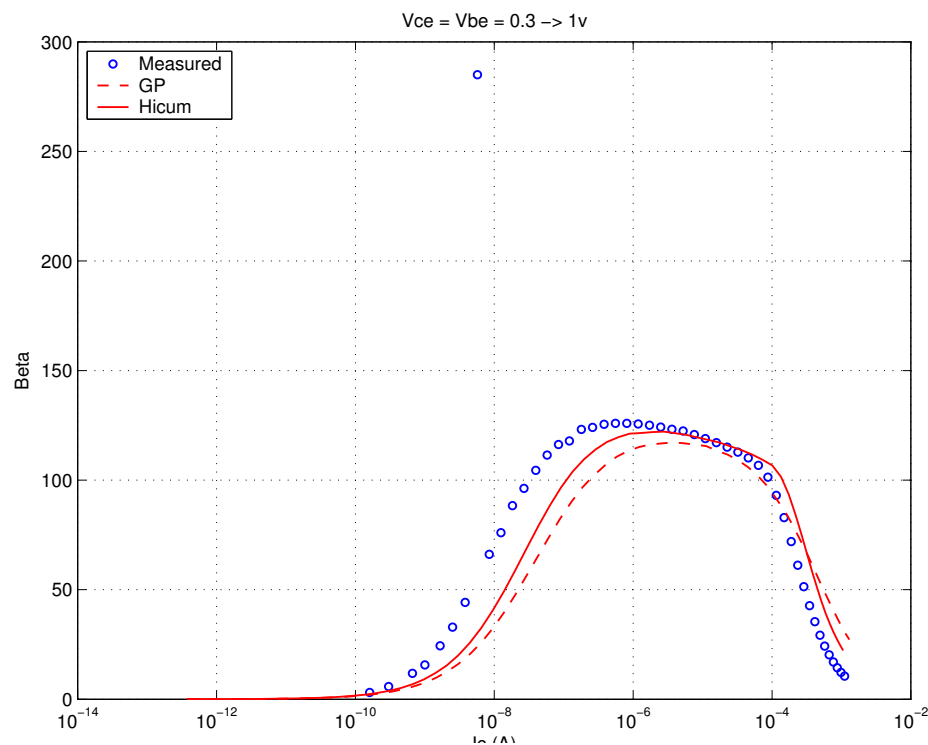
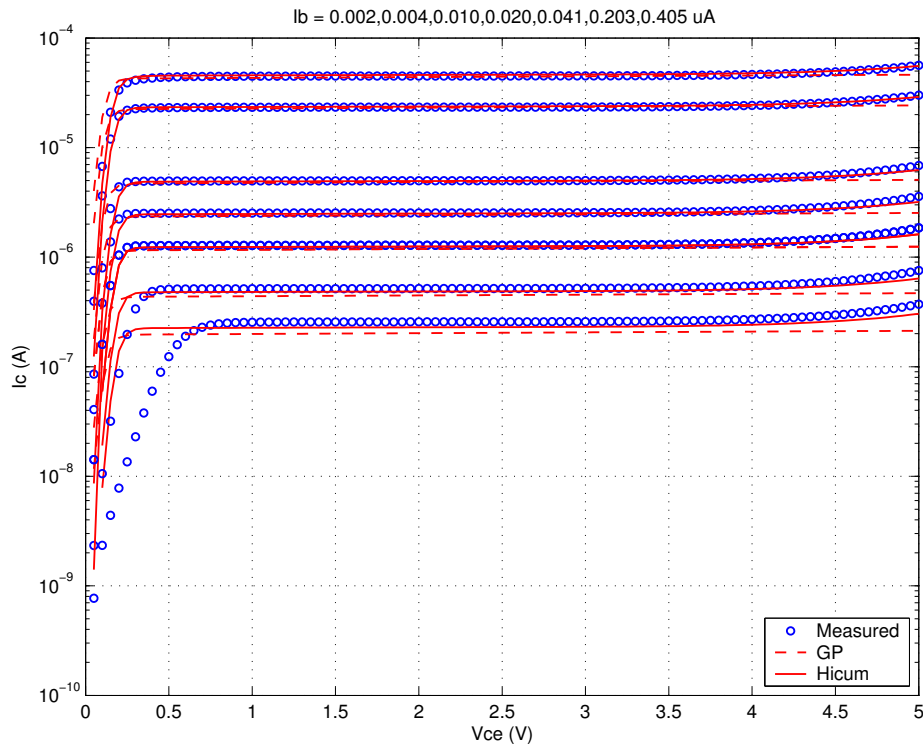


FIGURE 4.92 IC vs. VCE at constant IB: HV 0.2x0.76x1_122



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FIGURE 4.93 Gummel Plot HV 0.2x4.52x1_122

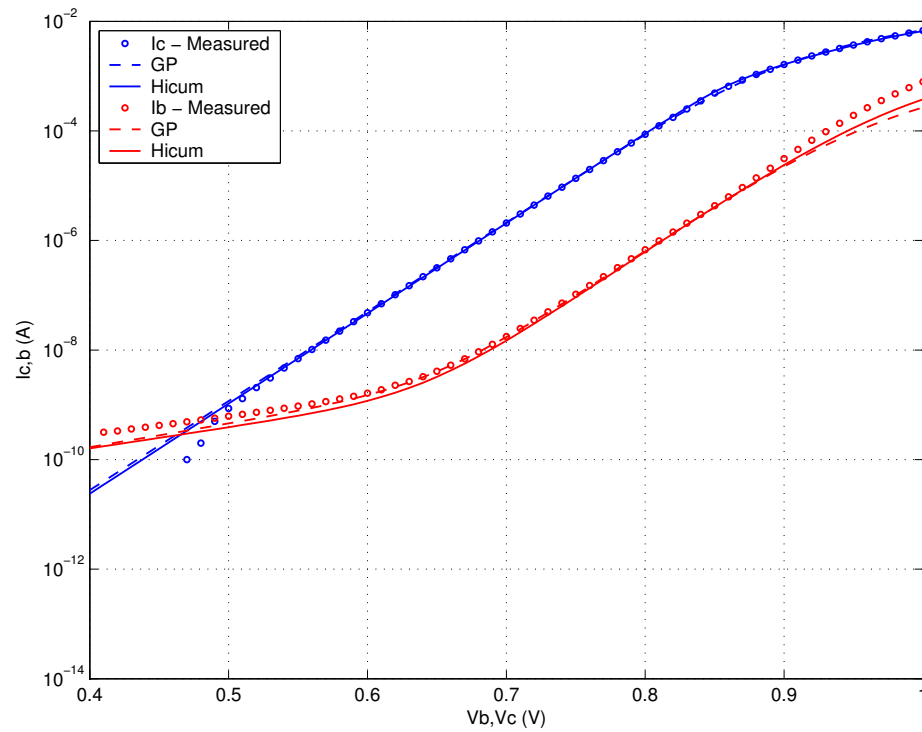
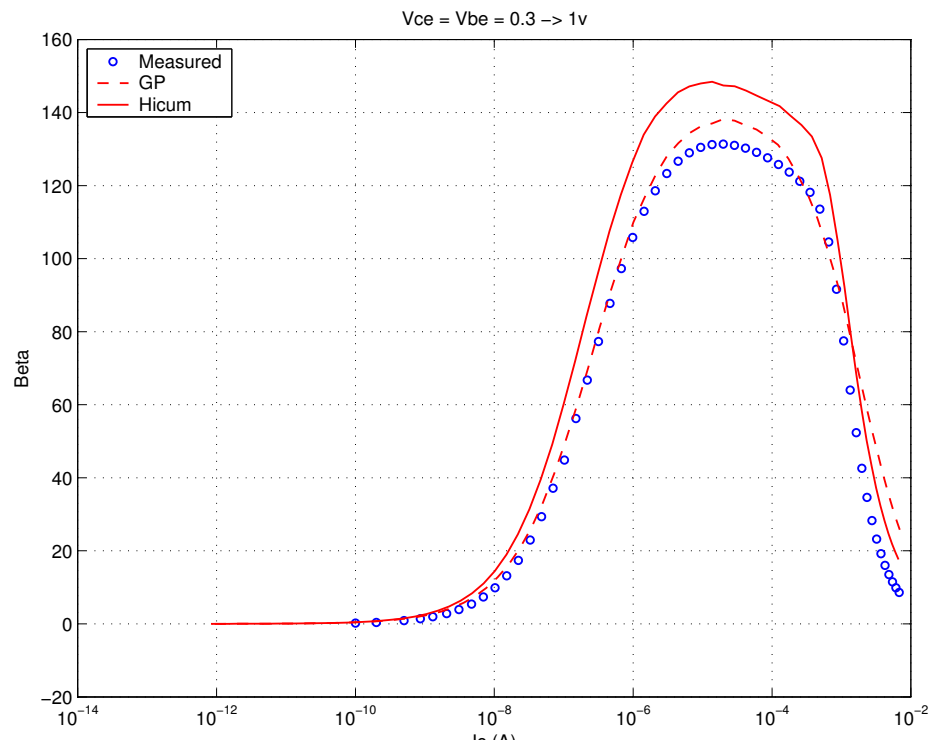
FIGURE 4.94 Beta vs. I_c : HV 0.2x4.52x1_122

FIGURE 4.95 I_C vs. V_{CE} at constant I_B : HV 0.2x4.52x1_122

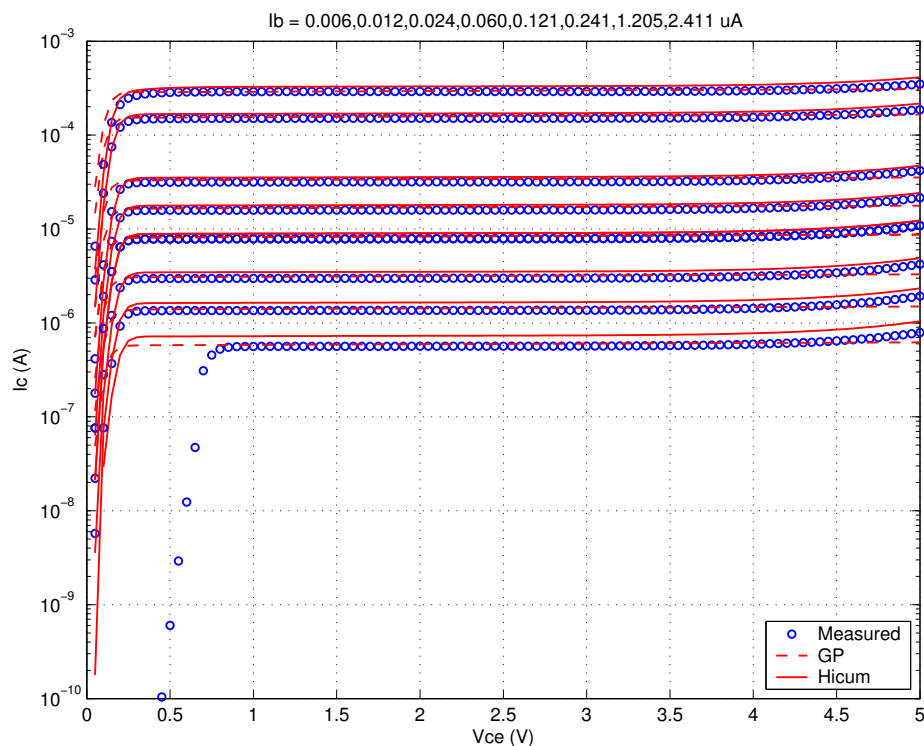


FIGURE 4.96 f_T vs. I_C : HV 0.2x4.52x1_122

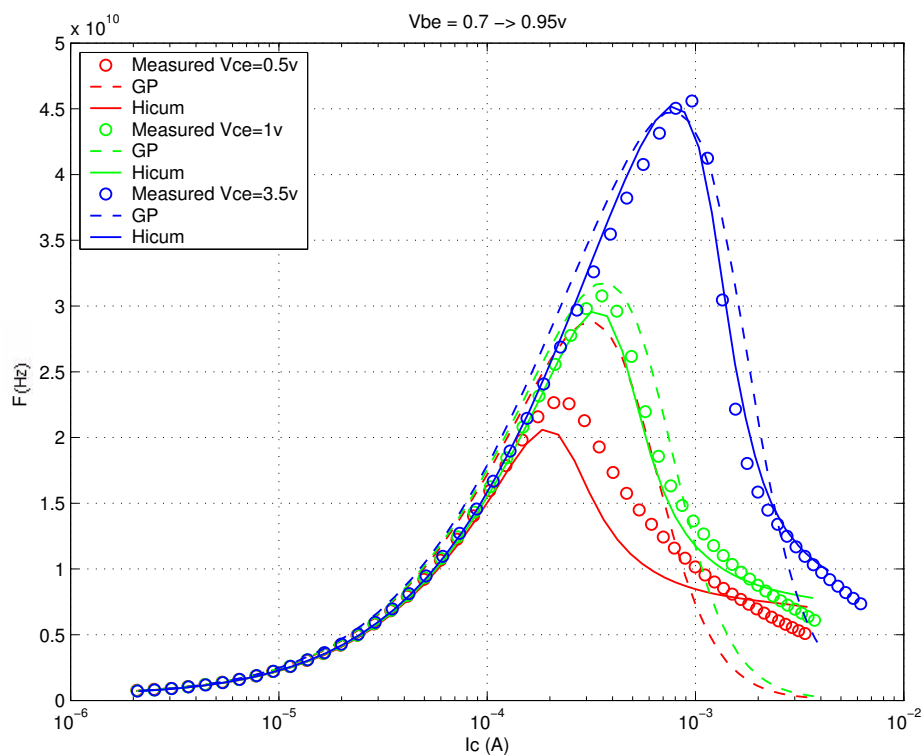
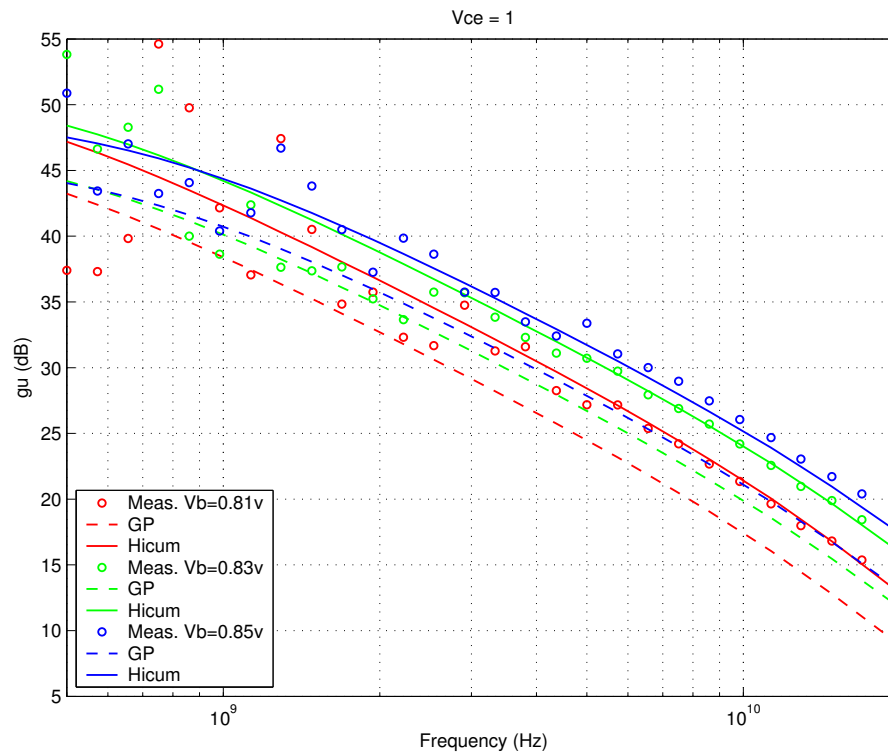


FIGURE 4.97 Power Gain vs. Freq: HV 0.2x4.52x1_122



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FIGURE 4.98 Y-parameters vs. FREQ: HV 0.2x4.52x1_122

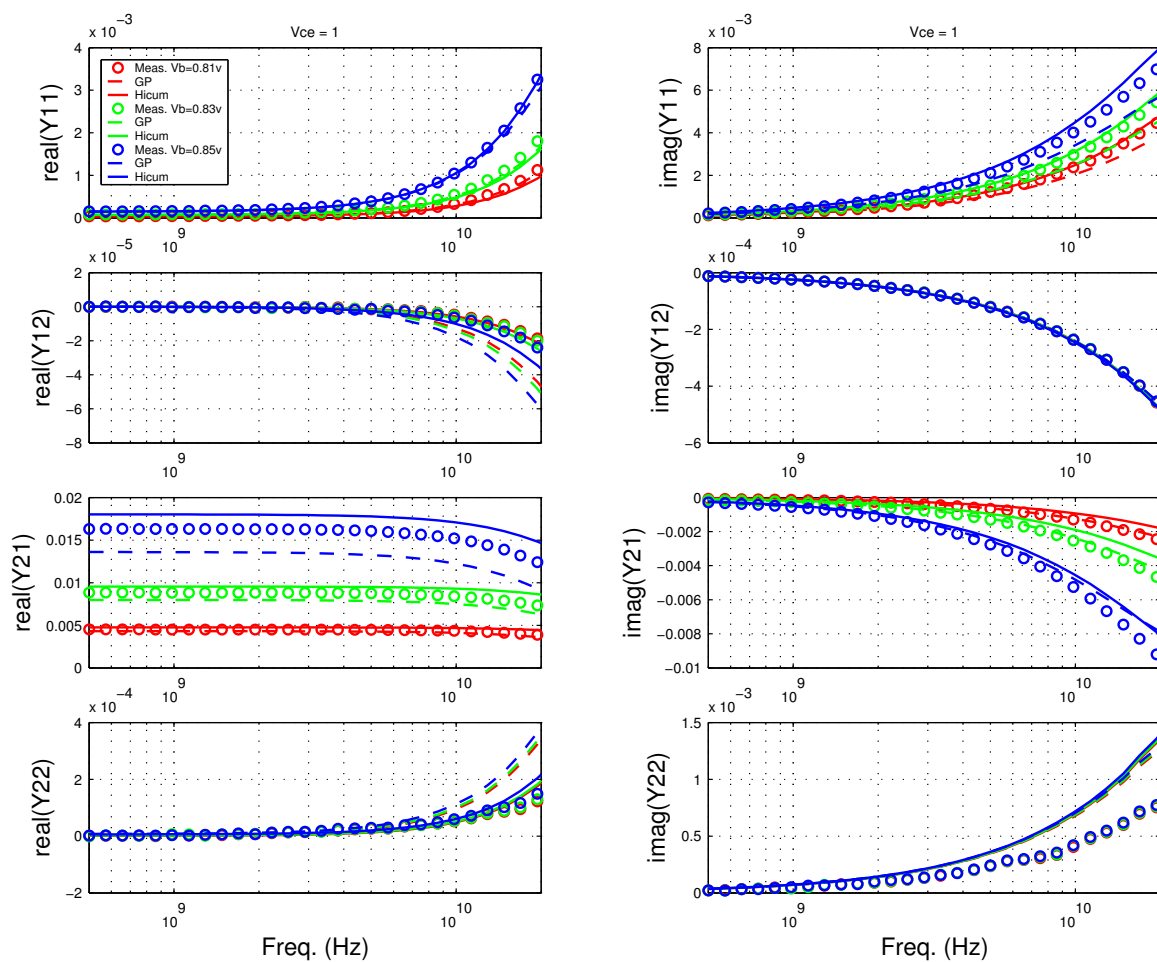


FIGURE 4.99 Gummel Plot HV 0.2x10.16x1_122

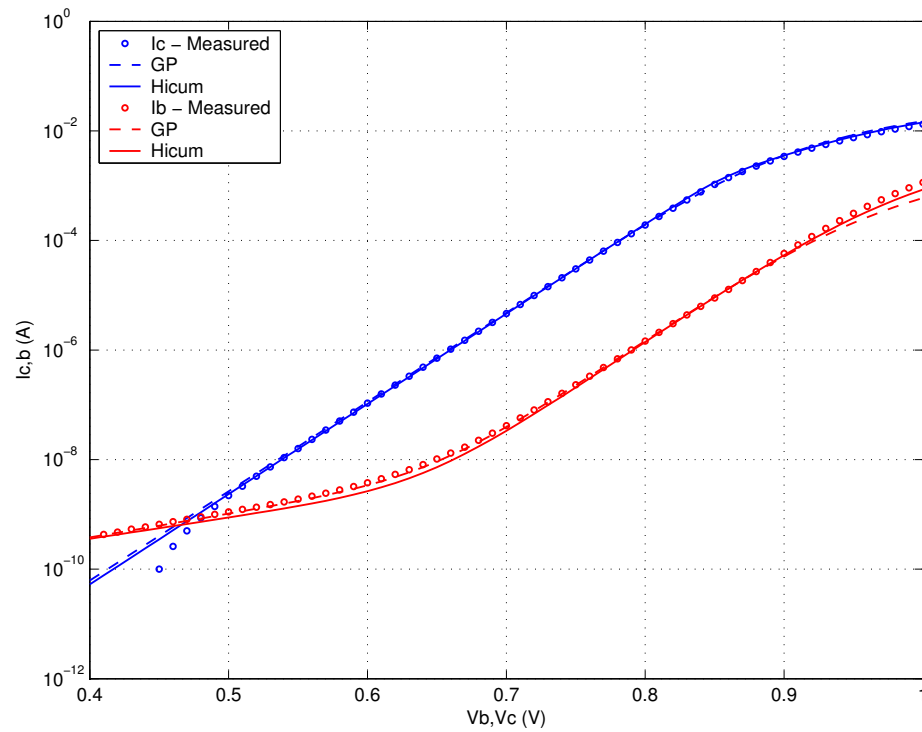
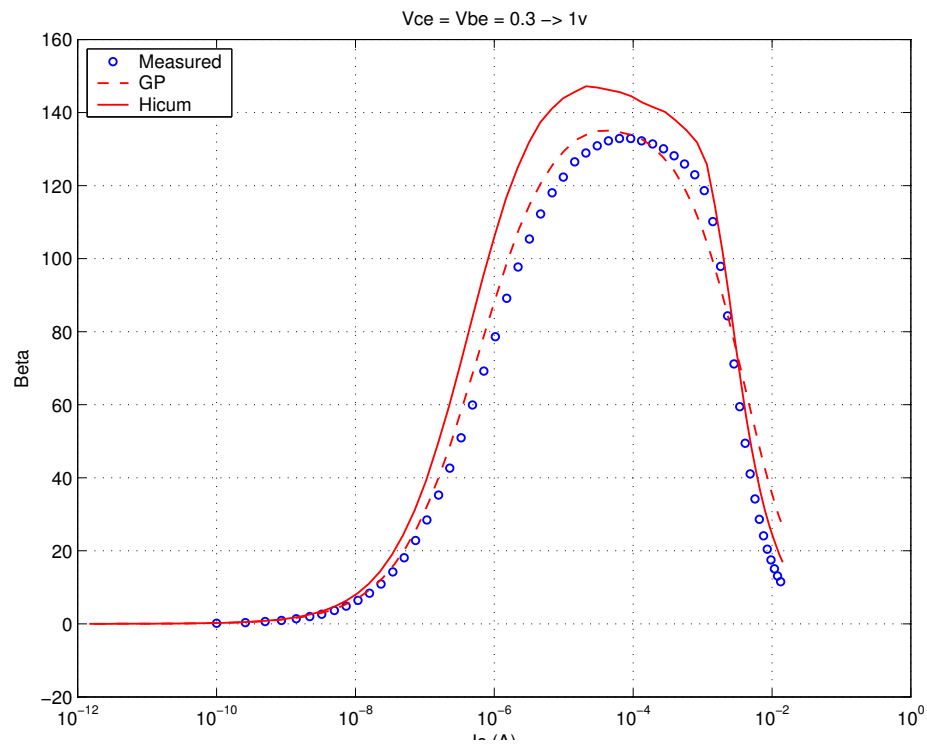
FIGURE 4.100 Beta vs. I_c : HV 0.2x10.16x1_122

FIGURE 4.101 I_C vs. V_{CE} at constant I_B : HV 0.2x10.16x1_122

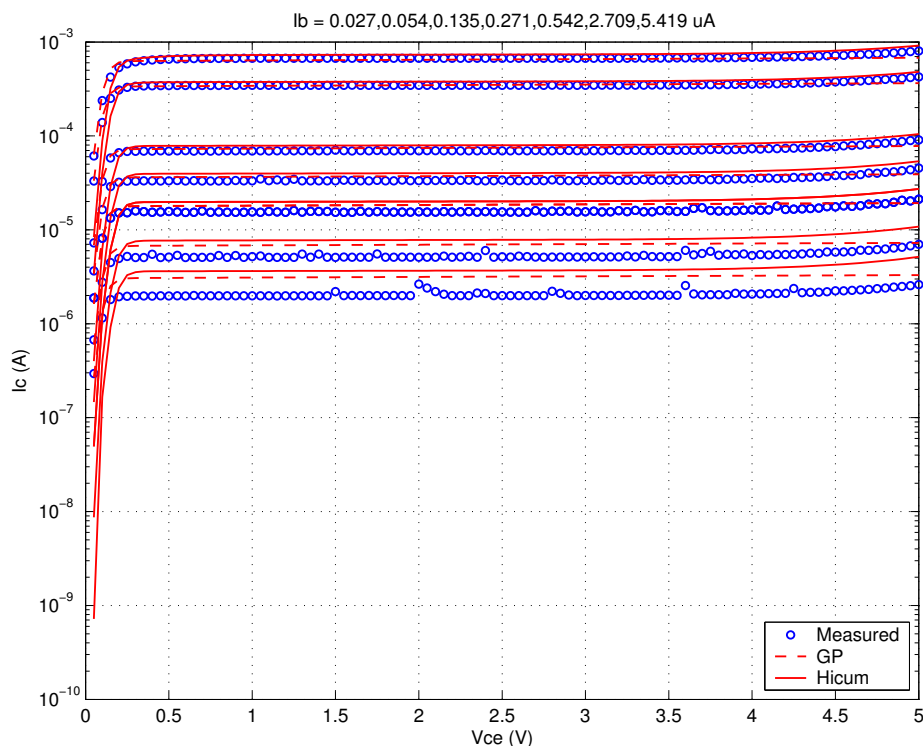


FIGURE 4.102 f_T vs. I_C : HV 0.2x10.16x1_122

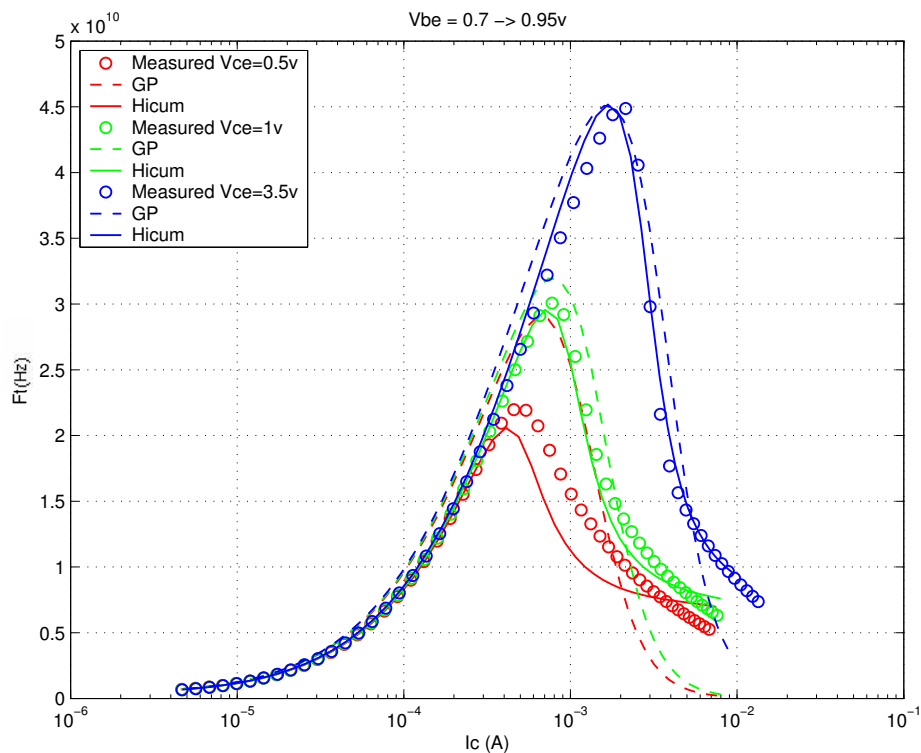
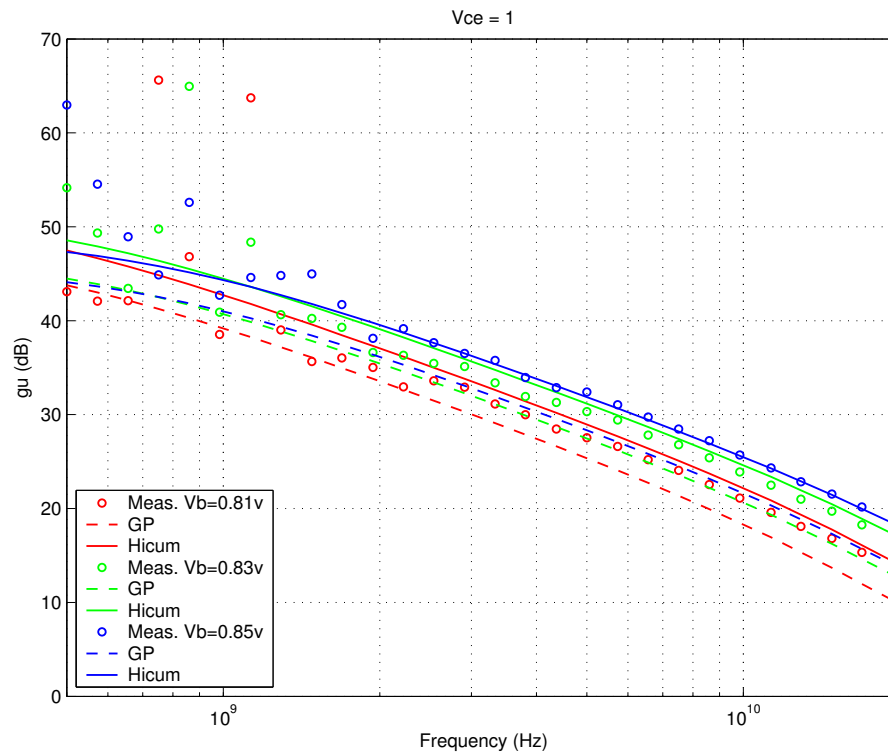


FIGURE 4.103 Power Gain vs. Freq: HV 0.2x10.16x1_122



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FIGURE 4.104 Y-parameters vs. FREQ: HV 0.2x10.16x1_122

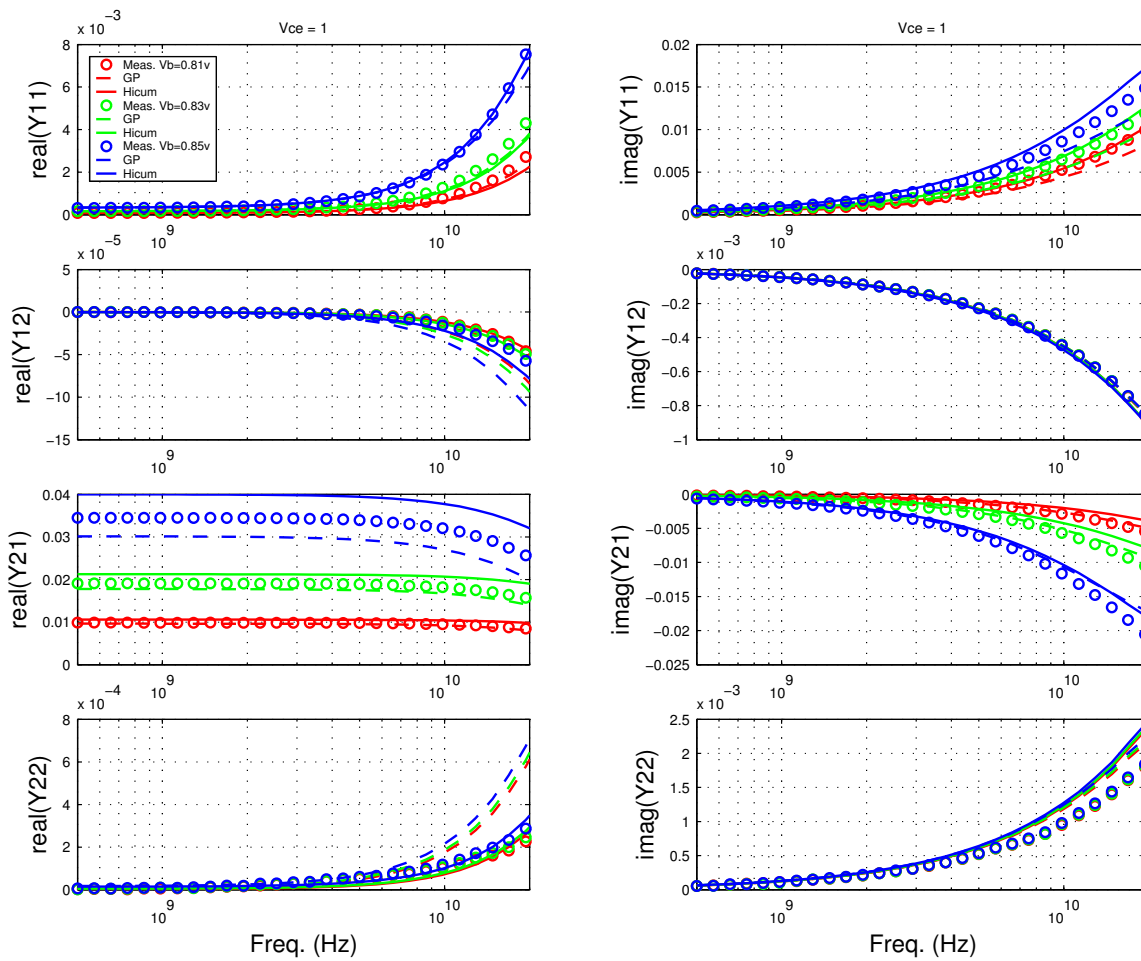


FIGURE 4.105 Gummel Plot HV 0.6x4.52x1_122

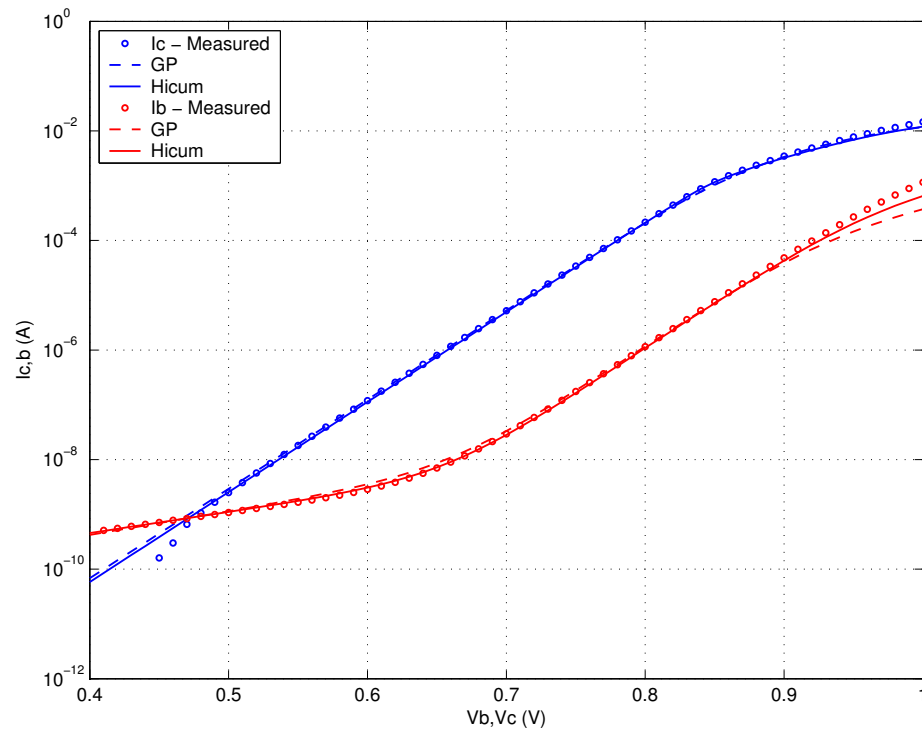
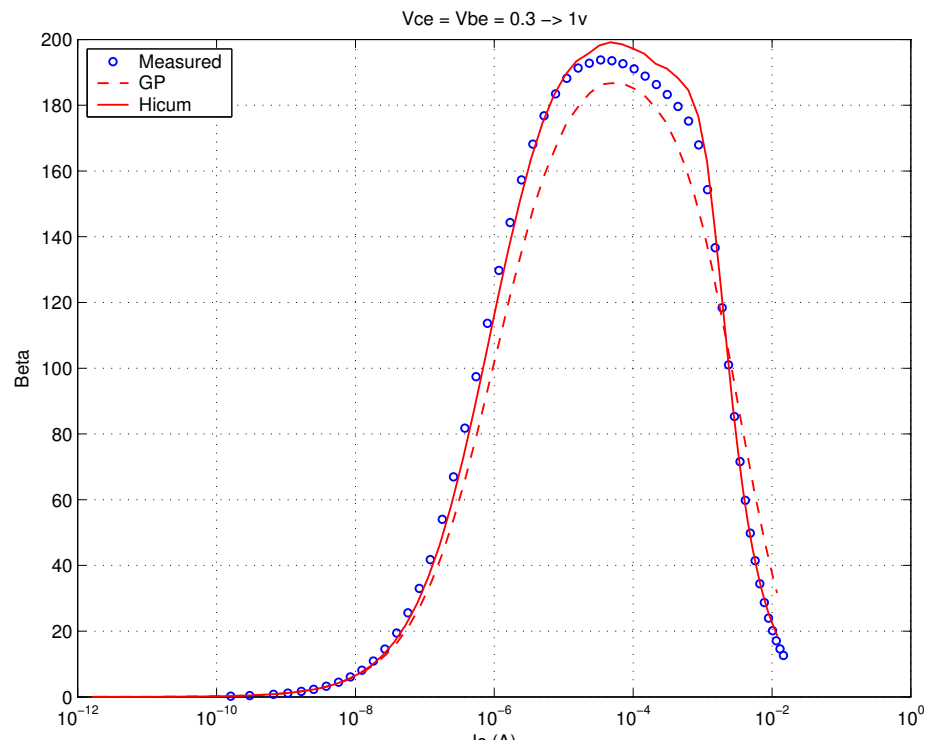
FIGURE 4.106 Beta vs. I_c : HV 0.6x4.52x1_122

FIGURE 4.107 I_C vs. V_{CE} at constant I_B : HV 0.6x4.52x1_122

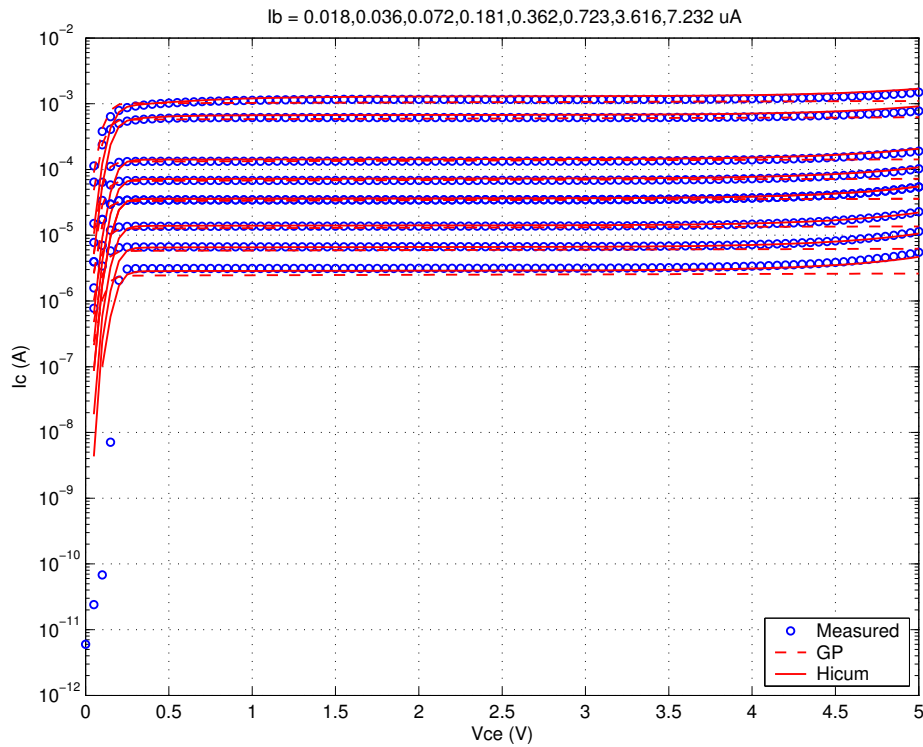


FIGURE 4.108 f_T vs. I_C : HV 0.6x4.52x1_122

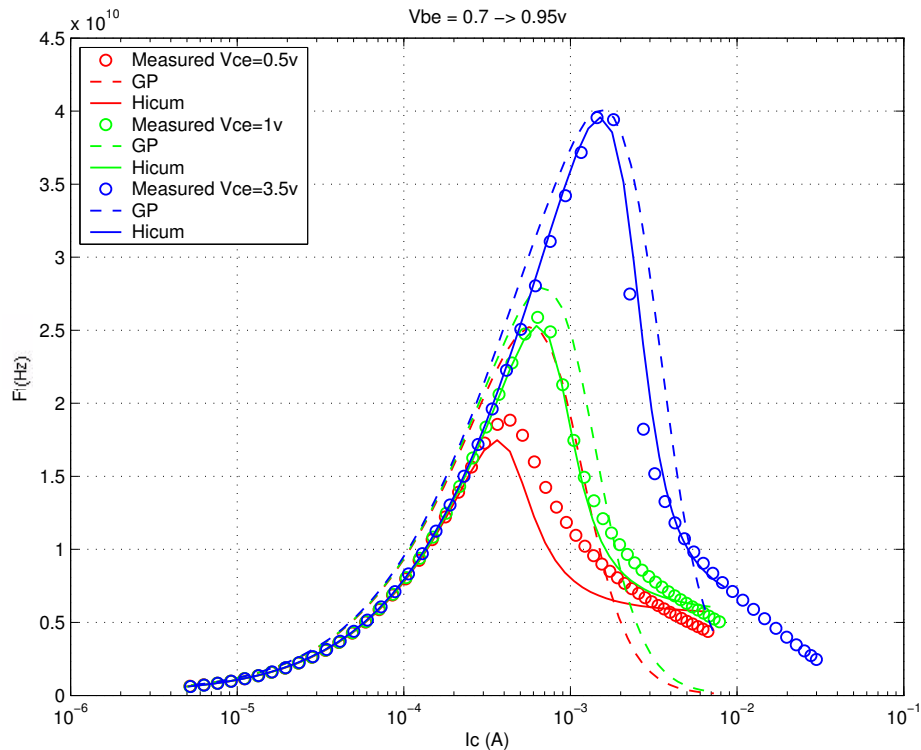
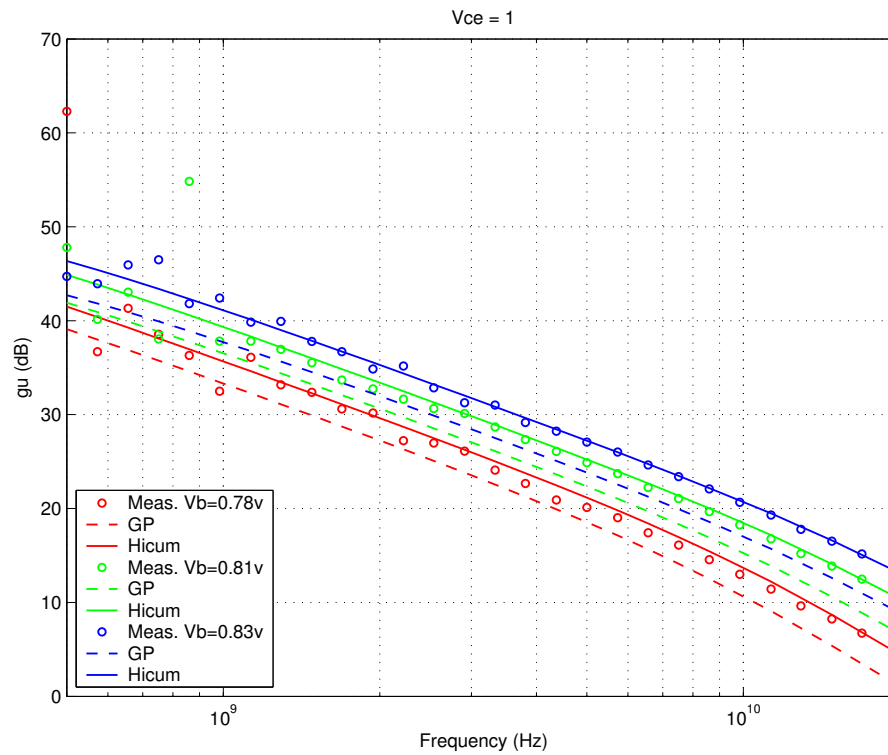


FIGURE 4.109 Power Gain vs. Freq: HV 0.6x4.52x1_122



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FIGURE 4.110 Y-parameters vs. FREQ: HV 0.6x4.52x1_122

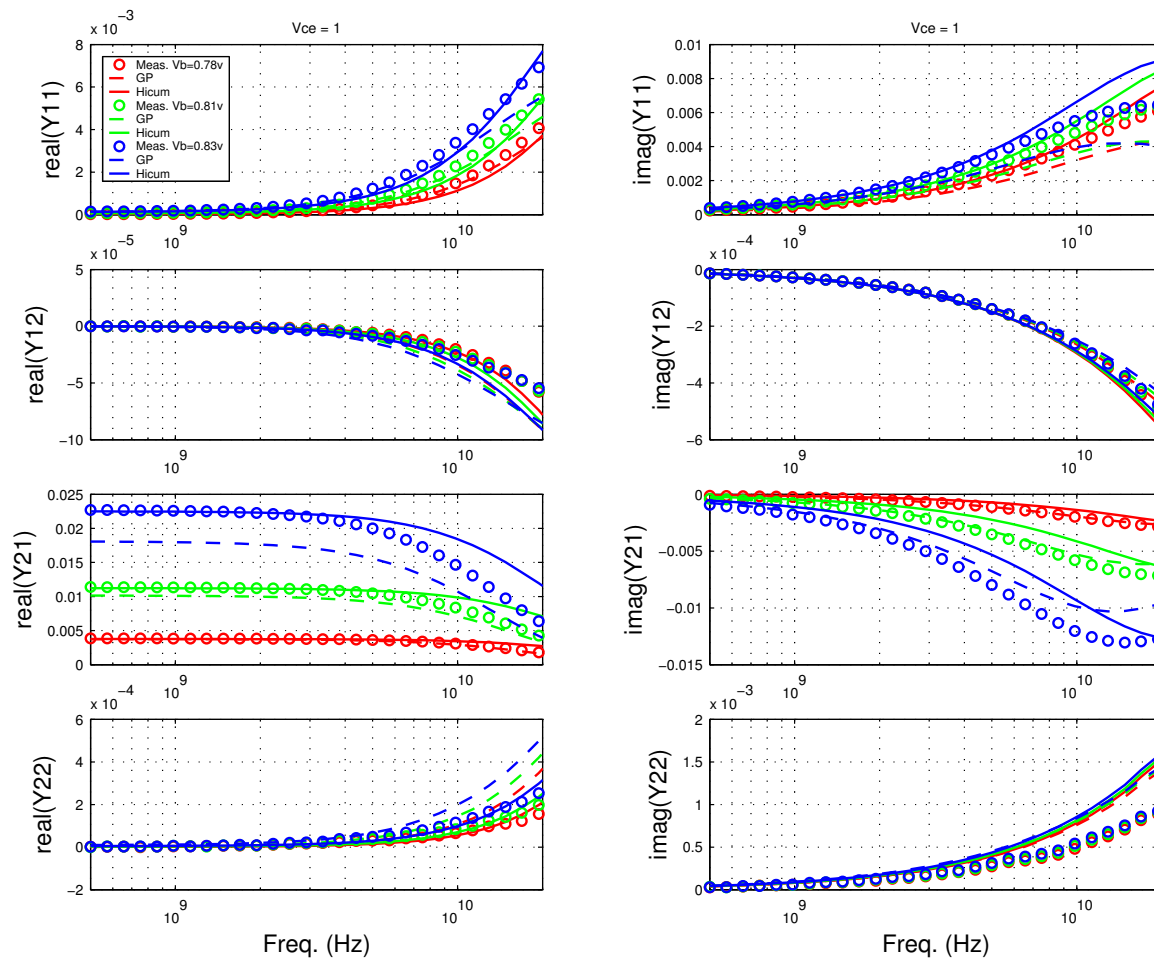


FIGURE 4.111 Gummel Plot HV 0.6x10.16x1_122

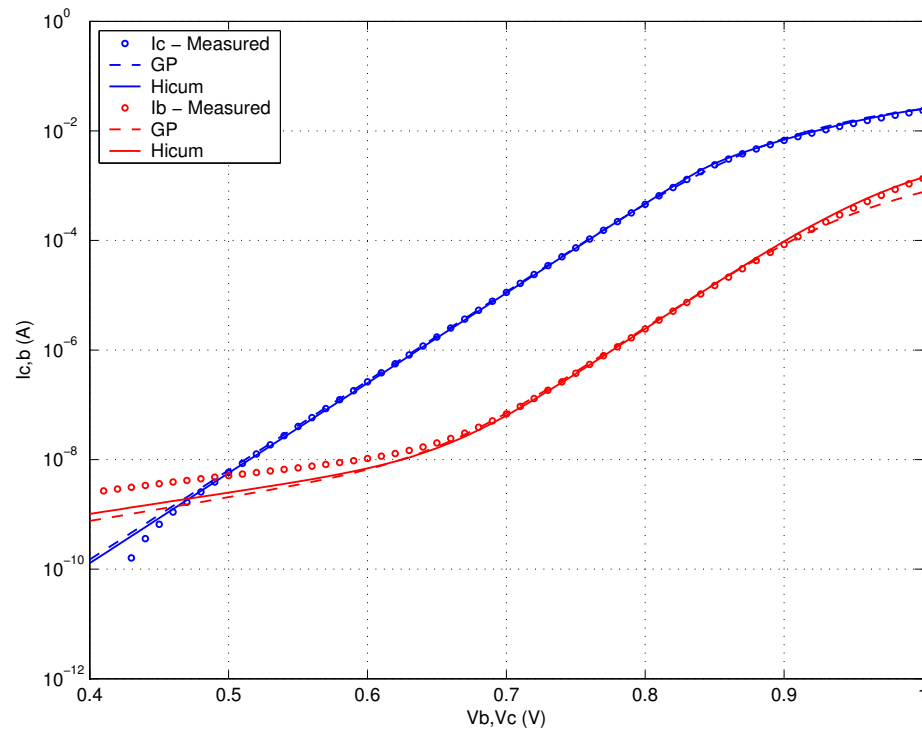
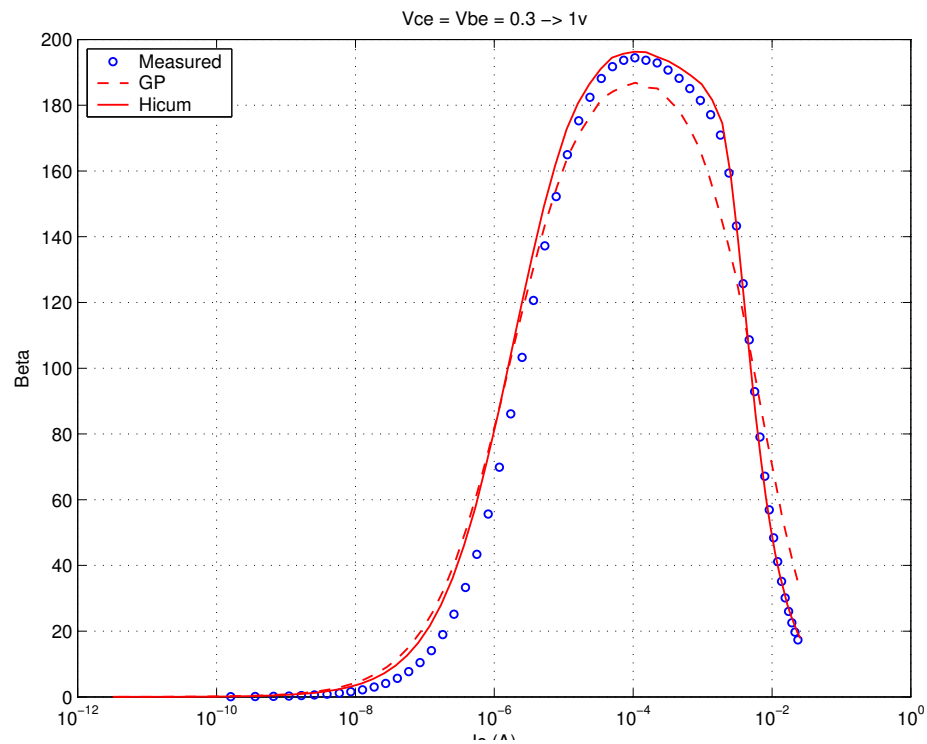
FIGURE 4.112 Beta vs. I_c : HV 0.6x10.16x1_122

FIGURE 4.113 IC vs. VCE at constant IB: HV 0.6x10.16x1_122

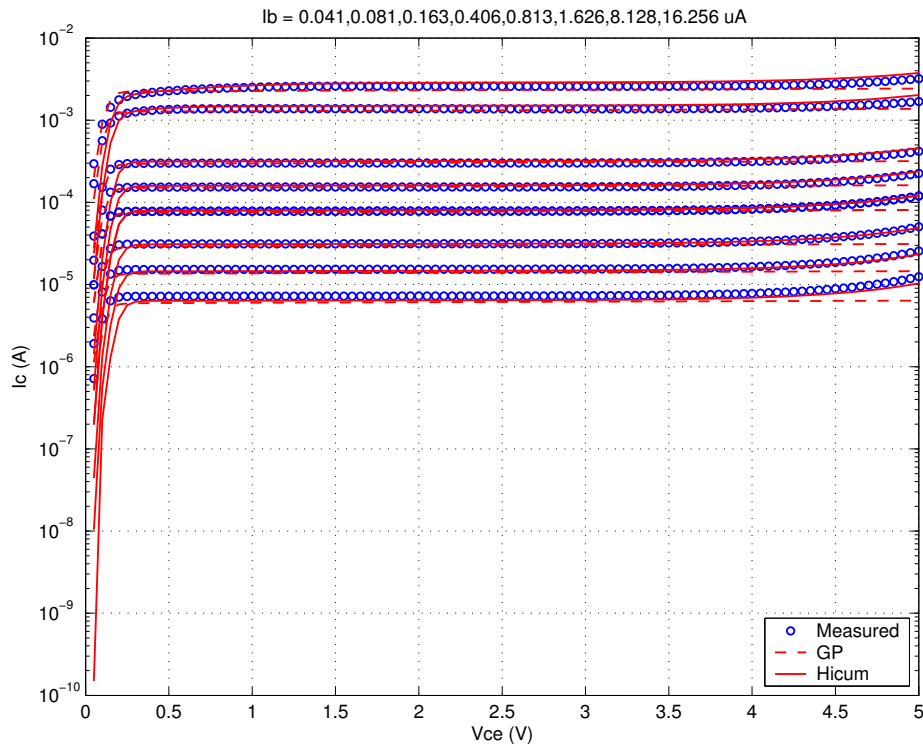


FIGURE 4.114 FT vs. IC: HV 0.6x10.16x1_122

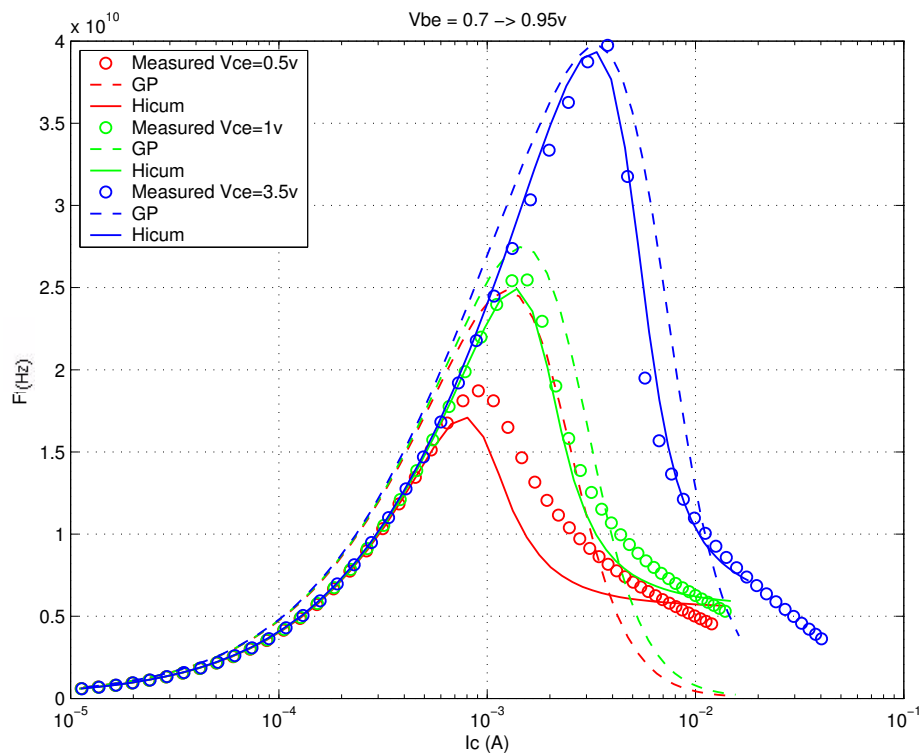
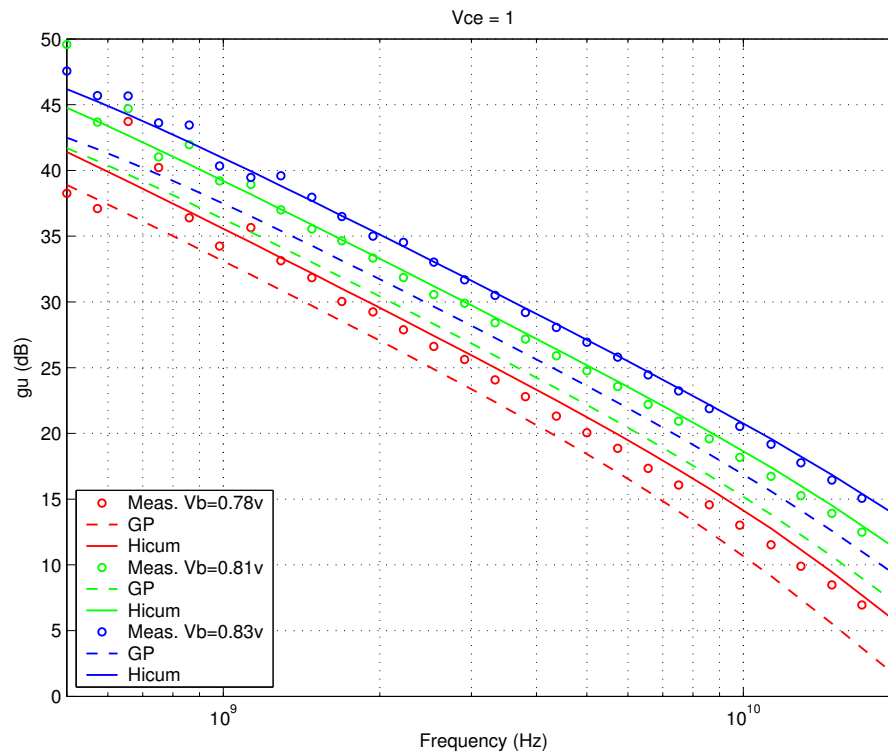


FIGURE 4.115 Power Gain vs. Freq: HV 0.6x10.16x1_122



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FIGURE 4.116 Y-parameters vs. FREQ: HV 0.6x10.16x1_122

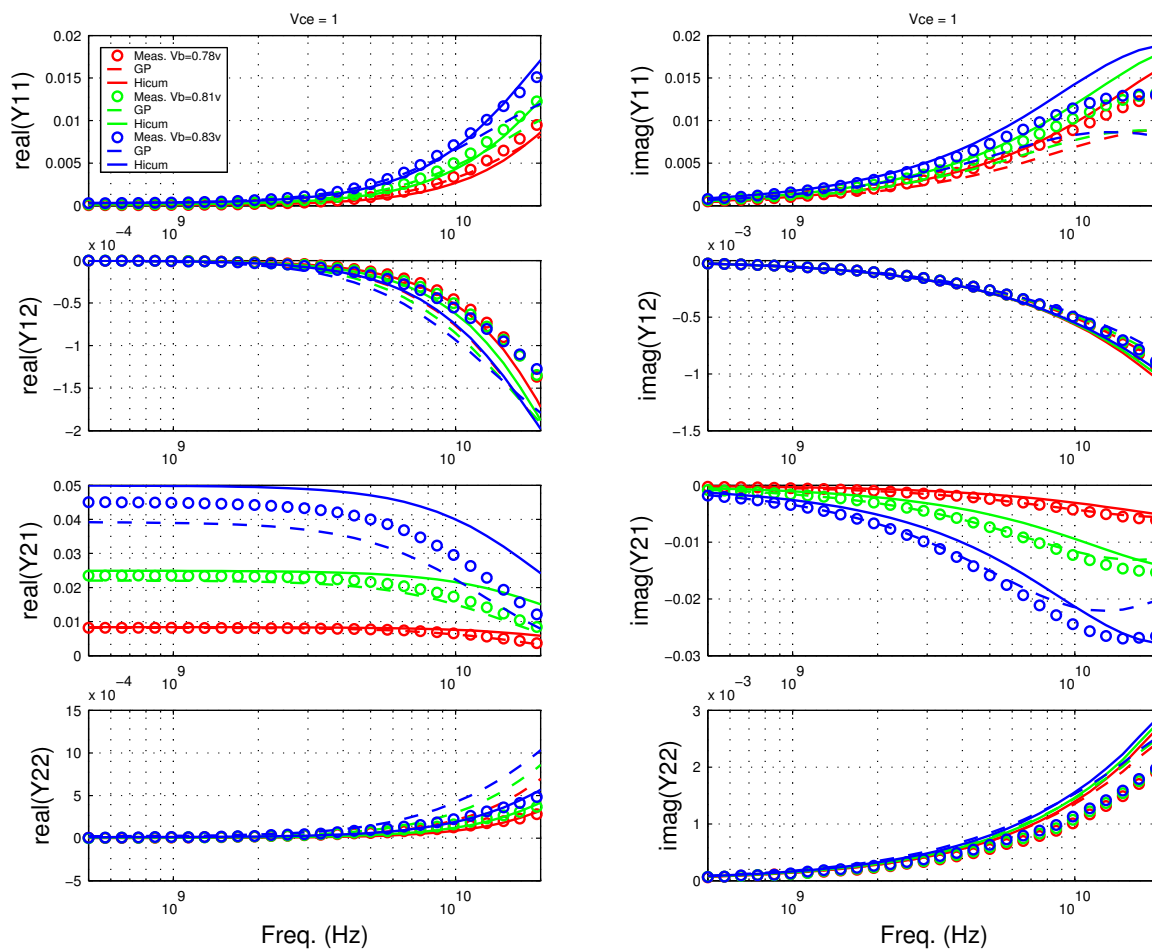


FIGURE 4.117 Gummel Plot HV 0.9x4.52x1_122

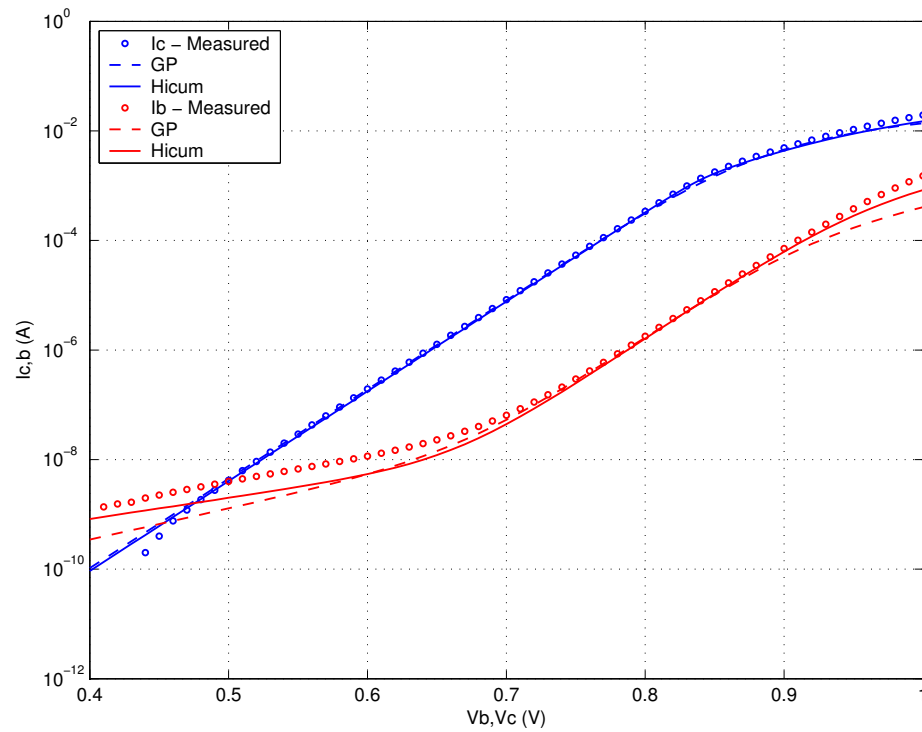
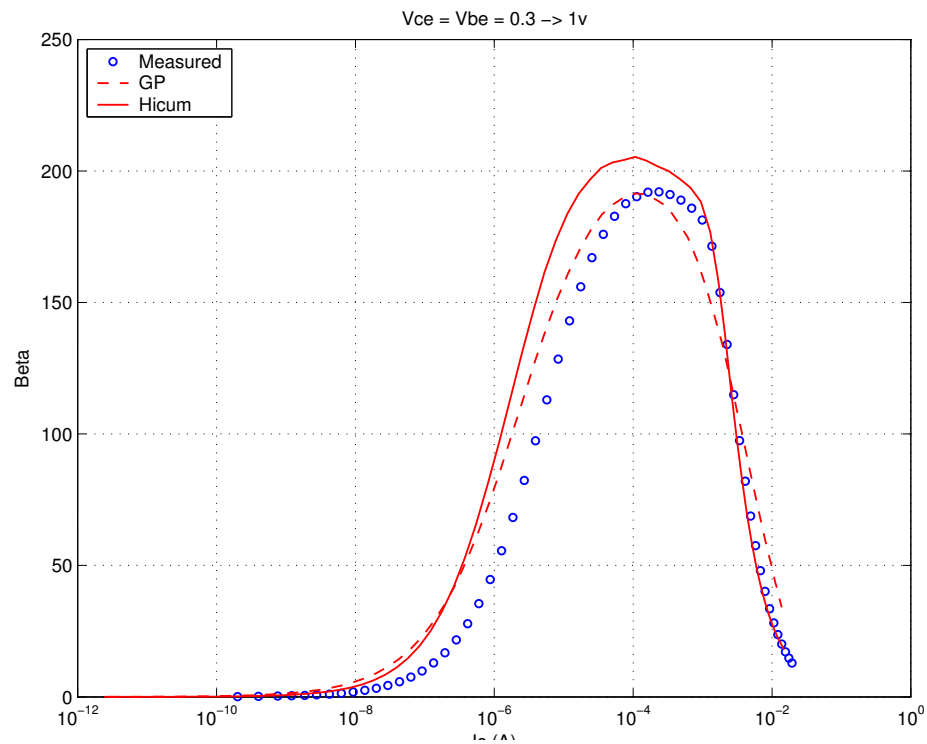
FIGURE 4.118 Beta vs. I_c : HV 0.9x4.52x1_122

FIGURE 4.119 I_C vs. V_{CE} at constant I_B : HV 0.9x4.52x1_122

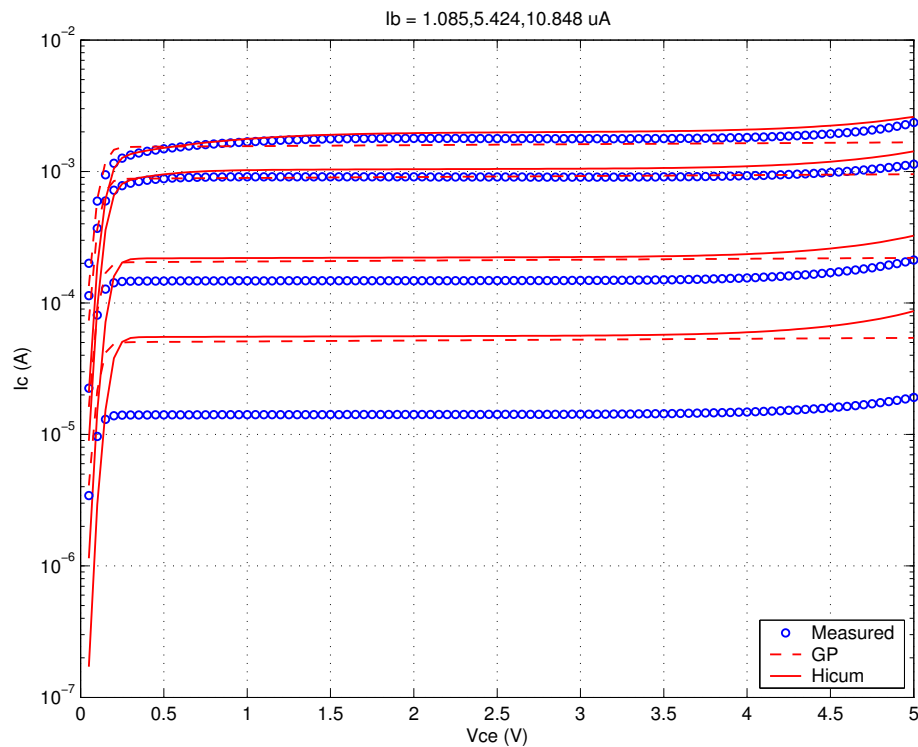


FIGURE 4.120 F_T vs. I_C : HV 0.9x4.52x1_122

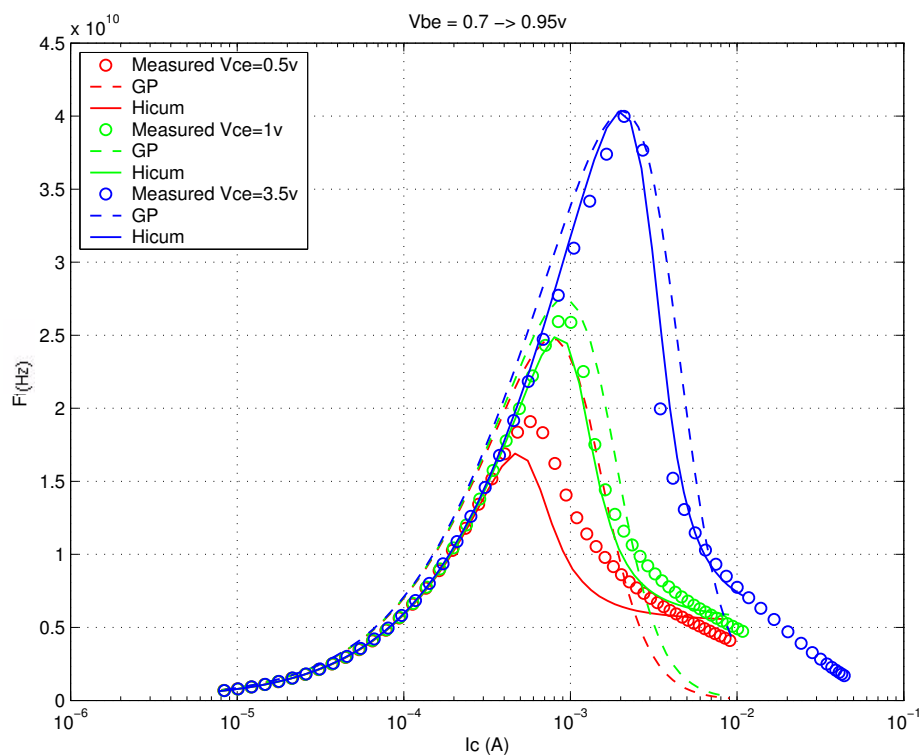
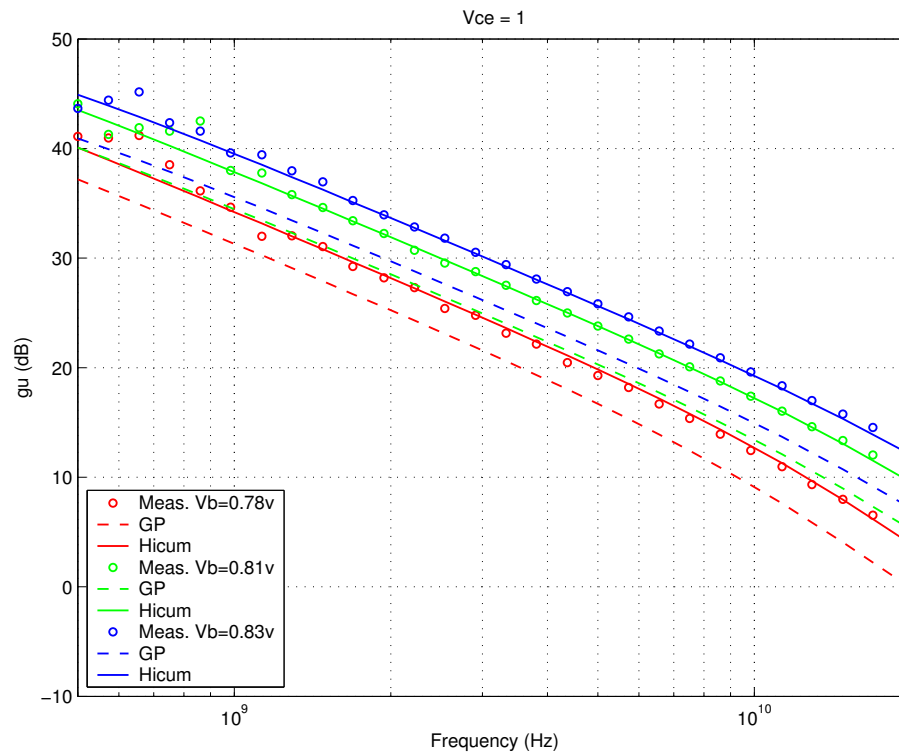


FIGURE 4.121 Power Gain vs. Freq: HV 0.9x4.52x1_122



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FIGURE 4.122 Y-parameters vs. FREQ: HV 0.9x4.52x1_122

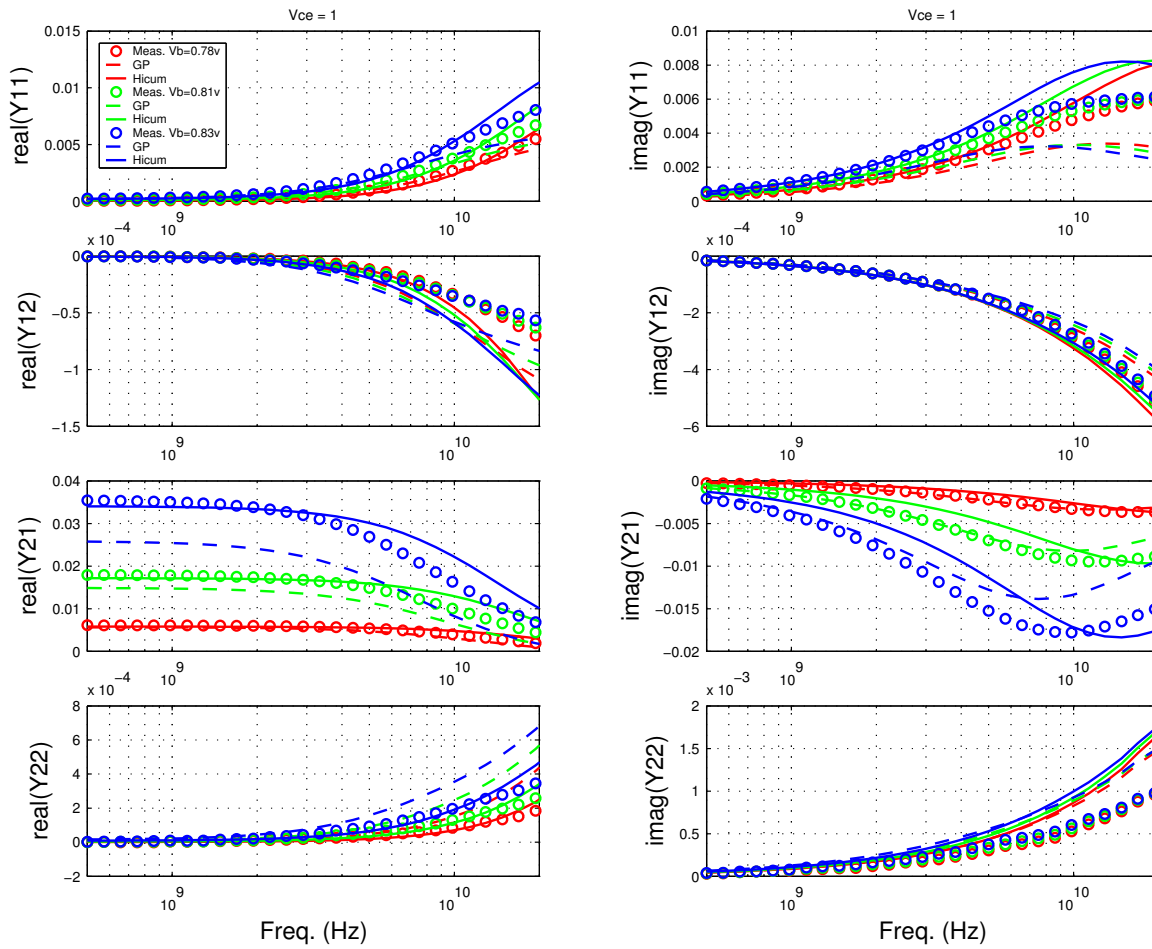


FIGURE 4.123 Gummel Plot HV 0.9x10.16x1_122

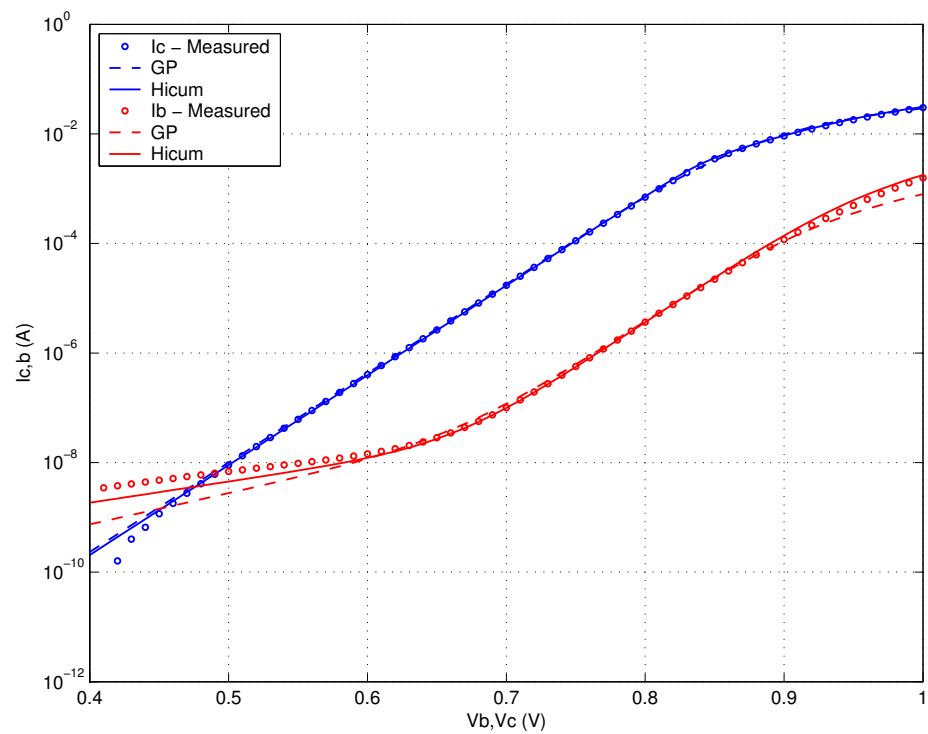


FIGURE 4.124 Beta vs. I_c : HV 0.9x10.16x1_122

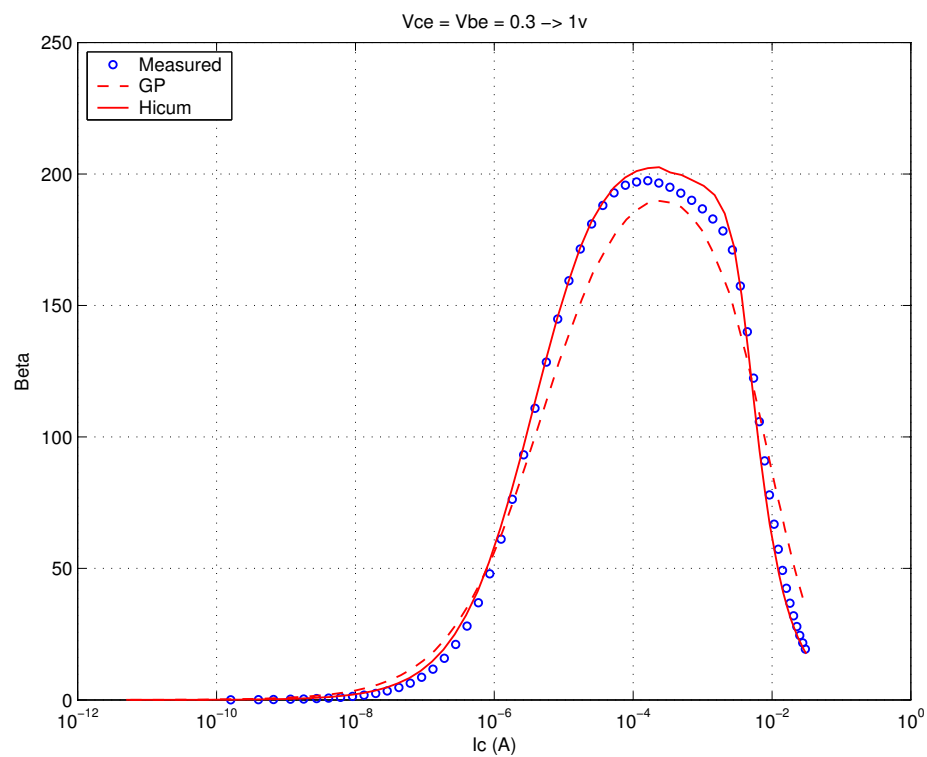


FIGURE 4.125 IC vs. VCE at constant IB: HV 0.9x10.16x1_122

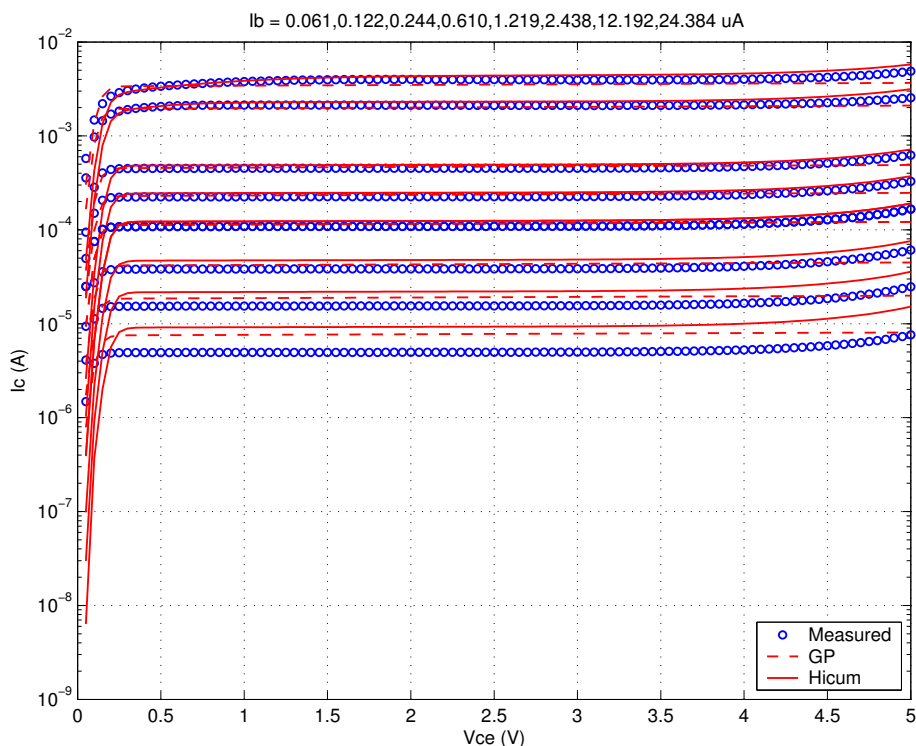


FIGURE 4.126 FT vs. IC: HV 0.9x10.16x1_122

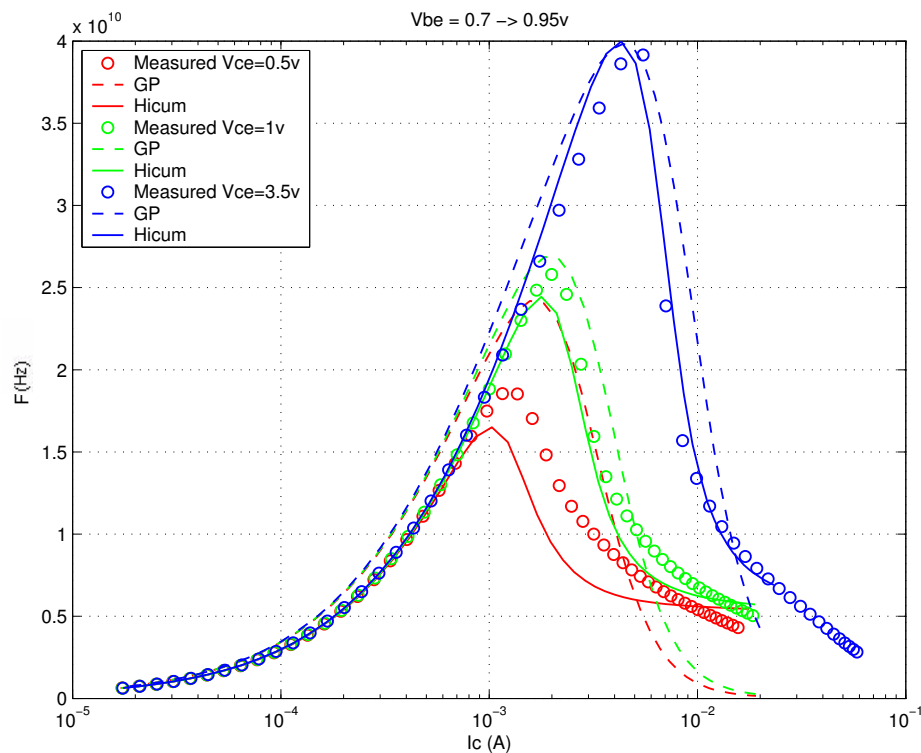
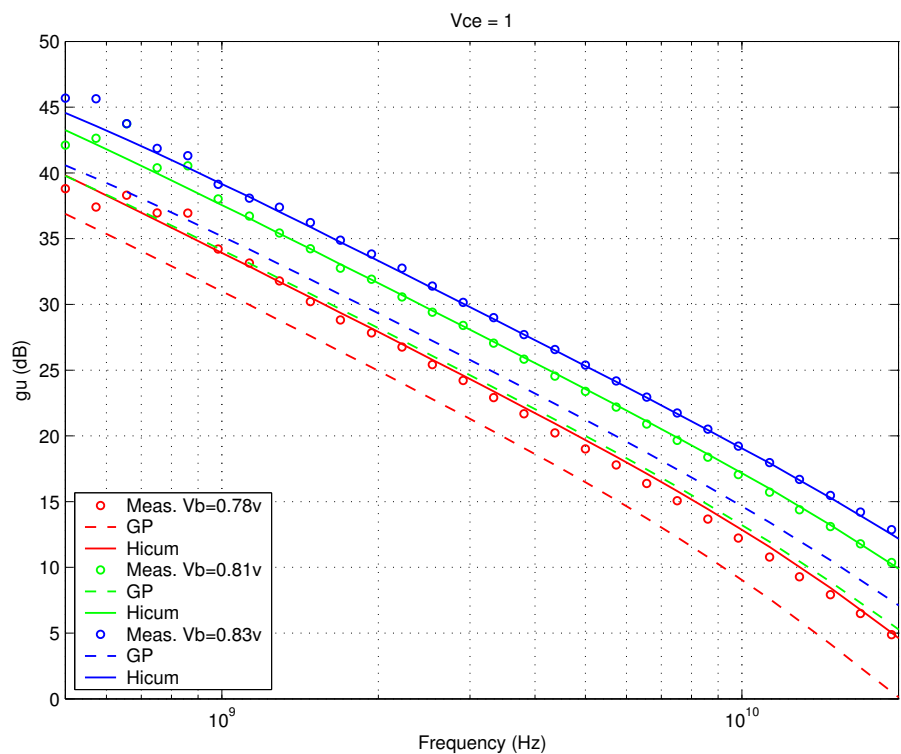


FIGURE 4.127 Power Gain vs. Freq: HV 0.9x10.16x1_122



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FIGURE 4.128 Y-parameters vs. FREQ: HV 0.9x10.16x1_122

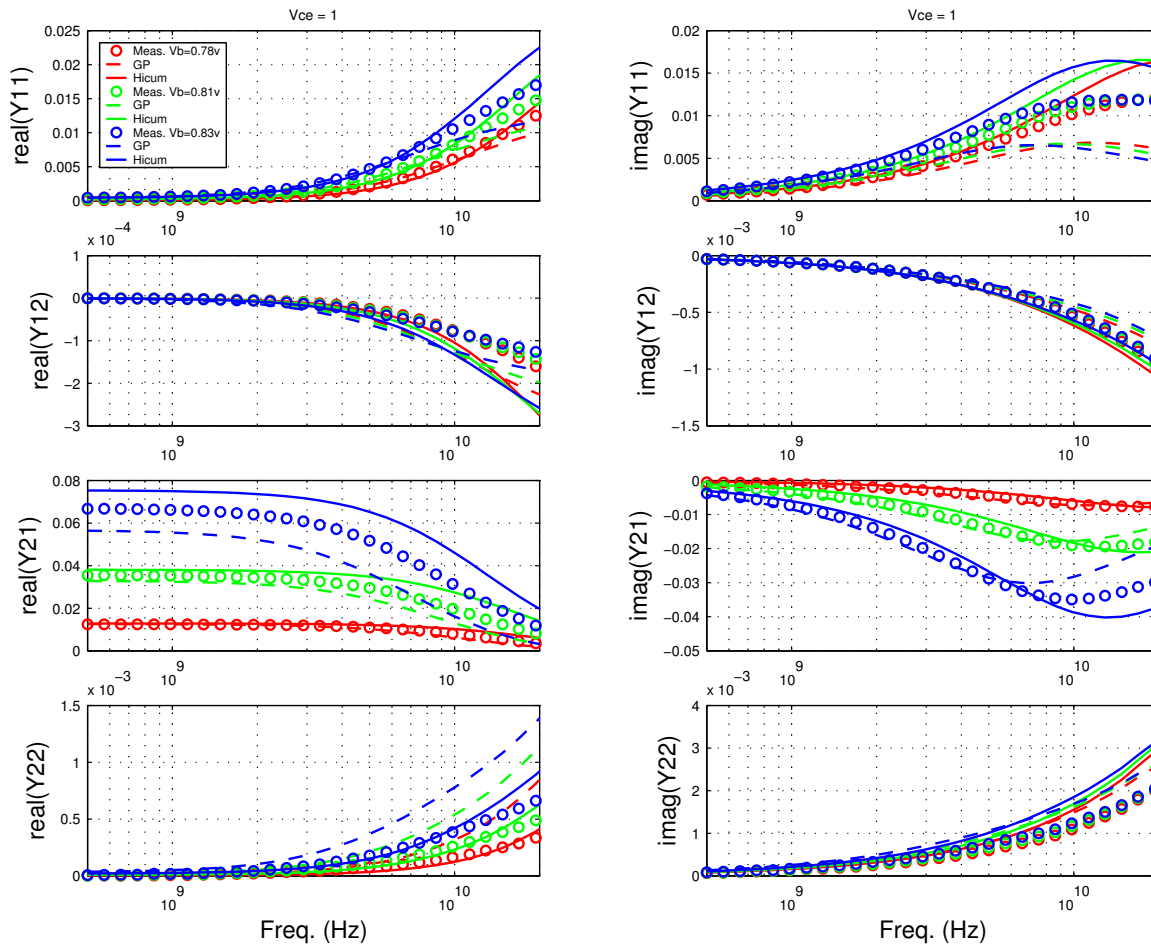


FIGURE 4.129 Gummel Plot: HV 0.2x10.16x1_452

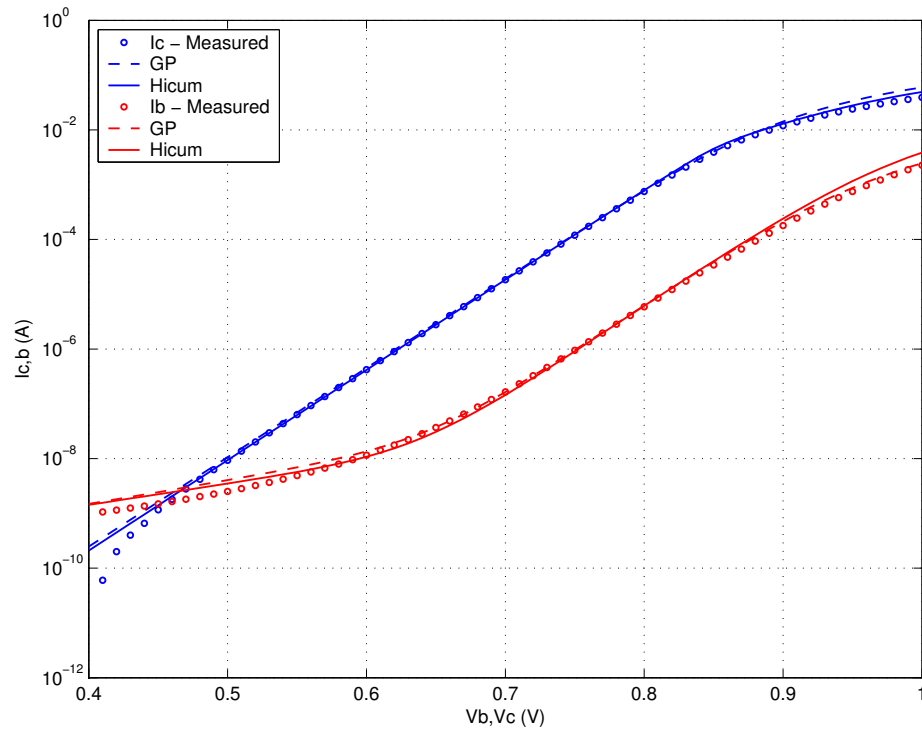
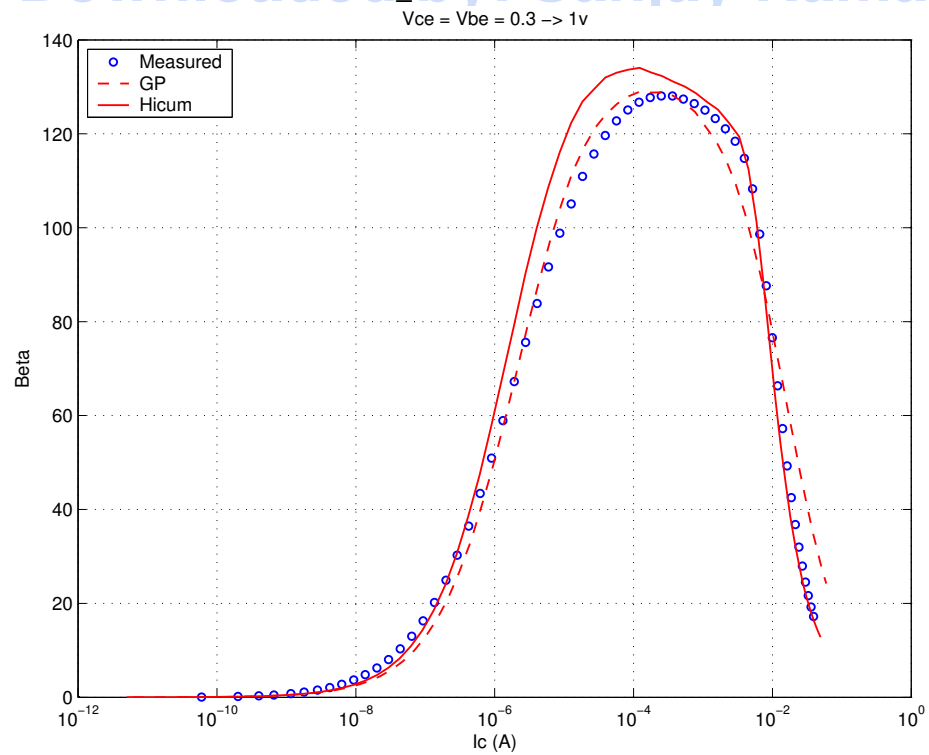
FIGURE 4.130 Beta vs. I_c : HV 0.2x10.16x1_452

FIGURE 4.131 I_C vs. V_{CE} at constant I_B : HV 0.2x10.16x1_452

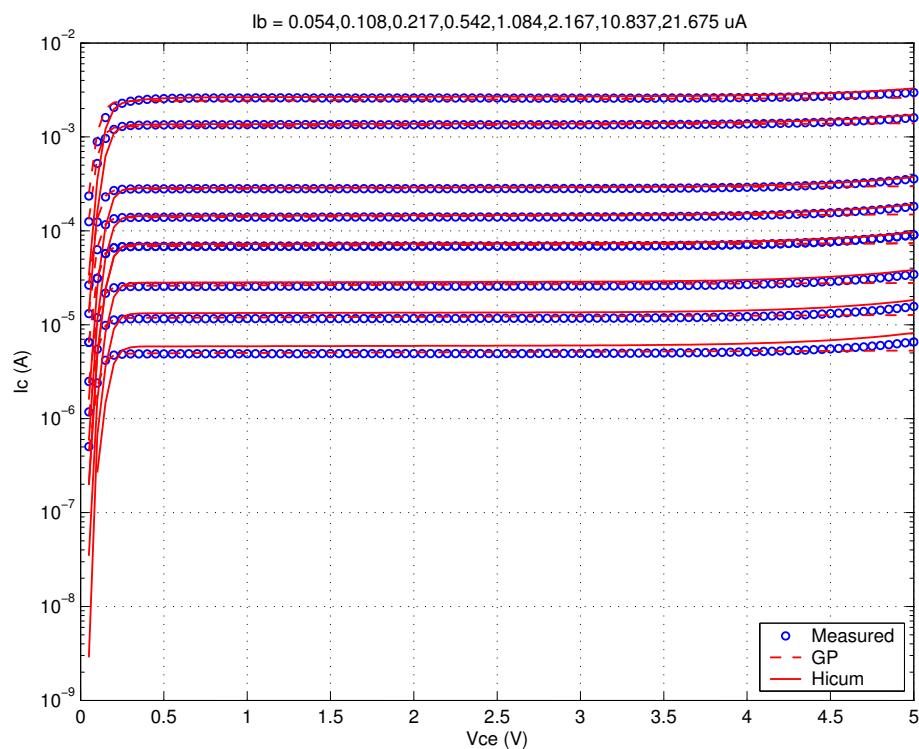


FIGURE 4.132 F_T vs. I_C : HV 0.2x10.16x1_452

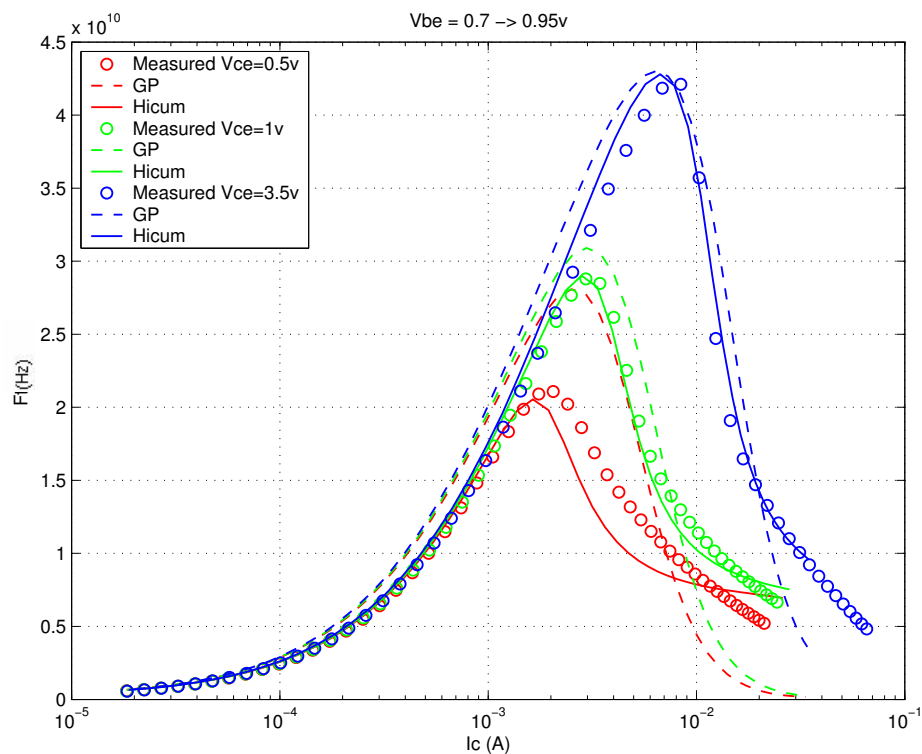
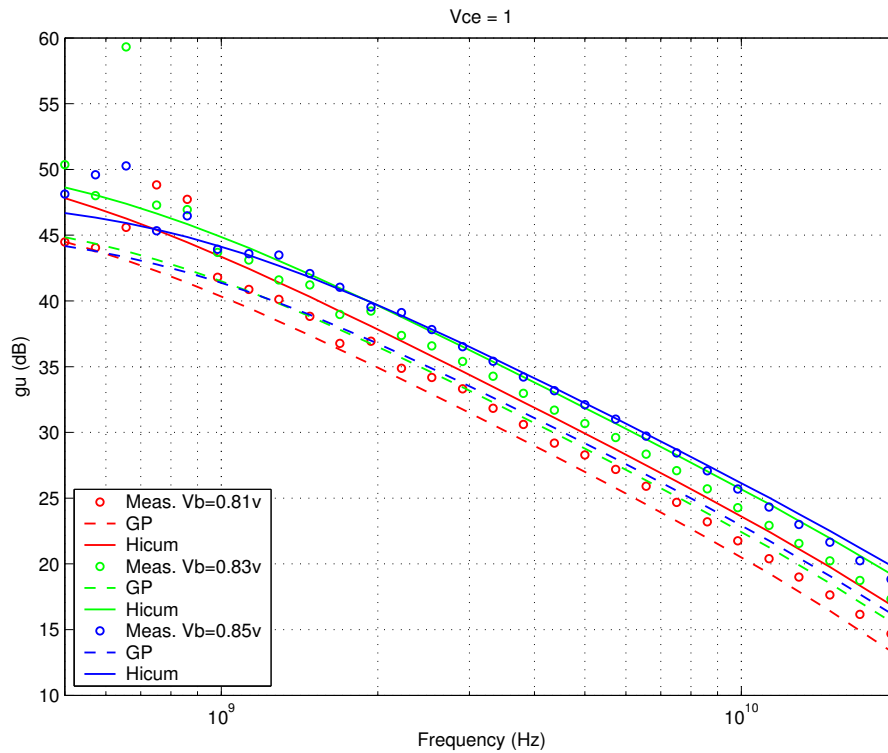


FIGURE 4.133 Power Gain vs. Freq: HV 0.2x10.16x1_452



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FIGURE 4.134 Y-parameters vs. FREQ: HV 0.2x10.16x1_452

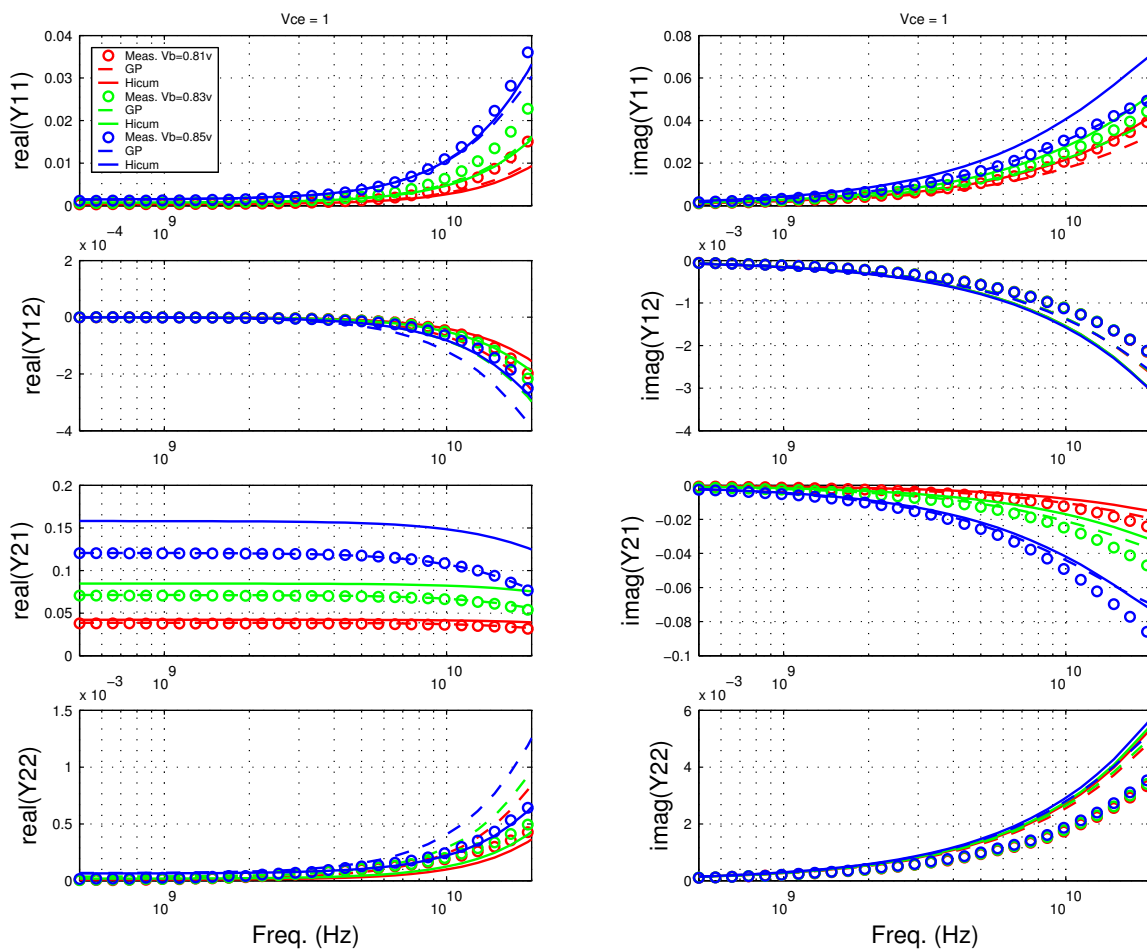


FIGURE 4.135 Gummel Plot HV 0.9x10.16x1_452

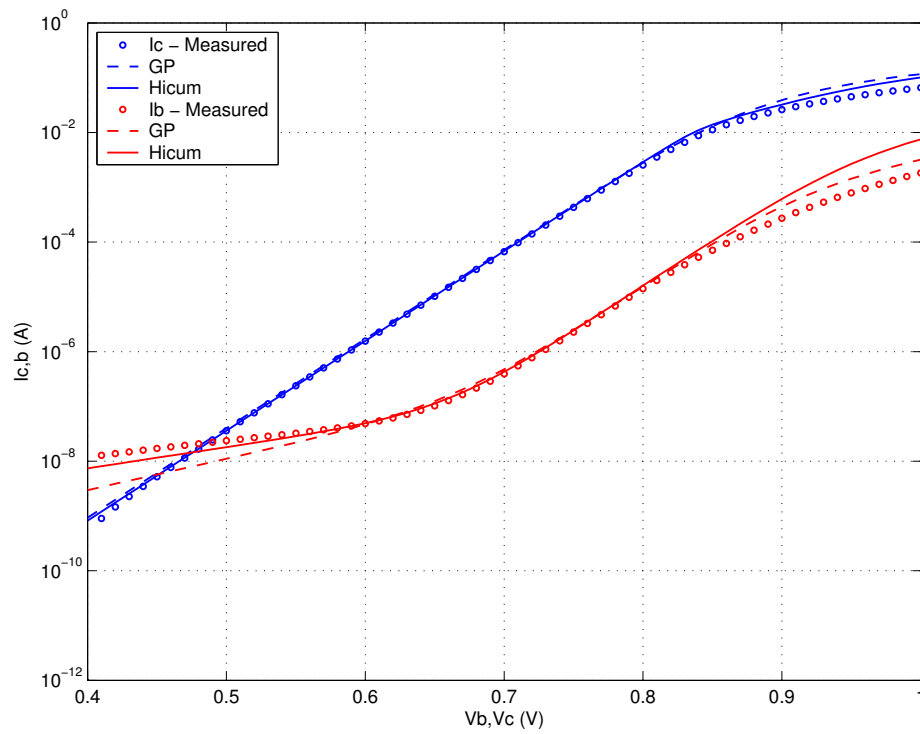
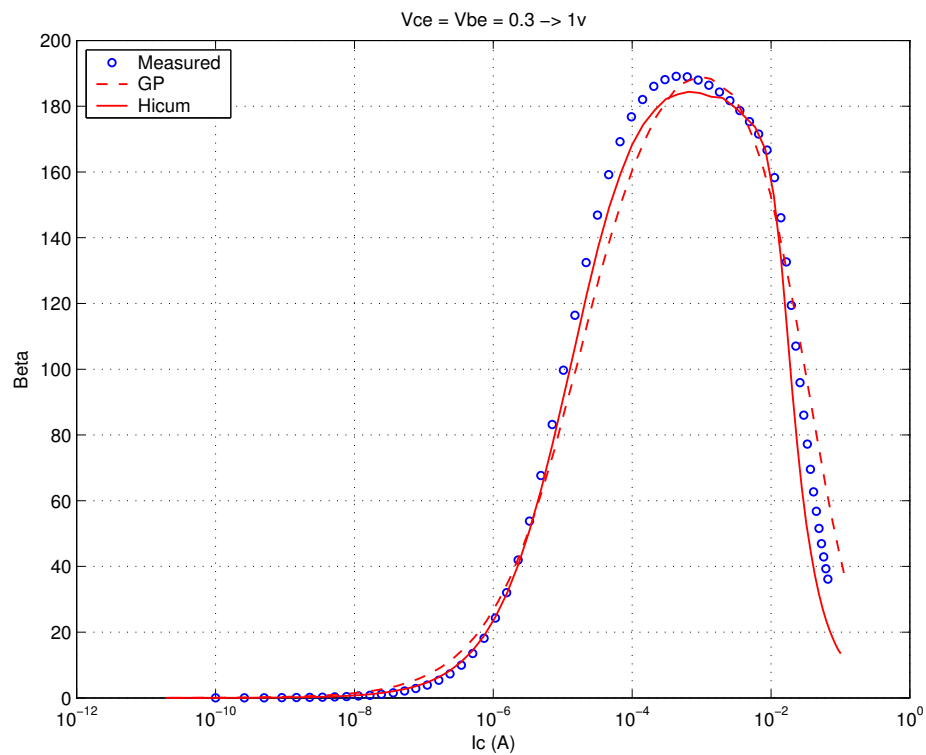
FIGURE 4.136 Beta vs. I_c : HV 0.9x10.16x1_452

FIGURE 4.137 IC vs. VCE at constant IB: HV 0.9x10.16x1_452

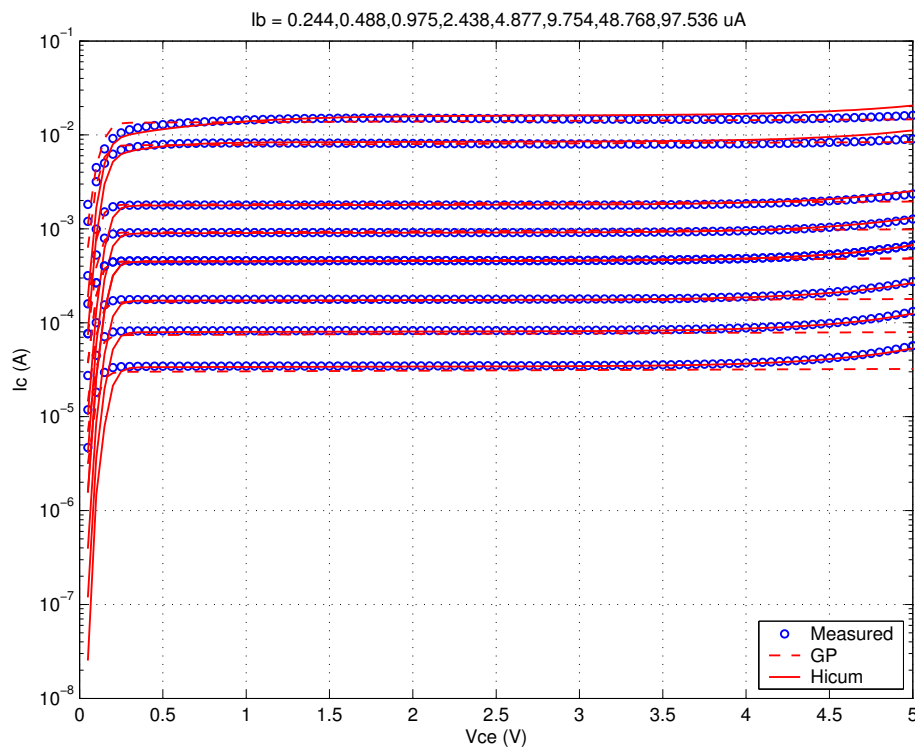


FIGURE 4.138 FT vs. IC: HV 0.9x10.16x1_452

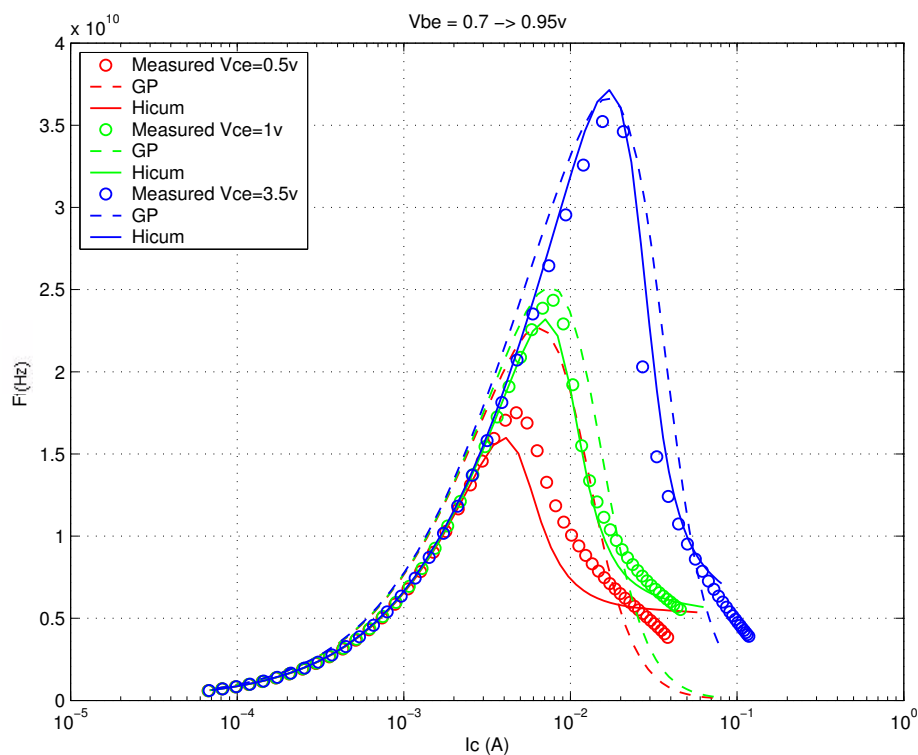
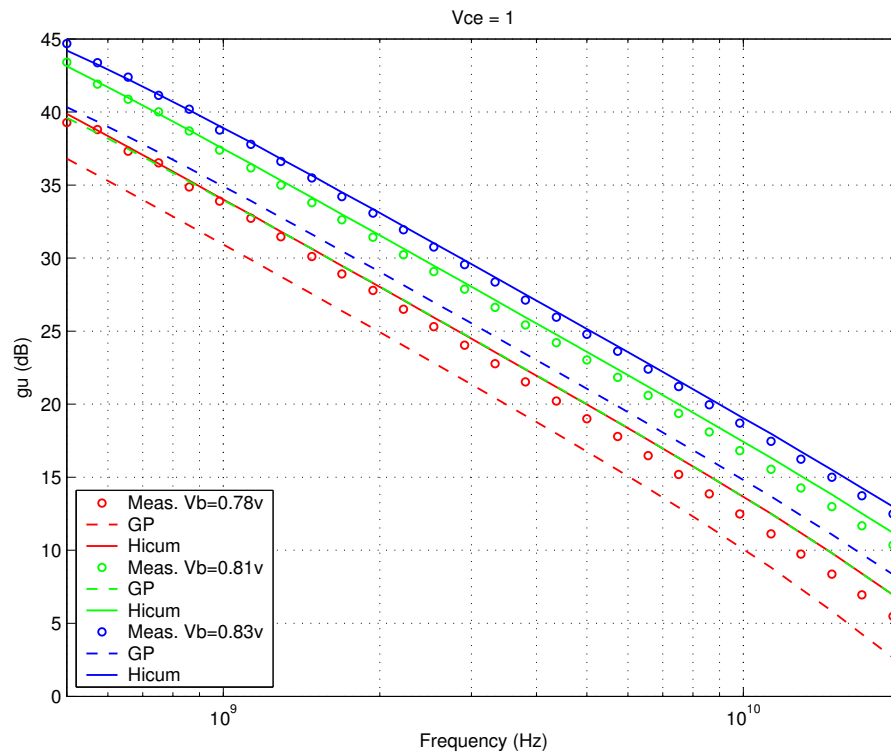
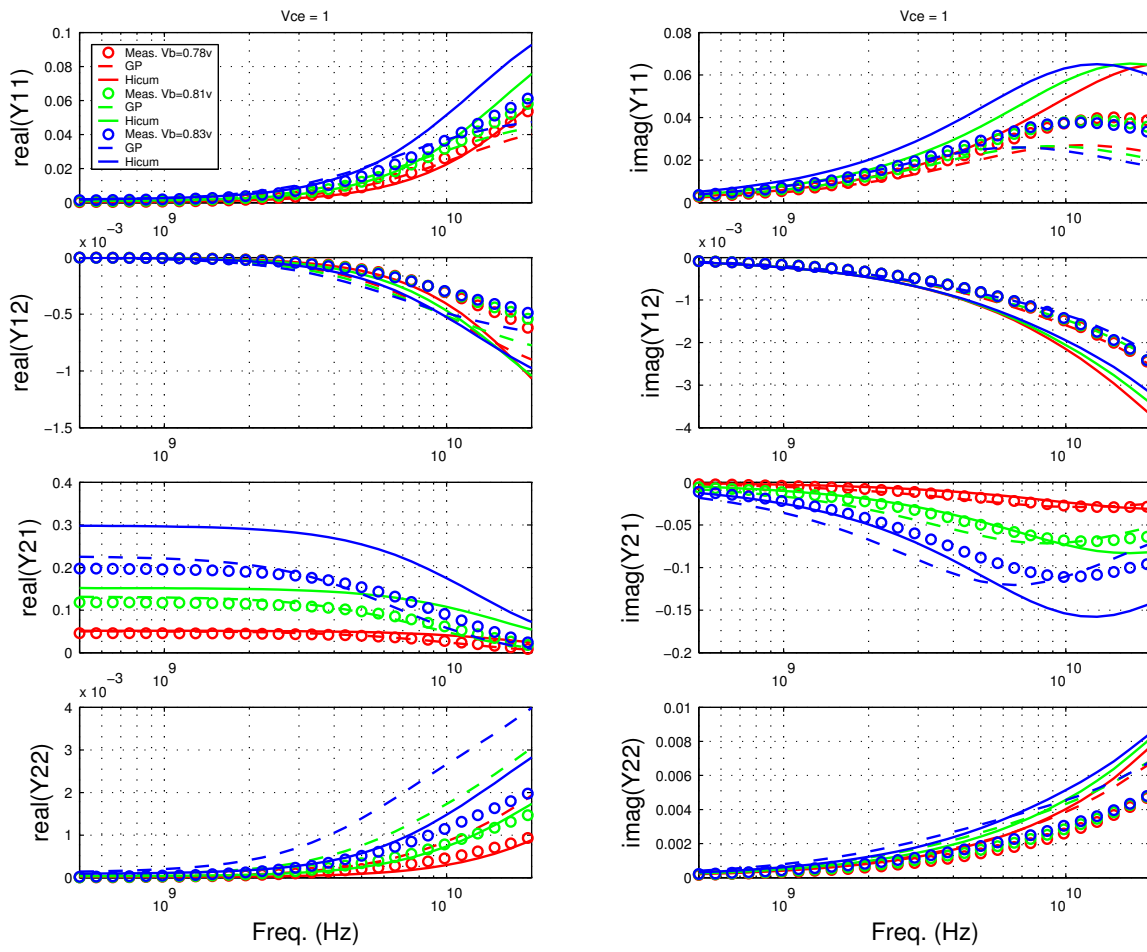


FIGURE 4.139 Power Gain vs. Freq: HV 0.9x10.16x1_452



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Date: 08/15/2012 10:15
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FIGURE 4.140 Y-parameters vs. FREQ: HV 0.9x10.16x1_452



4.5 NPN Statistical and Corner Models

4.5.1 Statistical Model

A detailed description of the Backward Propagation of Variance (BPV) approach to statistical model generation is given in the MOSFET chapter. Only additional information exclusive to the NPN statistical models is given here. Unlike MOSFET models, the map between process and geometry parameters into model parameters is not well defined for NPN models. Mappings between process parameters, model parameters, and geometry parameters must be developed. The stand alone NPN models (Gummel-Poon, VBIC, Hicum, etc.) do not provide the physical correlation of the model parameters. Thus, a set of independent process parameters, rather than model parameters, are defined as the fundamental statistical variables in the simulator. Mappings for the process and geometry parameters into model parameters are developed based on device physics. A handful of process parameter variances are forward propagated in the BPV infrastructure based on expected variances at the process level such as Emitter-Poly CD variations. The remaining process parameter variances are directly BPV'd based on the variances in the ESPECs. A well conditioned system physically and mathematically results, guaranteeing precise simulation of the ESPEC variances and reasonable and consistent statistical simulation of non ESPEC quantities such as base resistance. The process parameters, the propagation technique, the affected model parameters, and target ESPECs for the Spice Gummel-Poon model (SGPM) are listed in Table 4.3. The statistically simulated ESPECs are listed in Table 4.5 - Table 4.7. Refer to the MOSFET chapter for statistical model usage guidelines.

TABLE 4.3 The Process Variables and the Affected Model Parameters in SGPM.

Process Parameters	BPV or FPV	Affected Model Parameters	Target ESPEC for BPV	Mismatch
Emitter Window CD	FPV	RE, RB, RBX, RC, CEOX, CJE, CJC, IS, ISE, BF (GP), IBEIS (Hicum)	NA	IC, BETA
Emitter Poly CD	FPV	CEOX, RBX	NA	
Base Ge doping concentration	BPV	IS (GP), C10 (Hicum)	Vbe at mod. Ic	
Base Boron doping concentration	BPV	CBE, RBI, RBX, IS (GP), C10 (Hicum)	Cbe	
Emitter Si/Poly interface property	BPV	BF (GP), IBEIS (Hicum), RE	Peak Beta	IB
Emitter/Base Junction Leakage	BPV	ISE (GP), IREIS (Hicum)	Beta @ low Vbe	IB @ low Vbe
Emitter doping concentration	BPV	RE, BF (GP), IBEIS (Hicum)	Ic @ Vbe=1.1v	
Substrate doping concentration	BPV	CJS	Ccs	
Base width	BPV	RBI, TF (GP), T0 (Hicum)	Ft of LV & HV dev.	
Local Collector Implant (LV dev.)	BPV	CJC of LV dev.	CBC of LV dev.	
Local Collector Implant (MV dev.)	BPV	CJC of MV dev.	CBC of MV dev.	

4.5.2 Centering

Refer to section 2.6.1 for centering within the BPV framework. The NPN model is extracted from a golden die which measures very close to the nominal of the ESPECs. As a result, the model parameter variation needed to exactly align the model to the nominal ESPECs is small. The simulated NOM ESPECs are listed in Table 4.5 - Table 4.7.

4.5.3 Corner Models

The goal of the corner models are to capture the device electrical performance limits through appropriate variation of the process parameters. Slow and fast corners are provided. Details of the corner models are given in Table 4.4. All the NPN ESPEC limits can not be captured with 2 corners. The target ESPEC parameters for the corner models are I_C , BETA, and F_t . The C_{BE} and C_{CS} ESPECs are also aligned to the ESPECs in the corner model. C_{BC} variation in the corner models is reduced from the ESPEC limit in order to retain consistent and physical F_t prediction. The verification of the simulated corner ESPECs are listed in Table 4.5.

TABLE 4.4 Corner model specifications

	FAST	SLOW
Emitter resistance	Component 1 is higher due to lower I_b (high Beta); Component 2 is lower due to higher emitter doping. Net is ~15% lower	Component 1 is lower due to higher I_b (low Beta); Component 2 is higher due to lower emitter doping. Net is ~15% higher
Extrinsic base resistance	Component 1 is lower (Nom. - 1σ link dist.); Component 2 is higher due to lower base doping (low Cbe). Net is ~10% higher	Component 1 is higher (Nom. + 1σ link dist.); Component 2 is lower due to higher base doping (high Cbe). Net is ~10% lower
Intrinsic base resistance	Component 1 is higher due to shorter base width; Component 2 is higher due to lower base doping (low Cbe). Net is 30% higher	Component 1 is lower due to longer base width; Component 2 is lower due to higher base doping (high Cbe). Net is 30% lower
Base emitter junction cap.	90% of NOM case	110% of NOM case
Base collector junction cap.	Max. case of Cbc	Min. case of Cbc
Collector substrate junction cap.	Min. case of Ccs	Max. case of Ccs
Intrinsic collector resistance	~15% lower; aligned to higher collector doping (higher Cbc)	~15% higher; aligned to lower collector doping (lower Cbc)
Collector saturation current	Min. case of V_{be} for fixed and moderate I_c	Max. case of V_{be} for fixed and moderate I_c
Base current	Max. case of beta (lower I_b)	Min. case of beta (higher I_b)
Base width	Smaller; aligned to max. F_t E-spec.	Larger; aligned to min. F_t E-spec.

TABLE 4.5 Statistical and corner model predictions for 0.2x0.76 μ m 1E1B1C NPNs

Device Model Design-kit name	E-spec. Name	Unit	SLOW			NOM			FAST		
			Espec	Corner	Stat.	Espec	Corner	Stat.	Espec	Corner	Stat.
High-Voltage Gummel-Poon hn01	F_t	GHz	22.20	26.21	30.00	33.20	36.39	36.10	44.20	42.20	42.20
	Cbc	fF	1.35	0.82	0.84	1.50	0.86	0.87	1.65	0.91	0.89
	Beta ¹	A/A	40.00	50.47	52.00	100.00	105.50	106.0	250.00	180.20	160.00
	Ccs ²	fF	4.80	4.78	4.68	4.00	3.98	4.02	3.20	3.19	3.36
	Ccs_nodt	fF	12.00	11.94	11.70	10.00	9.94	10.00	8.00	7.97	8.34
	Cbe ³	fF	2.90	3.42	3.63	2.50	3.41	3.42	2.10	3.31	3.21
	I_c	μ A	0.12	0.12	0.12	0.32	0.26	0.27	0.52	0.44	0.41

TABLE 4.5 Statistical and corner model predictions for 0.2x0.76µm 1E1B1C NPNs

Device Model Design-kit name	E-spec. Name	Unit	SLOW			NOM			FAST		
			Espec	Corner	Stat.	Espec	Corner	Stat.	Espec	Corner	Stat.
High-Voltage Hicum hn01_hicum	Ft	GHz	22.20	27.10	32.70	33.20	37.49	37.10	44.20	43.05	41.50
	Cbc	fF	1.35	1.45	1.46	1.50	1.50	1.50	1.65	1.59	1.54
	Beta ¹	A/A	40.00	48.44	53.10	100.00	116.80	117.0	250.00	245.10	181.00
	Ccs ²	fF	4.80	4.77	4.70	4.00	4.00	4.04	3.20	3.18	3.38
	Ccs_nodt	fF	12.00	11.92	11.80	10.00	10.00	10.10	8.00	7.95	8.44
	Cbe ³	fF	2.90	2.49	2.62	2.50	2.44	2.45	2.10	2.40	2.28
	Ic	µA	0.12	0.12	0.13	0.32	0.27	0.28	0.52	0.45	0.42
Standard Gummel-Poon ln01	Ft	GHz	57.00	57.66	63.60	72.00	75.24	74.90	87.00	84.97	86.20
	Cbc	fF	1.80	1.14	1.17	2.00	1.23	1.23	2.20	1.40	1.29
	Beta ¹	A/A	40.00	54.07	56.30	100.00	114.90	116.0	250.00	193.00	176.00
	Ccs ²	fF	4.80	4.78	4.68	4.00	3.98	4.02	3.20	3.19	3.36
	Ccs_nodt	fF	12.00	11.94	11.70	10.00	9.94	10.00	8.00	7.97	8.34
	Cbe ³	fF	2.90	3.51	3.64	2.50	3.43	3.43	2.10	3.33	3.22
	Ic	µA	0.12	0.13	0.13	0.32	0.28	0.28	0.52	0.45	0.42
Standard Hicum ln01_hicum	Ft	GHz	57.00	60.35	64.10	72.00	70.77	70.70	87.00	77.01	77.30
	Cbc	fF	1.80	1.87	1.92	2.00	2.01	2.01	2.20	2.14	2.10
	Beta ¹	A/A	40.00	52.30	54.40	100.00	117.20	118.0	250.00	244.90	182.00
	Ccs ²	fF	4.80	4.77	4.70	4.00	4.00	4.04	3.20	3.18	3.38
	Ccs_nodt	fF	12.00	11.92	11.80	10.00	10.00	10.10	8.00	7.95	8.44
	Cbe ³	fF	2.90	2.67	2.78	2.50	2.60	2.60	2.10	2.55	2.42
	Ic	µA	0.12	0.12	0.13	0.32	0.26	0.27	0.52	0.43	0.40
High-speed Gummel-Poon dn01	Ft	GHz	110.00	114.50	131.0	134.00	153.60	153.0	158.00	186.60	175.00
	Cbc	fF	2.90	2.97	3.10	3.20	3.25	3.26	3.50	3.53	3.42
	Beta ¹	A/A	40.00	48.06	60.50	100.00	115.00	116.0	250.00	249.20	172.00
	Ccs	fF	4.80	4.78	4.68	4.00	3.98	4.02	3.20	3.19	3.36
	Cbe ³	fF	3.00	3.46	3.60	2.60	3.40	3.40	2.20	3.29	3.20
	Ic	µA	0.12	0.12	0.14	0.32	0.26	0.27	0.52	0.43	0.40
High-speed Hicum dn01_hicum	Ft	GHz	110.00	95.84	95.50	134.00	102.40	103.0	158.00	105.50	110.00
	Cbc	fF	2.90	2.98	3.07	3.20	3.22	3.23	3.50	3.52	3.39
	Beta ¹	A/A	40.00	44.59	50.40	100.00	101.10	120.0	250.00	264.80	190.00
	Ccs	fF	4.80	4.77	4.70	4.00	4.00	4.04	3.20	3.18	3.38
	Cbe ³	fF	3.00	2.83	2.94	2.60	2.77	2.77	2.20	2.68	2.60
	Ic	µA	0.12	0.10	0.12	0.32	0.23	0.23	0.52	0.38	0.34

TABLE 4.6 Statistical and corner model predictions for 0.2x10.16μm 1E2B2C NPNs

Device Model Design-kit name	E-spec. Name	Unit	SLOW			NOM			FAST		
			Espec	Corner	Stat.	Espec	Corner	Stat.	Espec	Corner	Stat.
High-Voltage Gummel-Poon hn112c2	Ft	GHz	34.00	27.73	32.50	38.00	38.03	37.90	42.00	43.76	43.30
	Fmax ⁴	GHz	NA	94.16	104.0	183.00	119.90	119.0	NA	135.60	134.00
	Fmax_nodt	GHz	NA	75.41	88.10	120.00	103.40	103.0	NA	123.80	118.00
	Cbc	fF	7.60	7.50	7.59	8.00	7.78	7.78	8.40	8.10	7.97
	Beta ¹	A/A	60.00	60.34	60.80	140.00	140.70	140.0	300.00	302.40	219.00
	Ccs ²	fF	19.20	19.20	18.80	16.00	15.98	16.10	12.80	12.80	13.40
	Ccs_nodt	fF	48.00	47.99	47.00	40.00	39.95	40.30	32.00	32.01	33.60
	Cbe ³	fF	30.00	31.00	32.70	27.00	30.79	30.80	24.00	29.50	28.90
	Ic	μA	1.50	2.00	1.97	4.20	4.20	4.23	6.90	6.90	6.49
High-Voltage Hicup hn112c2_hicup	Ft	GHz	34.00	29.65	34.10	38.00	37.92	37.80	42.00	42.98	41.50
	Fmax ⁴	GHz	NA	152.60	161.0	183.00	176.30	177.0	NA	190.40	193.00
	Fmax_nodt	GHz	NA	126.20	144.0	120.00	160.20	160.0	NA	180.50	176.00
	Cbc	fF	7.60	7.70	7.78	8.00	7.96	7.97	8.40	8.40	8.16
	Beta ¹	A/A	60.00	58.51	64.10	140.00	139.70	140.0	300.00	295.30	216.00
	Ccs ²	fF	19.20	19.21	19.00	16.00	16.10	16.30	12.80	12.80	13.60
	Ccs_nodt	fF	48.00	48.01	47.40	40.00	40.26	40.70	32.00	32.01	34.00
	Cbe ³	fF	30.00	27.48	28.70	27.00	26.79	26.80	24.00	26.12	24.90
	Ic	μA	1.50	1.92	1.97	4.20	4.20	4.22	6.90	6.92	6.47
Standard Gummel-Poon In112c2	Ft	GHz	70.00	65.24	70.10	78.00	78.77	78.70	86.00	86.16	87.30
	Fmax ⁴	GHz	NA	149.80	152.0	284.00	161.10	161.0	NA	163.30	170.00
	Fmax_nodt	GHz	NA	117.70	126.0	201.00	138.90	138.0	NA	148.90	150.00
	Cbc	fF	10.60	9.00	9.08	11.20	9.45	9.46	11.80	10.24	9.84
	Beta ¹	A/A	60.00	60.43	60.50	140.00	139.90	140.0	300.00	306.20	220.00
	Ccs ²	fF	19.20	19.20	18.80	16.00	15.98	16.10	12.80	12.80	13.40
	Ccs_nodt	fF	48.00	47.99	47.00	40.00	39.95	40.30	32.00	32.01	33.60
	Cbe ³	fF	32.00	31.80	32.90	29.00	30.80	30.90	26.00	29.60	28.90
	Ic	μA	1.50	2.00	2.02	4.20	4.20	4.24	6.90	6.90	6.46
Standard Hicup In112c2_hicup	Ft	GHz	70.00	68.24	70.50	78.00	78.08	78.00	86.00	86.01	85.50
	Fmax ⁴	GHz	NA	334.70	287.0	284.00	314.60	314.0	NA	302.50	341.00
	Fmax_nodt	GHz	NA	266.10	260.0	201.00	282.20	282.0	NA	286.50	304.00
	Cbc	fF	10.60	10.60	10.80	11.20	11.19	11.20	11.80	11.80	11.60
	Beta ¹	A/A	60.00	63.02	65.70	140.00	139.90	141.0	300.00	293.50	216.00
	Ccs ²	fF	19.20	19.21	19.00	16.00	16.10	16.30	12.80	12.80	13.60
	Ccs_nodt	fF	48.00	48.01	47.40	40.00	40.26	40.70	32.00	32.01	34.00
	Cbe ³	fF	32.00	29.90	30.90	29.00	28.81	28.90	26.00	28.10	26.90
	Ic	μA	1.50	1.94	2.04	4.20	4.20	4.25	6.90	6.92	6.46

TABLE 4.6 Statistical and corner model predictions for 0.2x10.16µm 1E2B2C NPNs

Device Model Design-kit name	E-spec. Name	Unit	SLOW			NOM			FAST		
			Espec	Corner	Stat.	Espec	Corner	Stat.	Espec	Corner	Stat.
High-speed Gummel-Poon dn112c2	Ft	GHz	135.00	130.30	135.0	150.00	150.00	150.0	165.00	167.50	165.00
	Fmax ⁴	GHz	NA	177.50	172.0	190.00	180.70	181.0	NA	177.60	190.00
	Cbc	fF	17.20	18.00	18.00	18.70	18.99	19.00	20.20	20.20	20.00
	Beta ¹	A/A	60.00	58.32	72.60	140.00	139.80	141.0	300.00	304.80	209.00
	Ccs	fF	19.20	19.20	18.80	16.00	15.98	16.10	12.80	12.80	13.40
	Cbe ³	fF	33.00	31.50	32.60	30.00	30.77	30.80	27.00	29.50	29.00
	Ic	µA	1.50	1.90	2.18	4.20	4.20	4.25	6.90	6.90	6.32
High-speed Hicum dn112c2_hicum	Ft	GHz	135.00	135.10	135.0	150.00	150.00	151.0	165.00	165.80	167.00
	Fmax ⁴	GHz	NA	185.10	145.0	190.00	177.20	17.00	NA	158.70	209.00
	Cbc	fF	17.20	17.70	17.80	18.70	18.77	18.80	20.20	20.20	19.80
	Beta ¹	A/A	60.00	51.78	56.90	140.00	116.90	143.0	300.00	310.80	229.00
	Ccs	fF	19.20	19.21	19.00	16.00	16.10	16.30	12.80	12.80	13.60
	Cbe ³	fF	33.00	31.40	32.30	30.00	30.48	30.50	27.00	29.20	28.70
	Ic	µA	1.50	1.93	2.18	4.20	4.20	4.25	6.90	6.95	6.32

TABLE 4.7 Statistical and corner model predictions for 0.9x10.16µm 1E2B2C NPNs

Device Model Design-kit name	E-spec. Name	Unit	SLOW			NOM			FAST		
			Espec	Corner	Stat.	Espec	Corner	Stat.	Espec	Corner	Stat.
High-Voltage Gummel-Poon hw112c2	Ft	GHz	27.50	24.05	27.20	32.50	32.33	32.50	36.50	36.70	37.80
	Fmax ⁴	GHz	NA	54.92	55.50	88.00	59.57	59.50	NA	59.74	63.50
	Fmax_nodt	GHz	NA	52.35	54.30	70.00	58.58	58.40	NA	59.29	62.50
	Cbc	fF	8.50	10.10	9.58	10.40	10.39	10.40	12.30	10.90	11.20
	Beta ¹	A/A	60.00	57.46	68.80	160.0	160.50	160.0	300.0	302.40	251.0
	Ccs ²	fF	20.80	20.79	20.40	17.40	17.41	17.60	14.00	14.02	14.80
	Ccs_nodt	fF	52.00	51.97	51.00	43.50	43.54	44.00	34.50	35.05	37.00
	Cbe ³	fF	100.0	99.00	107.0	90.00	96.49	96.70	80.00	92.00	86.90
	Ic	µA	3.90	5.69	6.21	15.80	15.80	15.90	27.70	27.69	25.60
High-Voltage Hicum hw112c2_hicum	Ft	GHz	27.50	25.13	28.20	32.50	32.46	32.30	36.50	36.83	36.30
	Fmax ⁴	GHz	NA	86.95	85.50	88.00	90.23	91.60	NA	91.86	97.70
	Fmax_nodt	GHz	NA	84.11	84.20	70.00	88.99	90.10	NA	90.96	96.00
	Cbc	fF	8.50	11.10	10.70	10.40	11.47	11.50	12.30	11.90	12.30
	Beta ¹	A/A	60.00	56.19	67.10	160.0	160.70	161.0	300.0	329.20	255.0
	Ccs ²	fF	20.80	20.80	20.40	17.40	17.43	17.60	14.00	13.99	14.80
	Ccs_nodt	fF	52.00	52.01	51.10	43.50	43.57	44.00	34.50	34.98	36.90
	Cbe ³	fF	100.0	93.00	100.0	90.00	90.23	90.50	80.00	86.00	80.60
	Ic	µA	3.90	5.82	6.17	15.80	15.80	15.80	27.70	27.43	25.40

TABLE 4.7 Statistical and corner model predictions for 0.9x10.16μm 1E2B2C NPNs

Device Model Design-kit name	E-spec. Name	Unit	SLOW			NOM			FAST		
			Espec	Corner	Stat.	Espec	Corner	Stat.	Espec	Corner	Stat.
Standard Gummel-Poon lw112c2	Ft	GHz	55.00	50.72	55.70	63.00	63.16	63.30	71.00	72.41	70.90
	Fmax ⁴	GHz	NA	64.29	60.80	121.0	64.42	64.40	NA	62.88	68.00
	Fmax_nodt	GHz	NA	60.96	59.40	104.0	62.89	62.80	NA	62.13	66.20
	Cbc	fF	18.80	15.40	15.40	16.40	16.39	16.40	14.00	17.60	17.40
	Beta ¹	A/A	60.00	57.68	72.50	160.0	160.50	161.0	300.0	327.00	250.0
	Ccs ²	fF	20.80	20.79	20.40	17.40	17.41	17.60	14.00	14.02	14.80
	Ccs_nodt	fF	52.00	51.97	51.00	43.50	43.54	44.00	34.50	35.05	37.00
	Cbe ³	fF	110.0	100.50	107.0	100.0	96.49	96.70	90.00	92.00	86.90
	Ic	μA	3.90	5.70	6.49	15.80	15.80	16.00	27.70	27.70	25.50
Standard Hicup lw112c2_hicup	Ft	GHz	55.00	53.91	55.20	63.00	62.78	63.60	71.00	70.61	72.00
	Fmax ⁴	GHz	NA	127.60	116.0	121.0	124.50	125.0	NA	122.00	134.0
	Fmax_nodt	GHz	NA	122.90	114.0	104.0	122.50	123.0	NA	120.90	132.0
	Cbc	fF	18.80	16.40	16.50	16.40	17.45	17.50	14.00	18.60	18.50
	Beta ¹	A/A	60.00	56.66	70.10	160.0	159.30	161.0	300.0	318.10	252.0
	Ccs ²	fF	20.80	20.80	20.40	17.40	17.43	17.60	14.00	13.99	14.80
	Ccs_nodt	fF	52.00	52.01	51.10	43.50	43.57	44.00	34.50	34.98	36.90
	Cbe ³	fF	110.0	103.00	109.0	100.0	99.28	99.50	90.00	95.00	89.70
	Ic	μA	3.90	5.90	6.62	15.80	15.80	16.10	27.70	26.96	25.60

Notes:

1. Beta: The beta E-spec is asymmetrical across the NOM case. The statistical model prediction is +/- 3 sigma and is thus symmetrical across NOM.
2. Ccs: Two different values are specified for the collector to substrate capacitance. The first is for processes with deep trench (DT) isolation, while the second higher value is for processes without deep trench isolation.
3. Cbe: Cbe variation in the corner models is reduced from the ESPEC limit in order to retain consistent and physical Ft prediction.
4. Fmax: Only nominal E-spec for variants with and without deep-trench are specified. Corner and statistical model predictions are shown for processes with and without DT isolation. This parameter is not a BPV targeted E-spec for corner or statistical model extraction.

4.6 NPN Mismatch Model

The mismatch model captures the local variation between identical devices. The collector current and the current gain (Beta) mismatch between two identical NPNs (~10μm apart) with identical V_{BE} and V_{CE} are characterized and captured in the mismatch model.

NPN mismatch is characterized in terms of percentage difference in Beta (β) and I_C. The I_C mismatch percentage is calculated using the following expression:

$$\Delta I_C = 100 \times \frac{I_{C1} - I_{C2}}{I_{C1}} \quad (\text{EQ 1})$$

The β mismatch is calculated using the following expression:

$$\Delta \beta = 100 \times \frac{\beta_1 - \beta_2}{\beta_1} \quad (\text{EQ 2})$$

The Ge concentration and EW CD mismatch sigmas are used to fit the I_C mismatch. The emitter surface recombination velocity sigma fits the additional mismatch seen in the β measurements. In operational regions where I_C and β are not affected by series resistance, low or high bias effects, NPN mismatch can be adequately represented with the aforementioned process parameters, combined with an inverse square root dependence on active emitter area.

Figure 4.141 through Figure 4.143 show the I_C and β mismatch for the SBC18 NPNs. Discrepancies in low current I_C mismatch are due to leakage current mismatch and are not modelled.

FIGURE 4.141 Measured and simulated I_C and Beta mismatch plots of High-voltage NPNs

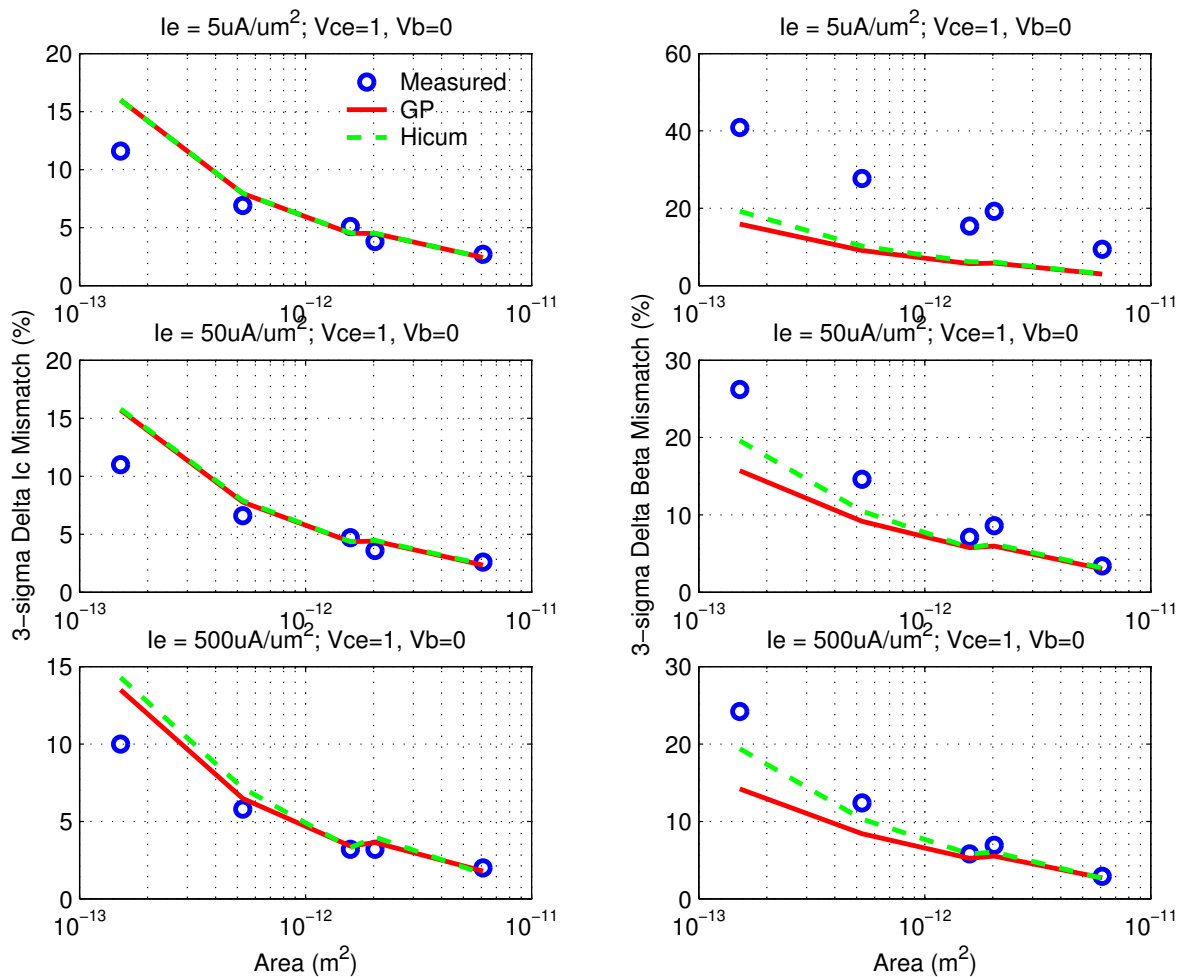


FIGURE 4.142 Measured and simulated I_c and Beta mismatch plots of Standard NPNs

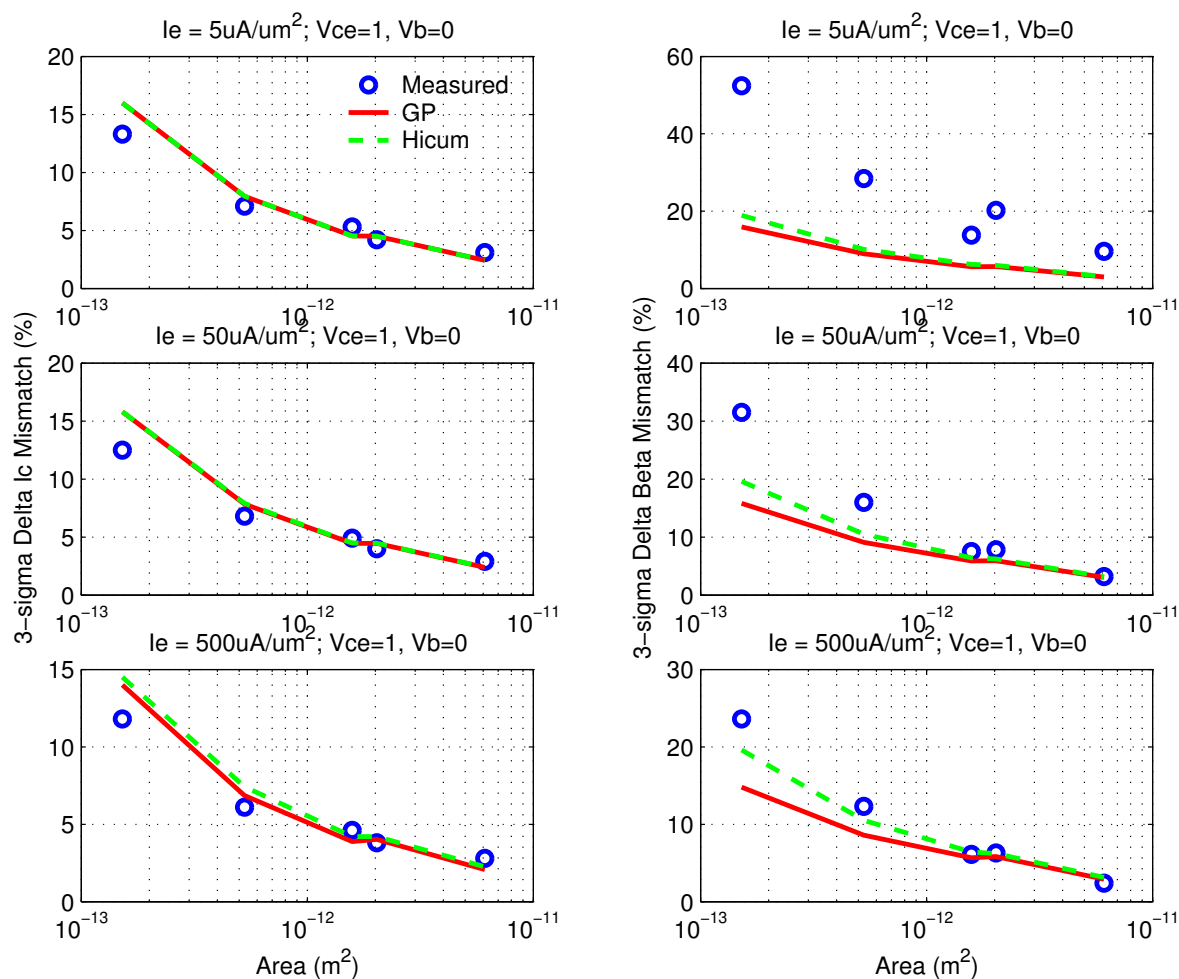
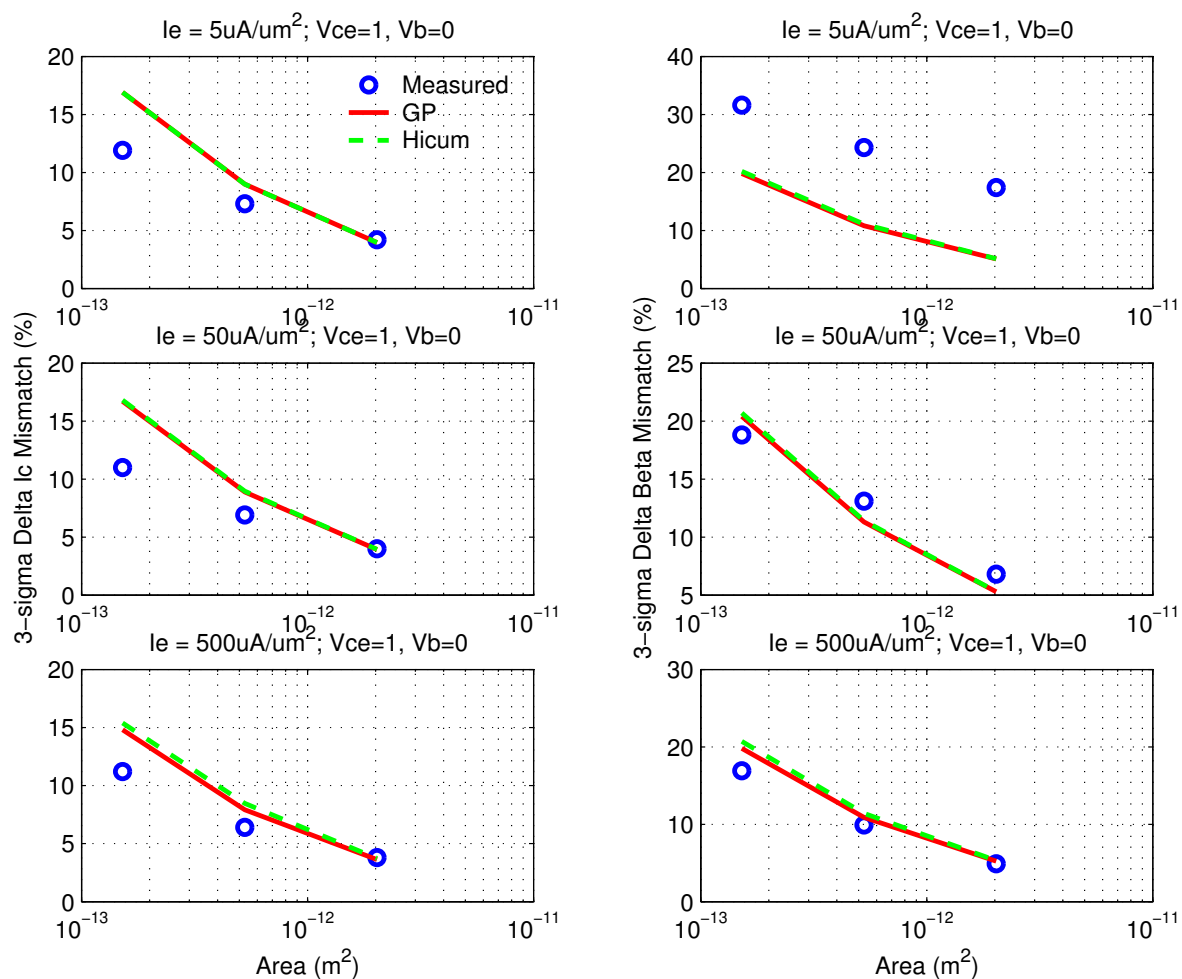


FIGURE 4.143 Measured and simulated I_c and Beta mismatch plots of High-Speed NPNs

4.7 8V NPN Support

The L-scalable 8V NPN hicup models are now supported in the sbc18qpa versions of design kit. Model validation will be provided in a subsequent update of this document.

4.8 Model Update History

The following tables list the model updates with each revision. Unlisted model revisions indicate that no changes have occurred in that revision.

TABLE 4.8 NPN model specific updates in model release version 4.9

v4.9 update	Devices	Reason	Impact on user
Improved alignment of statistical model and corner models to ESPEC	All	Improve process variation modeling	Capacitance parameters and base resistance corners modified. NOM models largely unchanged.

TABLE 4.9 NPN model specific updates in model release version 6.0

v6.0 update	Devices	Reason	Impact on user
X-Sigma corner model support	All NPNs	Allow for process variation settings different than conventional +/- 3 sigma corner models	Added flexibility in corner simulation
Updated temperature co-coefficients of parasitic resistors (Re, Rb) in Hicup	Hicup NPNs	Align to Gummel-Poon model and measurements	No change for room temperature simulations 5-10% increase in Re and Rb at 125C 5-10% decrease in Re and Rb at -40C
New FAST/SLOW corners ¹ for 1. Rb based on Cbe (base doping) variation 2. Re based on high-Vbe Ic 3. High-current Ft/Beta degradation parameters and Rc that change physically with Cbc (collector doping)	All NPNs	Improved correlation between model parameters Better match to Espec corner values	No change to NOM Gummel-Poon model NOM Hicup model largely unchanged (see above row) Base resistance is higher (was lower in previous version) for FAST case and lower (was higher in previous version) in SLOW case. The magnitude of the spread from FAST to SLOW is about the same as the previous version Spread in Emitter resistance is about +/- 25% (was +/- 20% in previous version) Collector resistance spread is about +/- 10% (no spread in previous version). This increases the Ft/Beta degradation vs. collector current at high collector current for the FAST case, and vice-versa for the SLOW case.

TABLE 4.10 NPN model specific updates in model release version 6.2

v6.2 update	Devices	Reason	Impact on user
Re-extracted NPN model parameters	All	Reflects most recent hardware	Ideal NPN current is reduced by approximately 12%. Beta remains unchanged. The high-speed device had a reduction in Ft from 155 to 150GHz.
Re-centered NOM, SLOW, and FAST corners and statistical models to new E-specs	All	Reflects most recent Fab data	Better hardware to model correlation
Improved modeling of quasi-saturation and high-current regime	All	Improved model to hardware correlation	

TABLE 4.11 NPN model specific updates in model release version 6.2a

v6.2a-d update	Devices	Reason	Impact on user
Updated NPN mismatch	All	Fixed syntax error in NPN mismatch code	
Added switch to include thermal resistance effect in NPN models	All	Add more flexibility to the NPN models	Can select whether or not to include thermal resistance (RTH) modeling

TABLE 4.12 NPN model specific updates in model release version 6.3

v6.3 update	Devices	Reason	Impact on user
Re-formated models to support I-scalable NPNs. Changed emitter length variable from "eml" to "l"	All SiGe NPNs	Align to PDK that now supports I-scalable SiGe NPNs	Improved flexibility in choosing and optimizing SiGe NPN transistor size

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5.0 SBC18H2 Bipolar Model

5.1 Device Description

The SBC18H2 200GHz process offers 2 NPN device types, low and medium voltage, differentiated by BV_{CEO} and F_t targets listed in Table 5.1. These devices are exclusive to SBC18H2 and cannot coexist with the npn devices described in Chapter 4.0. A cross section of a high-speed NPN device is shown in Figure 5.1.

Figure 5.2 shows the layout of a 1 emitter, 2 base, 1 collector configuration. Layout configurations are further described in Section 5.2.

TABLE 5.1 SBC18H2 NPN Specification by BV_{CEO} and F_t

NPN	BV_{CEO} (V)	F_t (GHz)	Design Kit Name	Model Name
low voltage	1.9	200	nnp	ln[1,2][1,2,3][1,2]_hicum
medium voltage	3.2	75	nnp	mn[1,2][1,2,3][1,2]_hicum

FIGURE 5.1 Cross Section of NPN

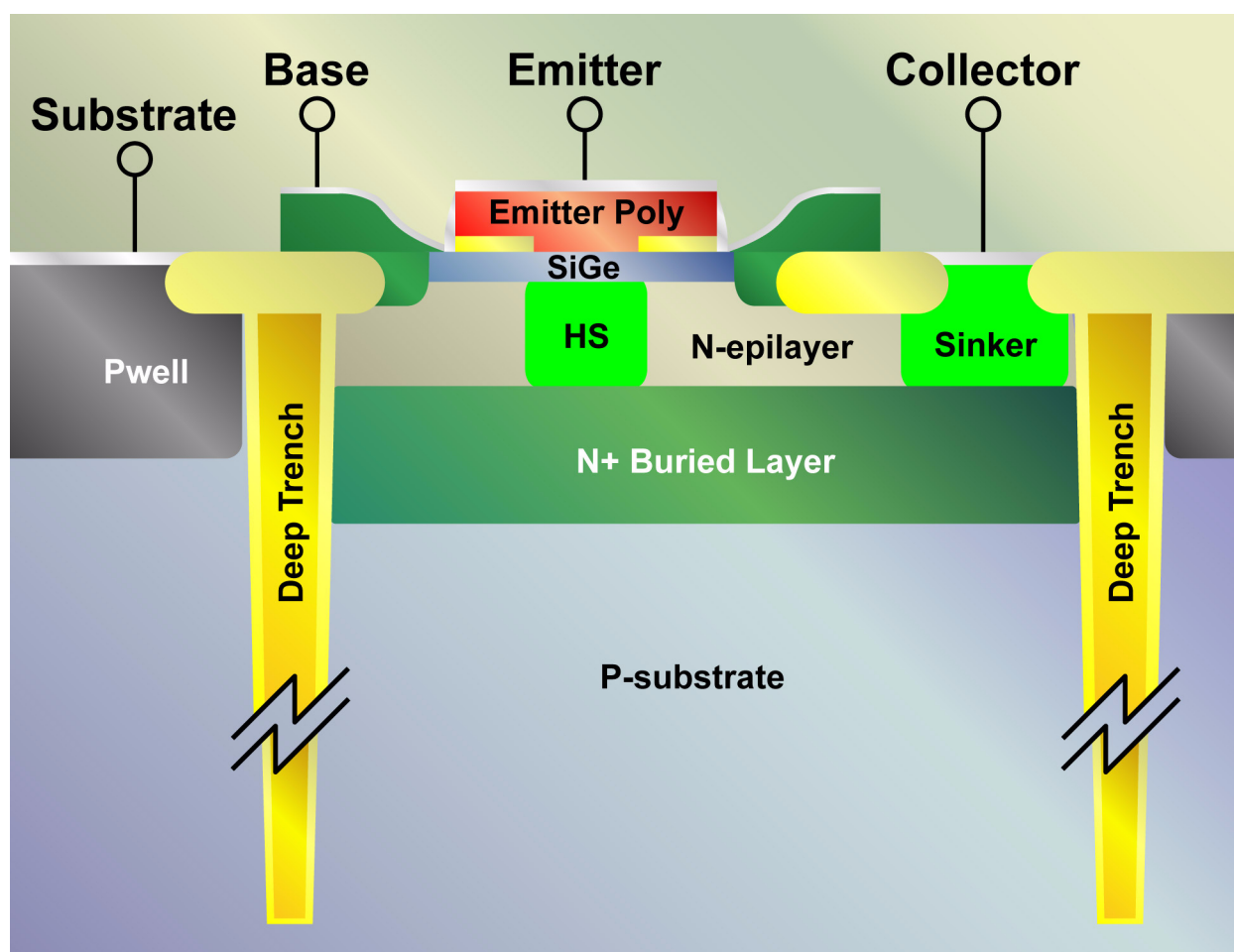
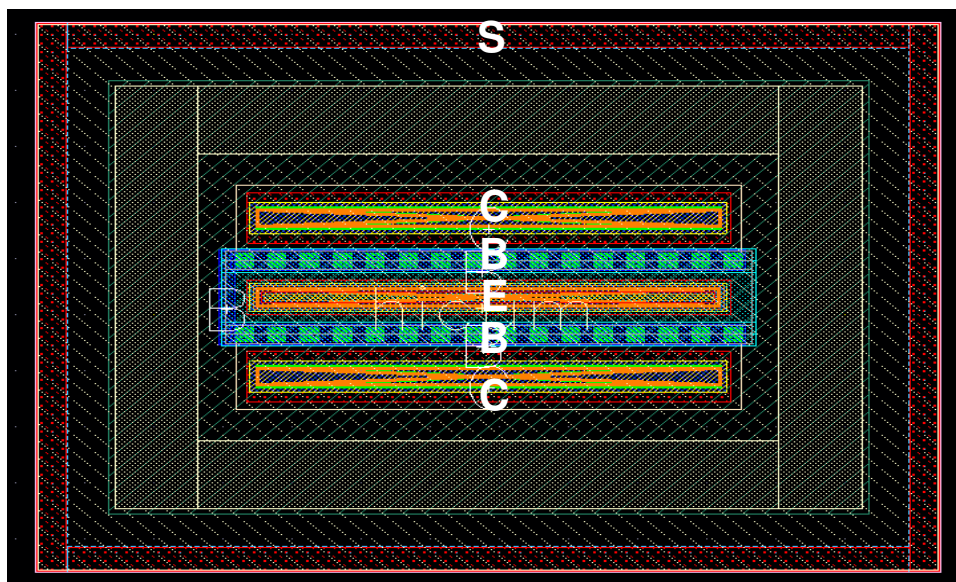


FIGURE 5.2 Layout of NPN: 1 Emitter, 2 Base, and 2 Collector configuration



5.2 Available NPN Configurations and Usage Guidelines

Table 5.2 provides a detailed description of the NPN configurations and parameter ranges.

Emitters Lengths: Scalable, see Table 5.2 for length range.

Emitters Widths: A single emitter width ($0.15\mu\text{m}$) is offered in the sbc18h2 technology.

Multiple device instances vs. multiple emitter fingers: use of multiple emitter fingers instead of multiple device instances generally results in more efficient footprint and lower parasitic capacitance. The trade-off is collector resistance.

TABLE 5.2 SiGe200 NPN Configurations

Configuration	Device Type: l=low voltage m=medium voltage	Emitter Width n= $0.15\mu\text{m}$	Emitter Length (μm)	No. of Emitters	No. of Bases	No. of Collectors
121	l, m	n	0.76-20.0	1	2	1
122	l, m	n	0.76-20.0	1	2	2
232	l, m	n	2.84-20.0	2	3	2

5.3 Model Description

5.3.1 L-Scalable Model

The emitter length can be varied within the grid spacing and within the boundaries listed in Table 5.2. Separate models are extracted for the various combinations of emitter width and finger configuration described in Table 5.2.

5.3.2 HICUM Model

The HICUM model was introduced to overcome the shortcomings of the SGPM (Standard Gummel-Poon Model). The name of HICUM is derived from “High Current Model”. HICUM was initially developed with special emphasis on the modeling of the high current region, very important for many high-speed applications. Compared with SGPM, HICUM is based on an extended and generalized integral charge control relationship, and approaches the transistor dynamic behaviors in a more physical way. For more detailed information about HICUM, please refer to HICUM official web page (http://www.iee.et.tu-dresden.de/iee/eb/hic_new/hic_start.html).

5.4 Model Extraction and Verification

Scalable NPN models are extracted based on DC, CV, and RF measurements over a wide geometry and bias range.

Figures 5.3 through 5.44 display the characterization plots for the low voltage NPN. Figures 5.45 through 5.86 display the characterization plots for the medium voltage NPN. Multiple devices in parallel are characterized for smaller emitter lengths to reduce de-embedding errors. The device type and size are encoded in the figure caption as “Voltage LxWxM_Configuration.” Thus a MV 0.15x1x10_122 caption refers to a medium voltage NPN with a width (W) of 0.15 μ m, a length (L) of 1 μ m, with 10 devices in parallel (M) and a 122 emitter/base/collector finger configuration.

5.4.1 Low Voltage Verification Plots

FIGURE 5.3 Gummel Plot LV 0.15x10.16x1_122

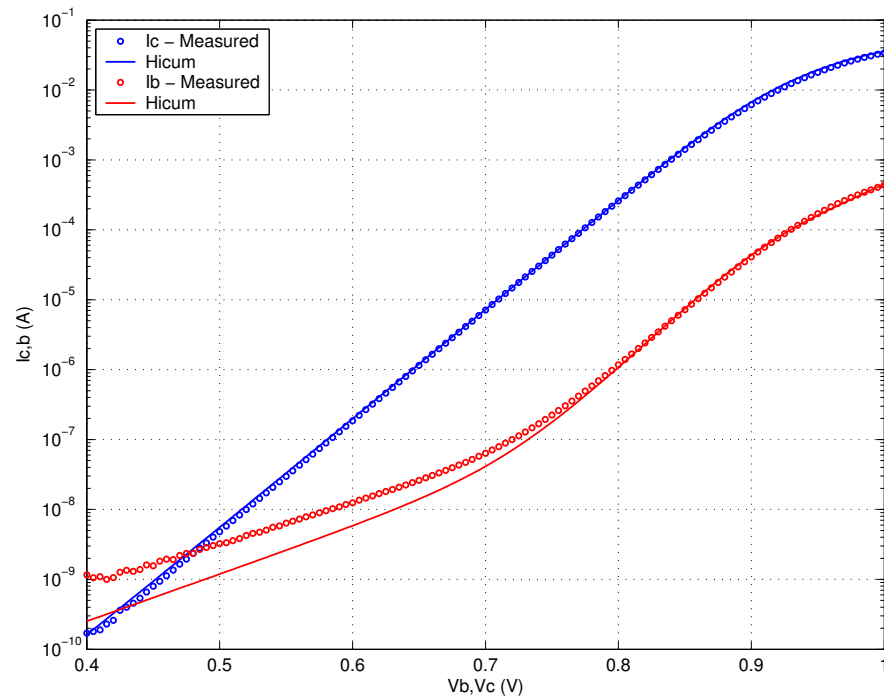


FIGURE 5.4 Beta vs. I_c : LV 0.15x10.16x1_122

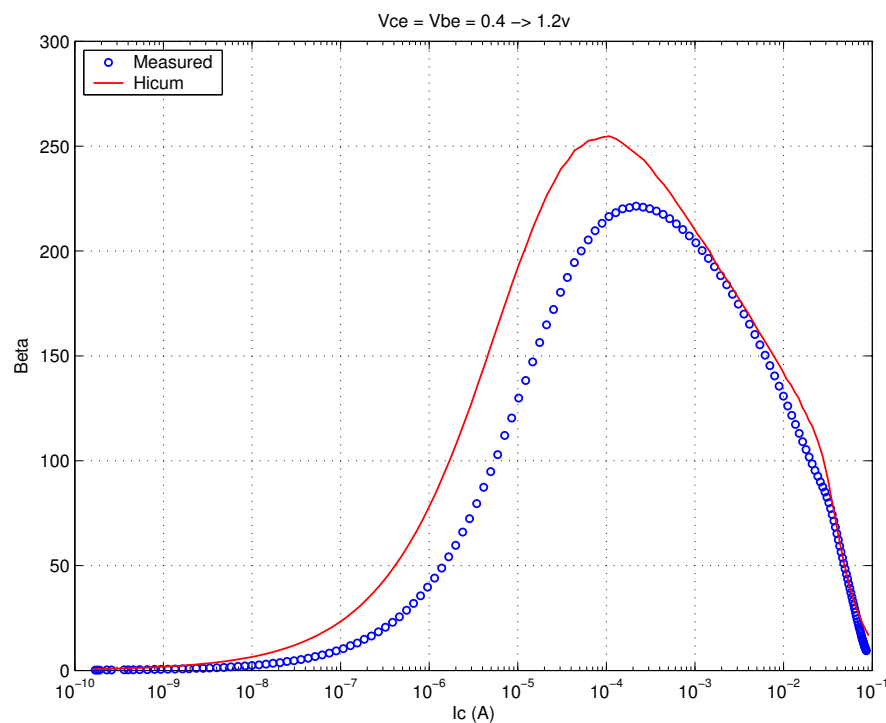


FIGURE 5.5 IC vs. VCE at constant IB: LV 0.15x10.16x1_122

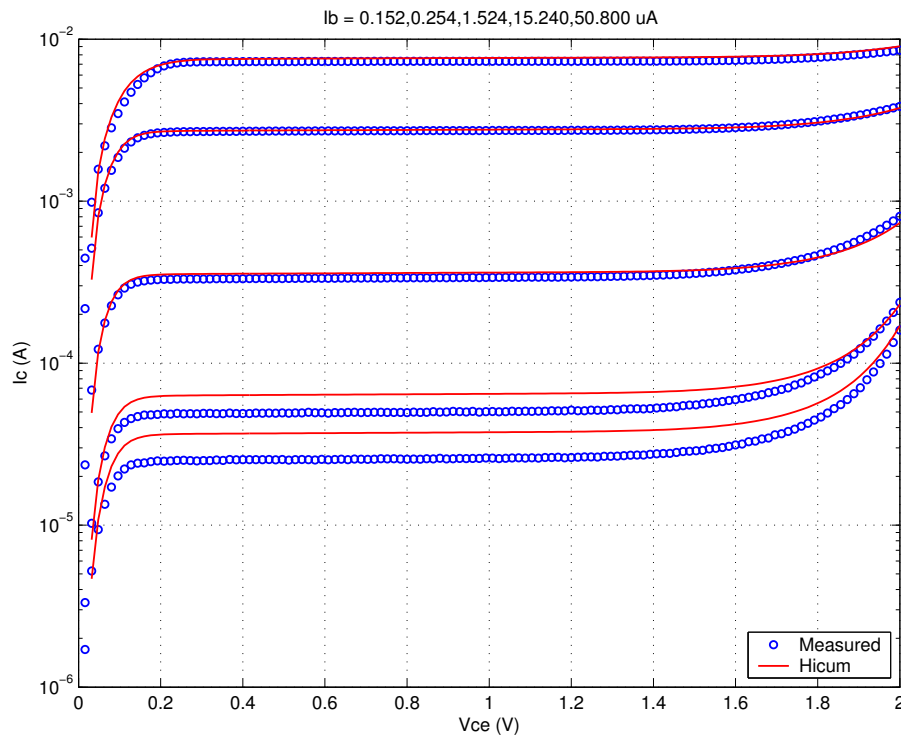


FIGURE 5.6 FT vs. IC: LV 0.15x10.16x1_122

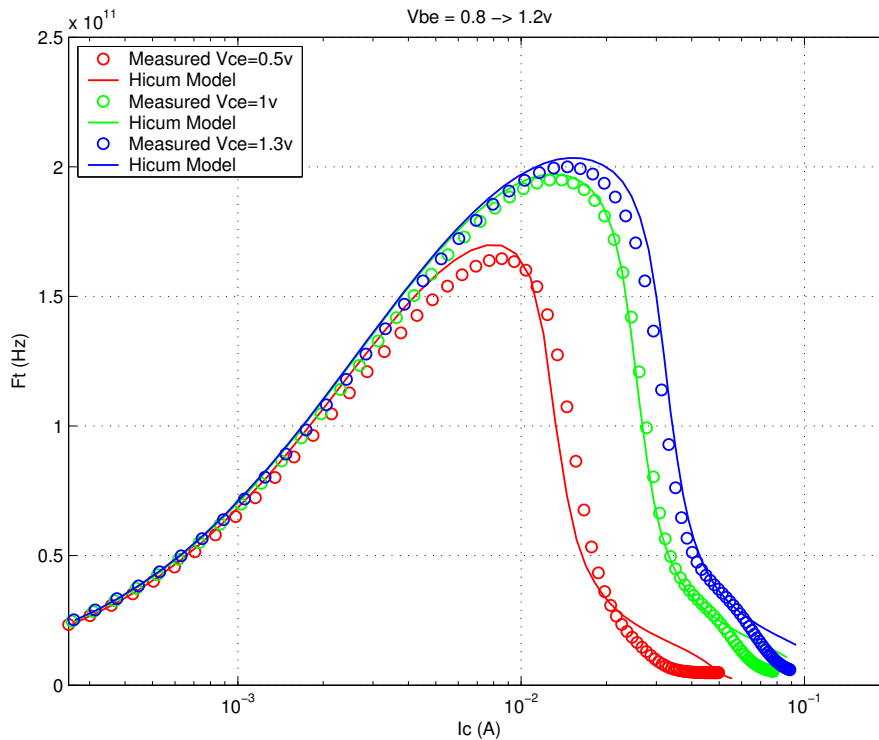
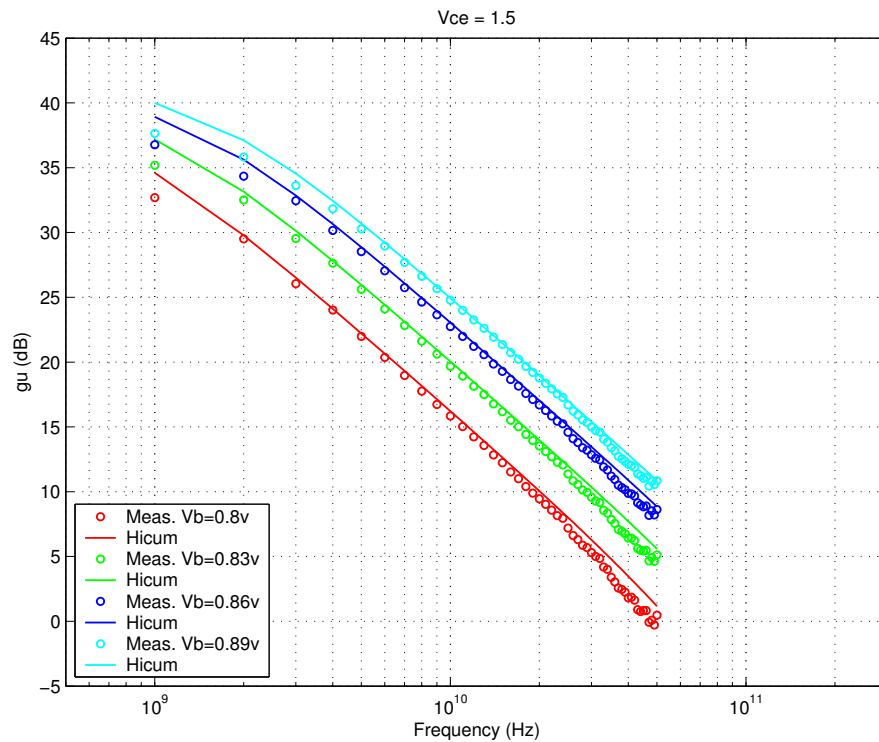


FIGURE 5.7 Power Gain vs. Freq: LV 0.15x10.16x1_122



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FIGURE 5.8 Y-parameters vs. FREQ: LV 0.15x10.16x1_122

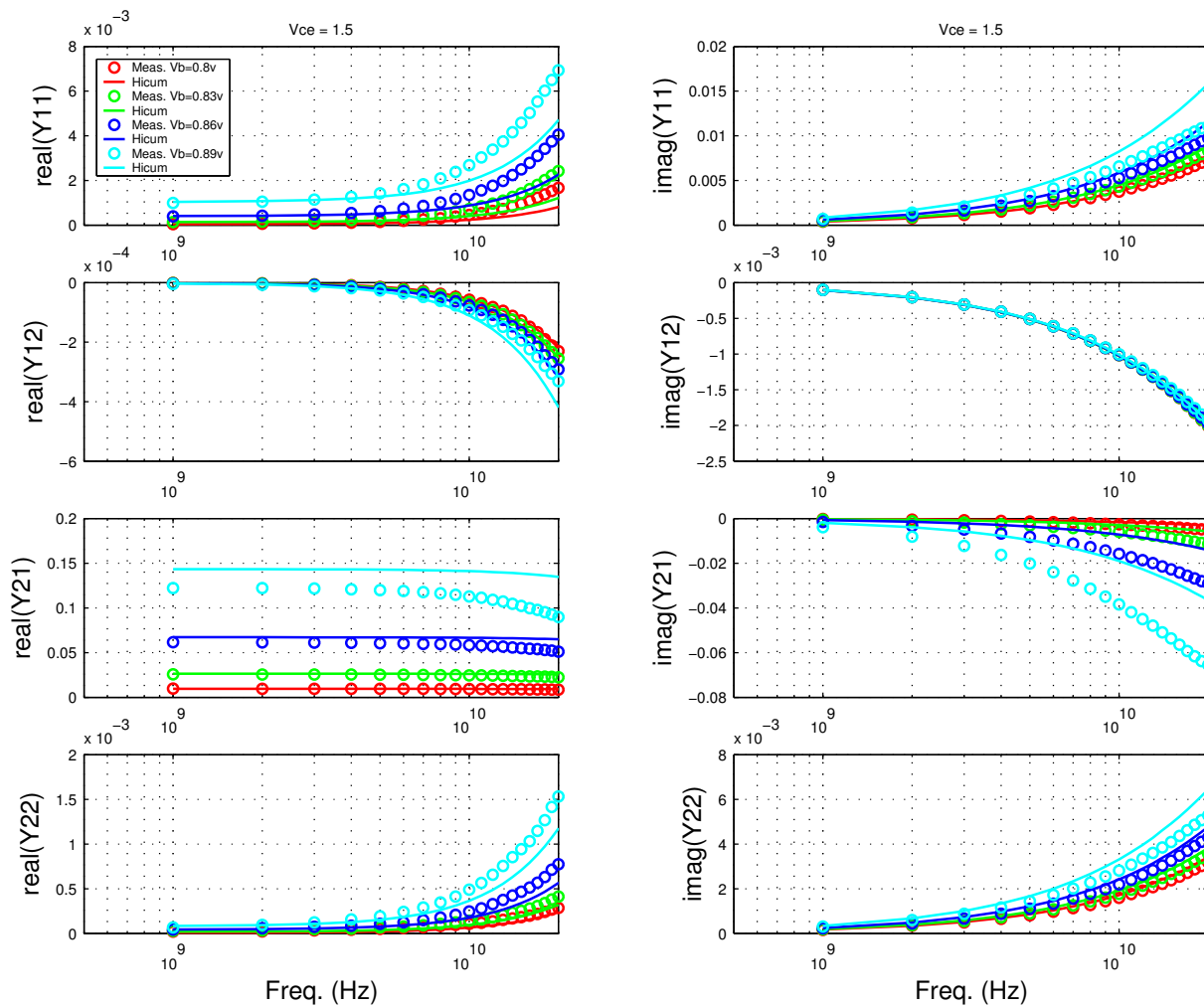


FIGURE 5.9 Gummel Plot LV 0.15x4.52x1_122

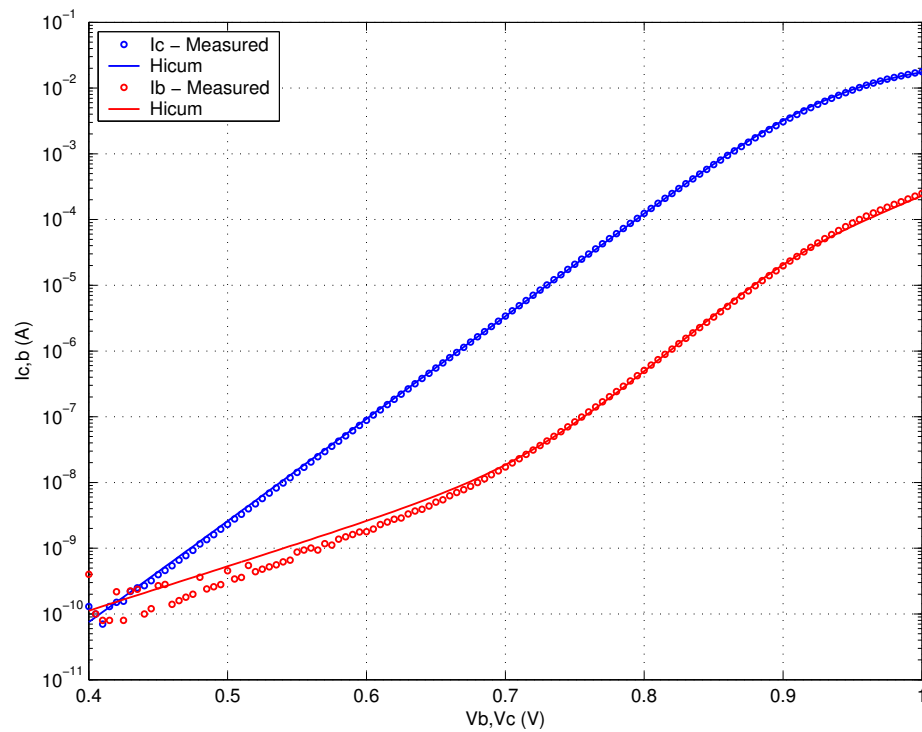
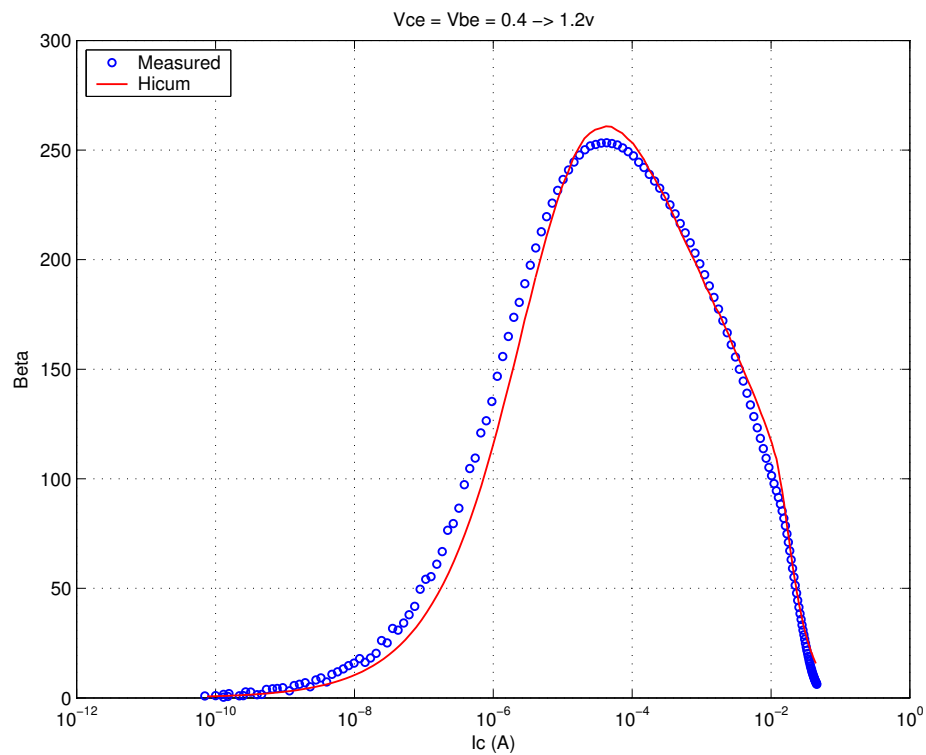
FIGURE 5.10 Beta vs. I_c : LV 0.15x4.52x1_122

FIGURE 5.11 IC vs. VCE at constant IB: LV 0.15x4.52x1_122

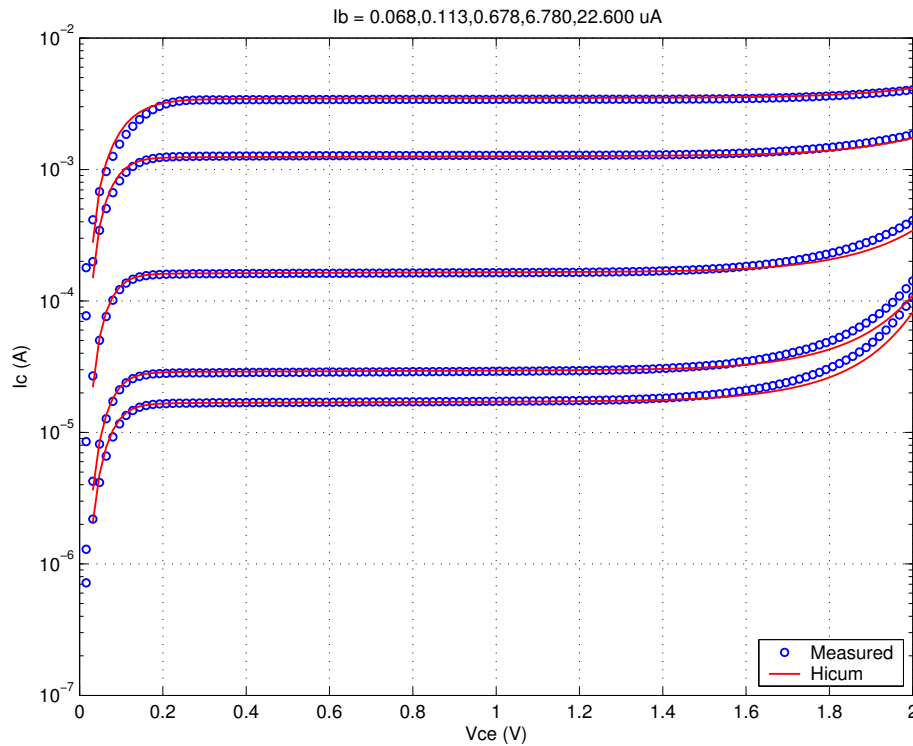


FIGURE 5.12 FT vs. IC: LV 0.15x4.52x1_122

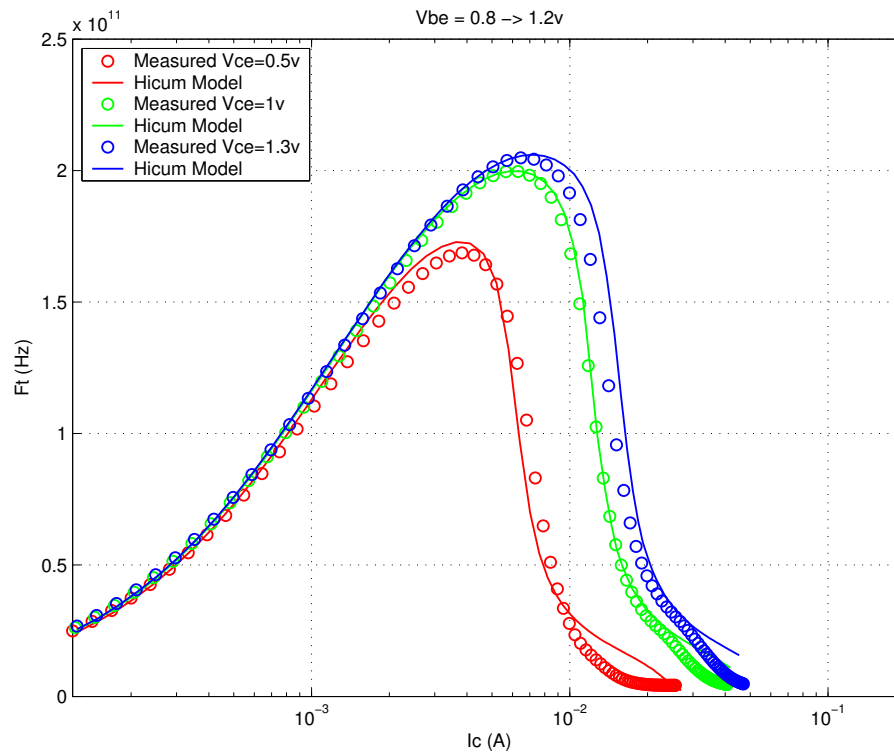
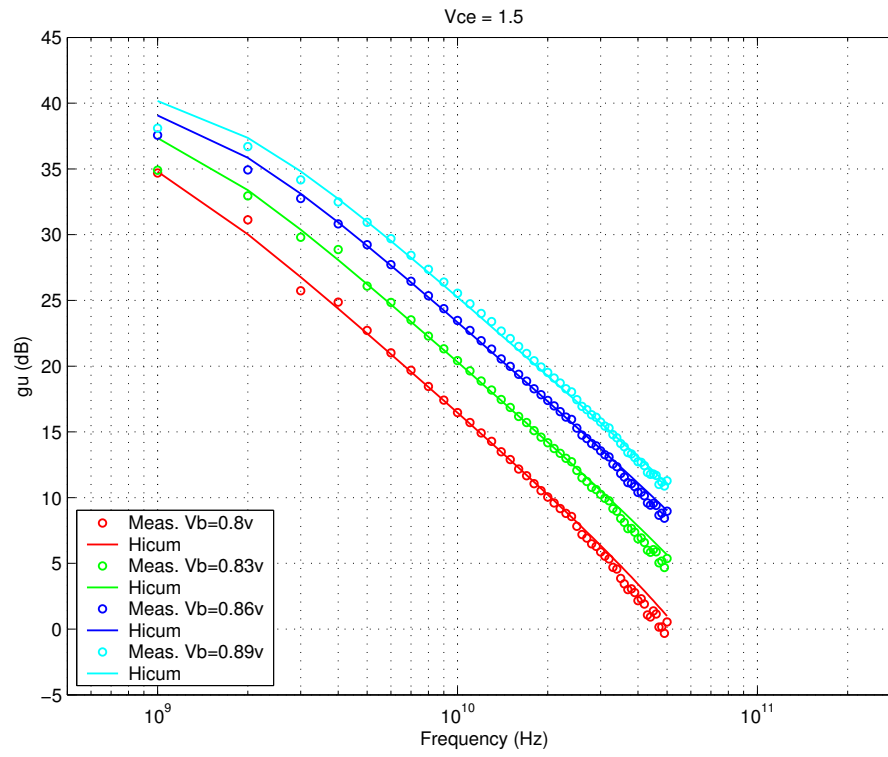


FIGURE 5.13 Power Gain vs. Freq: LV 0.15x4.52x1_122



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FIGURE 5.14 Y-parameters vs. FREQ: LV 0.15x4.52x1_122

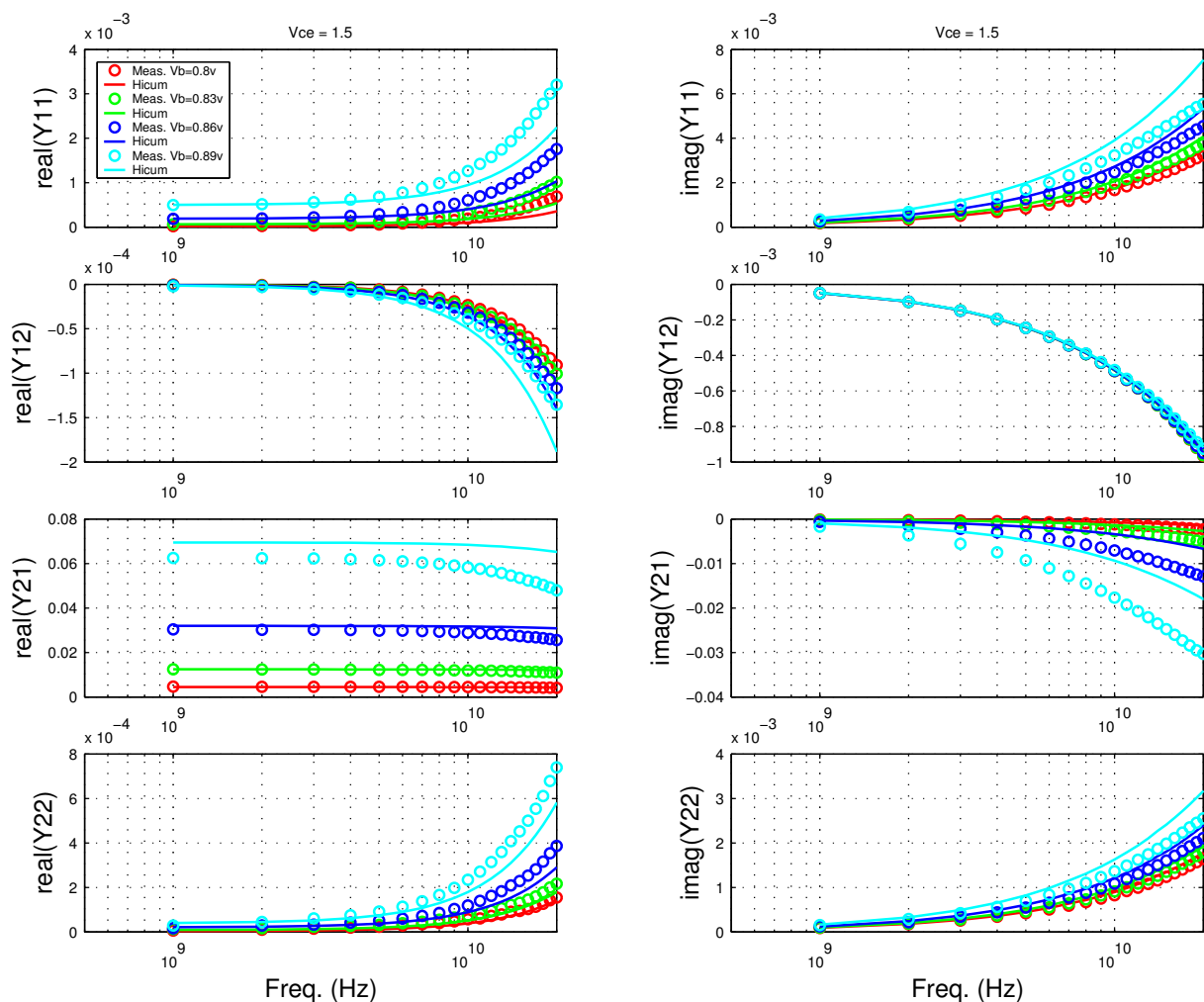


FIGURE 5.15 Gummel Plot: LV 0.15x2.84x1_122

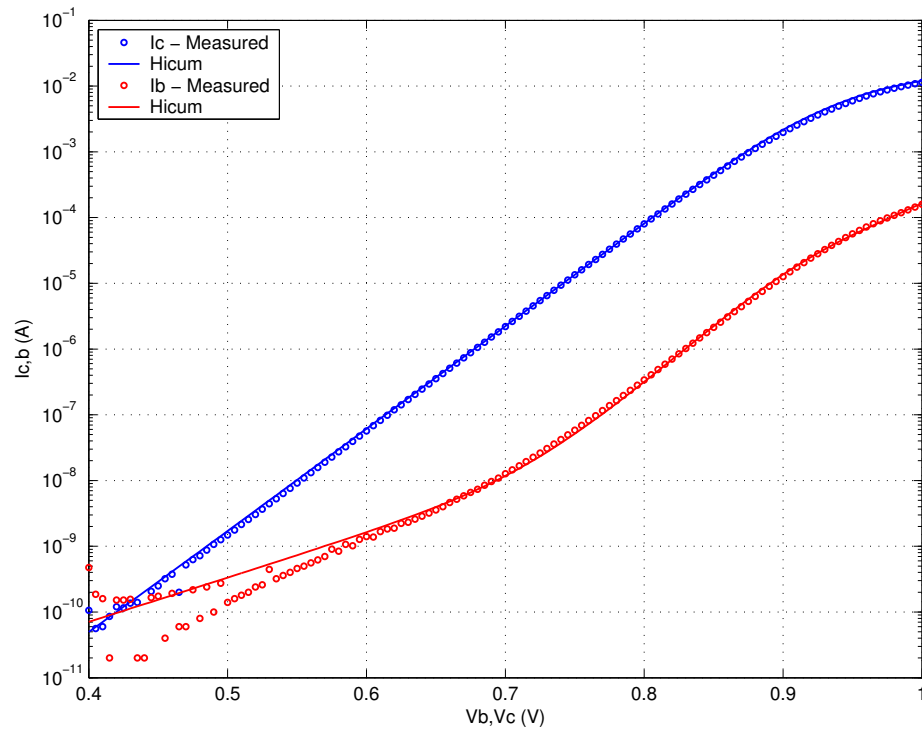
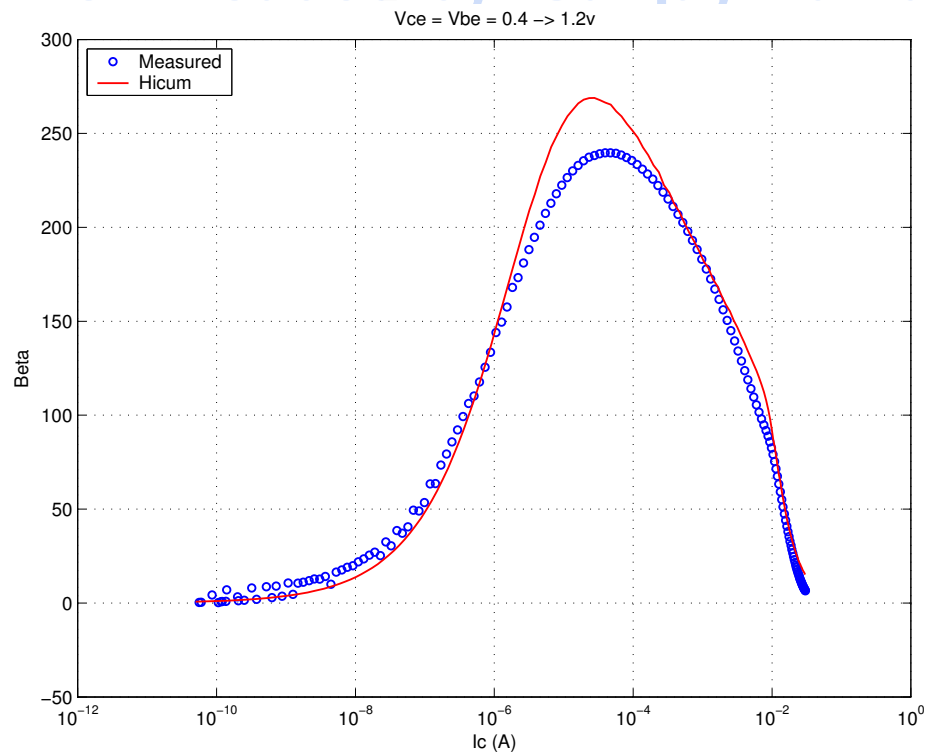
FIGURE 5.16 Beta vs. I_c : LV 0.15x2.84x1_122

FIGURE 5.17 IC vs. VCE at constant IB: LV 0.15x2.84x1_122

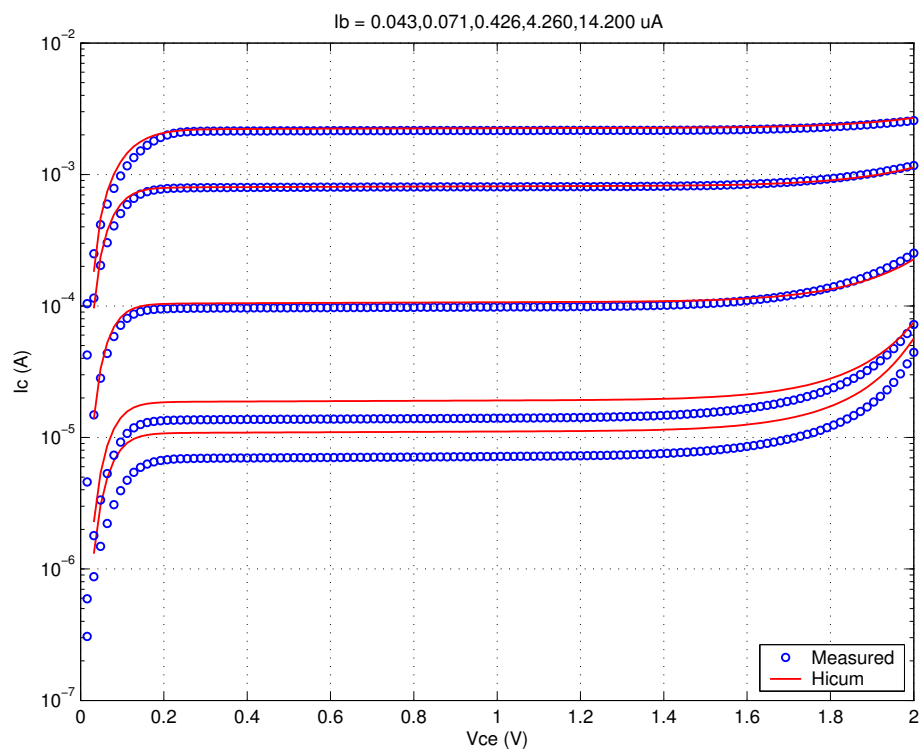


FIGURE 5.18 FT vs. IC: LV 0.15x2.84x1_122

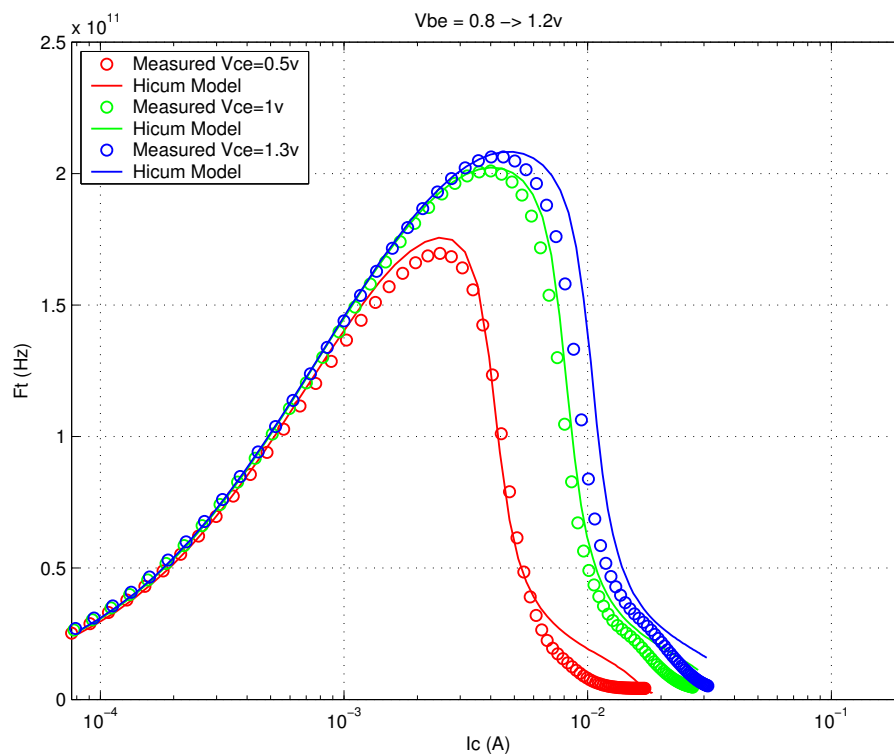
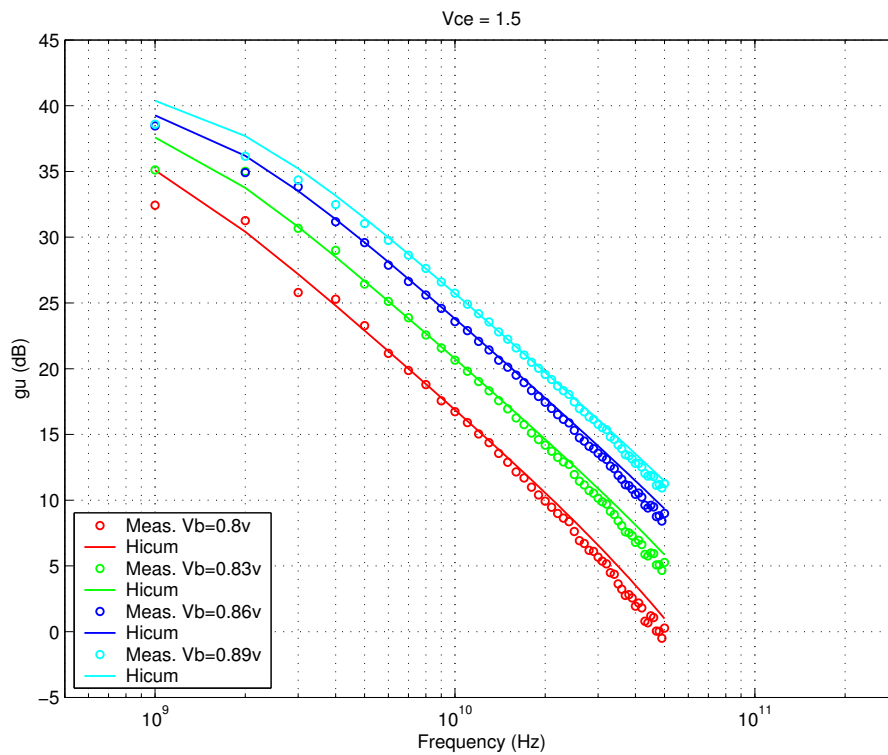


FIGURE 5.19 Power Gain vs. Freq: LV 0.15x2.84x1_122



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FIGURE 5.20 Y-parameters vs. FREQ: LV 0.15x2.84x1_122

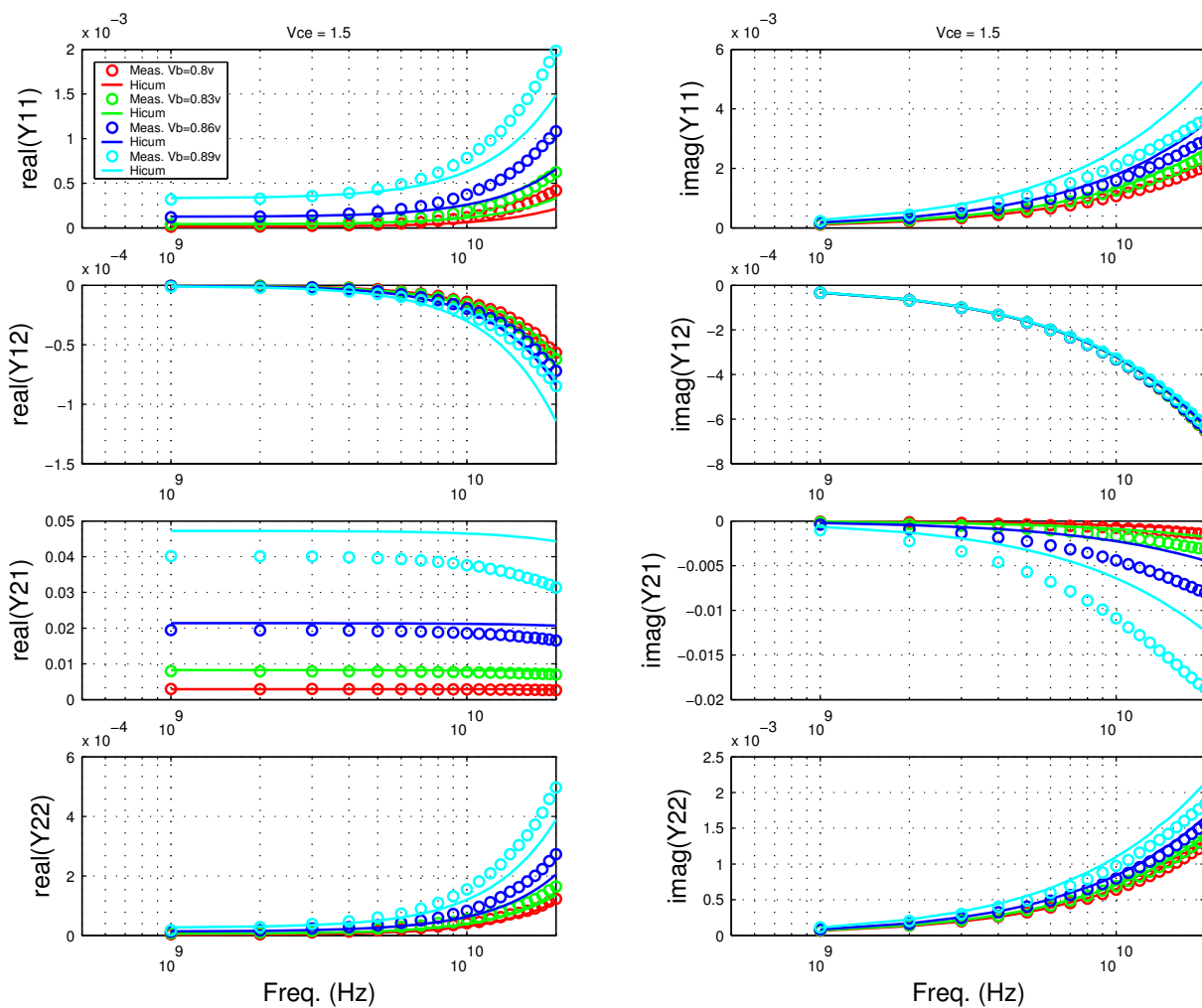


FIGURE 5.21 Gummel Plot LV 0.15x10.16x1_121

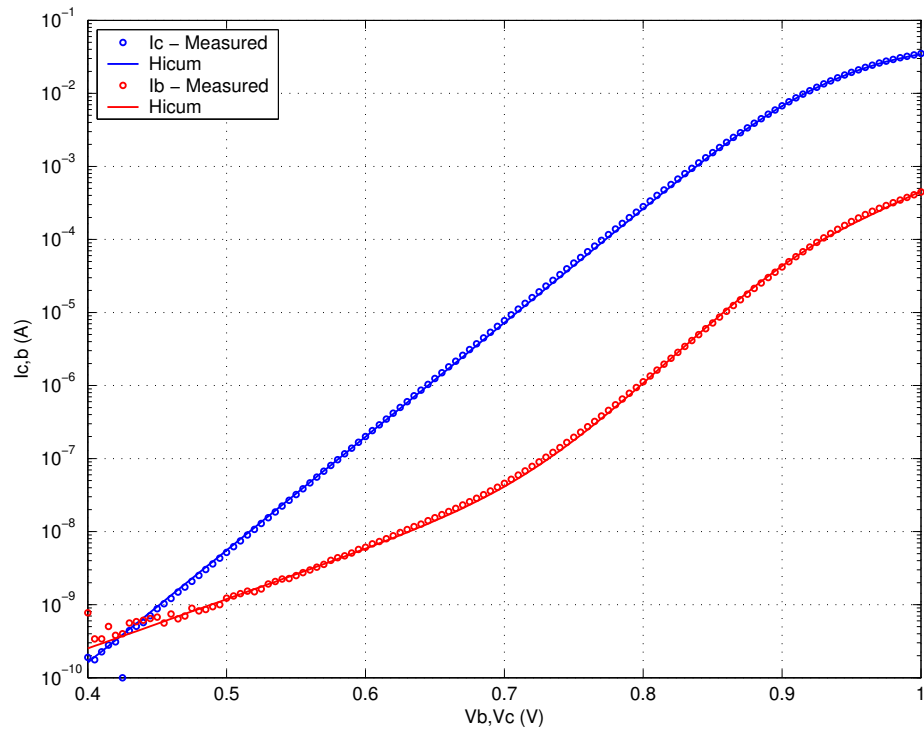
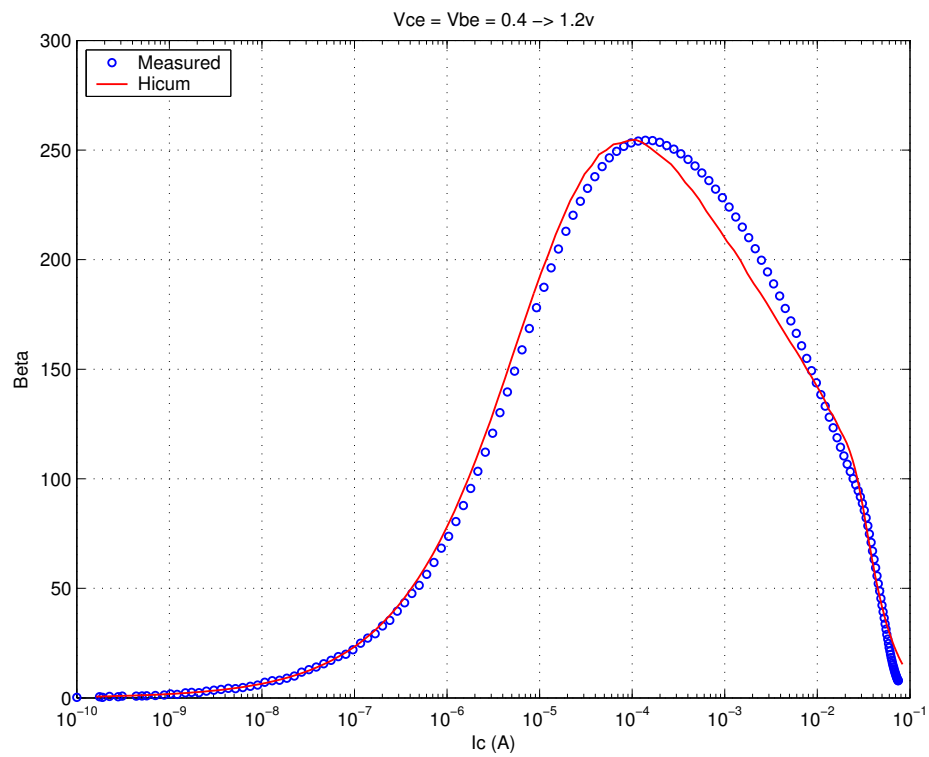
FIGURE 5.22 Beta vs. I_c : LV 0.15x10.16x1_121

FIGURE 5.23 IC vs. VCE at constant IB: LV 0.15x10.16x1_121

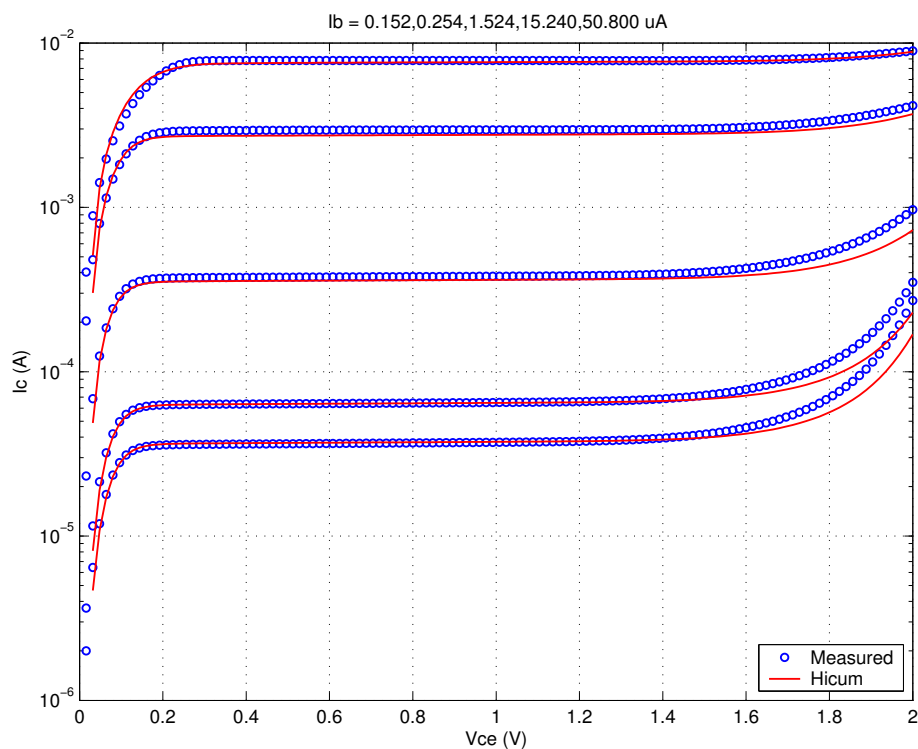


FIGURE 5.24 FT vs. IC: LV 0.15x10.16x1_121

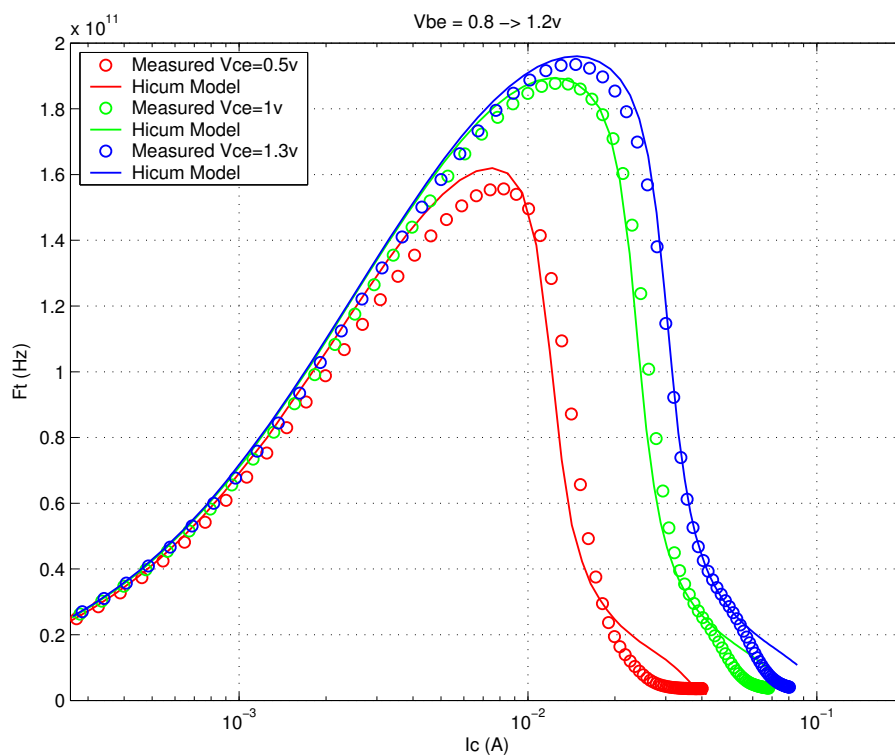
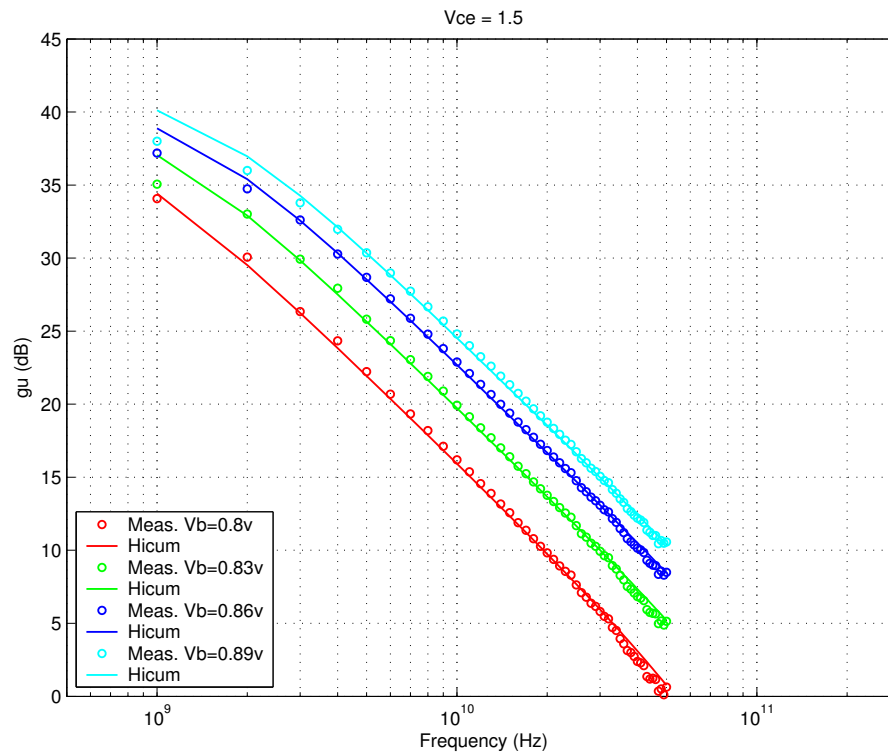


FIGURE 5.25 Power Gain vs. Freq: LV 0.15x10.16x1_121



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FIGURE 5.26 Y-parameters vs. FREQ: LV 0.15x10.16x1_121

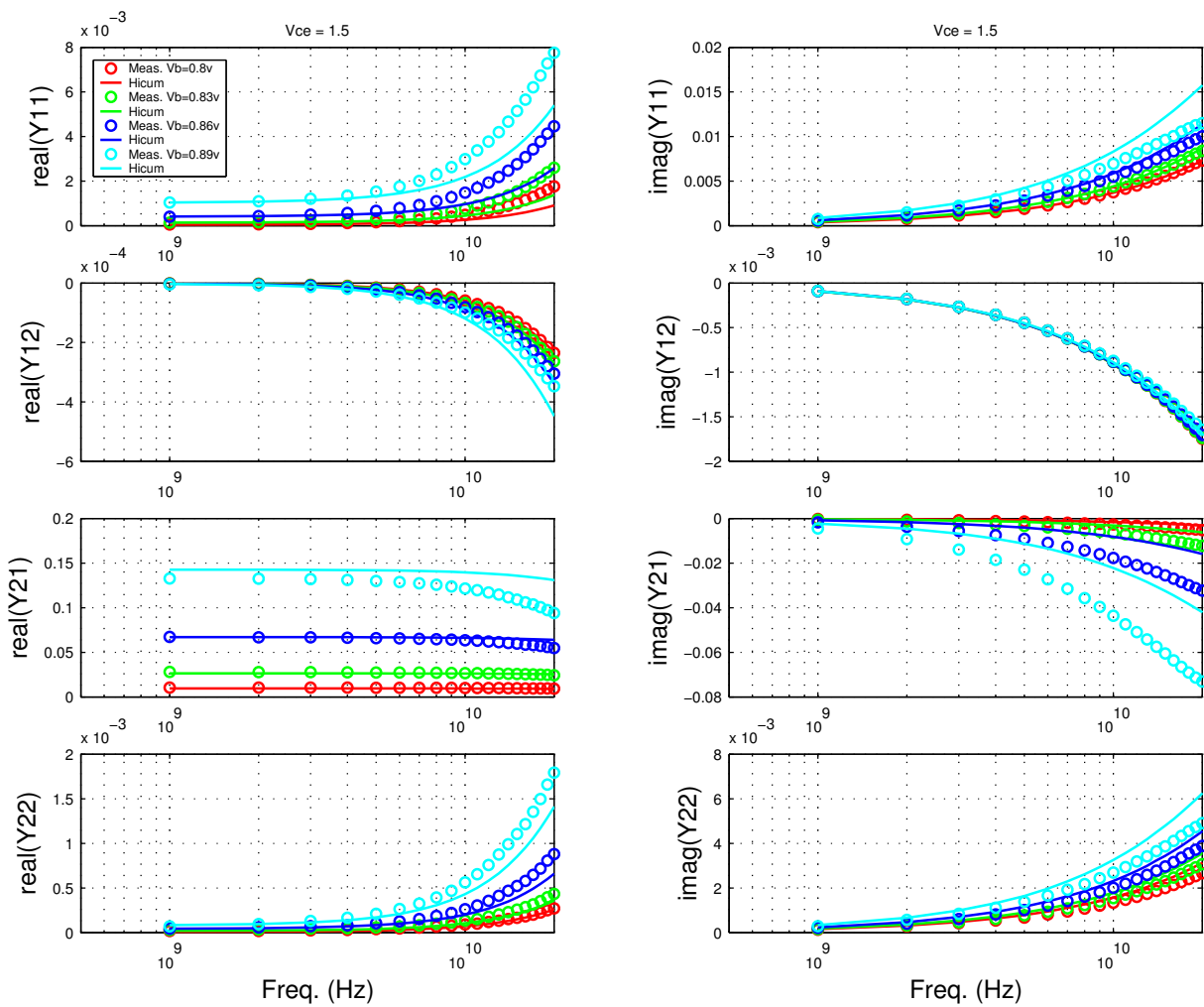


FIGURE 5.27 Gummel Plot LV 0.15x10.16x1_232

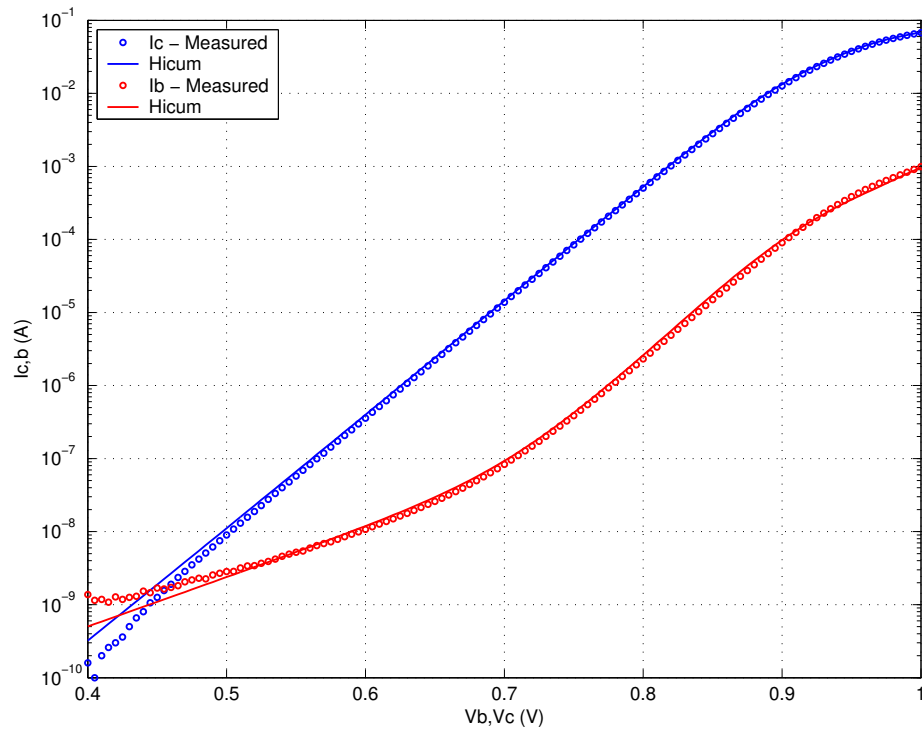
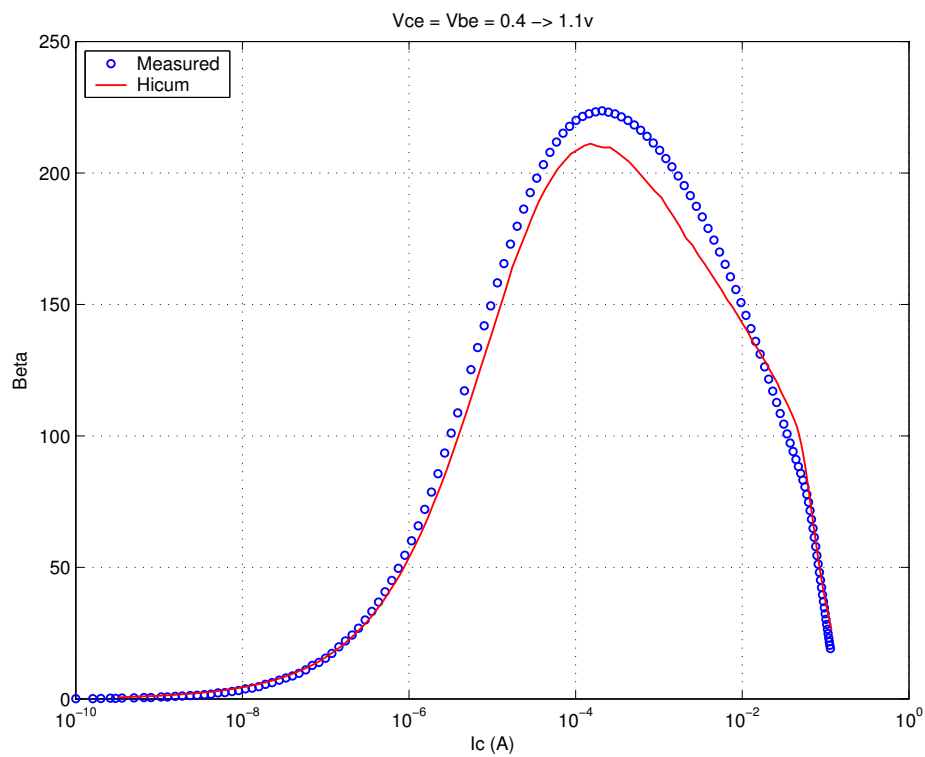
FIGURE 5.28 Beta vs. I_c : LV 0.15x10.16x1_232

FIGURE 5.29 IC vs. VCE at constant IB: LV 0.15x10.16x1_232

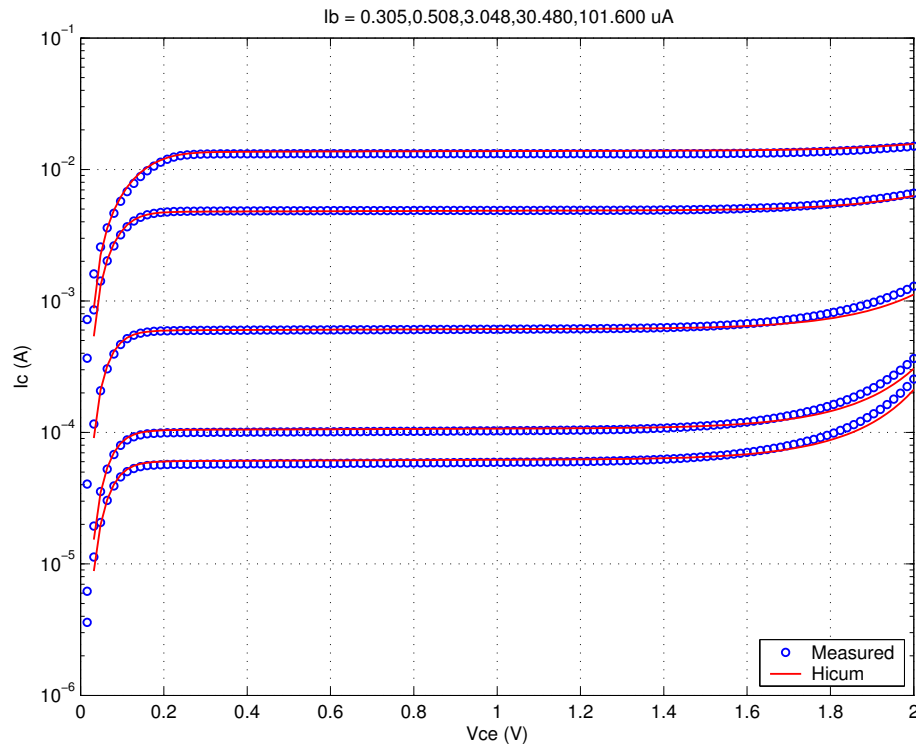


FIGURE 5.30 FT vs. IC: LV 0.15x10.16x1_232

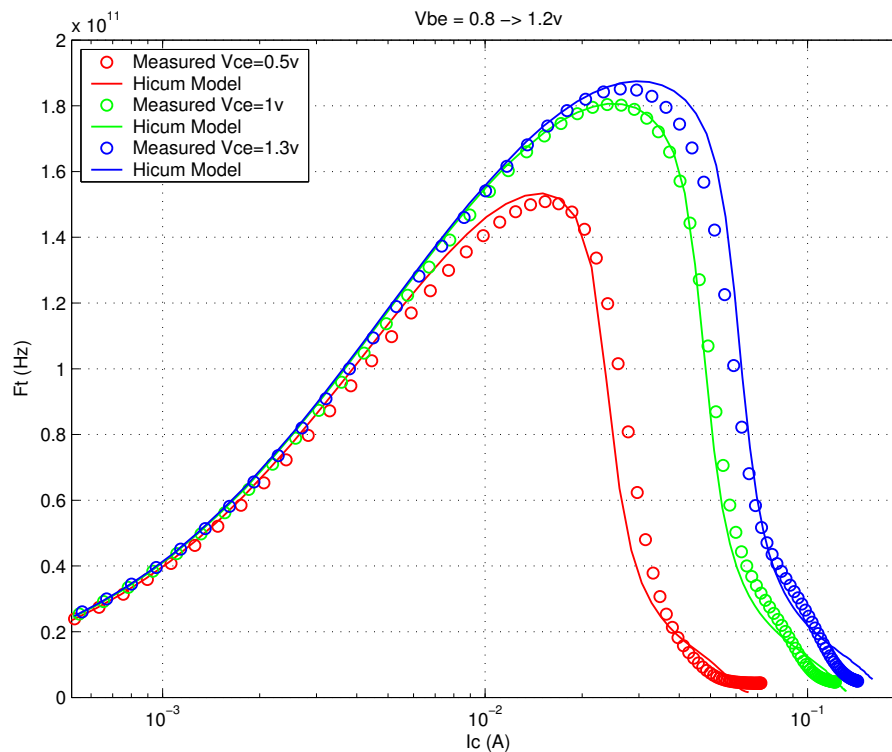
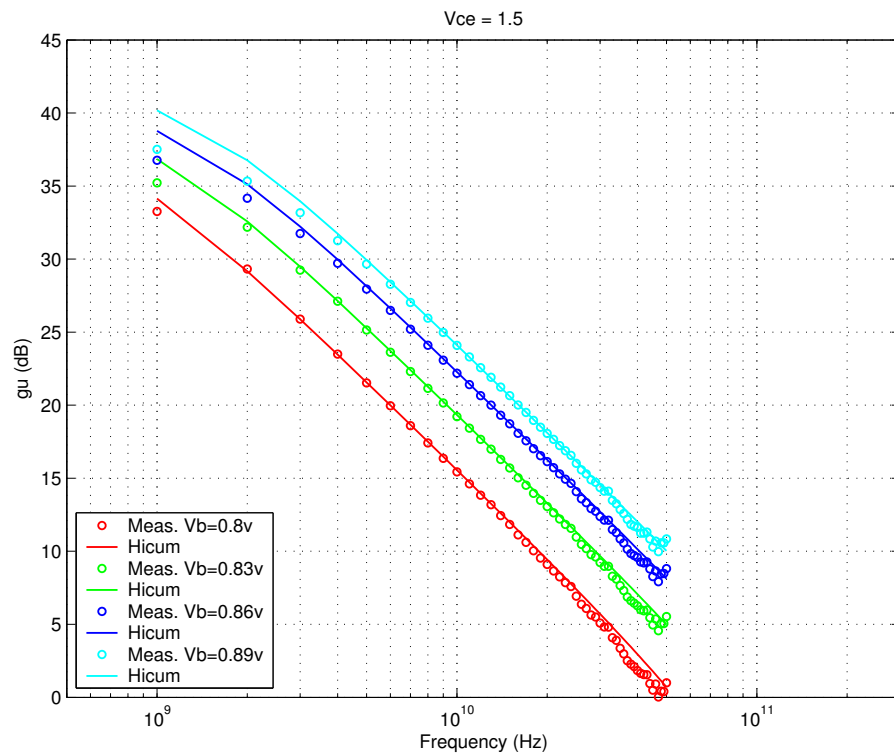


FIGURE 5.31 Power Gain vs. Freq: LV 0.15x10.16x1_232



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FIGURE 5.32 Y-parameters vs. FREQ: LV 0.15x10.16x1_232

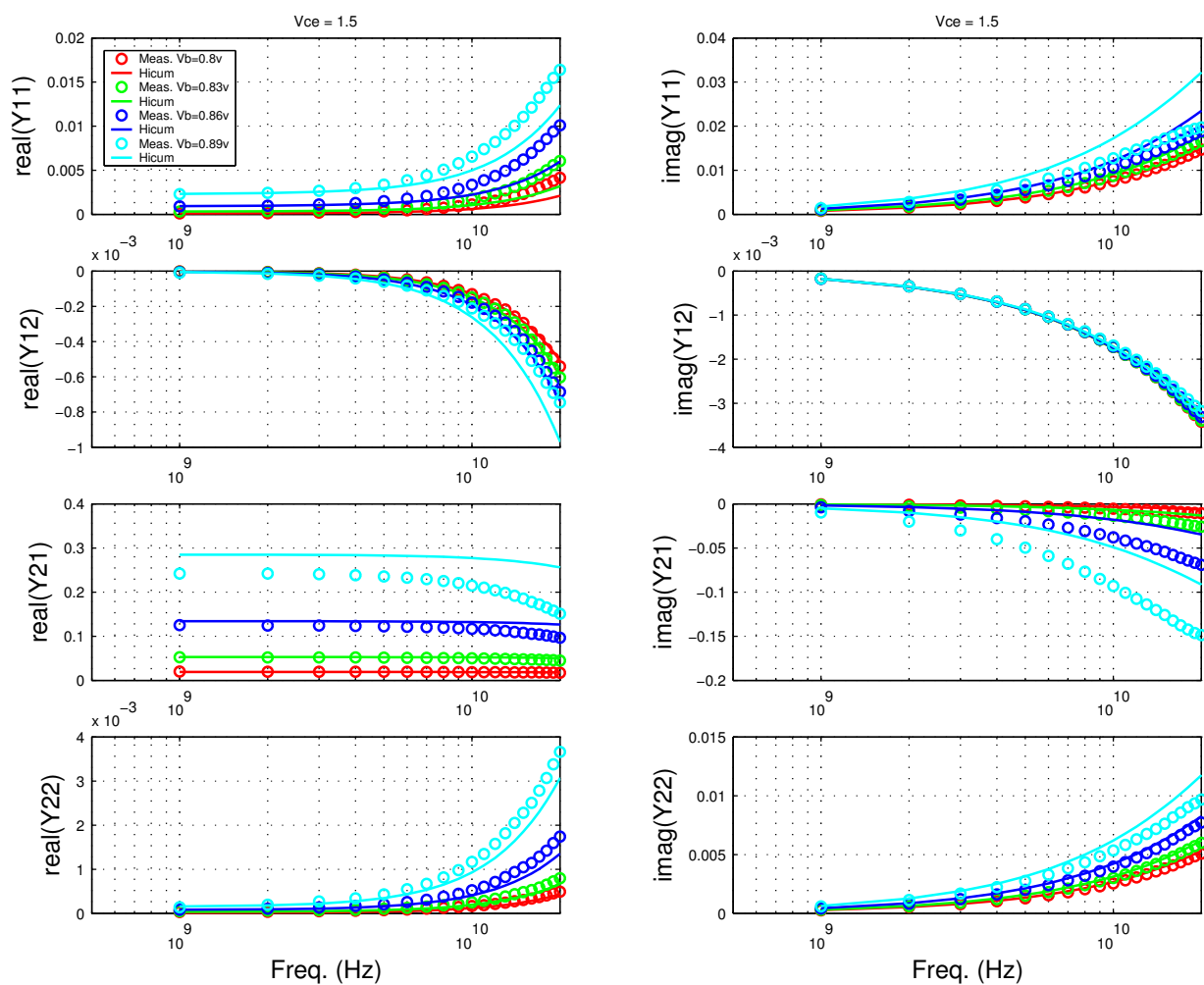


FIGURE 5.33 Gummel Plot LV 0.15x4.52x1_232

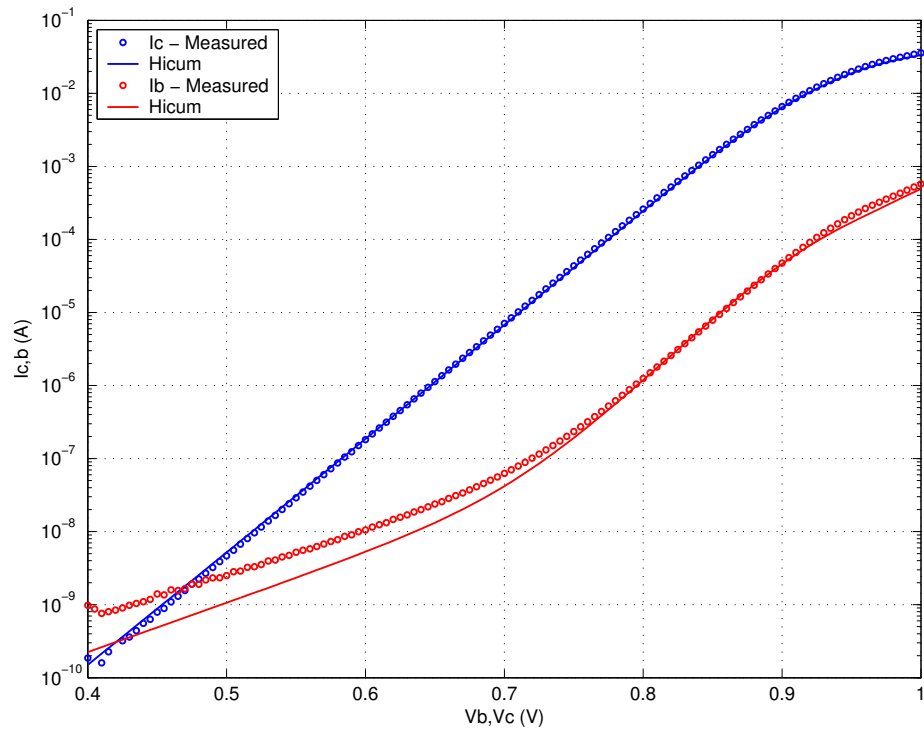
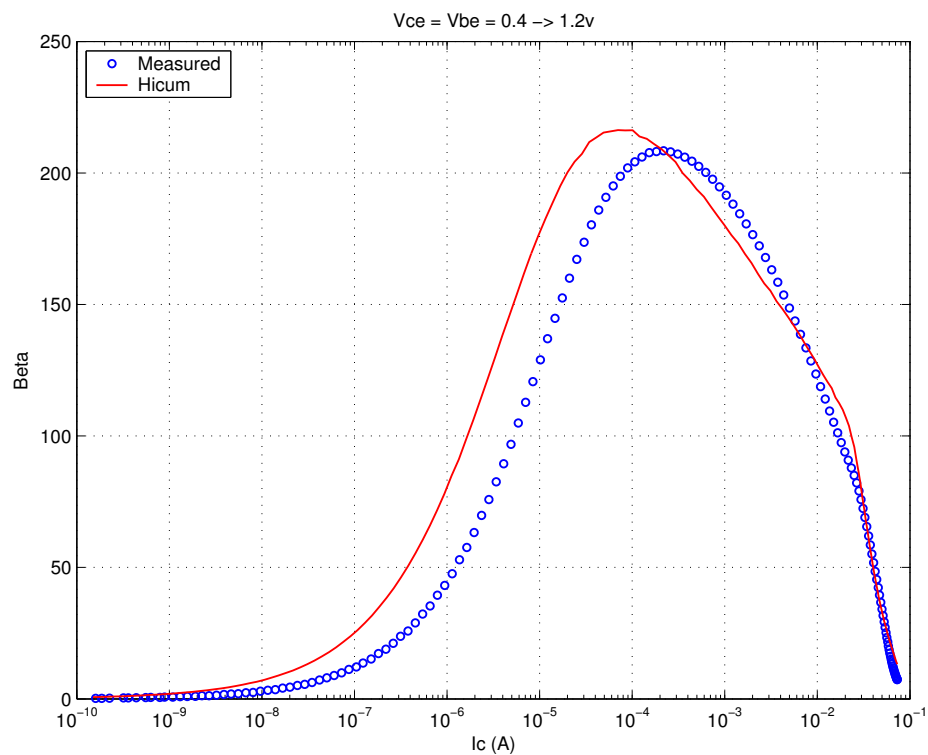
FIGURE 5.34 Beta vs. I_c : LV 0.15x4.52x1_232

FIGURE 5.35 I_C vs. V_{CE} at constant I_B : LV 0.15x4.52x1_232

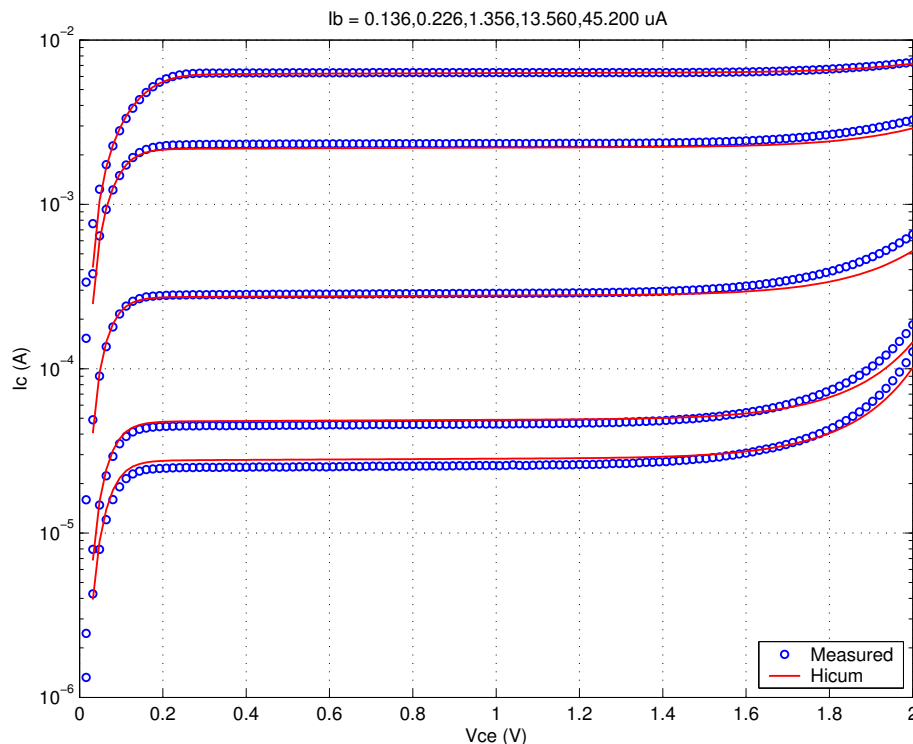


FIGURE 5.36 F_T vs. I_C : LV 0.15x4.52x1_232

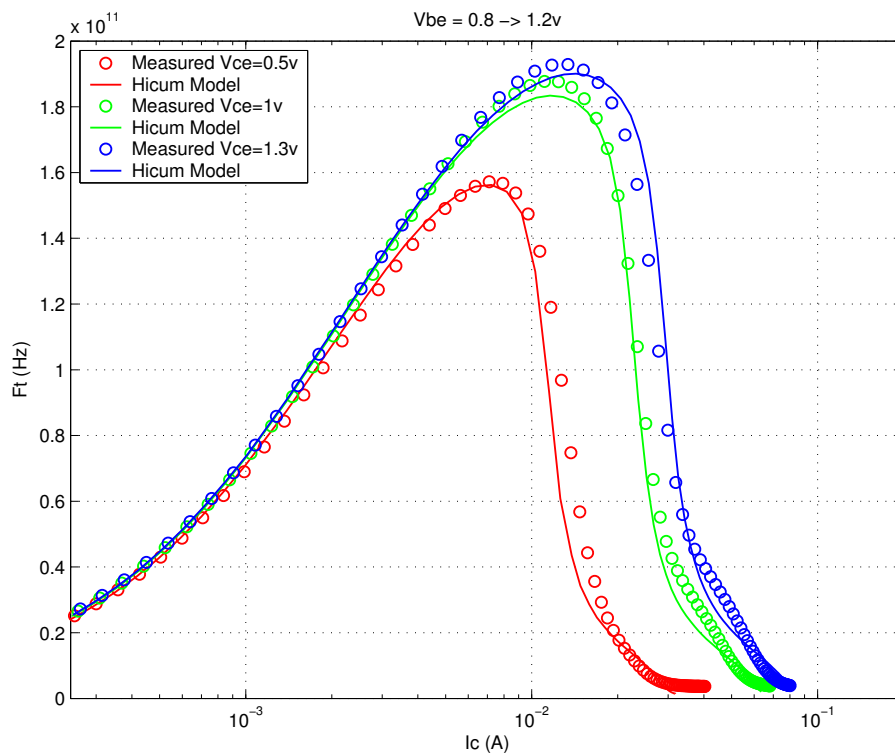
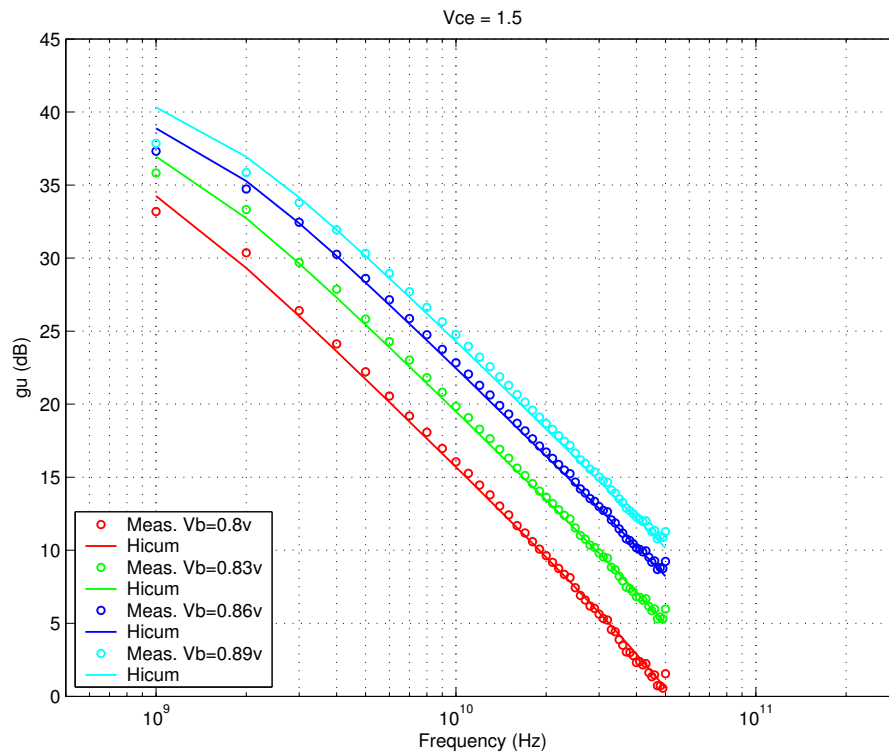


FIGURE 5.37 Power Gain vs. Freq: LV 0.15x4.52x1_232



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FIGURE 5.38 Y-parameters vs. FREQ: LV 0.15x4.52x1_232

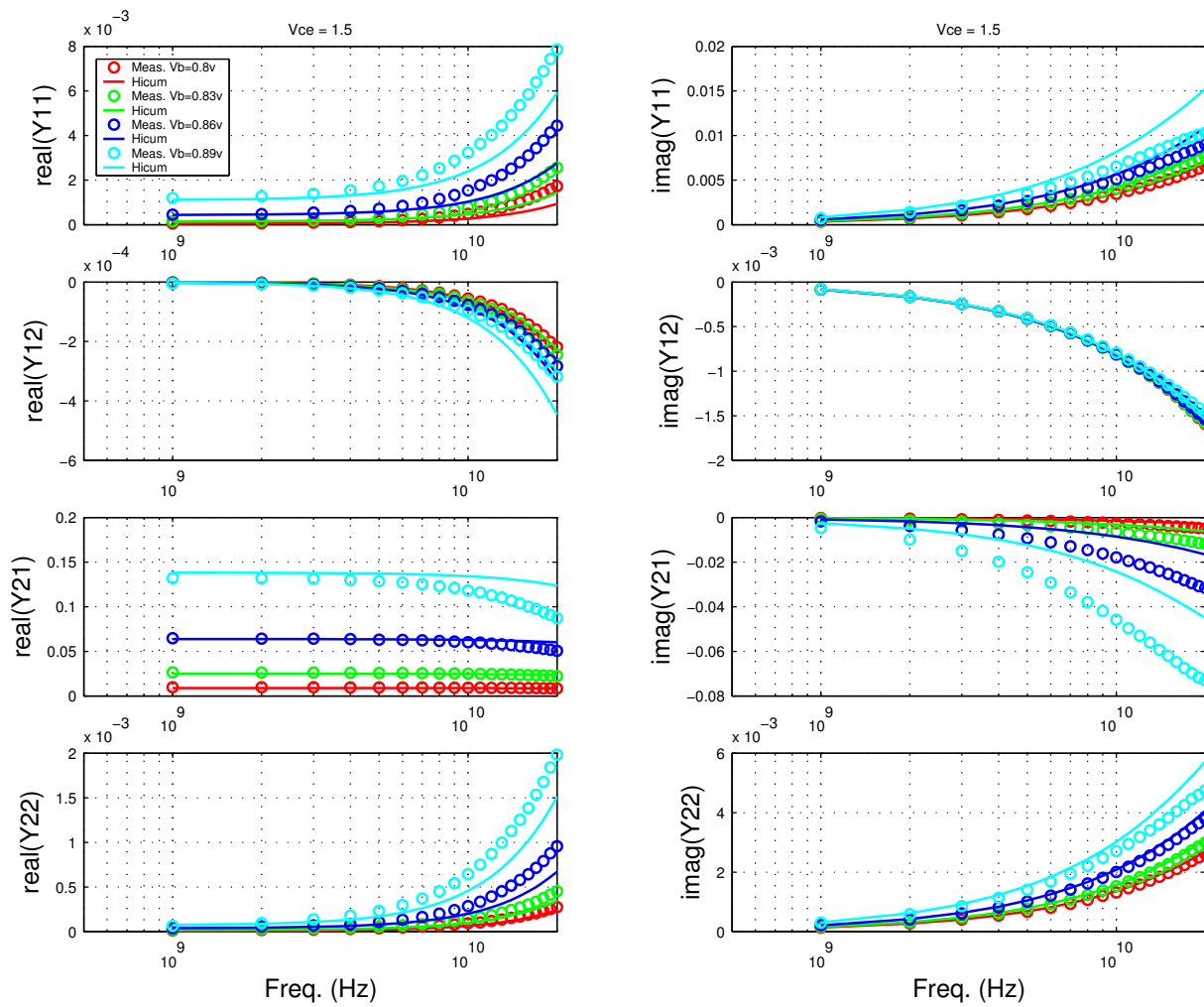


FIGURE 5.39 Gummel Plot LV 0.15x2.84x1_232

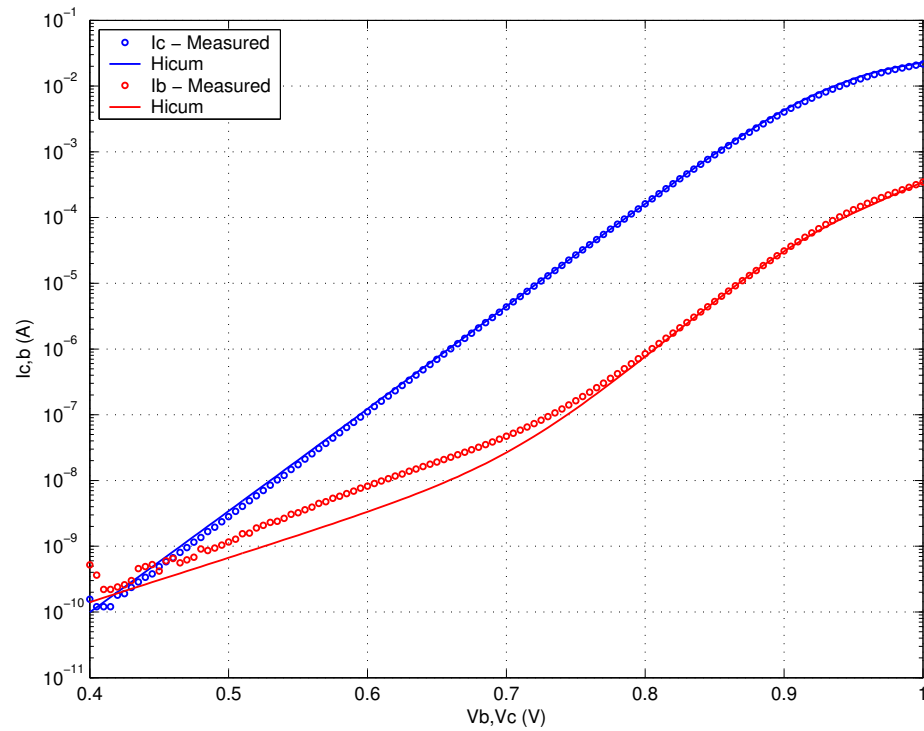
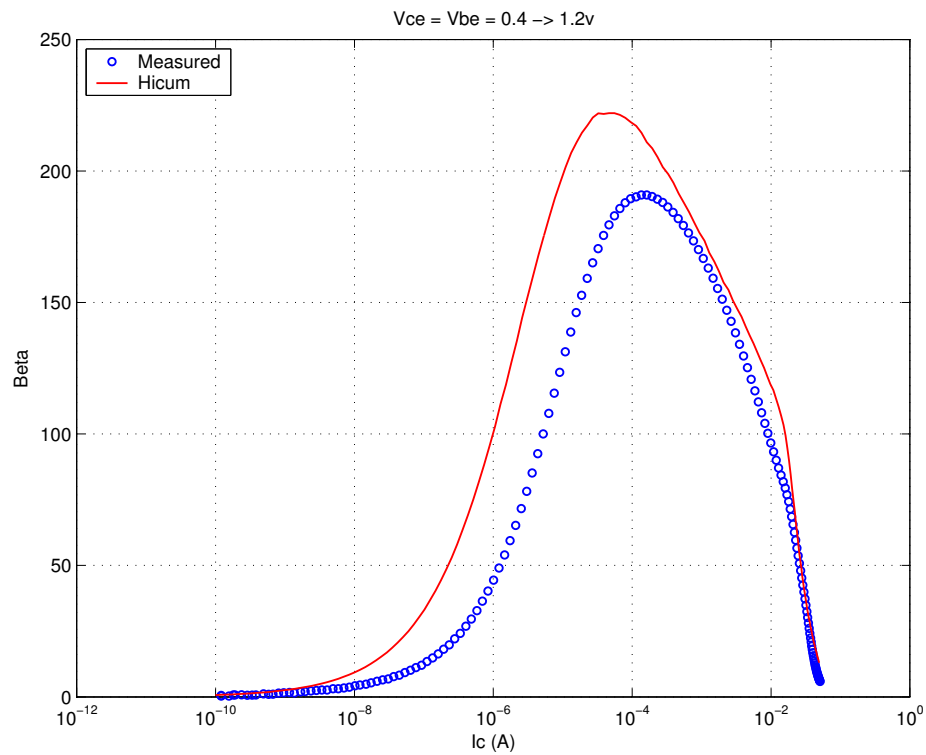
FIGURE 5.40 Beta vs. I_c : LV 0.15x2.84x1_232

FIGURE 5.41 IC vs. VCE at constant IB: LV 0.15x2.84x1_232

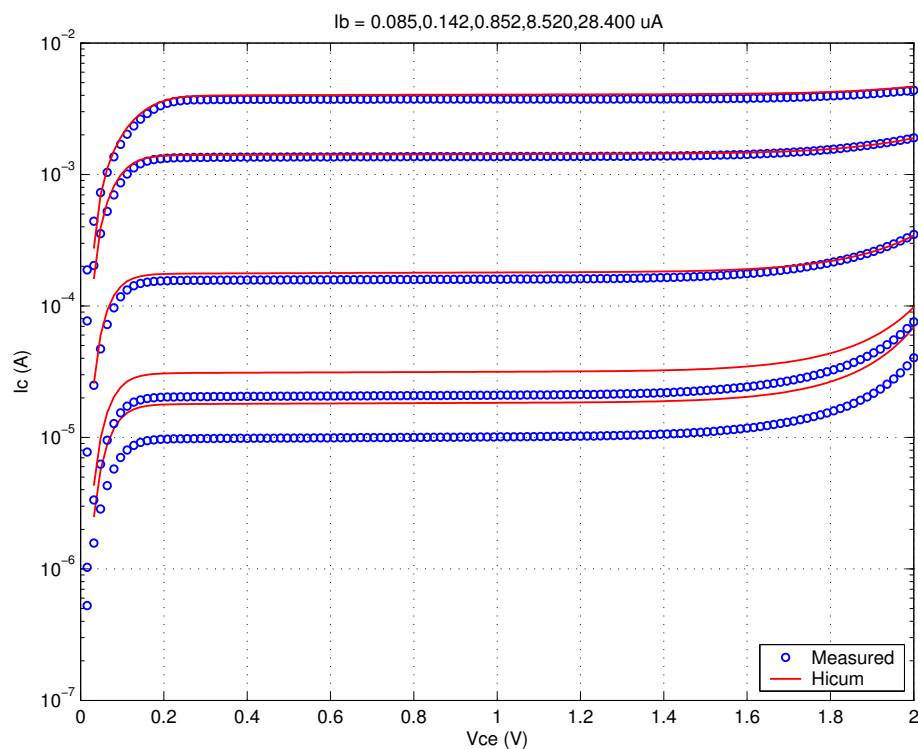


FIGURE 5.42 FT vs. IC: LV 0.15x2.84x1_232

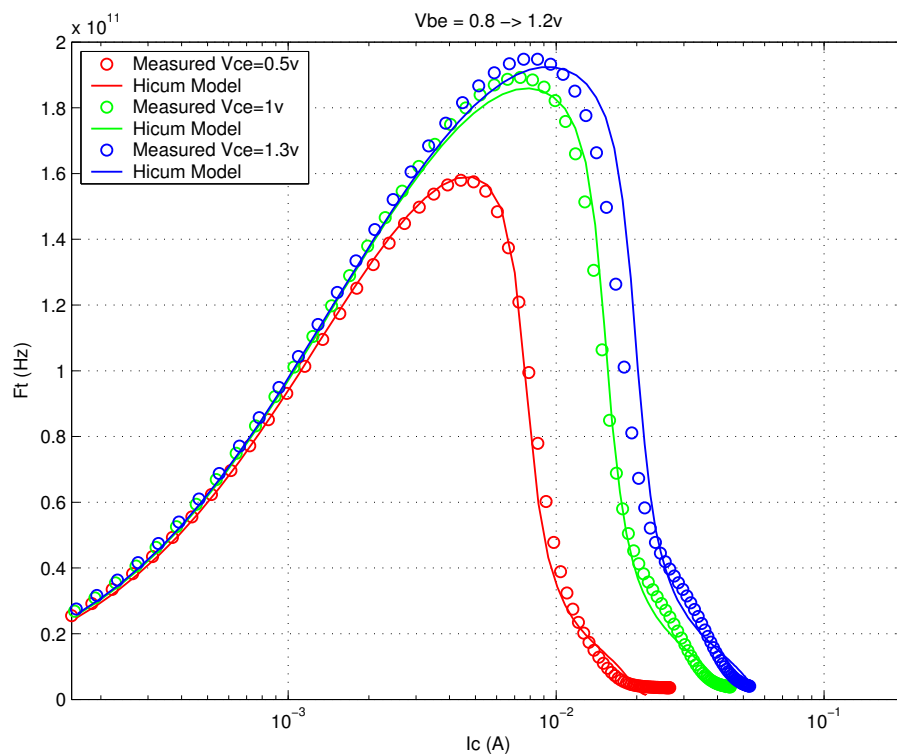
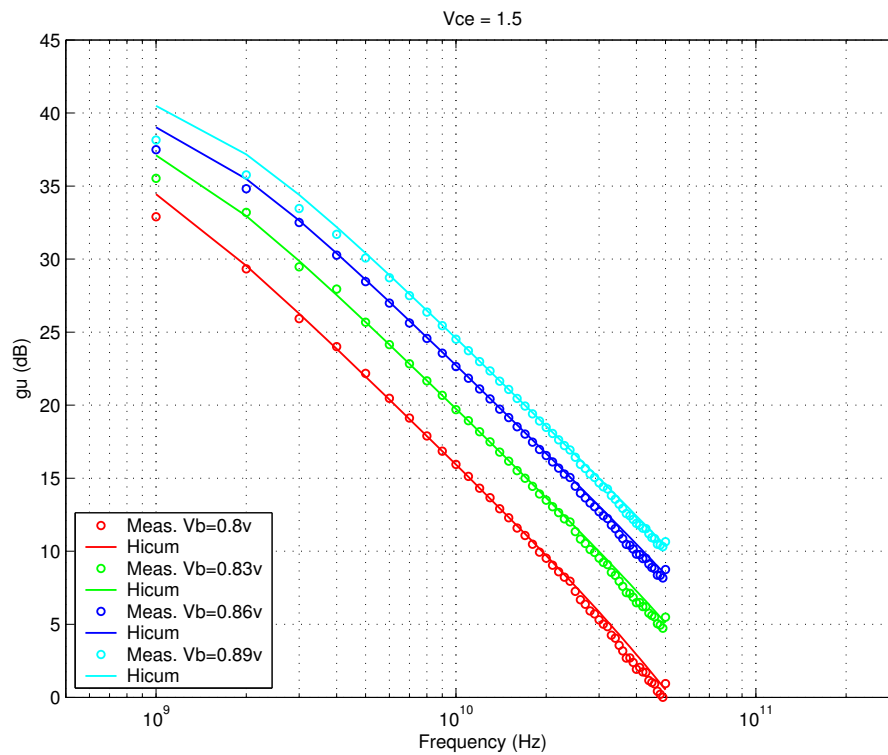
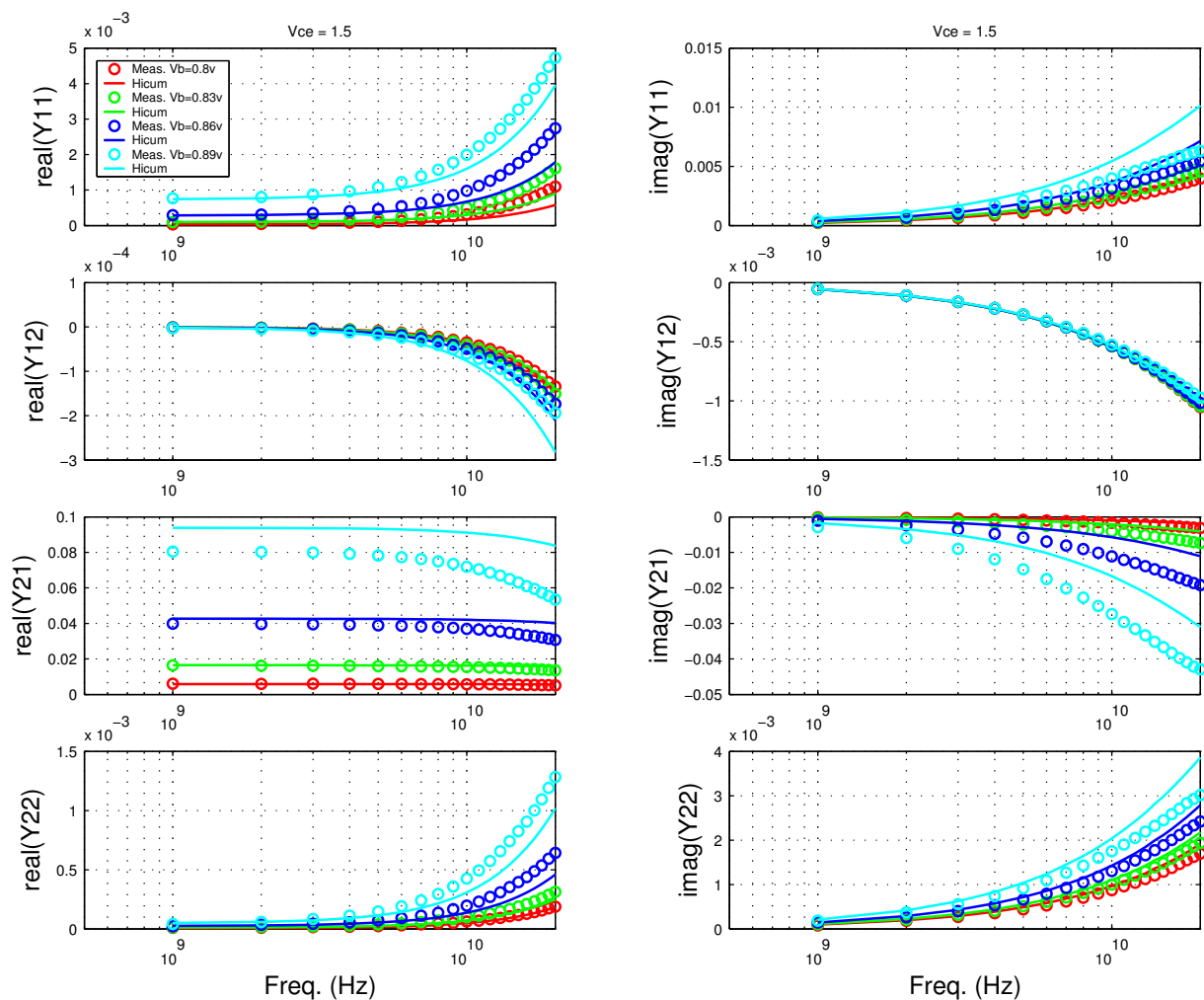


FIGURE 5.43 Power Gain vs. Freq: LV 0.15x2.84x1_232



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FIGURE 5.44 Y-parameters vs. FREQ: LV 0.15x2.84x1_232



5.4.2 Medium Voltage NPN Verification Plots

FIGURE 5.45 Gummel Plot MV 0.15x8.28x1_122

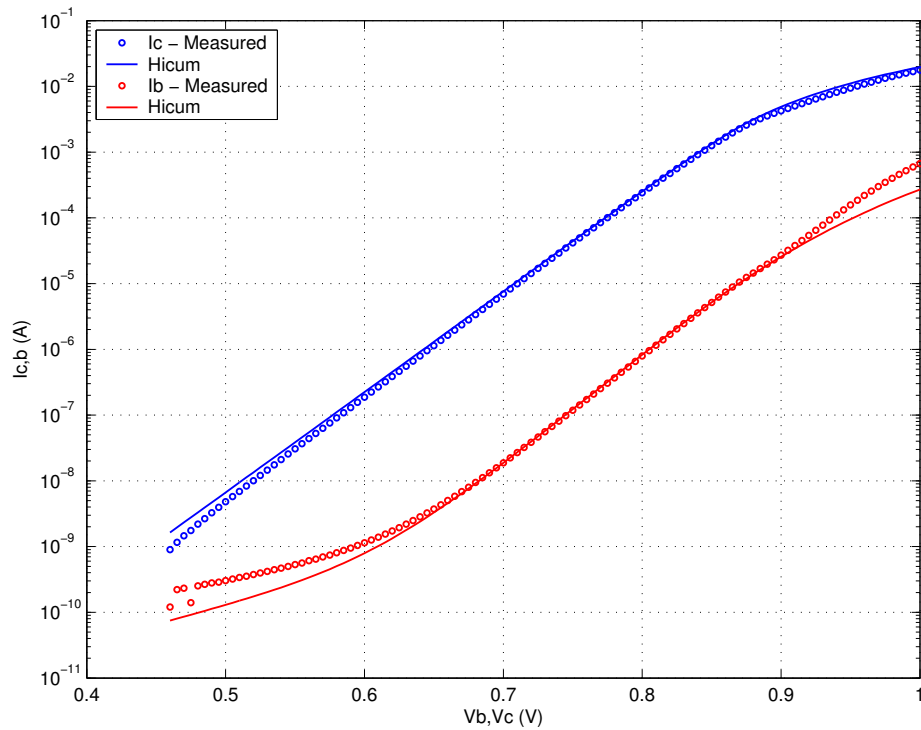


FIGURE 5.46 Beta vs. I_c : MV 0.15x8.28x1_122

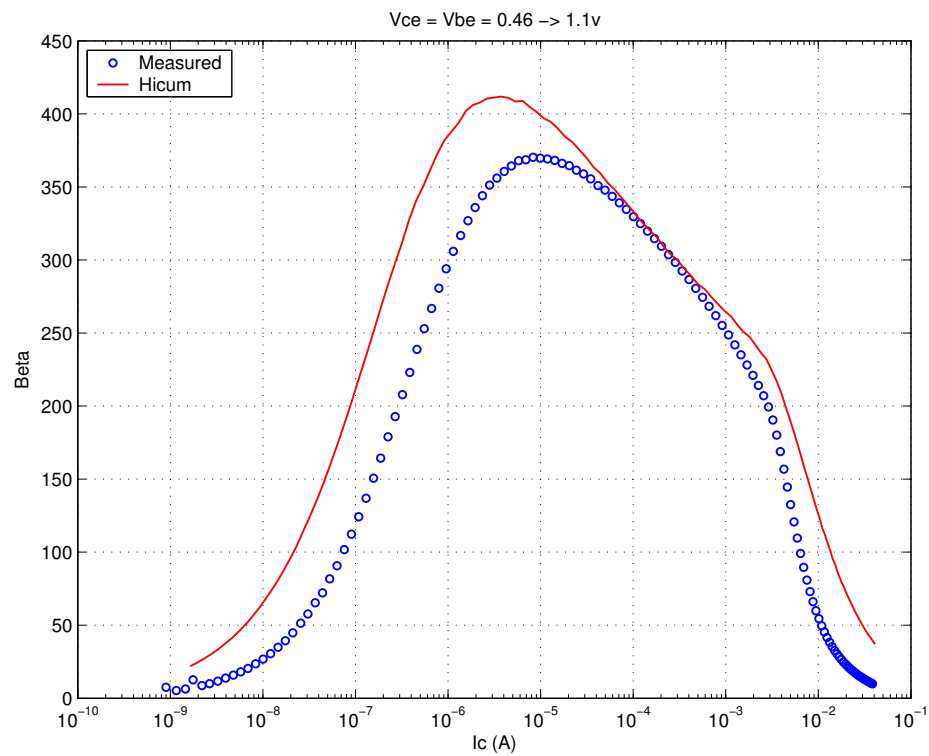


FIGURE 5.47 IC vs. VCE at constant IB: MV 0.15x8.28x1_122

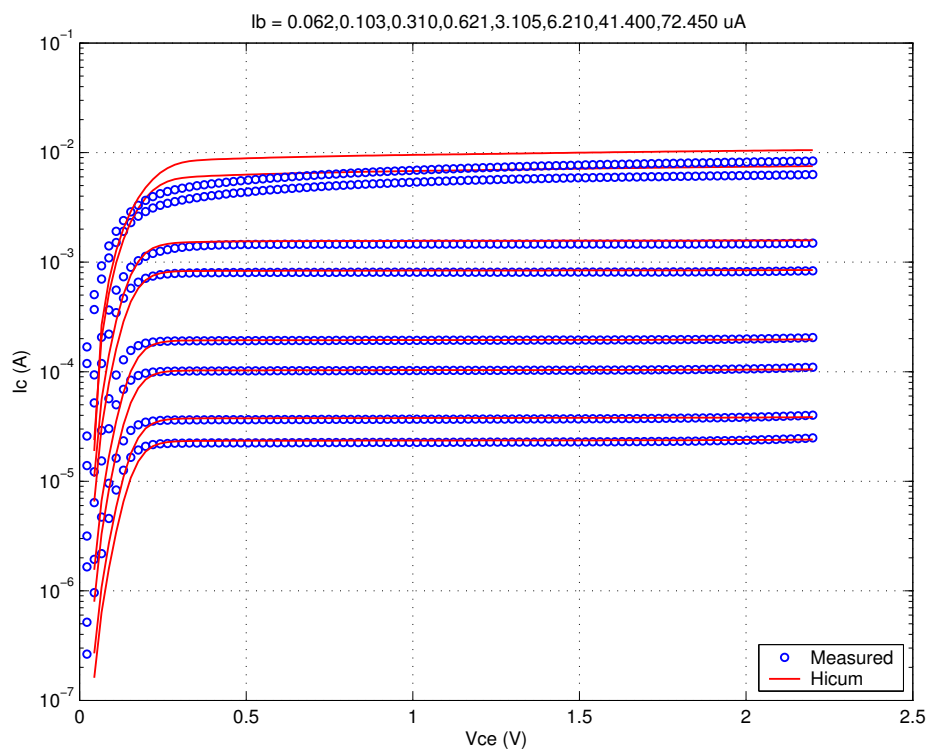


FIGURE 5.48 FT vs. IC: MV 0.15x8.28x1_122

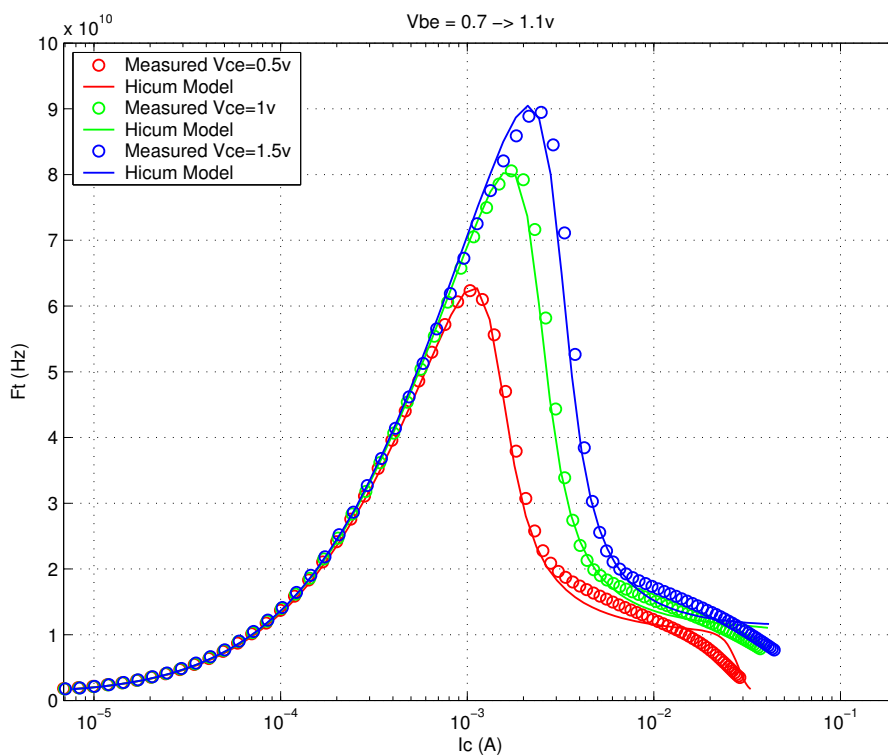
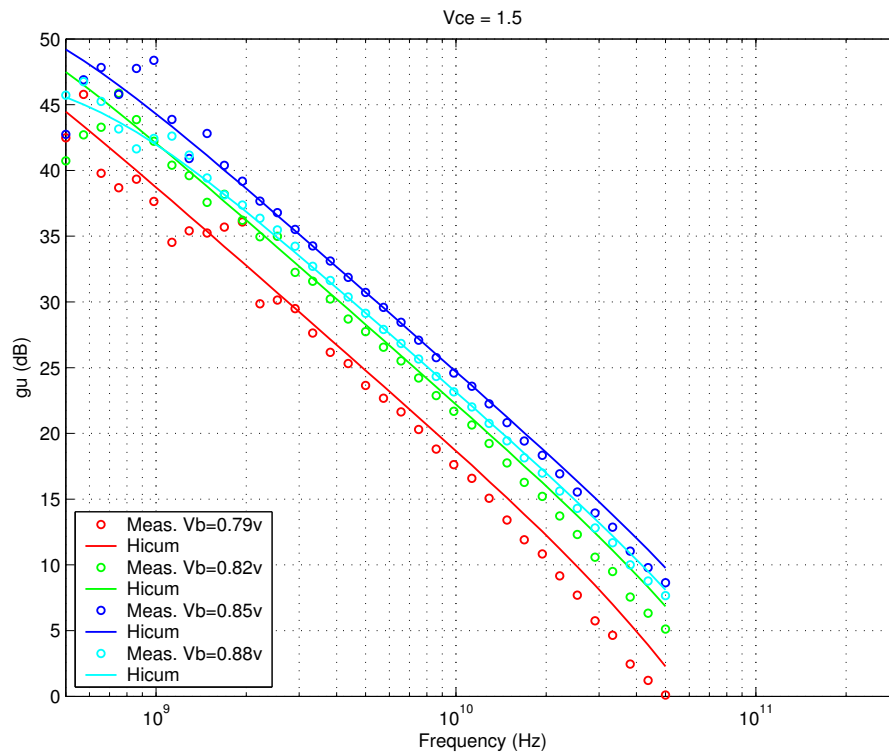


FIGURE 5.49 Power Gain vs. Freq: MV 0.15x8.28x1_122



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FIGURE 5.50 Y-parameters vs. FREQ: MV 0.15x8.28x1_122

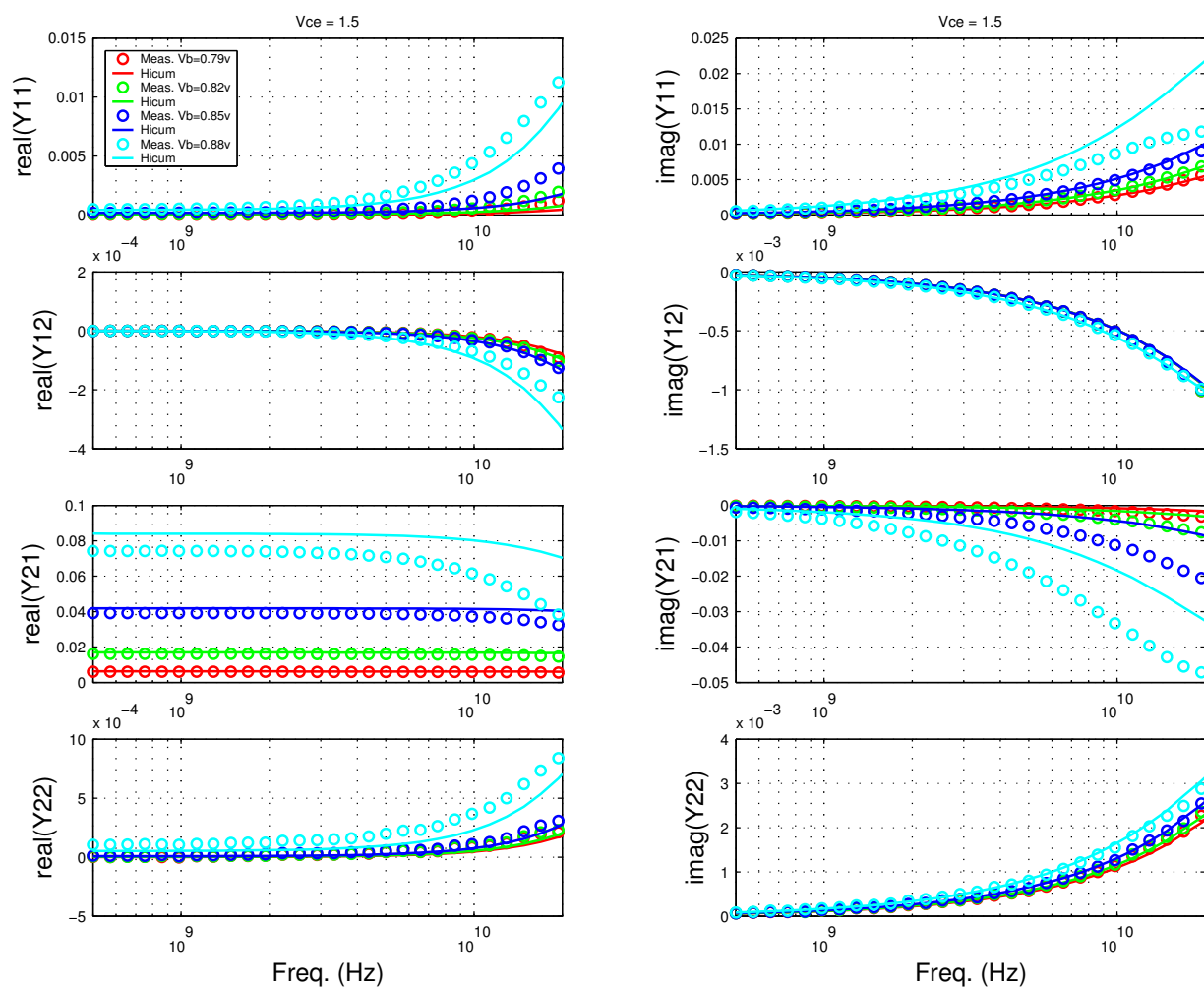


FIGURE 5.51 Gummel Plot MV 0.15x4.52x1_122

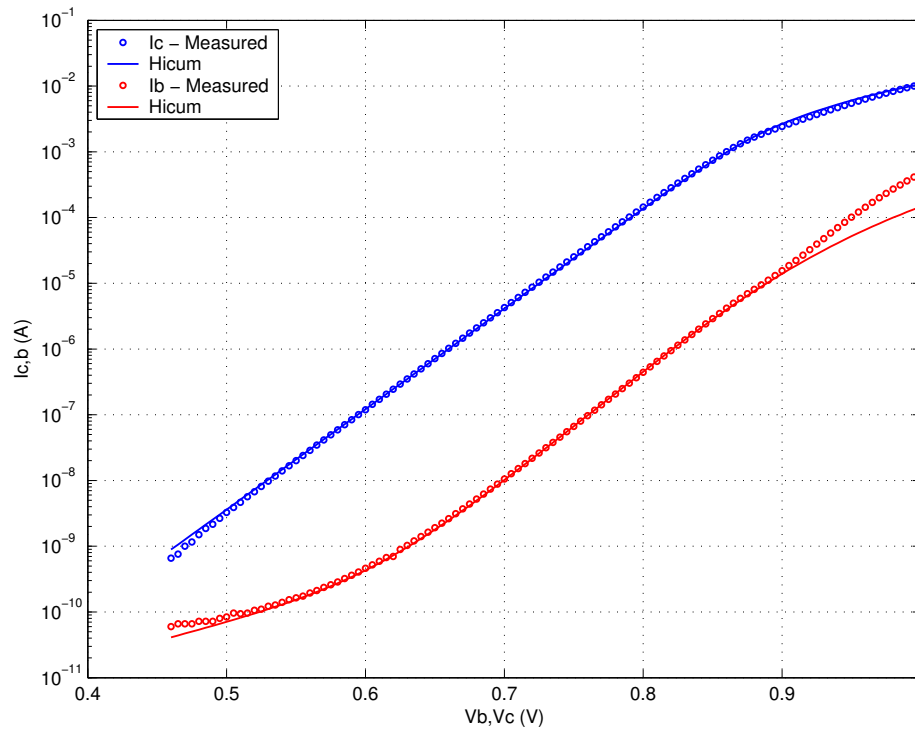
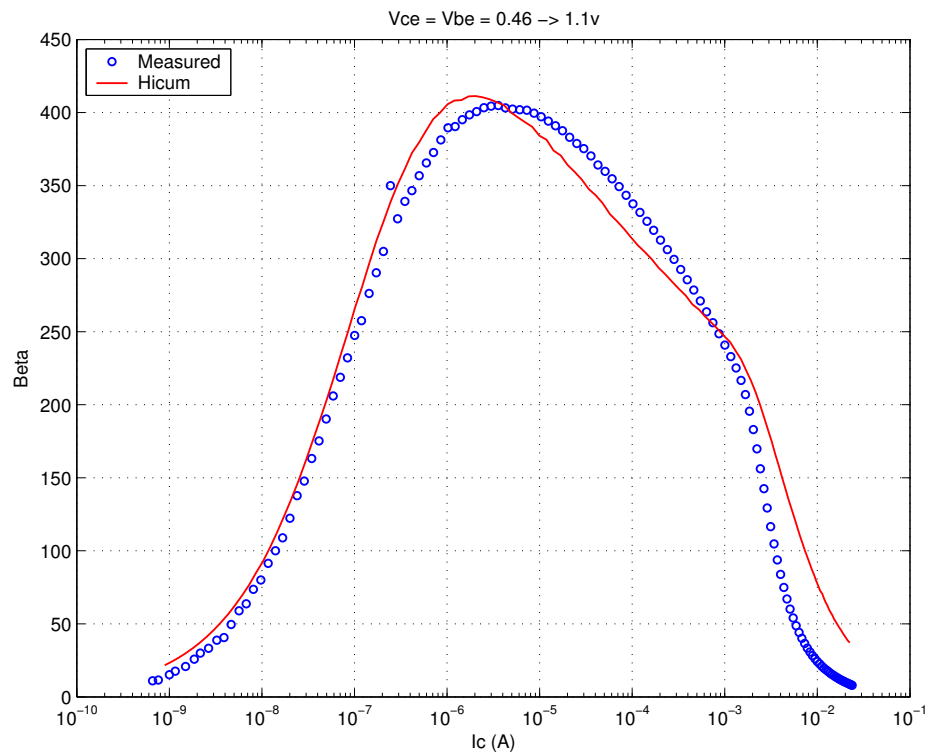
FIGURE 5.52 Beta vs. I_c : MV 0.15x4.52x1_122

FIGURE 5.53 IC vs. VCE at constant IB: MV 0.15x4.52x1_122

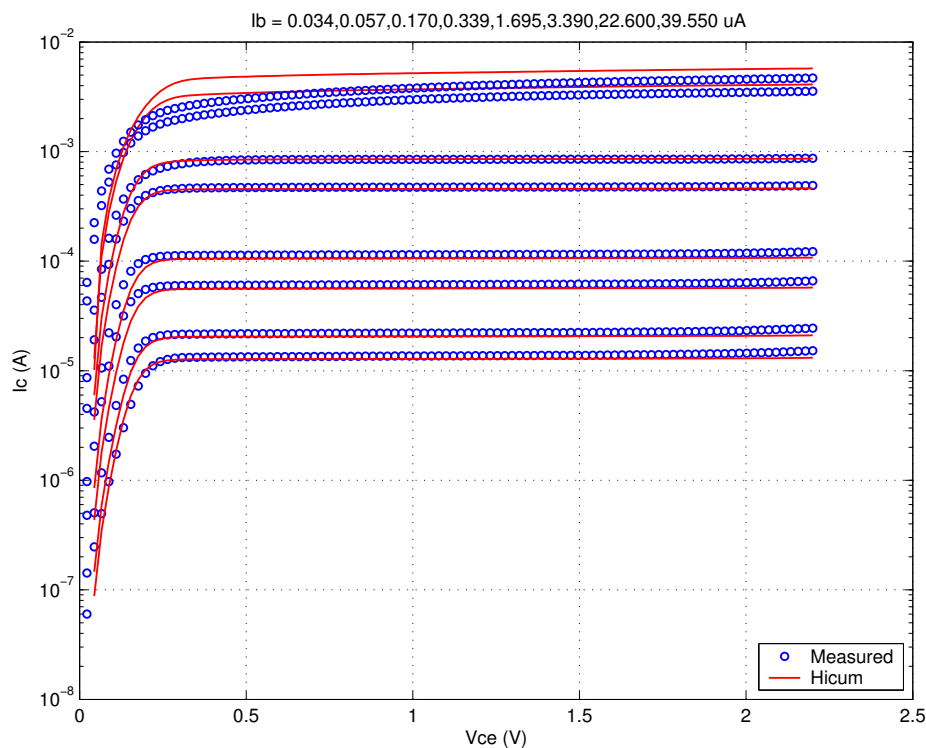


FIGURE 5.54 FT vs. IC: MV 0.15x4.52x1_122

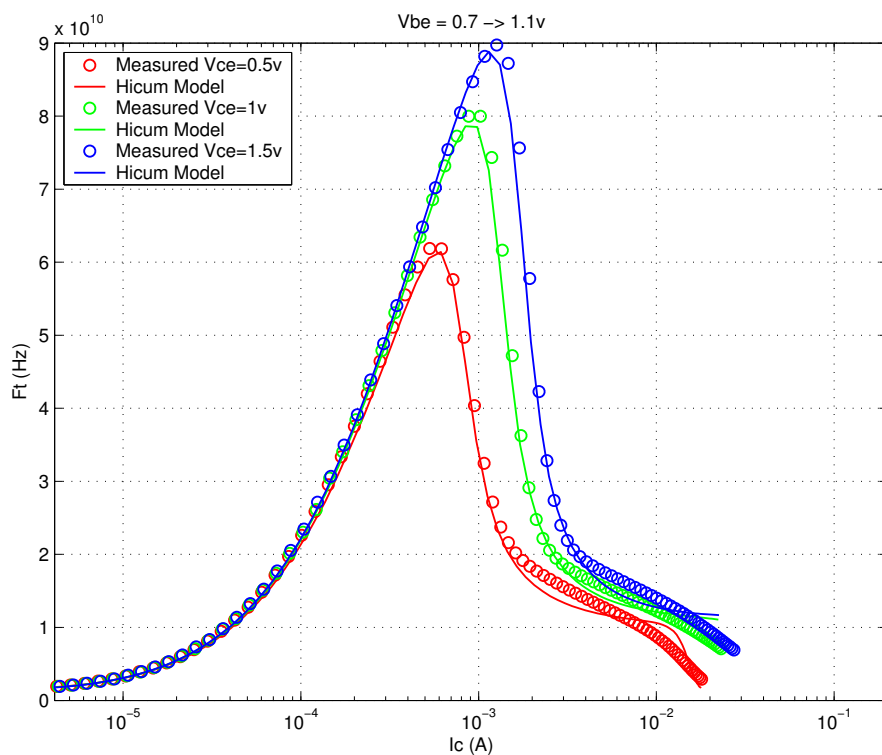
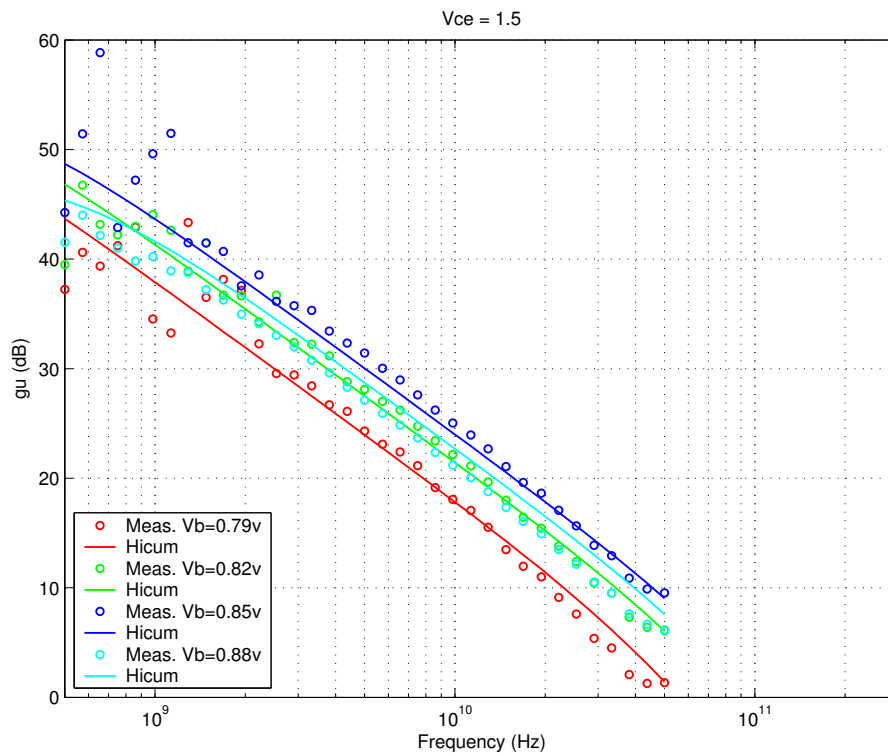


FIGURE 5.55 Power Gain vs. Freq: MV 0.15x4.52x1_122



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FIGURE 5.56 Y-parameters vs. FREQ: MV 0.15x4.52x1_122

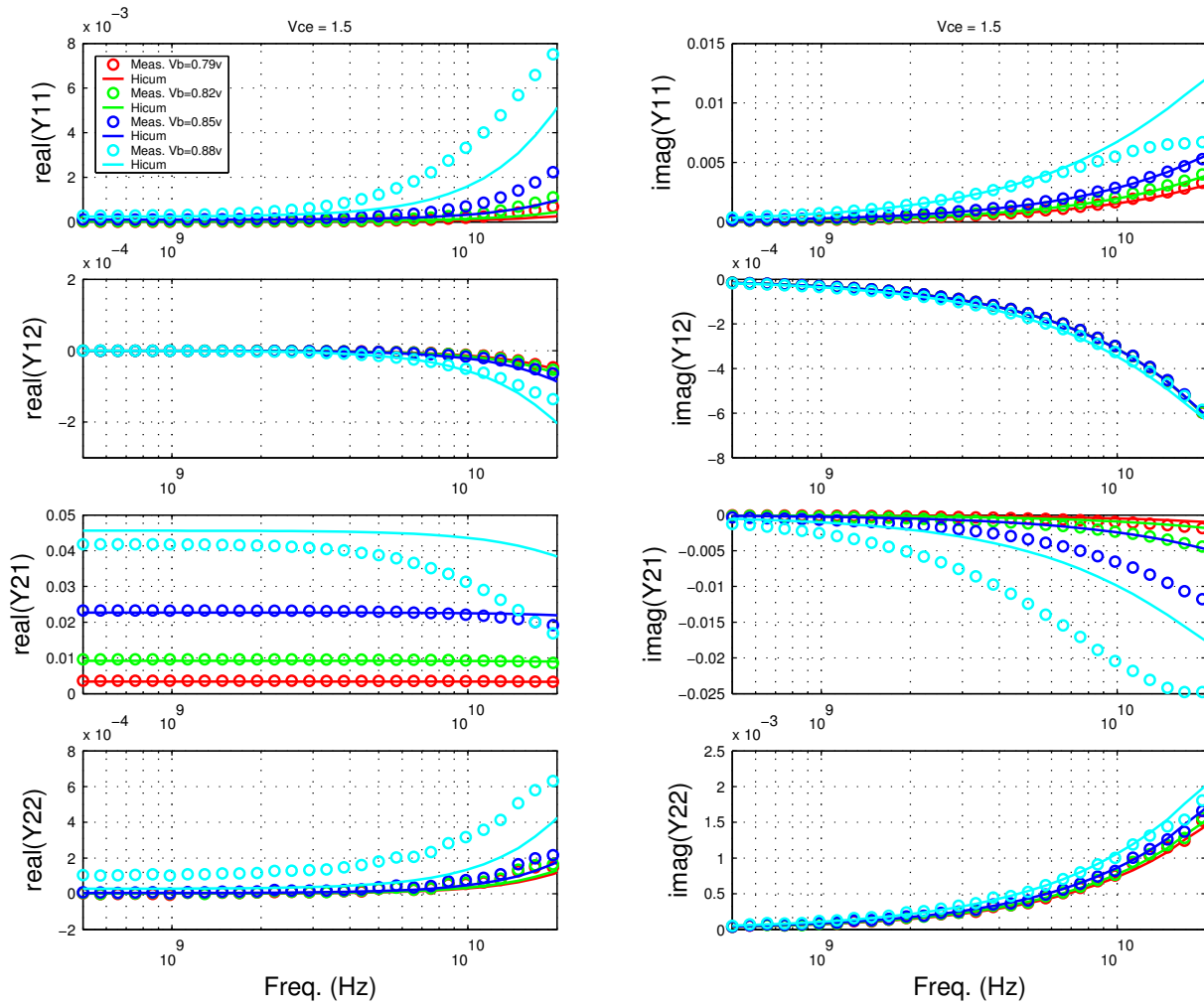


FIGURE 5.57 Gummel Plot: MV 0.15x0.76x10_122

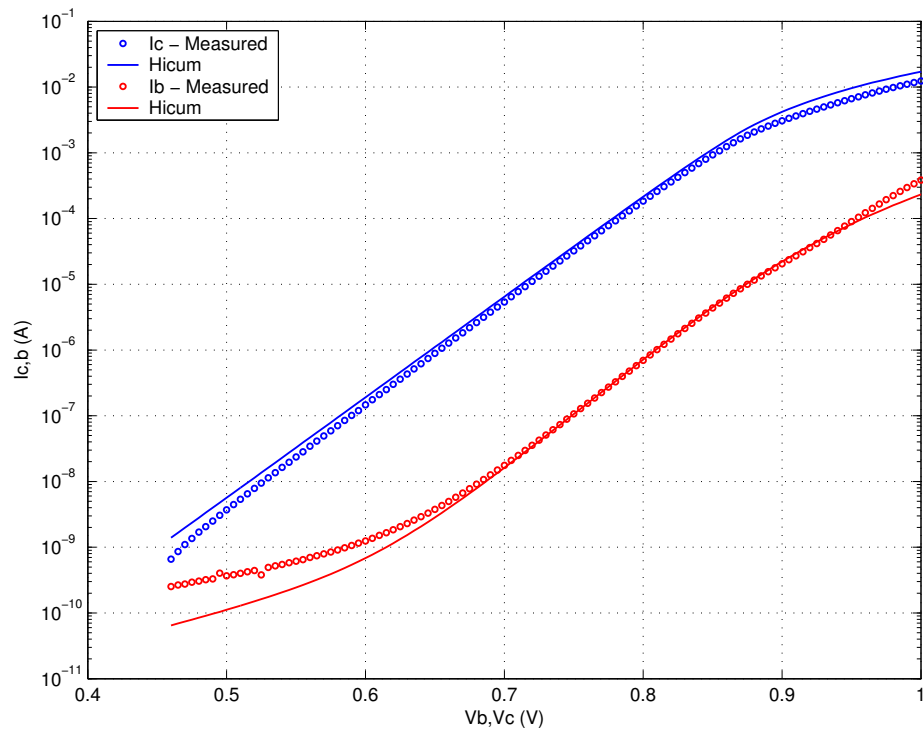
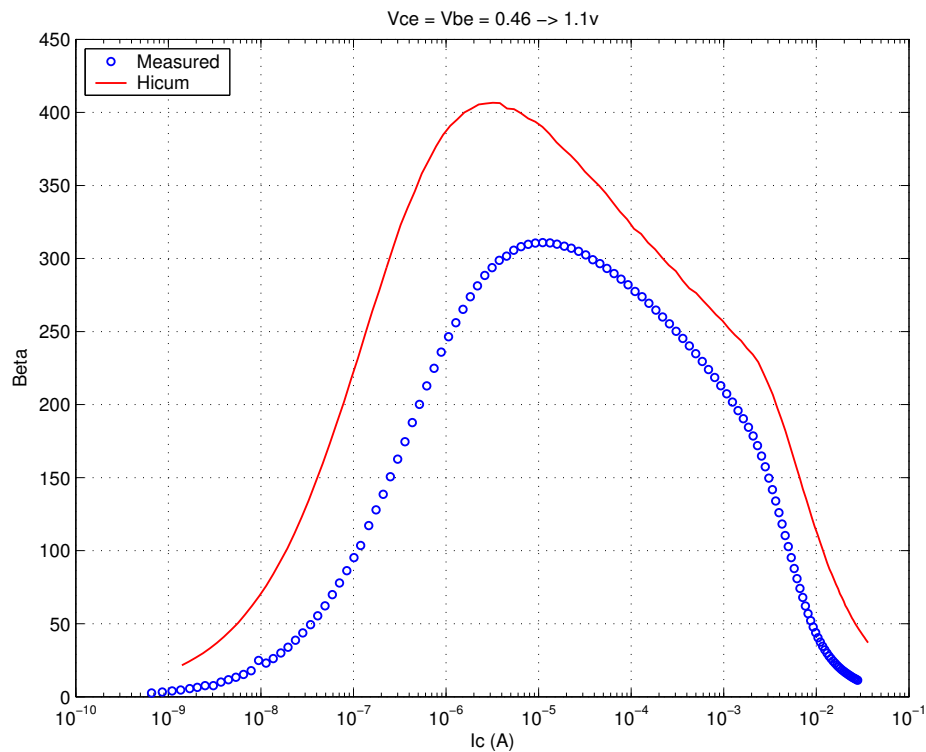
FIGURE 5.58 Beta vs. I_c : MV 0.15x0.76x10_122

FIGURE 5.59 I_C vs. V_{CE} at constant I_B : MV 0.15x0.76x10_122

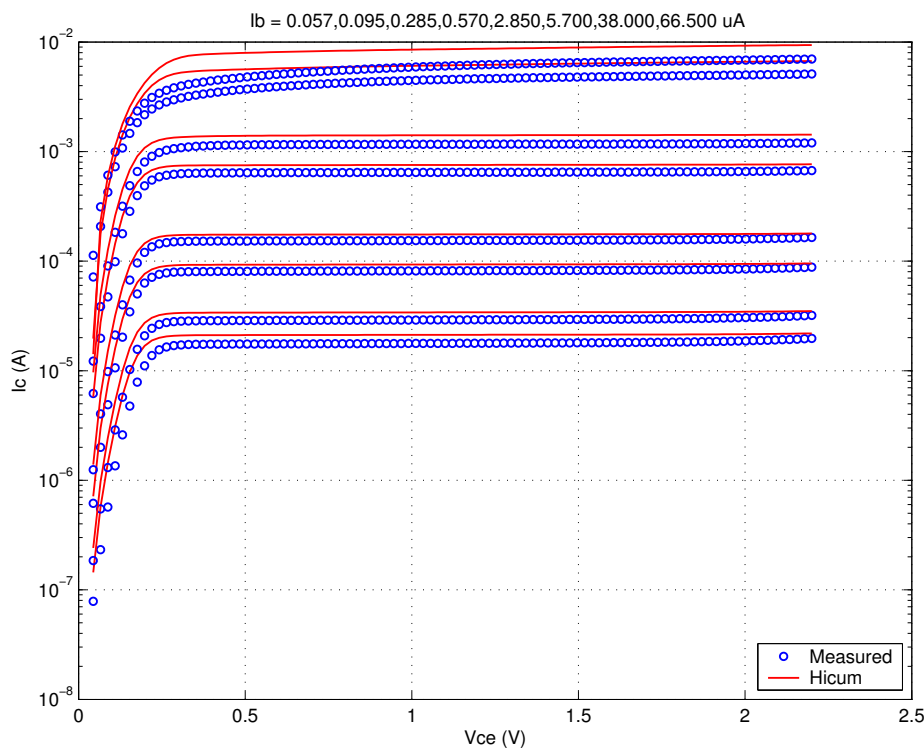


FIGURE 5.60 f_T vs. I_C : MV 0.15x0.76x10_122

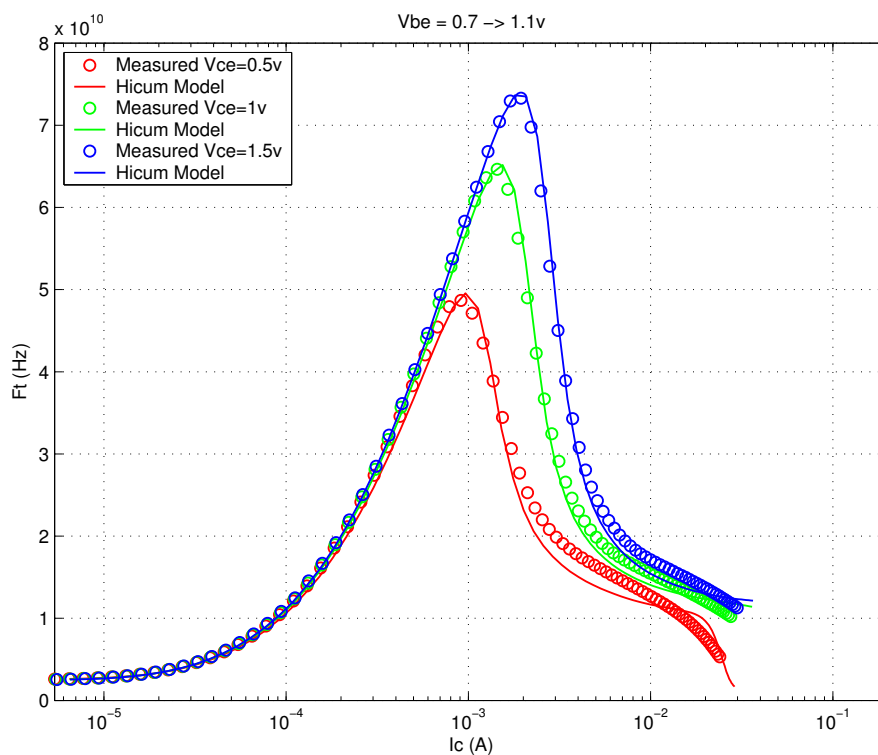
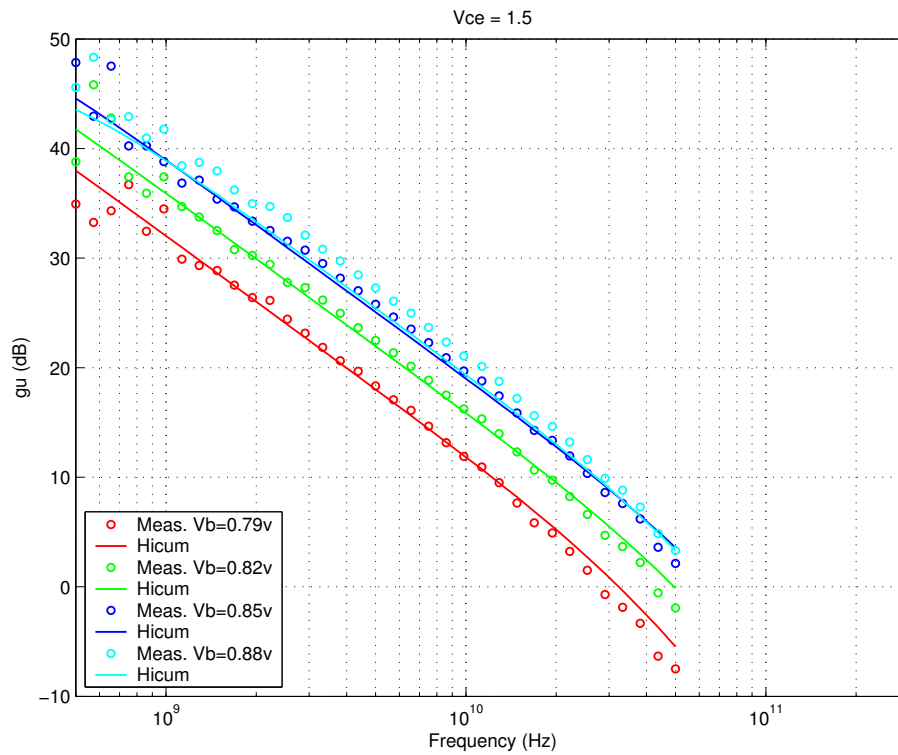


FIGURE 5.61 Power Gain vs. Freq: MV 0.15x0.76x10_122



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FIGURE 5.62 Y-parameters vs. FREQ: MV 0.15x0.76x10_122

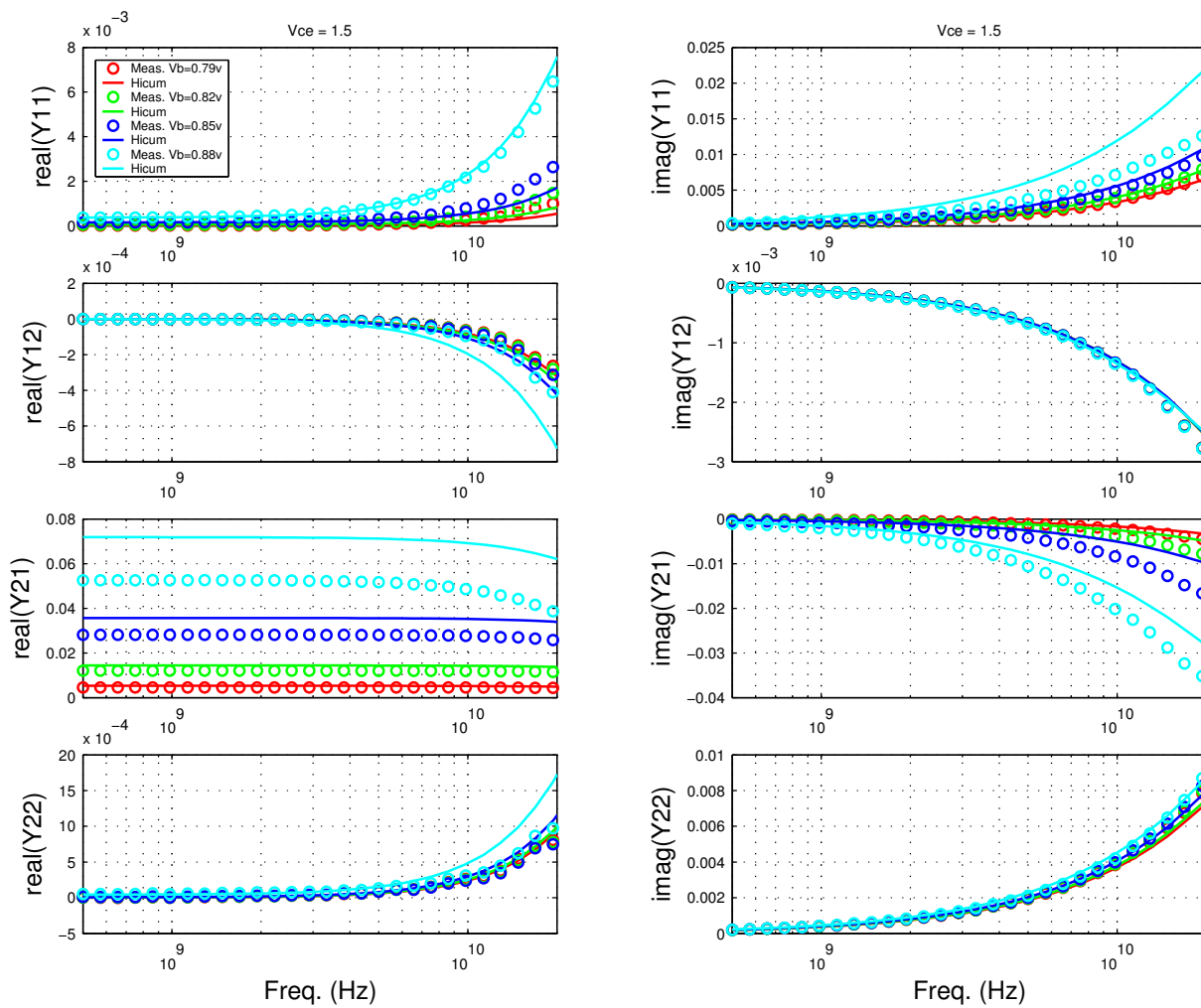


FIGURE 5.63 Gummel Plot MV 0.15x10.16x1_121

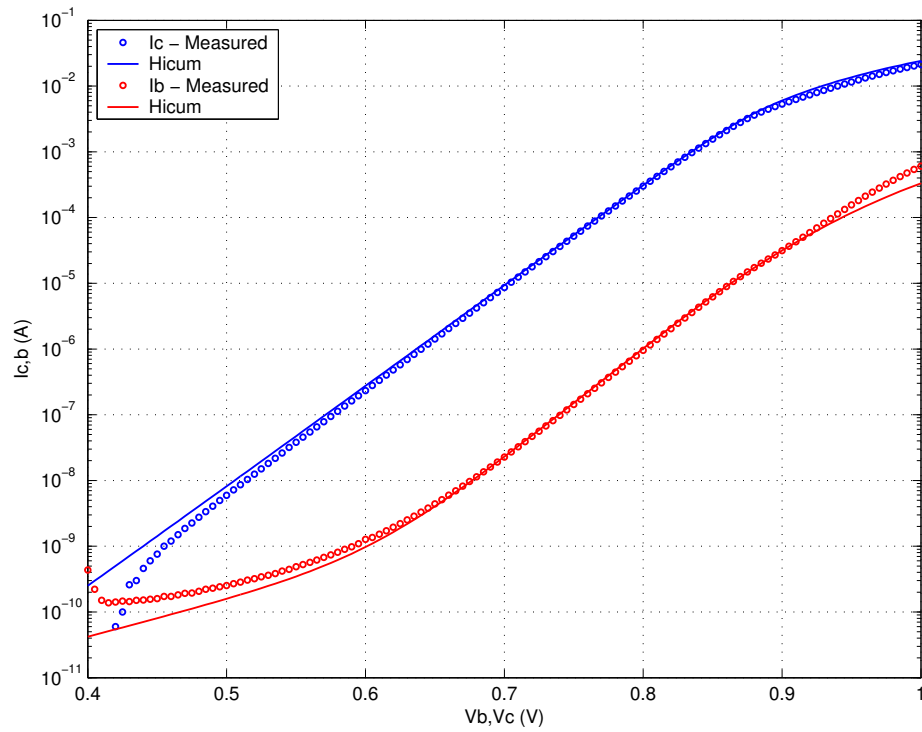
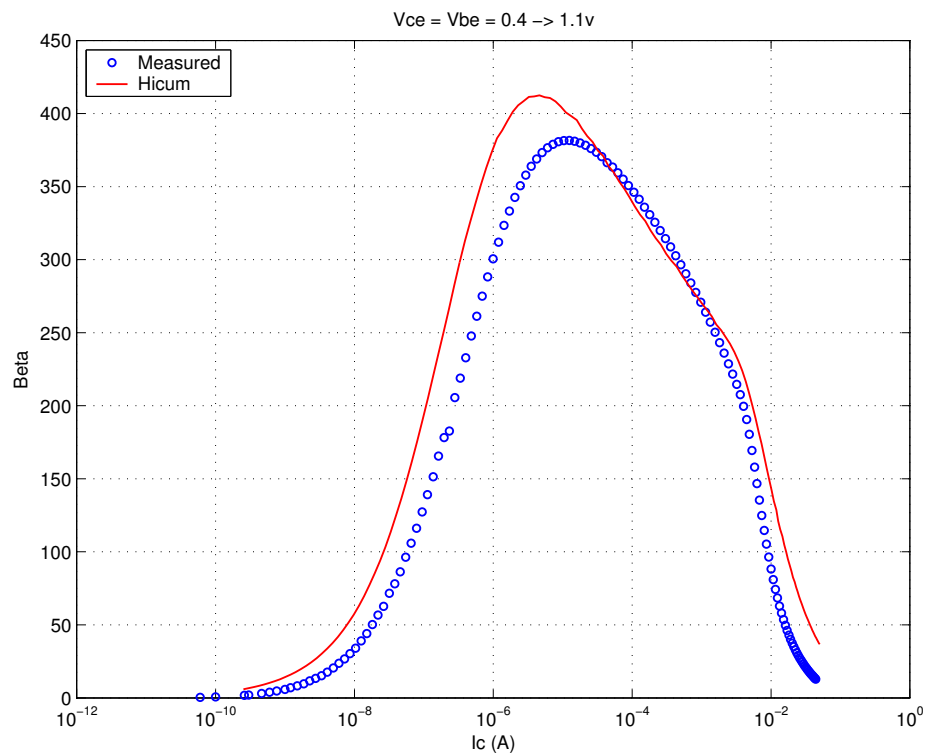
FIGURE 5.64 Beta vs. I_c : MV 0.15x10.16x1_121

FIGURE 5.65 I_C vs. V_{CE} at constant I_B : MV 0.15x10.16x1_121

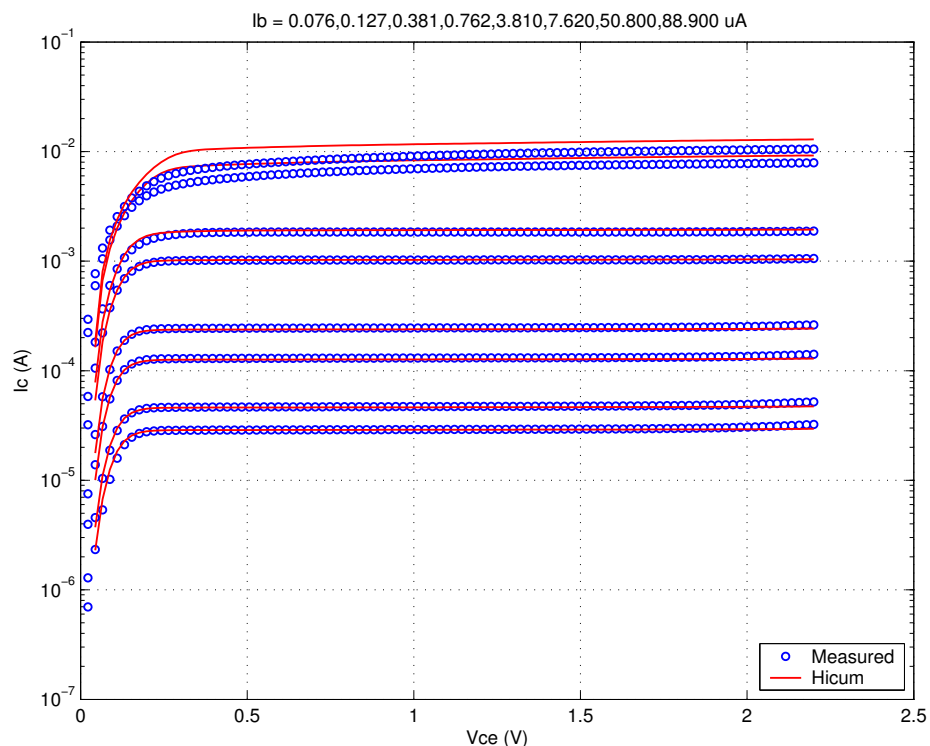


FIGURE 5.66 F_T vs. I_C : MV 0.15x10.16x1_121

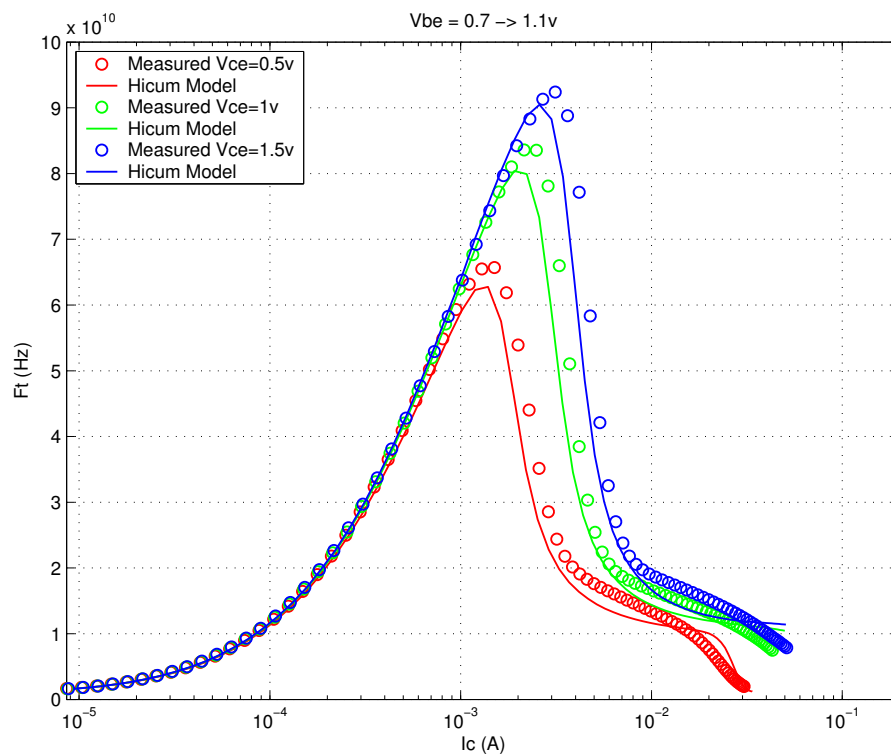
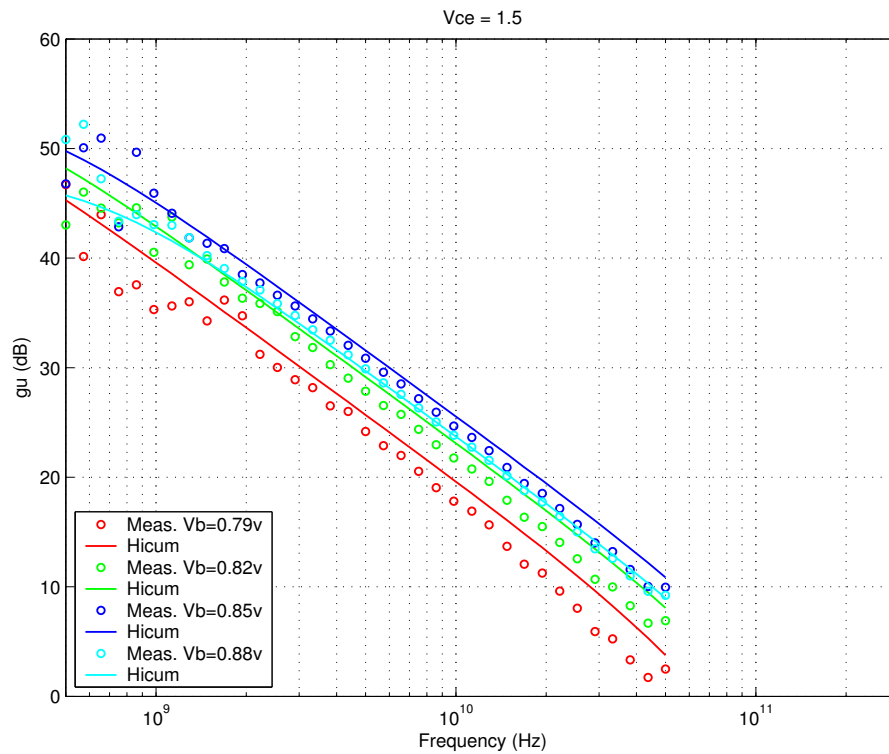


FIGURE 5.67 Power Gain vs. Freq: MV 0.15x10.16x1_121



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FIGURE 5.68 Y-parameters vs. FREQ: MV 0.15x10.16x1_121

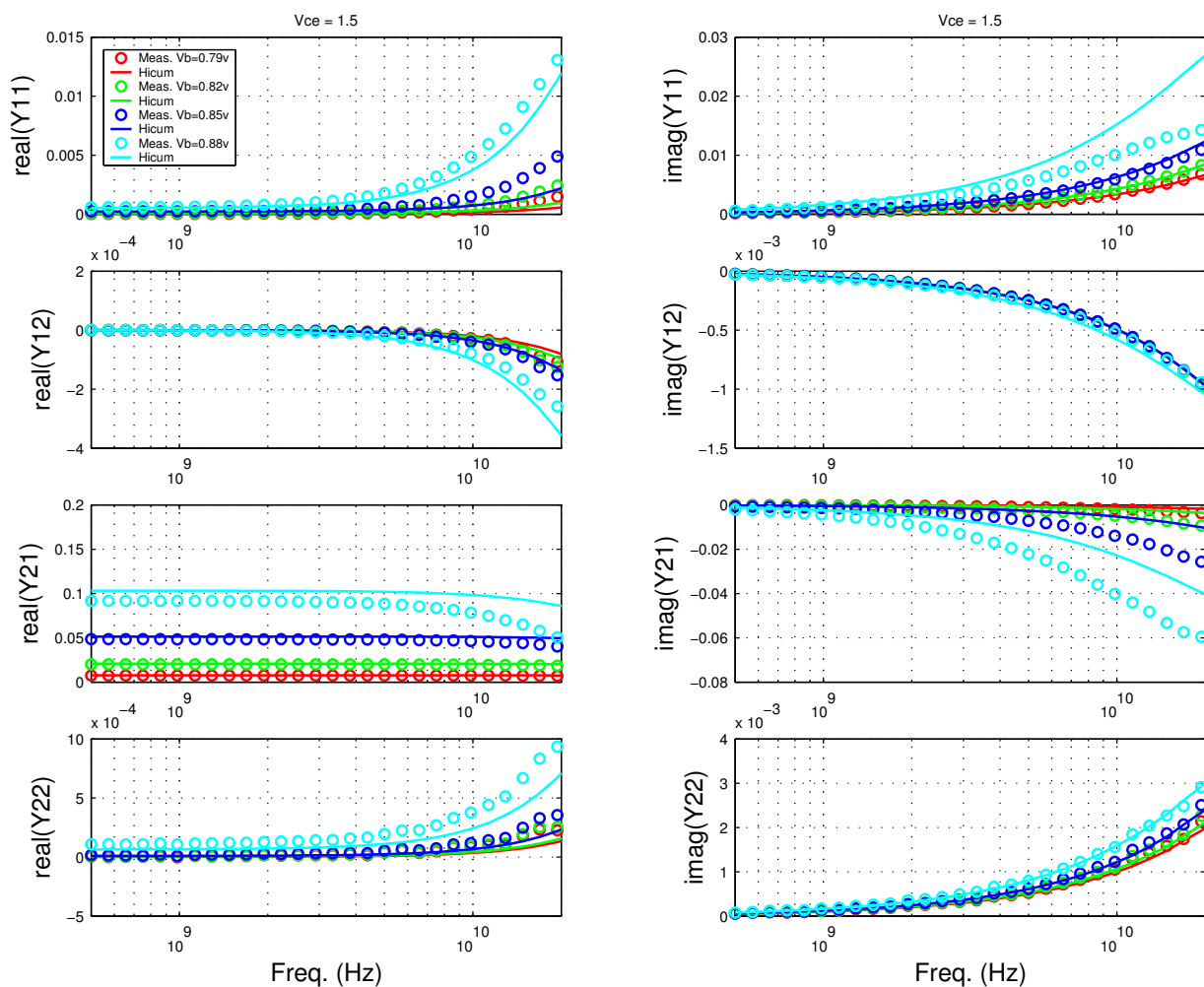


FIGURE 5.69 Gummel Plot MV 0.15x10.16x1_232

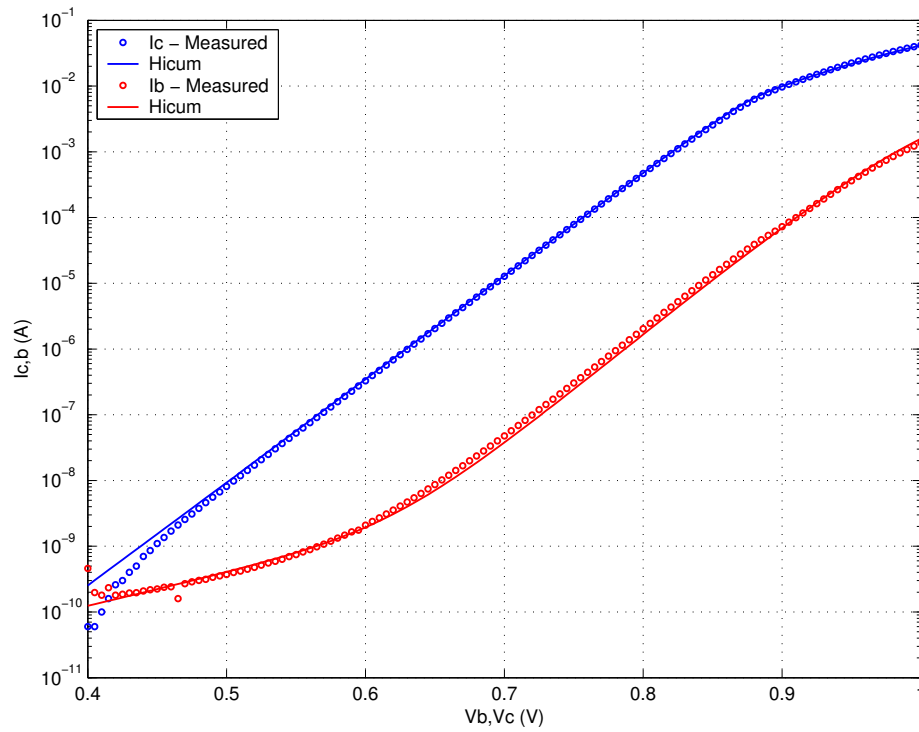
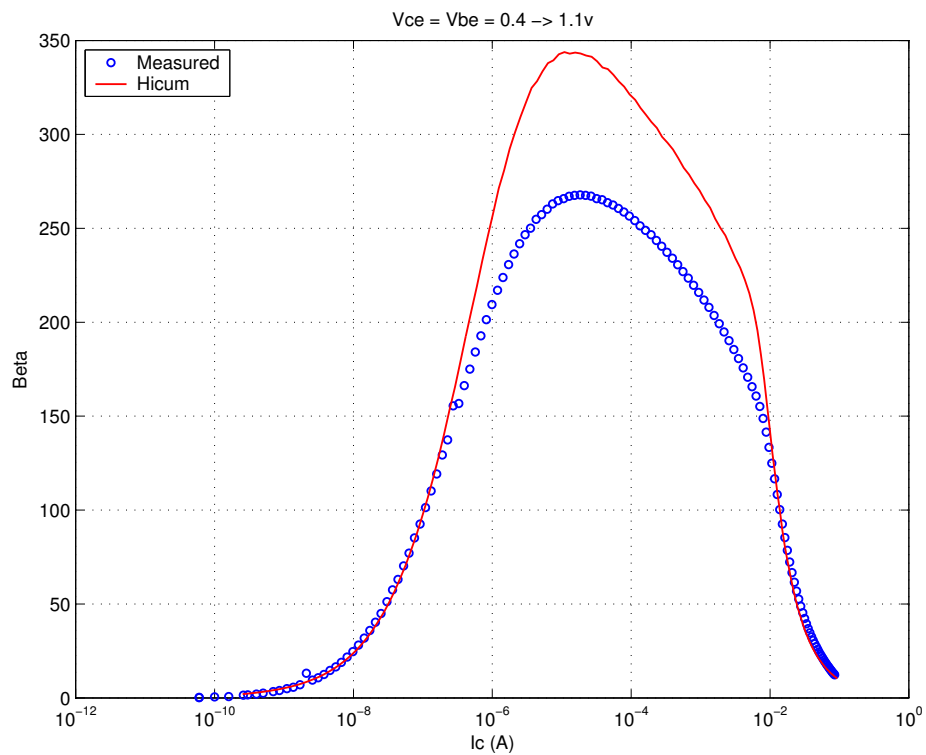
FIGURE 5.70 Beta vs. I_c : MV 0.15x10.16x1_232

FIGURE 5.71 IC vs. VCE at constant IB: MV 0.15x10.16x1_232

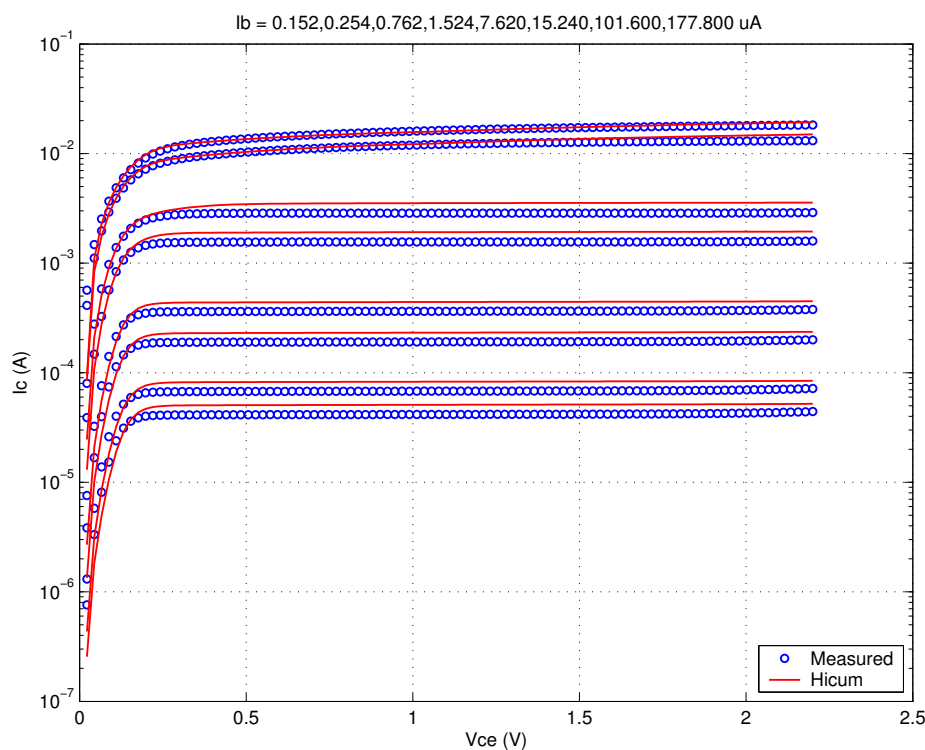


FIGURE 5.72 FT vs. IC: MV 0.15x10.16x1_232

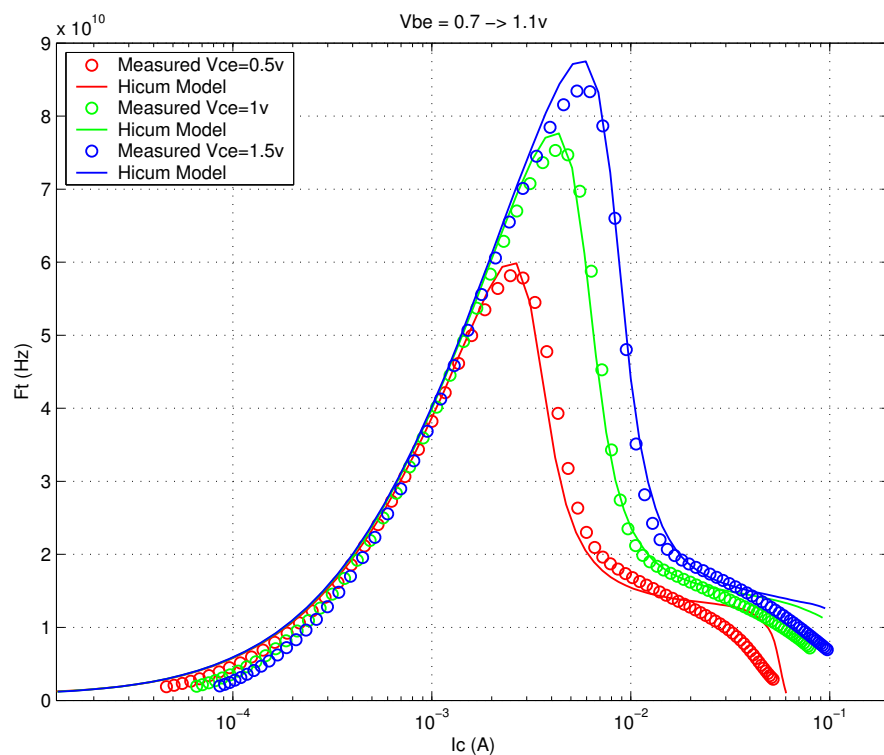
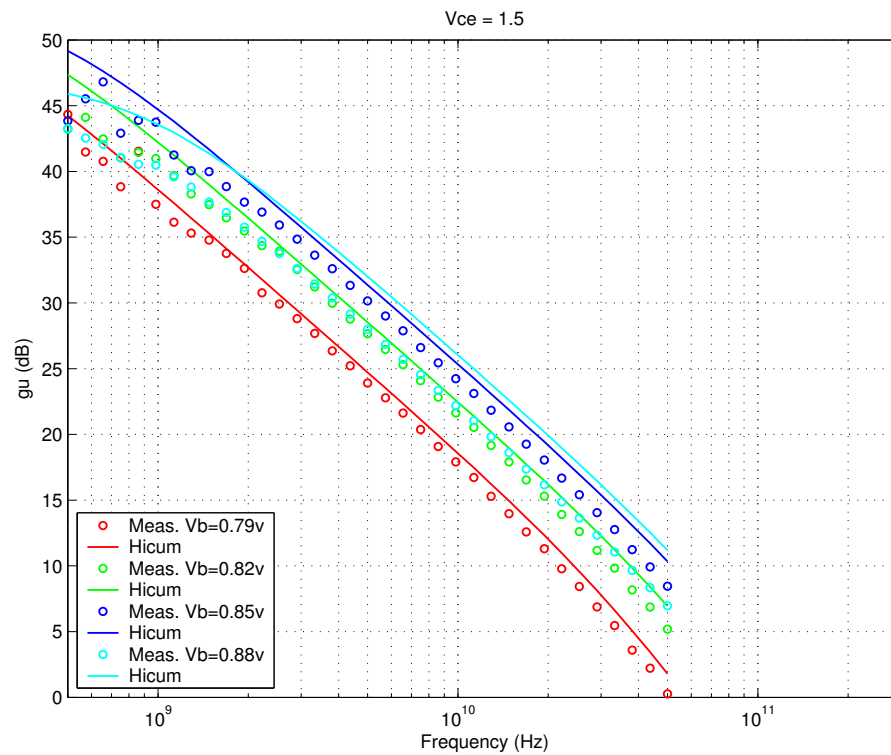


FIGURE 5.73 Power Gain vs. Freq: MV 0.15x10.16x1_232



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FIGURE 5.74 Y-parameters vs. FREQ: MV 0.15x10.16x1_232

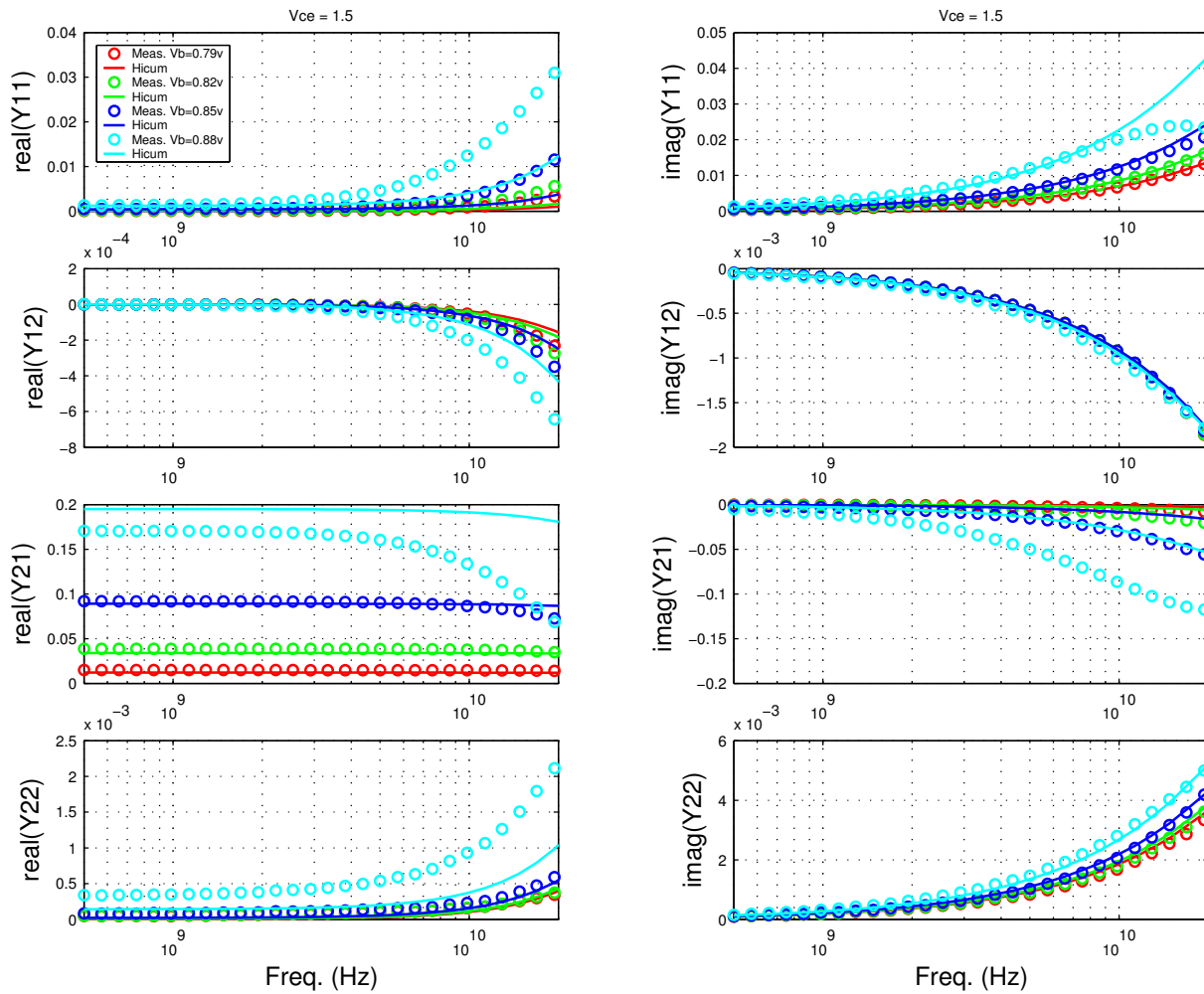


FIGURE 5.75 Gummel Plot MV 0.15x4.52x1_232

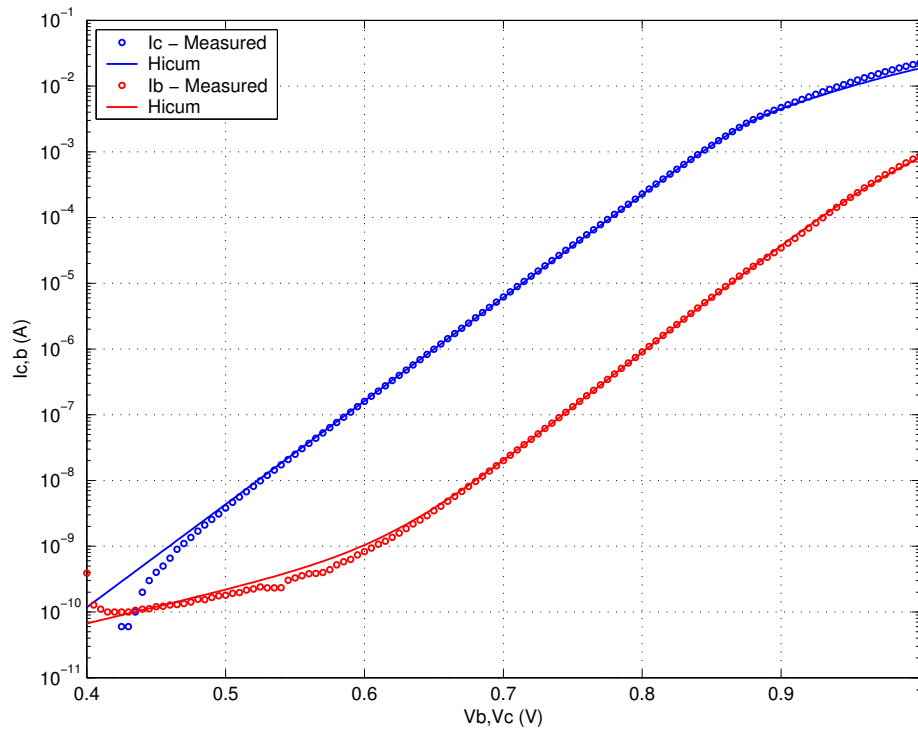
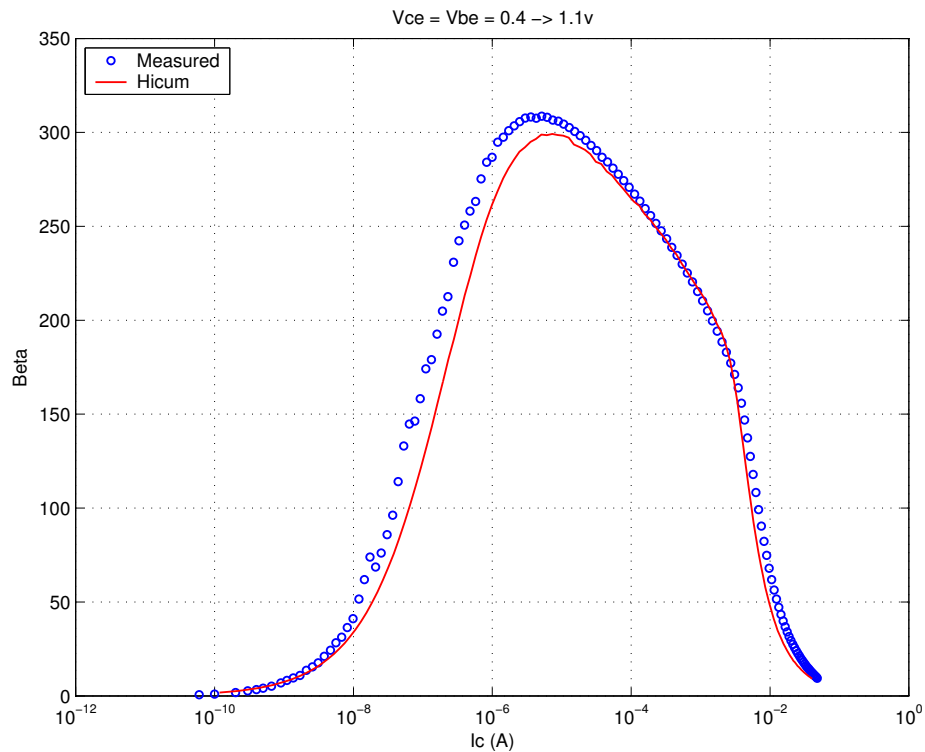
FIGURE 5.76 Beta vs. I_c : MV 0.15x4.52x1_232

FIGURE 5.77 IC vs. VCE at constant IB: MV 0.15x4.52x1_232

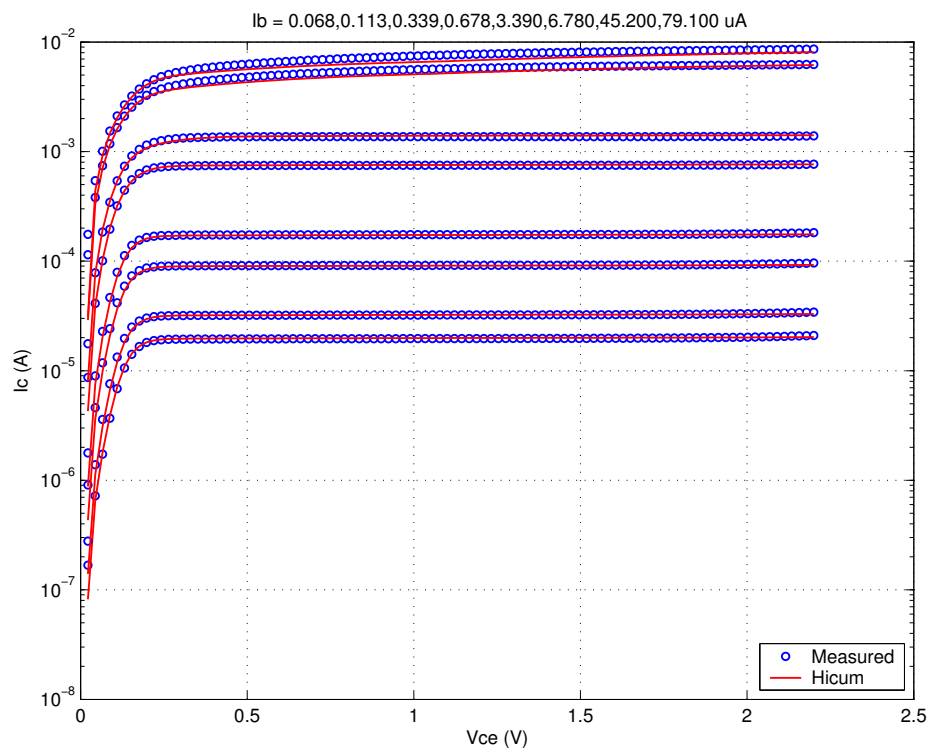


FIGURE 5.78 FT vs. IC: MV 0.15x4.52x1_232

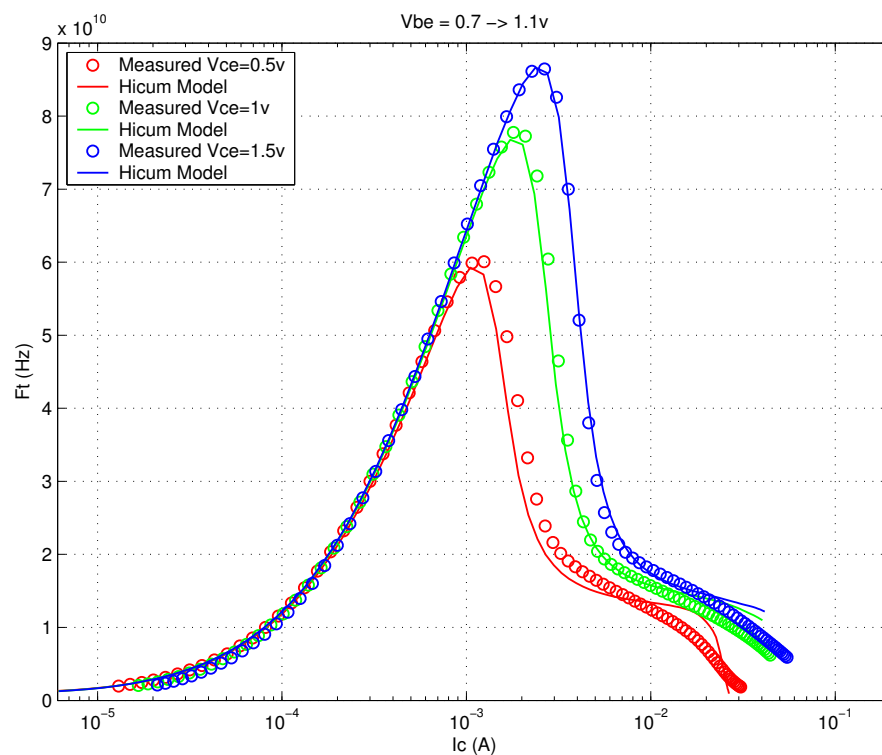
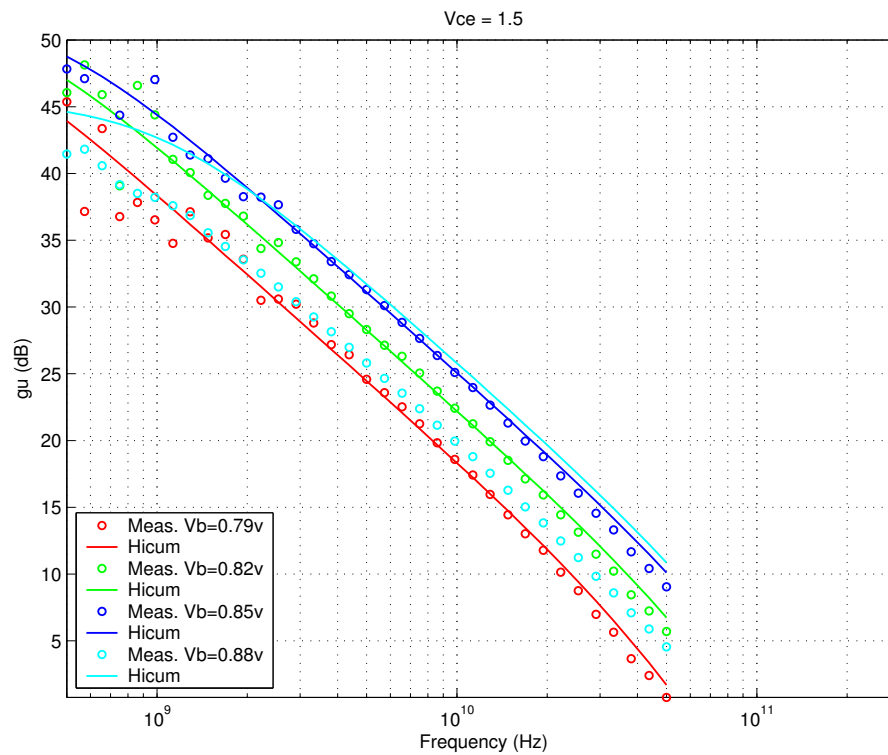


FIGURE 5.79 Power Gain vs. Freq: MV 0.15x4.52x1_232



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FIGURE 5.80 Y-parameters vs. FREQ: MV 0.15x4.52x1_232

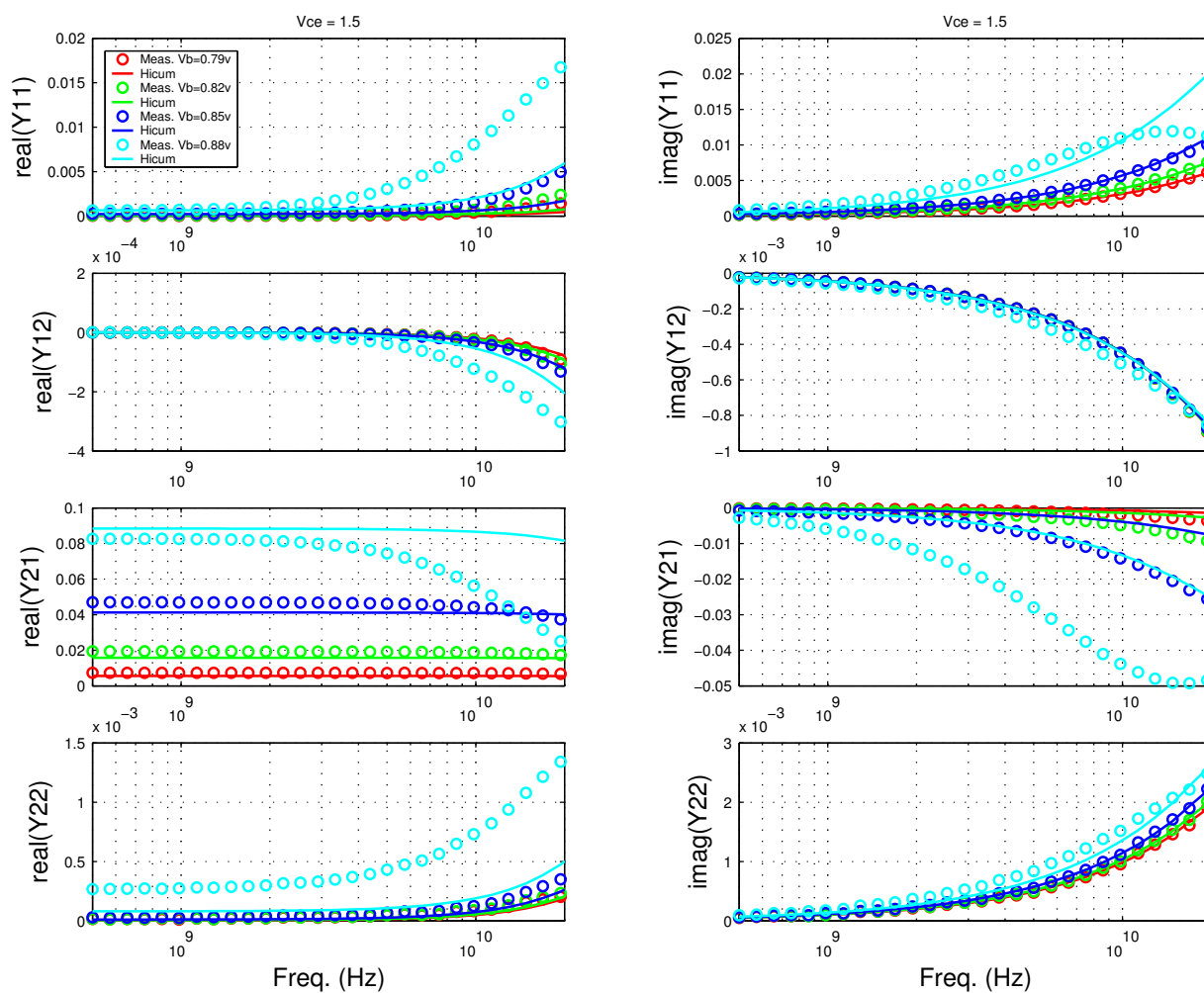


FIGURE 5.81 Gummel Plot MV 0.15x2.84x1_232

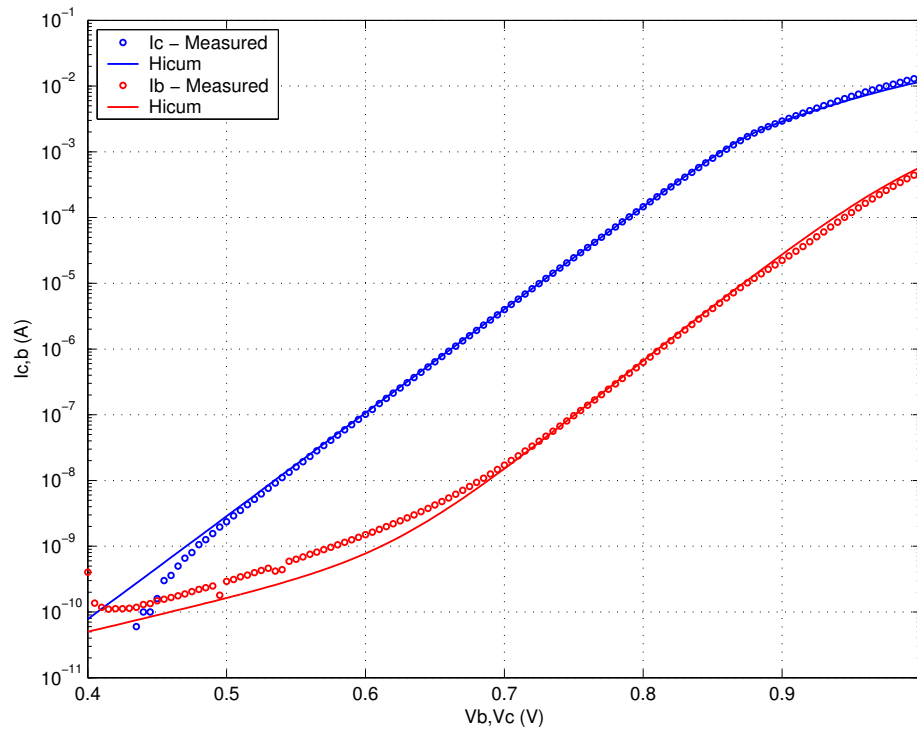
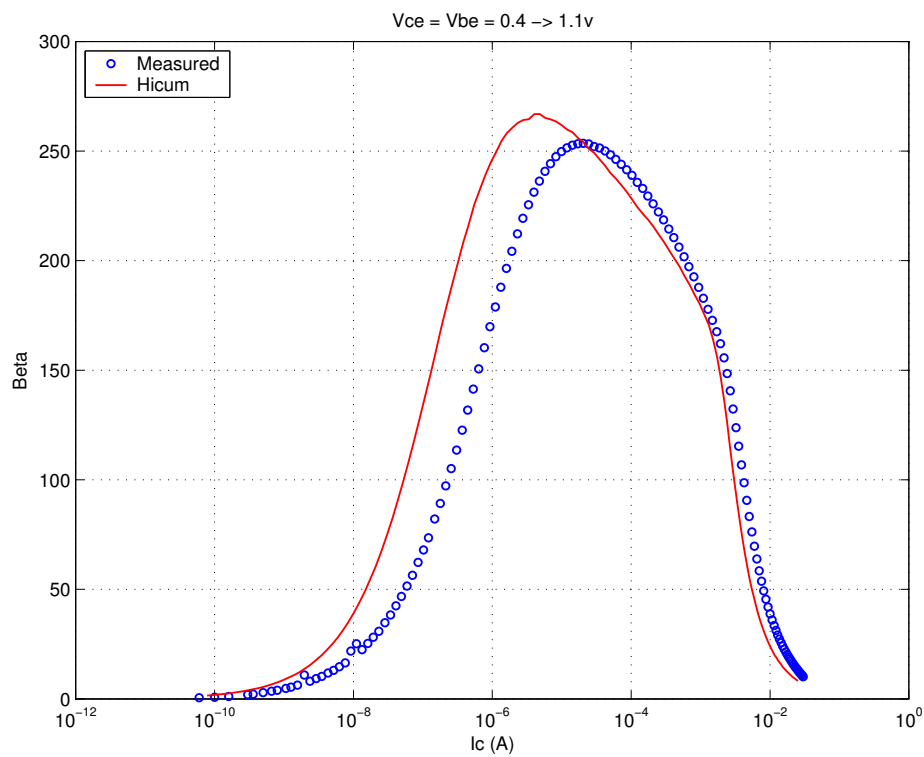
FIGURE 5.82 Beta vs. I_c : MV 0.15x2.84x1_232

FIGURE 5.83 IC vs. VCE at constant IB: MV 0.15x2.84x1_232

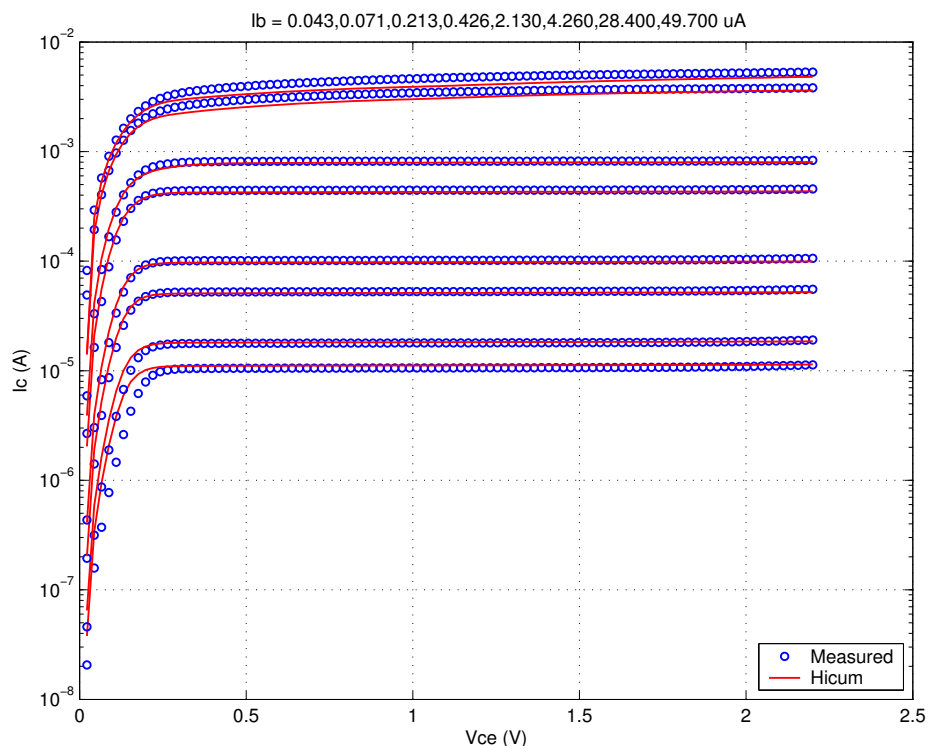


FIGURE 5.84 FT vs. IC: MV 0.15x2.84x1_232

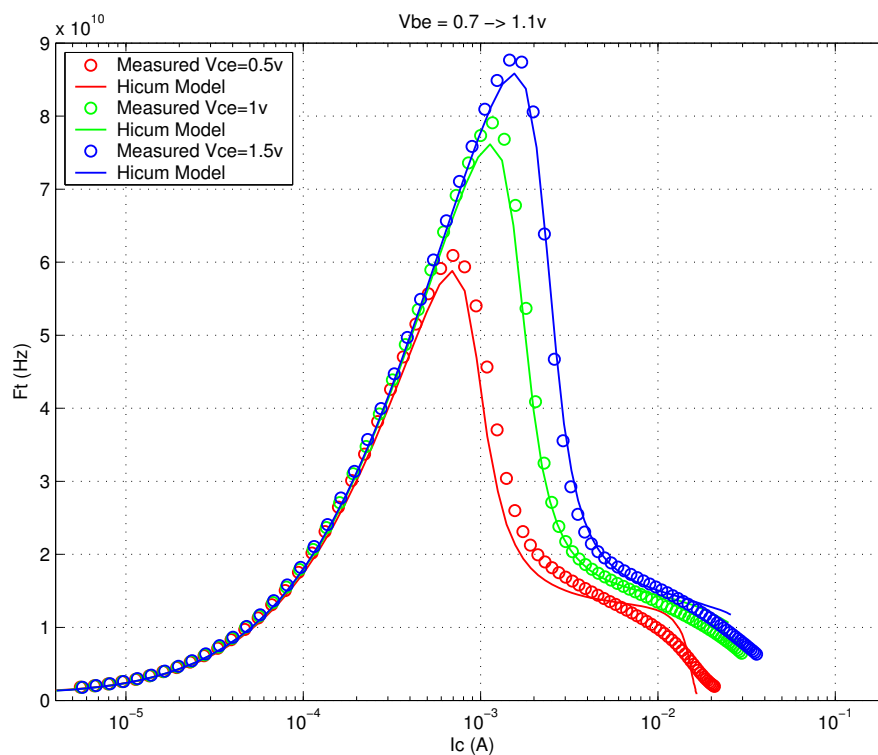
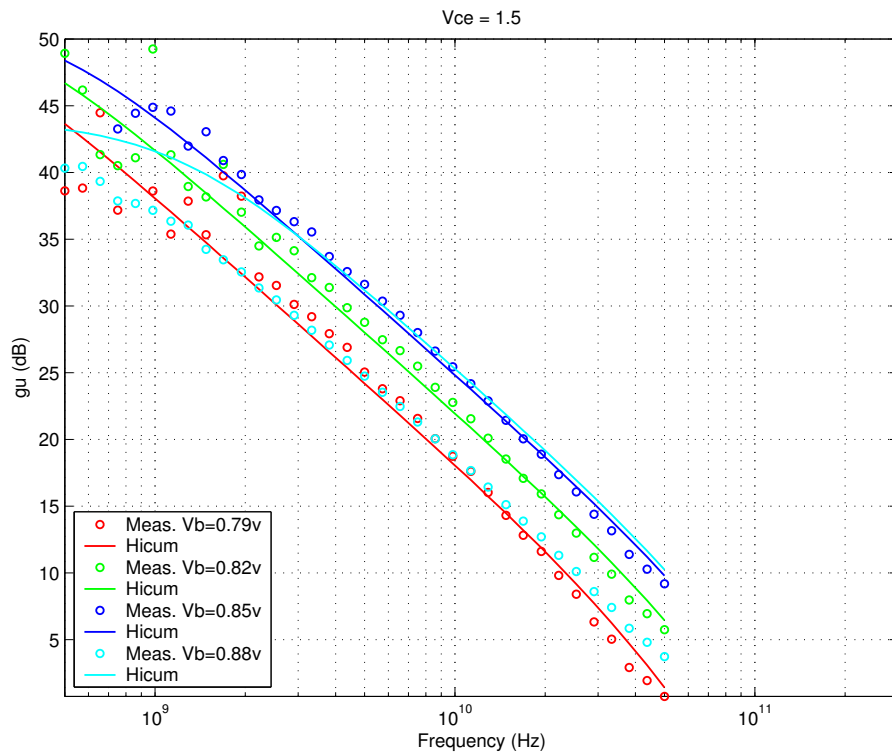


FIGURE 5.85 Power Gain vs. Freq: MV 0.15x2.84x1_232

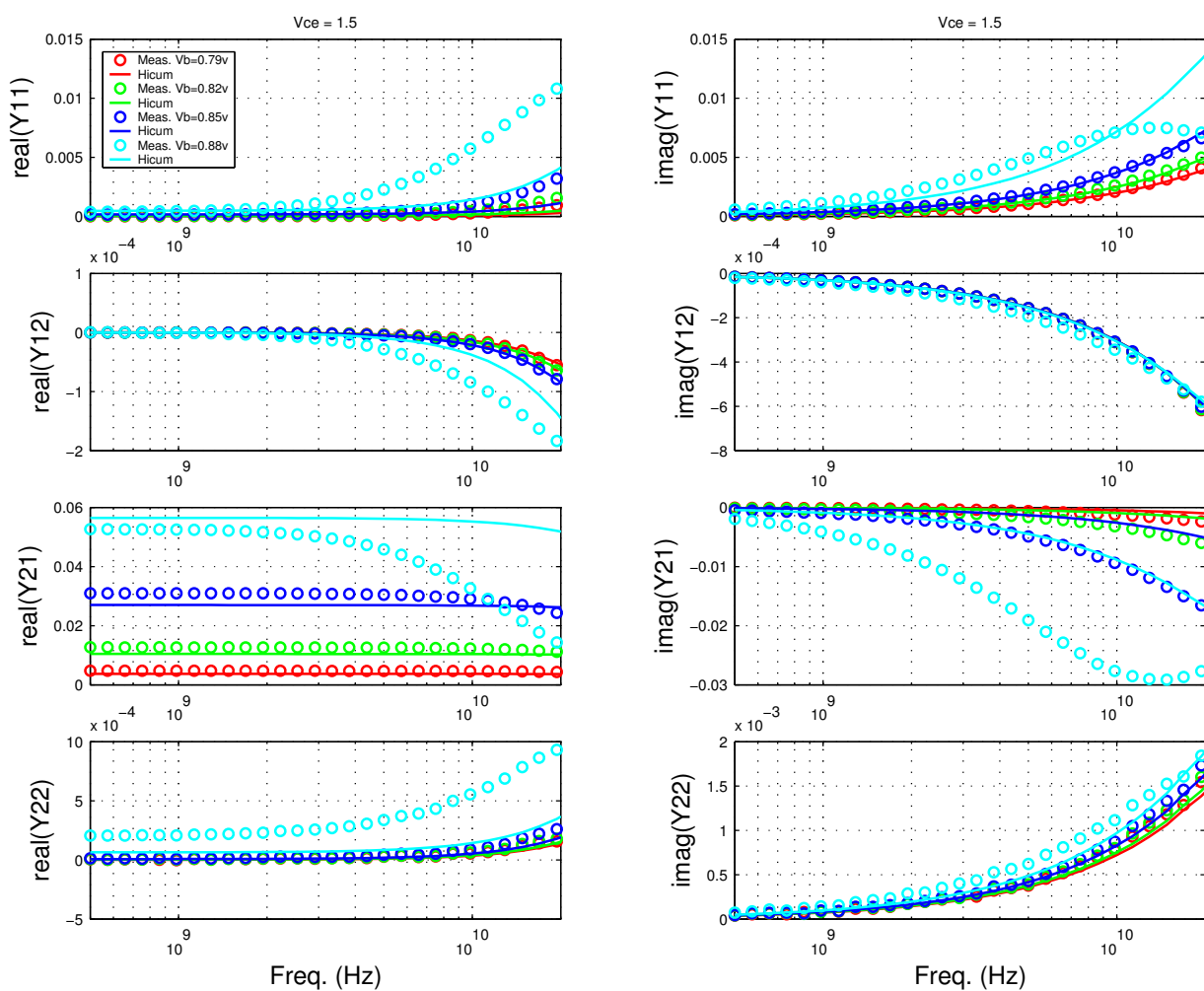


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FIGURE 5.86 Y-parameters vs. FREQ: MV 0.15x2.84x1_232



5.5 NPN Statistical and Corner Models

5.5.1 Statistical Model

A detailed description of the Backward Propagation of Variance (BPV) approach to statistical model generation is given in the MOSFET chapter. Only additional information exclusive to the NPN statistical models is given here. Unlike MOSFET models, the map between process and geometry parameters into model parameters is not well defined for NPN models. Mappings between process parameters, model parameters, and geometry parameters must be developed. The stand alone NPN models (Gummel-Poon, VBIC, Hicup, etc.) do not provide the physical correlation of the model parameters. Thus, a set of independent process parameters, rather than model parameters, are defined as the fundamental statistical variables in the simulator. Mappings for the process and geometry parameters into model parameters are developed based on device physics. A handful of process parameter variances are forward propagated in the BPV infrastructure based on expected variances at the process level such as Emitter-Poly CD variations. The remaining process parameter variances are directly BPV'd based on the variances in the ESPECs. A well conditioned system physically and mathematically results, guaranteeing precise simulation of the ESPEC variances and reasonable and consistent statistical simulation of non ESPEC quantities such as base resistance. The process parameters, the propagation technique, the affected model parameters, and target ESPECs for the BJT model are listed in Table 5.3. The statistically simulated ESPECs are listed in Table 5.5. Refer to the MOSFET chapter for statistical model usage guidelines.

TABLE 5.3 The Process Variables and the Affected Model Parameters in SGPM.

Process Parameters	BPV or FPV	Affected Model Parameters	Target ESPEC for BPV	Mismatch
Emitter Window CD	FPV	RE, RB, RBX, RC, CEOX, CJE, CJC, IS, ISE, IBEIS	NA	IC, BETA
Emitter Poly CD	FPV	CEOX, RBX	NA	
Base Ge doping concentration	BPV	C10	Vbe at mod. Ic	
Base Boron doping concentration	BPV	CBE, RBI, RBX, C10	Cbe	
Emitter Si/Poly interface property	BPV	IBEIS, RE	Peak Beta	IB
Emitter/Base Junction Leakage	BPV	IREIS	Beta @ low Vbe	IB @ low Vbe
Emitter doping concentration	BPV	RE, IBEIS	Ic @ Vbe=1.1v	
Substrate doping concentration	BPV	CJS	Ccs	
Base width	BPV	RBI, T0	Ft of LV & HV dev.	
Local Collector Implant (LV dev.)	BPV	CJC of LV dev.	CBC of LV dev.	
Local Collector Implant (MV dev.)	BPV	CJC of MV dev.	CBC of MV dev.	

5.5.2 Centering

Refer to section 2.6.1 for centering within the BPV framework. The NPN model is extracted from a golden die which measures very close to the nominal of the ESPECs. As a result, the model parameter variation needed to exactly align the model to the nominal ESPECs is small. The simulated NOM ESPECs are listed in Table 5.6.

5.5.3 Corner Models

The goal of the corner models are to capture the device electrical performance limits through appropriate variation of the process parameters. Slow and fast corners are provided. Details of the corner models are given in Table 5.4. All the NPN ESPEC limits can not be captured with 2 corners. The target ESPEC parameters for the corner models are I_C , β , and F_t . The C_{BE} and C_{CS} ESPECs are also aligned to the ESPECs in the corner model. C_{BC} variation in the corner models is reduced from the ESPEC limit in order to retain consistent and physical F_t prediction. The verification of the simulated corner ESPECs are listed in Table 5.5.

TABLE 5.4 Corner model specifications

	FAST	SLOW
Emitter resistance	Component 1 is higher due to lower I_b (high β); Component 2 is lower due to higher emitter doping. Net is ~15% lower	Component 1 is lower due to higher I_b (low β); Component 2 is higher due to lower emitter doping. Net is ~15% higher
Extrinsic base resistance	Component 1 is lower (Nom. - 1σ link dist.); Component 2 is higher due to lower base doping (low C_{be}). Net is ~10% higher	Component 1 is higher (Nom. + 1σ link dist.); Component 2 is lower due to higher base doping (high C_{be}). Net is ~10% lower
Intrinsic base resistance	Component 1 is higher due to shorter base width; Component 2 is higher due to lower base doping (low C_{be}). Net is 30% higher	Component 1 is lower due to longer base width; Component 2 is lower due to higher base doping (high C_{be}). Net is 30% lower
Base emitter junction cap.	90% of NOM case	110% of NOM case
Base collector junction cap.	Max. case of C_{bc}	Min. case of C_{bc}
Collector substrate junction cap.	Min. case of C_{cs}	Max. case of C_{cs}
Intrinsic collector resistance	~15% lower; aligned to higher collector doping (higher C_{bc})	~15% higher; aligned to lower collector doping (lower C_{bc})
Collector saturation current	Min. case of V_{be} for fixed and moderate I_c	Max. case of V_{be} for fixed and moderate I_c
Base current	Max. case of β (lower I_b)	Min. case of β (higher I_b)
Base width	Smaller; aligned to max. F_t E-spec.	Larger; aligned to min. F_t E-spec.

TABLE 5.5 E-spec. vs. Model (Long transistor - 0.15x10.16 μ m emitter with 122 configuration)

Device	Espec Name (unit)	Slow			Nom			Fast		
		Espec	Corner	Stat	Espec	Corner	Stat	Espec	Corner	Stat
Low Voltage NPN Hicum (ln122_hicum)	β ¹	100.00	118.30	93.00	300.00	300.20	312.00	600.00	577.60	531.00
	c_{bc} ² (fF)	17.30	17.45	17.70	18.30	18.30	18.30	19.30	19.55	18.90
	c_{be} (fF)	22.80	22.80	23.00	20.80	20.84	20.80	18.80	18.80	18.60
	c_{cs} (fF)	14.20	14.20	14.80	11.60	11.60	11.60	9.00	8.70	8.42
	f_t (GHz)	180.00	179.60	177.00	200.00	199.80	200.00	220.00	221.10	223.00
	i_c (uA)	NA	5.11	3.92	10.00	10.00	10.10	NA	15.80	16.30
	J_c^3 (Pk. Ft)	NA	10.24	8.60	10.7	10.71	10.89	NA	14.79	13.19
	f_{max} ⁴ (GHz)	NA	200.60	180.00	196.00	195.90	196.00	NA	188.10	212.00
	bv_{ceo} ⁵ (V)	2.30	2.29	2.37	1.90	1.99	1.99	1.50	1.43	1.61

TABLE 5.5 E-spec. vs. Model (Long transistor - 0.15x10.16μm emitter with 122 configuration)

Medium Volt- age NPN Hicup (mn122_hicup)	beta ¹	100.00	109.20	113.00	300.00	300.50	297.00	600.00	563.70	481.00
	cbc ² (fF)	9.00	9.50	9.02	9.90	9.89	9.85	10.80	10.30	10.70
	cbe (fF)	22.00	22.00	21.80	20.00	20.00	20.00	18.00	18.00	18.20
	ccs (fF)	17.50	17.56	17.60	14.60	14.65	14.50	11.70	11.74	11.40
	ft (GHz)	65.00	65.14	64.90	75.00	75.00	74.50	85.00	84.47	84.10
	ic (uA)	NA	4.07	4.39	10.00	10.00	9.88	NA	16.49	15.40
	Jc ³ (Pk. Ft)	NA	0.71	0.59	1.5	0.85	0.986	NA	0.98	1.14
	fmax ⁴ (GHz)	NA	168.10	157.00	200.00	171.10	171.00	NA	172.10	185.00
	bvceo ⁵ (V)	3.80	3.80	3.84	3.20	3.18	3.23	2.50	2.77	2.62

Notes:

1. Beta: The E-spec is asymmetrical across the NOM case. The statistical model prediction is +/- 3 sigma and is thus symmetrical across NOM.
2. C_{bc}: Variation in the corner models is reduced from the E-spec limit in order to retain consistent and physical Ft prediction.
3. J_c is the current density (mA/μm²) at peak Ft. Only nominal E-spec is specified. This parameter is not a BPV targeted E-spec for corner or statistical model extraction.
4. F_{max}: Only nominal E-spec. is specified. Corner and statistical model predictions are shown for all cases. This parameter is not a BPV targeted E-spec. for corner or statistical model extraction.
5. BV_{ceo}: Gummel-Poon model does not include breakdown effects. Hicup model predictions are shown. This parameter is not a BPV targeted E-spec. for corner or statistical model extraction.

5.6 NPN Mismatch Model

The mismatch model captures the local variation between identical devices. The collector current and the current gain (Beta) mismatch between two identical NPNs (~10μm apart) with identical V_{BE} and V_{CE} are characterized and captured in the mismatch model.

NPN mismatch is characterized in terms of percentage difference in Beta (β) and I_C. The I_C mismatch percentage is calculated using the following expression:

$$\Delta I_C = 100 \times \frac{I_{C1} - I_{C2}}{I_{C1}} \quad (\text{EQ 1})$$

The β mismatch is calculated using the following expression:

$$\Delta \beta = 100 \times \frac{\beta_1 - \beta_2}{\beta_1} \quad (\text{EQ 2})$$

The Ge concentration and EW CD mismatch sigmas are used to fit the I_C mismatch. The emitter surface recombination velocity sigma fits the additional mismatch seen in the β measurements. In operational regions where I_C and β are not affected by series resistance, low or high bias effects, NPN mismatch can be adequately represented with the aforementioned process parameters, combined with an inverse square root dependence on active emitter area.

Figure 5.87 through Figure 5.88 show the I_C and β mismatch for the SBC18 200GHz NPNs. Discrepancies in low current I_C mismatch are due to leakage current mismatch and are not modelled.

FIGURE 5.87 Measured and simulated I_c and Beta mismatch plots of high-speed NPNs (In122_hicum)

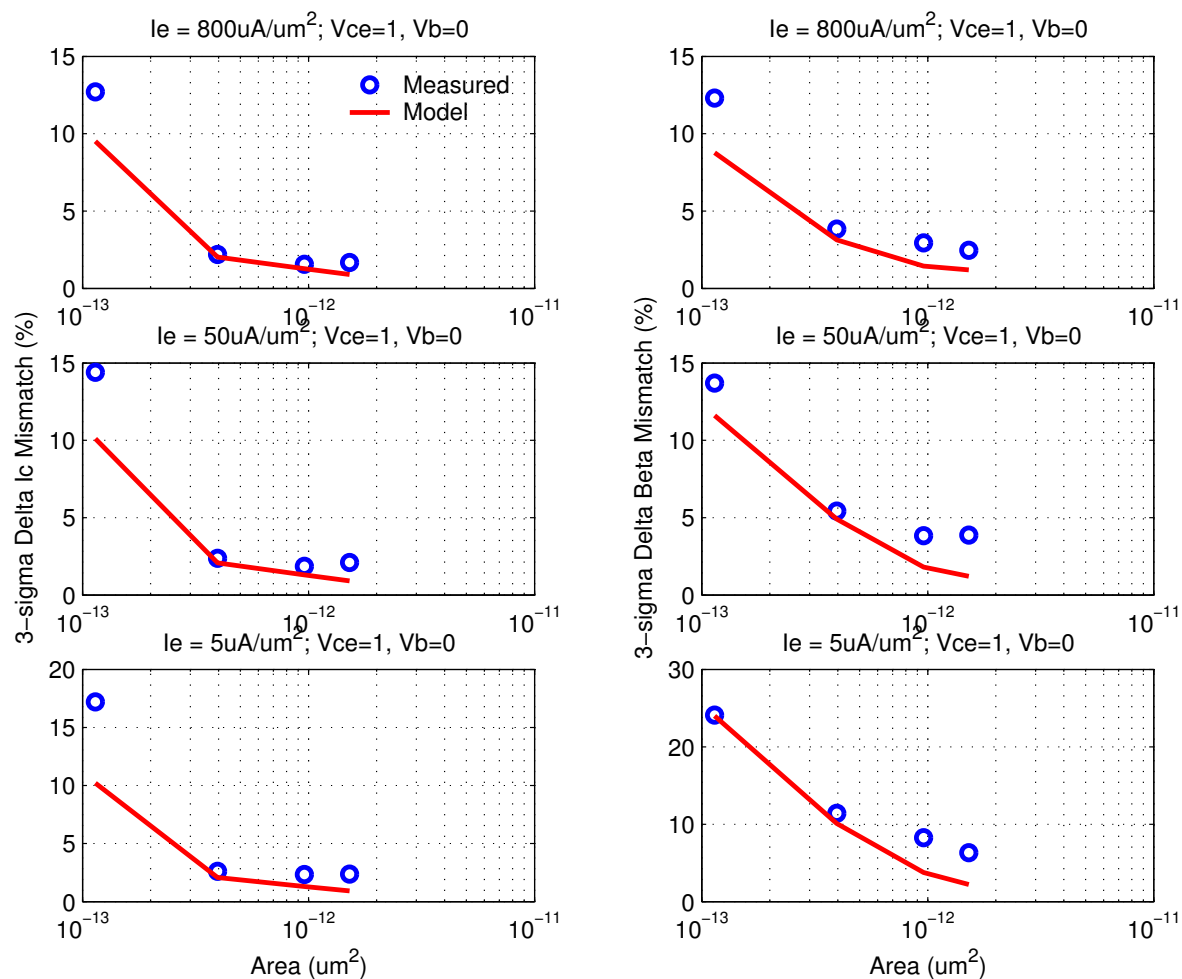
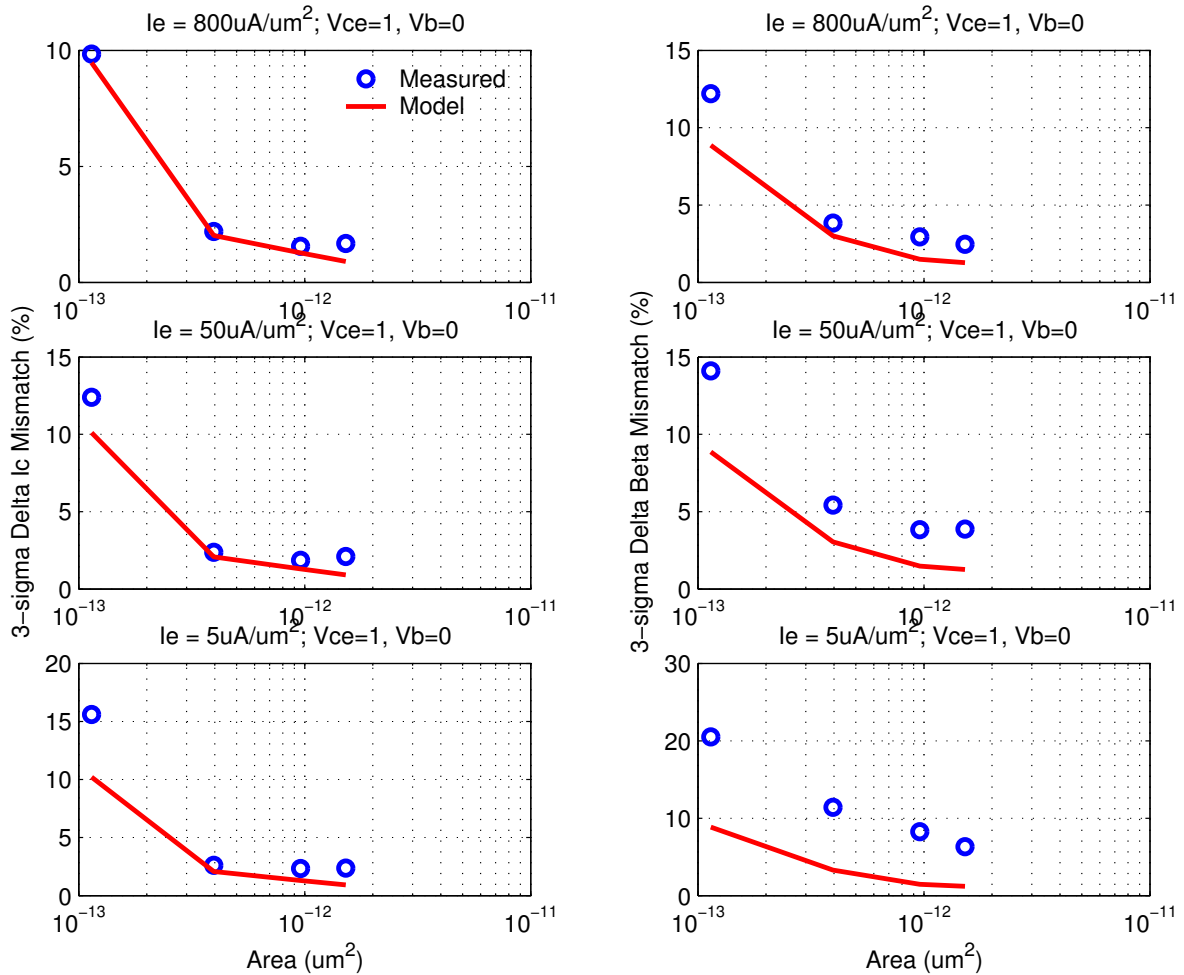


FIGURE 5.88 Measured and simulated I_C and Beta mismatch plots of Standard NPN (mn122_hicum)

5.7 Released Model Quality Assurance (QA)

A rigorous QA procedure is executed before any new model release. The geometry dependence of 9 key device parameters is examined for any non-physical behavior for all 3 cases: Nominal, Fast, and Slow. These parameters are listed in Table 5.6.

TABLE 5.6 NPN electrical parameters list examined as part of model release QA

Parameter	Description
BETA	Current gain
I_C	I_C at $V_{be}=0.7\text{V}$
F_t	Unity gain cut-off frequency
F_{max}	Unity power gain cut off frequency

TABLE 5.6 NPN electrical parameters list examined as part of model release QA

Parameter	Description
C_{BE}	Base-Emitter capacitance
C_{BC}	Base-Collector capacitance
C_{CS}	Collector-Substrate capacitance
R_E	Emitter Resistance
R_B	Base Resistance

Figures 5.89 through 5.90 illustrate the emitter length dependence of these 9 parameters.

FIGURE 5.89 QA Plots: LV 0.15x10.0_122

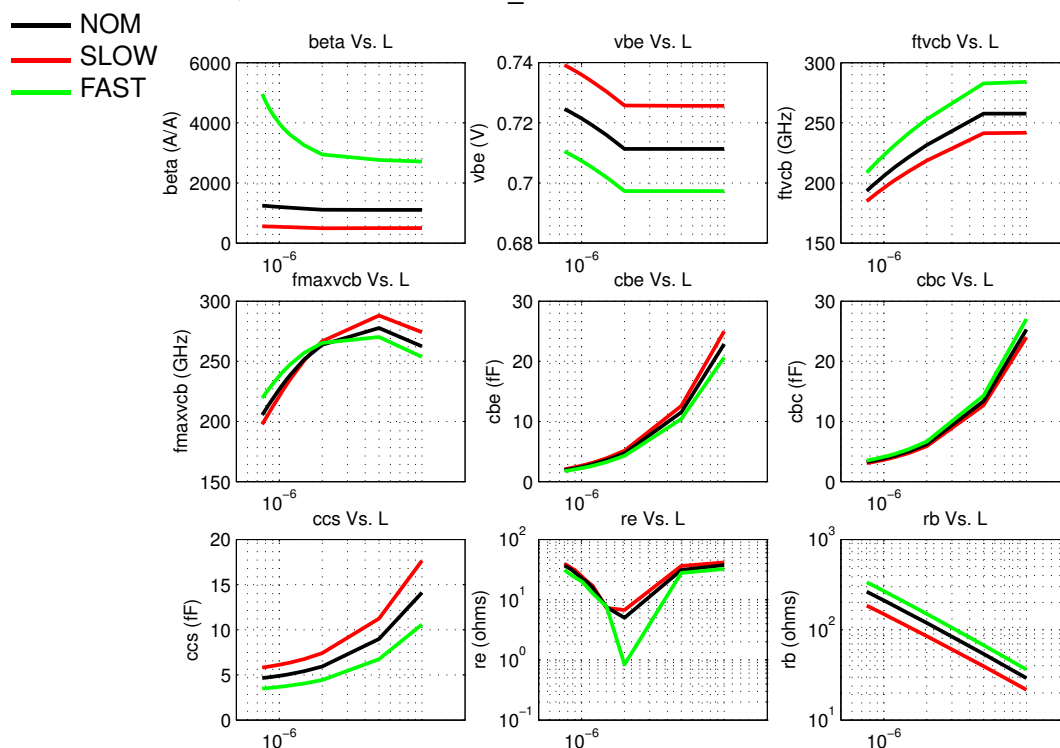
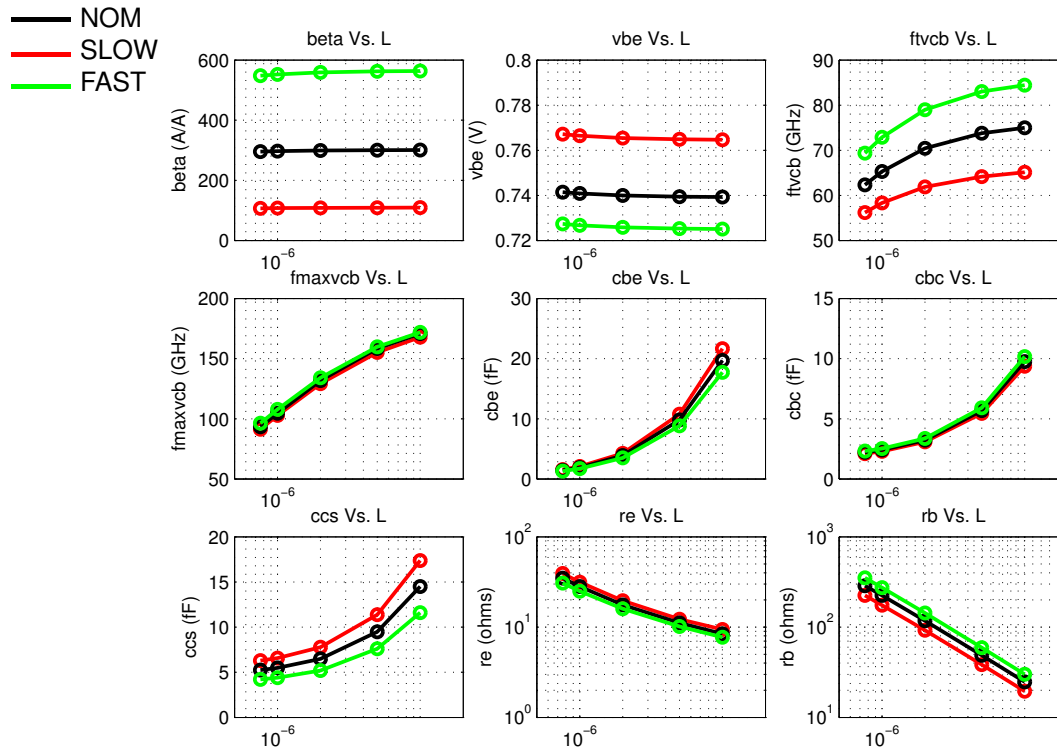


FIGURE 5.90 QA Plots: MV 0.15x10.0_122

5.8 Model Update History

TABLE 5.7 NPN model specific updates in model release version SBC18 v6.0b, SBC13 2.0

v6.0b update	Devices	Reason	Impact on user
Updated low-voltage (lnxxx) and medium-voltage (mnxxx) hicum models based on recent silicon	All	New models extracted from extensive set of test structures from more mature process	Improved accuracy
NOM Beta increased from 200 to 300	All	Align to recent silicon and updated E-spec.	Increased current gain
Peak Ft of the medium voltage npn increased from 70 to 85 GHz	MV	Align to recent silicon and updated E-spec.	Higher cut-off frequency for current gain
BVceo of medium voltage npn lowered to new E-spec (3v)	MV	Align to recent silicon and updated E-spec.	Lower breakdown voltage

TABLE 5.8 NPN model specific updates in model release version SBC18 v6.2

v6.2 update	Devices	Reason	Impact on user
Updated low-voltage (lnxxx) hicum models based on recent silicon	LV	Models re-extracted to better reflect current process.	Improved model to hardware accuracy. Increased Fmax from 180 to 196 GHz.

TABLE 5.9 NPN model specific updates in model release version SBC18 v6.3

v6.3 update	Devices	Reason	Impact on user
Aligned NPN models to new E-specs.	High-speed and medium voltage NPNs	Align to Fab data and specs	Major change is NOM IC at $V_{be}=0.7V$ reduced from 10uA to ~7.5uA
Added mismatch model for SiGe200 NPNs	High-speed and medium voltage NPNs	New capability	Ability to include monte-carlo mismatch in simulations
Added thermal resistance flag in the model selection dialog-box	High-speed and medium voltage NPNs	New capability	Ability to include self-heating in simulations

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6.0 SBC18H3 Bipolar Model

6.1 Device Description

The SBC18H3 process offers 2 NPN device types, low and medium voltage, differentiated by BV_{CEO} and F_t targets listed in Table 6.1. These devices are exclusive to SBC18H3 and cannot coexist with the npn devices described in Chapter 4.0 and Chapter 5.0. A cross section of a high-speed NPN device is shown in Figure 6.1. Figure 6.2 shows the layout of a 1 emitter, 2 base, 1 collector configuration. Layout configurations are further described in Section 6.2.

TABLE 6.1 SBC18H3 NPN Specification by BV_{CEO} and F_t

NPN	BV_{CEO} (V)	F_t (GHz)	F_{max} (GHz)	Design Kit Name	Model Name
low voltage	1.6	240	260	nnp	ln[1,2][1,2,3][1,2]_hicum
medium voltage	~3.2	56	145	nnp	mn[1,2][1,2,3][1,2]_hicum

FIGURE 6.1 Cross Section of NPN

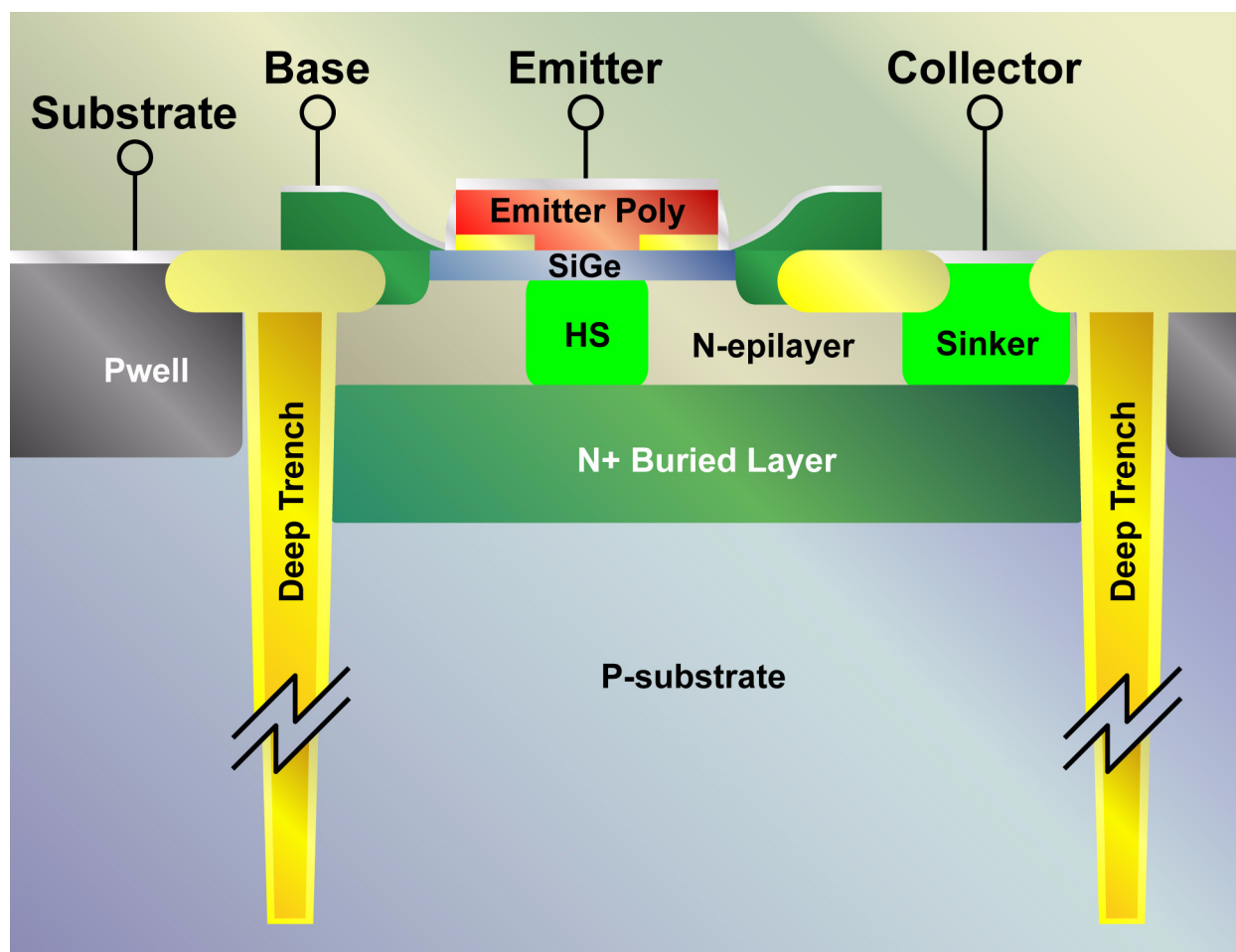
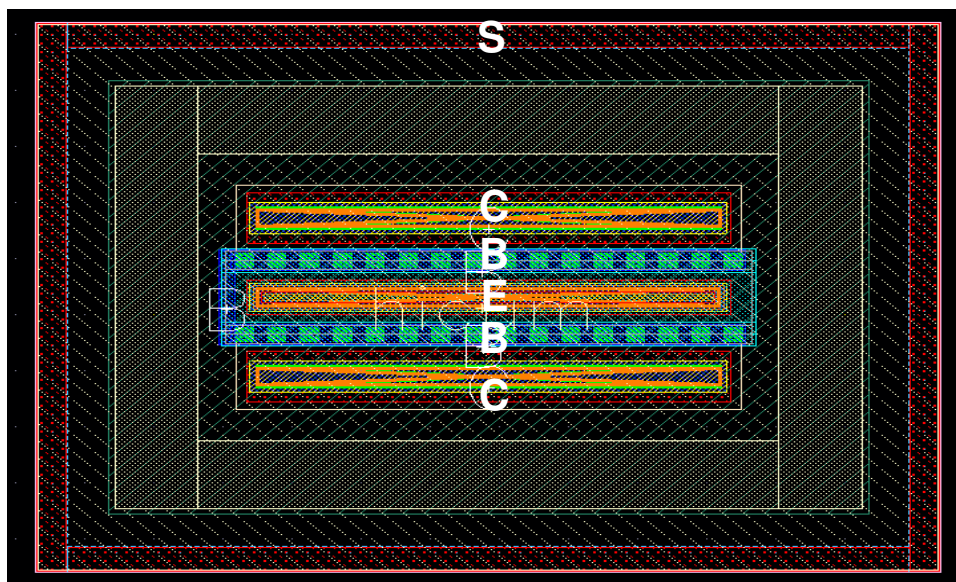


FIGURE 6.2 Layout of NPN: 1 Emitter, 2 Base, and 2 Collector configuration



6.2 Available NPN Configurations and Usage Guidelines

Table 6.2 provides a detailed description of the NPN configurations and parameter ranges.

Emitters Lengths: Scalable, see Table 6.2 for length range.

Emitters Widths: A single emitter width ($0.13\mu\text{m}$) is offered in the sbc18h3 technology.

Multiple device instances vs. multiple emitter fingers: use of multiple emitter fingers instead of multiple device instances generally results in more efficient footprint and lower parasitic capacitance. The trade-off is collector resistance.

TABLE 6.2 SBC18H3 NPN Configurations

Configuration	Device Type: l=low voltage m=medium voltage	Emitter Width n= $0.13\mu\text{m}$	Emitter Length (μm)	No. of Emitters	No. of Bases	No. of Collectors
121	l, m	n	0.76-10.16	1	2	1
122	l, m	n	0.76-10.16	1	2	2
232	l, m	n	2.84-10.16	2	3	2

6.3 Model Description

6.3.1 L-Scalable Model

The emitter length can be varied within the grid spacing and within the boundaries listed in Table 6.2. Separate models are extracted for the various combinations of emitter width and finger configuration described in Table 6.2.

6.3.2 HICUM Model

The HICUM model was introduced to overcome the shortcomings of the SGPM (Standard Gummel-Poon Model). The name of HICUM is derived from “High Current Model”. HICUM was initially developed with special emphasis on the modeling of the high current region, very important for many high-speed applications. Compared with SGPM, HICUM is based on an extended and generalized integral charge control relationship, and approaches the transistor dynamic behaviors in a more physical way. For more detailed information about HICUM, please refer to HICUM official web page (http://www.iee.et.tu-dresden.de/iee/eb/hic_new/hic_start.html).

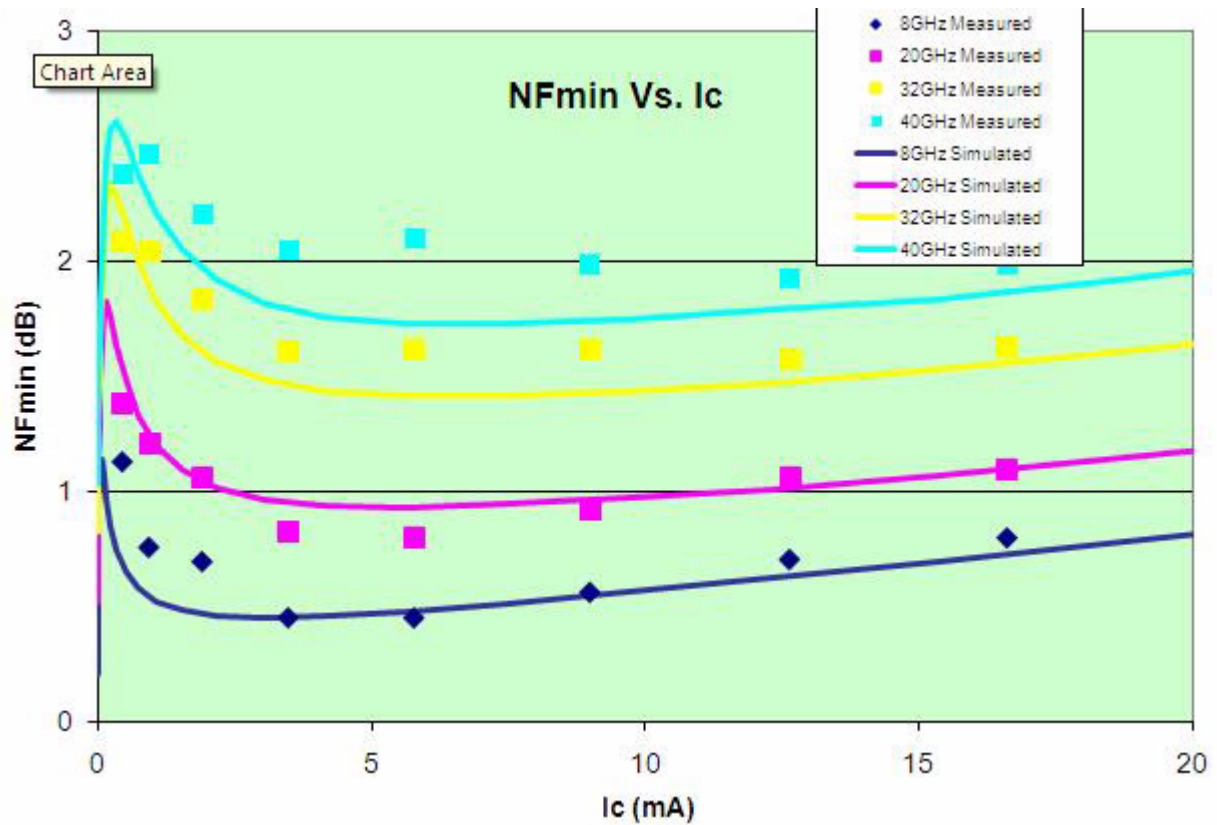
6.4 Model Extraction and Verification

Scalable NPN models are extracted based on DC, CV, and RF measurements over a wide geometry and bias range.

Figures 6.4 through 6.33 display the characterization plots for the low voltage NPN. Figures 6.34 through 6.51 display the characterization plots for the medium voltage NPN. In some instances, multiple devices in parallel are characterized for smaller emitter lengths to reduce de-embedding errors. The device type and size are encoded in the figure caption as “Voltage LxWxM_Configuration.” Thus a MV 0.13x1x10_122 captions refers to a medium voltage NPN with a width (W) of 0.13 μ m, a length (L) of 1 μ m, with 10 devices in parallel (M) and a 122 emitter/base/collector finger configuration.

Due to high Ge concentration needed for the High-speed NPN, the medium voltage device exhibits an unusual base current. This can be seen in the Gummel-plots at $V_{be} > \sim 0.8V$, and the I_C - V_{ce} curves shown below. The Hicup compact model cannot account for these fully, and as such model accuracy is reduced. It is recommended that the medium-voltage NPN model be used with caution in applications where a high-degree of accuracy is required.

6.4.1 Low Voltage Verification Plots

FIGURE 6.3 Minimum Noise Figure for In122 device with emitter length=20 μ m

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FIGURE 6.4 Gummel Plot LV 0.13x3x1_122

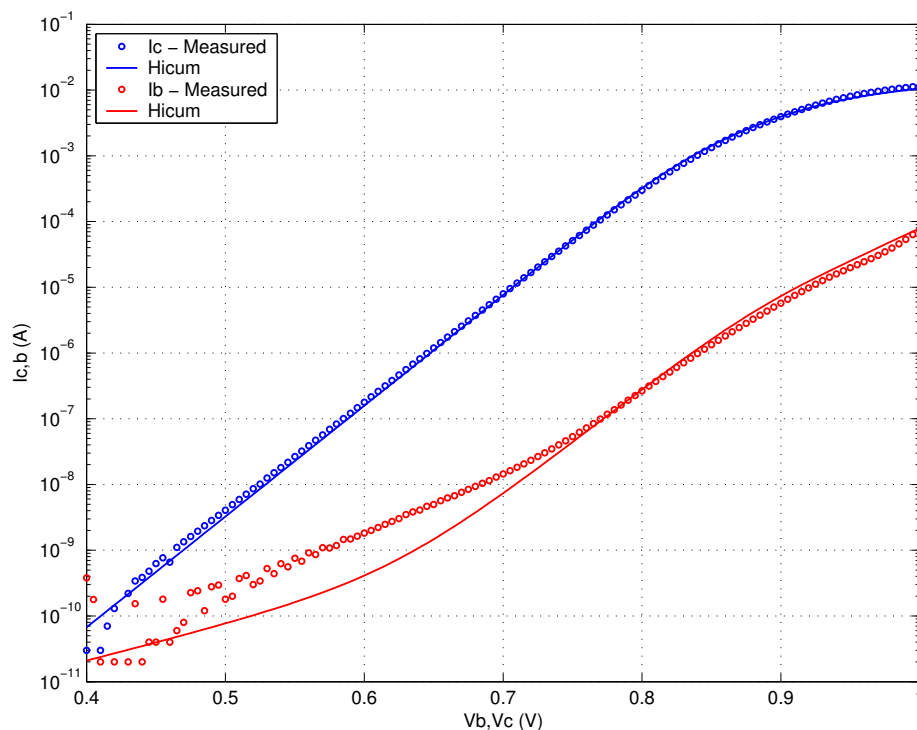


FIGURE 6.5 Beta vs. I_c : LV 0.13x3x1_122

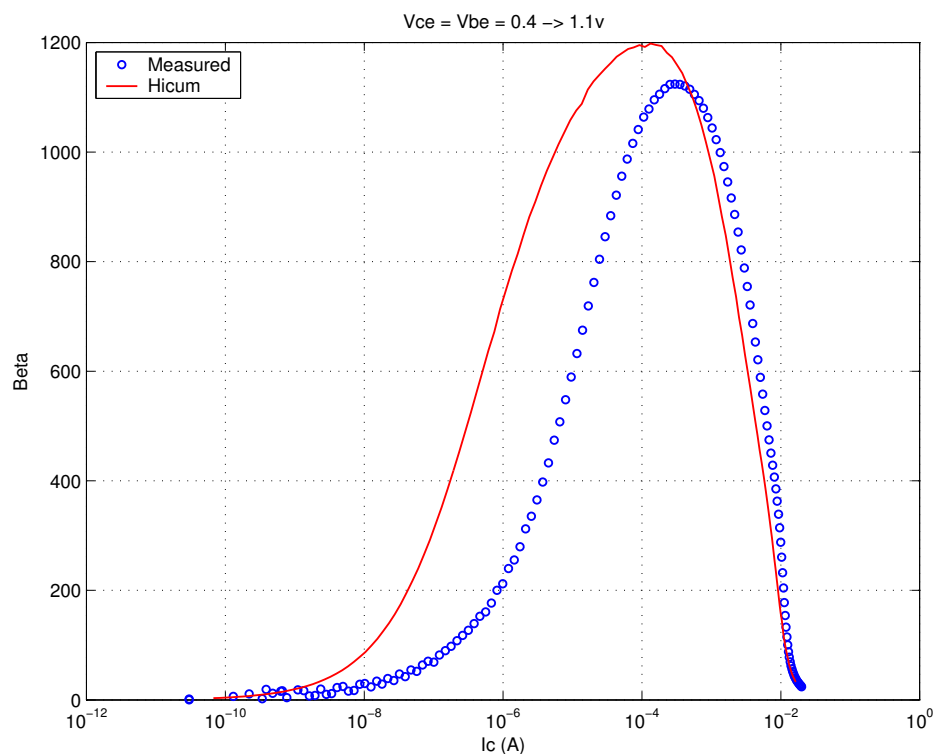


FIGURE 6.6 IC vs. VCE at constant IB: LV 0.13x3x1_122

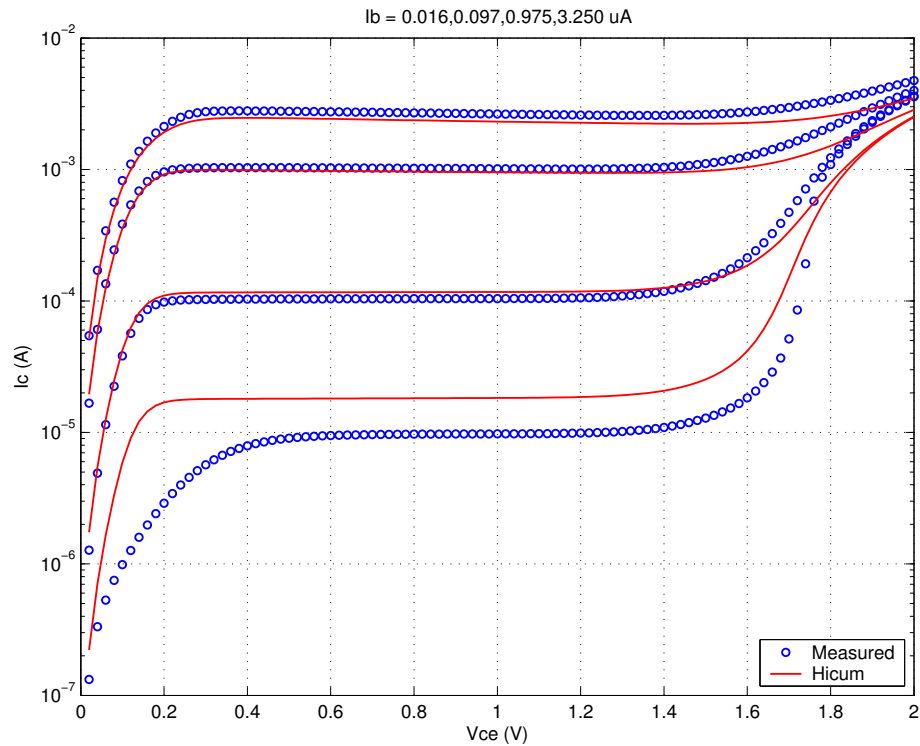


FIGURE 6.7 FT vs. IC: LV 0.13x3x1_122

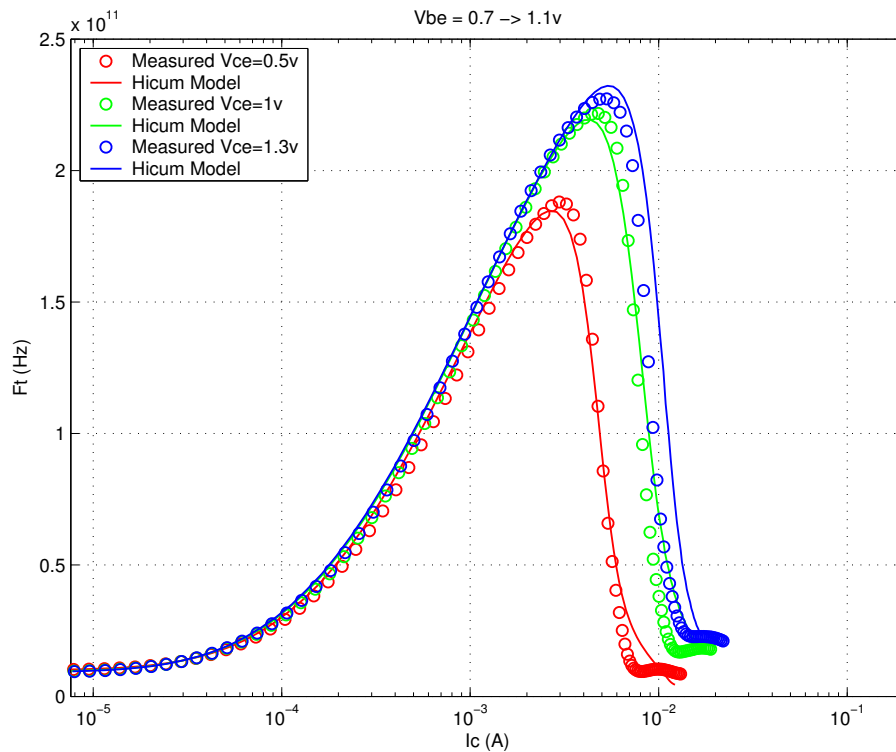
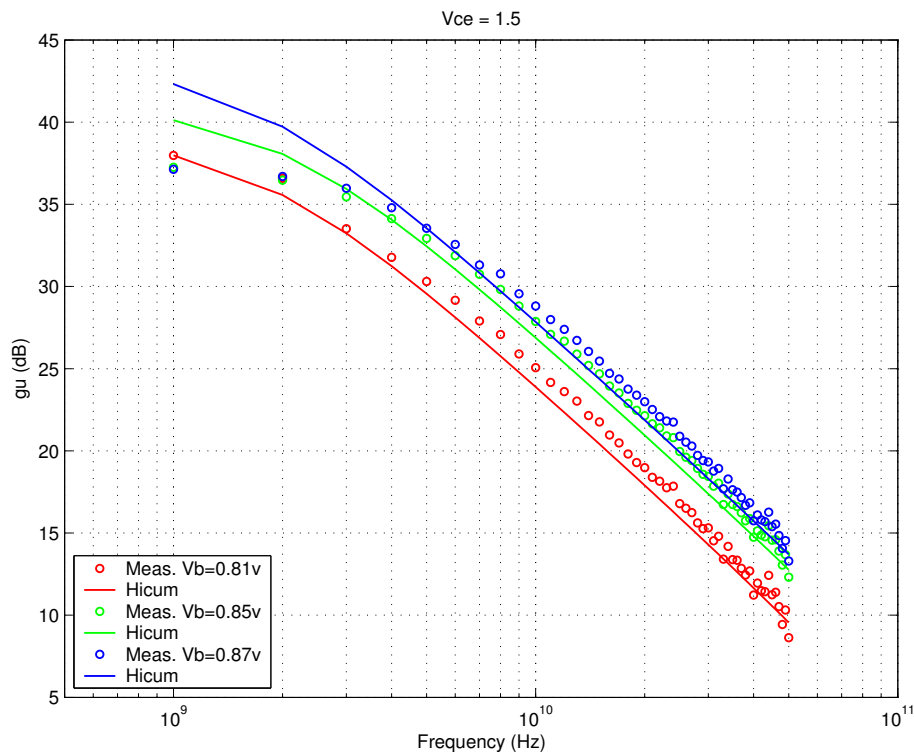


FIGURE 6.8 Power Gain vs. Freq: LV 0.13x3x1_122



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FIGURE 6.9 Y-parameters vs. FREQ: LV 0.13x3x1_122

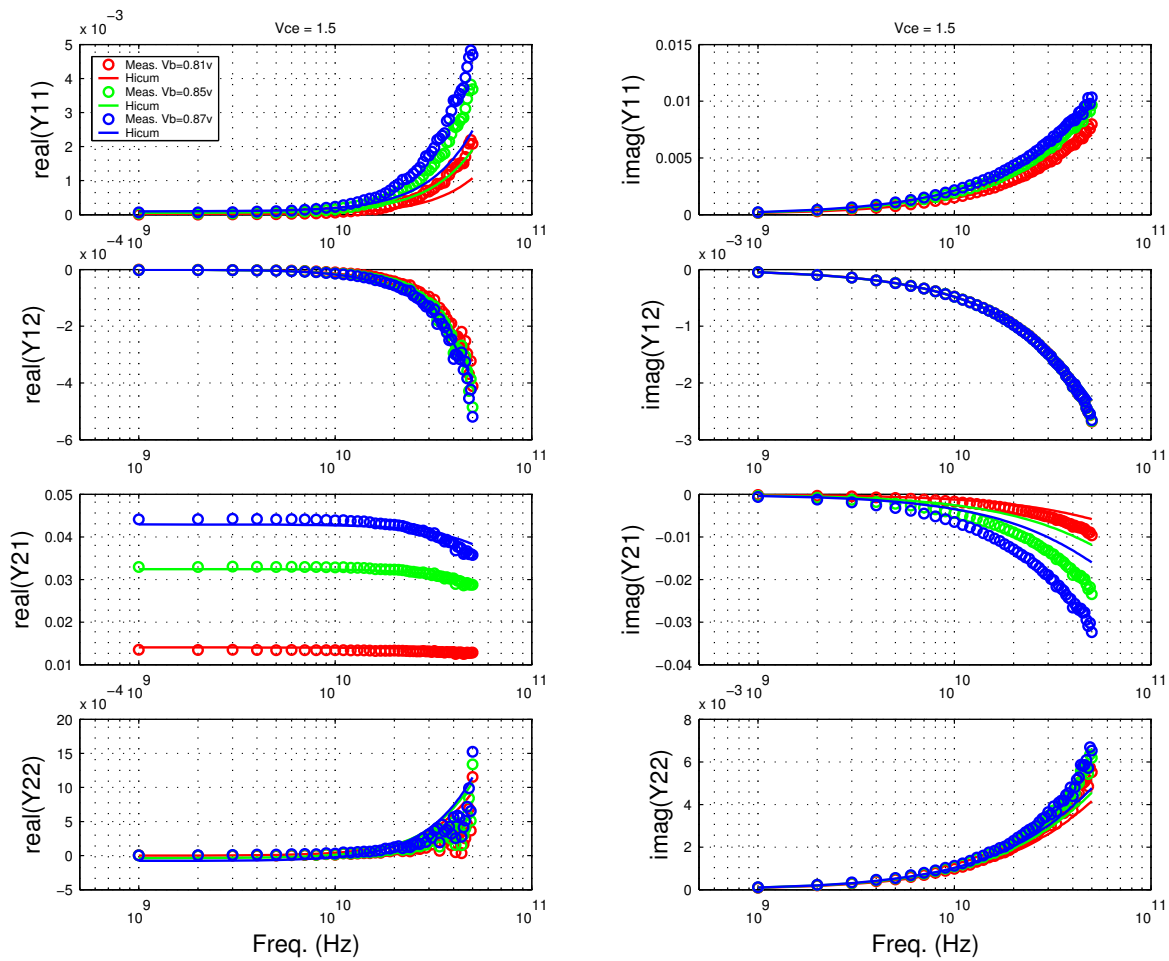


FIGURE 6.10 Gummel Plot LV 0.13x10x1_122

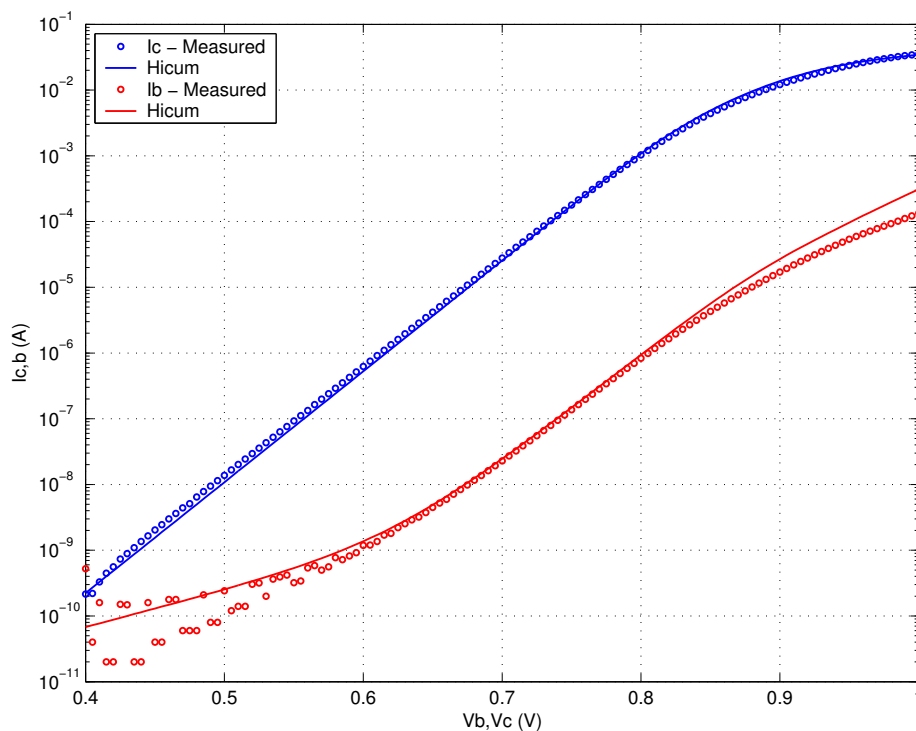


FIGURE 6.11 Beta vs. I_c : LV 0.13x10x1_122

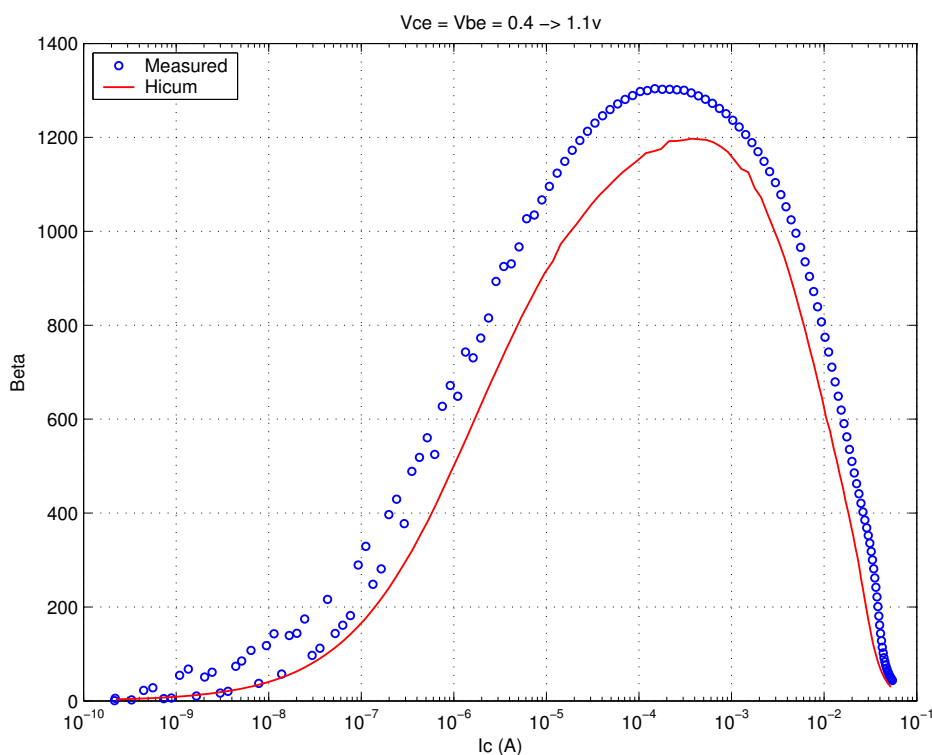


FIGURE 6.12 IC vs. VCE at constant IB: LV 0.13x10x1_122

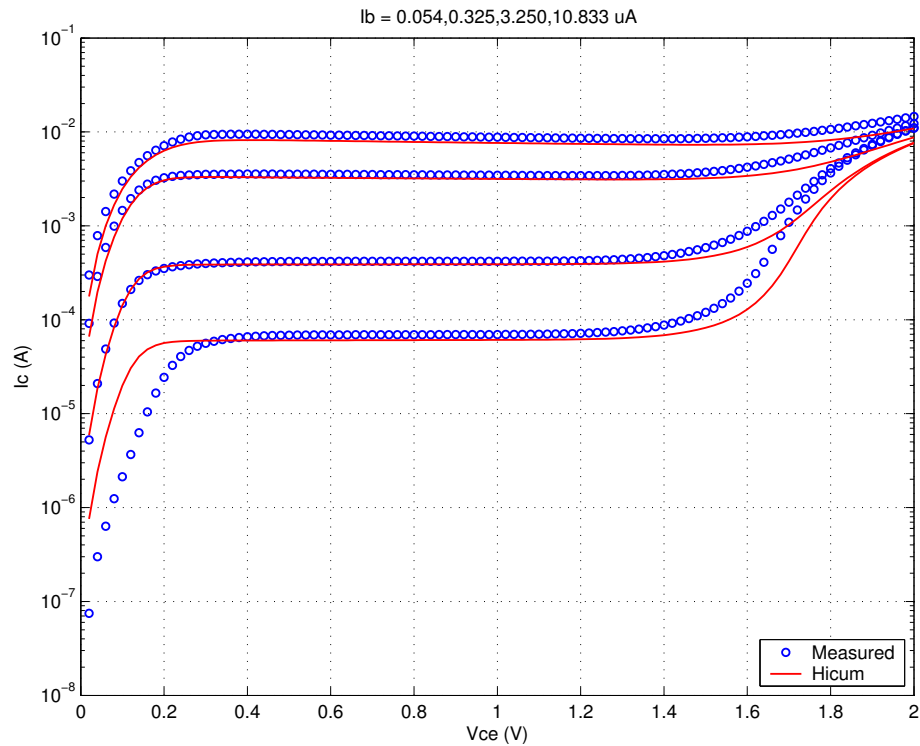


FIGURE 6.13 FT vs. IC: LV 0.13x10x1_122

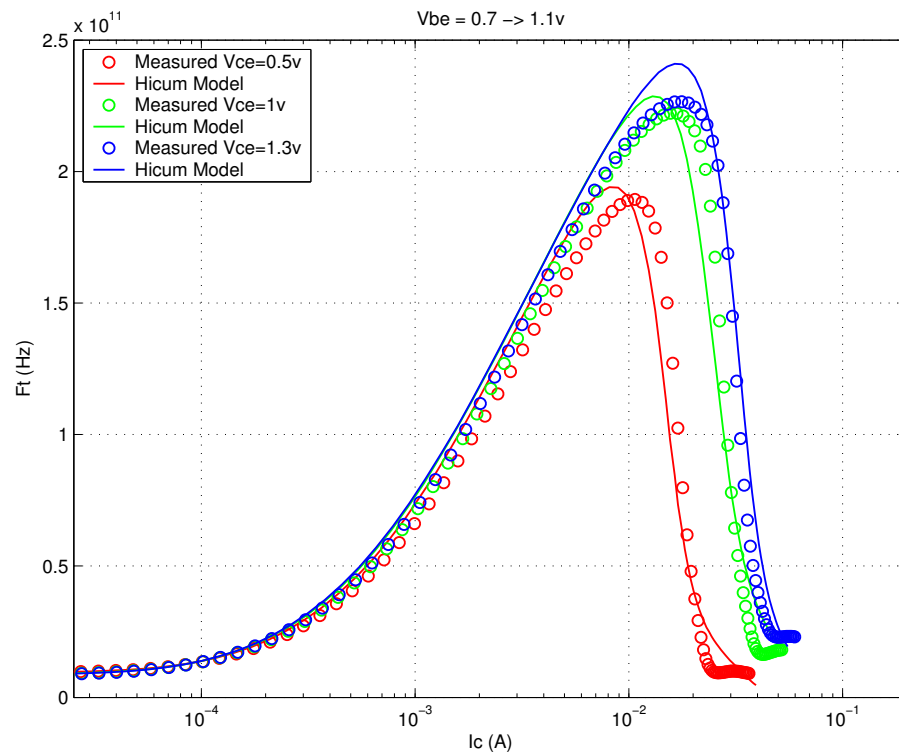
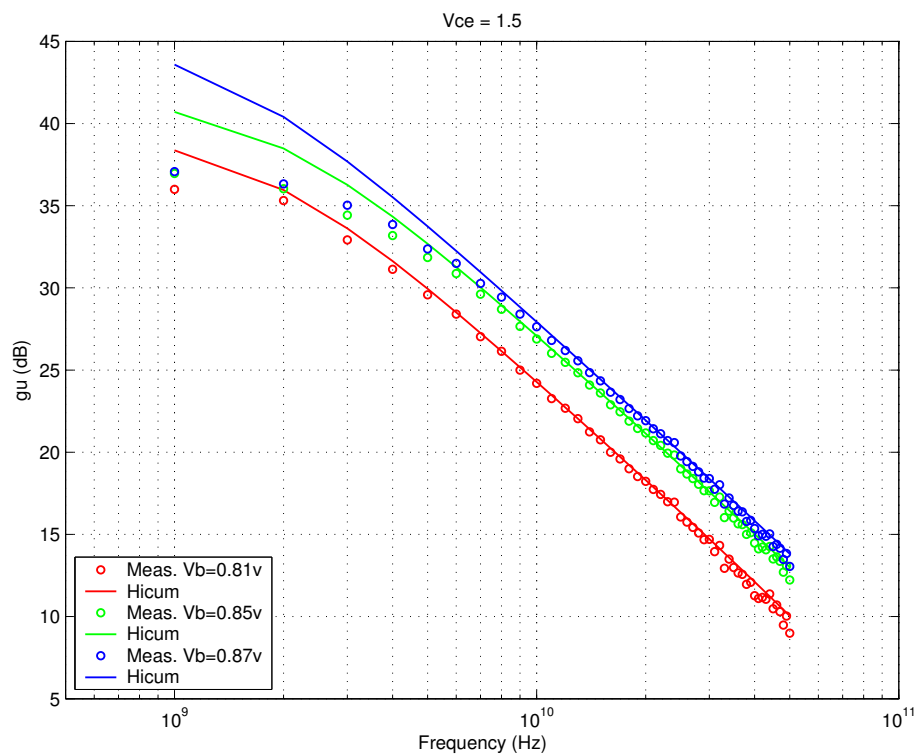


FIGURE 6.14 Power Gain vs. Freq: LV 0.13x10x1_122



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FIGURE 6.15 Y-parameters vs. FREQ: LV 0.13x10x1_122

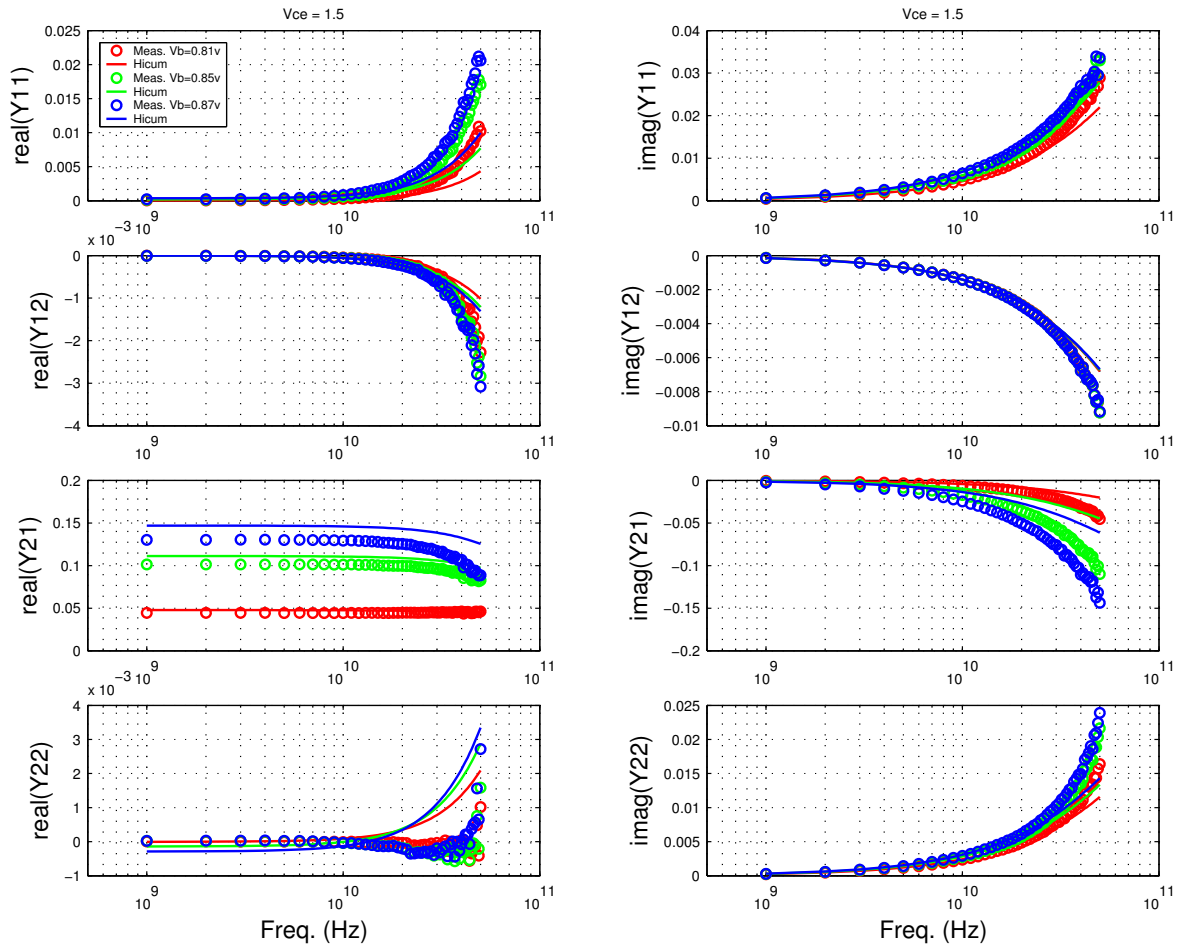


FIGURE 6.16 Gummel Plot: LV 0.13x1.5x1_122

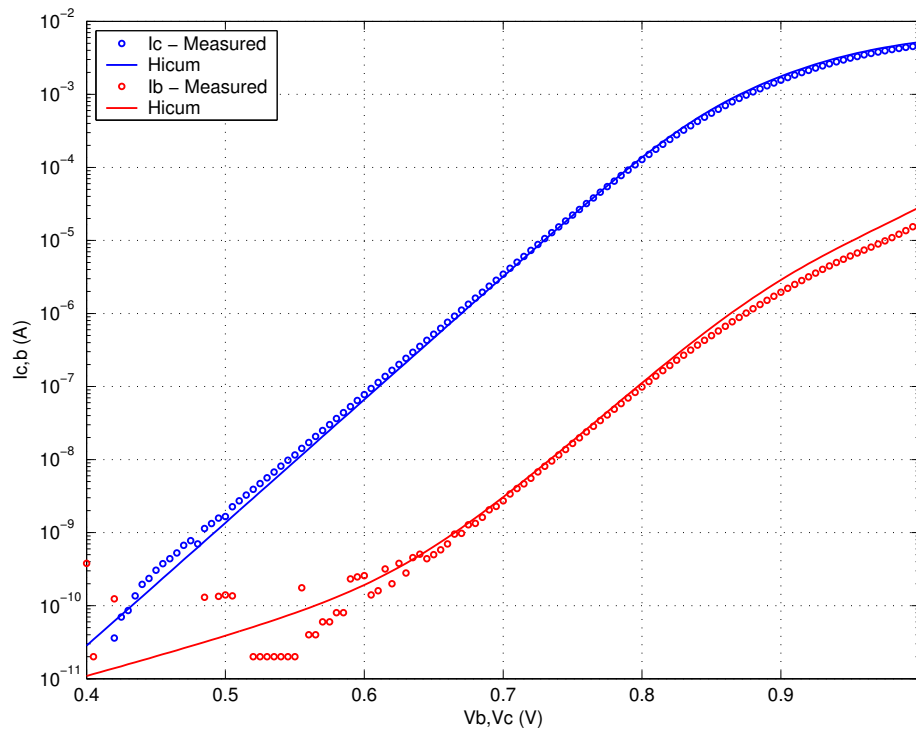


FIGURE 6.17 Beta vs. I_c : LV 0.13x1.5x1_122

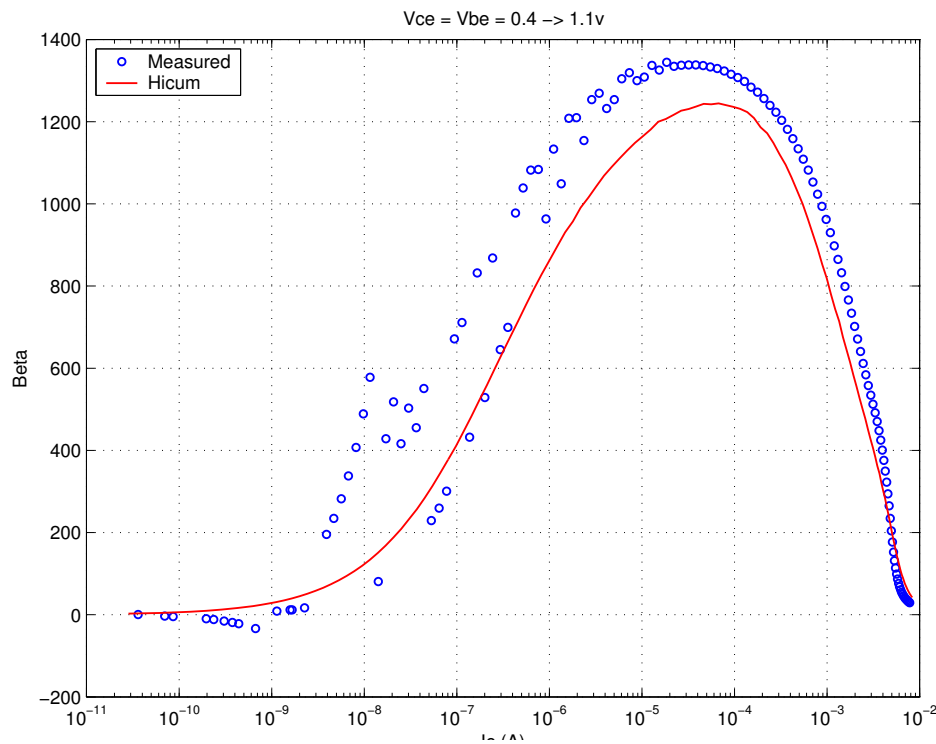


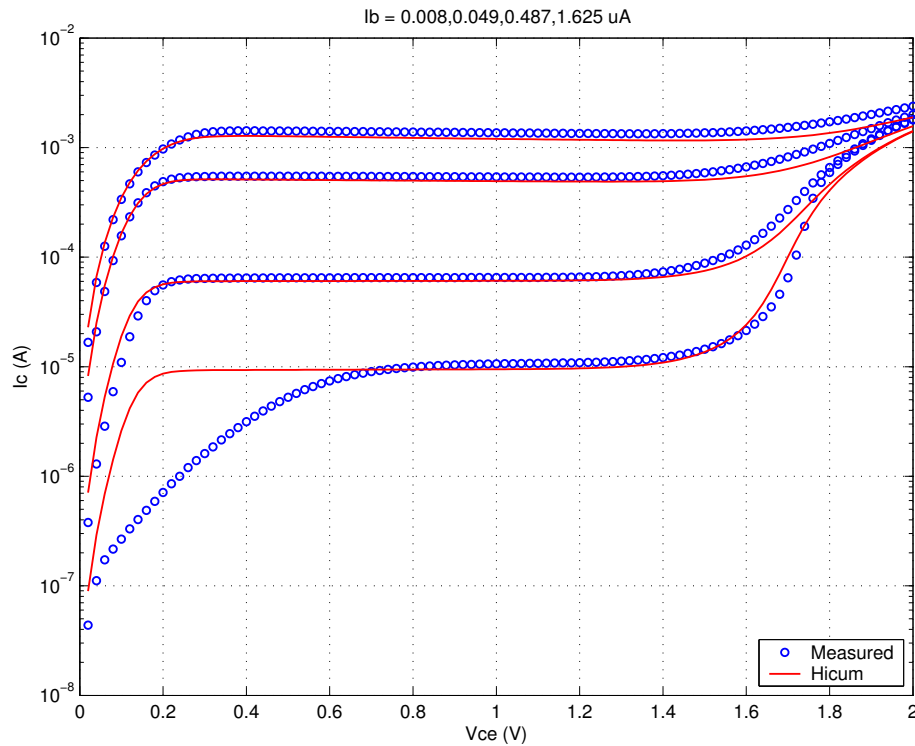
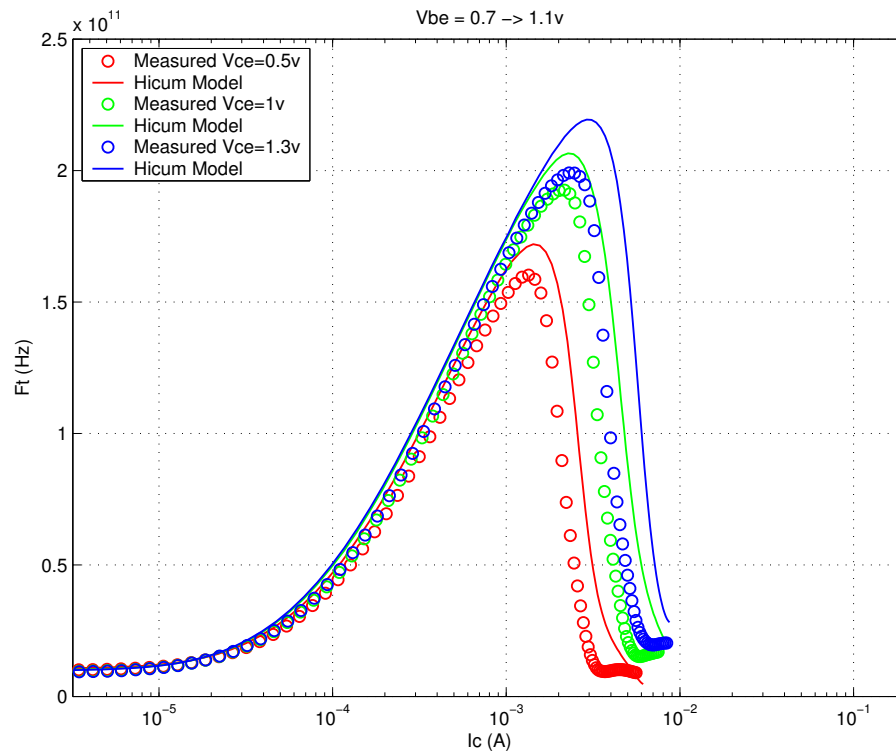
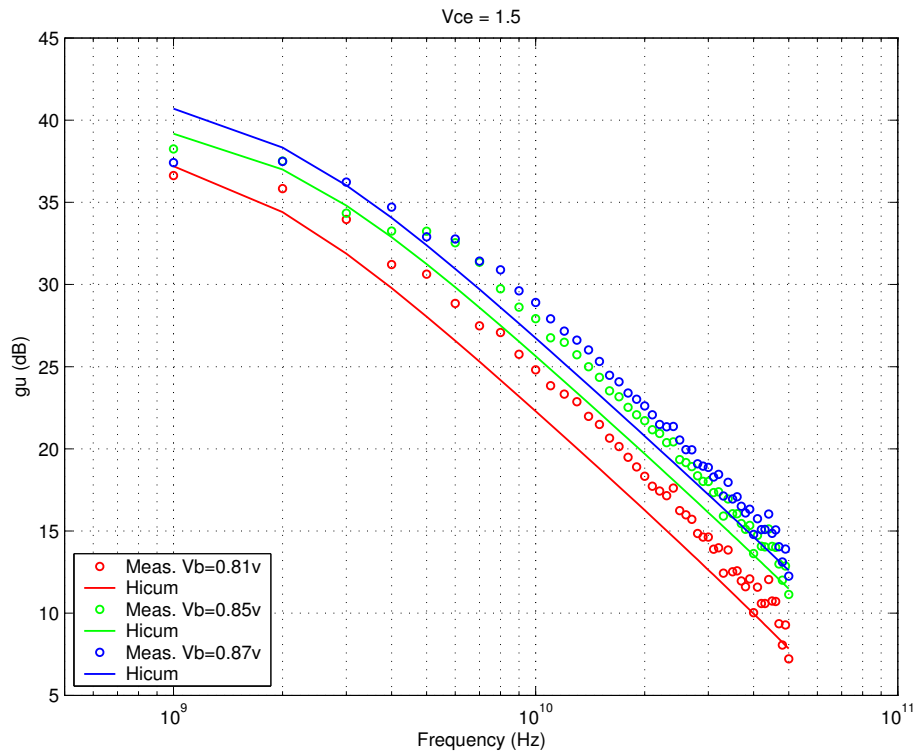
FIGURE 6.18 I_C vs. V_{CE} at constant I_B : LV 0.13x1.5x1_122FIGURE 6.19 F_T vs. I_C : LV 0.13x1.5x1_122

FIGURE 6.20 Power Gain vs. Freq: LV 0.13x1.5x1_122



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FIGURE 6.21 Y-parameters vs. FREQ: LV 0.13x2.84x1_122

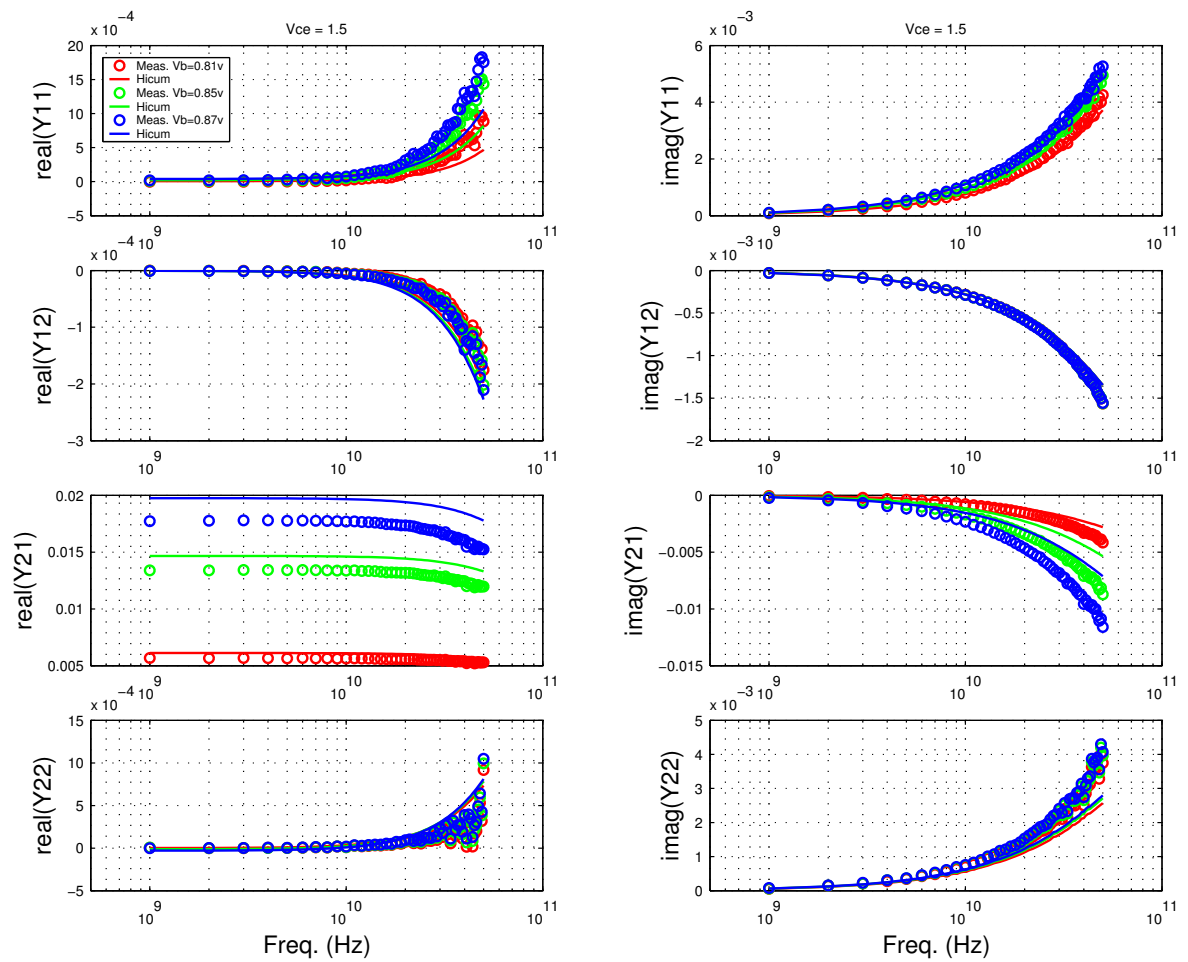


FIGURE 6.22 Gummel Plot LV 0.13x3x1_121

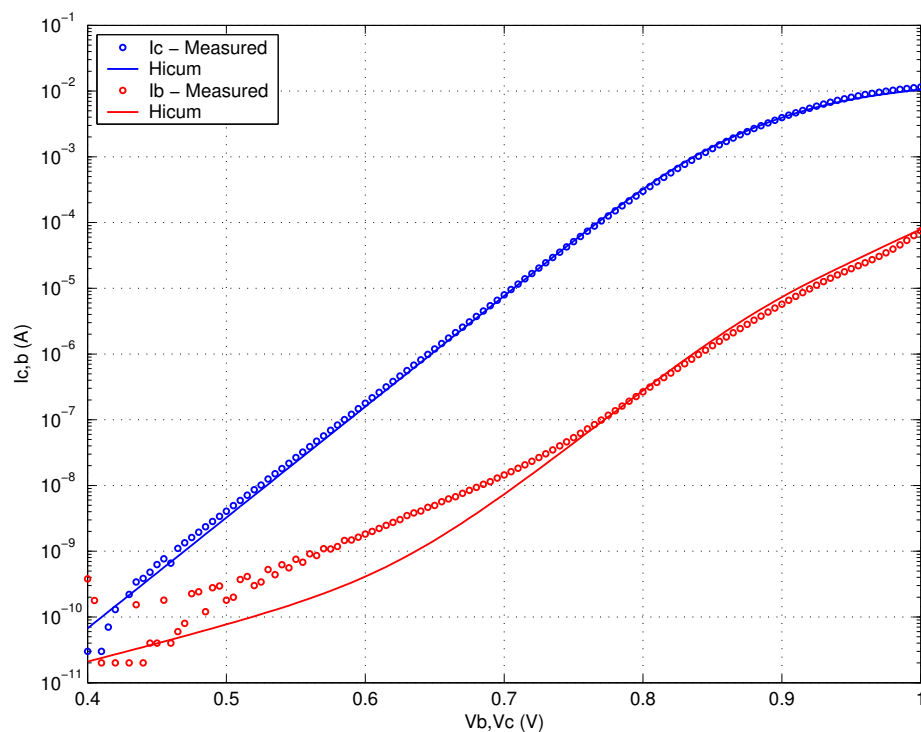


FIGURE 6.23 Beta vs. I_c : LV 0.13x3x1_121

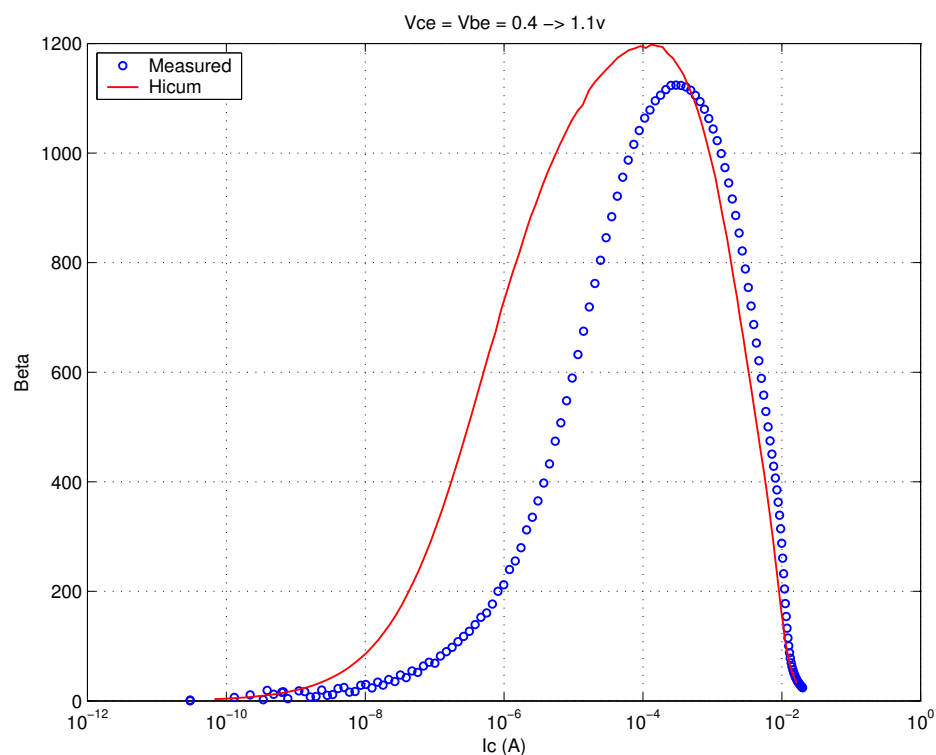


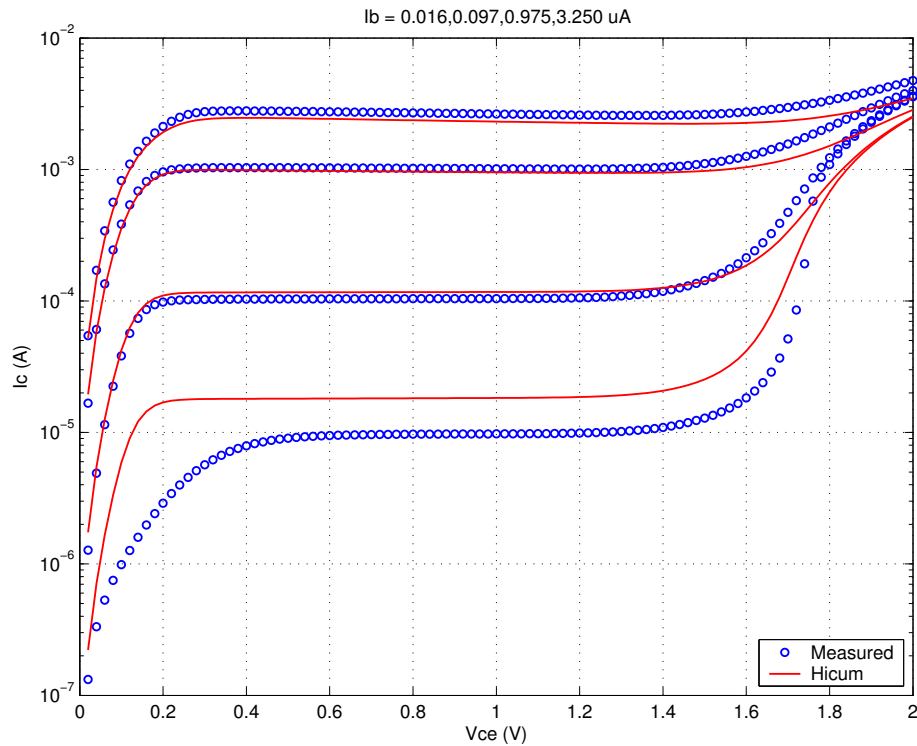
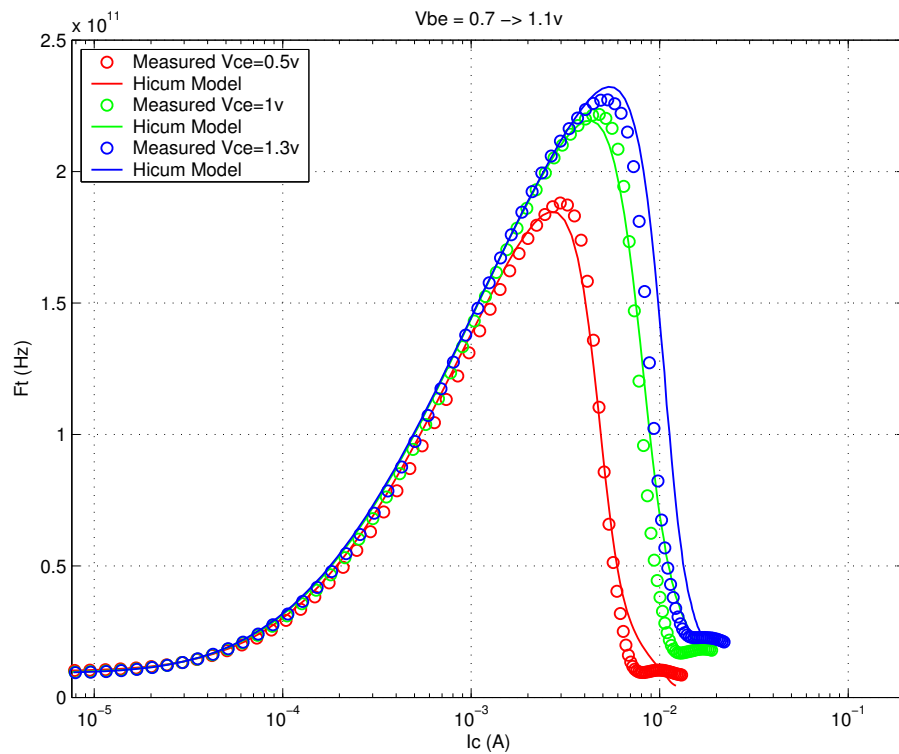
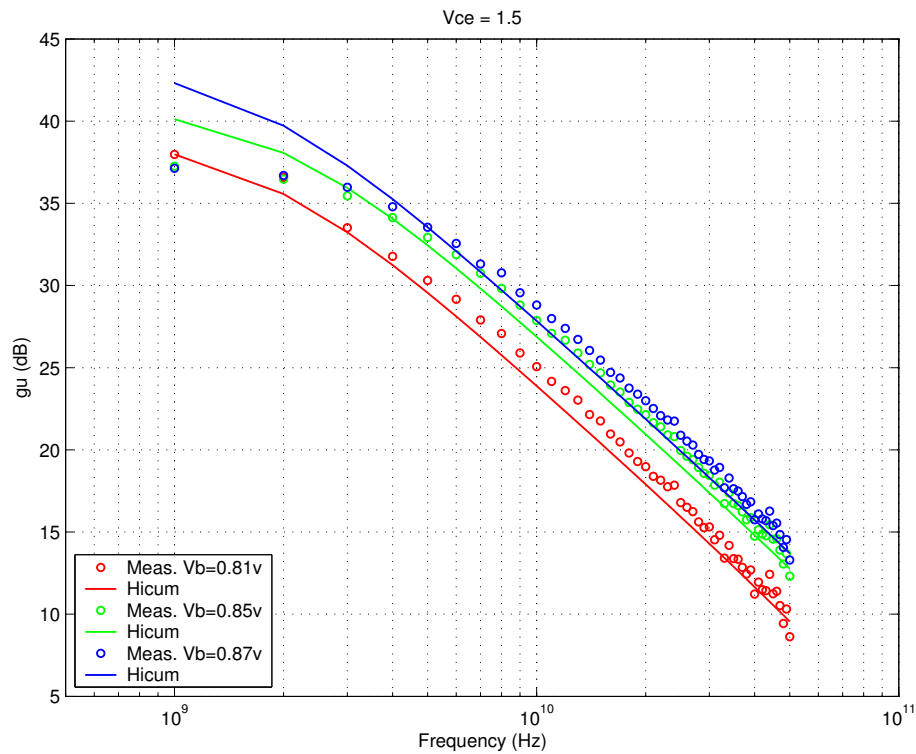
FIGURE 6.24 I_C vs. V_{CE} at constant I_B : LV 0.13x3x1_121FIGURE 6.25 F_T vs. I_C : LV 0.13x3x1_121

FIGURE 6.26 Power Gain vs. Freq: LV 0.13x3x1_121



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FIGURE 6.27 Y-parameters vs. FREQ: LV 0.13x3x1_121

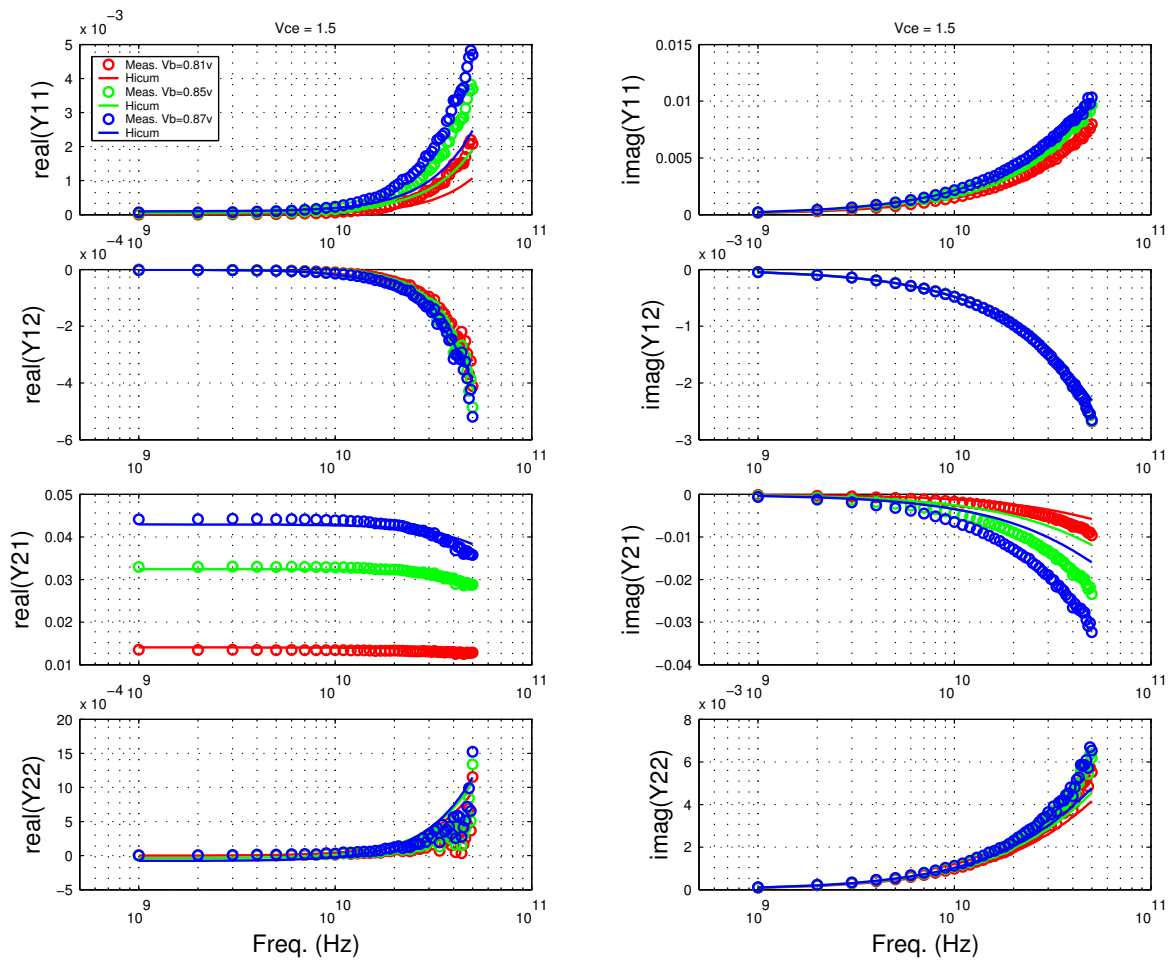


FIGURE 6.28 Gummel Plot LV 0.13x3x1_232

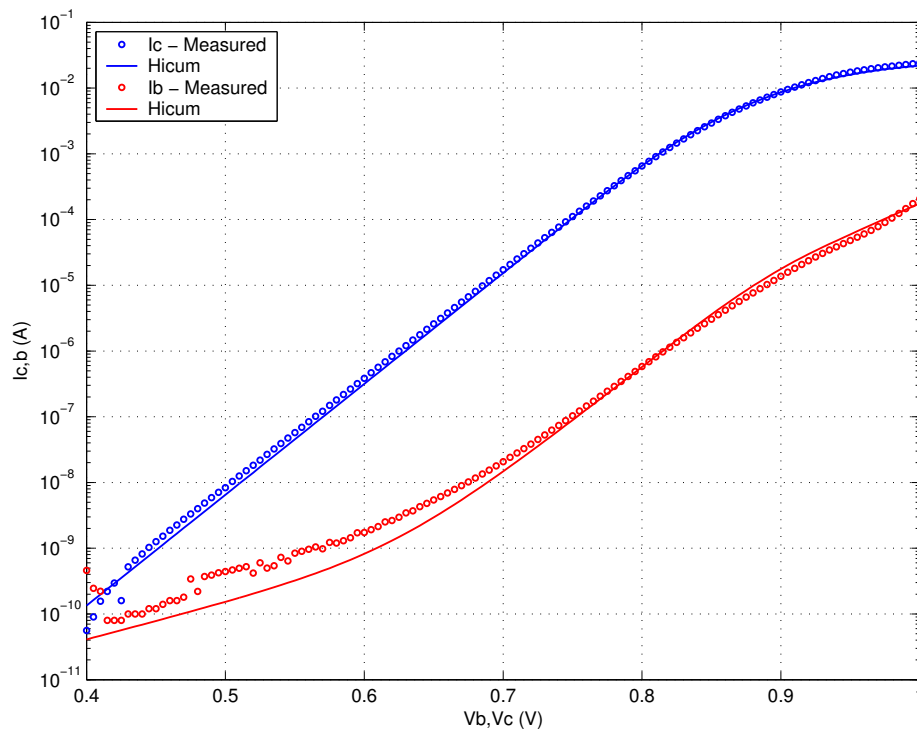


FIGURE 6.29 Beta vs. I_c : LV 0.13x3x1_232

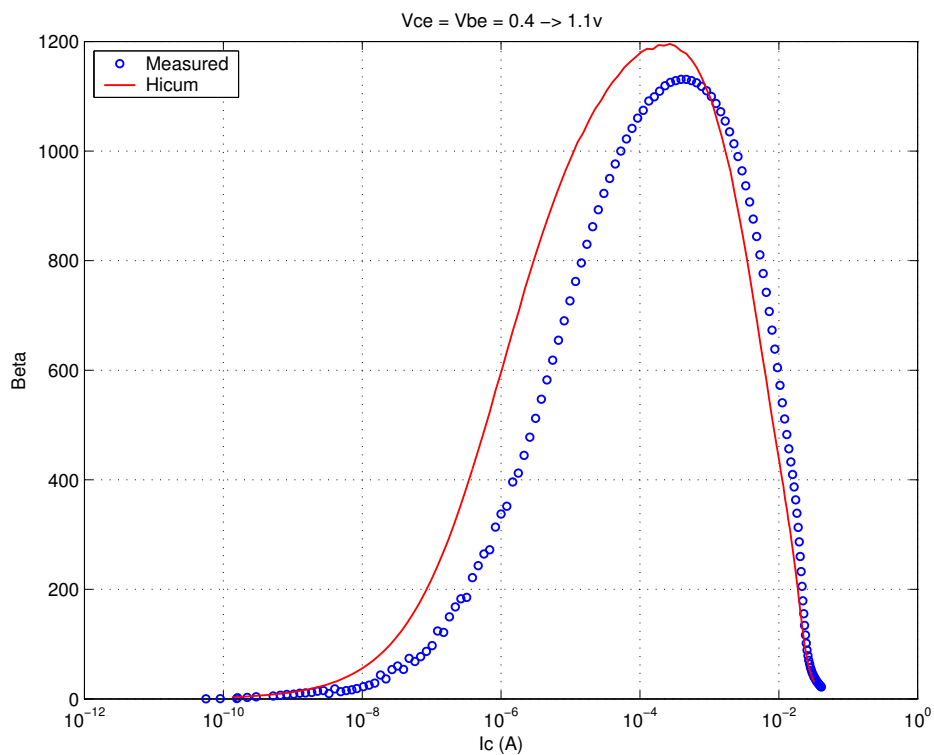


FIGURE 6.30 IC vs. VCE at constant IB: LV 0.13x3x1_232

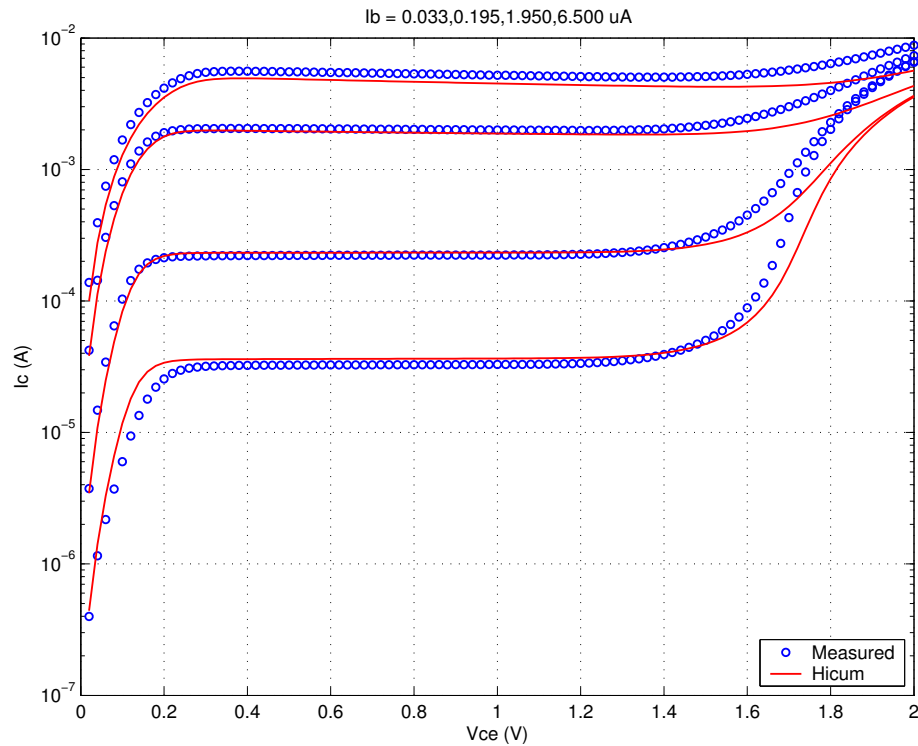


FIGURE 6.31 FT vs. IC: LV 0.13x3x1_232

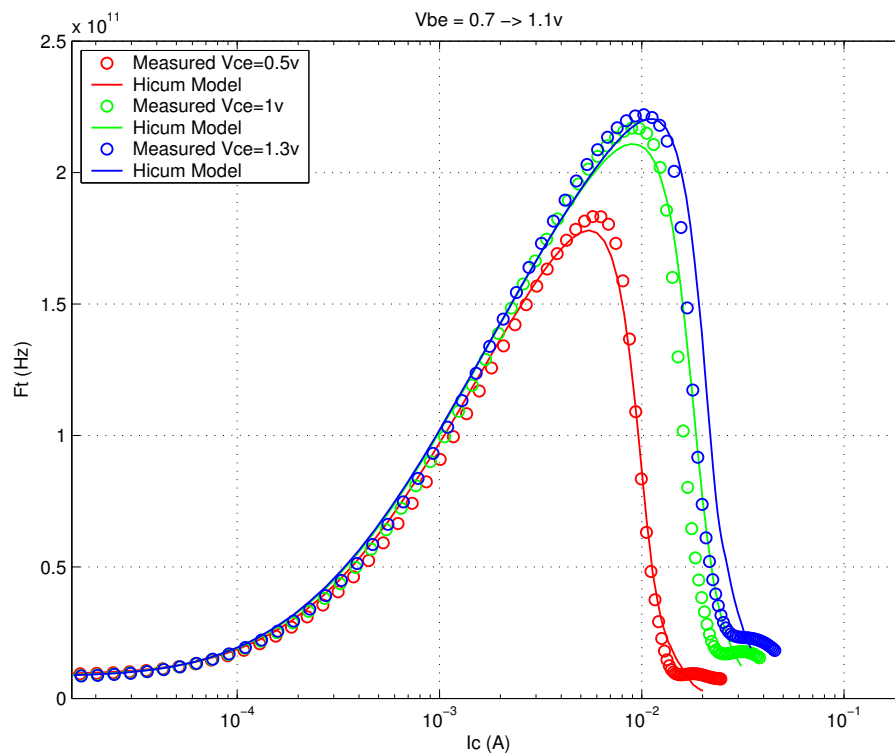
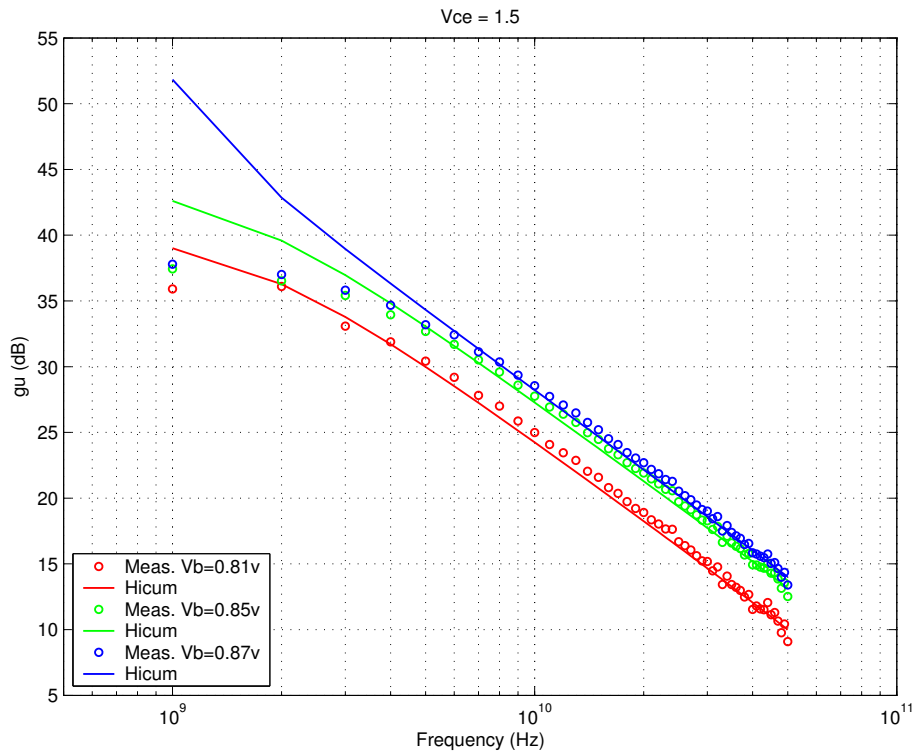


FIGURE 6.32 Power Gain vs. Freq: LV 0.13x3x1_232



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FIGURE 6.33 Y-parameters vs. FREQ: LV 0.13x3x1_232

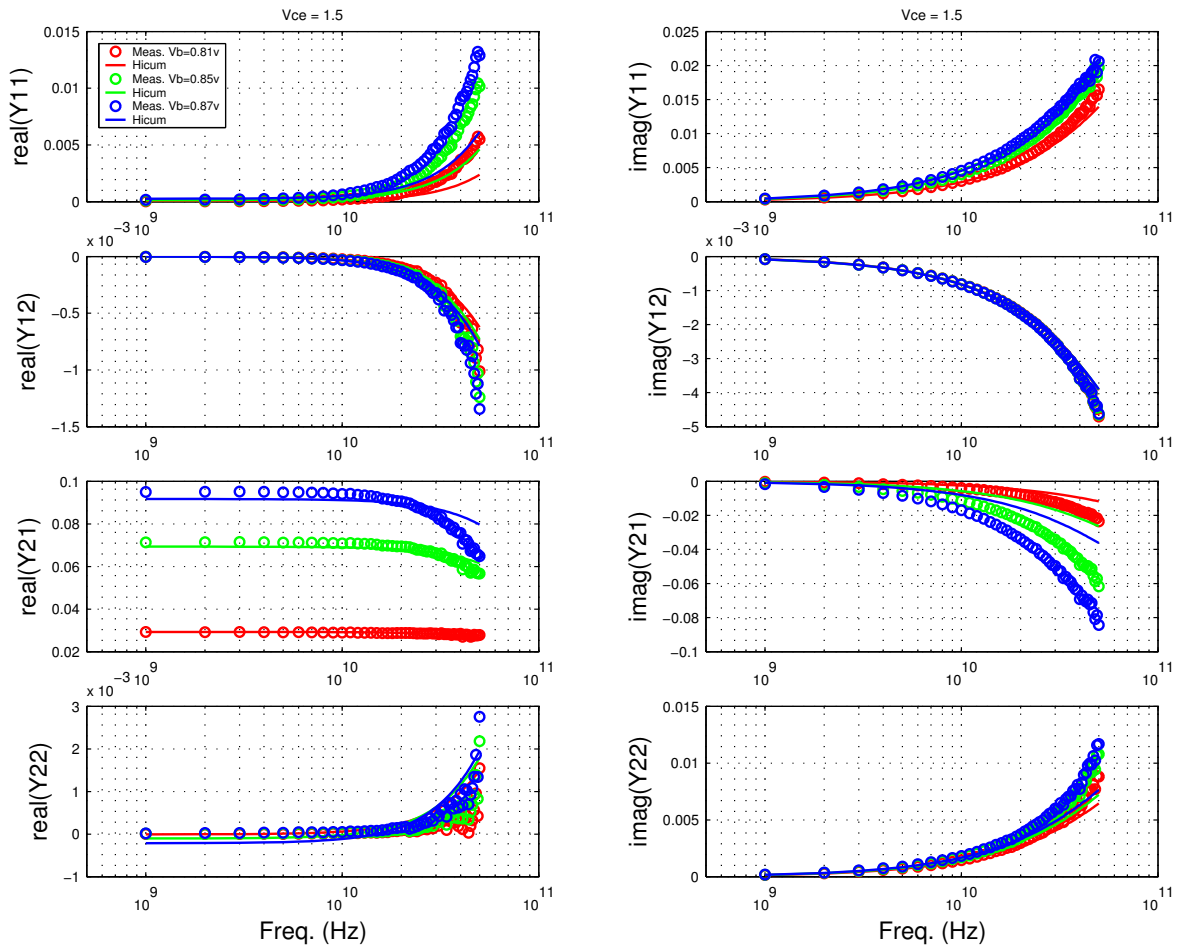


FIGURE 6.34 Gummel Plot MV 0.13x3x1_121

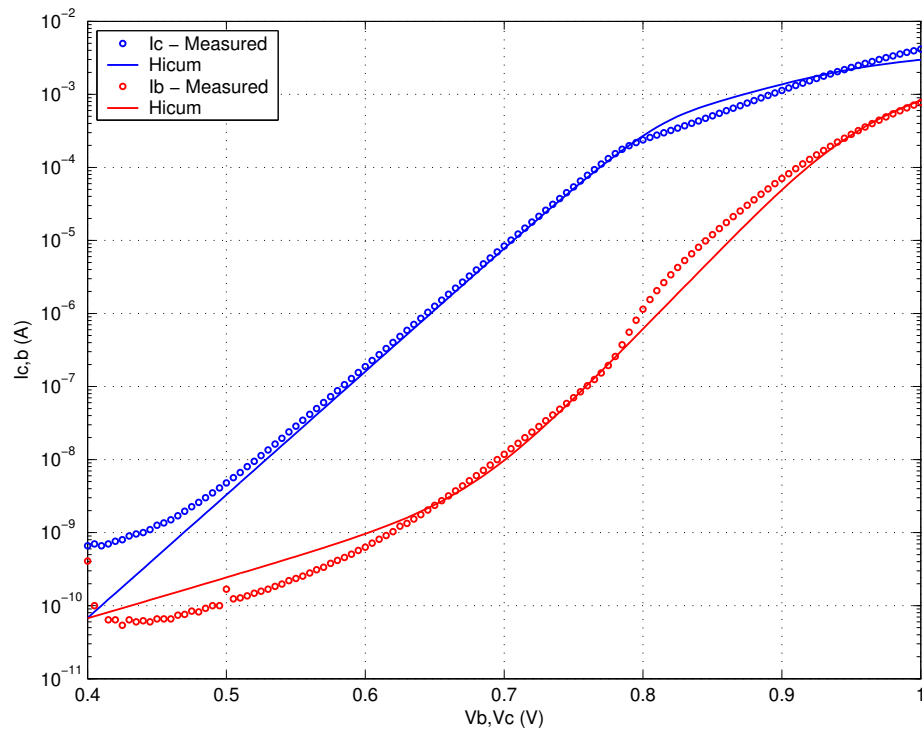


FIGURE 6.35 Beta vs. I_c : MV 0.13x3x1_121

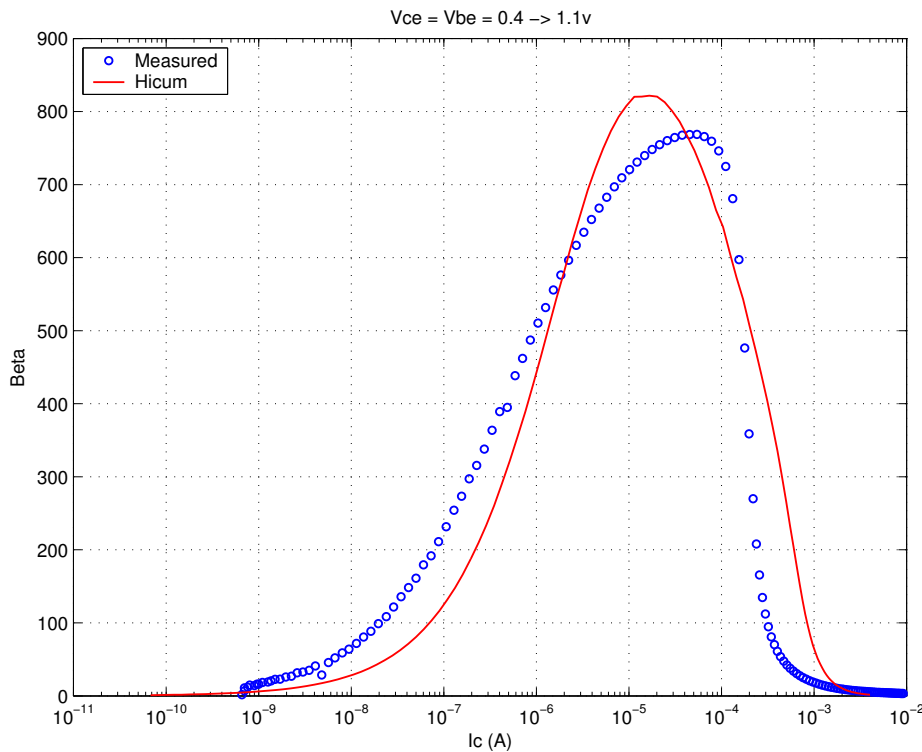


FIGURE 6.36 IC vs. VCE at constant IB: MV 0.13x3x1_121

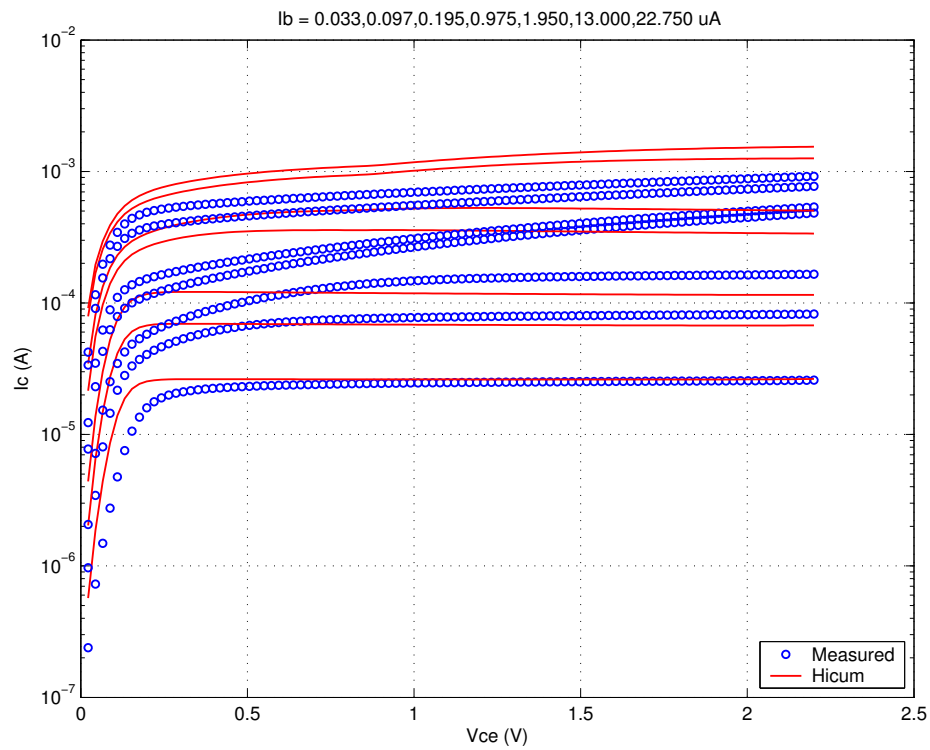
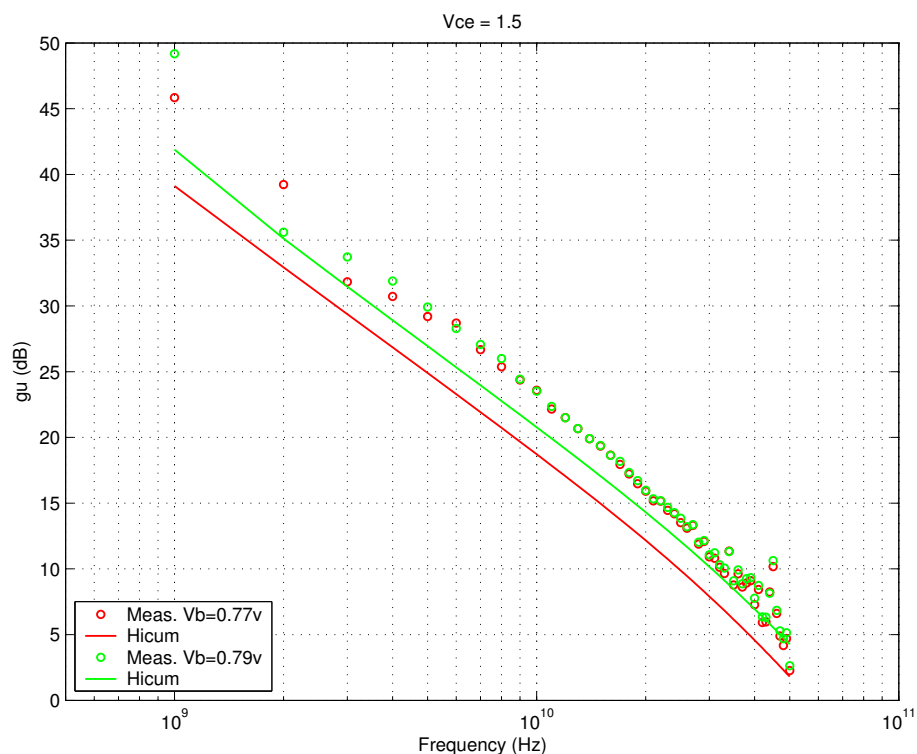


FIGURE 6.37 FT vs. IC: MV 0.13x3x1_121

FIGURE 6.38 Power Gain vs. Freq: MV 0.13x3x1_121



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FIGURE 6.39 Y-parameters vs. FREQ: MV 0.13x3x1_121

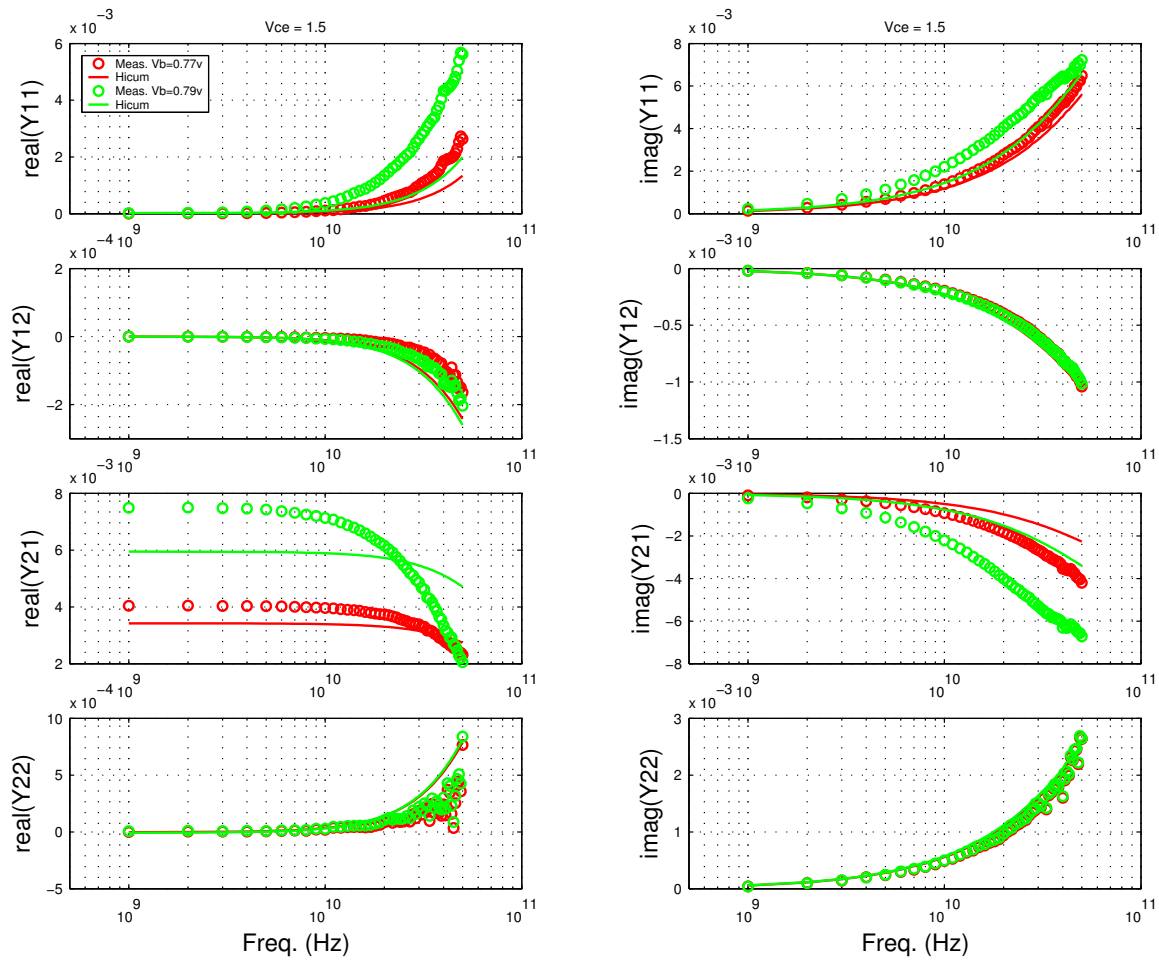


FIGURE 6.40 Gummel Plot MV 0.13x3x1_122

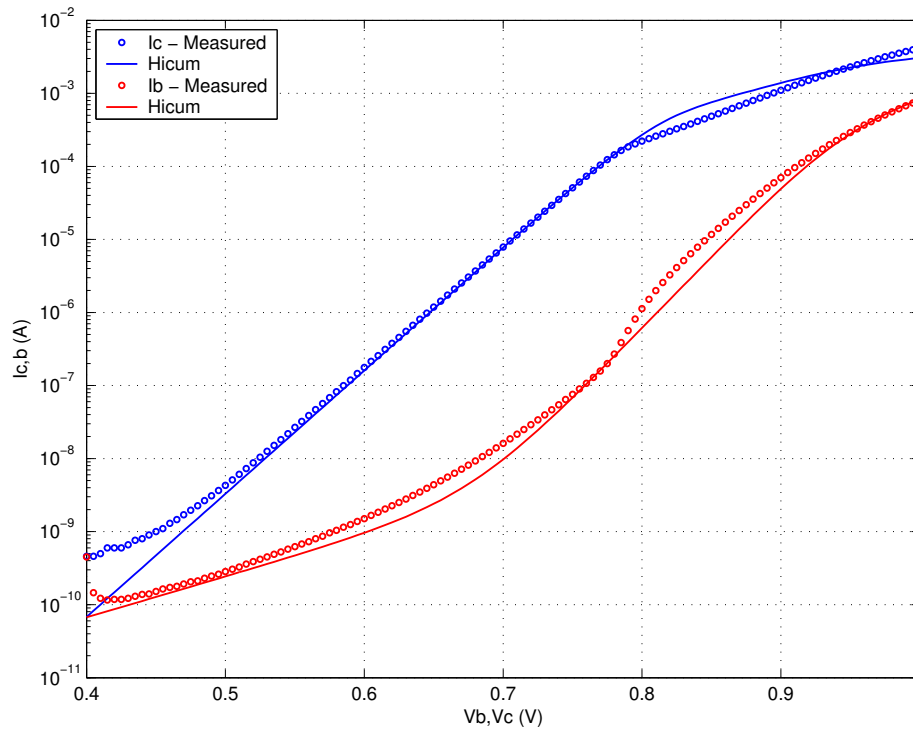


FIGURE 6.41 Beta vs. I_c : MV 0.13x3x1_122

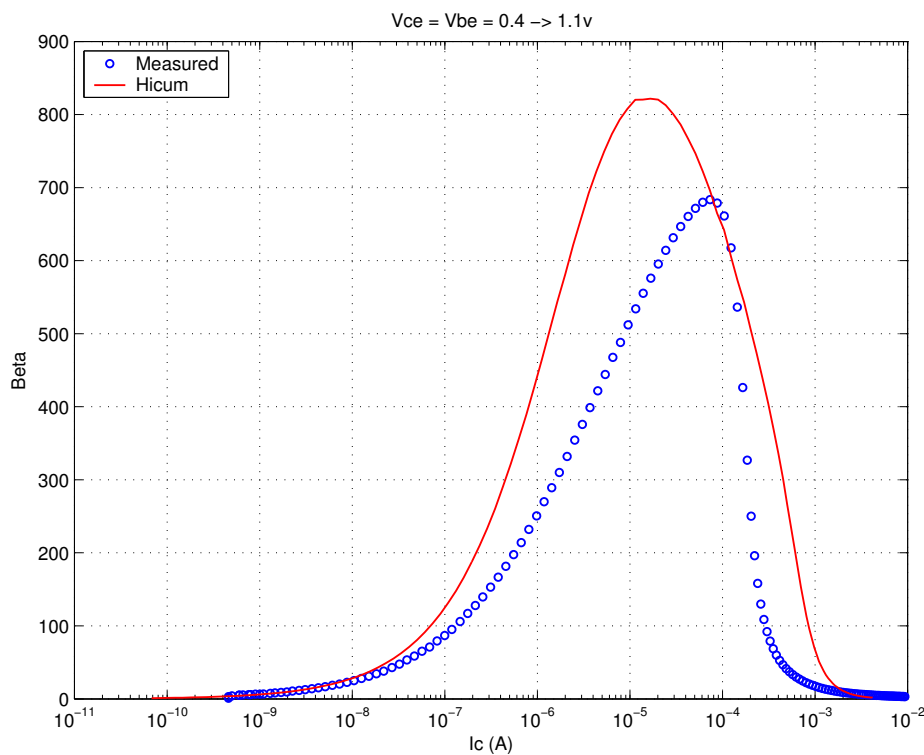


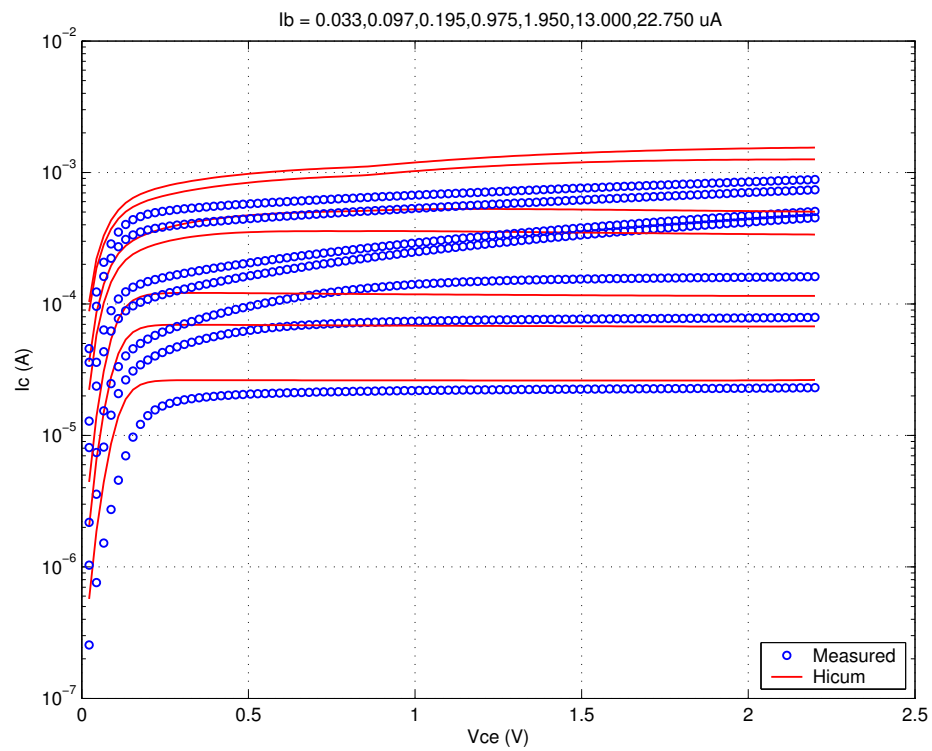
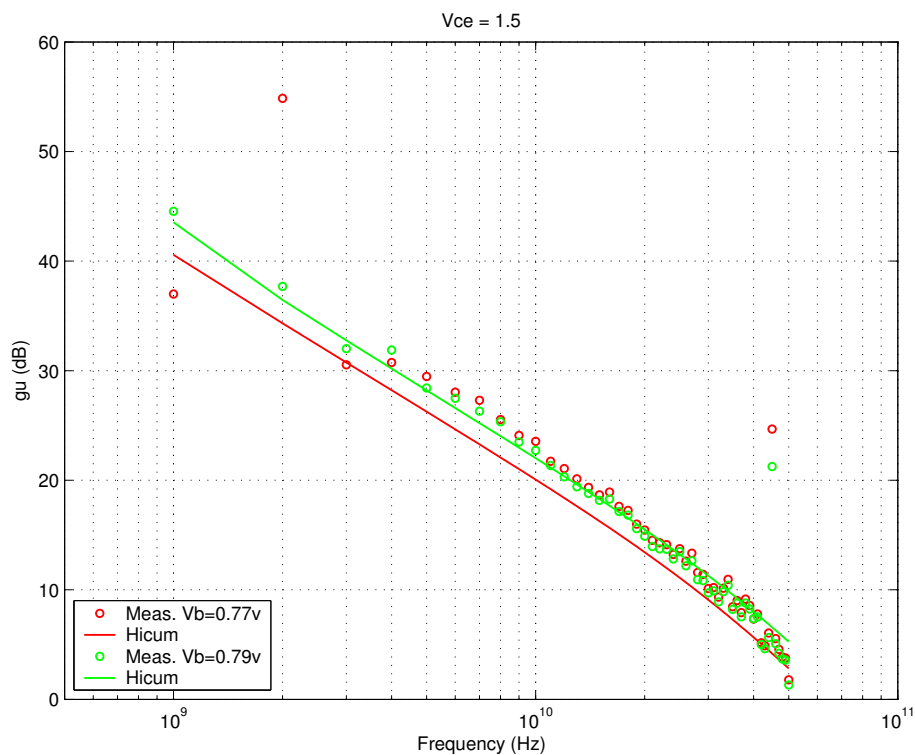
FIGURE 6.42 I_C vs. V_{CE} at constant I_B : MV 0.13x10x1_122FIGURE 6.43 f_T vs. I_C : MV 0.13x10x1_122

FIGURE 6.44 Power Gain vs. Freq: MV 0.13x10x1_122



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FIGURE 6.45 Y-parameters vs. FREQ: MV 0.13x10x1_122

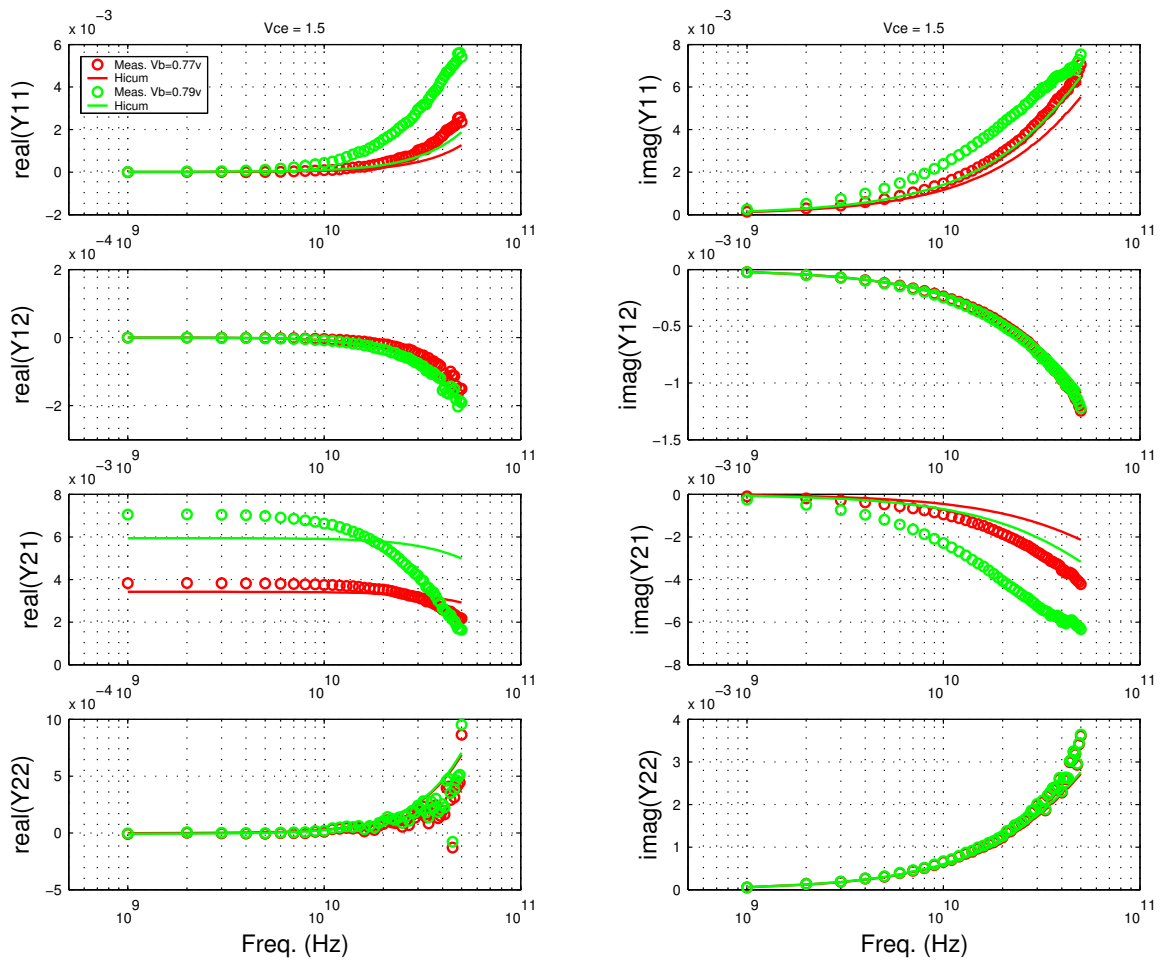


FIGURE 6.46 Gummel Plot MV 0.13x3x1_232

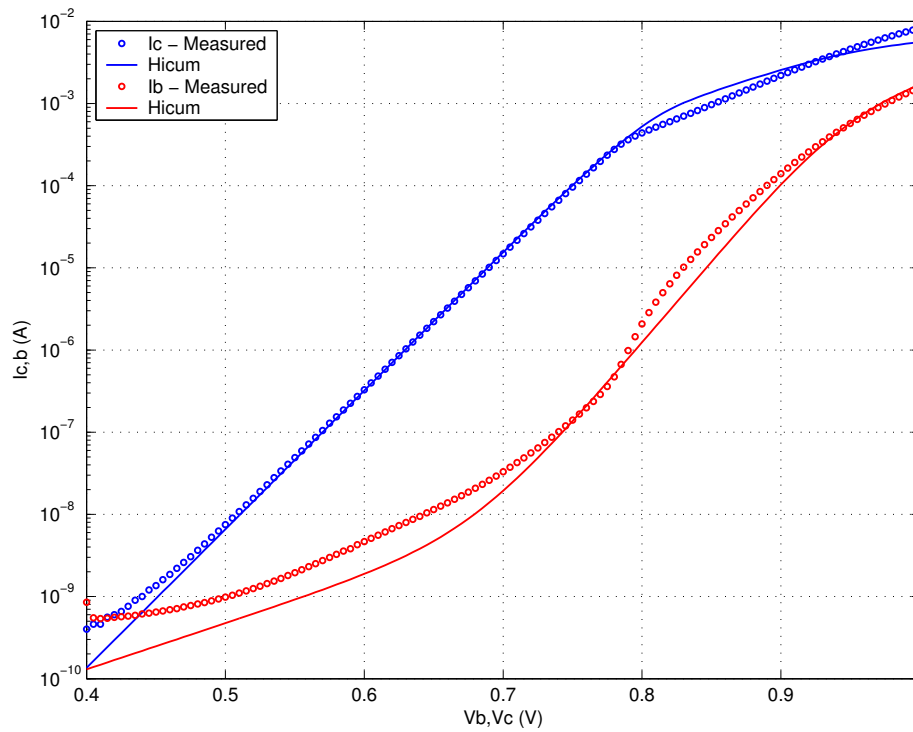


FIGURE 6.47 Beta vs. I_c : MV 0.13x3x1_232

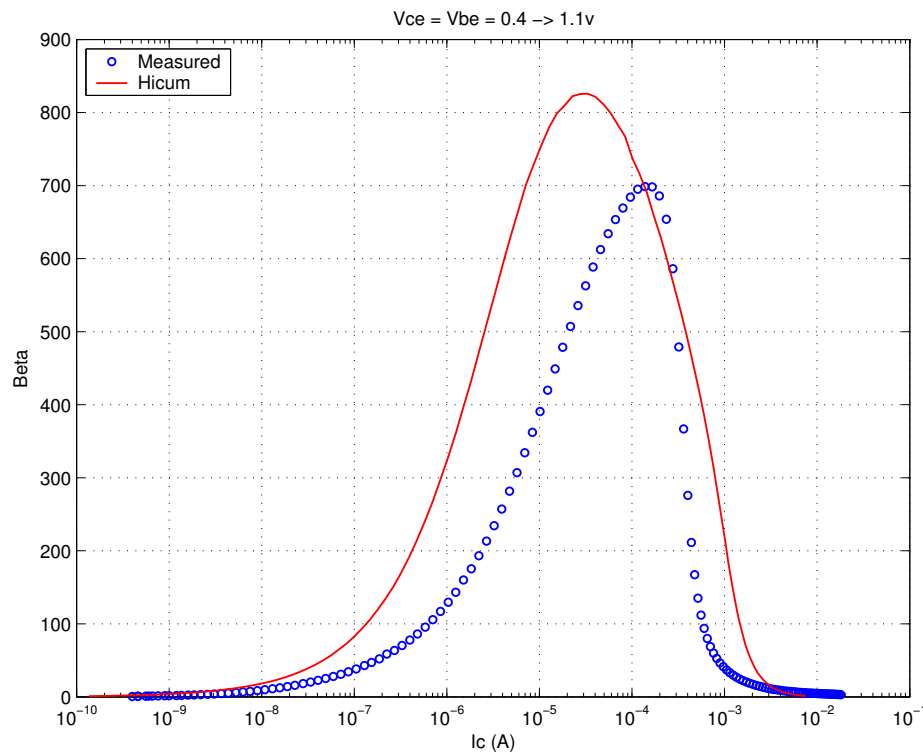


FIGURE 6.48 IC vs. VCE at constant IB: MV 0.13x3x1_232

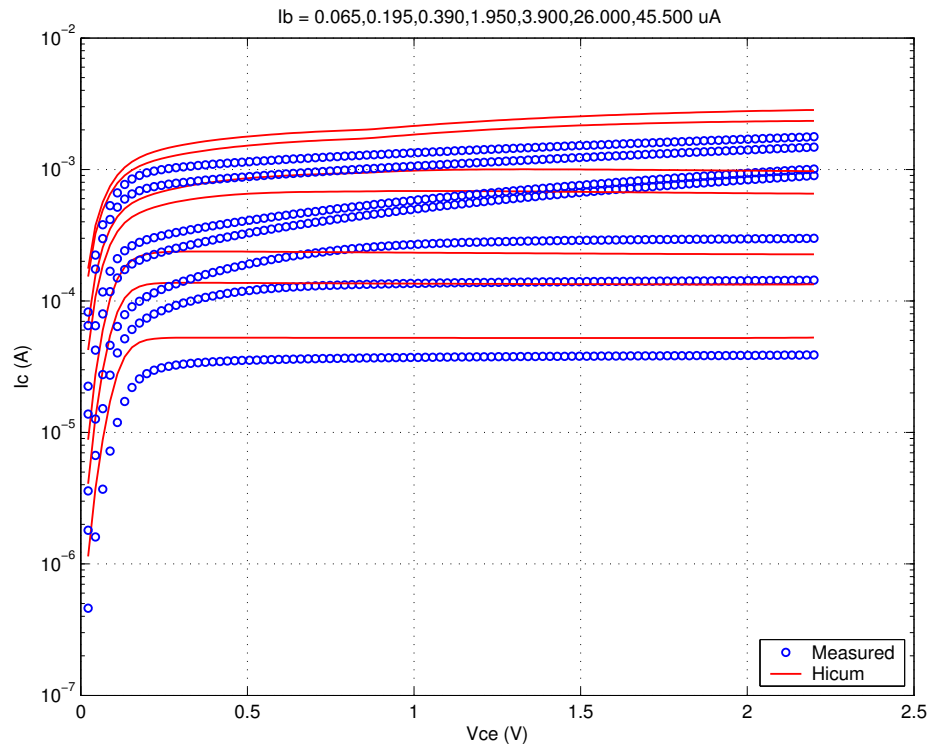
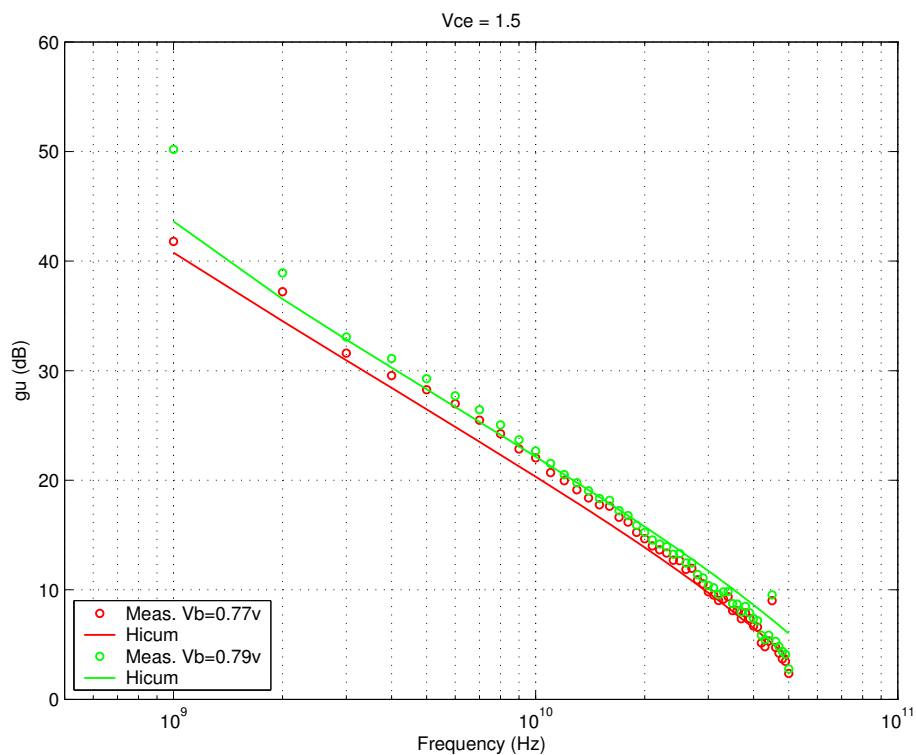


FIGURE 6.49 FT vs. IC: MV 0.13x3x1_232

FIGURE 6.50 Power Gain vs. Freq: MV 0.13x3x1_232

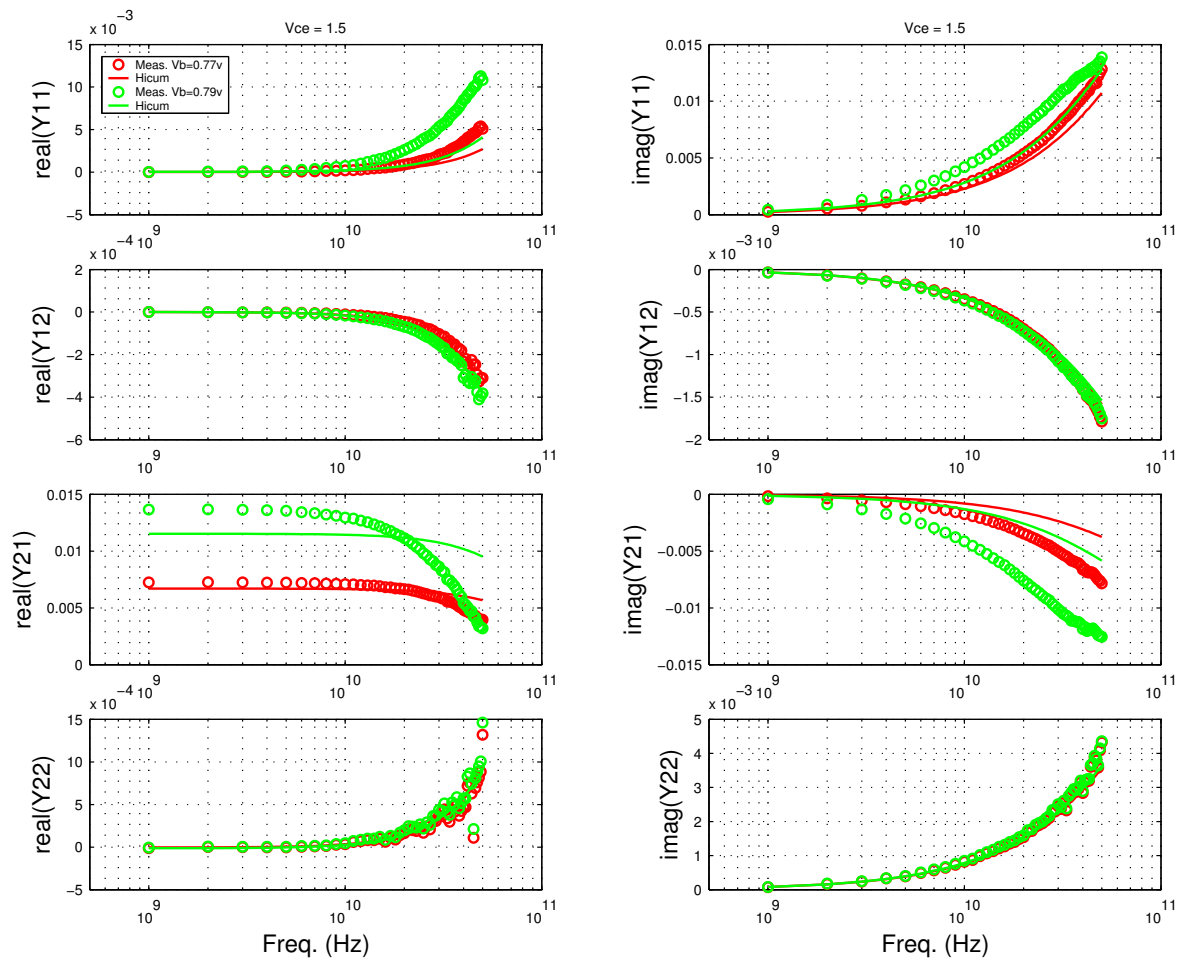


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FIGURE 6.51 Y-parameters vs. FREQ: MV 0.13x3x1_232



6.5 NPN Statistical and Corner Models

6.5.1 Statistical Model

A detailed description of the Backward Propagation of Variance (BPV) approach to statistical model generation is given in the MOSFET chapter. Only additional information exclusive to the NPN statistical models is given here. Unlike MOSFET models, the map between process and geometry parameters into model parameters is not well defined for NPN models. Mappings between process parameters, model parameters, and geometry parameters must be developed. The stand alone NPN models (Gummel-Poon, VBIC, Hicum, etc.) do not provide the physical correlation of the model parameters. Thus, a set of independent process parameters, rather than model parameters, are defined as the fundamental statistical variables in the simulator. Mappings for the process and geometry parameters into model parameters are developed based on device physics. A handful of process parameter variances are forward propagated in the BPV infrastructure based on expected variances at the process level such as Emitter-Poly CD variations. The remaining process parameter variances are directly BPV'd based on the variances in the ESPECs. A well conditioned system physically and mathematically results, guaranteeing precise simulation of the ESPEC variances and reasonable and consistent statistical simulation of non ESPEC quantities such as base resistance. The process parameters, the propagation technique, the affected model parameters, and target ESPECs for the Spice Gummel-Poon model (SGPM) are listed in Table 6.3. The statistically simulated ESPECs are listed in Table 6.5. Refer to the MOSFET chapter for statistical model usage guidelines.

TABLE 6.3 The Process Variables and the Affected Model Parameters in SGPM.

Process Parameters	BPV or FPV	Affected Model Parameters	Target ESPEC for BPV	Mismatch
Emitter Window CD	FPV	RE, RB, RBX, RC, CEOX, CJE, CJC, IS, ISE, IBEIS	NA	IC, BETA
Emitter Poly CD	FPV	CEOX, RBX	NA	
Base Ge doping concentration	BPV	C10	Vbe at mod. Ic	
Base Boron doping concentration	BPV	CBE, RBI, RBX, C10	Cbe	
Emitter Si/Poly interface property	BPV	IBEIS, RE	Peak Beta	IB
Emitter/Base Junction Leakage	BPV	IREIS	Beta @ low Vbe	IB @ low Vbe
Emitter doping concentration	BPV	RE, IBEIS	Ic @ Vbe=1.1v	
Substrate doping concentration	BPV	CJS	Ccs	
Base width	BPV	RBI, T0	Ft of LV & HV dev.	
Local Collector Implant (LV dev.)	BPV	CJC of LV dev.	CBC of LV dev.	
Local Collector Implant (MV dev.)	BPV	CJC of MV dev.	CBC of MV dev.	

6.5.2 Centering

Refer to section 2.6.1 for centering within the BPV framework. The NPN model is extracted from a golden die which measures very close to the nominal of the ESPECs. As a result, the model parameter variation needed to exactly align the model to the nominal ESPECs is small. The simulated NOM ESPECs are listed in Table 6.6.

6.5.3 Corner Models

The goal of the corner models are to capture the device electrical performance limits through appropriate variation of the process parameters. Slow and fast corners are provided. Details of the corner models are given in Table 6.4. All the NPN ESPEC limits can not be captured with 2 corners. The target ESPEC parameters for the corner models are I_C , BETA, and F_t . The C_{BE} and C_{CS} ESPECs are also aligned to the ESPECs in the corner model. C_{BC} variation in the corner models is reduced from the ESPEC limit in order to retain consistent and physical F_t prediction. The verification of the simulated corner ESPECs are listed in Table 6.5.

TABLE 6.4 Corner model specifications

	FAST	SLOW
Emitter resistance	Component 1 is higher due to lower I_b (high Beta); Component 2 is lower due to higher emitter doping. Net is ~15% lower	Component 1 is lower due to higher I_b (low Beta); Component 2 is higher due to lower emitter doping. Net is ~15% higher
Extrinsic base resistance	Component 1 is lower (Nom. - 1σ link dist.); Component 2 is higher due to lower base doping (low Cbe). Net is ~10% higher	Component 1 is higher (Nom. + 1σ link dist.); Component 2 is lower due to higher base doping (high Cbe). Net is ~10% lower
Intrinsic base resistance	Component 1 is higher due to shorter base width; Component 2 is higher due to lower base doping (low Cbe). Net is 30% higher	Component 1 is lower due to longer base width; Component 2 is lower due to higher base doping (high Cbe). Net is 30% lower
Base emitter junction cap.	90% of NOM case	110% of NOM case
Base collector junction cap.	Max. case of Cbc	Min. case of Cbc
Collector substrate junction cap.	Min. case of Ccs	Max. case of Ccs
Intrinsic collector resistance	~15% lower; aligned to higher collector doping (higher Cbc)	~15% higher; aligned to lower collector doping (lower Cbc)
Collector saturation current	Min. case of V_{be} for fixed and moderate I_c	Max. case of V_{be} for fixed and moderate I_c
Base current	Max. case of beta (lower I_b)	Min. case of beta (higher I_b)
Base width	Smaller; aligned to max. F_t E-spec.	Larger; aligned to min. F_t E-spec.

TABLE 6.5 E-spec. vs. Model (Long transistor - 0.13x3 μ m emitter with 122 configuration)

Device	Espe Name (unit)	Slow			Nom			Fast		
		Espe c	Corner	Stat	Espe c	Corner	Stat	Espe c	Corner	Stat
Low Voltage NPN Hicum (ln122_hicum)	beta ¹	800.0	489.5	387.0	1200.0	1114.0	1260.0	1600.0	1882.0	2130.0
	cbc ² (fF)		8.16	8.14	17.10	8.60	8.60		9.20	9.06
	cbe (fF)		7.62	7.70	20.00	6.99	6.88		6.32	6.06
	ccs (fF)		8.69	8.79	14.60	6.95	6.94		5.21	5.09
	ft (GHz)	225.00	227.50	226.00	250.00	242.40	248.00	275.00	263.60	270.00
	ic (uA)		4.37	3.72	10.00	7.63	7.74		13.12	11.80
	Jc ³ (Pk. Ft)		13.85	12.00	39.54	16.57	16.69		20.74	21.38
	fmax ⁴ (GHz)		274.90	289.00	240.00	265.80	305.00		258.50	321.00
	bvceo ⁵ (V)	2.00	1.90	2.14	1.60	1.66	1.67	1.20	1.31	1.20

TABLE 6.5 E-spec. vs. Model (Long transistor - 0.13x3μm emitter with 122 configuration)

Medium Volt- age NPN Hicum (mn122_hicum)	beta ¹	400	386.50	394	800	817.90	826	1600	1674	1260
	cbc ² (fF)		3.84	3.77	3.90	3.93	3.93		4.03	4.09
	cbe (fF)		7.40	7.96	6.90	6.92	6.93		6.43	5.90
	ccs (fF)		8.68	8.79	6.90	6.94	6.94		5.21	5.09
	ft (GHz)	50.00	50.61	50.00	56.00	56.22	56.50	62.00	62.80	63.00
	ic (uA)	4.50	4.50	3.58	7.50	7.74	7.84	12	14.35	12.10
	Jc ³ (Pk. Ft)		1.04	0.93	6.00	1.19	1.27	6.90	1.46	1.61
	fmax ⁴ (GHz)		153.10	145.00	160.00	158.30	159.00		162.80	173.00
	bvceo ⁵ (V)	3.65	3.79		3.20	3.19		2.75	2.73	

Notes:

1. Beta: The E-spec is asymmetrical across the NOM case. The statistical model prediction is +/- 3 sigma and is thus symmetrical across NOM.
2. C_{bc}: Variation in the corner models is reduced from the E-spec limit in order to retain consistent and physical Ft prediction.
3. J_c is the current density (mA/μm²) at peak Ft. Only nominal E-spec is specified. This parameter is not a BPV targeted E-spec for corner or statistical model extraction.
4. F_{max}: Only nominal E-spec. is specified. Corner and statistical model predictions are shown for all cases. This parameter is not a BPV targeted E-spec. for corner or statistical model extraction.
5. BV_{ceo}: Gummel-Poon model does not include breakdown effects. Hicum model predictions are shown. This parameter is not a BPV targeted E-spec. for corner or statistical model extraction.

6.6 NPN Mismatch Model

The mismatch model captures the local variation between identical devices. The collector current and the current gain (Beta) mismatch between two identical NPNs (~10μm apart) with identical V_{BE} and V_{CE} are characterized and captured in the mismatch model.

NPN mismatch is characterized in terms of percentage difference in Beta (β) and I_C. The I_C mismatch percentage is calculated using the following expression:

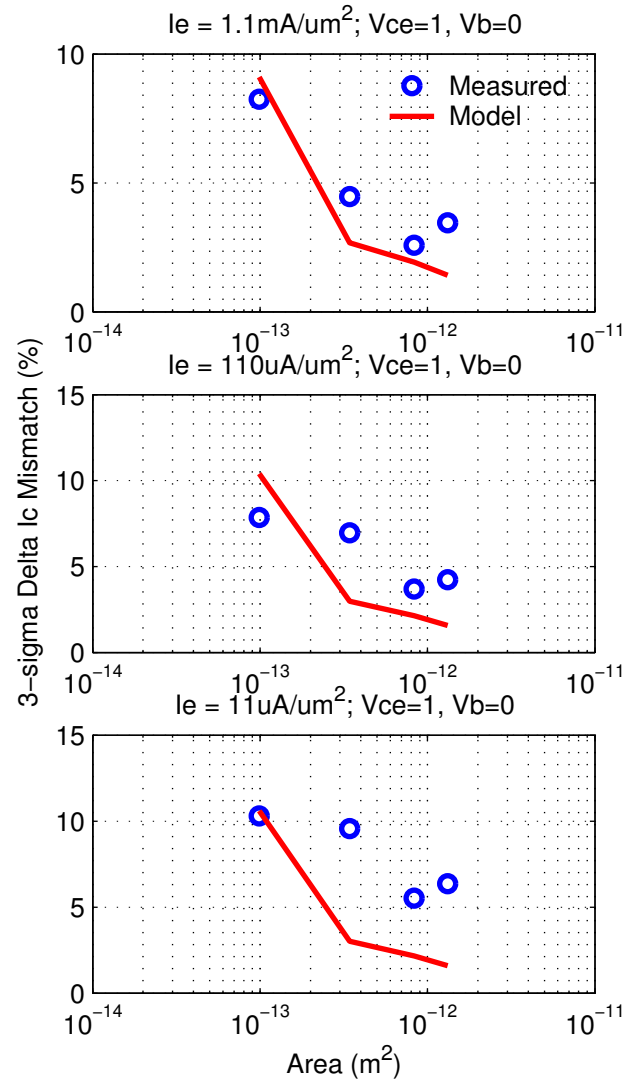
$$\Delta I_C = 100 \times \frac{I_{C1} - I_{C2}}{I_{C1}} \quad (\text{EQ 1})$$

The β mismatch is calculated using the following expression:

$$\Delta \beta = 100 \times \frac{\beta_1 - \beta_2}{\beta_1} \quad (\text{EQ 2})$$

The Ge concentration and EW CD mismatch sigmas are used fit the I_C mismatch. The emitter surface recombination velocity sigma fits the additional mismatch seen in the β measurements. In operational regions where I_C and β are not affected by series resistance, low or high bias effects, NPN mismatch can be adequately represented with the aforementioned process parameters, combined with an inverse square root dependence on active emitter area.

FIGURE 6.52 Measured and simulated I_c and Beta mismatch plots of high-speed NPNs (ln122_hicum)



6.7 Released Model Quality Assurance (QA)

A rigorous QA procedure is executed before any new model release. The geometry dependence of 9 key device parameters is examined for any non-physical behavior for all 3 cases: Nominal, Fast, and Slow. These parameters are listed in Table 6.6.

TABLE 6.6 NPN electrical parameters list examined as part of model release QA

Parameter	Description
BETA	Current gain
I_C	IC at $V_{be}=0.7v$
F_t	Unity gain cut-off frequency
F_{max}	Unity power gain cut off frequency
C_{BE}	Base-Emitter capacitance
C_{BC}	Base-Collector capacitance
C_{CS}	Collector-Substrate capacitance
R_E	Emitter Resistance
R_B	Base Resistance

Figures 6.53 through 6.54 illustrate the emitter length dependence of these 9 parameters.

FIGURE 6.53 QA Plots: LV 0.13xL_122

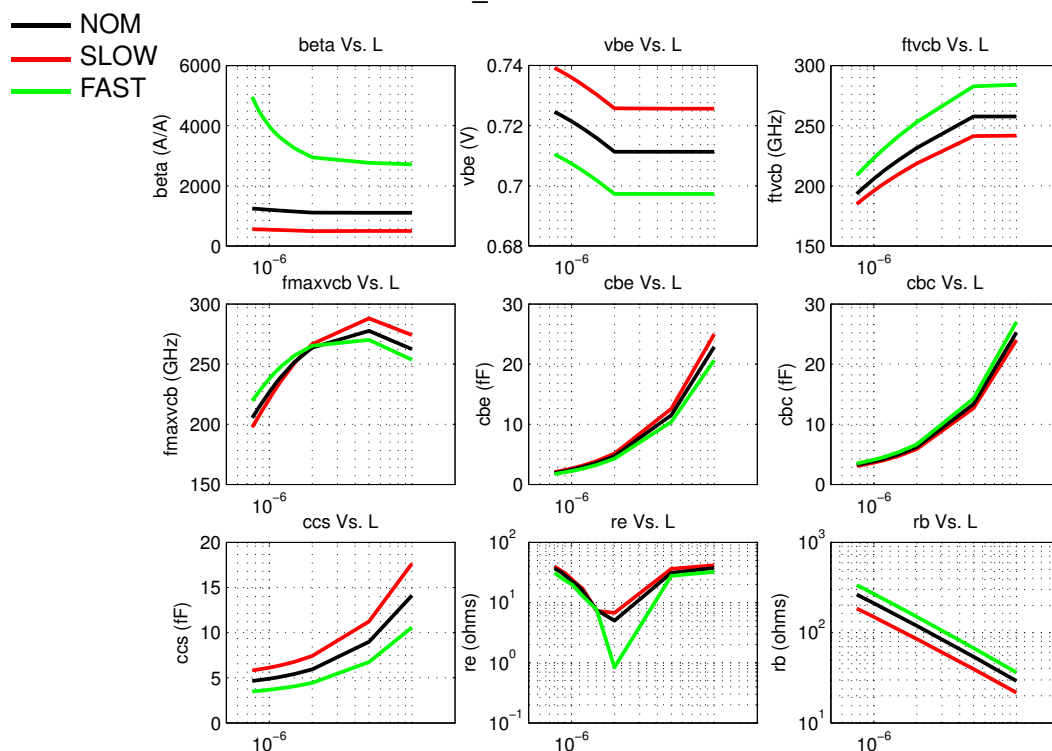
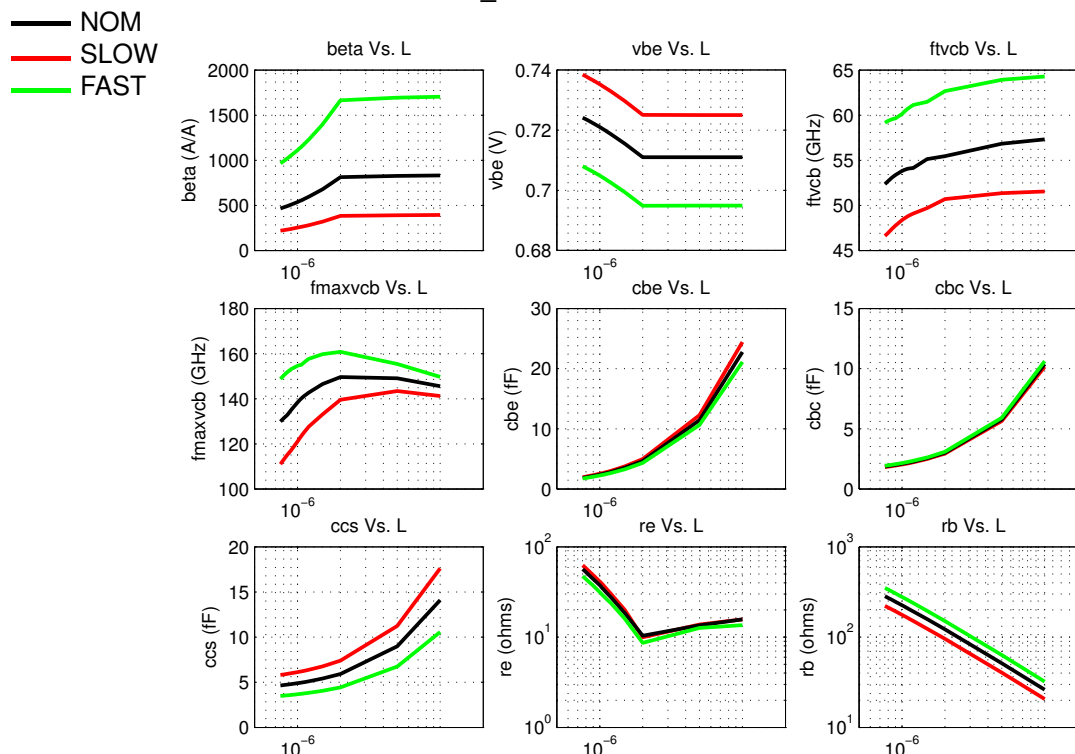


FIGURE 6.54 QA Plots: MV 0.13xL_122



6.8 Model Update History

TABLE 6.7 NPN model specific updates in model release version SBC18 v6.3

v6.3 update	Devices	Reason	Impact on user
Evaluation models for H3 NPNs	[l,m],n	Initial evaluation release	

TABLE 6.8 NPN model specific updates in model release version SBC18 v6.4

v6.4 update	Devices	Reason	Impact on user
Modified high-speed npn model	ln*	To align to latest measurements	
Deleted medium-voltage NPN model	mn*	Existing model from sbc18h2 was not an accurate representation of the sbc18h3 process	Cannot simulate circuits with medium-voltage NPNs

TABLE 6.9 NPN model specific updates in model release version SBC18 v6.5

v6.5 update	Devices	Reason	Impact on user
Modified high-speed npn model	ln*	To align to latest measurements	Lower Ic for given Vbe. Spot differences in RF behavior. Overall, a more accurate representation of expected device behavior

TABLE 6.10 NPN model specific updates in model release version SBC18 v6.5

v6.5 update	Devices	Reason	Impact on user
Added silicon based model for the medium voltage NPN	mn*	To align to latest measurements	New silicon based model added. Previous release did not include this model.

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7.0 PNP Model

7.1 Lateral PNP

7.1.1 Device Description

TABLE 7.1 Lateral PNP summary

Device Name	Emitter Area	Model Name
lpnp	1x1 μm^2	pl1g

The SBC18 technology supports a fixed device size lateral PNP symbol (pnpl) where multiple devices can be placed in parallel. The device cross section and layout view of the are shown in Figure 7.1 and Figure 7.2. The epi-layer of the NPN transistors form the intrinsic base of the PNP. The deep N+ sinker and buried layer, common to the NPN and high performance varactor, form the extrinsic base.

FIGURE 7.1 Cross-section of Lateral pnp layout

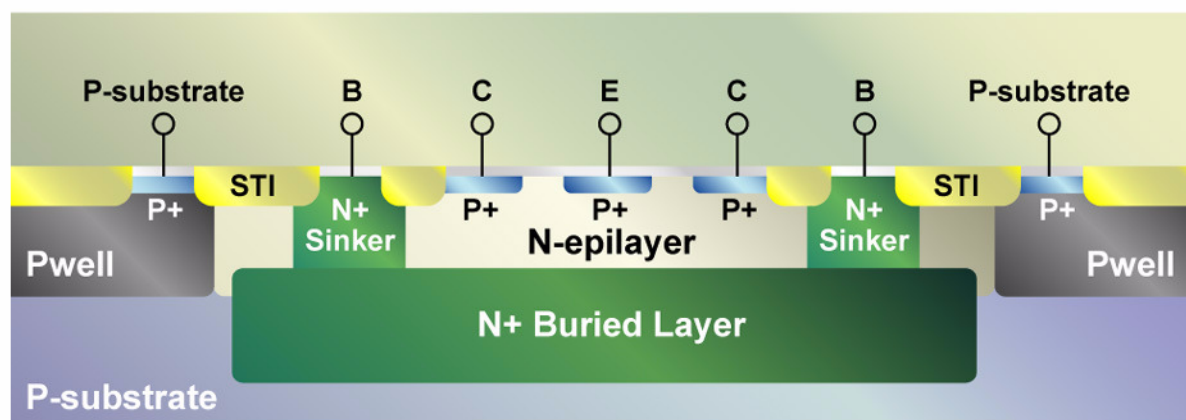
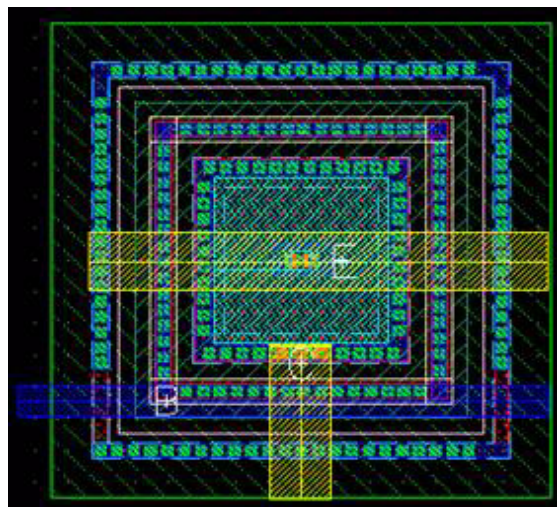


FIGURE 7.2 Layout of the lateral PNP transistor



7.1.2 Model Description

The PNP transistor model is a Gummel-Poon based sub-circuit. Therefore, it is extracted based upon the standard SGPM bipolar extraction routine. The equivalent circuit of the PNP transistor is shown in Figure 7.3. A three-transistor sub-circuit model captures all the parasitic components associated with the lateral PNP transistor. LPNP is the main PNP transistor. Table 7.2 provides descriptions of the sub circuit elements.

FIGURE 7.3 Equivalent Circuit of pnp

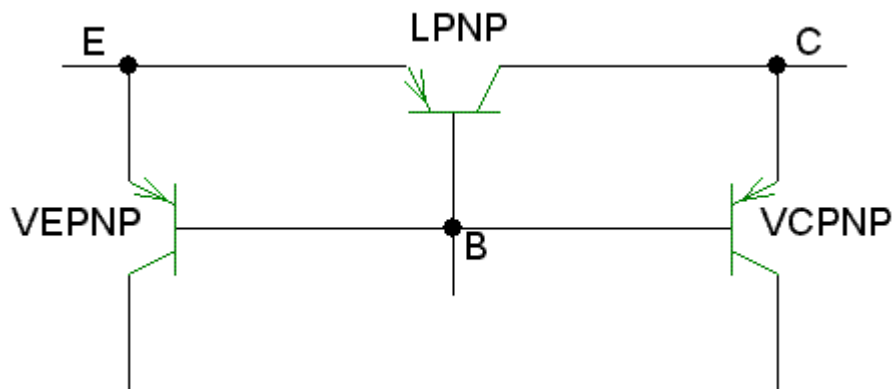


TABLE 7.2 Model Sub-circuit Element Names

Element Description	
LPNP	Intrinsic lateral PNP
VEPNP	Parasitic PNP formed by emitter-base-substrate
VCPNP	Parasitic PNP formed by collector-base-substrate

7.1.3 LPNP Model Verification

Figure 7.4 through Figure 7.6 display the lateral PNP gummel plot, beta, and output characteristics. Figure 7.7 displays the temperature characterization for the lateral PNP. For verification purpose, the forward beta (BF) model parameter is shifted from the nominal model by 22% in order to match this measured data. This shift is within the corner specification.

FIGURE 7.4 PNP Gummel Plot

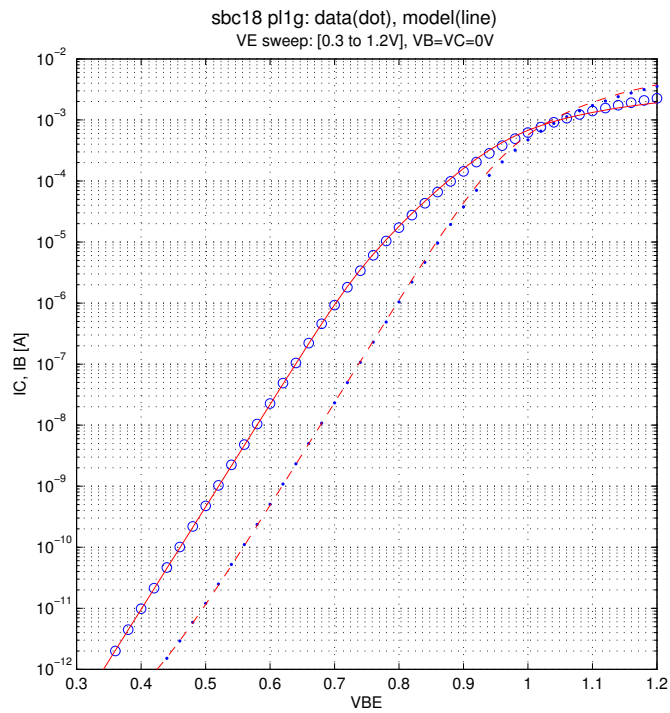


FIGURE 7.5 PNP IV Forward Beta

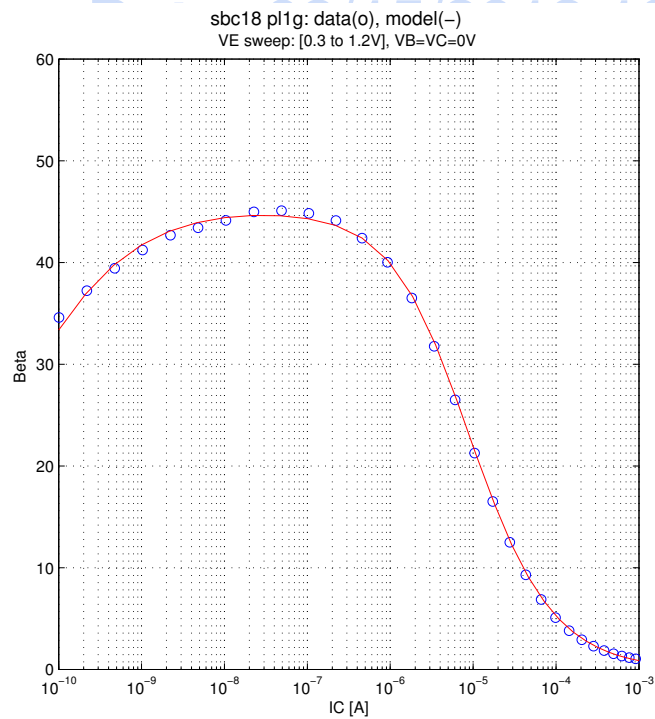
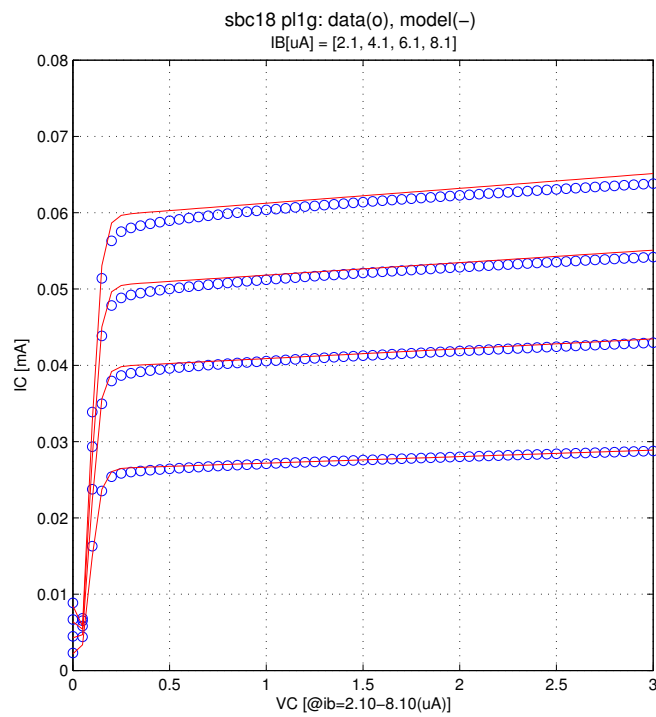
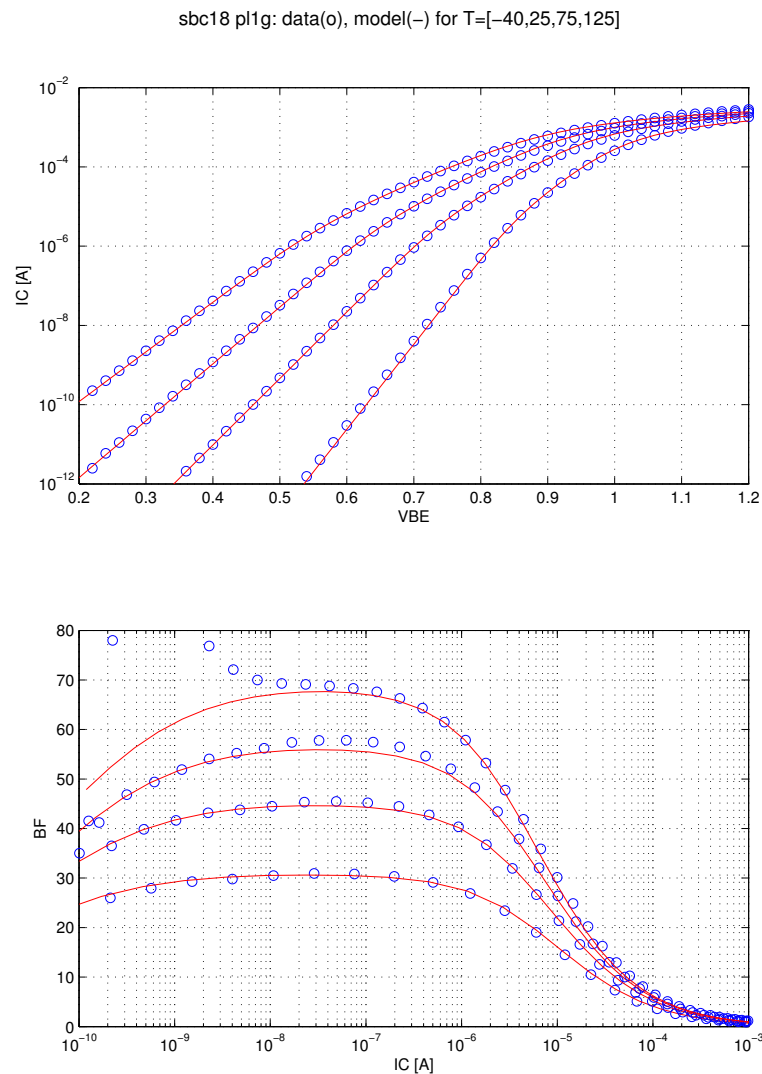


FIGURE 7.6 PNP I_c vs V_{ce} 

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FIGURE 7.7 PNP temperature characteristics



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7.1.4 LPNP Statistical and Corner Models

The primary process parameter that controls the statistical behavior of the LPNP is the base doping (N-epi layer doping). The current gain (β), saturation current (I_s), and Early Voltage (V_{AF}) are the primary device performances affected. See Section 15.0 for further explanation of the device interdependencies in the corner models and use of the X-Sigma corner models. Table 7.3 lists the ESPEC values compared to simulated corner and statistical values for lateral pnp device (pl8g).

TABLE 7.3 Espec, Corner and Statistical model comparison for lnp device: pl8g (8x pl1g's in parallel)

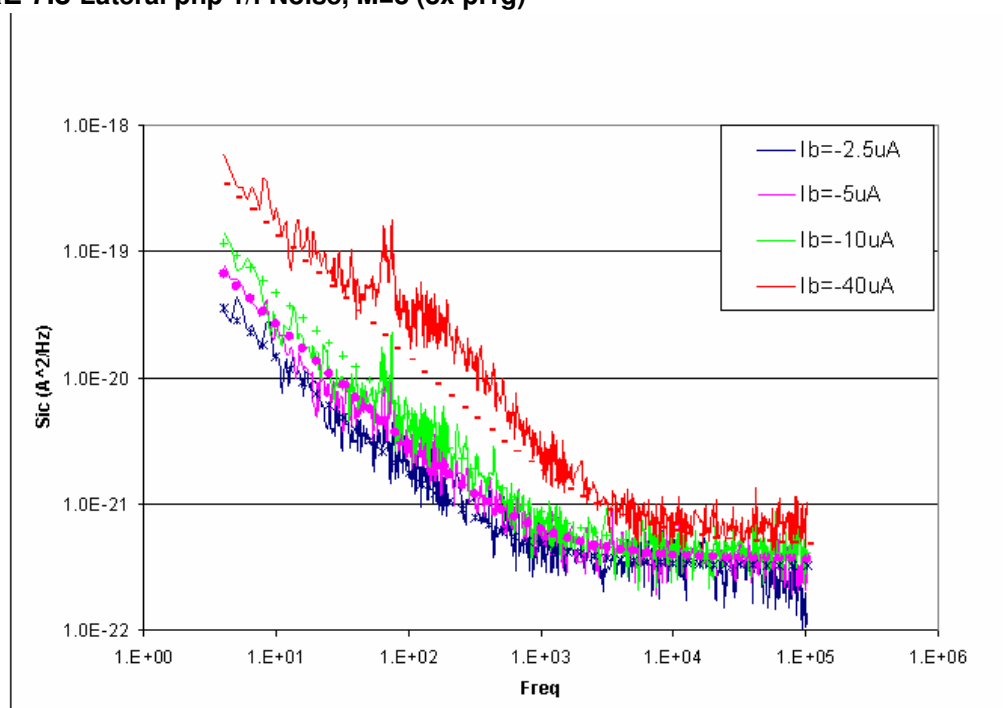
Device	name	units	slow			nomi			fast		
			Espec	Corner	Stat	Espec	Corner	Stat	Espec	Corner	Stat
8xpl1g	beta (Ie=10uA)		20	20	13.3	32	32	32.1	58	58.0	50.9
	Va	V	20	20	20.1		32.9	33.2		45.8	46.3

7.1.5 LPNP Mismatch Models

Mismatch is not supported for the LPNP device.

7.1.6 Lateral PNP 1/f Noise Data vs. Model

Figure 7.8 displays the 1/f noise characterization for eight LPNPs in parallel.

FIGURE 7.8 Lateral pnp 1/f Noise, M=8 (8x pl1g)

7.2 Vertical PNP

7.2.1 Device Description

The SBC18 process offers a vertical PNP transistor formed by a p+ emitter, Nwell base, and psub collector as shown in Figure 7.9. There are four discrete vertical PNP transistors in the model library given in Table 7.4. The layout view is shown in Figure 7.9.

FIGURE 7.9 Cross Section of the Vertical PNP

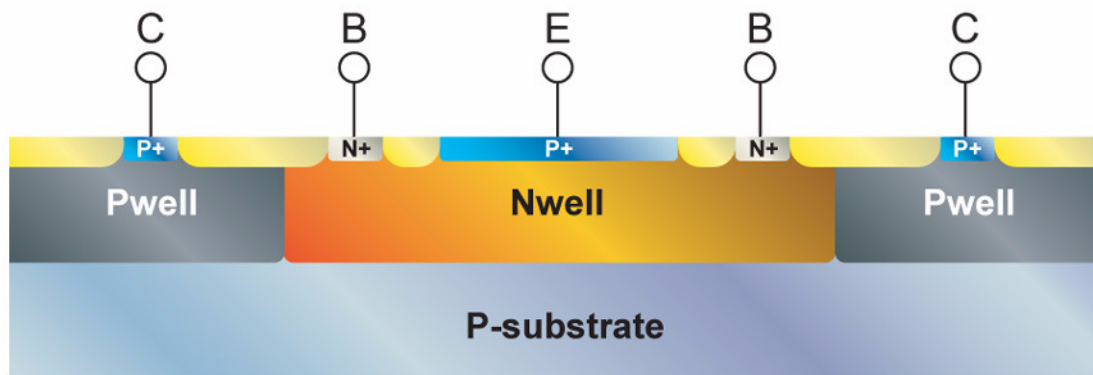
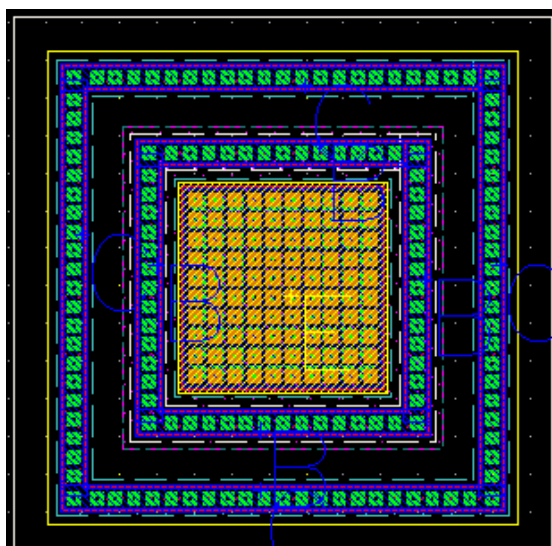


TABLE 7.4 VNP Devices

Design Kit Name	Model Name	Emitter Area
vpnp	PNPa	25x25 μm^2
vpnp	PNPb	11x11 μm^2
vpnp	PNPc	5.4x5.4 μm^2
vpnp	PNPd	3x3 μm^2

FIGURE 7.10 Top view of the vertical PNP transistor



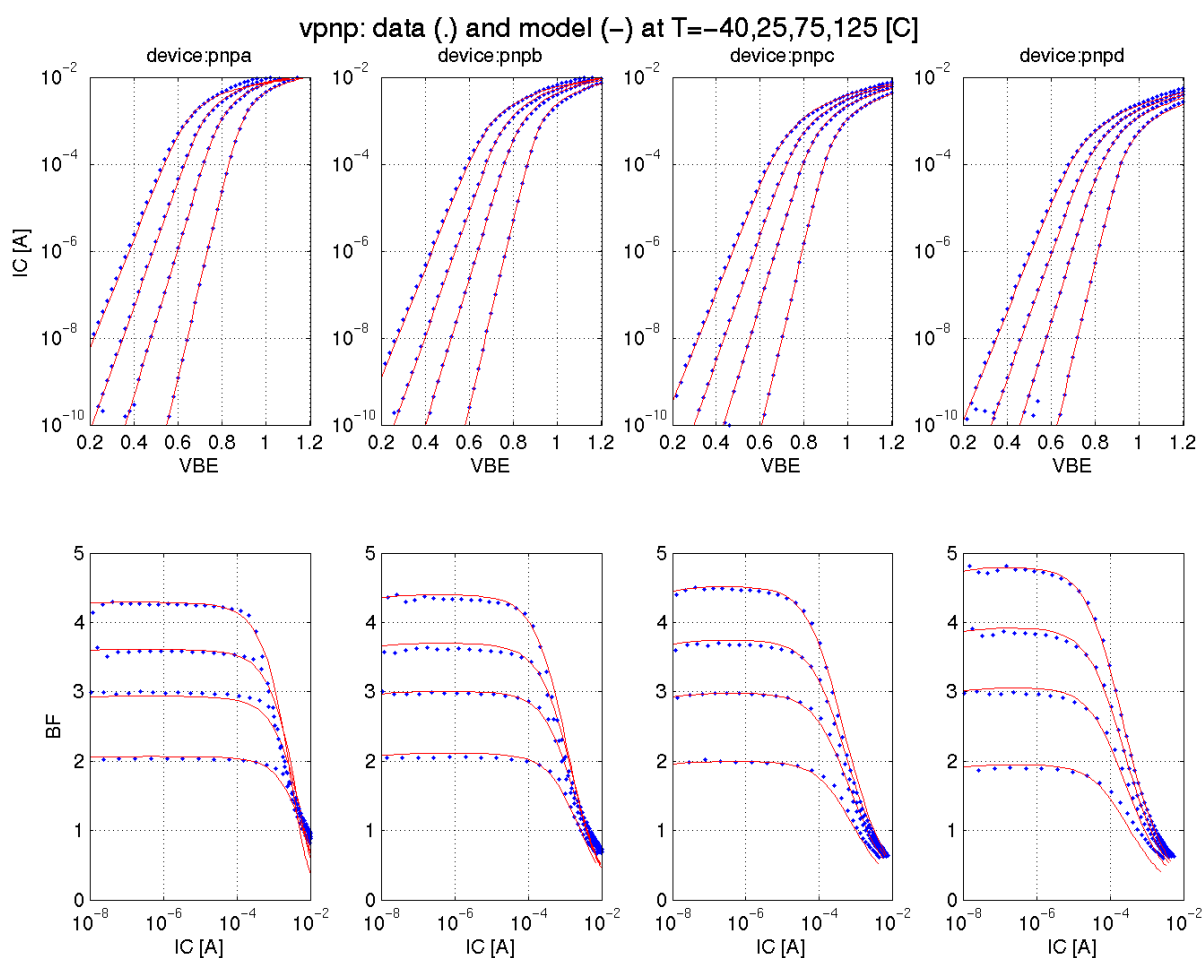
7.2.2 Model Description

The VPNP is modeled with a standard Gummel-Poon model. Four discrete model cards are extracted for the four different emitter sizes given in Table 7.4.

7.2.3 Model Verification

Figure 7.11 displays vertical PNP performance across different temperatures. The forward beta (BF) model parameter is shifted from the nominal model by -14% in order to match this measured data. This shift is within the corner specification.

FIGURE 7.11 Verification Plots for VPNP



7.2.4 VPNP Statistical and Corner Models

The primary process parameter that controls the statistical behavior of the VPNP is the Nwell doping. The current gain (β), saturation current (I_s), and Early Voltage (V_{AF}) are affected by the Nwell doping. See Section 15.0 for further explanation of the device interdependencies in the corner models and use of the X-

Sigma corner models. Table 7.5 lists the VPNP specific ESPECs compared to simulated corner and statistical values.

TABLE 7.5 Espec, Corner and Statistical model comparison for VPNP

Device	name	units	slow			nomi			fast		
			Espec	Corner	Stat	Espec	Corner	Stat	Espec	Corner	Stat
pnpa	beta (Ie=10uA)		2.5	2.51	2.49	3.5	3.5	3.49	4.5	4.5	4.5
	Va	V	100	101	107		214	220		327	332

7.2.5 VPNP Mismatch Models

Mismatch is not supported for the VPNP device.

7.3 High-performance PNP (HP-PNP)

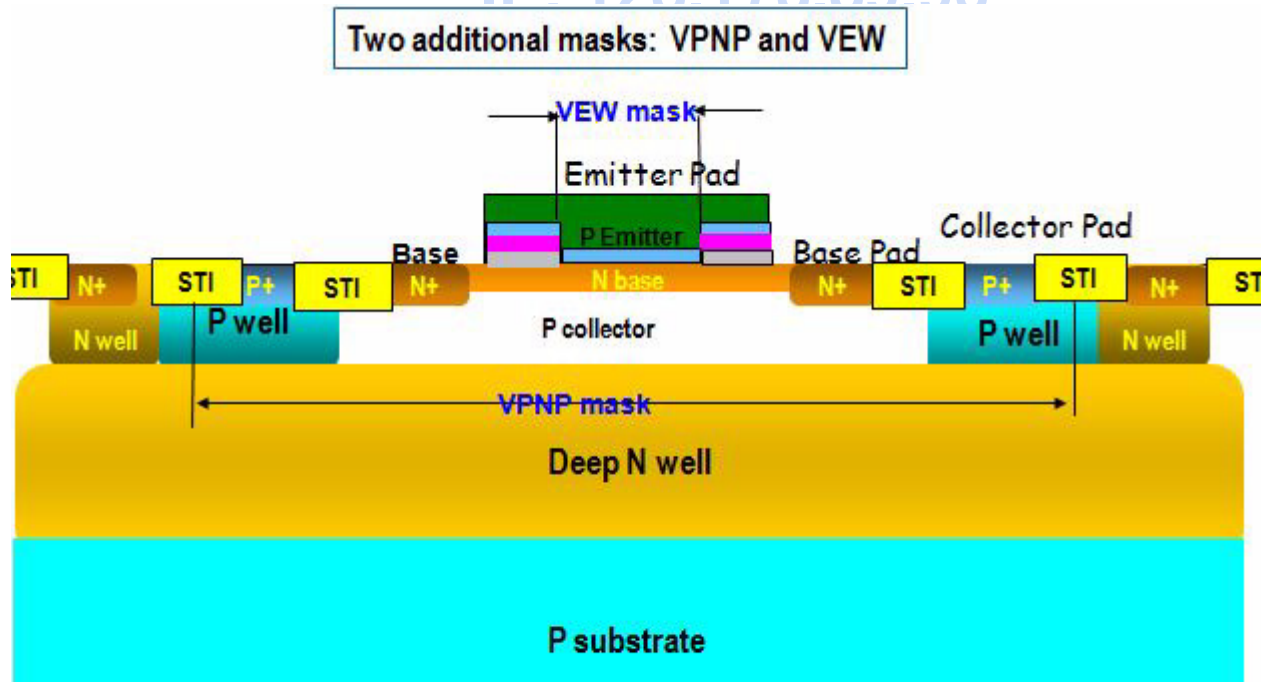
7.3.1 Device Description

A high-Ft vertical PNP device is offered in certain variants (e.g. SBC18PTD) of the SBC18 family of processes. Tables 7.6 summarizes the electrical and physical properties of the device.

TABLE 7.6 SBC18 HP-PNP Specification by BV_{CEO} (when Vec is 5 Volt) and Ft

Design Kit Name	BV _{CEO} (V)	Ft (GHz)	Beta	Emitter Width (um)	Emitter Length (um)
vpnpvp or pnpv_hp	9	16.5	45	0.8 or 2.5	Scalable from 5 -> 30

FIGURE 7.12 Cross Section of the high-performance PNP



7.3.2 Model Description

The HICUM compact model is used for the high-performance PNP device. The HICUM model was introduced to overcome the shortcomings of the SGPM (Standard Gummel-Poon Model). The name of HICUM is derived from “High Current Model”. HICUM was initially developed with special emphasis on the modeling of the high current region, very important for many high-speed applications. Compared with SGPM, HICUM is based on an extended and generalized integral charge control relationship, and approaches the transistor dynamic behaviors in a more physical way. For more detailed information about HICUM, please refer to HICUM official web page (http://www.iese.et.tu-dresden.de/iese/eb/hic_new/hic_start.html).

7.3.3 Model Verification

Model vs. measured data plots for the high-performance PNP are shown in Figures 7.13 through 7.16. The discrete symbols are the measured data, while the solid lines are the simulated data.

FIGURE 7.13 Gummel plots for emitter size $0.8 \times 10 \text{ } \mu\text{m}^2$ with 1 Emitter, 2 Bases, and 2 Collectors

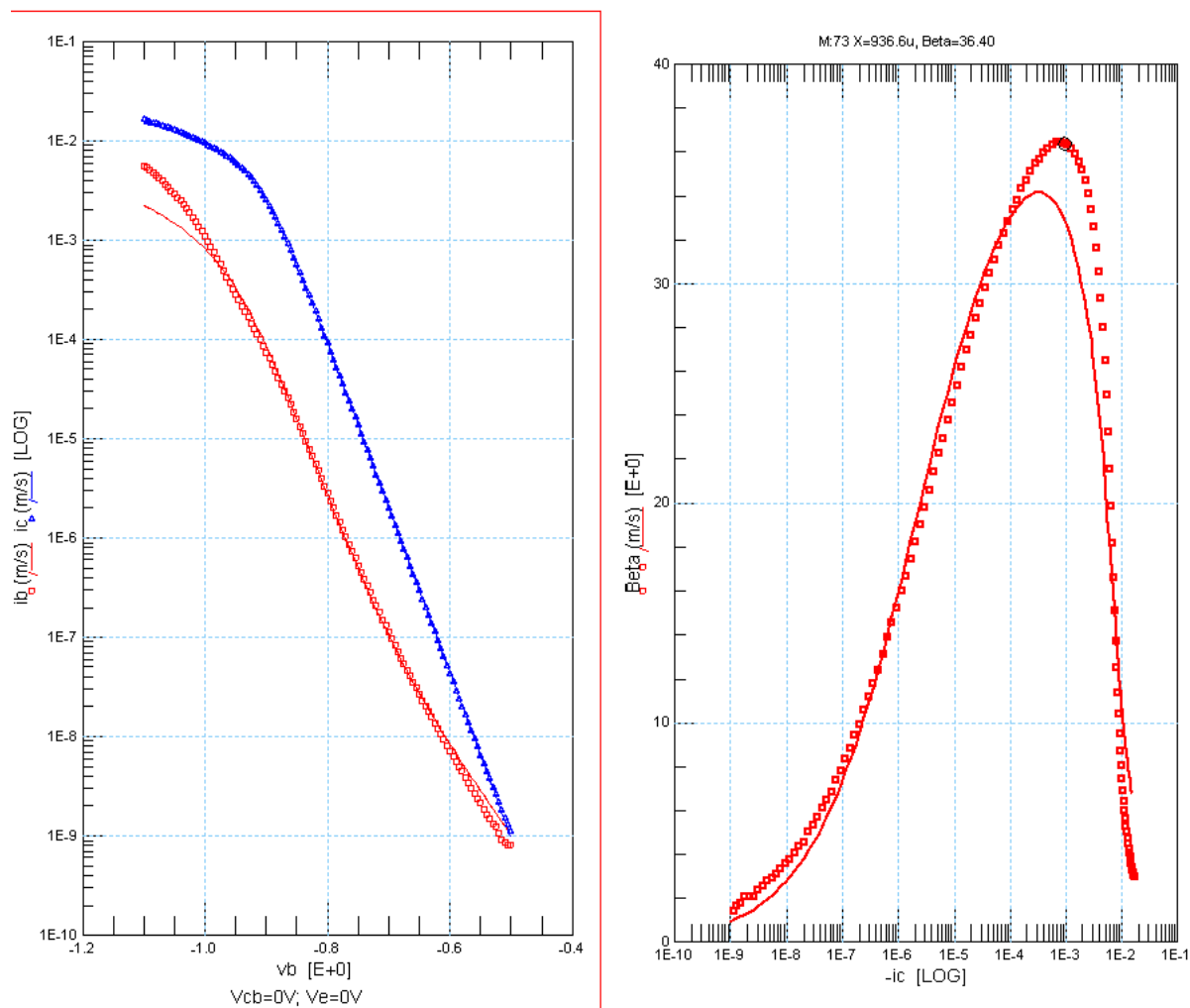


FIGURE 7.14 IC-Vce plots for emitter size $0.8 \times 10 \text{ } \mu\text{m}^2$ with 1 Emitter, 2 Bases, and 2 Collectors

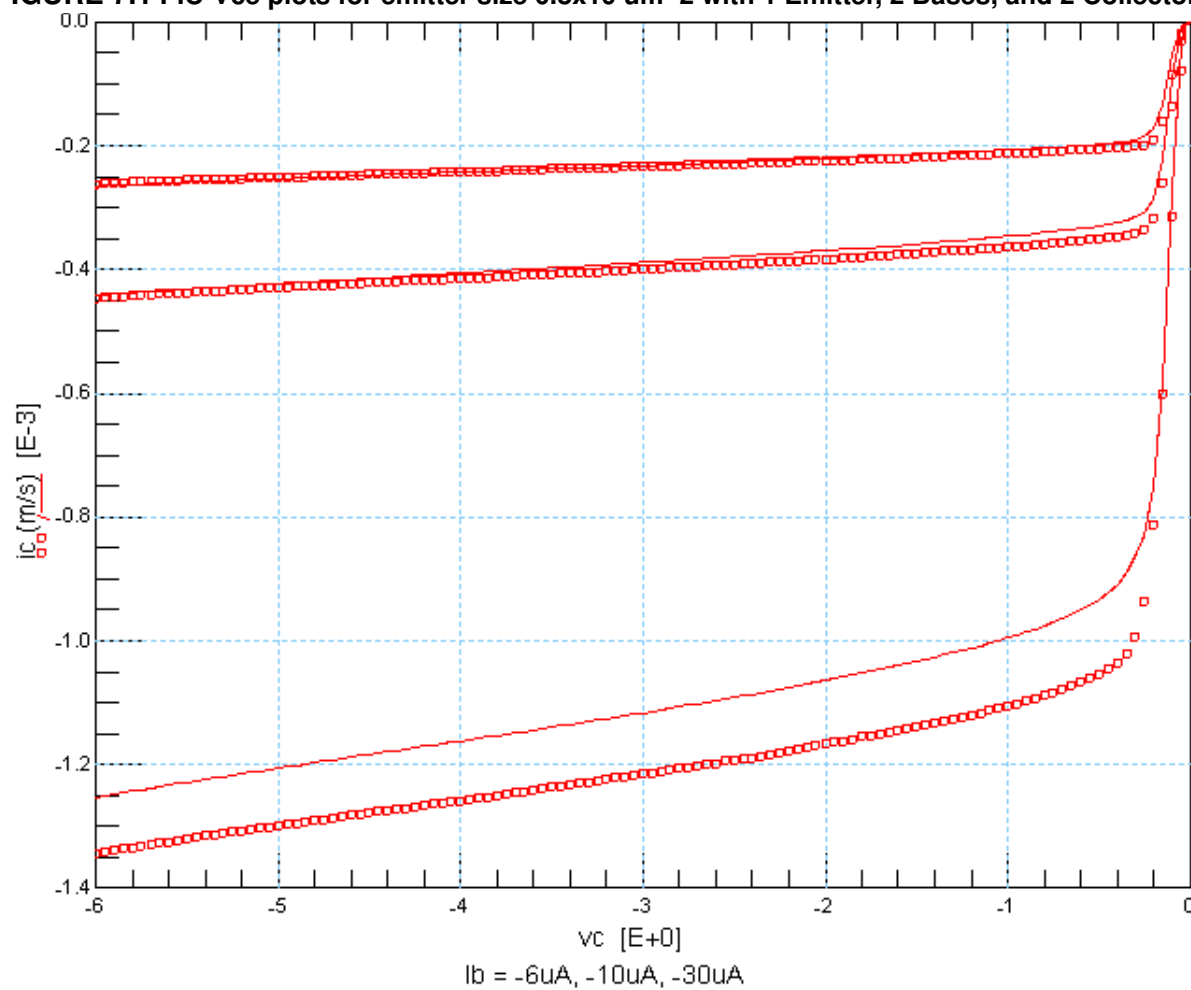


FIGURE 7.15 f_t , f_{max} Vs. I_c plots for emitter size $0.8 \times 10 \text{ } \mu\text{m}^2$ with 1 Emitter, 2 Bases, and 2 Collectors

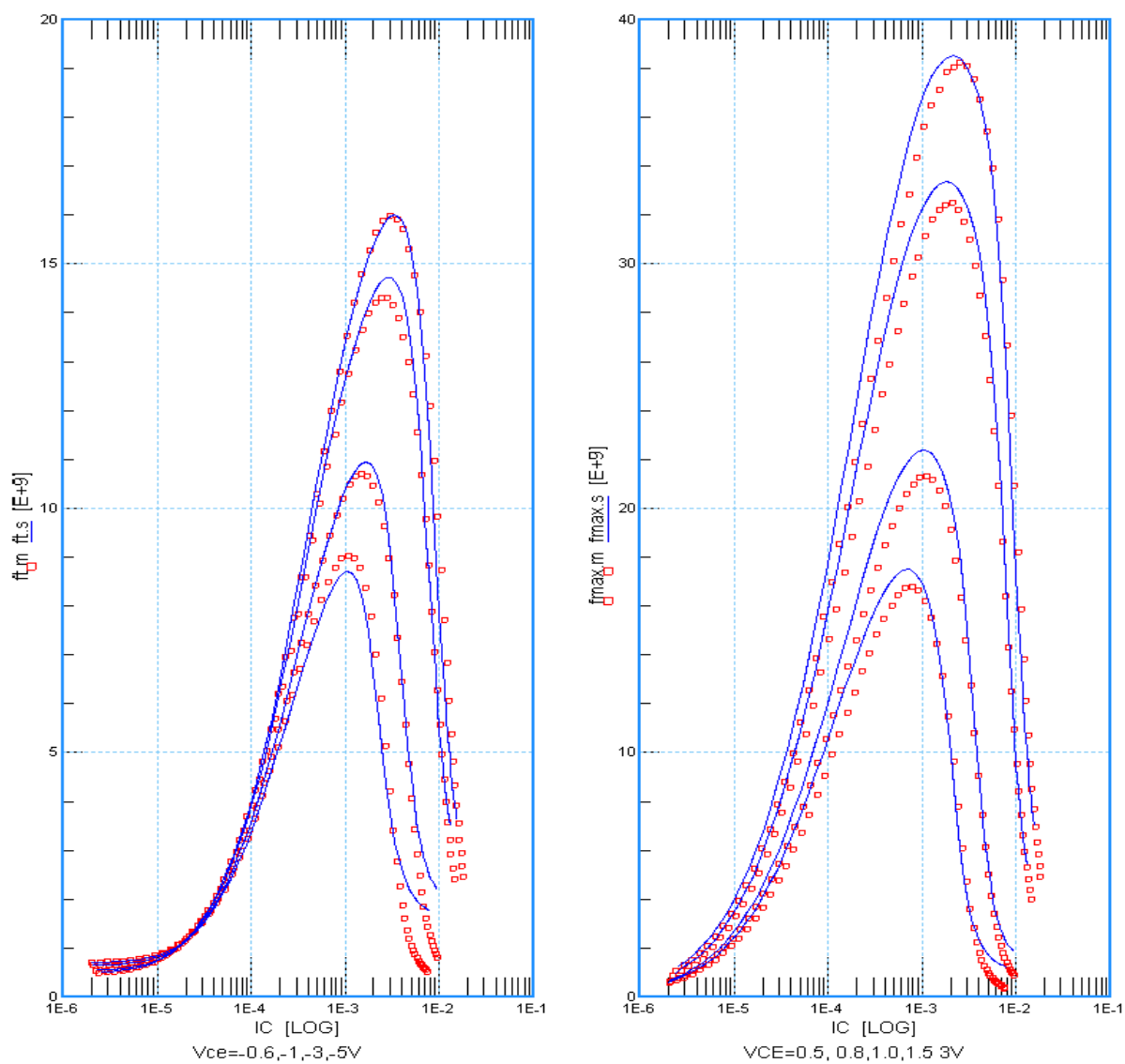
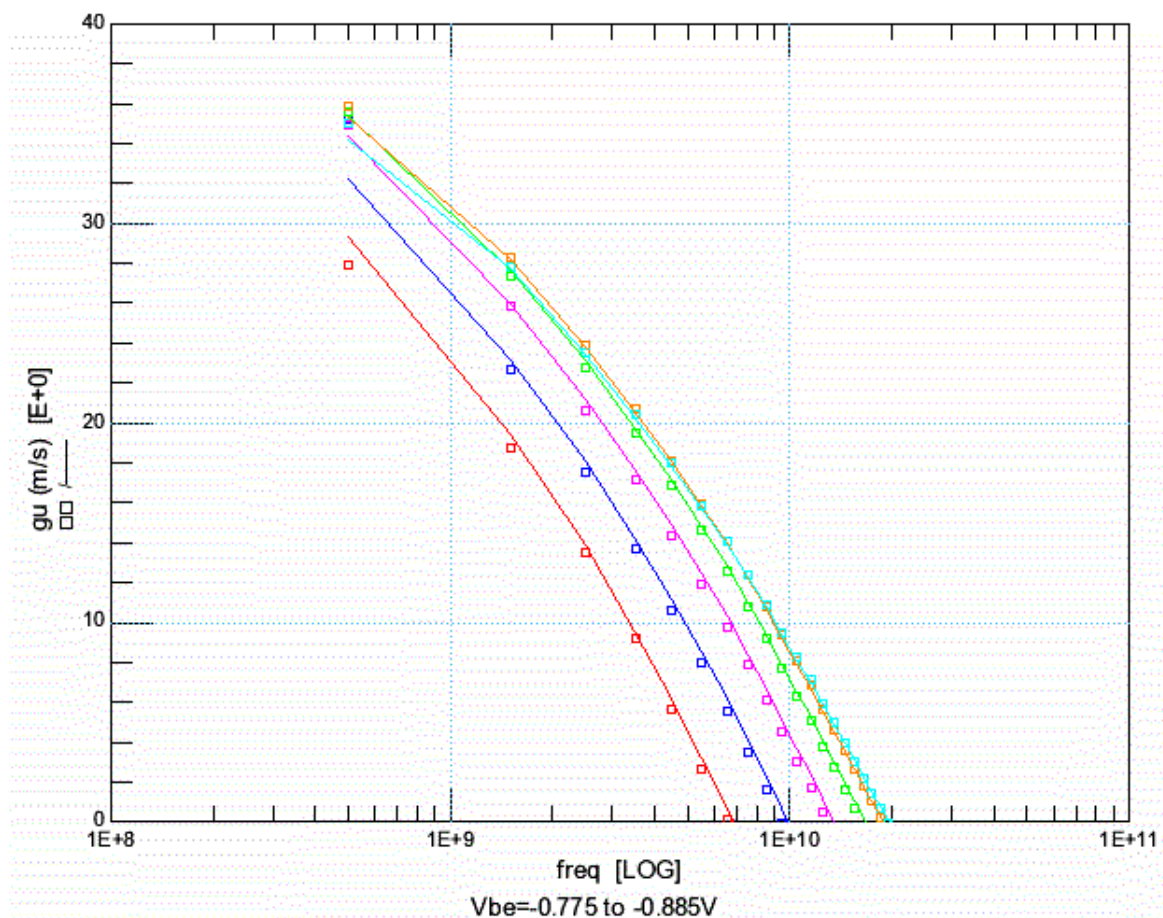


FIGURE 7.16 Unilateral power gain vs. frequency plots for emitter size 0.8x10 μm^2 with 1 Emitter, 2 Bases, and 2 Collectors



7.4 PNP Model Update History

TABLE 7.7 PNP models specific updates

Update	Devices	Reason	Impact on user
v5.0			
Adjust model to match improved emitter silicide block (SB-opening=0.8x0.8 μm^2)	LPNP	Process change improves emitter contact resistance and high current variation	Improved device performance, requires resimulation of sensitive circuits
v6.0			
X-Sigma Corner Model Support	LPNP and VPNP	Allow for process variation settings different than conventional +/- 3 sigma-corner models	Added flexibility in corner simulation
Improved temperature modeling	LPNP	More accurate modelling of temperature dependence	Improved simulation of temperature behavior.
v6.2c			
Mismatch model bug-fix for lateral pnp	LPNP (pl1g)	Bug-fix	

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8.0 Inductor Model

8.1 Device Description

The SBC18 design kit provides single-ended and differential inductors with square and octagonal spiral geometry in 2.81 μm and 5.26 μm metal processes. For single-ended inductors, the kit offers an optional ground shield drawn in silicided active. The capacitive effect of the packaging compound can be taken into account by selecting the dielectric constant of the compound through the inductor Component Description Format (CDF). An inductor instance is defined by its dimensions and can be modified through the CDF. The minimum metal width and metal space is 2.5 μm and 2.0 μm , respectively. A schematic cross section and layout snap shots of single-ended and differential inductors are shown in Figure 8.1 through Figure 8.5. The substrate ties in the cross section view are drawn for completeness of the example. Further information on substrate contacts is given in Section 8.2.6.1 on page 383.

FIGURE 8.1 Cross section view of inductor

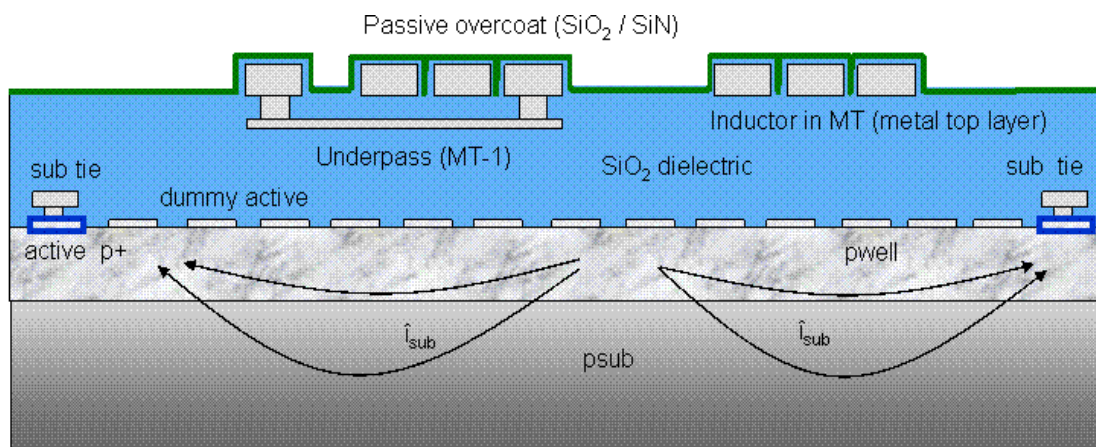


FIGURE 8.2 Square Single-Ended Inductor

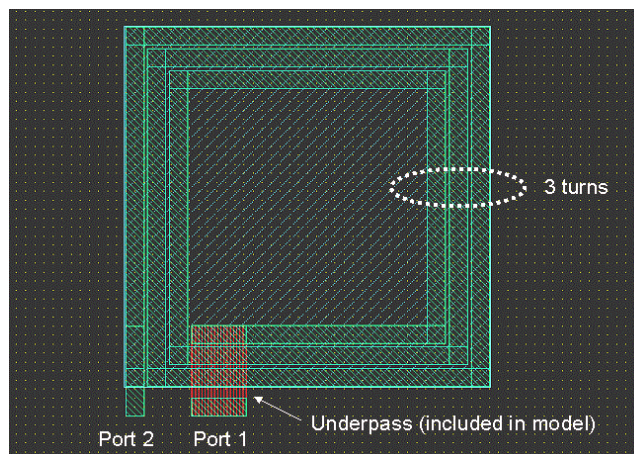


FIGURE 8.3 Square Differential Inductor

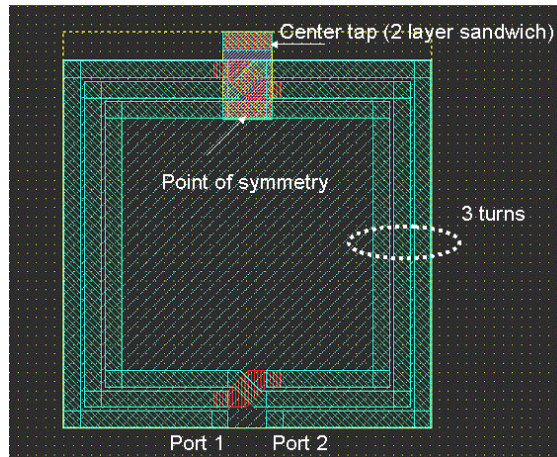
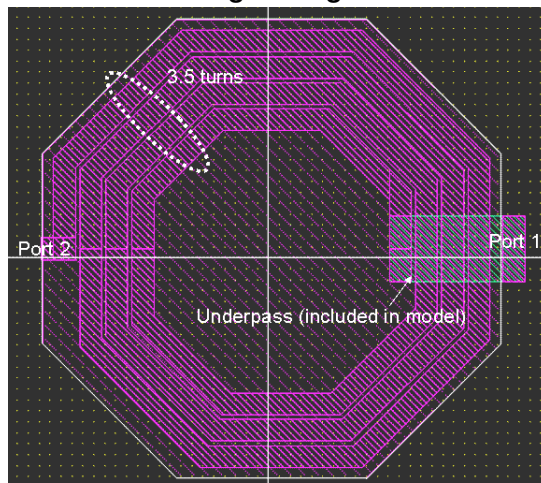
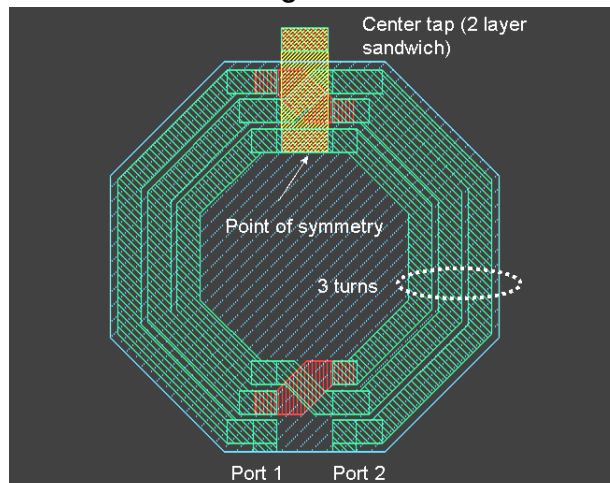


FIGURE 8.4 Octagon Single-Ended Inductor**FIGURE 8.5 Octagon Differential Inductor**

8.1.1 Inductor Layout Generator (PCELL)

The inductor layout generator creates the layout using the information entered through the CDF properties window. For singled-ended inductors, the inner end uses an underpass to connect to port 1. The underpass exit can be chosen between “straight”, “perpendicular” and “none”. In all cases the underpass is included in the inductor model. For the “none” option which does not draw an underpass, a dimension equal to the inductor line width is used to model the underpass. For options “straight” and “perpendicular” the underpass width is scaled by a factor 3. The maximum scaled width is 30 μ m, beyond which the underpass width is set equal to the inductor line width.

Differential inductors offer the choice of a center tab through the CDF property. To minimize the dc resistance, the tab width is scaled by 3 to a maximum width of 30 μ m. For line width greater 30 μ m the tab width is set equal to the inductor line width. To reduce the parasitic of the tab connection, the tab exit from the symmetric point in the core of the inductor is routed vertically down and then sandwiched in the 2 metal layers beneath the cross-over layer. In case that greater flexibility is needed in designing the tab, the layout pcell can be flattened and the tab can be customized. However it should be avoided to run the tab through the core of the inductor to avoid increasing the ac resistance and degrading quality factor Q of the inductor.

The designer must verify that the number of vias drawn at the cross-overs or underpass connections are sufficient to carry the current in the inductor. For allowable current densities please refer to the electrical specifications document. If additional vias are required, the layout pcell can be flattened and vias be added manually.

8.2 Model Description

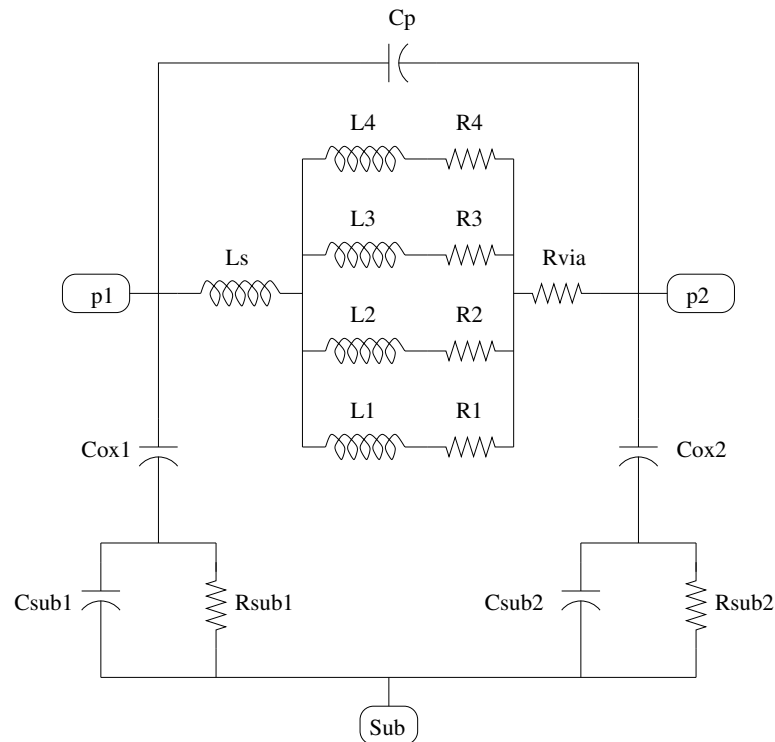
The inductor modeling within the design kit is enabled through the JAZZ Inductor ToolBox (JIT). The JIT is a matlab program which takes as inputs inductor layout parameters and produces netlist component values for

the inductor sub circuit model. The layout parameters entered through the inductor CDF in the design kit are outer dimension, line width, line space and number of turns.

8.2.1 Sub-circuit representation

The equivalent circuit representations of single-ended and differential inductors are shown in Figure 8.6 and Figure 8.7, respectively. The individual model components which are listed in Table 8.1, are based on physical models and are computed using geometrical and electrical process specification (espec) information.

FIGURE 8.6 Sub-Circuit Model for Single-Ended Inductor



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FIGURE 8.7 Sub-Circuit Model for Differential Inductor

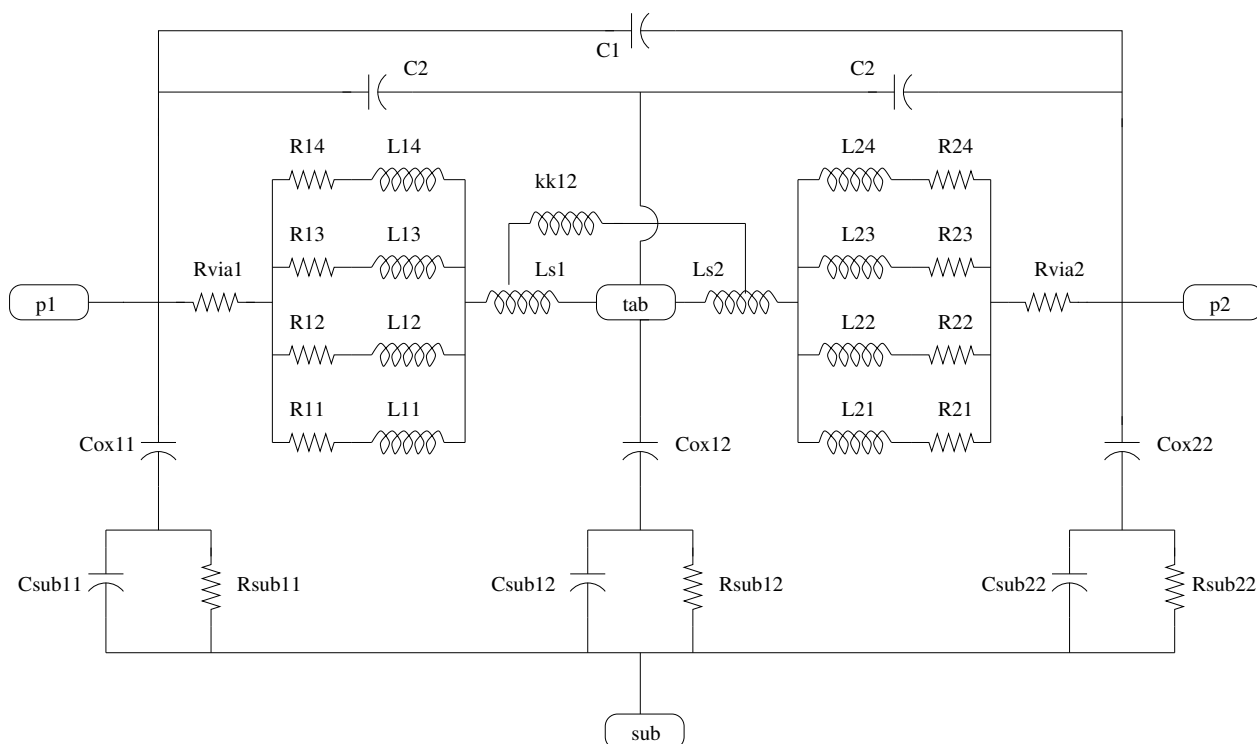


TABLE 8.1 Inductor Model Components

Component	Description
Csub	Substrate capacitance
Rsub	Substrate resistance
Cox	Oxide capacitance
Cp / C1, C2	Interwinding and cross-over capacitance
Rvia	Underpass / cross-over via resistance
Ls	Inductor series inductance
R1 - R4	Ladder resistance components (equal to R of spiral and underpass / cross-over)
L1 - L4	Ladder inductance components (circuit phase equal to phase at low frequency)
kk	Mutual inductance

The radio frequency (RF) skin effect pushes the current at higher frequencies to the surface of the metal line, effectively increasing the resistance of the inductor (AC resistance). This effect is modeled using a ladder circuit comprised of resistors and inductors that approximate the conductor as 4 concentric shells. The parallel combination of resistors in the ladder circuit resistance corresponds to the DC resistance of the inductor, while the inductance of the ladder corresponds to the internal inductance of the metal trace. This internal inductance is due to the flux linkage of the current to itself and is gradually turned off as the current conducting cross-section is restricted with increasing frequency. For this reason, a droop of the inductance from the DC value is observed on inductors that are affected by the skin effect.

Series inductance and mutual coupling are calculated using the Grover - Greenhouse formulations [1]. The ac resistance model and the series inductance describe the rising section of the Q curve and determine the peak Q value that is achievable with a particular inductor design.

The interwinding capacitance or feed forward capacitance, electrically couples the ports of the inductors. The oxide capacitance couples the inductor to the substrate. Both capacitances are significant in determining the self-resonant frequency of the inductor. Their values are calculated using a 2 dimensional interconnect solver. The packaging compound material affects primarily the interwinding capacitance whose value will increase with the dielectric constant of the material.

The substrate parasitic resistance is empirically fit to inductor RF measurements. The substrate capacitance is calculated using a simple fringing capacitance formulation. These parasitic affect the roll-off section and the shape of the Q curve.

Single-ended inductors can be drawn over active ground shield to improve the Q value. The sub circuit topology is identical to the case of un-shielded inductor in Figure 8.6. Using a ground shield lowers the substrate resistance by moving the ground return path from bulk silicon to the shield structure. The reduced ground return resistance is absorbed into the substrate resistance component, leaving the circuit topology unchanged.

8.2.2 Model selection

The inductor CDF allows for selection of geometric information of "Xsize", "Ysize", "Width", "Spacing", "Number of Turns" and information on operating frequency and frequency range. After modification of these properties, the inductor performance results and sub circuit component values for the nominal case at the nominal temperature of the circuit simulator are calculated and displayed. For proper simulation results it is necessary to include a substrate pin connected to ac ground into the schematic. The substrate pin name must be identical to the CDF parameter name defined under "Substrate Node".

For differential inductors, the center tab connection point is included in the model. Simulated results returned from the RF simulation engine and inductor performance CDF results listed in Table 8.2 must match closely.

TABLE 8.2 Inductor CDF Performance Results

Performance	Description
PeakQ / PeakqDiff	maximum Q value
FPeakQ / FPeakqDiff	frequency at Peak Q
SRF / SRFDiff	self resonance frequency
Qinterest / QinterestDiff	Q value at operating frequency
Linterest / LinterestDiff	effective inductance at operating frequency
Rinterest / RinterestDiff	effective resistance at operating frequency
Lfgoes0 / Lfgoes0Diff	effective inductance as frequency approaches zero (Ldc)
Rfgoes0 / Rfgoes0Diff	effective resistance as frequency approaches zero (Rdc)

The performance data for single ended and differential inductors are calculated differently. In single-ended configuration, the port 1 terminal at the inner end of the spiral inductor is connected to ac ground. The resulting impedance seen at the outer terminal port 2 is:

$$R + j \cdot X = \frac{1}{Y_{22}} \quad (\text{EQ 1})$$

In differential configuration, the ground connection of the equivalent circuit is assumed a virtual, floating ground and the resulting impedance from port 1 to port 2 is:

$$R + j \cdot X = Z_{11} + Z_{22} - 2 \cdot Z_{12} \quad (\text{EQ 2})$$

The reported metrics in the differential inductor CDF use the impedance from port to center tab, which is half the value from port 1 to port 2 or:

$$R + j \cdot X = \frac{1}{2} \cdot (Z_{11} + Z_{22} - 2 \cdot Z_{12}) \quad (\text{EQ 3})$$

The inductor Q, L and R as reported in the inductor CDF are calculated from the single-ended or differential impedance Z_L :

$$Q = \frac{\text{imag}(Z_L)}{\text{real}(Z_L)} \quad (\text{EQ 4})$$

$$L = \frac{\text{imag}(Z_L)}{2 \cdot \pi \cdot \text{freq}} \quad (\text{EQ 5})$$

$$R = \text{real}(Z_L) \quad (\text{EQ 6})$$

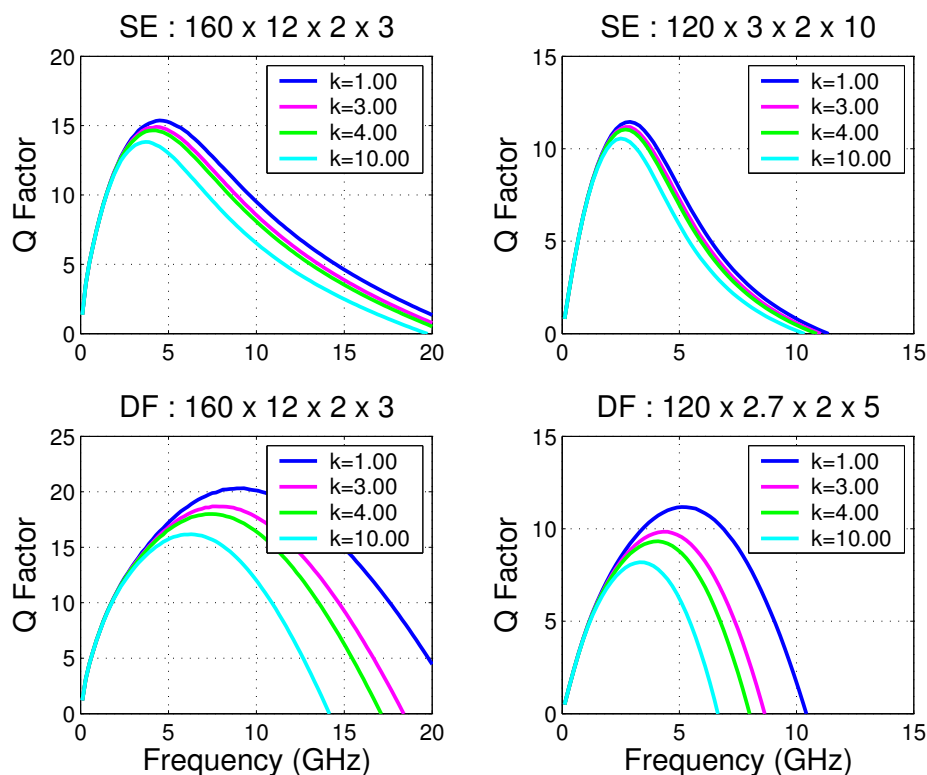
Since the parasitic capacitance of the underpass exit of the single-ended inductor is associated with the inner terminal port 1, the Q at port 2 is higher than the Q at port 1. In single-ended analysis, the admittance Y_{22} in the impedance equation is replaced by admittance Y_{21} to extract series inductance and series resistance.

8.2.3 Packaging Compound Material

The packaging compound material affects the interwinding capacitance and its value will increase with the dielectric constant of the material. Through the CDF a relative permittivity ϵ_r in the range from 1 to 10 can be entered to account for the effect of the packaging dielectric on the inductor performance. The default value is 1

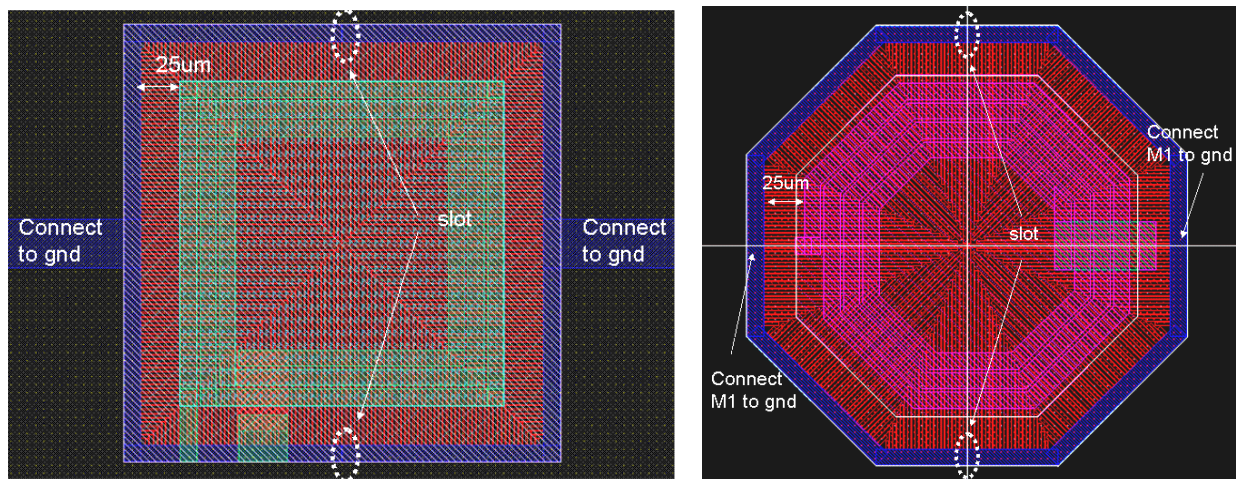
which represents air. Increasing ϵ_r will reduce the Q and self-resonant frequency of the inductor. Due to its stronger sensitivity to the interwinding capacitance, the differential inductor performance is more affected by the packaging material than the single-ended inductor. An example of the Spectre simulated Q curve on 4 inductors in the 5.26 μ m M5 process as a function of various packaging dielectric permittivity is provided with Figure 8.8.

FIGURE 8.8 Effect of Packaging Compound on Inductor Q



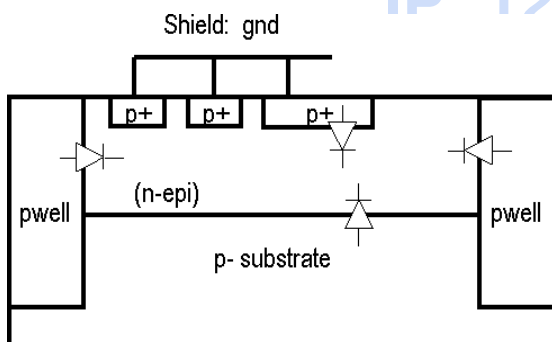
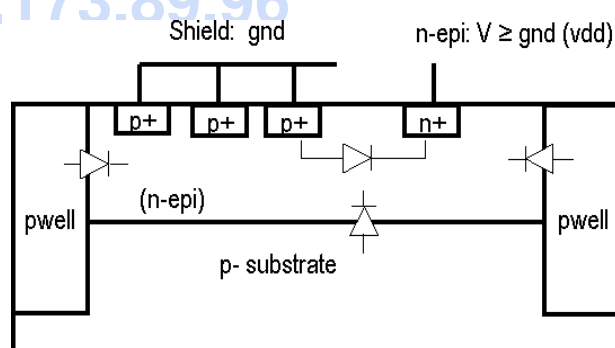
8.2.4 Ground Shield in Silicided Active

For single-ended inductors the Q performance can be boosted and noise isolation improved by inserting a ground shield below the inductor. A layout snapshot of square and octagonal inductors with shield is shown in Figure 8.9. The shield is by default 25 μ m per side larger than the inductor (outside edge of inductor to inside edge of shield metal 1). A metal 1 frame at the perimeter of the shield connects the shield fingers which are drawn in active, keeping the resistive loss over the shield small. This frame is slotted at the top and bottom to prevent a closed current loop and should be connected to ac gnd at the 2 sides of the frame segment. The connection however must not short out the slots.

FIGURE 8.9 Single-Ended Inductors with Gnd Shield

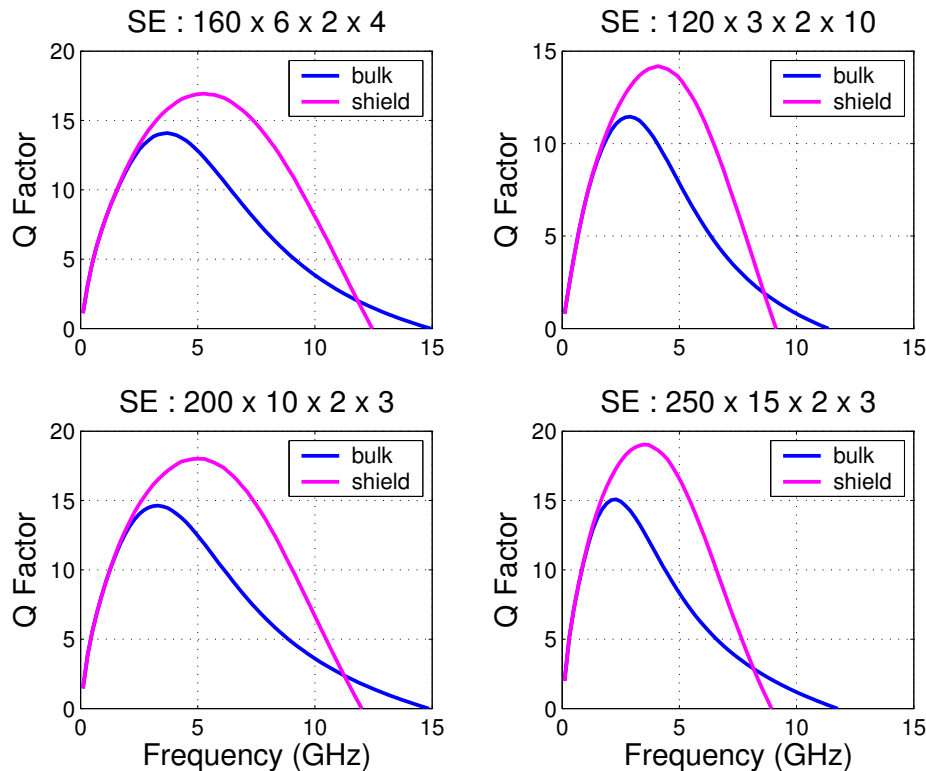
The shield fingers are drawn in silicided p+ active and are located in a n-epi layer (weak nwell). This configuration isolates the shield from the silicon substrate through a “pn”-junction. A schematic drawing of the shield and associated junctions is shown in Figure 8.10. This configuration was used for silicon model validation.

To improve noise isolation, the n-epi can be connected to vdd to minimize any diode current by keeping the “pn” –junctions zero or reverse biased as shown in Figure 8.11. The substrate noise will be shunted to ac ground reducing RF noise coupling with the neighboring area. This configuration has not been silicon validated. Not connecting the substrate, i.e. leaving it floating does not impair the function of the active shield

FIGURE 8.10 Shield Connection**FIGURE 8.11 Shield with Noise Shunt**

The ground shield structure defines an alternative current return path at a lower resistance than the return path through silicon to substrate contacts for the un-shielded case. Since the resulting substrate resistance is much lower, a very different dome-like shape Q curve is obtained, rendering the Q more broadband. The effective capacitance to the substrate is increased, approaching C_{ox} as the return path resistance decreases, reducing the self-resonant frequency. An example of the Spectre simulated Q curve on 4 inductors in the 5.26µm M5 process with and without shield is shown in Figure 8.12.

FIGURE 8.12 Effect of Shield on Inductor Q



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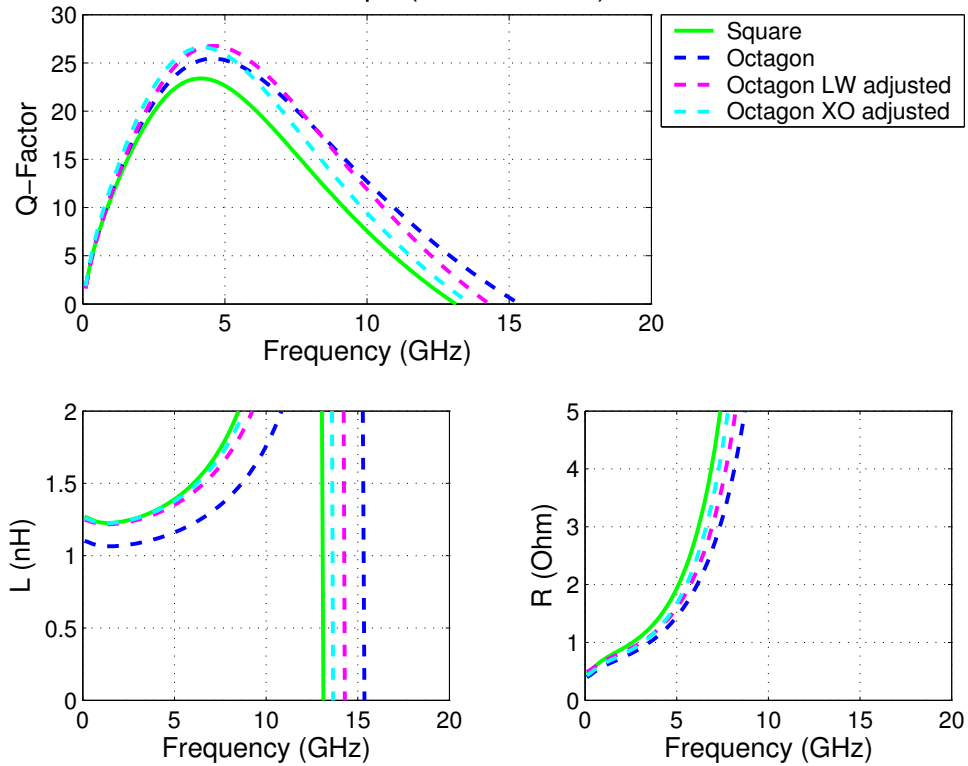
8.2.5 Octagonal Geometry

The performance of the inductor Q can be improved by using an octagonal geometry over the square geometry. When comparing a differential inductor with the same dimensions in square and octagon shape, the trace of the octagon is 20% shorter than the square leading to a higher Q and SRF with lower L and R (Figure 8.13). If the octagonal design is adjusted by reducing the line width or by increasing the outer dimension to match the same low frequency inductance and resistance as the square design, it can be seen that the octagon has an inherently better Q than the square inductor.

The differential inductor layout pcell allows a minimum of 1 turn for the octagon while the square differential requires a minimum of 2 turns. The single-ended device starts with 1.25 turns for both octagon and square layouts. A layout snapshot of minimum turn octagonal inductors is shown Figure 8.14 and Figure 8.15. The single-ended octagon is asymmetric in its layout with the lower left quadrant sides forming the “step-in” turn. A symmetric layout 1 turn single-ended device can be realized by using the 1 turn differential inductor without the center tab.

FIGURE 8.13 Q-Performance for Octagon versus Square

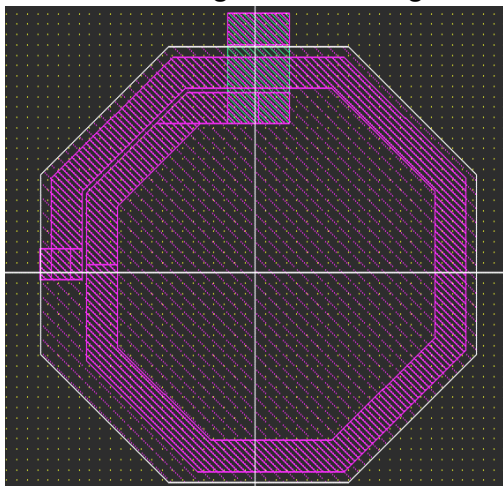
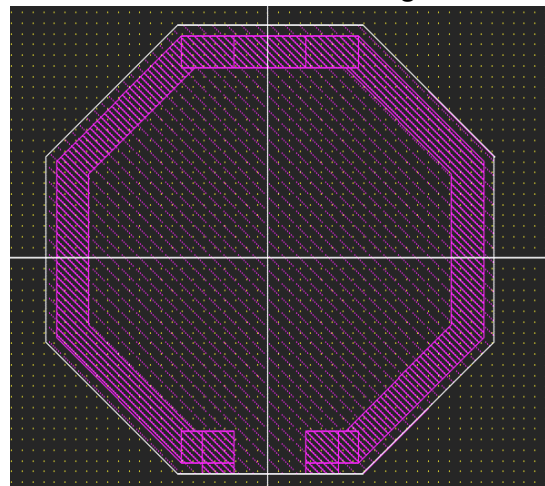
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FIGURE 8.14 Single-Ended Octagon N=1.25**FIGURE 8.15 Differential Octagon N=1**

8.2.6 Model Accuracy

8.2.6.1 Substrate Contacts

The ground-signal-ground 2-port test structure used for RF measurement on the intrinsic inductor structure, ties the silicon substrate to the equipment ground of the RF probe station and network analyzer. These substrate ties are at a distance of 75 μm - 100 μm from the inductor. To provide balanced ground return [3], the ground pads are connected between both S-parameter ports by a 100 μm wide bar in top metal which is surrounding the inductor, rendering the structure essentially into a coplanar waveguide. This configuration provides an ideal return path for the signal current to flow back through this bar to the ground probes of the port from which the signal originated. In an actual chip design this bar may not be present, but the measurement obtained on the structure with ideal return path will correspond to the intrinsic inductor as used in the design.

Substrate contacts are not included in the layout PCELL and need to be carefully considered when manually added in the vicinity to the inductor [4]. For a single-ended inductor, substrate ties within approximately 75 μm will affect the Q of the inductor. Generally an increase in Q is observed by reducing the substrate resistance. Concurrently, the effective capacitance to the substrate is increased, approaching C_{ox} in the limit of $R_{sub}=0$ (see Figure 8.6). Thus, the self resonance decreases due to the added capacitance. For differential inductors, substrate ties within 75 μm can cause asymmetry, degrading the Q [4]. In both cases the tie ring should not be a closed loop to avoid an induced current loop from lowering the inductor L through negative mutual coupling.

8.2.6.2 Inductor Q and Current Crowding

The models are verified for inductors using a line space of 2 μm and inductance values greater than 0.3 nH. Inductors with a high layout density suffer from excessive ac resistance due to the proximity or current crowding effect [5]. This effect is not included in the models and such inductors will not be modeled accurately in terms of ac resistance and Q factor. The JIT warns the user of poor inductor designs with a message prompting to reduce the layout density to below 75%. The inductor search tool that can be accessed through the inductor CDF offers a database of approximately 5000 single-ended inductors and 1800 differential inductors that are modeled well and do not exhibit the proximity effect issue.

8.2.6.3 Inductor Q Extraction

The traditional approach to Q extraction which is used for the design manual plots and for the JIT reporting in the unix background window from which the design kit was invoked, defines Q as the ratio of imaginary part of impedance to the real part of impedance

$$Q = \frac{\text{imag}(Z_L)}{\text{real}(Z_L)} \quad (\text{EQ 7})$$

This arbitrary definition has the awkward property that the Q is zero at self-resonance when the reactive terms of capacitance and inductance cancel and the impedance is purely real. In some applications when the inductor is used as a resonant tank, a more appropriate method of defining Q would be to use the 3 dB bandwidth of

impedance or the rate of change of phase of admittance when the inductor is shunted with a capacitor to resonate it at the frequency of interest [6]. The resulting admittance of inductor and shunt capacitor is

$$Y = \frac{1}{Z_L} + j \cdot \omega \cdot C_{Shunt} \quad (\text{EQ 8})$$

The shunt capacitance will resonate the device at the frequency of interest ω_0 canceling the admittance of the inductor.

$$C_{Shunt} = -\frac{\text{imag}\left(\frac{1}{Z_L}\right)}{\omega_0} \quad (\text{EQ 9})$$

For each frequency, the device is shunted to resonate. The Q at this frequency is calculated by dividing the frequency point f_0 by the 3dB frequency bandwidth of the magnitude of impedance of the shunted device.

$$Q = \frac{f_0}{\Delta f_{3dB}} \quad (\text{EQ 10})$$

Alternatively, the incremental change in phase of admittance at the frequency point f_0 can be used to calculate Q.

$$Q = \frac{f_0}{2} \cdot \left(\frac{\angle Y(f_0 + \Delta f) - \angle Y(f_0 - \Delta f)}{2 \cdot \Delta f} \right) \quad (\text{EQ 11})$$

Both methods return the same result but are fundamentally different to the result using equation [7]. These alternative methods are more computational intensive and require a finer frequency stepsize for the impedance vector to lead to a stable converged Q result. A resolution on the order of 10 MHz was found suitable and can be generated from the measurement or simulation data using cubic spline fitting. An example of shunt capacitance over frequency, tuned inductor and the Q results obtained with the different methods on measurement data of 5.26 μm M5 single-ended and differential inductors is shown in Figure 8.16 and Figure 8.17, respectively.

FIGURE 8.16 Q Methods on Single-Ended Inductor

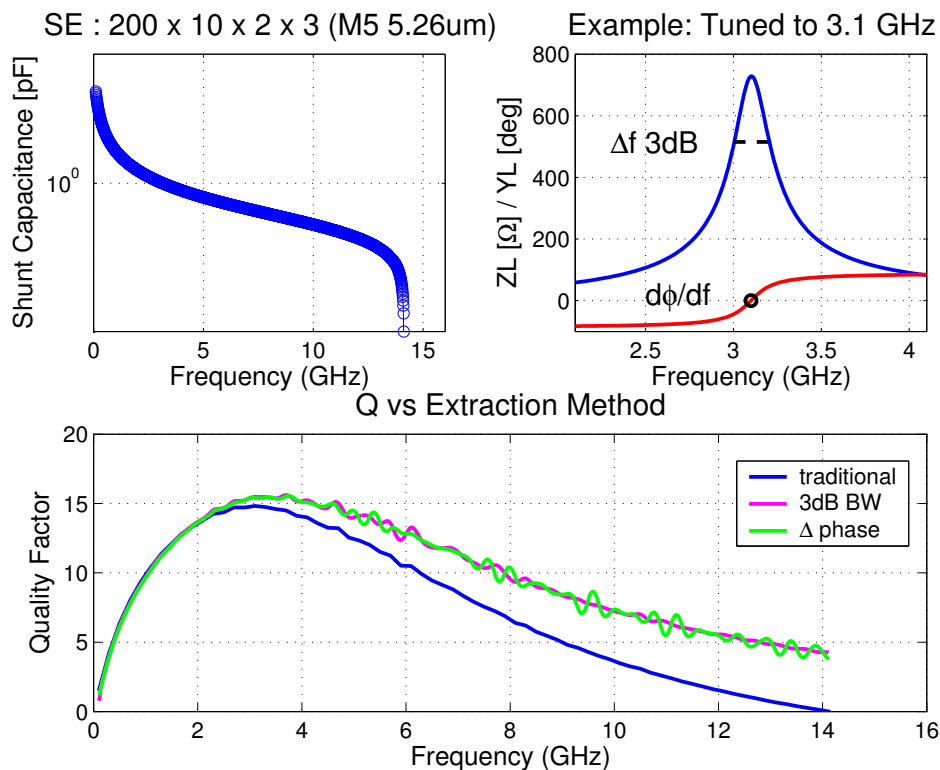
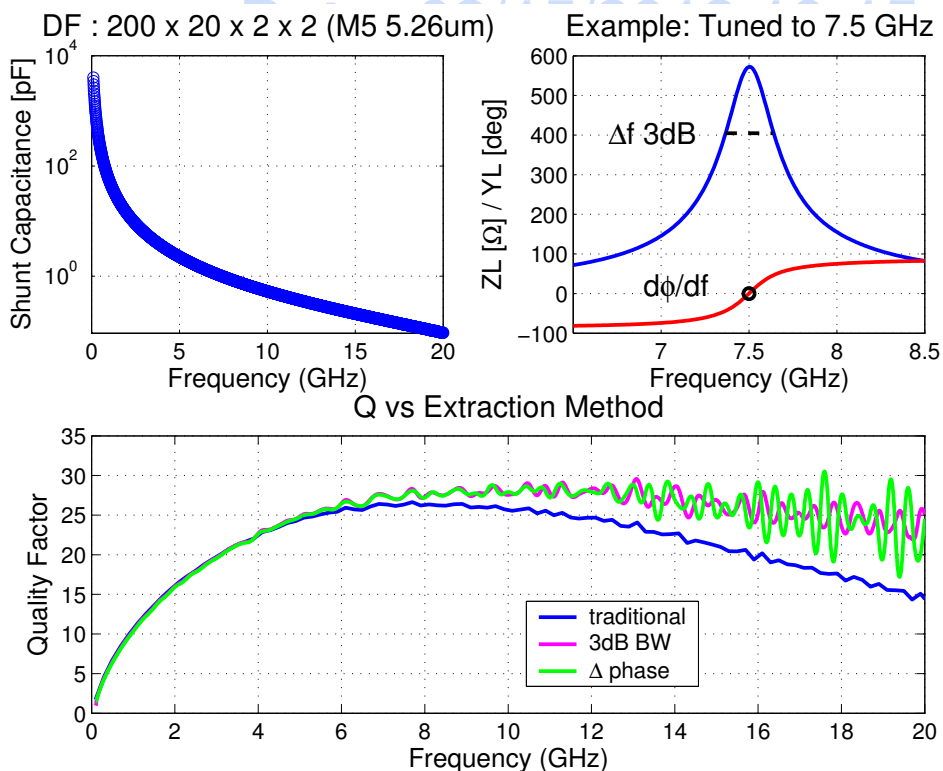


FIGURE 8.17 Q Methods on Differential Inductor

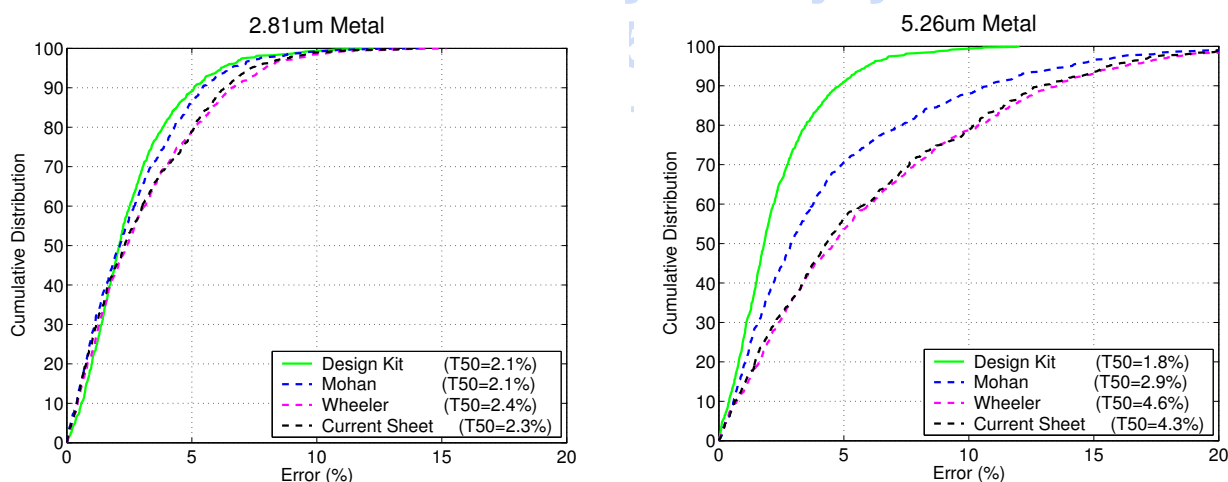


8.2.6.4 Inductance Accuracy

8.2.6.4.1 Square Geometry Inductors

Since it is difficult to obtain an accurate inductance result for the intrinsic device due to inherently small inductance on most inductor designs and contributing effects from the signal feeds, the accuracy of dc inductance was determined through comparison to electromagnetic simulations. The design kit model results on a set of 750 inductors with inductances ranging from 0.3 nH to 12 nH were bench marked against ASITIC [7] numerical simulations, similar to the study described by Mohan et.al [8]. The model inductance is calculated with the JIT using the Grover - Greenhouse equations on the inductor layout as generated by the design kit layout PCELL. ASITIC constructs and solves inductance and capacitance matrices if a low frequency, for example 1 kHz is chosen, which is the electrical analog to solving Maxwell's equation. For comparison, the inductance was also computed using Mohan's empirical equation, modified Wheeler and modified current sheet equations, all described by Mohan et.al. Figure 8.18 shows the cumulative inductance error distributions with respect to the ASITIC result for 2.81 μm and 5.26 μm metal inductors. From the cumulative error plots, a typical inductance error of 2.1% (median or T50) is obtained for 2.81 μm and 1.8% for 5.26 μm metal inductors demonstrating the accuracy of the design kit equations. The JIT results are slightly better than the alternatives provided by Mohan. The connecting feed lines to the inductor are not included in the design kit model and need to be accounted for separately by inductance extraction on the actual layout.

FIGURE 8.18 Cumulative error of dc inductance



8.2.6.4.2 Octagonal Geometry Inductors

The accuracy of the inductance models for octagonal single-ended and differential inductors were bench-marked against MIT's FastHenry [9]. FastHenry is a three-dimensional inductance extraction program that

computes the frequency dependent self and mutual inductances and resistances between conductors of complex shape.

The difference of the inductance result between design kit model and FastHenry is shown on a large set of 4455 octagonal single-ended inductors and 1485 octagonal differential inductors in 2.81 μm and 5.26 μm metal processes with Figure 8.19 and Figure 8.20. The geometry space covered by the histograms ranges from 3 to 35 μm line width, 2 to 10 μm line space and 1 to 9 turns. The JIT results are well within 2% of the FastHenry result. The connecting feed lines to the inductor are not included in the design kit model and need to be accounted for separately by inductance extraction on the actual layout.

FIGURE 8.19 Inductance Calculation Accuracy (Octagonal Single-Ended Inductor)

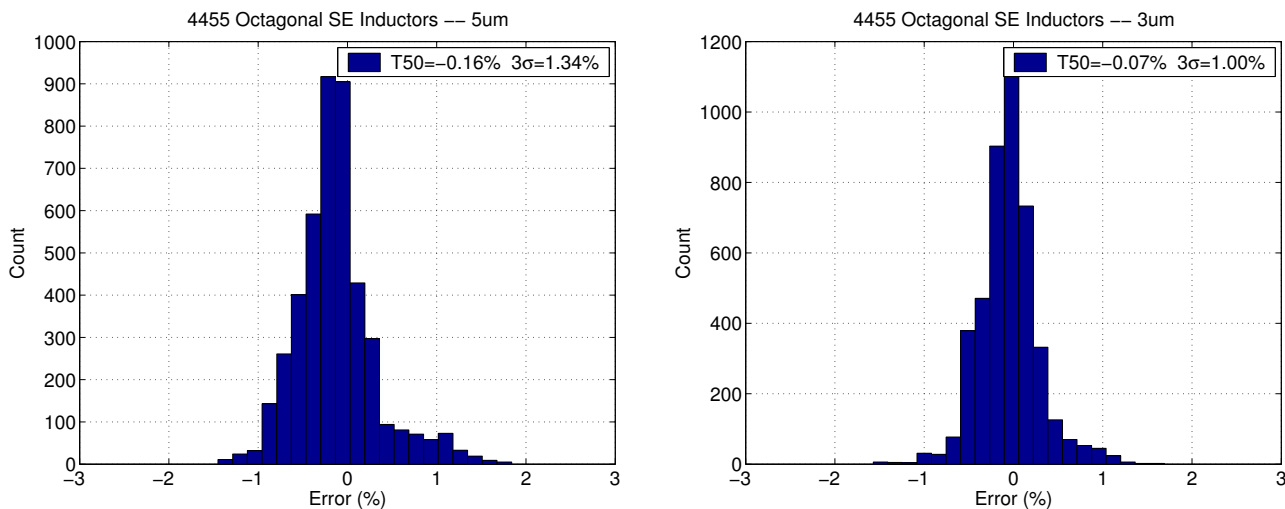
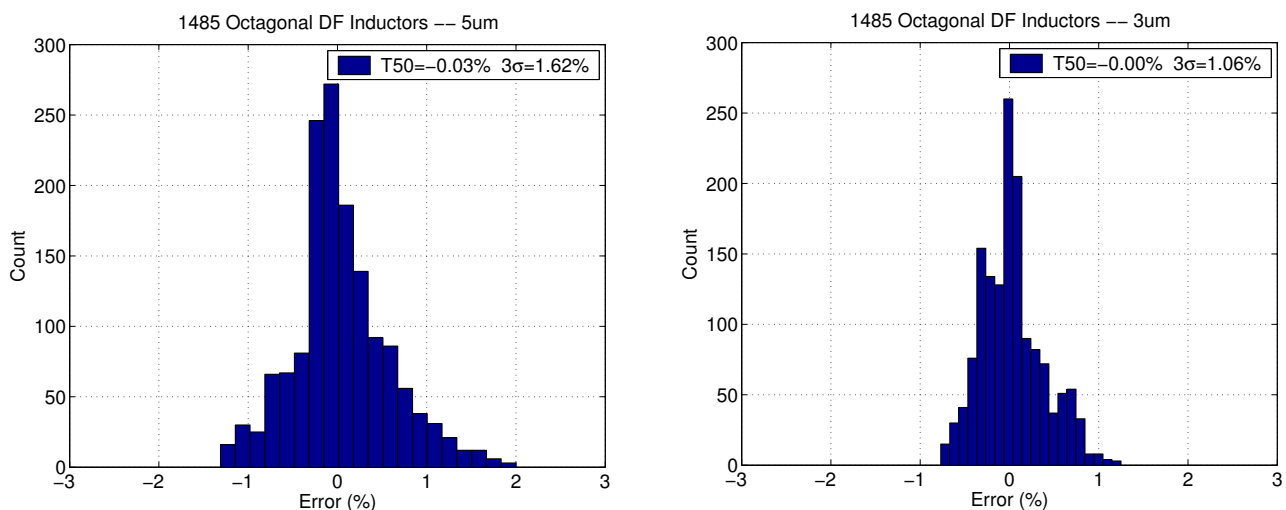


FIGURE 8.20 Inductance Calculation Accuracy (Octagonal Differential Inductor)



8.3 Model Verification

8.3.1 Silicon Validation

The inductor models have been verified by comparing measured high frequency characteristics at 25°C temperature with the Spectre simulation on the corresponding intrinsic device. Since the inductor verification in silicon requires the use of ground-signal-ground pads and feed lines to connect the device, the measurement results are afflicted with considerable parasitic capacitances, inductances and resistances. These parasitic effects were removed from the measured data to yield the intrinsic device by subtracting the pad admittance followed by an ABCD matrix multiplication to remove the feed lines. Any deembedding approach is imperfect and the result will only be the approximate true device. Substrate contacts are located in the ground-signal-ground test fixture which is generally at a distance of 75µm to 100µm to the inductor. Examples of Spectre simulated and measured Q, L, R results for various single-ended inductors over silicon substrate and over shield and for square and octagonal differential inductors over bulk silicon are shown in subsequent Figure 8.21 through Figure 8.99. Each figure groups 3 inductor designs in 2.81 µm metal 6, 5.26 µm metal 5 and 5.26 µm metal 4. The title describes the inductor type with “SE” for single-ended or “DF” for differential inductor and indicates in parentheses where a shield was used and whether square or octagonal layout for the differential inductors. The geometry information is following the inductor type information in sequence of outer dimension, line width, line space and turns. The specific process and JIT information is marked in the legend.

FIGURE 8.21 Inductor Model Verification

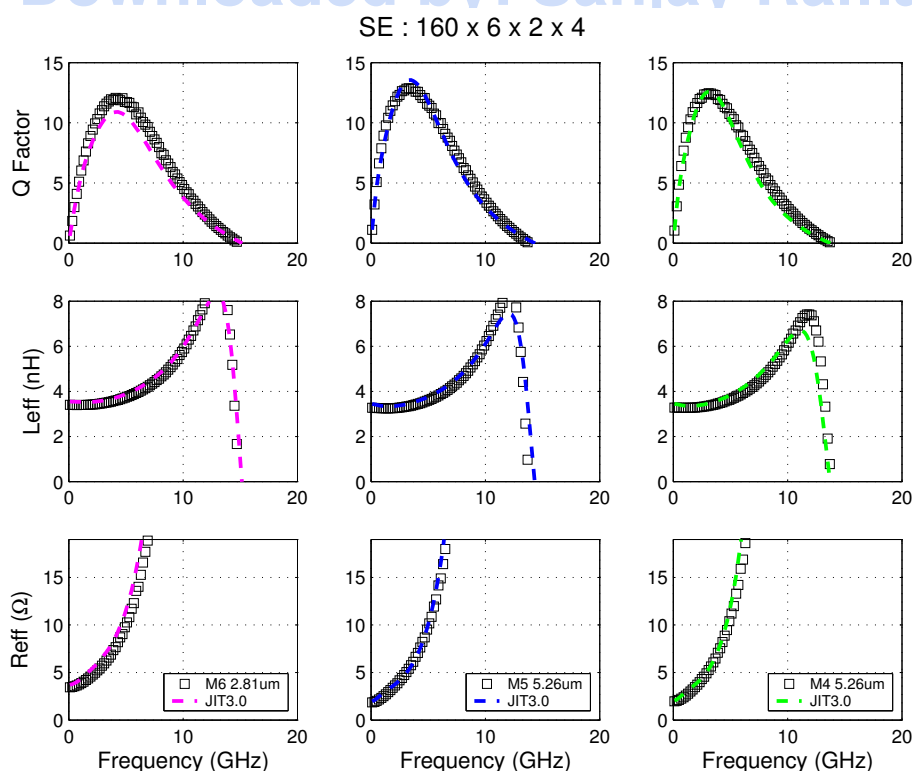


FIGURE 8.22 Inductor Model Verification

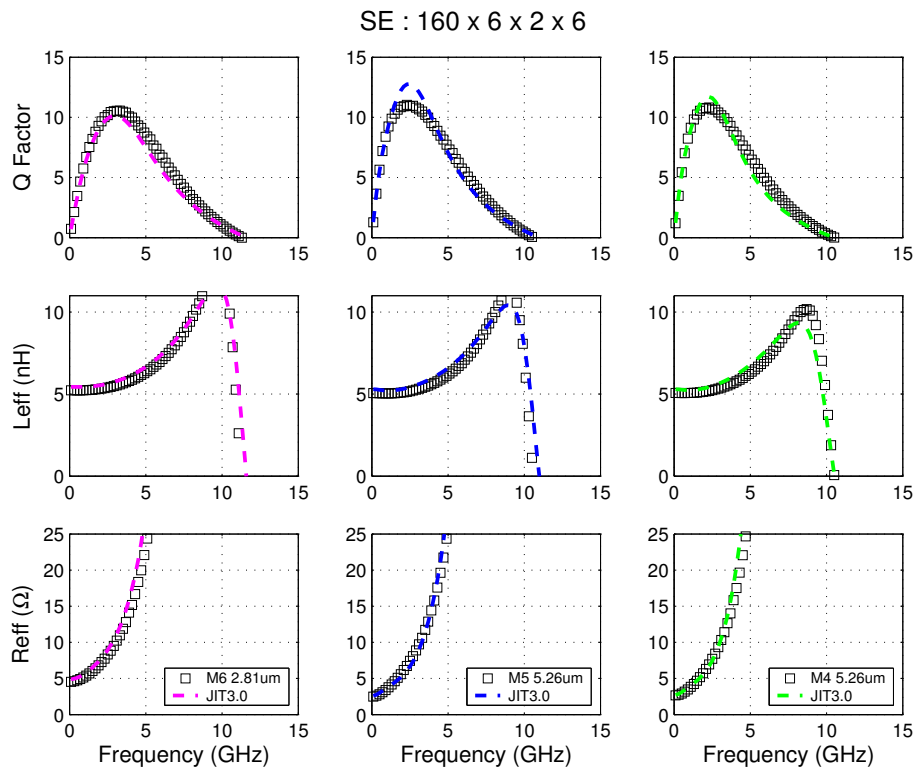


FIGURE 8.23 Inductor Model Verification

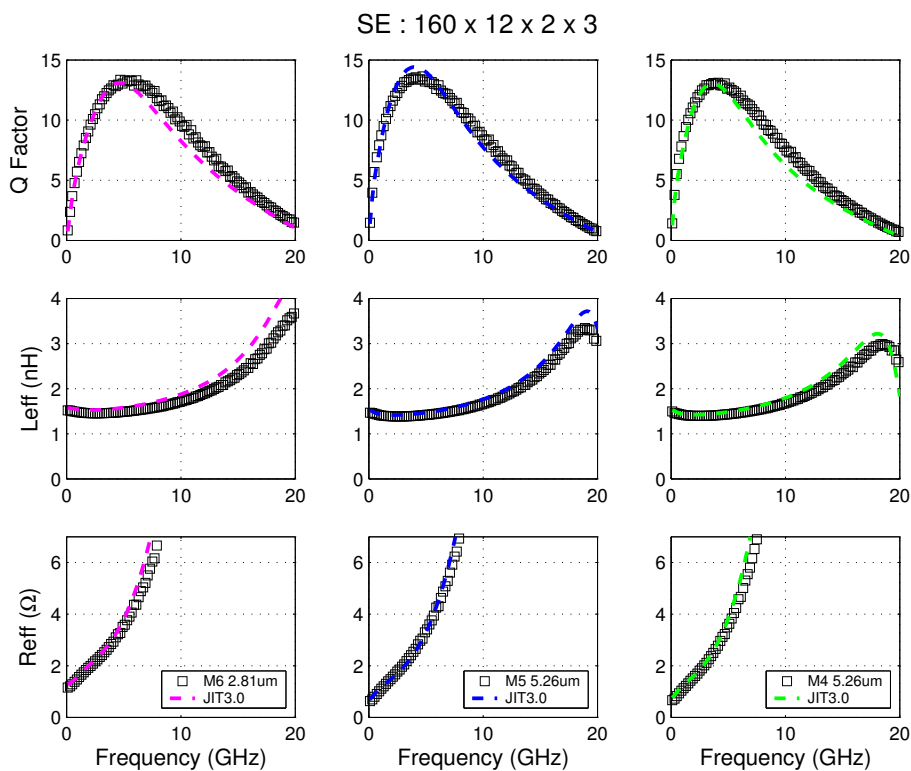


FIGURE 8.24 Inductor Model Verification

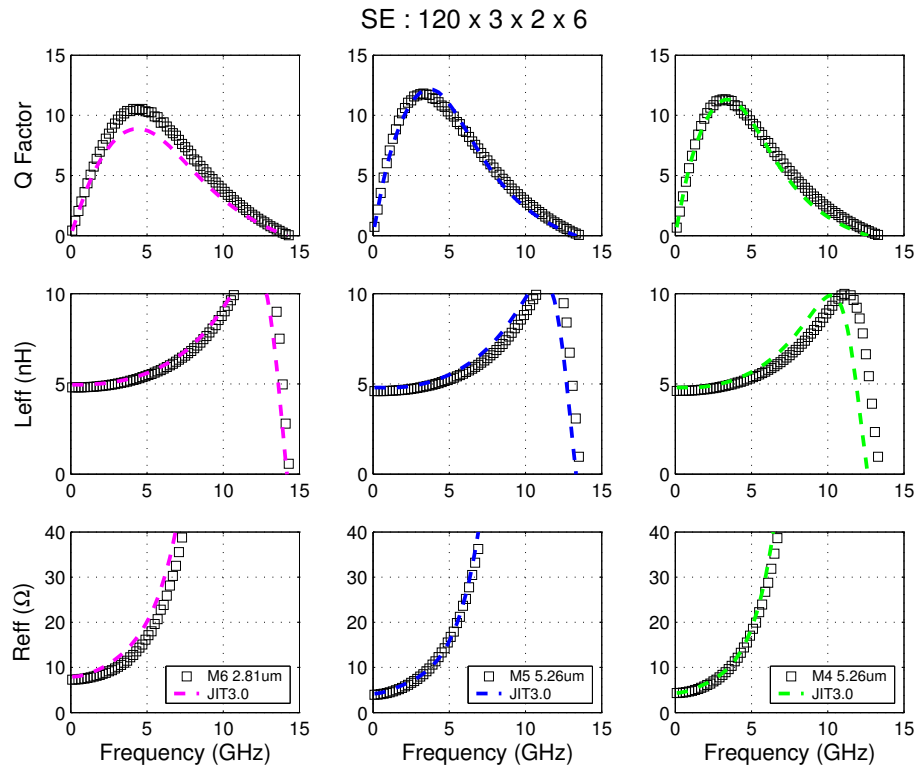


FIGURE 8.25 Inductor Model Verification

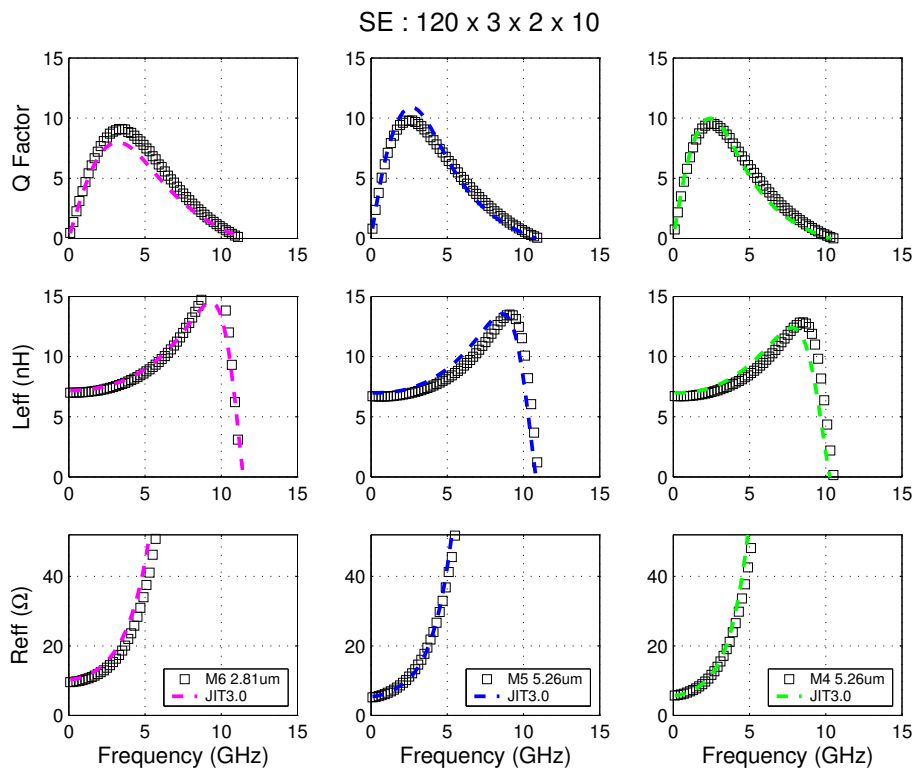


FIGURE 8.26 Inductor Model Verification

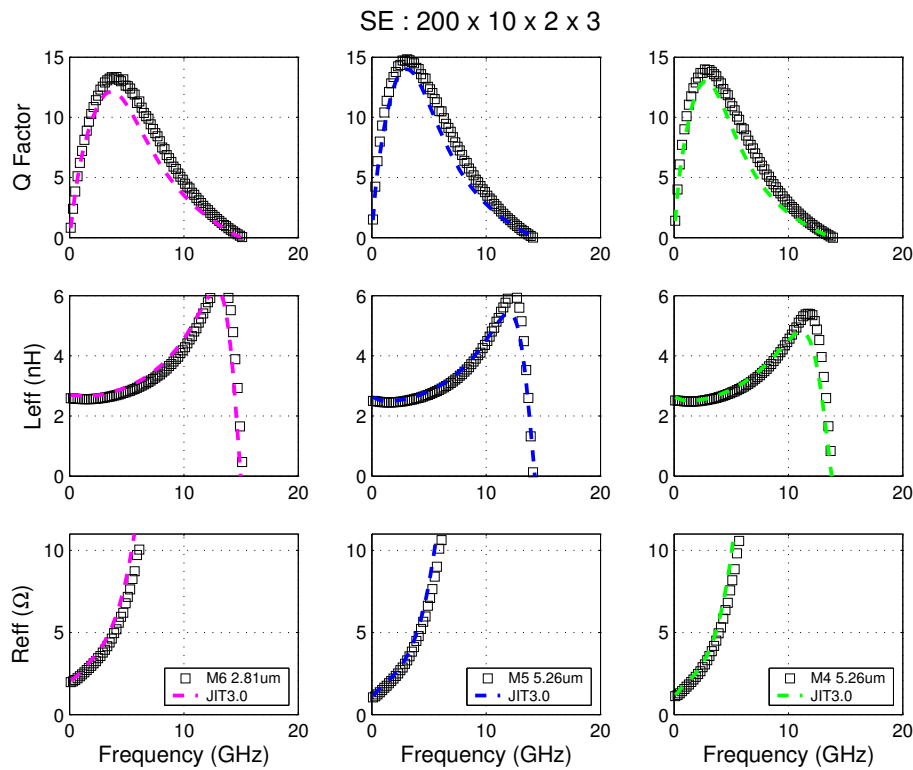


FIGURE 8.27 Inductor Model Verification

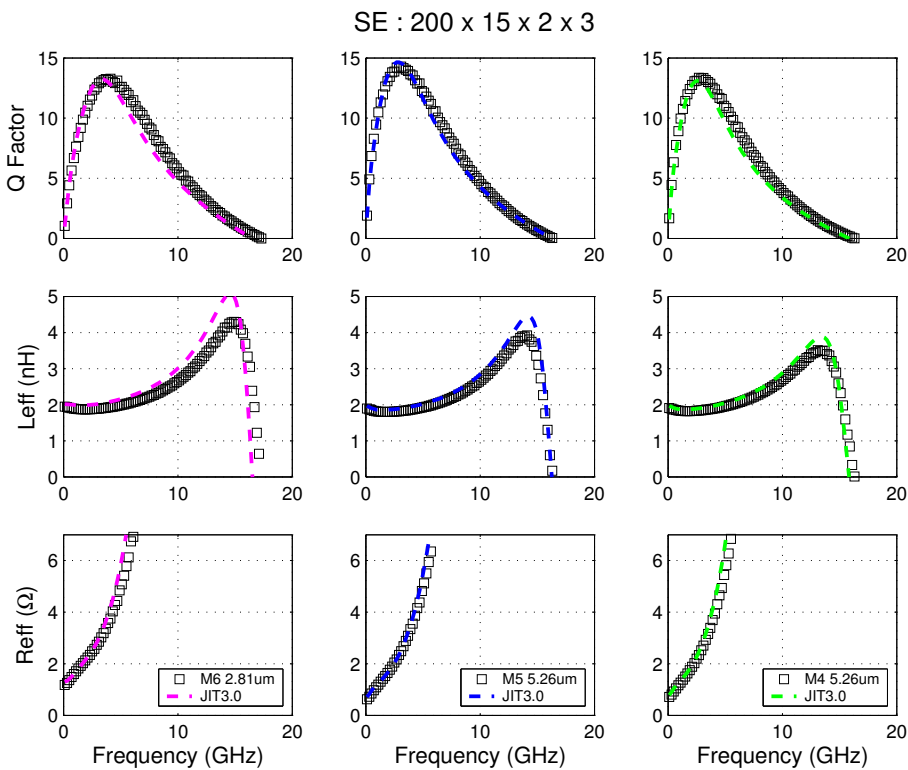


FIGURE 8.28 Inductor Model Verification

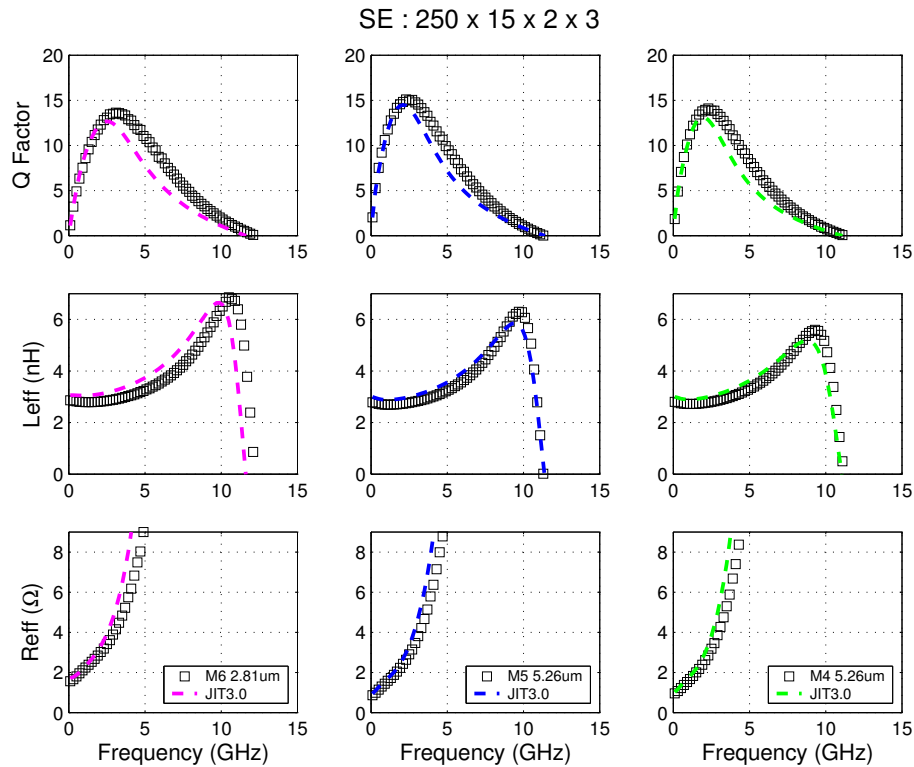


FIGURE 8.29 Inductor Model Verification

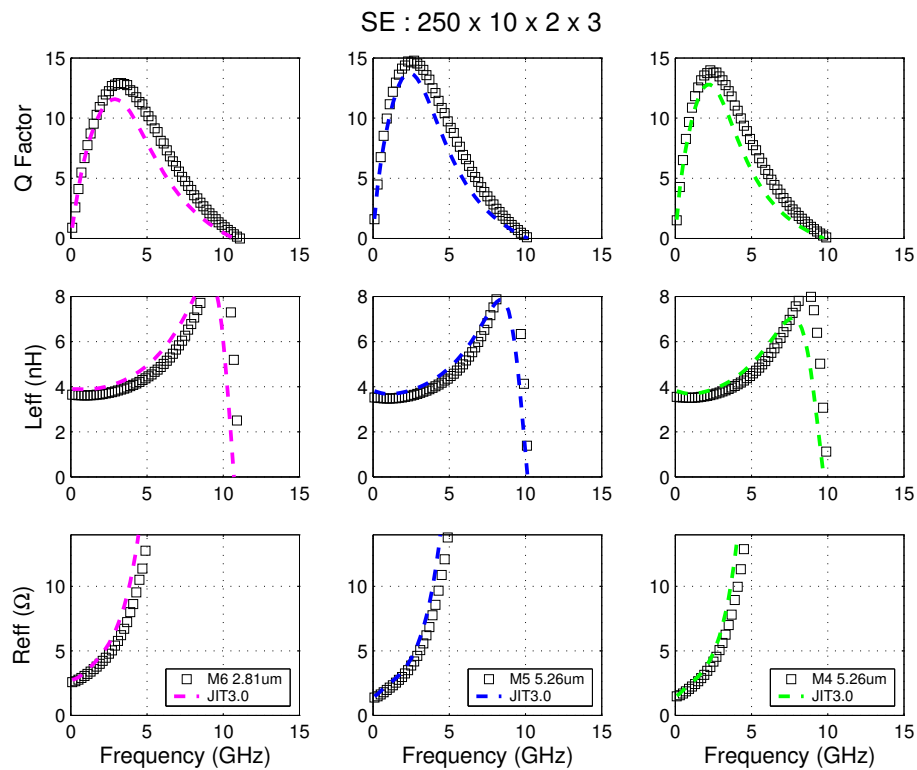


FIGURE 8.30 Inductor Model Verification

SE : 160 x 6 x 2 x 4 (shield)

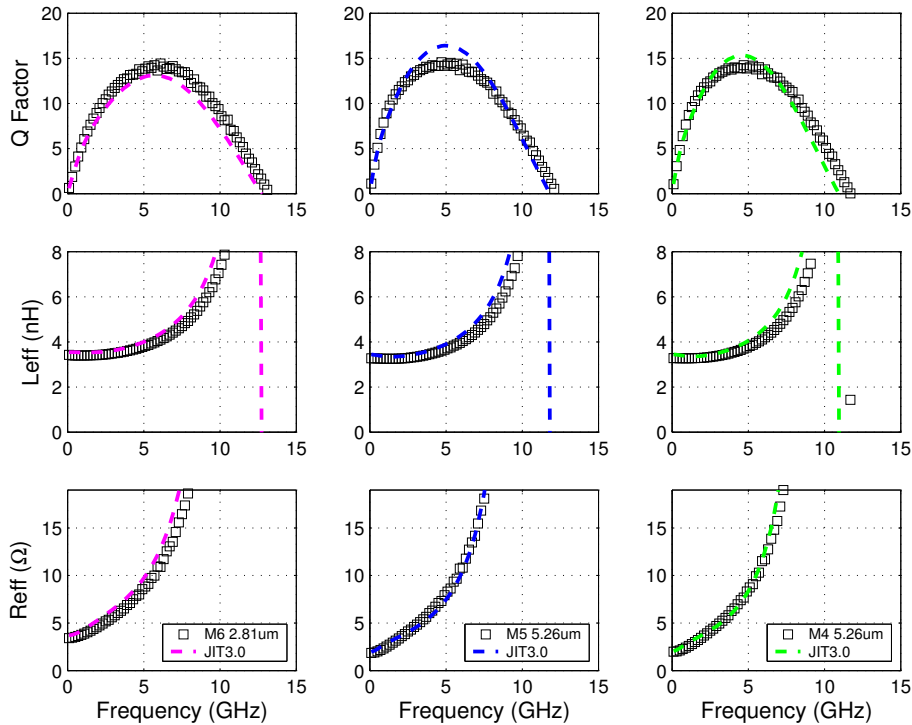


FIGURE 8.31 Inductor Model Verification

SE : 160 x 6 x 2 x 6 (shield)

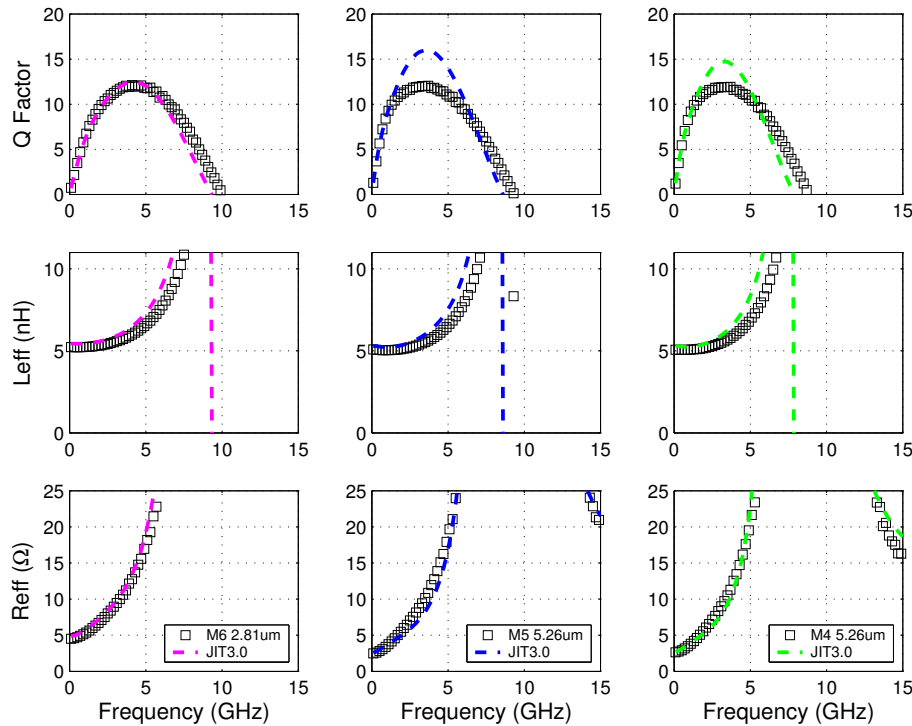


FIGURE 8.32 Inductor Model Verification

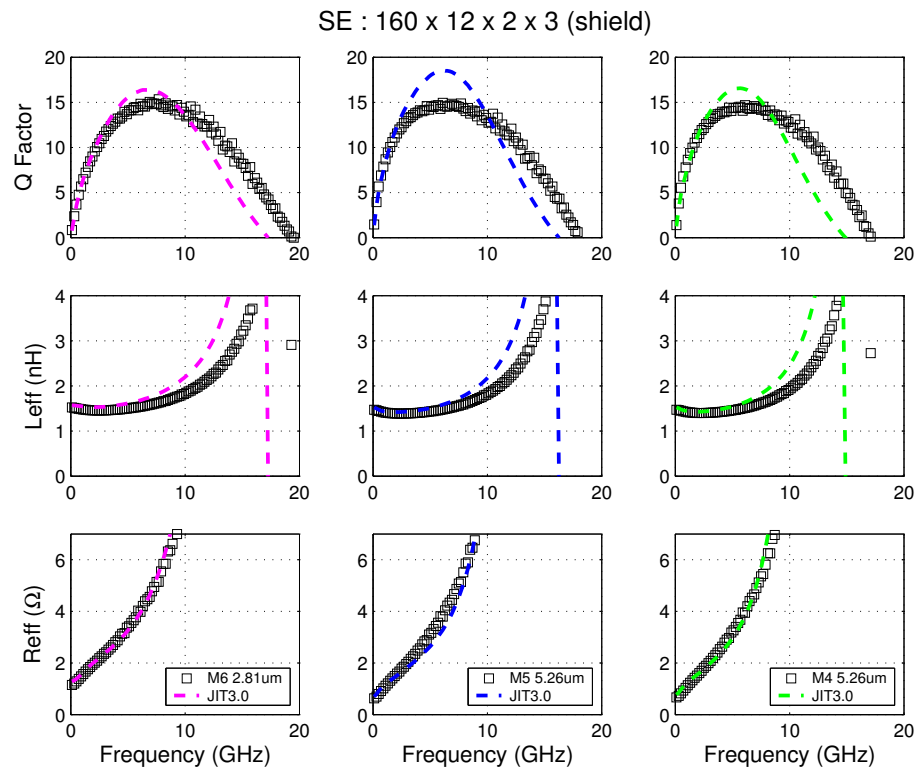


FIGURE 8.33 Inductor Model Verification

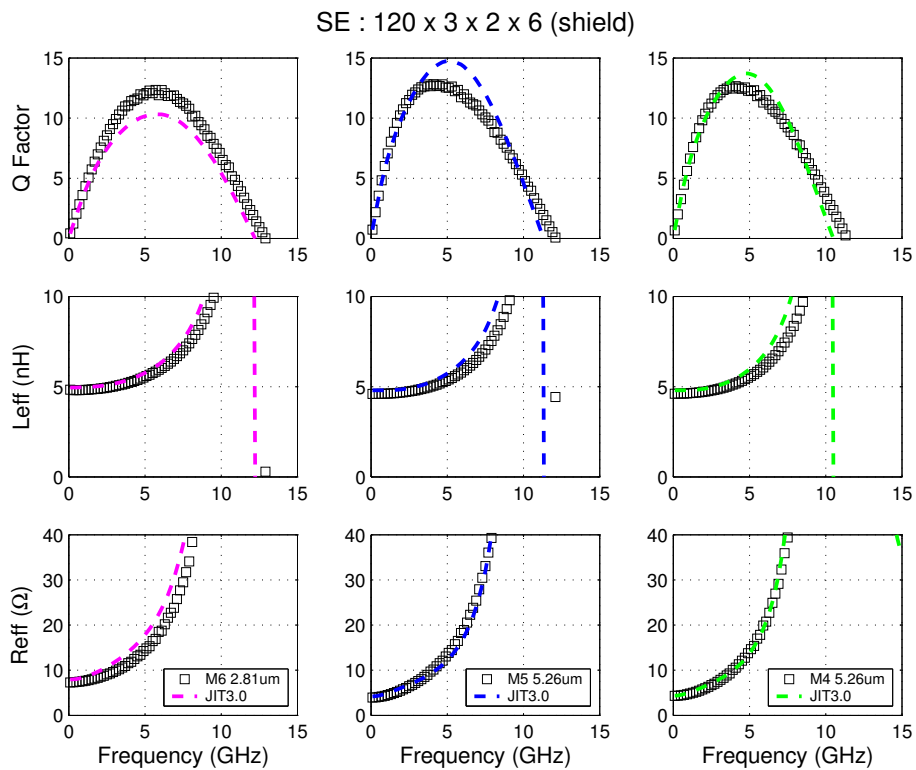


FIGURE 8.34 Inductor Model Verification

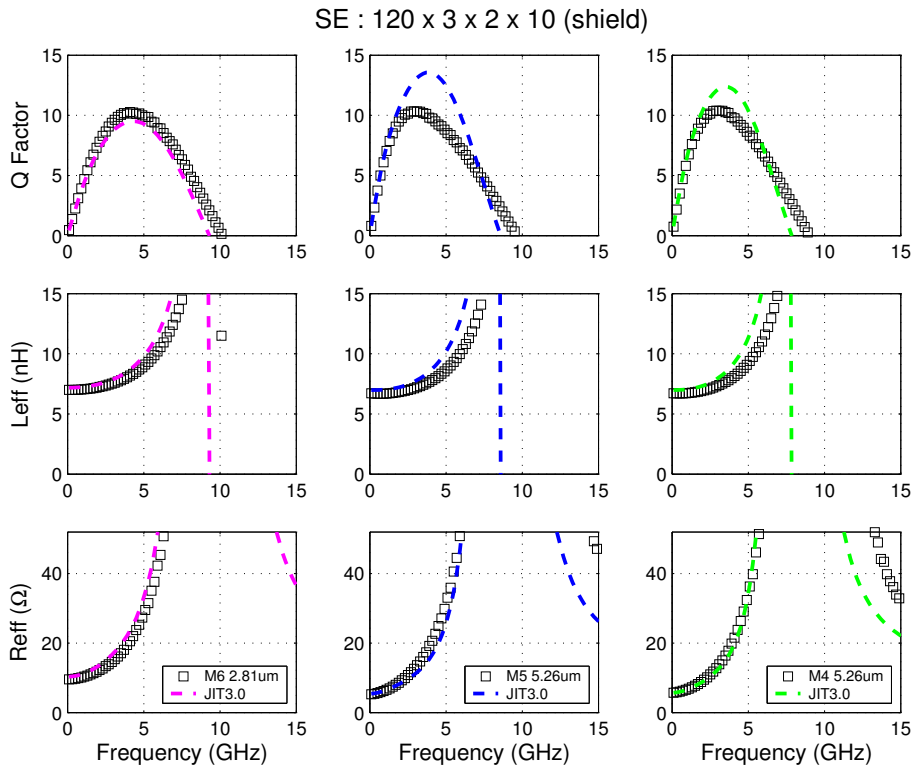


FIGURE 8.35 Inductor Model Verification

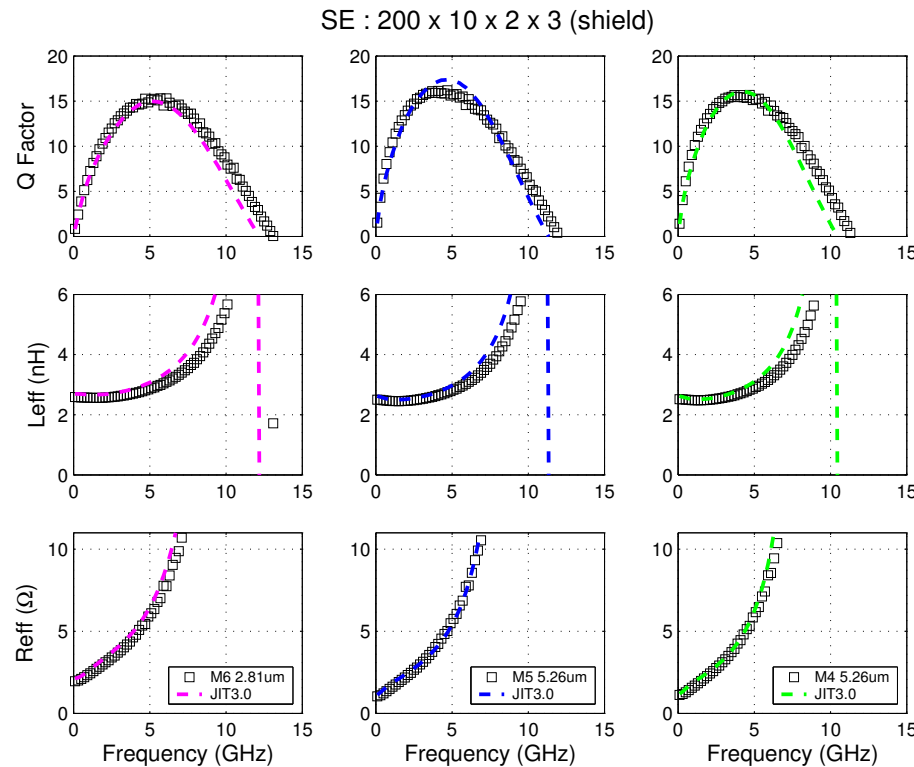


FIGURE 8.36 Inductor Model Verification

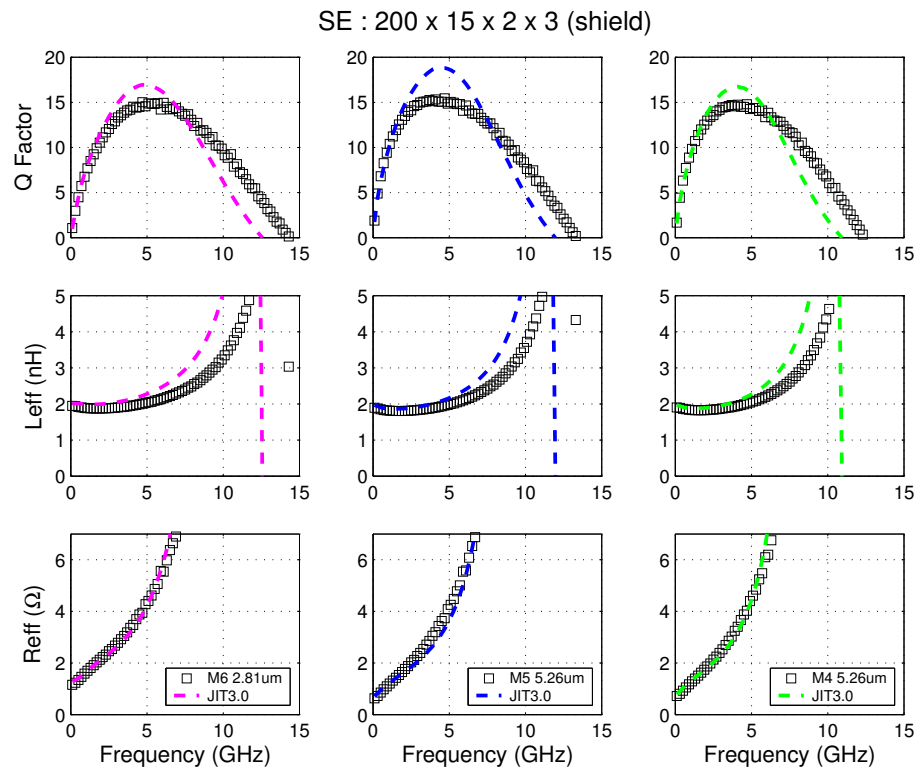


FIGURE 8.37 Inductor Model Verification

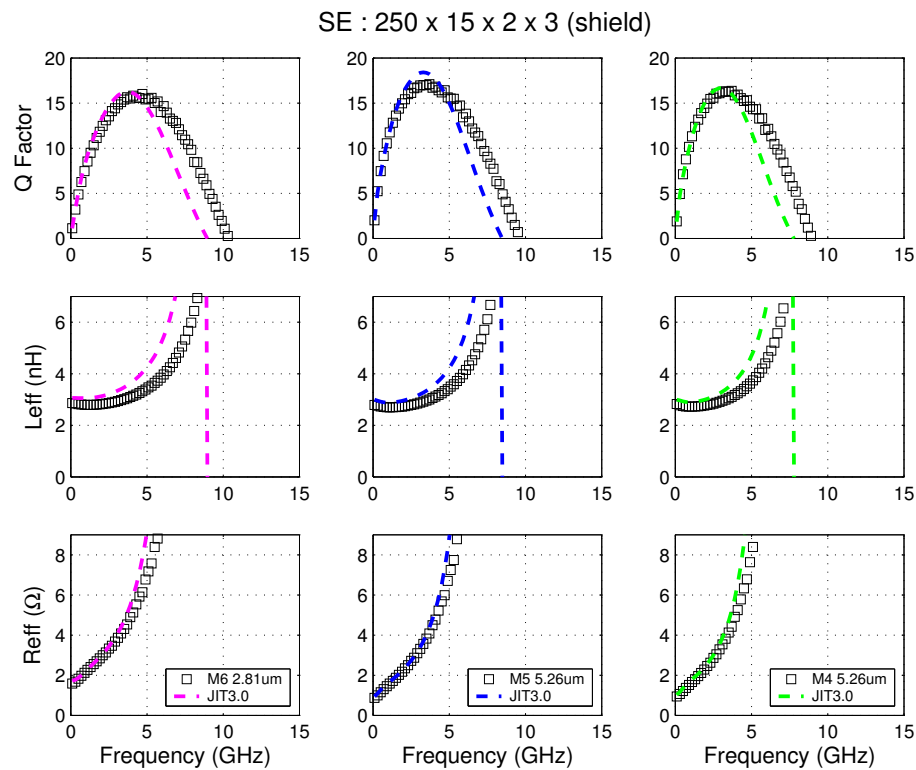


FIGURE 8.38 Inductor Model Verification

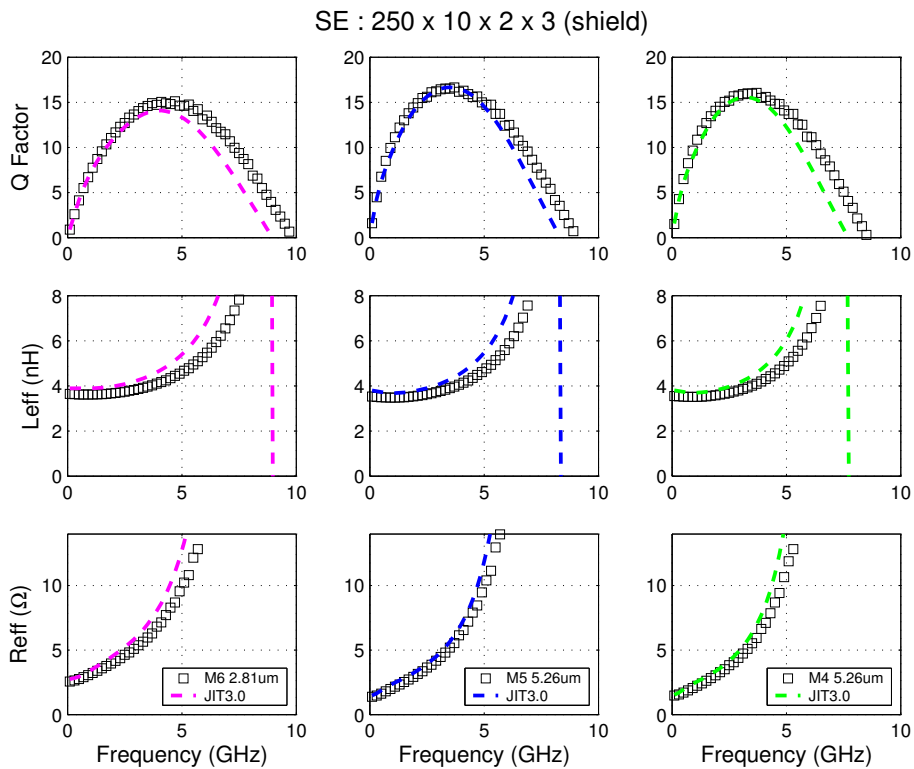


FIGURE 8.39 Inductor Model Verification

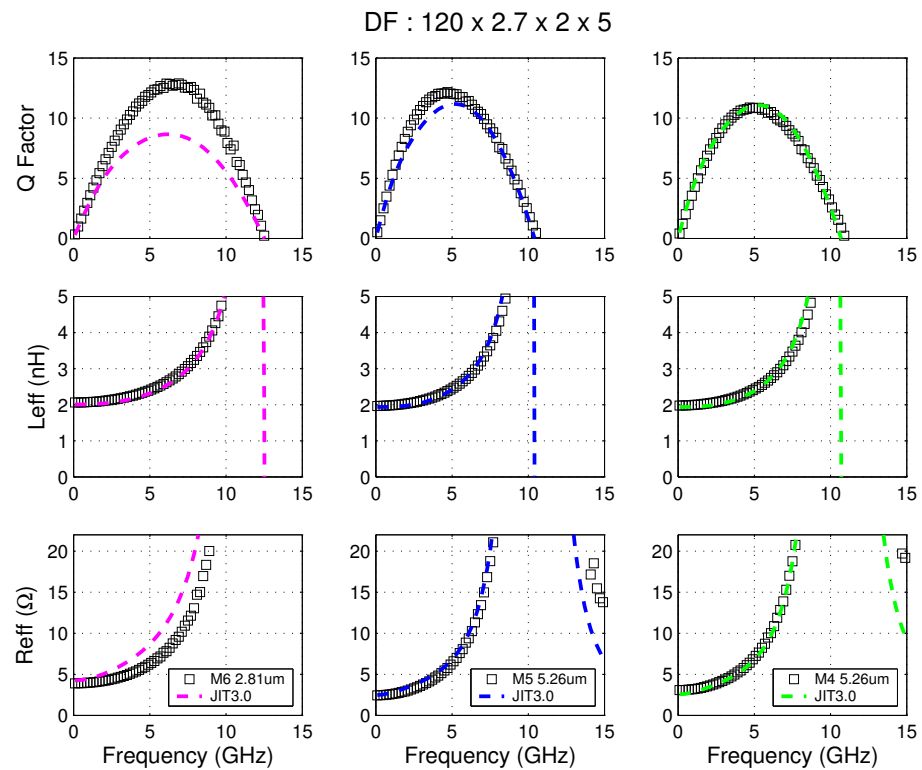


FIGURE 8.40 Inductor Model Verification

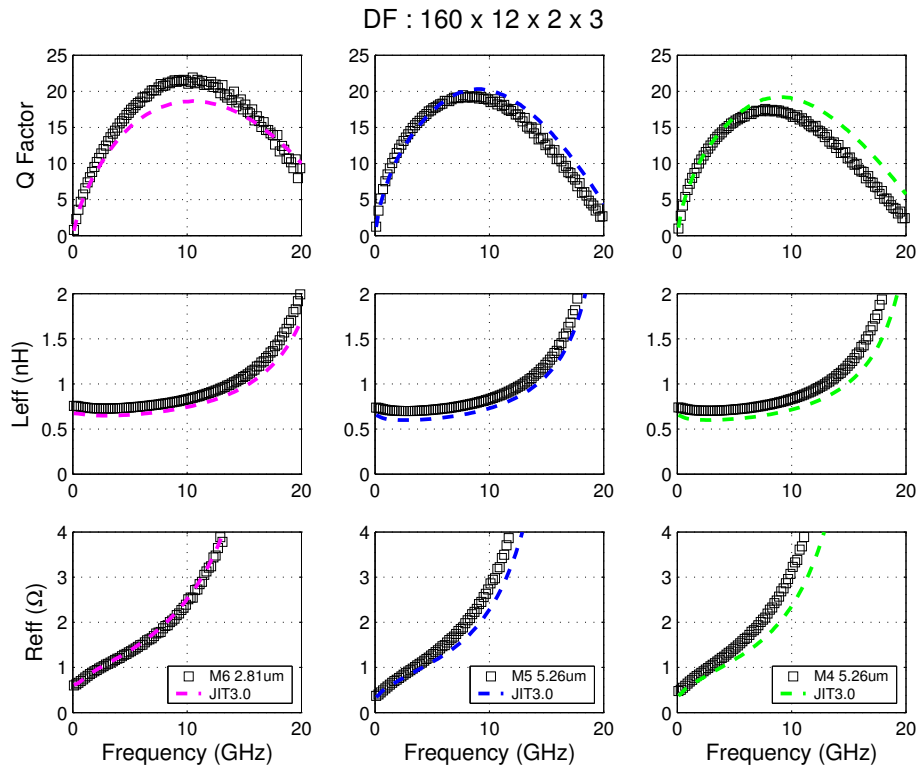


FIGURE 8.41 Inductor Model Verification

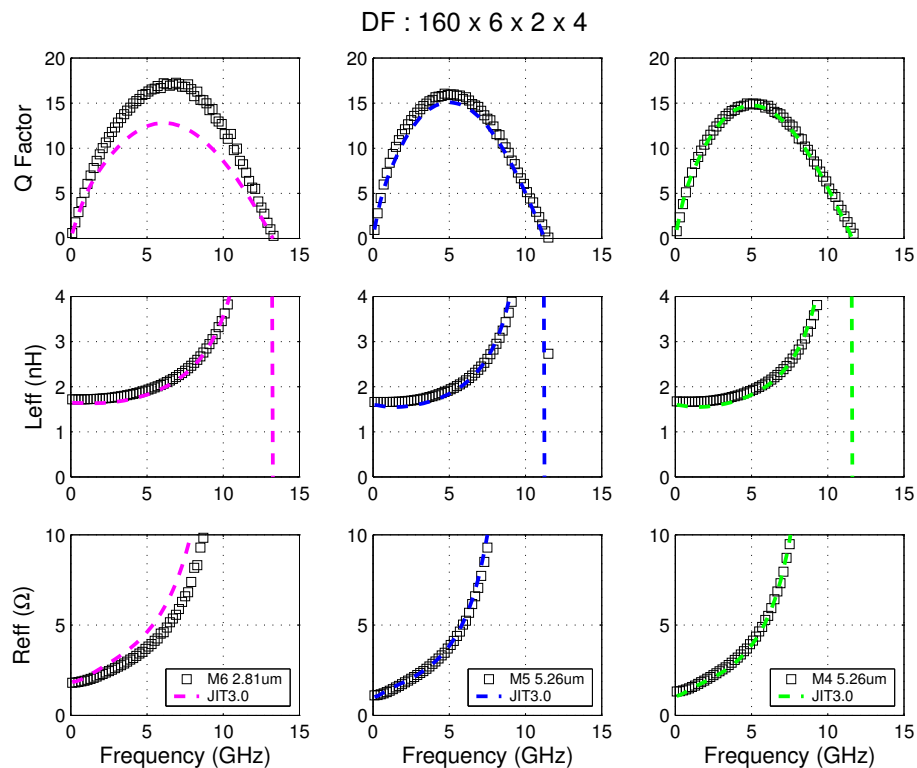


FIGURE 8.42 Inductor Model Verification

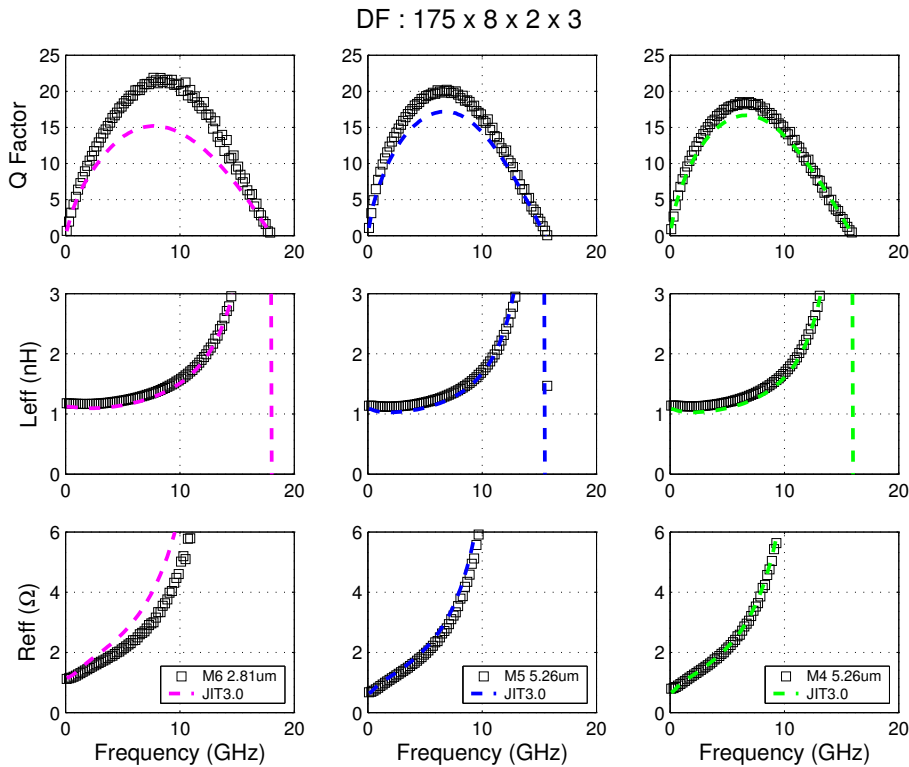


FIGURE 8.43 Inductor Model Verification

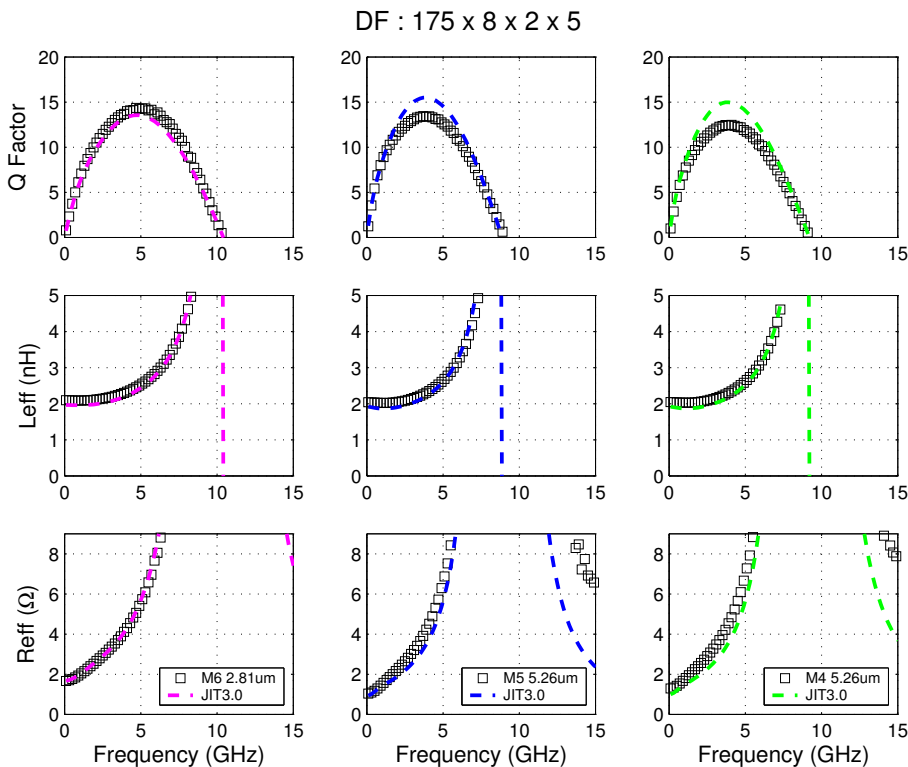


FIGURE 8.44 Inductor Model Verification

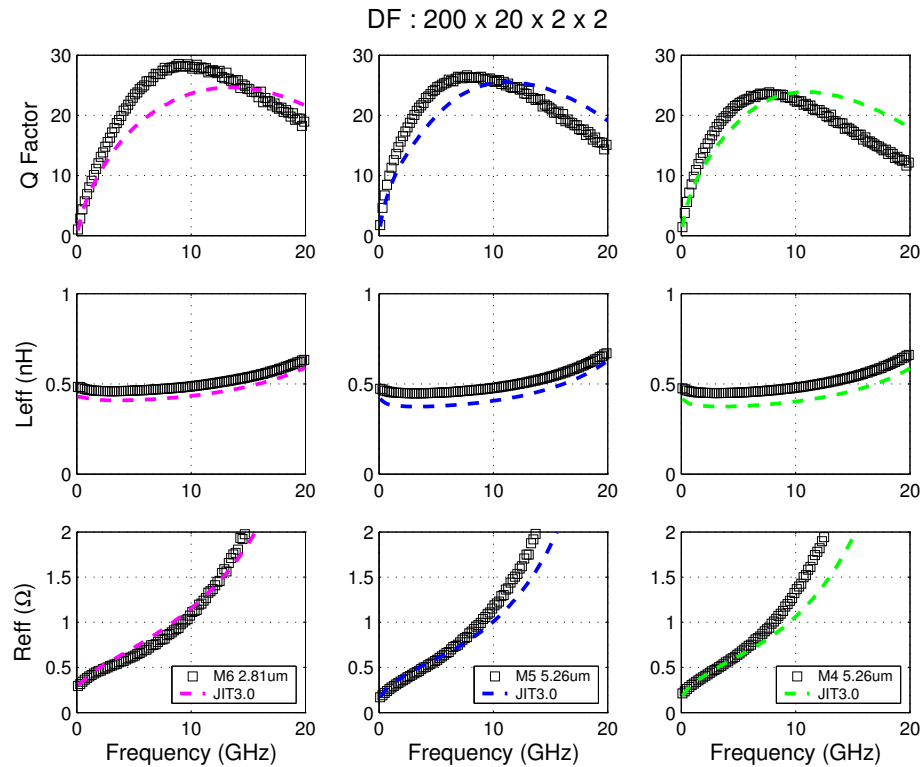


FIGURE 8.45 Inductor Model Verification

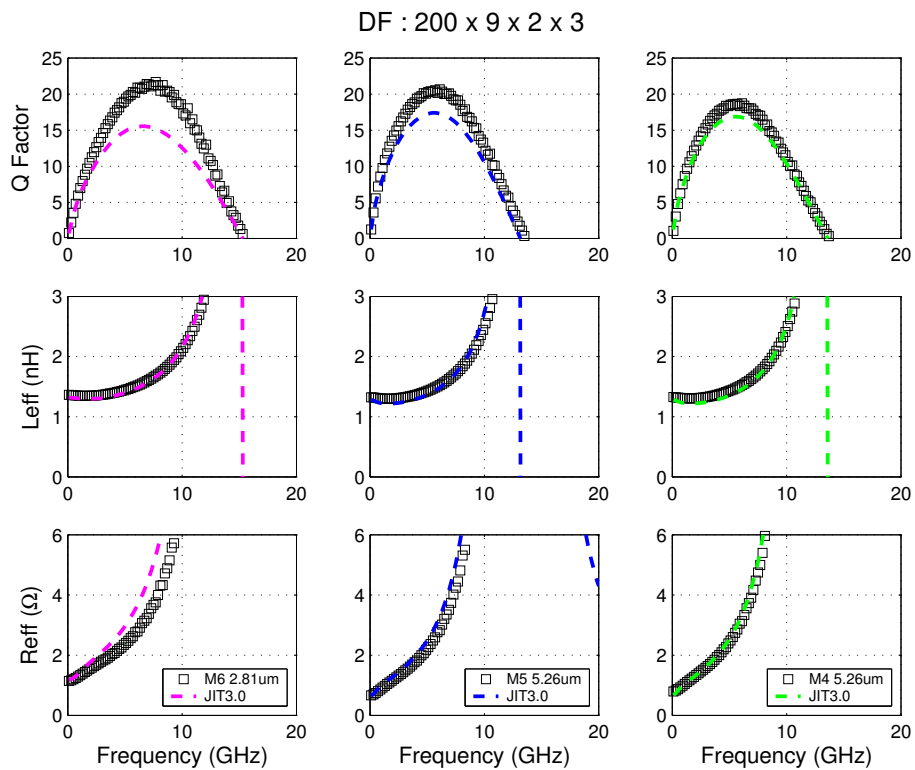


FIGURE 8.46 Inductor Model Verification

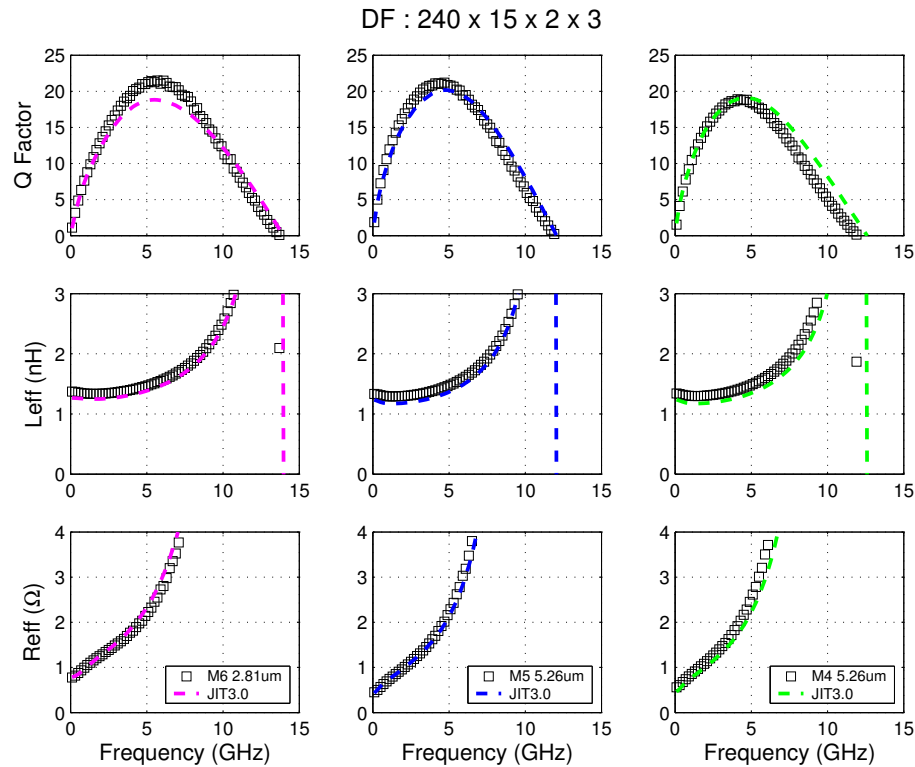


FIGURE 8.47 Inductor Model Verification

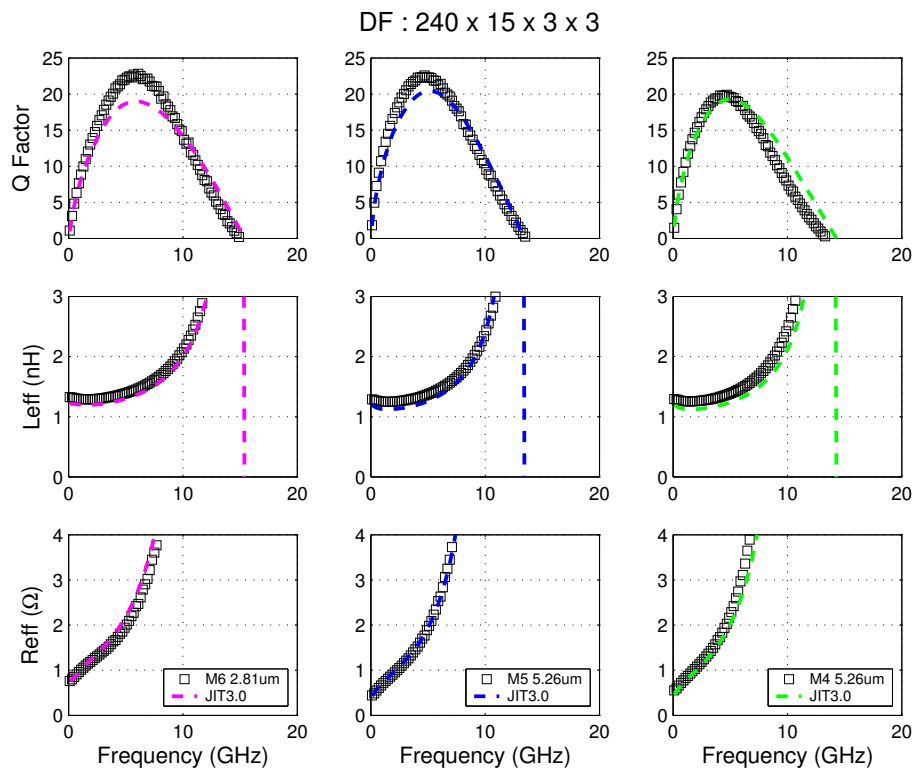


FIGURE 8.48 Inductor Model Verification

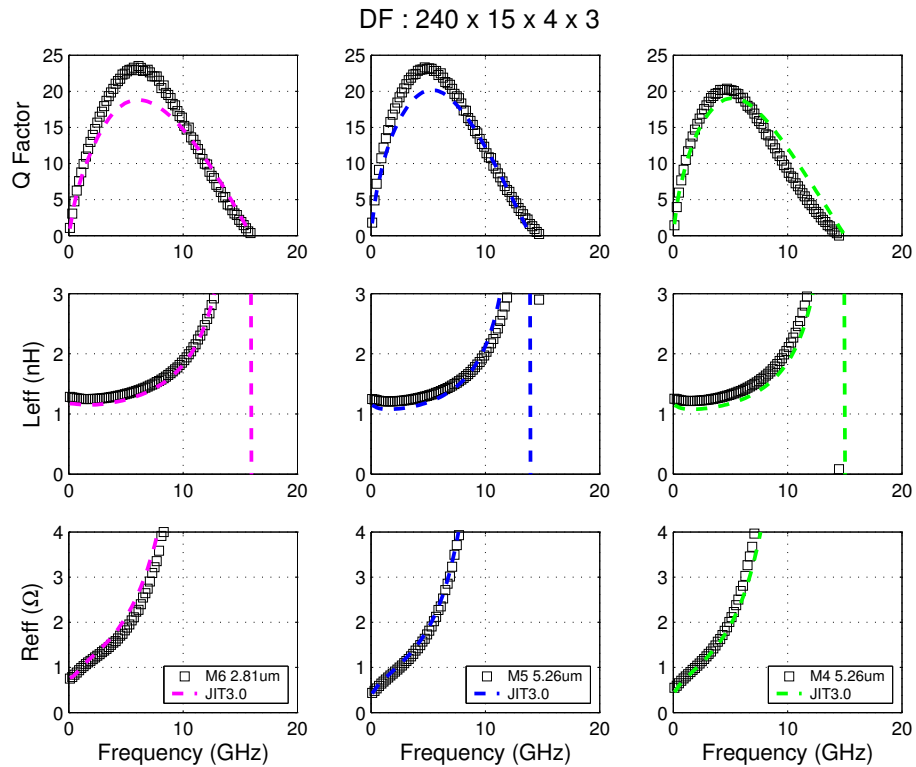


FIGURE 8.49 Inductor Model Verification

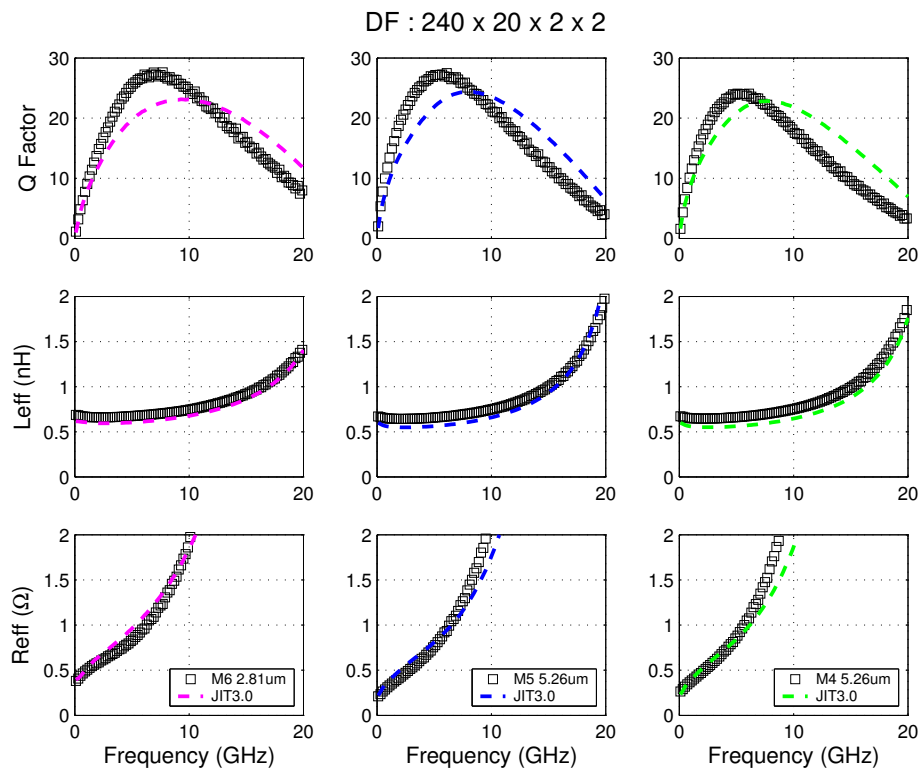


FIGURE 8.50 Inductor Model Verification

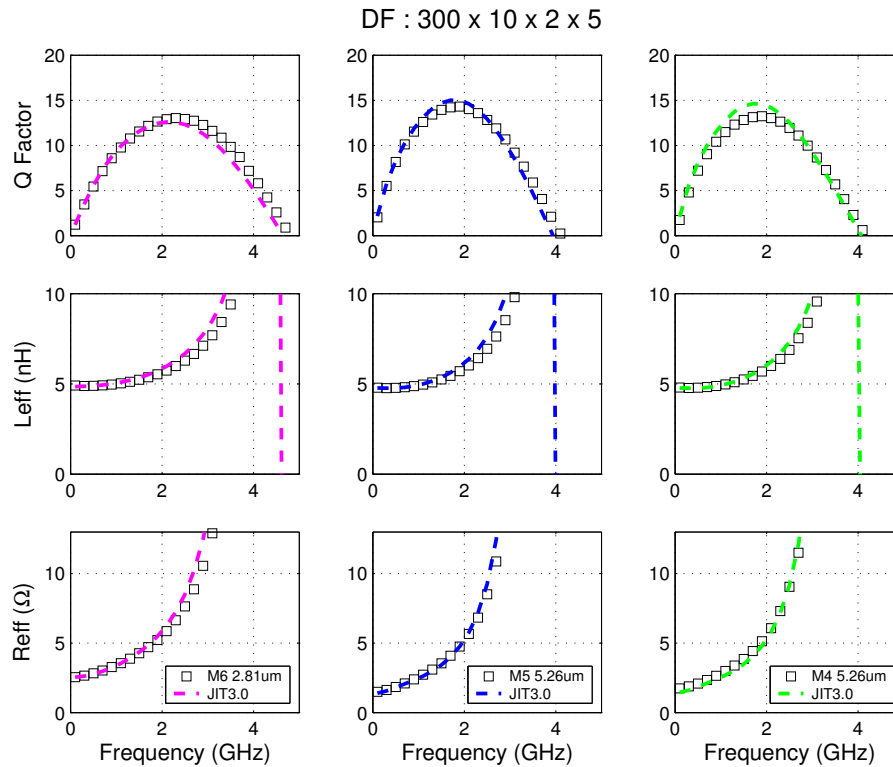


FIGURE 8.51 Inductor Model Verification

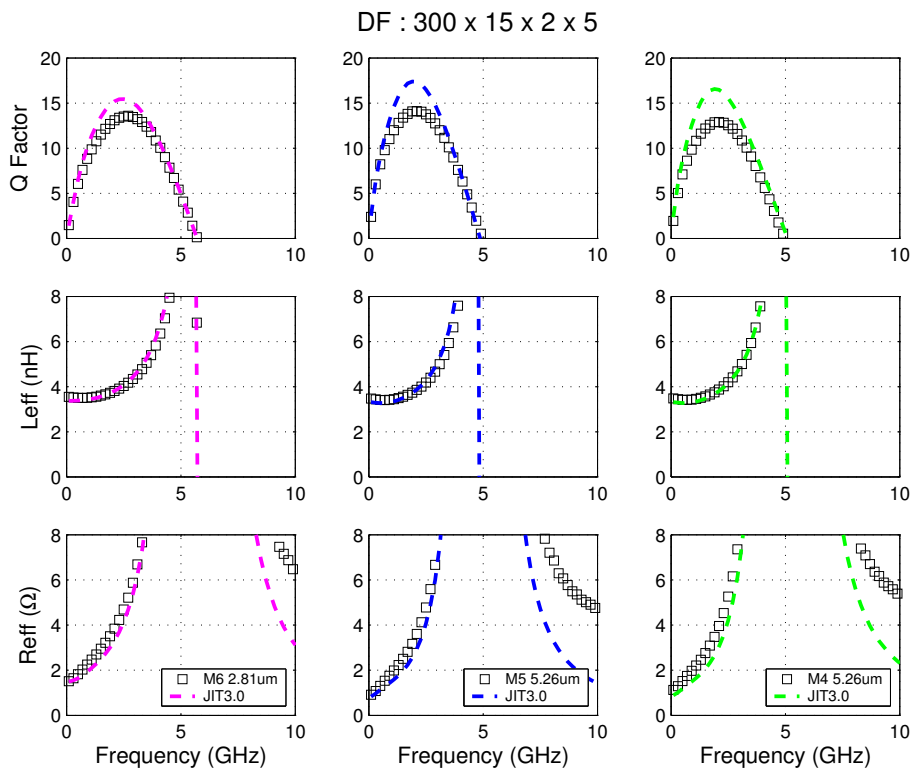


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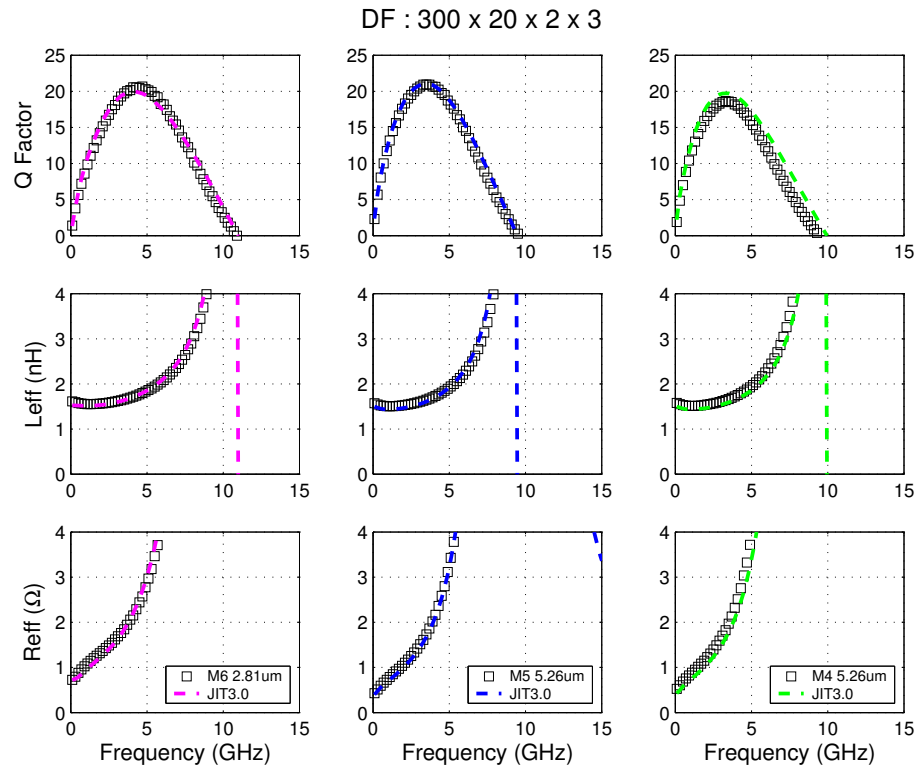


FIGURE 8.53 Inductor Model Verification

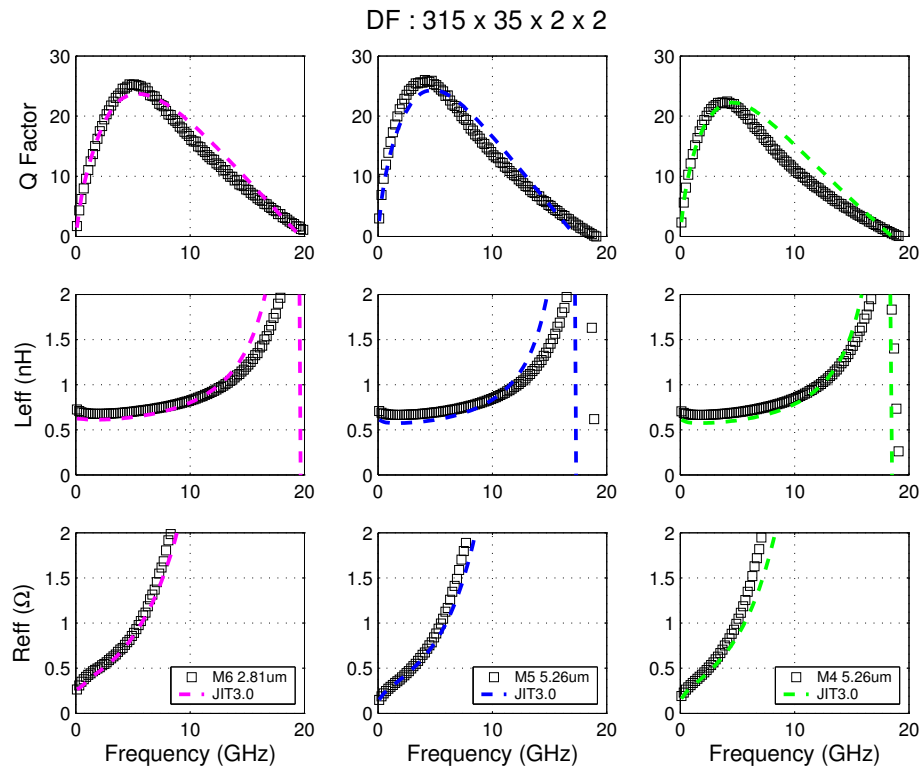


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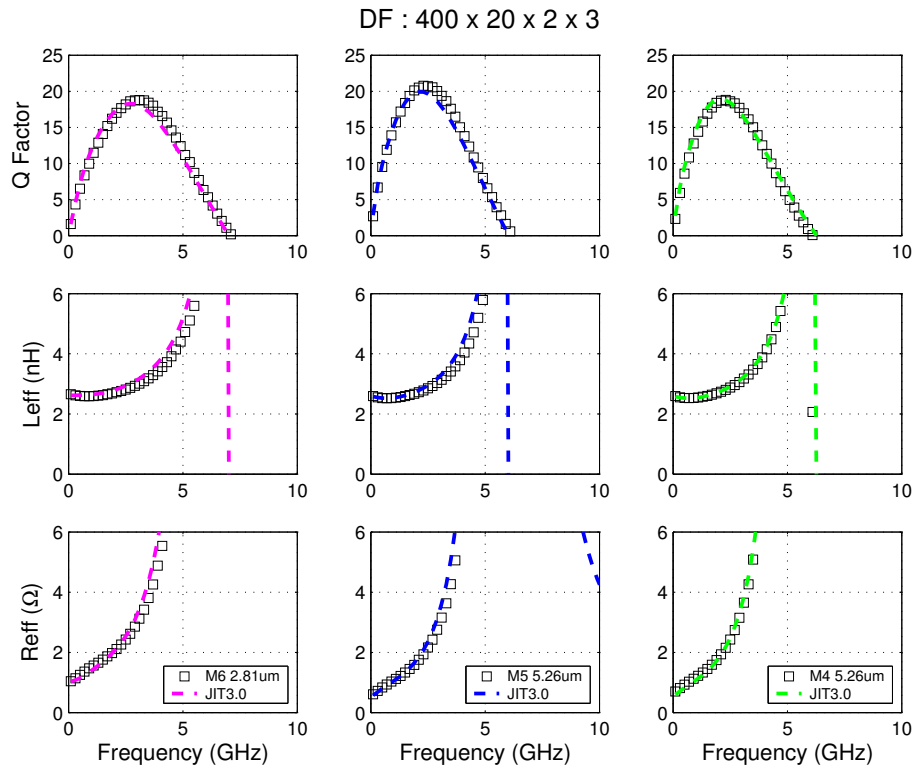


FIGURE 8.55 Inductor Model Verification

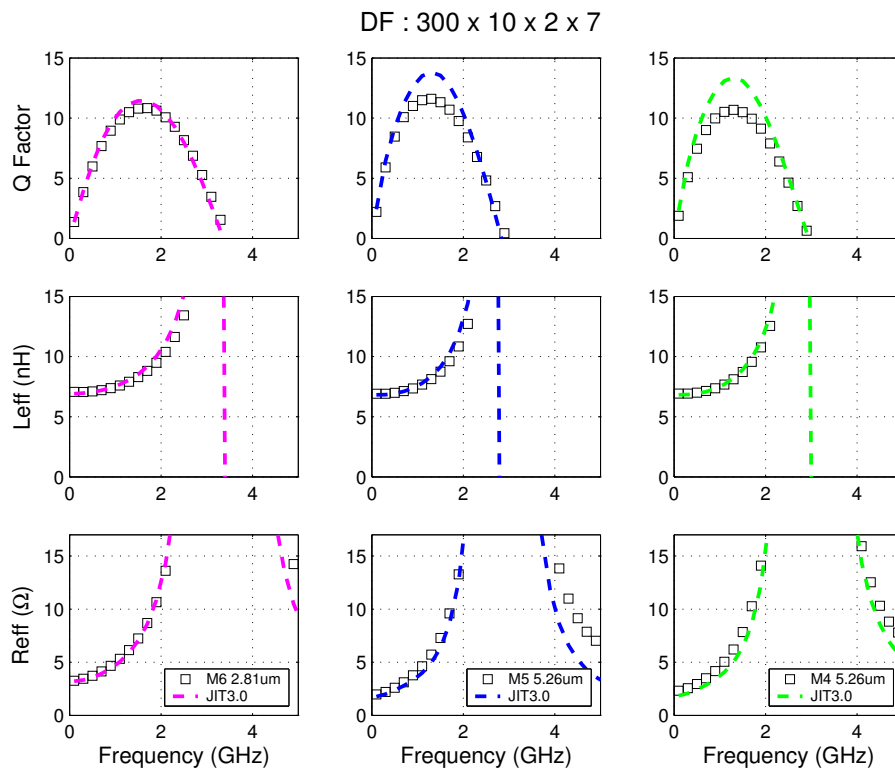


FIGURE 8.56 Inductor Model Verification

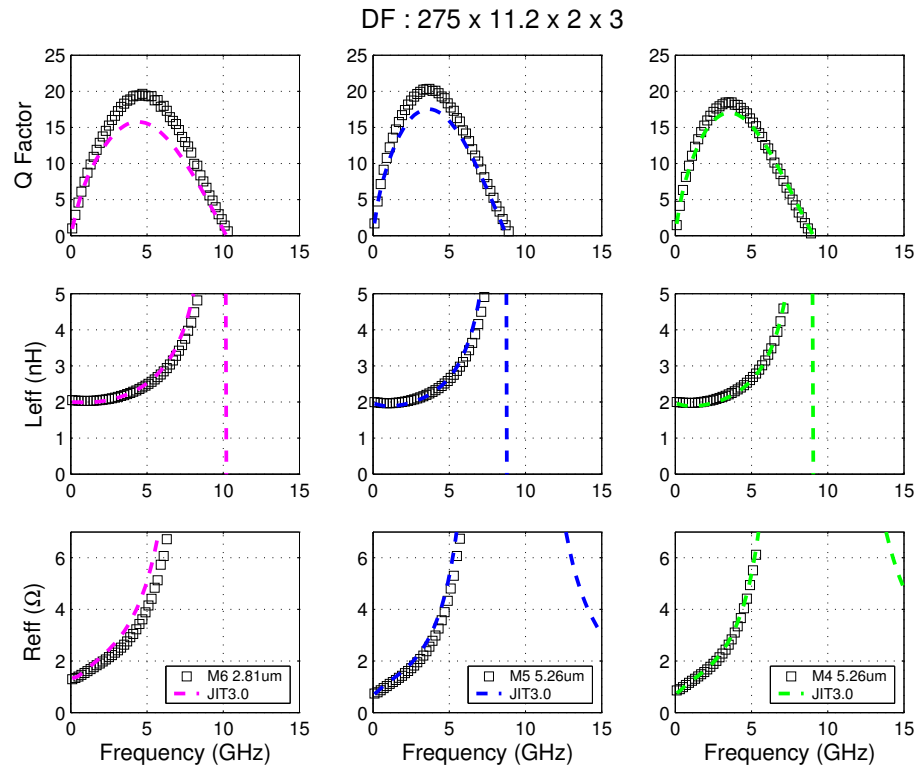


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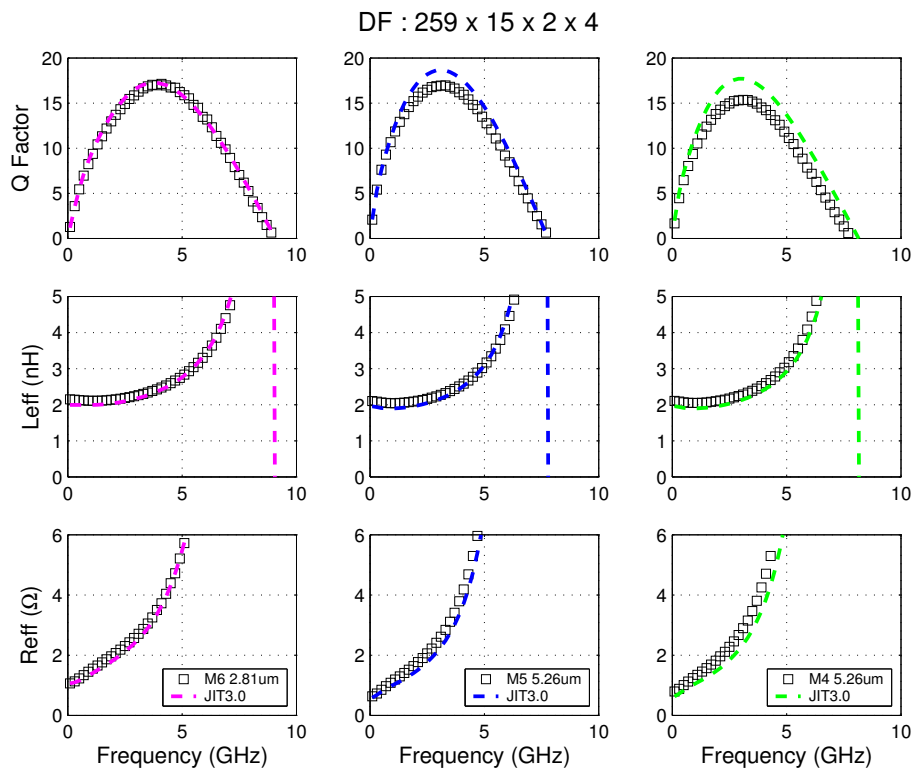


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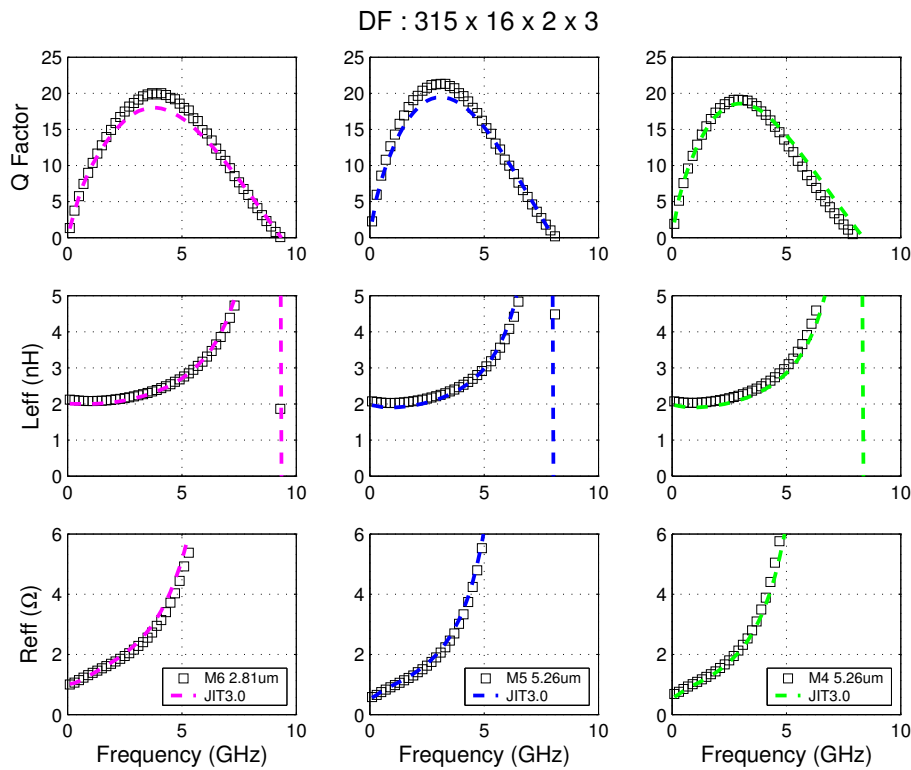


FIGURE 8.59 Inductor Model Verification

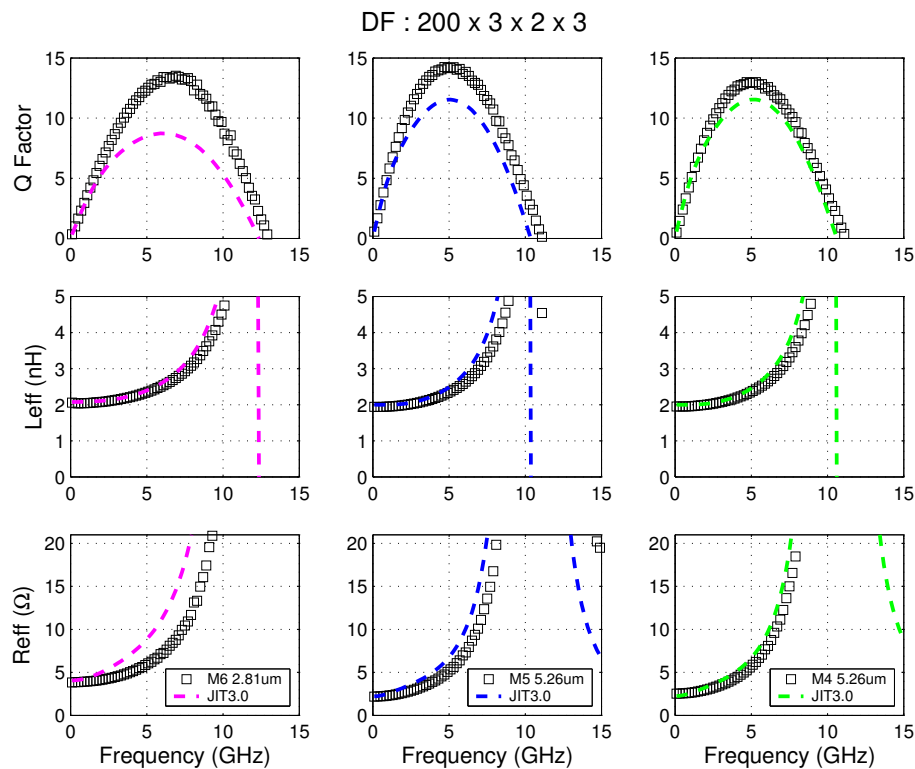


FIGURE 8.60 Inductor Model Verification

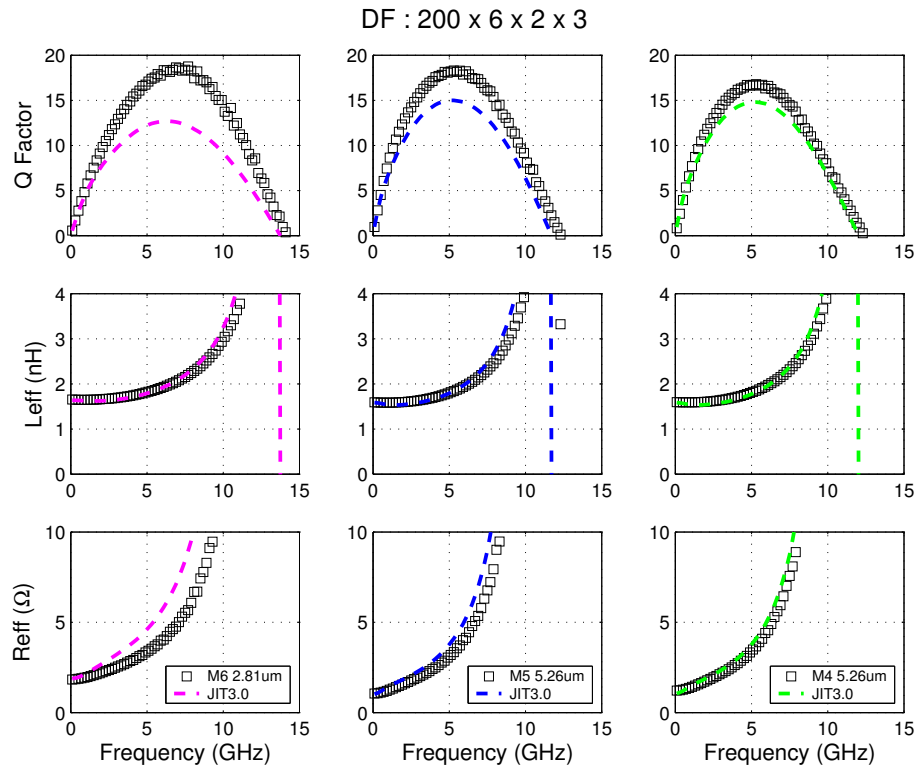


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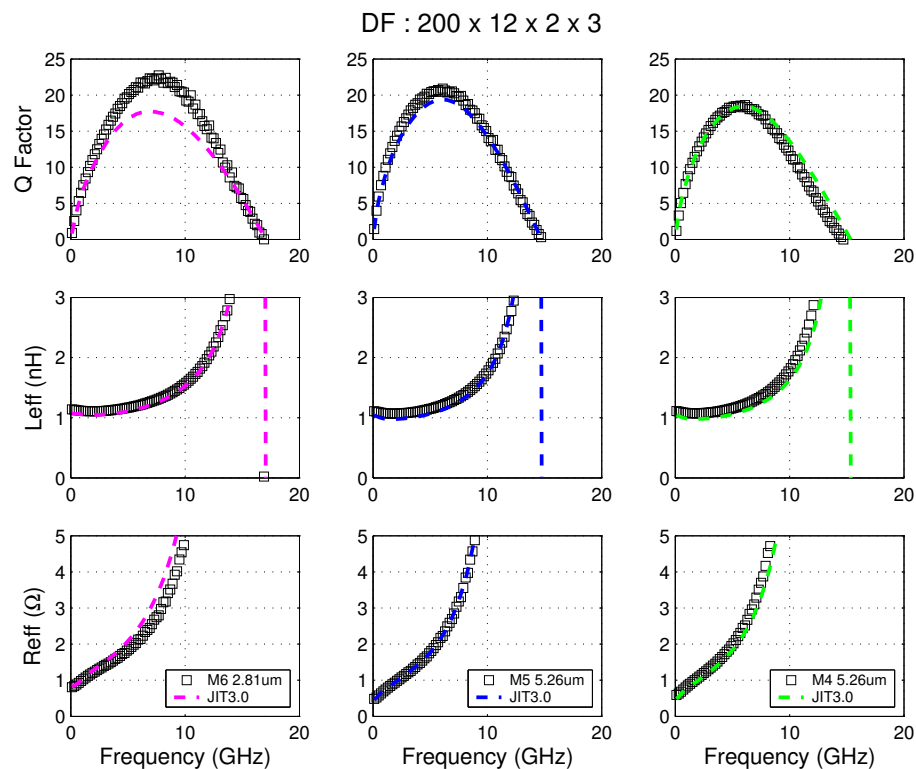


FIGURE 8.62 Inductor Model Verification

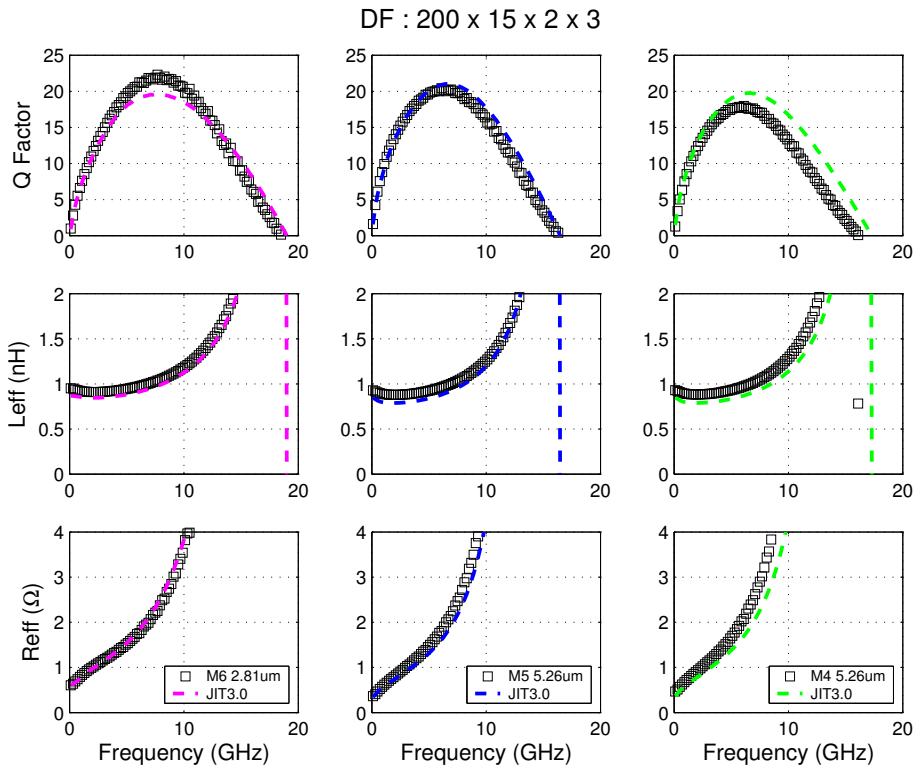


FIGURE 8.63 Inductor Model Verification

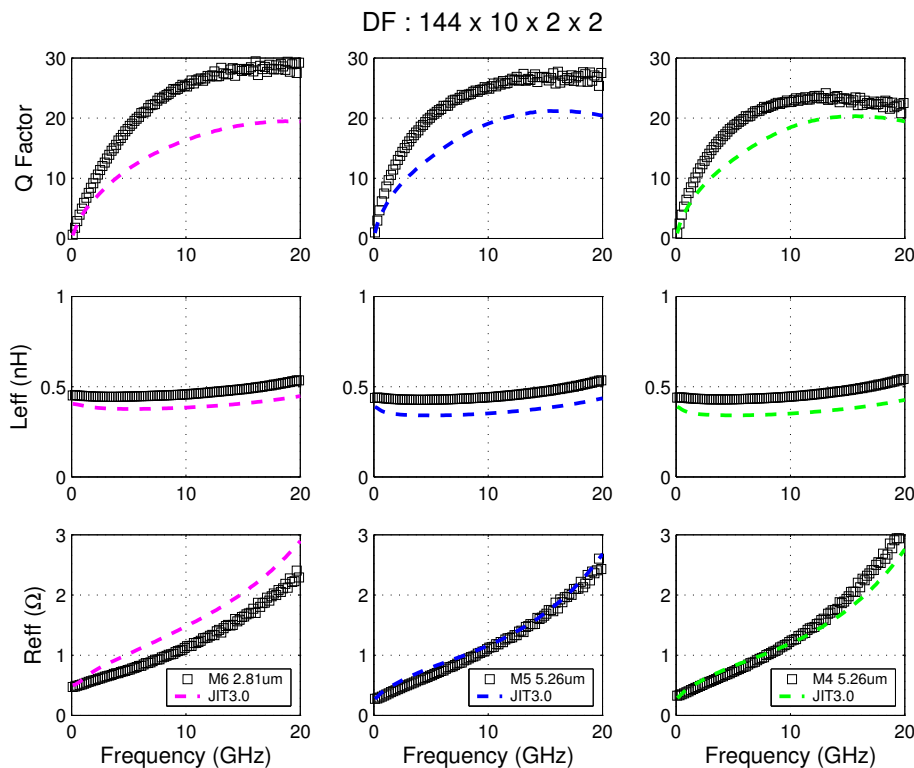


FIGURE 8.64 Inductor Model Verification

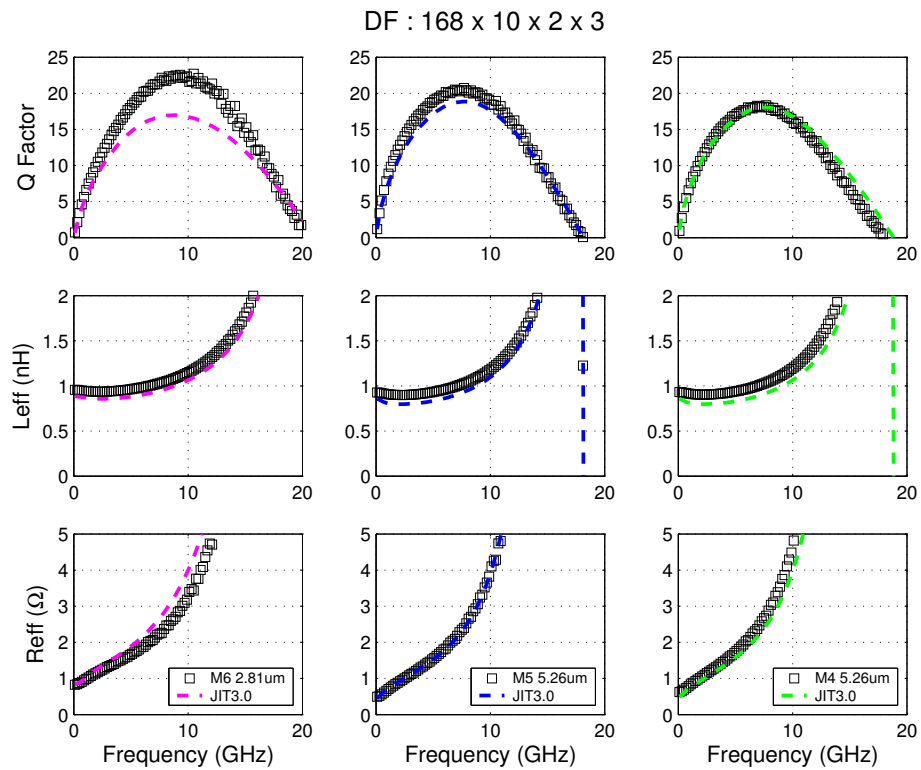


FIGURE 8.65 Inductor Model Verification

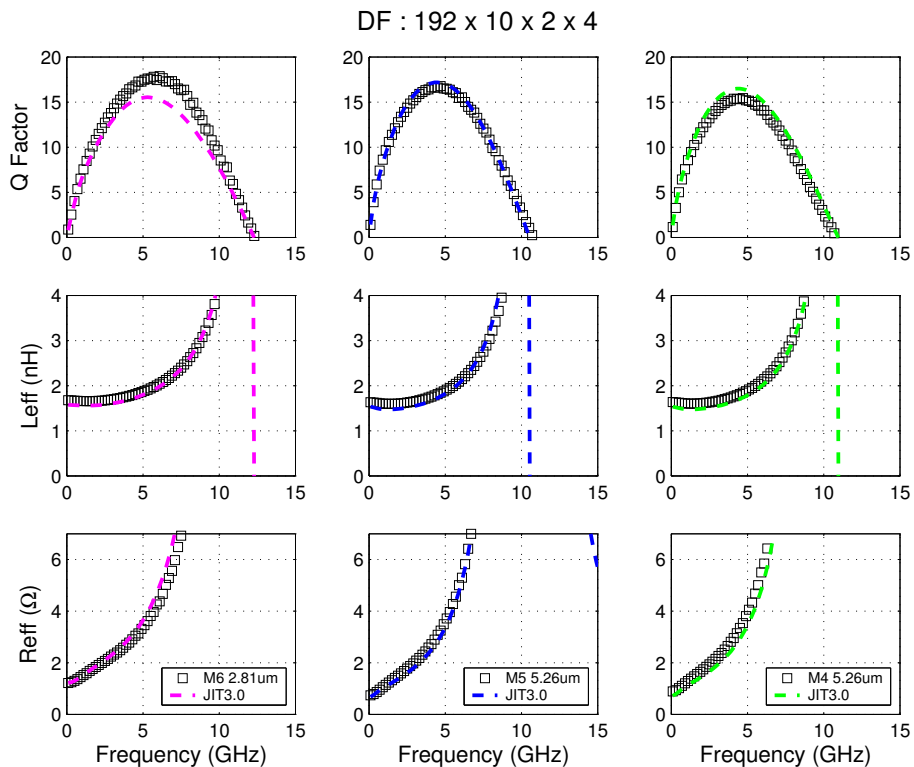


FIGURE 8.66 Inductor Model Verification

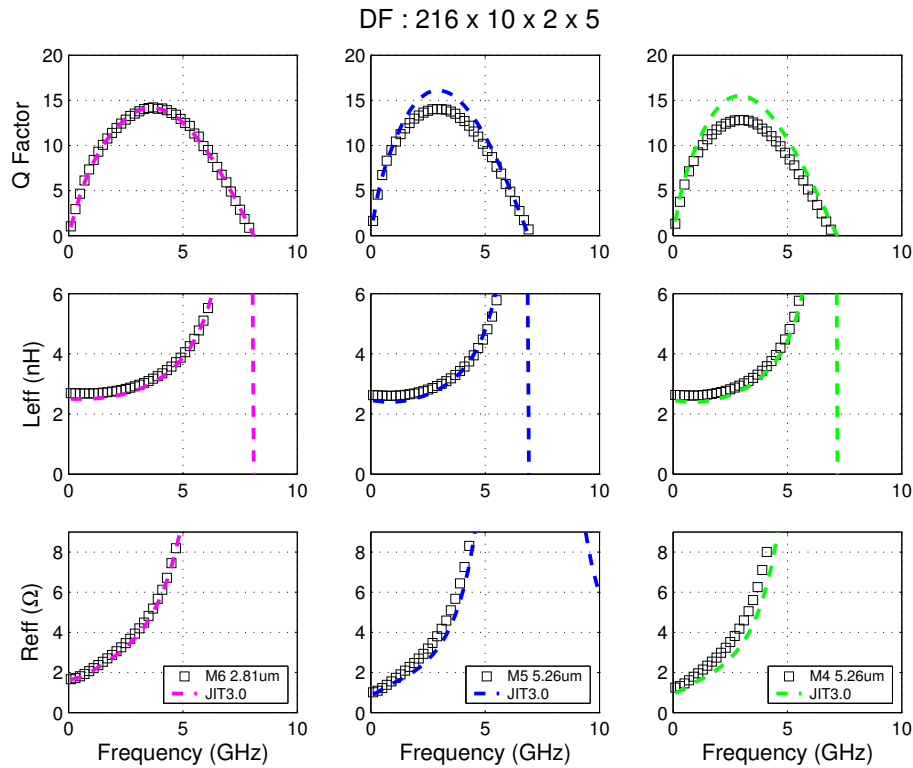


FIGURE 8.67 Inductor Model Verification

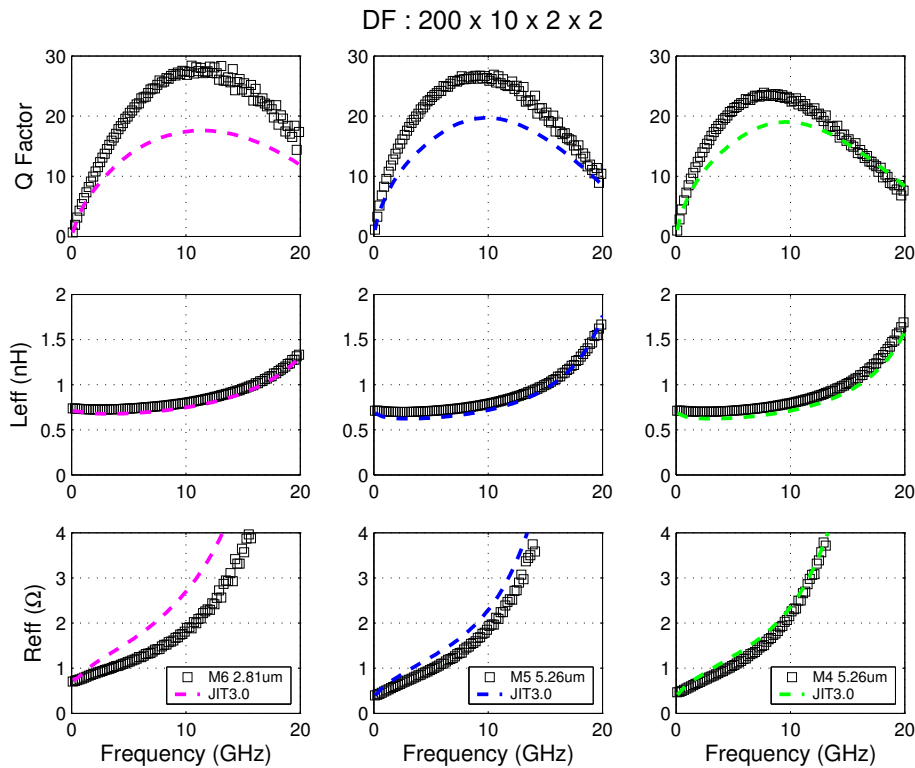


FIGURE 8.68 Inductor Model Verification

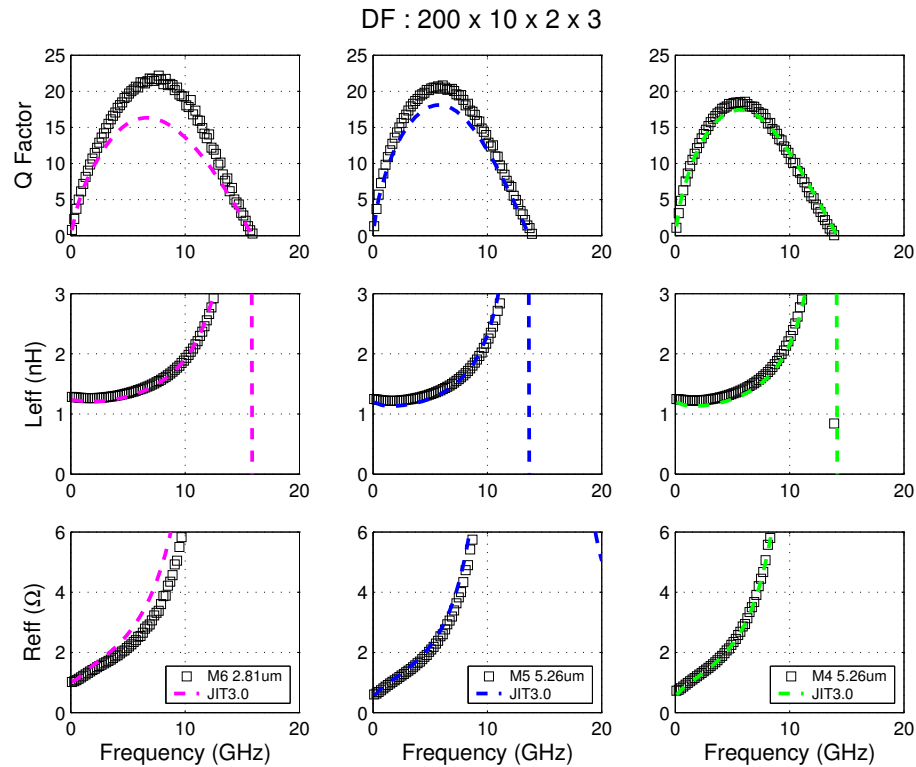


FIGURE 8.69 Inductor Model Verification

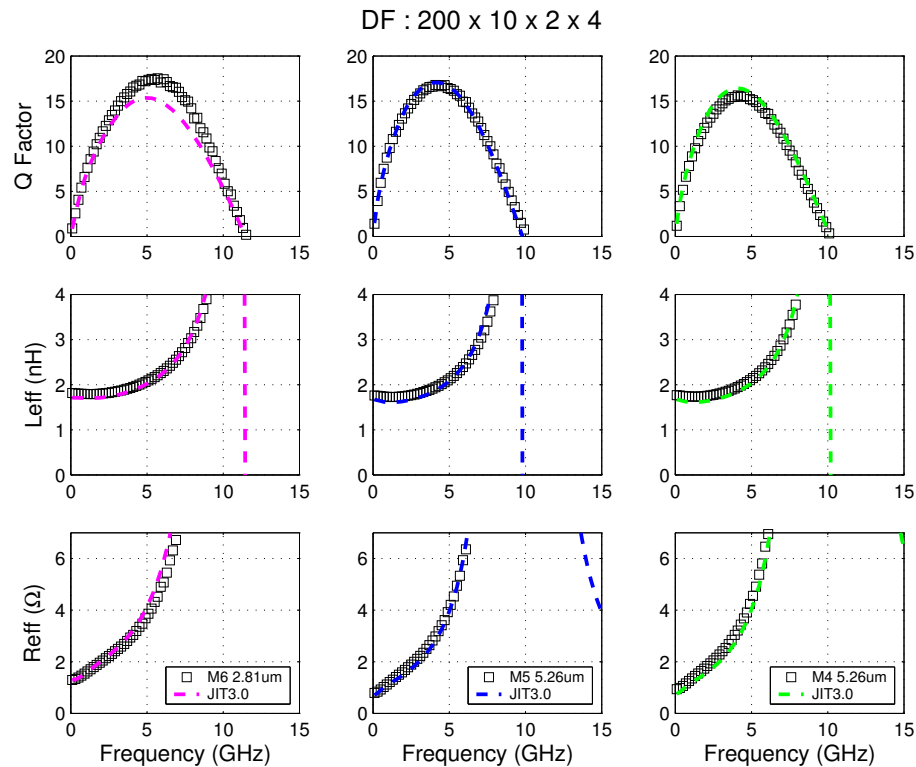


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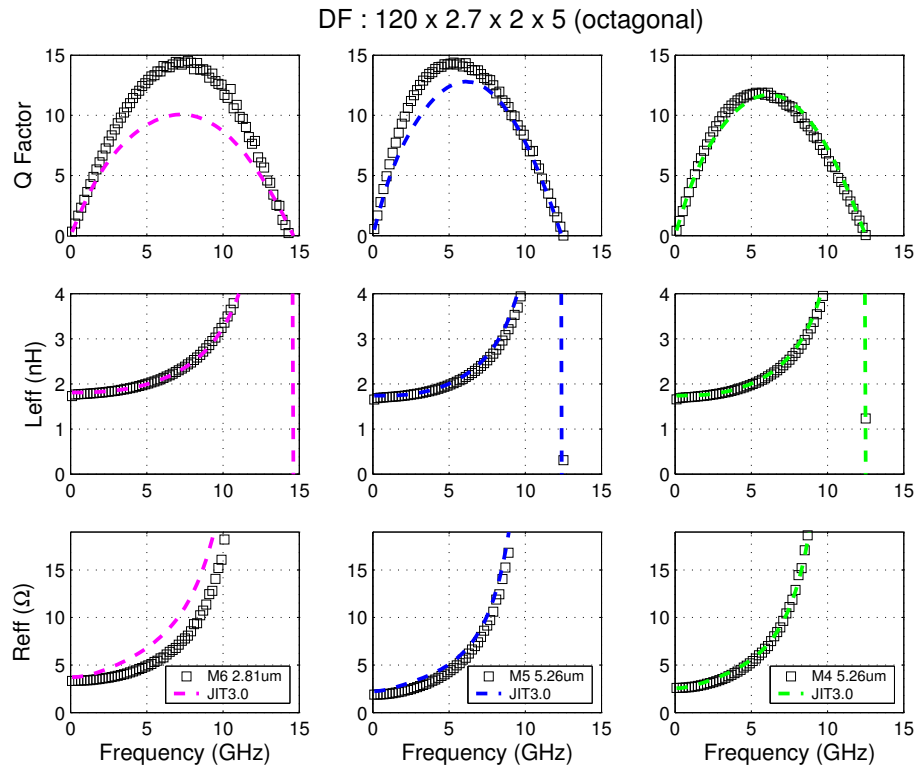


FIGURE 8.71 Inductor Model Verification

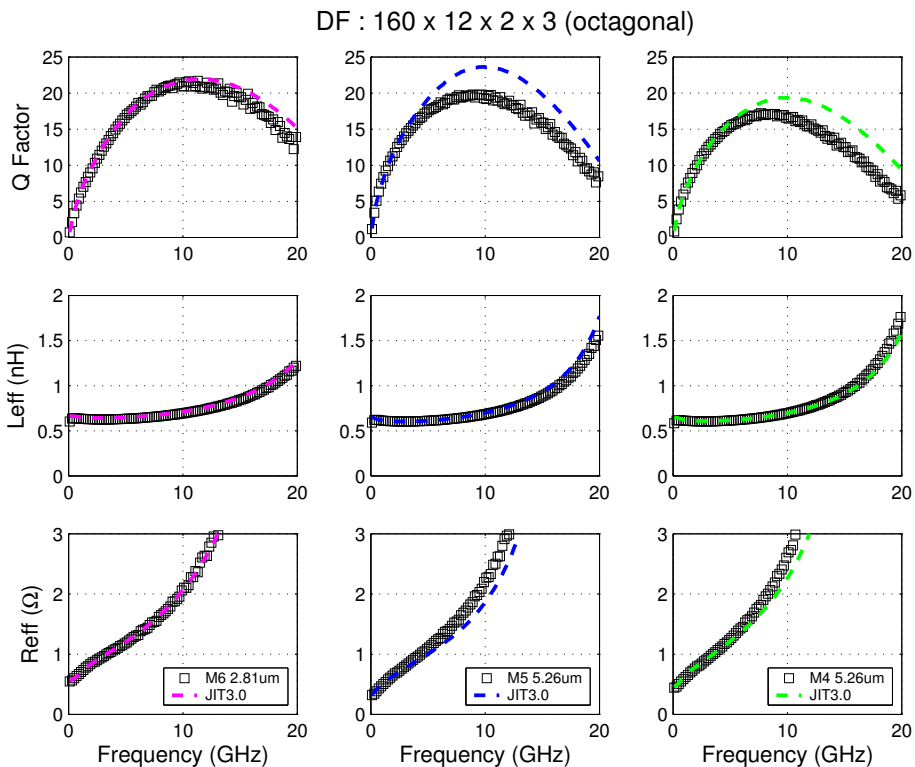


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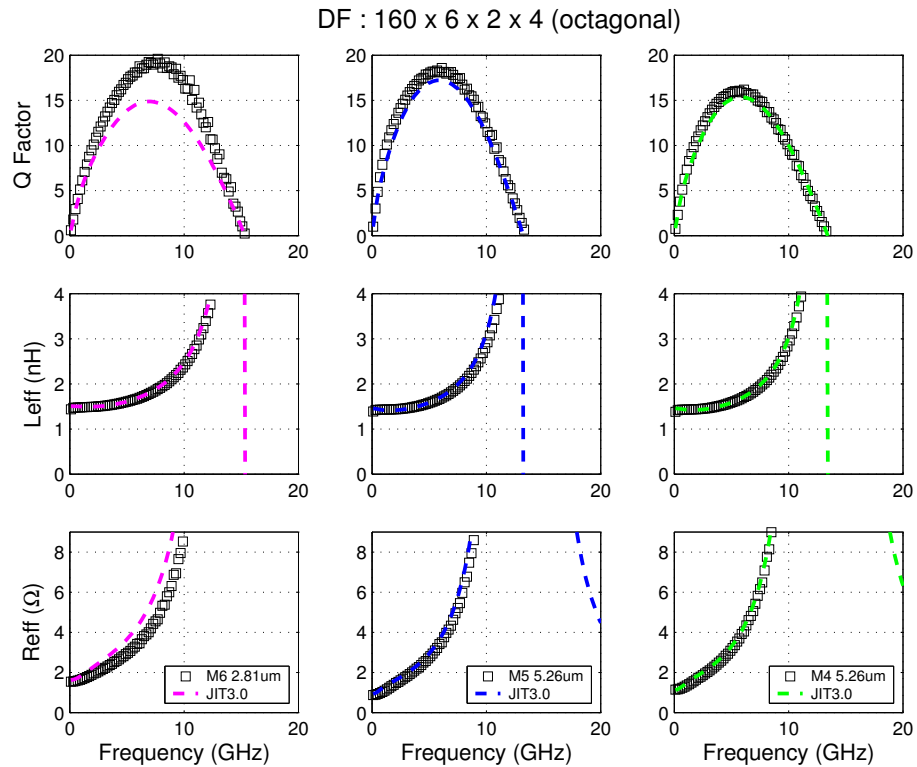


FIGURE 8.73 Inductor Model Verification

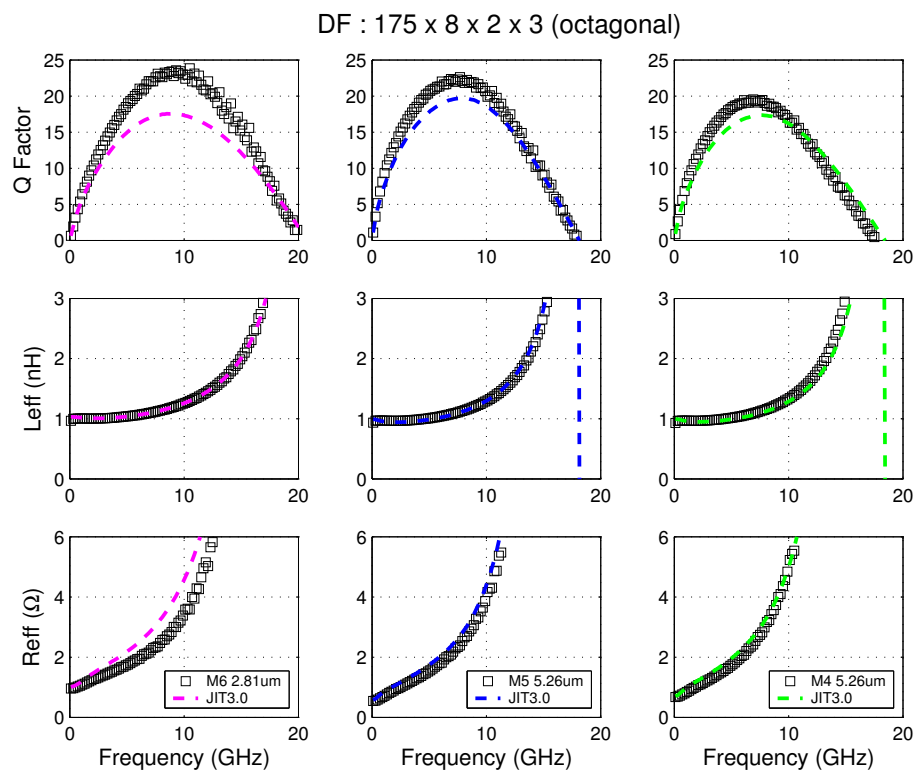


FIGURE 8.74 Inductor Model Verification

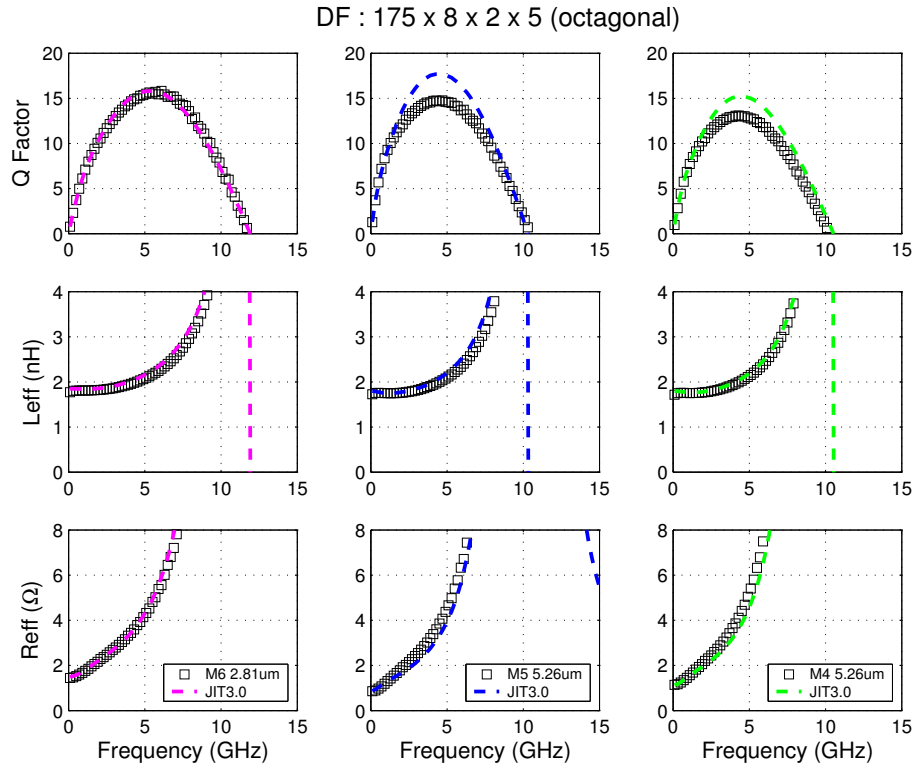


FIGURE 8.75 Inductor Model Verification

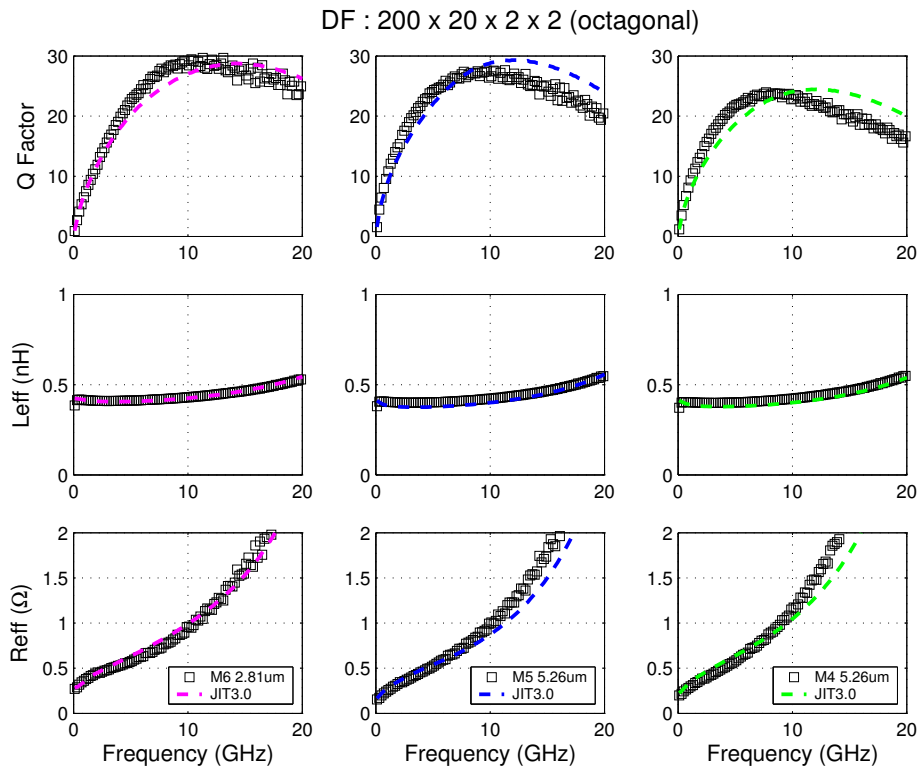


FIGURE 8.76 Inductor Model Verification

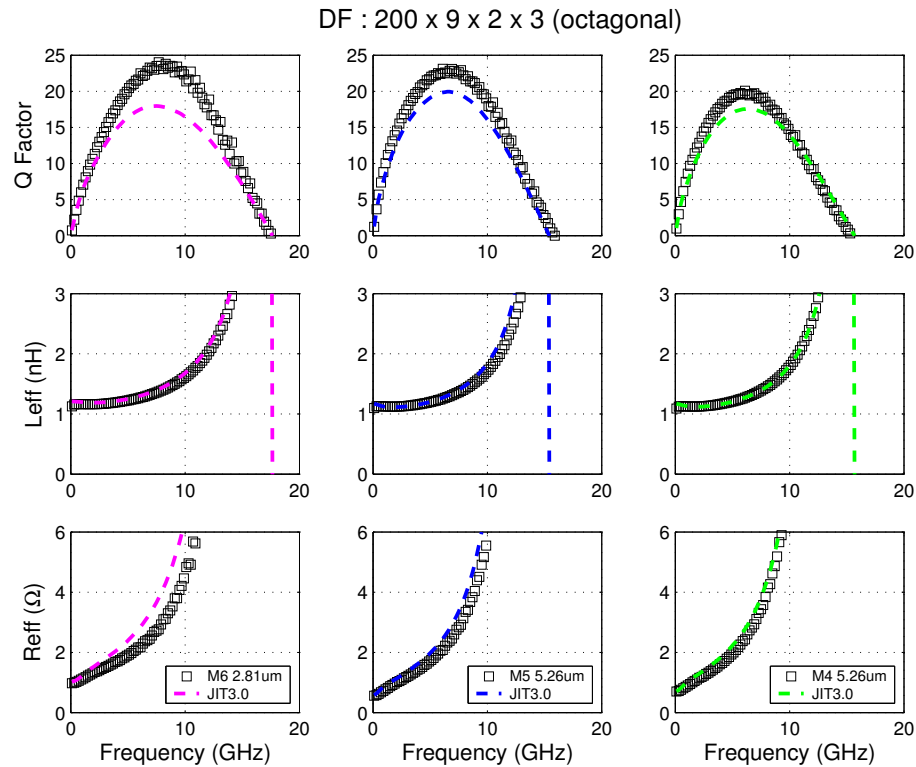


FIGURE 8.77 Inductor Model Verification

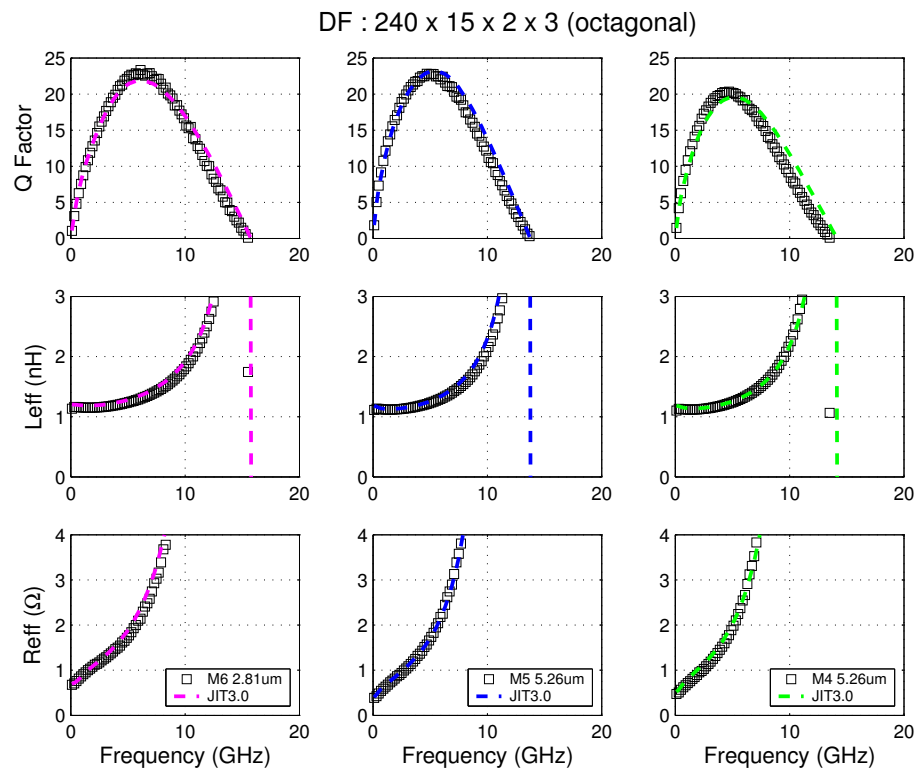


FIGURE 8.78 Inductor Model Verification

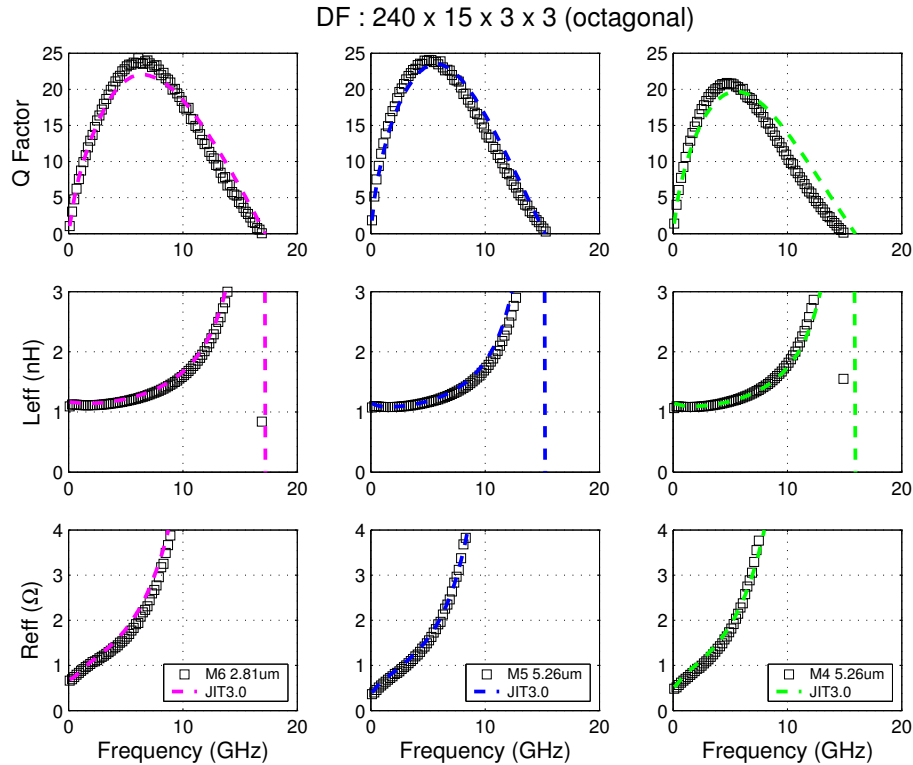


FIGURE 8.79 Inductor Model Verification

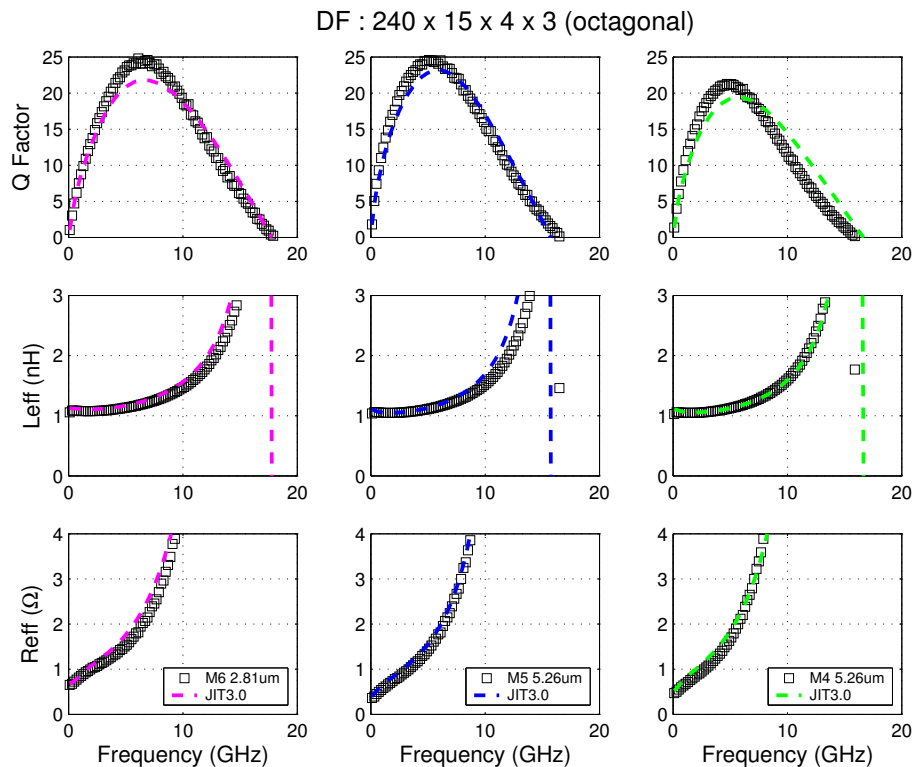


FIGURE 8.80 Inductor Model Verification

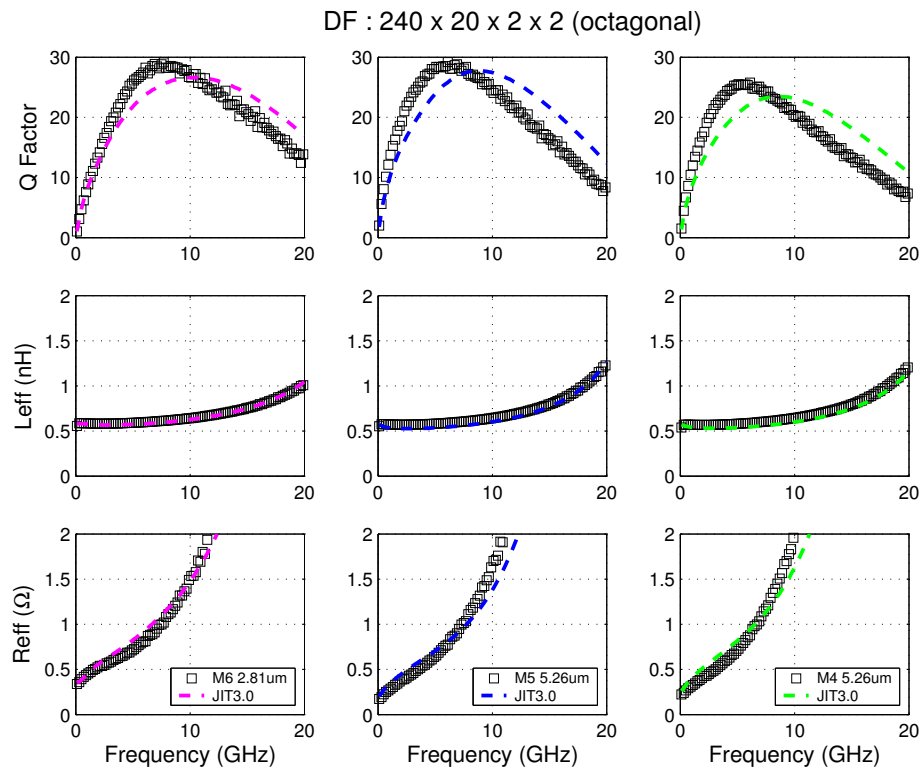


FIGURE 8.81 Inductor Model Verification

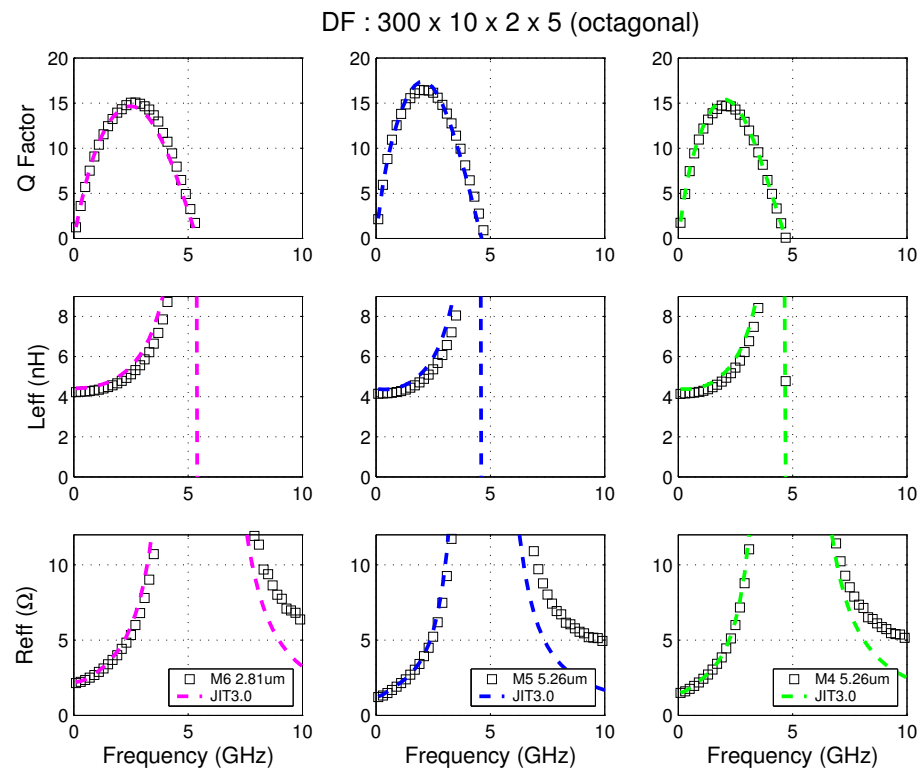


FIGURE 8.82 Inductor Model Verification

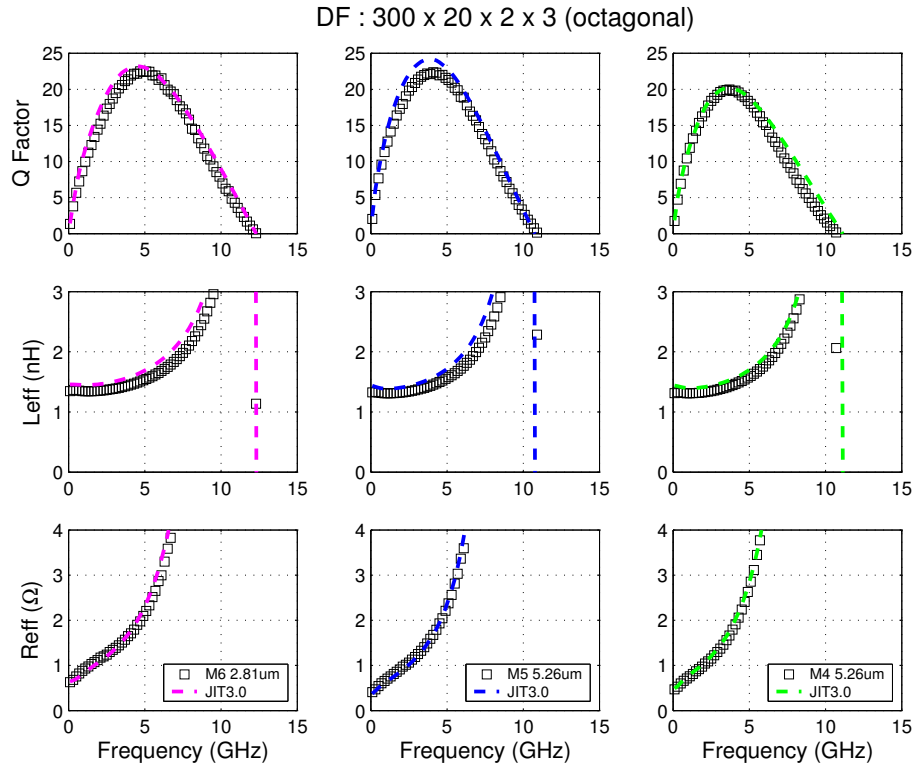


FIGURE 8.83 Inductor Model Verification

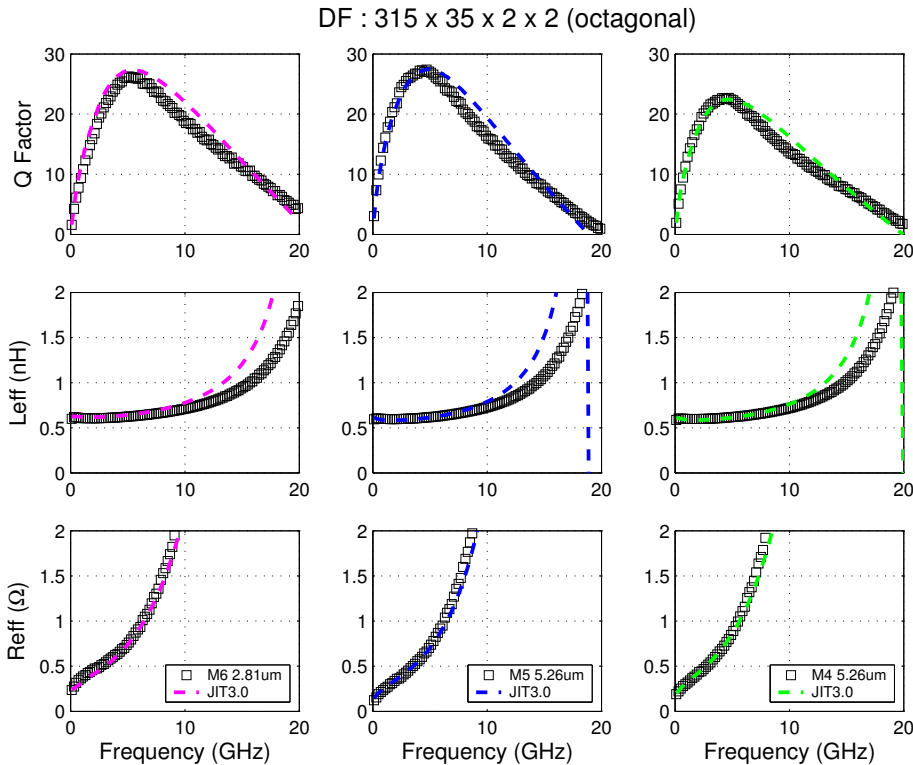


FIGURE 8.84 Inductor Model Verification

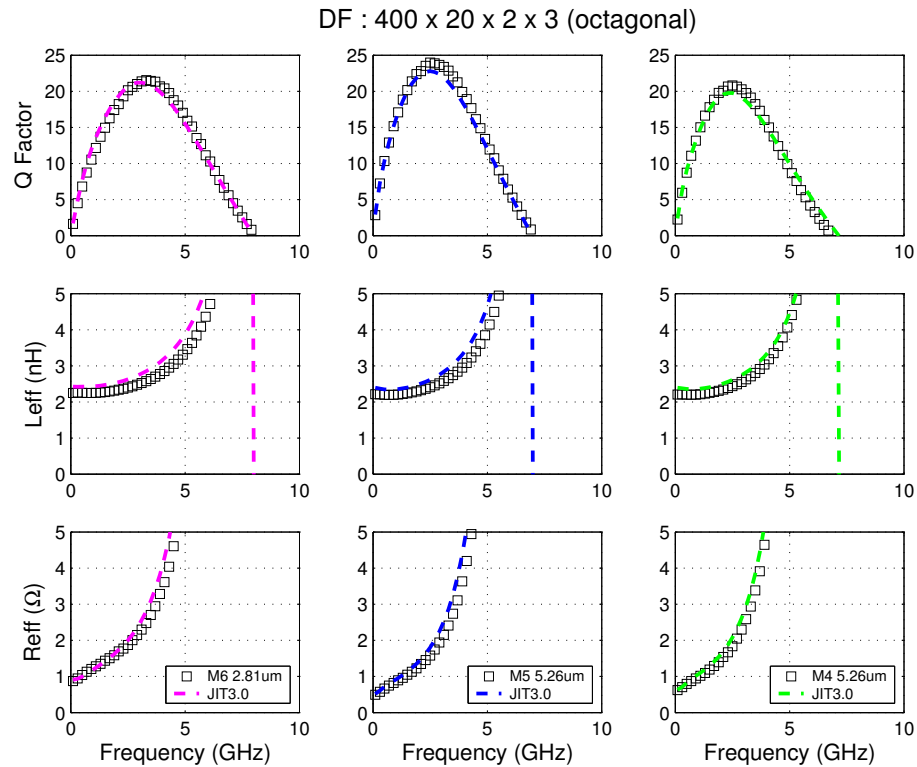


FIGURE 8.85 Inductor Model Verification

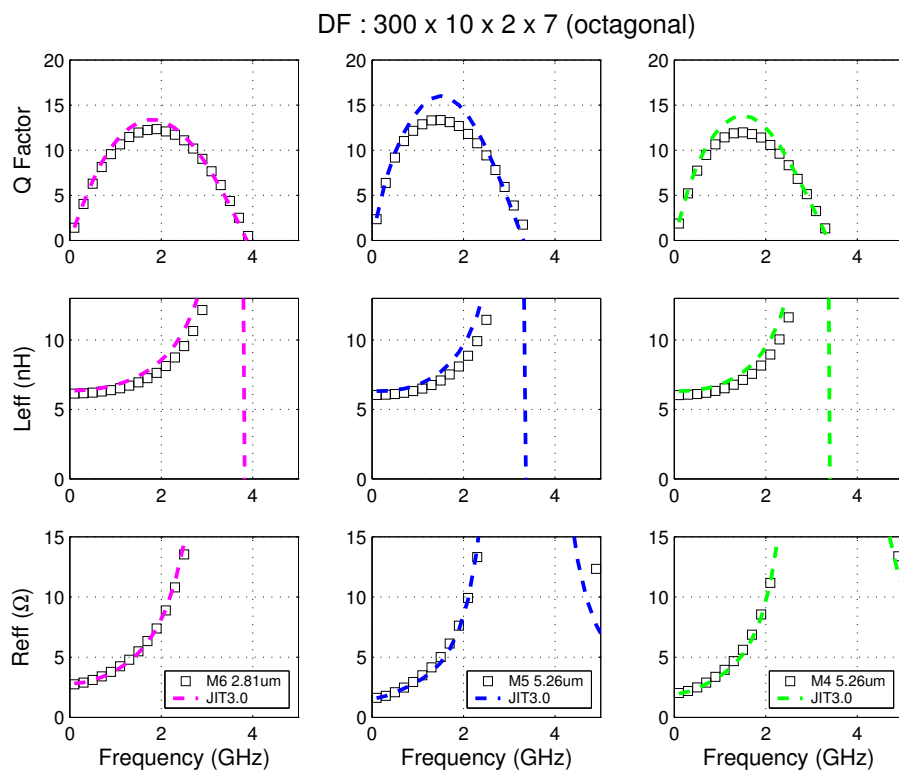


FIGURE 8.86 Inductor Model Verification

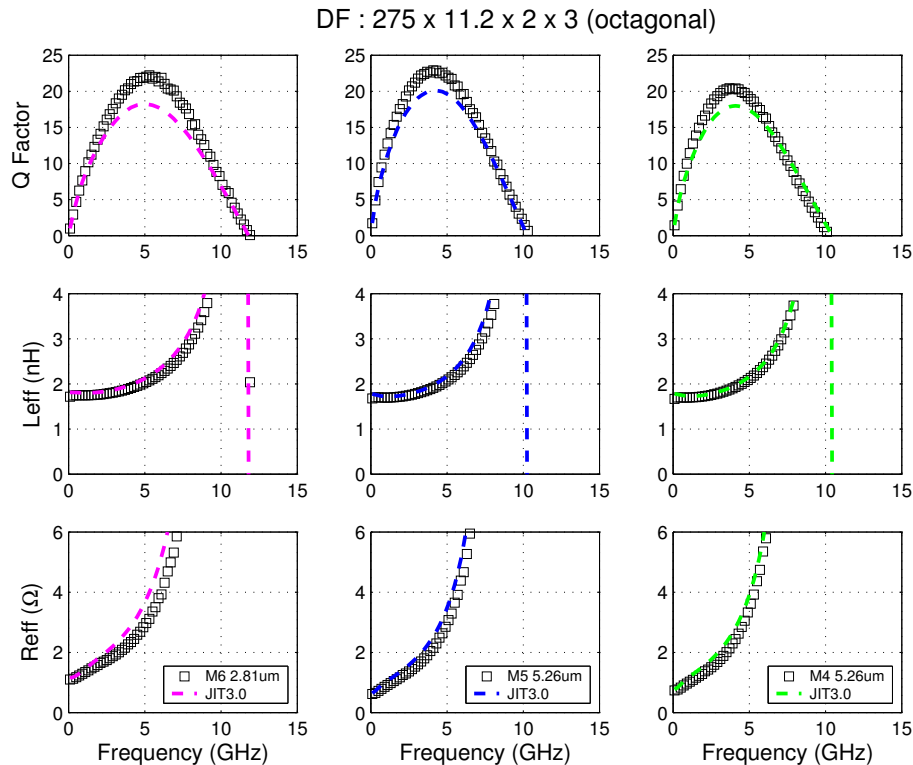


FIGURE 8.87 Inductor Model Verification

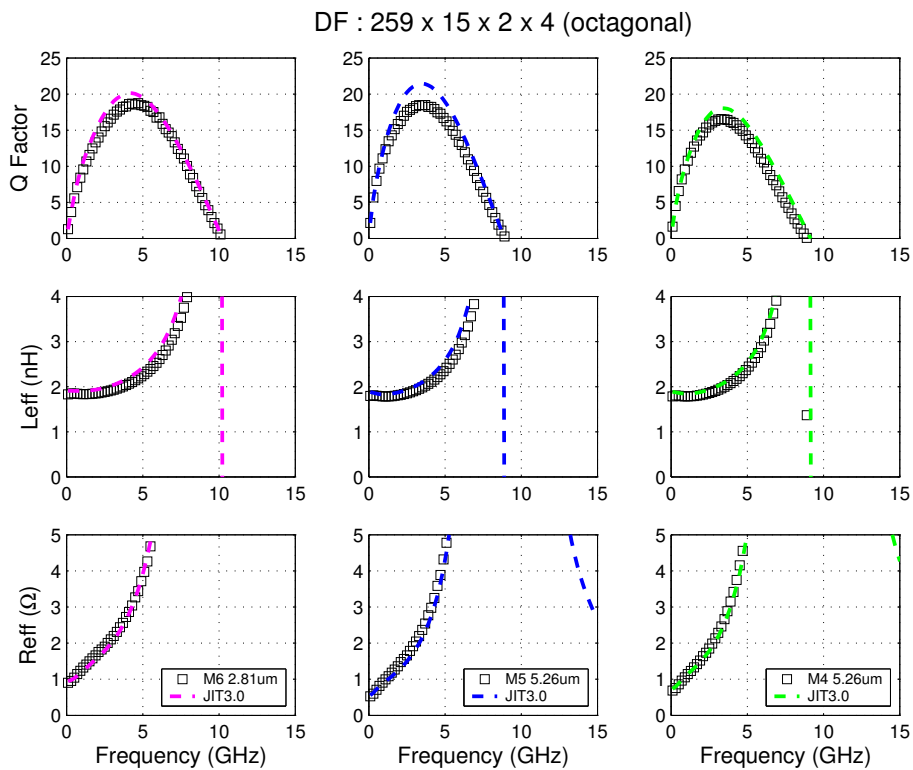


FIGURE 8.88 Inductor Model Verification

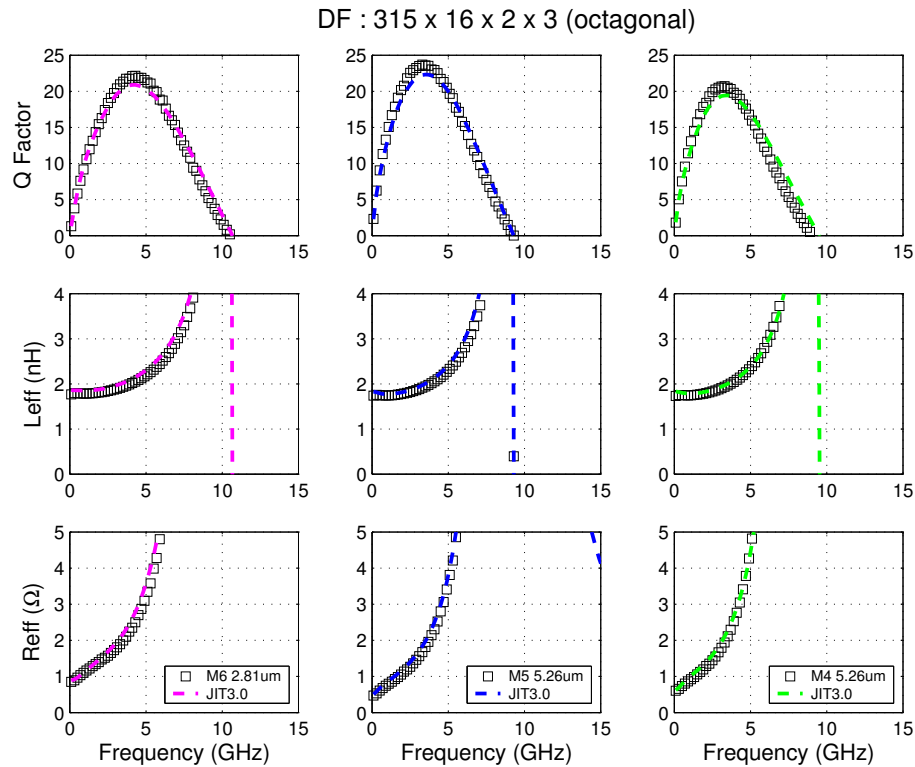


FIGURE 8.89 Inductor Model Verification

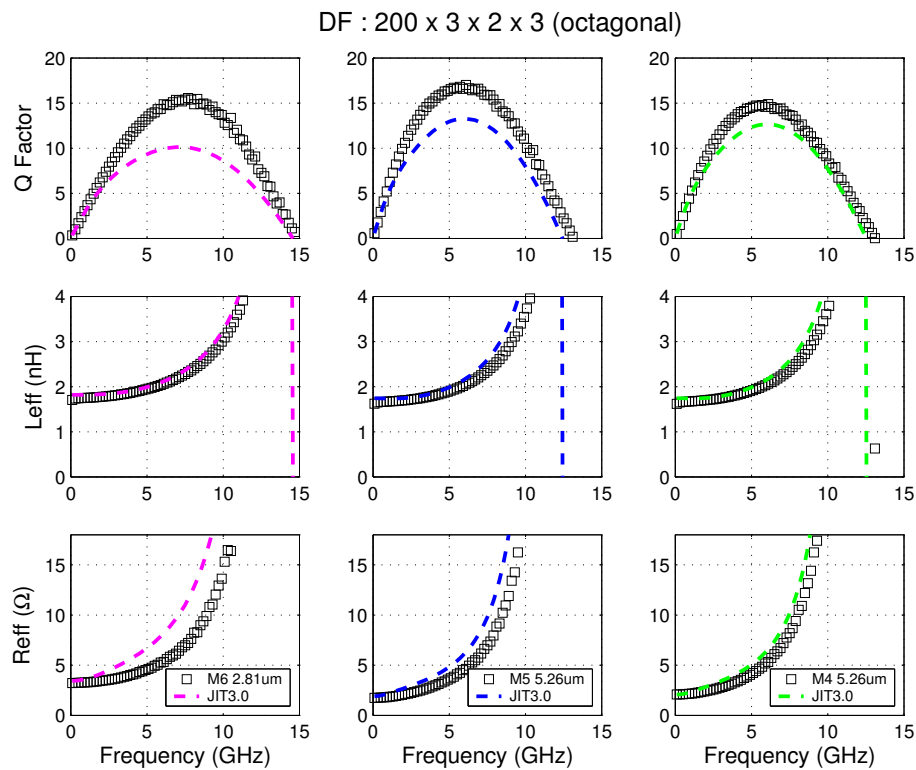


FIGURE 8.90 Inductor Model Verification

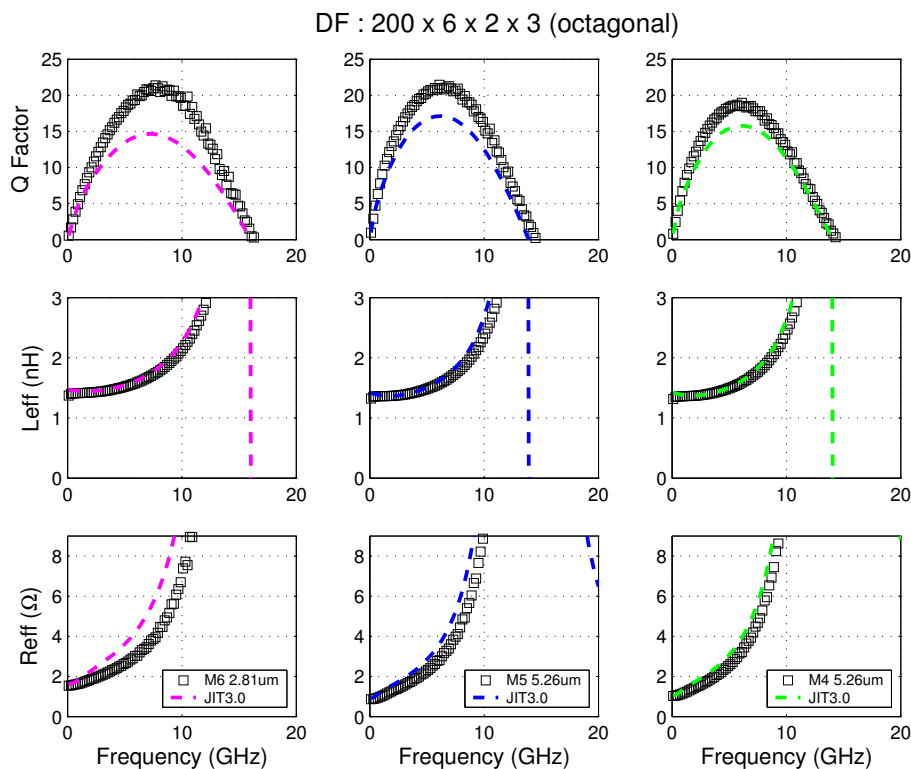


FIGURE 8.91 Inductor Model Verification

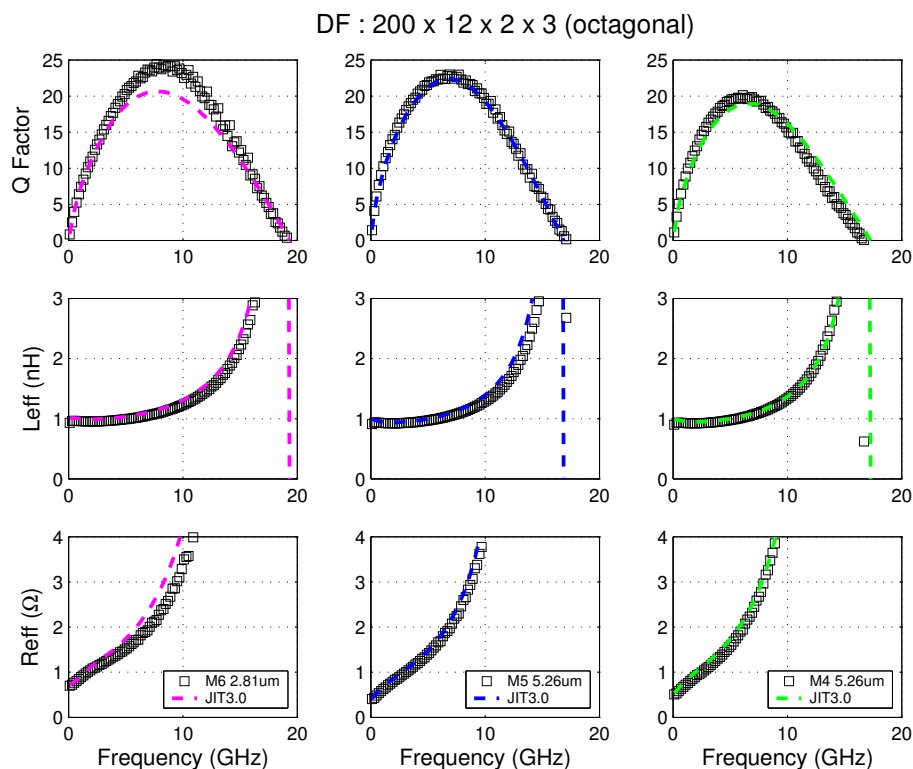


FIGURE 8.92 Inductor Model Verification

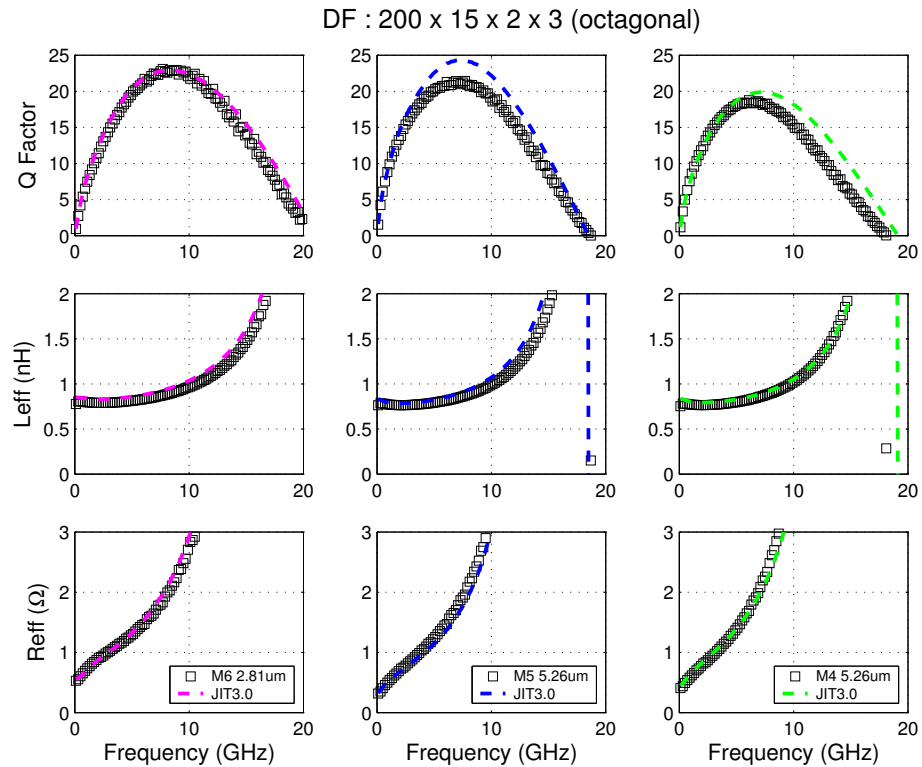


FIGURE 8.93 Inductor Model Verification

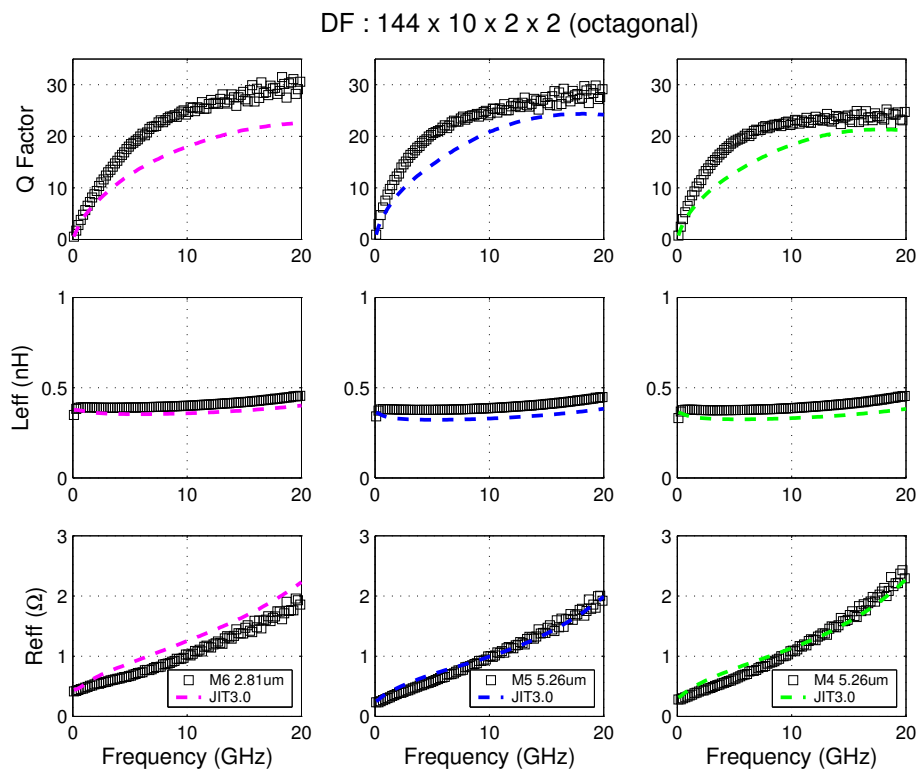


FIGURE 8.94 Inductor Model Verification

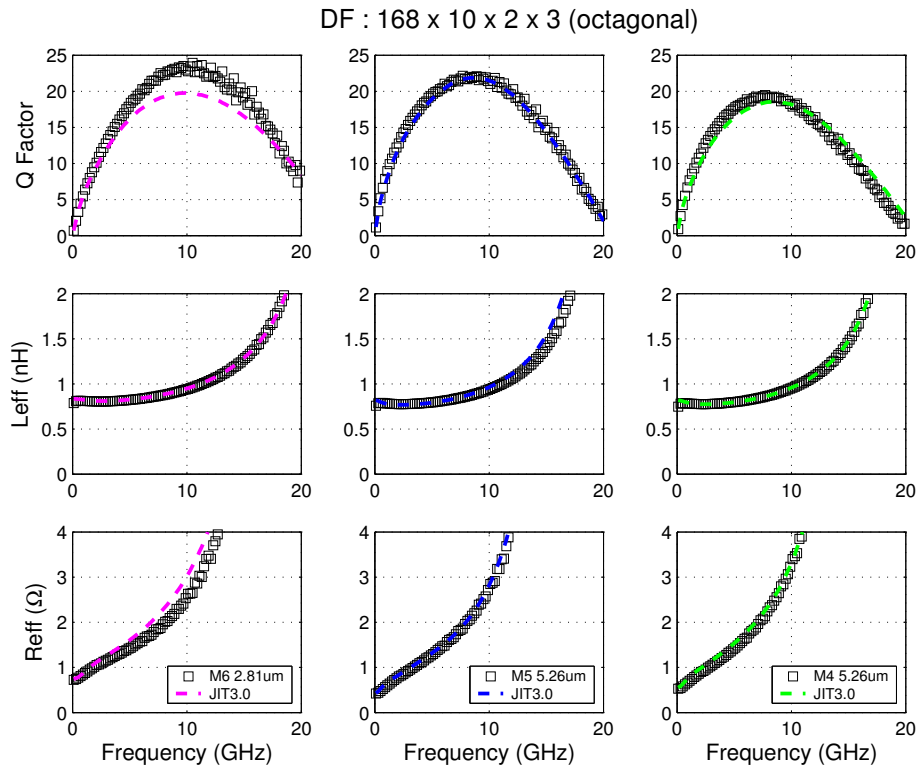


FIGURE 8.95 Inductor Model Verification

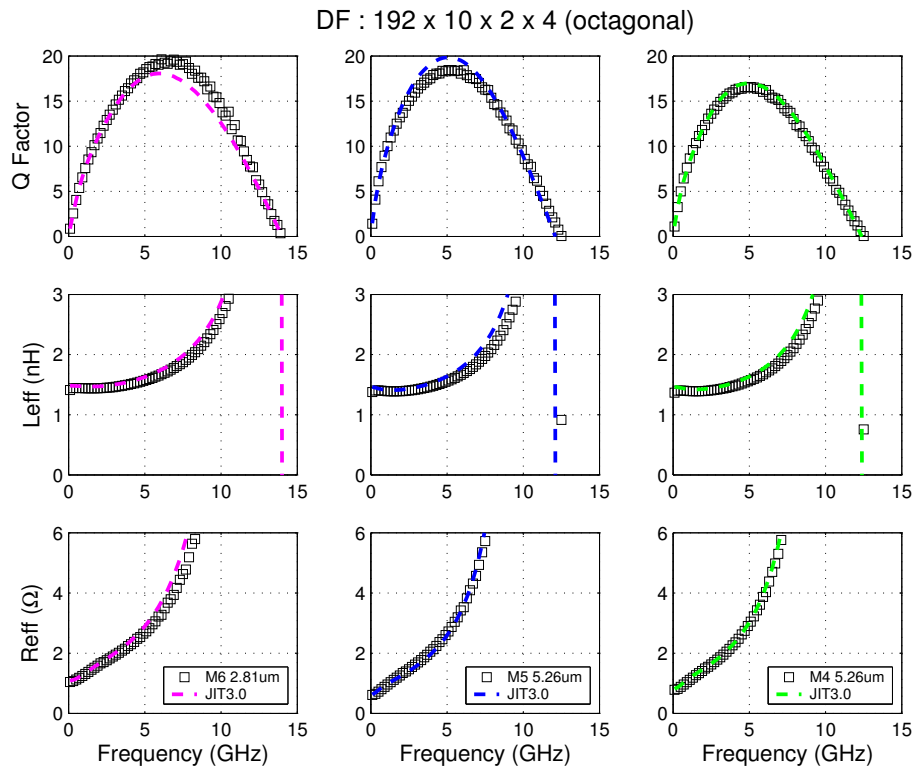


FIGURE 8.96 Inductor Model Verification

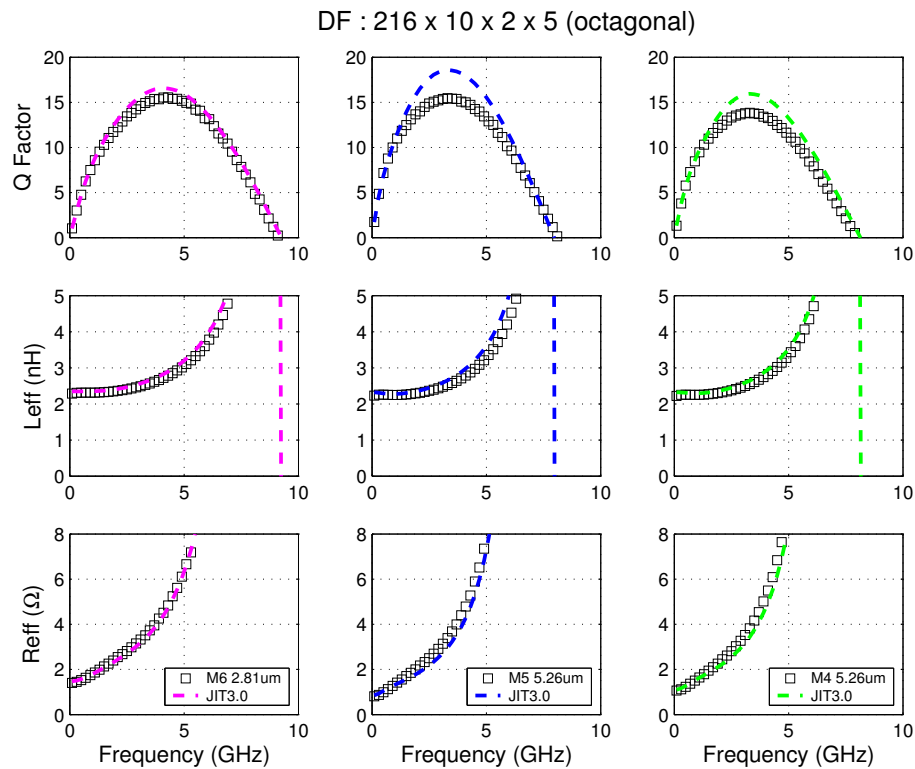


FIGURE 8.97 Inductor Model Verification

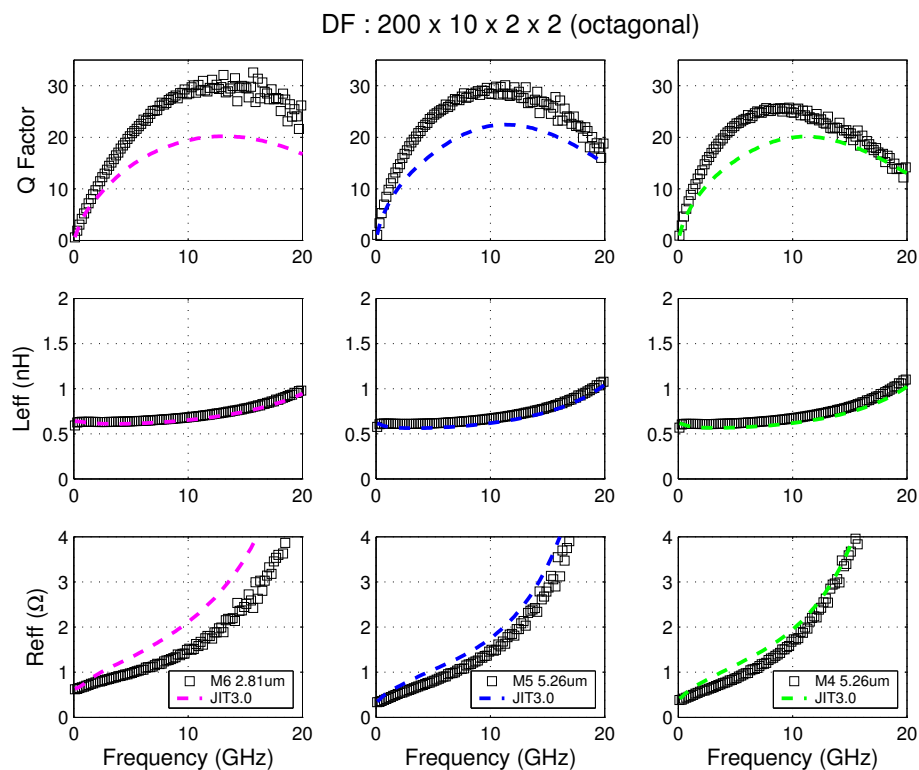


FIGURE 8.98 Inductor Model Verification

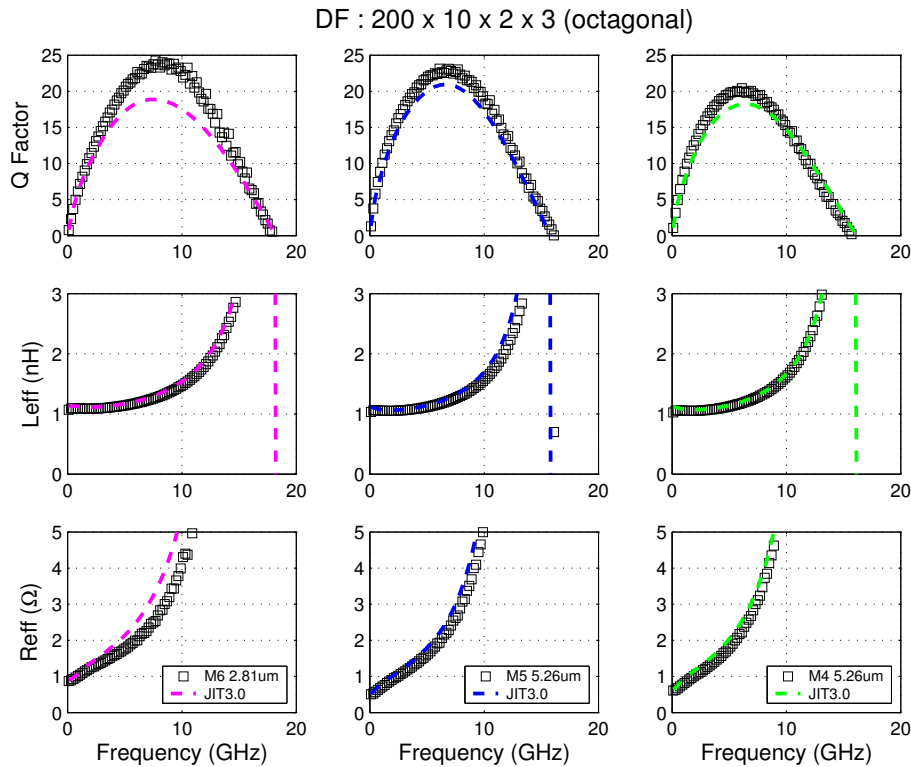
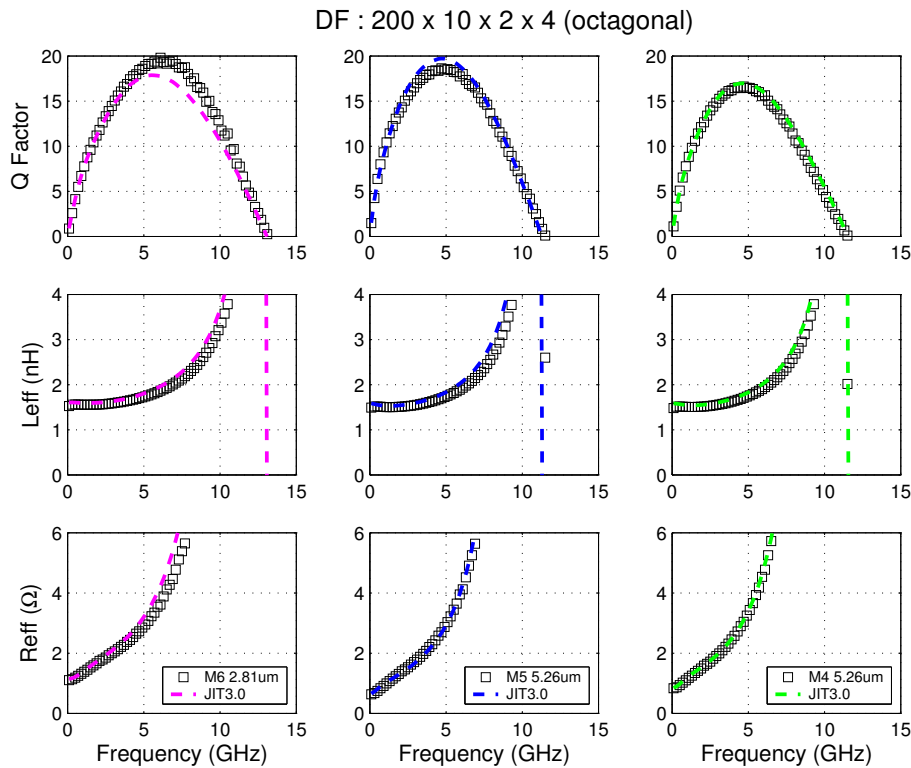


FIGURE 8.99 Inductor Model Verification



8.3.2 Validation with EM Simulation

The single-ended octagonal inductors is the newest addition to the JIT. Since there is no silicon data yet, the QLR models have been compared to ADS Momentum 2.5 EM simulations. The accuracy of the inductance models has already been established using FastHenry (Section 8.2.6.4.2 on page 386). Several examples in 5.26 μ m metal are shown in Figure 8.100 through Figure 8.105. The title of each Q,L,R plots contains geometry and special layout information with “UPV” for vertical underpass exit, “UPH” for horizontal underpass exit and “gnd” for ground shield configuration.

FIGURE 8.100 Inductor Model Verification - EM Simulation

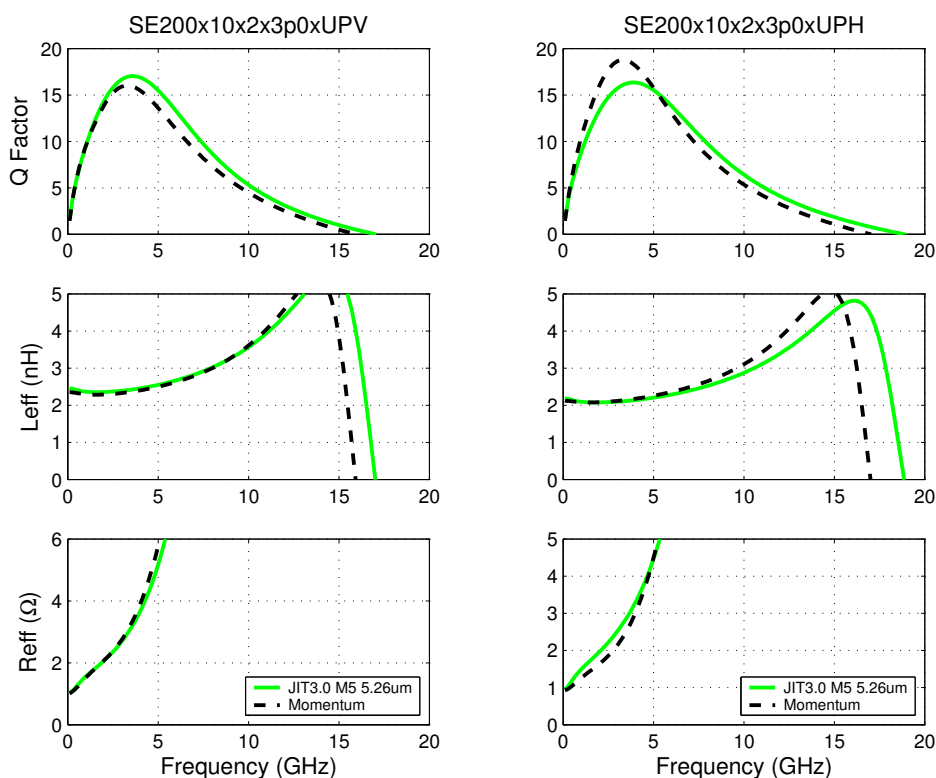


FIGURE 8.101 Inductor Model Verification - EM Simulation

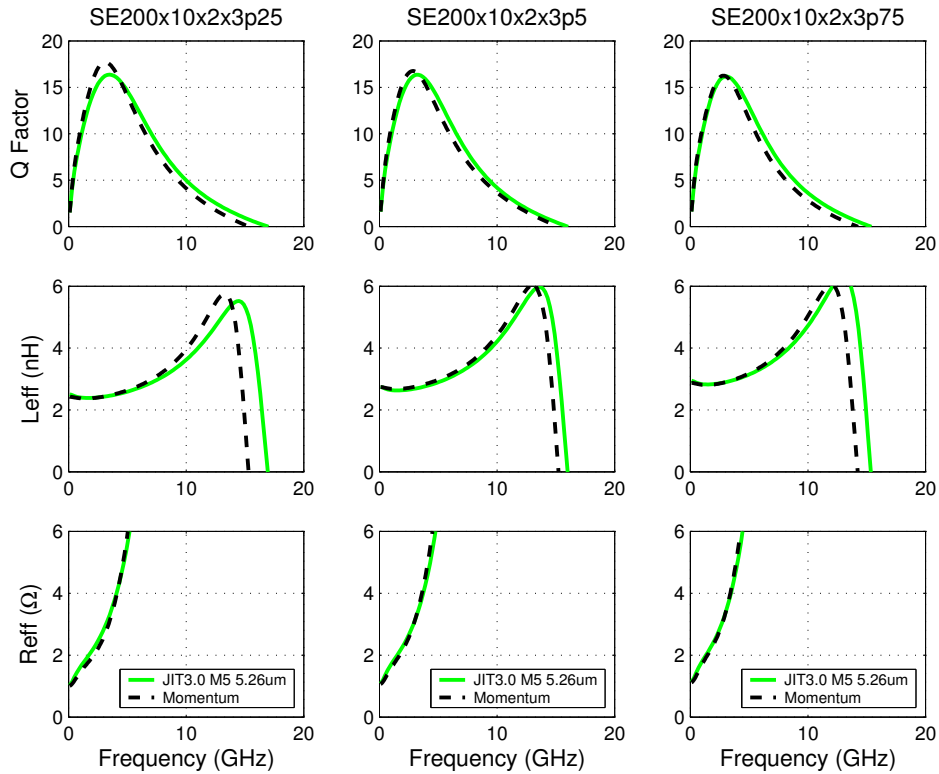


FIGURE 8.102 Inductor Model Verification - EM Simulation

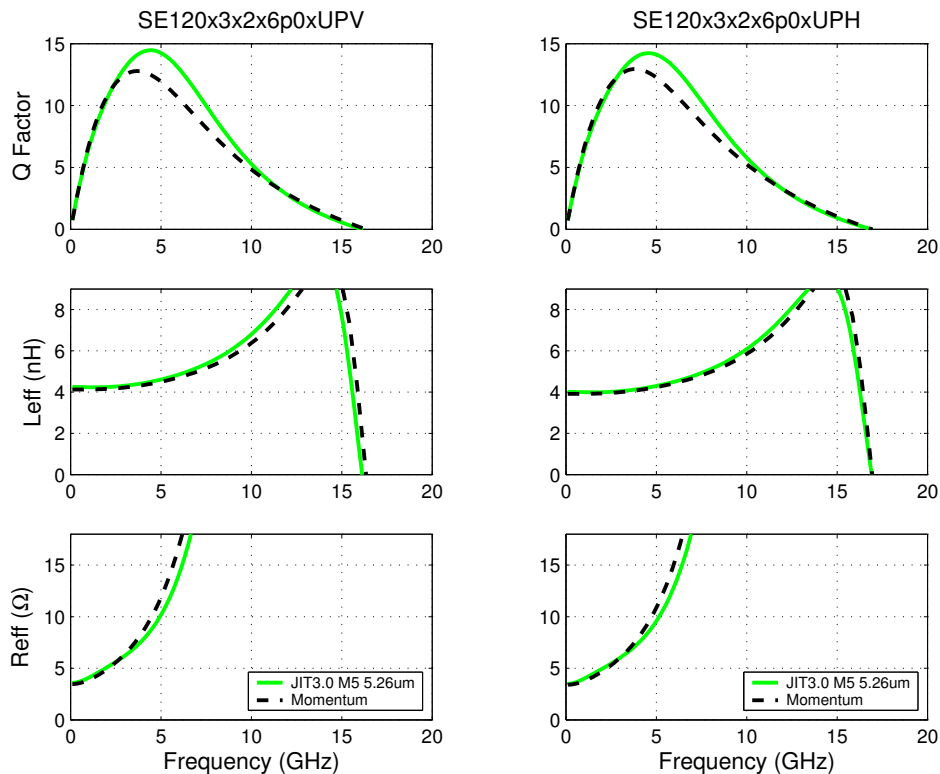


FIGURE 8.103 Inductor Model Verification - EM Simulation

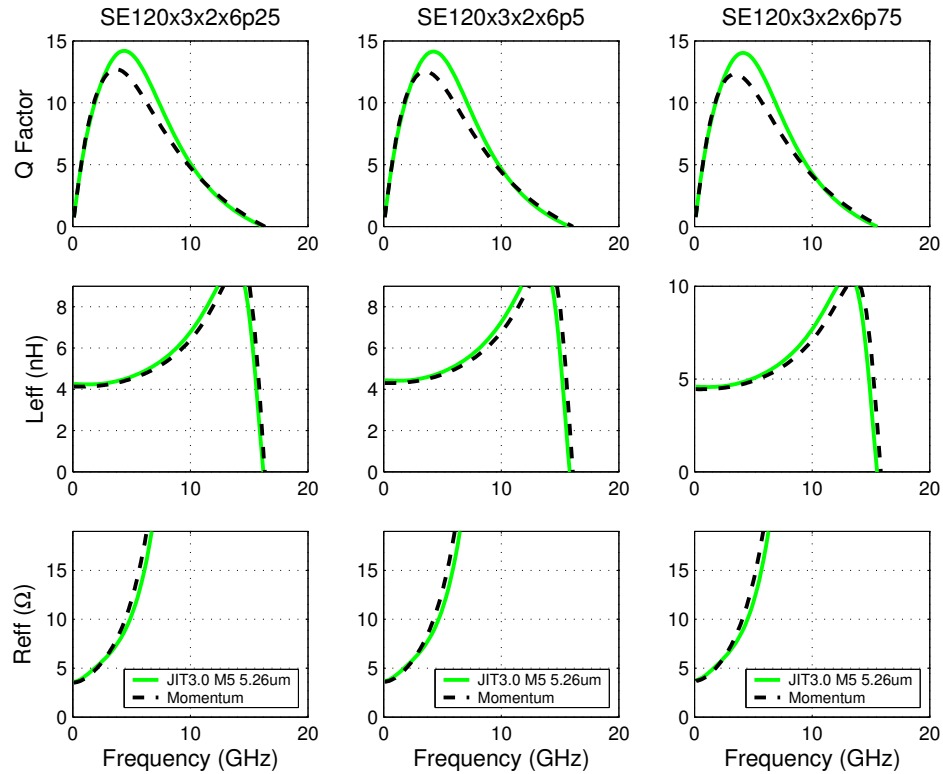


FIGURE 8.104 Inductor Model Verification - EM Simulation

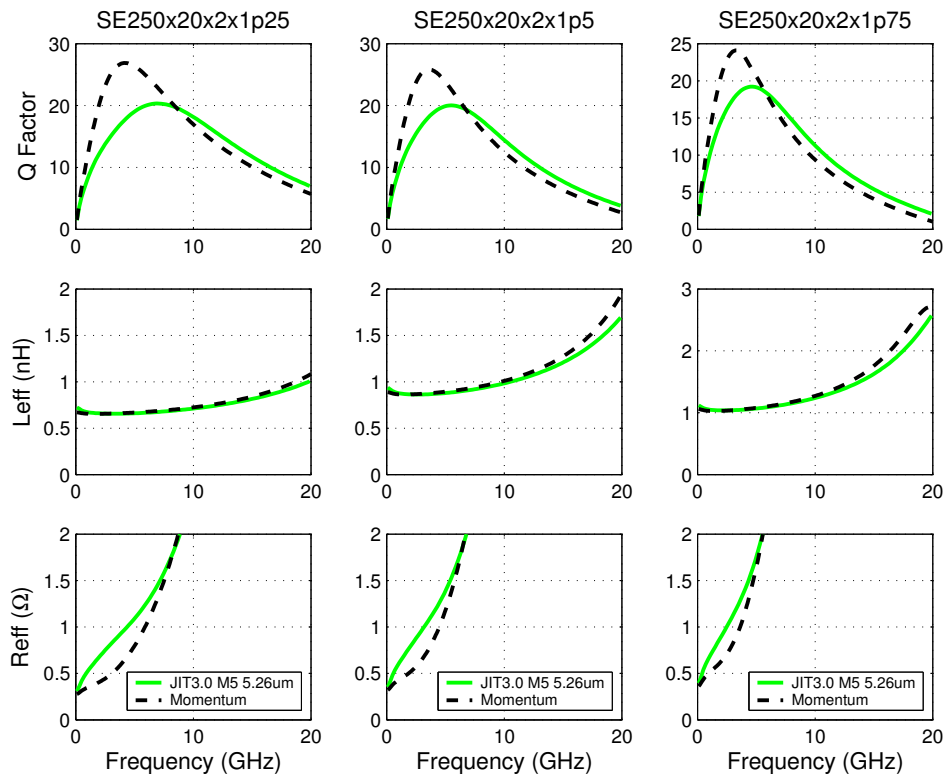
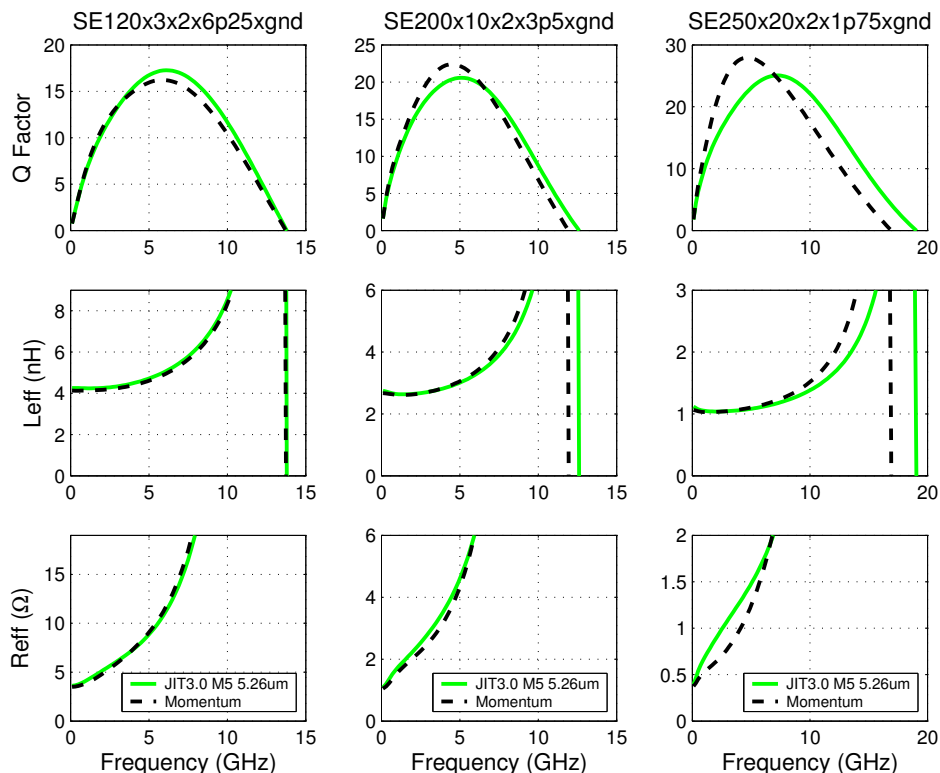


FIGURE 8.105 Inductor Model Verification - EM Simulation



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8.4 Inductor Statistical and Corner Models

8.4.1 Corner Models

The corner performance is simulated using the corner model card in the design kit. The equivalent circuit component values are provided by the JIT through the CDF with their nominal value. These nominal values are then multiplied by a factor within the model card to obtain the corner case which was optimized to maximize (fast corner) or minimize (slow corner) the peak Q value of the inductor. The multiplier factors are based on the $\pm 3\sigma$ electrical spec limits of the parameters that affect the value of the individual circuit components. The corner case can be simulated by changing the inductor corner from "NOM" to either "SLOW" or "FAST" under the "Set Active Library" menu in the Spectre "Analog Environment". The multiplier factors are tabulated in Table 8.3.

The component C_x is not represented by an individual element in the sub circuit diagram but is rather a part of the interwinding capacitance C_p . It is representing the capacitance between spiral trace and cross-overs. In its corners, the cross-over and turn-to-turn capacitances move opposite while they are both part of the feed forward capacitance C_p shown in Figure 8.6 and Figure 8.7. The corner value of component C_p is calculated in the sub circuit model card from these 2 parts resulting in an improved corner model.

TABLE 8.3 Corner Component Multipliers

Component	Multiplier	Fast	Nominal	Slow
L_s^2	lsig	0.980	1.00	1.020
R_s^1 (5.26um metal)	rsmsig_5u	0.730	1.00	1.270
R_s^1 (2.81um metal)	rsmsig_3u	0.790	1.00	1.210
C_{ox}^2	coxsig	0.930	1.00	1.070
C_p^2 (5.26 um metal)	cpsig_3u	1.230	1.00	0.770
C_p^2 (2.81 um metal)	cpsig_3u	1.200	1.00	0.800
C_x^2	cxsig	0.740	1.00	1.260
R_{sub}^2	rsbsig	0.710	1.00	1.290
C_{sub}^2	csbsig	0.990	1.00	1.010

PCM notes:

1. The R_s multiplier is consistent with the common PCM and ESPEC limits.
2. There is no PCM monitoring.

8.4.2 Statistical Model

The statistical models allow simulation of inductors as affected by the variation of process parameters. These variations are on a global scale affecting the variation of inductors over a larger set of wafers or wafer lots rather than within a given wafer. Generally it is observed that the performance variation between a particular inductor over a wafer is below the resolution of the RF measurements. Therefore, the mismatch of 2 closely located inductor structures is negligible; however mismatch is enabled within the statistical model card and set to an empirical number of 0.1σ . In comparison to the corner model card, the statistical model is not optimized under the constraint of maximizing or minimizing a particular figure of merit such as Q peak. Consequently, the statistical model is more meaningful in exploring the inductor performance space as dictated by the espec.

Since inductors are fairly large devices and their measurement involves a RF network analyzer, inductors don't lend itself to inline process control. Thus these structures are not monitored like process variables that are defined in the espec. Consequently, there is no data available on an inductor population to enable statistical modeling. Instead, the statistical models are based indirectly on the ESPEC via the corner multipliers of the component values described in the previous section. This method corresponds to the forward propagation of variance. The $\pm 3 \sigma$ variations in the component multipliers propagate through the Spectre model to simulate the device electrical behavior [2].

The statistical model cards were verified for the convergence of the average Qpeak to the nominal Qpeak obtained with the corner model card. Convergence to within 0.1σ is typically achieved with a sample size of less than 100 Monte Carlo simulations.

8.5 Model Update History

Table 8.4 lists the model updates with each revision. Unlisted model revisions indicate that no changes have occurred in that revision. Toolbox JIT3.0 represents a major change with added new functionality, simplified corner sub circuits and more accurate models.

TABLE 8.4 Model Updates in JIT3.0

JIT3.0 Update Detail	Devices	Reason	Impact on User
Active ground shield	Single-Ended Inductor	Improve Q.	Inductors with higher Q.
Modeling of packaging compound	All	Improved accuracy.	Model takes into account the capacitance increase through the packaging material.
New substrate resistance model	All	Improved accuracy, models are calibrated to Jazz silicon.	Better models for roll-off section of Q curve.
Cox and Cp account for distributed effect	All	Improved accuracy.	Better models for roll-off section of Q curve and self-resonant frequency.
Additional interwinding capacitance from port to center-tab	Differential Inductor	Improved accuracy.	More accurate prediction of self-resonant frequency.
Interchange of ports 1 and 2	Single-Ended Inductor	Align models with layout PCELL.	Q performance of port1 and port2 shifts. Port2 identifies the outer (non-underpass) port and has the higher Q due to lower Cox.
Proximity effect warning	Differential Inductor	Prevent usage of devices that are not modeled well.	The warning alerts users of dense inductor designs, whose Q is over predicted by the model.
New subcircuit model cards and optimized corner multipliers	All	Simplify kit maintenance and improve corner accuracy.	Corner results changed. The inductance corner flipped.
New octagonal inductors	All	Improve Q	Inductors with higher Q

8.6 References

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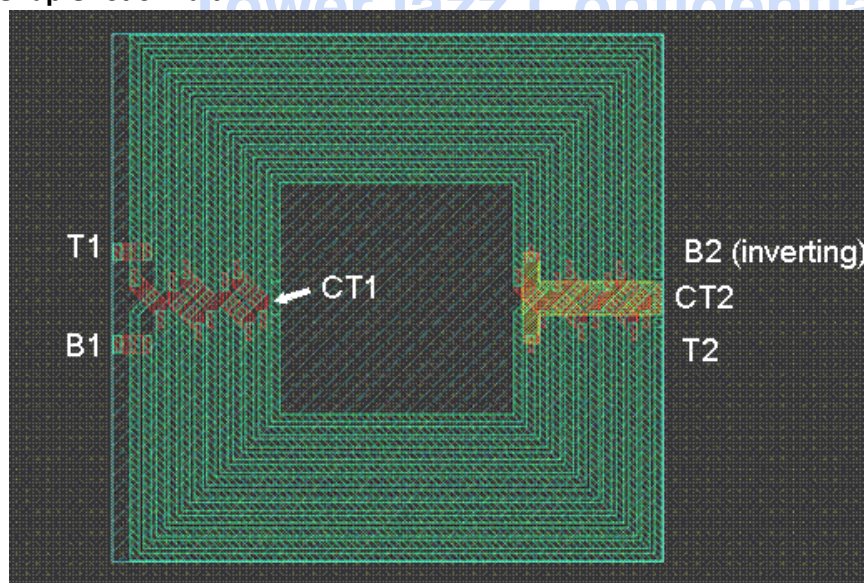
9.0 Balun Model

9.1 Model usage guidelines

9.1.1 Layout parameters

Most SBC18 design kits includes 3 discrete balun models in 2.81um metal 6, in 5.26um metal 5 and in 5.26um metal 4 processes that were designed for cellular phone and wireless LAN applications. The acronym balun stands for “balanced-to-unbalanced” conversion and defines a specific transformer configuration that converts a singled-ended signal to a balanced or differential signal. In this configuration, one port of the primary coil is at ground with the center tab left floating (single-ended), while the two ports of the secondary coil provide 2 output signals with a 180 degree phase difference referenced to the grounded center tab (balanced). The balun is a subset of a transformer and other configurations like balanced-to-balanced, unbalanced-to-unbalanced non-inverting and unbalanced-to-unbalanced inverting are realizable with the balun component. Going forward the acronym balun is used for the transformer in general. The layout cells are drawn for the balun configuration with a center tab to the secondary coil but omitting the tab at the primary coil. If a non-balun configuration is to be realized then the tab layout needs to be modified. Figure 9.1 shows a layout snap shot of the balun5 component.

FIGURE 9.1 Snap Shot of Balun



9.1.2 Sub-circuit representation

The equivalent circuit representation of the balun is shown in Figure 9.2. This topology has 70 circuit components. Most of the complexity is caused by the requirement to model center tab connections at primary and secondary coils. The individual model components, based on physical models and computed using geometrical and electrical process specification (espec) information, are listed in Table 9.1.

FIGURE 9.2 Sub-Circuit model for balun

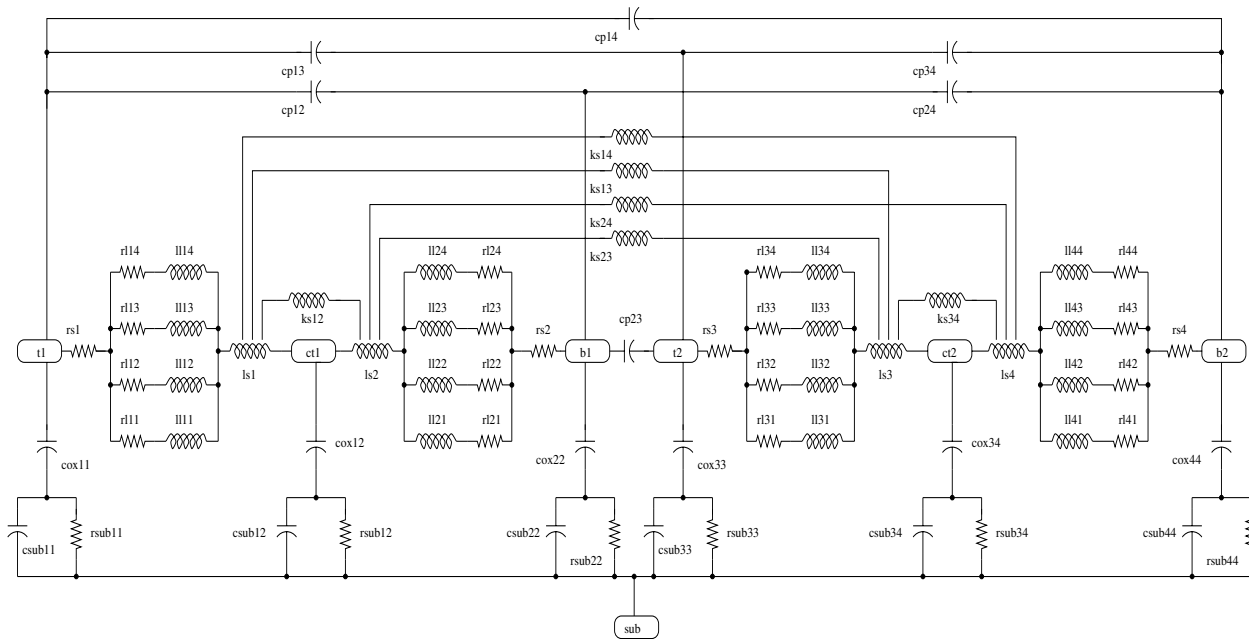


TABLE 9.1 Circuit Components

t1, b1, t2, b2	primary and secondary coil tabs
ct1, ct2	center tabs
csub#	Substrate capacitances
rsub#	Substrate resistances
cox#	Oxide capacitances
cp#	Interwinding and cross-over capacitance
rs#	cross-over via resistances
ls#	series inductances
rl#	Ladder resistance components
ll#	Ladder inductance components
kk#	Mutual inductances

The radio frequency (RF) skin effect is modeled using a ladder circuit. The balun model is an extension of the differential inductor model. It features 2 differential inductors, additional interwinding capacitances accounting for the electric coupling between the terminals and mutual inductance terms between all series inductances. More details on the component calculation and references can be found in the inductor section of the design manual.

9.1.3 Supported Baluns and Application

The balun components can be accessed in the component library under the name “balun”. After selecting the instance, a specific balun design can be chosen from the “Inductance” pull down menu selecting either 1nH, 5nH or 10nH. This inductance value is only an approximate number that was used as an initial design target.

The 3 balun components were designed for the most prominent wireless applications of 0.9 GHz (analog cellular), 1.8-2.0 GHz (digital cellular), 2.45 GHz (Bluetooth, networking 802.11b/g), 5.2-5.8 GHz (networking 802.11A) and 3.1-10.6 GHz (ultrawideband technology). Components “balun5” and “balun10” are useful for 0.9, 1.9 and 2.45 GHz frequencies while component “balun1” can be used in the 5.5 GHz area and beyond.

9.1.4 Balun Corner Models

The Balun corner models follow the inductors. Refer to Section 8.4.

9.1.5 Balun Configurations

The balun or transformer component can be used in various configurations which are all accommodated by the model. Some possible configurations are shown in Figure 9.3 through Figure 9.6.

FIGURE 9.3 Unbalanced to Balanced

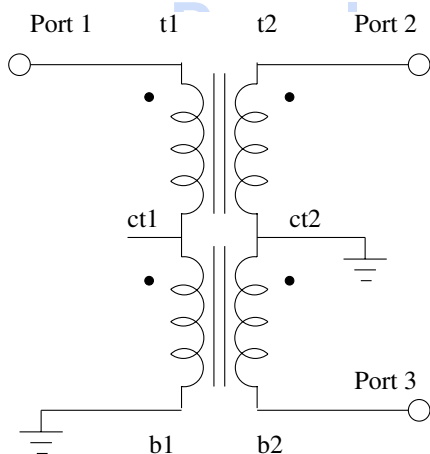


FIGURE 9.4 Balanced to Balanced

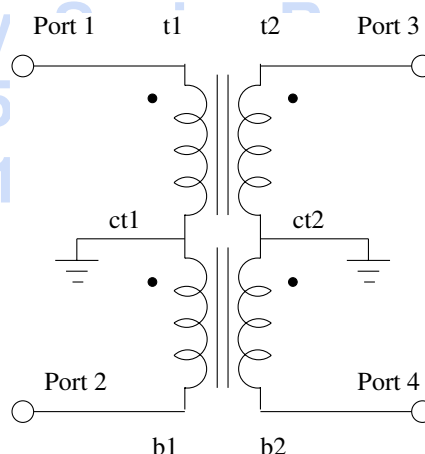
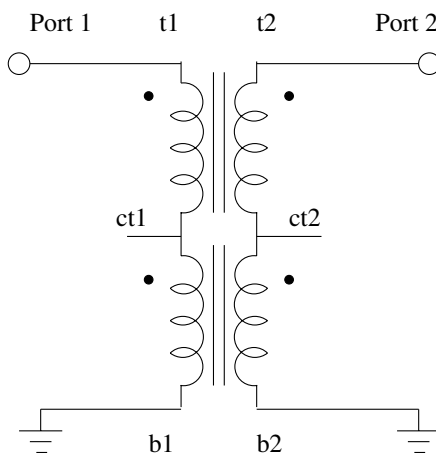
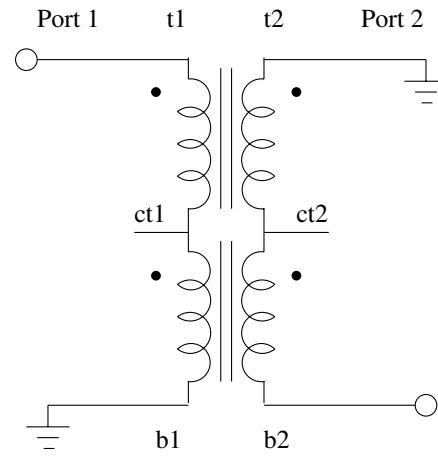


FIGURE 9.5 Unbalanced to Unbalanced (non-inverting)**FIGURE 9.6 Unbalanced to Unbalanced (inverting)**

9.2 Balun Model Verification

9.2.1 AC Analysis and Time Domain Characterization

The balun configuration of Figure 9.3 was simulated in Spectre using ac and transient analysis. An example plot for the 5nH balun component in 3um metal 6 is shown in Figure 9.7. The left-hand plots display the simulated amplitude and phase imbalance for the voltage between the balun output ports “t2” and “b2”, obtained from an ac frequency sweep of a 1V input signal. On the right-hand side the time domain response to a 1.9 GHz sinusoidal 1V signal at port “b1” is shown. The output signals at ports “t2” and “b2” have a 180 degree phase difference, with “t2” following the input in phase while “b2” is inverted. The output signal swing is attenuated by the balun insertion loss which is in addition to the -3dB reduction accounting for the division of the input power between both terminals. Note that the inverting terminal is diagonally across from the input signal terminal in the circuit diagram, while it is directly across for the layout component [1], Figure 9.1. The results of the ac analysis are recorded at several operating frequencies of interest in Table 9.2 and Table 9.3 to facilitate the choice of balun.

FIGURE 9.7 AC & Transient Response of 5 nH Balun (Unbalanced-to-Balanced)

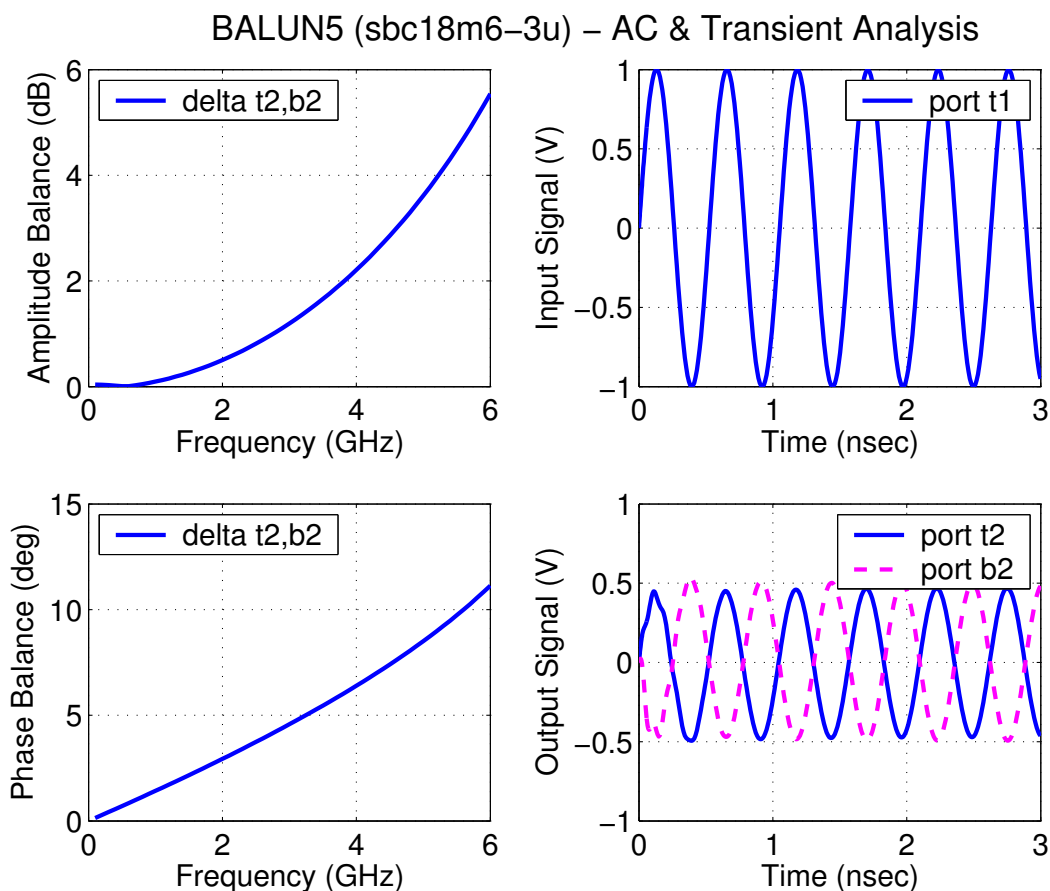


TABLE 9.2 Amplitude Balance

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Amplitude Balance in dB				
<i>Balun</i>	<i>0.90GHZ</i>	<i>1.90GHZ</i>	<i>2.40GHZ</i>	<i>5.50GHZ</i>
balun1_sbc18m6_3u	0.02	0.10	0.15	0.72
balun1_sbc18m5_6u	0.02	0.08	0.12	0.61
balun1_sbc18m4_6u	0.02	0.09	0.14	0.67
balun5_sbc18m6_3u	0.07	0.45	0.74	4.50
balun5_sbc18m5_6u	0.10	0.53	0.86	5.40
balun5_sbc18m4_6u	0.10	0.53	0.87	5.32
balun10_sbc18m6_3u	0.21	1.08	1.78	15.10
balun10_sbc18m5_6u	0.28	1.37	2.26	21.37
balun10_sbc18m4_6u	0.27	1.27	2.09	20.20

TABLE 9.3 Phase Balance

Phase Balance in degree				
Balun	0.90GHZ	1.90GHZ	2.40GHZ	5.50GHZ
balun1_sbc18m6_3u	0.17	0.43	0.60	1.84
balun1_sbc18m5_6u	0.13	0.34	0.45	1.36
balun1_sbc18m4_6u	0.15	0.40	0.54	1.59
balun5_sbc18m6_3u	1.28	2.78	3.58	9.74
balun5_sbc18m5_6u	1.09	2.38	3.08	9.17
balun5_sbc18m4_6u	1.17	2.62	3.42	10.35
balun10_sbc18m6_3u	1.88	4.22	5.54	28.97
balun10_sbc18m5_6u	1.58	3.61	4.81	54.98
balun10_sbc18m4_6u	1.68	3.94	5.29	88.14

9.2.2 High Frequency Characterization

The models were verified by comparing 2-port S-parameter measurements at 25 °C temperature with Spectre simulations. A single-ended configuration as shown in Figure 9.8 was used to extract the insertion loss which is a measure for the attenuation of a signal through the balun, the magnetic coupling coefficient K between primary and secondary coil and the impedance. Quality factor Q and inductance L were obtained using single-ended as well as open circuit configuration in Figure 9.9 and Figure 9.10. The equations used are listed below:

$$InsertionLoss = 20 \cdot \log[abs(S_{21})] \quad (EQ 1)$$

$$k = \sqrt{\frac{(Y_{11}^{-1} - Z_{11}) \cdot Z_{22}}{Im(Z_{11}) \cdot Im(Z_{22})}} \quad (EQ 2)$$

$$Q_p = \frac{Im(Z_{11})}{Re(Z_{11})} \quad (EQ 3)$$

$$L_p = \frac{Im(Z_{11})}{\omega} \quad (EQ 4)$$

$$Z_p = \frac{1}{Y_{11}} \quad (\text{EQ 5})$$

The Q, L and Z equations above give the results for the primary coil of the balun. By interchanging Z11 with Z22 and Y11 with Y22, the results for the secondary coil can be calculated. Besides extracting the impedance using Y-parameters, the Z-parameters were used for comparison. Depending on the method or equation used, different extraction results are obtained. Independent of the methodology, model and data do agree well.

FIGURE 9.8 Single-Ended Configuration

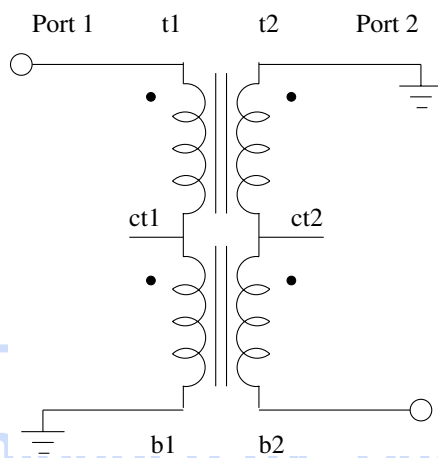


FIGURE 9.9 Open Circuit Secondary Coil

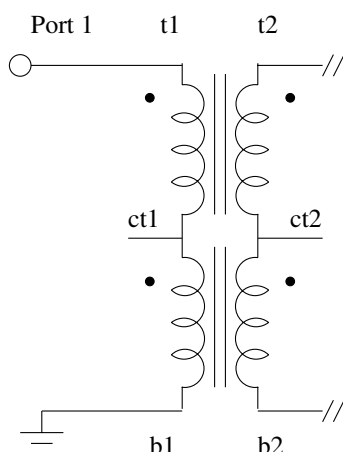
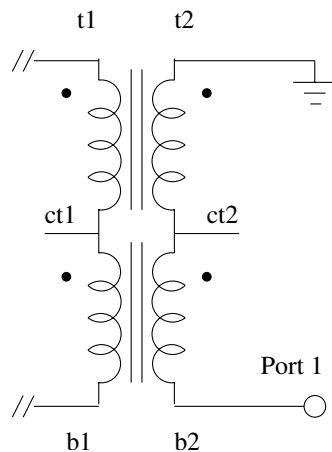


FIGURE 9.10 Open Circuit Primary Coil



The raw measurement results include the effects of ground-signal-ground frame and feed lines connecting the balun to the signal pads. These effects were deembedded by subtracting the pad admittance and by removing the feed lines through ABCD-matrix deembedding. The deembedded measurement and Spectre simulation results for the 3 baluns in 3um M4 and in 3um M3 are shown in Figure 9.11 through Figure 9.28. The title of

each plot identifies the balun name and the process type. The curves corresponding to the single-ended and open-circuit configuration are labeled “Spectre 2P” and “Spectre OC”, respectively.

A summary of the insertion loss at the operating frequencies of interest for the unmatched or untuned single-ended to single-ended configuration is provided with Table 9.4. This insertion loss is the attenuation across the balun to secondary coil port “b2”. The result on secondary coil port “t2” will be slightly different by the amplitude imbalance reported in Table 9.2. If the output signal is tabbed on both ports, then an additional -3dB is to be added to account for the division of the input power. The unmatched insertion loss can be improved by tuning the balun with a shunt capacitance [1].

TABLE 9.4 Insertion Loss

Insertion Loss in dB (unmatched)				
Balun	0.90GHZ	1.90GHZ	2.40GHZ	5.50GHZ
balun1_sbc18m6_3u	-13.85	-8.01	-6.39	-2.18
balun1_sbc18m5_6u	-13.78	-7.82	-6.10	-1.60
balun1_sbc18m4_6u	-13.82	-7.85	-6.13	-1.63
balun5_sbc18m6_3u	-3.71	-2.52	-2.41	-2.48
balun5_sbc18m5_6u	-2.61	-1.59	-1.55	-1.96
balun5_sbc18m4_6u	-2.81	-1.78	-1.75	-2.18
balun10_sbc18m6_3u	-2.75	-2.25	-2.27	-2.74
balun10_sbc18m5_6u	-1.83	-1.49	-1.58	-2.14
balun10_sbc18m4_6u	-1.97	-1.70	-1.83	-2.48

FIGURE 9.11 Model Verification - Insertion Loss, k, Q, L

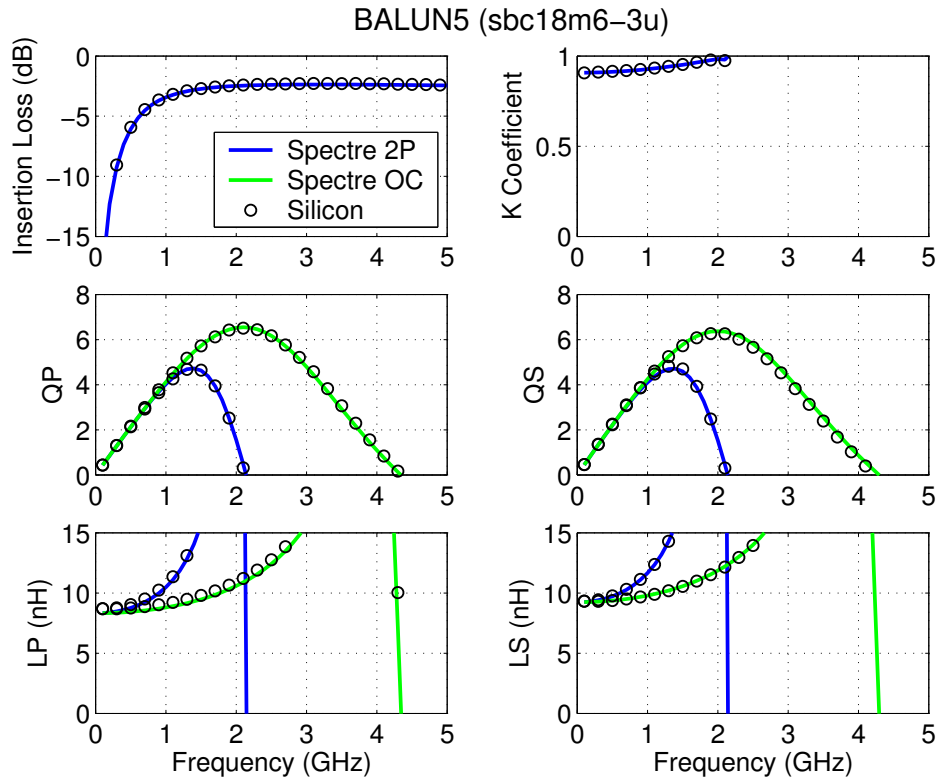


FIGURE 9.12 Model Verification - Impedance

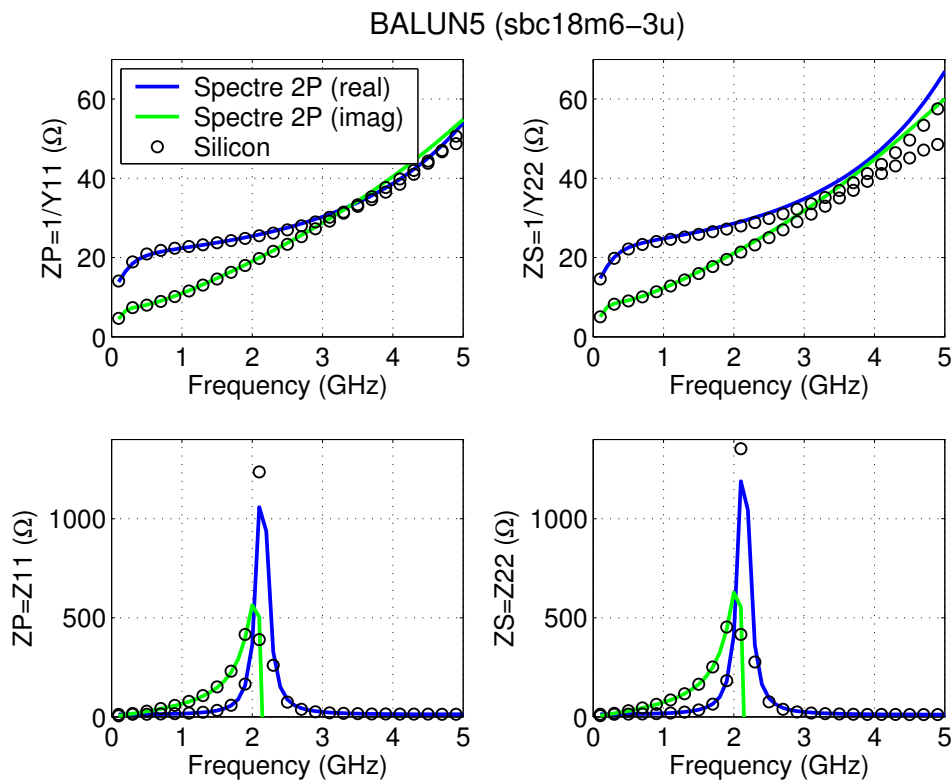


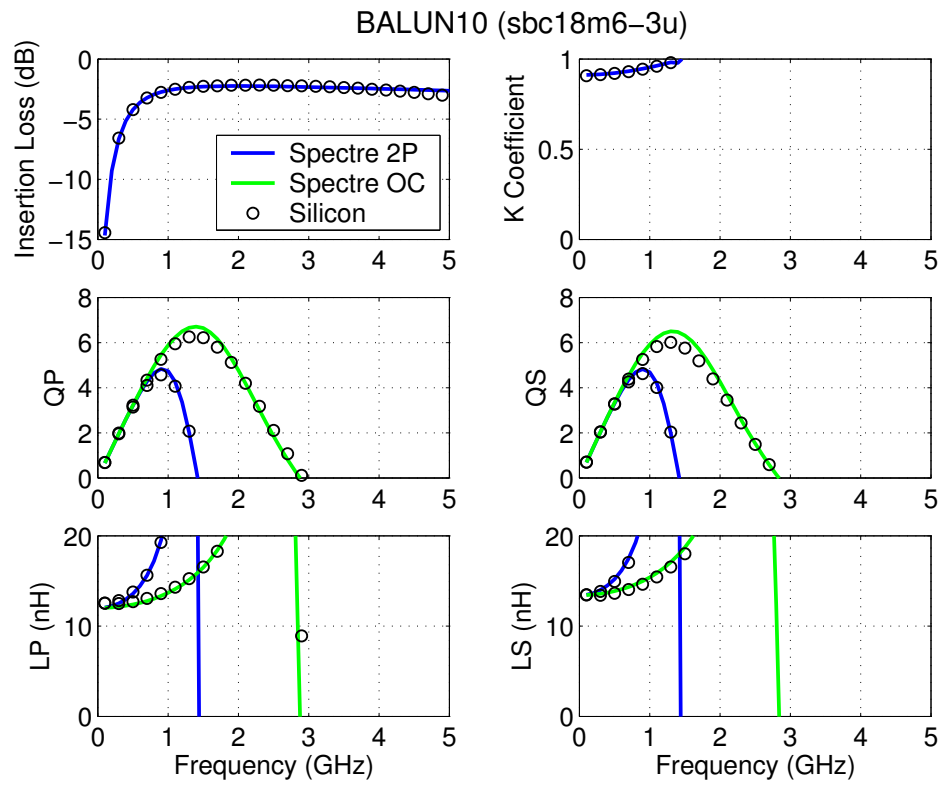
FIGURE 9.13 Model Verification - Insertion Loss, k , Q , L 

FIGURE 9.14 Model Verification - Impedance

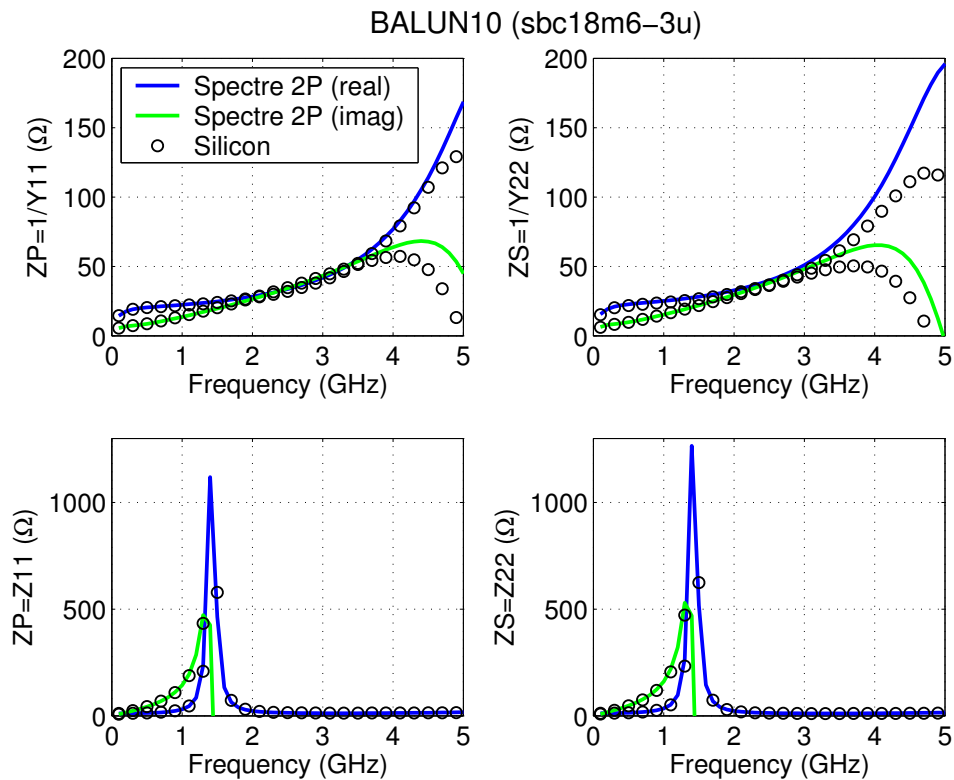


FIGURE 9.15 Model Verification - Insertion Loss, k, Q, L

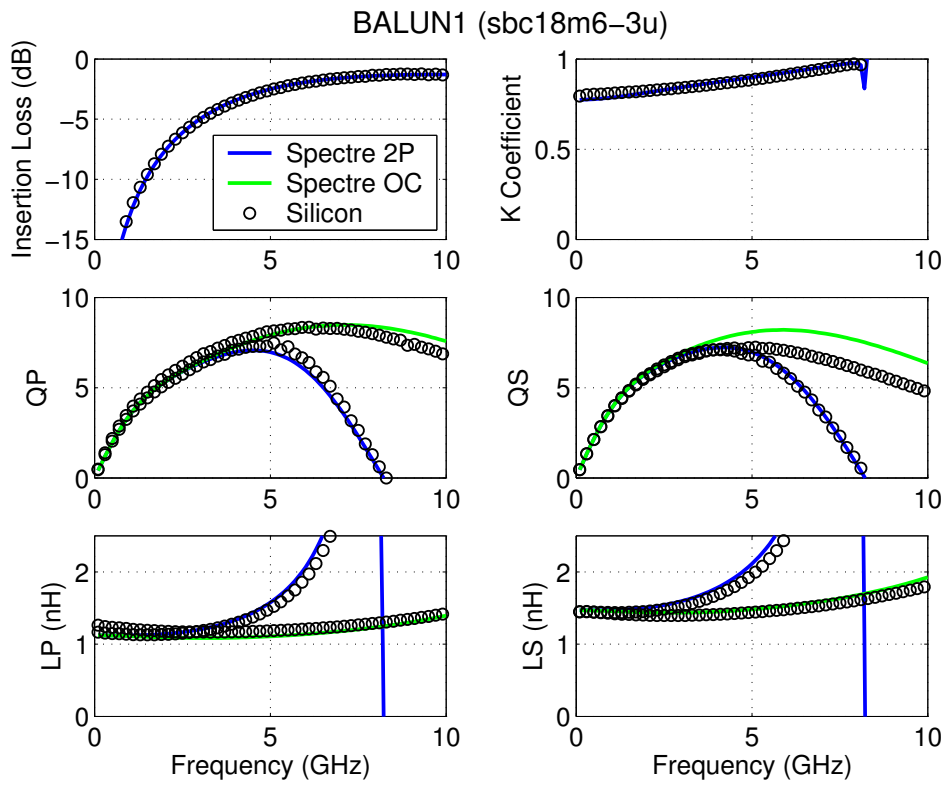


FIGURE 9.16 Model Verification - Impedance

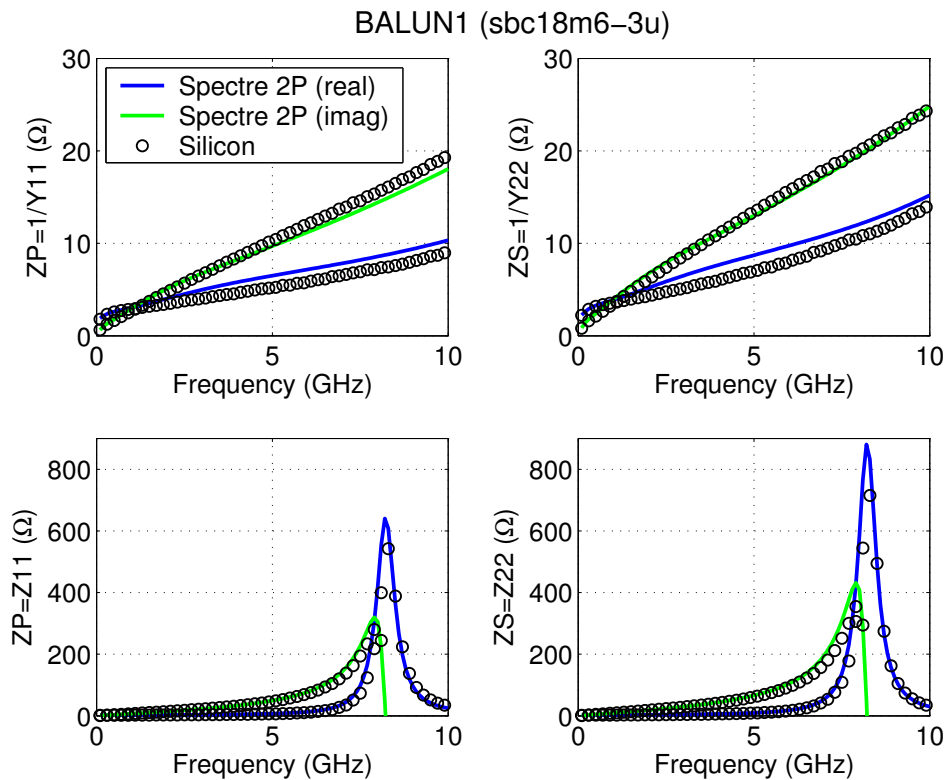


FIGURE 9.17 Model Verification - Insertion Loss, k, Q, L

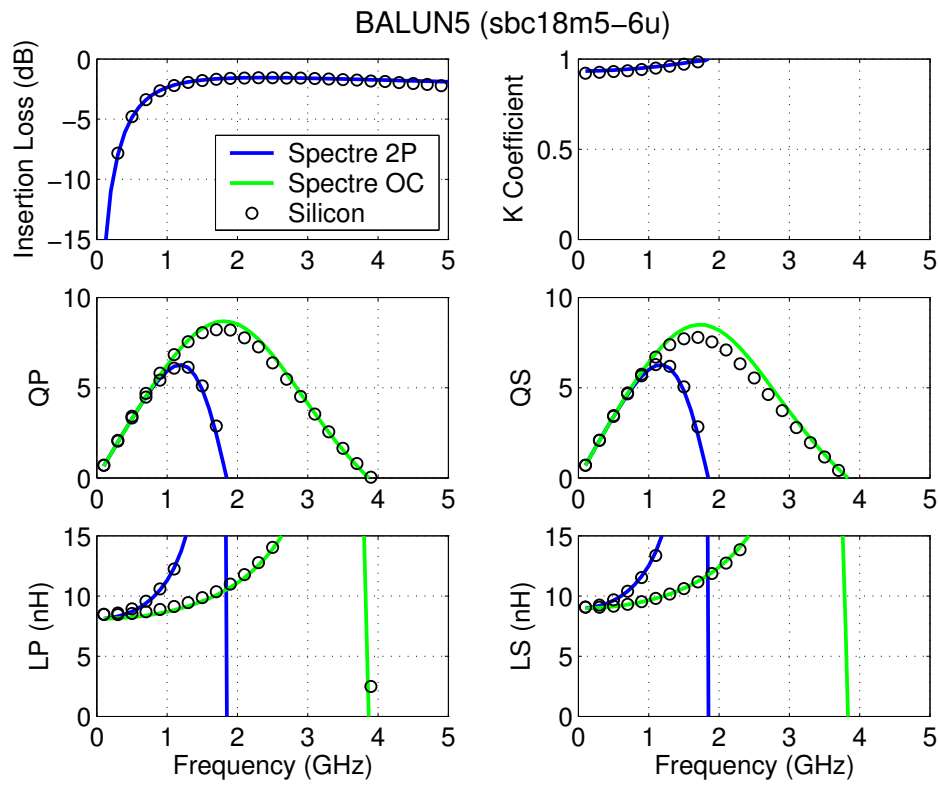


FIGURE 9.18 Model Verification - Impedance

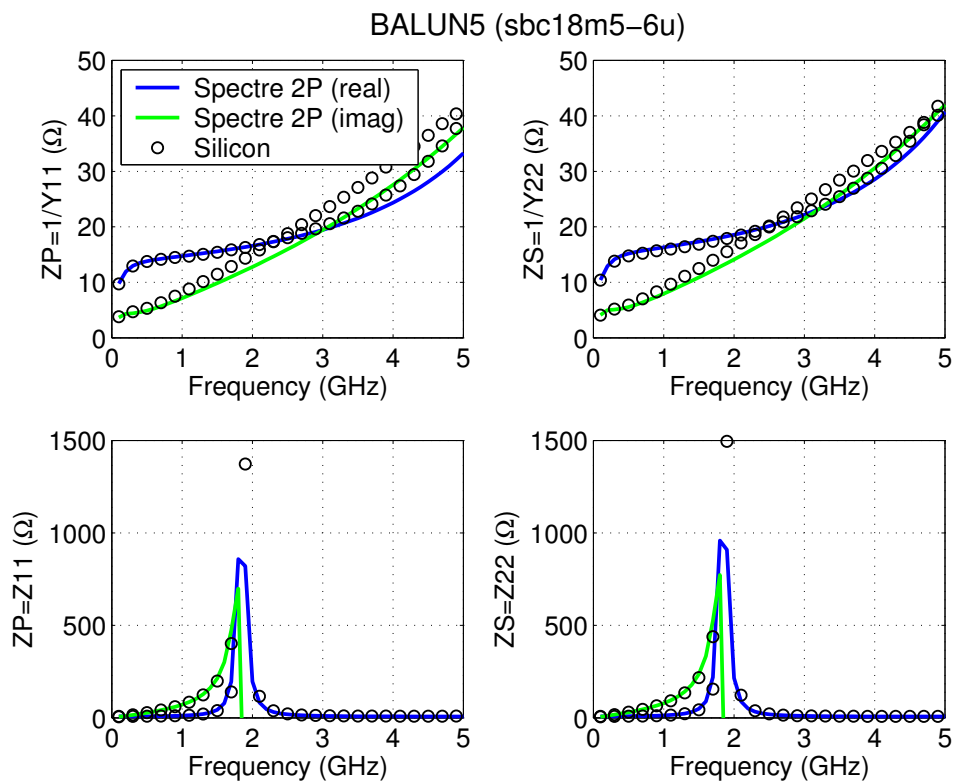


FIGURE 9.19 Model Verification - Insertion Loss, k, Q, L

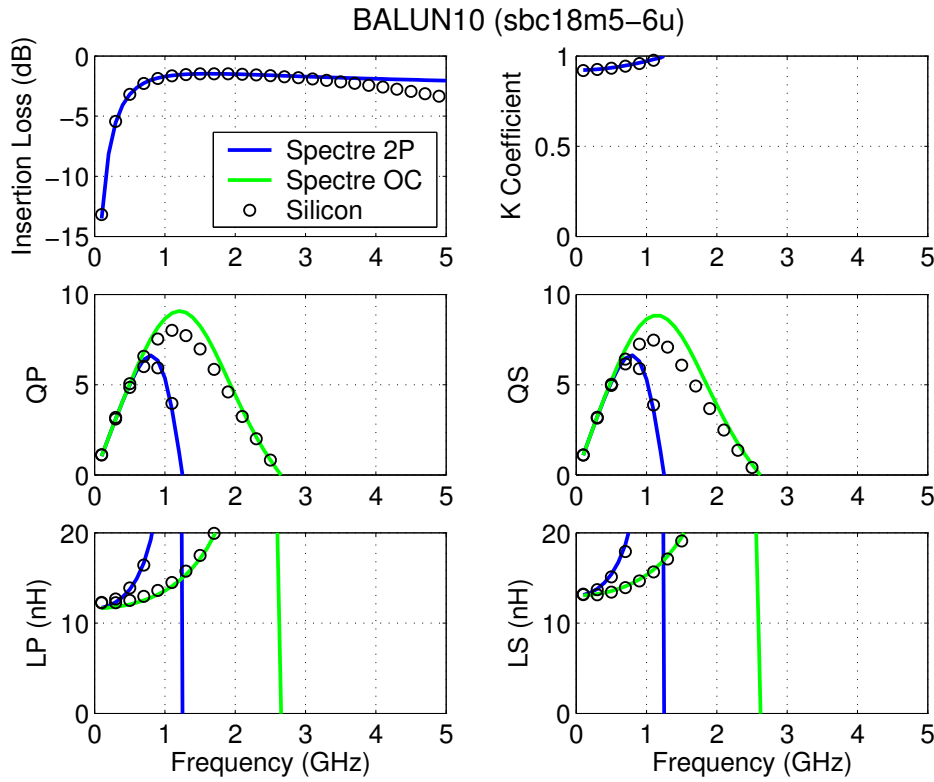


FIGURE 9.20 Model Verification - Impedance

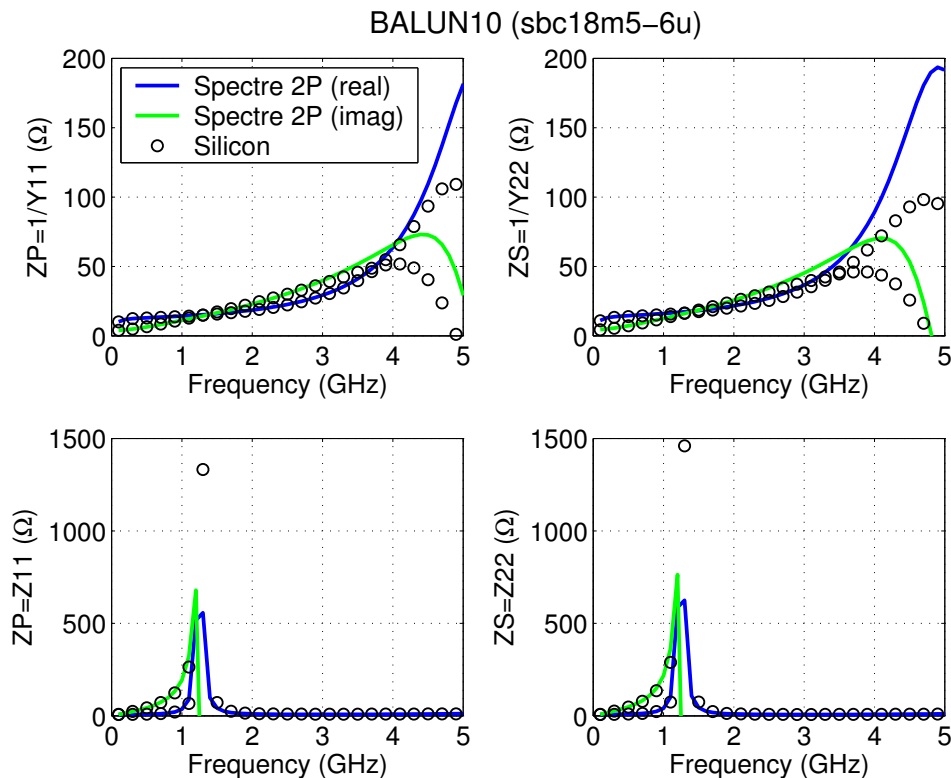


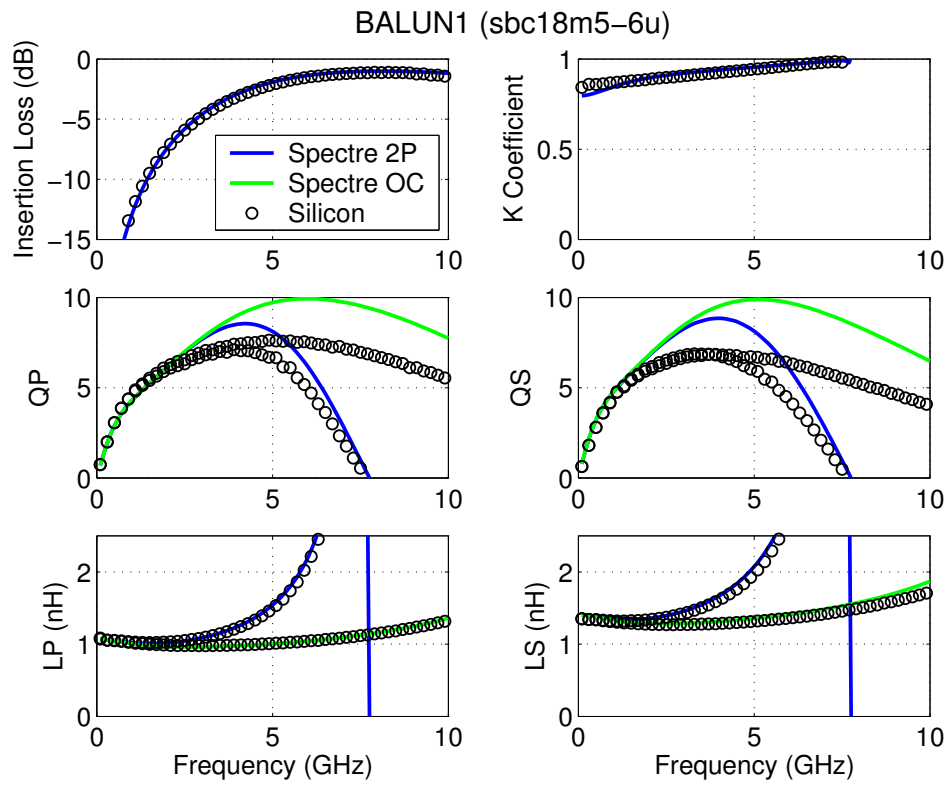
FIGURE 9.21 Model Verification - Insertion Loss, k , Q , L 

FIGURE 9.22 Model Verification - Impedance

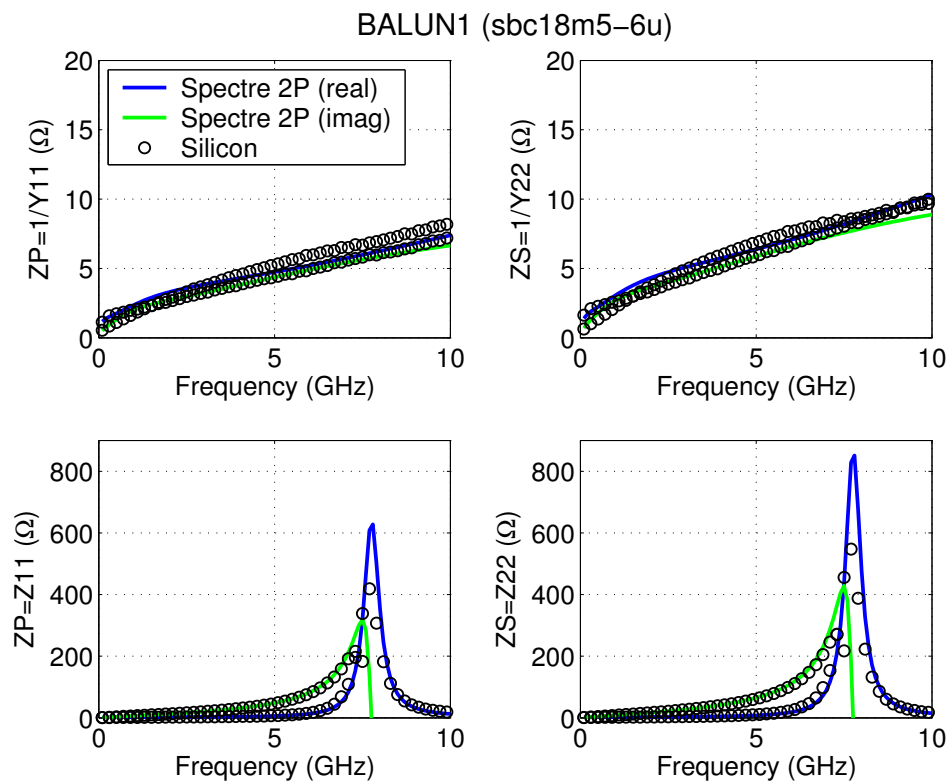


FIGURE 9.23 Model Verification - Insertion Loss, k, Q, L

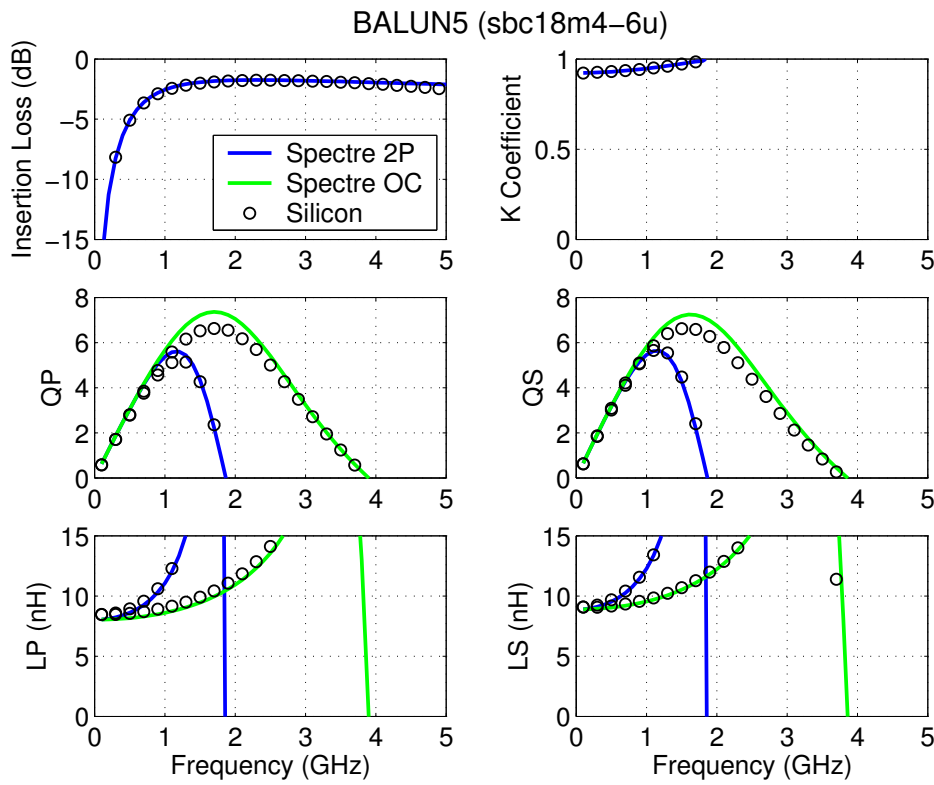


FIGURE 9.24 Model Verification - Impedance

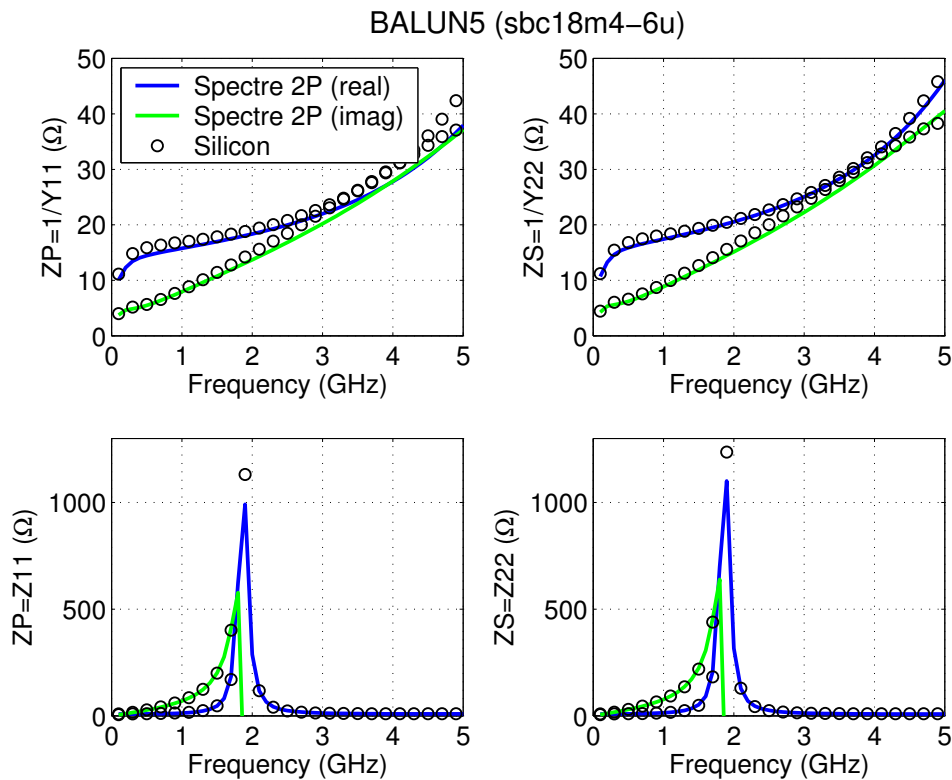


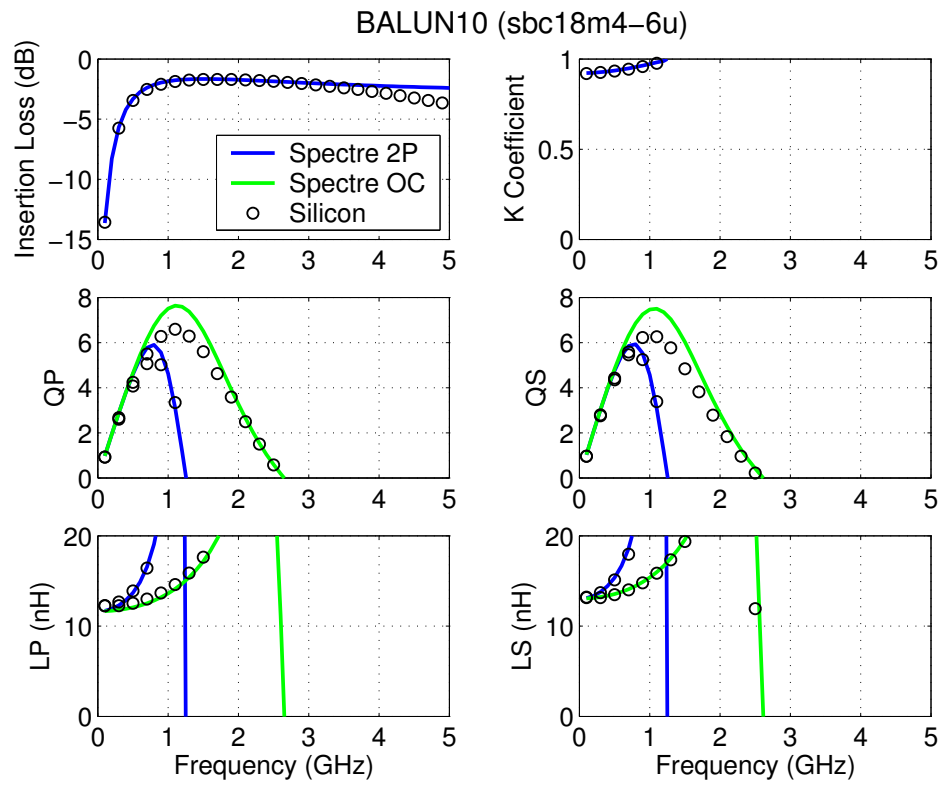
FIGURE 9.25 Model Verification - Insertion Loss, k , Q , L 

FIGURE 9.26 Model Verification - Impedance

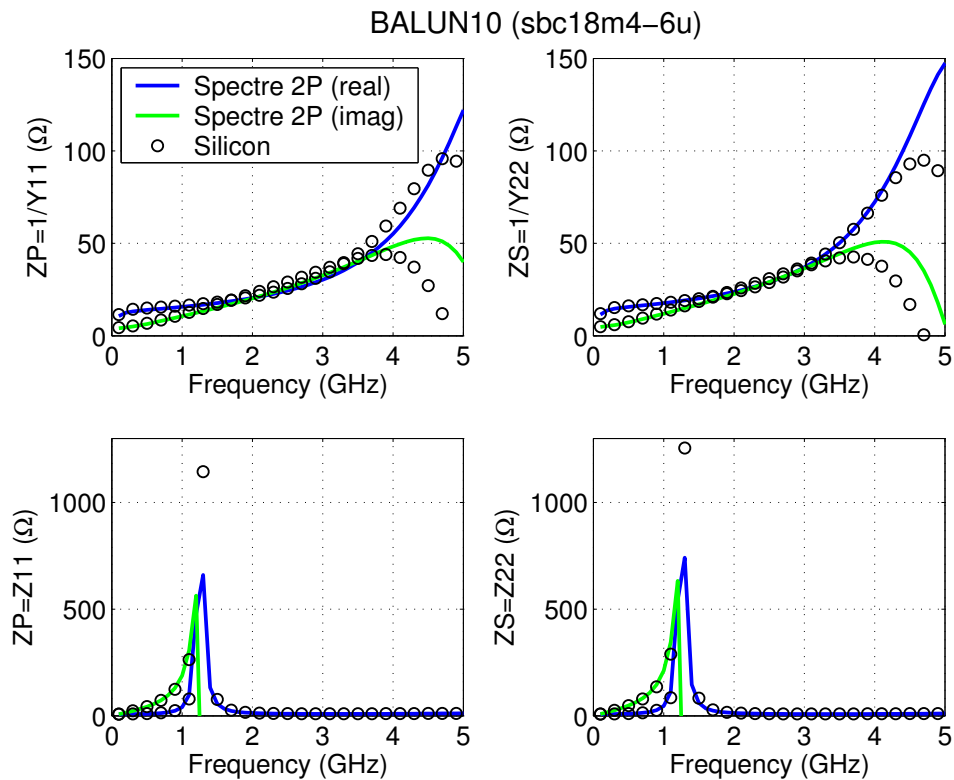


FIGURE 9.27 Model Verification - Insertion Loss, k, Q, L

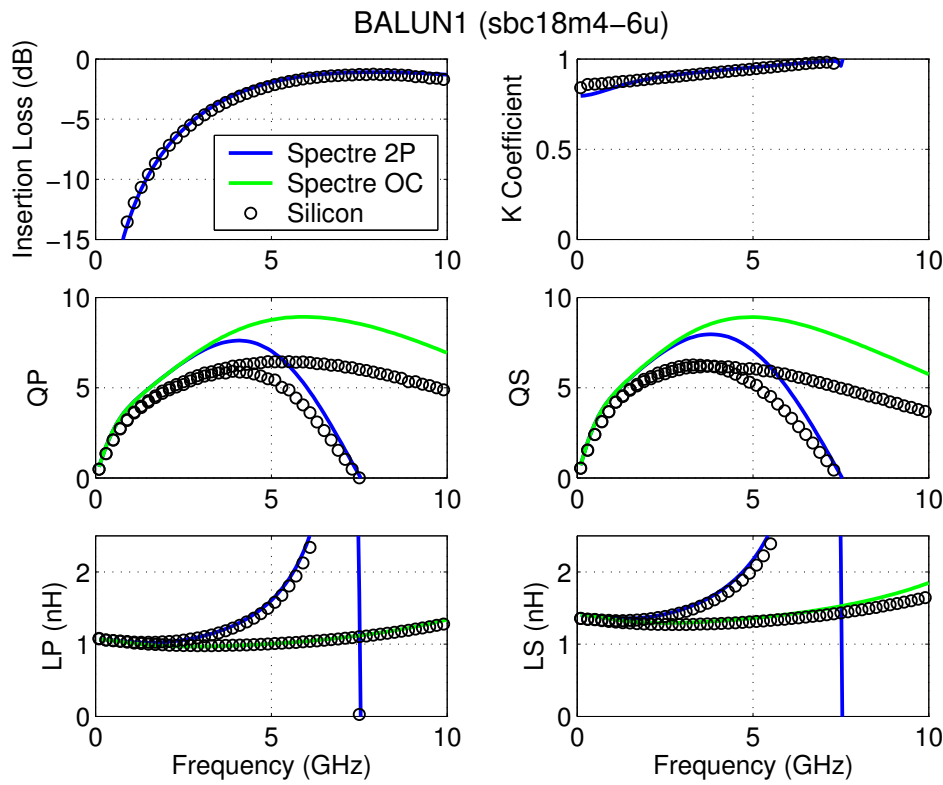
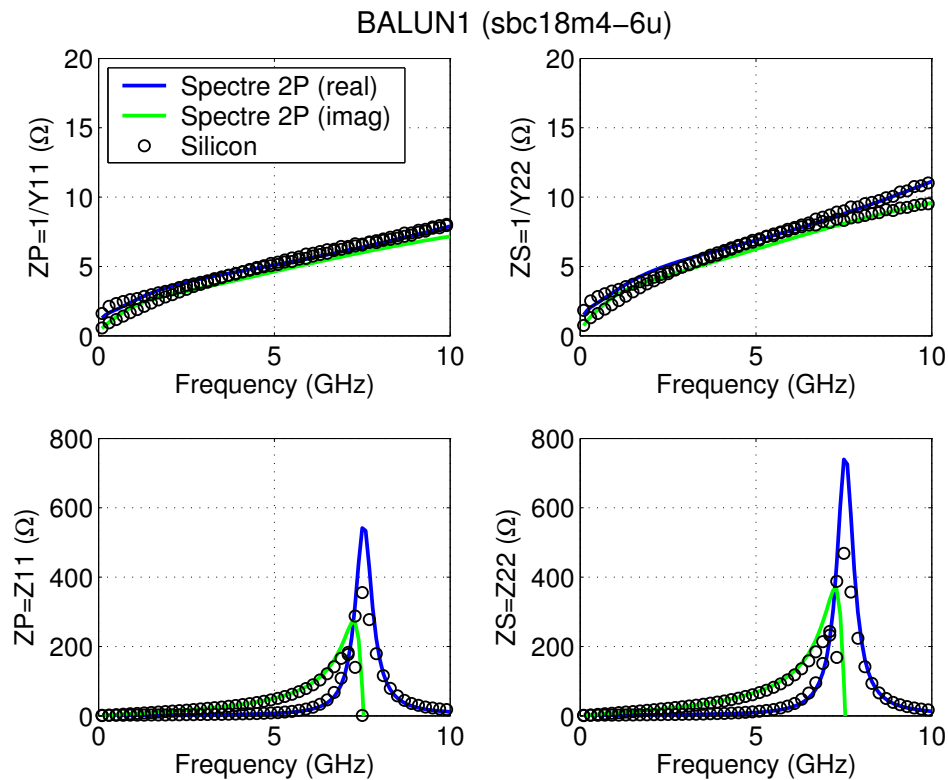


FIGURE 9.28 Model Verification - Impedance



9.3 Balun Statistical and Corner Models

See Section 8.4 on Inductor statistical and corner models.

9.4 Balun Model Update History

TABLE 9.5 Balun Model Updates in V6.0

V6.0 Update Detail	Devices	Reason	Impact on User
X-Sigma Corner Model Support	All	Allow for process variation settings different than conventional +/- 3 sigma-corner models	Added flexibility in corner simulation

9.5 References

1. John.R.Long, "Monolithic Transformers for Silicon RF IC Design", IEEE Journal of Solid-State Circuits, vol. 35, no.9, pp.1368-1382, Sep.2000

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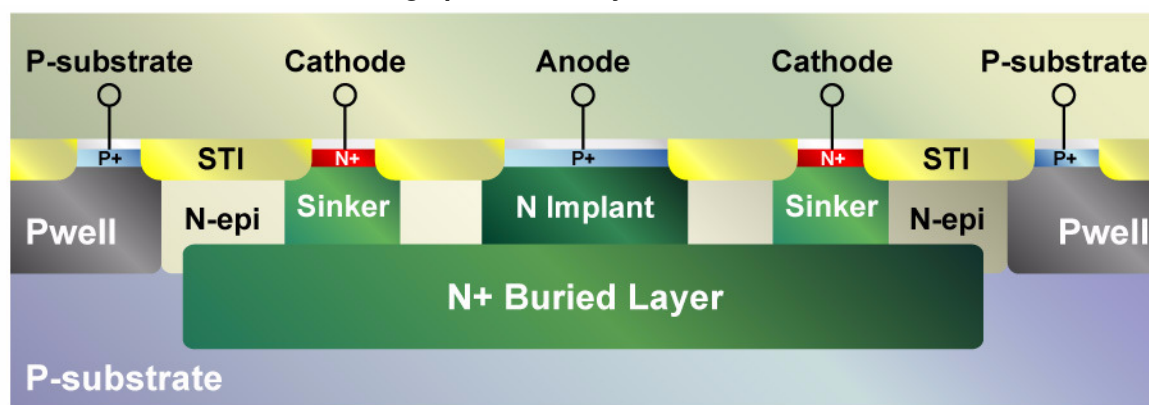
10.0 Varactor Model

10.1 High performance junction varactor

10.1.1 Device Structure and Layout

Figure 10.1 displays the cross section of the high performance junction varactor (device name: **varactor_bl**). The varactor (voltage controlled capacitance) is formed by the PN junction capacitance between anode (P+) and cathode (N-implant through buried and sinker layer). The top view of this varactor with key layout parameters is provided in Figure 10.2.

FIGURE 10.1 Cross section of high performance junction varactor



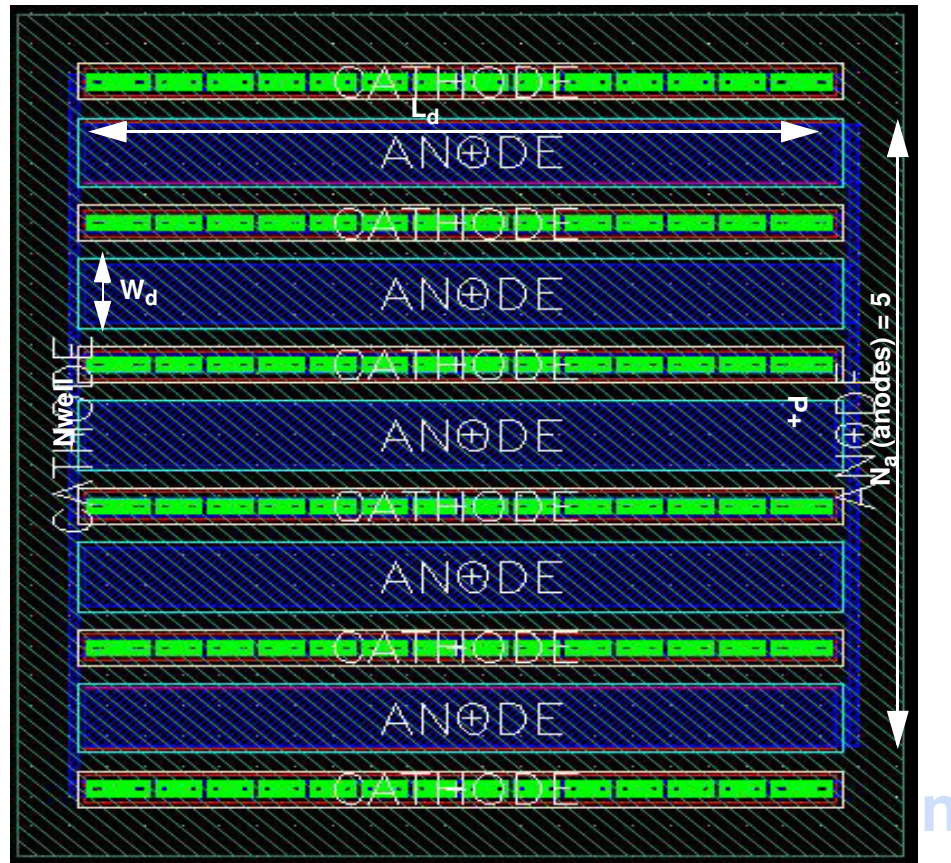
10.1.1.1 Layout Options

The high performance junction varactor pcell offers several design parameters to allow optimization of device performance. Table 10.1 provides detailed information on the pcell variables. The anode width (W_d) and length (L_d) control the capacitance (C) tuning range and quality factor (Q). Increased W_d and L_d provide higher tuning range as the contribution of fixed capacitance is reduced. However, the Q is reduced due to increased N-implant (W_d) and silicide/metal resistance (L_d). Section 10.1.5 provides further validation of C vs. Q trade-off. The C is further scaled through increasing the anodes (N_a).

TABLE 10.1 High Performance Junction Varactor parameter ranges

Design Kit Name	Parameter	Description	Typical	Min	Max
var_bl	W_d	anode width for each var_ni cell	1.4 ~ 2 μm	0.9 μm	5.5 μm
	L_d	anode length for each var_ni cell	20 ~ 30 μm	20 μm	50 μm
	N_a	number of var_ni anodes connected in parallel	scaled to give C	1	50

FIGURE 10.2 High Performance Junction Varactor Layout



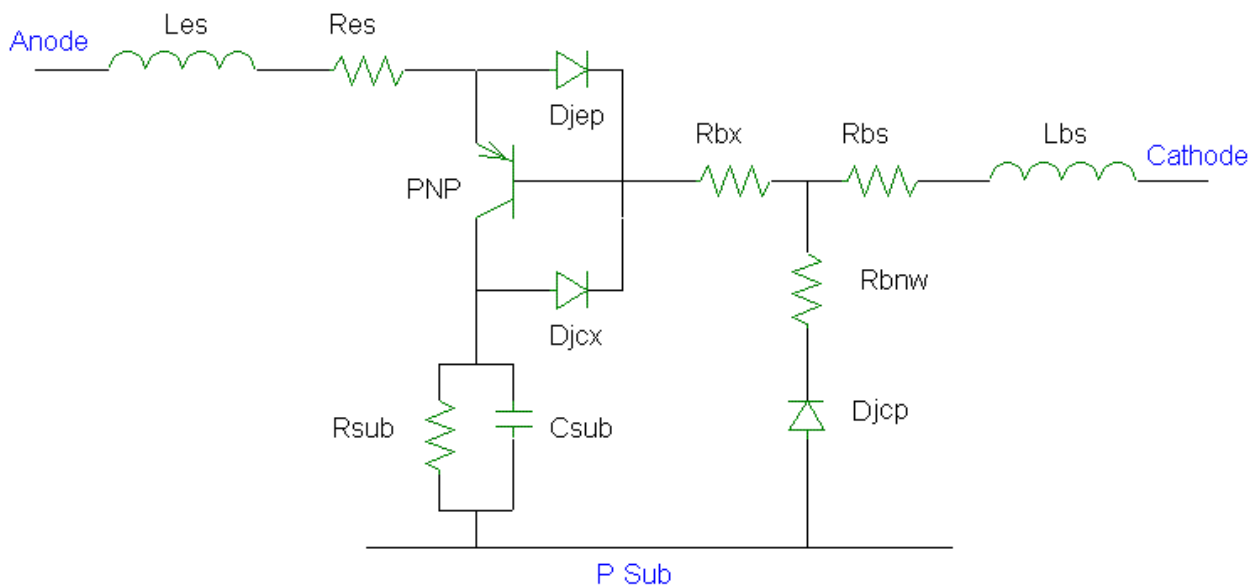
10.1.2 Sub circuit representation

The sub circuit used for the varactor_bl junction varactor scalable model is shown in Figure 10.3. The varactor capacitance formed by P+/N-implant junction capacitance is split into bottom-side (or area) capacitance (base-emitter of PNP) and perimeter-side capacitance (Djep). The dominant parasitic resistance is associated with the N-implant, N-buried layer, and sinker (Rbx). Descriptions of all the sub circuit components are given in Table 10.2.

TABLE 10.2 High Performance Junction Varactor Model Sub-Circuit Component Descriptions

Circuit Component Description	
PNP	BE junction forms area component of Varactor junction BC junction forms N-buried layer to PSUB junction under anode
Djep	Perimeter component of Varactor junction
Rbx	Resistance of N-implant, N-buried layer, and N-sinker.
Djcx	N-buried layer to PSUB junction not under anode (area component)
Djcp	N-buried layer to PSUB junction not under anode (perimeter component)
Rbnw	Parasitic resistance between cathode contact towards Djcp
Res, Lres	Parasitic resistance and inductance of anode metal
Rbs, Lbs	Parasitic resistance and inductance of cathode metal
Csub	Substrate capacitance
Rsub	Substrate resistance

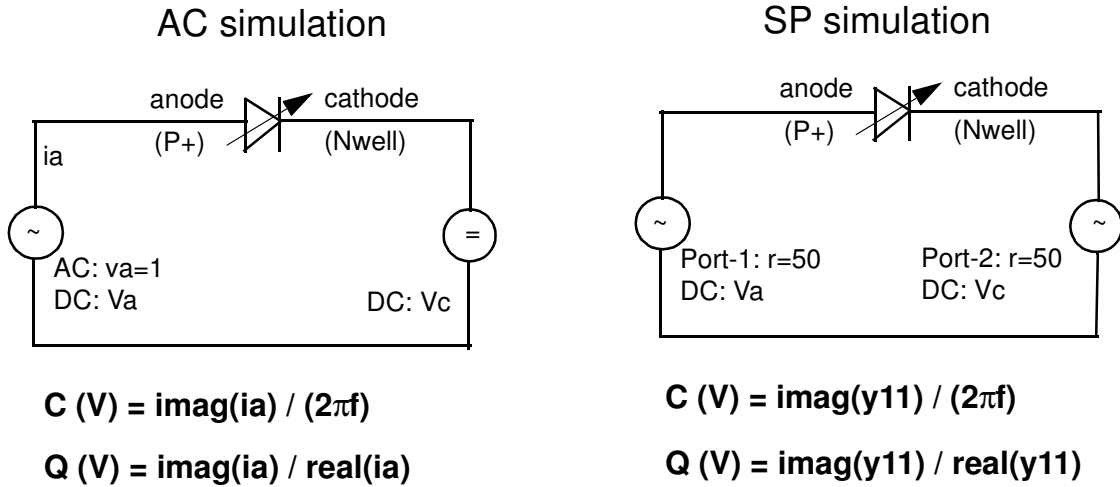
FIGURE 10.3 Sub circuit model for junction varactor



10.1.3 Effective Capacitance and Quality Factor (Q) simulation

There are two methods to simulate and verify junction varactor RF characteristics as shown in Figure 10.4. The key points for correctly simulating junction varactor RF characteristics are:

1. For ac simulation case, ac signal should always be applied at anode (P+) terminal, not at cathode (Nwell) terminal.
2. For s-parameter simulation case, only parameter y11 is used to calculate C and Q.
3. Make sure dc bias across Nwell-Psub diode is always reverse or zero bias.

FIGURE 10.4 Test diagrams for simulating junction varactor

DC bias condition: (1) V_a sweep (0 to 2.5V), $V_c \geq 2.5V$, $V_{sub} = 0V$; or

(2) V_c sweep (0 to 2.5V), $V_a = 0V$, $V_{sub} = 0V$

10.1.4 Parameter Extraction

The varactor_bl model parameters are physically extracted based on test devices with varying W_d (0.9 μm to 5 μm) at fixed $L_d=30\mu\text{m}$ and $N_a=20$. The bottom and perimeter portions of varactor capacitance can be extracted from the measured CV curves. The parasitic N-implant, N-buried layer, and sinker resistance parameters are extracted from the Quality Factor (Q). Parasitics associated with the metal are based on physical equations. Future characterization will include test devices with varying L_d .

10.1.5 Model Verification

Due to its different epi layer technology, SBC18H2 offers a slightly different buried layer varactor than all other SBC18 process family variants. Section 10.1.5.1 provides validation for the standard device while Section 10.1.5.2 documents the SBC18H2 device.

10.1.5.1 Model Verification for Standard Buried Layer Varactor

The SBC18 high performance junction varactor RF data uses OPEN-THRU de-embedding methodology (refer to OPEN-THRU de-embedding methodology in MOS varactor Section 10.3.6).

Figures 10.5 through 10.7 display model and data behavior at $T=25^\circ\text{C}$ across W_d , L_d , and N_a . Tables 10.3 through 10.5 list the performance summaries. As W_d increases (0.9 μm to 5.5 μm), the capacitance sensitivity (tuning) increases significantly due to higher area/perimeter ratio. The Q decreases as a result of increased parasitic resistance path from N-implant to cathode contact. As L_d increases, the sensitivity is constant while the Q begins to drop due to the parasitic metal resistance. The sensitivity and Q are constant for varying N_a .

Temperature coefficients are included in the model and have been verified on limited data. Future versions of the design manual will contain enhanced temperature verification.

TABLE 10.3 Performance Summary Table for Varying W_d

$L_d=20, N_a=10$	$W_d (\mu m)$			
	0.9	1.4	2	3.5
Sensitivity/Tuning $[C(-0.5V) - C(-2.5V)] / [C(-0.5V) + C(-2.5V)] * 100$	26	28	29	30
Q (@ 2GHz, -0.5V)	98	80	70	60

TABLE 10.4 Performance Summary Table for Varying L_d

$W_d=2, N_a=10$	$L_d (\mu m)$		
	10	20	40
Sensitivity/Tuning $[C(-0.5V) - C(-2.5V)] / [C(-0.5V) + C(-2.5V)] * 100$	29	29	29
Q (@ 2GHz, -0.5V)	75	70	60

TABLE 10.5 Performance Summary Table for Varying N_a

$W_d=2, L_d=20$	$N_a (\mu m)$			
	5	10	15	20
Sensitivity/Tuning $[C(-0.5V) - C(-2.5V)] / [C(-0.5V) + C(-2.5V)] * 100$	29	29	29	29
Q (@ 2GHz, -0.5V)	70	70	70	70

FIGURE 10.5 Verification plot for varactor_bl - (varying Wd)

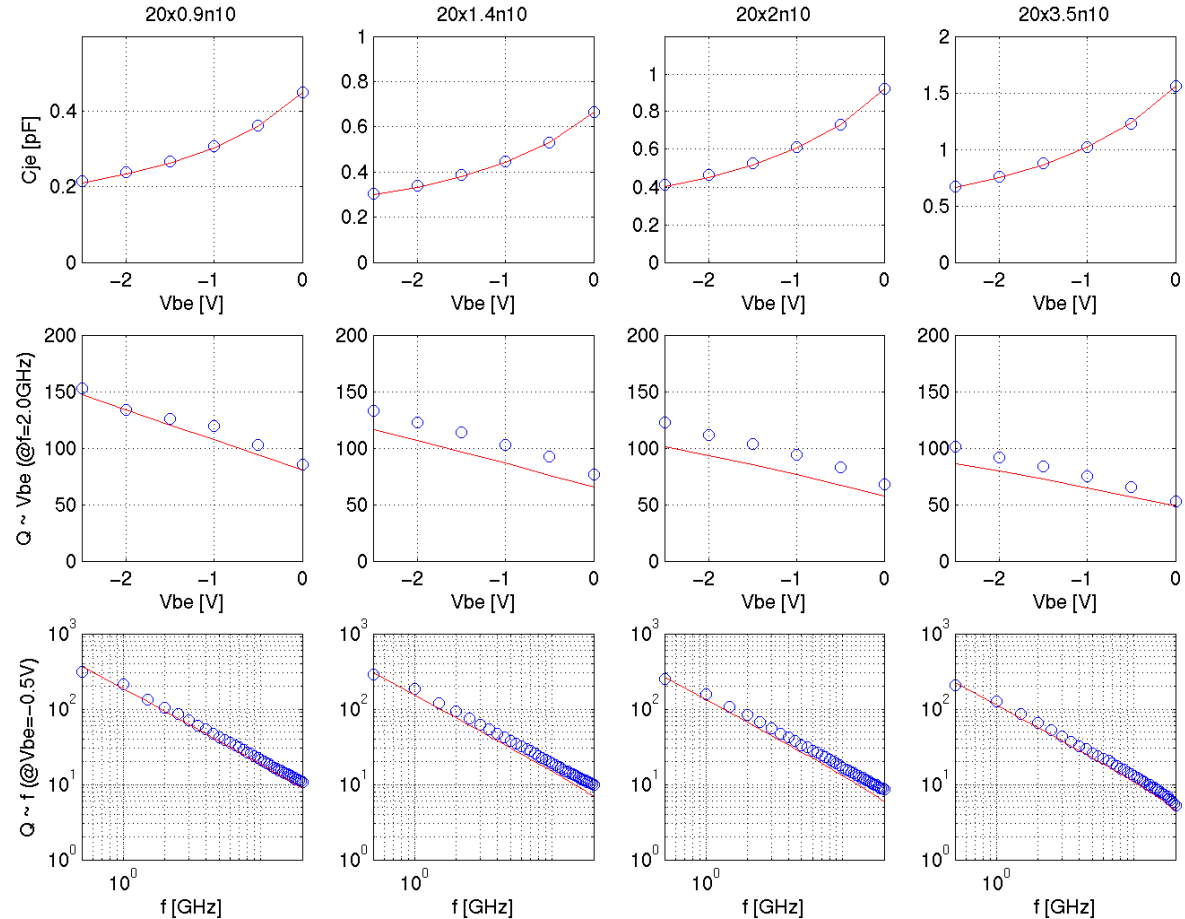
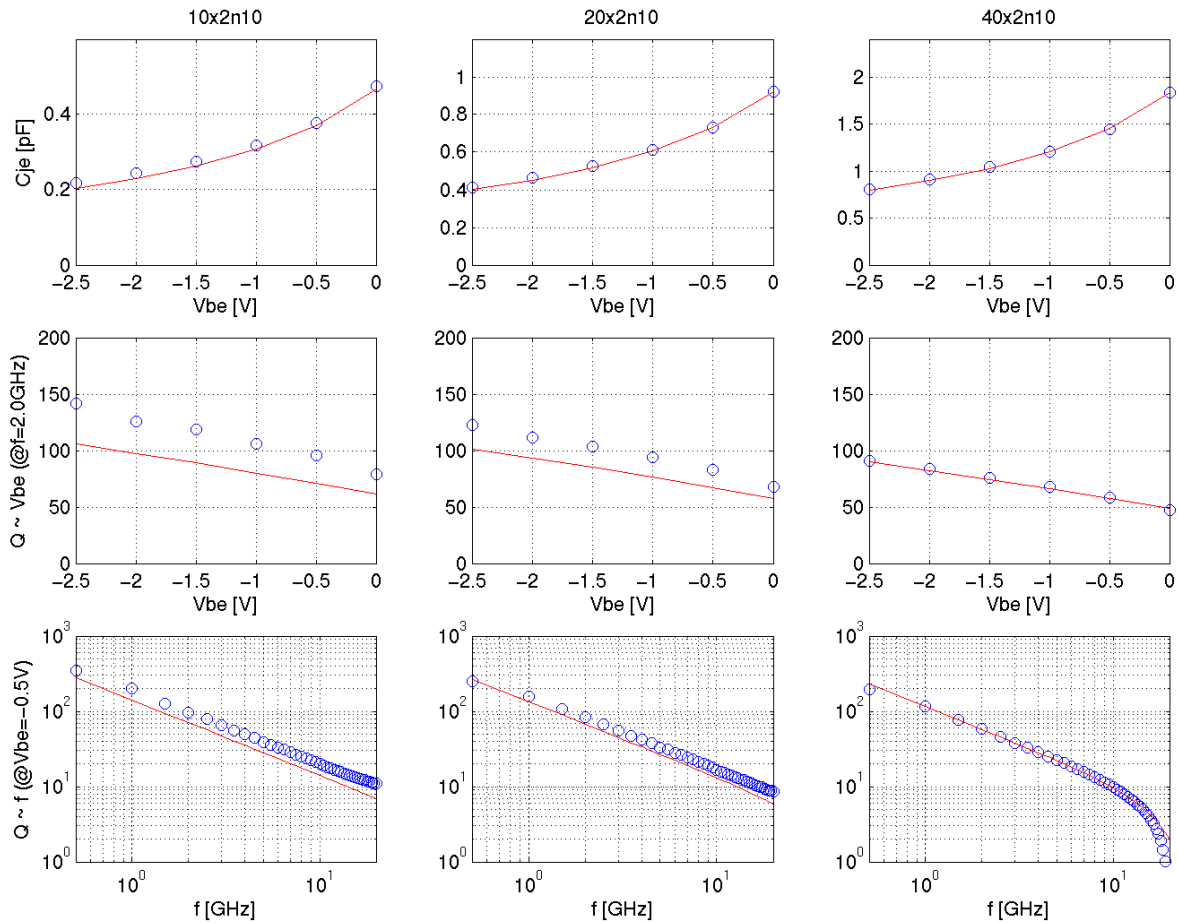
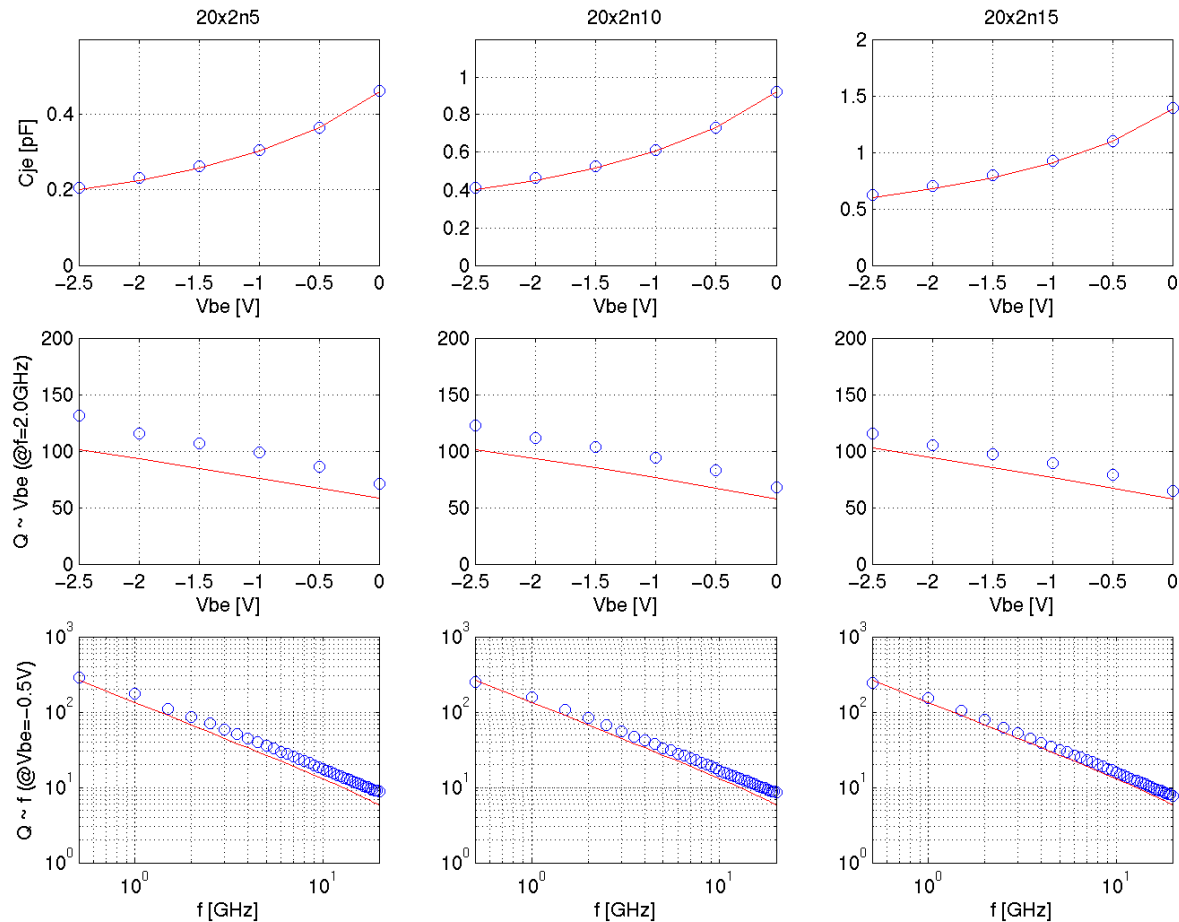


FIGURE 10.6 Verification plot for varactor_b1 - (varying L_d)



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FIGURE 10.7 Verification plot for varactor_bl - (varying Na)

10.1.5.2 Model Verification for SBC18H2/H3 Buried Layer Varactor

The SBC18H2/H3 buried layer varactor differs from the SBC18 flavor, due to differences in the epi-layer. The model validation plots will be added in a future update.

10.1.6 Corner and Statistical models

For the varactor_bl junction varactor, due to the special N-implant under anode region in order to form high performance varactor characteristics (higher sensitivity and higher Q), most of the process-related corner variation in corner and statistical models are independent from other devices. See Section 15.0 for further explanation of the device interdependencies in the corner models and use of the X-Sigma corner models.

Figure 10.8 displays the corner simulation for varactor_bl varactor at the 3-sigma limits. Table 10.6 lists the Espec values compared to simulated corner and statistical values for varactor_bl junction varactor.

TABLE 10.6 Espec, Corner and Statistical model comparison for high performance junction varactor

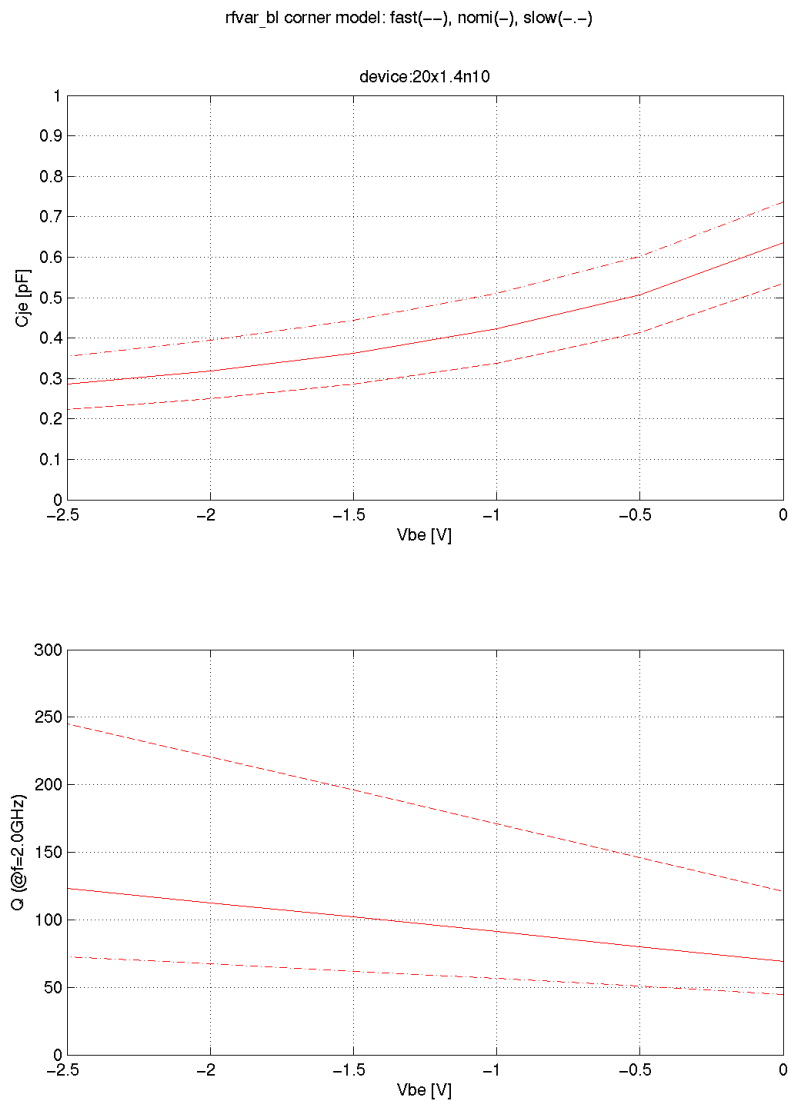
Parameters		Slow			Nom			Fast		
		Espec	Corner	Stat	Espec	Corner	Stat	Espec	Corner	Stat
1.4x30n20 WdxLdxNa	unit									
Capacitance (0V)	pF	2.20	2.20	2.18	1.90	1.90	1.90	1.60	1.60	1.62
sensitivity ¹	%/V	26.0	26.0	26.4	28.0	28.0	28.2	30.0	30.0	30.0
Q(1.9G,-0.5V)		50	50	50	80	80	80			
I (leakage current at -2.5V)	nA							1	1	1

ESPEC notes:

1. Capacitance sensitivity definition: $[C(-0.5V) - C(-2.5V)] / [C(-0.5V) + C(-2.5V)] * 100$
2. Due to the asymmetrical statistical variation of Q, the slow Q value from statistical Monte Carlo simulation shows lower 3- σ variation based on symmetric gaussian interpreting to extract sigma.

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FIGURE 10.8 Varactor_bl - Corner Model



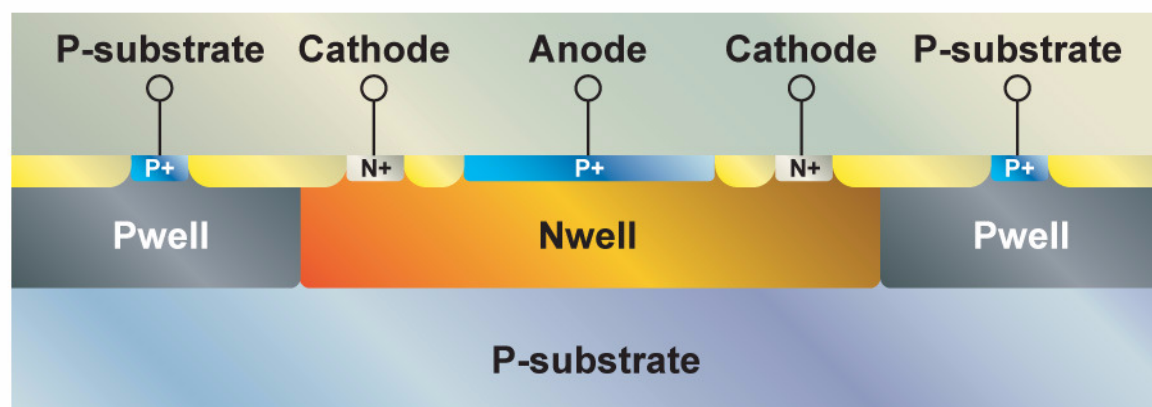
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10.2 P+/Nwell Junction Varactor

10.2.1 Device Description

Figure 10.9 displays the cross section of the P+/Nwell junction varactor (device name: **varactor_ni**). The varactor (voltage controlled capacitance) is formed by the PN junction capacitance between anode (P+) and cathode (Nwell). There is no additional mask required for this varactor. The device is supported in the SBC18MW and SBC18QW only.

FIGURE 10.9 Cross section of the P+/Nwell junction varactor



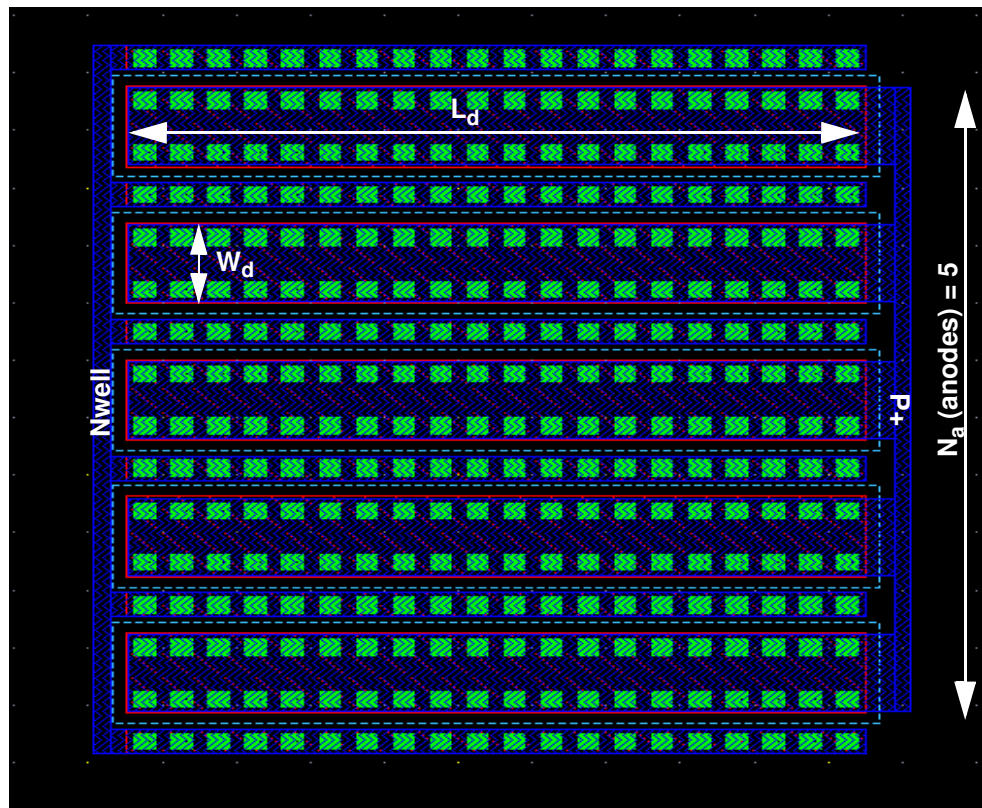
10.2.1.1 Layout Options

The junction varactor pcell offers several design parameters to allow optimization of device performance. Table 10.1 provides detailed information on the pcell variables. The anode width (W_d) and length (L_d) control the capacitance (C) tuning range and quality factor (Q). Increased W_d and L_d provide higher tuning range as the contribution of fixed capacitance is reduced. However, the Q is reduced due to increased Nwell (W_d) and silicide/metal resistance (L_d). Section 10.2.5 provides further validation of C vs. Q trade-off. The C is further scaled through increasing the anodes (N_a).

TABLE 10.7 P+ / Nwell Junction Varactor parameter ranges

Parameter	Description	Typical	Min	Max
W_d	anode width for each var_ni cell	1.4 ~ 2 μm	0.9 μm	5.5 μm
L_d	anode length for each var_ni cell	20 ~ 30 μm	10 μm	50 μm
N_a	number of var_ni anodes connected in parallel	scaled to give C	1	30

FIGURE 10.10 Junction Varactor Layout



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10.2.2 Model Description

The sub circuit used for varactor_ni junction varactor scalable model is the same as varactor_bl model as shown in Figure 10.3. Unique model parameters are extracted for the varactor_ni device, different from those in the varactor_bl device. The varactor capacitance formed by P+/Nwell junction capacitance is split into bottom-side (or area) capacitance (base-emitter of PNP) and perimeter-side capacitance (Djep). The dominant parasitic resistance is associated with the Nwell towards the cathode contact (Rbx). Descriptions of all the sub circuit components are given in Table 10.8.

TABLE 10.8 P+/Nwell Junction Varactor Model Sub-Circuit Component Descriptions

Circuit Component Description	
PNP	BE junction forms area component of Varactor junction BC junction forms Nwell to PSUB junction under anode
Djep	Perimeter component of Varactor junction
Rbx	Resistance of Nwell
Djcx	Nwell to PSUB junction not under anode (area component)
Djcp	Nwell to PSUB junction not under anode (perimeter component)
Rbnw	Parasitic resistance between cathode contact towards Djcp
Res, Lres	Parasitic resistance and inductance of anode metal
Rbs, Lbs	Parasitic resistance and inductance of cathode metal
Csub	Substrate capacitance
Rsub	Substrate resistance

10.2.3 Test diagram

The test diagram for varactor_ni device is exactly the same as varactor_bl device as shown in Figure 10.4.

10.2.4 Parameter Extraction

The principle for junction varactor model parameters extraction is covered in Section 10.1.4 on page 456.

10.2.5 Model Verification Plots

The SBC18 junction varactor RF data is characterized with OPEN-THRU de-embedding methodology (refer to OPEN-THRU de-embedding methodology in MOS varactor Section 10.3.6).

Figures 10.11 through 10.13 display model and data behavior at $T=25^{\circ}\text{C}$ across W_d , L_d , and N_a . Tables 10.9 through 10.11 list the performance summaries. As W_d increases the capacitance sensitivity (tuning) increases significantly due to higher area/perimeter ratio. The Q decreases as a result of increased parasitic resistance path to the cathode contact. As L_d increases, the sensitivity is constant while the Q begins to drop due to the parasitic metal resistance. The sensitivity and Q are constant for varying N_a . Temperature coefficients are included in the model and have been verified on limited data. Future versions of the design manual will contain enhanced temperature verification.

TABLE 10.9 Performance Summary Table for Varying W_d

$L_d=20, N_a=10$	$W_d (\mu\text{m})$			
	0.9	1.4	2	3.5
Sensitivity/Tuning $[C(-0.5\text{V}) - C(-2.5\text{V})] / [C(-0.5\text{V}) + C(-2.5\text{V})] * 100$	8.9	10.5	11.8	13.5
Q (@ 2GHz, -0.5V)	106	83	65	41

TABLE 10.10 Performance Summary Table for Varying L_d

$W_d=2, N_a=10$	$L_d (\mu m)$		
	10	20	40
Sensitivity/Tuning $[C(-0.5V) - C(-2.5V)] / [C(-0.5V) + C(-2.5V)] * 100$	11.6	11.8	11.9
Q (@ 2GHz, -0.5V)	65	65	61

TABLE 10.11 Performance Summary Table for Varying N_a

$W_d=2, L_d=20$	$N_a (\mu m)$			
	5	10	15	20
Sensitivity/Tuning $[C(-0.5V) - C(-2.5V)] / [C(-0.5V) + C(-2.5V)] * 100$	11.8	11.8	11.8	11.8
Q (@ 2GHz, -0.5V)	65	65	65	65

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FIGURE 10.11 Verification plot for varactor_ni - (varying Wd)

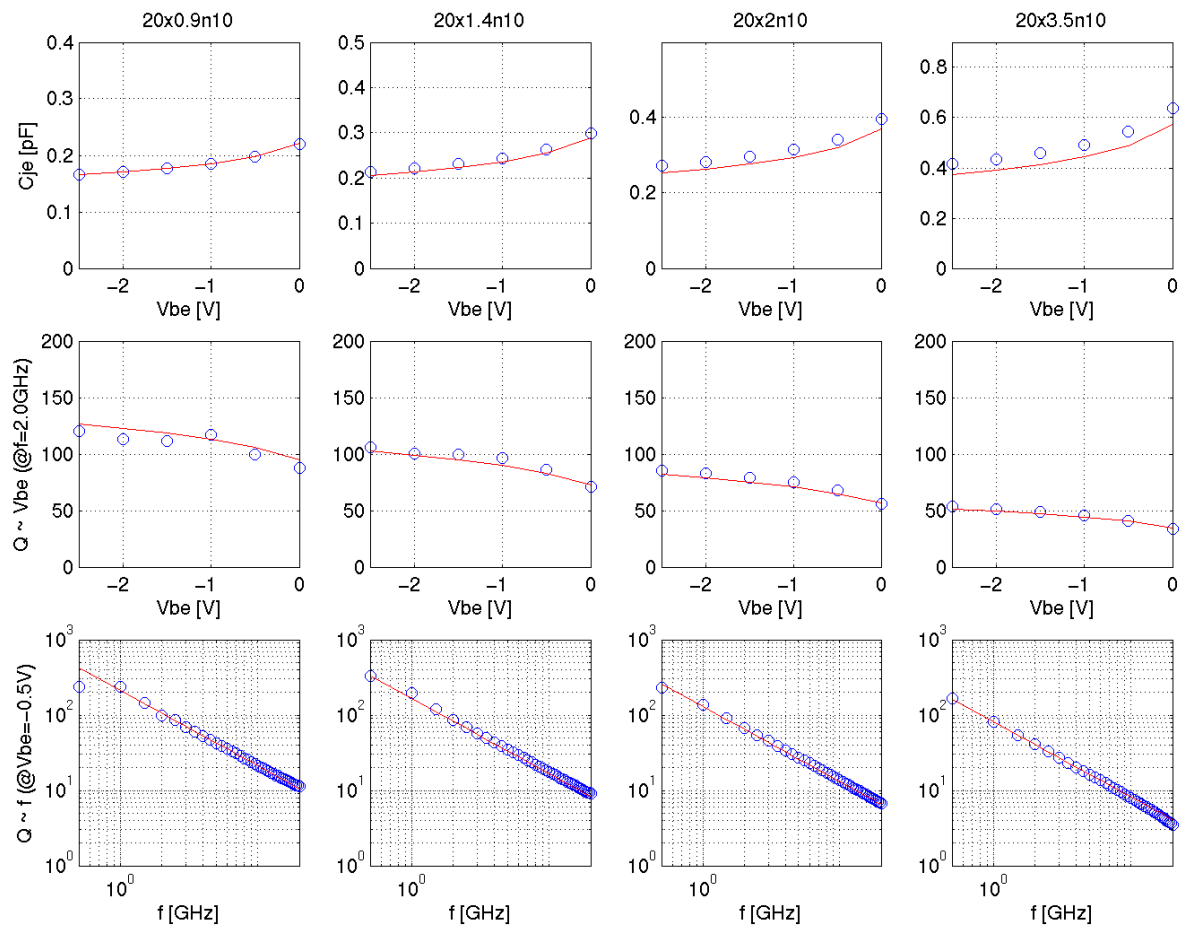


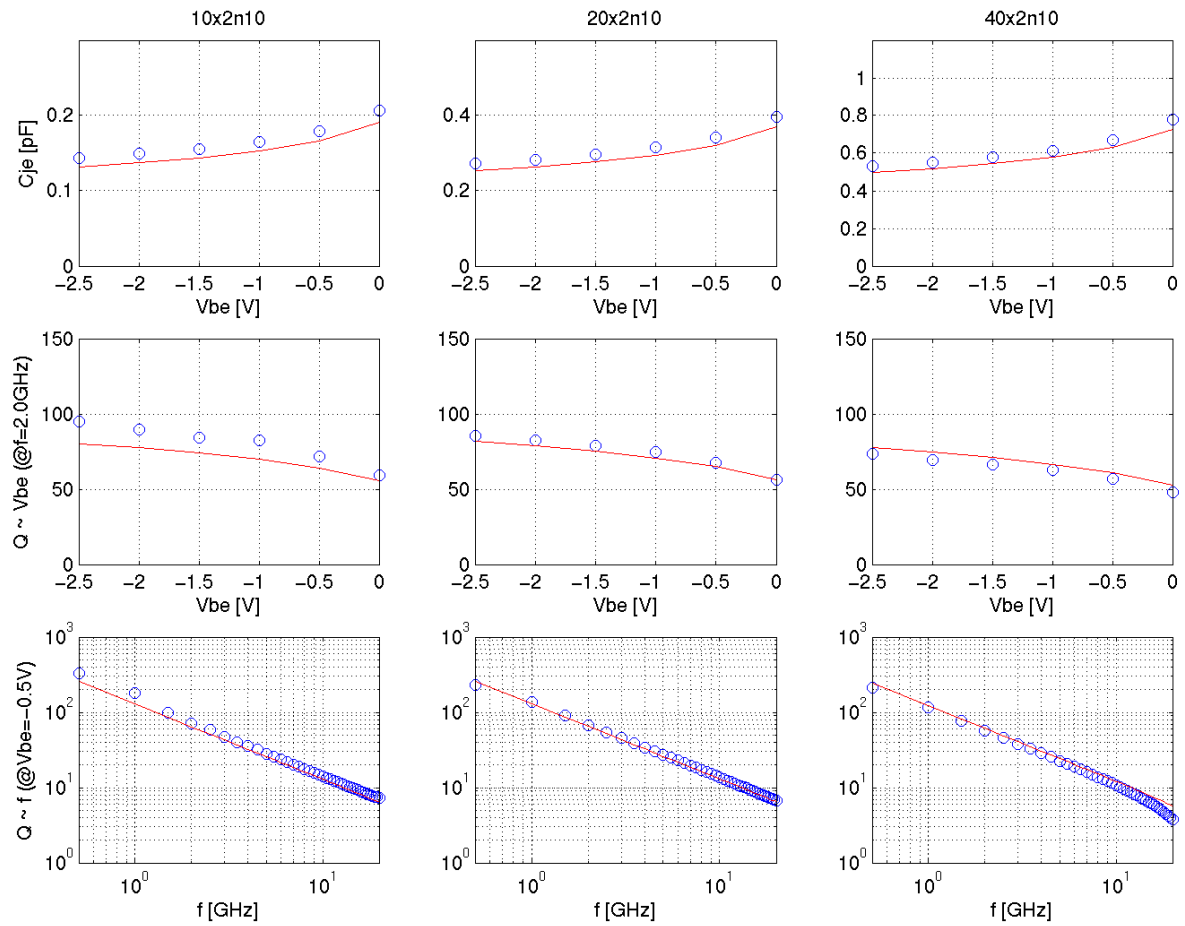
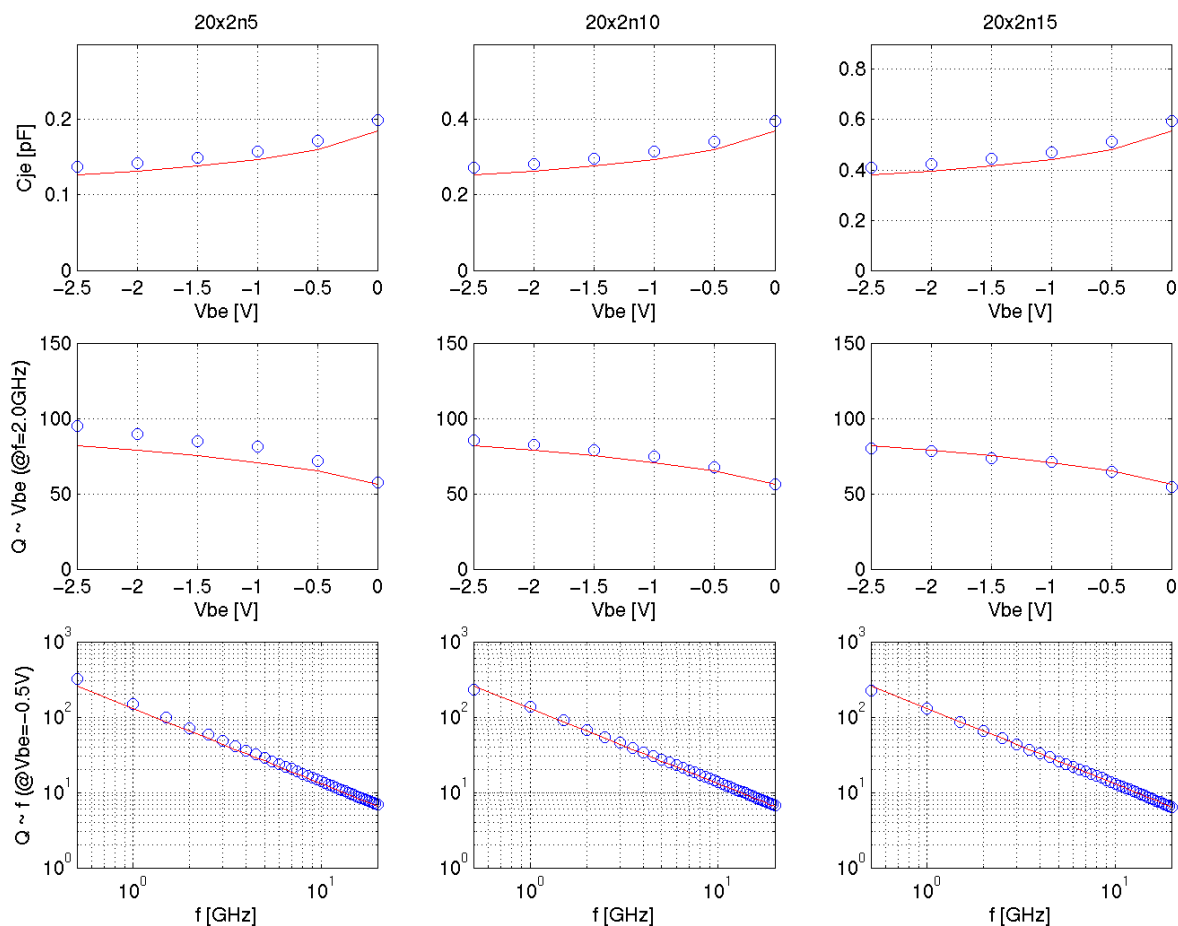
FIGURE 10.12 Verification plot for varactor_ni - (varying L_d)

FIGURE 10.13 Verification plot for varactor_ni - (varying Na)



10.2.6 Statistical and Corner models

For varactor_ni junction varactor, the junction capacitance formed between P+ and Nwell is heavily dependent on the Nwell doping. Thus, the process-related variation in corner and statistical models are correlated with other devices such as the Nwell resistors. See Section 15.0 for further explanation of the device interdependencies in the corner models and use of the X-Sigma corner models. Figure 10.14 displays the corner simulation for varactor_ni varactor at the 3-sigma limits. Table 10.12 lists the ESPEC values compared to simulated corner and statistical values for the varactor_ni junction varactor.

TABLE 10.12 Espec, Corner and Statistical model comparison for P+/Nwell junction varactor

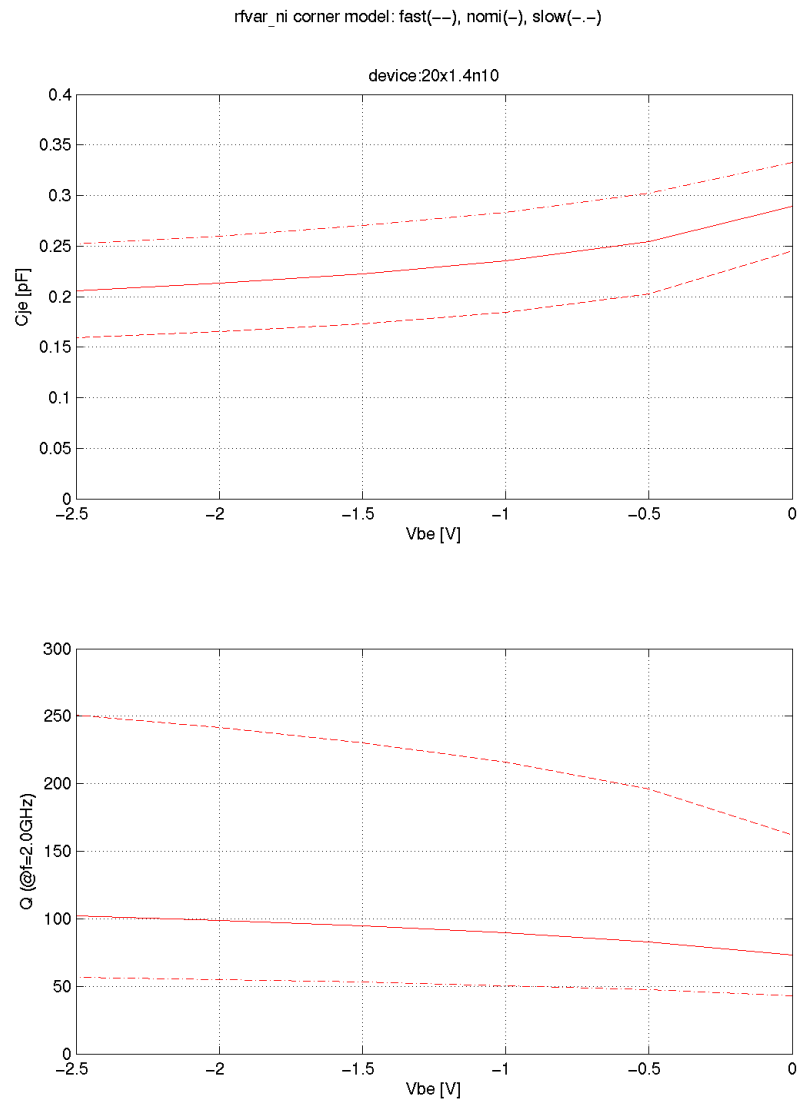
Parameters		Slow			Nom			Fast		
1.4x30n20 WdxLdxNa	unit	Espec	Corner	Stat	Espec	Corner	Stat	Espec	Corner	Stat
Capacitance (0V)	pF	0.99	0.99	0.974	0.86	0.86	0.856	0.73	0.73	0.738
sensitivity ¹	%/V	9.2	9.2	9.3	10.6	10.59	10.7	12.0	11.98	11.98
Q(1.9G _s -0.5V)		50	49	50						
I (leakage current at -2.5V)	pA							500	500	500

ESPEC notes:

1. Capacitance sensitivity definition: $[C(-0.5V) - C(-2.5V)] / [C(-0.5V) + C(-2.5V)] * 100$
2. Due to its asymmetrical statistical variation of Q, the slow Q value from statistical Monte Carlo simulation shows lower 3- σ variation based on symmetric gaussian interpreting to extract sigma.

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FIGURE 10.14 Varactor_ni - Corner Model



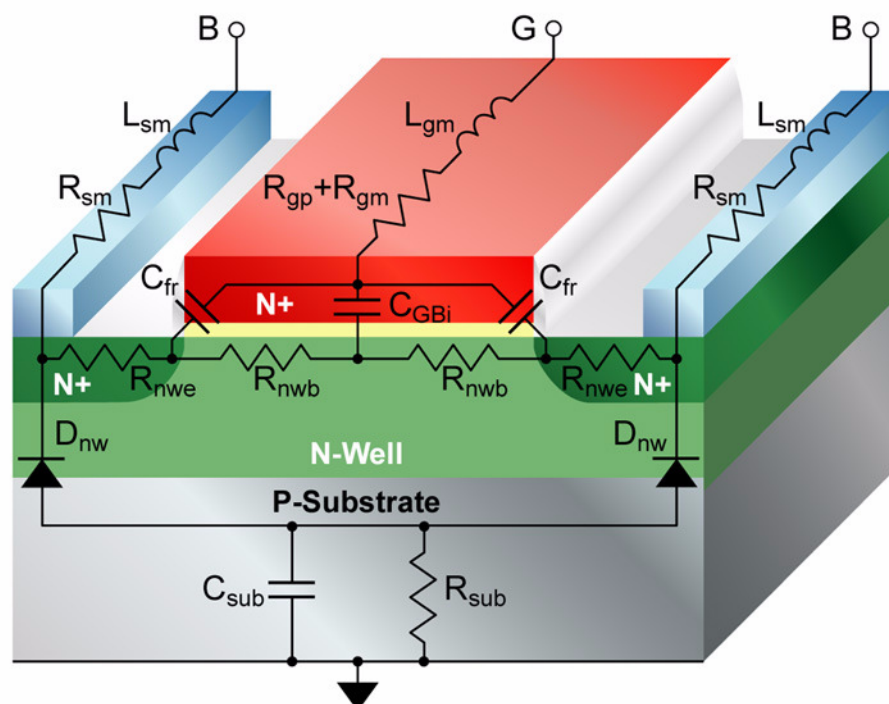
nan

10.3 MOS Varactor

10.3.1 Device Description

The MOS varactor (device name: **varactor_mos**) is formed by thin gate-oxide over Nwell, with N+ implant at both source / drain regions to form ohmic contacts with varactor Nwell region. The cross section of this device is shown in Figure 10.15. The device is the same in cross section to the 1.8V poly capacitors. The device is only supported in SBC18 technologies with 1.8V TOX (SBC18HX, SBC18HXL, SBC18PT, SBC18QB, and SBC18HK).

FIGURE 10.15 MOS Varactor Cross Section: n+ poly to Nwell capacitor as MOS Varactor



10.3.2 Layout Options

The MOS varactor pcell offers several design parameters to allow optimization of device performance. Table 10.13 provides detailed information on the pcell variables. The gate width (W_g) and length (L_g) control the capacitance (C) tuning range and quality factor (Q). Increased W_g and L_g provide higher tuning range as the contribution of fixed capacitance is reduced. However, the Q is reduced due to increased Nwell and poly gate resistance. Section 10.3.6 provides further validation of C vs. Q trade-off.

The C is scaled through arraying the device as *slices* (N_s) and *fingers* (N_f). There is no break in the poly or metal 1 between successive slices. There is a break in the active to allow for metal 1 contact to the poly gate in order to minimize the gate resistance. Two different *metal style* options (metal 1 and metal 2) are offered for the

MOS varactor in the SBC18 design kit. The metal one option is shown in Figure 10.16. Metal 1 fingers are drawn parallel to the gate poly and Nwell contacts. The metal 2 option exists as *unconnected* and *connected*. The metal 2 *connected* option is shown in Figure 10.17. In the *unconnected* option, the vertical metal bars are removed. In the metal 2 option, the metal 2 fingers are drawn orthogonal to the metal 1 fingers with vias dropped to connect to the gate and Nwell metal 1 fingers. The metal 2 option provides for lower metal resistance for larger N_s layouts ($N_s > 5$) at the expense of increased parasitic metal 1 to metal 2 capacitance which degrades the tuning range.

TABLE 10.13 MOS Varactor Parameter Description

Design Kit Name	Variable	Description	Typical	Min	Max
var_mos	L_g	gate length for each var_mos cell	0.5 μm	0.18 μm	2 μm
	W_g	gate width for each var_mos cell	3.0 μm	2 μm	4.0 μm
	N_s (slices)	number of slices which controls the number of var_mos cells in series	4	1	10
	N_f (fingers)	number of fingers connected in parallel for each slices	scaled to give C	1	40
	Metal Style	metal connection type	metal 1, metal 2, metal 2 connected		

FIGURE 10.16 MOS varactor - Metal 1 Layout Option

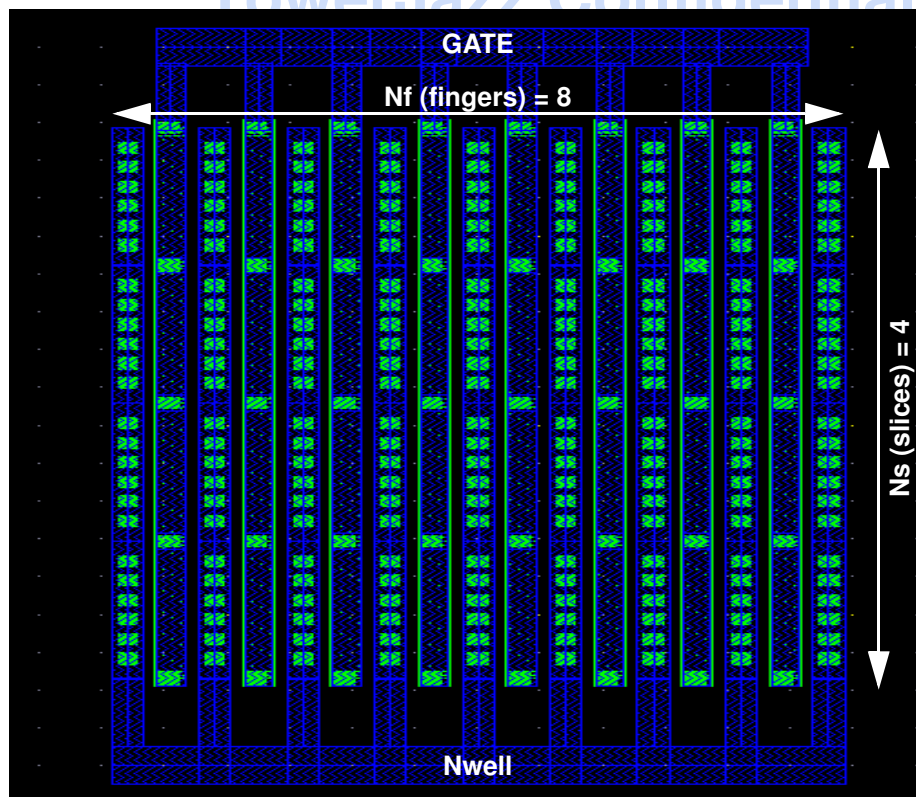
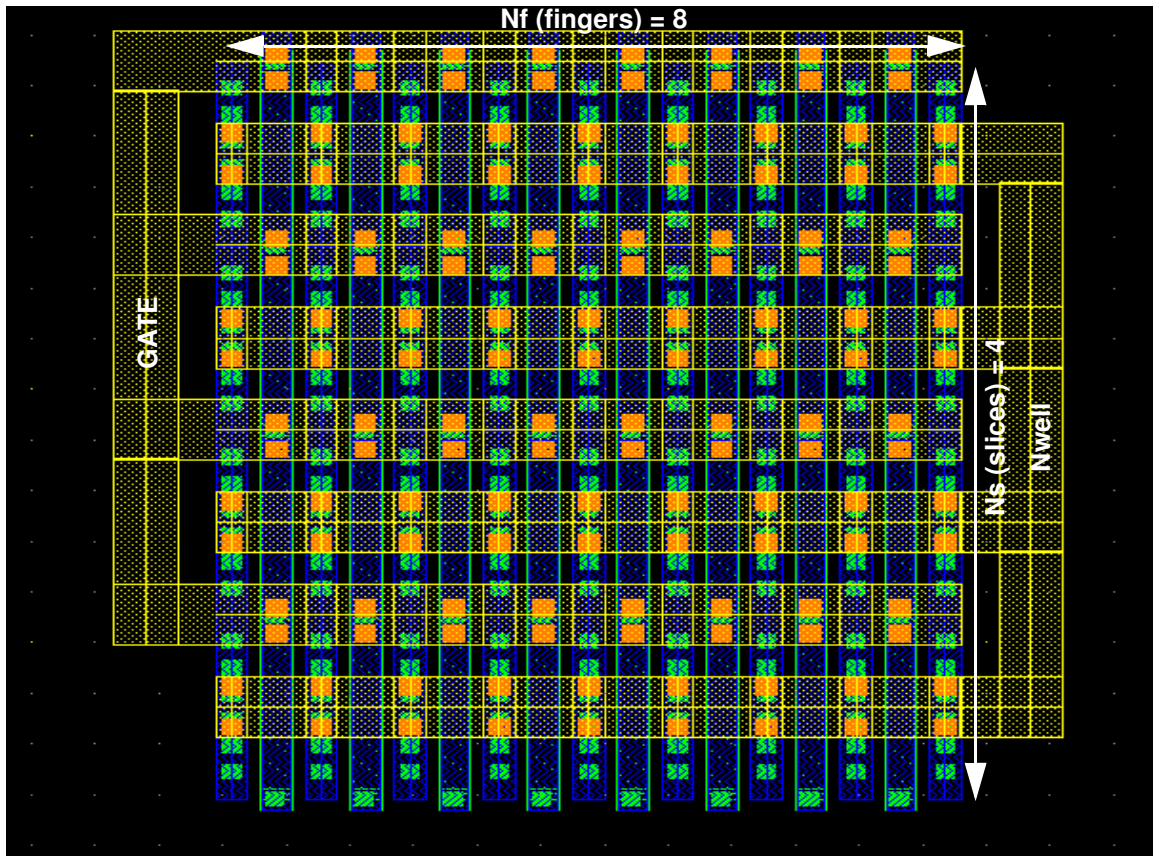


FIGURE 10.17 MOS varactor - Metal 2 Connected Layout Option



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10.3.3 Model Description

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The sub circuit used for mos varactor scalable model is shown embedded in Figure 10.15. Table 10.14 provides the descriptions of all sub circuit components. The intrinsic capacitance C_{GBi} is the oxide capacitance C_{ox} in series with a voltage dependent depletion capacitance C_d . The total capacitance swings from a maximum of C_{ox} in accumulation for positive V_{gb} to the series combination of C_{ox} and C_d in depletion when V_{gb} is negative. Overlap and fringing capacitances (C_{fr}) are considered to be constant. The parasitic resistance is dominated by the Nwell resistance ($R_{nwb} + R_{nwe}$). The model takes into account the metal style options in calculating parasitic metal capacitance, inductance, and resistance.

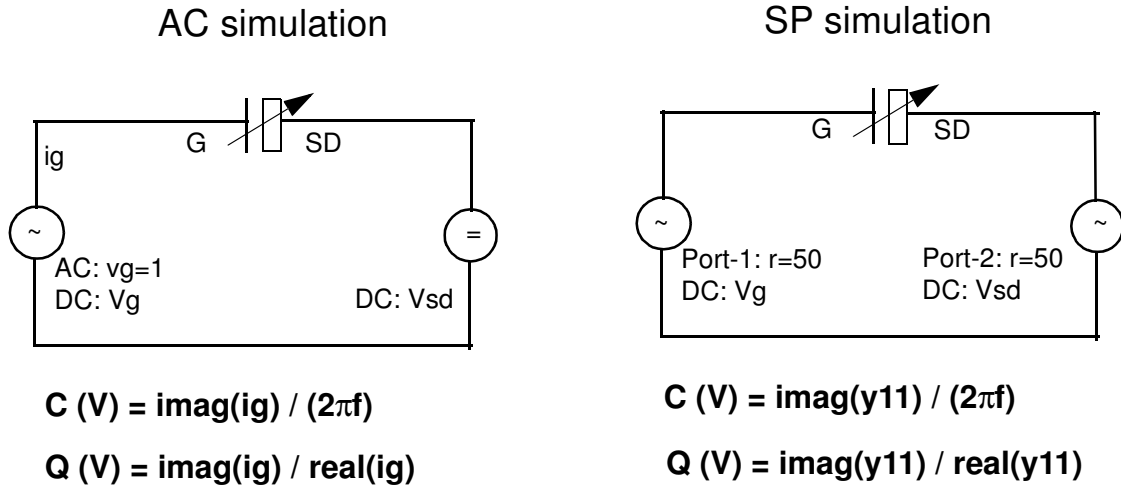
TABLE 10.14 MOS Varactor Model Sub-Circuit Component Descriptions

Circuit Component Description	
C_{GBi}	Intrinsic MOS capacitor
C_{fr}	Overlap and fringing capacitance for poly and metal 1
C_{m2}	Metal 1 to metal 2 capacitance (Metal 2 layout option only)
R_{nwb}	Nwell resistance under oxide
R_{nwe}	Nwell end and contact resistance
R_{gp}	Gate poly resistance (see RF MOSFET chapter, Section 3.2 on page 135 for details)
R_{gm}, L_{gm}	Parasitic resistance and inductance of gate metal
R_{sm}, L_{sm}	Parasitic resistance and inductance of Nwell metal
D_{nw}	Nwell-PSUB junction
C_{sub}	Substrate capacitance
R_{sub}	Substrate resistance

10.3.4 Effective Capacitance and Quality Factor (Q) simulation

There are two methods to simulate MOS varactor RF characteristics as shown in Figure 10.18. The key points for correctly simulating MOS varactor RF characteristics for model verification are:

1. For ac simulation case, ac signal should always be applied at gate (G) terminal, not at source/drain (SD) terminal.
2. For s-parameter simulation case, only parameter y11 is used to calculate C and Q.
3. Make sure dc bias across Nwell-Psub diode is always be set to reversed or zero bias, never goes to forward bias.

FIGURE 10.18 Test diagrams for simulating MOS varactor

DC bias condition: (1) V_g sweep (-2V to 2V), $V_{sd} = 0$, $V_{sub} = 0$;

or (2) V_{sd} sweep (-2V to 2V), $V_g = 0$, $V_{sub} \leq -2V$

10.3.5 Parameter Extraction

The MOS varactor model parameters were physically extracted based on the following sets of test devices:

1. Varying gate length L_g ($0.5\mu\text{m}$ to $2\mu\text{m}$) at fixed $W_g = 3\mu\text{m}$, $N_s=2$, $N_f=10$;

$L_g > 2\mu\text{m}$ gives very low Q values with minimal returns in tuning range. $L_g < 0.5\mu\text{m}$ significantly reduces the tuning range at minimal returns in Q improvement.

2. Varying gate width W_g ($2\mu\text{m}$ to $8\mu\text{m}$) at fixed $L_g = 0.5\mu\text{m}$, $N_s=2$, $N_f=10$;

At $W_g = 8\mu\text{m}$ the Q values drops significantly compare to $W_g = 4\mu\text{m}$, the design kit limit. $W_g < 2\mu\text{m}$ will begin to degrade the tuning range at minimal returns in Q improvement since the Nwell resistance dominates.

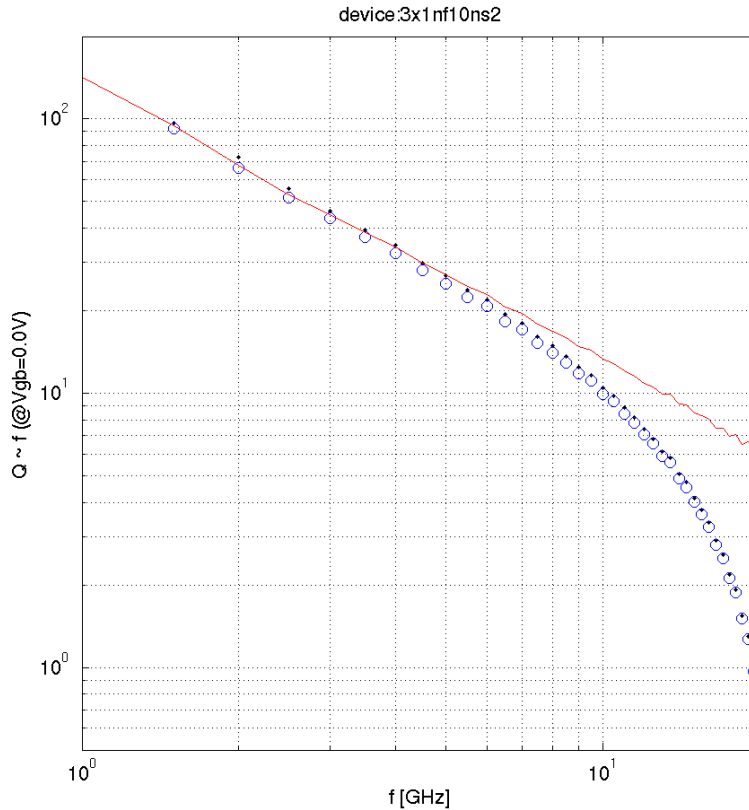
3. Varying N_s and N_f at fixed $L_g = 0.5\mu\text{m}$ and $W_g = 3\mu\text{m}$.

10.3.6 Model Verification

Prior to extracting model parameters, all measurement data is rigorously de-embedded. A detailed OPEN-THRU de-embedding methodology is used in order to properly de-embed all pad and feedline related parasitic resistance, capacitance and inductance. The THRU de-embedding uses an ABCD matrix to extract transmission line related model parameters such as characteristic impedance (z_0) and propagation constant (γ).

Figure 10.19 shows the example of Q vs. frequency data for device: $W_g=3\mu\text{m}$, $L_g=1\mu\text{m}$, $N_s=2$, and $N_f=10$. In this plot, dots represent the raw measured data, circles represents the OPEN de-embedding only data, the solid line represents the data after further THRU de-embedding. The THRU de-embedding technique provides reliable data up to 20GHz.

FIGURE 10.19 Q vs. f for raw data (..), after de-embedding with OPEN (o) and THRU (-)



Figures 10.20 through 10.22 illustrate the MOS varactor model performance, summarized in Table 10.15 through Table 10.17. As L_g increases ($0.5\mu\text{m}$ to $2\mu\text{m}$), capacitance sensitivity (tuning) increases due to more oxide capacitance area relative to fixed fringing capacitor. The minimum Q decreases as a result of significantly increased Nwell resistance with increasing L_g . As W_g increases ($2\mu\text{m}$ to $4\mu\text{m}$), capacitance sensitivity (tuning) increases and Q_{min} decreases slightly. Further increasing W_g to $8\mu\text{m}$, Q starts to drop significantly mainly due to higher gate poly resistance. Figure 10.22 displays model vs. data behavior for the constant $N_s \times N_f$ at fixed $W_g=3\mu\text{m}$, and $L_g=0.5\mu\text{m}$ for *metal 1* style layout. As expected, large N_f and small N_s yields highest Q. Large N_s results in Q degradation from long metal fingers resulting in high metal resistance. All data presented is for *metal 1 only* layouts. Data for *metal 2 style* layouts is currently not available.

TABLE 10.15 Varactor_mos Performance Summary Table for Varying L_g

$W_g=3\mu\text{m}, N_s=2, N_f=10$	$L_g (\mu\text{m})$		
	0.5	1	2
Sensitivity/Tuning [C(0.5V) - C(-0.5V)] / {[C(0.5V) + C(-0.5V)] / 2} * 100	69.2	94.8	111.6
Q (@ 2GHz, 0.5V)	91	43	18

TABLE 10.16 Varactor_mos Performance Summary Table for Varying W_g

$L_g=0.5\mu\text{m}$, $N_s=2$, $N_f=10$	$W_g (\mu\text{m})$			
	2	3	4	8
Sensitivity/Tuning $[C(0.5\text{V}) - C(-0.5\text{V})] / \{ [C(0.5\text{V}) + C(-0.5\text{V})] / 2 \} * 100$	65.4	69.2	71.3	74.8
Q (@ 2GHz, 0.5V)	92	91	88	70

TABLE 10.17 Varactor_mos Performance Summary Table for Varying N_a

$W_g=3\mu\text{m}$, $L_g=0.5\mu\text{m}$	$N_s \times N_f$		
	2x10	5x4	10x2
Sensitivity/Tuning $[C(0.5\text{V}) - C(-0.5\text{V})] / \{ [C(0.5\text{V}) + C(-0.5\text{V})] / 2 \} * 100$	69.2	69.9	70.2
Q (@ 2GHz, 0.5V)	91	84	68

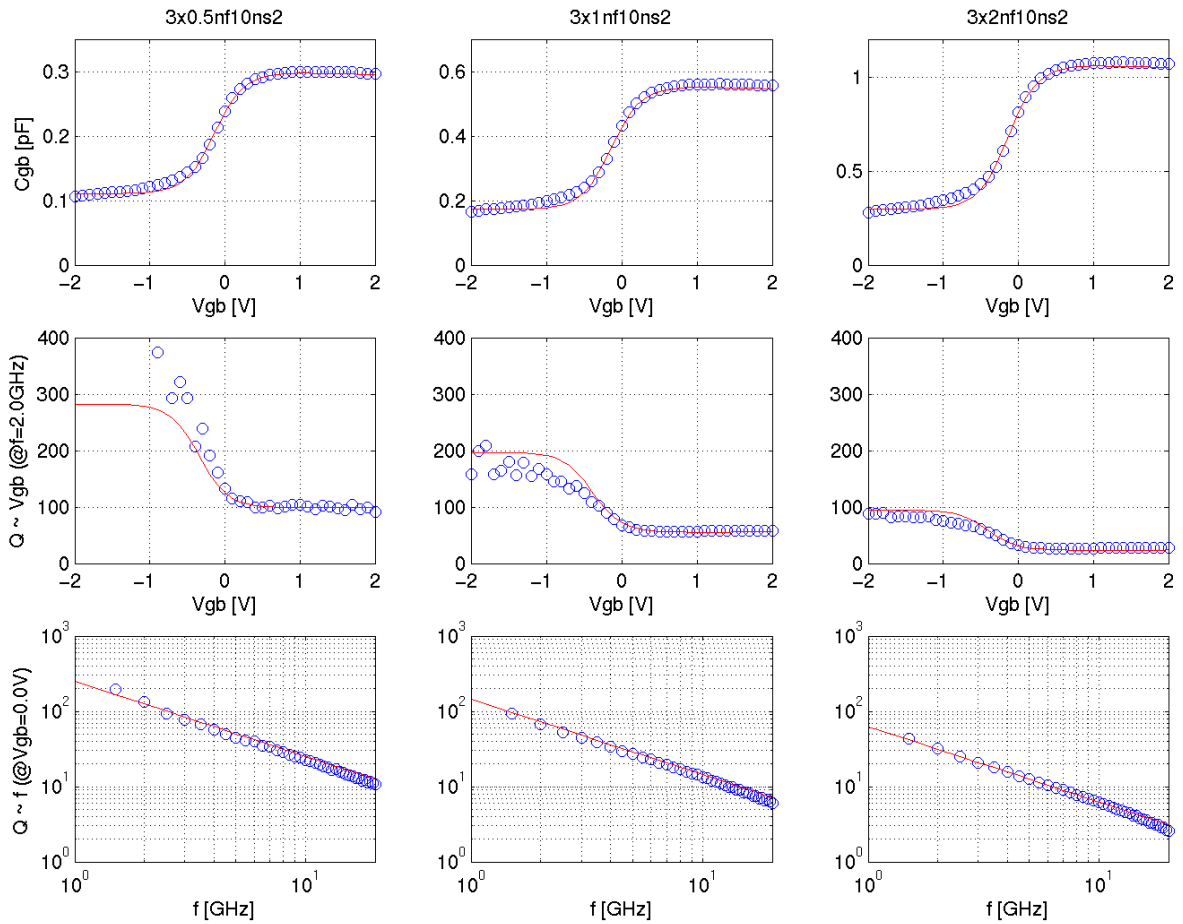
FIGURE 10.20 MOS varactor - Varying L_g 

FIGURE 10.21 MOS varactor - Varying W_g

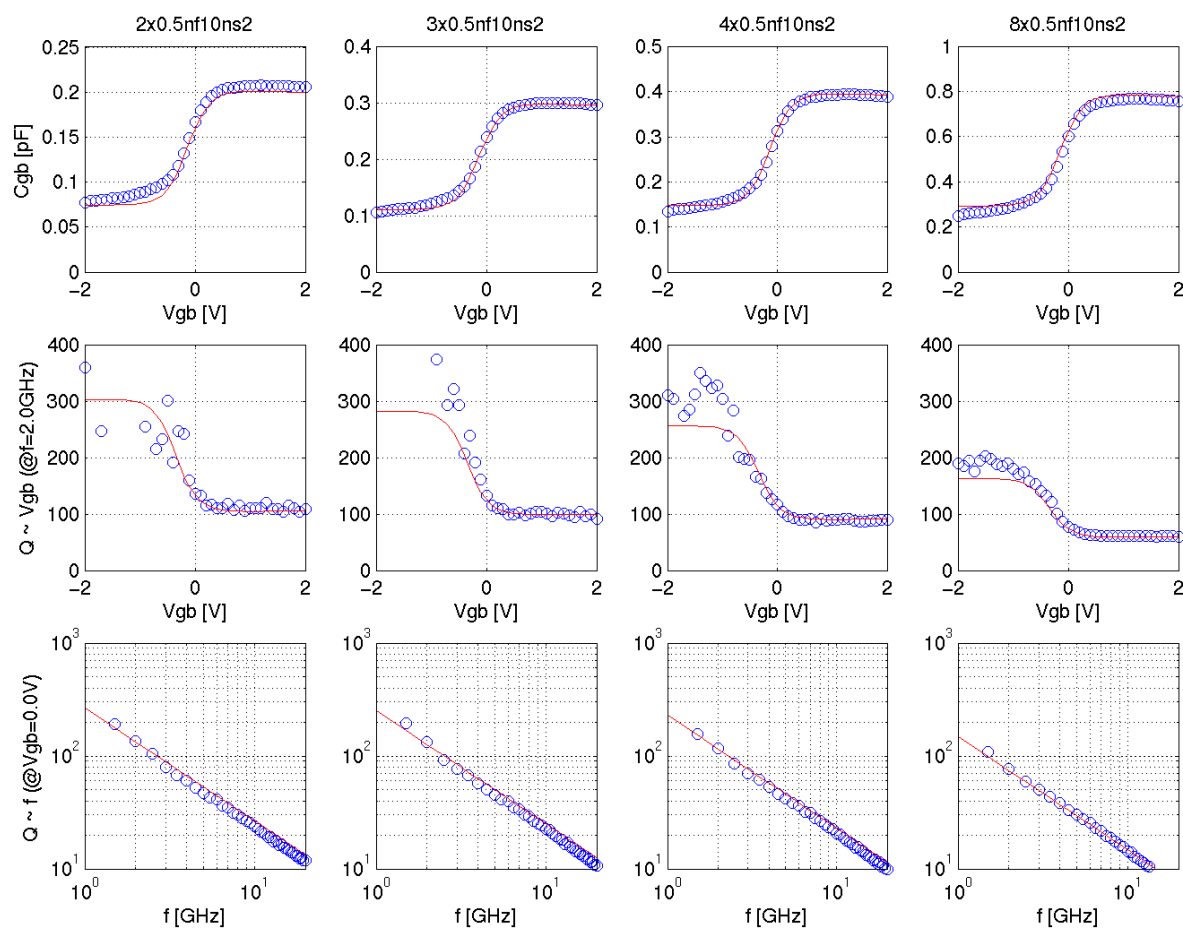
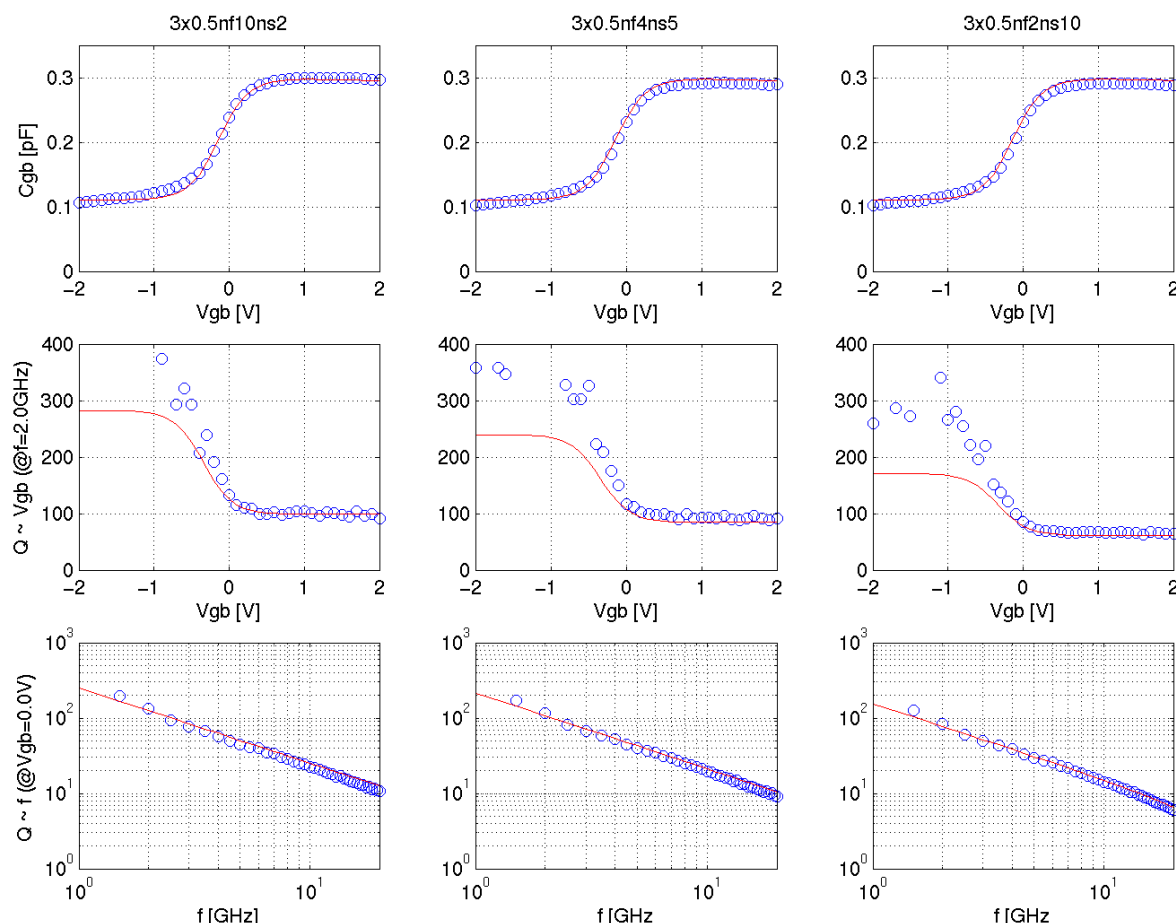


FIGURE 10.22 MOS varactor - Varying $N_s \times N_f$, with constant C_{gb} 

10.3.7 MOS Varactor Statistical and Corner models

For the most part, the MOS varactor is directly correlated with the MOSFET statistical parameters. The MOS capacitance is directly correlated with the MOSFETs. The Nwell resistance under the gate is dominated by the surface doping and hence is correlated with the threshold variance of the PFET. For the FAST case, the capacitance increases and the nwell resistance increases from the lower threshold implant. Thus, the fast case yields lowest Q and vice versa for the SLOW case. See Section 15.0 for further explanation of the device interdependencies in the corner models and use of the X-Sigma corner models. Figure 10.23 displays the 3 sigma corner simulations for the MOS varactor with typical device size of 3x0.5x2x10.

Table 10.18 lists the measured and simulated ESPEC values for MOS varactor. The capacitance value $C(1V)$ in the table shows the highest capacitance value at $V_{gb}=1V$ for a larger device size 3x0.5x15x25 used in the PCM test. The Q values listed in the table show the Q_{min} (at $V_{gb}=1V$) at three different frequencies (1.9G, 5G and 10G) for a typical RF test device size: 3x0.5x2x10.

FIGURE 10.23 MOS varactor - Corner Model

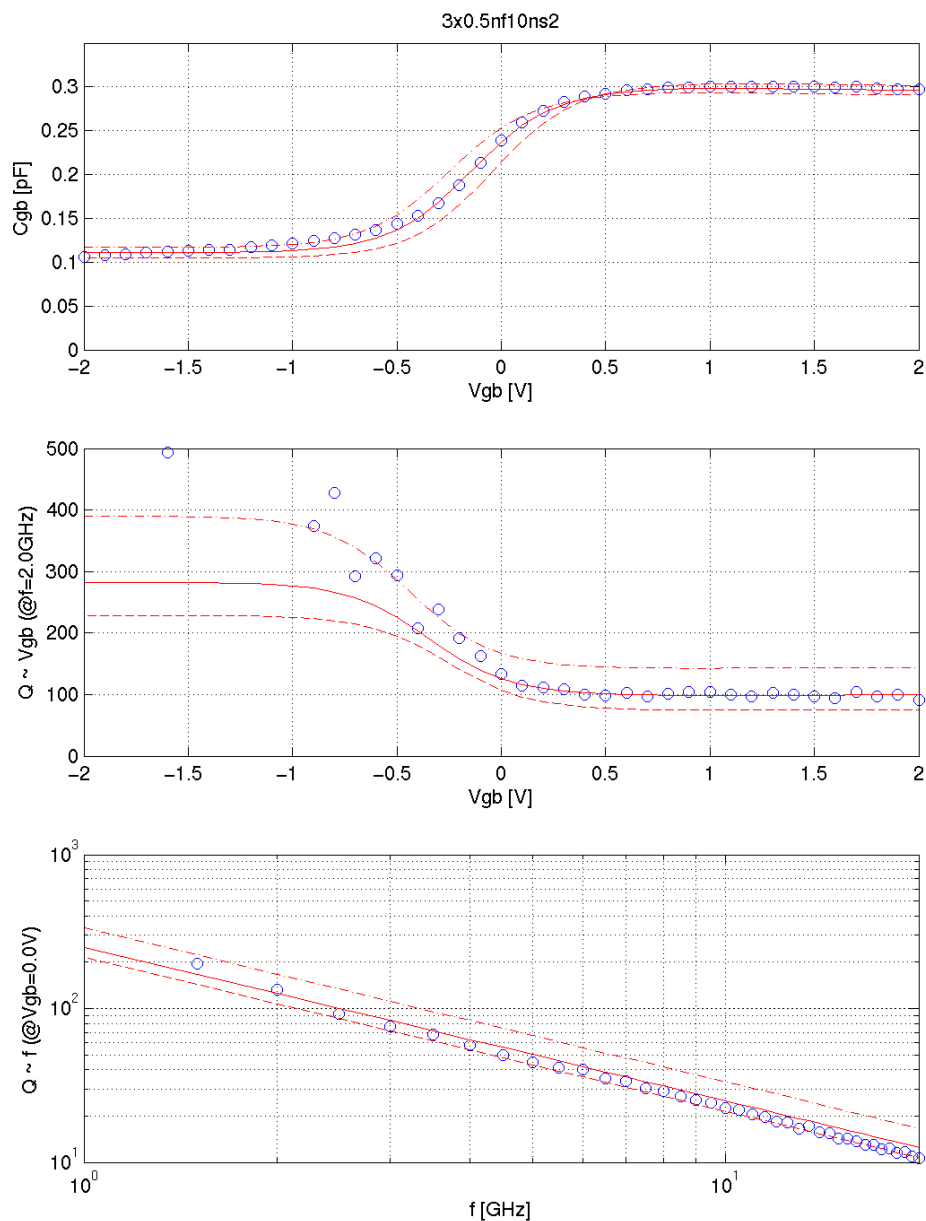


TABLE 10.18 Espec, Corner and Statistical Model Comparison for MOS Varactor Model

Parameter	device WgxLgxNsxNf	unit	Slow			Nom			Fast		
			Espec	Corner	Stat	Espec	Corner	Stat	Espec	Corner	Stat
C(1V)	3x0.5x15x25	pF	TBD	5.48	5.44	5.63	5.59	5.62	TBD	5.7	5.79
sensitivity ¹	3x0.5x15x25	%/V	60.9	61	61.2	72.5	72.3	71.8	84.1	83.8	82.4
Q(1.9G,1V)	3x0.5x2x10		75	78.9	78.9	100	104	104			
Q(5G, 1V)	3x0.5x2x10		30	30	30.2	40	39.5	39.5			
Q(10G,1V)	3x0.5x2x10		15	15	15.1	20	19.7	19.7			

ESPEC notes:

1. Capacitance sensitivity definition: $[C(0.5V) - C(-0.5V)] / \{[C(0.5V) + C(-0.5V)] / 2\} * 100$

TABLE 10.19 TOX Variation in Corner and Statistical Models

	3- σ Corner		3- σ Stat	
	Espec	Model	Espec	Model
thin tox	+/- 1A	+/- 1A	+/- 1.5A	+/- 1.5A
thick tox	+/- 1.8A	+/- 1.8A	+/- 3A	+/- 3A

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10.4 Varactor models update history

TABLE 10.20 MOS Varactor model specific updates in model release version 5.0

v5.0 update	Reason	Impact on user
Corner/Statistical model oxide thicknesses	Updated to match new E-spec. with tighter variation	No change in NOMINAL model. Reduced corner/statistical model variation in gate oxide capacitance: corner model: v3.3a +/- 3Å; v3.4 +/- 1Å 1stat. model: v3.3a +/- 3Å; v3.4 +/- 1.5Å
Corner Model Change so that fast gives low Q, slow gives high Q. Q controlled by 1/RC. For FAST MOSFET, means high C (thinner tox) and low surface implant, high resistance, hence low Q varactor.	Provide consistency with MOSFET corners.	FAST and SLOW MOSFET Corners will yield reverse Q results from prior release.
Added silicide-polysilicon contact resistance to the gate resistance	Silicide-polysilicon gate resistance is a significant component of gate resistance for narrow width (<3µm) RF FETs with 2-sided gate contacts	No real impact as Wg range for Mos Varactor is 2-4µm. Old model was able to compensate for this effect. New model is more physical and consistent with MOSFET.

TABLE 10.21 All varactor models specific updates in model release version 6.0

v6.0 update	Devices	Reason	Impact on user
X-Sigma Corner Model Support	varactor_bl, varactor_ni, varactor_mos	Allow for process variation settings different than conventional +/- 3 sigma-corner models	Added flexibility in corner simulation
Increase Q	varactor_bl, varactor_ni	Improved measurement techniques	Higher Q simulation. Qmin increased from 35 to 50 for varactor_bl, and 40 to 50 for varactor_ni

10.5 References

1. P. Andreani and S. Mattisson, "On the use of MOS varactor in RF VCO's," IEEE JSC, June 2000
2. H. M. Greenhouse, "Design of planar rectangular microelectronic inductors," IEEE PHP, June, 1974

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11.0 Resistor Models

11.1 Device Description

The SBC18 process supported resistors are given in Table 11.1 with cross sections shown in Figure 11.1. The poly and metal resistors are very linear for reasonable length geometries and are thus modeled by linear resistors. Short resistors can experience velocity saturation for larger biases which is not modeled. Due to the lower doping of the Nwell, non linear effects due to JFET pinching are significant for all geometries. This JFET effect is included in the model.

For all resistors, the resistance can be changed through choice of Finger Width “W”, length “L” and number of fingers “Strips” in the component property window. A CDS calculator updates the resistance value using the nominal electrical specification. For the Nwell resistor, this result corresponds to zero bias at the terminals.

TABLE 11.1 SBC18 Supported Resistors

Design Kit Name	Description	sheet rho
rppoly_sal or rps	Salicided poly resistor	5.5
rppoly_lo or rpp3t	Low value unsalicided poly resistor	235
rppoly_hi or rph3t	High value unsalicided poly resistor	1K
rtin, rtin_m1	TiN metal resistor between M3 & M4	24.5
rnwell or rw3t	Nwell resistor	890

FIGURE 11.1 Cross section of Salicided Poly Resistor; Low Value and High Value Poly Resistor

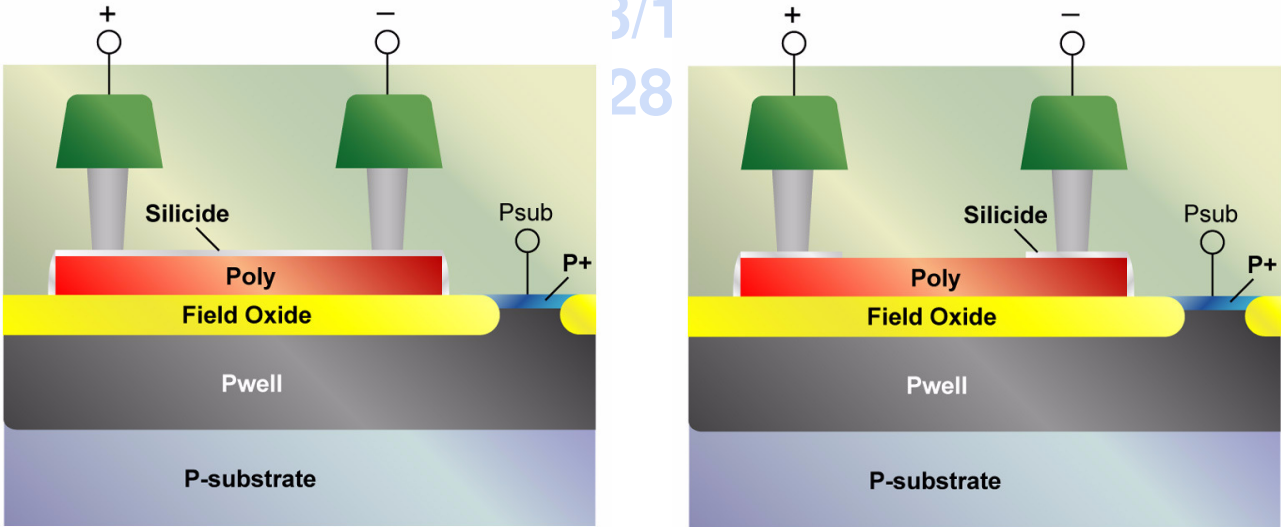
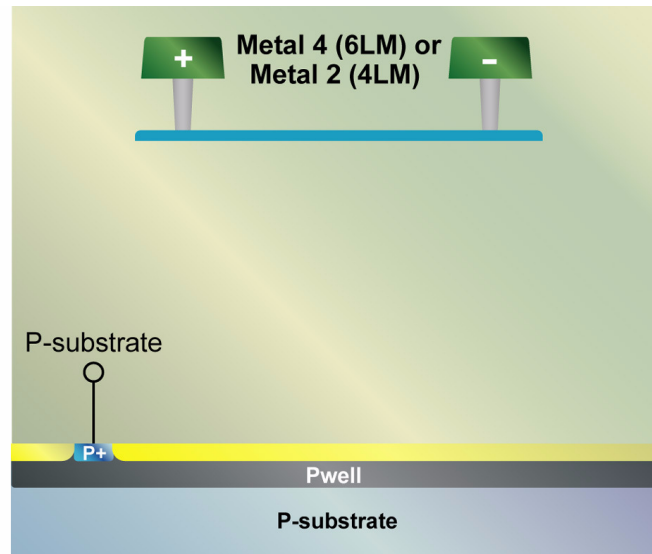
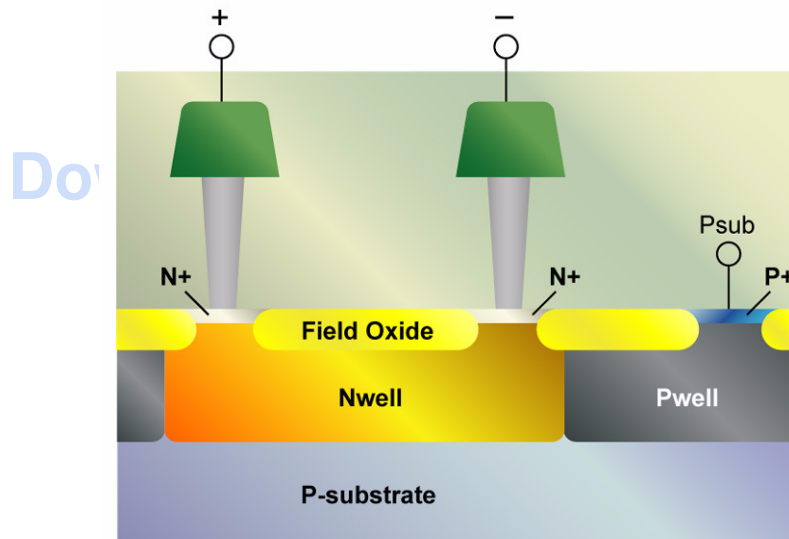


FIGURE 11.2 Cross section of the Metal Resistor**FIGURE 11.3 Cross section of the Nwell Resistor**

11.1.1 Poly Resistors Over Nwell

Poly resistors may be placed over Nwell to provide improved isolation from the substrate. In this case, the poly resistor must be entirely inside the Nwell. The poly may not straddle any Nwell layer. The models do not account for Nwell. The Nwell is netlisted to the 3rd terminal, Psub, in Figure 11.4. There is no connectivity between the Nwell and Psub checked by the LVS decks, thus placing Nwell under poly resistors should be done with great caution.

11.2 Model Description

The equivalent circuit representation of the poly resistors is shown in Figure 11.4. The individual components listed in Table 11.2 are based on physical models and are computed using geometrical and electrical process spec information. The base resistance equation is given by

$$R = \frac{\rho_{\square} \cdot L + R_{end}}{W + \Delta W} \quad (\text{EQ 1})$$

where ΔW is the change in effective width, ρ_{\square} is the sheet resistance, and R_{end} is the end resistance. The equivalent circuit for an Nwell resistor is shown in Figure 11.5 where R_{nwell} is described by a voltage dependent resistance implemented in Verilog-A. R_{nwell} is given by (EQ 1) at zero bias.

FIGURE 11.4 Sub-Circuit model for resistor

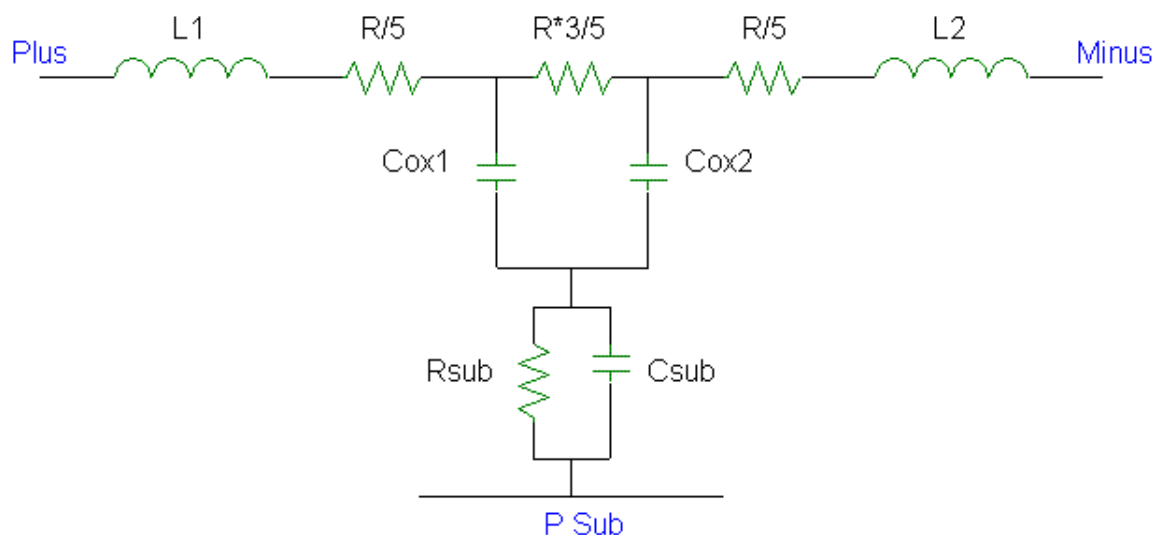


FIGURE 11.5 Sub-Circuit model for Nwell resistor

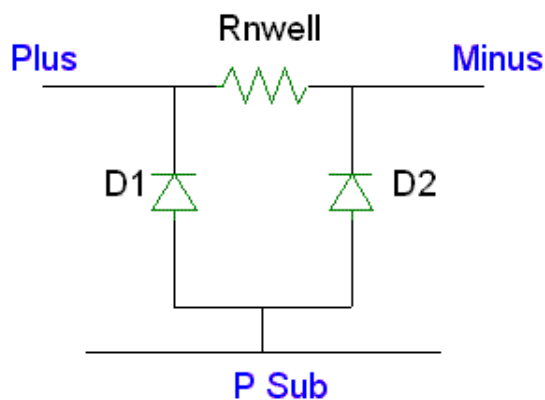


TABLE 11.2 Resistor Model Sub-circuit Component Names

Circuit Components	
R	Poly resistance
L1, L2	Resistor self-inductance
Cox1, Cox2	Oxide capacitance
Rnwell	Resistance of Nwell
D1, D2	Diodes associated with Nwell
Csub	Substrate capacitance
Rsub	Substrate resistance

11.3 Model Verification

DC measurements are performed over temperature for the SBC18 resistors. The temperature coefficients TC1 and TC2 are extracted based from measurements with ranging from -40 to 125 C. The temperature model equation is

$$R(T) = R_{T25} \cdot [1 + TC1 \cdot (T - T25) + TC2 \cdot (T - T25)^2] \quad (\text{EQ 2})$$

Figure 11.6 - Figure 11.10 show the measured data and the simulated results for temperature range from -40C to 125C for low value unsalicyded poly resistor (rpp3t), high value unsalicyded poly resistor (rph3t), salicyded P - poly resistor (rps), metal resistor (rtin) and nwell resistor (rw3t) respectively. Figure 11.11 shows the nwell resistor model validation over voltage.

FIGURE 11.6 rpp3t temperature characteristics comparison between data and model

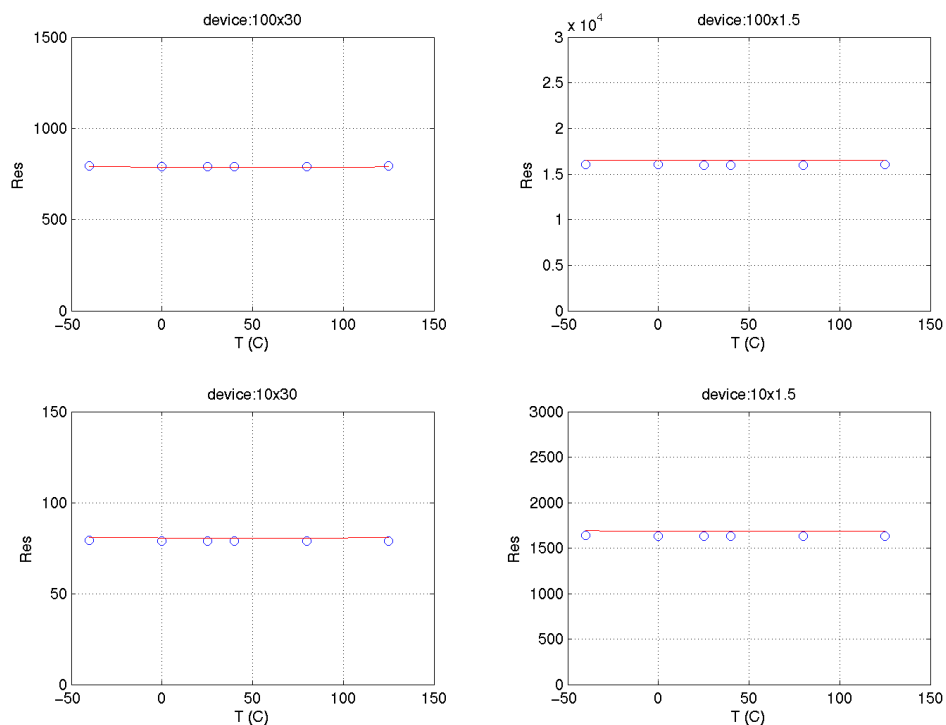


FIGURE 11.7 rph3t temperature characteristics comparison between data and model

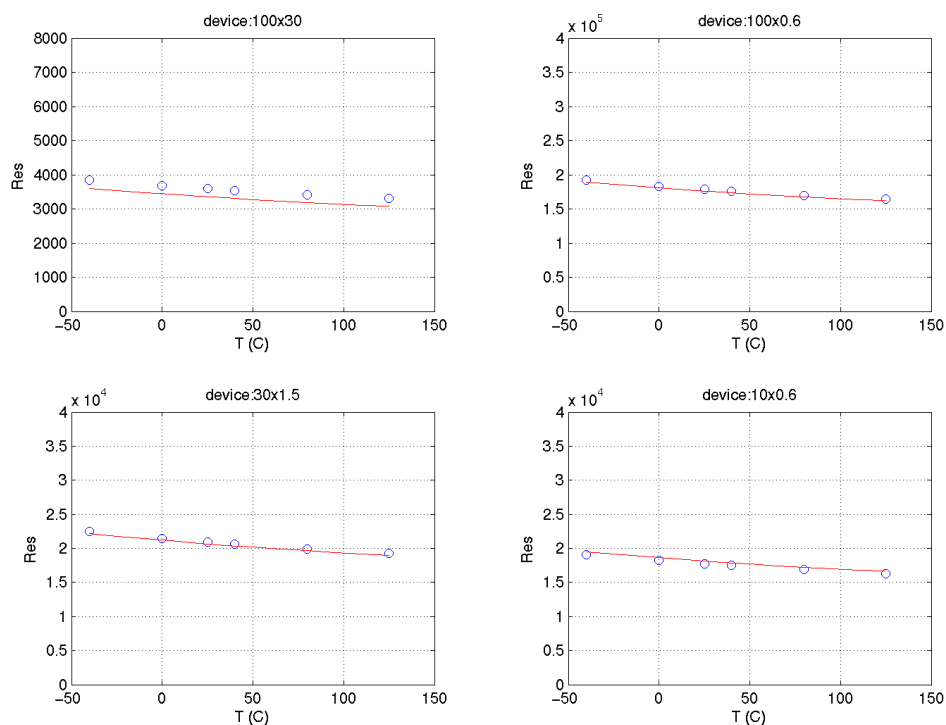


FIGURE 11.8 rps temperature characteristics comparison between data and model

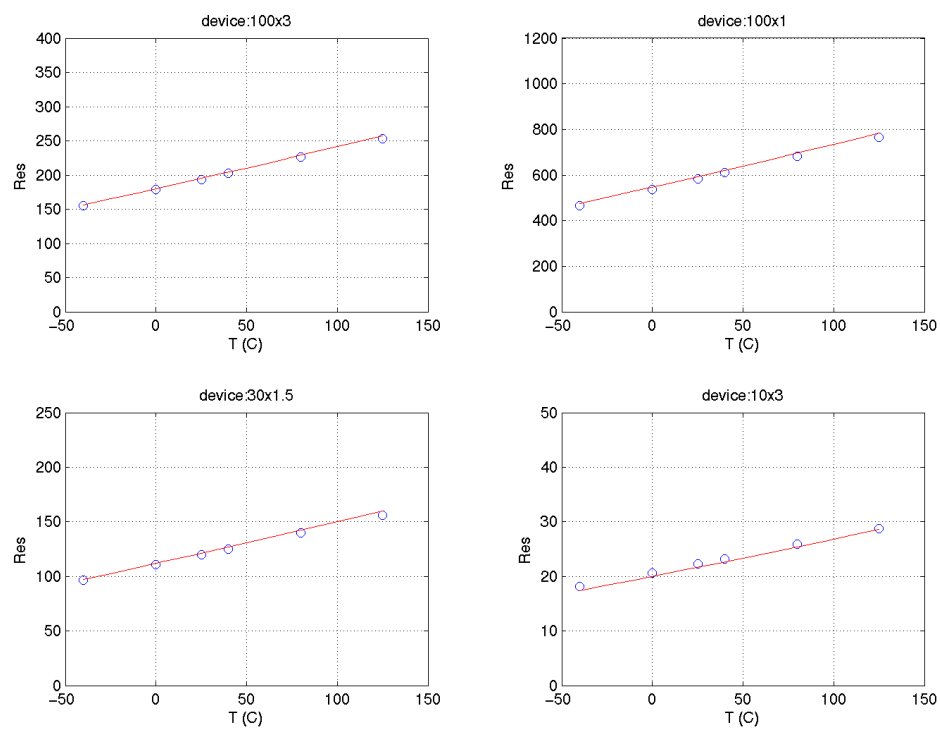


FIGURE 11.9 rtin temperature characteristics comparison between data and model

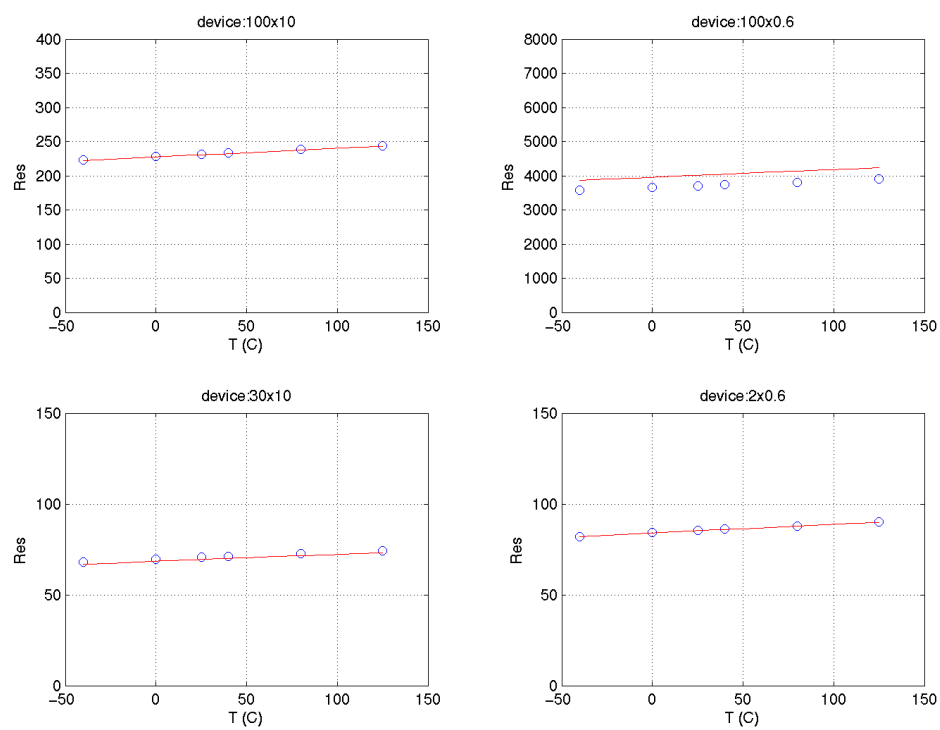


FIGURE 11.10 rw3t temperature characteristics comparison between data and model

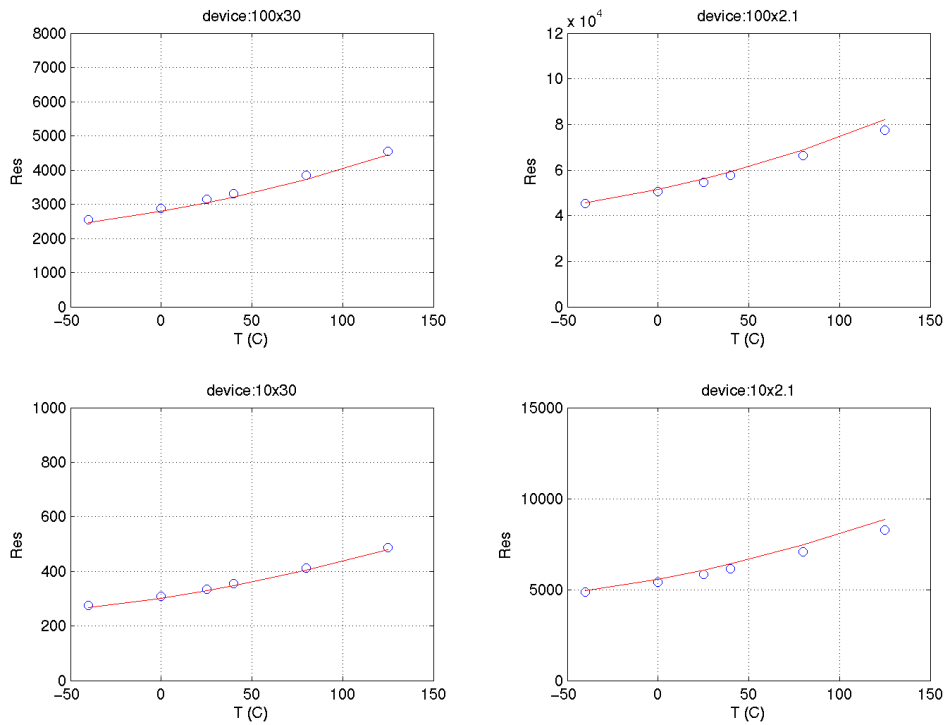
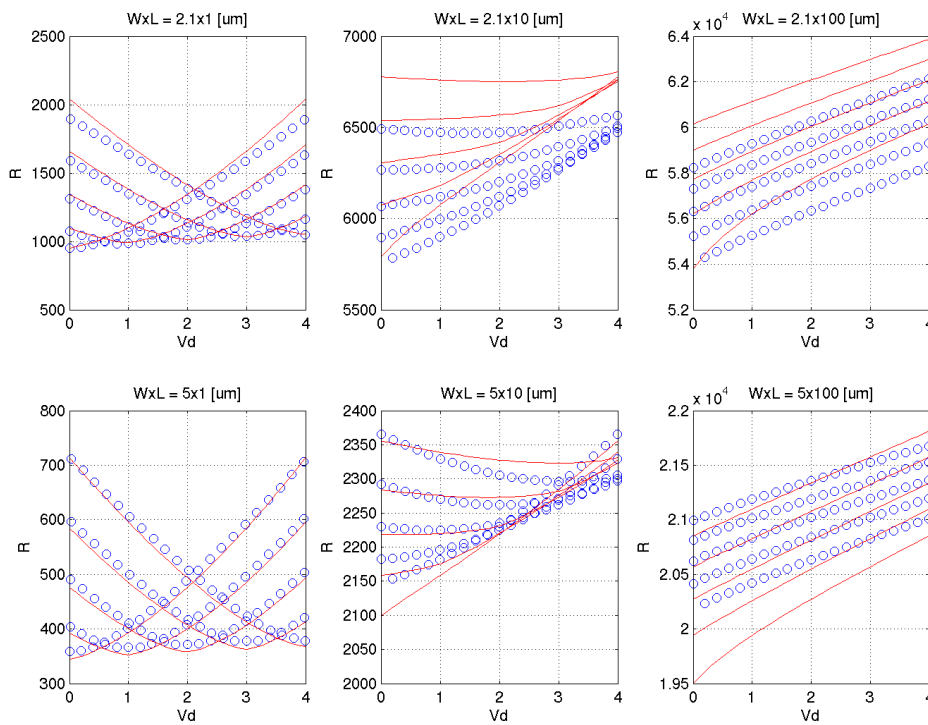


FIGURE 11.11 Nwell resistor (rw3t) over voltage (T=25C)



11.3.1 Espec, Corner and Statistical model comparison

The resistor statistical and corner models account for process variation of the ΔW , sheet resistance ρ_q , and end resistance R_{end} derived directly from the process ESPECs. The Resistor model parameters are directly correlated with the process parameters. The corner performance is determined using the min and max values in the ESPECs. See Section 15.0 for further explanation of the device interdependencies in the corner models and use of the X-Sigma corner models. Table 11.3 lists the resistor specific ESPEC value compared to simulated corner and statistical values for the SBC18 resistors.

TABLE 11.3 Espec, Corner and Statistical model comparison for resistor model

Device	name	units	Slow			Nom			Fast		
			Espec	Corner	Stat	Espec	Corner	Stat	Espec	Corner	Stat
rpp3t	rs	ohm/sq	265	266	264	235	235	235	205	204	205
	rend	ohm-um	90	90	89.9	60	60	60.4	30	30	30.8
	dw	um	-0.04	-0.04	-0.04	-0.00	-0.00	-0.00	0.04	0.04	0.04
rph3t	rs	ohm/sq	1150	1150	1150	1000	1000	1000	850	852	855
	rend	ohm-um	600	601	614	320	321	326	40	40	39
	dw	um	-0.04	-0.04	-0.04	-0.00	-0.00	-0.00	0.04	0.04	0.04
rps	rs	ohm/sq	6.8	6.78	6.81	5.5	5.47	5.49	4.2	4.15	4.18
	rend	ohm-um	9.2	9.16	9.25	7.2	7.16	7.15	5.2	5.15	5.04
	dw	um	0	0	0	-0.02	-0.02	-0.02	-0.04	-0.04	-0.04
rtin	rs	ohm/sq	28	28	28	24.5	24.5	24.5	21	21	21
	rend	ohm-um	19	18.9	19.6	12	12	12.2	5	5	4.7
	dw	um	-0.05	-0.05	-0.05	-0.03	-0.03	-0.03	-0.01	-0.01	-0.01
rw3t	rs	ohm/sq	1070	1070	1070	890	888	889	710	710	708
	rend	ohm-um	900	920	913	680	688	684	450	455	456
	dw	um	-0.72	-0.74	-0.71	-0.45	-0.45	-0.45	-0.17	-0.17	-0.18

11.4 Resistor Mismatch Models

11.4.1 Mismatch Measurements

A detailed description of resistor mismatch characterization methodology and results are available in the Jazz Semiconductor document NPB PS-0392 titled “Analog Characterization Report for SBC18.” The basic set-up is a kelvin measurement of 2 matched pairs. Resistor mismatch characterization is only available for poly resistors.

11.4.1.1 Resistor Mismatch Modeling

The resistor mismatch included in the design kit takes into account area and perimeter capacitance mismatch variations. Mismatch due to spacing variation is not included in the model. The mismatch models for the ΔW , sheet resistance ρ_q , end resistance R_{end} are given by

$$\rho_{\square mm} = \rho_{\square nom} \left(1 - \frac{\sigma_A}{\sqrt{LW}} \right) \quad (\text{EQ 3})$$

$$R_{endmm} = R_{endnom} \left(1 - \frac{\sigma_B}{\sqrt{LW}} \right) \quad (\text{EQ 4})$$

$$\Delta W_{mm} = \Delta W_{nom} \left(1 - \frac{\sigma_C}{\sqrt{W}} \right) \quad (\text{EQ 5})$$

where σ_A , σ_B , and σ_C are the mismatch coefficients extracted via a nonlinear least squares global optimization method to best fit the measured data.

11.4.1.2 Mismatch Model Usage Guidelines

The mismatch model is available in Spectre, which provides the necessary framework to model the local mismatch between resistors. It is implemented inside the “sub-circuit” definition of the resistors allowing for “instance to instance” variations in the process parameters. The “variations” variable inside Spectre should be set equal to “mismatch.” Typically, ~100 monte-carlo runs are sufficient to accurately simulate the local-mismatch between the resistors. The user should, however, increase the “numruns” variable inside Spectre until the improvement in the simulated results is small.

11.4.2 Mismatch Model Verification

The mismatch between closely spaced resistor pairs follows a geometric dependence. An extraction process was performed to determine the mismatch coefficients for resistor parameters of ΔW , ρ_{\square} , and R_{end} . These coefficients are used in the statistical model card. The Spectre to measurement mismatch results are shown in Figure 11.12 through Figure 11.15 for the poly and metal resistors. Mismatch characterization and modeling is not available for N-well resistors. To obtain good matching results, it is preferable to not use minimum dimension but larger size resistors.

FIGURE 11.12 Low-Value Unsalicided Poly resistor mismatch

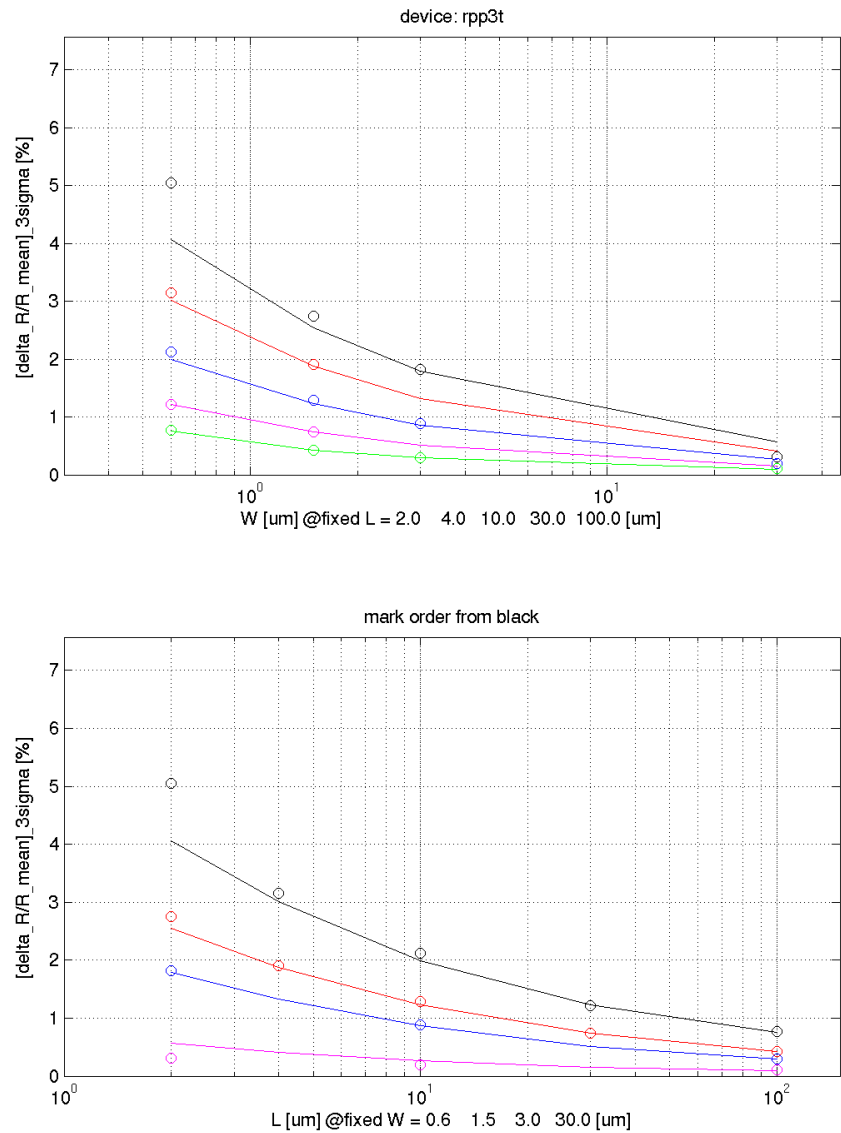
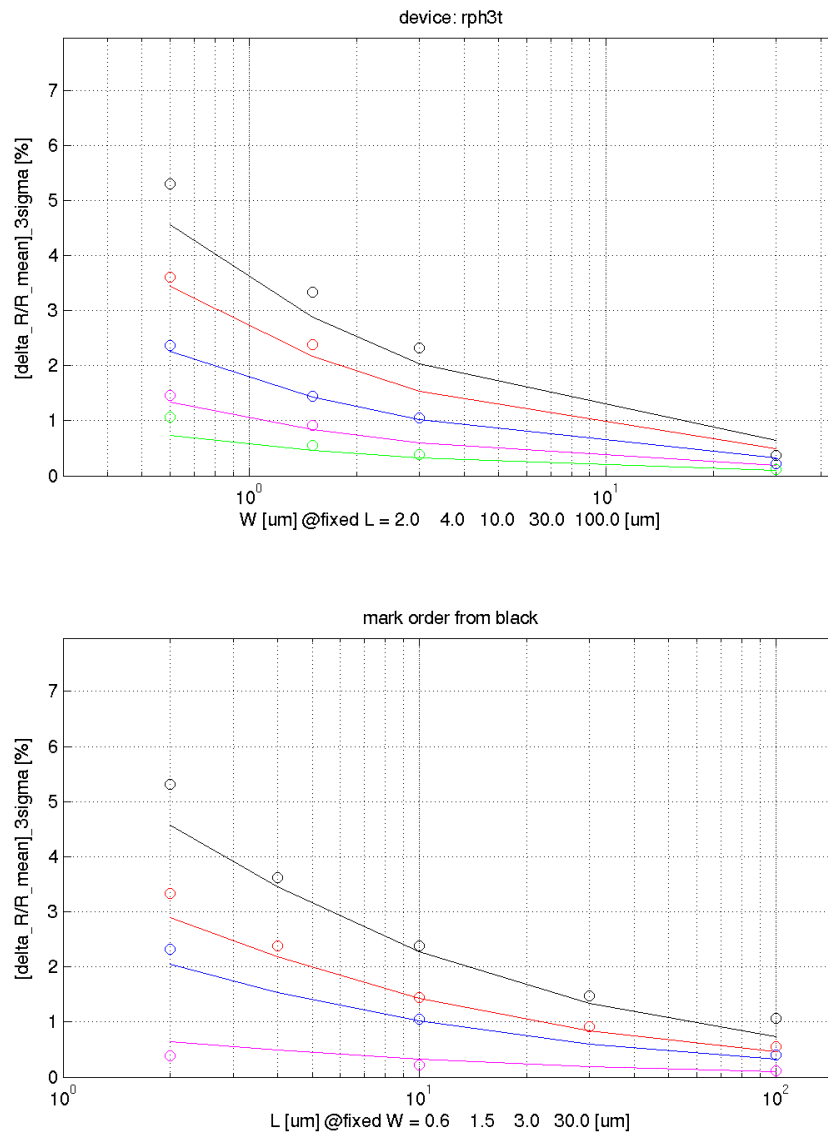


FIGURE 11.13 High-Value Unsalicded Poly resistor mismatch



in

FIGURE 11.14 Salicided Poly resistor mismatch

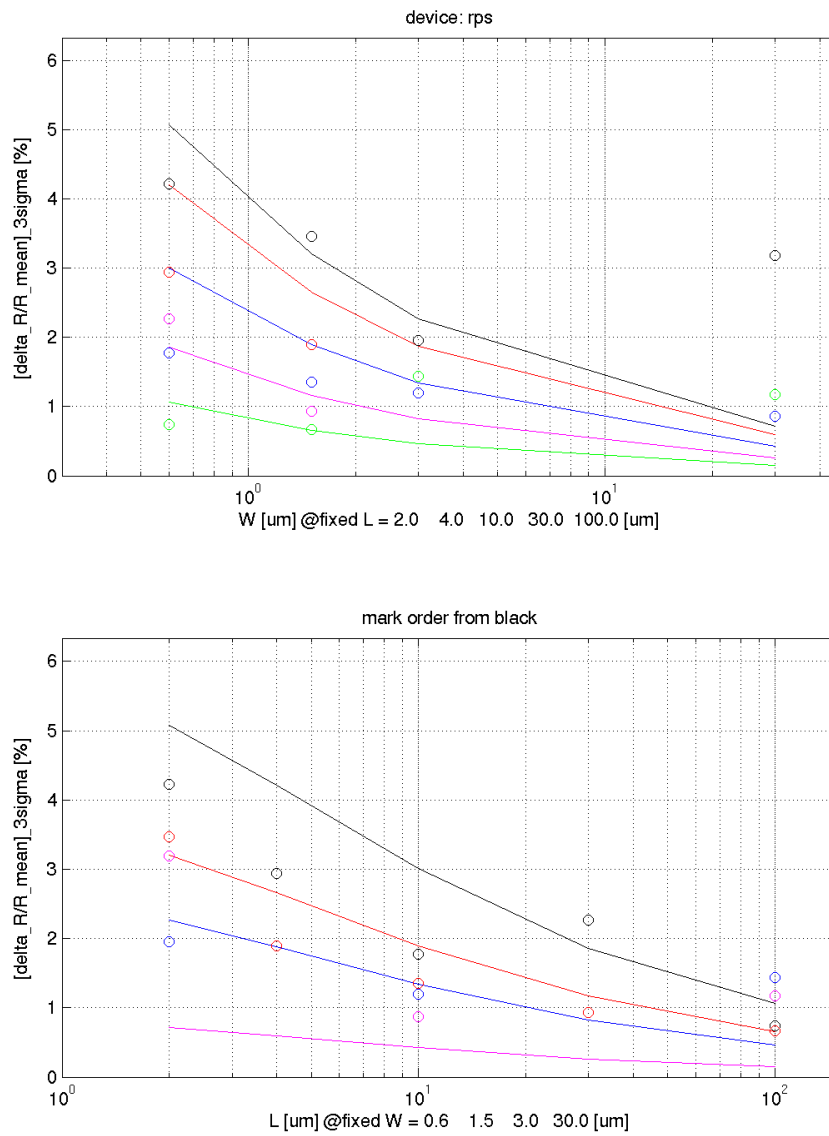
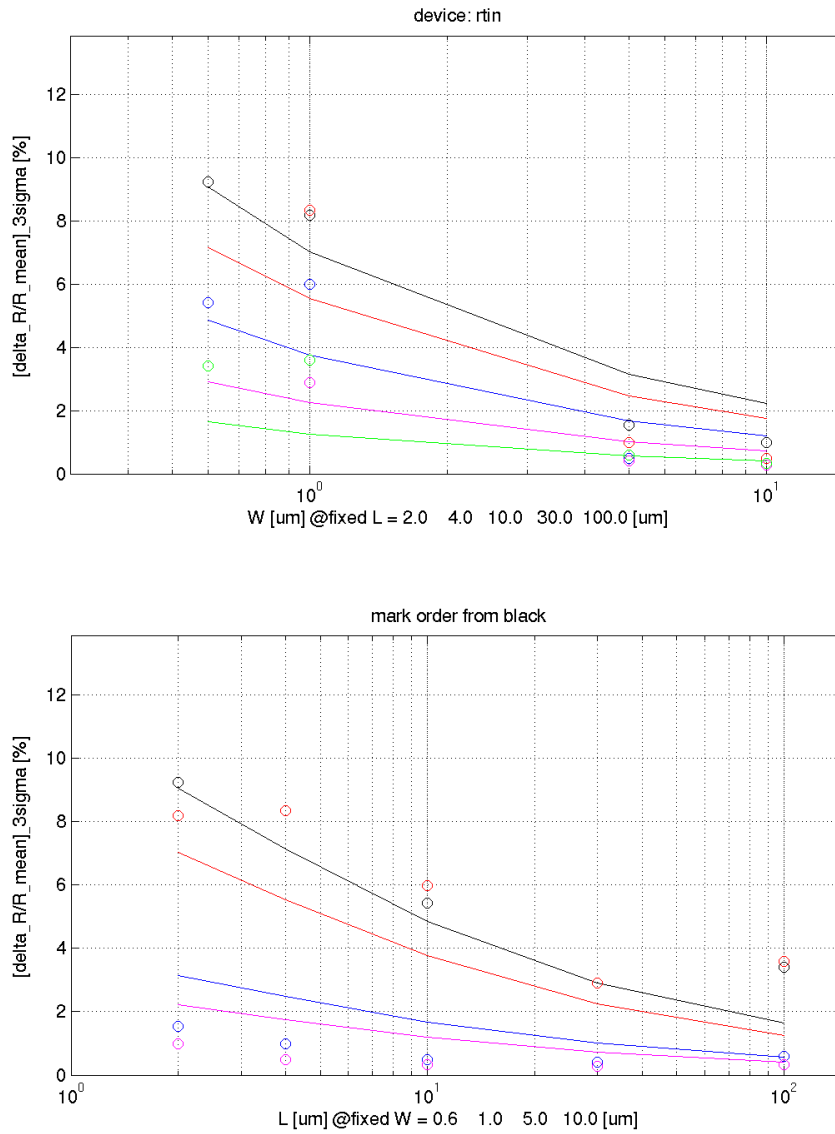


FIGURE 11.15 TiN resistor mismatch



11.5 UnsaliCided Poly Resistor 1/f Noise Model and Verification

Poly-silicon resistors exhibit current noise that is at lower frequencies inversely proportional to frequency and area of the resistor. At higher frequencies the 1/f dependence is replaced by thermal noise which is described by

$$\sqrt{S_{th}} = \sqrt{\frac{4 \cdot k \cdot T}{R}} \quad \left[\frac{A}{\sqrt{Hz}} \right] \quad (\text{EQ 6})$$

The 1/f noise is caused by charge trapping and de-trapping events at the poly-silicon grain boundaries. These events change the energetic barrier and thus modulate the resistance or current over the grain boundary. A physics based equation was proposed in IEEE Transactions on Electron Devices, Vol48, No.6, June 2001 by Brederlow et al.

$$S_I = \frac{I^2}{W \cdot L} \cdot \frac{\alpha}{f} \quad \left[\frac{A^2}{Hz} \right] \quad (EQ 7)$$

where S_I is the noise current per frequency band width and α is the parameter extracted to measured data. This equation was implemented in the Spectre model cards for **unsalicided poly resistors** by matching it with the coefficients of the Spectre provided noise equation.

$$\sqrt{S_I} = \sqrt{\frac{KF \cdot I_r^{AF}}{f}} \quad \left[\frac{A}{\sqrt{Hz}} \right] \quad (EQ 8)$$

where $I_r = I$, $AF = 2$, and $KF = \alpha/(WL)$.

The model verification plots are shown in Figure 11.16 through Figure 11.18.

FIGURE 11.16 Flicker Noise (rpp3t)

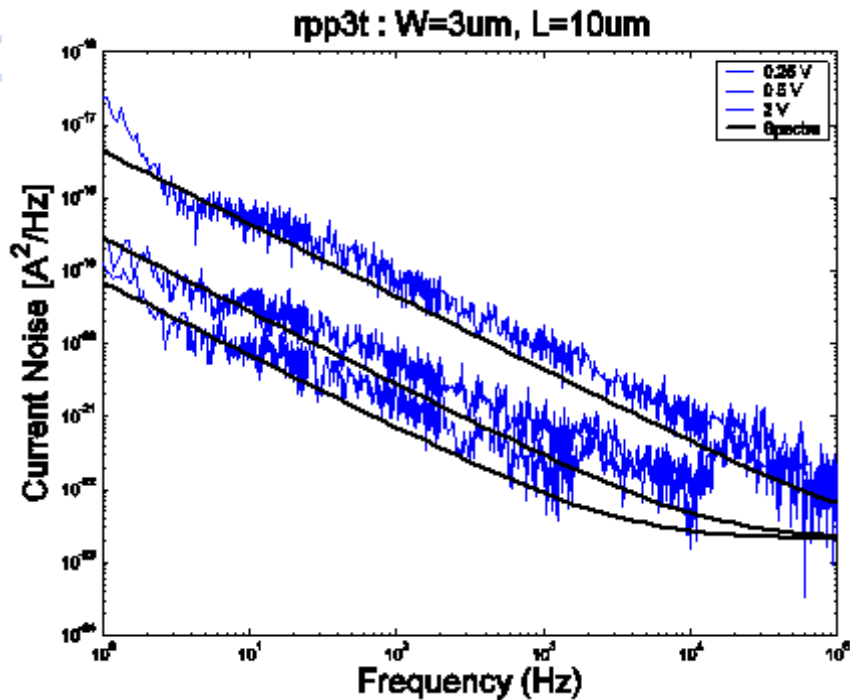


FIGURE 11.17 Flicker Noise (rpp3t)

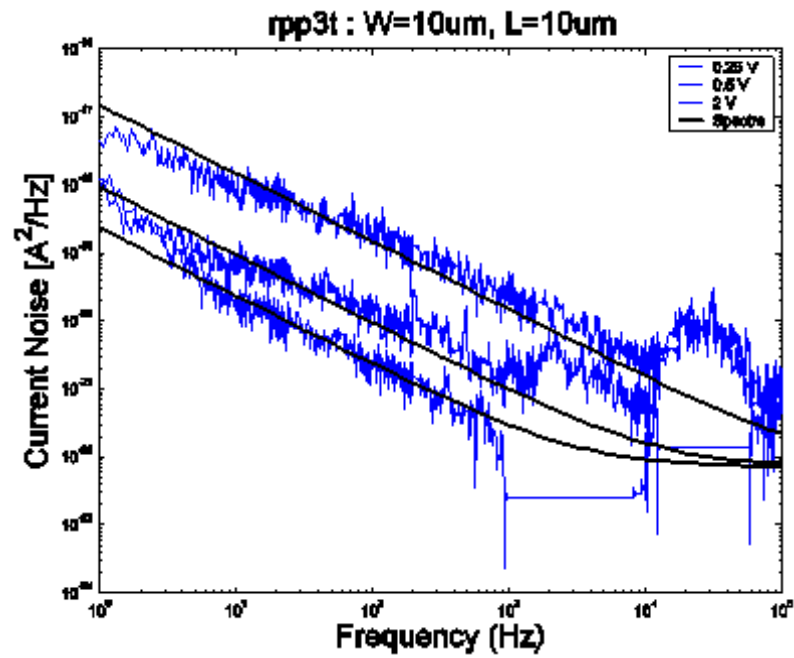
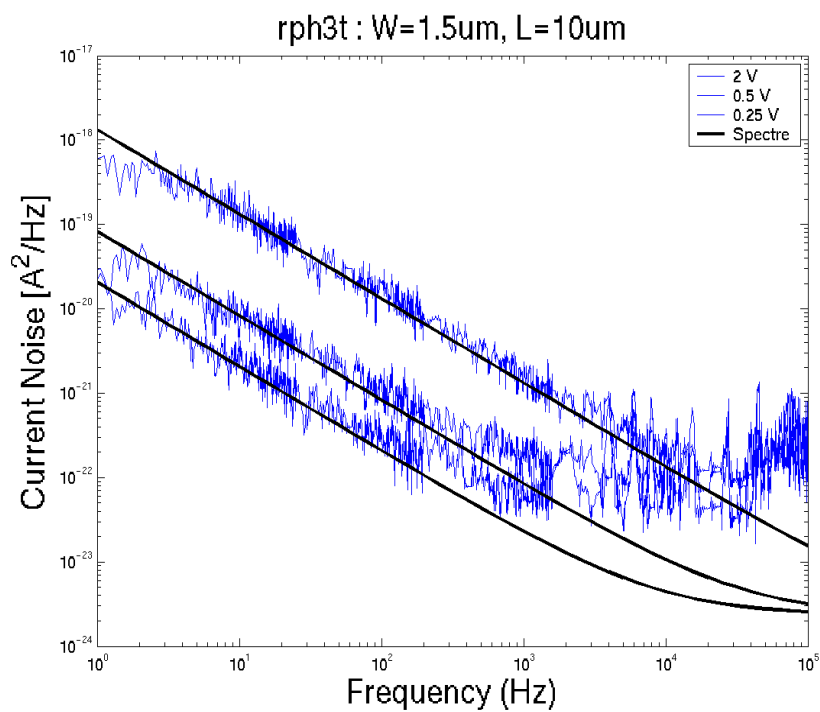


FIGURE 11.18 Flicker Noise (rph3t)



11.6 Resistor models update history

TABLE 11.4 Resistor models specific updates in model release version 6.0

v6.0 update	Devices	Reason	Impact on user
X-Sigma Corner Model Support	All	Allow for process variation settings different than conventional +/- 3 sigma-corner models	Added flexibility in corner simulation

TABLE 11.5 Resistor models specific updates in model release version 6.1

v6.1 update	Devices	Reason	Impact on user
Flicker noise in ADS and Hspice	rpp3t, rph3t	ADS and Hspice models now support flicker noise in resistors	Noise simulations will now include flicker noise

TABLE 11.6 Resistor model specific updates in model release version 6.2

v6.2 update	Devices	Reason	Impact on user
ΔW model parameter change from -0.03 to $0 \mu\text{m}$	rph3t (high-value poly resistor)	Aligned model to new E-specs based on Fab statistics	Increased resistance in narrow width resistors
ΔW model parameter change from -0.07 to $0 \mu\text{m}$	rpp3t (low-value poly resistor)	Aligned model to new E-specs based on Fab statistics	Increased resistance in narrow width resistors

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Downloaded by: Sanjay Raman
Date: 08/15/2012 10:15
IP: 128.173.89.96

12.0 Capacitor Model

12.1 MIM capacitor model

12.1.1 Definitions and usage guidelines

The SBC18 technology offers vertical MiM capacitor densities and metal layer configurations given in Table 12.1. Refer to the SBC18 design rule document NPB PS 0179 for available MiM configurations in the various technology nodes.

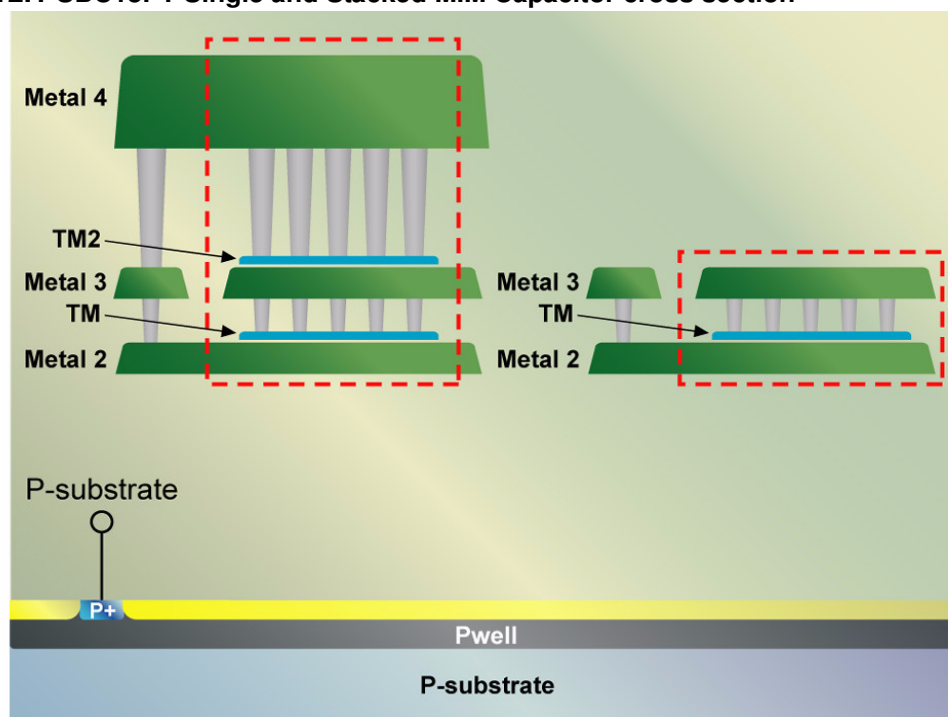
TABLE 12.1 SBC18 MIM Capacitors

MiM Definition	PDK Name	Leagacy PDK Device Name
2fF between M2-M3	cmim[w]2[_4] (3/4-terminal), cmim2_2 (2-terminal)	c3t_mim2, c3t_mimw2
2fF between M4-M5	cmim[w]2[_4] (3/4-terminal), cmim2_2 (2-terminal)	cmim2, cmimw2_4
4fF stacked between M2-M4	csmim[w]4[_4] (3/4-terminal)	c3t_smim4, c3t_smimw4
1fF between M5-M4	cmim[w][_4] (3/4-terminal), cmim_2 (2-terminal)	c3t_mim, c3t_mimw
2.8fF between M4-M5	cmim[w]3[_4] (3/4-terminal), cmim3_2 (2-terminal)	c3t_mim3, c4t_mimw3
5.6fF stacked between M3-M5	csmim[w]6[_4] (3/4-terminal)	c3t_smim6, c4t_smimw6

MIM capacitors can be placed over Nwell (“w” in device name) or over Psubstrate. MIM capacitors over Nwell have an additional Nwell to P-substrate junction isolation between the bottom plate and P-substrate which is included in the model. For devices over Psubstrate, the 3rd terminal is the Psubstrate.

In select SBC18 technologies four terminal devices (“_4” suffix) are available and should be used for devices over Nwell where the 4th terminal is the Psubstrate. In legacy design kits or in cells without the “_4” suffix, when a device is placed over Nwell, the 3rd terminal is the Nwell and the Psubstrate is hard wired to SPICE node “0”.

Table 12.2 provides a description of the terminal connections. In order to obtain better isolation between the MIM capacitors over Nwell and nearby devices, it is recommended to tie the Nwell to AC ground (VDD for example). Figure 12.1 illustrates a cross section of a SBC18PT stacked MIM capacitor and base MIM capacitor. Please note that this cross section is specific to SBC18PT, other SBC18 variants will have different cross sections that are not illustrated in this manual.

FIGURE 12.1 SBC18PT Single and Stacked MIM Capacitor cross section**TABLE 12.2** NWELL and SUB Terminals

Terminals	OVER NWELL?	SUB Terminal	NWELL Terminal
3	NO	3rd terminal	none
3	YES	No terminal, SUB hard coded to SPICE node 0 in model	3rd terminal
4	YES	4th terminal	3rd terminal

12.1.2 Model Description

Figure 12.2 through Figure 12.5 show the sub circuits used to model the MiM and stacked MiM devices respectively. Please refer to Table 12.3 for sub circuit component names and physical descriptions. The model includes all elements within the dashed box shown in Figure 12.1 including metal and via parasitics. The bottom plate access is not included in the model since it's placement is controlled by the pcell with various options available. The model assumes one sided bottom and top plate routing which is a worst case scenario. Accurate simulations of the bottom plate access are achieved through post-extraction (Calibre PEX) simulation. See [Appendix A for more information on layout parasitics](#). The device over Nwell model includes the Nwell/psub diode. All models scale with MiM length (L) and width (W).

FIGURE 12.2 Sub-circuit and component description of a MIM capacitor over Nwell

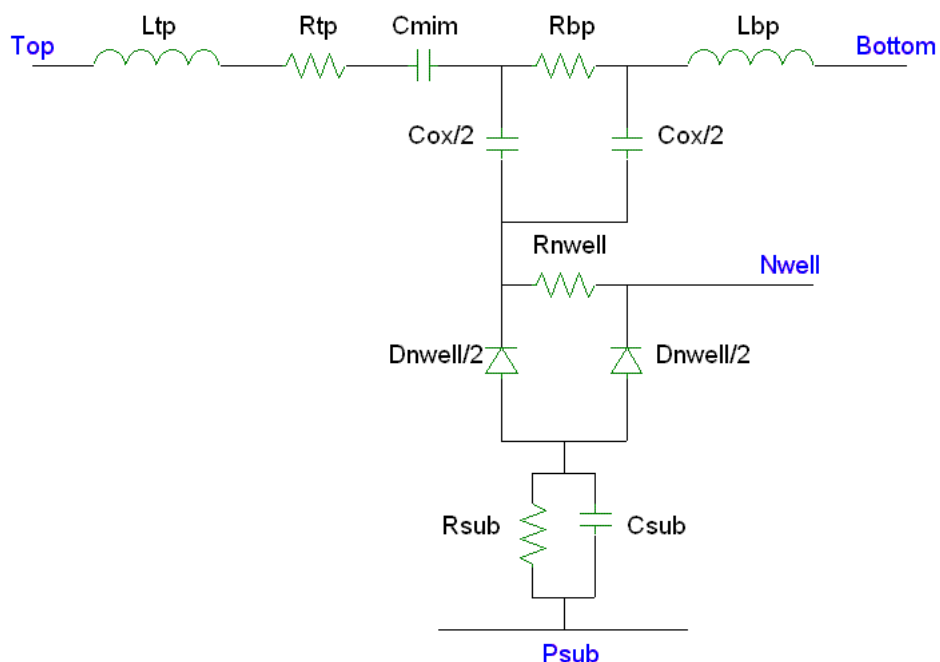


FIGURE 12.3 Sub-circuit and component description of a MIM capacitor over P substrate.

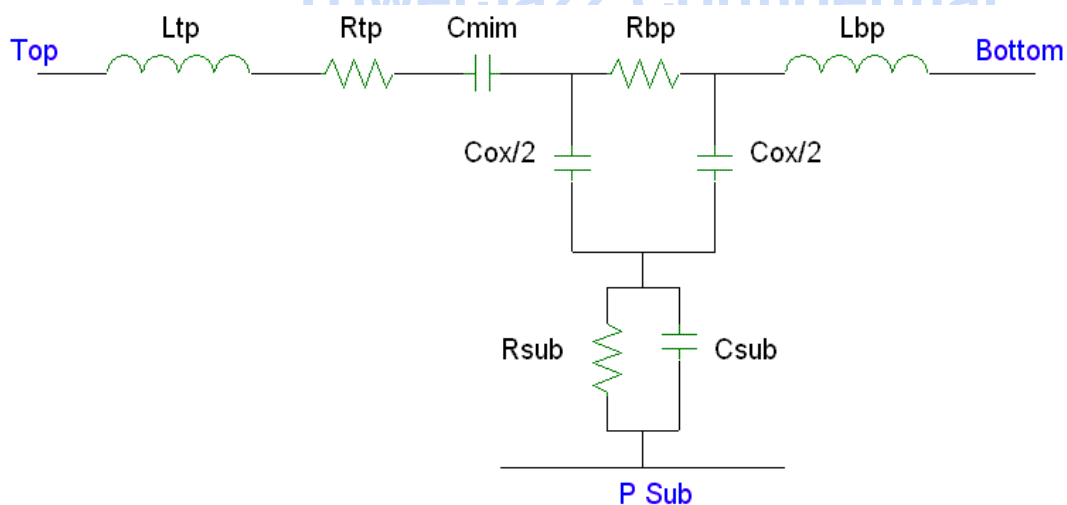


FIGURE 12.4 Sub-circuit and component description of a Stacked MIM capacitor over Nwell.

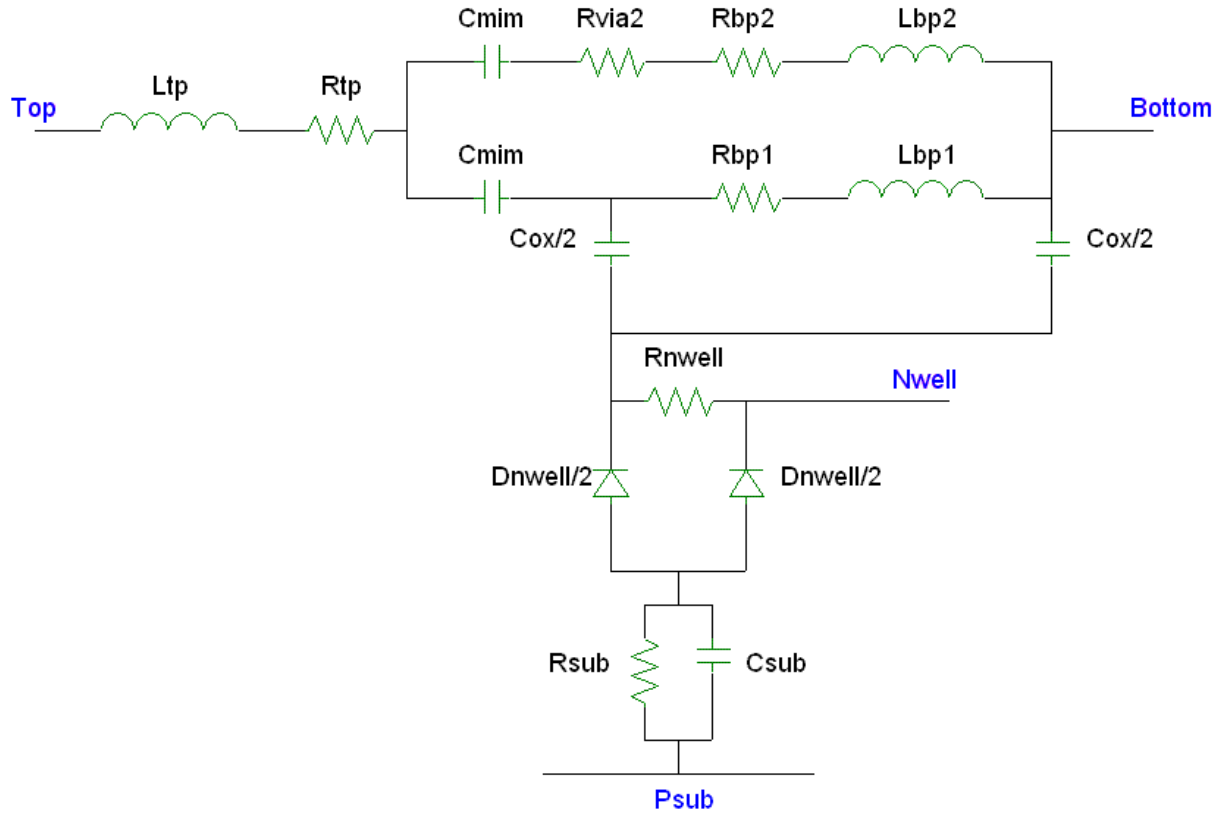


FIGURE 12.5 Sub-circuit and component description of a Stacked MIM capacitor over P substrate.

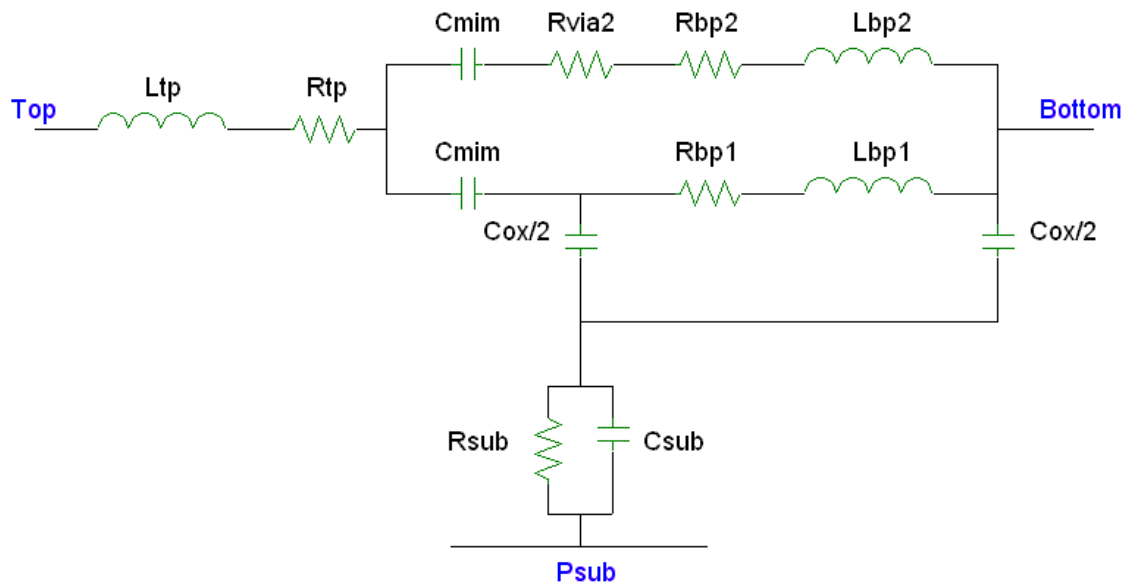


TABLE 12.3 Capacitor Model Sub-circuit component names

Circuit Components		Characterization Method
cmim	MIM Capacitance	Verified by low frequency s-parameters
Ltp	Top Plate Inductance	Calculated by Greenhouse equation, verified by SRF characteristics from high frequency s-parameters
Rtp	Top Plate Metal and VIA Resistance	Calculated directly from geometry and sheet p
Rbp	Bottom Plate Resistance	Calculated directly from geometry and sheet p
Lbp	Bottom Plate Inductance	Calculated by Greenhouse equation, verified by SRF characteristics of Ceff data
Cox	Oxide Capacitance	Calculated directly from ESPEC
RNwell	Nwell Resistance	Calculated directly from ESPEC
DNwell	Nwell to P Sub junction diode	Calculated directly from ESPEC
Csub	Substrate Capacitance	Estimated
Rsub	Substrate Resistance	Estimated
Rvia	Via Resistance	Calculated directly from ESPEC

12.1.3 Model Verification

RF measurements are performed on various MiM capacitors. As MiM caps have very small resistance (on the order of a few hundred milliohms and smaller), accurate measurements of the device resistance are difficult. Contact resistance de-embedding errors and repeatability are the limiting factors. Short and thru line de-embedding methods will not yield the true device resistance. Thru line de-embedding is applied in order to eliminate the feed line inductance and capacitance and verify the capacitor self-resonance. Effective capacitance plots are shown for several geometries of 1fF and 2fF and devices in Figure 12.6 and Figure 12.7 respectively. RF characterization data for the 2.8fF MiM and 4fF and 5.6fF stacked MiM capacitors is not available for SBC18 presently. The effective capacitance increases at higher frequencies due to the inductance of the metal plates, eventually approaching a self-resonance. Larger capacitors show this effect at lower frequencies since the large capacitance equates to lower resonance frequency. The MiM capacitors give very high Q due to the low resistive losses of the metal plates and vias. As parasitics of the metal connections to the MiMs in layout will significantly reduce the Q, post layout parasitic extraction simulation is crucial for accurate Q simulation. Figure 12.8 shows a comparison of the 3 MiM densities as a function of device area.

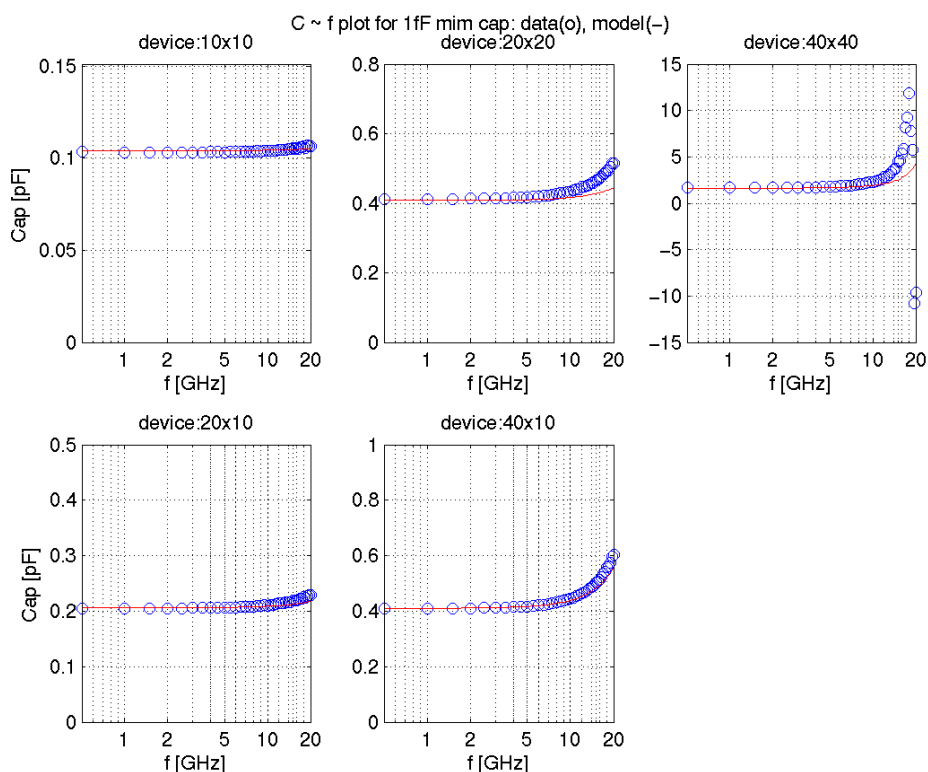
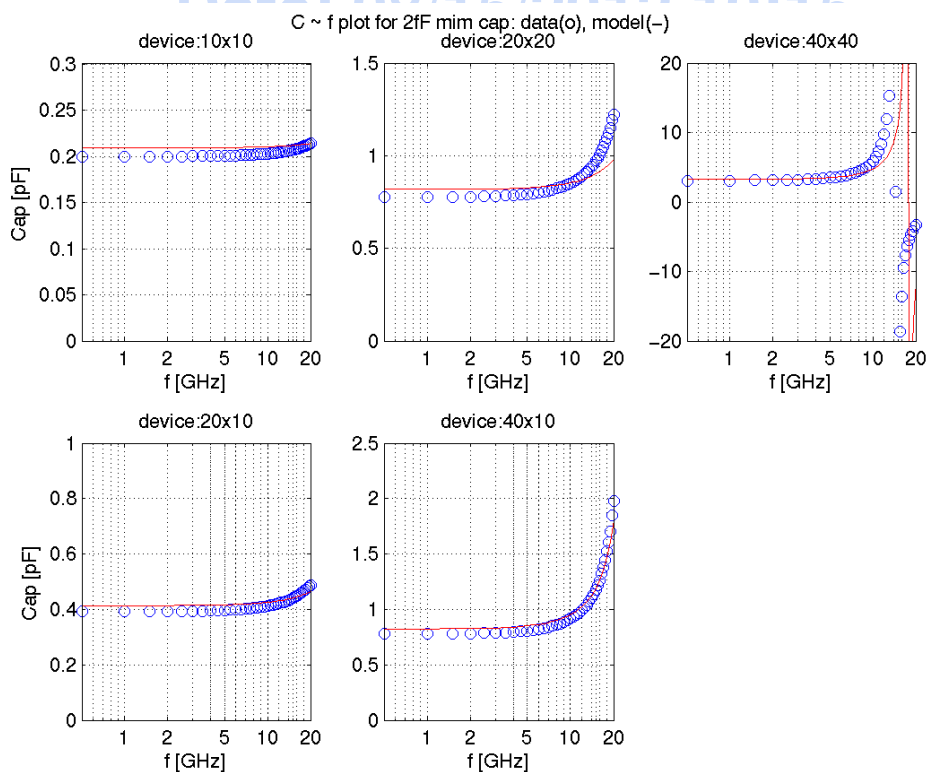
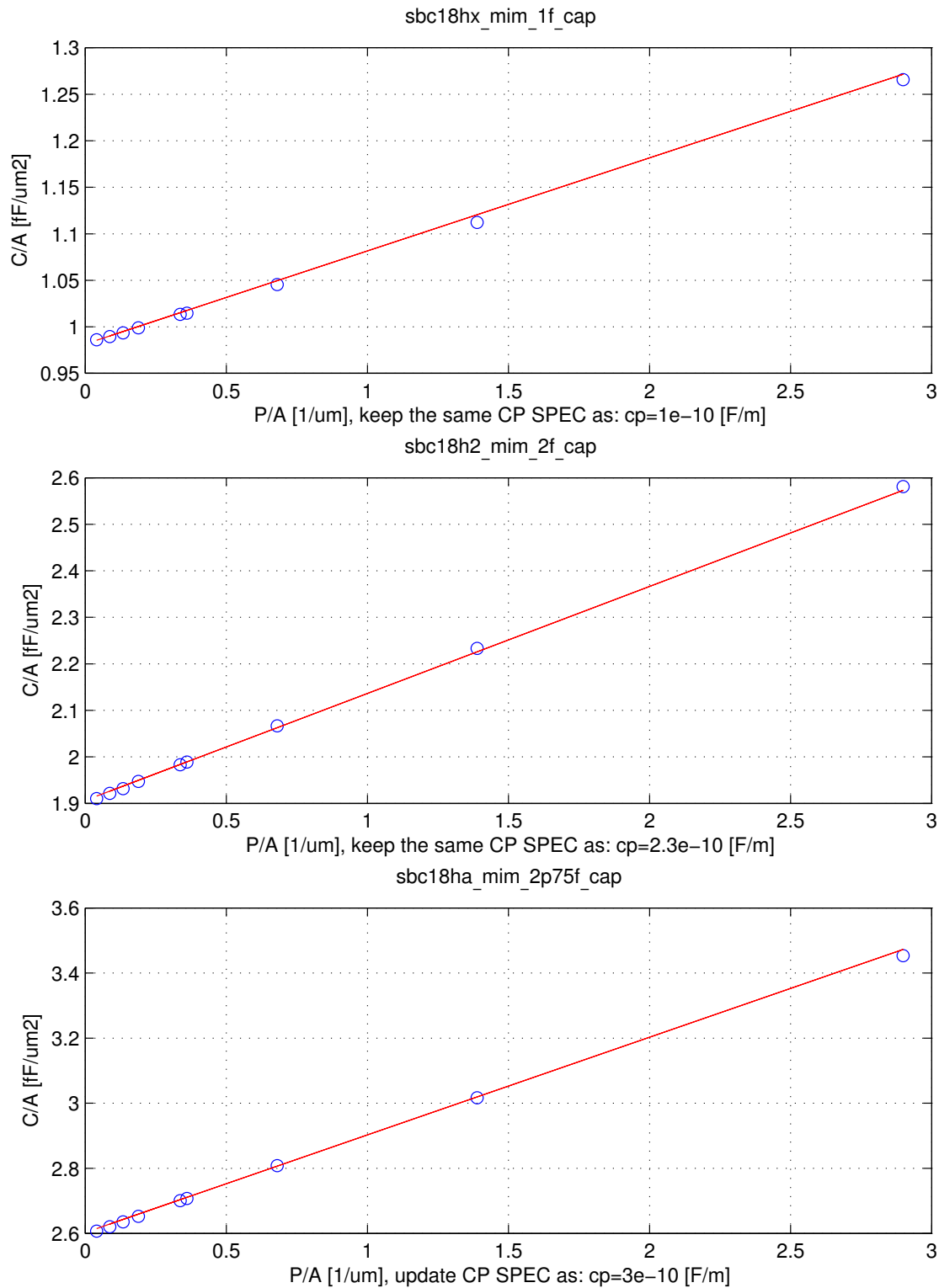
FIGURE 12.6 $1\text{fF}/\mu\text{m}^2$ MIM capacitance characteristicsFIGURE 12.7 $2\text{fF}/\mu\text{m}^2$ MIM capacitance characteristics

FIGURE 12.8 Comparison between MIM capacitor model and measured data



12.1.4 Corner Models

12.1.5 MiM Statistical and Corner Models

The MiM statistical and corner models account for process variation of the MiM oxide thickness, metal thickness (sheet resistivity), and ILD thickness derived directly from the process ESPECs. The MiM model parameters are directly correlated with the process parameters. See Section 15.0 for further explanation of the device interdependencies in the corner models and use of the X-Sigma corner models. Table 12.4 lists the MiM specific ESPECs compared to simulated corner and statistical values for three MiM capacitor devices.

TABLE 12.4 ESPEC, Corner and Statistical Model Comparison for MiM Capacitor Model

Device	name	units	slow			nomi			fast		
			Espec	Corner	Stat	Espec	Corner	Stat	Espec	Corner	Stat
c3t_mim	ca	fF/um2	1.15	1.15	1.16	1	1	1	0.85	0.85	0.85
	cp	fF/um	0.13	0.13	0.13	0.1	0.1	0.1	0.07	0.07	0.07
	tc	ppm/v		36	36	36	36	36		36	36
c3t_mim2	ca	fF/um2	2.3	2.3	2.32	2	2	2	1.7	1.7	1.69
	cp	fF/um	0.35	0.34	0.34	0.23	0.23	0.23	0.12	0.12	0.12
	tc	ppm/v		20	20	20	20	20		20	20
c3t_smim4	ca	fF/um2	4.6	4.6	4.62	4	4	4.0	3.4	3.4	3.39
	cp	fF/um	0.8	0.8	0.8	0.6	0.6	0.6	0.4	0.4	0.4
	tc	ppm/v		20	20	20	20	20		20	20

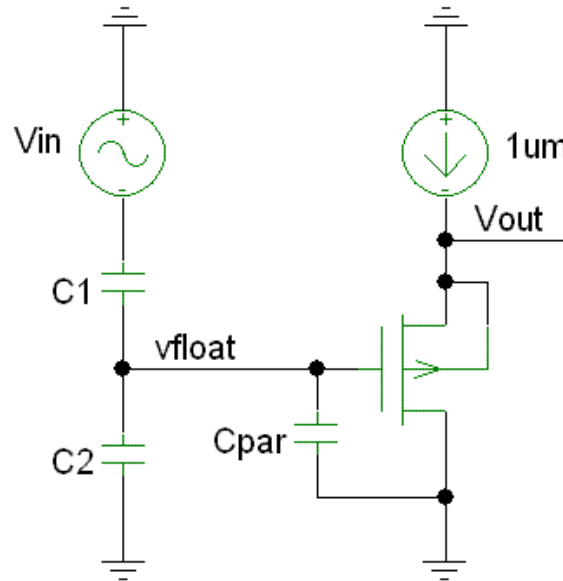
12.1.6 MiM Mismatch Models

12.1.6.1 Mismatch Measurements

A detailed description of MiM mismatch characterization methodology and results are available in the Jazz Semiconductor document NPB PS-0392 titled “Analog Characterization Report for SBC18.” The basic set-up is a voltage divider circuit as shown in Figure 12.9. By reversing the terminals of the capacitor pairs, the mismatch can be calculated independent of the circuit parasitics, given by

$$\frac{\Delta C}{C} = 2 \cdot \left(\frac{C1 - C2}{C1 + C2} \right) \quad (\text{EQ 1})$$

FIGURE 12.9 MiM Mismatch Measurement Schematic



12.1.6.2 MiM Mismatch Modeling

The MiM mismatch included in the design kit takes into account area and perimeter capacitance mismatch variations. Mismatch due to spacing variation is not included in the model. The mismatch models for area and perimeter effects are given by

$$CA_{mm} = CA_{nom}(1 - \sigma_A[LW]^{\delta_A}) \quad (\text{EQ 2})$$

$$CP_{mm} = CP_{nom}(1 - \sigma_P[LW]^{\delta_P}) \quad (\text{EQ 3})$$

where σ_A , σ_P , δ_A , and δ_P are the area and perimeter coefficients and exponents extracted via a nonlinear least squares global optimization method to best fit the measured data.

12.1.6.3 Mismatch Model Usage Guidelines

The mismatch model is available in Spectre, which provides the necessary framework to model the local mismatch between capacitors. It is implemented inside the “sub-circuit” definition of the MiMs allowing for “instance to instance” variations in the process parameters. The “variations” variable inside Spectre should be set equal to “mismatch.” Typically, ~100 monte-carlo runs are sufficient to accurately simulate the local-mismatch between the MiMs. The user should, however, increase the “numruns” variable inside Spectre until the improvement in the simulated results is small.

12.1.6.4 Mismatch Model Verification

Figure 12.10 through Figure 12.12 compare the mismatch model prediction of the measured data for the minimum spacing (4μm) 3-σ $\frac{\Delta C}{C}$ vs. capacitance value which is scaled through geometry variation. For smaller devices, the mismatch increases due to perimeter effect dominance. For larger devices, the mismatch increases due to area effect dominance. The model accurately predicts the trends and can be used to design for minimum mismatch between 2 capacitor pairs. More elaborate mismatch configurations such as common centroid are characterized in the SBC18 Analog Characterization report.

12.1.7 Model Update History

The following tables list the model updates with each revision. Unlisted model revisions indicate that no changes have occurred in that revision.

TABLE 12.5 MiM model specific updates in model release version 5.0

v5.0 update	Devices	Reason	Impact on user
All device resistances and inductances defined by pcell included in the model.	All	Improve pre-extraction simulation of C and Q of the MiM capacitors	Simulated capacitance will roll up due to self inductance at high frequencies. Model will now simulate all plate and via parasitics. The extraction decks will no longer add these elements.

TABLE 12.6 MiM model specific updates in model release version 6.0

v6.0 update	Devices	Reason	Impact on user
X-Sigma Corner Model Support	All	Allow for process variation settings different than conventional +/- 3 sigma-corner models	Added flexibility in corner simulation

FIGURE 12.10 1.0fF/ μm^2 MIM capacitor mismatch

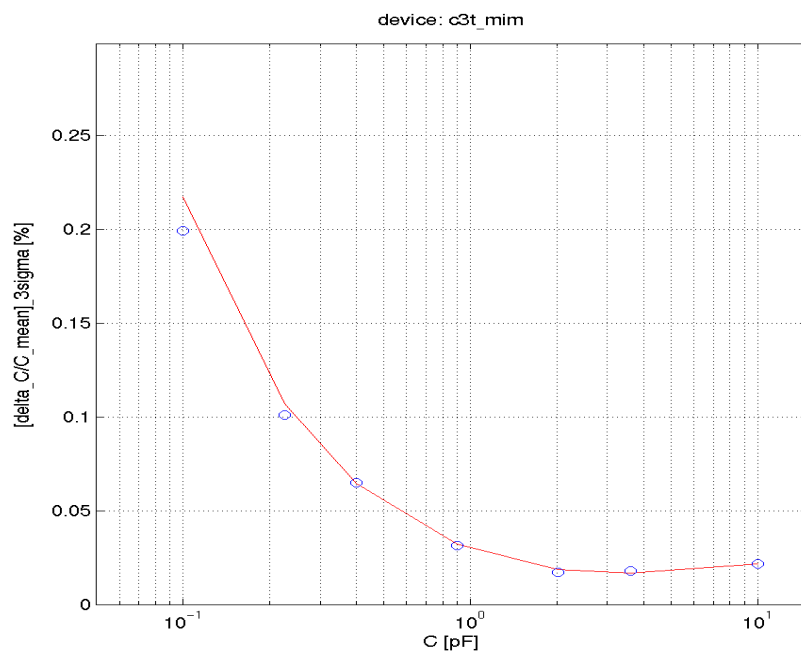


FIGURE 12.11 2.0fF/ μm^2 MIM capacitor mismatch

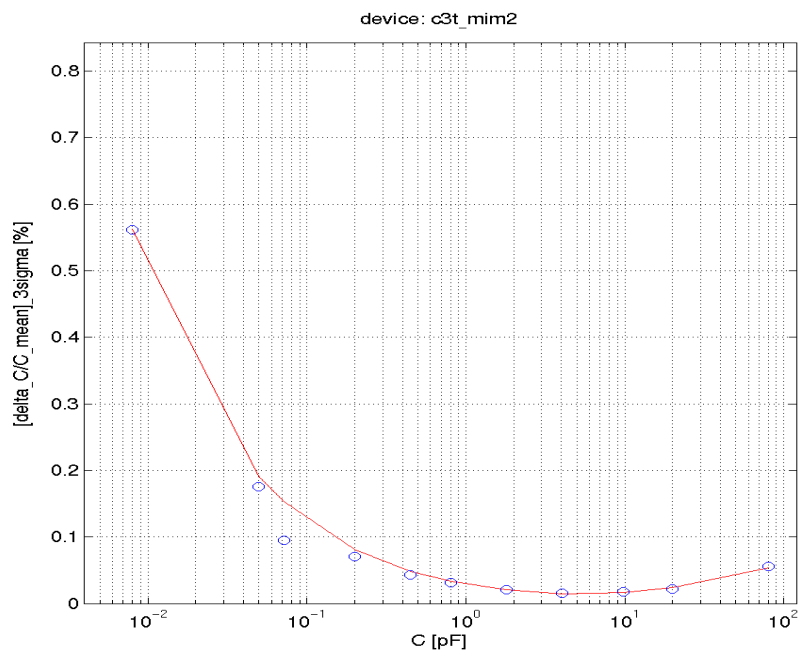
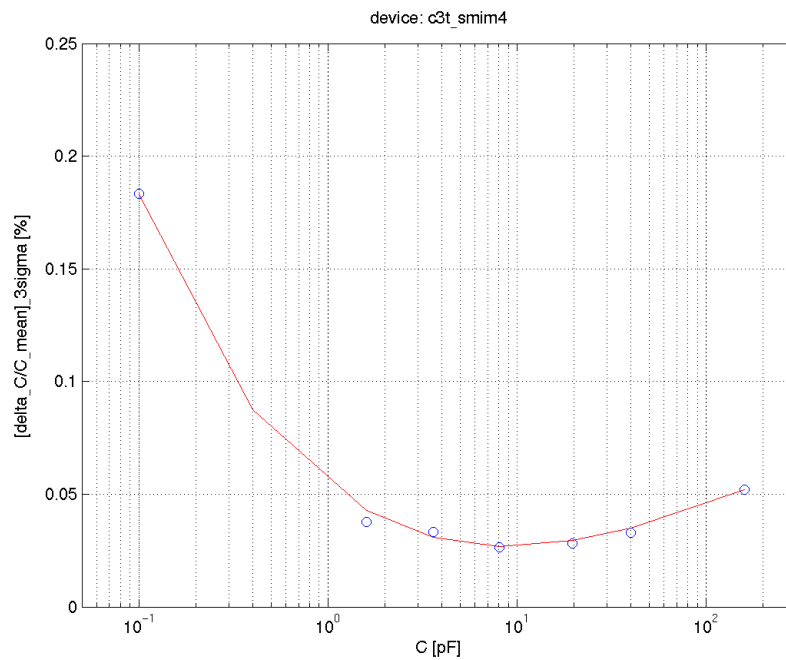


FIGURE 12.12 $4.0\text{fF}/\mu\text{m}^2$ MIM capacitor mismatch

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12.2 Poly Capacitor

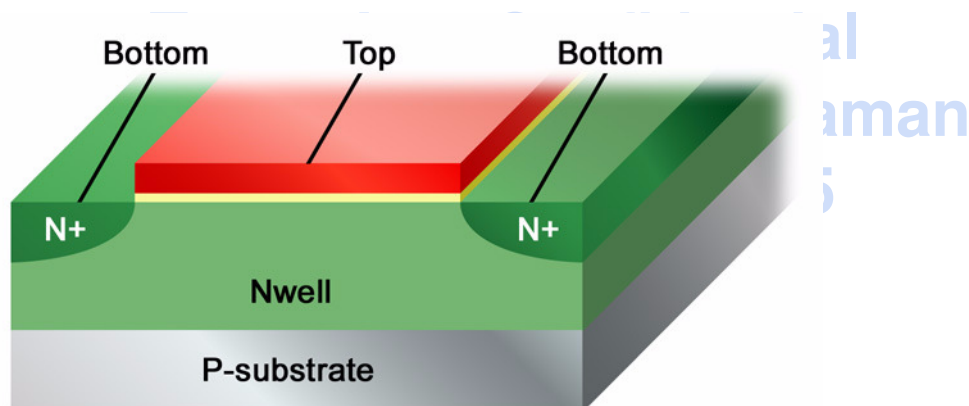
12.2.1 Device Description

TABLE 12.7 Poly-capacitor summary

Design Kit Name	Gate Oxide	Model Name
cpoly	1.8V	pc
cpoly3p3	3.3V	pc3p3
cpoly5p0	5V	pc5p0

Poly capacitors are formed by MOS structures with Nwell beneath the n+ poly gate and n+ Nwell contacts as shown in Figure 12.13. Without p+ source/drains, there is no source for inversion charge, resulting in depletion capacitance in inversion. Maximum capacitance is achieved in accumulation when the poly gate is positively biased with respect to the Nwell. The device is available in thin oxide (library name: **cpoly** or **pc**) and thick oxide (3.3 or 5V) (library name: **cpoly3p3** or **pc3p3** and **cpoly5p0**) versions. The **cpoly** device is exactly the same in cross section to the MOS varactor Section 10.3 on page 472. The difference between the **cpoly** device and the MOS Varactor is in layout and modeling.

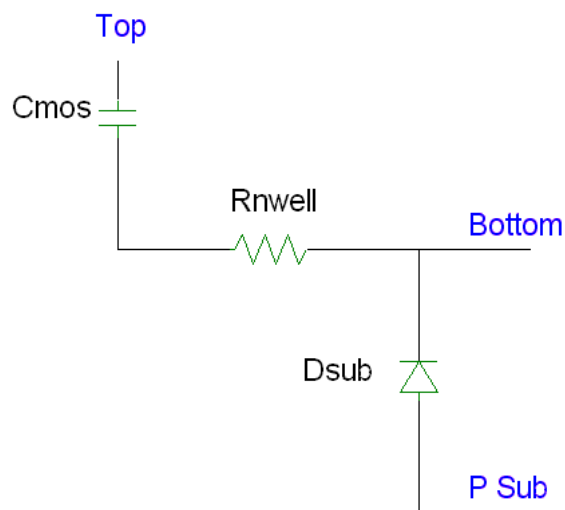
FIGURE 12.13 Poly Capacitor cross-section



12.2.2 Model Description

Figure 12.14 shows the sub circuit model for the **pc** device. The **pc** model consists of MOS capacitance (emulated through a BSIM element) in series with a Nwell resistance. The parasitic Nwell/Psub junction diode is also included. The Nwell resistance is estimated in order to give reasonable simulations of RC effects. **The pc or pc3p3 devices should not be used in varactor applications.** For varactor applications which require very accurate nonlinear capacitance and parasitic modeling over bias, frequency and geometry, the **varactor_mos** device should be used (see Chapter 5.2).

FIGURE 12.14 Poly Capacitor Sub-circuit description



12.2.3 Model Verification

Figures 12.15 through 12.18 show the measured and simulated CV data for **pc** and **pc3p3** devices. The models are extracted and validated over a wide range of geometries.

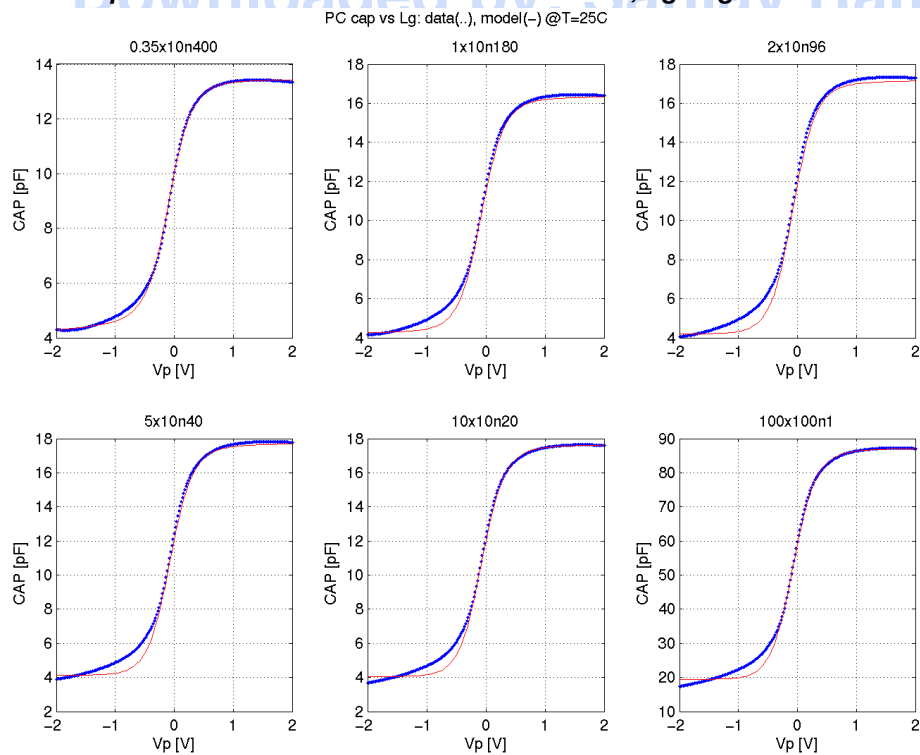
FIGURE 12.15 **pc** CV curve measurement vs. simulation, $L_g \times W_g \times N$ 

FIGURE 12.16 *pc* CV curve measurement vs. simulation, LgxWgxN

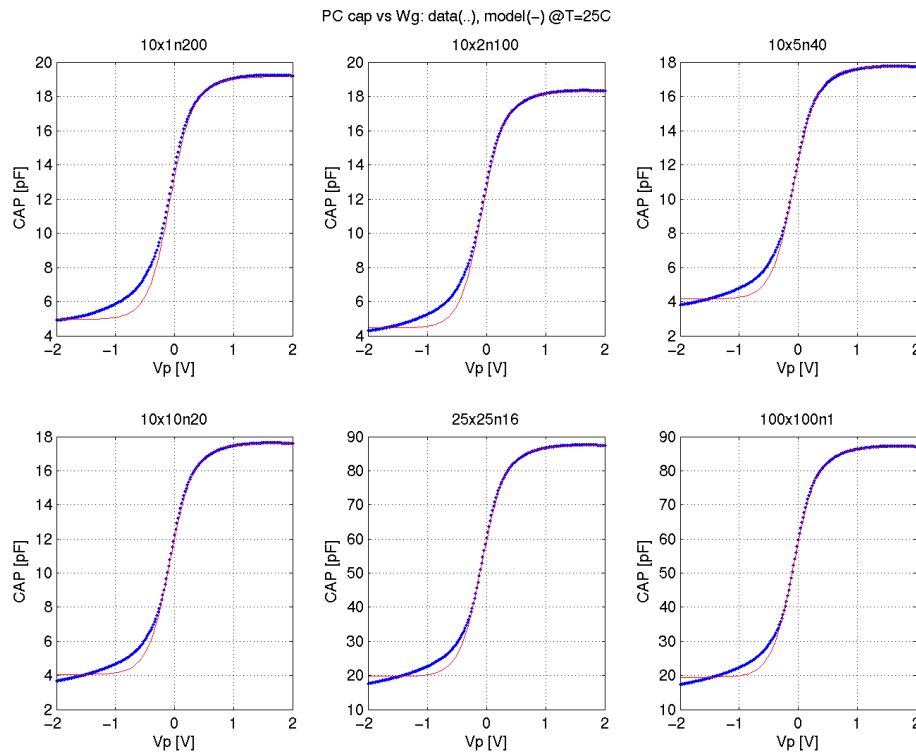


FIGURE 12.17 *pc3p3* CV curve measurement vs. simulation, LgxWgxN

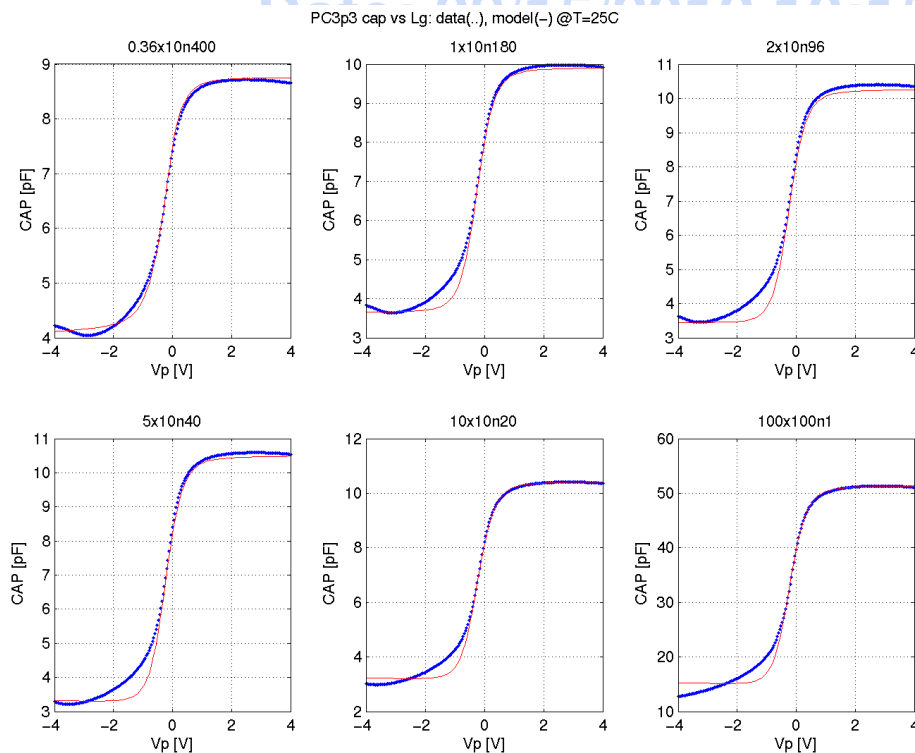
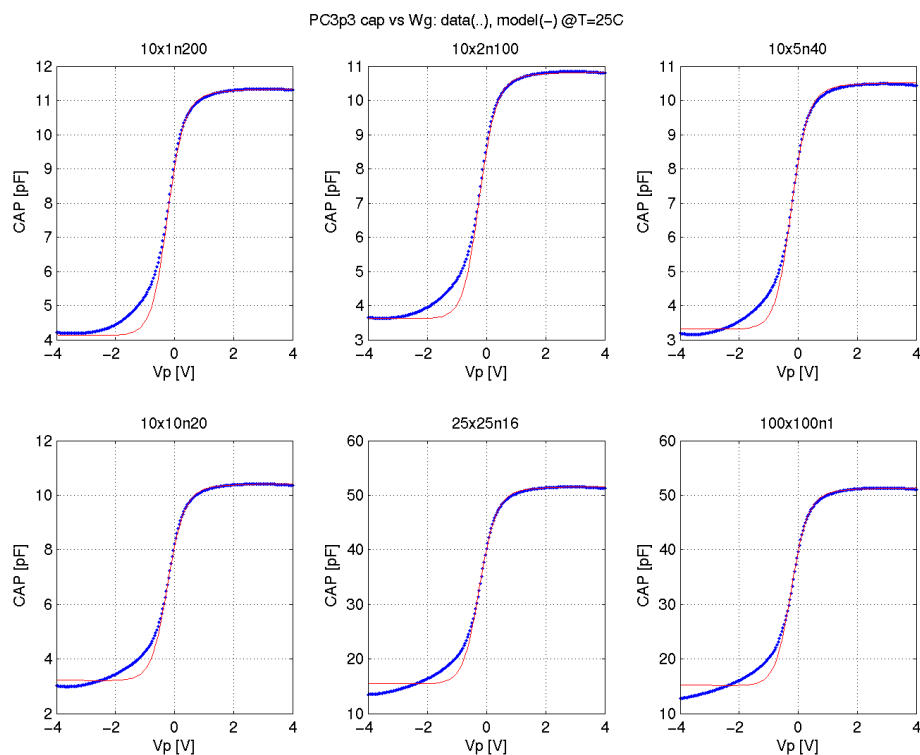


FIGURE 12.18 *pc3p3* CV curve measurement vs. simulation, LgxWgxN

12.2.4 Poly Capacitor Statistical and Corner Models

The statistical and corner models for the **pc** devices are correlated directly with the MOSFETs. See Section 15.0 for further explanation of the device interdependencies in the corner models and use of the X-Sigma corner models.

12.2.5 Poly Capacitor MisMatch Models

Mismatch models for **pc** and **pc3p3** are not supported.

12.2.6 Poly Capacitor Model Update History

TABLE 12.8 Poly Capacitor model specific updates in model release version 6.0

Update	Devices	Reason	Impact on user
v6.0			
Re-extraction of the model to include full geometry ranges	All	Previous models based on large plate, causing inaccuracies for dimensions below 2 μ m	Increased accuracy over entire design space
X-Sigma Corner Model Support	All	Allow for process variation settings different than conventional +/- 3 sigma corner models	Added flexibility in corner simulation
v6.2b			
Add voltage coefficient (vc1 & vc2) based on the Espec values	MiM caps	New capability in the models	Bias dependence of capacitance
v6.4			
Added 2-terminal MiM cap	MiM caps	New capability to allow fast simulation (without 3rd terminal and inductive parasitics) at low frequencies where coupling to bulk is not important.	Allows user to include effect of adjoining metal routing coupling to MiM capacitor

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13.0 Diode Models

13.1 Junction Diode Model

13.1.1 Device description

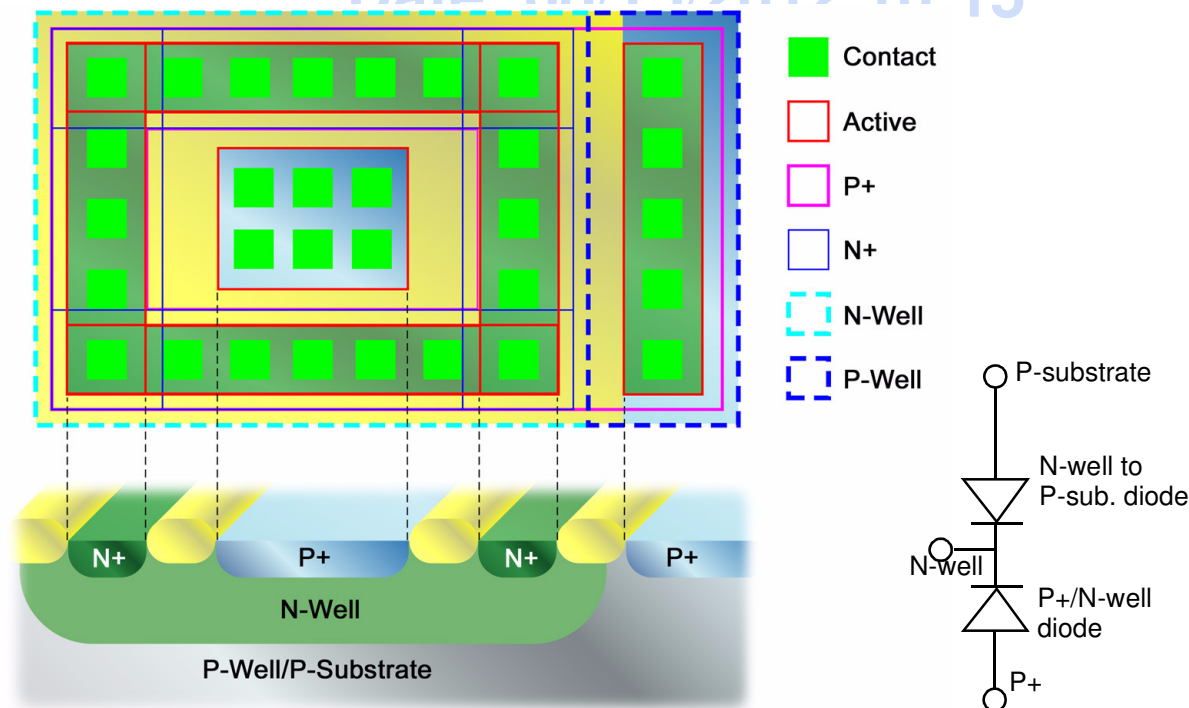
Four diodes are offered in the sbc18 process. These are summarized in Table 13.1

TABLE 13.1 Summary of junction diode models

Design Kit Name	Model Name	Cathode	Anode	Characterized Bias Range (Forward Bias/Reverse Bias) (V)	Characterize Temperature Range (°C)
dn or ndiode	ndiode	N+/1.8v NLDD	P-well	0.7/2	-40-125
dp or pdiode	pdiode	N-well	P+/1.8v PLDD	0.7/2	-40-125
dn3p3 or n3p3diode	n3p3diode	N+/3.3v NLDD	P-well	0.7/3.3	-40-125
dp3p3 or p3p3diode	p3p3diode	N-well	P+/3.3v PLDD	0.7/3.3	-40-125
dnwell or nwdiode	nwdiode	nwell	psub		
ddnw	dnw_psub	Deep nwell	p-sub		
diso	dnw_pwell	Deep nwell	isolated pwell		

Some versions of the design kit also offers 3-terminal extensions to the pdiode (pdiod_3t) and p3p3diode (p3p3diode_3t) by including the n-well to p-sub diode (nwdiode) as shown in Figure 13.1, which also shows the layout and cross-section of a typical p+/n-well diode.

FIGURE 13.1 p+/n-well diode layout and cross-section



13.1.2 Model Description and Verification

Spice based diode models are extracted from two different structures. The first is an area intensive structure with $W \times L = 250\mu\text{m} \times 250\mu\text{m}$. The second structure is a perimeter intensive structure with 99 fingers of $W \times L = 1.6\mu\text{m} \times 250\mu\text{m}$. The capacitances were measured via a CV meter @ 100 KHz for reverse biases ranging from 0 to 1.8v for the low-voltage diodes, and from 0 to 3.5v for the high-voltage diodes. The area and perimeter capacitance densities and their bias dependencies were extracted simultaneously from measurements of the two test structures described above. The junction capacitance model is valid for reverse biases from 0 to 1.8v for the low voltage diodes and from 0 to 3.5v for the high voltage diodes, at room temperature. Default temperature coefficients in the diode model allow usage of the model at temperatures ranging from -40 to 125C. The measurements at room temperature along with model playbacks are plotted in Figures 13.2 through 13.5.

Similarly, the diode current as a function of reverse and forward bias was measured for the two flavors of diodes, allowing simultaneous extraction of saturation current densities for the bulk (area) and sidewall (perimeter) components for the forward bias. The junction leakage current for the reverse bias characteristics is not modeled. The dc current diode model is valid up to a 0.6v forward bias and at room temperature. Default temperature coefficients in the diode model allow usage of the model at temperatures ranging from -40 to 125C. The measurements along with model playbacks are shown in Figures 13.6 through 13.9.

13.1.3 Diode Statistical and Corner Models

The area and perimeter components of the capacitance are varied by to give 3- σ values of +/- 10% based on typical expected variation. The numbers have not been verified through process monitoring or electrical data of ring oscillators. The SBC18 ESPEC Document, NPB PS-0267 lists a 20% variation for area components. The junction current is not varied. The junction capacitances nor junction currents are monitored in the PCM.

FIGURE 13.2 Measured junction capacitance and model playbacks for ndiode

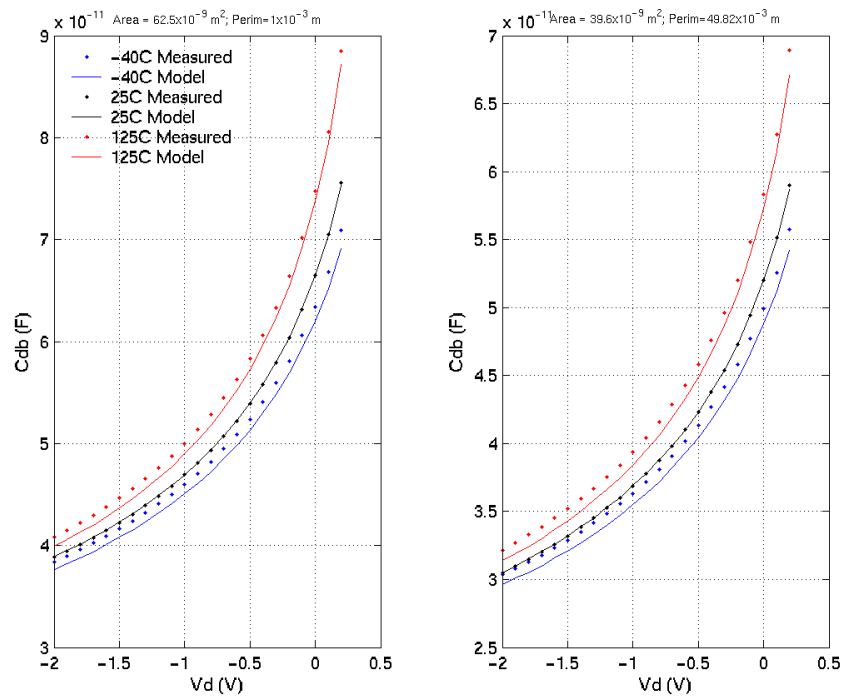


FIGURE 13.3 Measured junction capacitance and model playbacks for pdiode

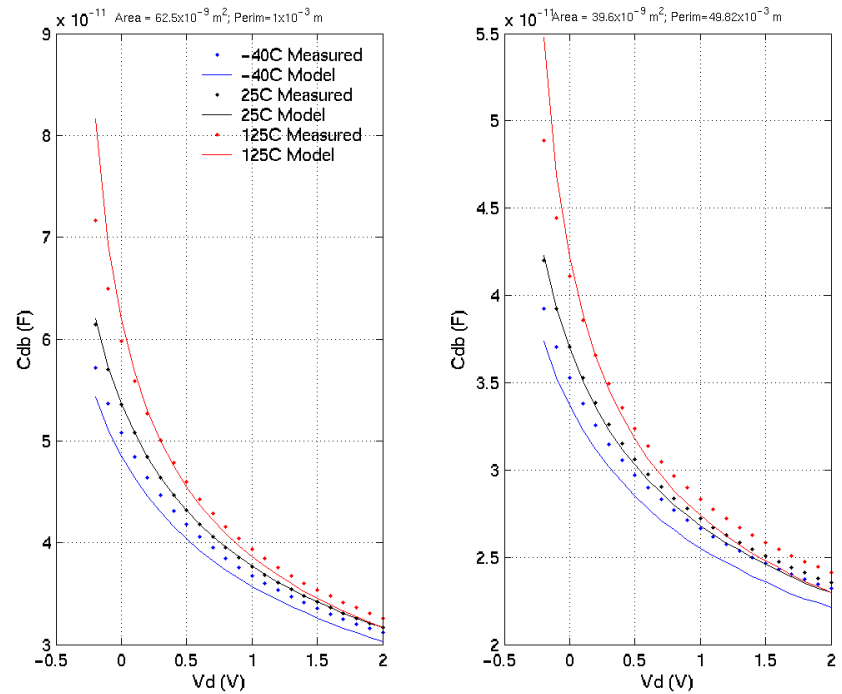


FIGURE 13.4 Measured junction capacitance and model playbacks for n3p3diode

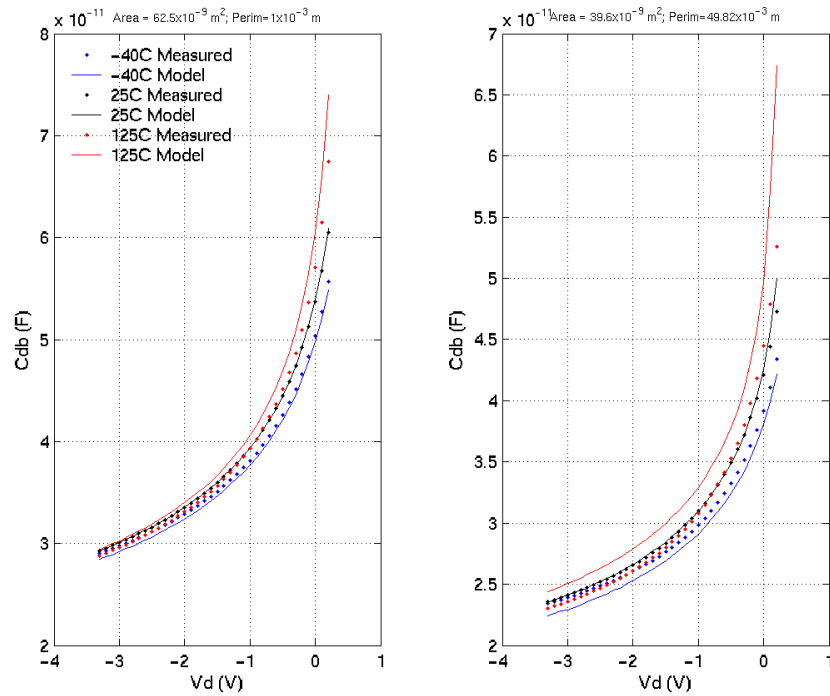


FIGURE 13.5 Measured junction capacitance and model playbacks for p3p3diode

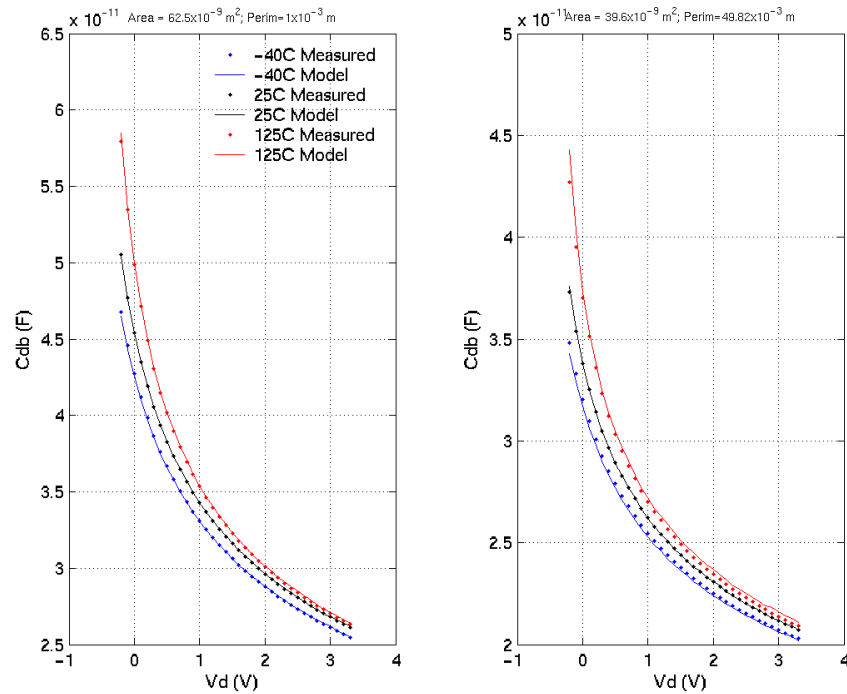


FIGURE 13.6 Measured junction diode current characteristics and model playbacks for ndiode

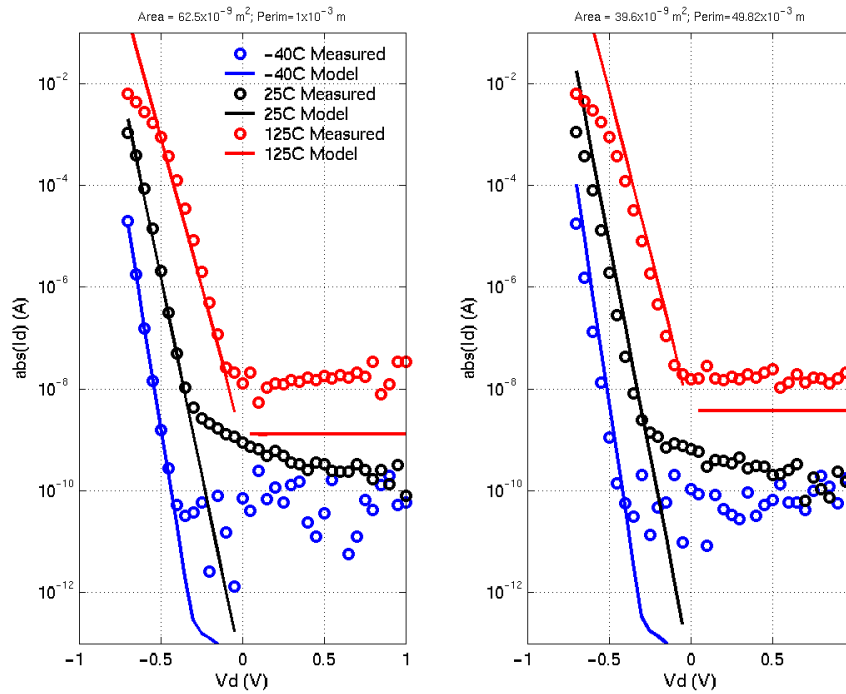


FIGURE 13.7 Measured junction diode current characteristics and model playbacks for pdiode

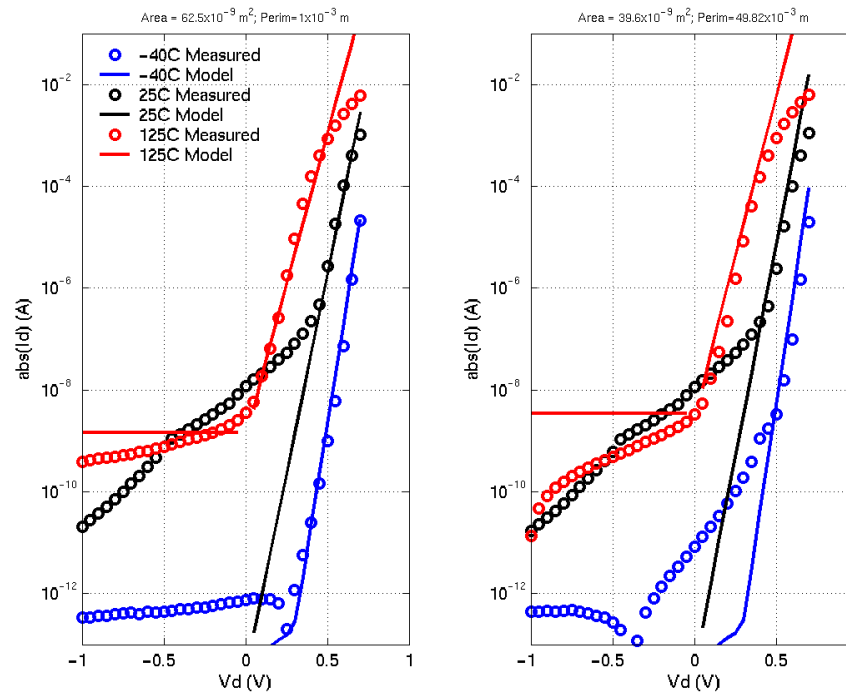


FIGURE 13.8 Measured junction diode current characteristics and model playbacks for n3p3diode

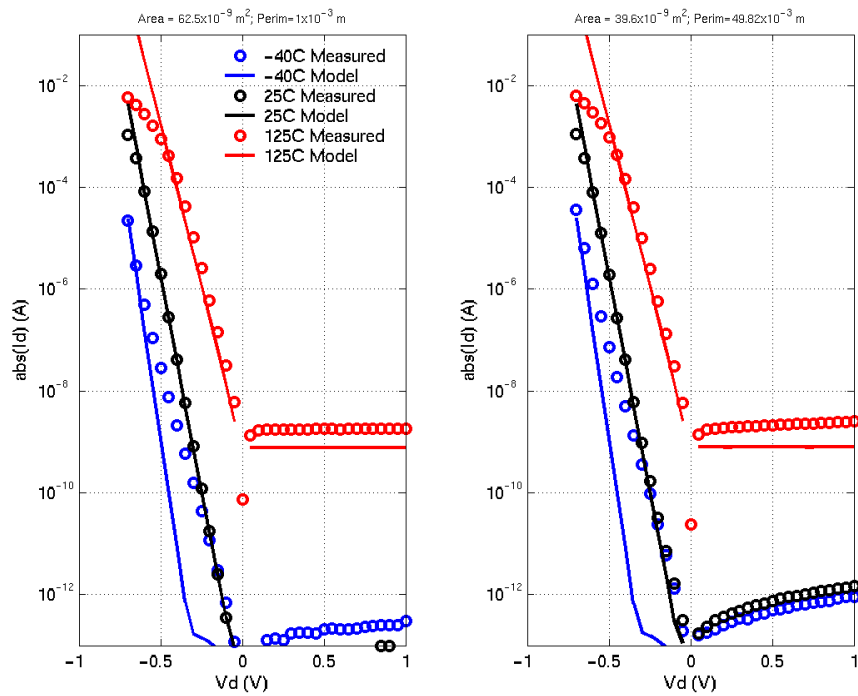
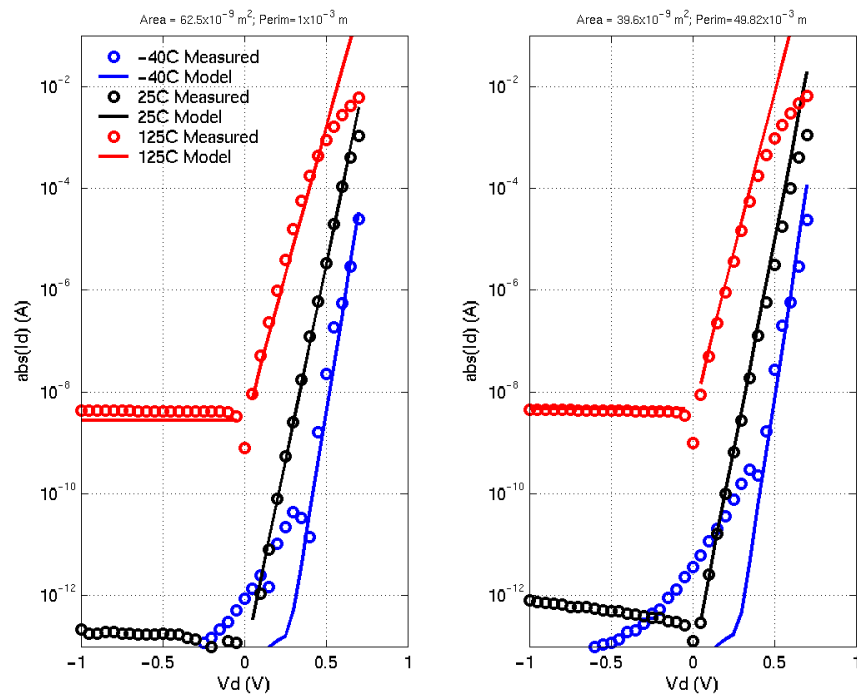


FIGURE 13.9 Measured junction diode current characteristics and model playbacks for p3p3diode



13.2 Schottky Diode

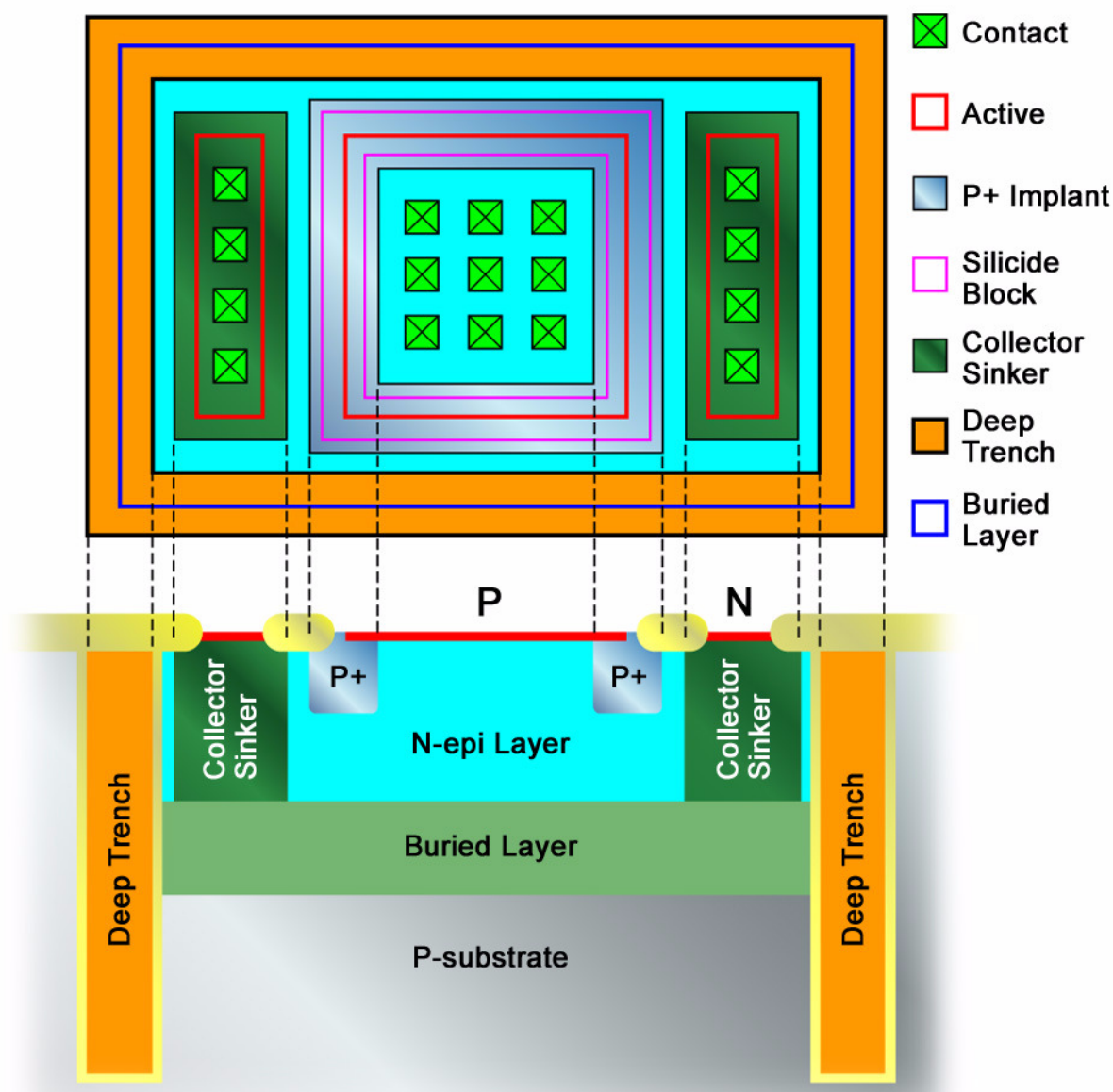
13.2.1 Device and model description

The SBC18 technology offers scalable Schottky diodes in the 2-5x2-5 μ m anode geometry range. In addition, fixed anode geometry diodes of 20x20 and 10x10 μ m are supported. The schottky diode is formed from the p+ silicide to n-epi junction. The device cross section and layout views are shown in Figure 13.10.

TABLE 13.2 Schottky Diode Summary

Design Kit Name	Scalable WxL (um)	Discrete WxL (um)
dschottky or d_schottky	2-5 x 2-5	10x10 and 20x20

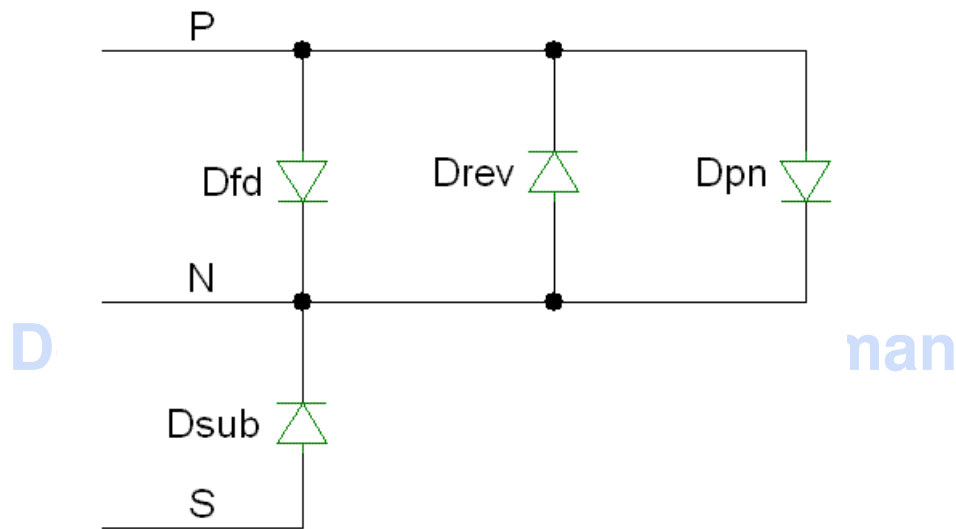
FIGURE 13.10 Schottky Diode Cross Section and Layout



13.2.2 Model Description

To capture all the parasitic components associated with the device, the model uses a four diode sub-circuit to improve the modeling accuracy shown in Figure 13.11. Due to the design of the device layout, a parasitic PN junction diode is present and is connected in parallel with the intrinsic Schottky diode. This PN junction diode could turn on if the forward bias voltage is above $\sim 0.6\text{V}$. If on, the diode affects the Schottky forward IV curve significantly at higher current ranges, especially for small device sizes (2x2 or 3x3). The measurement data (see figure 10.5) clearly shows this effect as the diode behaves more like a PN junction than a Schottky device starting at the mentioned $\sim 0.6\text{V}$. This parasitic PN junction diode has been added to the model and equivalent circuit in order to replicate the IV characteristics more accurately. In addition, please note that in the sub circuit below, Drev is not a physical device: it is used to model the Schottky diode reverse current only.

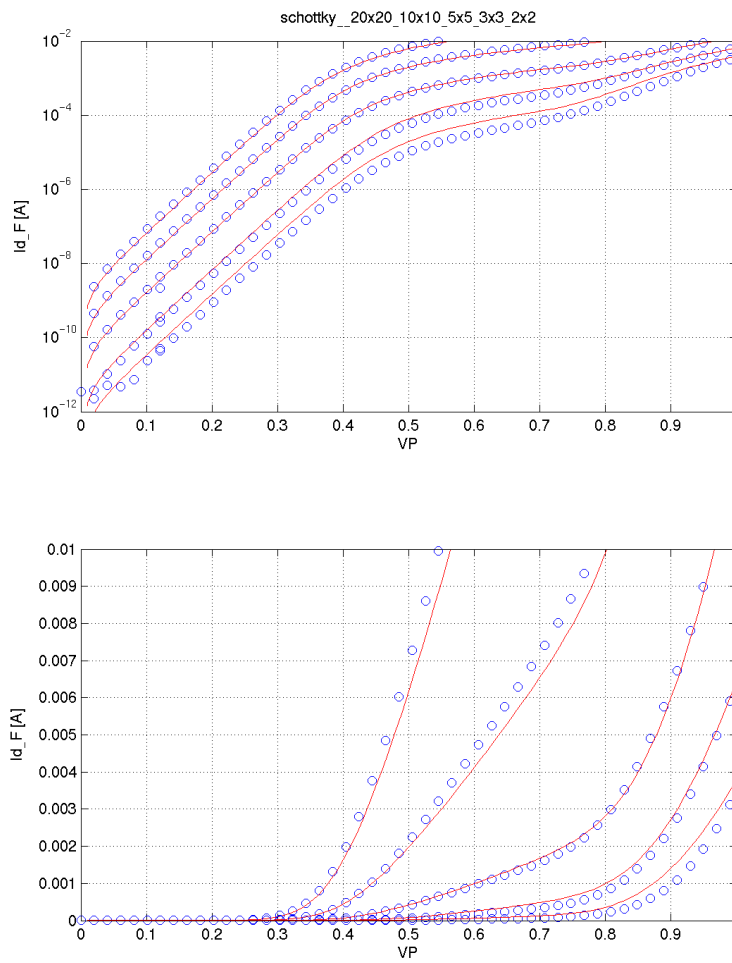
FIGURE 13.11 Schottky Diode Equivalent Circuit



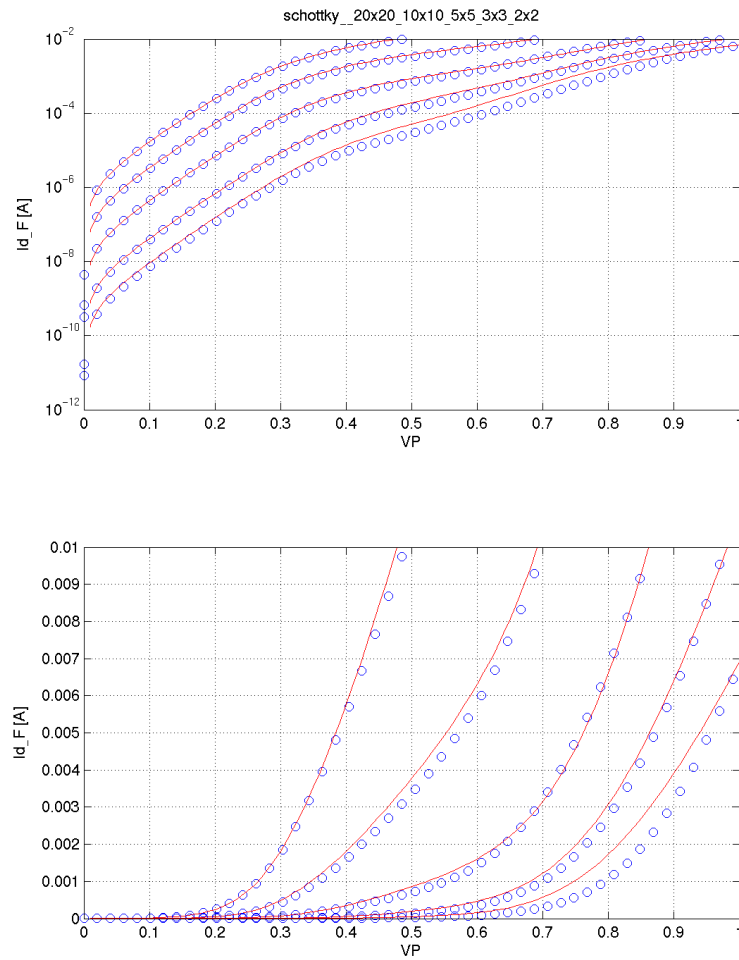
13.3 Model Verification Plots

Figure 13.12 and Figure 13.13 show the forward IV results at 25 and 125C respectively. Figure 13.13 and Figure 13.14 show the reverse IV results at 25 and 125C. Figure 13.15 displays the Y-parameter data for the 20x20 device at 1 GHz.

FIGURE 13.12 Schottky Diode IV curves at T=25C. Device Sizes: 20x20, 10x10, 5x5, 3x3, 2x2



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FIGURE 13.13 Schottky Diode IV curves at T=125C. Device Sizes: 20x20, 10x10, 5x5, 3x3, 2x2

an

FIGURE 13.14 Schottky Diode reverse IV curves at T=25C. Device Sizes: 20x20, 10x10, 5x5, 3x3, 2x2

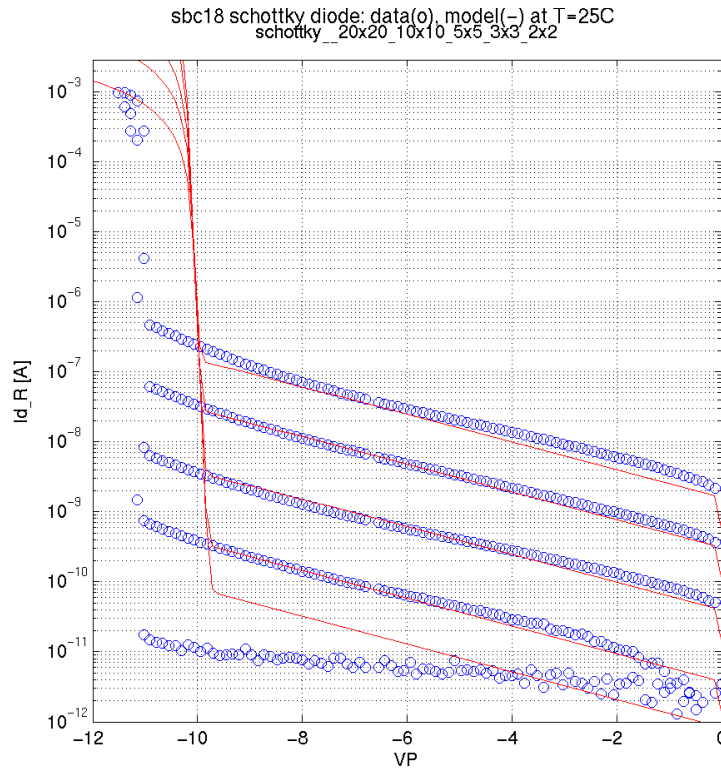


FIGURE 13.15 Schottky Diode reverse IV curves at T=125C. Device Sizes: 20x20, 10x10, 5x5, 3x3, 2x2

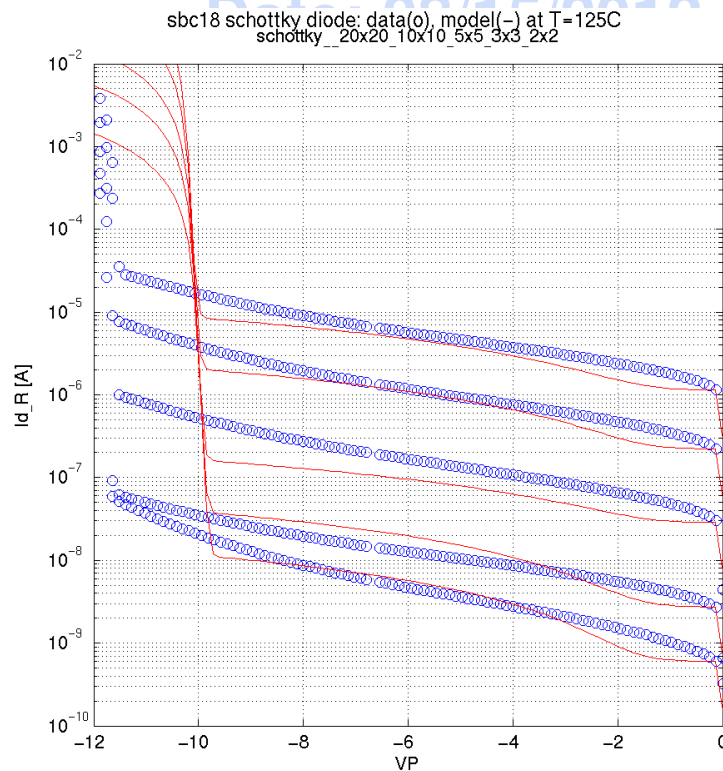
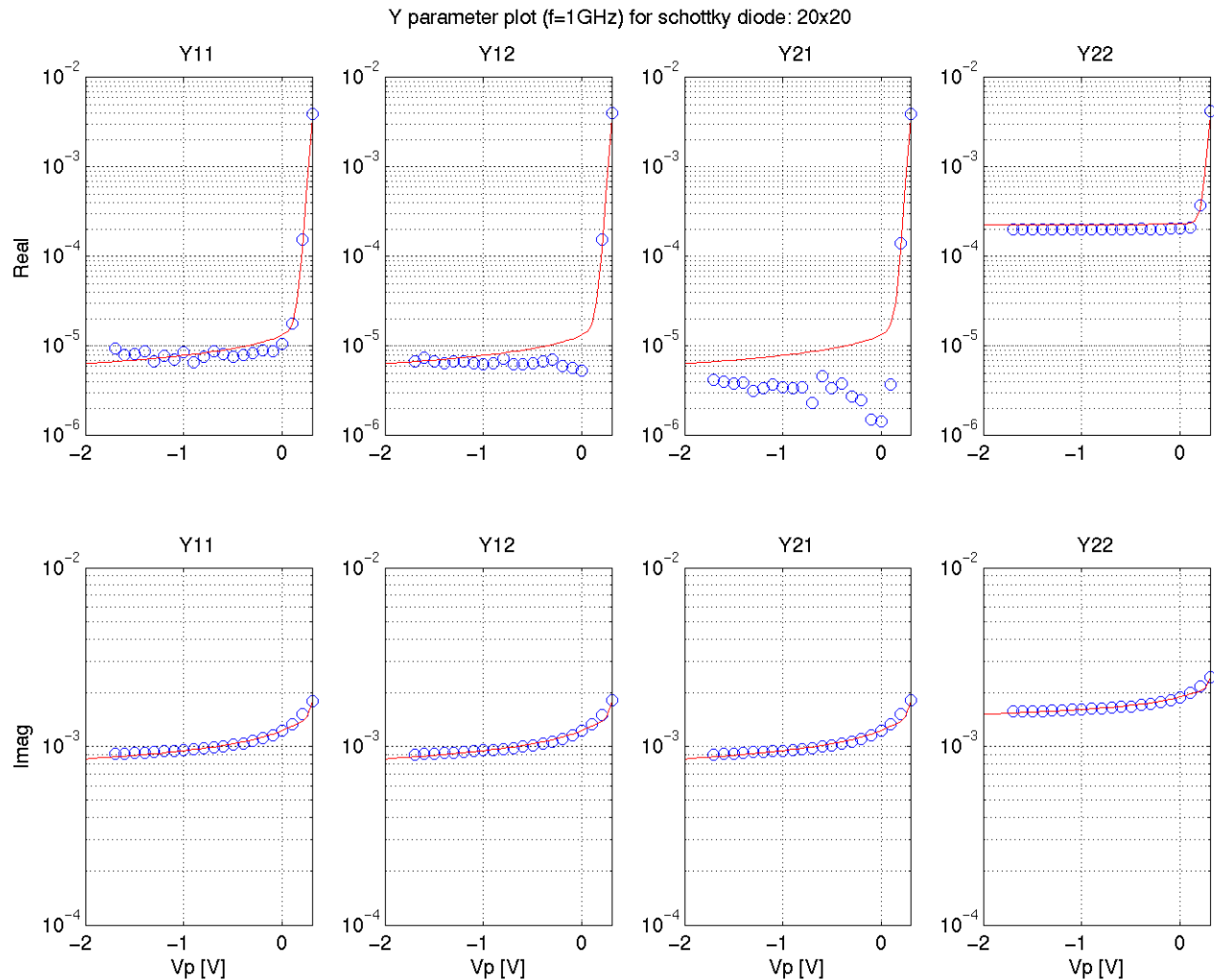


FIGURE 13.16 20x 20 Schottky diode Y-parameters

13.3.1 Schottky Diode Statistical and Corner Models

The schottky diode performance is largely controlled by the silicide resistance and the epi doping. Table 13.3 lists the ESPEC values compared to simulated corner and statistical values for the schottky diode device ($5 \times 5 \mu\text{m}^2$).

TABLE 13.3 Espec, Corner and Statistical model comparison for schottky diode

Parameter [$5 \times 5 \mu\text{m}^2$]	units	slow			nomi			fast		
		Espec	Corner	Stat	Espec	Corner	Stat	Espec	Corner	Stat
Von (Id=0.1mA)	V	0.48	0.48	0.45	0.42	0.42	0.42	0.36	0.36	0.38
Csd (V=0V)	fF/ μm^2	18	18	18.1	16.5	16.5	16.6	15	15	15.1
Rsd (V=0V)	ohm		120	121	100	100	100		81	80
Ir (Vr=3.3V)	nA							1.0	1.0	

13.4 Diode Model Update History

TABLE 13.4 Diode model specific updates in model release version 4.9

v4.9 update	Devices	Reason	Impact on user
Change forward biased diode IV model parameters	All 1.8v and 3.3v FETs and diodes	Corrected un-physical diode ideality factors	Better prediction of forward biased current. Possible improvement in convergence in some simulations

TABLE 13.5 Diode model specific updates in model release version 6.0

v6.0 update	Devices	Reason	Impact on user
X-Sigma Corner Model Support	All	Allow for process variation settings different than conventional +/- 3 sigma-corner models	Added flexibility in corner simulation

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14.0 High Frequency

14.1 High Frequency De-embedding Techniques

The SBC18 models are typically validated up to 10-20GHz, and conventional open-short de-embedding techniques are sufficient at these frequencies. For SBC18 designs operating at 50GHz and beyond model validation at frequencies > 20GHz is needed. To measure fet and bipolar data at these frequencies a 4-step de-embedding technique is used.

FIGURE 14.1 Impedance model for grounded-shielded test structure

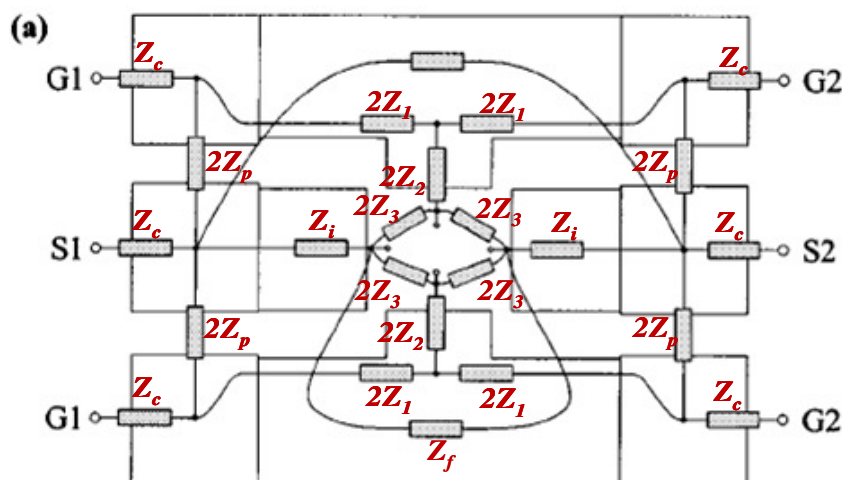
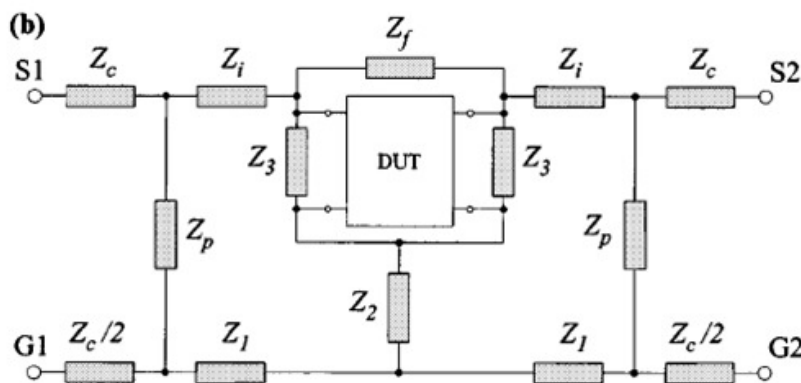


FIGURE 14.2 Equivalent impedance model for grounded-shielded test structure

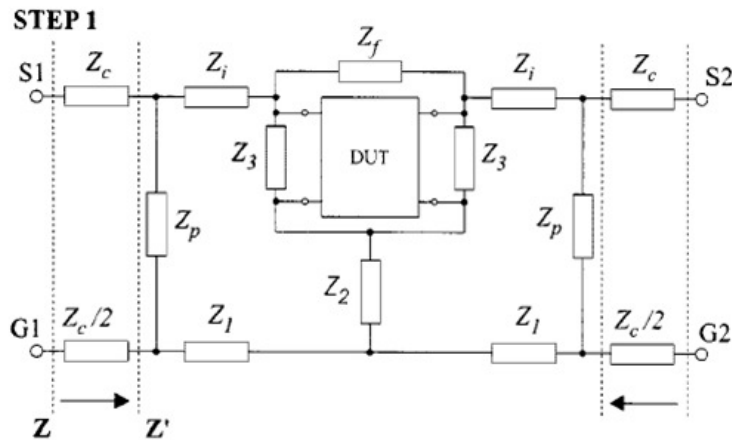


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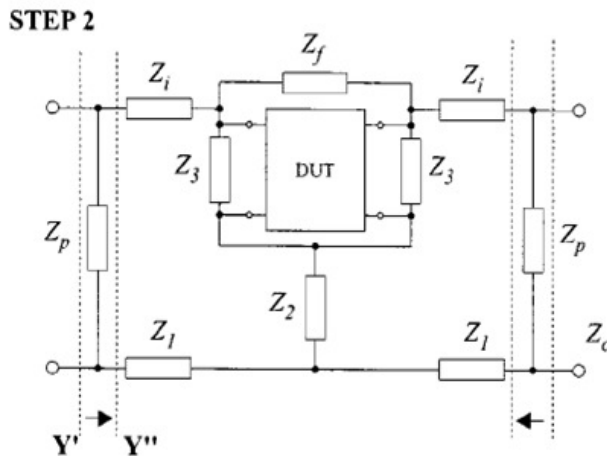
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FIGURE 14.3 Step 1



$$Z' = Z - \begin{bmatrix} \frac{3}{2} & 0 \\ 0 & \frac{3}{2} \end{bmatrix} Z_c$$

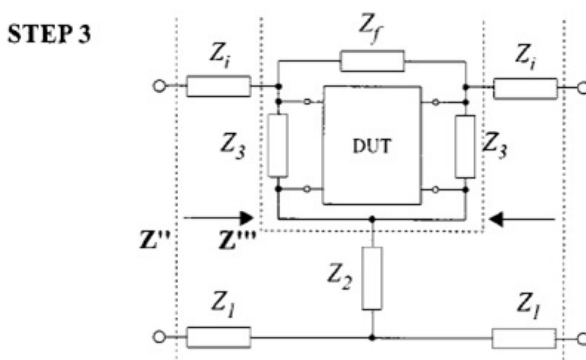
FIGURE 14.4 Step 2



$$Y'' = Y' - \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \frac{1}{Z_p}$$

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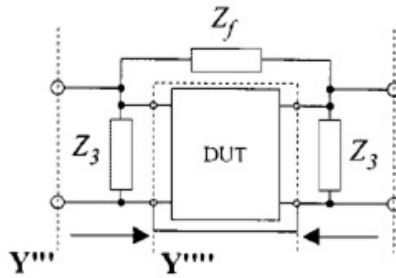
FIGURE 14.5 Step 3



$$Z''' = Z'' - \begin{bmatrix} Z_i + Z_1 + Z_2 & Z_2 \\ Z_2 & Z_i + Z_1 + Z_2 \end{bmatrix}$$

FIGURE 14.6 Step 4

STEP 4



$$Y''' = Y'' - \begin{bmatrix} \frac{1}{Z_3} + \frac{1}{Z_4} & -\frac{1}{Z_f} \\ -\frac{1}{Z_f} & \frac{1}{Z_3} + \frac{1}{Z_4} \end{bmatrix}$$

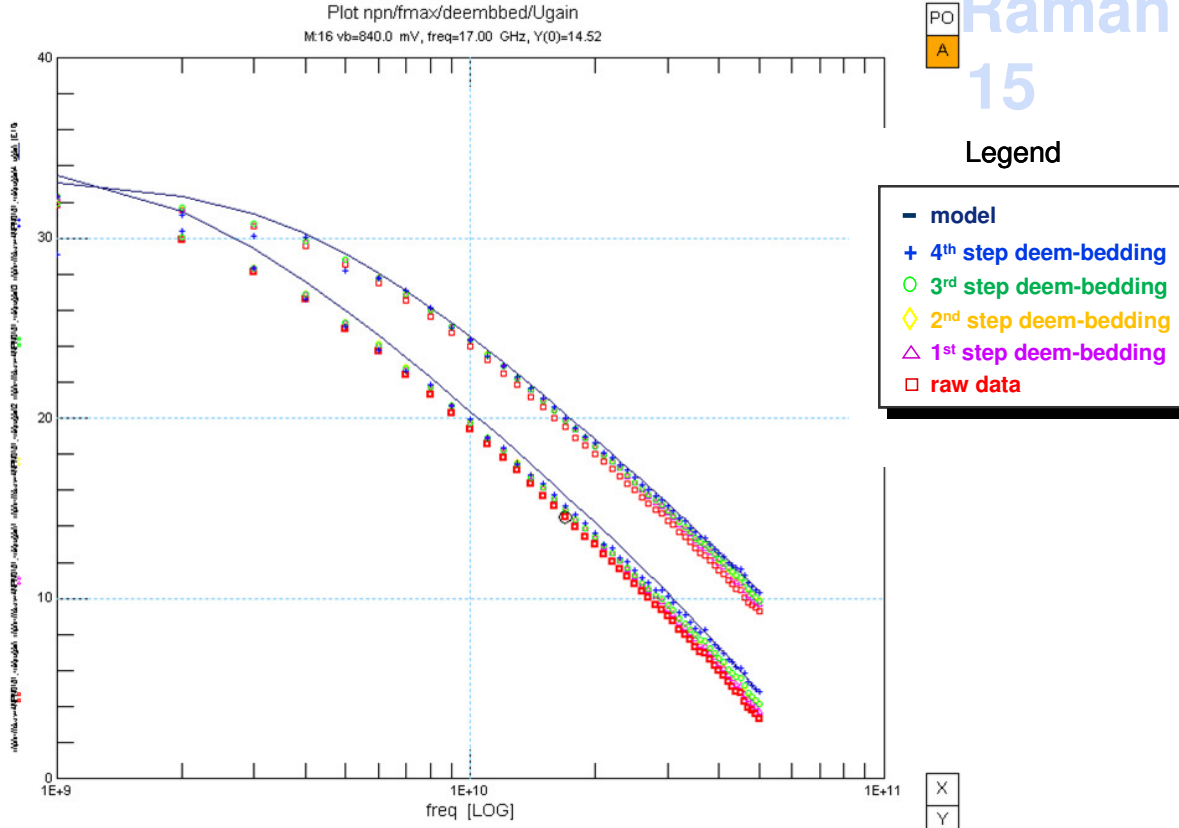
Ref.: Troels Emil Kolding, "A Four-Step Method for De-Embedding Gigahertz On-Wafer CMOS Measurement" IEEE TRANSACTIONS ON ELECTRONIC DEVICES, VOL. 47, NO 4, April 2000 pp. 734-740

14.2 High Frequency Model Validation for NPNs

14.2.1 NPN Plot Description

Figure 14.7 shows the Ugain plot using the local bipolar model against the raw data, the data after the first deembedding step, second step, third step and fourth step.

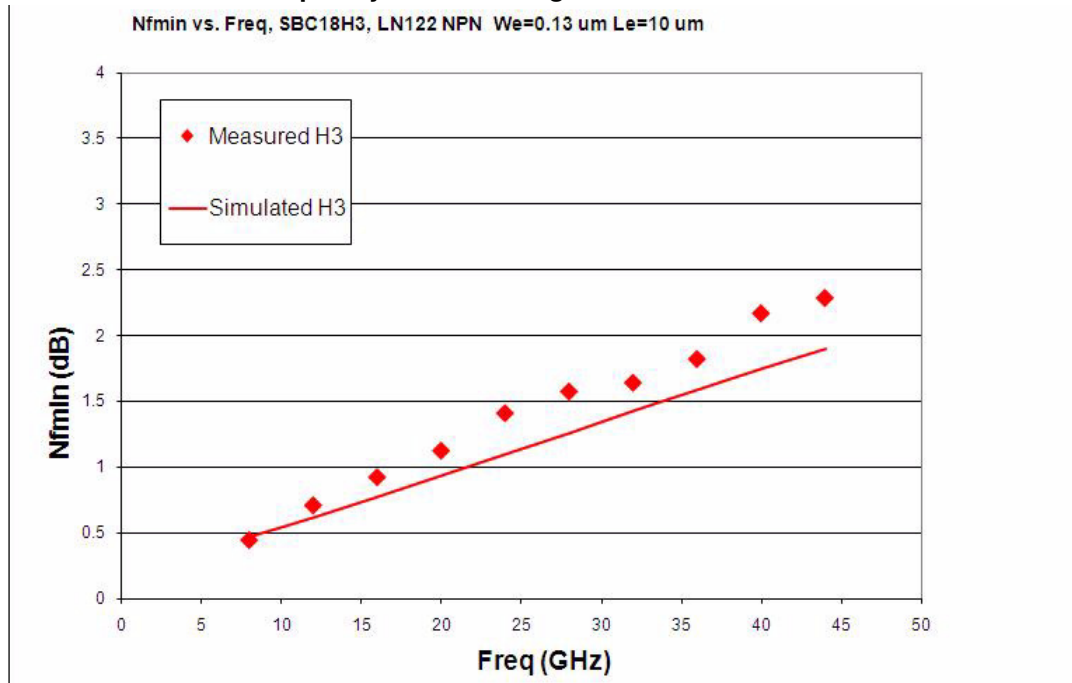
FIGURE 14.7 Ugain plot for Vb=0.86 and 0.90 Volts



14.2.2 Noise-Figure Model Validation

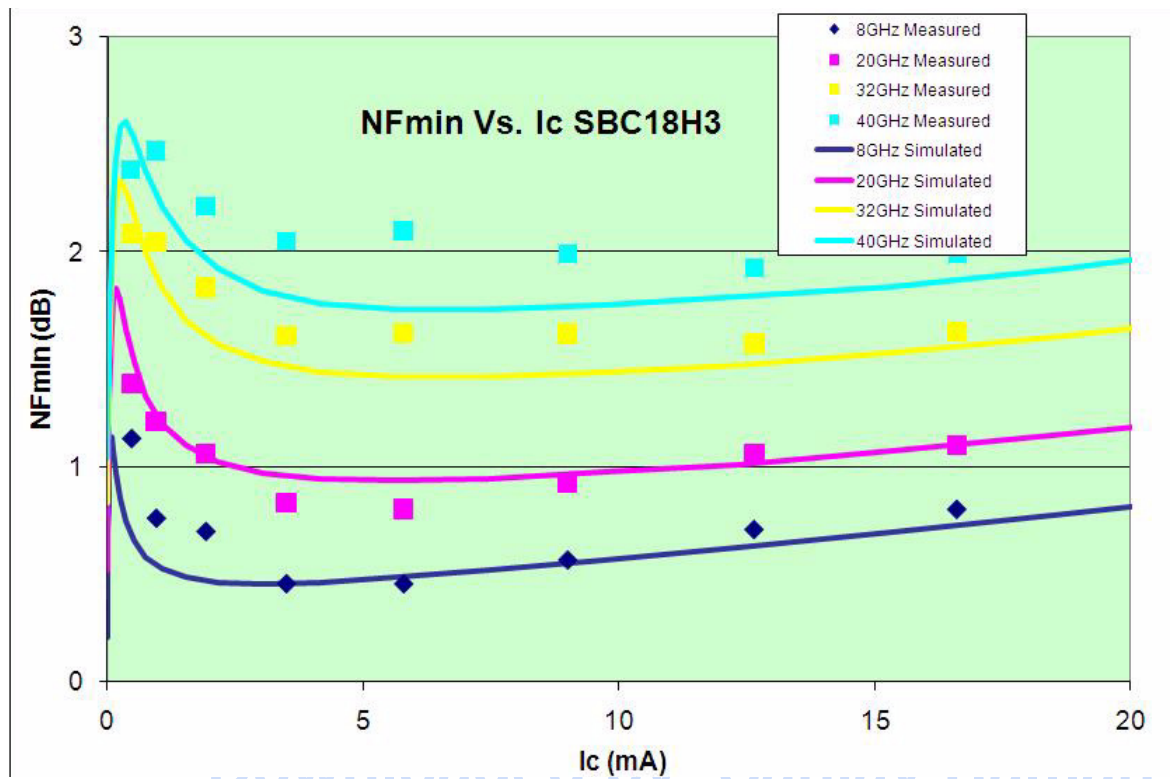
The minimum Noise Figure was measured on the Maury system, and compared with simulated data in Figures 14.8 and 14.9.

FIGURE 14.8 NFmin vs. frequency for low-voltage SBC18H3 SiGe NPNs



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FIGURE 14.9 NFmin vs. I_c for low-voltage SBC18H3 EWxEL = 0.13x20um SiGe NPNs

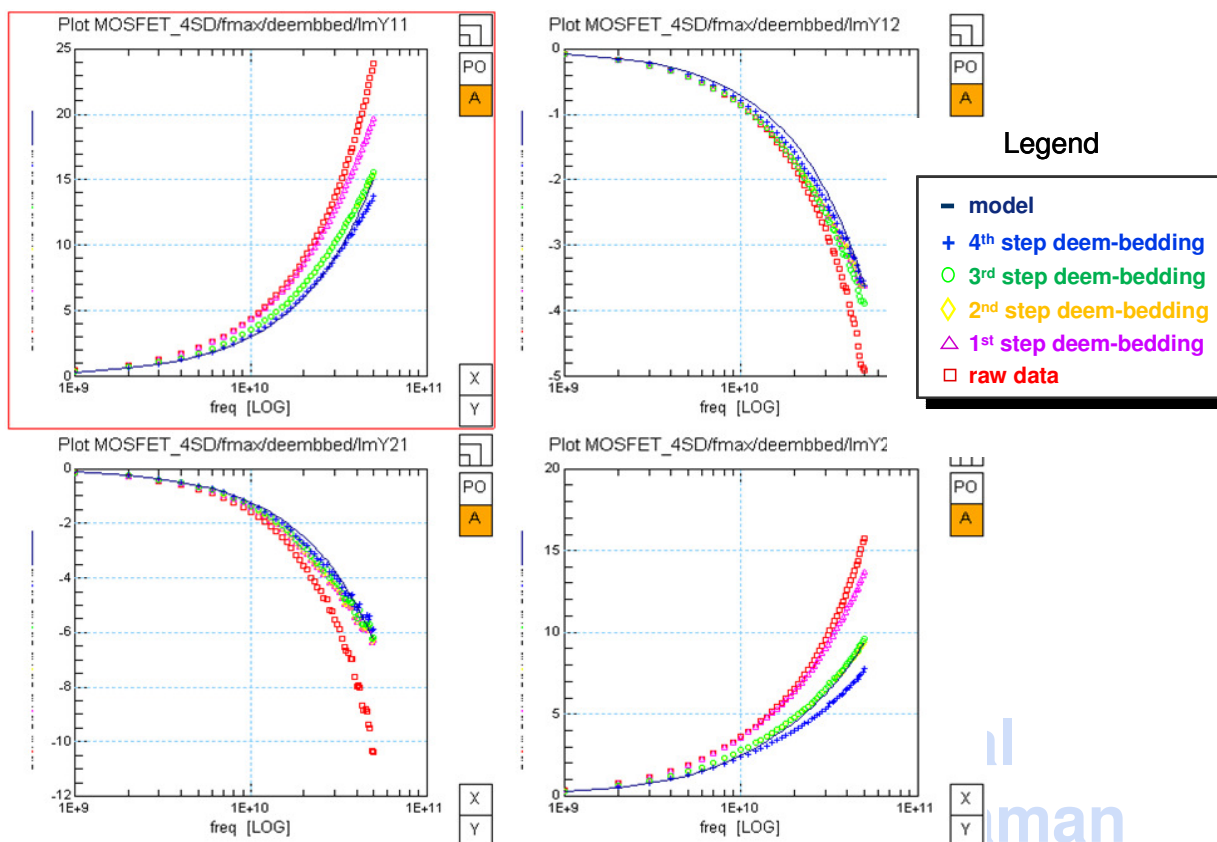


14.3 High Frequency Model Validation for PSP MOSFET

14.3.1 MOSFET Plot Description

Figure 14.10 shows the imaginary component of the Y-parameter (after the first deembedding step, second step, third step and fourth step) plotted vs. the PSP NQS (non-quasi static) model. The device is a 16 finger RF NFET with a width of 10um and a length of 0.18um.

FIGURE 14.10 Y-parm PSP MOSFET model with $V_g=0.85$ and $V_d=1.8$ Volts

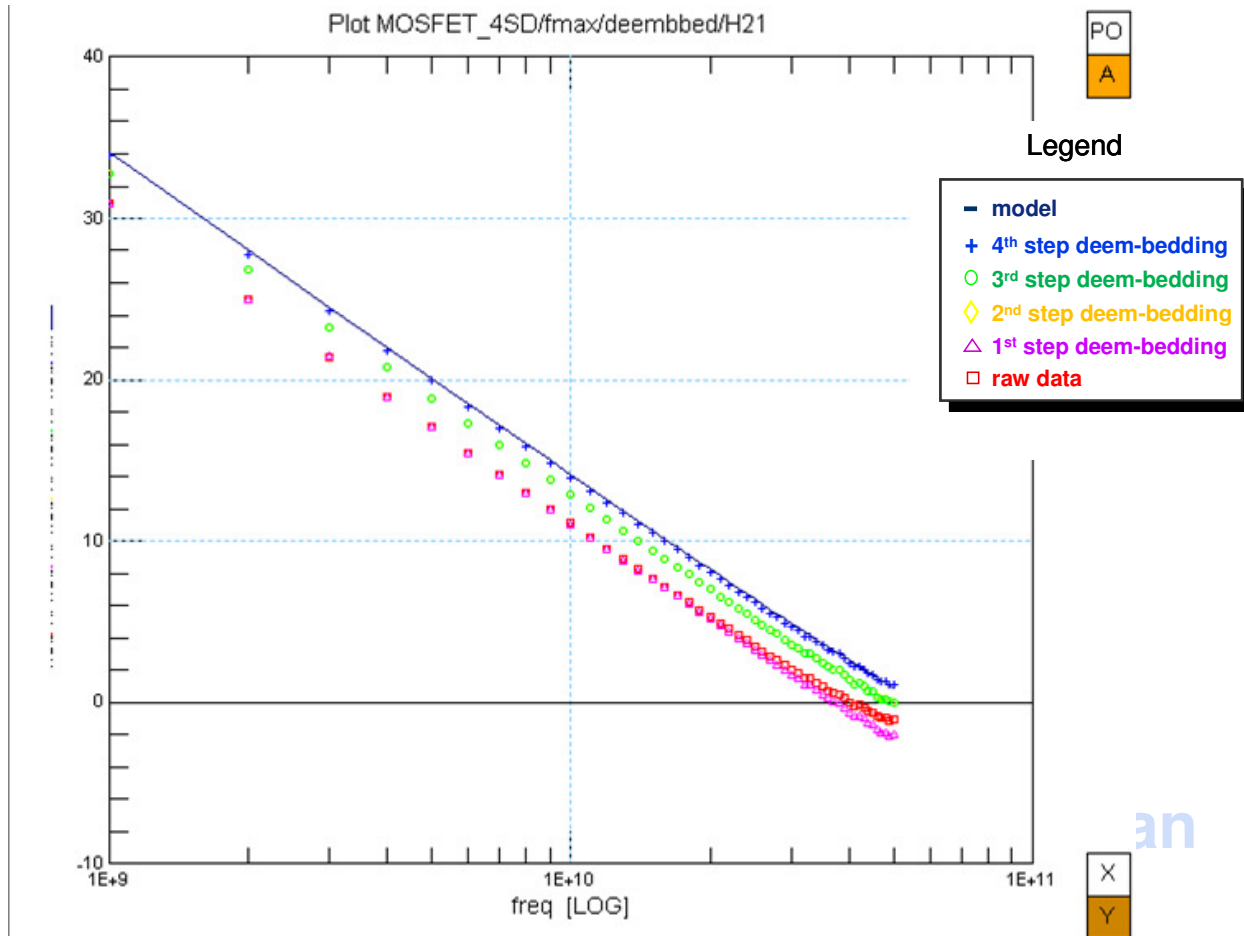


14.4 High Frequency Model Validation for BSIM MOSFET

14.4.1 MOSFET Plot Description

Figure 14.11 shows the magnitude of H_{21} vs. frequency (after the first deembedding step, second step, third step and fourth step) plotted vs. the BSIM model. The device is a 16 finger RF NFET with a width of 10 μ m and a length of 0.18 μ m.

FIGURE 14.11 H21 BSIM MOSFET model with $V_g=0.85$ and $V_d=1.8$ Volts



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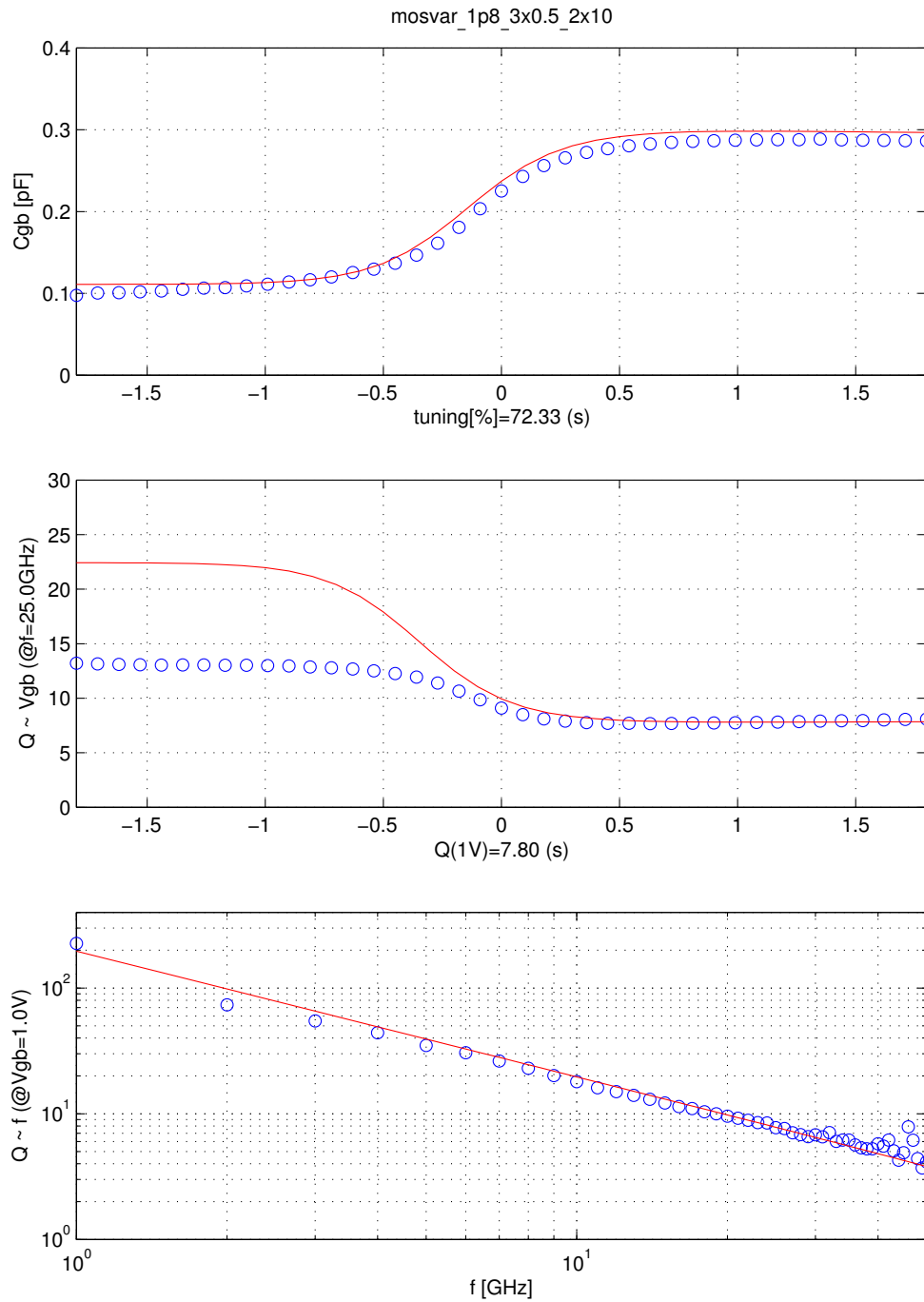
14.5 High Frequency Model Validation for 1.8V MOS Varactor

14.5.1 1.8V MOS Varactor Plot Description

Figure 14.12 shows three plots for the 1.8V MOS Varactor model against de-embedded data (using an open and thru de-embedding technique). All plots are from a device with size $w_g=3.0\mu\text{m}$ x $l_g=0.5\mu\text{m}$ x slices=2 x fingers=10. The first plot shows $C_{gb}(@\text{low freq})$ vs. V_{gb} , the second shows $Q(@25\text{GHz})$ vs. V_{gb} and the third shows the Q vs. frequency.

FIGURE 14.12 1.8V MOS Varactor model plots

sbc18 – mosvar_1p8: data(bo), model(r–) @T=[25]C



15.0 X-Sigma Corner and Statistical Models

15.1 X-Sigma Corner Models

X-Sigma corner models, introduced in model version 6.0, allow for process variation settings different than conventional corner models which typically set the process variation to worst case ± 3 sigma. Process sigmas, classified into device types, are variable inputs. In their limits, the X-Sigma models align to the limits of the ESPECs. The ESPECs limits are mostly aligned with the PCM limits. Typically, the process may run tighter than the PCM limits. Combined with PCM data tracking, the X-Sigma models allow design to a more aggressive process variation than is predicted by the ESPECs. The added flexibility provides for direct insight into circuit sensitivities previously hidden by the fixed corner settings.

15.1.1 Device Correlation

The X-Sigma models provide 100% correlation among device types. Table 15.1 shows the device class groupings and the related independent process variables which fall under their control. The individual devices are listed in the horizontal axis of the table. Table entries indicate variation caused by the given process variable on the particular device. Some horizontal device names represent groups of devices (e.g. hs, std and hv npns under NPN). When a process variable affects more than one device type, a judgement is made on the relative significance of the process variable. This in turn determines which class controls the sigma variation. A master slave approach is used where the secondary device, or slave device, follows the variation determined by the master device. For example, the 3.3V nwell doping impacts both the 3.3V pfet and the VPNP devices. The master device in this case is the 3.3V PFET, since the nwell is specifically tailored to meet the needs of this OSFET. A FET sigma set to $+3$ sigma results in a smaller poly CD, yielding higher I_D and a “faster” FET. Conversely, the smaller poly CD yields a larger poly resistance which is considered a “slower” RES. If the RES class is set to $+3$ in this case, the other process variables affecting the poly resistors, sheet rho and end resistance, are set to their $+3$ case, tending towards the “faster”, lower resistance. Combined with the $+3$ FET setting, the poly resistors will not be at their fastest setting due to the smaller width set by the poly CD. The “fastest” poly resistor is only realized when the RES is set to $+3$ and the FET is set to -3 . Figure shows a graphical representation of this case. Figure 15.2 shows the X-Sigma variation of some key ESPECs for the STD NPN device.

15.1.2 Design Kit Implementation

Figure 15.3 shows the Cadence analog environment implementation of the X-Sigma models. Entry fields for the sigma number are given for each device class. The legacy corner model buttons are listed for backward compatibility and can not be used in unison with the X-Sigma or STAT models. Once X-Sigma is selected for a device class, all device classes are switched to X-Sigma. When the X-Sigma models are chosen, the device class sigma variables become design variables as shown in the Figure 15.3. Users are then free to access these variables within the environment, enabling custom parametric sweeping for example. Figure 15.4 shows an example VCO circuit and plots resulting from a sweep of the FET global sigma with a parametric CAP global sigma sweep.

TABLE 15.1 X-Sigma Model Matrix showing individual device dependence on global process variables

Device Class	Independent Process Variables	Device											
		1 . 8 N F E T	1 . 8 P F E T	3 . 3 N F E T	3 . 3 P F E T	S i G e N P N	1 . 8 M O S V A R	3 . 3 M O S V A R	3 . 3 V P N P	S A L R E S	U N S A L R E S	M I M C A P	I N D U C T O R
GLOBAL (+ve values yield fast FETs)	Active CD	✓	✓	✓	✓		✓	✓					
	1.8V oxide thickness	✓	✓				✓						
	3.3V oxide thickness			✓	✓			✓					
	Poly CD	✓	✓	✓	✓		✓	✓		✓	✓		
	Surface roughness (channel mobility)	✓	✓	✓	✓								
	Flat-band voltage	✓	✓	✓	✓		✓	✓					
	Poly/silicide contact resistance	✓	✓	✓	✓		✓	✓					
	STI thickness									✓	✓		
1.8V NFET	Channel doping	✓											
	Pocket doping	✓											
	LDD doping	✓											
1.8V PFET	Channel doping		✓				✓						
	Pocket doping		✓										
	LDD doping		✓										
3.3V NFET	Channel doping			✓									
	Pocket doping			✓									
	LDD doping			✓									
3.3V PFET	Channel doping				✓			✓	✓				
	Pocket doping				✓								
	LDD doping				✓								

TABLE 15.1 X-Sigma Model Matrix showing individual device dependence on global process variables

Device Class	Independent Process Variables	Device											
		1 . 8 N F E T	1 . 8 p F E T	3 . 3 N F E T	3 . 3 P F E T	S i G e N P N	1 . 8 M O S V A R	3 . 3 M O S V A R	3 . 3 V P N P	S A L R E S	U N S A L R E S	M I M C A P	I N D U C T O R
NPN	Emitter-base oxide thickness					✓							
	Emitter doping					✓							
	Emitter Poly/Si Interface					✓							
	Base Boron doping					✓							
	Base thickness					✓							
	Collector epi doping					✓							
	Collector epi thickness					✓							
	NPN selective collector implantaion dosage					✓							
	Base Ge doping					✓							
	Emitter-base recombination concentration					✓							
Buried layer resistance/doping					✓								
silicided Resistors	Salicide sheet resistance	✓	✓	✓	✓		✓	✓		✓			
	End resistance									✓			
Unsilicided Resistors	Poly doping										✓		
	End resistance										✓		
CAP	Top metal thickness											✓	
	MiM oxide thickness											✓	
INDUCTOR	Top metal thickness												✓
	Metal CD												✓
	Inter-layer dielectric thickness												✓

S

TABLE 15.2 X-Sigma Numbers to Achieve Worst Case Devices

		X-sigma Variable														
Device	Figure of Merit	global	n1p8	p1p8	n3p3	p3p3	npn	salres	lvres	hvres	rnw	cap	ind	hpvar	hppnp	
1.8V NFET	Low Idsat, High Vt and Gate res.	-3	-3					-3								
1.8V PFET		-3		-3				-3								
3.3V NFET		-3			-3			-3								
3.3V PFET		-3				-3		-3								
1.8V MOS VAR ¹	Lower Cap. and Q	-3		-3				-3								
SiGe NPN	Lower Beta, Ic, Ft						-3									
VPNP	Low Ic, Beta										-3					
Lateral PNP	Low Ic, Beta						-3									
Sal. RES	High Resistance	3						-3								
LV RES	High Resistance	3							-3							
HV RES	High Resistance	3								-3						
Nwell RES	High Res	-3									-3					
MIM CAP	High Cap											-3	-3			
INDUCTOR	High Ind., Low Q	-3											-3			
HP VAR	High Cap., low Q and tuning range	-3												-3		
HP PNP	Low Ic, Beta														-3	

1. The 1.8V MOS Varactor device is a slave device without an independent control variable.

FIGURE 15.1 Example FET (e.g. n1p8_global_sigma) and RES X-Sigma Correlation Plots
1.8v nfet 10x0.18 μ m

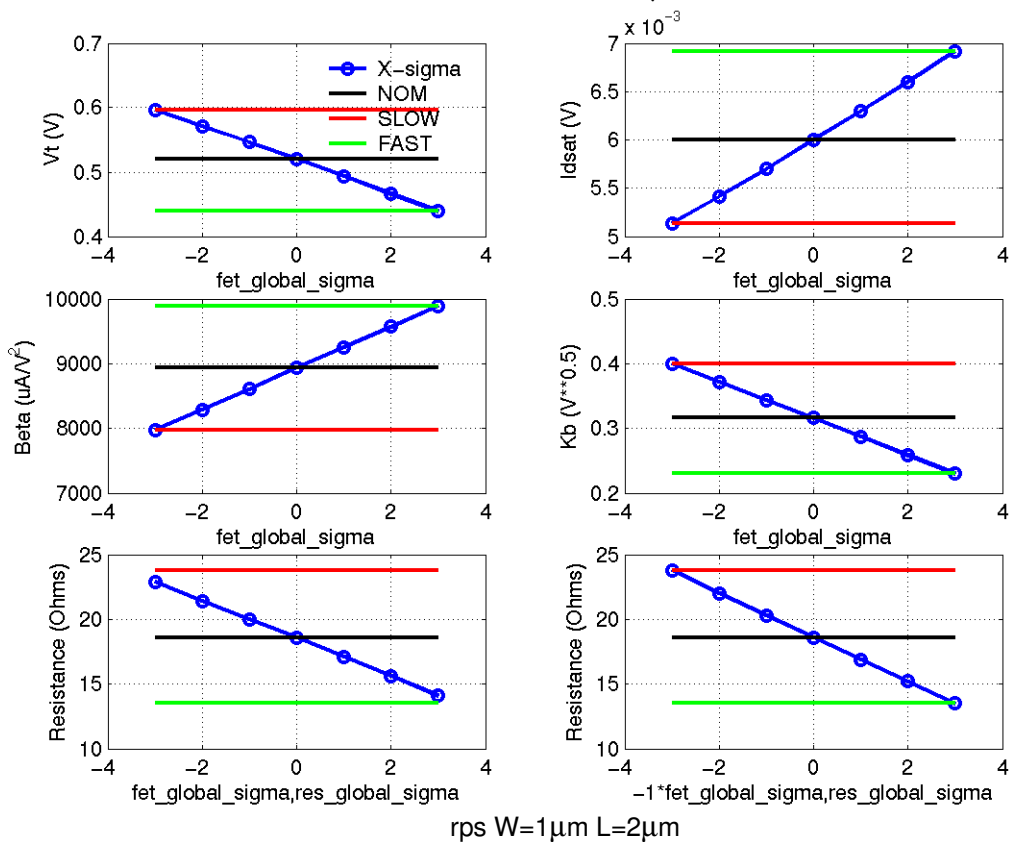


FIGURE 15.2 Example NPN X-Sigma Plots

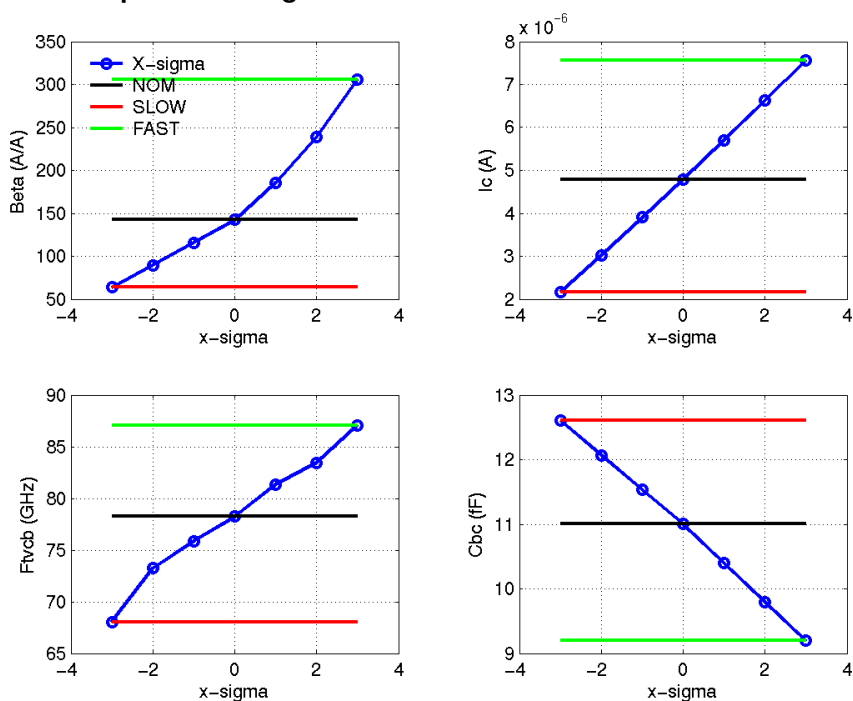


FIGURE 15.3 JAZZ Design Kit Model Library Selection Form

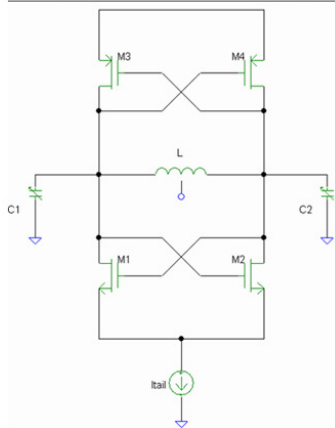
The screenshot shows the 'Jazz Model Libraries' dialog box. The 'Library' is set to 'sbc18' and 'Versions' is 'v6.2a (default)'. The dialog lists various corner models with radio button options for each. Annotations include:

- A red arrow pointing to the 'ONE_SIGMA' option with the text 'Set σ_s '.
- A red arrow pointing to the 'params' option with the text 'Provided for backward compatibility'.
- A blue box highlights the 'NOM', 'FAST', and 'SLOW' options for the 'global comers' through 'hpnnp comers'.
- A red arrow points to the 'RTH' option for 'nnp_rth comers' with the text 'Run stat on device class basis'.
- A red arrow points to the 'PSP' option for 'fet comers' with the text 'NPN thermal resistance'.
- A blue oval highlights the 'STAT' and 'X_SIGMA' options for the 'global comers' through 'hpnnp comers'.

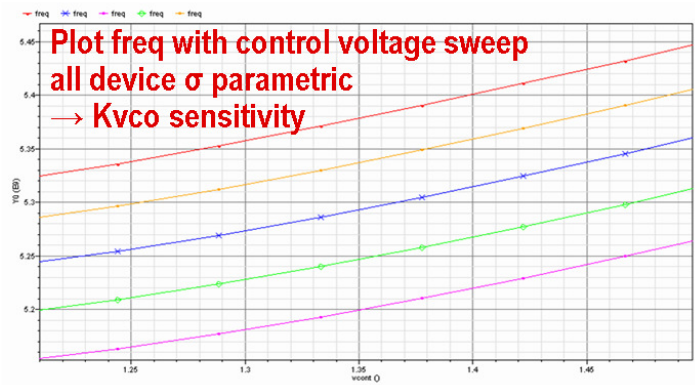
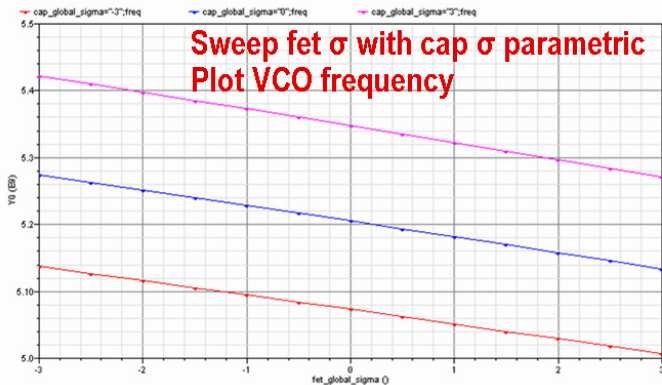
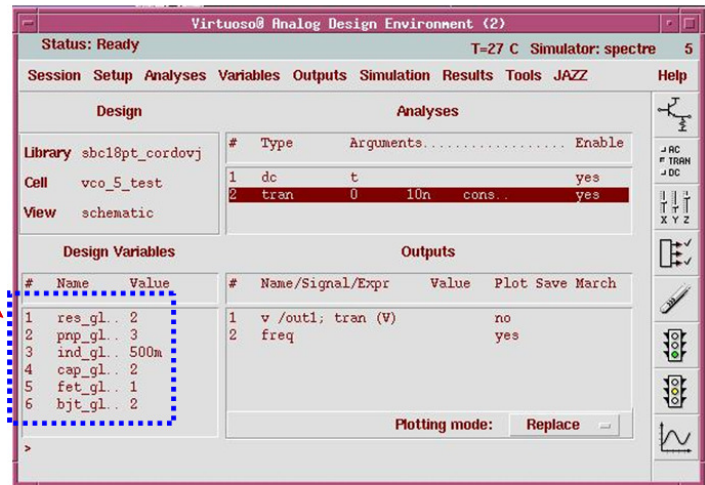
Model Category	ONE_SIGMA	params	NOM	FAST	SLOW	STAT	X_SIGMA
one_sigma comers	<input checked="" type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>
statistics comers	<input checked="" type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>
global comers	<input checked="" type="radio"/>	<input type="radio"/>	<input checked="" type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>
ind comers	<input checked="" type="radio"/>	<input type="radio"/>	<input checked="" type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>
nnp comers	<input checked="" type="radio"/>	<input type="radio"/>	<input checked="" type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>
lvres comers	<input checked="" type="radio"/>	<input type="radio"/>	<input checked="" type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>
hvres comers	<input checked="" type="radio"/>	<input type="radio"/>	<input checked="" type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>
salres comers	<input checked="" type="radio"/>	<input type="radio"/>	<input checked="" type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>
mw comers	<input checked="" type="radio"/>	<input type="radio"/>	<input checked="" type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>
n1p8 comers	<input checked="" type="radio"/>	<input type="radio"/>	<input checked="" type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>
p1p8 comers	<input checked="" type="radio"/>	<input type="radio"/>	<input checked="" type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>
n3p3_5p0 comers	<input checked="" type="radio"/>	<input type="radio"/>	<input checked="" type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>
p3p3_5p0 comers	<input checked="" type="radio"/>	<input type="radio"/>	<input checked="" type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>
cap comers	<input checked="" type="radio"/>	<input type="radio"/>	<input checked="" type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>
hpvar comers	<input checked="" type="radio"/>	<input type="radio"/>	<input checked="" type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>
hpnnp comers	<input checked="" type="radio"/>	<input type="radio"/>	<input checked="" type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>
nnp_rth comers	<input checked="" type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input checked="" type="radio"/>	<input type="radio"/>
circuit comers	<input checked="" type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>
fet comers	<input checked="" type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input checked="" type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>

FIGURE 15.4 X-Sigma Parametric Sweep Example

Simple VCO Example



Access σ_s as
design variables



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15.2 Statistical Models

Statistical models provide the most accurate simulation of the process variation at the expense of simulation time. The random nature of Monte-Carlo simulation emulates the true process variation. The statistical and X-Sigma models use the same model libraries and statistical mappings. Thus, Table 15.1 applies fully to the statistical models. The difference lies in the amount of sigma variation (simulator defined for statistical simulation, user defined for the X-Sigma model simulation). In the V6.1 and subsequent model and related design kit releases, the statistical simulation is set by device class as shown in Figure 15.3. Prior releases required simultaneous statistical simulation of all devices. Isolated statistical simulation provides more direct access to circuit sensitivities to particular devices. Statistical simulation of one device (or multiple) device class can be combined with X-Sigma simulation of another (or multiple) device class. The statistical models are not compatible with the legacy corner models.

15.3 Verification

Tables for each device type showing the corner and statistical simulation match to the technology ESPECs are contained in the relevant device chapters of this design manual.

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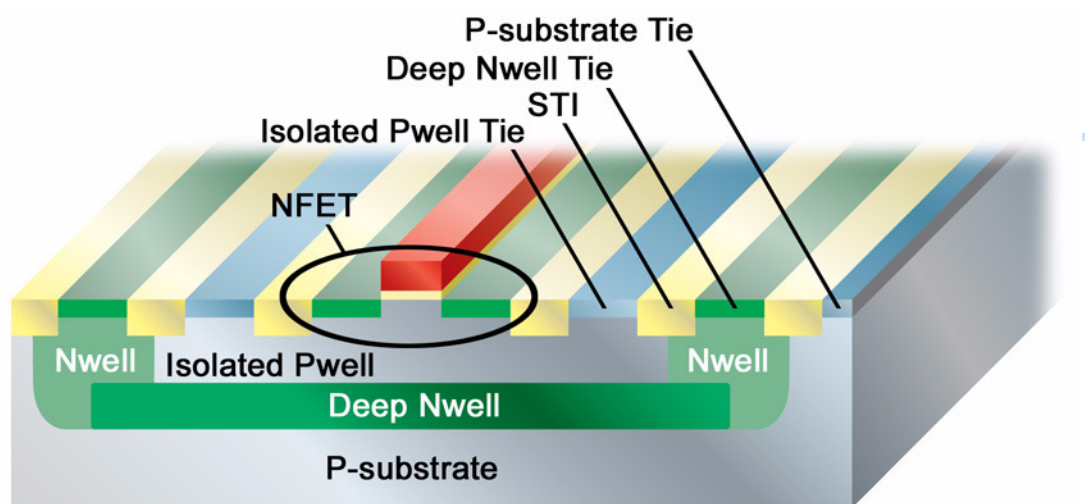
16.0 Deep Nwell

16.1 Introduction

The purpose of this section is to describe the use of the Deep Nwell module to provide additional substrate isolation for sensitive circuitry using elements such as the `nfet_rf`, `MiM` or resistor passive devices. This chapter describes how the TowerJazz design environment accounts for the Deep Nwell process module. This document will cover the modeling, schematic, layout, and verification aspects of this technology. For details on Deep Nwell process availability and specifications please refer to the respective design rules and electrical specification documents.

The current Deep Nwell implementation provides a methodology that allows for robust connectivity and verification and provides a basic model. Among some of the benefits, this methodology allows the designer to bias the isolated Pwell separately from the outer P-substrate. It will also prevent the improper biasing (such as forward bias) of the junctions formed by the Deep Nwell by reporting design rule and LVS violations. Please refer to Figure 16.1 and Figure 16.3 for Deep Nwell silicon cross section, top views, and legend.

FIGURE 16.1 Deep Nwell Silicon Cross Section including isolated NFET.



16.2 Modeling

The addition of Deep Nwell will form two PN junction diodes across the physical circuit area. The Jazz design environment models these junctions as separate diodes ***diso*** and ***ddnw*** as seen in Figure 16.2. The first diode ***diso*** is formed by the Deep Nwell/Nwell to Isolated Pwell junction. The second diode, ***ddnw***, is formed by the the P-substrate to Deep Nwell/Nwell junction. Table 16.1 lists the ESPEC and NOM model simulation of the area and perimeter capacitances. Corner and statistical models are not supported. Investigation of the DC and RF effects of the Deep Nwell is given in Section 16.6.

TABLE 16.1 Deep Nwell Diode ESPEC vs. NOM Model

Capacitance	units	Espec	NOM
Pwell to DNW CA ¹	$\mu\text{F}/\text{m}^2$	546.6	546.7
Pwell to DNW CP ¹	nF/m	1.346	1.346
DNW to P-Sub CA ¹	$\mu\text{F}/\text{m}^2$	126.7	126.8
DNW to P-Sub CP ¹	nF/m	3.124	3.122

PCM notes:

1. PCM and ESPEC share the same limits.

16.3 Schematic Entry

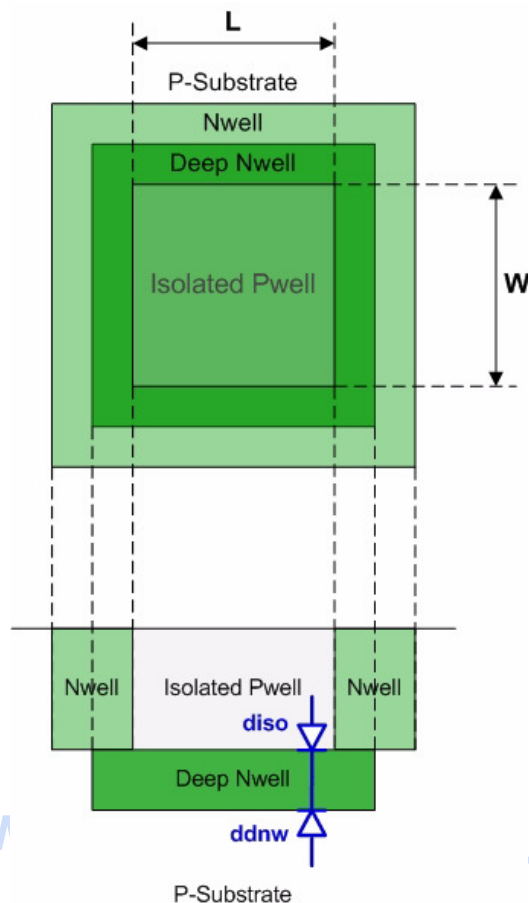
The two diodes, **ddnw** and **diso**, are shown in Figure 16.2.

FIGURE 16.2 ddnw Device Schematic

16.3.1 Device Attributes

The geometry of each of the diodes can be entered by A/P (area and perimeter), L/W (length and width), or A/R (area and aspect ratio). For the **diso**, the geometry is a measure of the isolated Pwell. For the **ddnw**, the geometry is a measure of the drawn deep Nwell layer. Typically these devices can be used during schematic entry and simulation to give an estimate of the Deep Nwell construction.

FIGURE 16.3 Deep Nwell Top view and Cross section



Once layout is completed, the schematic should be updated to reflect the final geometries. Section 10.5.2 will describe how these parameters are included in LVS.

FIGURE 16.4 *ddnw* device attributes

CDF Parameter	Value
Model name	dnw_psub
Specify	<input checked="" type="radio"/> A/P <input type="radio"/> WL <input type="radio"/> A/R
Width	5u M
Length	5u M
Area	25.0p M ²
Perimeter	20u M
Aspect - Ratio	1
Count	1

16.3.2 Connectivity

The **diso** and **ddnw** devices allow the designer to connect and bias the Isolated Pwell and P-substrate independently. By default, the Jazz three terminal FETs come embedded with an inherited substrate connection

“sub_inh” set to “sub”. The value of the sub_inh property may be changed through the object properties page as shown in Figure 16.5. Four terminal FETs allow for more explicit definition of the substrate connection. Finally, for all other devices allowed in deep nwell such as diodes, poly resistors, and capacitors, the user may edit the **Substrate Node** property directly through the CDF.

FIGURE 16.5 How to define a FET substrate name

The screenshot shows the 'Edit Object Properties' dialog box with the following sections:

- Buttons:** OK, Cancel, Apply, Defaults, Previous, Next, Help.
- Apply To:** only current (selected), instance.
- Show:** ☐ system, ☒ user, ☒ CDF.
- Property Table:**

Property	Value	Display
Library Name	sbcl8pt	off
Cell Name	nfet_rf	value
View Name	symbol	off
Instance Name	M2	off
- User Property Table:**

User Property	Master Value	Local Value	Display
sub_inh		PISQ	off
- CDF Parameter Table:**

CDF Parameter	Value	Display
Model Name	nfet_rf	off
Substrate Node	PISQ	off

Figure 16.6 illustrates the schematic view of two NFET transistors. The right hand side NFET (M2) will be placed over Deep Nwell, while the left hand side device (M0) will be placed over P-substrate. The schematic also shows how the ddnw device can be properly connected to each transistor.

FIGURE 16.6 Deep Nwell connectivity example



The Deep Nwell (Cadence layer “dnw”, number 36) can be drawn around a circuit block or an element. At this point, no layout view is provided to generate the Deep Nwell/Nwell ring structure. The user must draw the Deep Nwell, Nwell layers, and ntap and ptap contacts when applicable. The figure below pictures the layout view of the example given in the proceeding section.

FIGURE 16.7 Deep Nwell layout example



16.5 Verification

16.5.1 Design Rules

Please refer to the design rule document for complete details.

16.5.2 LVS

The LVS routine will check for accurate connectivity matching. In addition, the LVS deck provides the “**CompareDnwDiode**” switch. Once enabled, this switch will trigger the comparison of the **Area** and **Perimeter** properties defined in the **ddnw** and **diso** schematic elements with the physical properties, as defined by layout, of the Isolated Pwell.

16.6 RF and DC Measurement Validation

The deep n-well structure can greatly improve the device isolation from substrate. On the modeling side, in order to provide an accurate RF SPICE model, the impact on both DC and RF performance from the deep n-well must be studied. This section focuses on the impact of deep n-well on the CMOS transistor using the **nfet** device in the Jazz 0.18 μ m CMOS as a test case.

16.6.1 Test Structure and Experiment Description

Test structures are fabricated in order to compare the DC and RF performance of deep nwell and standard devices. Table 16.2 lists the 4 types of tests along with test structure description and WELL connections. For all tests, the *gate* is port 1, the *drain* is port 2, and the *source* is connected to ground of the GSG probe.

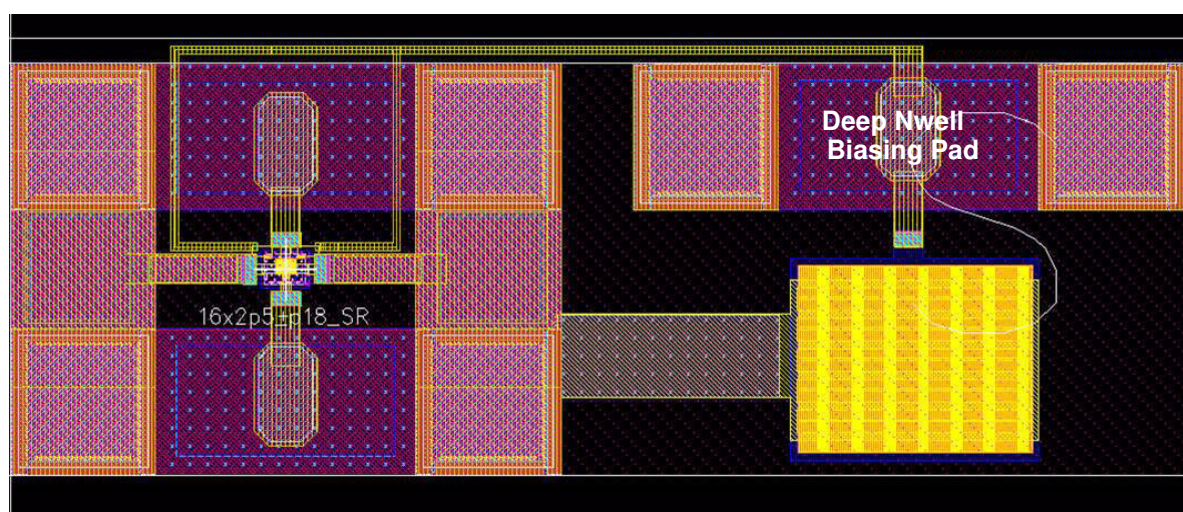
TABLE 16.2 Test Descriptions

Test Name	Test Structure Description	PWELL	Deep Nwell	P-Sub
<i>NDNW</i>	standard device in P-Substrate	G (of GSG)	NA	G
<i>DNWA</i>	deep Nwell device with isolated PWELL, deep Nwell, and P-Substrate all tied to ground of GSG.	G	G	G
<i>DNWB</i>	deep Nwell device with isolated PWELL and P-Substrate all tied to ground of GSG. Deep Nwell connected to separate DC bias with large de-coupling capacitor.	G	0 V	G
<i>DNWB3</i>	deep Nwell device with isolated PWELL and P-Substrate all tied to ground of GSG. Deep Nwell connected to separate DC bias with large de-coupling capacitor.	G	3 V	G

The DC and S-parameters are measured at different bias conditions. For the RF characterization, the measured raw S-parameters are de-embedded from the *Open* and *Short* S-parameters. After the de-embedding,

the Y-parameters are plotted against frequency. We compared Y-parameters with *NDNW* vs. *DNWA*, *DNWA* vs. *DNWB*, and *DNWB* vs. *DNWB3*. The purpose of the *DNWA* vs. *DNWB* comparison is to verify that the DC biasing scheme for the deep Nwell is correct. The Y-parameters for these two cases should be identical since the deep Nwell is grounded in both. The purpose of the *DNWB3* test is to investigate any “pinching” effects of the depletion region into the isolated PWELL. In normal circuit operation, the deep Nwell is biased to the VDD of the circuit. This test will illuminate any requirement to modify the substrate network in the RF MOSFET model for deep Nwell devices. Figure 16.8 shows the layout for the *DNWB* and *DNWB3* measurements. A GSGGSG probe is used to contact the deep Nwell and *drain* at port 2, assuring consistent DC and AC grounding.

FIGURE 16.8 DNWB Layout



16.6.2 DC Measurements and Analysis

In all 4 cases the DC Output characteristic are measured. The bias conditions are listed Table 16.3.

TABLE 16.3 DC Measurement Conditions

Sweep	Start	Stop	Step
VD	0	1.8	0.05
VG	0	1.8	0.3
VS	0	0	0
VB	0	0	0

In the case of *DNWB* and *DNWB3*, additional DC biases of $V_{dnw}=0$ and $V_{dnw}=3V$ are applied respectively to the Deep Nwell to monitor the change of the drain current I_d and output conductance g_{ds} . The output conduc-

tance g_{ds} is derived numerically from the drain current data where a small step = 50mV is applied to keep the g_{ds} smooth. The DC measurement is performed by the Agilent E5270A parametric Measurement Unit.

Figure 16.9 compares the *NDNW* and *DNWA* drain current I_d and output conductance g_{ds} . Figure 16.10 shows a zoom in of the output conductance. The differences seen are on the same order of measurements on exact devices (both without deep Nwell) in different die. Therefore the differences can be attributed to process variation. Furthermore, comparisons of *DNWB* and *DNWB3* yield the same results as expected.

FIGURE 16.9 NDNW vs. DNWA Drain Current I_d

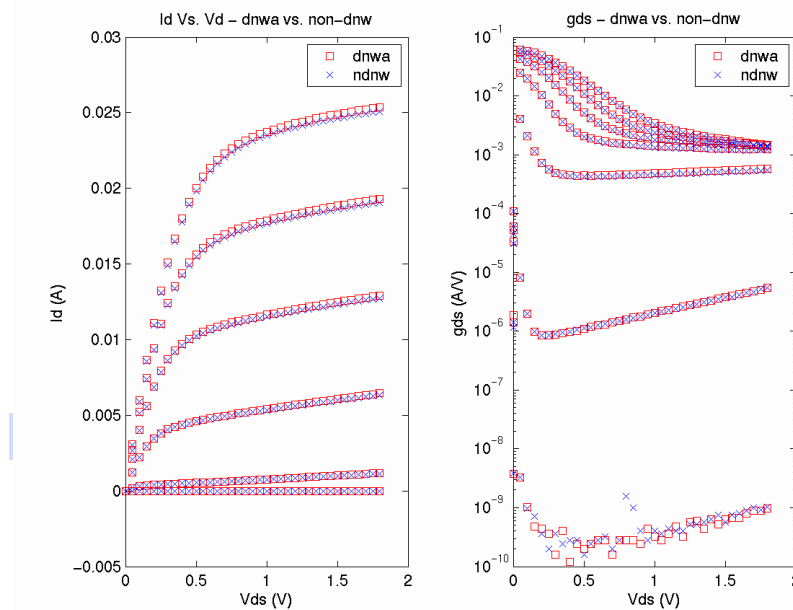
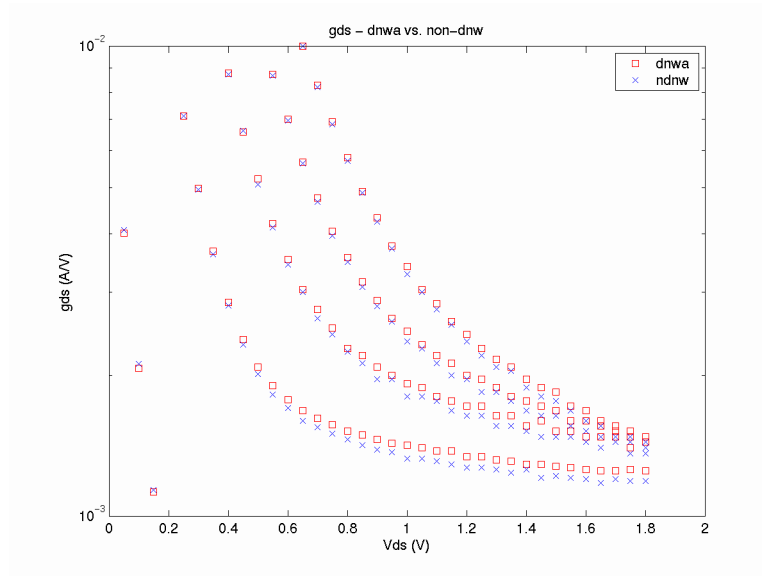


FIGURE 16.10 NDNW vs. DNWA Output Conductance gds



At VG=0.9, VD=1.8, Δgds=15%

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16.6.3 Y-parameter Measurements and Analysis

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S-parameter measurements are performed by the Agilent network analyzer E8376B with the frequency sweep from 100MHz to 10.1 GHz. Two step, open-short de-embedding is performed and the results converted to Y-parameters. The DC bias conditions are listed in Table 16.4. Figure 16.9 through Figure 16.10 display the *NDNW* vs. *DNWA* comparisons for a device with $NF_xW_gxL_g=16x2.5x0.18$. The expected potential difference is in $Real(Y_{22})$ where the bulk resistance affects the high frequency data. At low frequencies, $Real(Y_{22})$ is proportional to g_{ds} . The shifts in $Real(Y_{22})$ can be attributed to the difference in the DC output conductance shown in Figure 16.11. Similarly, shifts in the $Real(Y_{21})$ are a result of small differences in the transconductance g_m . The Y-parameters are all close in value and frequency dependence except for $Real(Y_{11})$ and $Real(Y_{12})$ whose values are all close to the dynamic range limit of the NWA¹. It was also discovered that there are minor differences between the gate connection in the layout between the *NDNW* and *DNWA* which can be amplified when operating close to the dynamic range limit. Figure 16.13 through Figure 16.15 show the Y-parameter *NDNW* vs. *DNWA* comparisons for a device with $NF_xW_gxL_g=16x2.5x0.3$. All the Y-parameters

1. Improved test structures are under development to eliminate measurement error seen in $Real(Y_{11})$ and $Real(Y_{21})$.

match, including $Real(Y_{11})$ and $Real(Y_{12})$, whose values are now well above the dynamic range limit due to the increased channel resistance.

To investigate the effects of applying a DC bias to the deep Nwell, the test structures previously described in Figure 16.8 are measured. The first step is to ensure the measurements are accurate. This is achieved by comparing a 0V bias applied to the deep Nwell (*DNWB* test) with the hard wired ground applied to the deep Nwell (*DNWA* test). Figure 16.16 shows the comparison where the Y-parameters are the same except for slight differences in conductances due to different devices. The scale of the plot is very small, thus the differences are very small. The next step is to apply a DC bias of 3V to the deep Nwell (*DNWB3*). Figure 16.17 shows the *DNWB* vs. *DNWB3* comparison where the Y-parameters are exact (no DC difference since the measurements are performed on the same device).

TABLE 16.4 DC Measurement Conditions for S-parameter Sweeps

	VG	VD
<i>sweep 1</i>	1.8	0
<i>sweep 2</i>	0.9	1.8
<i>sweep 3</i>	1.8	1.8

16.6.4 Conclusions

The experiments performed show that the deep Nwell has no influence on the DC or RF performance of the **nfet** devices. Therefore, the MS and RF models are not altered in the presence of deep Nwell. The junction isolation effects of the deep Nwell and added terminals are modeled by the **ddnw** component as described in Section 16.2.

FIGURE 16.11 $W_g=2.5\mu\text{m}$, $L_g=0.18\mu\text{m}$, $NF=16$, $V_d=0$, $V_g=1.8\text{V}$

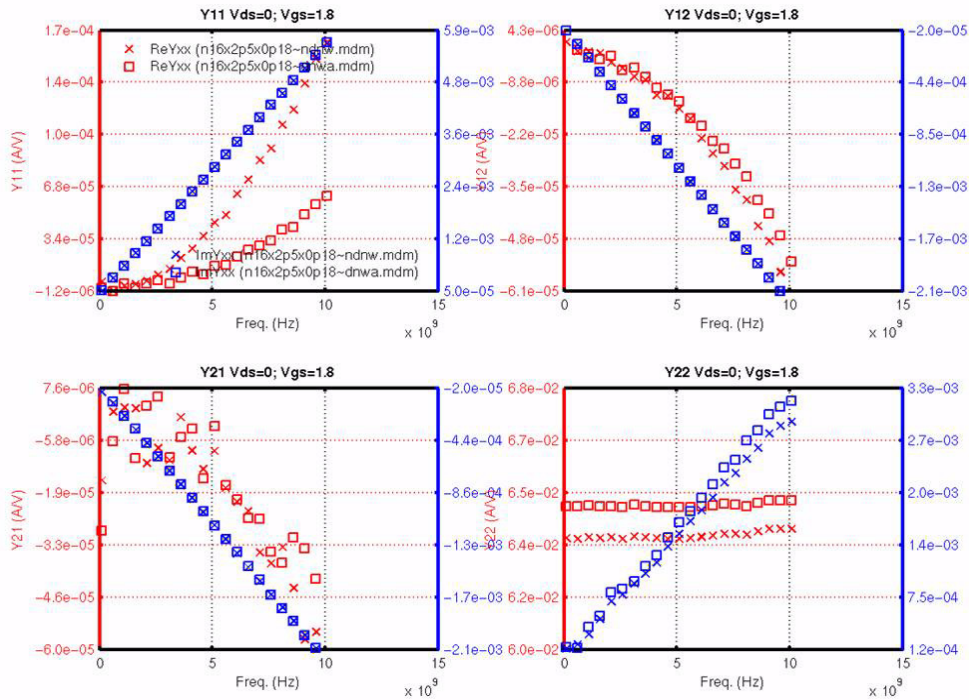


FIGURE 16.12 $W_g=2.5\mu\text{m}$, $L_g=0.18\mu\text{m}$, $NF=16$, $V_d=1.8\text{V}$, $V_g=0.9\text{V}$

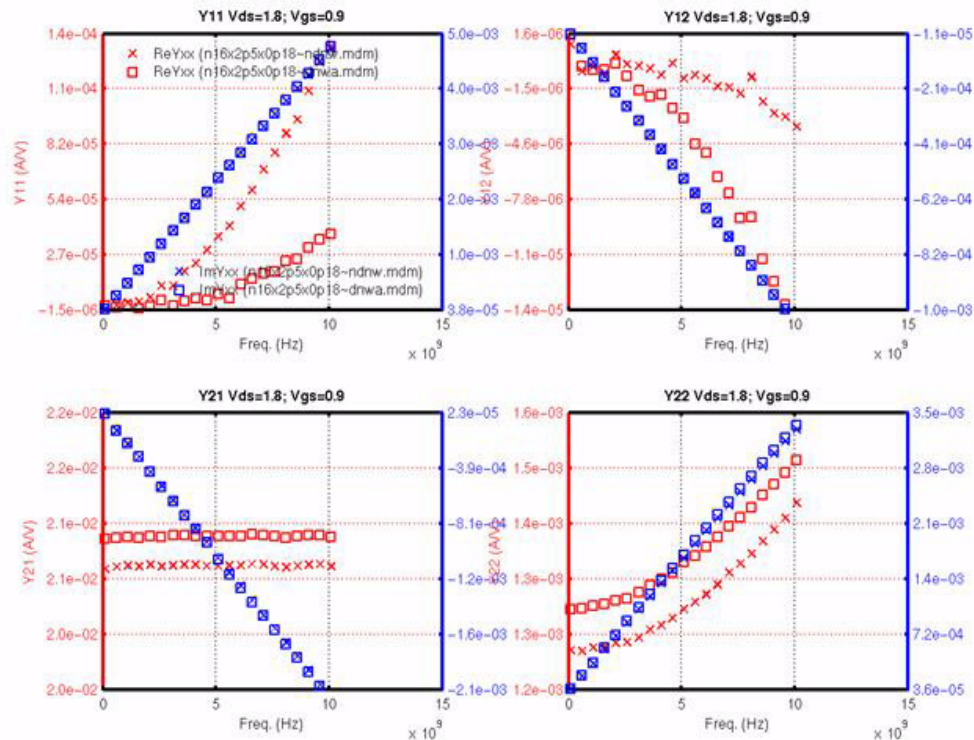


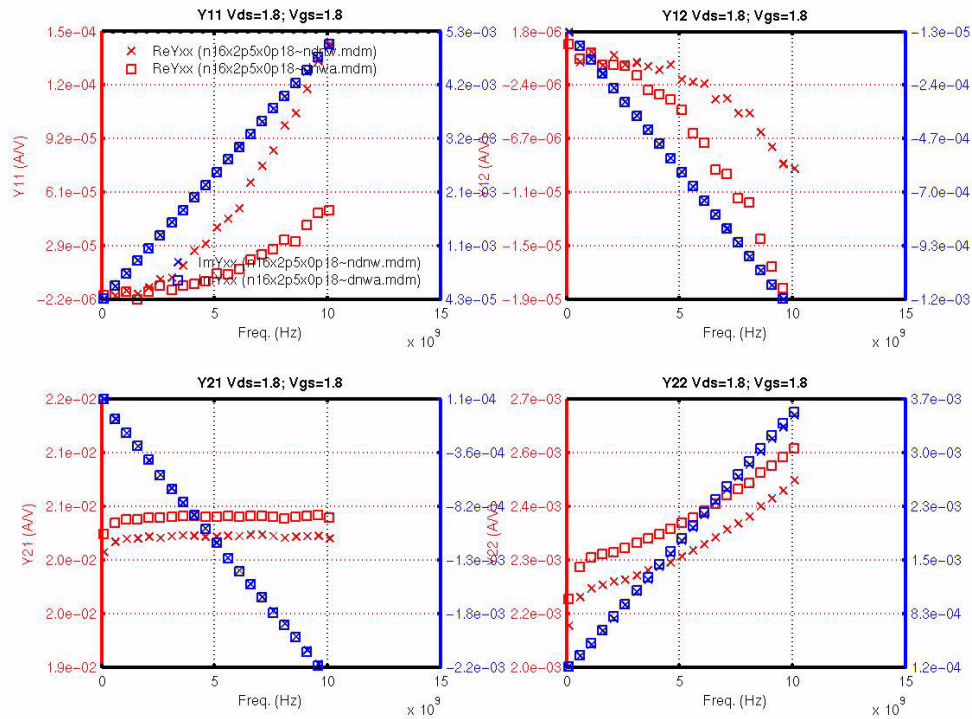
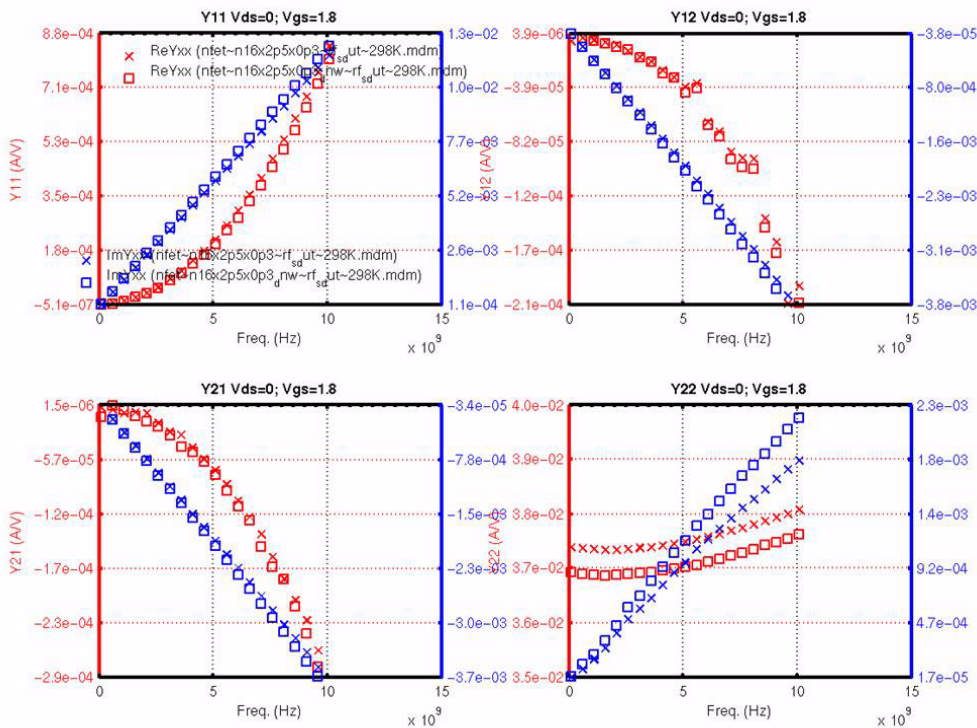
FIGURE 16.13 $W_g=2.5\mu\text{m}$, $L_g=0.18\mu\text{m}$, $NF=16$, $V_d=1.8\text{V}$, $V_g=1.8\text{V}$ FIGURE 16.14 $W_g=2.5\mu\text{m}$, $L_g=0.3\mu\text{m}$, $NF=16$, $V_d=0$, $V_g=1.8\text{V}$ 

FIGURE 16.15 $W_g=2.5\mu\text{m}$, $L_g=0.3\mu\text{m}$, $NF=16$, $V_d=1.8\text{V}$, $V_g=0.9\text{V}$

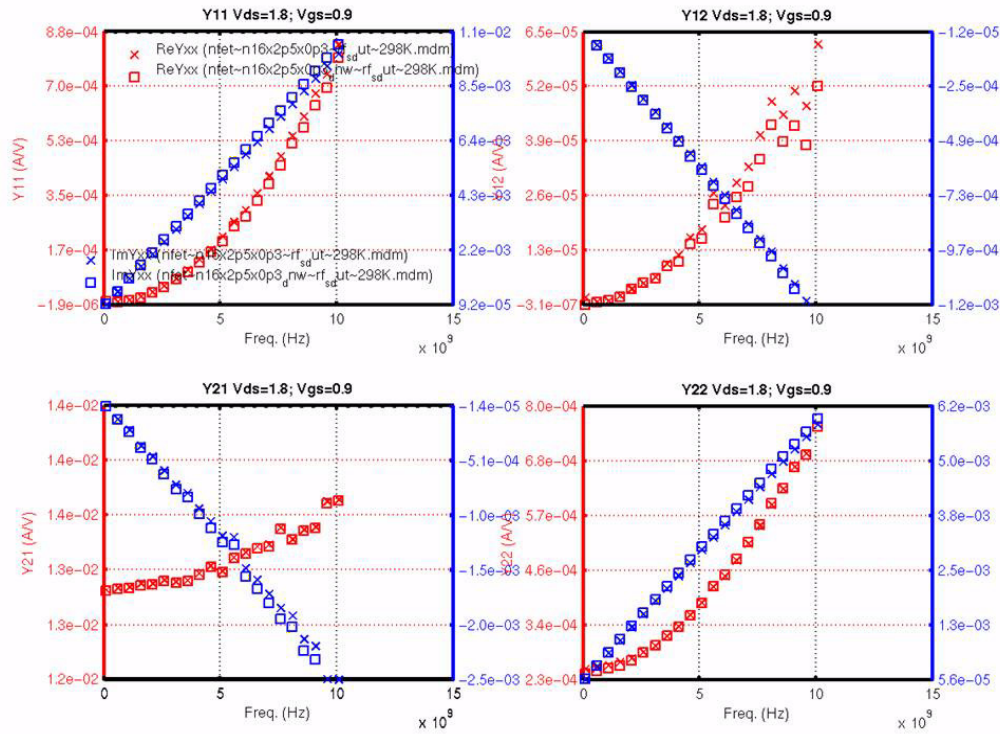


FIGURE 16.16 $W_g=2.5\mu\text{m}$, $L_g=0.3\mu\text{m}$, $NF=16$, $V_d=1.8\text{V}$, $V_g=1.8\text{V}$

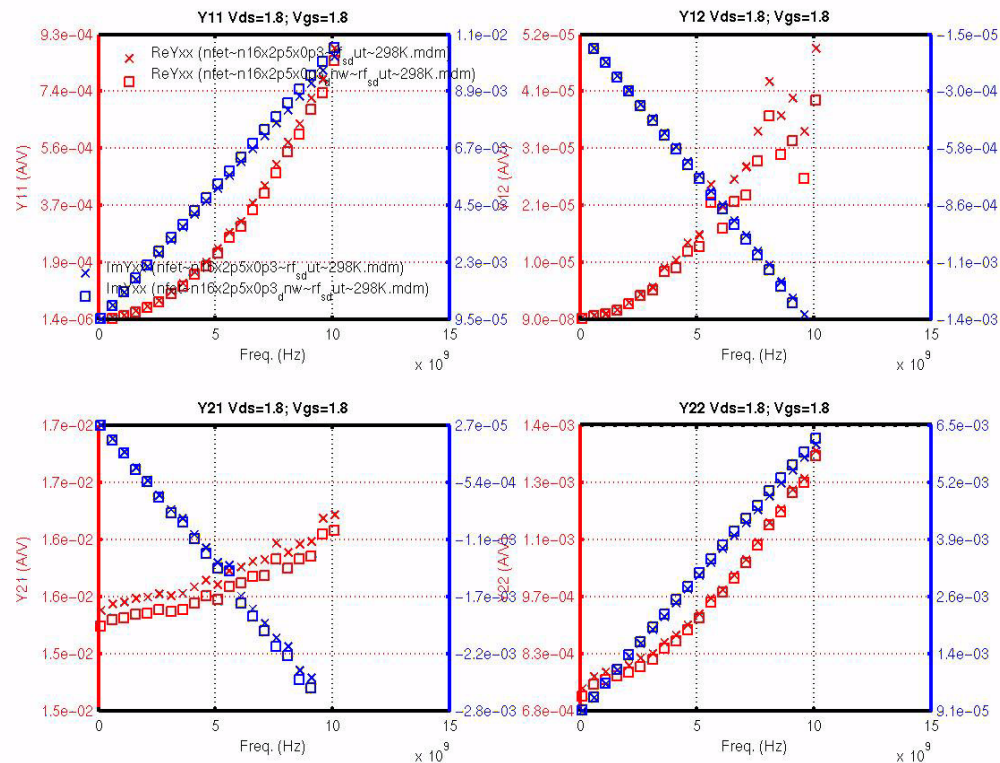
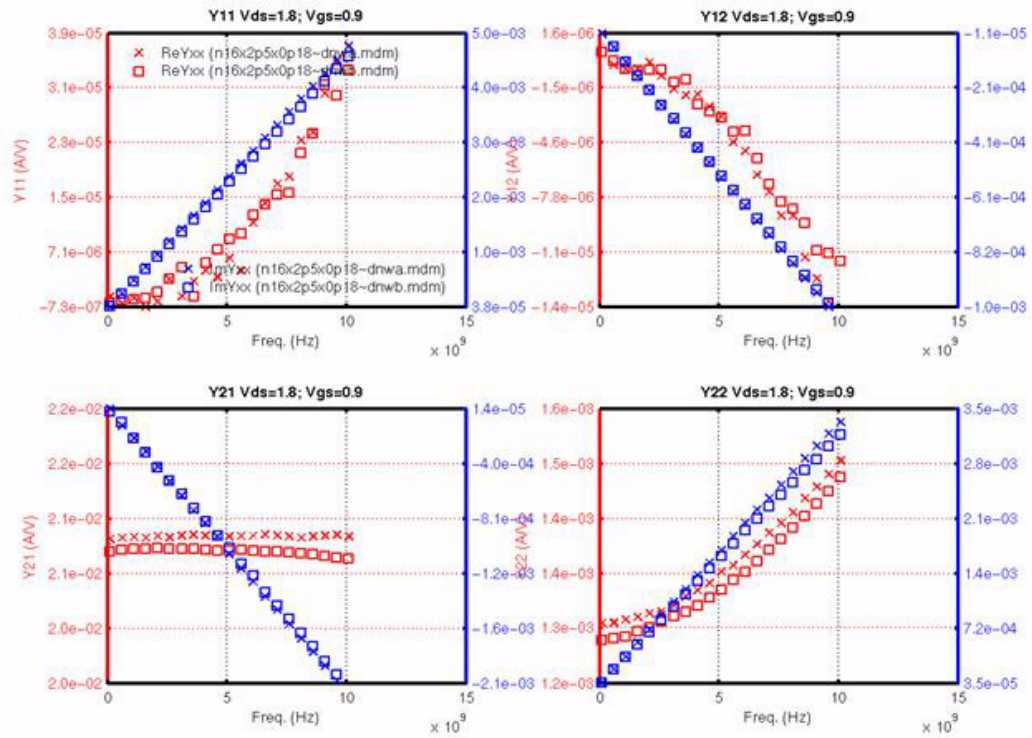
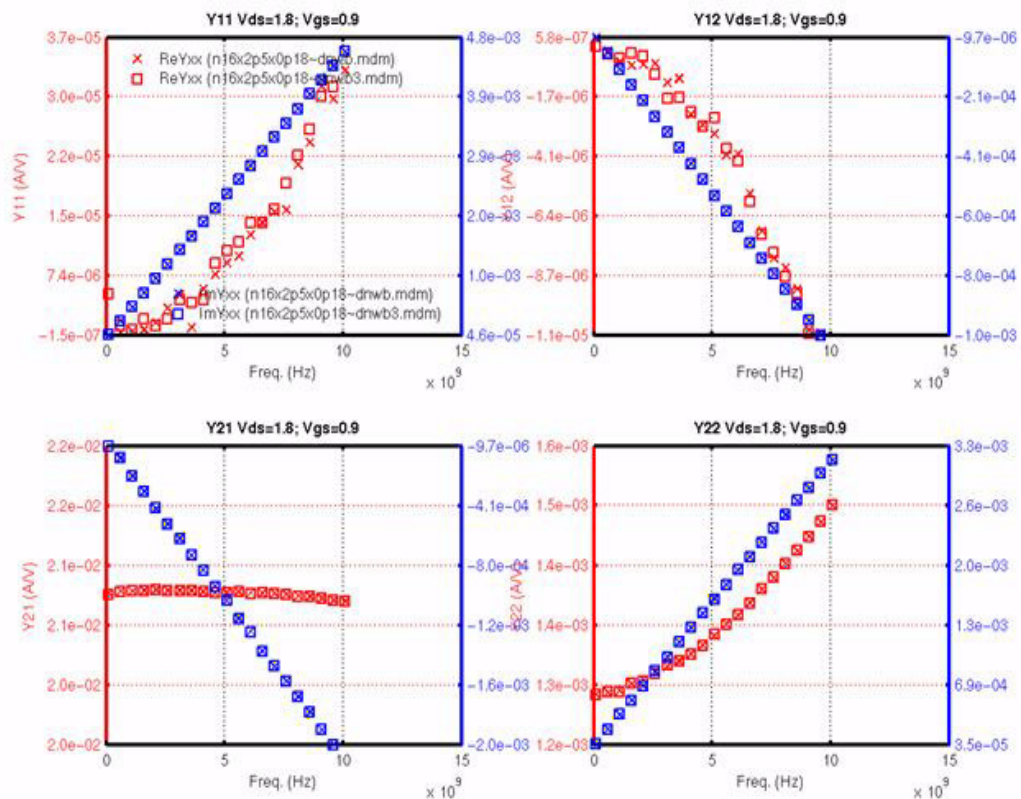


FIGURE 16.17 DNWA vs. DNWB ($W_g=2.5\mu\text{m}$, $L_g=0.18\mu\text{m}$, $NF=16$, $V_d=1.8\text{V}$, $V_g=0.9\text{V}$)FIGURE 16.18 DNWB vs. DNWB3 ($W_g=2.5\mu\text{m}$, $L_g=0.18\mu\text{m}$, $NF=16$, $V_d=1.8\text{V}$, $V_g=0.9\text{V}$)

17.0 Appendix

17.1 Layout Parasitics

Jazz supports Calibre and Assura parasitic extraction in the SBC18 design kit. Table 12.4 gives a detailed device by device breakdown of what parasitics are included in the model compared to parasitics extracted by Calibre and Assura. The handling of NPN and MOSFET parasitics has been changed in next generation (GTE) generated PDKs (released since May 2011).

TABLE 17.1 Parasitic Extraction Reference Table

Device Model	Included in Model	Included in Extraction Deck
NPN	<p>Schematic Level (postlayout flag = 0):</p> <ul style="list-style-type: none"> ✓ M1, via1, and M2 on E and C ✓ M1 on B <p>Extracted view (postlayout flag = 1)</p> <ul style="list-style-type: none"> ✓ No metal parasitics are included in the model 	<ul style="list-style-type: none"> ✓ All parasitics in model are turned-off and all metal interconnects are fully extracted
MS MOSFET	<ul style="list-style-type: none"> ✓ Source/drain area and perimeter is calculated to be shared between the fingers and also scaled based on the “current” parameter. The default source/drain size uses the minimum design rule size for the gate/source/drain. ✓ No gate or contact resistance is modeled. 	<ul style="list-style-type: none"> ✓ Gate resistance, contact resistance, etc. even in active region ✓ Each finger is extracted separately with the proper shared source/drain extraction ✓ All metal interconnect.
RF MOSFET	<p>Schematic Level (postlayout flag = 0):</p> <ul style="list-style-type: none"> ✓ Estimated all source/drain area and perimeter calculations ✓ Estimated gate poly resistance and metal interconnect over active <p>Extracted view (postlayout flag = 1)</p> <ul style="list-style-type: none"> ✓ Silicide to poly contact resistance 	<ul style="list-style-type: none"> ✓ All metal resistance ✓ All source/drain area and perimeter calculations ✓ Each gate finger is extracted separately with the proper shared source/drain extraction ✓ Silicided gate sheet resistance is divided by 3 to account for the distributed nature at RF frequencies

Device Model	Included in Model	Included in Extraction Deck
Resistors/Fuse	<ul style="list-style-type: none"> ✓ Head resistance/capacitance on poly. This is an Espec value that includes the contact resistance. Head resistance scales inversely with width because more contacts are included with a wider resistor. ✓ Body resistance/capacitance on poly. ✓ Well-to-sub resistance and diode. 	<ul style="list-style-type: none"> ✓ All metal and interconnect except contact. Contact is part of the head resistance and is NOT extracted.
MIM Capacitor (3-terminal)	<ul style="list-style-type: none"> ✓ bottom metal resistance and capacitance ✓ topmm resistance and capacitance ✓ top metal resistance including via to topmm ✓ bottom plate to substrate or well capacitance ✓ Well-to-sub resistance and diode. 	<ul style="list-style-type: none"> ✓ bottom metal access resistance (see Section 12.1.1 on page 501)
MIM Capacitor (2-terminal)	<ul style="list-style-type: none"> ✓ bottom metal resistance and capacitance ✓ topmm resistance and capacitance ✓ top metal resistance including via to topmm 	<ul style="list-style-type: none"> ✓ bottom metal access resistance (see Section 12.1.1 on page 501)
Varactor_BL/ Varactor_NI	<ul style="list-style-type: none"> ✓ All M1 and contacts on fingers ✓ fingers (nf) 	<ul style="list-style-type: none"> ✓ Number of fingers extracted and passed to the model
Varactor_MOS	<ul style="list-style-type: none"> ✓ All M1, M2, via1, poly, and contacts over device area inside Nwell ✓ fingers (nf) and slices (ns) included ✓ 1 Nwell per device which scales with w,l, ns and nf. 	<ul style="list-style-type: none"> ✓ nf and ns extracted and passed to the model ✓ metal interconnect of end regions connecting up fingers outside of Nwell
Inductor/Balun	<ul style="list-style-type: none"> ✓ All metal parasitics 	<ul style="list-style-type: none"> ✓ Any interconnect outside of the inductor marking layer LCELL ✓ Connection metal not included with pcell but drawn on LCELL is ignored.
VPNP/LPNP/Schottky	<ul style="list-style-type: none"> ✓ No metal or contact parasitics 	<ul style="list-style-type: none"> ✓ All metal interconnect ✓ All contact resistance

17.2 F_T Simulation Test Bench

The RF MOSFET and NPN chapters in this document show plots of the cut-off frequency (F_T) plotted against the drain and collector currents, respectively. The F_T of a device is the frequency at which the ac current gain (h_{21}) reduces to unity. The peak F_T of a device can range from tens of GHz for high-voltage MOSFETs to 200 GHz for high-performance NPNs. Due to measurement inaccuracies at these high frequencies, F_T is extracted from h_{21} measurements at lower frequencies (1-20 GHz) and then extrapolated assuming a 20dB/decade slope. This allows a quick spot frequency measurement of F_T , and has been shown to be accurate for most cases. The simulated F_T , shown in the model playback sections of the RF MOSFET and NPN chapters is extracted in a manner consistent with the measurement set-up. The test-bench is schematically illustrated in Figure 17.1. A bias-T network is used to isolate the DC and AC signals to PORT1 (Gate or Base) and PORT2 (Drain or Collector). The collector voltage is either fixed (constant V_{CE}) or synchronized with the base (constant V_{CB}). The F_T vs. I_C plots in the NPN chapter use a constant V_{CE} biasing scheme, while the F_T E-spec. for the NPNs is extracted at a fixed $V_{CB}=1V$. The A 2-port s-parameter simulation is performed at a spot frequency (f_{spot}) for a series of gate or base biases. The s-parameters are converted to h-parameters, and the F_T is extracted as:

$$F_T = abs(h_{21}) \times f_{spot} \quad (EQ 1)$$

The extracted F_T is then plotted against the drain or collector current. The f_{spot} is chosen so as to be after the 3dB roll-off point on the h_{21} vs. frequency curve and is specified in Table 17.2.

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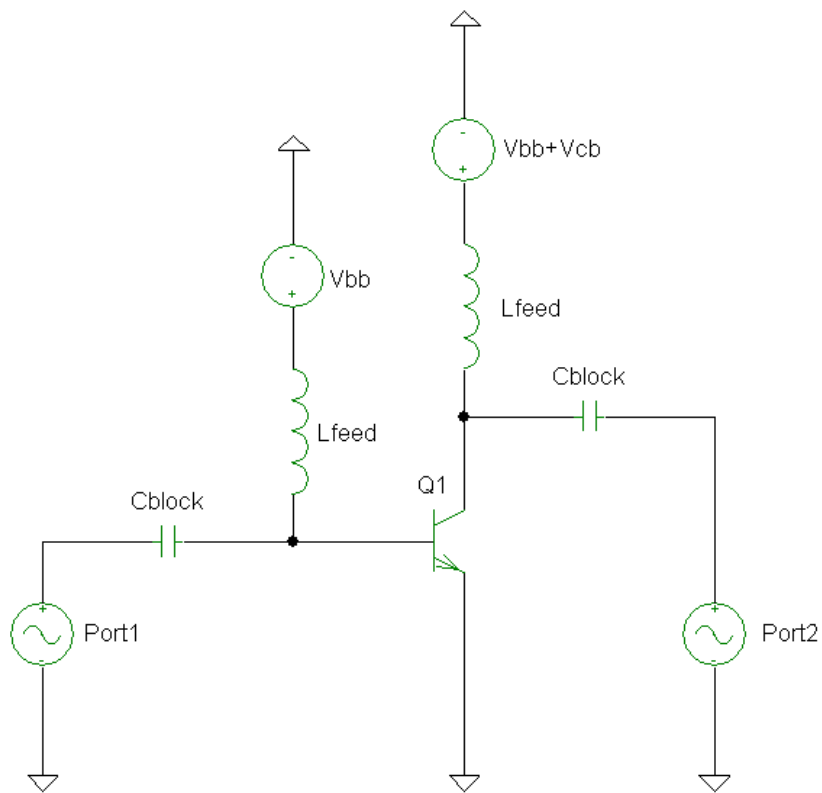
FIGURE 17.1 F_T simulation test-bench

TABLE 17.2 Spot frequency specification for various devices in the sbc18 process family

Variant	Device	Spot Freq. (GHz)
SBC18	HS NPN	10
	Std. NPN	3
	HV NPN	1
SBC18H2, H3	LV NPN	15
	MV NPN	5
All	All FETs	3