PREPARED BY: **Paul Hurwitz**	**Jazz Semiconductor.** 4321 Jamboree Road, Newport Beach, CA 92660-3095	DOCUMENT NUMBER: **NPB-PS-0267**
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TITLE:

ELECTRICAL PARAMETERS OF THE SBC18 PROCESS FAMILY

REV	REVISION DESCRIPTION (for last two years)	DATE
10	Updated MOS varactor specifications in Section 6.11.3; Clarified metal fuse resistance specifications (0.4 ohm actual versus 4.5 ohm measured, the latter including parasitic probe resistance)	04/01/04
11	Removed SBC18PTX process; Updated 10x10 3.3V NFET VT specs in Section 4.1; Updated 10x10 1.8VPFET Transconductance in Section 4.3; Updated Body constants in Section 4.6 Added specifications for 0.6x10.16 and 0.9x10.16 NPNs in Section 6.1.1; Updated Fmax specifications for 0.2x10.16 NPNs in Section 6.1.1; Added temperature coefficient of resistance specifications for resistors in Sections 6.2 to 6.6	08/02/04
12	Updated Kf for 1/f noise of Lateral PNP to 1.4e-11 from 2.4e-12 in Section 6.13.1; Added metal fuse resistance after blowing in Section 6.12.1; Added Section 6.16 on polyimide overcoat Tighten Specifications for thin and thick gate oxide in Section 3.2	06/15/05
13	Added SBC18HA process variant; Added schottky diode to SBC18HXL; Absolute Max Bias on stacked MIM capacitor changed from 3.6 to 5V in Section 6.9; Updated NPN specifications in Section 6.6.1 as follows: (a) Removed Rb specifications (b) Updated Ccs specifications for 0.9 x10.16 devices (c) updated Fmax nominal values and removed the corners for 10.16um (long) devices; Increased Q values of varactors in Section 6.11.1 based upon improved measurements	03/15/06

14	Clarify Max Voltage rating table 5.1.2 Define passivation stack for SBC18MVZ in 6.18.1 Section 3.2 – Correct TM to M3 oxide thickness Section 3.3 – Small correction to metal thickness for SBC18QTD, SBC18MW. Change TM, TM2 thickness. Add illustrated cross sections. Section 4 – Updated narrow FET electrical specifications: Min L,W 1.8V Pfet Vt and body constant, Idsat for min W devices. Section 4.14 – Add breakdown voltage of 2.8fF/um2 MIM capacitor. Section 4.15 – Change TM, TM2 sheet resistance. Section 4.18 – Correct M4-to-TM via resistance for SBC18HX	05/04/07
15	Added SBC18QTE,SBC18PTA process variant.	06/29/07
16	Added SBC18HKL process variant	07/27/07
17	Various small CMOS, NPN, LPNP spec adjustments to align with volume manufacturing statistical data. Attachment includes a table with the rev17 changes:	09/08/08

TABLE OF CONTENTS

1. PURPOSE AND SCOPE

This document covers both process parameters and device parameters for the SBC18 family of processes. The specifications shown in this document are intended to reflect the mean and ± 3 sigma variation of parameters at 25°C unless otherwise specified.

1.1. Description of Processes

The SBC18HX process has six layers of aluminium metal. It supports (a) both 1.8V and 3.3V FETs (b) high speed, standard and high voltage NPNs with deep trench (c) metal, low value unsilicided poly, silicided poly, and nwell resistors (d) 1fF/um^2 MIM capacitor on Metal 4 (e) high performance junction varactor and (f) inductors using 2.8um thick aluminium top metal layer (metal 6) and 2um thick top via layer (Via 5). The metal resistor is between metal 3 and metal 4. The MIM capacitor is between metal 4 and metal 5. The via4 is 2um in height and metal 5 is 1.6um thick aluminium.

The SBC18HXL process is identical to the SBC18HX process with the addition of a deep nwell mask to support triple well process for NFETs. It also supports schottky diodes.

The SBC18HKL process is identical to SBC18HXL with the following exceptions: SBC18HKL does not support the high performance junction varactor nor the high speed NPN HBT.

SBC18HA is a variant of HXL with (a) addition of high value poly resistor and (b) different MIM cap specifications of 2.8fF/um^2 single and 5.6fF/um^2 stacked MIM capacitors.

The SBC18PT process has five layers of aluminium metal. It supports (a) both 1.8V and 3.3V FETs (b) standard and high voltage NPNs without deep trench (c) high value unsilicided poly, low value unsilicided poly, silicided poly, and nwell resistors (d) 2fF/um^2 MIM capacitor on Metal 2 and 4fF/um^2 stacked MIM capacitor on Metal 2 and Metal 3 (e) high performance junction varactor and (f) inductors using 5.2um thick aluminium top metal layer (metal 5) and 2um thick top via layer (Via 4). The MIM capacitor is between metal 2 and metal 3. The via3 is 2um in height and metal 4 is 1.6um thick aluminium.

The SBC18QTD process has four layers of aluminum metal. It supports (a) 3.3V FETs only (b) standard and high voltage NPNs with deep trench (c) high value unsilicided poly, low value unsilicided poly, silicided poly, and nwell resistors (d) 2fF/um^2 MIM capacitor on Metal 2 (e) high performance junction varactor and (f) inductors using 5.2um thick Aluminum top metal layer (metal 4), 3um thick top via layer (Via 3). The MIM capacitor is between metal 2 and metal 3.

The SBC18QTR process is identical to the SBC18QTD process with the additions of (a) metal resistor between metal-1 and metal-2 and (b) Schottky diode.

The SBC18QTL process is identical to SBC18QTD process with the addition of a deep nwell mask to support triple well process for NFETs.

The SBC18QW process has four layers of aluminum metal. It supports (a) 3.3V FETs only (b) standard and high voltage NPNs without deep trench (c) high value unsilicided poly, low value unsilicided poly, silicided poly, and nwell resistors (d) 2fF/um^2 MIM capacitor on Metal 2 and 4fF/um^2 stacked MIM capacitor on Metal 2 and Metal 3 (e) p+/nwell junction varactor and (f) inductors using 2.8um thick Aluminum top metal layer (metal 4), 2um thick top via layer (Via 3). The MIM capacitor is between metal 2 and metal 3.

The SBC18MW process has three layers of aluminium metal. It supports (a) 3.3V FETs only (b) standard and high voltage NPNs without deep trench (c) high value unsilicided poly, low value unsilicided poly, silicided poly, and nwell resistors (d) 2fF/um^2 MIM capacitor on Metal 2 (e) p+/nwell junction varactor and (f) inductors using 2.8um thick Aluminum top metal layer (metal 3), 2um thick top via layer (Via 2). The MIM capacitor is between metal 2 and metal 3.

SBC18MWD process is the SBC18MW process with (a) the standard and high voltage NPNs having the deep trench and (b) the p+/nwell junction varactor replaced with the high performance junction varactor.

SBC18MV process is the SBC18MW process with the p+/nwell junction varactor replaced with the high performance junction varactor

The SBC18QTE process is identical to the SBC18QTD process with the addition of the High Speed NPN Device.

The SBCPTA process is identical to SB18PTH process without the HV Resistor and BL Varactor

The look-up tables below distinguish the various processes described above. Only typical values are provided in this summary

Table 1.1 : Front end process differentiators

	1.8V FET	3.3V FET	Nat-ive FET	Deep N Well for triple well isolation	Deep Trench Process	HS NPN*	Varactor type (bl, ni, or MOS)	High value poly resistor **	Schottky Diode
SBC18HX	Yes	Yes	No	No	Yes	Yes	Bl, MOS	No	No
SBC18HXL	Yes	Yes	No	Yes	Yes	Yes	Bl, MOS	No	Yes
SBC18HKL	Yes	Yes	No	Yes	Yes	No	MOS	No	Yes
SBC18HA	Yes	Yes	No	Yes	Yes	Yes	Bl, MOS	Yes	Yes
SBC18PT	Yes	Yes	No	No	No	No	Bl, MOS	Yes	No
SBC18PTA	Yes	Yes	No	No	No	No	MOS	No	No
SBC18QTD	No	Yes	No	No	Yes	No	Bl	Yes	No
SBC18QTR	No	Yes	No	No	Yes	No	Bl	Yes	Yes
SBC18QTL	No	Yes	No	Yes	Yes	No	Bl	Yes	No
SBC18QW	No	Yes	No	No	No	No	Ni	Yes	No
SBC18QTE	No	Yes	No	No	Yes	Yes	Bl	Yes	No
SBC18MW	No	Yes	No	No	No	No	ni	Yes	No
SBC18MWD	No	Yes	No	No	Yes	No	bl	Yes	No
SBC18MV	No	Yes	No	No	No	No	bl	Yes	No

* Standard and high voltage NPNs are available for all processes
** Silicided poly resistors, low value unsilicided poly resistors and nwell resistors are available for all processes

Table 1.2 : Back end process differentiators

	No. of metal layers	MIM cap	Stacked MIM cap	Metal resistor	MT thickness/ VT height*	MT-1 thickness / VT-1 height
SBC18HX	6	1fF between M4/M5	No	Yes	2.8um/ 2.0um	1.6um/ 2.0um
SBC18HXL SBC18HKL	6	1fF between M4/M5	No	Yes	2.8um/ 2.0um	1.6um/ 2.0um
SBC18HA	6	2.8fF between M4/M5	Yes***	Yes	2.8um/ 2.0um	1.6um/ 2.0um
SBC18PT	5	2fF between M2/M3	Yes**	No	5.2um/ 2.0um	1.6um/ 2.0um
SBC18PTA	5	2fF between M2/M3	Yes**	No	5.2um/ 2.0um	1.6um/ 2.0um
SBC18QTD	4	2fF between M2/M3	No	No	5.2um/ 3.0um	0.635um/0.95um
SBC18QTR	4	2fF between M2/M3	No	Yes	5.2um/ 3.0um	0.635um/0.95um
SBC18QTL	4	2fF between M2/M3	No	No	5.2um/ 3.0um	0.635um/0.95um
SBC18QW	4	2fF between M2/M3	Yes**	No	2.8um/ 2.0um	0.635um/0.95um
SBC18QTE	4	2fF between M2/M3	No	No	5.2um/ 3.0um	0.635um/0.95um
SBC18MW	3	2fF between M2/M3	No	No	2.8um/ 2.0um	0.635um/0.95um
SBC18MWD	3	2fF between M2/M3	No	No	2.8um/ 2.0um	0.635um/0.95um
SBC18MV	3	2fF between M2/M3	No	No	2.8um/ 2.0um	0.635um/0.95um

* MT = topmost metal; VT = topmost via
** Stacked capacitor density is 2 + 2 = 4fF/um2 between M2/M3/M4
*** Stacked capacitor density is 2.8+2.8 = 5.6fF/um2 between M3/M4/M5

Note: Process names which end with letter “Z” have polyimide overcoats

2. APPLICABLE DOCUMENTS

SBC18 Electrical Specification	NPB-PS-0267
SBC18 Analog Characterization Report	NPB- PS 0392
SBC18 Design Manual	NPB-PS-0288
Digital Design Manual	NPB PS-0402
Spice Data Bank	NPB-PS-0268

3. PROCESS PARAMETERS

3.1. Substrate

P type bulk wafer, crystal orientation (100)

Description	Min.	Nom.	Max.	Units
Resistivity of p- bulk	6	8	10	Ω-cm

3.2. Dielectric Thicknesses (final thickness)

Description	Min.	Nom.	Max.	Units
For SBC18HX, HXL, HKL, HA, PT,PTA only				
Gate Oxide-thin (measured by ellipsometer)	24.5	26	27.5	Angstroms
Electrical Gate Oxide-thin (for NFET at -3.3V) [@ -3V]	35 [37.5]	36.5 [39]	38 [40.5]	Angstroms
Electrical Gate Oxide-thin (for PFET at +3.3V) [@ +3V]	33.5 [35.5]	35 [37]	36.5 [38.5]	Angstroms
Electrical Gate Oxide-thin (for NFET at +1.8V)	39.5	41	42.5	Angstroms
Electrical Gate Oxide-thin (for PFET at -1.8V)	39.5	41	42.5	Angstroms
N+Poly/Nwell Gate Oxide-thin (at +1.8V)	39.5	41	42.5	Angstroms
For SBC18HX, HXL, HKL, HA PT,PTA, QTD, QTR, QTL, QW, MW, MV, MWD,QTE only				
Gate Oxide-thick (measured by ellipsometer)	54	57	60	Angstroms
Electrical Gate Oxide-thick (for NFET at -5.0V; for PFET at +5.0V)	62	65	68	Angstroms
Electrical Gate Oxide-thick (for NFET at +3.3V)	66	69	72	Angstroms
Electrical Gate Oxide-thick (for PFET at -3.3V)	66	69	72	Angstroms
N+Poly/Nwell Gate Oxide-thick (at +3.3V)	67	70	73	Angstroms

Description (for all SBC18 processes)	Min.	Nom.	Max.	Units
SiGe poly base to substrate (silicon under STI)	2.1	2.8	3.5	Kangstroms
Poly to substrate (silicon under STI)	2.1	2.8	3.5	Kangstroms
Metal 1 to poly 1	4.5	6.5	8.5	Kangstroms
Metal 1 to diffusion	6.6	8.6	10.6	Kangstroms
Metal 1 to Emitter Poly	0.5	2.6	4.7	Kangstroms
Metal 1 to collector sinker	6.6	8.6	10.6	Kangstroms
Metal 1 to substrate (silicon under STI)	9.3	11.4	13.5	Kangstroms
Metal 2 to metal 1	5.5	8.0	10.5	Kangstroms
Metal 2 to poly 1	16.4	19.7	23.0	Kangstroms
Metal 2 to diffusion	18.5	21.8	25.1	Kangstroms
Metal 2 to substrate (silicon under STI)	21.2	24.6	28.0	Kangstroms
Overcoat oxide * For SBC18HX, HXL, HKL, HA, QW, MW, MV, MWD only	1.80	2.00	2.20	Kangstroms
Overcoat nitride * For SBC18HX, HXL, HKL, HA, QW, MW, MV, MWD only	5.40	6.00	6.60	Kangstroms
Overcoat oxide * For SBC18PT,PTA, QTD,QTE, QTR, QTL only	3.60	4.00	4.40	Kangstroms
Overcoat nitride * For SBC18PT,PTA, QTD,QTE, QTR, QTL only	10.8	12.0	13.2	Kangstroms

* The thicknesses of the conformally deposited overcoat oxide and overcoat nitride at the sidewall of the top metal layer are about 70% of the thickness at the top of the topmost metallization layer. The gap between two adjacent metal lines at the topmost metallization layer, remaining beyond the sidewall overcoat dielectrics, is typically filled by resins used in packaging.

Note: 1) Depth of STI trench is difference between “Metal 1 to silicon under field” and “Metal 1 to diffusion” thicknesses

Description – applicable to SBC18MW, SBC18MV, SBC18MWD only				
Top capacitor plate TM to metal2 (nitride)	285	335	385	Angstroms
Top capacitor plate TM to metal 3 (oxide)	13.415	17.665	21.915	Kangstroms
Metal 3 to metal 2	16.0	20.0	24.0	Kangstroms
Metal 3 to metal 1	29.6	34.4	39.1	Kangstroms
Metal 3 to poly 1	40.8	46.1	51.3	Kangstroms
Metal 3 to diffusion	42.9	48.2	53.4	Kangstroms
Metal 3 to substrate (silicon under STI)	45.7	51.0	56.2	Kangstroms

Description – applicable to SBC18QW only				
Top capacitor plate TM to metal2 (nitride)	285	335	385	Angstroms
Top capacitor plate TM to metal 3 (oxide)	4.415	7.165	9.915	Kangstroms
Metal 3 to metal 2	7.0	9.5	12.0	Kangstroms
Metal 3 to metal 1	20.2	23.9	27.5	Kangstroms
Metal 3 to poly 1	31.3	35.6	39.8	Kangstroms
Metal 3 to diffusion	33.4	37.7	41.9	Kangstroms
Metal 3 to substrate (silicon under STI)	36.2	40.5	44.7	Kangstroms
Top capacitor plate TM2 to metal3 (nitride)	285	335	385	Angstroms
Top capacitor plate TM2 to metal 4 (oxide)	13.715	17.665	21.615	Kangstroms
Metal 4 to metal 3	16.0	20.0	24.0	Kangstroms
Metal 4 to metal 2	31.1	35.9	40.6	Kangstroms
Metal 4 to metal 1	44.7	50.2	55.7	Kangstroms
Metal 4 to poly 1	56.0	61.9	67.8	Kangstroms
Metal 4 to diffusion	58.1	64.0	69.9	Kangstroms
Metal 4 to substrate (silicon under STI)	60.9	66.8	72.7	Kangstroms
Description – applicable to SBC18QTD, SBC18QTE,SBC18QTR, SBC18QTL only				
Top capacitor plate TM to metal2 (nitride)	285	335	385	Angstroms
Top capacitor plate TM to metal 3 (oxide)	4.415	7.165	9.915	Kangstroms
Metal 3 to metal 2	7.0	9.5	12.0	Kangstroms
Metal 3 to metal 1	20.2	23.9	27.5	Kangstroms
Metal 3 to poly 1	31.3	35.6	39.8	Kangstroms
Metal 3 to diffusion	33.4	37.7	41.9	Kangstroms
Metal 3 to substrate (silicon under STI)	36.2	40.5	44.7	Kangstroms
Metal 4 to metal 3	26.0	30.0	34.0	Kangstroms
Metal 4 to metal 2	41.1	45.9	50.6	Kangstroms
Metal 4 to metal 1	54.7	60.2	65.7	Kangstroms
Metal 4 to poly 1	66.0	71.9	77.8	Kangstroms
Metal 4 to diffusion	68.1	74.0	79.9	Kangstroms
Metal 4 to substrate (silicon under STI)	70.9	76.8	82.7	Kangstroms
Description – applicable to SBC18QTR only				
Metal resistor plate TR to poly 1	10.5	13.0	15.5	Kangstroms
Metal resistor plate TR to Metal 2	3.7	6.2	8.7	Kangstroms
Metal resistor plate TR to substrate (silicon under STI)	15.3	17.9	20.5	Kangstroms

Description – applicable to SBC18PT,PTA only	Min.	Nom.	Max.	Units
Top capacitor plate TM to metal2 (nitride)	285	335	385	Angstroms
Top capacitor plate TM to metal 3 (oxide)	3.165	5.665	8.165	Kangstroms
Metal 3 to metal 2	5.5	8.0	10.5	Kangstroms
Metal 3 to metal 1	17.6	21.2	24.8	Kangstroms
Metal 3 to poly 1	28.7	32.9	37.1	Kangstroms
Metal 3 to diffusion	30.8	35.0	39.2	Kangstroms
Metal 3 to substrate (silicon under STI)	33.5	37.8	42.1	Kangstroms
Stacked top capacitor plate TM2 to metal3 (nitride)	285	335	385	Angstroms
Stacked top capacitor plate TM2 to metal 4 (oxide)	13.415	17.665	21.915	Kangstroms
Metal 4 to metal 3	16.0	20.0	24.0	Kangstroms
Metal 4 to metal 2	28.4	33.2	38.0	Kangstroms
Metal 4 to metal 1	40.9	46.4	51.9	Kangstroms
Metal 4 to poly 1	52.2	58.1	64.0	Kangstroms
Metal 4 to diffusion	54.3	60.2	66.1	Kangstroms
Metal 4 to substrate (silicon under STI)	57.1	63.0	68.9	Kangstroms
Metal 5 to metal 4	16.0	20.0	24.0	Kangstroms
Metal 5 to metal 3	49.6	55.9	62.2	Kangstroms
Metal 5 to metal 2	62.3	69.1	75.9	Kangstroms
Metal 5 to metal 1	75.0	82.3	89.6	Kangstroms
Metal 5 to poly 1	86.4	94.0	101.6	Kangstroms
Metal 5 to diffusion	88.5	96.1	103.7	Kangstroms
Metal 5 to substrate (silicon under STI)	91.3	98.9	106.5	Kangstroms

Description – applicable to SBC18HX, SBC18HXL, SBC18HKL, SBC18HA only	**Min.**	**Nom.**	**Max.**	**Units**
Metal 3 to metal 2	5.5	8.0	10.5	Kangstroms
Metal 3 to metal 1	17.6	21.2	24.8	Kangstroms
Metal 3 to poly 1	28.7	32.9	37.1	Kangstroms
Metal 3 to diffusion	30.8	35.0	39.2	Kangstroms
Metal 3 to substrate (silicon under STI)	33.5	37.8	42.1	Kangstroms
Metal resistor plate TR to metal 2	12.0	14.5	17.0	Kangstroms
Metal resistor plate TR to metal 4	3.7	6.2	8.7	Kangstroms
Metal resistor plate TR to substrate (silicon under STI)	39.9	44.2	48.5	Kangstroms
Metal 4 to metal 3	5.5	8.0	10.5	Kangstroms
Top capacitor plate TM2 to metal 3 (nitride) – SBC18HA only	225	250	275	Angstroms
Top capacitor plate TM2 to metal 4 (oxide) – SBC18HA only	3.7	6.2	8.7	Kangstroms
Metal 4 to metal 2	17.6	21.2	24.8	Kangstroms
Metal 4 to metal 1	29.9	34.4	38.9	Kangstroms
Metal 4 to poly 1	41.1	46.1	51.1	Kangstroms
Metal 4 to diffusion	43.2	48.2	53.2	Kangstroms
Metal 4 to substrate (silicon under STI)	46.0	51.0	56.0	Kangstroms
Top capacitor plate TM to metal4 (nitride) – SBC18HX, SBC18HXL, SBC18HKL only	540	600	660	Angstroms
Top capacitor plate TM to metal4 (nitride) – SBC18HA only	225	250	275	Angstroms
Top capacitor plate TM to metal 5 (oxide)	13.4	17.4	21.4	Kangstroms
Metal 5 to metal 4	16.0	20.0	24.0	Kangstroms
Metal 5 to metal 3	29.4	34.2	39.0	Kangstroms

Metal 5 to metal 2	41.9	47.4	52.9	Kangstroms
Metal 5 to metal 1	54.5	60.6	66.7	Kangstroms
Metal 5 to poly 1	65.9	72.3	78.7	Kangstroms
Metal 5 to diffusion	68.0	74.4	80.8	Kangstroms
Metal 5 to substrate (silicon under STI)	70.7	77.2	83.7	Kangstroms
Metal 6 to metal 5	16.0	20.0	24.0	Kangstroms
Metal 6 to metal 4	49.6	55.9	62.2	Kangstroms
Metal 6 to metal 3	63.3	70.1	76.9	Kangstroms
Metal 6 to metal 2	76.5	83.3	90.1	Kangstroms
Metal 6 to metal 1	89.2	96.5	103.8	Kangstroms
Metal 6 to poly 1	100.2	108.2	116.2	Kangstroms
Metal 6 to diffusion	102.3	110.3	118.3	Kangstroms
Metal 6 to substrate (silicon under STI)	105.0	113.1	121.2	Kangstroms

3.3. Conductor Thicknesses (final thicknesses)

Description (applicable to SBC18HX, SBC18HXL, SBC18HKL, SBC18HA only)	Min.	Nom.	Max.	Units
Poly 1 (including polycide)	1850	2100	2350	Angstroms
Top capacitor plate TM	2400	2600	2800	Angstroms
Top capacitor plate TM2 (SBC18HA only)	2400	2600	2800	Angstroms
Metal 1, Metal 2, Metal 3	4400	5200	6000	Angstroms
Metal 4	5400	6200	7000	Angstroms
Metal 5	13200	15900	18600	Angstroms
Metal 6	25100	28100	31100	Angstroms

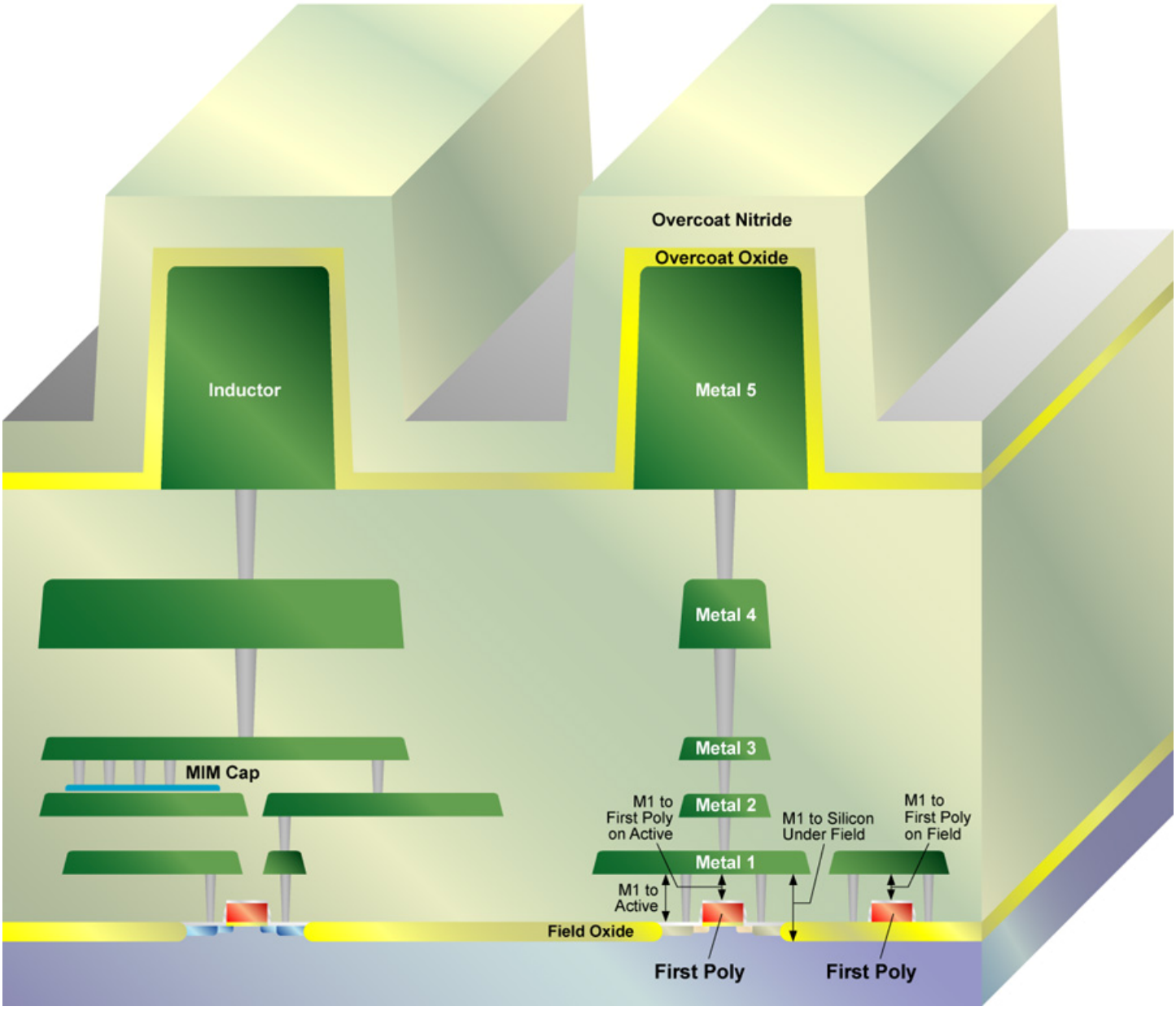
Description (applicable to SBC18PT,PTA only)	Min.	Nom.	Max.	Units
Poly 1 (including polycide)	1850	2100	2350	Angstroms
Top capacitor plates TM, TM2	2400	2600	2800	Angstroms
Metal 1, Metal 2, Metal 3	4400	5200	6000	Angstroms
Metal 4	13200	15900	18600	Angstroms
Metal 5	46800	52600	58400	Angstroms

Description – Applicable to SBC18QTD, SBC18QTE,SBC18QTR, SBC18QTL only	Min.	Nom.	Max.	Units
Poly 1 (including polycide)	1850	2100	2350	Angstroms
Top capacitor plate TM	2400	2600	2800	Angstroms
Metal 1	4400	5200	6000	Angstroms
Metal 2, Metal 3	5400	6200	7000	Angstroms
Metal 4	46800	52600	58400	Angstroms

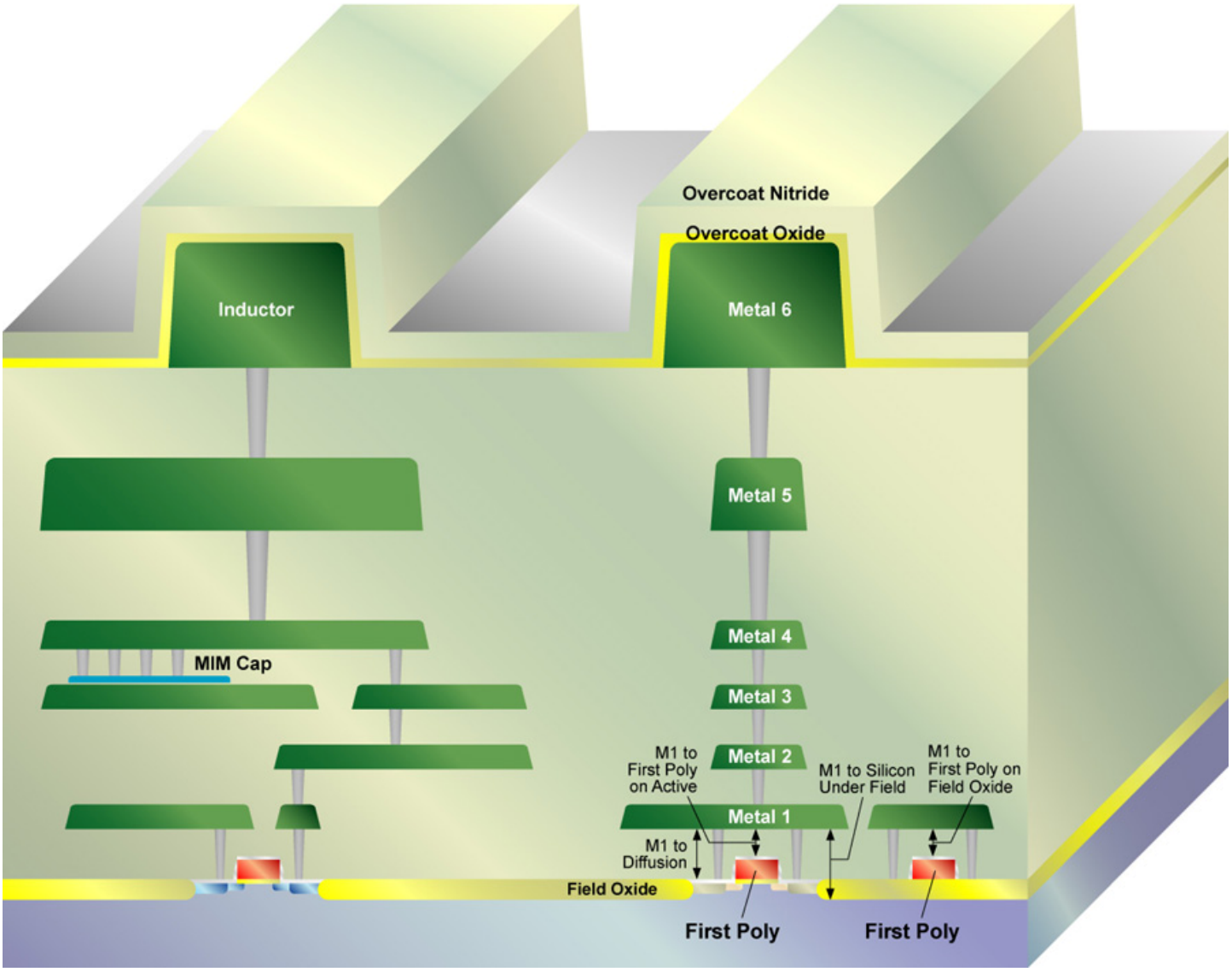
Description – Applicable to SBC18QW only	**Min.**	**Nom.**	**Max.**	**Units**
Poly 1 (including polycide)	1850	2100	2350	Angstroms
Top capacitor plates TM, TM2	2400	2600	2800	Angstroms
Metal 1	4400	5200	6000	Angstroms
Metal 2, Metal 3	5400	6200	7000	Angstroms
Metal 4	25100	28100	31100	Angstroms

Description – Applicable to SBC18MW, SBC18MV, SBC18MWD only	**Min.**	**Nom.**	**Max.**	**Units**
Poly 1 (including polycide)	1850	2100	2350	Angstroms
Top capacitor plate TM	2400	2600	2800	Angstroms
Metal 1	4400	5200	6000	Angstroms
Metal 2	5400	6200	7000	Angstroms
Metal 3	25100	28100	31100	Angstroms

SBC18PT*



SBC18H*



3.4. Diffusion Depths (final depth)

Description	SRP	SIMS	Units
N+ junction depth (from top of silicide)-low voltage N+ junctions	0.10	0.19	µm
N+ junction depth (from top of silicide)-high voltage N+ junctions	0.12	0.20	µm
P+ junction depth (from top of silicide)	0.10	0.19	µm
N+ junction depth (below silicide) for low voltage N+ junctions	0.07	0.12	µm
N+ junction depth (below silicide) for high voltage N+ junctions	0.08	0.13	µm
P+ junction depth (below silicide)	0.07	0.12	µm
N-well junction depth (field area, under trench)	0.7		µm
N-well junction depth (active area)	1.2		µm

Note: Depth is given for both SRP and SIMS measurement (estimates for this revision). The SIMS measurements are generally considered to provide more reliable values for very shallow junctions than SRP.

4. FET AND INTERCONNECT ELECTRICAL PARAMETERS

4.1. Threshold Voltages

Description	N-channel			P-channel			
	Min.	Nom.	Max.	Min.	Nom.	Max.	Units
For SBC18HX, HXL, HKL, HA, PT,PTA only							
10µm x 10µm-1.8v fets	0.31	0.35	0.39	-0.34	-0.40	-0.46	volts
10µm x 0.18µm-1.8v fets	0.41	0.49	0.57	-0.36	-0.44	-0.52	volts
0.22µm x 10µm- 1.8v fets	0.15	0.22	0.29	-0.32	-0.39	-0.46	volts
0.22µm x 0.18µm- 1.8v fets	0.27	0.39	0.51	-0.27	-0.39	-0.51	Volts
For SBC18HX, HXL, HKL, HA, PT,PTA, QTD,QTE, QTR, QTL, QW, MW, MV, MWD only							
10µm x 10µm-3.3v fets	0.56	0.61	0.66	-0.72	-0.79	-0.86	Volts
10µm x 0.36µm-3.3v fets	0.50	0.60	0.70	-0.66	-0.76	-0.86	Volts
10µm x 0.30µm-3.3v Pfets				-0.64	-0.74	-0.84	Volts

Note: Threshold voltage, V_T, is calculated from a measured Id versus Vgs curve at Vs=0 and Vd=+50mV (-50mV for P-channel). A line tangent to this curve at the maximum slope point is found. The intercept of this tangent with the Vgs axis is then determined. V_T is defined as the value of the Vgs intercept minus 1/2 Vd.

4.2. Temperature Dependence of Threshold Voltages

Description	**N-channel**			**P-channel**			
	Min.	**Nom.**	**Max.**	**Min.**	**Nom.**	**Max.**	**Units**
For SBC18HX, HXL, HKL, HA, PT ,PTAonly							
10µm x 10µm for 1.8v fets		-0.88E-3			0.90E-3		Volt/°C
For SBC18HX, HXL, HKL, HA, PT, PTA,QTD,QTE, QTR, QTL, QW, MW, MV, MWD only							
10µm x 10µm for 3.3v fets		-1.00E-3			1.20E-3		Volt/°C

4.3. Transconductances

Description	**N-channel**			**P-channel**			
	Min.	**Nom.**	**Max.**	**Min.**	**Nom.**	**Max.**	**Units**
For SBC18HX, HXL, HKL, HA, PT ,PTA only							
10µm x 10µm-1.8v fets	130	143	156	30	32	34	$\mu A/V^2$
For SBC18HX, HXL, HKL, HA, PT, PTA,QTD,QTE, QTR, QTL, QW, MW, MV, MWD only							
10µm x 10µm-3.3v fets	85	90	95	17.5	19.5	21.5	$\mu A/V^2$

Note: Transconductance is calculated from the maximum slope of transfer curve @Vd=0.05 V and defined as $\mu_0 C_{ox}/2$.

4.4. Saturation Currents

Description	N-channel			P-channel			
	Min.	Nom.	Max.	Min.	Nom.	Max.	Units
For SBC18HX, HXL, HKL, HA, PT,PTA only							
10µm x 0.18µm - for 1.8v fets	5.1	6.0	6.9	2.1	2.55	3.0	mA
0.60µm x 0.18µm - for 1.8v fets	290	370	450	120	150	180	µA
0.42µm x 0.18µm –for 1.8v fets	180	250	320	75	100	125	µA
0.22µm x 0.18µm –for 1.8v fets	80	140	200	40	60	80	µA

Note: Vd=Vg=1.8V or -1.8V for 1.8v N-ch or P-ch fets respectively. The 0.22um wide device was drawn with dogbone active and minimum poly to active spacing, so the current drive is higher than devices with wider poly to active spacing. All the specified structures have isolated transistor.

Description	N-channel			P-channel			
	Min.	Nom.	Max.	Min.	Nom.	Max.	Units
For SBC18HX, HXL, HKL, HA, PT, PTA,QTD, QTE,QTR, QTL, QW, MW, MV, MWD only							
10µm x 0.36µm for 3.3v fets	5.0	6.0	7.0	2.05	2.45	2.85	mA
10µm x 0.30µm for 3.3v Pfet				2.4	2.9	3.4	mA
0.60µm x 0.36µm –for 3.3v fets	285	360	435	110	140	170	µA
0.60µm x 0.30µm –for 3.3v Pfet				130	180	230	µA

Note: Vd=Vg=3.3V or –3.3V for N-ch or P-ch fets respectively. All structures have isolated transistor.

4.5. Transconductances/Saturation Current Ratio (gm/Id)

Description	N-channel			P-channel			
	Min.	Nom.	Max.	Min.	Nom.	Max.	Units
For SBC18HX, HXL, HKL, HA, PT,PTA only							
10µm x 0.18µm-1.8V FETs	9.5	11	12.5	-15.5	-13	-10.5	1/V
For SBC18HX, HXL, HKL, HA, PT, PTA,QTD,QTE, QTR, QTL, QW, MW, MV, MWD only							
10µm x 0.36µm-3.3V FETs	9	11.7	14.4				1/V
10µm x 0.30µm-3.3V FETs				-15	-11	-7	1/V

Note: gm/Id is measured at Vg=V_T+0.1V or V_T -0.1V for N-ch or P-ch, Vd=0.4V or –0.4V for N-ch or P-ch PFETs.

4.6. Body Constants

Description	N-channel			P-channel			
	Min.	Nom.	Max.	Min.	Nom.	Max.	Units
For SBC18HX, HXL, HKL, HA, PT only							
10µm x 10µm - 1.8v fets	0.32	0.34	0.36	0.49	0.53	0.57	$V^{0.5}$
10µm x 0.18µm - 1.8v fets	0.25	0.32	0.39	0.43	0.51	0.59	$V^{0.5}$
0.22µm x 10µm - 1.8v fets	0.21	0.28	0.35	0.34	0.44	0.54	$V^{0.5}$
0.22µm x .18µm - 1.8v fets	0.17	0.27	0.37	0.31	0.43	0.55	$V^{0.5}$
For SBC18HX, HXL, HKL, HA, PT, PTA,QTD,QTE, QTR, QTL, QW, MW, MV, MWD only							
10µm x 10µm - 3.3v fets	0.58	0.64	0.70	0.86	0.91	0.96	$V^{0.5}$
10µm x 0.36µm - 3.3v fets	0.42	0.52	0.62	0.78	0.88	0.98	$V^{0.5}$
10µm x 0.30µm - 3.3v Pfet				0.74	0.84	0.94	$V^{0.5}$

Note: Body constant is measured at Vbs=0V and Vbs=-0.9V for N-channel 1.8v devices, and measured at Vbs=0V and Vbs=+0.9V for P-channel 1.8v devices. Body constant is measured at Vbs=0V and Vbs=-1.65V for N-channel 3.3v devices, and measured at Vbs=0V and Vbs=+1.65V for P-channel 3.3v devices.

4.7. Effective Channel Lengths / External Resistances

4.7.1. Effective Channel Lengths

Description	**N-channel**			**P-channel**			
	Min.	**Nom.**	**Max.**	**Min.**		**Max.**	**Units**
For SBC18HX, HXL, HKL, HA, PT,PTA only							
10µm x 0.18µm (Leff2) - 1.8v fets	0.13	0.16	0.19	0.12	0.15	0.18	µm
10µm x 0.18µm (traditional) – 1.8v fets	0.15	0.175	0.20	0.143	0.168	0.193	µm
For SBC18HX, HXL, HKL, HA, PT,PTA, QTD, QTE,QTR, QTL, QW, MW, MV, MWD only							
10µm x 0.36µm (Leff2) - 3.3v fets	0.24	0.28	0.33	0.24	0.27	0.31	µm
10µm x 0.36µm (traditional)- 3.3v fets	0.31	0.35	0.39	0.24	0.28	0.32	µm
10µm x 0.30µm (Leff2) - 3.3v Pfet				0.19	0.21	0.25	µm
10µm x 0.30µm (traditional)- 3.3v Pfet				0.18	0.22	0.26	µm

Note: The Leff2 method uses two channel lengths of 0.18µm and 10µm for the 1.8v fets and lengths of 0.36/0.30µm and 10µm for the 3.3v fets. The effective channel length is derived by first plotting device resistances at five Vg's (with Vg-Vt = 0.5, 0.6, 0.7, 0.8, 0.9V at Vds=0.05V) as a function of the drawn channel lengths. The slope and intercept for each Vg are then used as X and Y values respectively to plot another straight line to obtain the external resistance and delta Leff from the Y-intercept and slope respectively. The Leff2 is obtained by subtracting delta Leff from drawn dimension. The traditional method of the effective channel length is simply calculated by the transconductance comparison with a 10µm x 10µm device. The Leff2 values for these FETs may not be accurately measured by the Leff2 method due to the additional Halo implant that gives a strong lateral variation of doping along the channel; the typical values are provided here for reference only.

4.7.2. External Resistances

Description	**N-channel**			**P-channel**			
	Min.	**Nom.**	**Max.**	**Min.**	**Nom.**	**Max.**	**Units**
For SBC18HX, HXL, HKL, HA, PT,PTA only							
10µm x 0.18µm (Leff2) - for 1.8v fets	10	25	35	30	60	90	Ohms
For SBC18HX, HXL, HKL, HA, PT, PTA,QTD,QTE, QTR, QTL, QW, MW, MV, MWD only							
10µm x 0.36µm (Leff2)- for 3.3v fets	25	45	65	80	120	160	Ohms
10µm x 0.30µm (Leff2)- for 3.3v Pfet				80	120	160	Ohms

Note: The external resistance of transistor is defined as the effective series resistance associated with both drain and source sides of the transistor and is obtained from Leff2 method used in the effective channel length calculation. Due to uncertainties in the accuracy of the above values, they are primarily useful for process control, and the range of values does not reflect the range of values used in SPICE models. The external resistance values for CG18 FETs may not be accurately measured by the Leff2 method due to the additional Halo implant that gives a strong lateral variation of doping along the channel; the typical values are provided here for reference.

4.8. Effective Channel Widths

Description	**N-channel**			**P-channel**			
	Min.	**Nom.**	**Max.**	**Min.**	**Nom.**	**Max.**	**Units**
For SBC18HX, HXL, HKL, HA, PT ,PTA only							
0.22µm x 10µm - for 1.8v isolated fets	0.15	0.19	0.23	0.17	0.22	0.27	µm
0.22µm x 10µm - for 1.8v dense array of parallel fets	0.13	0.16	0.19	0.17	0.21	0.25	µm
For SBC18HX, HXL, HKL, HA, PT,PTA, QTD,QTE, QTR, QTL, QW, MW, MV, MWD only							
0.40µm x 10µm - for 3.3v fets	0.28	0.34	0.4	0.30	0.36	0.42	µm

Note: The effective channel width is calculated by transconductance comparison with a 10µm x 10µm device.

4.9. Subthreshold Slopes

Description	N-channel			P-channel			
	Min.	Nom.	Max.	Min.	Nom.	Max.	Units
For SBC18HX, HXL, HKL, HA, PT ,PTA only							
10µm x 0.18µm - for 1.8v fets		78	85		78	85	mV/decade
For SBC18HX, HXL, HKL, HA, PT, PTA,QTD,QTE, QTR, QTL, QW, MW, MV, MWD only							
10µm x 0.36µm- for 3.3v fets		85			85		mV/decade
10µm x 0.30µm- for 3.3v Pfet					85		mV/decade

Note: The subthreshold slope is measured at a drain voltage of 0.05V at RT.

4.10. Maximum Substrate Current Densities

Description	N-channel			P-channel			
	Min.	Nom.	Max.	Min.	Nom.	Max.	Units
For SBC18HX, HXL, HKL, HA, PT ,PTAonly							
10µm x 0.18µm - for 1.8v fets	0.05	0.2	1.0		0.0008	0.02	µA/µm
For SBC18HX, HXL, HKL, HA, PT, PTA,QTD,QTE, QTR, QTL, QW, MW, MV, MWD only							
10µm x 0.36µm- for 3.3v fets	0.5	1.2	3.0		0.06	0.15	µA/µm
10µm x 0.30µm- for 3.3v Pfet					0.09	0.25	µA/µm

Note: Measured at Vd=2.0V for the 1.8v fets and Vd=3.6V for the 3.3v fets with Vg selected for maximum substrate current. The range of peak substrate currents are approximately from Vg=0.7v to 1.3v

4.11. Transistor Off Leakage Currents

Description	N-channel			P-channel			
	Min.	Nom.	Max.	Min.	Nom.	Max.	Units
For SBC18HX, HXL, HKL, HA, PT,PTA only							
10µm x 0.18µm (@25°C) - for 1.8v fets			0.1			0.1	nA/µm
10µm x 0.18µm (@85°C) - for 1.8v fets			5			5	nA/µm
For SBC18HX, HXL, HKL, HA, PT, PTA,QTD, QTE,QTR, QTL, QW, MW, MV, MWD only							
10µm x 0.36µm (@25°C)- for 3.3v Nfets			0.04				nA/µm
10µm x 0.36µm (@85°C)- for 3.3v Nfets			2.0				nA/µm
10µm x 0.30µm (@25°C)- for 3.3v Pfets						0.04	nA/µm
10µm x 0.30µm (@85°C)- for 3.3v Pfets						2.0	nA/µm

Note: Vg=0V, Vd=2.0V or -2.0V for the 1.8v N-ch or P-ch fets respectively. Vg=0V, Vd=3.6V or -3.6V for the 3.3v N-ch or P-ch fets respectively. For estimation of circuit standby current only.

4.12. Diode Leakage Currents

Description	N-channel			P-channel			
	Min.	Nom.	Max.	Min.	Nom.	Max.	Units
Perimeter - for low voltage junctions			10			20	fA/µm
Area - for low voltage junctions			1			1	fA/µm^2
Perimeter - for high voltage junctions			10			10	fA/µm
Area - for high voltage junctions			1			1	fA/µm^2

Note: Vg=0V, Vd=2.0V or -2.0V for low voltage N-diffusion or standard P-diffusion, respectively, at 25°C. Vg=0V, Vd=3.6V or -3.6V for high voltage N-diffusion or standard P-diffusion, respectively, at 25°C. The area leakage current increases by less than a factor of 2 for each 10°C increase in temperature. The perimeter leakage current increases by a factor of 2 for every 15C increase in temperature.

4.13. Breakdown Voltages

Description	N-ch	P-ch	Units
Low voltage fets (1.8v fets): **For SBC18HX, HXL, HKL, HA, PT,PTA only**			
10µm x 10µm - 1.8v fets	>4.0	<-4.0	volts
10µm x 0.18µm - 1.8v fets	>3.2	<-3.2	volts
0.6µm x 10µm - 1.8v fets	>4.0	<-4.0	volts
0.6µm x 0.18µm - 1.8v fets	>3.2	<-3.2	volts
0.24µm x 10µm - 1.8v fets	>4.0	<-4.0	volts
0.24µm x 0.18µm - 1.8v fets	>3.2	<-3.2	volts
0.44µm x 0.18µm - 1.8v fets	>3.2	<-3.2	volts
High voltage fets (3.3v fets): **For SBC18HX, HXL, HKL, HA, PT,PTA, QTD,QTE, QTR, QTL, QW, MW, MV, MWD only**			
10µm x 10µm - 3.3v fets: (DG masked)	>6.0	<-5.0	volts
10µm x 0.36µm - 3.3v Nfets: (DG masked)	>6.0		volts
10µm x 0.30µm - 3.3v Pfets: (DG masked)		<-5.0	volts
10µm x 0.36µm - 3.3v fets: (DG masked) open-source configuration	>7.0		volts
Junctions: **For SBC18HX, HXL, HKL, HA, PT,PTA only**			
Junction; low voltage junctions (1.8v nominal operation)	>4.0	<-4.0	volts
Junctions: **For SBC18HX, HXL, HKL, HA, PT,PTA, QTD,QTE, QTR, QTL, QW, MW, MV, MWD only**			
Junction; high voltage junctions: (DG masked) (3.3v nominal operation)	>7.0	<-5.0	volts
VFI (field inversion test):			

For SBC18HX, HXL, HKL, HA, PT,PTA only			
Poly VFI 50x0.28μm; low voltage junctions	>4.0	<-4.0	volts
Metal 1 to (N-1) VFI 50x0.28μm; for low voltage junctions	>4.0	<-4.0	volts
Metal N VFI 50x0.28μm; for low voltage junctions	>4.0	<-4.0	volts
VFI (field inversion test):For SBC18HX, HXL, HKL, HA, PT,PTA QTD, QTE,QTR, QTL, QW, MW, MV, MWD only			
Poly VFI 50x0.28μm; high voltage junctions:(DG masked)	>6.0	<-5.0	volts
Metal 1 to (N-1) VFI 50x0.28μm; high voltage junctions: (DG masked)	>7.0	<-5.0	volts
Metal N VFI 50x0.28μm; high voltage junctions:(DG masked)	>7.0	<-5.0	volts

Notes: The breakdown voltage is measured at Idrain=1μA for N-channel (or -1μA for P-channel) devices at room temperature.

The open-source configuration is for the high voltage nfet test to verify 5v tolerant operation of input receivers. The configuration is a breakdown voltage test. The breakdown is measured at Idrain=1μA for N-channel at room temperature. The source is open, gate is 3.3v, substrate is grounded.

4.14. Dielectric Breakdown Voltages

Description		Units
Gate oxide (TDDB) for thin oxide **For SBC18HX, HXL, HKL, HA, PT,PTA only**	>4.0	Volts
Gate oxide (TDDB) for thick oxide **For SBC18HX, HXL, HKL, HA, PT, PTA,QTD, QTE, QTR, QTL, QW, MW, MV, MWD only**	>8.0	Volts
Poly to substrate	>200	Volts
Metal 1 to poly 1	>200	Volts
Metal 2 to metal 1	>200	Volts
Metal 3 to metal 2	>200	Volts
Metal 4 to metal 3	>200	Volts
Metal 5 to metal 4	>200	Volts
Metal 6 to metal 5	>200	Volts
MIM Capacitor – TDDB (1fF/um^2 density)	>18.0	Volts
MIM Capacitor – TDDB (2fF/um^2 density)	>14.0	Volts
MIM Capacitor – TDDB (2.8fF/um^2 density)	>10.0	Volts

Note: The maximum voltage allowed to be applied to gate oxide is 2.0 V, not 4.0 V for the thin gate oxides. The maximum voltage allowed to be applied to gate oxide is 3.6 V, not 9 V for the thick gate oxides. The quoted breakdown voltage of gate oxide (the TDDB gate oxide accelerated reliability tests) is measured at the rupture of the oxide under voltage ramp of 2V/sec.

4.15. Sheet Resistivity

Description	Min.	Nom.	Max.	Units
N-well sheet resistance R_s(under field oxide) †	710	890	1070	Ω/ ☐
N+ diffusion sheet resistance		6	12	Ω/ ☐
P+ diffusion sheet resistance		6	12	Ω/ ☐
Salicided poly sheet resistance-Rs*	4.2	5.5	6.8	Ω/ ☐
Metal 1 sheet resistance (for all SBC18)	69	82	95	mΩ/ ☐
Metal 2 sheet resistance (for SBC18HX, HXL, HKL, HA, PT,PTA)	69	82	95	mΩ/ ☐
Metal 2 sheet resistance (for SBC18QTD, QTE, QTR, QTL, QW, MW, MV, MWD)	46	66	86	mΩ/ ☐
Metal 3 sheet resistance (for SBC18HX, HXL, HKL, HA, PT,PTA)	69	82	95	mΩ/ ☐
Metal 3 sheet resistance (for SBC18QTD, QTE, QTR, QTL, QW)	46	66	86	mΩ/ ☐
Metal 3 sheet resistance (for SBC18MW, MV, MWD)	9	10.5	12	mΩ/ ☐
Metal 4 sheet resistance (for SBC18HX, HXL, HKL, HA)	46	66	86	mΩ/ ☐
Metal 4 sheet resistance (for SBC18PT,PTA)	14	18	22	mΩ/ ☐
Metal 4 sheet resistance (for SBC18QTD,QTE, QTR, QTL)	4.5	5.5	6.5	mΩ/ ☐
Metal 4 sheet resistance (for SBC18QW)	9	10.5	12	mΩ/ ☐
Metal 5 sheet resistance (for SBC18HX, HXL, HKL, HA)	14	18	22	mΩ/ ☐
Metal 5 sheet resistance (for SBC18PT,PTA only)	4.5	5.5	6.5	mΩ/ ☐
Metal 6 sheet resistance (for SBC18HX, HXL, HKL, HA only)	9	10.5	12	mΩ/ ☐
Top metal (TM) sheet resistance (for MIM capacitor)	3.6	4.9	6.2	Ω/ ☐
Stacked top metal (TM) sheet resistance (for stacked MIM capacitor) for SBC18PT,PTA, QW, HA only	3.6	4.9	6.2	Ω/ ☐

Note: The sheet resistivity for diffusion or poly is the combination result of resistivities of both silicide and diffusion (poly) layer.

† The total N-well resistance R_{well} can be calculated using the formula below:

$$R_{well} = R_S*L/(W+\Delta W) + R_{end}/(W+\Delta W)$$

W is the drawn width and L is the drawn length, respectively. ΔW is used here to account for the difference between the electric width vs. the drawn width caused by the dopant diffusion and the non-ideal photo (well) exposure effects. To correct for the modulation partly caused by retrograde well profiles and shallow trench isolation, the end resistance (including both ends) R_{end} has to be included in the formula to correctly calculate the total N-well resistance. Values of ΔW and R_{end} are listed in Nwell resistor sub section of Section 6.

* The salicided poly resistance R_{poly} can be calculated using the formula below:

$$R_{poly} = R_S*L/(W+\Delta W) + R_{end}/(W+\Delta W)$$

W is the drawn width and L is the drawn length, respectively. ΔW is used here to account for poly patterning effects (photo and etch). Values of ΔW and R_{end} are listed in silicided poly resistor sub section of Section 6.

4.16. Capacitance

4.16.1. Front-End CMOS Capacitances

Description	N-channel			P-channel			
	Min.	Nom.	Max.	Min.	Nom.	Max.	Units
For SBC18HX, HXL, HKL, HA, PT,PTA only							
N-well area capacitance				140	180	220	aF/μm^2
N-well perimeter capacitance				600	750	900	aF/μm
Gate oxide capacitance-thin oxide (N+ Poly over N-ch at -3.3V & P+ Poly over P-ch at +3.3v)	8.6	9.5	10.5	9.0	9.9	10.9	fF/μm^2
Gate oxide capacitance-thin oxide (N+ Poly over N-ch at +1.8V & P+ Poly over P-ch at –1.8V)	7.5	8.0	8.6	7.3	7.8	8.4	fF/μm^2
Gate overlap drain/source for 1.8v fets (V_{GS}=0V)	365	395	435	440	480	520	aF/μm
Gate overlap drain/source for 1.8v fets (V_{GS} = -0.9V for NFET; +0.9V for PFET)	237	267	297	215	345	375	aF/μm
P+/N+ junction area cap for low voltage junctions	800	1000	1200	1000	1200	1400	aF/μm^2
P+/N+ 1.8v junction sidewall to field	180	200	220	40	70	100	aF/μm
P+/N+ junction sidewall to channel for 1.8v fets	300	330	360	360	400	440	aF/μm

Description	N-channel			P-channel			
	Min.	Nom.	Max.	Min.	Nom.	Max.	Units
For SBC18HX, HXL, HKL, HA, PT, PTA,QTD,QTE, QTR, QTL, QW, MW, MV, MWD only							
N-well area capacitance				140	180	220	aF/μm^2
N-well perimeter capacitance				600	750	900	aF/μm
Gate oxide capacitance-thick oxide (N+ Poly over N-ch at –3.3V & P+ Poly over P-ch at +3.3v)	4.54	4.93	5.40	4.54	4.93	5.40	fF/μm^2
Gate overlap drain/source for 3.3v fets (V_{GS}=0V)	200	300	400	260	360	460	aF/μm
Gate overlap drain/source for 3.3v fets (V_{GS} = -1.65V for NFET; +1.65V for PFET)	230	260	290	245	275	305	aF/μm
P+/N+ junction area cap for high voltage (3.3V) junctions	800	1000	1200	575	720	865	aF/μm^2
P+/N+ 3.3v junction sidewall to field	120	140	160	35	60	85	aF/μm
P+/N+ junction sidewall to channel for 3.3v fets	270	300	330	270	300	330	aF/μm

4.16.2. Back-End Capacitances

Description – applicable to all SBC18	Min.	Nom.	Max.	Units
Poly to substrate (silicon under STI)	106.2	132.8	177.1	aF/μm^2
Metal 1 to poly 1	42.7	55.8	80.7	aF/μm^2
Metal 1 to diffusion	35.0	43.2	56.5	aF/μm^2
Metal 1 to substrate (silicon under STI)	27.5	32.6	40.1	aF/μm^2
Metal 2 to metal 1	35.4	46.5	67.6	aF/μm^2
Metal 2 to poly 1	16.2	18.9	22.7	aF/μm^2
Metal 2 to diffusion	14.8	17.1	20.1	aF/μm^2
Metal 2 to substrate (silicon under STI)	13.3	15.1	17.5	aF/μm^2

Description – applicable to SBC18HX, HXL, HKL, HA only	**Min.**	**Nom.**	**Max.**	**Units**
Metal 3 to metal 2	35.4	46.5	67.6	aF/µm^2
Metal 3 to metal 1	15.0	17.5	21.2	aF/µm^2
Metal 3 to poly 1	10.0	11.2	13.0	aF/µm^2
Metal 3 to diffusion	9.5	10.6	12.1	aF/µm^2
Metal 3 to substrate (silicon under STI)	8.8	9.8	11.1	aF/µm^2
Metal resistor plate TR to metal 2	21.9	25.6	31.0	aF/µm^2
Metal resistor plate TR to metal 4	42.7	60.0	100.5	aF/µm^2
Metal resistor plate TR to substrate (silicon under STI)	7.7	8.4	9.3	aF/µm^2
Metal 4 to metal 3	35.4	46.5	67.6	aF/µm^2
Metal 4 to metal 2	15.0	17.5	21.2	aF/µm^2
Metal 4 to metal 1	9.6	10.8	12.4	aF/µm^2
Metal 4 to poly 1	7.3	8.1	9.0	aF/µm^2
Metal 4 to diffusion	7.0	7.7	8.6	aF/µm^2
Metal 4 to substrate (silicon under STI)	6.6	7.3	8.1	aF/µm^2
Metal 5 to metal 4	15.5	18.6	23.3	aF/µm^2
Metal 5 to metal 3	9.5	10.9	12.6	aF/µm^2
Metal 5 to metal 2	7.0	7.8	8.9	aF/µm^2
Metal 5 to metal 1	5.6	6.1	6.8	aF/µm^2
Metal 5 to poly 1	4.7	5.1	5.6	aF/µm^2
Metal 5 to diffusion	4.6	5.0	5.5	aF/µm^2
Metal 5 to substrate (silicon under STI)	4.4	4.8	5.3	aF/µm^2
Metal 6 to metal 5	15.5	18.6	23.3	aF/µm^2
Metal 6 to metal 4	6.0	6.7	7.5	aF/µm^2
Metal 6 to metal 3	4.8	5.3	5.9	aF/µm^2
Metal 6 to metal 2	4.1	4.5	4.9	aF/µm^2
Metal 6 to metal 1	3.6	3.9	4.2	aF/µm^2
Metal 6 to poly 1	3.2	3.4	3.7	aF/µm^2
Metal 6 to diffusion	3.1	3.4	3.6	aF/µm^2
Metal 6 to substrate (silicon under STI)	3.1	3.3	3.5	aF/µm^2

Description – applicable to SBC18PT,PTA only	Min.	Nom.	Max.	Units
Metal 3 to metal 2	35.4	46.5	67.6	aF/μm^2
Metal 3 to metal 1	15.0	17.5	21.2	aF/μm^2
Metal 3 to poly 1	10.0	11.2	13.0	aF/μm^2
Metal 3 to diffusion	9.5	10.6	12.1	aF/μm^2
Metal 3 to substrate (silicon under STI)	8.8	9.8	11.1	aF/μm^2
Metal 4 to metal 3	15.5	18.6	23.2	aF/μm^2
Metal 4 to metal 2	9.8	11.2	13.1	aF/μm^2
Metal 4 to metal 1	7.2	8.0	9.1	aF/μm^2
Metal 4 to poly 1	5.8	6.4	7.1	aF/μm^2
Metal 4 to diffusion	5.6	6.2	6.8	aF/μm^2
Metal 4 to substrate (silicon under STI)	5.4	5.9	6.5	aF/μm^2
Metal 5 to metal 4	15.5	18.6	23.2	aF/μm^2
Metal 5 to metal 3	6.0	6.7	7.5	aF/μm^2
Metal 5 to metal 2	4.9	5.4	6.0	aF/μm^2
Metal 5 to metal 1	4.2	4.5	5.0	aF/μm^2
Metal 5 to poly 1	3.7	4.0	4.3	aF/μm^2
Metal 5 to diffusion	3.6	3.9	4.2	aF/μm^2
Metal 5 to substrate (silicon under STI)	3.5	3.8	4.1	aF/μm^2

Description - applicable to SBC18QTD,QTE, QTR, and QTL only	**Min.**	**Nom.**	**Max.**	**Units**
Metal 3 to metal 2	31.0	39.1	53.1	aF/μm^2
Metal 3 to metal 1	13.5	15.6	18.4	aF/μm^2
Metal 3 to poly 1	9.4	10.4	11.9	aF/μm^2
Metal 3 to diffusion	8.9	9.9	11.1	aF/μm^2
Metal 3 to substrate (silicon under STI)	8.3	9.2	10.3	aF/μm^2
Metal 4 to metal 3	10.9	12.4	14.3	aF/μm^2
Metal 4 to metal 2	7.3	8.1	9.1	aF/μm^2
Metal 4 to metal 1	5.7	6.2	6.8	aF/μm^2
Metal 4 to poly 1	4.8	5.2	5.6	aF/μm^2
Metal 4 to diffusion	4.7	5.0	5.5	aF/μm^2
Metal 4 to substrate (silicon under STI)	4.5	4.8	5.2	aF/μm^2
Description - applicable to SBC18QTD,QTE, QTR, and QTL, HA only	**Min.**	**Nom.**	**Max.**	**Units**
Metal resistor plate TR to poly 1	24.0	28.6	35.4	aF/μm^2
Metal resistor plate TR to Metal 2	42.7	60.0	100.5	aF/μm^2
Metal resistor plate TR to substrate (silicon under STI)	18.1	20.8	24.3	aF/μm^2

Description - applicable to SBC18QW only	Min.	Nom.	Max.	Units
Metal 3 to metal 2	31.0	39.1	53.1	aF/μm^2
Metal 3 to metal 1	13.5	15.6	18.4	aF/μm^2
Metal 3 to poly 1	9.4	10.4	11.9	aF/μm^2
Metal 3 to diffusion	8.9	9.9	11.1	aF/μm^2
Metal 3 to substrate (silicon under STI)	8.3	9.2	10.3	aF/μm^2
Metal 4 to metal 3	15.5	18.6	23.2	aF/μm^2
Metal 4 to metal 2	9.4	10.4	11.9	aF/μm^2
Metal 4 to metal 1	6.7	7.4	8.3	aF/μm^2
Metal 4 to poly 1	5.5	6.0	6.6	aF/μm^2
Metal 4 to diffusion	5.3	5.8	6.4	aF/μm^2
Metal 4 to substrate (silicon under STI)	5.1	5.6	6.1	aF/μm^2

Description - applicable to SBC18MW, MV, MWD only	Min.	Nom.	Max.	Units
Metal 3 to metal 2	15.5	18.6	23.2	aF/μm^2
Metal 3 to metal 1	9.5	10.8	12.6	aF/μm^2
Metal 3 to poly 1	7.2	8.0	9.1	aF/μm^2
Metal 3 to diffusion	7.0	7.7	8.7	aF/μm^2
Metal 3 to substrate (silicon under STI)	6.6	7.3	8.1	aF/μm^2

4.17. Intermetal and Intrametal Dielectric Constants

Description	Min.	Nom.	Max.	Units
Poly on field to silicon		4.2		ε/ε0
Metal 1 to Poly		4.1		ε/ε0
Metal N to metal (N-1), N=2 to 6		4.2		ε/ε0
Metal N to metal N, N = 1 to 6		4.2		ε/ε0
Oxide overcoat		4.2		ε/ε0
Nitride overcoat		7.0		ε/ε0

4.18. Contact and Via Resistance

Description – applicable to all SBC18	Min.	Nom.	Max.	Units
Metal 1 to N+ silicide (0.22μ)		12.5	25.0	Ω/contact
Metal 1 to P+ silicide (0.22μ)		12.5	25.0	Ω/contact
Metal 1 to poly 1 silicide (0.22μ)		8.0	20	Ω/contact
Metal 1 to base poly (0.22μ)		12.5	25.0	Ω/contact
Metal 1 to collector slotted contact (See Section 4.18.1)				
Metal 1 to emitter slotted contact (See Section 4.18.1)				
Metal 2 to metal 1 slotted via (See Section 4.18.1)				
Metal 2 to metal 1 (via) resistance (0.26μ)		5.5	10	Ω/contact

Description – applicable to SBC18HX, HXL, HKL, HA only	Min.	Nom.	Max.	Units
Metal 3 to metal 2 (via2) resistance (0.26μ)		5.5	10	Ω/contact
Metal 4 to metal 3 (via3) resistance (0.26μ)		5.5	10	Ω/contact
Metal 4 to TR via resistance	3	8	20	Ω/contact
Metal 5 to metal 4 (via4) resistance (0.50μ)		2.2	8	Ω/contact
Metal 5 to TM via resistance		2.2	8	Ω/contact
Metal 4 to TM2 via resistance		8	20	Ω/contact
Metal 6 to metal 5 (via5) resistance (0.50μ)		2.2	8	Ω/contact

Description – applicable to SBC18PT,PTA only	Min.	Nom.	Max.	Units
Metal 3 to metal 2 (via2) resistance (0.26μ)		5.5	10	Ω/contact
Metal 3 to TM via resistance	3	8	20	Ω/contact
Metal 4 to metal 3 (via3) resistance (0.50μ)		2.2	8	Ω/contact
Metal 5 to metal 4 (via4) resistance (0.50μ)		2.2	8	Ω/contact

Description - applicable to SBC18QW, QTD,QTE, QTR , QTL only	**Min.**	**Nom.**	**Max.**	**Units**
Metal 3 to metal 2 (via2) resistance (0.38μ)		5.0	12.0	Ω/contact
Metal 3 to TM via resistance		3.5	8.0	Ω/contact
Metal 4 to Metal 3 (via3) resistance (0.50μ)		2.2	8.0	Ω/contact

Description - applicable to SBC18QTR only	**Min.**	**Nom.**	**Max.**	**Units**
Metal 2 to TR via resistance (0.26μ)	3	8	20	Ω/contact

Description - applicable to SBC18MW, MV, MWD only	**Min.**	**Nom.**	**Max.**	**Units**
Metal 3 to metal 2 (via2) resistance (0.50μ)		2.2	8.0	Ω/contact
Metal 3 to TM via resistance		2.2	8.0	Ω/contact

4.18.1. Slotted Contact and Slotted Via Resistance

For slots with less than 0.5 μm width, the nominal resistance is ***estimated*** as:

$$R = \frac{4\left(\rho_{c,v} + \rho_W H\right)}{\pi w^2 + 4w(L - w)} \quad \Omega/\text{contact},$$

where H = contact height
w = slot width
L = slot length
ρ_w = 12 μΩcm (Tungsten resistivity)
$\rho_{c,v}$ = fitted interface resistivity (use ρ_c for contact and ρ_v for via)
ρ_c = 0.45 Ωμm^2 (for contact)
ρ_v = 0.22 Ωμm^2 (for via)

The maximum resistance is two times the obtained nominal resistance.

4.19. Interconnect Current Densities for Reliable Operation

4.19.1 DC Operation

	@85°C	@110°C	@125°C	Units
Metal 1, Metal 2 (for all SBC18)	3	1.0	0.5	mA/µm
Metal 3 (for SBC18HX, HXL, HKL, HA, PT,PTA, QW, QTD,QTE, QTR, QTL)	3	1.0	0.5	mA/µm
Metal 3 (for SBC18MW, MV, MWD)	16	5.8	2.7	mA/µm
Metal 4 (for SBC18HX, HXL, HKL, HA)	3	1.0	0.5	mA/µm
Metal 4 (for SBC18PT,PTA)	7.5	2.5	1.25	mA/µm
Metal 4 (for SBC18QTD, QTE,QTR, QTL)	24	8.7	4.2	mA/µm
Metal 4 (for SBC18QW)	16	5.8	2.7	mA/µm
Metal 5 (for SBC18HX, HXL, HKL, HA)	7.5	2.5	1.25	mA/µm
Metal 5 (for SBC18PT,PTA)	24	8.7	4.2	mA/µm
Metal 6 (for SBC18HX, HXL, HKL, HA)	15	5.0	2.5	mA/µm
Contact (0.22µm x 0.22µm) (for all SBC18)	0.8	0.6	0.5	mA/Contact
Slotted Emitter Contact (0.3µm wide) Slotted Collector Contact (0.36µm wide) Slotted Via 1(0.3µm wide) (for all SBC18)	3.84	2.88	2.4	mA/(slot-Contact µm)
Via 1 (for all SBC18)	0.85	0.7	0.6	mA/Via
Via 2 (0.26µm x 0.26µm) (for SBC18HX, HXL, HKL, HA, PT,PTA)	0.85	0.7	0.6	mA/Via
Via 2(0.38µm x 0.38µm), (for SBC18QW, QTD,QTE, QTR, QTL)	1.5	1.2	1.0	mA/Via
Via 2 (0.50µm x 0.50µm), (for SBC18MW, MV, MWD)	2.5	2.1	1.7	mA/Via
Via 3 (0.26µm x 0.26µm) (for SBC18HX, HXL, HKL, HA)	0.85	0.7	0.6	mA/Via
Via 3 (0.5µm x 0.5µm) (for SBC18PT ,PTAonly)	3.1	2.6	2.2	mA/Via
Via 3 (0.50µm x 0.50µm) (for SBC18QW, QTD,QTE, QTR, QTL)	2.5	2.1	1.7	mA/Via
Via 4 (0.5µm x 0.5µm) (for SBC18HX, HXL, HKL, HA, PT,PTA)	3.1	2.6	2.2	mA/Via
Via 5 (0.5µm x 0.5µm) (for SBC18HX, HXL, HKL, HA)	3.1	2.6	2.2	mA/Via

Note: Ratings provide 10 FIT reliability for 10 years. For Pulsed DC current operation, use the average current density.

4.19.2 Average Current Density for AC Operation (Frequency > 1 kHz)

	@85°C	@110°C	@125°C	Units
Metal 1, Metal 2 (for all SBC18)	12	4	2	mA/µm
Metal 3 (for SBC18HX, HXL, HKL, HA PT, ,PTA,QW, QTD,QTE, QTR, QTL)	12	4	2	mA/µm
Metal 3 (for SBC18MW, MV, MWD)	65	23	11	mA/µm
Metal 4 (for SBC18HX, HXL, HKL, HA)	12	4	2	mA/µm
Metal 4 (for SBC18PT,PTA)	30	10	5	mA/µm
Metal 4 (for SBC18QTD,QTE, QTR, QTL)	98	35	17	mA/µm
Metal 4 (for SBC18QW)	65	23	11	mA/µm
Metal 5 (for SBC18HX, HXL, HKL, HA)	30	10	5	mA/µm
Metal 5 (for SBC18PT,PTA)	98	35	17	mA/µm
Metal 6 (for SBC18HX, HXL, HKL, HA)	60	20	10	mA/µm
Contact (0.22µm x 0.22µm) (for all SBC18)	1.6	1.2	1.0	mA/Contact
Slotted Emitter Contact (0.3µm wide) Slotted Collector Contact (0.36µm wide) Slotted Via 1(0.3µm wide) (for all SBC18)	7.68	5.76	4.8	mA/(slot-Contact µm)
Via 1 (for all SBC18)	1.7	1.4	1.2	mA/Via
Via 2 (0.26µm x 0.26µm) (for SBC18HX, HXL, HKL, HA, PT,PTA)	1.7	1.4	1.2	mA/Via
Via 2(0.38µm x 0.38µm), (for SBC18QW, QTD, QTE,QTR, QTL)	3.0	2.4	2.0	mA/Via
Via 2 (0.50µm x 0.50µm), (for SBC18MW, MV, MWD)	5.0	4.2	3.4	mA/Via
Via 3 (0.26µm x 0.26µm) (for SBC18HX, HXL, HKL, HA)	1.7	1.4	1.2	mA/Via
Via 3 (0.5µm x 0.5µm) (for SBC18PT,PTA only)	6.2	5.2	4.4	mA/Via
Via 3 (0.50µm x 0.50µm) (for SBC18QW, QTD, QTE,QTR, QTL)	5.0	4.2	3.4	mA/Via
Via 4 (0.5µm x 0.5µm) (for SBC18HX, HXL, HKL, HA, PT,PTA)	6.2	5.2	4.4	mA/Via
Via 5 (0.5µm x 0.5µm) (for SBC18HX, HXL, HKL, HA)	6.2	5.2	4.4	mA/Via

Note: Ratings provide 10 FIT reliability for 10 years.

5. ELECTRICAL CIRCUIT DESIGN SPECIFICATONS

The following specifications apply to all circuits to be produced using the CMOS portion of SBC18 processes. Achievement of this performance level relies on proper circuit designs, and is not an inherent feature of the SBC18 process. It is the responsibility of the circuit designer to meet these criteria.

5.1. Power Supply Voltage

5.1.1. Maximum D.C. Operating Voltage

Description	Min.	Nom.	Max.	Units
The maximum applied D.C. voltage between ANY two terminals for 1.8V FETs (for SBC18HX, HXL, HKL, HA, PT,PTA only)		1.8	2.0	Volts
The maximum applied D.C. voltage between ANY two terminals for 3.3V FETs (for all SBC18)		3.3	3.6	Volts

5.1.2. Absolute Maximum Ratings

Description	Min.	Nom.	Max.	Units
The maximum applied voltage between ANY two terminals for 1.8V FETs (for SBC18HX, HXL, HKL, HA, PT,PTA only)	-0.5		2.5	Volts
The maximum applied voltage between ANY two terminals for 3.3V FETs (for all SBC18)	-0.5		4.6	Volts

Note: Absolute maximum continuous rating are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation above maximum operating voltage or under absolute-maximum conditions is not implied. This limit allows for startup or switching transient spikes that can be tolerated by the MOSFET, and do not refer to a continuous DC and/or AC signal magnitude.
These ratings conform to the JEDEC standards JESD8-A and EIA/JESD8-7.

5.2. Latch-up

Description	@25°C			@125°C			
	Min.	Nom.	Max.	Min.	Nom.	Max.	Units
Trigger current @circuit I/O pins *	300			150			mA
Vdd @overvoltage test for 1.8v fets (for SBC18HX, HXL, HKL, HA, PT,PTA only)	3.0			3.0			Volts
Vdd @overvoltage test for 3.3v fets (for all SBC18)	5.4			5.4			Volts

Note: Latch-up should be tested in the “use configuration” of the circuit.
*Trigger currents are tested in both negative and positive polarities.

5.3. Minimum ESD Threshold Voltage @25C

Description	Absolute value @25°C	Units
Circuit I/O pins (HBM)	2500	Volts

Note: Minimum ESD threshold voltage depends on whether Human Body Model (HBM) with both positive and negative voltage polarities or Charge Device Model (CDM) is used.

6. BIPOLARS PASSIVE ELEMENT AND MIXED SIGNAL COMPONENT ELECTRICAL PARAMETERS

6.1. NPN Transistors

6.1.1. NPN Transistor Parameters

Minimum size transistor (0.2 um x 0.76 um emitter with a single base contact):

Description	High Speed NPN**			Standard NPN			High Voltage NPN			
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Units
Beta (Je = 10μA/μm^2)	40	100	250	40	100	250	40	100	250	
Ic at Vbe=0.7V	0.12	0.32	0.52	0.12	0.32	0.52	0.12	0.32	0.52	μA
Va*	60			100			100			V
Bvceo	1.8	2.2	2.6	2.8	3.5	4.2	4.5	6.0	7.5	V
Bvebo (Je = 10μA/μm^2)	1.2	1.6	2.0	1.2	1.6	2.0	1.2	1.6	2.0	V
Bvcbo (Ic = 1μA)	6.0	7.0	8.0	11.5	13	14.5	12.0	14.0	16.0	V
Cbe (0 V)	2.2	2.6	3.0	2.1	2.5	2.9	2.1	2.5	2.9	fF
Cbc (0 V)	2.9	3.2	3.5	1.8	2.0	2.2	1.35	1.5	1.65	fF
Ccs (0 V) for SBC18HX, HXL, HA, QTD,QTE, QTR, QTL, MWD only	3.2	4	4.8	3.2	4	4.8	3.2	4	4.8	fF
Ccs (0 V) for SBC18PT,PTA, QW, MW, MV, only				8.0	10.0	12.0	8.0	10.0	12.0	fF

* Va (Early voltage) is measured at Jc of 1mA/μm^2 for HS and STD devices and 0.5mA/μm^2 for HV device.

**** Note: The High Speed NPN is available in SBC18HX, SBC18HXL, SBC18HA, SBC18QTE processes only**

Long transistor (0.2 um x 10.16 um emitter with double base contacts):

Description	**High Speed NPN****			**Standard NPN**			**High Voltage NPN**			
	Min	**Nom**	**Max**	**Min**	**Nom**	**Max**	**Min**	**Nom**	**Max**	**Units**
Beta (Je = 10μA/μm^2)	60	140	300	60	140	300	60	140	300	
Ic* at Vbe = 0.7V	1.5	4.2	6.9	1.5	4.2	6.9	1.5	4.2	6.9	uA
Va**	60			100			100			V
Bvceo	1.8	2.2	2.6	2.8	3.5	4.2	4.5	6	7.5	V
Bvebo (Je = 10μA/μm^2)	1.3	1.7	2.1	1.2	1.7	2.1	1.45	1.70	1.95	V
Bvcbo (Ic = 1μA)	6.0	7.0	8.0	11.5	13	14.5	12.0	14.0	16.0	V
Ft**** at Vbc = 1V	135	150	165	70	78	86	34	38	42	GHz
Jc at peak Ft		6.3			1.9			0.54		mA/μm^2
Fmax**** at Vbc = 1V for SBC18HX, HXL, QTD,QTE, QTR, QTL, MWD only		190			284			183		GHz
Fmax**** at Vbc = 1V for SBC18PT,PTA, QW, MW, MV only					201			120		GHz
Cbe (0 V)	27	30	33	26	29	32	24	27	30	fF
Cbc (0 V)	17.2	18.7	20.2	10.6	11.2	11.8	7.6	8.0	8.4	fF
Ccs (0 V) for SBC18HX, HA, HXL, QTD,QTE, QTR, QTL, MWD only	12.8	16	19.2	12.8	16	19.2	12.8	16	19.2	FF
Ccs (0 V) for SBC18PT, PTA,QW, MW, MV only				32	40	48	32	40	48	FF

* Note parametric test specifications may differ from electrical specifications because the PCM test temperatures are not identical to those used for modeling data collection.
** Va (Early voltage) is measured at Jc of 1mA/μm2 for HS and STD devices and 0.5mA/μm2 for HV device.
*** Note: The High Speed NPN is available in SBC18HX, SBC18HXL, SBC18HA, SBC18QTE processes only
**** Ft is extracted from abs(h21) measured at 10 / 3 / 1GHz for the HS, STD, and HV NPNs respectively assuming a 20dB/dec frequency dependence. Fmax is extracted from unilateral gain (U) measured at 15GHz assuming 20db/dec frequency dependence.

Long transistor (0.9 um x 10.16 um emitter with double base contacts):

Description	**Standard NPN**			**High Voltage NPN**			
	Min	**Nom**	**Max**	**Min**	**Nom**	**Max**	**Units**
Beta (Je=10uA/um^2)	60	160	300	60	160	300	uA
Ic at Vbe = 0.7V	3.9	15.8	27.7	3.9	15.8	27.7	uA
Ft at Vbc = 1V	55	63	71	27.5	32.5	36.5	GHz
Jc at peak Ft	-	0.81	-	-	0.31	-	mA/μm^2
Fmax at Vbc = 1V for SBC18HX, HXL, HA, QTD,QTE, QTR, QTL, MWD only		121			88		GHz
Fmax at Vbc = 1V for SBC18PT,PTA, QW, MW, MV only		104			70		GHz
Cbe (0 V)	90	100	110	80	90	100	fF
Cbc (0 V)	14	16.4	18.8	8.5	10.4	12.3	fF
Ccs (0 V) for SBC18HX, HXL, HA, QTD,QTE, QTR, QTL, MWD only	14.0	17.4	20.8	14.0	17.4	20.8	fF
Ccs (0 V) for SBC18PT,PTA, QW, MW, MV only	34.5	43.5	52	34.5	43.5	52	fF

6.1.2. NPN Transistor Ic Matching

The delta Ic matching results are reported as a function of collector current density and Vce bias and a function of emitter area for each type of NPN. The data here is preliminary characterization data only and is subject to change. The NPNs are 15um apart. See analog characterization report NPB PS-0392 for more details.

				3 sigma (%diff)	3 sigma (%diff)	3 sigma (%diff)
W (um)	**L(um)**	**Vce (v)**	**Jc (mA/um2)**	**HS NPN**	**Std NPN**	**HV NPN**
0.2	0.76	0.6	0.005	11.8	13.2	11.6
0.2	2.64	0.6	0.005	7.3	7.1	6.9
0.6	2.64	0.6	0.005	4.8	5.2	5.1
0.2	10.16	0.6	0.005		4.2	3.8
0.6	10.16	0.6	0.005	2.2	3.0	2.7
0.2	0.76	1	0.005	11.9	13.3	11.6
0.2	2.64	1	0.005	7.3	7.1	6.9
0.6	2.64	1	0.005	5.0	5.3	5.1
0.2	10.16	1	0.005		4.2	3.8
0.6	10.16	1	0.005	2.3	3.1	2.7
0.2	0.76	1.4	0.005	12.0	13.4	11.7
0.2	2.64	1.4	0.005	7.4	7.2	6.9
0.6	2.64	1.4	0.005	5.1	5.3	5.0
0.2	10.16	1.4	0.005		4.2	3.7
0.6	10.16	1.4	0.005	2.7	3.1	2.8
0.2	0.76	0.6	0.05	11.0	12.5	11.0
0.2	2.64	0.6	0.05	6.8	6.7	6.6
0.6	2.64	0.6	0.05	4.2	4.8	4.6
0.2	10.16	0.6	0.05		4.0	3.6
0.6	10.16	0.6	0.05	2.1	2.9	2.6
0.2	0.76	1	0.05	11.0	12.5	11.0
0.2	2.64	1	0.05	6.9	6.8	6.6
0.6	2.64	1	0.05	4.4	4.9	4.7
0.2	10.16	1	0.05		4.0	3.6
0.6	10.16	1	0.05	2.1	2.9	2.6
0.2	0.76	1.4	0.05	11.1	12.6	11.0
0.2	2.64	1.4	0.05	6.9	6.8	6.7
0.6	2.64	1.4	0.05	4.5	4.9	4.7
0.2	10.16	1.4	0.05		4.0	3.6
0.6	10.16	1.4	0.05	2.2	2.9	2.6
0.2	0.76	0.6	0.5	11.1	11.7	9.0
0.2	2.64	0.6	0.5	6.3	6.0	5.3
0.6	2.64	0.6	0.5	4.0	4.4	2.7
0.2	10.16	0.6	0.5		3.7	2.8
0.6	10.16	0.6	0.5	1.8	2.6	1.7
0.2	0.76	1	0.5	11.2	11.8	10.0
0.2	2.64	1	0.5	6.4	6.1	5.8
0.6	2.64	1	0.5		4.6	3.2
0.2	10.16	1	0.5	4.2	3.8	3.2
0.6	10.16	1	0.5	1.9	2.8	2.0
0.2	0.76	1.4	0.5	11.3	11.9	10.4
0.2	2.64	1.4	0.5	6.6	6.2	6.0
0.6	2.64	1.4	0.5	4.5	4.8	3.9
0.2	10.16	1.4	0.5		3.9	3.3
0.6	10.16	1.4	0.5	2.0	2.9	2.4

6.1.3. NPN Transistor Beta Matching

The delta Ic matching results are reported as a function of collector current density and Vce bias and a function of emitter area for each type of NPN. The data here is preliminary characterization data only and is subject to change. The NPNs are 15um apart. See analog characterization report NPB PS-0392 for more details.

				HS NPN		Std NPN		HV NPN	
W (um)	L(um)	Vce (v)	Jc (mA/um2)	Mean Beta	3 sigma (%diff)	Mean Beta	3 sigma (%diff)	Mean Beta	3 sigma (%diff)
0.2	0.76	0.6	0.005	134	31.5	106	52.3	105	40.9
0.2	2.64	0.6	0.005	176	24.1	143	29.5	140	27.6
0.6	2.64	0.6	0.005	198	19.0	201	14.3	198	15.4
0.2	10.16	0.6	0.005	172	17.0	140	20.2	139	19.2
0.9	10.16	0.6	0.005	199	10.4	190	9.7	189	9.4
0.2	0.76	1	0.005	135	31.6	107	52.4	105	40.9
0.2	2.64	1	0.005	176	24.3	143	28.4	140	27.7
0.6	2.64	1	0.005	199	19.8	202	13.8	199	15.4
0.2	10.16	1	0.005	173	17.4	139	20.2	139	19.2
0.9	10.16	1	0.005	200	10.6	191	9.6	190	9.4
0.2	0.76	1.4	0.005	137	32.4	107	52.3	105	40.9
0.2	2.64	1.4	0.005	180	24.7	143	28.5	140	27.7
0.6	2.64	1.4	0.005	203	19.3	202	13.8	199	15.3
0.2	10.16	1.4	0.005	177	17.4	140	20.3	139	19.2
0.9	10.16	1.4	0.005	202	10.6	191	9.5	190	9.3
0.2	0.76	0.6	0.05	126	18.7	102	31.5	100	26.2
0.2	2.64	0.6	0.05	126	13.2	137	15.9	138	14.5
0.6	2.64	0.6	0.05	170	8.0	191	7.6	190	6.8
0.2	10.16	0.6	0.05	189	6.7	135	7.8	135	8.6
0.9	10.16	0.6	0.05	199	3.7	181	3.2	180	3.4
0.2	0.76	1	0.05	127	18.8	102	31.5	100	26.2
0.2	2.64	1	0.05	170	13.1	137	16.0	138	14.6
0.6	2.64	1	0.05	190	8.1	192	7.5	191	7.1
0.2	10.16	1	0.05	166	6.8	135	7.8	135	8.6
0.9	10.16	1	0.05	188	3.7	181	3.2	180	3.4
0.2	0.76	1.4	0.05	128	19.0	102	31.6	100	26.2
0.2	2.64	1.4	0.05	172	13.2	137	15.8	139	14.6
0.6	2.64	1.4	0.05	192	8.1	192	7.5	191	6.8
0.2	10.16	1.4	0.05	168	6.9	135	7.8	136	8.6
0.9	10.16	1.4	0.05	190	3.7	181	3.2	180	3.3
0.2	0.76	0.6	0.5	112	16.9	89	23.6	84	23.4
0.2	2.64	0.6	0.5	149	9.9	121	12.3	115	11.8
0.6	2.64	0.6	0.5	166	5.3	167	6.1	140	5.7
0.2	10.16	0.6	0.5	145	4.9	118	6.3	112	7.1
0.9	10.16	0.6	0.5	160	2.8	155	2.4	120	3.0
0.2	0.76	1	0.5	112	16.9	89	23.6	87	24.2
0.2	2.64	1	0.5	149	9.9	121	12.3	120	12.4
0.6	2.64	1	0.5	165	5.4	167	6.1	157	5.8
0.2	10.16	1	0.5	145	4.9	118	6.3	116	6.9
0.9	10.16	1	0.5	160	2.8	154	2.4	139	2.9
0.2	0.76	1.4	0.5	113	17.0	89	23.6	88	24.3
0.2	2.64	1.4	0.5	150	10.0	121	12.3	121	12.5
0.6	2.64	1.4	0.5	166	5.4	166	6.0	163	5.7
0.2	10.16	1.4	0.5	145	4.9	118	6.3	117	6.9
0.9	10.16	1.4	0.5	159	2.8	153	2.4	148	2.9

6.1.4. NPN 1/f Noise Parameters

1/f noise obeys the classical formulation:

$$S_{ib} * f = K_F * Ib^{AF} \qquad Amps^2$$

where Ib is the device base current (A), f is the signal frequency (Hz), AF = 2, and S_{ib} is the fundamental base current noise spectral density (A^2/Hz) embedded in the hybrid-π small signal BJT model.

Description	Max.	Units
K_F*A_e	1.43E-8	
AF	2	

Where, A_e is the emitter area (in um^2)

6.2. Metal Resistors

The metal resistor is available for SBC18HX and SBC18QTR processes only. The metal resistor is physically located in the interlayer dielectric space between Metal 1 and Metal 2 in SBC18QTR and between Metal 3 and Metal 4 in SBC18HX process.

The resistor characterization, matching, voltage coefficient of resistances and temperature coefficient of resistances are available in the SBC18 analog characterization report NPB PS-0392 document.

6.2.1. Metal Resistor Resistance

$$R = \frac{Rs \cdot L}{W + \Delta W} + \frac{Rend}{W + \Delta W}$$

Description	Min.	Nom.	Max.	
Sheet Resistance – Rs	21	24.5	28	ohm/sq
End Resistance – Rend	5	12	19	ohm-um
Delta W	-0.05	-.03	-.01	um
Linear temperature coefficient of resistance TC1*		556.8		ppm/°C
Quadratic temperature coefficient of resistance TC2*		-0.158		ppm/°C^2

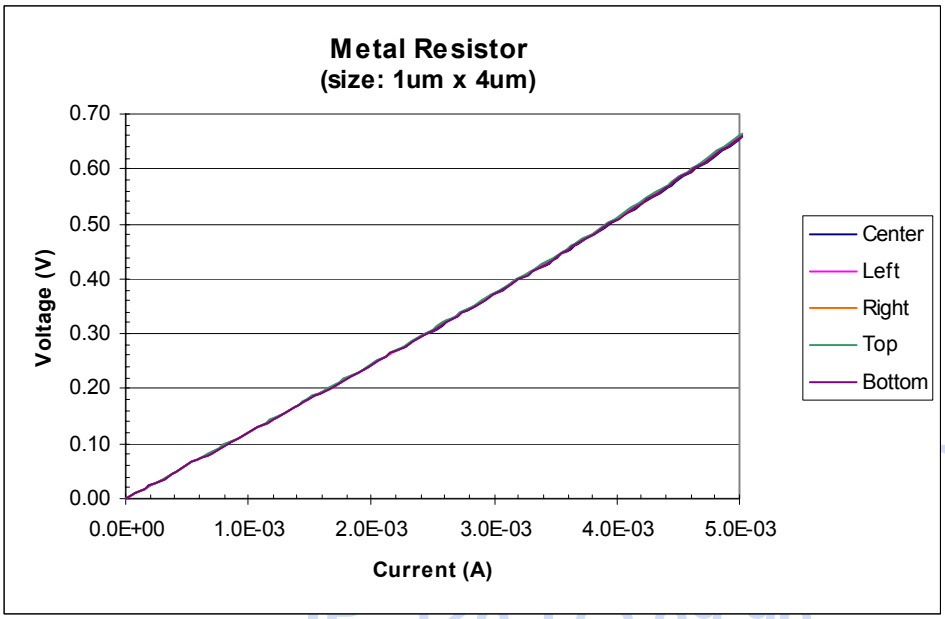
* Note: The TCR of a resistor is modeled as TC_1 and TC_2 as in following equation :

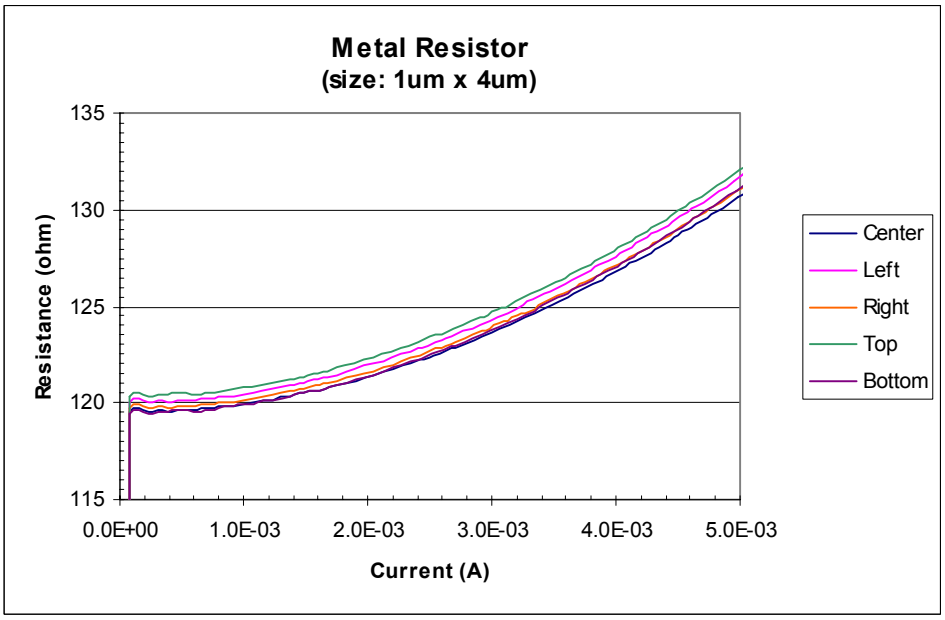
$R = R_0 *(1 + TC_1\Delta T + TC_2\Delta T^2)$

6.2.2. Maximum Current Density and Temperature Rise for Metal Resistors (Steady State):

Description	Min.	Nom.	Max.	Units
Jmax (Steady State)_preliminary * (based on 1% resistance change in size width=1.0um and Length=4.0um)			1	mA/μm

* The limitation for maximum steady state current density ,Jmax (mA/um), appears to be caused primarily by the change in temperature due to ohmic heating. Based on TCR data, 20°C temperature change which is an acceptable criterion for electromigration (EM) stress gives 1% resistance change





6.3. Low Value Unsilicided P-poly Resistors

The low value unsilicided poly resistor is available for all SBC18 processes

The resistor characterization, matching, voltage coefficient of resistances and temperature coefficient of resistances are available in the SBC18 analog characterization report NPB PS-0392 document.

6.3.1. Low Value Unsilicided P-type Poly Resistor Resistance

$$R = \frac{Rs \cdot L}{W + \Delta W} + \frac{Rend}{W + \Delta W}$$

Description	Min.		Max.	Units
Sheet Resistance – Rs	205	235	265	Ω/ □
End Resistance (Both Ends) – Rend	30	60	90	Ω - μm
Delta W	-0.04	0	0.04	μm
Linear temperature coefficient of resistance TC1*		-23.79		ppm/°C
Quadratic temperature coefficient of resistance TC2*		0.48		ppm/°C^2

* Note: The TCR of a resistor is modeled as TC_1 and TC_2 as in following equation :

$R = R_0 *(1 + TC_1\Delta T + TC_2\Delta T^2)$

6.3.2. Maximum Current Density for Low Value Unsilicided Poly Resistors

Low Value Unsalicided P-poly resistors

Description	Min.	Nom.	Max.	Units
Jmax (Steady State)			1.3	mA/μm

6.3.3. Maximum Temperature Rise for Poly Resistors (Steady State)

For P-poly resistors

Single resistor (no similar resistor within 5 um)

$\Delta T <= 0.26 * Rs * Jmax^2$ °C

Multiple resistors (similar resistor within 5 um)

$\Delta T <= 0.52 * Rs * Jmax^2$ °C

where, Rs = low value unsalicided poly sheet resistance (Ohm/square)
Jmax = maximum steady state current density (mA/um)

6.4. High Value Unsilicided Poly Resistors

The high value unsilicided poly resistor is available for SBC18PT, HA, QTD, QTE, QTR, QTL, QW, MW, MV, MWD processes only.

The resistor characterization, matching, voltage coefficient of resistances and temperature coefficient of resistances are available in the SBC18 analog characterization report NPB PS-0392 document.

6.4.1. High Value Unsilicided Poly Resistor Resistance

$$R = \frac{Rs \cdot L}{W + \Delta W} + \frac{Rend}{W + \Delta W}$$

Description	Min.	Nom.	Max.	Units
Sheet Resistance – Rs	850	1000	1150	Ω/ ☐
End Resistance (Both Ends) – Rend	40	320	600	Ω - um
Delta W	-0.04	0	0.04	um
Linear temperature coefficient of resistance TC1*		-1001		ppm/°C
Quadratic temperature coefficient of resistance TC2*		1.873		ppm/°C^2

* Note: The TCR of a resistor is modeled as TC_1 and TC_2 as in following equation :

$R = R_0 *(1 + TC_1\Delta T + TC_2\Delta T^2)$

6.4.2. Maximum Current Density for High Value Unsilicided Poly Resistors

Description	Min.	Nom.	Max.	Units
Jmax (Steady State)			0.2	mA/μm

6.5. Salicided P-poly Resistors

The silicided p-poly resistor is available for all SBC18 processes

The resistor characterization, matching, voltage coefficient of resistances and temperature coefficient of resistances are available in the SBC18 analog characterization report NPB PS-0392 document.

6.5.1. Salicided P-poly Resistor Resistance

$$R = \frac{Rs \cdot L}{W + \Delta W} + \frac{Rend}{W + \Delta W}$$

Description	Min.	Nom.	Max.	Units
Sheet Resistance – Rs	4.2	5.5	6.8	Ω/ ☐
End Resistance (Both Ends) – Rend	5.2	7.2	9.2	Ω - um
Delta W	-0.04	-0.02	0	um
Linear temperature coefficient of resistance TC1*		3089		ppm/°C
Quadratic temperature coefficient of resistance TC2*		0.982		ppm/°C^2

* Note: The TCR of a resistor is modeled as TC_1 and TC_2 as in following equation :

$R = R_0 *(1 + TC_1\Delta T + TC_2\Delta T^2)$

6.5.2. Maximum Current Density for Salicided Poly Resistors

Description	Min.	Nom.	Max.	Units
Jmax (Steady State)			1.3	mA/μm

6.6. Nwell Resistors

The n-well resistor is available for all SBC18 processes

The resistor characterization, matching, voltage coefficient of resistances and temperature coefficient of resistances are available in the SBC18 analog characterization report NPB PS-0392 document.

6.6.1. Nwell Resistor Resistance.

$$R = \frac{Rs \cdot L}{W + \Delta W} + \frac{Rend}{W + \Delta W}$$

Description	Min.		Max.	Units
Sheet Resistance – Rs	710	890	1070	Ω/ □
End Resistance (Both Ends) – Rend	450	680	900	Ω - um
Delta W	-0.17	-0.45	-0.72	um
Linear temperature coefficient of resistance TC1*		3552		ppm/°C
Quadratic temperature coefficient of resistance TC2*		10.5		ppm/°C^2

* Note: The TCR of a resistor is modeled as TC_1 and TC_2 as in following equation :

$R = R_0 *(1 + TC_1 \Delta T + TC_2 \Delta T^2)$

6.7. Vertical Metal-Insulator-Metal (MIM) Capacitors (1fF/μm^2 density)

These vertical MIM capacitors are TM to Metal 4 capacitors with a thin nitride film as the dielectric. These capacitors are available for SBC18HX , SBC18HXL, and SBC18HKL, processes only.

Description	Min.	Nom.	Max.	Units
Area Capacitance	0.85	1.0	1.15	fF/μm^2
Perimeter Capacitance	.07	0.1	.13	fF/μm
Linear Voltage Coefficient (LVCC), polarity with bias on TM plate	-25	-12	0	ppm/V
Quadratic Voltage Coefficient (QVCC)	0	5	10	ppm/V^2
Temperature Coefficient	TBD	36	TBD	ppm/°C
Absolute Applied Voltage Bias			6	V
Leakage current @25C, 10V (area: 60,000um^2)			10	nA

The following cannot be directly measured and is for design guidelines only (for SBC18HX, SBC18HXL, SBC18HKL only).

Leakage current @25C, 3.3V (area: 60,000um^2)		10		pA

The capacitor characterization, matching, voltage coefficient of resistances and temperature coefficient of resistances are available in the SBC18 analog characterization report NPB PS-0392 document.

6.8. Vertical Metal-Insulator-Metal (MIM) Capacitors (2fF/μm^2 density)

These vertical MIM capacitors are TM to Metal 2 capacitors with a thin nitride film as the dielectric. These capacitors are available for SBC18PT,PTA, QTD, QTE, QTR, QTL, QW, MW, MWD processes only.

Note: SBC18PT,PTA, QTD, QTE, QTR, QTL, QW, MW, MV, MWD processes only

Description	Min.	Nom.	Max.	Units
Area Capacitance	1.7	2.0	2.3	fF/μm^2
Perimeter Capacitance (for SBC18QTD, QTE,QTR, QTL, QW, MW, MV, MWD only)	0.115	0.23	0.345	fF/μm
Perimeter Capacitance (for SBC18PT,PTA only)	0.2	0.4	0.6	fF/μm
Linear Voltage Coefficient (LVCC), polarity with bias on TM plate.	-60	-40	-20	ppm/V
Quadratic Voltage Coefficient (QVCC)	0	20	40	ppm/V^2
Temperature Coefficient	TBD	20	TBD	ppm/°C
Absolute Applied Voltage Bias			5	V
Leakage current @25C, 10V (area: 60,000um^2)			10	nA

The following cannot be directly measured and is for design guidelines only (for SBC18PT,PTA, QTD,QTE QTR, QTL, QW, MW, MV, MWD only).

Leakage current @25C, 3.3V (area: 60,000um^2)		10		pA

The capacitor characterization, matching, voltage coefficient of resistances and temperature coefficient of resistances are available in the SBC18 analog characterization report NPB PS-0392 document.

6.9. Stacked Vertical Metal-Insulator-Metal (MIM) Capacitors (4fF/μm^2 density)

These stacked vertical MIM capacitors are TM2 to Metal 3 capacitors stacked on top of TM to Metal 2 capacitors. Each of the capacitors has a thin nitride film as the dielectric. These capacitors are available for SBC18PT,PTA, and SBC18QW processes only.

Note: SBC18PT, PTA,QW processes only

Description	Min.	Nom.	Max.	Units
Area Capacitance	3.4	4.0	4.6	fF/μm^2
Perimeter Capacitance (for SBC18QW only)	0.2	0.4	0.6	fF/μm
Perimeter Capacitance (for SBC18PT,PTA only)	0.4	0.6	0.8	fF/μm
Linear Voltage Coefficient (LVCC), polarity with bias on TM plate.	-20	0	20	ppm/V
Quadratic Voltage Coefficient (QVCC)	0	20	40	ppm/V^2
Temperature Coefficient	TBD	20	TBD	ppm/°C
Absolute Applied Voltage Bias			5.0	V
Leakage current @25C, 10V (area: 60,000um^2)			10	na

6.10. Vertical Metal-Insulator-Metal (MIM) Capacitors (2.8fF/μm^2 density)

These vertical MIM capacitors are TM to Metal 4 capacitors with a thin nitride film as the dielectric. These capacitors are available in SBC18HA only.

Description	Min.		Max.	Units
Area Capacitance	2.34	2.75	3.16	fF/μm^2
Perimeter Capacitance	0.05	0.15	0.25	fF/μm
Linear Voltage Coefficient (LVCC), polarity with bias on TM plate	-70	-50	-30	ppm/V
Quadratic Voltage Coefficient (QVCC)	0	20	40	ppm/V^2
Temperature Coefficient		20		ppm/°C
Absolute Applied Voltage Bias			3.6	V
Leakage current @25C, 3.6 V (area: 60,000um^2)			10	nA

6.11. Stacked Vertical Metal-Insulator-Metal (MIM) Capacitors (5.6fF/μm^2 density)

These stacked vertical MIM capacitors are TM2 to Metal 3 capacitors stacked under TM to Metal 4 capacitors. Each of the capacitors has a thin nitride film as the dielectric. These capacitors are available in the SBC18HA process only.

Description	Min.	Nom.	Max.	Units
Area Capacitance	4.68	5.5	6.33	fF/μm^2
Perimeter Capacitance	0.1	0.3	0.5	fF/μm
Linear Voltage Coefficient (LVCC), polarity with bias on TM plate	-10	0	10	ppm/V
Quadratic Voltage Coefficient (QVCC)	0	20	40	ppm/V^2
Temperature Coefficient		20		ppm/°C
Absolute Applied Voltage Bias			3.6	V
Leakage current @25C, 3.6 V (area: 60,000um^2)			20	nA

6.12. FET 1/f Noise

6.12.1. FET 1/f Noise Parameters

Two noise models for 1/f noise are provided. Note that AF has different meanings in the two models.

Model 1: `BSIM3 NOIMOD = 4`

Sidn = $(K_F * Id^{AF})/(Cox * Leff^2 * f^{EF})$

Description	**1.8V FETs** **(for SBC18HX, HXL, HA, PT,PTA processes only)**	**3.3V FETs**	
	Max.	**Max.**	**Units**
AF NFET	1.0	1.0	
K_F NFET (Gate area >1.5 μm^2)	7.6 x10^{-28}	7.6 x10^{-28}	Amp*F
EF NFET	1.0	1.0	
AF PFET	1.0	1.0	
K_F PFET (Gate area >1.5 μm^2)	2.5 x10^{-28}	1.1 x10^{-28}	Amp*F
EF PFET	1.0	1.0	

Model 2: HSPICE NLEV = 2, 3

Sidn = $K_F * gm^2/(Cox * W * L * f^{AF})$

Description	**1.8V FETs** **(for SBC18HX, HA, HXL, PT,PTA processes only)**	**3.3V FETs**	
	Max.	**Max.**	**Units**
AF NFET	1.0	1.0	
K_F NFET (Gate area >1.5 μm^2)	1.35 x10^{-24}	2.21x10^{-24}	FV^2
AF PFET	1.0	1.0	
K_F PFET (Gate area >1.5 μm^2)	2.15 x10^{-24}	1.45 x10^{-24}	FV^2

Note: All data in Model 2 are derived from Model 1.

6.13. Varactors

6.13.1. High performance Junction Varactor

This varactor uses an additional VR implant mask layer.
This varactor is available for SBC18HX, HXL, HA, PT, QTD, QTE, QTR, QTL, MV, MWD processes only.
All parameters are for 1.4 um wide, 30 um long varactor with 20 fingers.

Description	Min.	Nom.	Max.	Units
Capacitance@ 0 V (pF)	1.7	2.0	2.3	pF
Capacitance Sensitivity* (%/V)	26	28	30	%/V
Q (1.9GHz at 0.5 V)	50	80		
Leakage current at 2.5 V			5	nA

* Capacitance Sensitivity = (Cap @ 0.5V - Cap @ 2.5V)/(Cap @ 0.5V + Cap @ 2.5V)

6.13.2. P+/Nwell Junction Varactor

This varactor is made by the N-well/PFET source/drain junction.
This varactor is available for SBC18MW, QW processes only.
All parameters are for 1.4 um wide, 30 um long varactor with 20 fingers.

Description	Min.	Nom.	Max.	Units
Capacitance@ 0 V (pF)	0.73	0.86	0.99	pF
Capacitance Sensitivity* (%/V)	9.2	10.6	12.0	%/V
Q (1.9GHz at 0.5 V)	50			
Leakage current for 20x1.4X30 device at 2.5 V			500	pA

* Capacitance Sensitivity = (Cap @ 0.5V - Cap @ 2.5V)/(Cap @ 0.5V + Cap @ 2.5V)

6.13.3. MOS Varactor

This varactor is made by the N+ Poly and gate oxide over Nwell
This varactor is available for SBC18HXL, SBC18HX, SBC18HKL, HA, and SBC18PT,PTA processes only which have the thin 1.8V FET gate oxides.

Description	Min.		Max.	Units
Capacitance@ 1 V (pF) for 3 x 0.5 x 15 x 25 device	TBD	5.63	TBD	pF
Capacitance Sensitivity* (%/V)	60.9	72.5	84.1	%/V
Q (1.9GHz at 1 V) for 3 x 0.5 x 2 x 10 device	75	100		
Q (5GHz at 1 V) for 3 x 0.5 x 2 x 10 device	30	40		
Q (10GHz at 1 V) for 3 x 0.5 x 2 x 10 device	15	20		

* Capacitance Sensitivity = 2*(Cap @ 0.5V - Cap @ -0.5V)/(Cap @ 0.5V + Cap @ -0.5V)

6.14. Metal Fuses

The metal fuse is fabricated from metal (N-2).

In SBC18HX,HXL, HKL, HA processes the fuse metal is metal 4
In SBC18PT,PTA processesthe fuse metal is metal 3
In SBC18QTD, QTE, QTR, QTL, QW processes the fuse metal is metal 2
In SBC18MW, MV, MWD no fuses are available

Fuse programming
A 3 Volt pulse (width = 5 msec) with current limit of 500mA is used to program the metal fuse.

Description	Min.		Max.	Units
J (Fuse Programming Current)		350		mA/μm

Note: The fuse programming rating is to be used only during fuse programming pulses. Adequate contacts, Vias, and metal line widths should be used to handle current flow during programming.

The fuse is 5um long by 1um wide.

6.14.1. Metal Fuse Resistance

Description	Min.	Nom.	Max.	Units
R_{fuse} (before blowing)		0.4 note 1		Ohms
R_{fuse} (after blowing)	1.0			MegaOhms

Note 1: If measured between probe pads, approx 4.5 ohm nominal value is measured. This value includes parasitic probe resistance.

6.14.2. Metal Fuse Temperature Coefficient of Resistance

Description	Min.	Nom.		Units
TCR R_{fuse}		4000		ppm/C

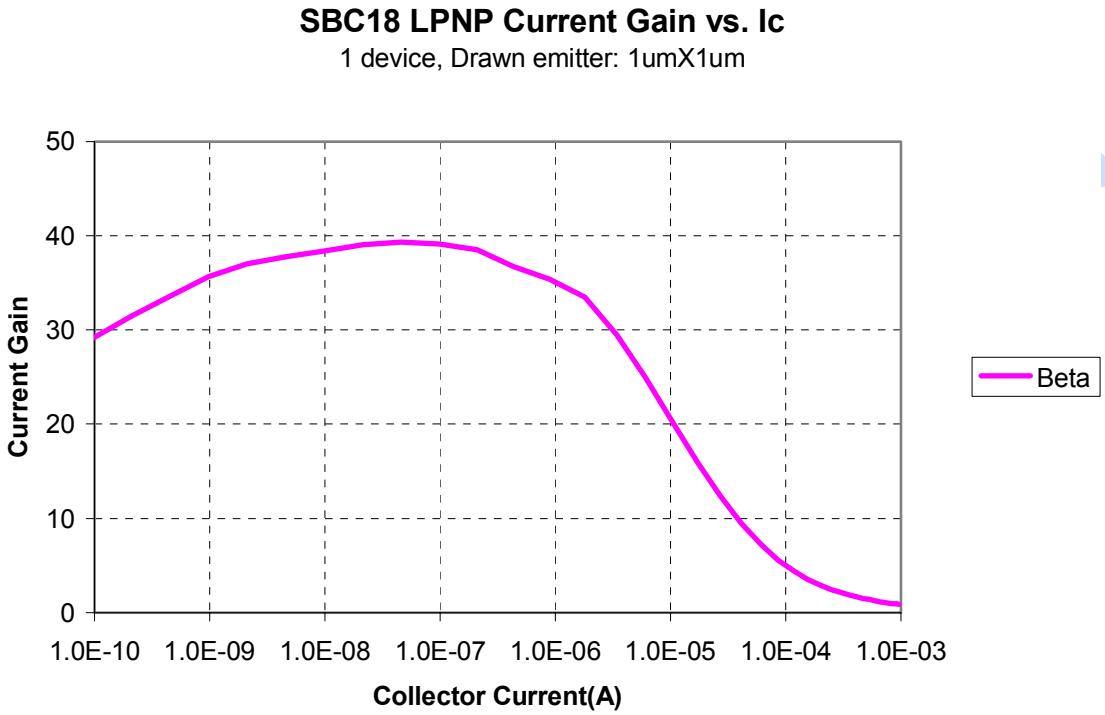
6.15. PNP Transistors

6.15.1. Lateral PNP Transistors

All lateral PNP parameters are given for an emitter area of 8 x (1.0 um x 1.0 um)

Description	Min.	Nom.	Max.	Units
Beta (Ie=10 uA)	20	32	58	
Va (Ic = 10uA)	20			V
Bvceo	6			V
Bvebo	6			V
Bvcbo	6			V

A typical current gain versus Ic plot is provided below



1/f Noise in Lateral PNP

1/f noise obeys the classical formulation:

$$S_{ib} * f = K_F * Ib^{AF} \qquad Amps^2$$

where Ib is the device base current (A), f is the signal frequency (Hz), AF = 1.75, and S_{ib} is the fundamental base current noise spectral density (A^2/Hz) embedded in the hybrid-π small signal BJT model.

Description	Max.	Units
K_F	1.14e-11	
AF	1.75	

Mismatch in Lateral PNP

The Ic mismatch of PNPs in a pair is summarized below. The data here is preliminary characterization data only and is subject to change.

Array size:	Vce=-.5	Vce=-1	Vce=-1.5	Vce=-2	Je (uA/ per unit)
2x32	0.97	1.02	0.99	1.03	Jc=-.1
2x4	1.25	1.29	1.33	1.37	Jc=-.1
2x32	2.13	2.15	2.18	2.25	Jc=-1.0
2x4	4.36	4.38	4.39	4.40	Jc=-1.0
2x32	5.97	5.98	5.99	6.00	Jc=-10.0
2x4	11.58	11.58	11.59	11.58	Jc=-10.0

The current gain mismatch of PNPs in a pair is summarized below. The data here is preliminary characterization data only and is subject to change.

Array size:	Vce=-.5	Vce=-1	Vce=-1.5	Vce=-2	Je (uA/ per unit)
2x32	0.74	0.70	0.72	0.75	Jc=-.1
2x4	1.49	1.48	1.52	1.53	Jc=-.1
2x32	0.60	0.63	0.65	0.68	Jc=-1.0
2x4	1.04	1.11	1.16	1.19	Jc=-1.0
2x32	0.95	1.12	1.23	1.38	Jc=-10.0
2x4	1.27	1.31	1.33	1.35	Jc=-10.0

6.15.2. Vertical PNP Transistors

All vertical PNP parameters are given for an emitter area of 25.0 um x 25.0 um

Description	Min.	Nom.	Max.	Units
Beta (Ie=10 uA)	2.5	3.5	4.5	
Va	100			V
BVceo	12	15	18	V
BVebo	10	12	14	V
BVcbo	12	15	18	V

6.16. Deep N Well Specifications for Triple Well Isolation

These parameters are applicable to SBC18HXL, HKL and SBC18QTL processes only

6.16.1. Breakdown voltages

Description	Min.	Nom.	Max.	Units
Deep Nwell to isolated pwell junction	6			Volts
Deep nwell to p-substrate junction	6			Volts

6.16.2. Deep Nwell Resistances

Description	Min.	Nom.	Max.	Units
Sheet Resistance*		470		ohm/sq
End Resistance*		3400		ohm-um
Delta W		0.3		um

*Total Resistance = [L / (W + Delta W)] * Sheet Resistance + End Resistance /(W + Delta W)

6.16.3. Deep Nwell Capacitances

Description	Min.	Nom.	Max.	
Area capacitance deep nwell to isolated pwell junction		546.6		uF/m^2
Sidewall capacitance deep nwell to isolated pwell junction		1.346		nF/m
Area capacitance deep nwell to p-substrate junction		126.7		uF/m^2
Sidewall capacitance deep nwell to p-substrate junction		3.124		nF/m

6.17. Schottky Diodes

The Schottky diode is formed between the unimplanted silicide to n-epi junctions.
The Schottky diode is available in the SBC18QTR, SBC18HXL, SBC18HKL and SBC18HA processes only
The following specifications are for a 5um x 5um device

Description	Min.	Nom.	Max.	
Von	0.36	0.42	0.48	Volts
Leakage current (@Vr = 3.3V)			1	nA
Breakdown voltage	9			Volts
Capacitance	15.0	16.5	18.0	fF/μm^2
Rs		100		ohm

6.18. Polyimide Overcoat

The polyimide overcoat is added on top of the oxide/nitride passivation overcoat for some process variants with greater than 2.5um thick top metal. The polyimide overcoat helps to improve the top planarization of the finished wafers even with the thick patterned top metal features. See Illustration POLYIMIDE.

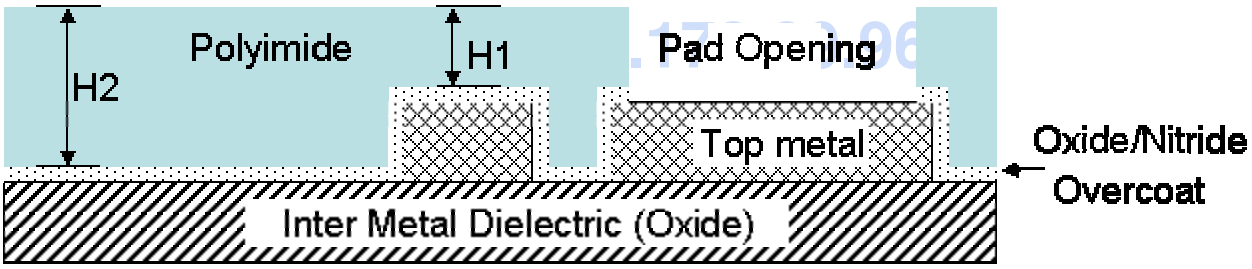


ILLUSTRATION POLYIMIDE

Process variants with polyimide overcoat are identified by the addition of the letter “Z” at the end of the process name. For example, the polyimide overcoat process variant of the process SBC18HX would be called SBC18HXZ process.

6.18.1. Dielectric Thicknesses for processes with polyimide overcoat

Description (for SBC18**Z processes only)	Min.	Nom.	Max.	Units
Overcoat oxide thickness*Ŧ	1.80	2.00	2.20	Kangstroms
Overcoat nitride thickness*	5.40	6.00	6.60	Kangstroms
Polyimide Passivation thickness on top metal (see H1 in Illustration POLYIMIDE) ** **(Applicable to all process variants with ~ 2.8um thick top metal)**	6	23	40	Kangstroms
Polyimide Passivation thickness not on top metal (see H2 in Illustration POLYIMIDE) ** **(Applicable to all process variants with ~2.8um thick top metal)**	20	45	70	Kangstroms
Polyimide Passivation thickness on top metal (see H1 in Illustration POLYIMIDE) ** **(Applicable to all process variants with ~ 5.2um thick top metal)**	6	34	62	Kangstroms
Polyimide Passivation thickness not on top metal (see H2 in Illustration POLYIMIDE) ** **(Applicable to all process variants with ~ 5.2um thick top metal)**	45	70	95	Kangstroms

* The thicknesses of the conformally deposited overcoat oxide and overcoat nitride at the sidewall of the top metal layer are about 70% of the thickness at the top of the topmost metallization layer. The gap between two adjacent metal lines at the topmost metallization layer, remaining beyond the sidewall overcoat dielectrics, is typically filled by resins used in packaging.
Ŧ The nominal overcoat thickness for SBC18MVZ is 4.00 KÅ. Min and max are 3.6 and 4.4 KÅ respectively.
** The thickness specification is valid at a distance of at least 10um from any metal edge

6.18.2. Dielectric Constant of polyimide

Description	Min.	Nom.	Max.	Units
Polyimide		3.0		ε/ε0