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TITLE:

SBC18 ESD Design Manual

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TABLE OF CONTENTS

Overview

Various real-world electrostatic discharge (ESD) events can cause large, potentially destructive currents to flow thru the pins of integrated circuits. IC products must usually carry a certain level of on-chip ESD protection to survive these stresses, and this is evaluated by standardized testing along with other quality requirements.

Mainstream component-level laboratory tests include the Human Body Model (HBM), the Charged Device Model (CDM) and the Machine Model (MM). Good overall product ESD quality is usually demonstrated by a combination of acceptable HBM and CDM, or HBM and MM ratings. However, only the HBM reliability of products can be predicted to first order based on schematic and layout information. A typical HBM reliability goal for products is to pass 2000V HBM and 1000V HBM for stress combinations involving regular and high performance pins. Jazz is committed to providing customers with guidelines and engineering data relevant to meeting this goal.

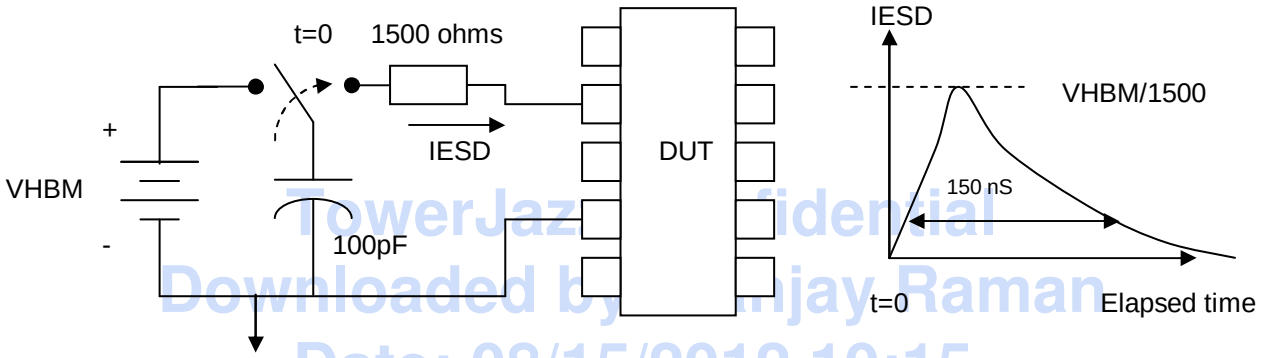
This document describes a methodology, standard devices and data to support favorable design of on-chip ESD protection circuitry for the HBM. Certain key schematic and layout requirements cannot be verified by layout DRC evaluation and must be checked manually. Otherwise, the passivation of parasitic devices that could defeat the ESD circuit is checked by the latch-up DRC rules.

Guidelines to meet specific MM or CDM ratings cannot be defined because product responses to MM/CDM testing are complex and may depend on off-chip factors. However, some general recommendations are suggested.

Definition and Countermeasures for the Human Body Model

In the HBM test, a 100pF external capacitor charged to a static voltage (VHBM) is discharged across pairs of designated package pins thru a 1500ohm external series resistor. This is shown in the figure below. All uninvolved package pins are floating; including pins that are normally connected to power and ground. A typical HBM test plan will involve stressing all possible pairs of pins under a given VHBM level. Component failure is usually determined by circuit non-functionality after all stresses on a part are completed.

Achieving a product passing rating of 1000-2000V HBM is a common goal because ESD events of that level are not readily detectable by human beings but have a significant destructive capability and can easily occur in poorly regulated product handling environments.



Unless the DUT impedance between the pins being tested is significant relative to 1500 ohms, a HBM strike usually results in a double-exponential discharge waveform with a consistent peak current, rise time and pulse width of approximately VHBM/1500 ohms, 1-10nS, and 150 nS. Neither parasitic-type series inductance nor shunting capacitance is usually factored into HBM analyses, because they typically do not strongly affect the peak current to first order.

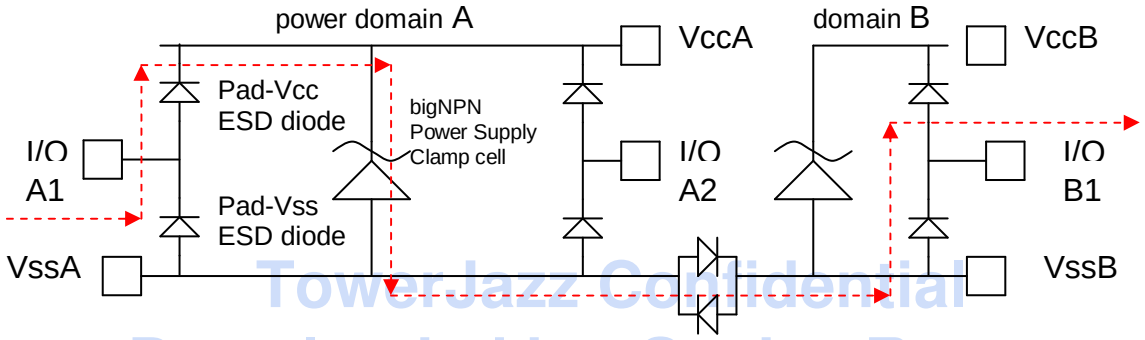
This is the case for pins connected to reasonable implementations of an on-chip ESD network and is why product response to HBM events can be engineered if the IV characteristics and failure thresholds of the ESD circuit and signal paths are known.

On-chip ESD protection circuits generally consist of a network of discharge paths connecting all bonding pads wired to package pins. In response to a HBM strike, this discharge network carries excess pin-pin test current that does not flow thru signal or parasitic paths. In the best case, the network will conduct most of the pin-pin test current and clamp voltages across the signal paths to safe values. If relevant data is available, simple calculations can be used to ensure this to first order.

The standby characteristics of the network should be nominal (not leaky or restrict the voltage travel of IO pins). This means that it may be necessary to compromise ESD protection for certain pins with large voltage travel. By the same token, it may be possible to tighten the ESD circuit for pins with reduced voltage travel (such as bipolar inputs in the common emitter configuration).

Protection for Custom Mixed Signal Circuits

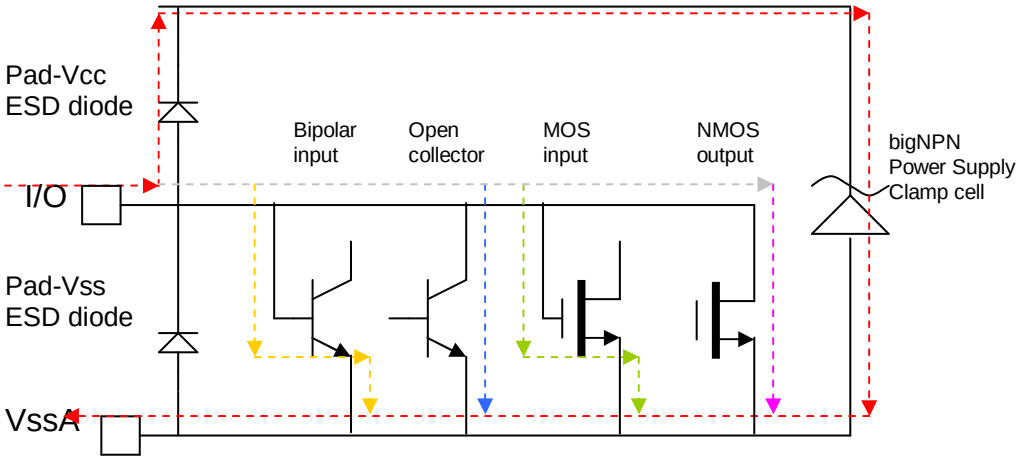
The basic protection network recommended for most mixed signal applications is shown below. ESD diodes are used to couple test currents from the IO pins to the power domain rails, and transiently-triggered "bigNPN" clamp cell(s) route currents from rail to rail as necessary. The idealized discharge path for HBM current entering an IO pin of one domain (A) and leaving an IO pin of another (B) is shown in red (signal paths are not shown). To enable discharge paths between all pins on the chip, a metallized connection is required between isolated power domain grounds, using cross-coupled ESD diodes to provide noise or substrate isolation if necessary. Multiple grounds can be daisy-chained serially if IO circuitry is not connected across different domains, but it is preferable to connect the grounds in a star pattern to minimize pin-pin voltages during cross domain strikes.



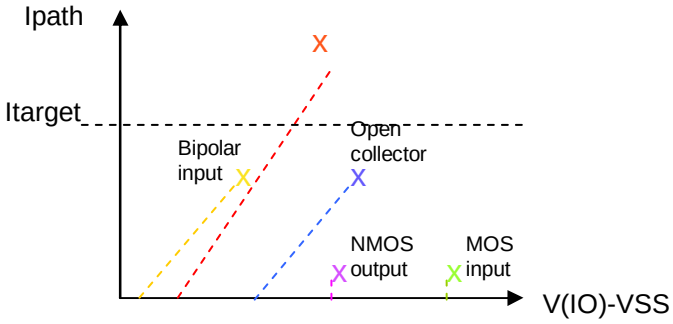
Basic on-chip ESD protection scheme. Discharge current is routed from pin to pin thru series combinations of ESD diodes and power supply clamps, using cross-coupled ESD diodes between grounds to provide noise isolation, if necessary.

Aside from two basic layout requirements for the discharge paths: 1) metal width should be greater than the equivalent of 8um of METAL1, and 2) the number of vias at each interchange should support the desired maximum ESD current (approximately 30 vias for 2KV HBM); favorable implementation of the Jazz-recommended ESD network is mostly a schematic design problem provided strong parasitic npn devices in the layout that might bypass the network are passivated.

The schematic below showing typical partial paths connected between an IO pad and ground illustrates how the dedicated ESD path must compete against the signal paths for discharge current. The indicated direction of current flow is consistent with a positive polarity HBM strike between IO and ground. Note that ESD analyses usually focus on positive IO-gnd and negative IO-supply stress combinations when using the recommended ESD circuit topology because they are often the worst situations from a dedicated discharge impedance point of view (the discharge path involves multiple series devices, so large pin-pin voltages can develop). Unless signal devices are connected directly between IO pads of different power domains, however, it's usually adequate to analyze these stress configurations within a given domain. For example, Vds of the NMOS in the schematic below only depends on the discharge path between IO and VSSA, not to some other power domain ground. If signal devices must be connected directly across pads of different power domains, steps should be taken to ensure that the dedicated discharge path in the ESD circuit has a reasonable chance of preventing signal path failure (eg. more clamps, star vs. daisy chained ground connections, etc.) In these cases, it may be necessary to buffer the signal path so that it can withstand higher voltage.



It's instructive to examine a conceptual plot of all partial discharge paths between the IO pin and Vss in this schematic. Each curve has an "x" indicating its point of failure. Acting in parallel, the dedicated path (red) is not able to prevent the bipolar input (orange) from conducting a significant fraction of the test current, and failure to the bipolar input itself occurs at a voltage below the voltage failure level of the ESD circuit or other partial discharge paths. However, the total current flowing thru the bipolar input and the dedicated discharge path may be sufficient for the pin to pass the targeted testing level (Itarget) without damage. Following similar arguments, if the bipolar input were not present, the dedicated discharge path as drawn should be able to safely channel most of the total test current upto the targeted testing level without allowing any of the MOS signal paths to be damaged. Making this plot is not necessary when analyzing circuits, but it's useful to keep this picture in mind.



Signal paths should ideally not carry significant currents for total pin currents corresponding to the targeted testing level (Itarget). Certain problematic paths, such as the base input, cannot be prevented from conducting significant fractions of total ESD current. Other paths, such as NMOS outputs, have a very low failure current and Vds must be kept below its failure value.

Paths such as the NMOS output are at high risk of failure if the ESD circuit is not optimized to clamp Vds below its failure value because NMOS Ids failure current can be very low in Jazz processes for arbitrary device layout. Other paths with high failure voltages, such as MOS inputs, are at low risk of failure even though their current failure thresholds are low because typical ESD protection circuits will probably limit Vgs voltage below its failure value (3.3V MOS gate oxide can survive > 16V under HBM test conditions, for example). However, it's clear that some kind of explicit discharge path must be present to shunt the oxide terminals, or destructive levels of voltage (upto the VHBM testing level) can develop across the victim device.

There is some latitude in choosing a viable topology for the on-chip ESD network. As shown in the figures below, power supply clamps can be shared between different domains by using ESD diodes (to conserve layout area; this scheme is used in the digital IO cells). To minimize noise coupling, users may daisy-chain or couple the grounds of each power domain to a common ESD ground bus (in a star configuration) instead of using a single global ground bus. For fail-safe operation, the supply side diode may be routed to an uninterruptible ESD bus that is not directly connected to the signal path circuitry. At high performance pins, the parasitic capacitance of ESD diodes can be managed by using smaller standard diodes with fewer active fingers. Series diodes can be employed to extend IO pin voltage travel or provide better protection for IO pins with reduced voltage travel.

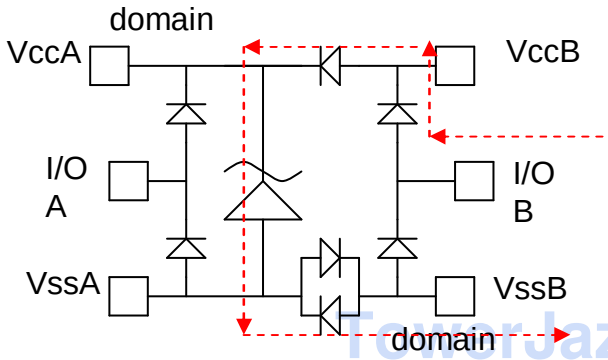


Figure_4A. Sharing ESD clamp in domain A with IO circuitry in domain B

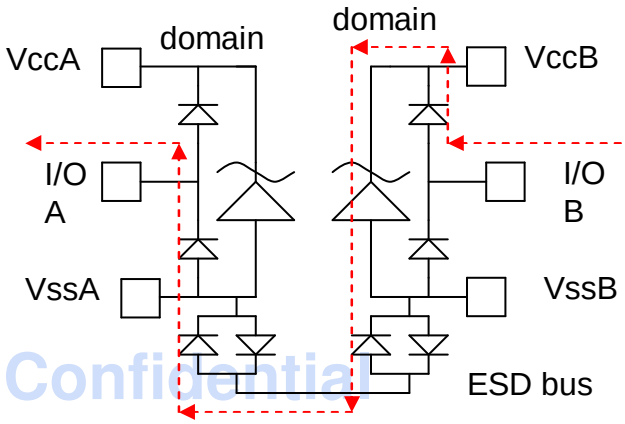


Figure_4B. Using a dedicated ESD ground bus to couple power domains

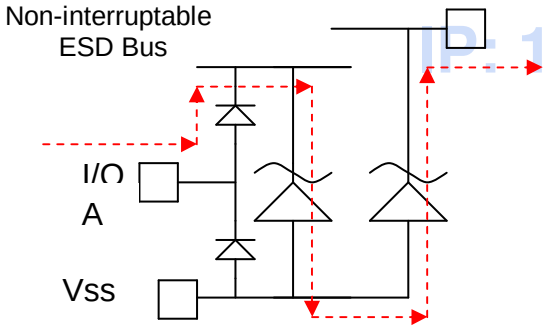


Figure 4C. ESD protection for fail-safe IO pin. (IO circuitry connected to interruptable Vcc.)

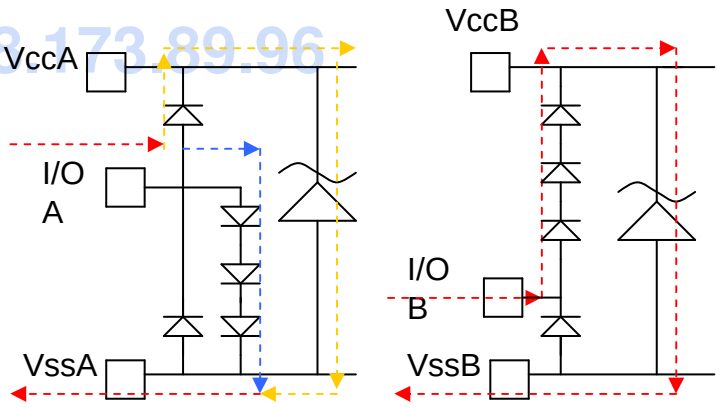


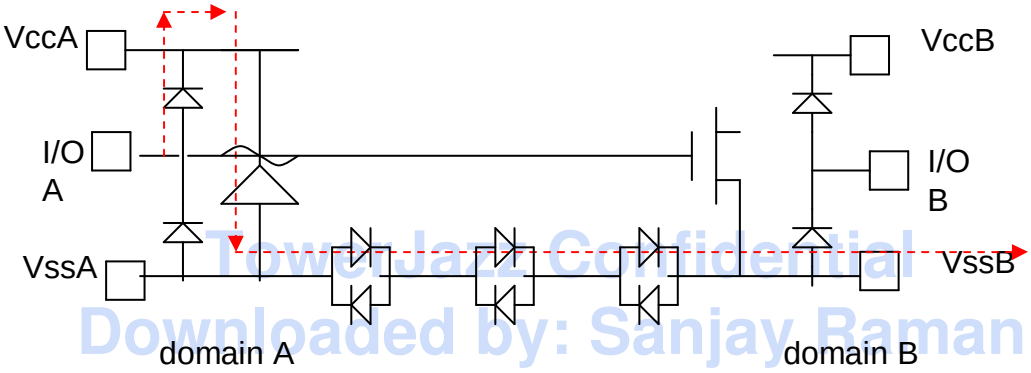
Figure 4DA and 4DB. ESD protection for pins with limited voltage travel (I/O A) or extended voltage travel (I/O B)

For special applications, it may also be possible to rely on the survivability of the signal devices themselves, or to use signal devices for ESD protection. Large devices or devices with many fingers or in large arrays can collectively have a high failure current. “Snapback” devices, or HV npn transistors with the base floating, may have certain advantageous standby behaviors compared to diode-based ESD protection schemes. However, the results of these non-standard solutions are difficult to predict to first order.

Cross domain protection and passivation of parasitic npn's

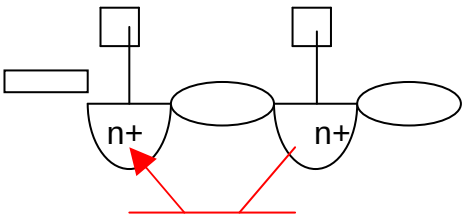
It's clear that HBM strikes across pins of different power domains can develop larger voltages than across pins belonging to the same domain, especially if a product has multiple power domains and uses cross coupled ESD diodes to isolate their grounds in an open daisy-chained fashion. This higher voltage can attack signal paths that are connected to pads in the different domains, as well as trigger parasitic npn devices connected to the pads that may not otherwise be active during lower-level HBM events associated with lower peak pin-pin voltages.

One undesirable situation occurs when signal circuitry clamped by the ESD protection network of a given power domain is actually connected to the power or ground of a different power domain. This may happen, for example, if core circuitry is connected directly to an IO pin without using a buffer.

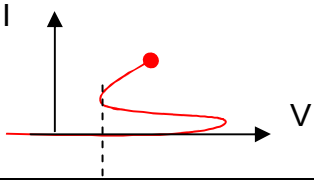


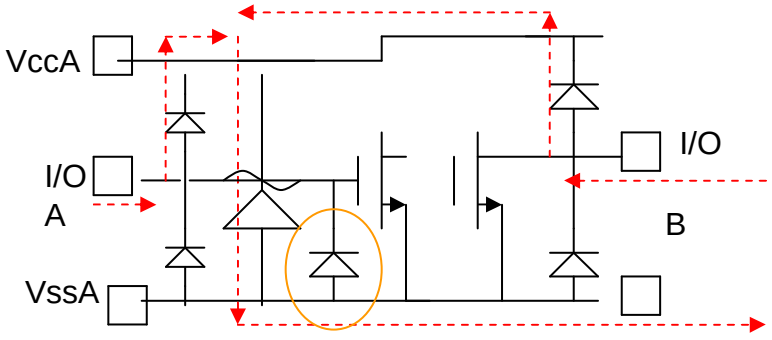
Vgs of the MOS input above is not necessarily clamped to safe levels because it is determined by multiple cross-domain ESD components and bus resistance.

Parasitic npn's are made from adjacent n-type diffusions in the same pwell. If the emitter/collector terminals are connected to pins that develop high voltage, the npn may snap-back and draw current. If the parasitic npn is strong, not passivated by body tie-downs, the device snapback holding voltage can be very low, which causes current to focus thru it instead of the ESD circuit and burn it out.



Parasitic npn cross section (above) and IV characteristics (below); dashed line represents snapback holding voltage.





Parasitic npn cross can form between cathode of n+/sub antenna diode (circled) and source of NMOS input, or between nmos open drain (B) and source of MOS input, for example.

ESD protection for digital IO cells

Some products will use IO cells from the digital library to form part of the pad ring. Certain supporting cells are required to complete the ESD circuit in such digital domains (in each padcell, IO pins are coupled to the 3V (VDDP) or 5V (VGG) supply rails thru ESD diodes but do not have any power supply clamp). In particular, corner cells (ptgcor) should be connected to the pad cells. Each corner cell has separate 5V and 3V tolerant "bigFET" power supply clamps for the VESD and VDD busses, respectively, where the corner cell VESD clamp is shared with the VDDP and VGG busses thru ESD diodes, as shown in the diagram below. Alternatively, it may be possible to connect a mixed signal bignpn cell to the VDDP or VGG rails directly.

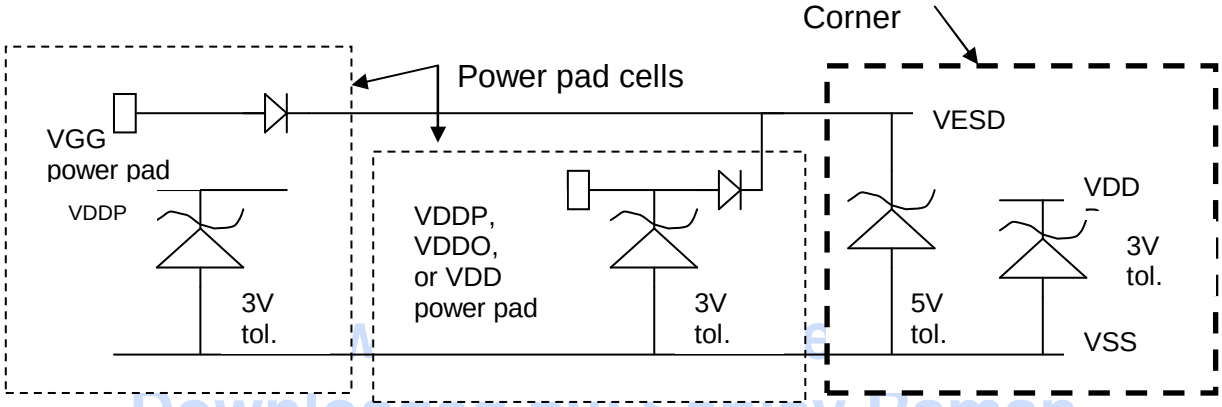


Figure 1. Schematic showing cell content and connectivity of on-chip ESD protection circuitry.
VDDO – power pad for output buffer circuitry
VDDP – power pad for pad-ring logic circuitry (level shifters, etc.)
VDD – power pad for core logic
VGG – 5V tolerant power pad
VESD – internal bus

Certain non-corner cells (power padcells and pesdclamp1) contain bigFET clamps connected to the VDDP power domain rails, but these are not rated to handle full HBM events. Furthermore, if 5V tolerant padcells are being used for 3V applications, it is advisable to shunt the VDDP and VESD power rails together, because the 3V-tolerant clamp in the corner cell is superior to the 5V-tolerant clamp. See the digital IO cell documentation for more specific connectivity information.

It's important to know that the VESD bus may be at risk of charging up after successive HBM strikes because there is no regular circuitry that will bleed accumulated residual charge. The efficiency of a transiently-triggered clamp may be reduced if the initial voltage on the sense node is large enough to turn off the driver transistor (see description of bigNPN in a later section). It's recommended to add a de-biasing resistor between the VESD bus and ground to keep the VESD discharged and ready to respond to additional ESD pulses. A long and narrow PFET transistor configured as a resistor in the mega-ohm range has been found to be beneficial.

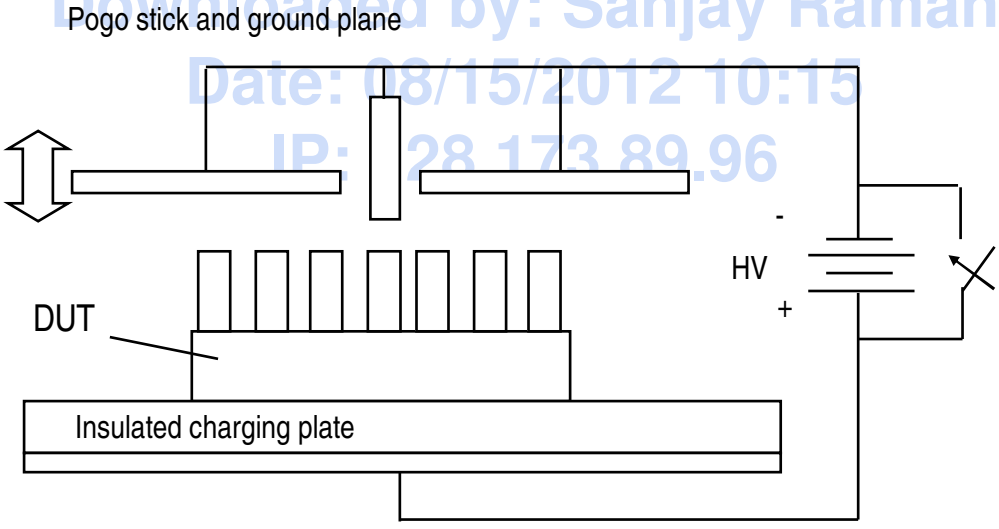
As was specified earlier, all analog and digital grounds should be coupled with a metallized path, using cross-coupled ESD diodes for noise or substrate isolation if necessary, to create a low impedance discharge path between all bonding pads wired to package pins.

Countermeasures for Machine and Charged Device Model (MM, CDM)

The external test circuit and typical testing plan for MM is similar to HBM, except that the fixed capacitor is 200pF, and the series 1500 ohm resistor is omitted. The peak magnitude and waveform of current flowing into a pair of pins is strongly influenced by the resistance looking into the pins themselves. The pulse rise time may be very sharp, such that the current waveform may be oscillatory and sensitive to the product's pin-pin input reactance. The uncertain current waveform in response to MM events makes it difficult to predict how a product will respond to a standard testing level.

Since MM testing can expose HBM type failure modes, good component-level HBM reliability can contribute to better component-level MM reliability. Since MM testing may also expose CDM type failure modes, following the recommendations for CDM in the next paragraphs may also result in better MM reliability.

In the CDM test, a part is placed dead-bug position between isolated charging plates with an applied electric field of zero (HV shorted out). Under a non-zero electric field, a single pin is grounded using a "pogo stick", resulting in charge flowing into the part to re-establish electrostatic equilibrium. The pin may be retracted and re-attached after the field is returned to zero, resulting in a bipolar stress event.



The magnitude of current depends in part on the capacitance of the circuit relative to the backside of the plate, which in influenced by die size, package form factor, etc. Since individual pulses may also have sharp rise times, series inductances in the discharge paths may develop large pin-pin voltages that can threaten dielectrics, such as gate oxides. Unlike the HBM event, where the discharge current is on the order of amps and ideally flows only thru the controlled i/o branches of the chip, CDM current can conceivably be on the order of 10's of amps, and may flow to all internal nodes as the voltages on the chip equalize.

CDM testing results are therefore very difficult to predict using simple calculations. Foundries cannot specify minimum CDM reliability targets for arbitrary product designs.

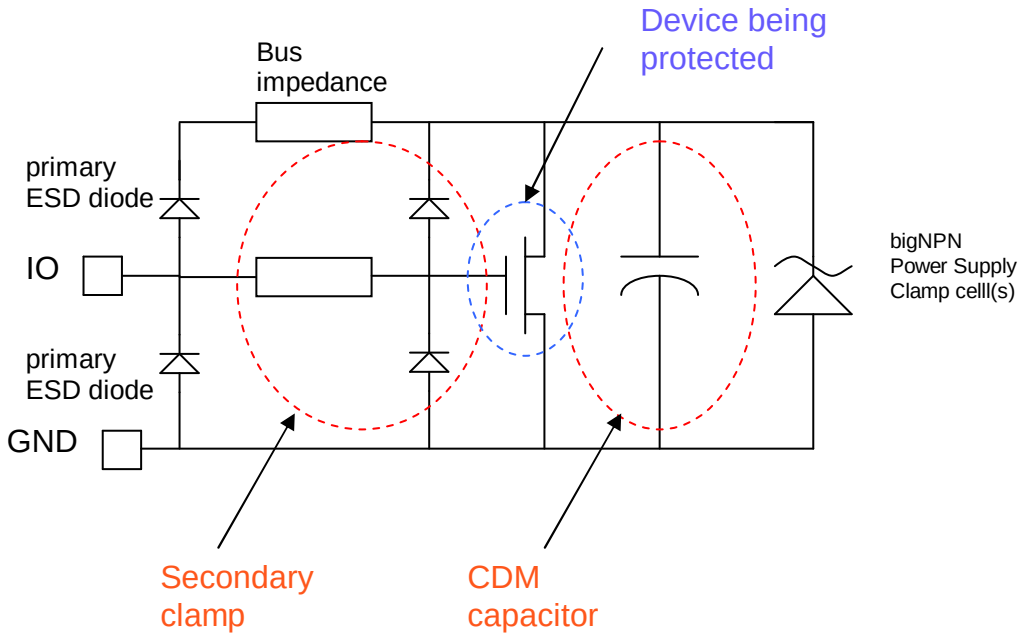
For products with smaller capacitance, total charge and peak total currents, the thermal damage (melting) caused by CDM events may not be extensive. However, higher peak currents associated with larger products may have sufficient power to enable HBM-like failure modes. This means that good component-level HBM reliability may contribute to better component-level CDM reliability.

A common goal for on-chip CDM protection is to prevent gate oxides that would ordinarily be connected directly to different bonding pads from being blown out by large pin-pin voltages. Assuming that most of the CDM current is discharged thru the traditional HBM dedicated path, “secondary clamps” (typically using small ESD diodes) should be used together with a debiasing resistor to control the voltage developed across the oxide terminals in question. This is shown in the figure below.

The resistor (typically 150 ohms nwell) limits the reverse current thru the secondary diodes, whose reverse breakdown voltage is typically lower than the oxide failure threshold. Diodes can be minimum sized, because the peak power associated with the reverse current is expected to be small. ESD diodes are good choices because they come standard with the required latch-up guard rings. It’s not advisable to use gated diodes made from standard NMOS for this application because Jazz NFET transistors tend to fail immediately after snap back and may compromise the pin’s HBM rating. In the figure below, secondary diodes shunt the IO pin to both power and ground. Strictly speaking, the secondary clamp diodes are usually only “required” for shunting oxide terminals connected directly between IO and one of the rails.

Alternatively, a series gate resistor alone can be used to enable a RC charging delay >> 1nS that prevents the dielectric from developing a damaging voltage during the stress event.

Another CDM counter measure is to use large supply capacitance to clamp the power rails. SBC18 bignpn cells have a built-in CDM capacitor, but Jazz cannot estimate whether additional supply capacitance is necessary to solve a particular CDM problem.



Typical HBM failure thresholds of signal devices

WE and LE refer to the emitter width and length, #EBC corresponds to the number of emitter, base and collector fingers. Ifail and Vfail refer to the peak device current and voltage just prior to failure.

NPN Ic-Vceo failure thresholds:

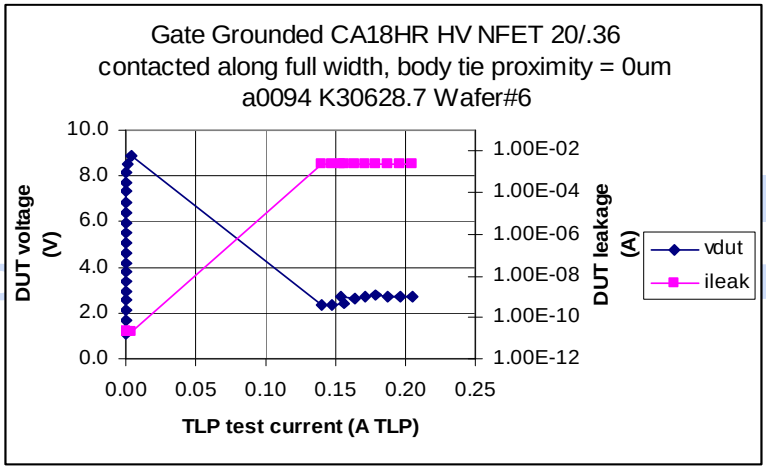
					HV npn		STD npn	
we	**le**	**#E**	**#B**	**#C**	Ifail (A)	Vfail (V)	Ifail (A)	Vfail (V)
0.2	0.76	1	1	1	0.019	7.8	0.016	7.8
0.2	1.7	1	1	1	0.027	7	0.029	7.3
0.2	0.76	1	2	1	0.013	6.9	-	-
0.2	1.7	1	2	1	0.033	7.1	0.024	7
0.2	2.64	1	2	1	0.040	7	0.036	7
0.2	4.52	1	2	1	0.065	7	0.061	7
0.2	8.28	1	2	1	0.109	7.2	0.105	7.5
0.2	10.16	1	2	1	0.131	7.5	0.125	7.7
0.3	0.76	1	2	1	0.020	7.1	-	-
0.3	10.16	1	2	1	0.147	7.3	0.131	7.5
0.4	10.16	1	2	1	0.160	7.4	-	-
0.6	4.52	1	2	1	0.093	6.8	-	-
0.6	10.16	1	2	1	0.192	7.8	0.173	7.8
0.9	10.16	1	2	1	0.253	8.1	-	-
0.2	10.16	1	2	2	0.149	7.2	0.143	7.5
0.6	10.16	1	2	2	0.207	7.2	-	-
0.9	10.16	1	2	2	0.273	7.8	-	-
0.2	10.16	2	3	2	0.277	8.1	0.247	8.2
0.6	10.16	2	3	2	0.373	8.6	-	-
0.2	10.16	4	5	2	0.480	10.5	-	-
0.6	10.16	4	5	2	0.613	11.5	-	-

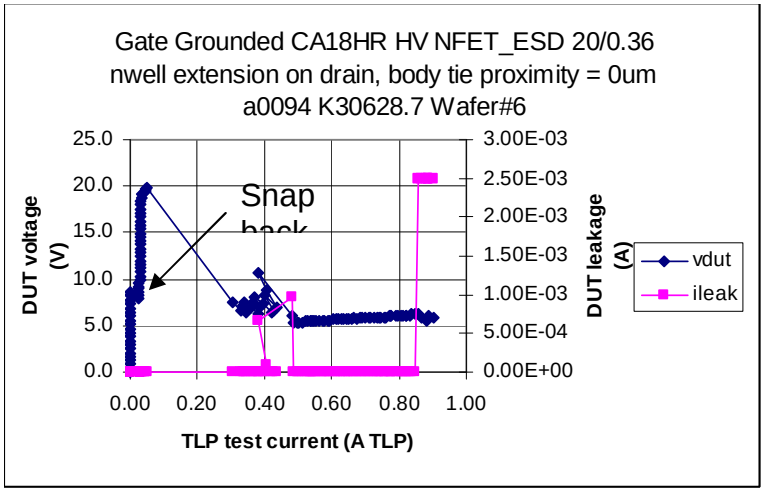
NPN Ib-Vbe failure thresholds (applicable to all NPN transistors)

we	**le**	**#E**	**#B**	**#C**	Ifail (A)	Vfail (V)
0.2	0.76	1	1	1	0.032	1.9
0.2	1.7	1	1	1	0.067	2.2
0.2	0.76	1	2	1	0.033	1.8
0.2	1.7	1	2	1	0.087	2.4
0.2	2.64	1	2	1	0.120	2.7
0.2	4.52	1	2	1	0.187	3.2
0.2	8.28	1	2	1	0.327	4.7
0.2	10.16	1	2	1	0.320	4.6
0.3	0.76	1	2	1	0.053	2.1
0.3	10.16	1	2	1	0.333	4.5
0.4	10.16	1	2	1	0.333	4.6
0.6	4.52	1	2	1	0.220	3.5
0.6	10.16	1	2	1	0.333	4.8
0.9	10.16	1	2	1	0.373	4.9

Reverse Veb and Vec stresses are expected to damage NPN transistors under low levels of testing unless they are shunted by forward biased ESD diodes. A shunting diode is always present in the recommended ESD protection network for most bipolar applications, either across bipolar transistors directly or the series combination of NPN transistor and its load.

3.3V NMOS output transistors in Jazz technologies typically do not survive Vds snap back without assistance from an NWELL resistor extension on the drain. In the figures shown below (for CA18HR), a standard gate-grounded 3.3V NMOS transistor is seen to fail immediately after snapping back. The snap back holding voltage is not resolvable in the measurement. A gate-grounded 3.3V NMOS transistor with NWELL extension has a snap back holding voltage of approximately 7V prior to developing upto 20V before failure at secondary breakdown. This suggests that standard NMOS outputs can fail at voltages as low as Vds = 7V. 1.8V NFET failure Vds is projected to be 5V.



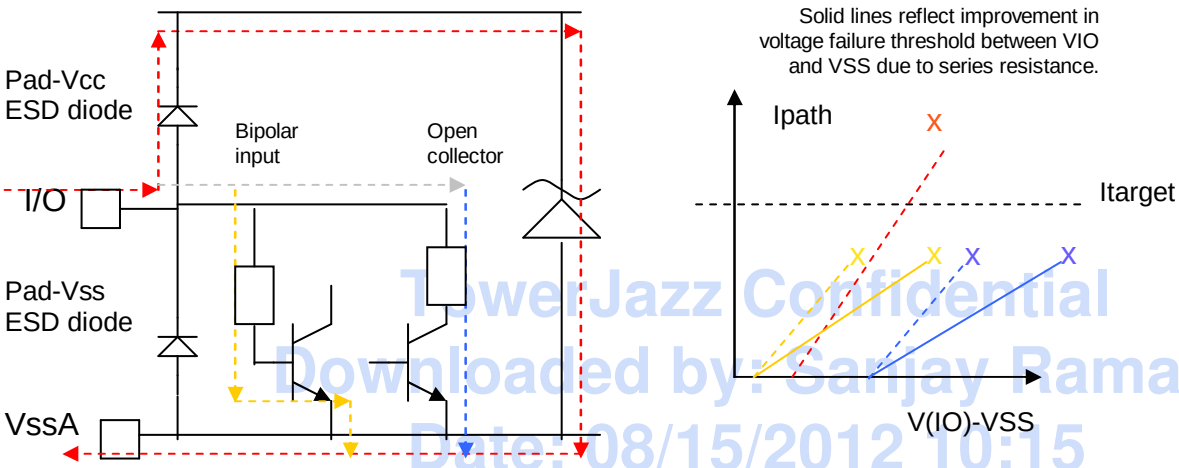


It's observed that PMOS transistors have a weak snap back characteristic after S/D junction breakdown ~ 9-10V and will conduct a finite current before failing. This suggests that their failure thresholds should be assumed to be > 9-10V, but no experimental data is available.

Gate oxide failure in 1.8V and 3.3V MOS is projected at 10V and > 16V, respectively.

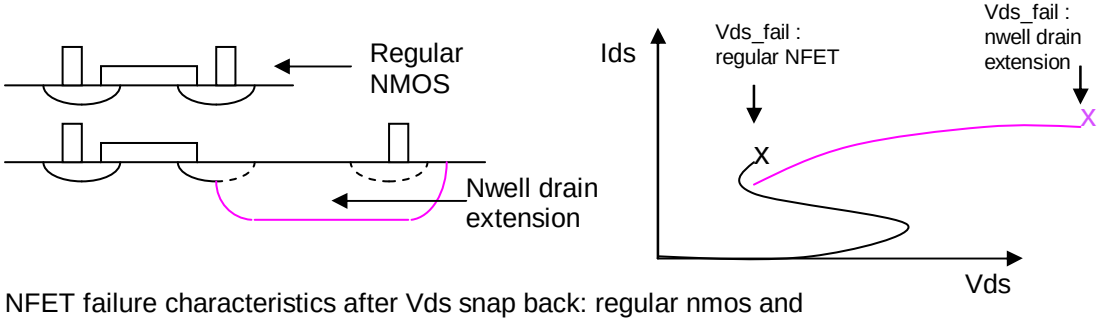
If a given ESD circuit is unable to protect the basic signal path and cannot be improved by redesign, it may be possible to enhance the signal paths to have higher failure voltage or current by adding ESD artifacts such as series resistors or following good layout practices.

NPN transistors have appreciable base and collector failure currents. These can be used together with series resistances to increase the effective failure threshold voltage of a signal path, as shown below by the solid curves with higher impedance compared to the dashed curves. The benefit from poly resistors can be calculated analytically using Ifail * R. nwell series resistance is very effective for this purpose because the sheet resistance of nwell increases non linearly with higher current density, as was seen in NMOS output data with nwell extension on the drain. If nwell resistors are used, it can be assumed that special sizing of the ESD protection circuit is not necessary.



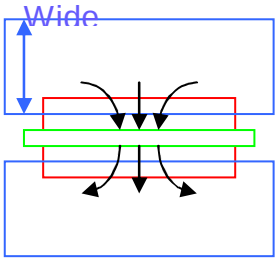
Using series resistances to elevate the voltage failure threshold of npn bipolar

Adding discrete resistance to NMOS outputs is not usually effective for the HBM because current crowding causes the device failure current to be small. As was seen above, however, an integrated nwell extension to the NFET drain can be added to an NMOS output device, to elevate its Vds failure threshold above the voltage clamping capability of most reasonably constructed ESD circuits.

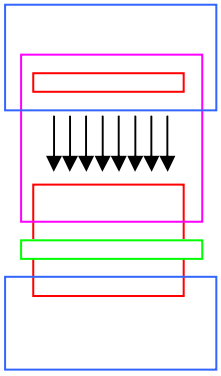


NFET failure characteristics after Vds snap back: regular nmos and

The above figure illustrates the IV benefit of adding the integrated nwell extension to the NMOS drain. Physically, the lateral effect of non-linear nwell sheet resistance on current density forces the drain current density to be uniform along the transistor width, eliminating hot spots and maximizing the total drain failure current. This is illustrated below. The longitudinal effect of the well resistor then elevates the transistor voltage failure threshold to as high as the well-substrate breakdown voltage.



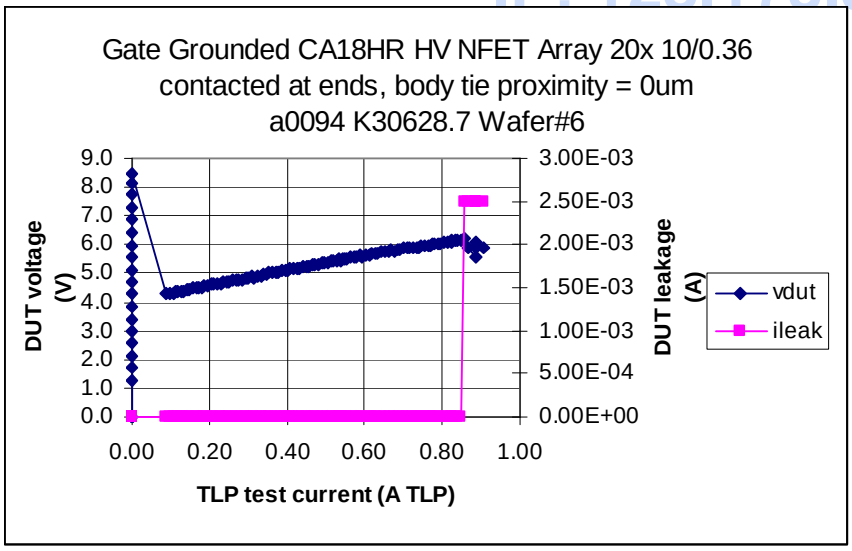
Wide metal connection on plain NFET allows current to focus at center of finger

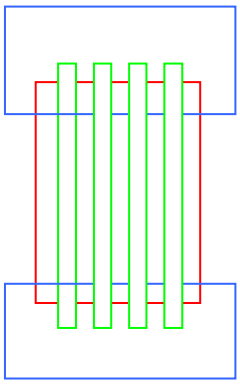


NWELL extension on drain keeps current density uniform and elevates failure Vds to 20V.

NMOS array finger connectivity can also apparently affect the total failure current associated with a transistor. Contacting the diffusions strongly at the finger ends instead of the full finger width encourages the current density to be more uniform along the width of the finger prior to transistor failure. Furthermore, assembling fingers into squarish arrays enables the parasitic npn's associated with the interior fingers to have larger base debiasing resistance, which results in higher failure current after snap back.

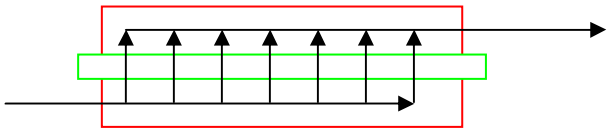
The figure below shows that a 20 finger array of 10/.36 gate-grounded HV NFET, with the S/D fingers contacted with wide metal only at the ends, conducts a respectable .85A TLP after snap back prior to failure, which has an equivalent HBM testing level of 1700V HBM. Note that the snap back holding voltage for the array is only 4.25V at approximately 10mA TLP. This is lower than the 7V value seen in single finger devices and is attributed to strong parasitic npn turn on. The failure threshold of the device is still around 7V (6V), however.





Jazz doesn't have a comprehensive model for MOS array failure current at this time. This array current may depend on several factors such as array size, proximity of body tiedowns, etc. It's recommended that MOS outputs not protected by an nwell extension on the drain continue to be clamped below Vds ~ 7V (assuming no current flows into the drain).

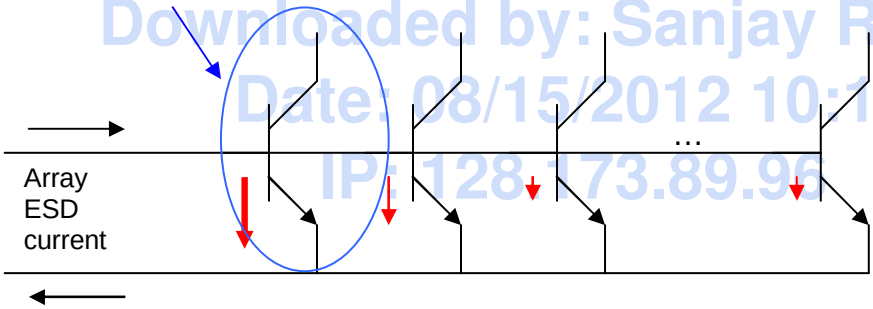
For this result, Jazz's understanding is that the "S" trajectory of current flowing in any given finger of an array creates a ballasting action, whereby a more uniform current density along the finger during the initial phases of snap back helps prevent early damage. This ballasting effect is present despite the drain being silicided and strapped by narrow MET1.

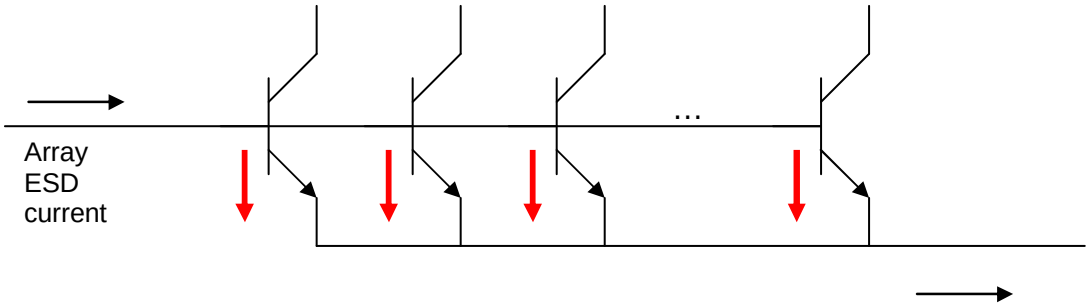


Diffusion resistance is believed to create a ballasting effect that makes drain current density uniform along the finger.

This general concept should be followed when arraying individual components to achieve higher total failure current, such as bipolar input transistors, as shown below. If this type of layout optimization is not used, it's possible that only a subset of components in an array will conduct significant current.

"C" shaped current trajectory focuses higher current thru devices with smaller series resistance





"S" shaped current trajectory encourages all transistors to conduct current uniformly because series resistance for each device is the same.

If the ESD circuit is not sized reasonably, it may eventually permit the activation of parasitic paths not explicit in the schematic. Parasitic npns formed from closely spaced n-type diffusions tied to different bonding pads (not in the same NFET) can snap back and conduct current. To some extent, these parasitics can be passivated by following the latch-up rules (strong body tiedowns), but the best practice is to design the ESD circuit capability conservatively according to typical signal path failure threshold data.

When screening a complex circuit for HBM weaknesses or doing an initial assessment of the balance between discharge network and signal paths, it's useful to abstract the failure conditions of signal path devices instead of trying to use the above detailed data. This is done in the table below. Signal paths exhibiting high voltage failure thresholds, possibly because of large series resistance or series stacked components, can often be quickly dismissed as being a failure concern.

Component	Typical Vfail	Typical Ifail	Comments
3.3V NMOS output	7V	0	Single finger, standard device Can't be ballasted by series R
3.3V NMOS output	6V	6mA/um W	Array, fingers contacted on ends can be ballasted with series R
3.3V NMOS output	20V	0	Nwell extension on drain
3.3V PMOS output	10V	0	Not usually a concern
Bipolar Vbe	2-5V	See table	Can be ballasted with series R
Bipolar Vce	7V	See table	Can be ballasted with series R
Bipolar Veb, Vec	-	-	Must be shunted by fwd. diode
3.3V MOS input	> dc BV value	0	Not usually a HBM concern
Resistors	-	-	Resistors limit current, failure not usually a concern
Series capacitors	-	-	Capacitors have high voltage breakdown, failure not usually a concern.
Metal	-	-	Equiv. > 8um wide MET1
Vias	-	-	~ 30 at each interchange (based on ESD diode data)

These typical values suggest that the discharge network can be very effective for most pins if the IO-power domain rail voltage is limited to below 7V for the targeted HBM testing level.

Examples of how to use this data to design the discharge protection networks are given in a later section.

Standard ESD Protection Devices

The standard esd library sbc18_esdlib consists of 3V and 5V tolerant transiently-triggered bignpn power supply clamps and various sizes of p+/nwell and n+/substrate ESD diodes (1-8 1x8 junction fingers), as indicated in the table below. The bignpn HBM ratings are for positive polarity HBM strikes between supply and ground. The diode ratings are for forward stress only. These component ratings are based on typical Transmission Line Pulser measurements. They do not necessarily correspond to the failure threshold of the pin being protected (see design examples later in this section).

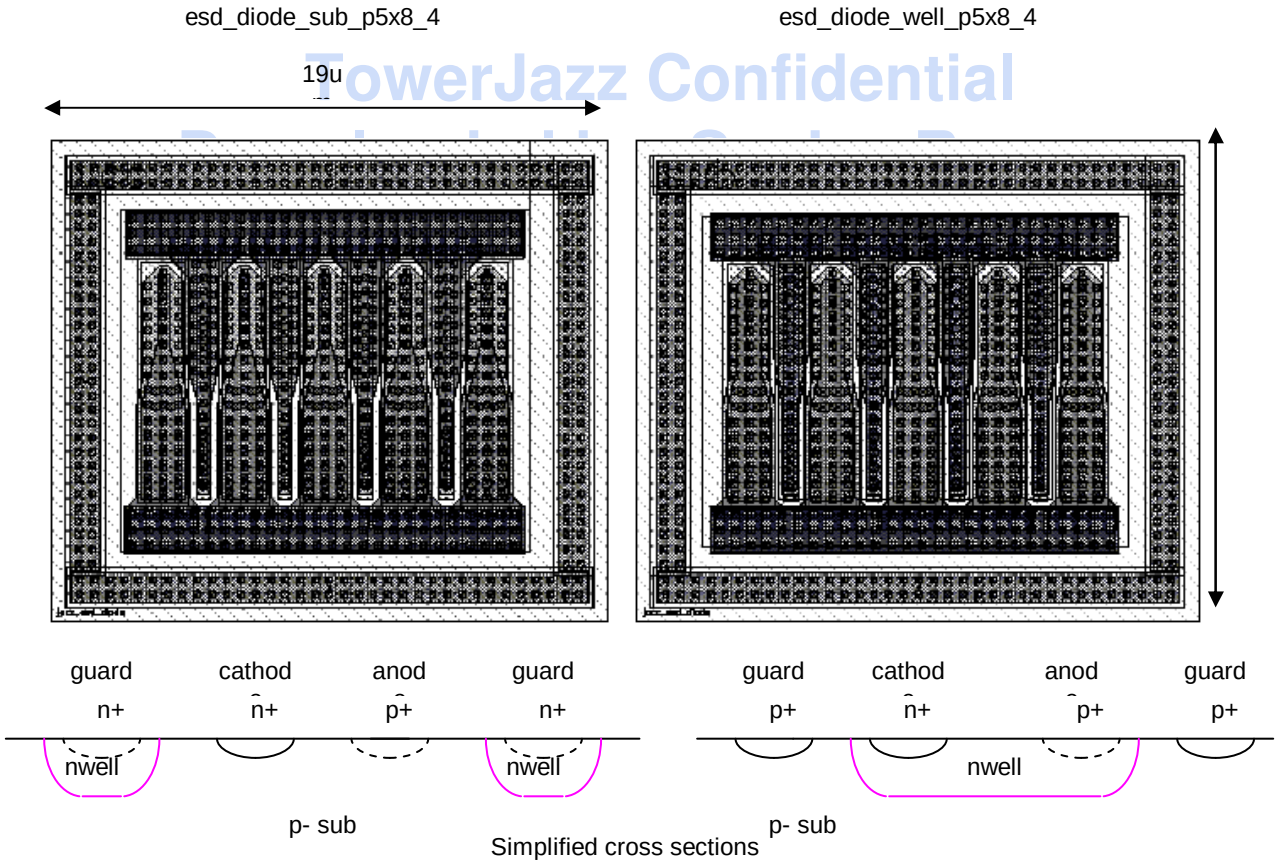
Component	Type and usage	HBM rating	Voff	Rserie	Other info
bignpn3_wp9_ignd	3.3V tol. power clamp	> 2KV	1	2	Isolated gnd.
bignpn_5v_sb_wd_ignd	5.0V tol. power clamp	> 2KV	1.22	1.68	Isolated gnd.
esd_diode_sub_p5x8_1	1x n+/sub ESD diode	0.6 A / 0.9 kV	1	3.01	C0= 11.43 fF
esd_diode_sub_p5x8_2	2x n+/sub ESD diode	1.1 A / 1.6 kV	1	1.51	C0= 21.55 fF
esd_diode_sub_p5x8_3	3x n+/sub ESD diode	1.5 A / 2.3 kV	1	1.14	C0= 31.66 fF
esd_diode_sub_p5x8_4	4x n+/sub ESD diode	2.0 A / 3.0 kV	1	0.79	C0= 41.78 fF
esd_diode_sub_p5x8_6	6x n+/sub ESD diode	2.8 A / 4.3 kV	1	0.54	C0= 62.01 fF
esd_diode_sub_p5x8_8	8x n+/sub ESD diode	3.8 A / 5.7 kV	1	0.40	C0= 82.24 fF
esd_diode_well_p5x8_1	1x p+/nwell ESD diode	0.6 A / 0.9 kV	1	3.01	C0= 9.31 fF
esd_diode_well_p5x8_2	2x p+/nwell ESD diode	1.1 A / 1.6 kV	1	1.51	C0= 18.74 fF
esd_diode_well_p5x8_3	3x p+/nwell ESD diode	1.5 A / 2.3 kV	1	1.14	C0= 28.17 fF
esd_diode_well_p5x8_4	4x p+/nwell ESD diode	2.0 A / 3.0 kV	1	0.79	C0= 37.60 fF
esd_diode_well_p5x8_6	6x p+/nwell ESD diode	2.8 A / 4.3 kV	1	0.54	C0= 56.46 fF
esd_diode_well_p5x8_8	8x p+/nwell ESD diode	3.8 A / 5.7 kV	1	0.40	C0= 75.31 fF
Legacy Component	Type and usage	HBM rating	Voff	Rseries	Other info
bignpn3_wp2	3.3V tol. power clamp	> 2KV	1.88	4.77	Gnd = sub

The power supply clamps behave like forward biased diodes under positive polarity HBM strikes between power and ground. Their operation and standby characteristics are described later in this section. Bignpn3_wp2 is classified as “legacy” because the bignpn3_wp9_ignd has superior HBM-relevant characteristics. This does not mean that that bignpn3_wp2 cannot be used in new products. Note that bignpn3_wp2 and bignpn3_wp9_ignd are 3.3V tolerant, and are compatible with 1.8V and 3.3V. Bignpn_5v_sb_wd_ignd is a 5V tolerant cell.

As with all transiently-triggered clamps, the bignpns should not be hot-plugged into a biased socket, because the timing mechanism that enables the cell to respond to ESD events limits its maximum slew rate. Also, bignpn cells do not provide any dc over-voltage protection for the supply rails.

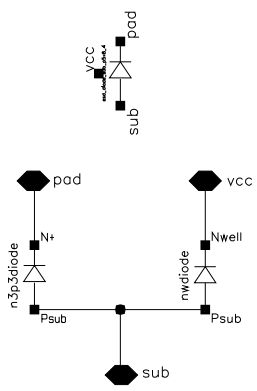
All standard ESD diodes are constructed from 3.3V MOS S/D junctions, which have a reverse breakdown of 8-10V. P+/nwell ESD diodes are intended for use between IO pins and supply, but can be used for all ESD diode applications, including series stacked applications to either extend IO pin voltage travel above supply or improve ESD protection for IO pins with limited voltage travel. N+/sub ESD diodes are only intended for connection between IO and ground, or possibly in-between grounds, because the anode is hard wired to the substrate. For the lowest parasitic IO pin capacitance and best RF characteristics, however, n+/sub diodes should be used between IO and ground. C0 values specified in the above table are 0V capacitances for the diode primary junction. Implicitly, the ESD circuit should be designed to avoid reverse voltages on ESD diodes greater than 8-10V.

ESD diodes are deliberately made “perimeter-intensive” to reduce capacitance while maintaining low series resistance. Their active junction areas are broken into multiple 0.5x8 um^2 fingers, and finger metallization is tapered along the stripe to enhance conduction of current to the ends, as shown below. ESD diodes are built with latch-up guard rings appropriate for their recommended use. This means that p+/nwell ESD diodes connected between IO and ground may benefit from an additional n-type guard ring (see the latch-up section for the recommended deployment of guard rings).

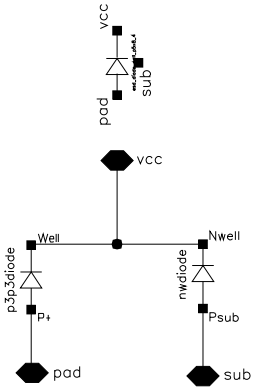


Simplified cross sections

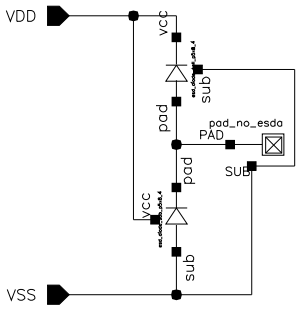
The layout and simplified cross sections of 4-fingered n+/sub and p+/nwell ESD diodes are shown above. Both devices are rated to survive 3KV HBM in the forward biased direction, and have a typical series resistance of 0.8 ohms under high current conditions. Their capacitances are on the order of 40fF at 0V dc bias. Their symbols, schematics and typical connection in an IO pad application are shown below.



n+/sub ESD diode
symbol and schem.

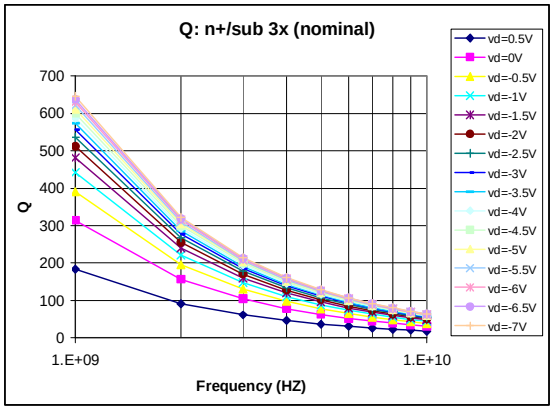


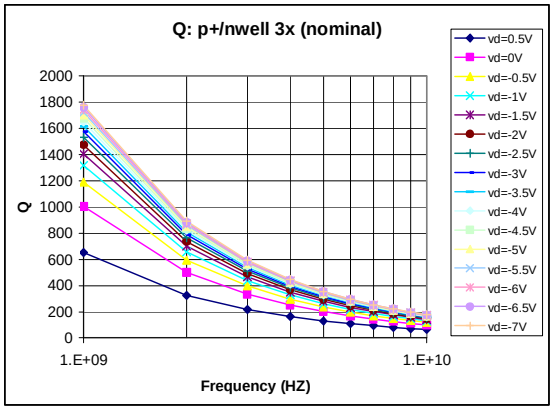
p+/well ESD diode
symbol and schem.

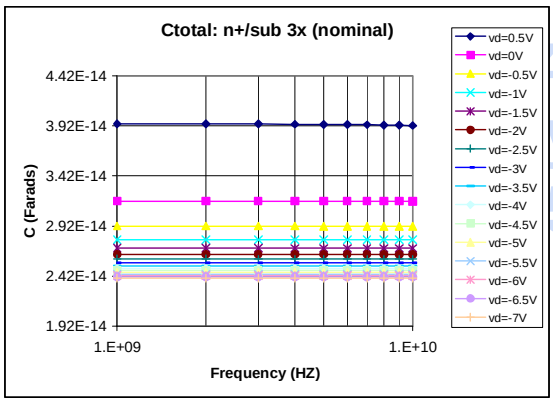


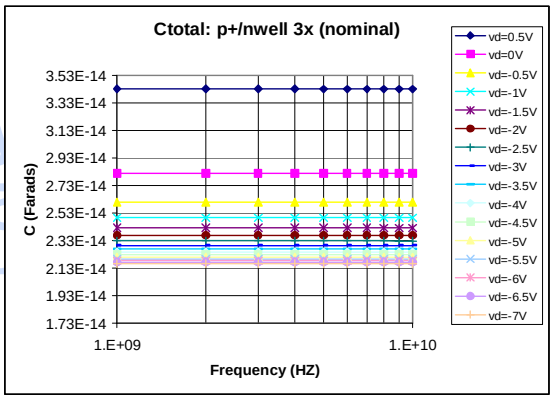
Typical ESD diode
usage at IO bond pad

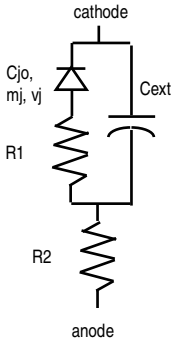
RF characteristics for the ESD diode primary junctions have been acquired and fitted to a lumped circuit model, but spice models are not yet available in the design kit. The projected single-ended Q and capacitance values for 3-fingered n+/sub and p+/nwell ESD diodes are shown below as a function of frequency between 1 and 10GHZ, and at reverse biases upto 7V. The lumped circuit model topology together with typical parameters for all the standard diode geometries is given at the bottom of the page.









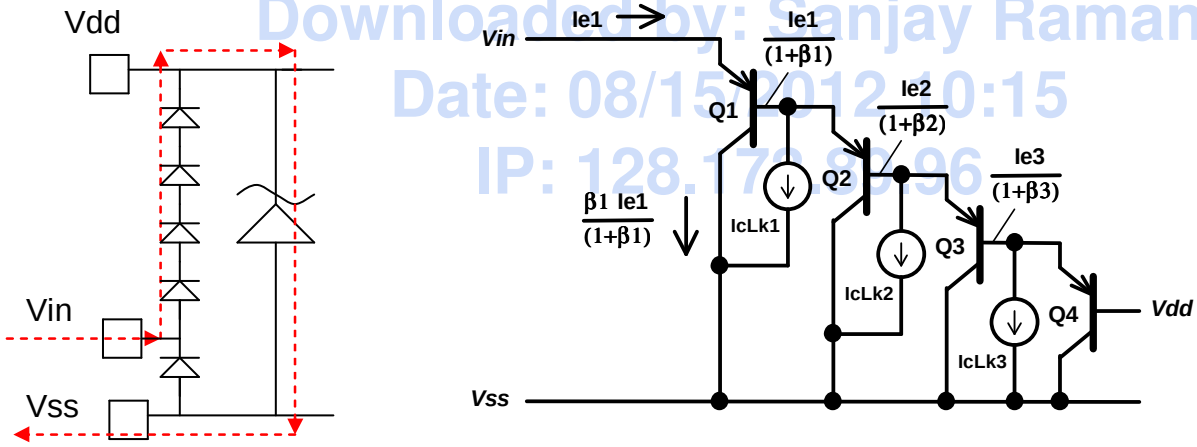


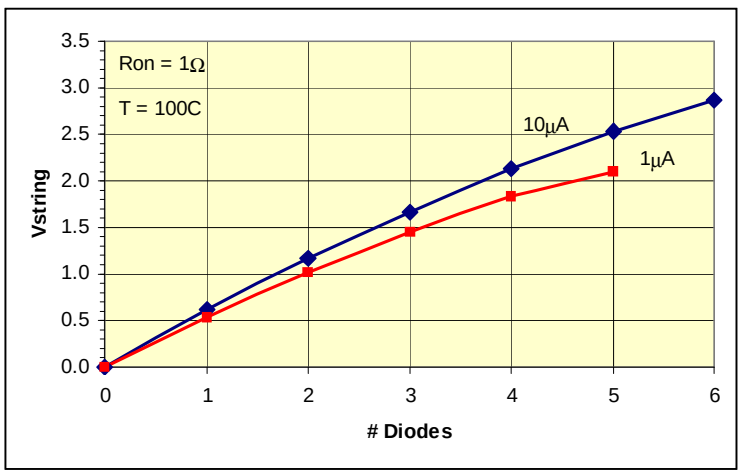
n+/sub	Cext	Cjo	mj	vj	R1	R2
NF	(femto-F)	(femto-F)			(ohms)	(ohms)
1	8.1307	3.3001	0.5292	0.7881	103.5610	42.4117
2	14.4139	7.1327	0.5292	0.7881	72.4565	16.1166
3	20.6971	10.9654	0.5292	0.7881	56.1313	9.2627
4	26.9803	14.7980	0.5292	0.7881	45.5425	6.1809
6	39.5467	22.4633	0.5292	0.7881	30.7616	3.9593
8	52.1131	30.1286	0.5292	0.7881	22.9212	3.0300
p+/nwell	Cext	Cjo	mj	vj	R1	R2
NF	(femto-F)	(femto-F)			(ohms)	(ohms)
1	6.8507	2.4638	0.5002	0.7985	29.3733	19.1346
2	12.6976	6.0455	0.5002	0.7985	20.5510	7.2712
3	18.5445	9.6272	0.5002	0.7985	15.5635	3.8230
4	24.3914	13.2089	0.5002	0.7985	12.9173	2.7886
6	36.0852	20.3724	0.5002	0.7985	8.7250	1.7863
8	47.7790	27.5358	0.5002	0.7985	6.5012	1.3670

It may be necessary to stack series p+/nwell diodes in series to either increase IO pin headroom above the supply rail or create conservative discharge paths (for bipolar inputs, for example). In all cases, standby current flowing thru a forward biased stack may see significantly smaller impedance than the sum of individual diode impedances carrying the same current. This is because each p+/nwell diode in a forward biased stack has a parasitic pnp transistor that diverts some fraction of the tail current into the substrate. Later stages in the stack will have a lower voltage because the incident current is attenuated.

This is illustrated for the schematic below, which consists of a stack of four p+/nwell ESD diodes. The diagram on the right shows how some fraction of the anode current at each diode will be diverted into the substrate. The current gain of the pnp's is approximately 4 at room temperature. This means that only 1/5 of the anode current is passed to the next diode.

The plot at the bottom of the page shows the typical nonlinear stack voltage vs. number of diodes behavior for a fixed tail current (ie1). This effect cannot currently be simulated using SPICE because the ESD diodes are constructed using independent primary and secondary junction diodes, instead of a pnp transistor. It may be necessary to use standard pnp transistors to create the stack if accurate standby characteristics need to be simulated. It's expected that pnp transistors will be more robust than the standard ESD diodes, but their RF characteristics may not be as desirable.

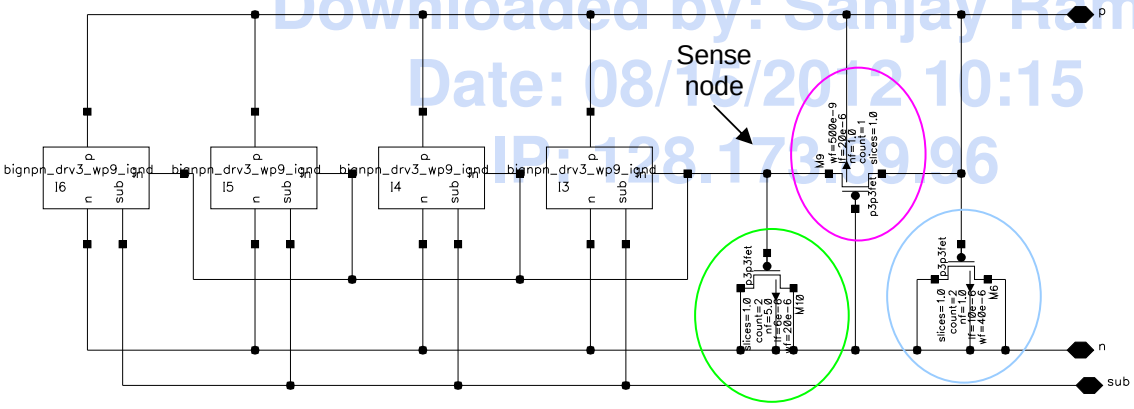




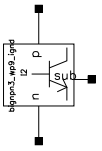
Bignpn power supply clamps are transiently-triggered cells that behave as forward biased diodes under positive polarity HBM strikes between power and ground. This characteristic for a rail-based protection scheme can be superior to a dc-triggered clamp response to ESD, because rail-rail voltage can be clamped below the nominal power supply value. Under dc bias > ~ 1V, the cells behave as reverse biased diodes, which free the rails for normal operation. One potential usage limitation is their maximum slew-rate during abrupt turn on, which is restricted by the same mechanism that makes them responsive to ESD events. Slew rate design information is provided for each clamp.

The symbol and schematic for the *bignpn3_wp9_ignd* is shown below. The cell consists of a CDM capacitor connected directly across the rails (blue), a sense circuit made up of a resistor (purples) and capacitor (green), and driver sections containing npn transistors that are used to discharge the ESD current. Essentially, if the sense node is charged to the supply rail, the driver transistors will be turned off and behave as reverse biased diodes. If the sense node is held low relative to the supply rail, the bases of the npns are pulled to supply, and the driver transistors behave as forward biased diodes.

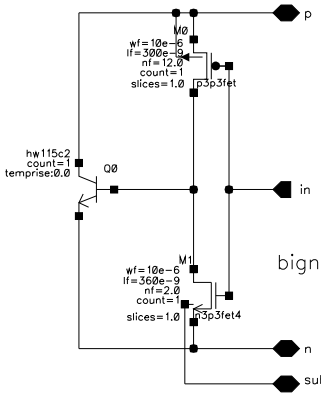
With the cell initially unbiased, as would be the case during HBM ESD testing, the sense node does not immediately charge up to the supply rail under positive ESD strikes and the cell will clamp the rail-rail voltage. Under steady state dc bias, the sense node is charged to the supply rail.



bignpn_wp9_ignd (top schematic)

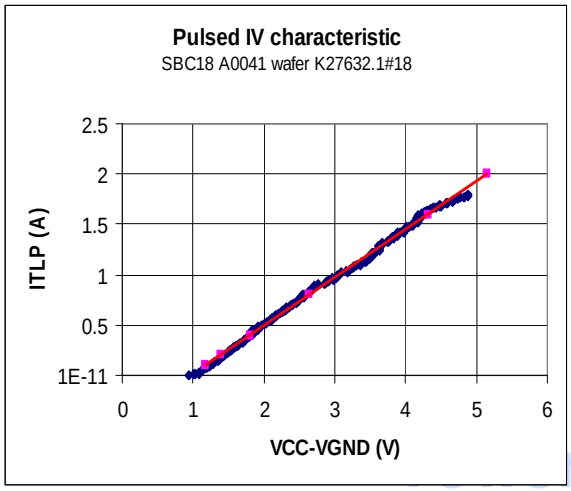


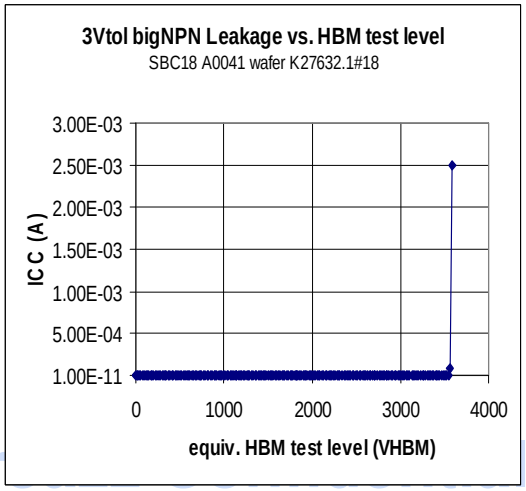
bignpn_drv_wp9_ignd (symbol)



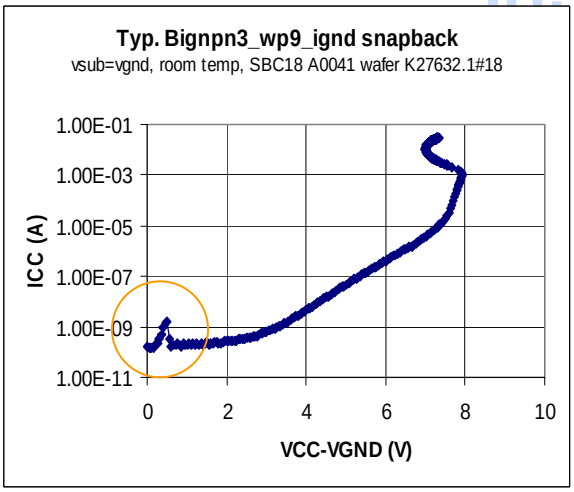
bignpn_drv_wp9_ignd (subcell)

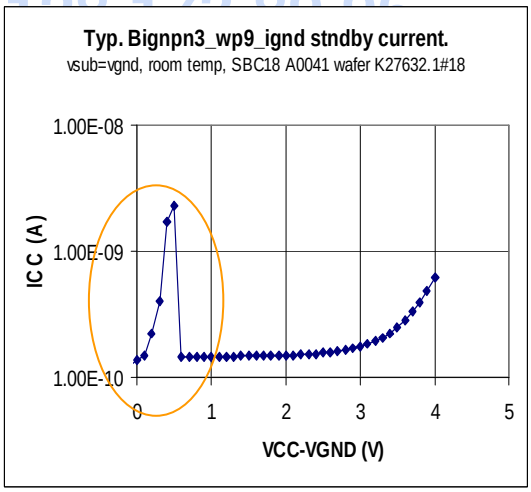
Experimental TLP pulsed IV and standby leakage curves of the bignpn3_wp9_ignd shown below indicate that the cell response to HBM testing can be well represented by a 1V battery with 2 ohms of series resistance. This is similar to the TLP characteristics of a forward-biased ESD diode. The standby leakage current at 3.3V of the cell does not change for TLP strikes below levels equivalent to 3500V HBM, which indicates that the clamp itself should not fail under lower levels of HBM testing.





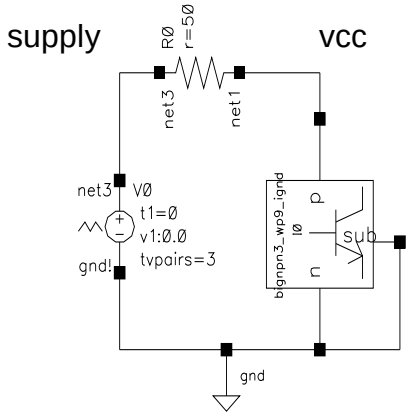
In the off state, the dc standby leakage plots below show that the cell will have a high impedance (~ 1nA) at room temperature for supply voltages up to 4V, and does not snap back under supply voltages as high as 6.5V. This is adequate for normal 3.3V operation.

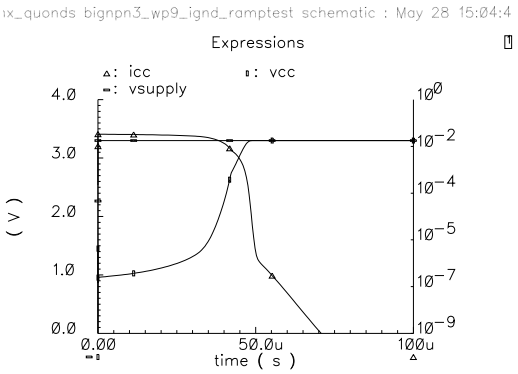


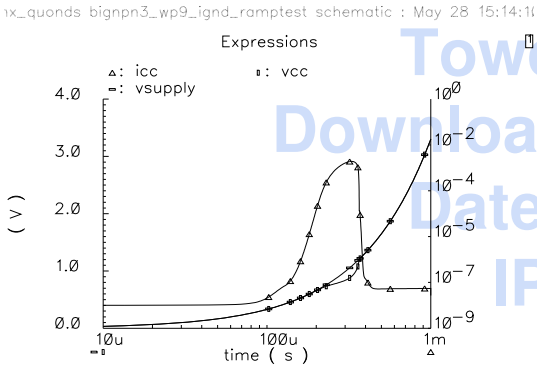


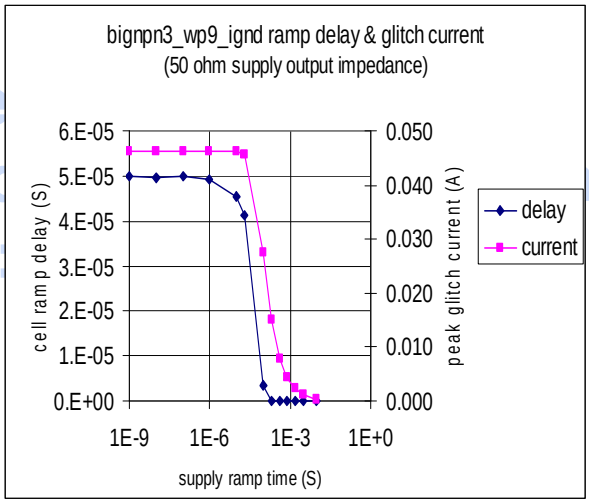
One potential usage issue for all transiently-triggered clamps is that they exhibit a delay for abrupt ramp-up, which can be accompanied by a current glitch whose magnitude and duration depend on the supply ramp time and output impedance. This glitch is seen circled in orange in the cell dc IV plots above.

To understand cell slew rate limitations, we can look at transient analyses of the following spice schematic, in which a bignpn3_wp9_ignd is driven by a piecewise linear power supply thru a 50 ohm series resistor from 0 to its nominal bias value of 3.3V.







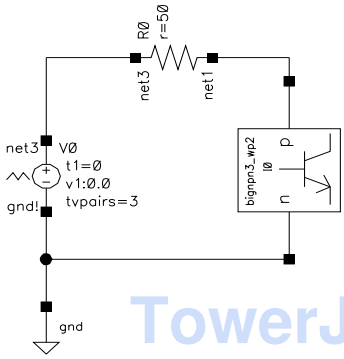


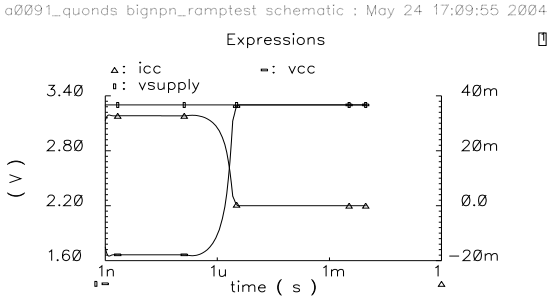
Two extreme cases in which the supply ramp time to 3.3V is 1ns and 1ms are shown in the top right and bottom left plots, respectively. For a 1nS supply ramp time, vcc ramp to 3.3V is delayed by 50uS, during which the supply draws a current of 45 mA. For a 1mS supply ramp time, there is no delay between supply and vcc ramp times to 3.3V, but a current glitch with a peak value of 3 mA is still observed.

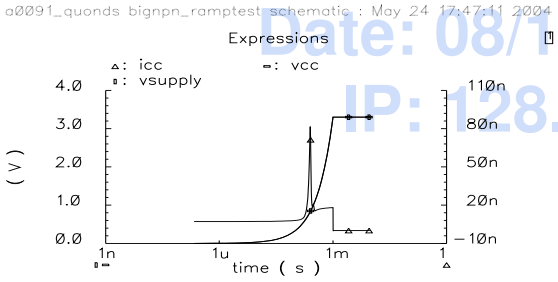
Sweeping the supply ramp between 1ns and 1mS, we see that the cell ramp delay and peak glitch current have break points near a supply ramp time of 300uS. To avoid significant glitching during power domain ramp, the minimum supply ramp time for bignpn3_wp9_ignd should be limited to 1mS.

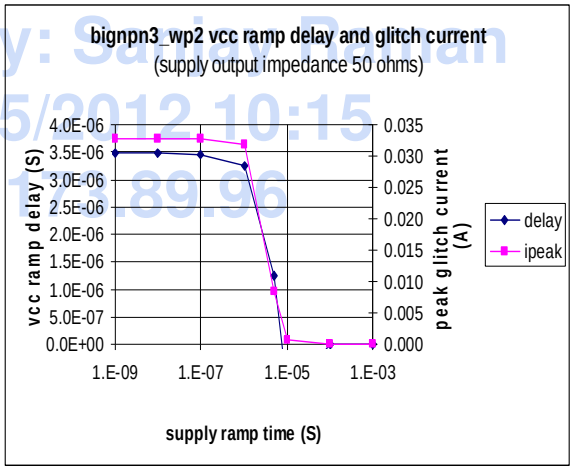
It's possible that this glitch can be mistaken for latch-up during the initial phases of power up. However, it's clear from the above simulations that cell high impedance should always recover within a millisecond.

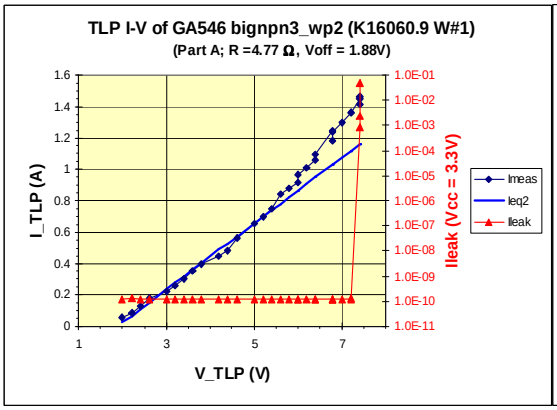
The legacy *bignpn3_wp2* cell has a similar schematic and qualitative response to supply ramp time, but its ramp delay and peak glitch current break points occur at a much smaller 10uS. This is attributed to the small sense capacitor in this cell, whose relatively weak ability to hold down the sense node during ESD events results in higher offset voltage (1.88V) and series resistance (4.77 ohms). Otherwise, the cell also has an acceptable snap back holding voltage of 6.5V, is found to survive greater than 2KV HBM, and is still viable for use in products provided its higher offset voltage and series resistance are accounted for in discharge network design.

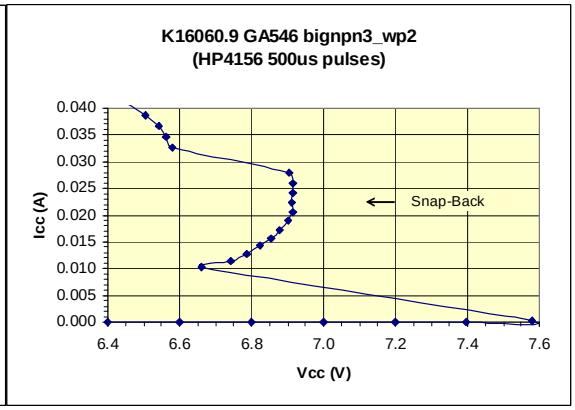


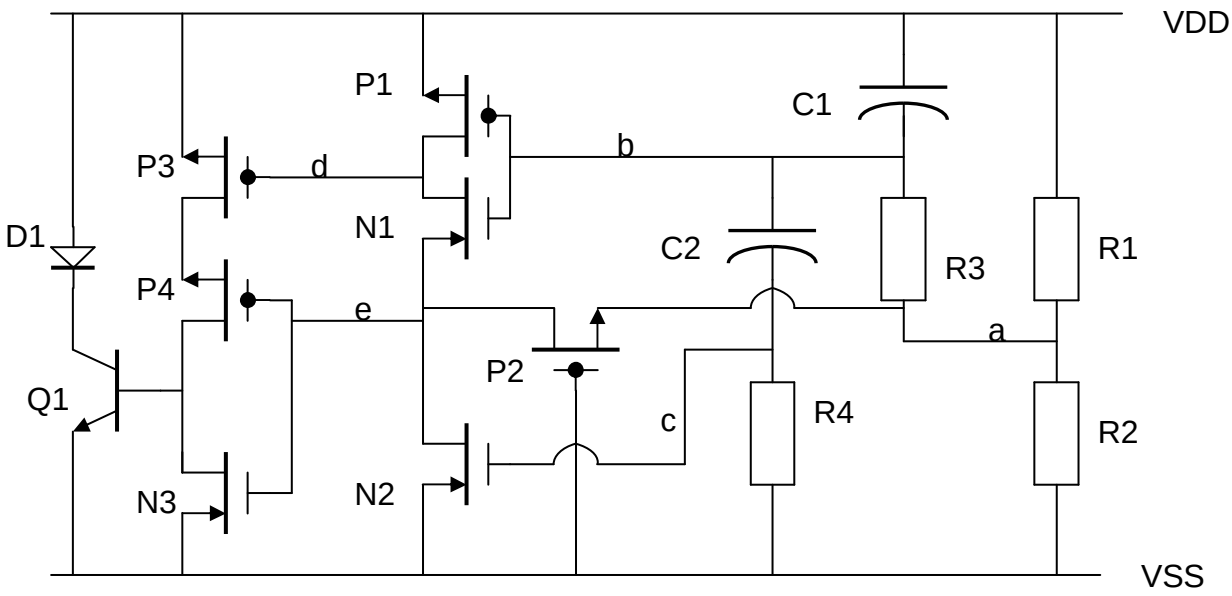












Simplified schematic of SBC18 5V tolerant BigNPN power supply clamp

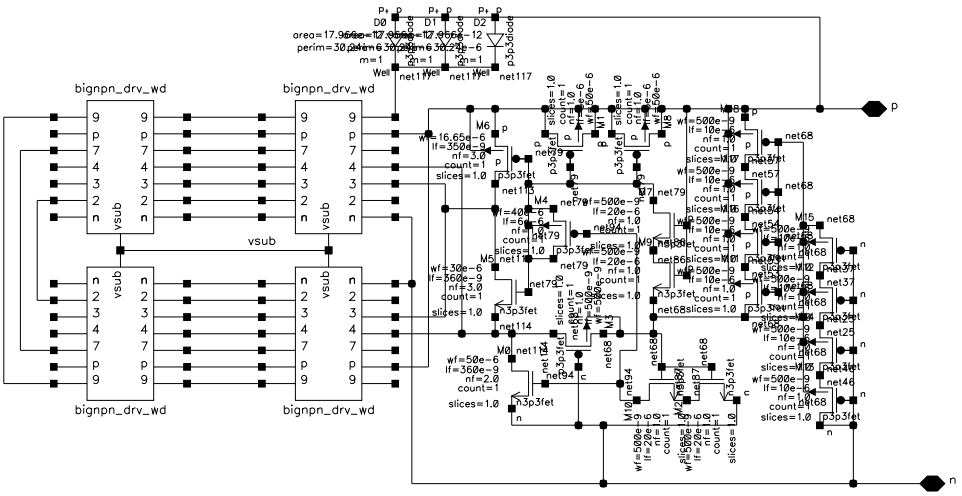
The above figure is a simplified schematic for the 5V-tolerant self-biased bigNPN clamp *bignpn_5v_sb_wd_ignd*. Resistor divider R1 = R2 forms a voltage reference for the cell under dc conditions, and all RC time constants (R3*C1 and R4*C2) are intended to be long enough to discharge HBM ESD events.

Under steady state VDD=5V bias, node a is fixed at 2.5V. Since all the capacitors are charged up with no static current flowing across R3 and R4, node b will be at 2.5V and node c will be at 0V. With node b at 2.5V, node d is pulled to 5V, turning off P3 and preventing any current flow thru P4. With node c set to 0V, N2 is turned off, and node e is charged up to within VT of 2.5V by P2. An enabling voltage on node e then ensures that the base of Q1 is fully discharged to ground by N3 and that Q1 is configured as a reverse biased diode.

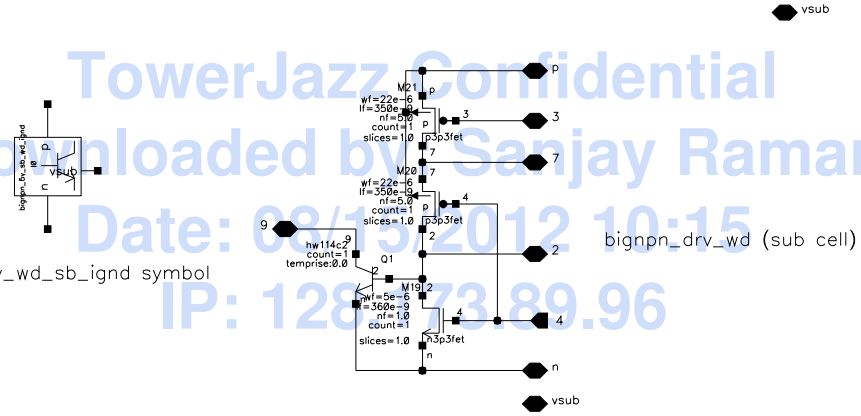
Under positive-polarity HBM-like ESD strikes between VDD and VSS with the power domain rails initially uncharged, nodes b and c are pulled initially to the voltage on VDD. A high node b relative to half the VDD voltage forces node d to be pulled down to approximately half of the supply voltage by N1 and the intermediate node between P3 and P4 to be coupled to the VDD voltage.

A high node c will pull node e to the VSS rail thru N2, which then couples the base of Q1 to the intermediate node between P3 and P4 and the voltage on VDD. Until nodes b and c relax to their steady state values, Q1 is configured as a forward biased ESD diode and strong voltage clamp between VDD and VSS.

The actual symbol and schematics for bignpn_5v_wd_sb_ignd are shown below.

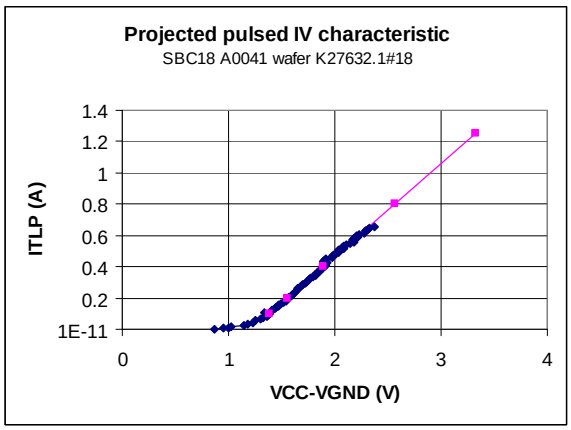


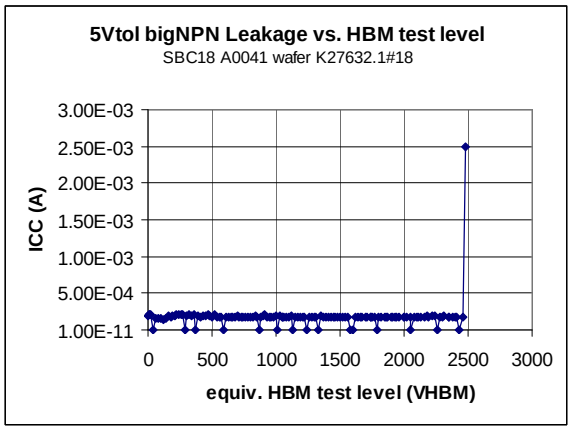
bignpn_5v_wd_sb_ignd (top level)



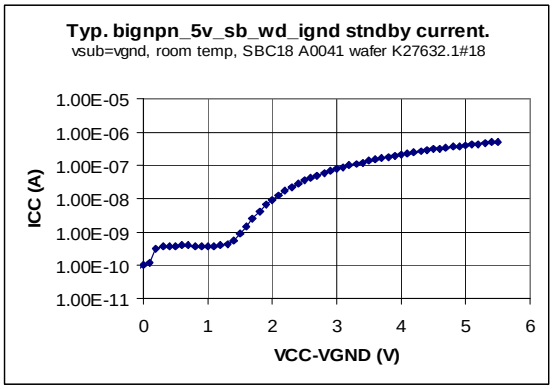
bignpn_5v_wd_sb_ignd symbol

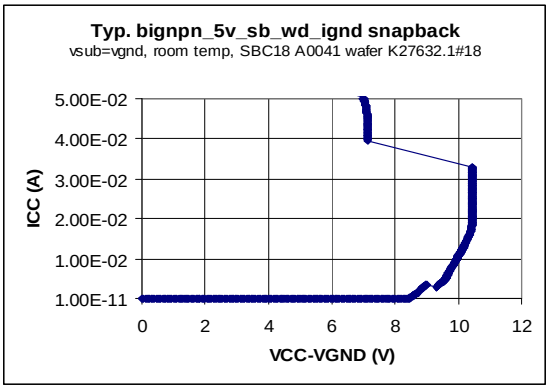
In response to HBM strikes, based on TLP characterization, the cell is expected to have a voffset and series resistance of 1.22V and 1.68 ohms and not be damaged by ESD testing upto 2500V HBM.



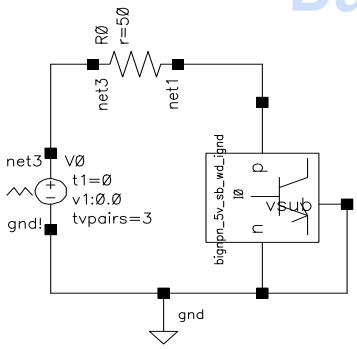


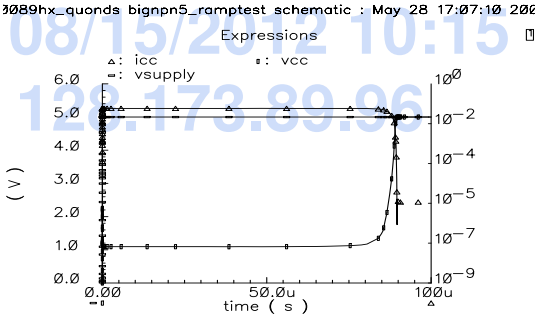
The cell's dc standby current of 1uA at 5V is as expected from the bias current flowing thru the resistor ladder. In 5V applications where 1uA is not tolerable and a 3.3V supply is available, the midpoint node of the ladder can be connected to the 3.3V supply instead. The cell snap back holding voltage is 7V, which is adequate for 5V circuit operation.

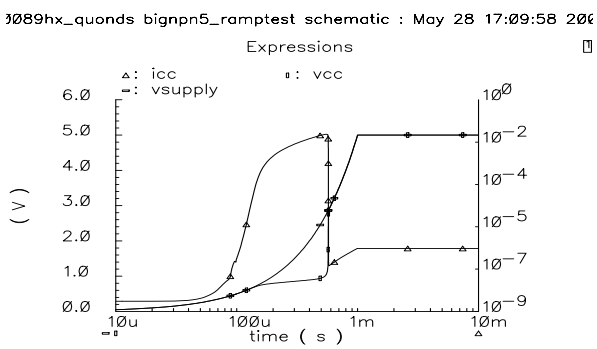


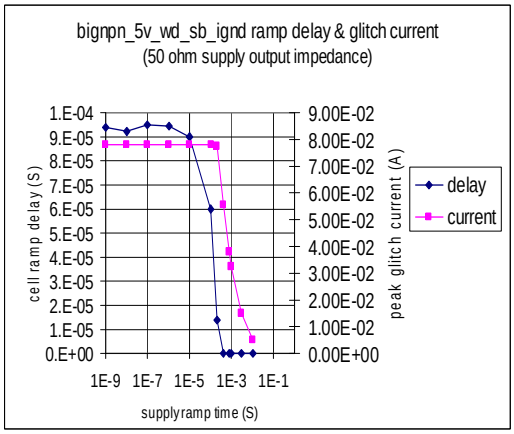


A maximum slew rate analysis for the cell indicates that the cell startup delay is approximately 90uS, with a peak glitch current of 78mA for a supply ramp time and output impedance of 1nS and 50 ohms. The cell ramp delay is negligible at a supply ramp time of 1mS, but a peak glitch current of 34mA is still observed. A breakpoint around 300uS suggests that supply ramp times should be kept greater than 1mS.



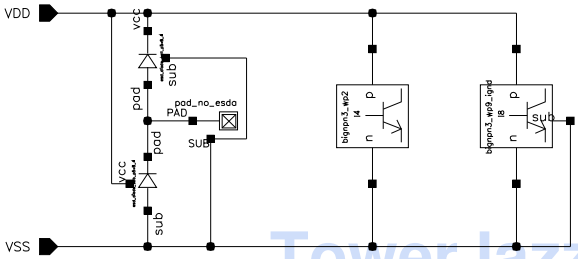




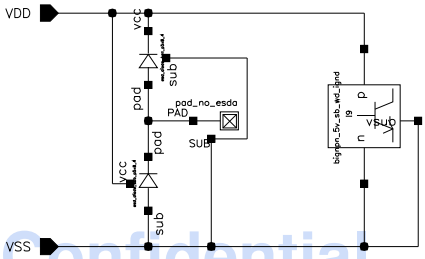


Bignpn cells with the "_ignd" extension have an isolated ground to enable circuits whose grounds are not tied directly to the substrate. Otherwise, the ground and substrate pins on these cells should be tied together. If the circuit ground is isolated from the substrate, an explicit ESD diode should be used to create a return path between the rails. This return diode replaces the parasitic pn junction(s) associated with n-type diffusions in substrate tied to supply and is superior to the return action provided by the dual ESD diodes connected to IO pins. The ESD circuit configurations for various 3V and 5V scenarios and the standard bignpn cells in power domains with either substrate-shorted or isolated grounds are shown below.

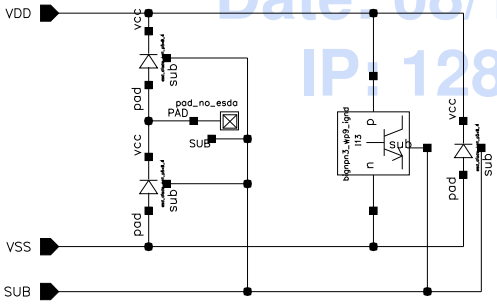
3.3V ESD ckt configs for
GND tied to substrate



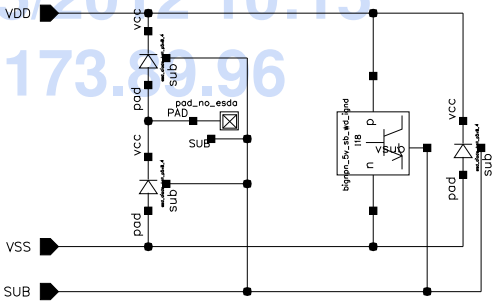
5V ESD ckt config for
GND tied to substrate



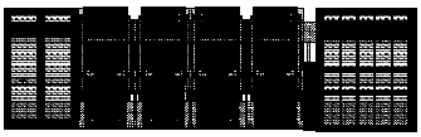
3.3V ESD ckt config for
GND isolated from substrate



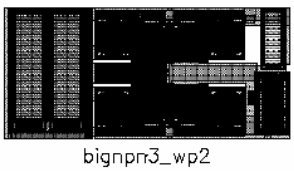
5V ESD ckt config for
GND isolated from substrate



The layouts for the sbc18 bignpn cells are shown below. The footprint sizes for bignpn3_wp9_ignd, bignpn3_wp2 and bignpn_5v_sb_wd_ignd are 157x47, 109x51, and 141x77, respectively. All cells are drawn using layers upto MET2.



bignpn3_wp9_ignd



bignpn3_wp2

bignpn_5v_sb_wd_ignd

Practical design examples for sizing ESD circuitry

Example 1.

Suppose that the goal for ESD testing is to pass 2000V HBM, and that we want to determine how well the standard ESD protection scheme will protect a given signal path connected between an IO pad and ground, as shown in the schematic below. As explained earlier, the critical question is whether the ESD discharge path consisting of the IO-supply ESD diode, power supply clamp and any series bus resistance will clamp the voltage between IO and ground below the failure threshold of the signal path, in response to a positive polarity strike between IO and ground (indicated by dashed path).

The peak current is 1.3A, so the voltage across the discharge path could be as high as

V_pad_gnd = Voff(diode) + 1.3*Rdiode + Voff(clamp) + 1.3*Rclamp + 1.3*R_bus

Substituting the piecewise linear parameters for a 3 fingered ESD diode and a standard bignpn3_p9_ignd power supply clamp, both of which are rated to handle 2KV HBM events, we find that

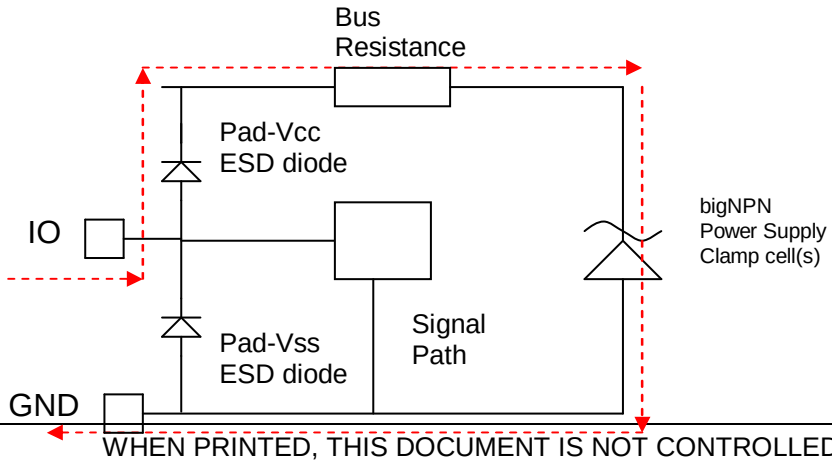
V_pad_gnd =6.082 (V) + 1.3 (A) * R_bus.

If the device to be protected were an open drain NMOS transistor with failure Vds = 7V, R_bus would have to critically be less than 0.71 ohms.

If the initial discharge components were a 4 fingered ESD diode and two bignpn3_wp2 cells in parallel, we would find that

V_pad_gnd =7.01 (V) + 1.3 (A) * R_bus.

This second network with any reasonable R_bus is not able to prevent a standard NMOS output from failing. It could be possible, however, to increase the number of bignpn3_wp2 clamps (not elegant), add an nwell extension to the NFET output (will work but requires special layout), use a larger diode (ok), or use the bignpn3_wp9_ignd clamp (best), as was done in the first configuration.



Example 2.

Suppose for the same on-chip protection network topology and test condition that we wanted to protect a forward biased base-emitter junction that had a failure voltage of 3.5V and failure current of 0.4A.

The protection circuit as defined is incapable of protecting the bare junction from failure under 2KV HBM using practical combinations of standard devices. However, if a series resistor (R_protect) is added to the junction, the ohmic drop corresponding to the critical junction failure current of 0.4A can be used to raise the pad voltage to values that would divert more current into the protection network before the transistor failed.

The IV relationships for the protection and signal paths are

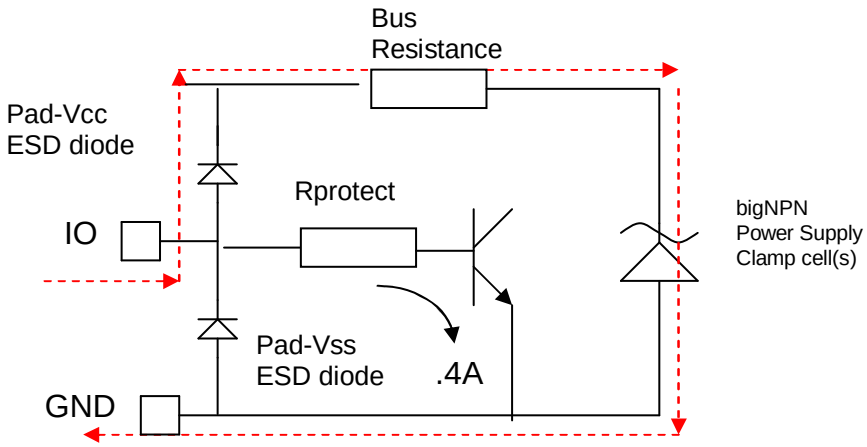
V_protect = Voff(diode) + 1.3*Rdiode + Voff(clamp) + 1.3*Rclamp + 1.3*R_bus
V_sigpath = 3.5 + 0.4A * R_protect

Setting these expressions equal and using a 3 fingered diode and bignpn3_wp9_ignd to realize the protection network,

6.082(V) + 1.3 (A) * R_bus = 3.5 + 0.4 * R_protect

Or R_bus = (0.4 * R_protect –2.58)/1.3

If R_protect = 50 ohms, the maximum tolerable value of R_bus is 13.4 ohms. If R_bus were zero, R_protect would have to be > 6.5 ohms.



Example 3.

Suppose for the same stress condition and device to be protected that we could not add any series resistance to the base current loop, but could add a shunting stack of 3 forward biased ESD diodes to the standard protection circuit, as shown in the schematic below. What would be the expected pin survivability?

First assume that the signal path is biased critically at its failure threshold: I1 = 0.4A and the pad voltage is IO-GND = 3.5V. We can solve for the currents in the bigFET (I2) and the series stack of ESD diodes (I3) to arrive at the total pin current corresponding to circuit failure.

Assuming all ESD diodes have 2 fingers, the clamp is a bignpn3_wp9_ignd, and R_bus = 1.1 ohm,

Vclamp = 3.5V = (1V + I2*2) + (1.1*I2) + (1V + 1.5*I2)
Vstack = 3.5V = 3 * (1V + I3 * 1.5)

or

I2 = .326 A HBM ; I3 = .111 A HBM, both of which are within the failure current ratings of the 2 fingered ESD diode (1.1A)

The total current entering the IO pin at the point of transistor failure is

Itotal = .4 + .326 + .111 = .837 A HBM, which is equivalent to 1255 V HBM.