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TITLE:

CA18 ESD Design Manual

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Overview

Various real-world electrostatic discharge (ESD) events may cause large, potentially destructive currents to flow thru the pins of integrated circuits. IC products must usually carry explicit on-chip ESD protection to survive these stresses. For product qualification purposes, standardized testing is used to simulate ESD events in the laboratory.

Mainstream component-level ESD tests include the Human Body Model (HBM), the Charged Device Model (CDM) and the Machine Model (MM). Good overall product ESD quality is usually demonstrated by a combination of acceptable HBM and CDM, or HBM and MM ratings. Based on schematic and layout information, however, only the HBM reliability of products can be predicted to first order.

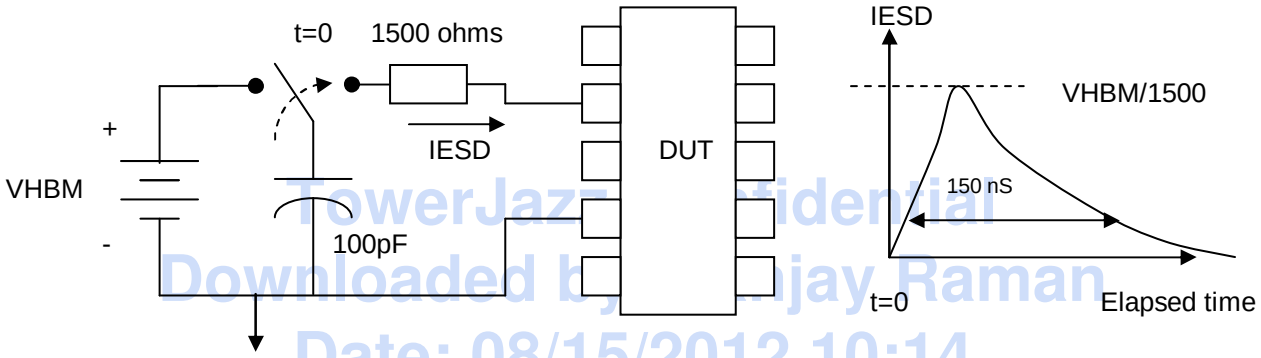
This document describes a methodology, standard devices and data to support favorable design of on-chip ESD protection circuitry for the HBM test. A typical goal is for products to pass 2000V HBM and 1000V HBM for regular and high performance (RF) pins. The satisfaction of schematic and layout criteria required to meet certain goals must be checked manually. Otherwise, the passivation of rogue parasitic devices that in extreme cases can defeat the ESD circuit is checked by the latch-up DRC rules.

Some general recommendations are suggested for MM/CDM, but guidelines to meet specific component ratings cannot be defined because product responses to MM/CDM testing are complex and may depend on off-chip factors.

Definitions and Countermeasures for the Human Body Model

In the HBM test, a 100pF external capacitor charged to a static voltage (VHBM) is discharged across pairs of designated package pins thru a 1500ohm external series resistor. This is shown in the figure below. All uninvolved package pins are floating; including pins that are normally connected to power and ground. A typical HBM test plan will involve stressing all possible pairs of pins under a given VHBM level. Component failure is usually determined by circuit non-functionality after all stresses on a part are completed.

Achieving a product passing rating of 1000-2000V HBM is a meaningful goal because ESD events of that level are not readily detectable by human beings but have a significant destructive capability and can easily occur in poorly regulated product handling environments.



Unless the DUT impedance between the pins being tested is significant relative to 1500 ohms, a HBM strike usually results in a double-exponential discharge waveform with a consistent peak current, rise time and pulse width of approximately VHBM/1500 ohms, 1-10nS, and 150 nS. Neither parasitic-type series inductance nor shunting capacitance is factored into HBM analyses, because they typically do not strongly affect the peak current to first order.

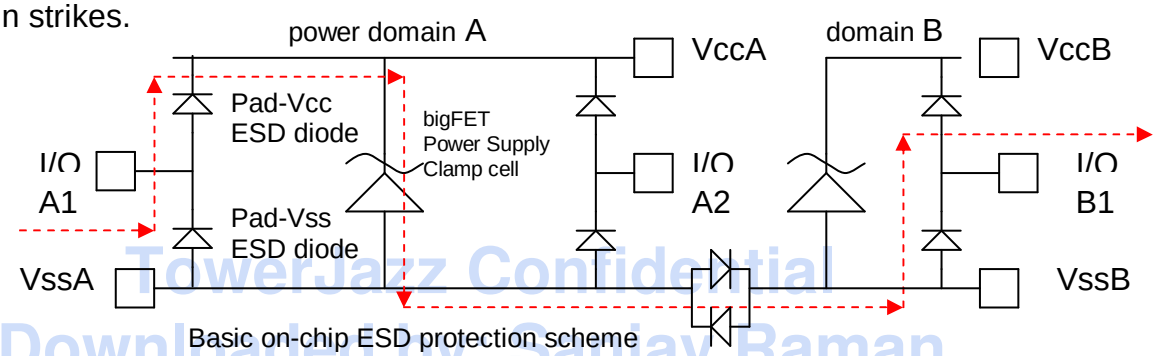
This is the case for pins connected to reasonable implementations of an on-chip ESD network and is why product response to HBM events can be engineered if the IV characteristics and failure thresholds of the ESD circuit and signal paths are known.

On-chip ESD protection circuits generally consist of a network of discharge paths connecting all bonding pads wired to package pins. In response to a HBM strike, this discharge network carries excess pin-pin test current that does not flow thru signal or parasitic paths. In the best case, the network will conduct most of the pin-pin test current and clamp voltages across the signal paths to safe values. If relevant data is available, simple calculations can be used to verify this to first order.

The standby characteristics of the network should be nominal (not leaky or restrict the voltage travel of IO pins). This means that it may be necessary to compromise ESD protection for certain pins with large voltage travel, or possible to tighten the ESD circuit for pins with reduced voltage travel (with operating point near ground, for example).

Protection for Mixed Signal Circuits

The basic protection network recommended for most mixed signal applications is shown below. ESD diodes route test currents from the IO pins to the power domain rails, and transiently-triggered "bigFET" clamp cell(s) route currents from rail to rail as necessary. The idealized discharge path for HBM current entering an IO pin of one domain (A) and leaving an IO pin of another (B) is shown in red (signal and parasitic paths are not shown). To enable discharge paths between all pins on the chip, a metallized connection is required between isolated power domain grounds, using cross-coupled ESD diodes to provide noise or substrate isolation if necessary. Multiple grounds can be daisy-chained (serially) if IO circuitry is not connected directly to pads belonging to different domains, but it is preferable to connect the grounds in a star pattern to minimize pin-pin voltages during cross domain strikes.



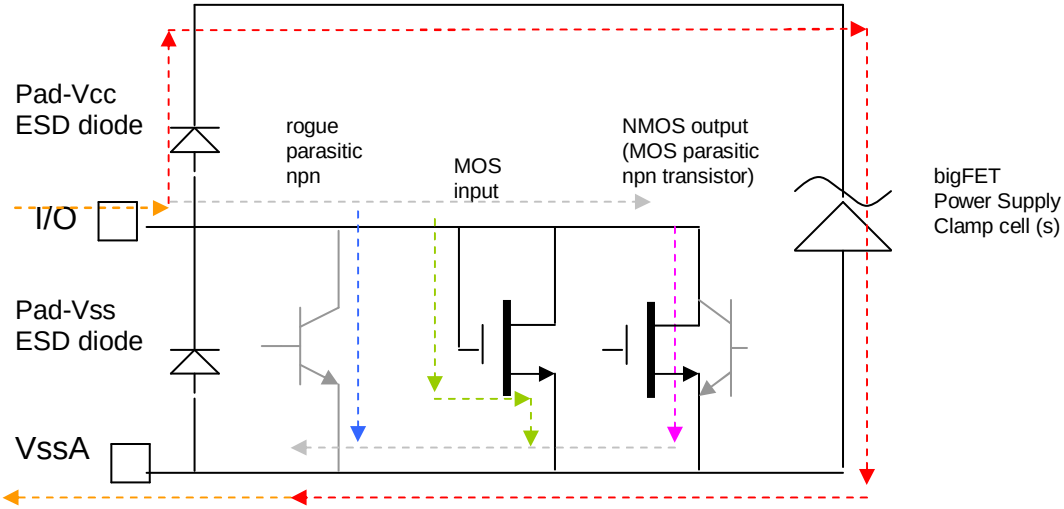
Basic on-chip ESD protection scheme

Aside from two basic layout requirements for the discharge paths: 1) metal width should be greater than the equivalent of 8um of METAL1, and 2) the number of vias at each interchange should support the desired maximum ESD current (approximately 30 vias for 2KV HBM); favorable implementation of the Jazz-recommended ESD network is mostly a schematic design problem provided rogue parasitic devices in the layout that might bypass the network are passivated. A reasonable target for pin-pin voltages within a given domain in response to a given HBM testing level should typically be < 10V, depending on the signal devices being protected.

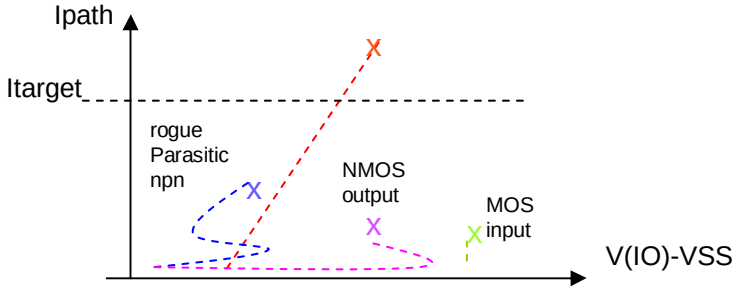
The schematic on the next page showing typical partial discharge paths between an IO pad and ground illustrates how the dedicated ESD path must compete against the signal or parasitic paths for discharge current. The indicated direction of current flow is consistent with a positive polarity HBM strike between IO and ground. Note that ESD analyses usually focus on positive IO-gnd and negative IO-supply stress combinations when using the recommended ESD circuit topology because they are often the worst situations from a dedicated discharge impedance point of view (the discharge path involves multiple series devices, so large pin-pin voltages can develop).

If all IO circuitry is fully contained within a certain power domain, it's adequate to analyze these stress configurations within that domain. For example, Vds of the NMOS output in the schematic below only depends to first order on the discharge path between IO and VSSA, not to pads in other power domains. If signal devices are connected directly across pads of different power domains, it may be necessary to customize the cross-domain voltage clamping capability of the protection circuit to match the failure threshold of the signal path, possibly by adding clamps or diodes directly across the threatened devices, or buffering the signal path with series resistance or intermediate stages.

The schematic includes parasitic npn devices that are either inherent to NMOS transistors or form between closely spaced but unrelated n-type diffusions. Rogue npns of the second type can factor into the ESD problem if they are not passivated by substrate tie-downs or if the ESD circuit capability is relatively poor.



It's instructive to examine a conceptual IV plot of all partial discharge paths between the IO pin and Vss. Each partial curve below has an "x" indicating its point of failure. Acting in parallel, the dedicated path (red) is not able to prevent the rogue parasitic npn from conducting some fraction of the total test current, and failure to the parasitic itself occurs at a voltage below the failure level of the ESD circuit or other partial discharge paths. It's possible that the total combined partial currents may be sufficient to pass the targeted test level without failure to the parasitic, but parasitic npn behavior is unpredictable and it is better to passivate such devices by following the latch-up rules. If the rogue npn were not a factor in the problem, the dedicated discharge path as drawn should be able to safely channel most of the total test current upto the targeted testing level without allowing any of the MOS signal paths to be damaged. Making this plot is not necessary when analyzing circuits, but it's useful to keep this picture in mind.



Signal/parasitic paths should ideally not carry significant currents for total pin currents corresponding to the targeted testing level (Itarget). Certain problematic paths, such as parasitic npn's, may bypass and defeat the ESD circuit, but not survive significant testing levels. Other paths, such as NMOS outputs, have a very low failure current and Vds must be kept below their failure values.

Partial paths such as the NMOS output are at high risk of failure if the ESD circuit is not optimized to clamp Vds below its failure value because NMOS Ids failure current can be very low in Jazz processes for arbitrary device layout. Other paths with high failure voltages, such as MOS inputs, are at relatively low risk of failure even though their current failure thresholds are low because typical ESD protection circuits will probably limit Vgs voltage below their failure values (3.3V MOS gate oxide can survive > 16V under HBM test conditions, for example). For all signal paths, however, it's clear that some kind of explicit discharge path must be present to shunt prospective victim devices, or destructive levels of voltage (upto the VHBM testing level) can develop.

There is some latitude in choosing a viable topology for the on-chip ESD network. As shown in the figures below, power supply clamps can be shared between different domains by using ESD diodes (to conserve layout area; this scheme is used in the digital IO cells). To minimize noise coupling, users may daisy-chain or couple the grounds of each power domain to a common ESD ground bus (in a star configuration) instead of using a single global ground bus. For fail-safe operation, the supply side diode may be routed to an uninterruptible ESD bus that is not directly connected to the signal path circuitry. At high performance pins, the parasitic capacitance of ESD diodes can be managed by using smaller standard diodes with fewer active fingers. Series diodes can be employed to extend IO pin voltage travel or provide better protection for IO pins with reduced voltage travel.

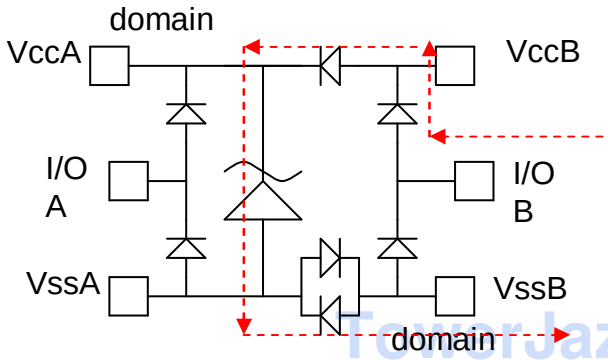


Figure_4A. Sharing ESD clamp in domain A with IO circuitry in domain B

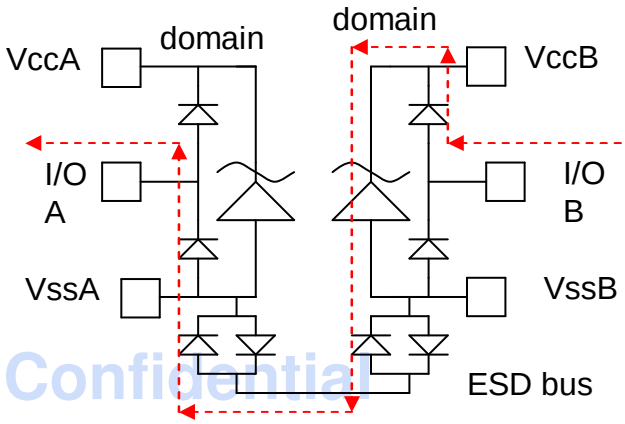


Figure_4B. Using a dedicated ESD ground bus to couple power domains

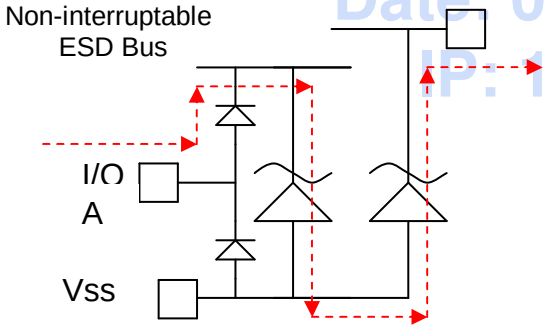


Figure 4C. ESD protection for fail-safe IO pin. (IO circuitry connected to interruptable Vcc.)

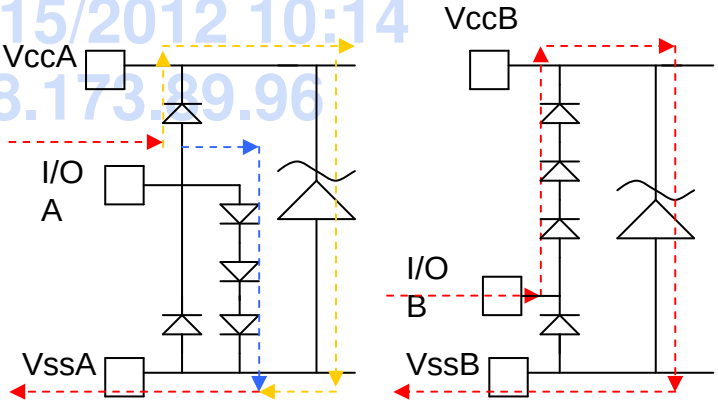


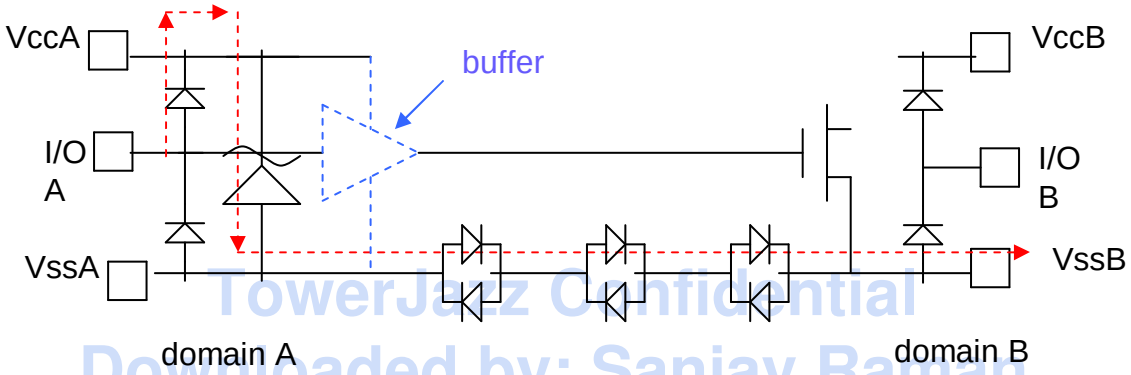
Figure 4DA and 4DB. ESD protection for pins with limited voltage travel (I/O A) or extended voltage travel (I/O B)

For special applications, it may be possible to rely on the self survivability of the signal devices themselves, or to use signal devices for ESD protection. Large transistors or transistors with many fingers or in large arrays may collectively have a high failure current. Typical failure threshold information for signal devices is provided in a later section. However, the actual performances of these non-standard solutions can be difficult to predict to first order, because their characteristics are sensitive to factors that are not always managed deliberately, such as layout symmetry, type of metal connection or the proximity of substrate tie-downs.

Cross domain protection and passivation of parasitic npn's

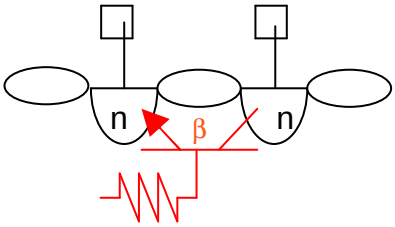
It's clear that HBM strikes across pins of different power domains can develop larger voltages than across pins belonging to the same domain, especially if a product has multiple power domains and uses cross coupled ESD diodes to isolate their grounds in an open daisy-chained fashion. This higher voltage can damage signal paths that are connected to pads in the different domains, and trigger parasitic npn devices that may not otherwise be activated by lower peak pin-pin voltages.

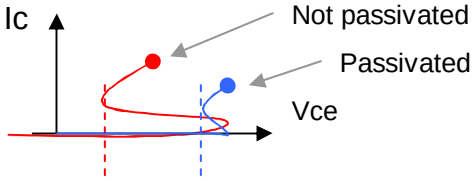
One undesirable situation occurs when signal circuitry clamped by the ESD protection network of a given power domain is actually connected to the power or ground of a different power domain. This may happen, for example, if core circuitry is connected directly to an IO pin without using a buffer.



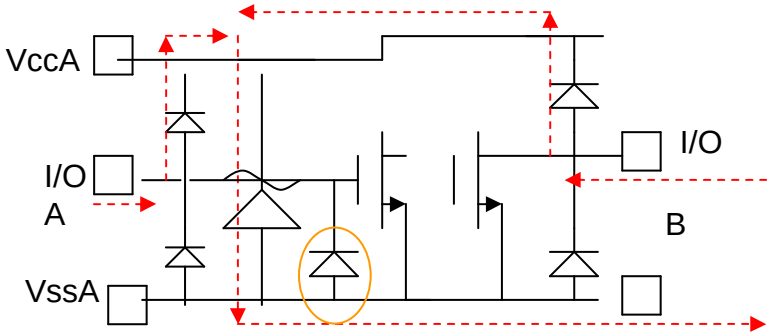
Vgs of the MOS input above is not necessarily clamped to safe levels because it is determined by multiple cross-domain ESD components and bus resistance.

Parasitic npn's are made from closely-spaced n-type diffusions in the same pwell. If the npn emitter/collector terminals are connected to pins that develop high voltage, the npn may snap-back, draw current and possibly burn out. The npn snapback holding value can be elevated by using stronger substrate tiedowns or larger n-n spacings to reduce npn base de-biasing resistance or current gain. Parasitic npns immunized in this way are effectively passivated and do not need to be considered as part of the ESD problem..





A typical parasitic npn cross section (above) and IV characteristics (below); dashed lines represent snapback holding voltage.



Prospective parasitic npns can form between cathode of n+/sub antenna diode (circled) and source of NMOS input or drain of the MOS output (B), or between nmos output and source of MOS input, for example, but relative risk can only be determined by inspection of the layout (large n-n spacings or presence of guard rings)

Protection for digital IO cells

Some products will use IO cells from the digital library to form part of the pad ring. Certain supporting cells must also be included in the ring to complete the ESD circuit for each isolated digital domain (in each padcell, IO pins are coupled to the 3V (VDDP) or 5V (VGG) supply rails thru ESD diodes but there is no supporting power supply clamp). Corner cells (ptgcor) should be connected to the pad cells. Each corner cell has separate 5V and 3V tolerant "bigFET" power supply clamps for the VESD and VDD busses, respectively, where the corner cell VESD clamp is shared with the VDDP and VGG busses thru ESD diodes, as shown in the diagram below. If a corner cell cannot be used, it may be possible to connect a mixed signal bigfet cell to the VDDP or VGG rails instead.

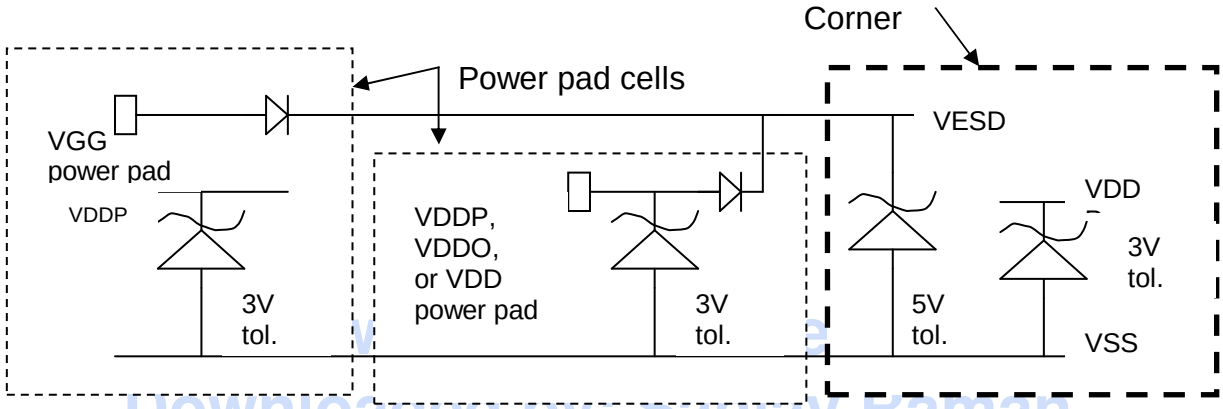


Figure 1. Schematic showing cell content and connectivity of on-chip ESD protection circuitry.
VDDO – power pad for output buffer circuitry
VDDP – power pad for pad-ring logic circuitry (level shifters, etc.)
VDD – power pad for core logic
VGG – 5V tolerant power pad
VESD – internal bus

Certain non-corner cells (power padcells and pesdclamp1) contain bigFET clamps connected to the VDDP power domain rails, but these are not rated to handle full HBM events (they may not be conductive for the entire HBM ESD event). Furthermore, if 5V tolerant padcells are being used for 3V applications, it is advisable to shunt the VDDP and VESD power rails together, because the 3V-tolerant clamp in the corner cell is superior to the 5V-tolerant clamp. See the digital IO cell documentation for more specific ESD circuit connectivity information.

It's important to know that the VESD bus may be at risk of charging up after successive HBM strikes because there is no regular circuitry that will bleed accumulated residual charge. The efficiency of a transiently-triggered clamp may be reduced if the initial voltage on the sense node is large enough to turn off the driver transistor (see description of mixed signal bigFET in a later section). It's recommended to add a de-biasing resistor between the VESD bus and ground to keep the VESD bus discharged and ready to respond to additional ESD pulses. A long and narrow PFET transistor configured as a resistor in the mega-ohm range is expected to be beneficial.

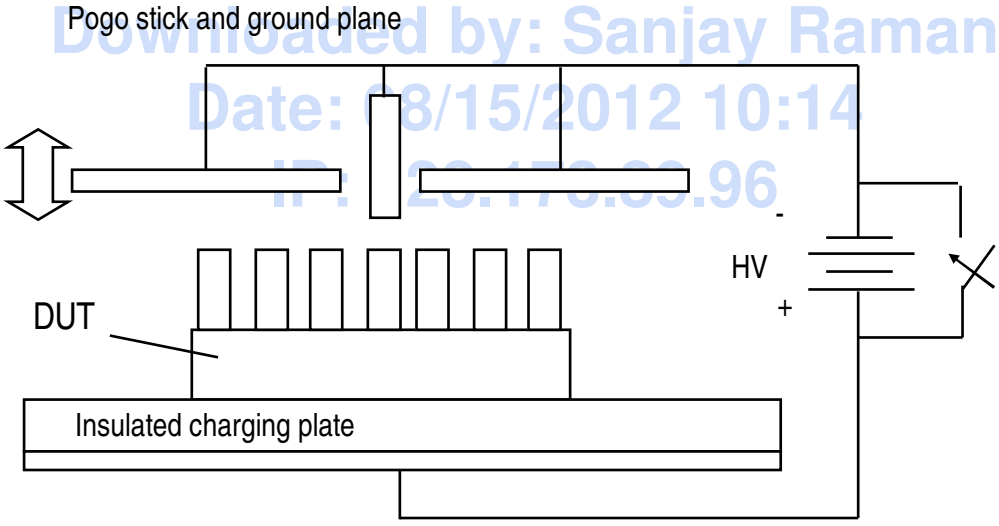
As was specified earlier, all analog and digital grounds should be coupled with a metallized path, using cross-coupled ESD diodes for noise or substrate isolation if necessary, to create a low impedance discharge path between all bonding pads wired to package pins.

Countermeasures for Machine and Charged Device Models (MM, CDM)

The external test circuit and typical testing plan for MM is similar to HBM, except that the fixed capacitor is 200pF, and the series 1500 ohm resistor is omitted. The current flowing into a pair of pins is strongly influenced by the resistance looking into the pins themselves. The pulse rise time may be very sharp, such that the current waveform may be oscillatory and sensitive to the product's pin-pin input reactance. The uncertain current waveform in response to MM events makes it difficult to predict how a product will respond to a standard testing level.

Since MM testing can expose HBM type failure modes, good component-level HBM reliability can contribute to better component-level MM reliability. Since MM testing may also expose CDM type failure modes, following the recommendations for CDM in the next paragraphs may also result in better MM reliability.

In the CDM test, a part is placed dead-bug position between isolated charging plates with an applied electric field of zero (HV shorted out). Under a non-zero electric field, a single pin is grounded using a "pogo stick", resulting in charge flowing into the part to re-establish electrostatic equilibrium. The pin may be retracted and re-attached after the field is returned to zero, resulting in a bipolar stress event.



The magnitude of current depends in part on the capacitance of the circuit relative to the backside of the plate, which in influenced by die size, package form factor, etc. Since individual pulses usually have very sharp rise times, series inductances in the discharge paths may develop large pin-pin voltages that can threaten dielectrics, such as gate oxides. Unlike the HBM event, where the discharge current is on the order of amps and ideally flows only thru the peripheral IO branches of the chip, CDM current can conceivably be on the order of 10's of amps, and may partially low to all internal nodes as the voltages on the chip equalize.

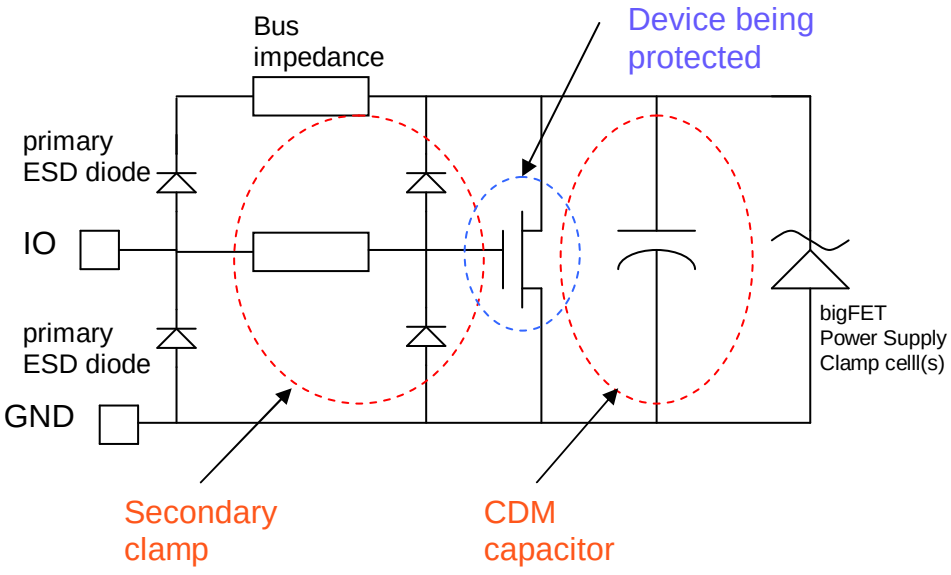
CDM testing results are therefore very difficult to predict using simple calculations. Foundries cannot specify minimum CDM reliability targets for arbitrary product designs.

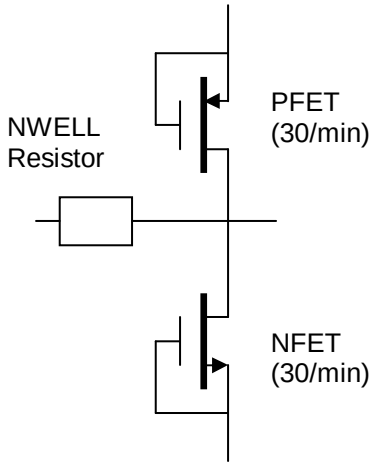
Higher CDM current pulses associated with larger products may have sufficient power to enable HBM-like failure modes. This means that good component-level HBM reliability may contribute to better component-level CDM reliability. However, for products with smaller capacitance, total charge and peak total currents, thermal damage (melting) may not be the primary concern.

A common strategy for on-chip CDM protection is to prevent gate oxides that would ordinarily be connected directly to different bonding pads from being blown out by large pin-pin voltages. Assuming that most of the CDM current is discharged thru the traditional HBM dedicated path, “secondary clamps” (typically using small ESD diodes) should be used together with a debiasing resistor to control the voltage developed across the oxide terminals in question. This is shown below.

The resistor (typically 150 ohms nwell) limits the reverse current thru the secondary diodes, whose reverse breakdown voltage is lower than the gate oxide failure threshold. Diodes can be minimum sized, because the peak power associated with the reverse current is expected to be small. ESD diodes are good choices for 3.3V MOS inputs because they come standard with the required latch-up guard rings. It’s not advisable to use gated diodes made from standard 3.3V NMOS for this application because Jazz 3.3V NFET transistors may fail immediately after snap back and can compromise the pin’s HBM rating. For 1.8V inputs, however, it may be advantageous to use gated 1.8V transistors instead of ESD diodes because 1.8V NMOS outputs are more robust under HBM stress and have reverse breakdown voltages that are better matched to the 1.8V gate oxide. In the figure below, secondary diodes shunt the IO pin to both power and ground. Note, however, that secondary clamp diodes are usually only “required” for shunting oxide terminals connected directly between IO and one of the rails.

Instead of a full secondary clamp, a series gate resistor alone can be used to enable a RC charging delay >> 1nS that prevents the dielectric from developing a damaging voltage. Another CDM counter measure is to use large supply capacitance to clamp the voltages that develop across the power domain rails. Jazz unfortunately cannot specify the required CDM capacitor values to achieve specific CDM ratings for arbitrary products.





Alternative implementation of secondary clamp (may be advantageous for 1.8V MOS Inputs)

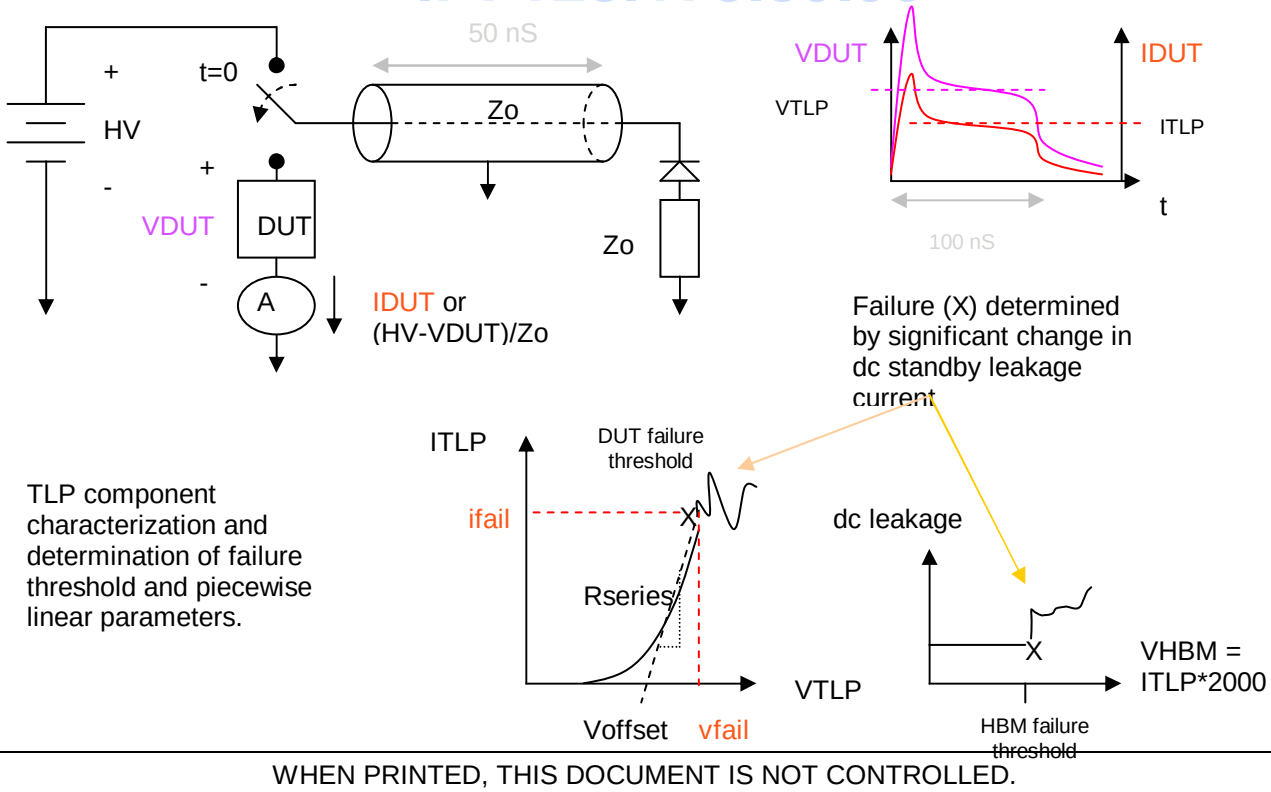
Typical HBM failure thresholds of signal devices

Transmission Line Pulser Measurements

Jazz has used transmission line pulser (TLP) measurements to acquire the fundamental IV characteristics and HBM failure thresholds of components relevant to solving ESD problems. TLP data consists of measured voltage, current and dc standby leakage in response to HBM-like (but rectangular) pulses forced through two terminals of a component, as shown in the simplified figure below.

Device IV behavior under incremental TLP conditions can often be represented by a battery (Voffset) with series resistor (Rseries). Forward biased ESD diodes, for example, will usually have Voffset = 1V (see table of standard ESD devices). Device failure is identified with TLP current and voltage values at which the dc standby leakage changes significantly. It's possible that subtle device changes affecting product functionality may occur prior to a strong change in dc leakage, but this is difficult to analyze. Most components are assumed to have well defined current and voltage failure thresholds that are abrupt and catastrophic.

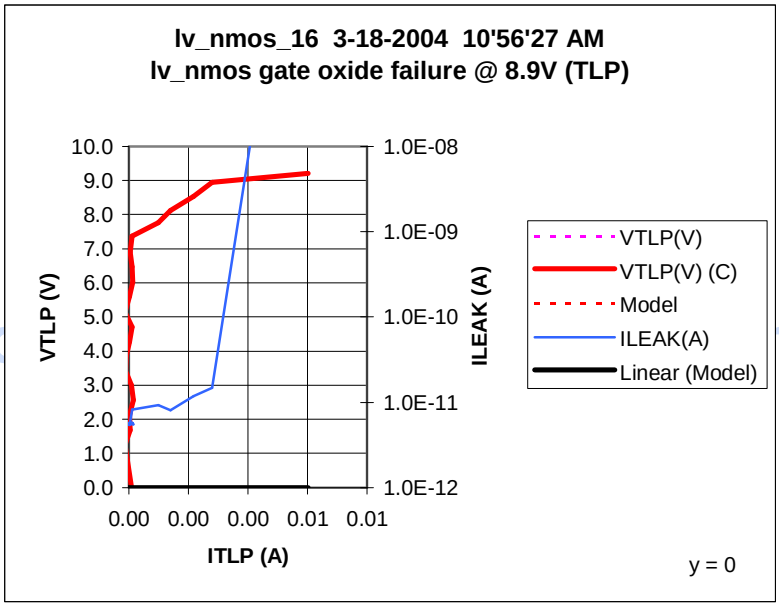
Note that TLP current and voltage are evaluated at waveform levels consistent with defining average pulse power, whereas HBM current and voltage are usually associated with peak pulse power. A conversion factor of 2KV HBM/A TLP derived from thermal equivalence calculations is used to map TLP current failure thresholds (A TLP) to definite HBM testing levels (V HBM). The equivalent HBM current is then 2KV HBM / A TLP / 1500 ohms or 1A TLP = 1.3 A HBM. For validating complex test structures, it is a good practice to extend TLP analysis to currents equal to their required HBM current value, just in case a failure mode is driven by peak voltage instead of thermal failure.

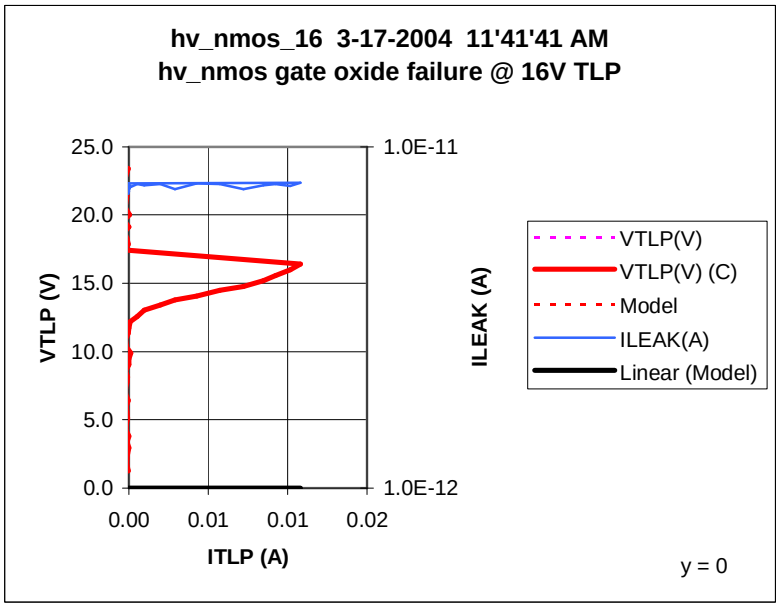


TLP component characterization and determination of failure threshold and piecewise linear parameters.

Gate Oxide

The figures below showing the pulsed IV curves for positive polarity stress on NMOS gates relative to device S/D/B grounded indicate that the 1.8V and 3.3V gate oxide voltage failure thresholds are typically 8.9V and 16V under TLP stresses. The onset of appreciable stress current is actually at 7V and 12V for 1.8V and 3.3V devices, respectively, but failure in terms of change in leakage or development of an open circuit occurs at 8.9V and 16V. Under actual HBM stress, it's expected that 1.8V and 3.3V gate oxide will sustain > 10V and > 16V because the total charge associated with a Gaussian HBM strike is smaller than in a rectangular TLP pulse with the same peak voltage.





MOS output overview:

It may be helpful to summarize some concepts and trends before reviewing detailed data:

- Wide metal strapping along the full width of transistor fingers may result in current crowding and low drain failure current after snapback in MOS outputs, especially 3.3V NMOS.

  Historically, conservative contact space to gate and active contain contact rules are expected to help elevate transistor failure current. For NMOS, current crowding was assumed to be correctable by adding NWELL drain extensions, which encourage the current density to be uniform along the finger width. The larger total drain failure current together with nwell resistance is supposed to create high effective Vds prior to device failure.

- Experimentally, a key factor in MOS survivability and ability to conduct current after snapback is found to be body tie-down strength/proximity. Transistors with very close body tie-down proximity or internal tie-downs (for arrays) may fail at very low currents and immediately after snapback, because the parasitic bipolar transistor that carries the snapback current cannot turn on. Transistors with strong body tie-downs may have higher snapback holding voltages, but they may have low failure currents.

- Negative factors for obtaining large drain failure current are then: close or interior body tie-downs for large arrays, and wide metal contacting the entire width of each arrayed finger.

- 3.3V NMOS transistors with nwell drain extension are found to typically not survive snapback if body tie-downs are at minimum proximity. 1.8V NMOS transistors also exhibit poorer failure current with body tie-downs spaced at minimum proximity, but are found to generally survive snapback. An nwell extension on the drain of 1.8V NMOS transistors will apparently consistently result in large drain failure voltage ~ 18-20V regardless of body tie proximity. This effect was only seen in 3.3V NMOS with non-minimum body proximity (~ 10um).

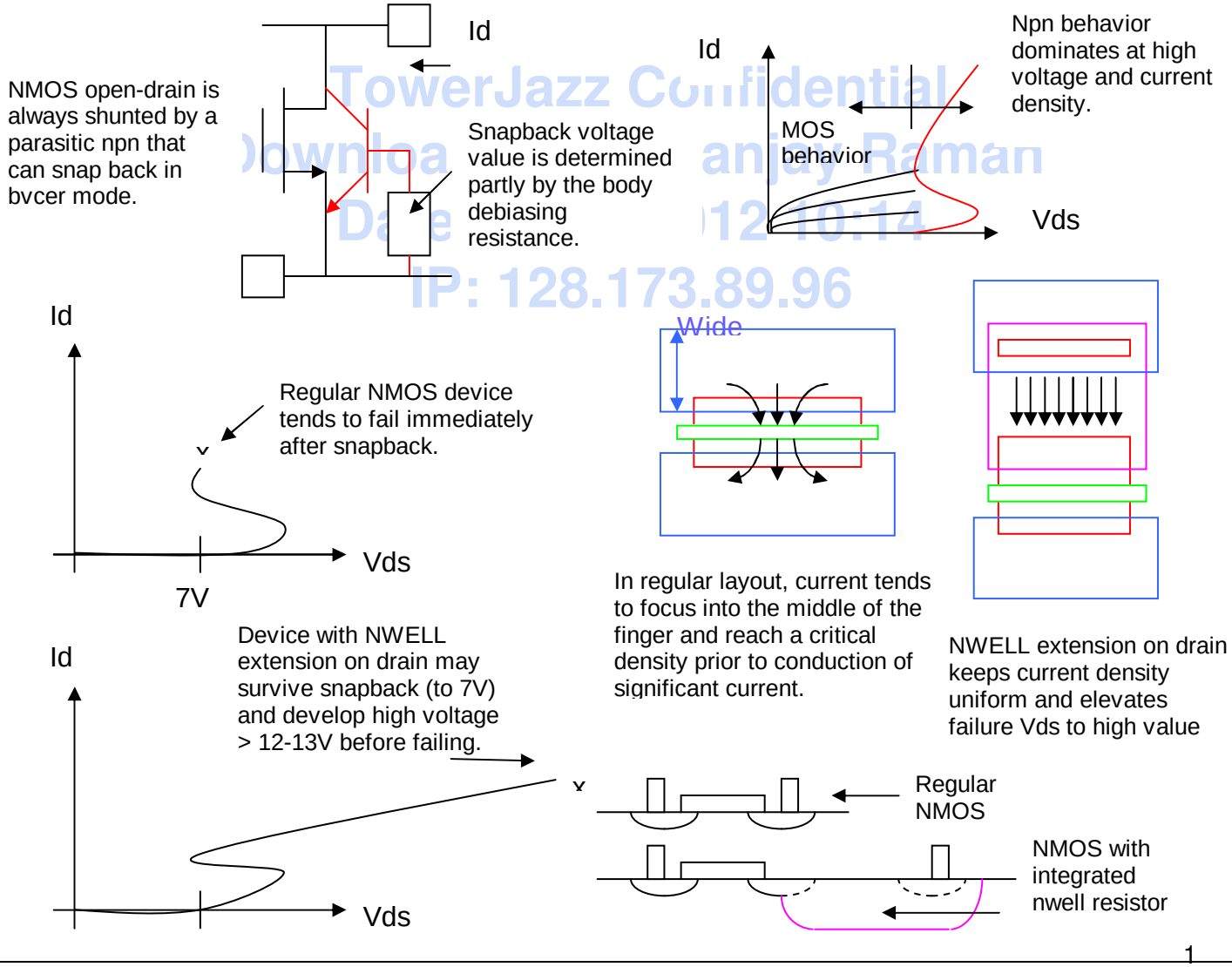
- The use of square-ish finger array geometries where fingers are only contacted with wide metal at their ends can also enable NMOS to survive snapback and demonstrate high drain failure current. 1.8V and 3.3V NMOS arrays with this style of layout exhibited relatively high failure drain current. These layout styles are considered positive factors for transistor self survivability and may be an alternative and more compact solution to adding nwell extensions to the drain. The snapback voltage may be reduced in such devices, but device failure voltage is usually comparable to that in devices that do not have positive layout factors, and can be much higher if significant discrete series resistance is added.

- PMOS failure voltage is typically greater than in NMOS transistors of the same type (1.8V or 3.3V) and PFETs tend to generally survive snapback and exhibit nonzero failure current. If the protection circuit is designed to clamp to reasonable values (<10V for 3.3V circuits and < 7V for 1.8V circuits), failure to PFETs at low testing levels should not be a concern.

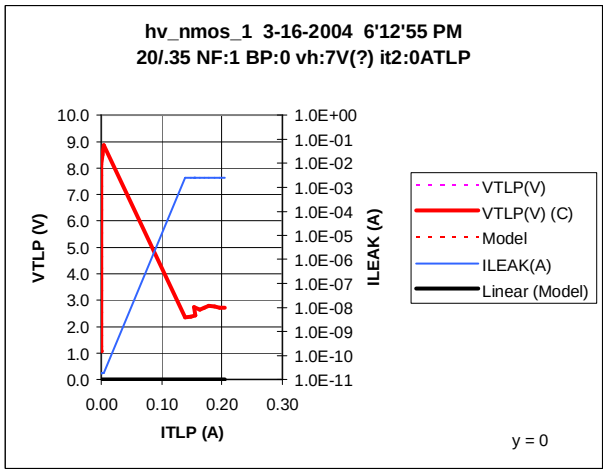
3.3V NMOS outputs

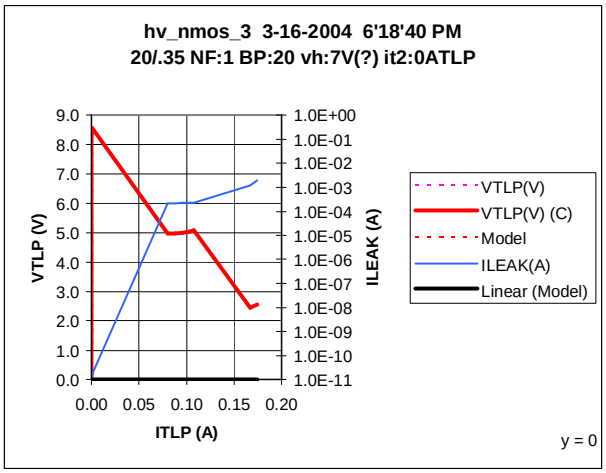
3.3V NMOS open-drain output transistors in Jazz technologies with arbitrary layout typically do not survive Vds snap back of the parasitic npn without the assistance from an integrated NWELL series resistor. Data specific to CA18 furthermore indicates that adding the NWELL resistor will not always prevent device failure. This suggests that, although using the drain extension is still recommended, limiting Vds below its snapback holding value is the most reliable HBM ESD protection strategy.

As explained in the figures below, the snapback holding voltage of a single finger transistor with strong body tie-downs is expected to be approximately 7V in all Jazz 3.3V NMOS. The failure current after snapback is understood to be low (assumed to be zero) because current tends to focus into the center of the transistor, and it may reach a critical density there prior to any significant conduction along the other partial widths. Traditionally, adding an integrated NWELL extension to the drain forces current to flow more uniformly along the transistor width and results in a somewhat larger total drain failure current. This effect, together with the longitudinal nwell resistance, is intended to give rise to a large effective Vds at the point of device failure.

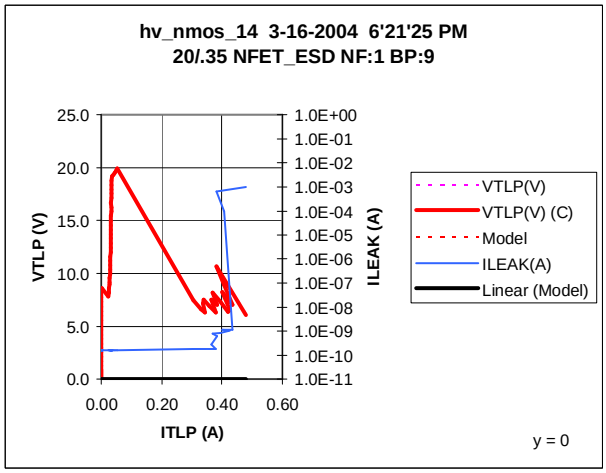


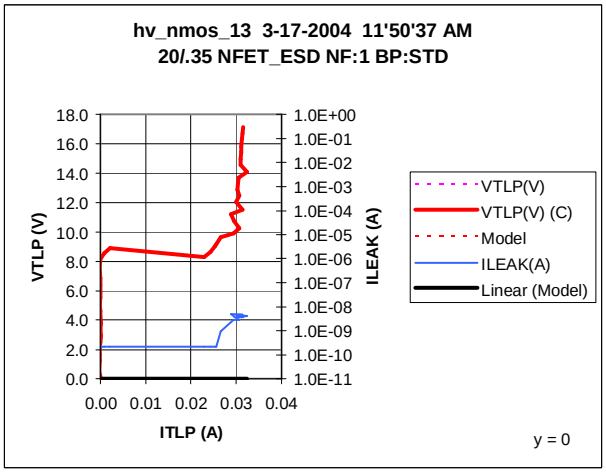
A regular gate-grounded 20/.36 single-fingered NFET with wide metal contacting the entire finger width has the typical Id-Vds TLP curves shown below for body tie-down proximities of min and 20um. In both cases, the device is damaged immediately after drain-body breakdown (noticeable change in leakage current) and (presumably) snapback of the npn transistor. (The actual snapback holding voltage is not resolved in the measurement because the failure current is too low)





A similar device with an integrated series nwell resistor (pcell nfet3p3_esd modified to have a body tie proximity of 9um (bottom left)) exhibits snapback to approximately 7V, and the effective Vds increases to ~ 20V prior to device failure under secondary breakdown. This is the desired result for nwell extensions. Vds~20V should be well within the voltage clamping capability of the on-chip ESD circuit. However, the same nfet_esd device with standard body tie-down proximity (bottom right) shows an increase in leakage shortly beyond the point of snapback and prior to the development of high effective Vds. This indicates that the drain extension doesn't always work. The combined result verifies that NMOS snapback holding voltage is approximately 7V (with strong body tie-down), and that it's possible that the NWELL extension can be effective, but not for strong body tie-down.

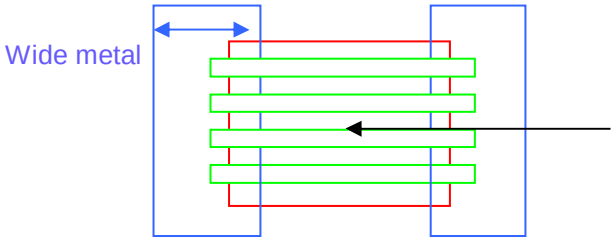




Since using the nwell extension consumes approximately 3x the layout area of a regular transistor, it's of interest to understand other approaches to improving 3.3V NMOS output survivability.

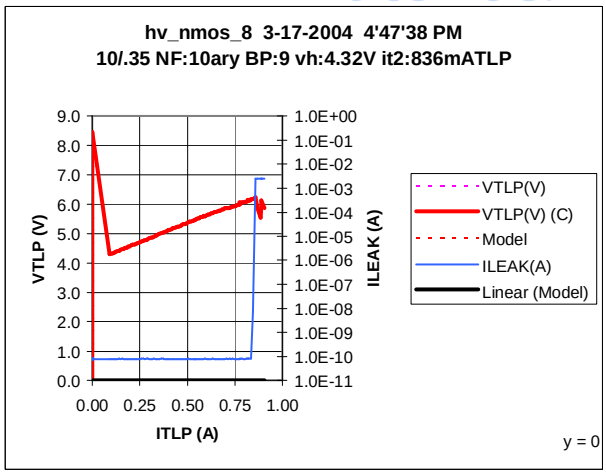
3.3V NMOS outputs (cont.)

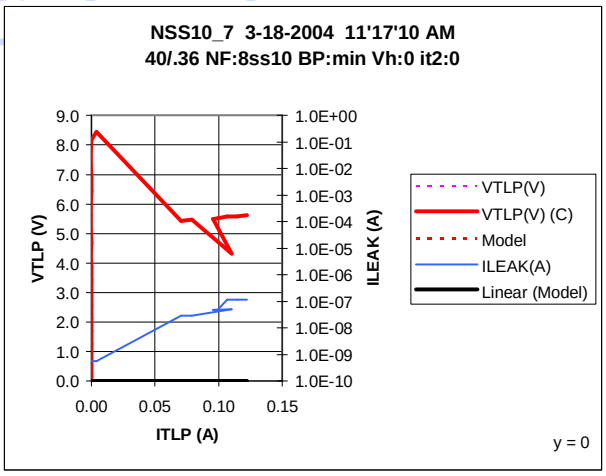
The interior fingers of large square-ish NMOS transistor arrays with a peripheral body tie-down will exhibit strong parasitic npn action because of high base debiasing resistance. Such arrays will usually have a lower snapback holding voltage (parasitic npn BVcer), accompanied by a larger failure current after snapback, especially if the fingers are only contacted at their ends by wide metal (not including silicide or narrow interconnect metal that is generated with the device).



Layout of array of parallel NMOS fingers with no interior body tie-downs and wide metal connections only at the finger ends. The parasitic npn associated with the interior fingers may turn on strongly and exibit finite failure current.

As shown below (left), a square-ish 10-fingered 10/.36 3.3V transistor array laid with these positive layout factors, with a 10um body tie proximity (near the source connection) and without NWELL drain extensions will survive snapback and conduct as much as 836mA TLP (1672V HBM, 1.11A HBM) prior to failure, which is a substantial 8mA/um TLP (11mA/um HBM). The snapback holding voltage is 4.32V, which is lower than in a single finger transistor with strong body tie-downs (7V), but the failure voltage is approximately 6V, which is close to the failure voltage of a transistor with very strong body tie-downs. In contrast, an 8-fingered 20/.36 3.3V transistor array (right) with 2um wide metal strapping on each finger fails immediately after snapback, even though the array is large and each finger is segmented into 10um to encourage good current uniformity.

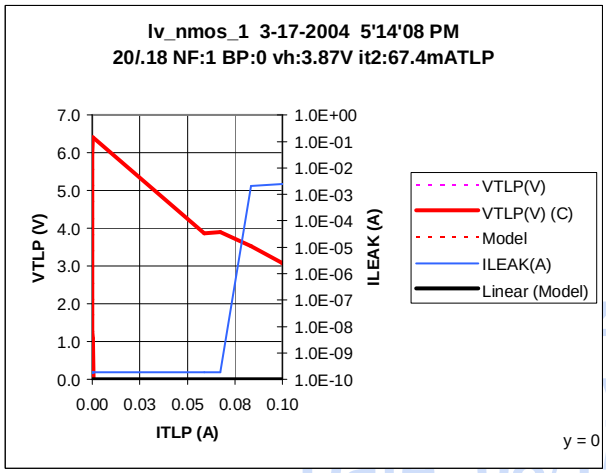


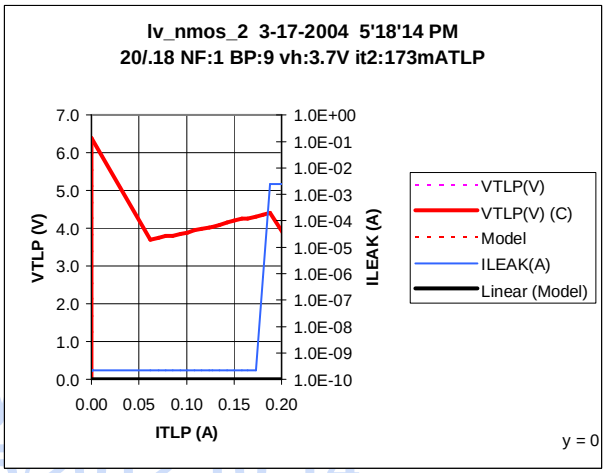


For the 10x10/36 array with positive layout factors, adding a non-integrated nwell or poly resistor in series with the drain could significantly elevate the effective Vds failure voltage above the snapback holding value. With a 1.1A HBM failure current, 10 ohms would increase the effective Vds failure threshold by ~ 11V, to likely well within the voltage clamping capability of a reasonable ESD protection circuit. However, it's clear that 3.3V MOS failure thresholds can vary significantly with finger geometry, substrate-tie proximity and metal connectivity. Unless these factors are managed deliberately, it's recommended to always design the ESD circuit to clamp Vds of 3.3 NMOS outputs to below 7V and assume the transistor failure current is zero.

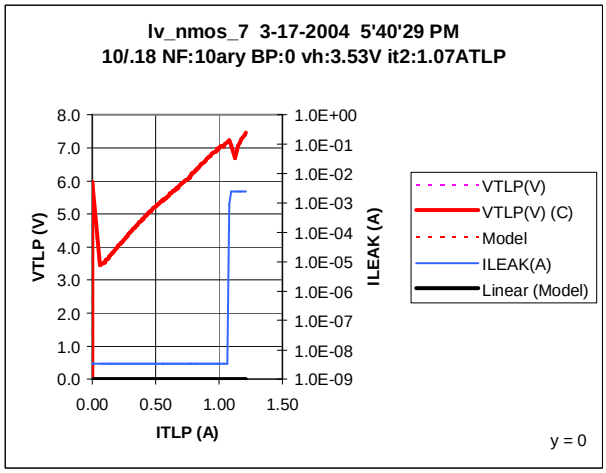
1.8V NMOS outputs

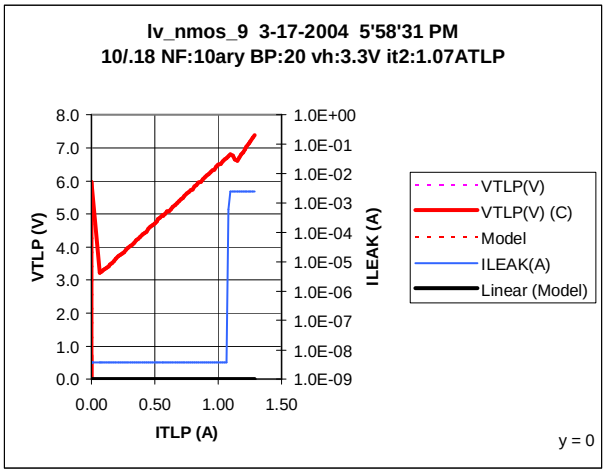
Single finger 1.8V NMOS transistors typically survive snapback and exhibit appreciable failure current values that vary with the proximity of the body tie-down. A 20/.18 NFET with minimum body tie proximity (single stripe near source) (left below) has a holding voltage of 3.9V and failure current density of 3.4 mA/um TLP. The same transistor with a 9um body tie proximity (right below), has a higher failure current density of almost 9mA/um TLP. Failure Vds is in both cases is 4V. Note that similar arrays of 40/.18 fingers (not shown) also exhibit ~ 10mA/um TLP, provided the body tie proximity is 10um. This suggests that body tie-down proximity is a contributing factor in determining the failure threshold of these devices, as it is for the 3.3V NMOS.





A 10x 10/.18 array with positive layout factors will also exhibit a failure current density close to 10mA/um TLP regardless of body-tie proximity between min and 20um, presumably because the interior npn fingers are always sufficiently isolated from the tie-down and turn on strong. The device holding voltage is 3.3-3.5V, which is slightly lower than the snapback holding voltage in single finger devices, but its failure voltage (~5V)is comparable after deembedding ~ 2 ohms.

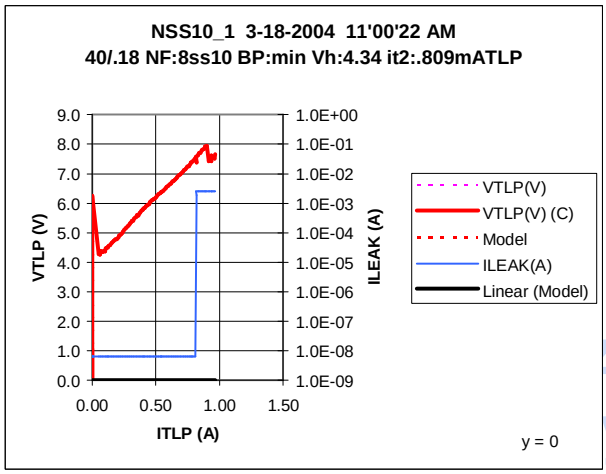


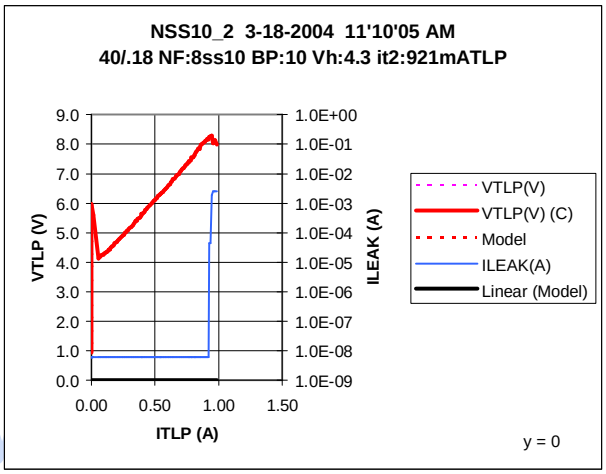


These data suggest that adding series resistance to 1.8V NMOS output transistors with positive layout factors and remote body tie-downs is always effective in elevating Vds failure threshold.

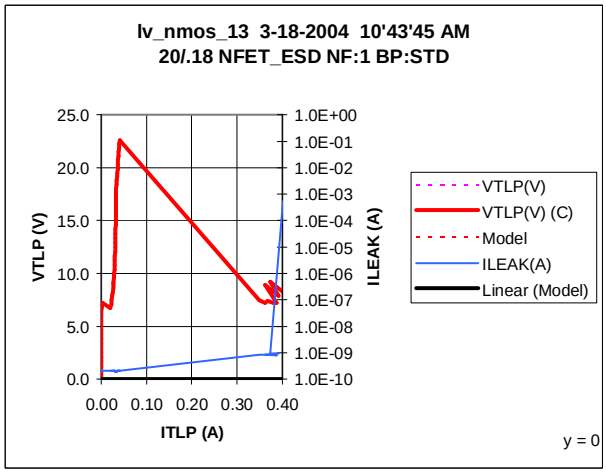
1.8V NMOS outputs (cont)

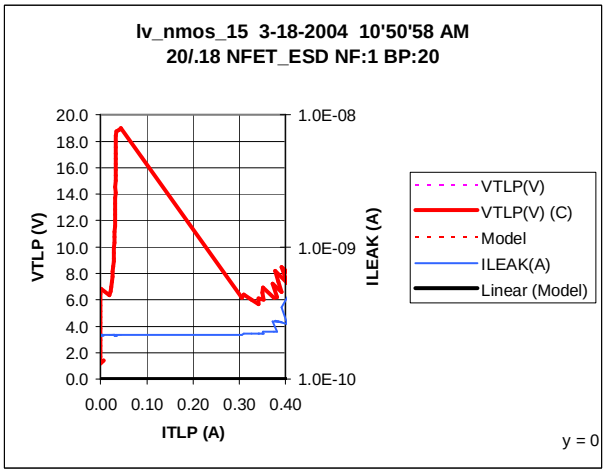
Large 1.8V NMOS arrays in which the fingers are segmented into 10um widths and are strapped by wide metal (2um) have a relatively low but nonzero failure current density of 2.6mA/um TLP, which is much smaller than in the array with shared active (9-10mA/umTLP. The device holding voltage is a higher 4.35V (compared to 3.3-3.5V in the square-ish array). The failure Vds is estimated at 6V. These trends are consistent with the parasitic npn not turning on as strong as in the non-segmented fingers, and current possibly crowding into the middle of each finger segment. 3.3V NMOS using this same geometry tend to fail immediately after snapback regardless of body tie proximity.





Using an nwell extension on the drain of 1.8V NMOS outputs is found to be generally viable for elevating 1.8V NMOS Vds failure voltage, regardless of body tie-down proximity. A 1.8V nfet_esd device with standard (min) and enlarged 20um body-tie proximity both survive snapback and exhibit holding voltages of approximately 6V. The effective Vds of both transistors is greater than 18V prior to catastrophic device failure.

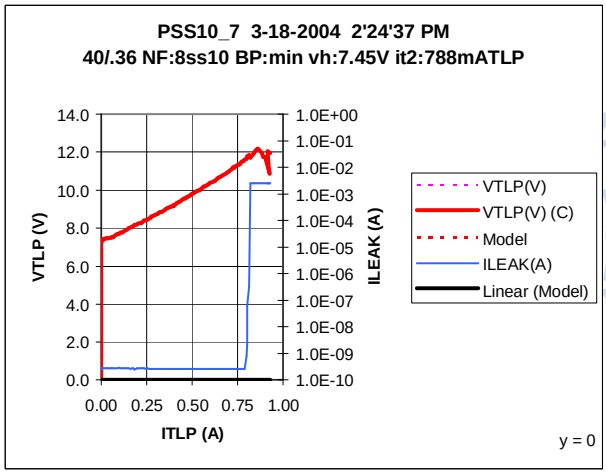


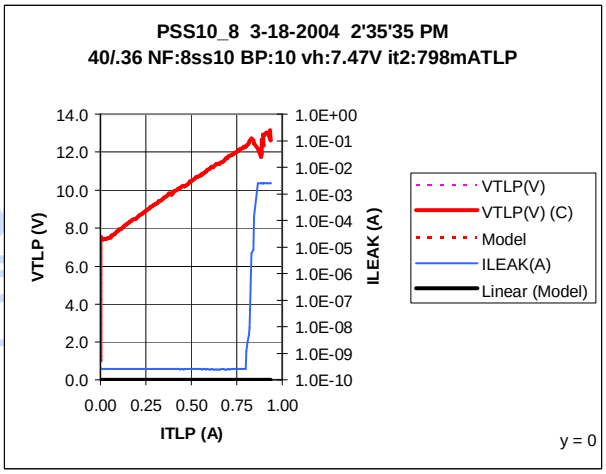


3.3V PMOS outputs

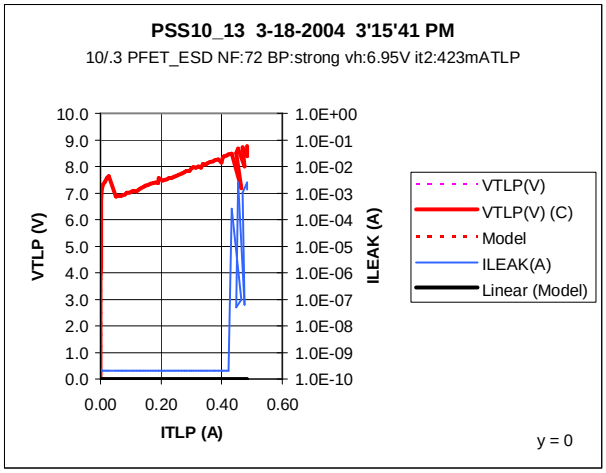
PMOS data was only available for arrays of transistors with fingers segmented into 10um widths and strapped with 2um wide metal. Based on the results for NMOS outputs, this is expected to reduce the failure current of the array relative to transistors having favorable layout factors.

Snapback in the parasitic pnp associated with 3.3V PMOS is not strong, as evidenced below for 8x 40/.36 arrays of fingers laid out in 10um segments with a peripheral body tie-down. The typical 2.5mA/um failure current failure threshold for the same geometry is comparable to that in segmented 1.8V NMOS arrays contacted by wide metal (2.6mA/um), and relatively high compared to 3.3V NMOS (zero). This suggests that typical 3.3V PMOS with positive layout factors may actually have a high failure current density. The similar responses for 8x 40/36 arrays of 10um segmented fingers with minimum (below left) and 10um (below right) body tiedown spacings suggest that device failure thresholds are not sensitive to body tie-down proximity (outside the array). The transistor failure voltage is consistently greater than 10V (compared to 6-7V in 3.3V NMOS), which should be within the voltage clamping capability of a reasonably designed ESD protection circuit (see examples).





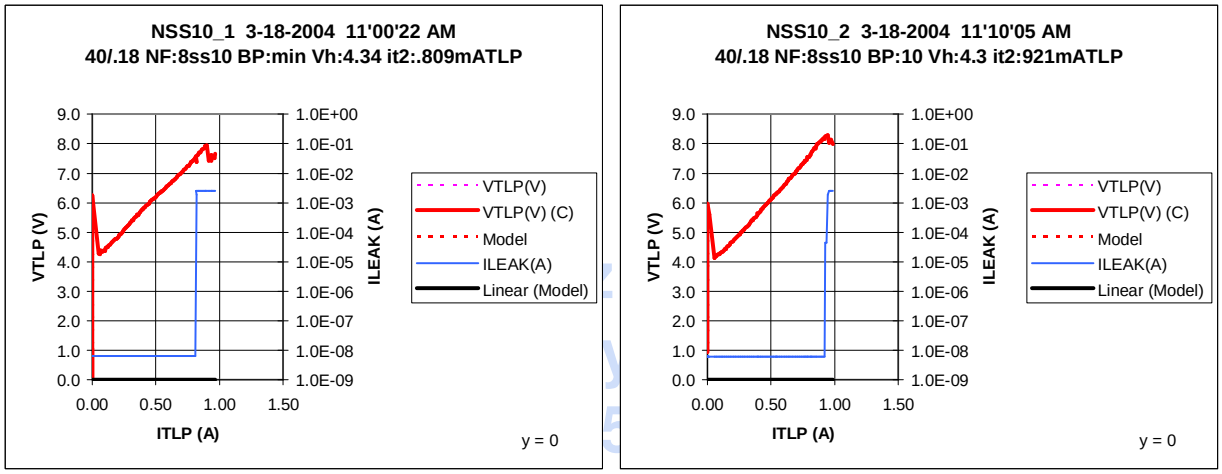
A standard cell pfet3p3_esd array incorporating conservative contact space to gate and active contain contact dimensions has very low failure current density < 1mA/um TLP, possibly because the body tie-downs are drawn in the interior of the array. This suggests that body ties should always be kept to the perimeter of the array.



1.8V PMOS outputs

The data below for 8x 40/18 arrays of 10um segmented fingers and 2um wide metal indicates that larger body tie-down proximity (minimum below left, 10um below right) can elevate the failure current density slightly from 2.5 to 2.9 mA/um TLP. These failure currents are again similar to those in 1.8V NMOS/PMOS and 3.3V PMOS devices with the same layout configuration, suggesting that the reported failure current may be limited by negative layout factors relating to the wide metal or weak parasitic bipolar transistor action.

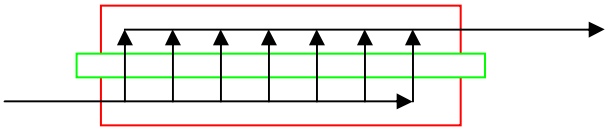
The transistor failure voltage is about 1V higher than in a comparable 1.8V NMOS device, which suggests that the NFET device in a 1.8V CMOS output may be relatively weaker under HBM stress.



There is a 1.8V pfet_esd cell available in the library, which uses more conservative contact space to gate and active contain contact. Jazz doesn't have any data for that device at this time but would suspect that its use of interior body tie-downs in array form would result in a very low failure current density, similar to the pfet3p3_esd array result.

Using layout to maximize the failure voltages of the signal path

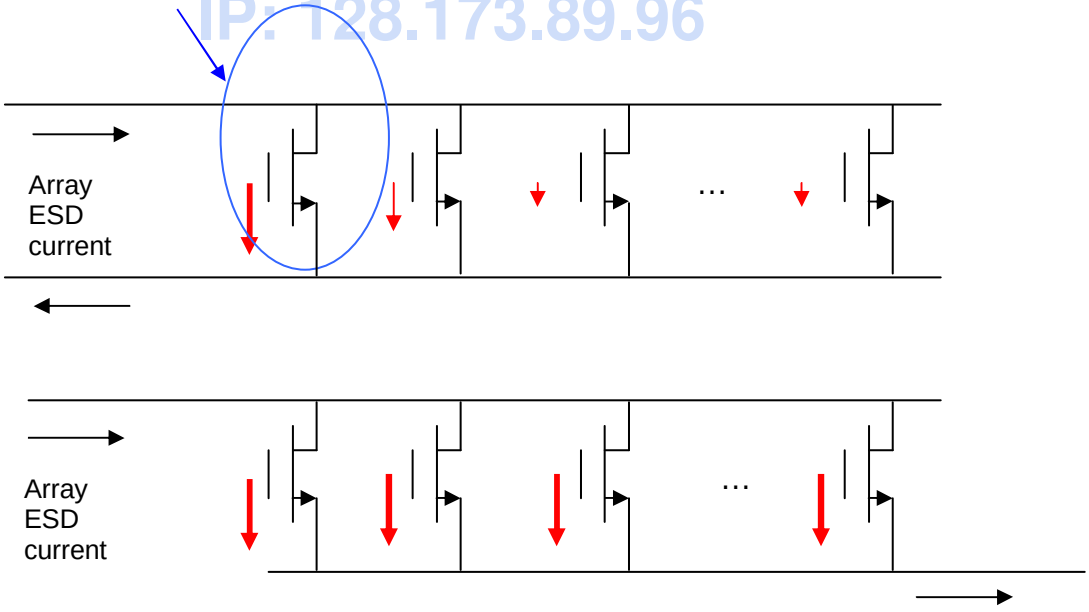
In the above MOS output data, it's observed that square-ish arrays of fingers with wide metal connections only to the ends of the fingers may have a higher failure current than equivalent transistors connected with wide metal along the entire width of the finger. Jazz's understanding is that the "S" trajectory of current flowing in any given finger of an array contacted only at the finger ends with wide metal creates a ballasting action that encourages a more uniform current density along the finger. This ballasting effect is present despite the drain being silicided and strapped by narrow MET1.



Diffusion and narrow metal resistance is believed to create a ballasting effect that encourages drain current density to be more uniform along the finger.

This general concept should be followed when arraying individual components to achieve higher total failure current, such as an array of NMOS outputs, as shown below. If this type of layout optimization is not used, it's possible that only a subset of components in an array will conduct significant current.

"C" shaped current trajectory focuses higher current thru devices with smaller series resistance



"S" shaped current trajectory encourages all transistors to conduct current uniformly because series resistance for each device is the same.

Table of simplified failure thresholds

When screening a complex circuit for HBM weaknesses it's useful to abstract the failure conditions of signal path devices instead of trying to use the above detailed data. This is done in the table below. Provided parasitic npn's are not a factor in bypassing the ESD protection circuit and a baseline pin-pin voltage clamping capability can be established (say worst case < 10V between IO and the power domain rails), signal paths in the schematic exhibiting high voltage failure thresholds, possibly because of large series resistance or series stacked components, can often be immediately dismissed as being an ESD reliability concern.

Component	Typical Vfail	Typical Ifail	Comments
3.3V NMOS output (single finger)	7V	0	Single finger, standard device. Strong Body tie-downs Can't be ballasted by series R
3.3V NMOS output (large array w/ wide metal)	7V	0	Large array of segmented (10um) fingers, 2um wide metal contacting diffusions along full width of each finger.
3.3V NMOS output (large array with positive layout factors)	6V	10mA/um (HBM)	Squarish array of fingers, only finger ends contacted by wide metal. Weak body tie-downs.
1.8V NMOS output (single finger)	4V	4.4mA/um (HBM)	Single finger, standard device. Strong Body tie-downs. Finger width <= 20um
1.8V NMOS output (large array w/ wide metal)	6V	3mA/um (HBM)	Large array, shared source and drain diffusions, 2um wide metal contacting diffusions along full width of each finger.
1.8V NMOS output (large array with positive layout factors)	5V	14mA/um (HBM)	Squarish array, shared source and drain diffusions, only finger ends contacted by wide metal. Weak body tie-downs.
nfet3p3_esd nfet_esd	20V	0	Body tie proximity may need to be kept >=10um for 3.3V NMOS
3.3V PMOS output	10V	> 3.6mA/um (HBM)	Not usually a concern if ESD circuit clamps Vds < 10V
1.8V PMOS output	7V	> 2.8mA/um (HBM)	Not usually a concern if ESD circuit clamps Vds < 7V
3.3V MOS input	> 16V	0	
1.8V MOS input	10V	0	
Resistors	-	-	Resistors limit current, failure not usually a concern
Series capacitors	-	-	Capacitors have high voltage breakdown, failure not usually a concern.
Metal	-	-	Equiv. > 8um wide MET1
Vias	-	-	~ 30 at each interchange (based on ESD diode data)

These typical values suggest that the discharge network can be very effective for most pins if the IO-power domain rail voltage is limited to below 7V in 3.3V circuits and less than 4-5V in 1.8V circuit for the targeted HBM testing level, provided rogue parasitic npn's in the layout are passivated. Examples of how to design the discharge protection networks are given in a later section.

ESD Protection Devices

Overview of Standard Library

The standard esd library ca18_esdlib consists of a 3V tolerant transiently-triggered bigfet power supply clamps and various sizes of p+/nwell and n+/substrate ESD diodes (1-8 0.5x8 junction fingers), as indicated in the table below. The bigFET HBM rating has not been verified in silicon yet, but is expected to survive 2KV HBM. The diode ratings are for forward stress only. These HBM component ratings are based on typical Transmission Line Pulser measurements (data for 6 and 8 fingered diodes is extrapolated). They do not necessarily correspond to the failure threshold of the pin being protected (see design examples later in this section).

Component	Voff (V)	Rseries(Ω)	Ifail / Vfail HBM	Comments
Bigfet_3p3	1	4	TBD	3V tol- clamp ; gnd port tied to substrate
esd_diod_X_p5x8_1	1	3.2	0.39 A / 580V	(Cn, Cp) = (11, 9) (fF)
esd_diod_X_p5x8_2	1	1.4	0.90 A / 1.36 kV	(Cn, Cp) = (22, 19) (fF)
esd_diod_X_p5x8_3	1	1.0	1.43 A / 2.14 kV	(Cn, Cp) = (32, 28) (fF)
esd_diod_X_p5x8_4	1	0.6	2 A / 3 kV	(Cn, Cp) = (42, 37) (fF)
esd_diod_X_p5x8_6	1	0.5	3 A / 4.5 kV	(Cn, Cp) = (62, 56) (fF)
esd_diod_X_p5x8_8	1	0.5	4 A / 6 kV	(Cn, Cp) = (82, 75) (fF)

The table provides the piecewise linear model for each component under forward HBM stress (ESD diodes are only recommended for use in the forward direction) in terms of a battery (Voff) and series resistor (Rseries). This information is useful in estimating the voltage across critical nodes in a given on-chip protection circuit. Device failure thresholds are listed in terms of HBM current and testing level, assuming the entire current of the indicated test level is flowing thru the device. Note that diodes with less than 3 fingers may themselves be destroyed under HBM testing below 3kV. X in the diode component names is either “sub” or “well” for n+/sub or p+/nwell ESD diodes. Cn is the estimated zero bias capacitance of the n+/substrate style diode. Cp is the estimated zero bias capacitance of the p+/nwell style diode

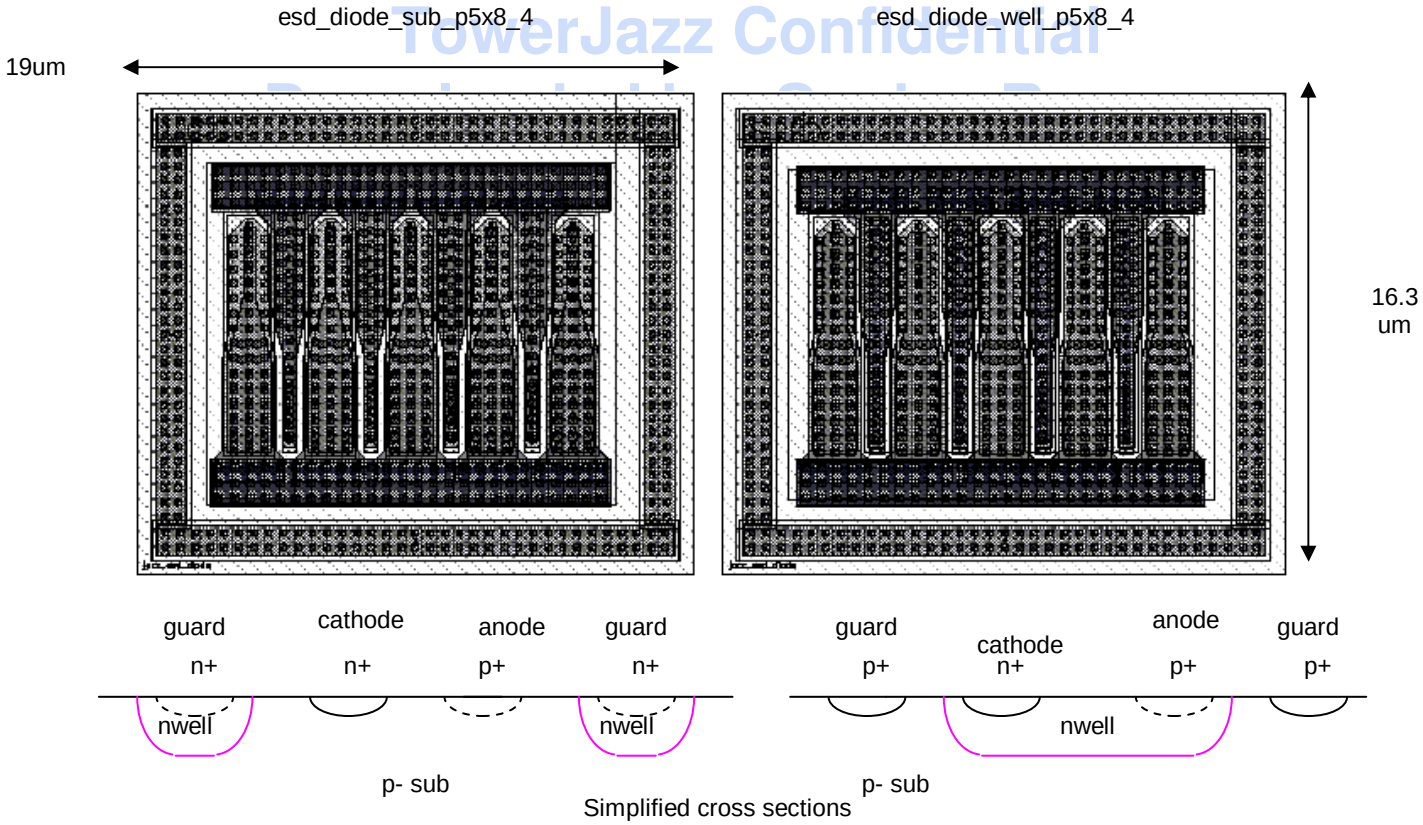
It’s clear that a bigFET cell under positive polarity strikes between supply and ground will behave like a forward biased ESD diode. An HBM strike between IO and ground in the standard on-chip ESD circuit will therefore be effectively discharged by two series diodes, or a battery of 2V with some series resistance. This gives the ESD circuit a reasonable chance to clamp IO pins to within single digit voltages of the power domain rails under typical HBM test conditions (2KV HBM, 1.3A). Factoring in bus resistance effects, however, It may be necessary to use multiple parallel clamps on the same power domain (see design examples).

The 3V tolerant bigFET clamp is compatible with 1.8 and 3.3V supplies. As with all transiently-triggered clamps, the bigFETs should not be hot-plugged into a biased socket, because the timing mechanism that enables the cell to respond to ESD events limits its maximum slew rate. Also, bigFET cells do not provide any dc over-voltage protection for the supply rails.

Mixed-signal ESD diodes

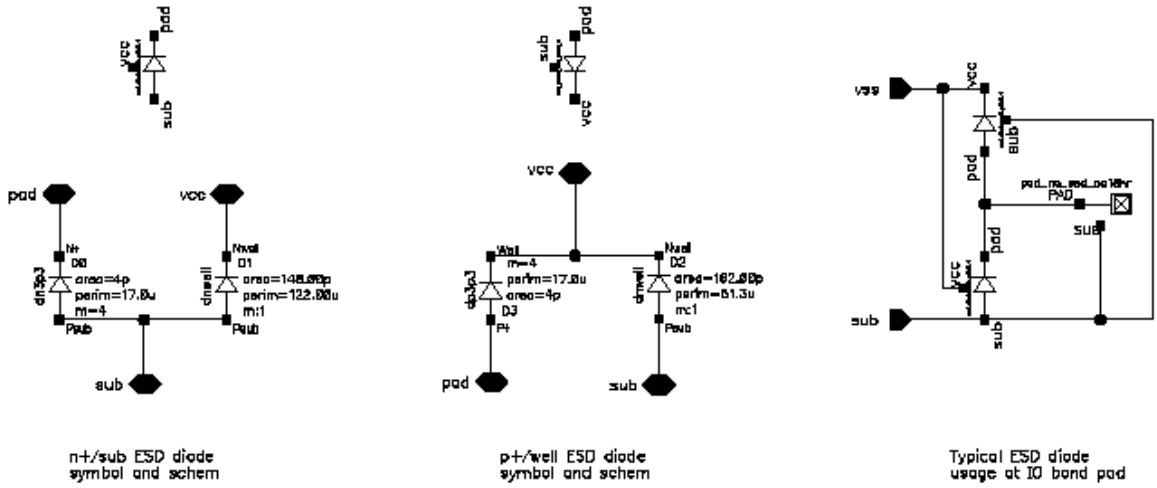
All standard ESD diodes are constructed from 3.3V MOS S/D junctions, which have a reverse breakdown of 8-10V. P+/nwell ESD diodes are intended for use between IO pins and supply, but can be used for all ESD diode applications, including series stacked applications to either extend IO pin voltage travel above supply or improve ESD protection for IO pins with limited voltage travel. N+/sub ESD diodes are only intended for connection between IO and ground, or possibly in-between grounds, because the anode is hard wired to the substrate. For the lowest parasitic IO pin capacitance and best RF characteristics, however, n+/sub diodes should be used between IO and ground. C0 values specified in the above table are 0V capacitances for the diode primary junction. Implicitly, the ESD circuit should be designed to avoid reverse ESD diode voltages > 8-10V.

ESD diodes are deliberately made “perimeter-intensive” to reduce capacitance while maintaining low series resistance. Their active junction areas are broken into multiple 0.5x8 um^2 fingers, and finger metallization is tapered along the stripe to enhance conduction of current to the ends, as shown below. ESD diodes are built with latch-up guard rings appropriate for their recommended use. This means that p+/nwell ESD diodes connected between IO and ground may benefit from an additional n-type guard ring (see the latch-up section for the recommended deployment of guard rings).



Simplified cross sections

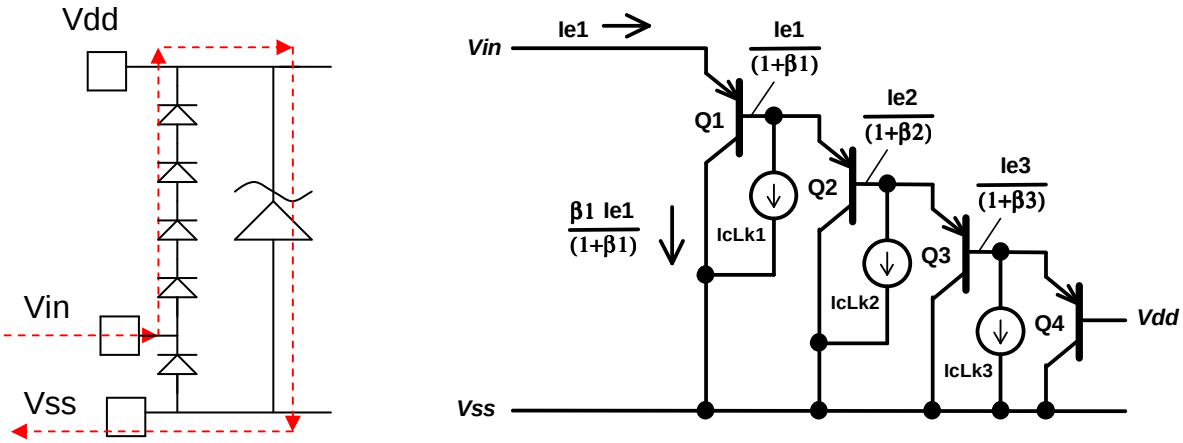
The layout and simplified cross sections of 4-fingered n+/sub and p+/nwell ESD diodes are shown above. Both devices are rated to survive 3KV HBM in the forward biased direction, and have a typical series resistance of 1 ohm under high current conditions. Their capacitances are on the order of 65fF at 0V dc bias. Their symbols, schematics and typical connection in an IO pad application are shown below.



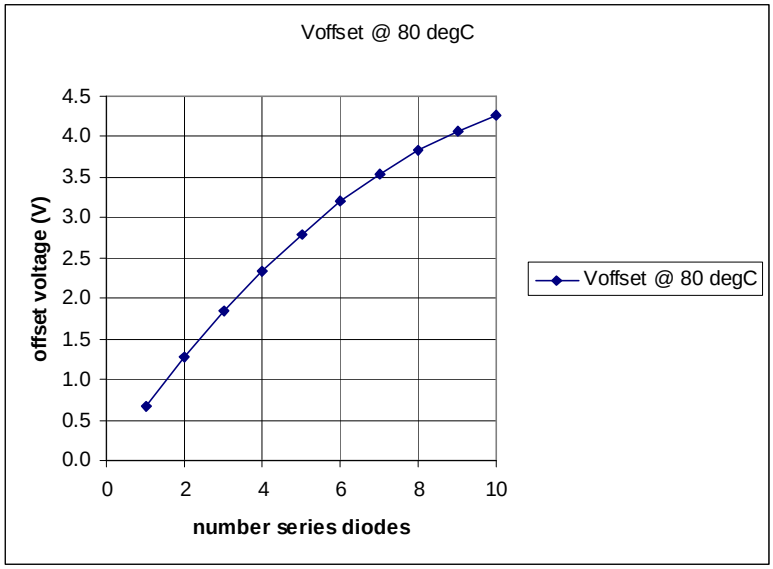
Stacking ESD diodes

Note that parasitic pnp behavior in the p+/nwell ESD diodes is not represented. If p+/nwell ESD diodes are stacked in series to create a desired amount of headroom, the stack size must account for the debiasing effects of the parasitic pnp transistors. It may be necessary to use standard pnp transistors to create the diode stack if accurate standby characteristics need to be simulated.

This is illustrated for the schematic below, which consists of a stack of four p+/nwell ESD diodes. The diagram on the right shows how some fraction of the anode current at each diode will be diverted into the substrate. The current gain of the pnp's is approximately 3 at room temperature. This means that only 1/4 of the anode current is passed to the next diode.



The plot on the next page shows the typical nonlinear stack voltage vs. number of 4-fingered ESD diodes behavior for fixed tail currents of 1u and 10u (ie1) at 100C.



Voltage developed across stack of forward biased 4-fingered ESD diodes as a function of number of diodes at 80C, for tail current of 10uA.

More generally, the voltage for a stack of m diodes in ca18 can be estimated as follows:

Vstring = A1 * m + A2 * m ^ 2 where …

$$A1 = \frac{kT}{q}\left\{ \ln\left[\frac{\beta}{(1+\beta)} * \frac{I\_in}{I\_co} \right] + 0.5 * \ln(1+\beta) \right\}$$

$$A2 = -\frac{kT}{q} * 0.5 * \ln(1+\beta)$$

I_in = standby head current per finger

I_eo = Ico / (1 + 1/β) (emitter current per finger)

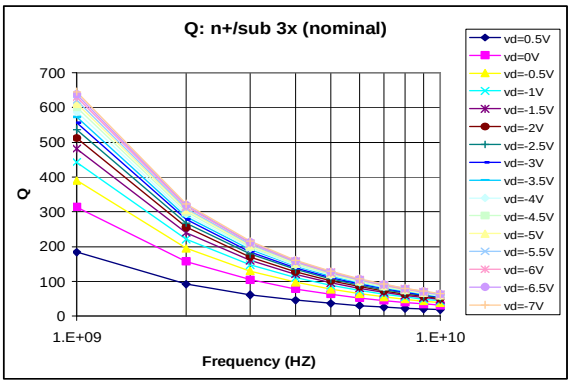
β ~ 0.0269 * T – 4.72 (current gain is relatively flat at low current densities)

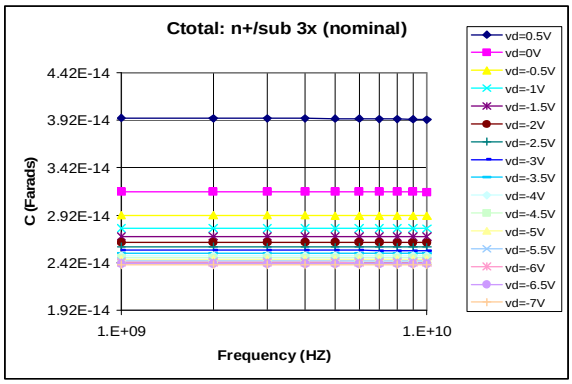
I_co = 683.2 * exp(-14506/T) (collector current per finger)

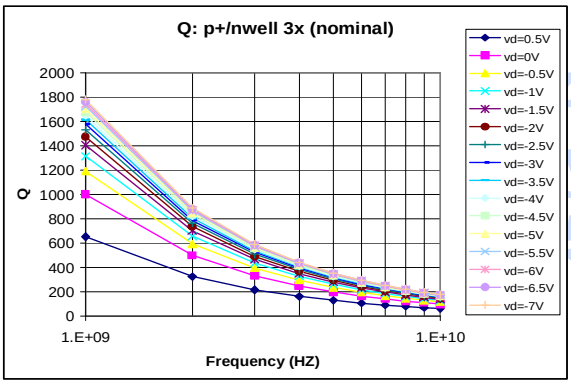
T is in Kelvin and kT/q = 0.0259 * T / 300

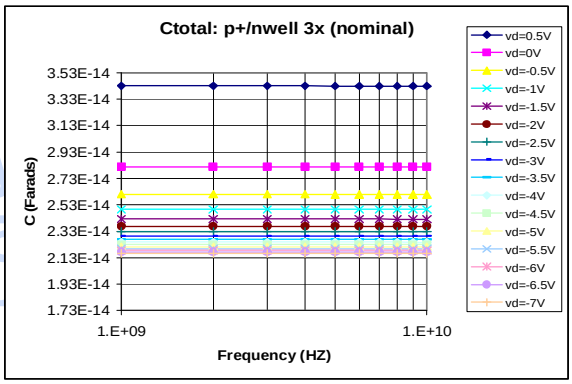
This is derived assuming IcLk = 0 for all stages in the above physical schematic and the fact that (0, 1, 3, 6 …) = m((m-1)/2

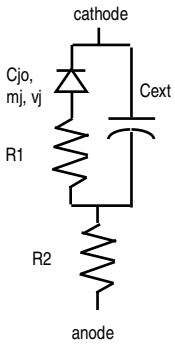
RF characteristics for the ESD diode primary junctions have been acquired and fitted to a lumped circuit model, but spice models are not yet available in the design kit. Typical single-ended Q and capacitance data for the primary junction of 3-fingered n+/sub and p+/nwell ESD diodes are shown below as a function of frequency between 1 and 10GHZ, and at reverse biases upto 7V. An averaged lumped circuit model topology together with typical parameters for all the standard diode geometries is given at the bottom of the page.







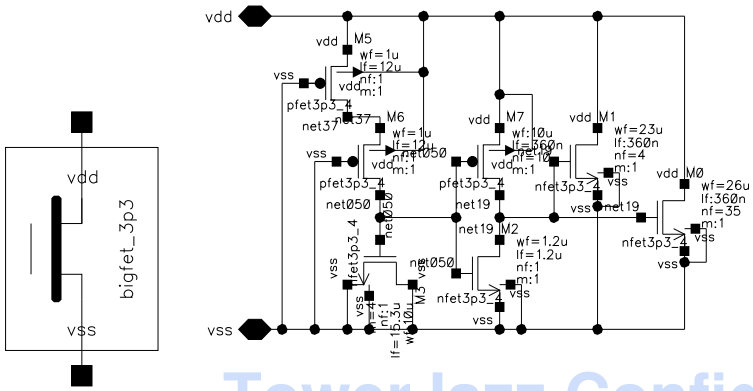




n+/sub	Cext	Cjo	mj	vj	R1	R2
NF	(femto-F)	(femto-F)			(ohms)	(ohms)
1	8.1307	3.3001	0.5292	0.7881	103.5610	42.4117
2	14.4139	7.1327	0.5292	0.7881	72.4565	16.1166
3	20.6971	10.9654	0.5292	0.7881	56.1313	9.2627
4	26.9803	14.7980	0.5292	0.7881	45.5425	6.1809
6	39.5467	22.4633	0.5292	0.7881	30.7616	3.9593
8	52.1131	30.1286	0.5292	0.7881	22.9212	3.0300
p+/nwell	Cext	Cjo	mj	vj	R1	R2
NF	(femto-F)	(femto-F)			(ohms)	(ohms)
1	6.8507	2.4638	0.5002	0.7985	29.3733	19.1346
2	12.6976	6.0455	0.5002	0.7985	20.5510	7.2712
3	18.5445	9.6272	0.5002	0.7985	15.5635	3.8230
4	24.3914	13.2089	0.5002	0.7985	12.9173	2.7886
6	36.0852	20.3724	0.5002	0.7985	8.7250	1.7863
8	47.7790	27.5358	0.5002	0.7985	6.5012	1.3670

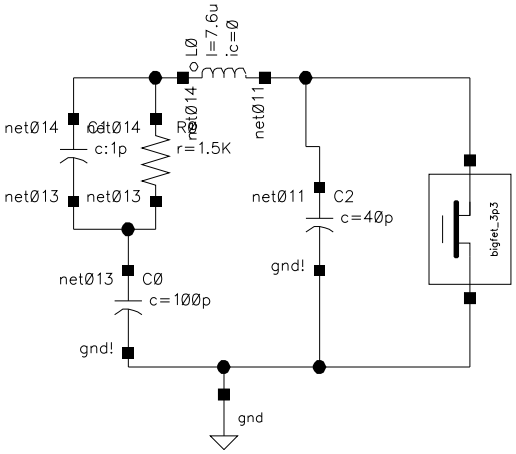
Characteristics of the bigfet_3p3 power supply clamp

The symbol and schematic for bigfet_3p3 are shown below. Under forward HBM stress, the cell behaves like a forward biased ESD diode and will have a pulsed IV characteristic consistent with a 1V battery with series resistance. Component values were designed to reduce cell series resistance while ensuring that the cell i) fully self-discharges after isolated positive-polarity HBM strikes, and ii) automatically de-latchs after ~ 10uS. Although experimental data is not yet available, the cell is based on a schematic design that is expected to be consistent with surviving 2KV HBM.

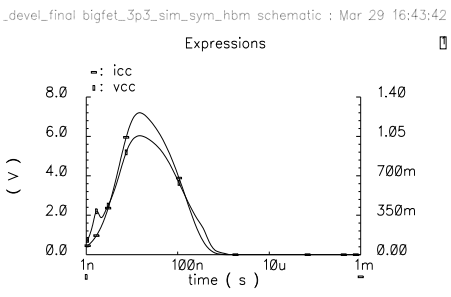


It's understood that SPICE simulations of bigFET responses to HBM strikes have good correspondence to actual laboratory TLP measurements provided the driver transistor is prevented from snapping back. Snapback can be avoided by designing the bigFET to itself clamp Vds below the snapback holding voltage of its NFET driver transistor (typically ~ 7V for a single isolated finger, but it can be lower in large arrays).

Below is the simulated cell response to a positive polarity 2KV HBM strike, where the HBM test voltage is set across C0 and all other node voltages are set to 0V at time t=0. The resulting peak cell voltage and current is Vcc=6.033V and Icc=1.26A, respectively. 1.26A is approximately the discharge current expected for a 2KV HBM event. It's clear that the Vcc rail is fully discharged after the ESD event expires (Vcc ~ 70mV @ 1uS).

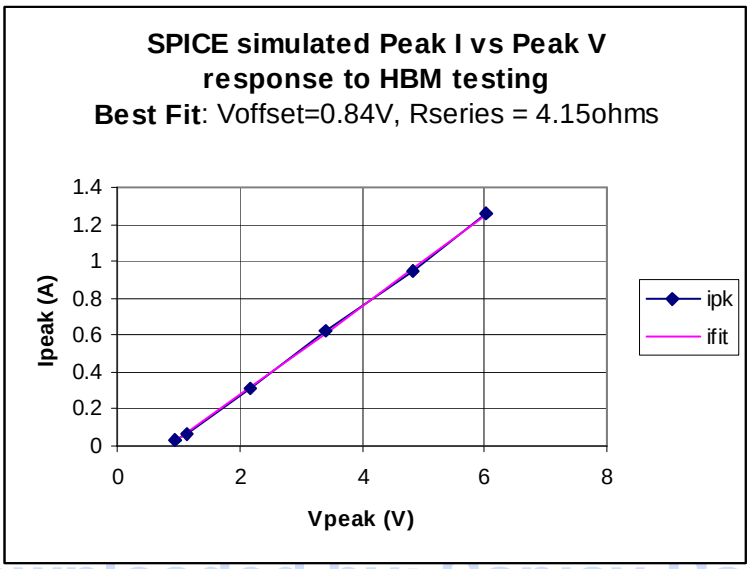


HBM test circuit for SPICE sim.



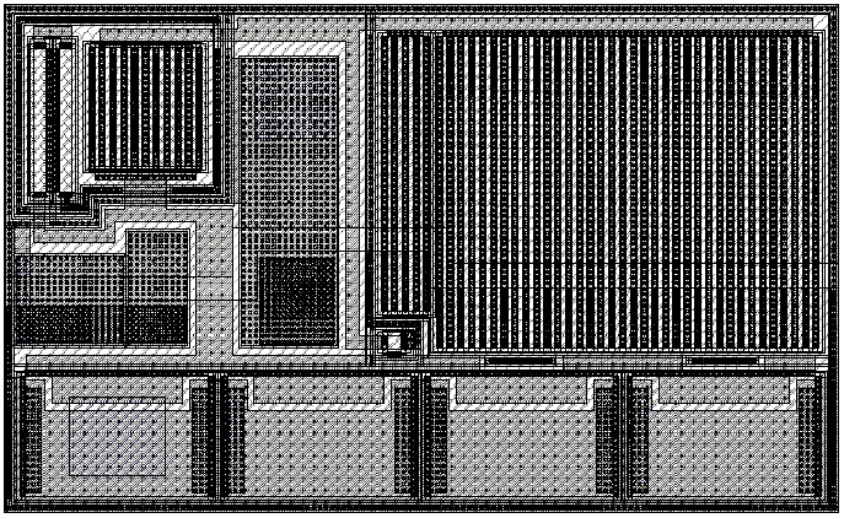
Cell Vcc and Icc vs. elapsed time

The SPICE-simulated cell peak current and voltage for an extended ESD testing range between 0 and 2KV HBM indicates that the cell offset voltage and series resistance for peak voltage and current is 0.84 V and 4.2 Ohms. 4.2 ohms is significantly lower than the value of 5.6 ohms associated with the original schematic, and should translate into better cell voltage clamping in response to HBM current.

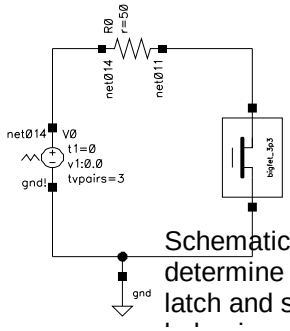


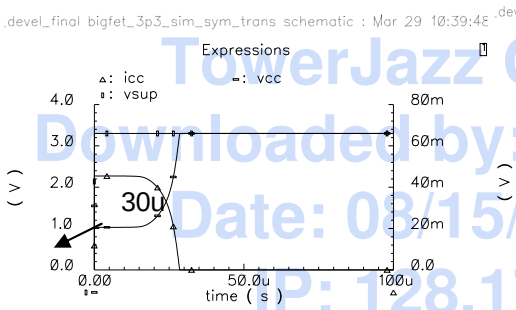
The bigfet_3p3 cell is compatible with 1.8V power domain rails, but the de-latch time for a 1nS Vcc ramp to 1.8V is 81uS instead of 30uS (for 3.3V). The latch current is smaller, around 20mA, and it may persist for as long as 750uS during a 1mS ramp. Note that the SPICE simulated dc standby current is < 1nA for both 3.3V and 1.8V operation.

The bigfet_3p3 cell layout (WxH = 69.78 x 42.52) is shown below. This cell uses positive layout factors defined on page 15 to survive snapback, instead of the traditional NWELL drain extension.

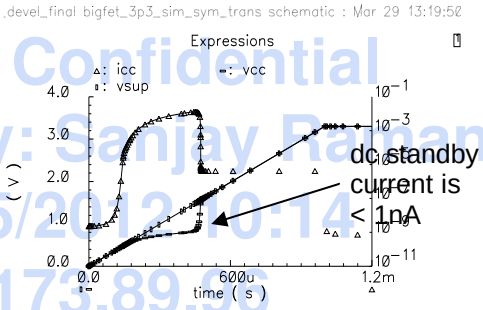


It's useful to examine the cell response to Vcc ramp thru a 50 ohm resistor, as shown below. For a 1nS ramp to 3.3V (top left, next page), the cell has a de-latch time of 30uS and a latched current of 45mA. This is comparable to the de-latch time and latched current for the schematic specified in the DRC document, and 30uS is long enough to fully discharge ESD events, but customers should determine whether this de-latch time interferes with normal product start-up. For a 1mS ramp to 3.3V (top right, next page), a similar 45mA persists for 500uS.

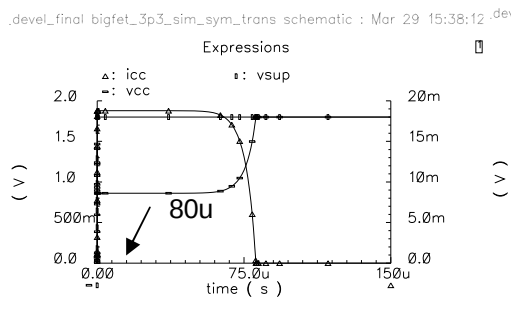




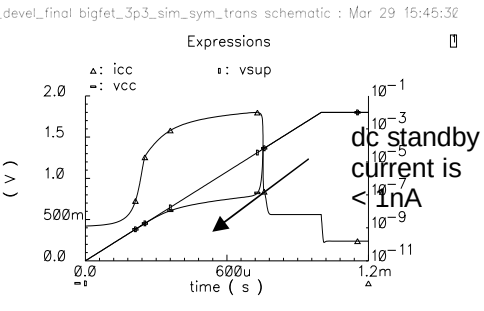
Latch response for 1nS ramp to 3.3V



Latch response for 1mS ramp to 3.3V



Latch response for 1nS ramp to 1.8V



Latch response for 1mS ramp to 1.8V

Characteristics of digital padring ESD protection devices

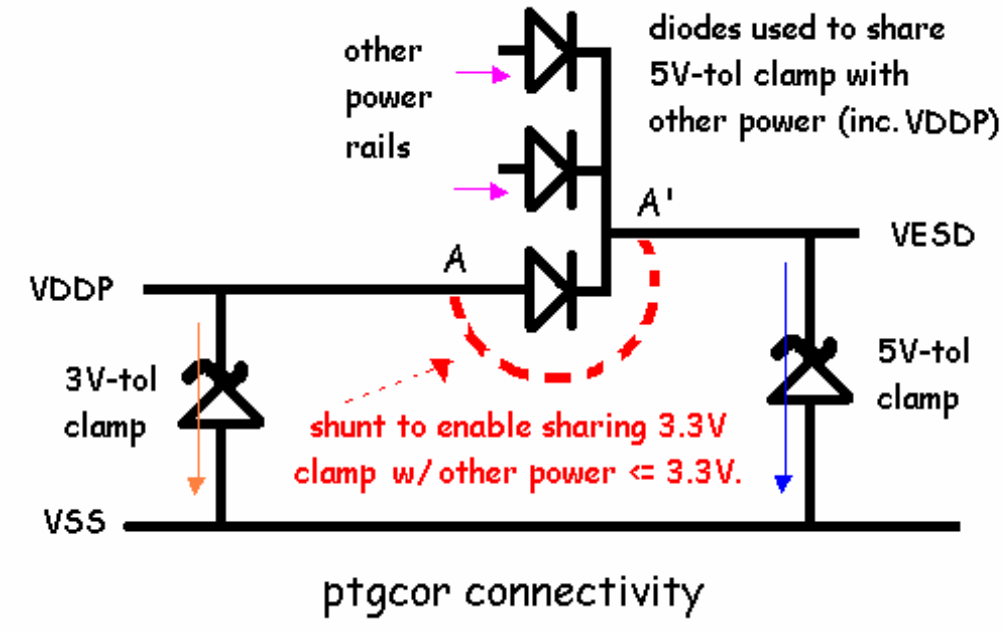
Digital padring cells are designed to form a rail-based ESD protection circuit when butted together along with power and corner cells. Each IO padcell has ESD diodes coupling the pad to the power domain rails (VGG, VDD or VDDP). These rails are coupled to the dedicated VESD bus thru ESD diodes.

Corner cells will contain a 3.3V tolerant clamp between VDDP and VSS, and a 5V tolerant clamp between VESD and VSS. Each pvdnpn power pad cell or pesd1 clamp cell will also contain a 3.3V tolerant power supply clamp coupling VDDP directly to VSS.

Ptgcor:

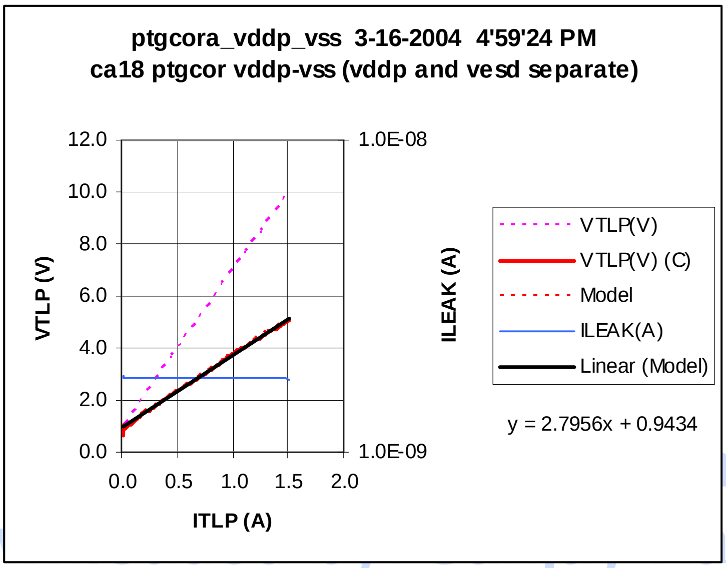
Corner cell **ptgcor** contains 3.3V and 5V tolerant clamps shunting power rails VDDP and VESD to VSS, respectively. These clamps enable positive polarity discharge currents to flow between power and ground. The capability of the 5V clamp is shared with all the other power rails via ESD diodes, as shown below.

The 5V clamp is inferior, however, to the 3.3V clamp. For products with maximum voltage of 3.3V, it's advisable to short VDDP and VESD together to share the superior 3.3V clamp capability with other power rails. (Note that since the 5V clamp relies on the voltage difference between VESD and VDDP to trigger, shorting VDDP to VESD effectively disables the 5V tolerant clamp)

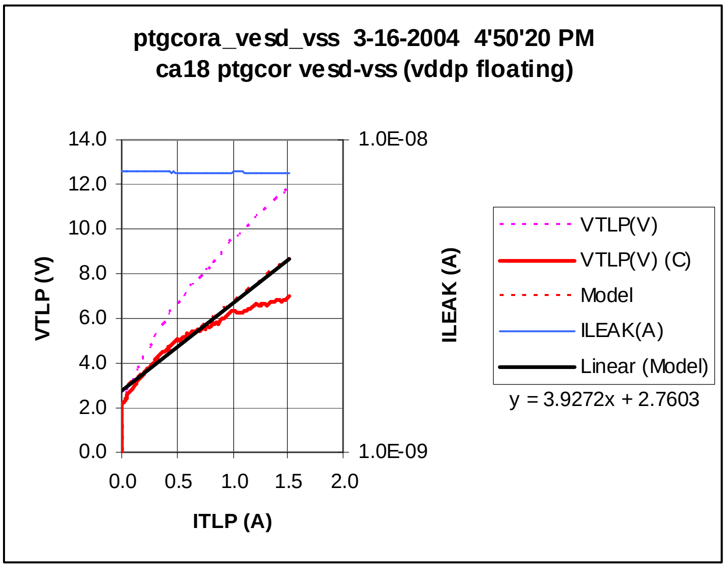


ptgcor connectivity

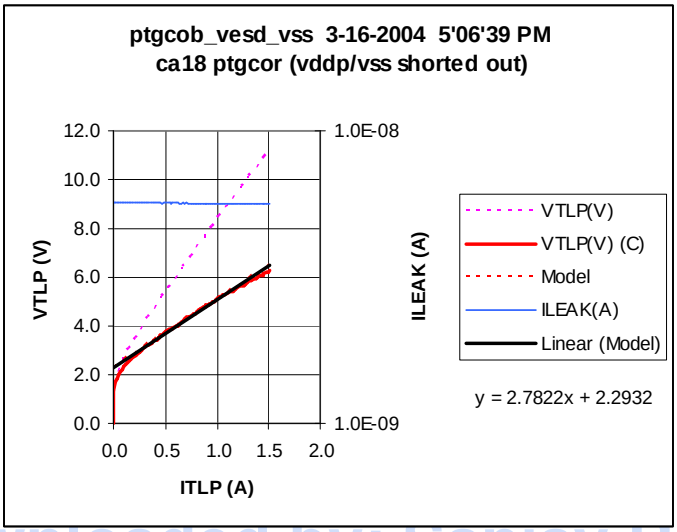
VDDP is the 3.3V rail used to bias IO circuitry. In ptgcor, it has its own capable 3.3V tolerant clamp to VSS. Measurements indicate that the 3.3V clamp offset voltage, series resistance, and a projected failure threshold are 0.9V, 2.8 ohms and > 1.5A TLP, respectively. (The cell standby leakage current as a function of TLP test current is unchanged by stress up to 1.5A TLP, which is thermally equivalent to 3KV HBM. Note that the data has been corrected (C) to de-embed ~ 3 ohms of external series resistance.)



VESD is an internal bus dedicated exclusively for carrying ESD current. The 5V tolerant clamp attached to VESD is shared with all other power domains thru forward biased ESD diodes. The circuit trigger is connected in part to VDDP. Although the cell is seen to still clamp 1.5A TLP to 6.5-7V with VDDP floating, its behavior is not clean an may indicate a problem with the measurement. One expected limitation of the cell, a tendency to not stay on for the full HBM strike and accumulate residual voltage, cannot be exposed TLP testing because TLP pulses are shorter than HBM pulses.

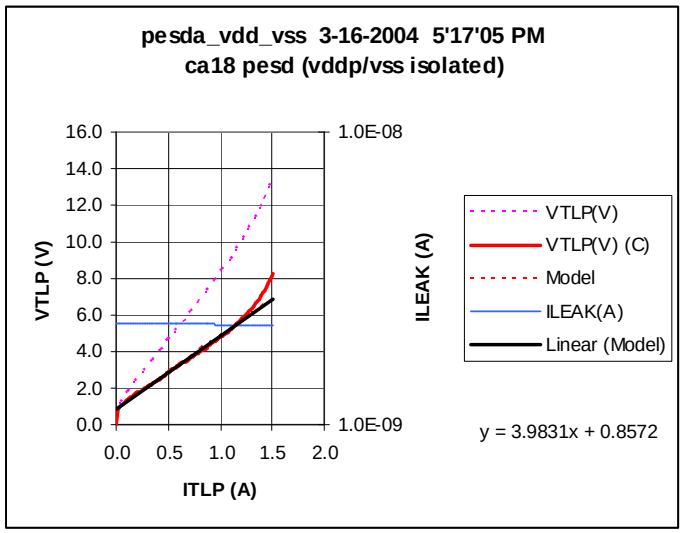


With VDDP shorted to VSS (simulating the effect of high VDDP supply capacitance), the 5V clamp is well behaved, with an offset voltage and series resistance of 2.3V and 2.8 ohms. The offset voltage is about 1.3V higher than in the 3.3V clamp. Similar to the 3.3V clamp on VDDP, the cell has a failure threshold greater than 1.5A TLP, which is thermally equivalent to 3KV HBM. This data suggests that the 5V clamp is better able to respond to HBM strikes on VESD if there is some kind of loading on the VDDP supply line.

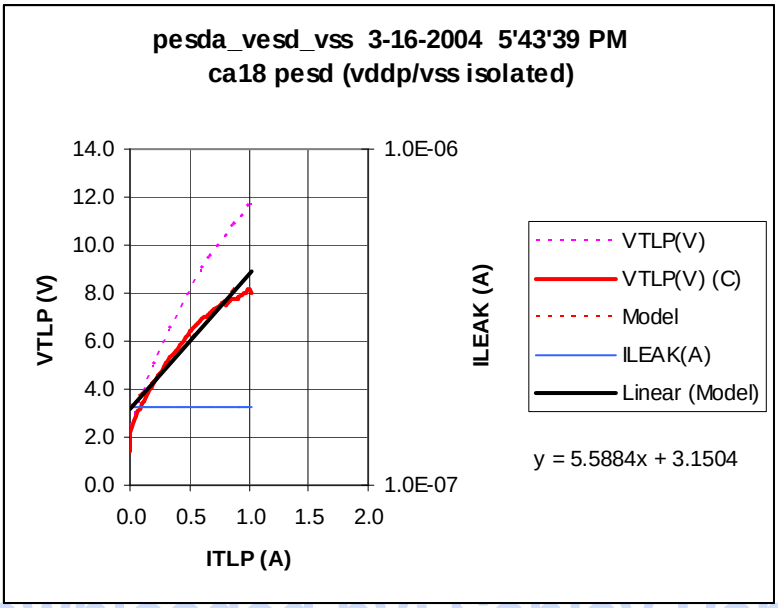


pesd:

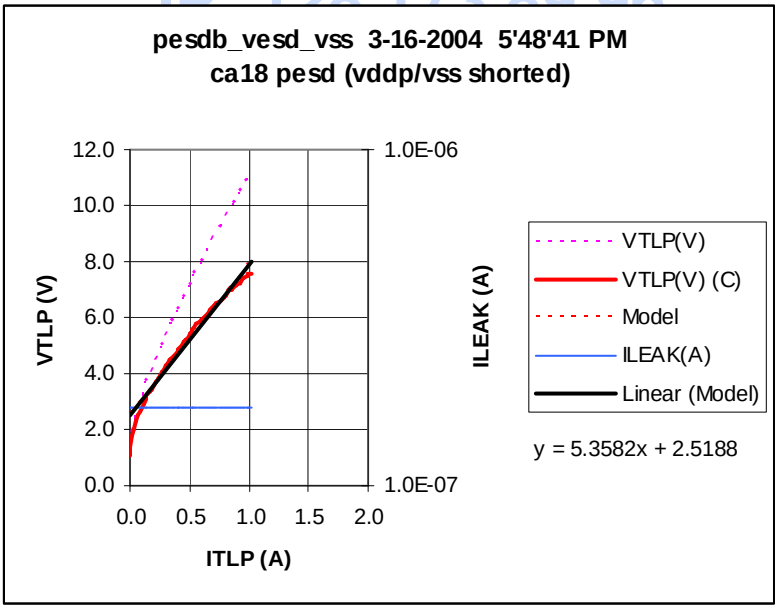
Non-corner cell **pesd** contains both 3.3V and 5V tolerant clamps on VDDP and VESD, although SPICE simulations indicate that the cell is not fully self-discharging and may not be capable of handling successive HBM ESD events alone. The measurements below indicate that the 3.3V clamp on VDDP is well behaved, at least for TLP strikes, with a offset voltage and series resistance of 0.9V and 4 ohms. No failure is found upto 1.5A TLP, which is thermally equivalent to 3KV HBM.



As in the corner cell, the 5V clamp on VESD is not triggered cleanly if VDDP is floating. Its offset voltage and series resistance is extracted as 3.2V and 5.6 ohms, but it's possible that the actual peak voltage is different from what is reported by the TLP machine, which determines voltage only at the trailing edge of TLP pulses.

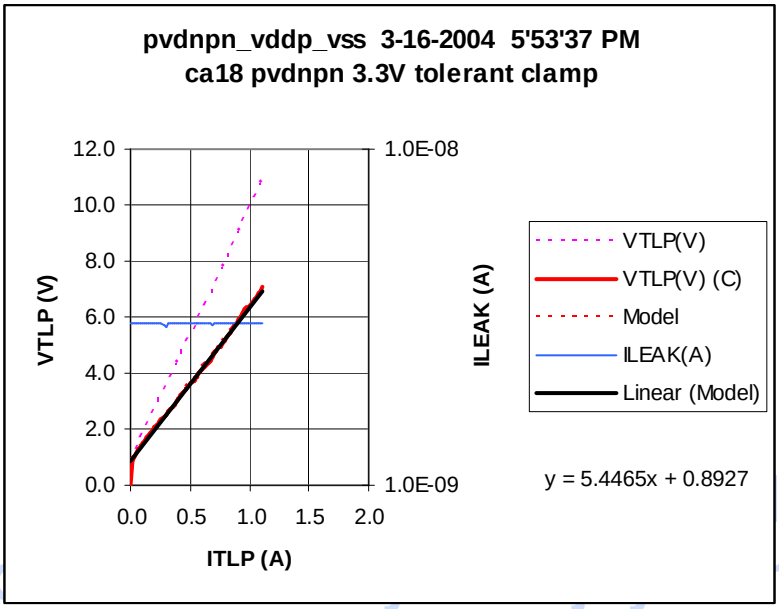


With VDDP shorted to VSS, the 5V tolerant clamp on VESD in pesd has a better behaved response to TLP current characterized by an offset voltage and series resistance of 2.5V and 5.4 ohms.



pvdnpn:

Non-corner cell **pvdnpn** contains 3.3V tolerant clamp on VDDP. The cell has a well defined response to TLP current characterized by an offset voltage and series resistance of 0.9V and 5.5 ohms.



Summary of digital IO pad ring ESD clamps

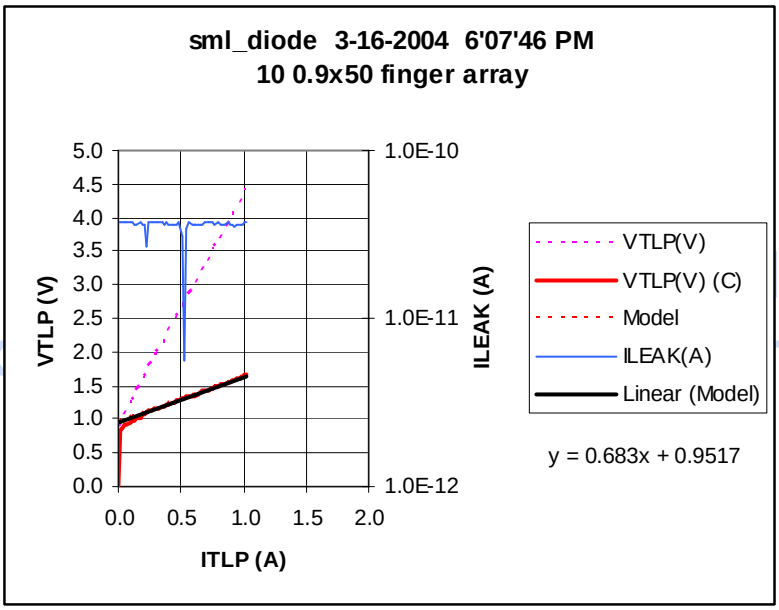
Cell / clamp	Condition	Stress w/r to VSS	Voffset	Rseries	VHBM	V_1A
ptgcor / 3.3V	-	VDDP	1	3	> 2KV	4
ptgcor / 5.0V	VDDP float *	VESD	2.8	4	> 2KV	6.8
ptgcor / 5.0V	VDDP-VSS	VESD	2.3	3	> 2KV	5.3
pesd / 3.3V	-	VDDP	1	4	> 2KV	5
pesd / 5.0V	VDDP float *	VESD	3.2	5.6	> 2KV	8.8
pesd / 5.0V	VDDP-VSS	VESD	2.5	5.4	> 2KV	7.9
pvdnpn / 3.3V	-	VDDP	1	5.5	> 2KV	6.5

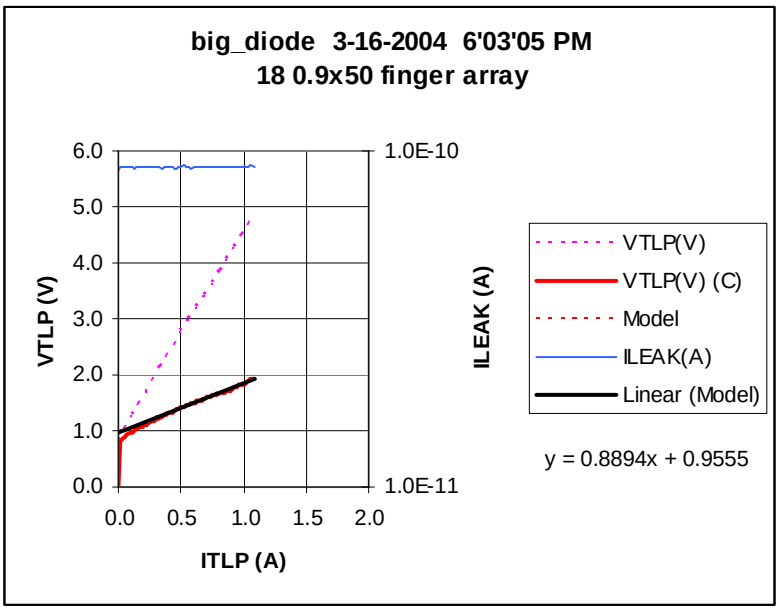
* Data acquired by the TLP machine is not well behaved, which may indicate that the cell as configured does not trigger cleanly or there is a problem with the measurement.

Digital IO cell ESD protection diodes

ESD diodes in digital pad ring cells are laid out in fingers with an 0.9x50 active geometry for the primary junction. It's not expected that the diode series resistance for an arbitrary device scale with number of parallel fingers because the forward ESD current carried by the diode is probably not uniformly distributed (not all fingers of a diode will turn on simultaneously).

Series resistance in p+/nwell ESD diodes with 10 and 18 parallel fingers is actually found to slightly increase with more fingers, from 0.68 ohms to 0.9 ohms. This suggests that series resistance could be on average 0.8 ohms for this style and size of ESD diode, regardless of specific number of fingers in parallel. ESD diode failure was not detected upto 1A TLP, which is thermally equivalent to 2KV HBM.

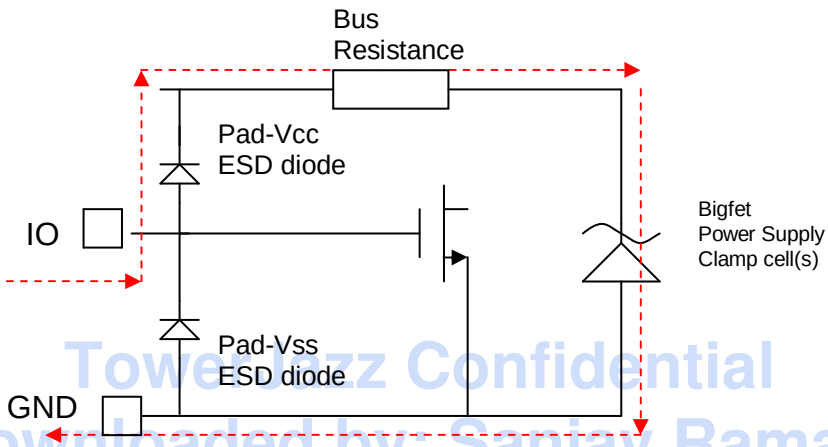




Practical design examples for sizing ESD circuitry

Example 1: Gate Oxide protection

Suppose the goal is to protect 1.8V and 3.3V gate oxides from failure under positive polarity 2KV HBM strikes between IO and ground. If the recommended ESD protection circuit is used, the intended discharge path should consist of the forward biased IO-supply ESD diode, bus resistance and the bigFET clamp. The total pin current for 2KV is approximately 2KV/1500 ohms = 1.3A.



Allowing for a multiplicity of M clamps in parallel, the voltage developed across the oxide is

V_IO-GND = (1 + 1.3 * Rdiode) + 1.3 * Rbus + (1 + 1.3 * Rbigfet / M)

If a 4 fingered ESD diode were used (to ensure that the diode itself would survive 2KV HBM with margin), data from the table of standard devices suggests that

V_IO-GND = (1 + 1.3 * 0.6) + 1.3 * Rbus + (1 + 1.3 * 4 / M)

If the input were a 1.8V MOS transistor, with a failure voltage projected at 10V,

V_IO-GND = 10 > (1 + 1.3 * 0.6) + 1.3 * Rbus + (1 + 1.3 * 4 / M)

With a single bigFET_3p3 (M=1), the total bus resistance would have to be less than 1.5 ohms. Using two bigFEt_3p3 cells in parallel (M=2) would relax the requirement to 3.5 ohms.

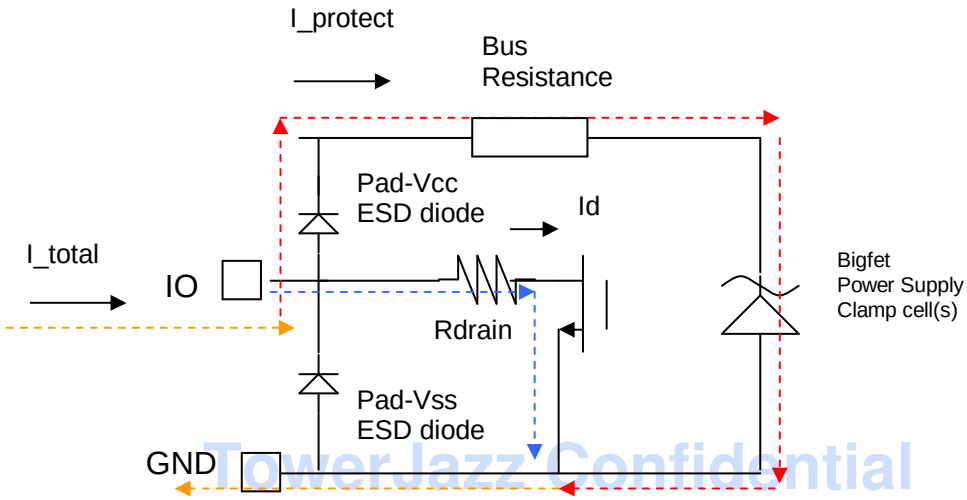
If the input were a 3.3V MOS transistor, with a failure voltage projected at > 16V,

V_IO-GND = 16 > (1 + 1.3 * 0.6) + 1.3 * Rbus + (1 + 1.3 * 4 / M)

With a single bigFET_3p3 (M=1), the total bus resistance would have to be less than 6 ohms. Using two bigFEt_3p3 cells in parallel (M=2) would relax the requirement to 8 ohms.

Example 2: NMOS output protection

Suppose the goal is to protect 1.8V and 3.3V NMOS open-drain outputs from failure under positive polarity 2KV HBM strikes between IO and ground. Again, if the recommended ESD protection circuit is used, the intended discharge path should consist of the forward biased IO-supply ESD diode, bus resistance and the bigFET clamp. However, part of the total current may flow into the drain, as shown below.



Historically, nmos open drains are recommended to use an integrated nwell extension, which is supposed to elevate the transistor Vds failure voltage to > 12-13V and block significant current from entering the transistor (Id=0). Typical data for 1.8V/3.3V NMOS indicates that the Vds failure voltage can be as high as 18V. Using the same ESD diodes as in the previous example, and a clamp multiplicity M = 1,

V_IO-GND = 18V > (1 + 1.3 * 0.6) + 1.3 * Rbus + (1 + 1.3 * 4 / 1)

can be satisfied with Rbus as high as 7.5 ohms.

It's found, however, that the nwell extension doesn't always work for 3.3V NMOS transistors (if the body tie-down is close) and such devices are expected to fail at Vds values as low as 7V with Id=0 (see table of simplified failure thresholds). In this case, the requirement on the protection circuit is

V_IO-GND = 7V > (1 + 1.3 * 0.6) + 1.3 * Rbus + (1 + 1.3 * 4 / M).

This is satisfied by M=2 and Rbus = 1.2 ohms, for example. Rbus could be 1.9 ohms if M=3.

A single finger 1.8V NMOS output transistor may fail at Vds voltages as low as 4-5V, according to the typical measurements. The requirement that

V_IO-GND = 4V < (1 + 1.3 * 0.6) + 1.3 * Rbus + (1 + 1.3 * 4 / M).

is difficult to satisfy without m>4, which may seem like an awkward solution. It may be more elegant to use the nwell drain extension, or exploit the finite drain failure currents seen in 1.8V NMOS.

The table of simplified failure thresholds indicates that a 1.8V NFET array may have a drain failure current density of approximately 3mA/um (possibly higher if positive layout factors are used). Device Vds failure is expected at approximately 6V.

A 200um wide transistor would be estimated to have a failure current of 600mA, which could be used together with an external resistor (Rdrain) to elevate the IO-gnd voltage at which the transistor failed. In this case, the relevant equations would be

V_IO-GND = (1 + I_protect * 0.6) + I_protect * Rbus + (1 + I_protect * 4 / M)

V_IO-GND = 6V + Id * Rdrain.

At the point of NFET failure, I_protect would be only 1.3A – 600mA = 700mA at 2KV HBM, and

V_IO-GND = (1 + 0.7 A * 0.6 ohms) + 0.7 A * Rbus + (1 +0.7 A * 4 ohms / M)

V_IO-GND = 6V + 0.6 A * Rdrain.

Here, it's seen that the benefit of assuming Id<>0 and using a series drain resistor is that the critical pad-pad voltage can be higher, and some of the total pin current is sunk by the signal path.

If a 10 ohm resistor could be used for Rdrain, V_IO-GND would be elevated to 12V at the point of transistor failure, and with M=1and I_protect reduced to 700mA, Rbus could be as high as 9.6 ohms.

Given the sensitivity of drain failure current to various layout factors, however, it may make sense to use conservative assumptions for the calculation, such as I_protect = 1.3A regardless of the value of Id, or assuming Id will be < 3mA/um width. With I_protect = 1.3A and Id = 300mA, V_IO-GND with Rdrain = 10 ohms is expected to be only 9V at the point of transistor failure, and Rbus with m=2 would have to be less than 2.7 ohms.