Jazz Digital I/O Usage Guidelines

Rev. 2.0
Doc Number: NPB PS-0696

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1 Revision History

Date	Rev	Author	Purpose
04/15/05	1.0	Felix Tom	• Initial release
05/05/06	2.0	Felix Tom	• Fixed a typo in section 3.2, I/O Supply Connection ("p" was replaced by "o")

2 Definitions

2.1 Single-voltage

System has a single low-voltage VDD for all devices (e.g., 3V-only, no 5V-tolerance).

2.2 5V-tolerant

System has a mix of low-voltage and high-voltage parts (e.g., both 3V and 5V devices).

5V-tolerant parts use TTL levels for communicating with 5V devices, which also meet CMOS levels when communicating with other 3V devices. The TTL interface requires a 3.0V minimum VDD (not 2.7V). The CMOS interface may be extended to 2.7V.

5V-tolerant outputs will withstand 5V applied only when the pad is in its high-impedance state. This prohibits using an external pull-up resistor to pull a 3V output up to 5V (the 5V would be applied even when the output is in its driving state). Under some conditions a high value resistor may be used to pull the output up to 5V in the high-impedance state. The resistor value must be high enough and the VDD supply sinking capability must be such that the pad voltage does not significantly exceed VDD when the output is driving. This restriction does not apply to input-only pads.

The current implementation of 5V-tolerant pull-up resistors will provide a logic-high for otherwise undriven pads, but will not provide a reliable logic-high to other system devices (output level would be VDD minus NFET threshold voltage).

2.3 Level-shifted

Core-to-padring and padring-to-core level shifters allow operation of the chip core and I/O at different voltages (I/O may be either single-voltage or 5V-tolerant).

NOTE: This does not refer to the "TTL-to-CMOS level shifter" that is the chip input receiver.

2.4 Core Supply (VDD)

Primary supply used to power the chip core.

2.5 Pad Ring Supply (VDDP)

Supply used to power the pad ring circuitry except for output buffers (i.e., output buffer predrivers and input receivers).

2.6 I/O Supply (VDDO)

Supply used to power the final NFETs or PFETs of the output buffers.

2.7 5V Clamp Bus (VGG)

VGG is the supply to which 5V-tolerant pads are diode-clamped. ***It is highly recommended that VGG be connected to an external power supply.*** If VGG is left floating, it will be charged up thru signal ESD diodes and will not provide overshoot clamping, increasing the latch-up risk. Pad pvgnnn is used to connect to VGG (the ESD bus). Other pvg--- pads short VGG to one or more of the VDD/VDDP/VDDO power supplies and may only be used in single-voltage systems.

2.8 ESD Bus (VESD)

Internal bus with ESD clamp circuits and CDM capacitors, diode-connected to all other VDD/VDDP/VDDO/VGG power-supply pads. VESD will be charged to within a diode-drop of the highest potential power supply. VESD is not connected externally and must be continuous thru all pads to ensure proper ESD clamping.

2.9 Core and Pad Ring Ground (VSS)

Ground return for the chip core and the pad ring circuitry.

2.10 I/O Ground (VSSO)

Ground return for the output buffers.

2.11 Output Drive

Output drive is specified as the maximum AC impedance determined by matching an ideal, unterminated transmission line. For reference, an approximate DC drive strength in mA is also given. The maximum DC drive is dependent on the output level and amount of margin desired. The margin is 200mV for 5V-tolerant pads, TTL interface, VDD = 3.0V, T_j = 120°C.

The drive ratings are also affected by the number of simultaneously switching outputs (SSO's) per power supply pad, and by the distance between the pads. The pad ratings use a different number of SSO's for each drive strength, with a maximum space of one pad width between SSO's: 32Ω - 4 SSO's; 50Ω - 6 SSO's; 80Ω - 8 SSO's; 120Ω - 12 SSO's.

NOTE: The SSO effect on drive strength ratings is based on resistance, not inductance. Supply inductance varies significantly for different packages.

3 I/O Pad Names

A list of pads included in each particular library can be found in the …/doc directory of the library installation.

3.1 Signal Pads

Signal pad names have the form p12345 (with a few exceptions), where the meaning of the positional characters follows the convention described below.

1 – Interface Type

c = Single-voltage
d = Single-voltage, level-shifted
t = 5V-tolerant
l = 5V-tolerant, level-shifted

2 – Pad Function

b = Bidirectional
t = Tri-state output
d = Input
o = 2-state output
c = Clock
x = Crystal oscillator

3 – Pad Function Options (does not apply to special pads, e.g., crystal oscillator)

0 = Non-inverting with CMOS or TTL/CMOS input receiver
1 = Non-inverting with CMOS Schmitt-trigger input receiver

4 – Output Drive (does not apply to special pads, e.g., crystal oscillator)

0 = None (input only)
1 = 120Ω, 2mA
2 = 80Ω, 4mA
3 = 50Ω, 8mA
4 = 32Ω, 12mA

5 – Pad Options

n = None
u = 75kΩ pull-up
d = 75kΩ pull-down
r = 75kΩ repeater (bus-keeper)

Exceptions to the above naming convention include corner, ESD clamp, and filler cells.

3.2 Power Pads

Power pad names have the form pv1234, where the meaning of the positional characters follows the convention described below.

1 – Supply Level Connected to Pad

d = Power (VDD, VDDO, and/or VDDP)
g = Power (VGG)
s = Ground (VSS and/or VSSO)
bd = Break power
bb = Break power and ground
bs = Break ground

2 – Core Supply Connection

c = Core supply is connected to pad (or is broken)
n = Core supply is not connect to pad (or is not broken)

3 – Pad ring Supply Connection

p = Pad ring supply is connected to pad (or is broken)
n = Pad ring supply is not connected to pad (or is not broken)

4 – I/O Supply Connection

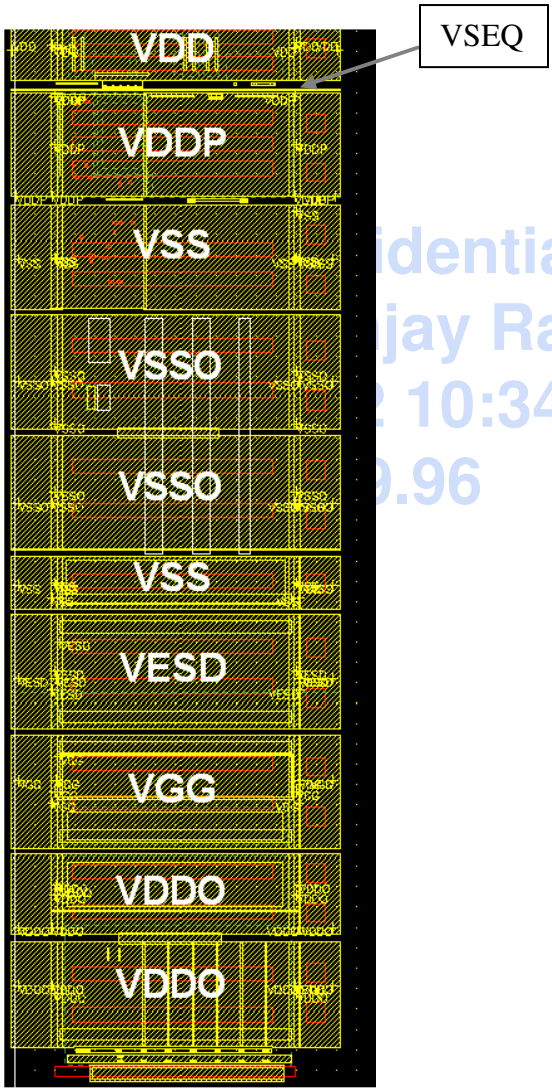
o = I/O supply is connected to pad (or is broken)
n = I/O supply is not connected to pad (or is not broken)

4 I/O Pad Usage

Jazz I/O pads are designed to be used in a contiguous pad ring with the supplied corner cells. ESD protection circuits are included in individual pads and work in conjunction with the corner cells, which contain large diodes.

All pads have 8-11 horizontal metal busses that abut together to form the various power, ground, and ESD rings. There can be up to 8 nets which are named VDD, VDDO, VDDP, VGG, VSS, VSSO, VESD (internal net), and VSEQ (internal net, A18 libraries only). Many of these can be shorted in the pad ring using various power pads supplied in the library, reducing the number of electrical nets. In the simplest case, three power supply connections will be needed: core power, I/O power, and a common ground.

The figure below shows an example of the physical stacking of the different busses.



4.1 Pad Ring Construction

After all the functional I/O pads have been selected a number of power pads, 4 corner cells, and one power-up sequencing pad (if present in the library) need to be added. Refer to page 9 for more information on power-up sequencing.

There are a number of power pads to choose from depending on which supplies need to be kept separate or can be shorted together. If the chip core and I/O operate at different voltages, then 3 supply nets – VDD, VDDO, and VSS – will be required at a minimum. These can be supplied using the following pads:

pvdcnn – VDD
pvdnpo – VDDO (shorted to VDDP)
pvscno – VSS (shorted to VSSO)
pvscnns/pvscnnu – VSS with power-sequencing protection enabled/disabled (if present in the library, one or the other pad ***must*** be used)

For maximum latch-up and ESD protection, at least one pvgnnn pad should be added to connect VGG to 5V. For a 3V-only system, the pvgnpo pad could be used instead of separate pvdnpo and pvgnnn pads.

In other configurations, VDDO and VDDP could be separated by using pvdnno and pvdnpn pads instead of pvdnpo. Separate core and I/O grounds could also be maintained by using pvscnn and pvsnno pads instead of pvscno. And multiple core power domains could be implemented by using pvbdcnn pads to keep them from shorting to each other.

4.2 Pad Location and Power Requirements

Calculations must be performed to determine (1) how many power/ground pads are required and (2) where to place these pads within the ring. There are two factors that must be taken into account when making these calculations: the power requirements of the core and the number of simultaneously switching outputs (SSO's).

Based on the power requirements of the core and the electromigration limits for each power pad, the number of VDD and VSS pads required can be found. Electromigration limits of the power rings will determine the maximum spacing between these pads.

There are two conditions that the pad ring needs to meet with regard to SSO's:

1. the total number of power/ground pads required for expected SSO activity, and

2. the maximum distance between SSO's and power pads.

For the first condition, once the total number and type of bidirectional and output pads is known, the total switching current requirements of the chip can be calculated. Since all outputs will not switch simultaneously, the total current requirement can usually be reduced by a factor of 2-6 depending on the expected number of SSO's. Dividing this re-

duced current by the electromigration limits of each power or ground pad yields the total number of pads required.

For the second condition the amount of current that can be carried between output and power pads needs to be determined. This limitation comes from the electromigration limits of the power busses (VDDP, VDDO, VGG for power and VSSO for ground) in the pad ring. Dividing this by the current requirements of each output/bidirectional pad in the ring yields the maximum number of pads that can be placed between power/ground pads.

Usually, satisfying the first condition causes the second condition to be satisfied as well. This is illustrated in the example below.

For condition #1, assume there are 516 bidirectionals rated at 12mA each for a total of 6,192mA. Further assume that only 25% of the outputs will ever switch simultaneously, so the maximum current requirement is 1,548mA. To handle that much current and if each power pad is limited to 19.5mA, then 1548/19.5 ≈ 80 pads will be needed. An additional 10 pads could be added to margin the design, resulting in a total requirement of 90 pads. Of course, the assumption is that the power pads will be evenly spread amongst the bidirectionals as required by condition #2. A few extra pads could be added for powering inputs as well.

For condition #2, if the amount of current that can be carried between output and power pads is limited to 263mA for power and 156mA for ground, then the maximum number of SSO's without a power pad in between is the smaller of 263/12 ≈ 22 pads or 156/12 = 13 pads.

Combining the 2 conditions and assuming that there are 650 non-power/ground pads on the chip, there can be approximately 650/90 = 7.2 signal pads between each power and each ground pad. Since 7.2 < 13, meeting condition #1 also meets condition #2.

5 Power-up Sequencing

Power-up sequencing refers to the order in which the I/O and core supplies are powered up, and the period of time between powering up each of these supplies.

When the I/O supply (VDDP/VDDO) is powered up first, the output drivers can be in an indeterminate state until the core supply (VDD) is powered up. If the delay in the power sequence is long enough (several milliseconds), the unknown state of the output drivers could cause system problems.

The A18 and A25L libraries include a signal (VSEQ) in the power bussing inside the pad ring to control power sequencing protection. This signal is automatically routed by pad/filler cell abutment similar to VDDO, VSSO, etc., and is connected to the level-shifter circuit of all output drivers to control the output enable. The source of the VSEQ signal is located in two core VSS pads, pvscnnu and pvscnns. If power sequencing protection is not desired, pvscnnu will pull VSEQ up to VDDP and the output drivers will not be affected. If power sequencing protection is desired, pvscnns will disable the output drivers when the I/O supply is detected and release them when the core supply is detected.

Regardless of whether pvscnnu or pvscnns is used, the recommended power-up sequence is:

5.0V (VGG)
3.3V (VDDP & VDDO)
1.8V (VDD)

The advantage of using pvscnns is that it ensures that the output drivers will be tri-stated when I/O power first comes up and releases the tri-state when core power is eventually brought up. The disadvantage of using pvscnns is that there is a constant static current of about 8uA maximum.