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TITLE:

Design Application Note for Efuses in 0.18um TowerJazz Newport Beach Processes

REV	REVISION DESCRIPTION	DATE	TDR #
01	Initial Release in QSI	02/02/2011	
02	Add 5v programming capability	08/05/2011	
	Add Reliability summaries		

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1. Purpose and Scope

This document defines the design rules and electrical specifications for implementing Efuse (poly fuses) into designs for the process families CA18 and SBC18 in bulk silicon or on epi silicon. It does not apply to SOI processes.

The Efuse cell described here has a fixed design. Circuits must not be deviated from the 1) Jazz gds provided for the Efuse cell or 2) this document spec. The Efuse is poly made over STI and uses P+ doped Cobalt silicided poly. No special masks or added process steps are needed for implementation.

The Efuse element has a length of 2um and width of 0.2um (10squares). Our characterization showed, for large database of ~50,000 fuses, that the initial resistance (Rinit) of the fuse is about 56 Ohms. After programming (burning), 99.997% of the fuses showed final resistance (Rprog) increased to over 5000 ohms, the lower spec limit. The spec limit of the post program fail rate is 100ppm.

2. Applicable Documents

CA18 Electrical Specification	NPB-PS-0173
CA18 Design Rules	NPB-PS-0176
CA18 Design Manual	NPB-PS-0417
CA18 Analog Characterization Report	NPB-PS-0281
CA18 ESD Design Manual	NPB-PS-0417
CA18 Design Application Note on HV design	NPB-PS-0711
SBC18 Electrical Specification	NPB-PS-0267
SBC18 Design Rules	NPB-PS-0179

3. Mask Set

3.1 Reticle Layers (Per Process Sequence)

No added reticle layers or exposures are needed to implement the Efuse.

3.2 Assigned Layer Numbers for Efuse Cell

Layer No.	Layer Name	Cadence Layer Name	Abbr	Type
Layer 118 DT 51	*MRKLYR EFUSE	mrklyr efuse		

- This layer must also be drawn over the Efuse cells.
- The mrklyr efuse is used for DRC checking and during the mask layer generation by maskcad.

3.3 GDS file of Efuse Pcell

GDS file for 0.18um Newport technologies is: **Efuse_Pcell_0p18.gds**.
File will be provided with Efuse kit for 0.18um technologies.

4. Design Rules for the Efuse implementation

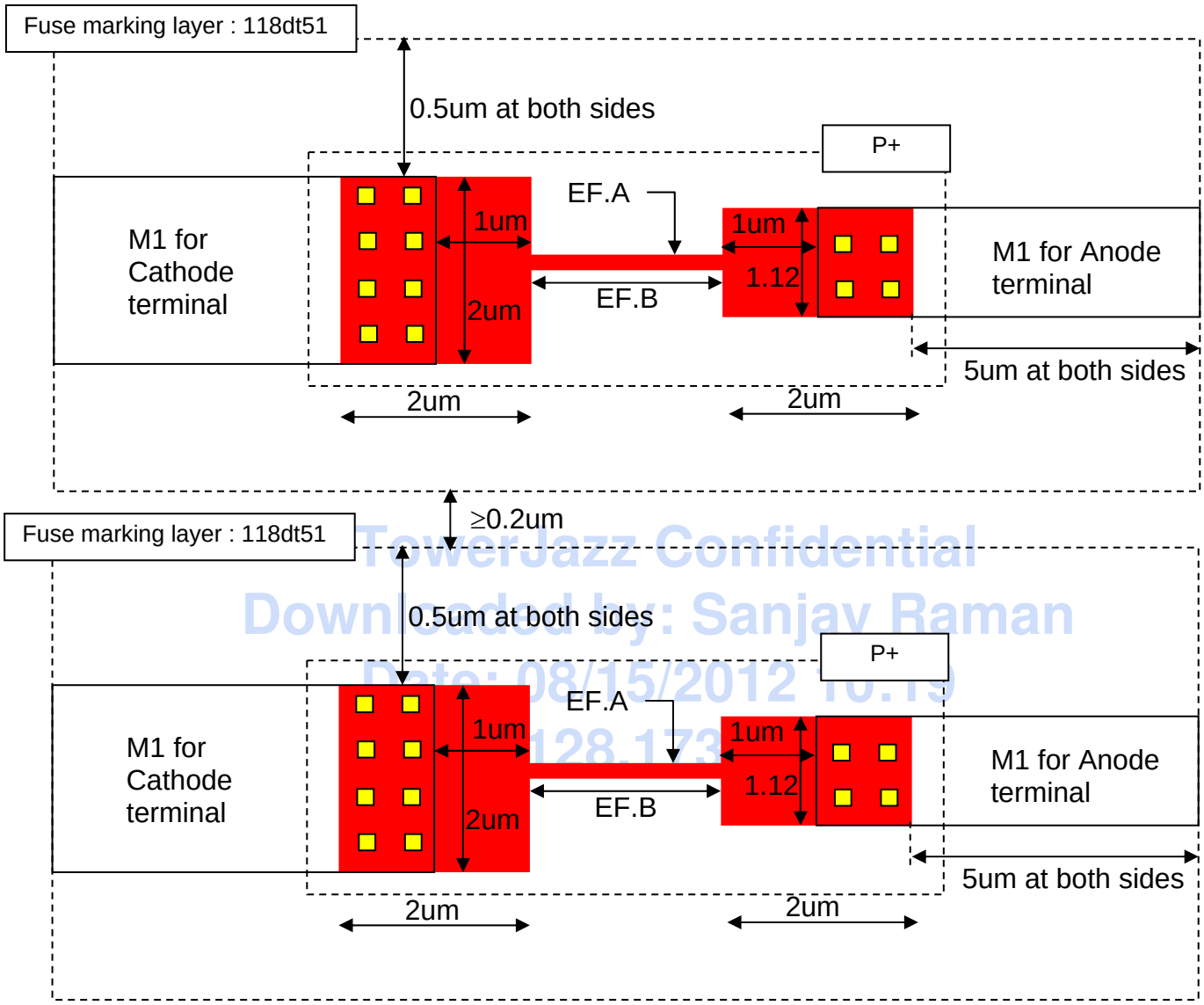
The design rules covered in this section supplement the CA18 and SBC18 design rules. See Applicable documents section. The rules presented here and implemented in the Efuse_Pcell_0p18.gds file must not be modified. Modification will adversely affect the programmability of the Efuse.
Efuse element is defined as the narrow poly portion of the poly polygon in the Efuse cell.

4.1 Efuse rules:

See Illustration 4-1.

Rule No.	Rule Name	
EF.A	Minimum/Maximum poly width of Efuse element (see illustration 4-1)	0.20
EF.B	Minimum/Maximum poly length of Efuse element	2.00
EF.C	Minimum distance between the Efuse element poly of two adjacent Efuses	3.0
EF.D	M1, M2 or M3 space to Efuse element. M1, M2 or M3 may not overlap the Efuse element.	0.8
EF.E	Mrklyr efuse is the marking layer for DRC, layer generation and LVS. It is rectangular must be centered on each efuse	3.0x16.0
EF.F	Mrklyr efuse space to mrklyr efuse	0.2
EF.G	The Efuse must consist of the following layers: salicided poly, contact, M1, mrklyr efuse, P+ implant, Pwell exclude, active dummy block, poly dummy block, M1 dummy block, M2 dummy block and M3 dummy block. All block layers must be co-incident with mrklyr efuse.	
EF.H	The mrklyr efuse (gds 118 dt 51) must not interact with the following layers: Active, Nwell, (Pwell if used), Buried Layer, DNW, N+ implant, Salicide block, All metals <= M3 (except for M1 terminal connections), dummy active, dummy poly, dummy M1 to M3 (even if M3 is Mtop).	
EF.J	Pad metal space to mrklyr efuse	2.0
EF.K	Only one Efuse allowed in each mrklyr efuse rectangle	
EF.L	P+ implant minimum overplot of Efuse poly (must be a rectangular polygon)	0.2
EF.M	Resistor marking layer or capacitor marking layer interaction with mrklyr efuse is not allowed.	
EF.BAD	Efuse not allowed in SOI processes	

Illustration 4-1.



4.2 Efuse Program Conditions:

See Program I/V Illustration 4-2:

Stage	Pre-Read/Program/Post-Read conditions	Min	Nom	Max	Units
Pre-READ	Efuse Cathode to Anode voltage (C=high, A=low), (higher than Max may burn fuse)		0.1	0.1	V
Pre-READ	Efuse current, (higher than Max may partially burn an efuse)			0.26	ma
Pre-READ	Efuse resistance (“cold”)	40	56	72	ohm
	Two efuse programming schemes are allowed. **A “5v scheme” and a “6.5v scheme”**				
Program – 5v scheme	Cathode to Anode voltage (C=high, A=low), [Vprog]	4.75	5.0	5.25	V
Program – 5v scheme	Voltage wave form: Pulse width (50% to 50%), [t_{pw}]	4.8	5	5.2	us
Program – 5v scheme	rise time, [t_r], & fall time, [t_f]		10		ns
Program – 6.5v scheme	Cathode to Anode voltage (C=high, A=low), [Vprog]	6.0	6.5	7.0	V
Program – 6.5v scheme	Voltage wave form: Pulse width (50% to 50%), [t_{pw}]	4.8	5	5.2	us
Program – 6.5v scheme	rise time, [t_r], & fall time, [t_f]		100		ns
Program	Expected peak current for the current pulse (current pulse typically lasts less than 0.6us)	40	46	52	ma
Program	Estimated resistance during program (“hot”)		250	500	ohm
Post-READ	Efuse Resistance (“cold”) of burned fuse	5K		open	ohms
Post-READ	Efuse Cathode to Anode voltage (C=high, A=low) for unprogrammed efuses, (higher than Max may burn fuses intended to be not burned)		0.1	0.1	V

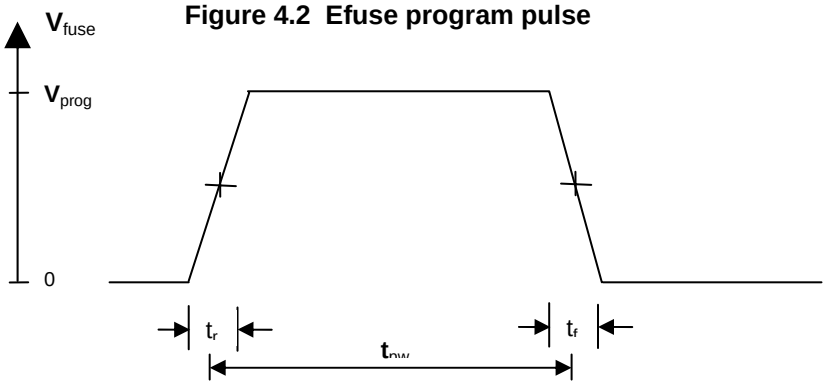


Figure 4.2 Efuse program pulse

Two programming schemes are allowed, the "5v scheme" and the "6.5v schemes".

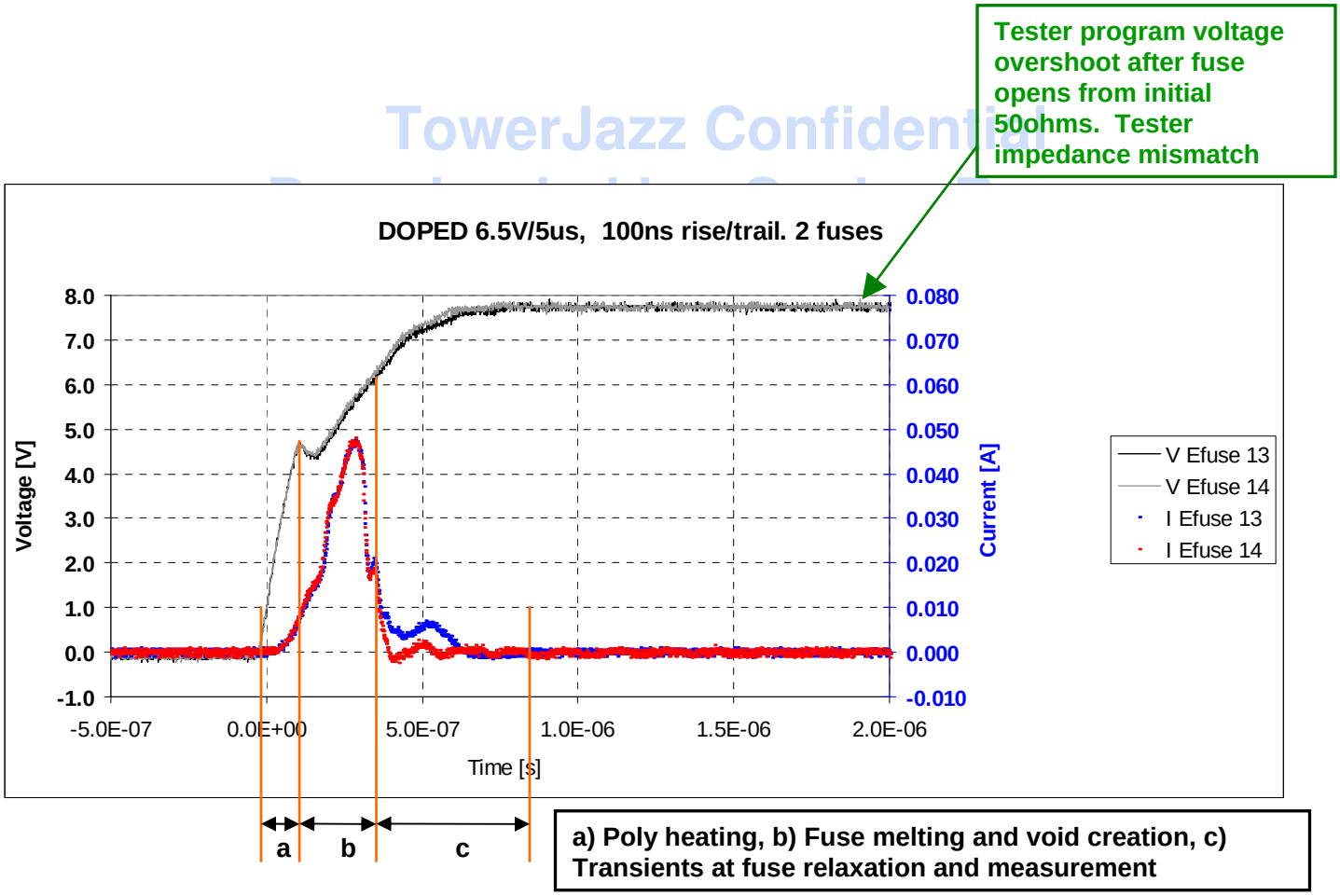
TOWERJAZZ NPB 0.18um E-Fuse specifications

	Units	Min	Nom	Max
Resistance (Cold/Pre_blown)	Ohms	40	56	72
Estimated Resistance - Transient (Hot)	Ohms		250	500
Resistance (Post _Blown)	Ohms	5000		open
"5v Program scheme" Programming voltage	Volt	4.75	5	5.25
Rise time	nsecs		10	
Width of pulse	us		5	
"6.5v Program scheme" Programming voltage	Volt	6.0	6.5	7.0
Rise time	nsecs		100	
Width of pulse	us		5	
Current (Programming)	mA	40	46	52
Iread (max)	mA		0.26	
Program Power Dissipated Efuse(estimated)	nj	30	42	55
Efuse Program Failure Rate - kit release	ppm			100
Efuse Program Failure Rate- final goal	ppm			2.5
Efuse Post-Program Failure Rate- leak to psub	ppm			1000

4.2.1 Program voltage and current expectation:

Our experiences of programming these Efuses are:
1) The current pulse typically lasts less than a microsecond even though the voltage lasts for 5us.
2) The current shows oscillations after it is burned. These are due to the test equipment and (we suspect) due to the Efuse relaxation after burning.
3) When the fuse starts to burn, the impedance changes dramatically. Our test equipment had 50ohms output into approx 30ohms (56ohm fuse paralleled with a 50ohm current probe). After the fuse burns the voltage is a mismatch to the TowerJazz tester supply and a voltage overshoot results.
4) Warning, when resistances are measured at the Pre-READ or Post-READ, care must be taken to not burn or damage the fuses. Keep the read voltage and current for initial efuse reads and reads of non-programmed efuse post-reads on the Efuse itself to <=0.1v and <26ua respectively.
5) In all CA18 (except for SOI) and SBC18 processes (both 3.3v and 5v CMOS versions) there are extended drain LDD transistors available to design drivers for above Vdd operation sections.

Illustration 4-2-1.



Programming setting of 6.5v w/50ohm output. 5us pulse w/100ns rise/fall times.

5. Reliability data for the NPB Efuse

5.1 Efuse Programming Statistics:

Programming test: Minimum spec for post program efuses (5Kohm) and a program failure rate of <100ppm. Data from the two programming schemes is presented here. The "5v scheme" is data for 4.75v to 5.25v and the "6.5v scheme" is for 6v to 7v.

NPB 0.18um CMOS E-Fuse Cumulative Program Statistics (Post-Burn OOS)

Vprogram w/50 ohm (v)	T-rise (ns)	OOS <5e3 ohm	Count	OOS ppm
4.75	10	3	31696	94
5	10	0	47704	<20
5.25	10	0	18080	<55
6.0	100	0	8112	<123
6.5	100	0	8008	<124
7.0	100	0	7020	<142
4.75 to 5.25	10	3	97480	30
6.0 to 7.0	100	0	23140	<43

NPB 0.18um SBC18 E-Fuse Cumulative Program Statistics (Post-Burn OOS)

Vprogram w/50 ohm (v)	T-rise (ns)	OOS <5e3 ohm	Count	OOS ppm
4.75	10			
5	10			
5.25	10			
6.0	100	0	8392	<119
6.5	100	0	8368	<119
7.0	100	0	7488	<133
4.75 to 5.25	10			
6.0 to 7.0	100	0	24248	<41

NPB 0.18um CA18 & SBC18 E-Fuse Cum Program Statistics (Post-Burn OOS)

Vprogram w/50 ohm (v)	T-rise (ns)	OOS <5e3 ohm	Count	OOS ppm
4.75	10	3	31696	94
5	10	0	47704	<20
5.25	10	0	18080	<55
6.0	100	0	16504	<60
6.5	100	0	16376	<61
7.0	100	0	14508	<68
4.75 to 5.25	10	3	97480	30
6.0 to 7.0	100	0	47388	<21

Post program leakage test to Psub spec is <1000ppm. 100% Pass

NPB 0.18um CA18 & SBC18 E-Fuse Post-Program Leakage to Psub				
Vprogram w/50 ohm (v)	T-rise (ns)	OOS <20Kohm	Count	OOS ppm
5	10	0	4624	<216
4.5	100	0	312	<3194
5.0	100	0	312	<3194
5.5	100	0	312	<3194
6.0	100	0	832	<1200
6.5	100	0	728	<1371
7.0	100	0	468	<2132
		0	7588	<131

5.2 Efuse Reliability Results:

5.2.1 High Temp Bake and Deep Temp Cycle Tests:

100% Pass

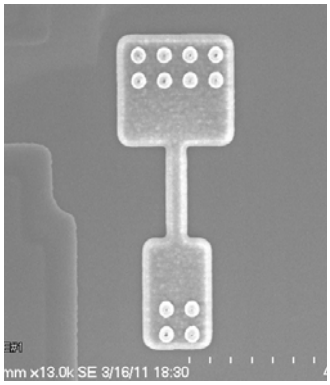
NPB 0.18um CA18 & SBC18 E-Fuse Post-Program Stability Tests				
Vprogram w/50 ohm (v)		OOS <5Kohm	Count	OOS ppm
6.0v, 6.5v, 7.0v	No HTS or DTC	0	3016	<331
6.0v, 6.5v, 7.0v	Post HTS or DTC	0	9048	<110

5.2.2 Post-Burn Pinhole Test:

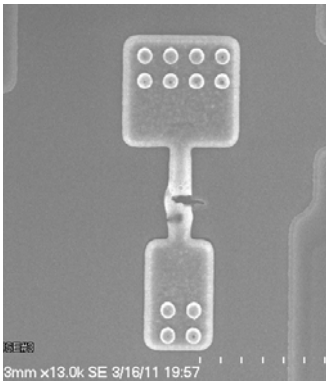
100% Pass

NPB 0.18um CA18 & SBC18 E-Fuse Post-DTC Pinhole Tests				
Vprogram w/50 ohm (v)		OOS <5Kohm	Count	OOS ppm
6.0v, 6.5v, 7.0v	No DTC	0	approx 3,000	<335
6.0v, 6.5v, 7.0v	Post DTC	0	3016	<331

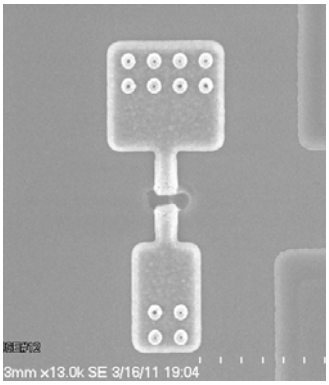
5.2.3 Post-Burn SEM Analysis summary:



Un-programmed fuse



3.5v programmed fuse



6v programmed fuse

SEM analysis for 6.5v program scheme: Pass

5.2.4 Post-Burn Proximity Analysis Summary:

Burn Efuse next to transistors and burn Efuse w/ M2 or M3 over Efuse. 100% Pass

NPB EFUSE PROXIMITY TESTS			
	Count	Criteria	Pass
FUSE TO FUSE	236	99% 0.95<Rfinal/Rinit<1.05	100%
METAL1 OVER FUSE	236	99% 0.95<Rfinal/Rinit<1.05	100%
METAL2 OVER FUSE	236	99% 0.95<Rfinal/Rinit<1.05	100%
METAL3 OVER FUSE	236	99% 0.95<Rfinal/Rinit<1.05	100%
TRANSISTOR TO FUSE	472 N 222 P	99% 0.95<Final/Initial<1.05 for Vt, K, Idsat, Log(Ioff), IsubpkN	100%