

Jazz Semiconductor

CA13 / SBL13 / SBC13 Design Manual

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Revision Number	Revision Description	Date
01	Initial release	08/03/05
02	Added 5.6 stacked MiM, cpoly capacitors, and MOS varactor	09/09/05
03	<p>Updated document to include CA13HC and SB13HC, the new super set process variant names</p> <p>Updated available device list to include high value resistor and high Vt FET</p> <p>Add NPN chapter, converting DM from CA13 to CA13/SBL13</p> <p>Add VPNP chapter</p> <p>Add X-Sigma Chapter</p> <p>Update MOSFET and MOSVAR chapters to reflect POR silicon.</p> <p>Added preliminary documentation on high Vt 1.2V CMOS devices</p> <p>Update poly resistor ESPECs</p> <p>Added high value poly resistor section</p> <p>Updated cross-sections for capacitor, resistor, and vertical pnp devices</p>	12/08/06
04	Added SBC13 200GHz NPN chapter	09/25/07

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1.0 Introduction

This document is intended to serve as a modeling design guide for CA13, SBL13, and SBC13 the Jazz Semiconductor 0.13um Analog/RF CMOS and SiGe BiCMOS processes family. SBL13 and SBC13 are identical to CA13 with the addition of the 90GHz SiGe-Lite and 200GHz SiGe NPN device modules, respectively. Please refer to the following design rule and electrical specification documents for additional information about the CA13, SBL13, and SBC13 process definitions and its variants:

NPB PS-0663 CA13 Design Rules

NPB PS-0577 CA13 Electrical Specifications

NPB PS-0746 SBL13 Design Application Note

NPB PS-0853 SBC13HA Design Application Note

The CA13, SBL13, and SBC13 models were verified using Cadence Spectre and ADS. Hspice simulators are also supported in selected processes. Table 1.1 lists the devices available to each process variant while Table 1.2 lists the different interconnect and triple well options available to CA13HC, SBL13HC, and SBC13HA.

TABLE 1.1 CA13HC and SBL13HC device availability table

Devices	CA13HC	SBL13HC	SBC13HA
High Voltage FET	X	X	X
Low Voltage FET	X	X	X
Low Voltage High Vt FET	X	X	X
Low Voltage 200GHz NPN			X
Medium Voltage 75GHz NPN			X
Low/Medium Voltage NPN		X	
High Voltage NPN		X	
Vertical PNP	X	X	X
Diodes	X	X	X
Low Value Poly Resistor	X	X	X
High Value Poly Resistor	X	X	X
Nwell Resistor	X	X	X
MOS Varactor	X	X	X
2.8fF MIM Capacitor	X	X	X
5.6fF Stacked MIM Capacitor	X	X	X
Inductors	X	X	X

TABLE 1.2 CA13, SBL13, and SBC13 interconnect and Deep Nwell options

Variant	Metal Layers	Deep Nwell	Top Metal Thickness
All Variants	6	Yes	2.8

1.1 Device List and Description

FETs:

- nfet (analog NFET, thin oxide, 4-terminal with implicit bulk pin, sub-circuit model NFETs)
- nfet_4 (analog NFET, thin oxide, 4-terminal with explicit bulk pin, sub-circuit model NFETs)
- pfet (analog PFET, thin oxide, 4-terminal with implicit bulk pin, sub-circuit model PFETs)
- pfet_4 (analog PFET, thin oxide, 4-terminal with explicit bulk pin, sub-circuit model PFETs)
- nfet3p3 (analog NFET, thick oxide, 4-terminal with implicit bulk pin, sub-circuit model n3p3fets)
- nfet3p3_4 (analog NFET, thick oxide, 4-terminal with explicit bulk pin, sub-circuit model n3p3fets)
- pfet3p3 (analog PFET, thick oxide, 4-terminal with implicit bulk pin, sub-circuit model p3p3fets)
- pfet3p3_4 (analog PFET, thick oxide, 4-terminal with explicit bulk pin, sub-circuit model p3p3fets)
- nfet_rf (RF NFET, thin oxide, 4-terminal with implicit bulk pin, sub-circuit model NFET_rf)
- pfet_rf (RF PFET, thin oxide, 4-terminal with implicit bulk pin, sub-circuit model PFET_rf)
- nfet3p3_rf (RF n3p3fet, thick oxide, 4-terminal with implicit bulk pin, sub-circuit model n3p3fet_rf)
- pfet3p3_rf (RF p3p3fet, thick oxide, 4-terminal with implicit bulk pin, sub-circuit model p3p3fet_rf)
- nfet_vth (high Vt NFET, thin oxide, 4-terminal with implicit bulk pin, sub-circuit model NFETs_vth)
- pfet_vth (high Vt NFET, thin oxide, 4-terminal with implicit bulk pin, sub-circuit model PFETs_vth)

NPNs:

- npn (npn, 4-terminal with implicit bulk pin, sub-circuit model name based on geometry)
 - device "L" type is for low voltage
 - device "M" type is for medium voltage
 - device "H" type is for high voltage

PNPs:

- vnpn (pnpa (25x25), pnpb (11x11), pnpc (5.4x5.4), pnpd (3x3) (3-terminal, primitive model))

Junction Diodes:

- dn (n+/sub junction diode, thin oxide, 2-terminal, primitive model ndiode)
- dp_3 (schematic based, 3 terminal p+/well junction diode, thin oxide)
- dn3p3 (n+/sub junction diode, thick oxide, 2-terminal, primitive model n3p3diode)

- dp3p3_3 (schematic based, 3 terminal p+/well junction diode, thick oxide)
- dnwell (nwell modeling diode, simulation only, 2-terminal, primitive model nwdiode)
- ddnw (nwell to deep nwell diode device, 2 terminal, primitive model diode)
- diso (pwell to nwell/deep nwell diode device, 2 terminal, primitive model diode)

Resistors:

- rnwell (Nwell resistor, 3-terminal, sub-circuit model rw3t)
- rppoly_lo (unsalicated poly resistor, 3-terminal, sub-circuit model rpp3t)
- rppoly_hi (unsalicated poly resistor, 3-terminal, sub-circuit model rph3t)
- r_dummy (dummy resistor for LVS, 2-terminal)

Capacitors:

- cmim3 (2.8fF MIM capacitor over substrate between M4-M5, 3-terminal, sub-circuit model c3t_mim3)
- cmimw3_4 (2.8fF MIM capacitor over well between M4-M5, 4-terminal: plus-minus-well-sub, sub-circuit model c3t_mimw3)
- cmim3_m5 (2.8fF MIM capacitor over substrate between M5-M6, 3-terminal, sub-circuit model c3t_mim3_5)
- cmimw3_4_m5 (2.8fF MIM capacitor over well between M5-M6, 4-terminal: plus-minus-well-sub, sub-circuit model c3t_mimw3_5)
- cmim6 (5.6fF MIM capacitor over substrate, 3-terminal, sub-circuit model c3t_mim6)
- csmimw6_4 (5.6fF MIM capacitor over well, 4-terminal: plus-minus-well-sub, sub-circuit model c3t_smimw6)
- cpoly (Thin Oxide poly capacitor, 4-terminal with implicit bulk pin, sub-circuit model pc)
- cpoly3p3 (Thick Oxide poly capacitor, 4-terminal with implicit bulk pin, sub-circuit model pc)

Varactors:

- var_mos3p3 (3.3V MOS varactor, 3-terminal, sub-circuit model mosvar_3p3)

Inductors:

- ind (top metal planar square inductor, 3-terminal, sub-circuit model ind_3u)
- ind_diff (top metal square differential inductor, 4-terminal, sub-circuit model inddiff_3u)
- ind_oct (top metal planar octagonal inductor, 3-terminal, sub-circuit model ind_3u)
- ind_diff_oct (top metal differential octagonal inductor, 4-terminal, sub-circuit model inddiff_3u)

Fuse:

- fuse (metal fuse, 2-terminal, sub-circuit resistor model fuse) (Data not available)

1.2 Device Model Availability

TABLE 1.3 Device Model availability

Device	DC	AC	RF	Noise	Corner	Statistical	Mismatch
Low Voltage FET	X	X	X	X	X	X	X
High Voltage FET	X	X	X	X	X	X	X
NPNs	X	X	X	X	X	X	X
VPNP	X	X			X	X	
Low Value Unsalicided Poly Resistor	X	X	X	X	X	X	X
High Value Unsalicided Poly Resistor	X	X	X	X	X	X	X
Nwell Resistor	X	X			X	X	
MIM Cap	X	X	X		X	X	X
Poly Capacitors	X	X			X	X	
MOS Varactor	X	X	X		X	X	
Low/High Voltage n/p diodes	X	X			X	X	
Inductor	X	X	X		X	X	X
Differential Inductor	X	X	X		X	X	X
Interconnect	X	X					

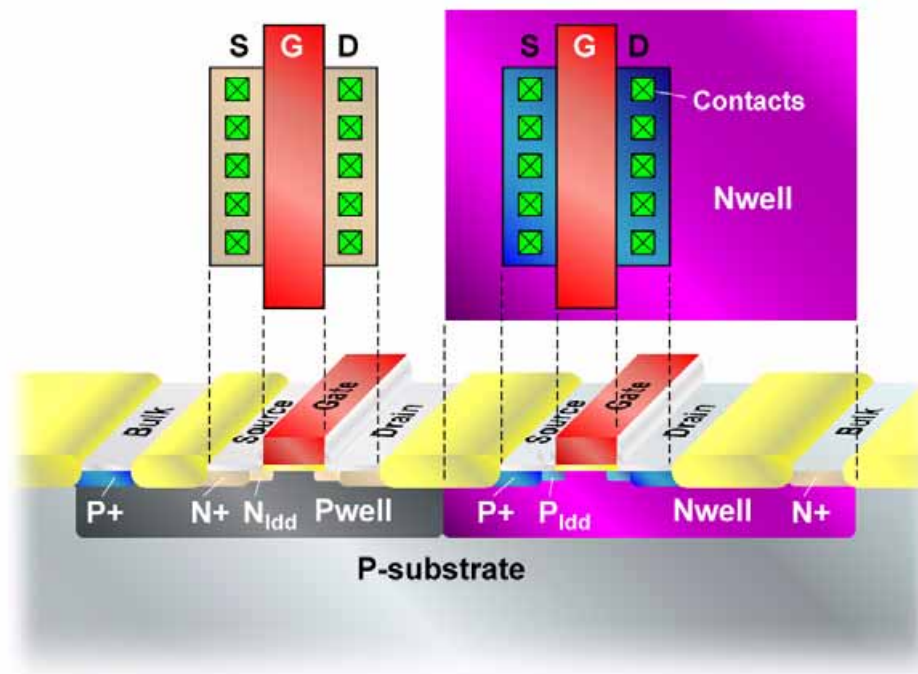
2.0 MOSFET Model

The following chapter documents the Jazz CA13 1.2V MOSFET model. Jazz would like to notify CA13 users of its intention to modify the MOSFET device structure to allow for an increase to 1.5V operation. This voltage headroom improvement requires a slight gate oxide thickness increase. The new device has been engineered to offer the same threshold and saturation current performance of the below described 1.2V device in efforts to minimize potential circuit performance changes. The models in the design kit have been updated to reflect these changes. Silicon validation of this new 1.5V model will be added to this chapter once validation completes. Please contact Jazz design support should you have additional questions.

2.1 Device Description

The SBL13/CA13 process supports two different mixed-signal (MS) models. The first model relates to the thin gate-oxide FETs with a maximum operation voltage of 1.2v. The second model relates to the thick gate-oxide FETs with a maximum operation voltage of 3.3V. The cross section of a typical SBL13/CA13 1.2v CMOS section is illustrated in Figure 2.1. High-Vt 1.2v N and PFETs, with thresholds 200mV higher than the regular FETs, are also supported. Characterization information for the high-Vt Fets will be provided in subsequent releases of this document.

FIGURE 2.1 NFET and PFET cross section



2.2 Model Description

TABLE 2.1 Model summary for 1.2v and 3.3v Fets

Property	1.2v Fets	3.3v Fets
Model name	nfet, pfet, nfet_vth (high-Vt), pfet_vth (high-Vt)	nfet3p3, pfet3p3
Temperature range	-40 to 125°C	-40 to 125°C
Channel length	0.12μm ≤ L < 100μm	0.36 (0.3 for pfet3p3) μm ≤ L < 100μm
Channel width	0.15μm ≤ W < 100μm	0.4μm ≤ W < 100μm
No. of fingers	1 ≤ NF ≤ 100	1 ≤ NF ≤ 100
Bias range	Vgs : 0 ~ 1.2V, Vds : 0 ~ 1.2V, Vbs : 0 ~ 1V	Vgs : 0 ~ 3.3V, Vds : 0 ~ 3.3V, Vbs : 0 ~ 3V

2.2.1 Scalable Model

A completely scalable BSIM4 model was used to fit devices of all geometries. A limited set of model parameters were made geometry dependent to improve model accuracy, as per the equation inside BSIM4:

$$P = P0 + \frac{LP}{L_{eff}} + \frac{WP}{W_{eff}} + \frac{PP}{(L_{eff} \times W_{eff})} \quad (\text{EQ 1})$$

where P is the effective parameter value, with P0, LP, WP, and PP defining the geometric dependencies of the parameter.

A scalable model is highly desirable as it maintains the “physical” nature of the model. Parameters such as DVT0, that define the short channel threshold voltage behavior of a MOSFET, are physically extracted. In contrast to the scalable modeling approach, the “binned” model methodology divides the channel length and width space into multiple “bins” and model parameter sets for each of the bins are independently extracted. Eq. 1 is used to make the model parameters continuous across bin boundaries. Parameters such as DVT0 have no physical meaning. A significant advantage of the scalable model approach is in the corner and statistical modeling. These models are generated by changing process specific model parameters such as mobility and channel length, and are intuitively more accurate if the original model was physically extracted.

2.2.2 “Golden” Die Selection

A rigorous Quality Assurance (QA) methodology was used to select the “golden” die on which detailed measurements are performed and the model parameters extracted. Electrical specifications (E-spec) such as threshold voltage, saturation current, body constant were measured over multiple die to select the die closest to the E-spec of the technology. The geometry dependence of these parameters was also plotted to ensure a clean set of measurements. The following checklist encompasses the measured data QA:

TABLE 2.2 Measured data QA checklist

Critical parameters (I_{dsat} for the small and short device, V_{th} for the 4 corners large, narrow, short, and small) vs. Electrical Specifications within 5%
Plot V_{th} vs. Length and Width

TABLE 2.2 Measured data QA checklist

Plot V_{th} vs. Temperature for large device
Plot I_{dsat} vs. Length and Width
Plot I_{dsat} vs. Temperature for short channel device
Plot Body constant vs. Length and Width
Plot Body constant vs. Temperature
Plot subthreshold slope (ST) vs. L and W

Any inconsistencies observed during the QA procedure results in either the deletion of the relevant measured data point or a re-measurement of that parameter or sweep.

2.2.3 1.2v FET Model Parameter Extraction Devices:

The 1.2v devices were measured using the Agilent IC-CAP characterization and modeling software. Table 2.3 lists the devices that were measured at 25°C. A limited set of devices ($W/L = 10/10, 10/0.12, 0.15/10, 0.15/0.12 \mu\text{m}$) were measured at -40 and 125°C to extract temperature coefficients of model parameters.

TABLE 2.3 List of sizes of the measured 1.2v N and P FETs

$W = 10\mu\text{m}$	$L = 0.12, 0.13, 0.14, 0.15, 0.18, 0.2, 0.3, 0.4, 0.6, 1, 2, 5, \text{ and } 10\mu\text{m}$	Large W, scale channel length
$L = 10\mu\text{m}$	$W = 0.15, 0.2, 0.3, 0.4, 0.6, 1, 2, 5, \text{ and } 10\mu\text{m}$	Large L, scale channel width
$W = 0.15\mu\text{m}$	$L = 0.12, 0.14, 0.2, 0.4, 10\mu\text{m}$	Small devices
$L = 0.12\mu\text{m}$	$W = 0.15, 0.2, 0.3, 0.4, 0.5, 1, 2, 5, 10\mu\text{m}$	Minimum L, scale channel width
L/W	0.2/0.14, 0.3/0.14, 0.3/0.2, 0.3/0.4, 0.5/0.14, 1/0.4, 2/2 μm	Misc. devices

Table 2.4 lists the various characteristics measured for each of the FETs listed in Table 2.3.

TABLE 2.4 List of measured characteristics for 1.2v FETs (TYPE=1 for NFET; TYPE=-1 for PFET)

Characteristic	Type	V_{DS} (V)	V_{GS} (V)	V_{BS} (V)
I_d Vs. V_{gs}	Threshold -Linear	TYPE*0.05	-0.4 to 1.2, 50mV steps	0 to -TYPE*1, in -TYPE *0.2V steps
I_d Vs. V_{gs}	Threshold -Saturation	TYPE*1.2	-0.4 to 1.2, 50mV steps	0 to -TYPE*1, in -TYPE *0.2V steps
I_d Vs. V_{ds}	Output	0 to TYPE*1.2V, TYPE*50mV steps	TYPE*0.2 to TYPE*1.2V, TYPE*0.2 V steps	0
I_d Vs. V_{ds}	Output with back bias	0 to TYPE*1.2V, TYPE*50mV steps	TYPE*0.2 to TYPE*1.2V, TYPE*0.2 V steps	-TYPE*1

2.2.4 Dog-Bone Effect for 1.2v Devices

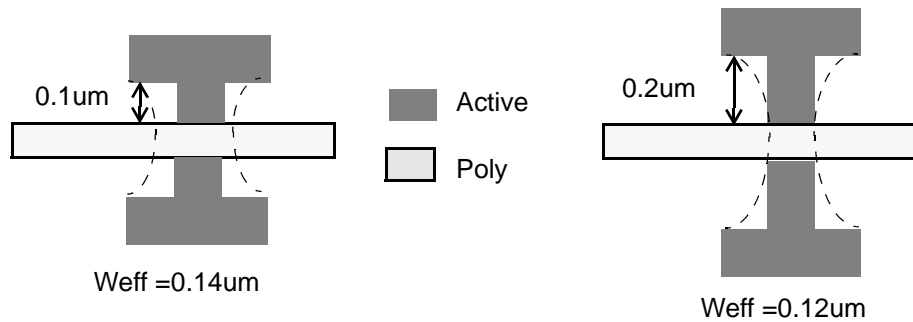
The CA13 design rules allow a minimum drawn standard FET width of 0.15 μm . FETs with W smaller than 0.3 μm require a dog-bone layout to make contact with the source/drain regions. The effective width of the narrow FETs ($W < 0.34\mu\text{m}$) increases as a result of the dog-bone layout. This effect is dominant for small channel lengths ($L < 0.6\mu\text{m}$). To account for the increase in W_{eff} , DW was gradually reduced for dog-boned FETs for small channel lengths by using the BSIM4 parameters WL and WW in Eq. 2:

$$\Delta W = WINT + \frac{WL}{L^{WLN}} + \frac{WW}{W^{WLN}} + \frac{WWL}{L^{WLN} \times W^{WLN}} \quad (\text{EQ 2})$$

The increased W_{eff} for short/narrow FETs is strongly dependent on the layout (gate poly to active shoulder spacing), as shown in Figure 2.2. This variation in W_{eff} is captured in the corner models, which account for both the layout and process variation for the short/narrow FETs.

No dog-bone layout is required for 3.3v FETs, which have a minimum channel width of 0.4 μm .

FIGURE 2.2 Schematic of layout showing impact of dog-bone on W_{eff}



2.2.5 3.3v FET Model Parameter Extraction Devices:

TABLE 2.5 List of sizes of the measured 3.3v N & P FETs

NFET		
$W = 10\mu\text{m}$	$L = 0.36, 0.5, 0.6, 0.8, 1, 2, 5, 10\mu\text{m}$	Large W, scale channel length
$L = 10\mu\text{m}$	$W = 0.4, 0.5, 0.6, 1, 2, 5, 10\mu\text{m}$	Large L, scale channel width
$W = 0.4\mu\text{m}$	$L = 0.36, 0.42, 0.6, 10\mu\text{m}$	Minimum W, scale channel length
$L = 0.36\mu\text{m}$	$W = 0.4, 0.6, 0.8, 1, 2, 10\mu\text{m}$	Minimum L, scale channel width
L/W	$0.4/0.42, 0.4/0.6, 0.6/0.42, 0.6/0.6, 1/0.6, 1/1, 2/2\mu\text{m}$	Misc. devices
PFET		
$W = 10\mu\text{m}$	$L = 0.3, 0.32, 0.34, 0.36, 0.4, 0.5, 0.6, 0.8, 1, 2, 5, 10\mu\text{m}$	Large W, scale channel length
$L = 10\mu\text{m}$	$W = 0.4, 0.6, 1, 2, 5, 10\mu\text{m}$	Large L, scale channel width
$W = 0.4\mu\text{m}$	$L = 0.3, 0.36, 0.42, 0.6, 10\mu\text{m}$	Minimum W, scale channel length
$L = 0.3\mu\text{m}$	$W = 0.4, 0.6, 0.8, 1, 10\mu\text{m}$	Minimum L, scale channel width
L/W	$0.6/0.36, 0.6/0.42, 0.6/0.6, 0.8/0.36, 1/0.36, 1/0.6, 1/1, 2/2\mu\text{m}$	

3.3v devices were measured using the Agilent IC-CAP characterization and modeling software. Table 2.5 lists the devices that were measured at 25°C. A limited set of devices ($W/L = 10/10, 10/0.36$ (10/0.3 for PFET), 0.4/

10, 0.4/0.36 (0.4/0.3 for PFET) μm) were measured at -40 and 125°C to extract temperature coefficients of model parameters. Table 2.6 lists the I-V characteristics measured for each of the FETs listed in Table 2.3.

TABLE 2.6 List of measured characteristics for 3.3v FETs (TYPE=1 for NFET; TYPE=-1 for PFET)

Characteristic	Type	V_{DS} (V)	V_{GS} (V)	V_{BS} (V)
I_D Vs. V_{GS}	Threshold -Linear	TYPE*0.05	0 to TYPE*3.3, TYPE*100mV steps	0 to -TYPE*3, in -TYPE*0.6V steps
I_D Vs. V_{GS}	Threshold - Saturation	TYPE*3.3	0 to TYPE*3.3, TYPE*100mV steps	0 to -TYPE*3, in -TYPE*0.6V steps
I_D Vs. V_{DS}	Output	0 to TYPE*3.3V, TYPE*100mV steps	TYPE*0.55 to TYPE*3.3V, TYPE*0.55 V steps	0
I_D Vs. V_{DS}	Output with back bias	0 to TYPE*3.3V, TYPE*100mV steps	TYPE*0.55 to TYPE*3.3V, TYPE*0.55 V steps	-TYPE*3

2.3 Parameter Extraction

2.3.1 IV Parameters

BSIM4 model parameters were physically extracted using BSIM Modeling Packages [1, 2]. Local optimization of selected parameters to the appropriate regions of the measured device characteristics was performed to better fit the measured data. RMS fitting errors were typically less than 1% on the I_D - V_{DS} curves and less than 3% on the g_{out} - V_{DS} curves. RMS fitting errors were typically less than 1% on the I_D - V_{GS} curves and less than 3% on the g_m - V_{GS} curves.

The temperature dependence of the model parameters was captured by using the relevant BSIM parameters to fit the measured data at -40C and 125C. The large channel threshold voltage in the linear and saturation regions, high field and back bias dependent mobility, the short channel threshold voltage and saturation currents, and the temperature dependence of the series drain/source resistances were fit to the measured data.

2.3.2 Capacitance Parameters

Junction capacitances were measured for bottom, field sidewall, and channel sidewall intensive structures. This capacitance was characterized for biases ranging from a small forward bias (0.2v) to a reverse bias equal to 1.2v for the 1.2v devices and 3.3v for the 3.3v devices. The measured values were separated into bottom (CJ), field sidewall (CJSW) and channel sidewall components (CJSWG) parameters by simultaneously solving the 3 equations.

The gate oxide capacitance characteristics were measured on a large area MOS transistor. The gate capacitance was fitted by using CAPMOD=2 model in BSIM4. These models takes into account quantum mechanical and poly depletion effects. The maximum error in fitting the intrinsic gate capacitances in inversion was less than 3%.

The gate-to-source/drain overlap capacitances and their bias dependencies were measured on minimum channel length and large width FETs. The gate overlap capacitance is a function of both the gate and substrate bias, though only the gate bias dependence is modeled in BSIM4.

The accuracy of the extracted capacitance parameters for the 1.2 and 3.3v FETs was verified by matching the measured delay times of ring oscillators with varying loads. The measured and simulated delay/stage for various ring-oscillator configurations are shown for the low and high voltage FETs in Table 2.7.

TABLE 2.7 Ring oscillator delay/stage.

Transistor	Ring Osc. load	Measured delay/stage (ps)	Simulated delay/stage (ps)
1.2v	No load	37.5	36.5
	1x N-gate	107.3	104.9
	2x N-gate	148.1	145.0
	5x N-gate	189.1	195.2
	1x P-gate	113.6	115.1
	2x P-gate	154.0	149.3
	5x P-gate	184.9	194.0
3.3v	No load	73.0	73.4
	1x N-gate	225.9	228.0
	2x N-gate	182.7	184.0
	5x N-gate	213.9	220.3
	8x N-gate	182.3	193.9
	1x P-gate	206.1	209.0
	2x P-gate	185.7	187.8
	5x P-gate	220.5	225.4
	8x P-gate	182.9	197.7

2.4 Model Verification

The model parameter set fitted to the measurements is referred to as the “measured” case, which is slightly different from the “NOM” model available in the SBL13/CA13 design kits. The simulated IV and CV characteristics with the measured case of the various MOSFETs are compared with the measured data in Figures 2.3 through 2.78. The device description is included in the figure caption and has the format of “max_operating_voltage_fetType_WxL_plotType_temperature”. For e.g. 1p2v_NFET_10x10_idvg_25C refers to the I_{drain} Vs. V_{gate} characteristic at 25°C of a 1.2v NFET with $W=10\mu\text{m}$ and $L=10\mu\text{m}$.

The CV plots show 6 different plots MOSFET capacitances. The top row plots are for junction capacitance from area, perimeter, and perimeter-under-gate intensive structures. The bottom row plots, from left to right, are for the oxide capacitances of large width and length MOSFET, oxide capacitance of a large W/short L MOSFET, and gate to source/drain overlap capacitance of a large W/short L MOSFET.

The IV plots show the threshold and output characteristics of the MOSFET. The threshold curves are a set of 6 plots, for I_d vs. V_{gs} in the linear region (top-left), I_d vs. V_{gs} in the saturation region (top-middle), and sub-threshold I_d vs. V_{gs} (top-right). The transconductance in the linear region (bottom left), transconductance in the saturation region (middle-right), and the substrate current vs. gate bias in saturation are shown in the second row. The output curves are a set of 4 plots: I_d vs. V_{ds} (top-left), I_d vs. V_{ds} with back-bias (top-right), and g_{ds} vs. V_{ds} (bottom-left), and g_{ds} vs. V_{ds} with back-bias (bottom-right).

Finally, unless otherwise labelled, the blue-circles are the measured data, and solid red lines are the model prediction.

FIGURE 2.3 1p2_NFET_cv_25C

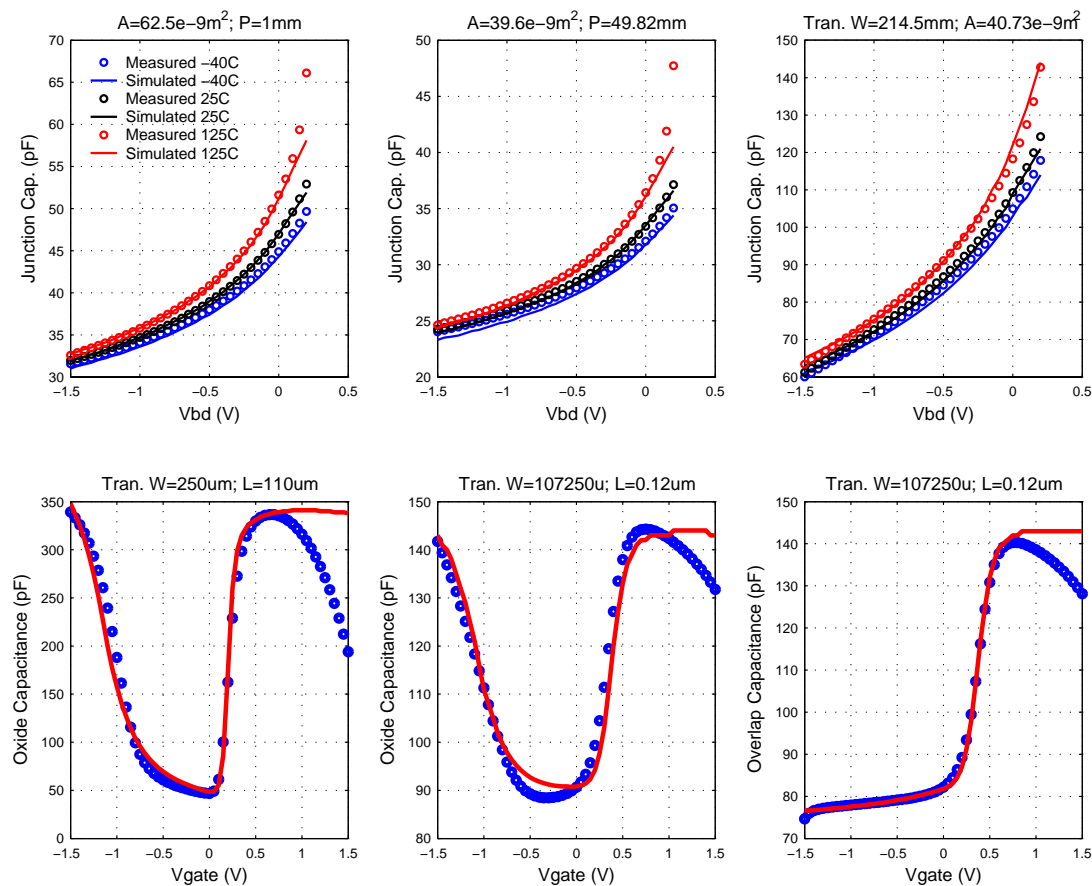
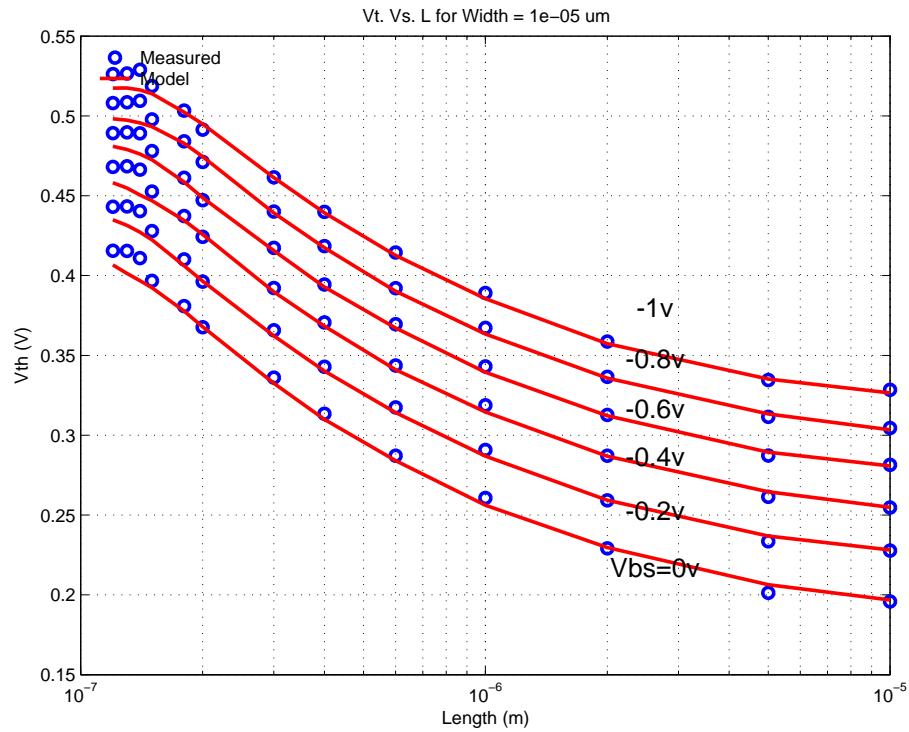


FIGURE 2.4 1p2v_NFET_vtVsL_25C



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FIGURE 2.5 1p2v_NFET_vtVsW_25C

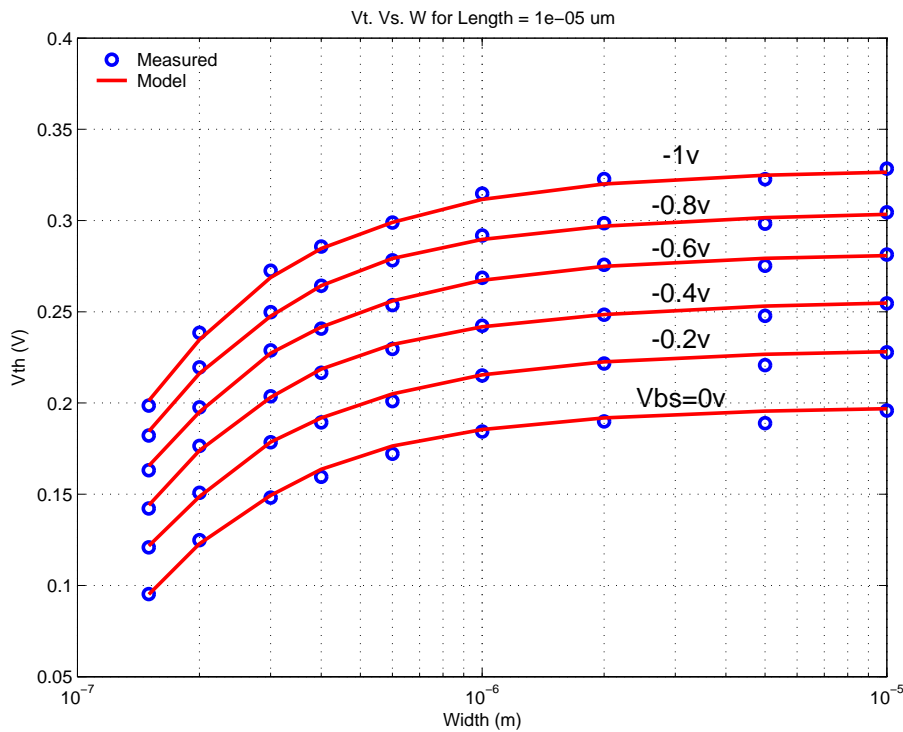


FIGURE 2.6 1p2v_NFET_10x10_idvd_25C

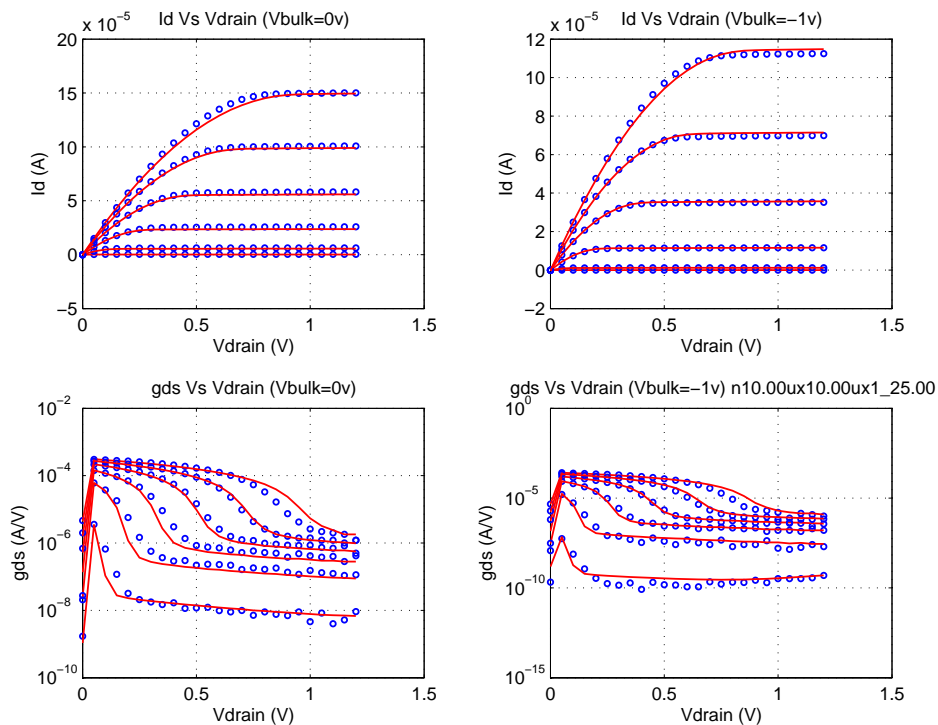


FIGURE 2.7 1p2v_NFET_10x10_idvg_25C

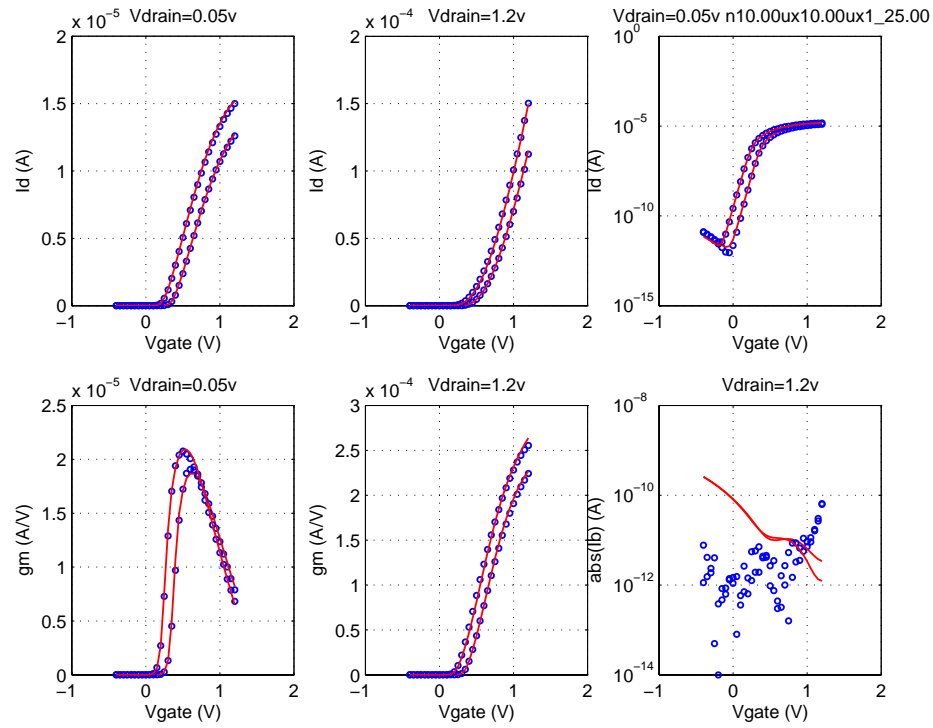


FIGURE 2.8 1p2v_NFET_10x0p12_idvd_25C

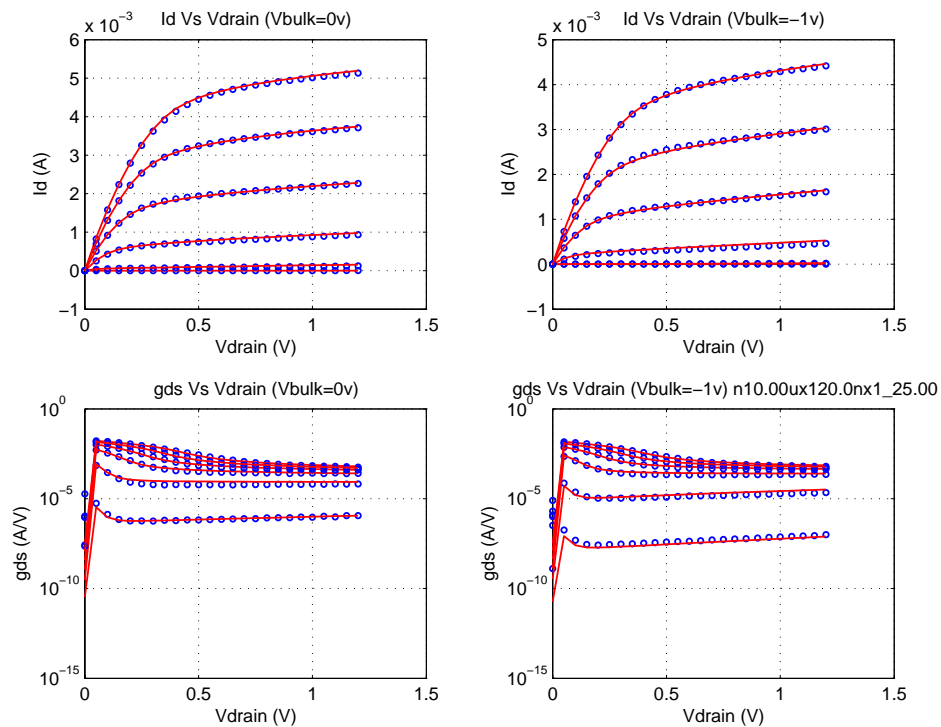


FIGURE 2.9 1p2v_NFET_10x0p12_idvg_25C

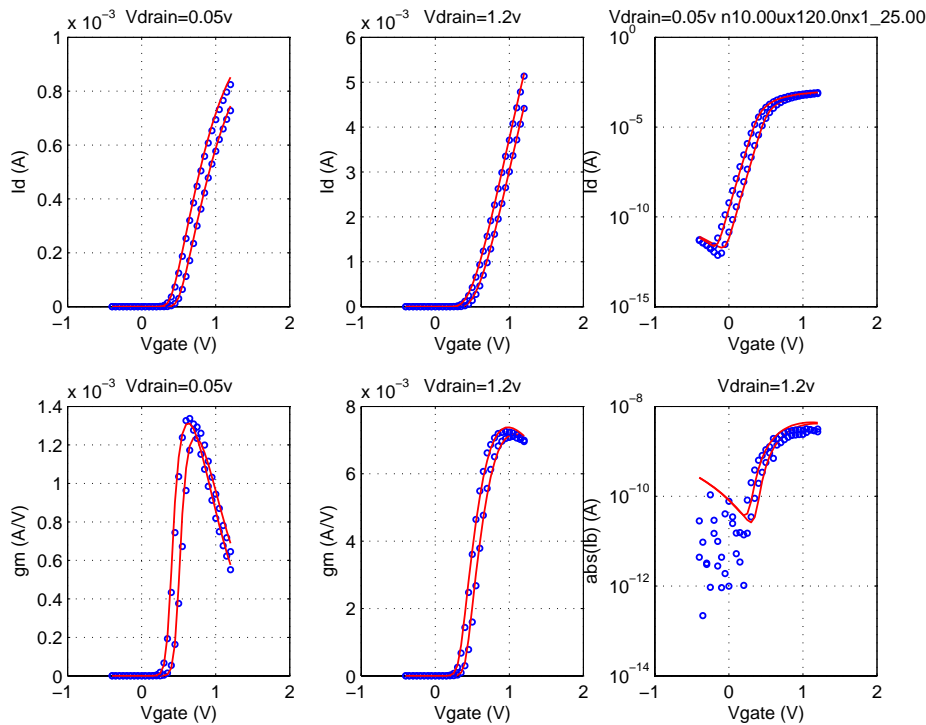


FIGURE 2.10 1p2v_NFET_0p15x10_idvd_25C

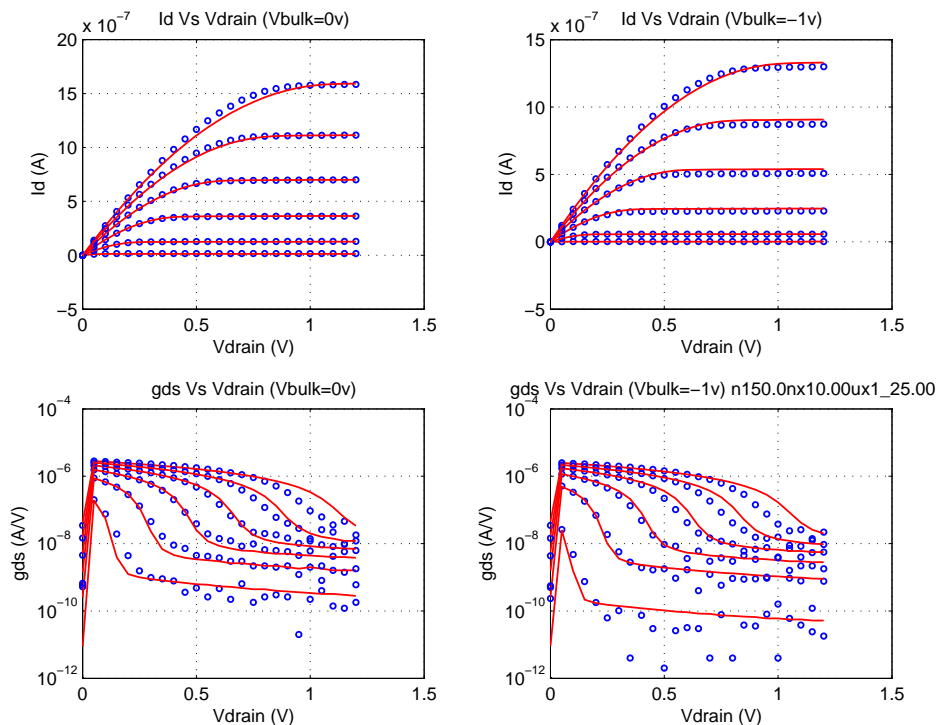


FIGURE 2.11 1p2v_NFET_0p15x10_idvg_25C

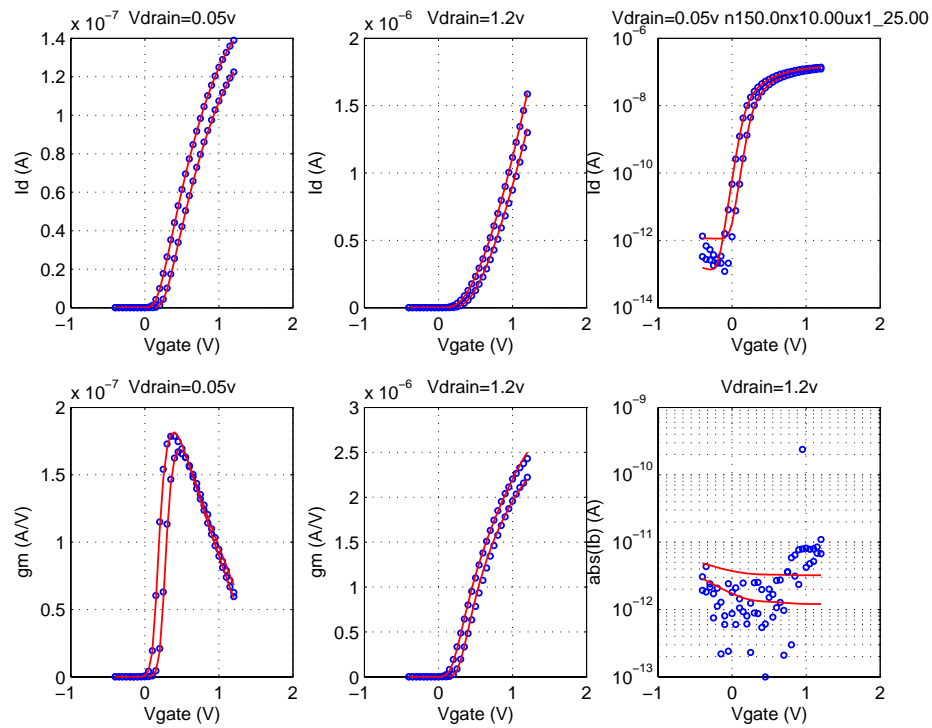


FIGURE 2.12 1p2v_NFET_0p15x0p12_idvd_25C

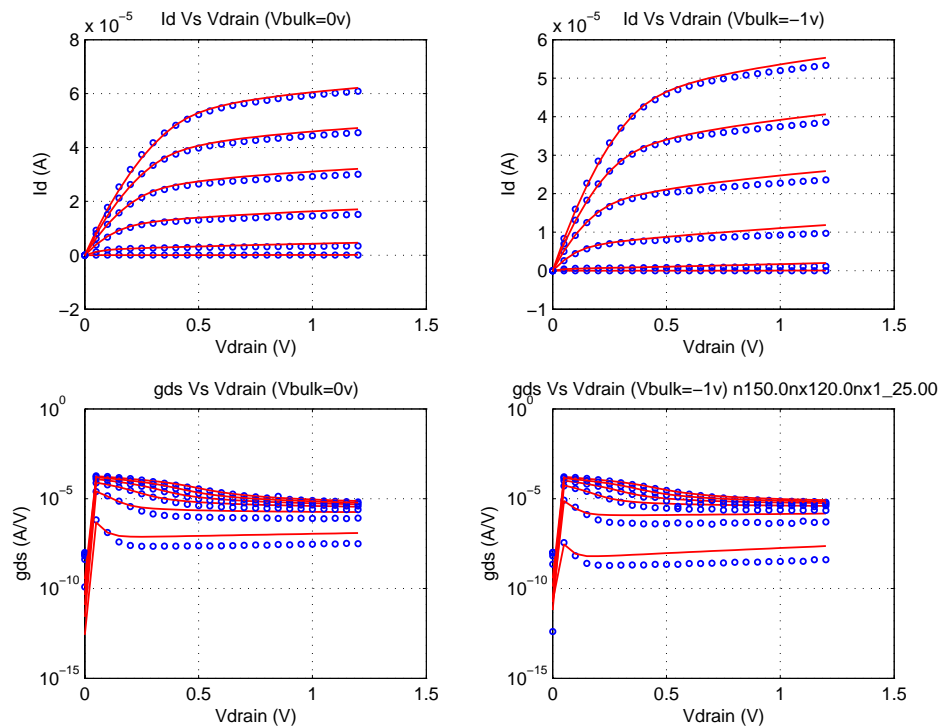


FIGURE 2.13 1p2v_NFET_0p15x0p12_idvg_25C

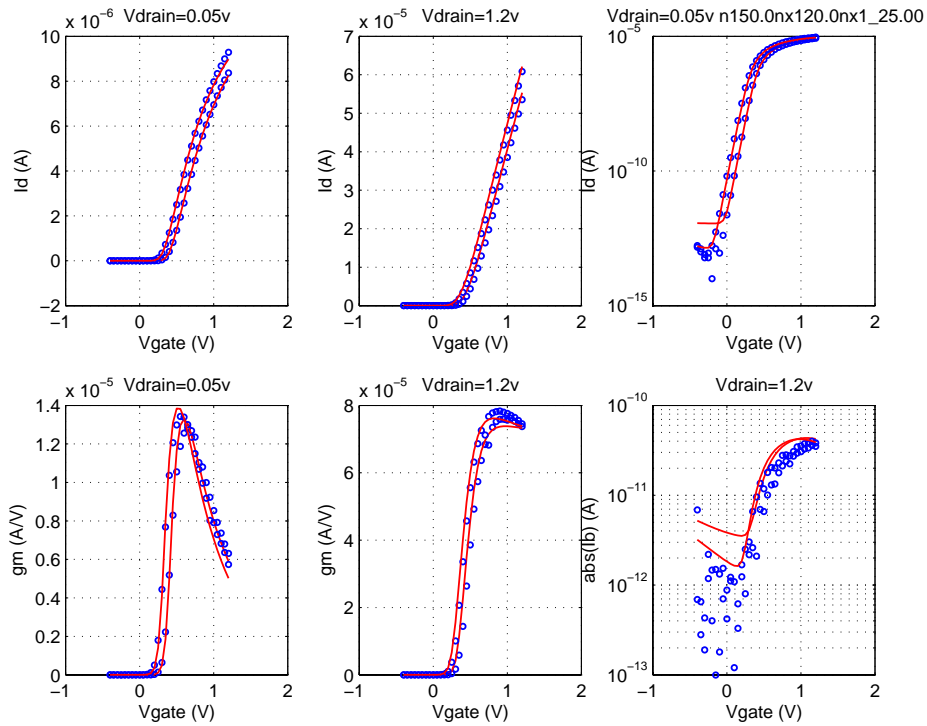


FIGURE 2.14 1p2v_NFET_0p5x0p12_idvd_25C

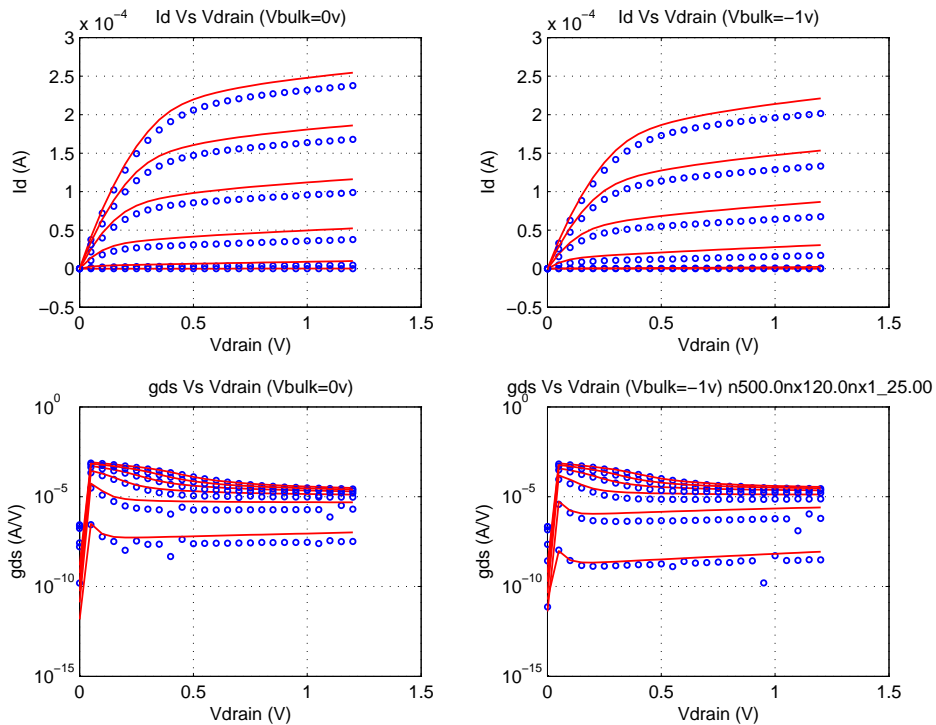


FIGURE 2.15 1p2v_NFET_0p5x0p12_idvg_25C

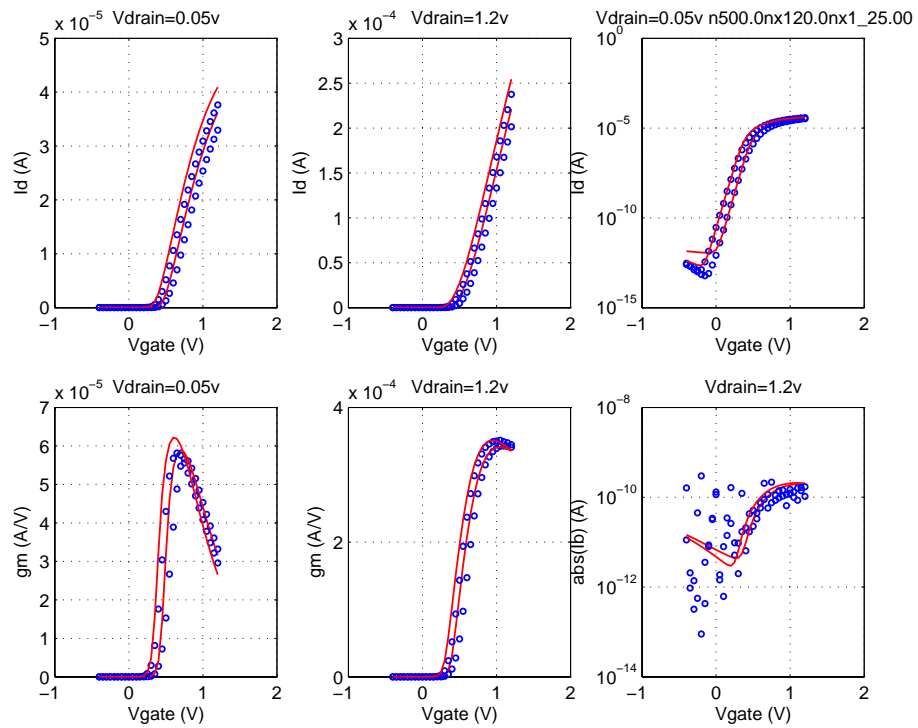


FIGURE 2.16 1p2v_NFET_10x0p18_idvd_25C

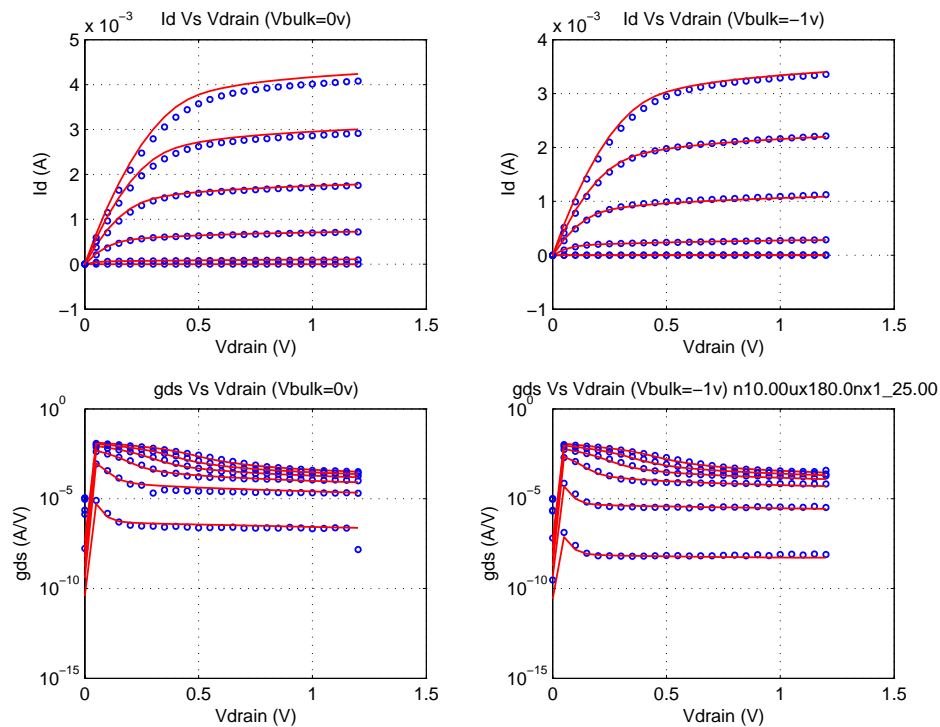


FIGURE 2.17 1p2v_NFET_10x0p18_idvg_25C

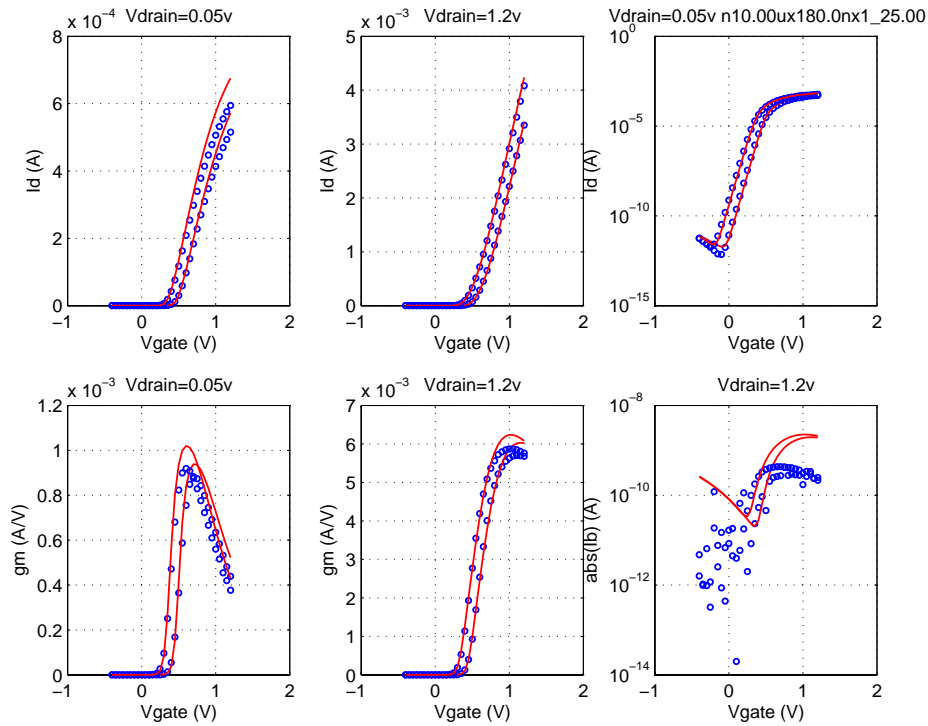


FIGURE 2.18 1p2v_NFET_10x0p12_idvd_-40C

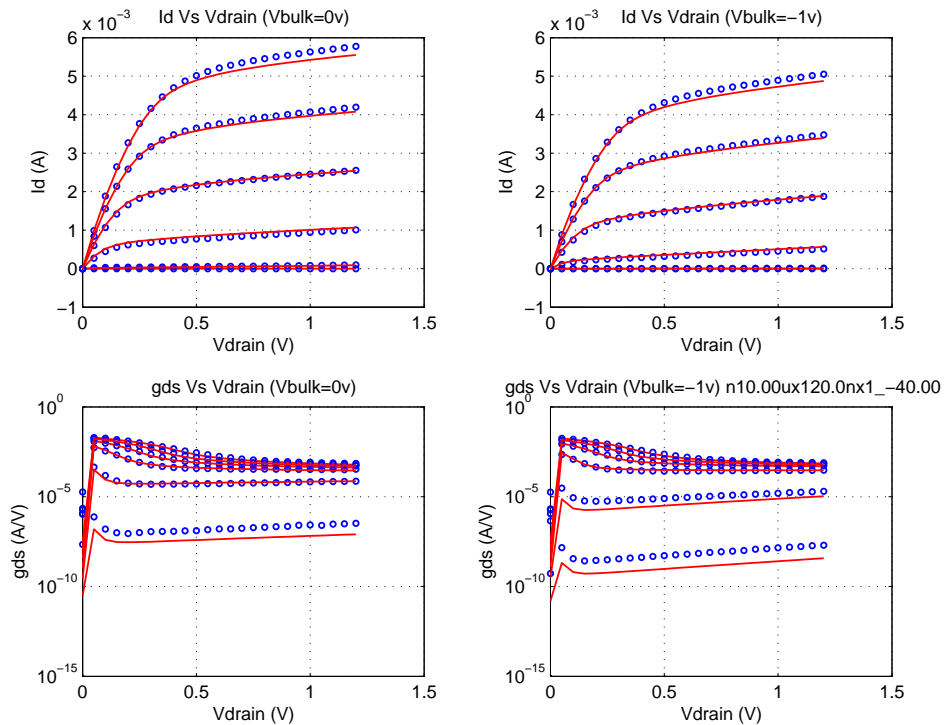


FIGURE 2.19 1p2v_NFET_10x0p12_idvg_-40C

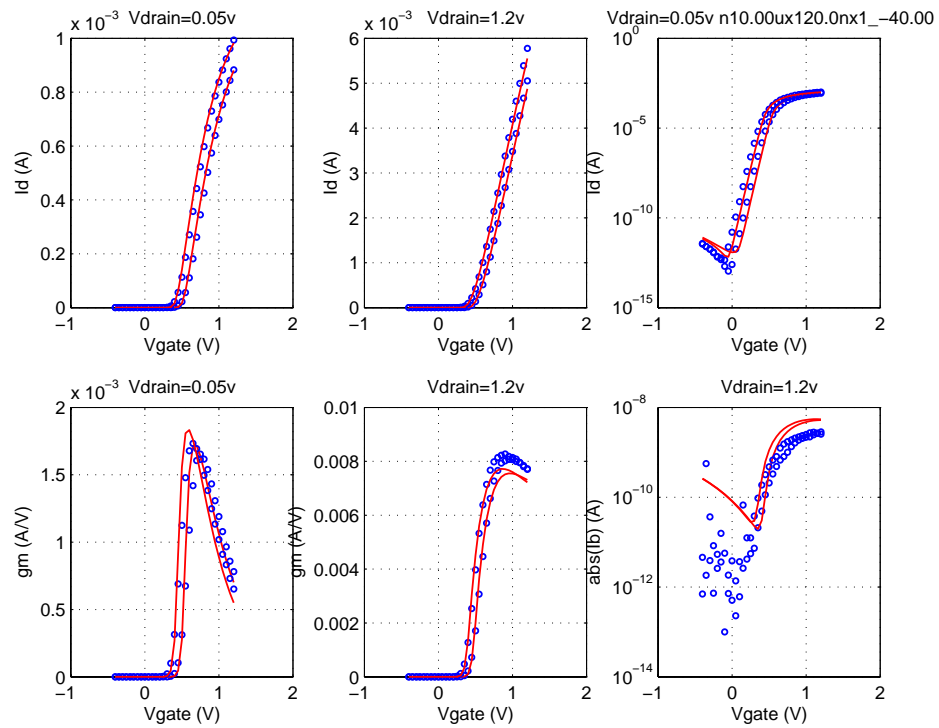


FIGURE 2.20 1p2v_NFET_10x0p12_idvd_125C

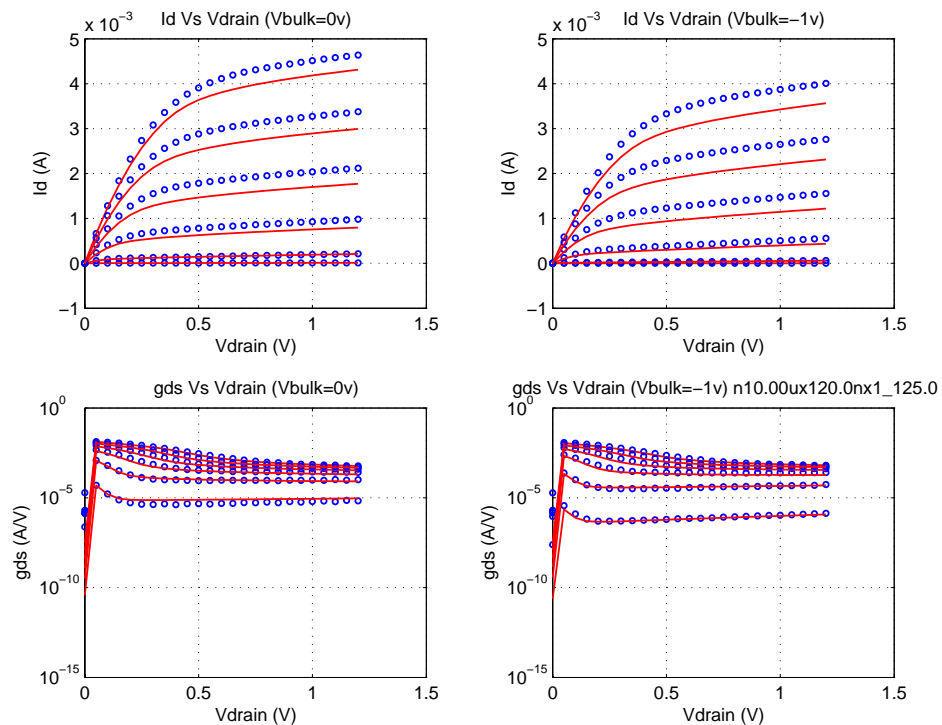
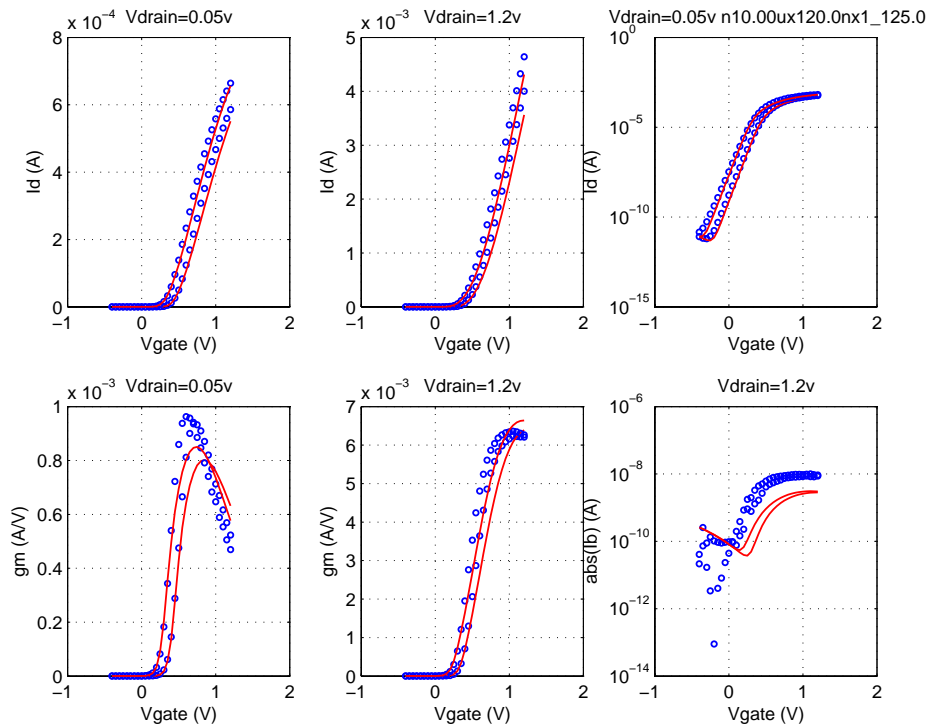


FIGURE 2.21 1p2v_NFET_10x0p12_idvg_125C



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FIGURE 2.22 1p2_PFET_cv_25C

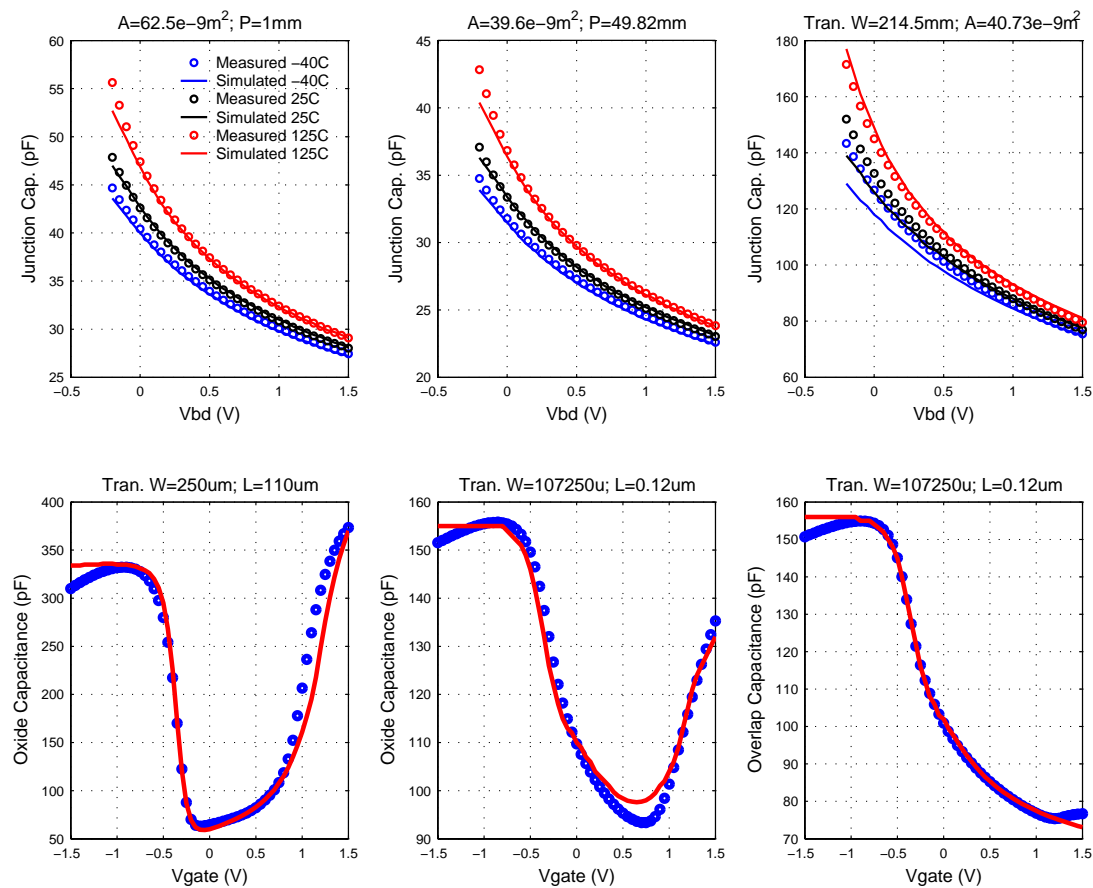


FIGURE 2.23 1p2v_PFET_vtVsL_25C

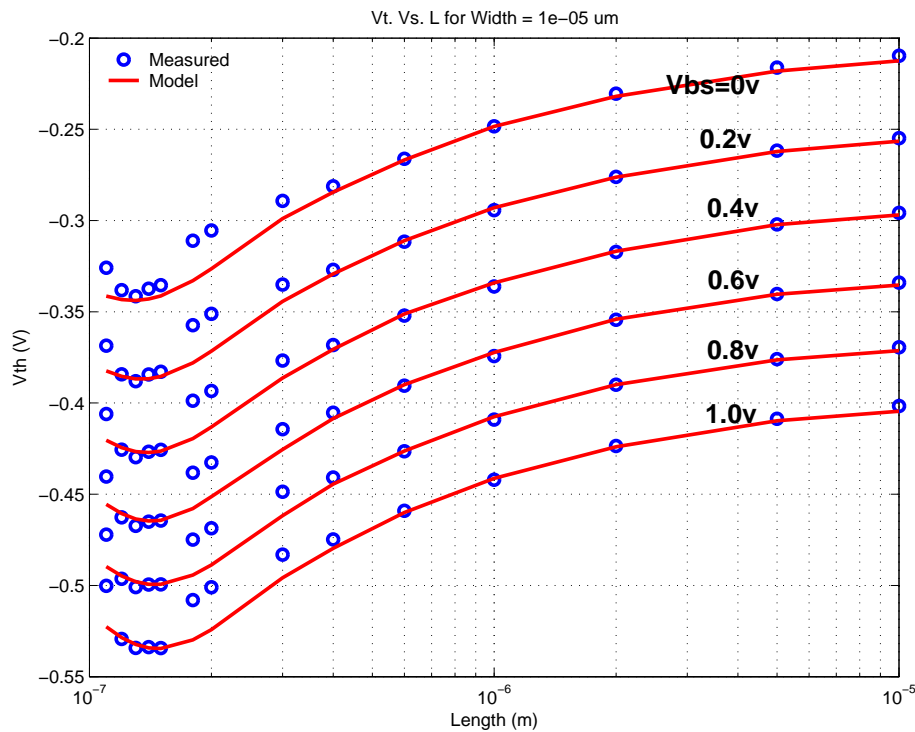


FIGURE 2.24 1p2v_PFET_vtVsW_25C

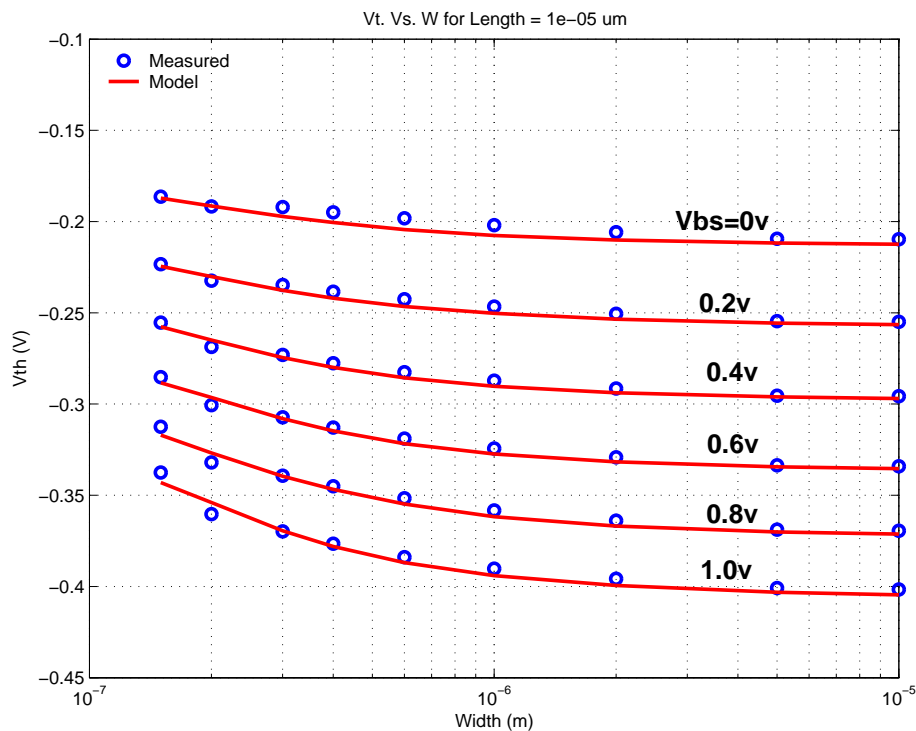


FIGURE 2.25 1p2v_PFET_10x10_idvd_25C

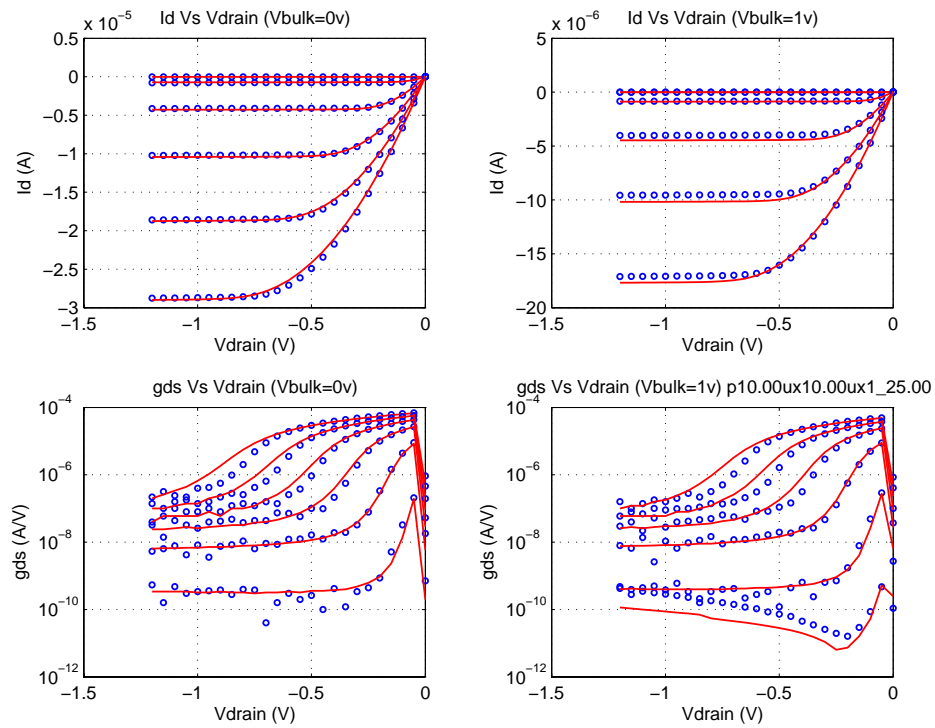


FIGURE 2.26 1p2v_PFET_10x10_idvg_25C

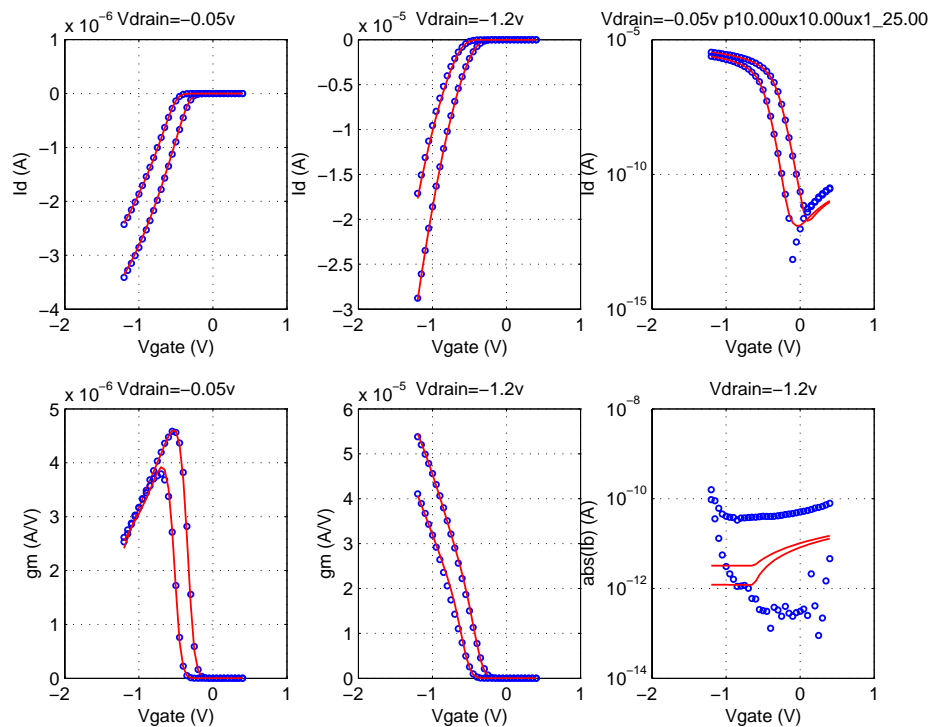


FIGURE 2.27 1p2v_PFET_10x0p12_idvd_25C

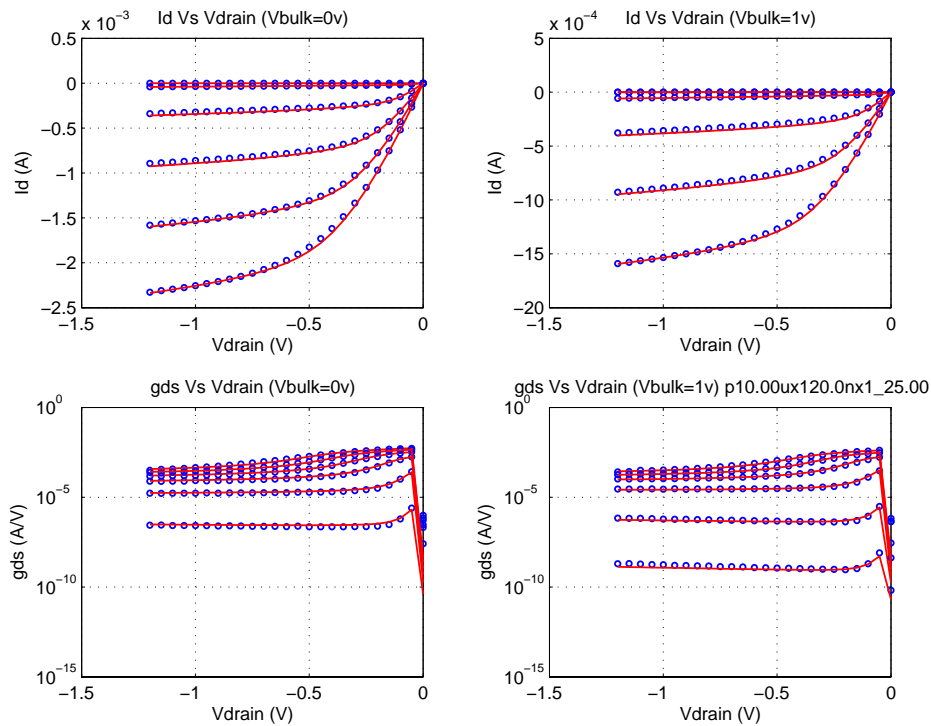


FIGURE 2.28 1p2v_PFET_10x0p12_idvg_25C

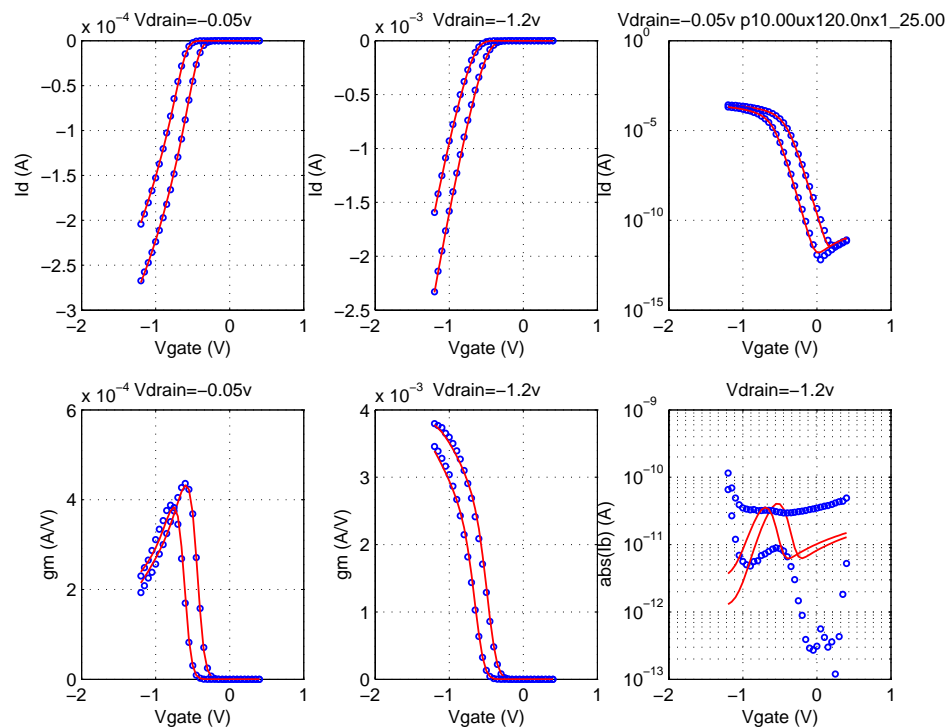


FIGURE 2.29 1p2v_PFET_0p15x10_idvd_25C

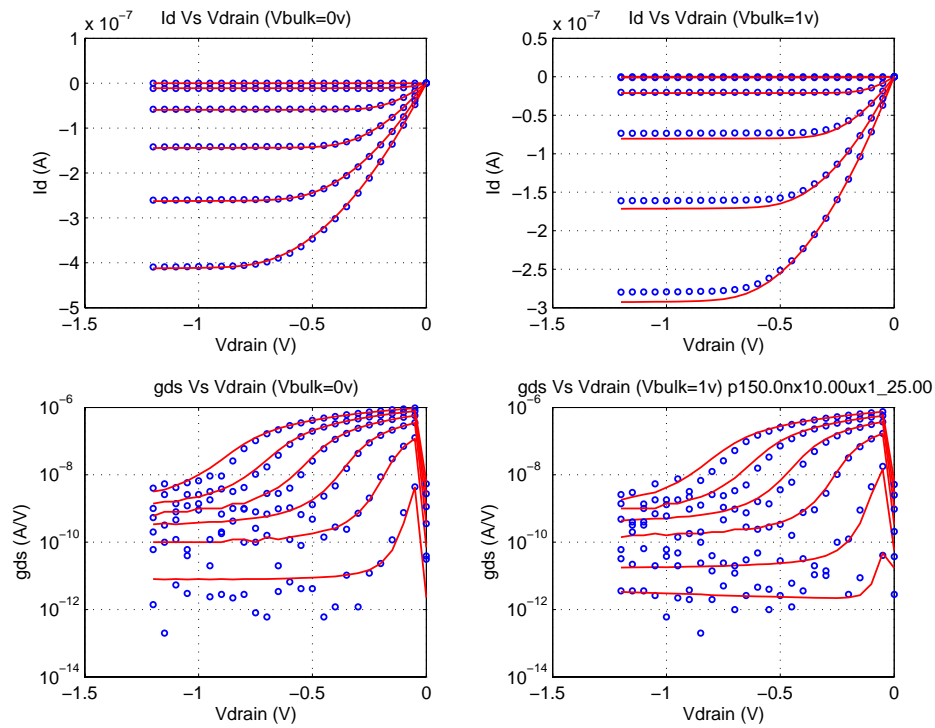


FIGURE 2.30 1p2v_PFET_0p22x10_idvg_25C

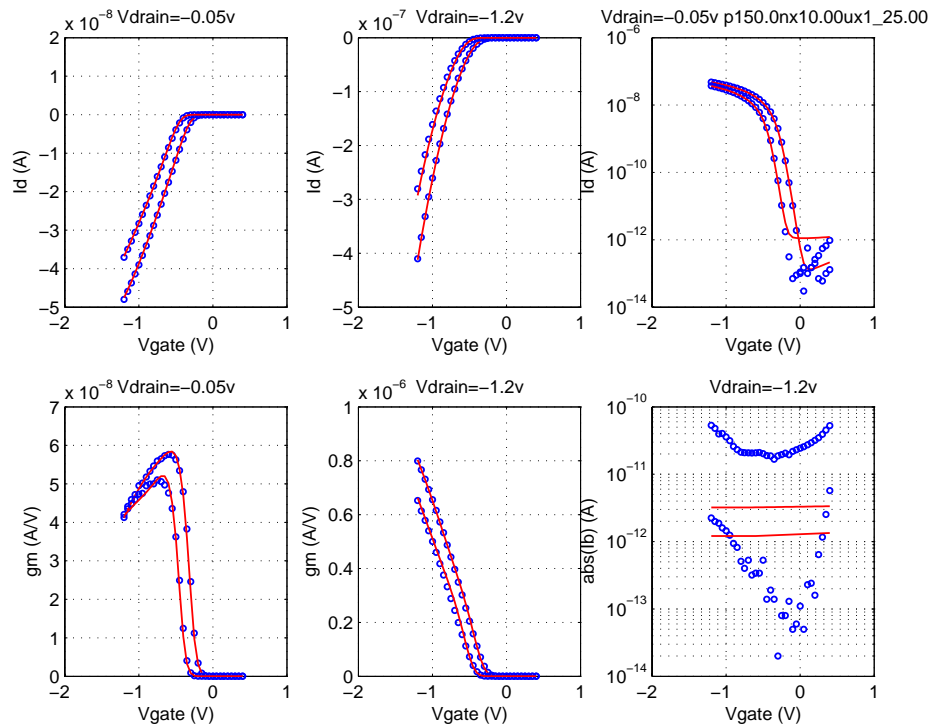


FIGURE 2.31 1p2v_PFET_0p15x0p12_idvd_25C

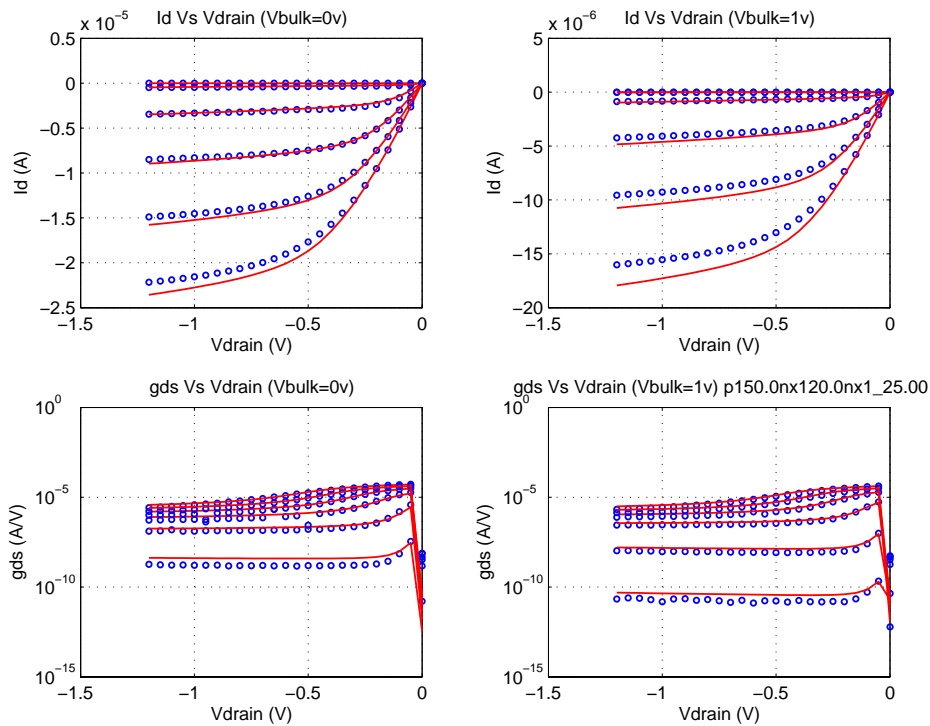


FIGURE 2.32 1p2v_PFET_0p15x0p12_idvg_25C

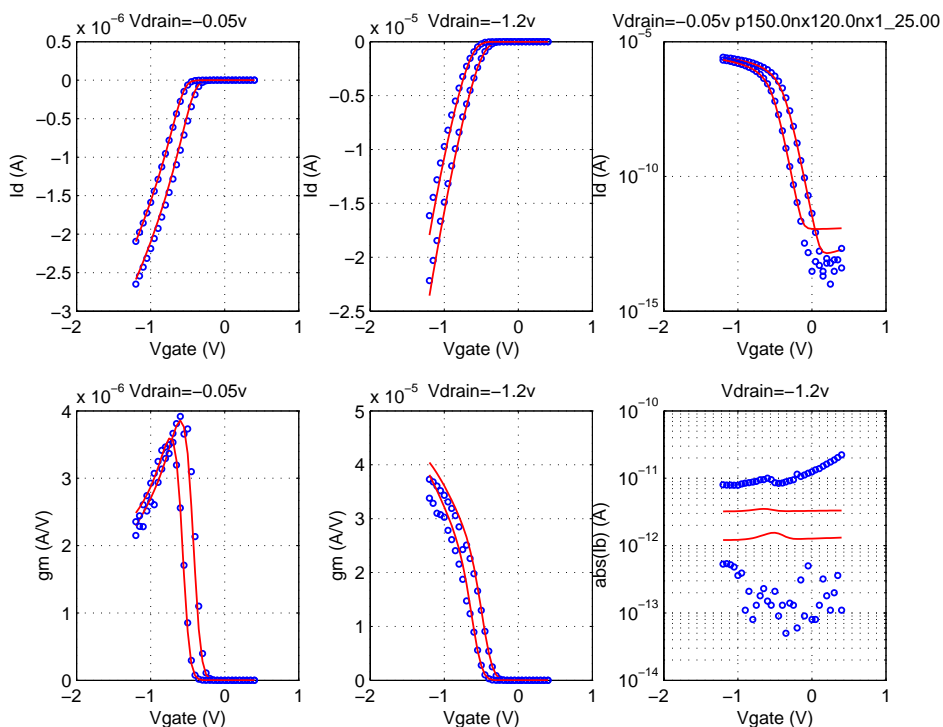


FIGURE 2.33 1p2v_PFET_0p5x0p12_idvd_25C

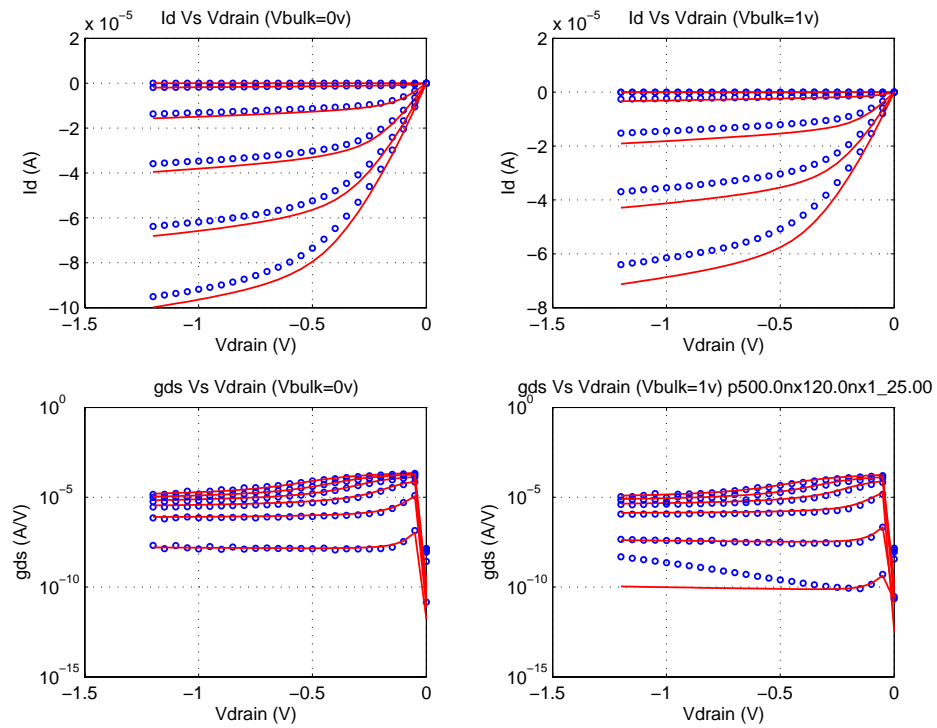


FIGURE 2.34 1p2v_PFET_0p5x0p12_idvg_25C

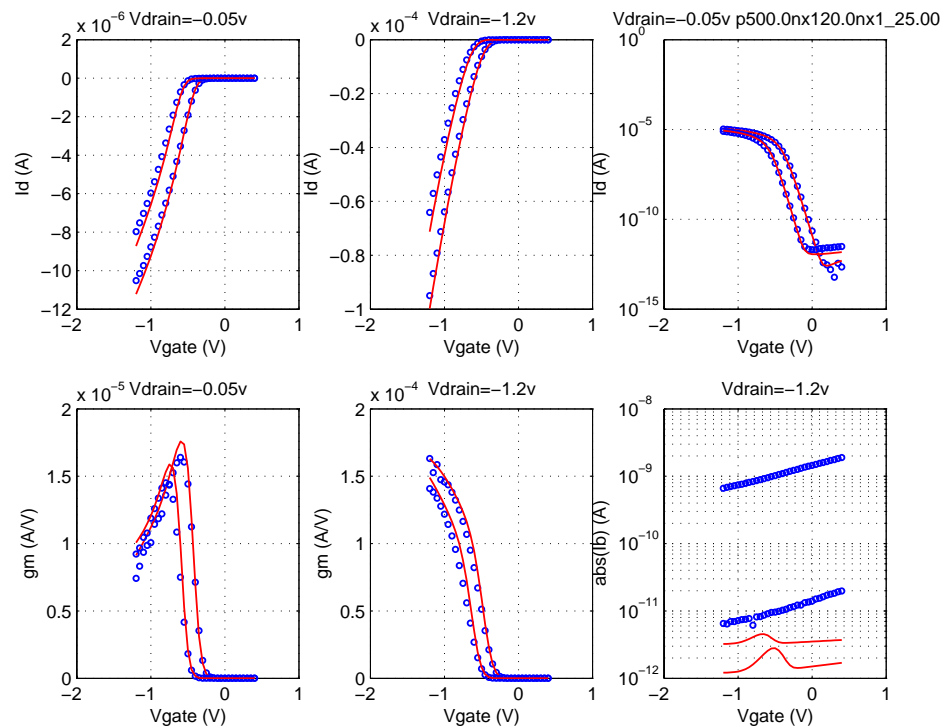


FIGURE 2.35 1p2v_PFET_10x0p18_idvd_25C

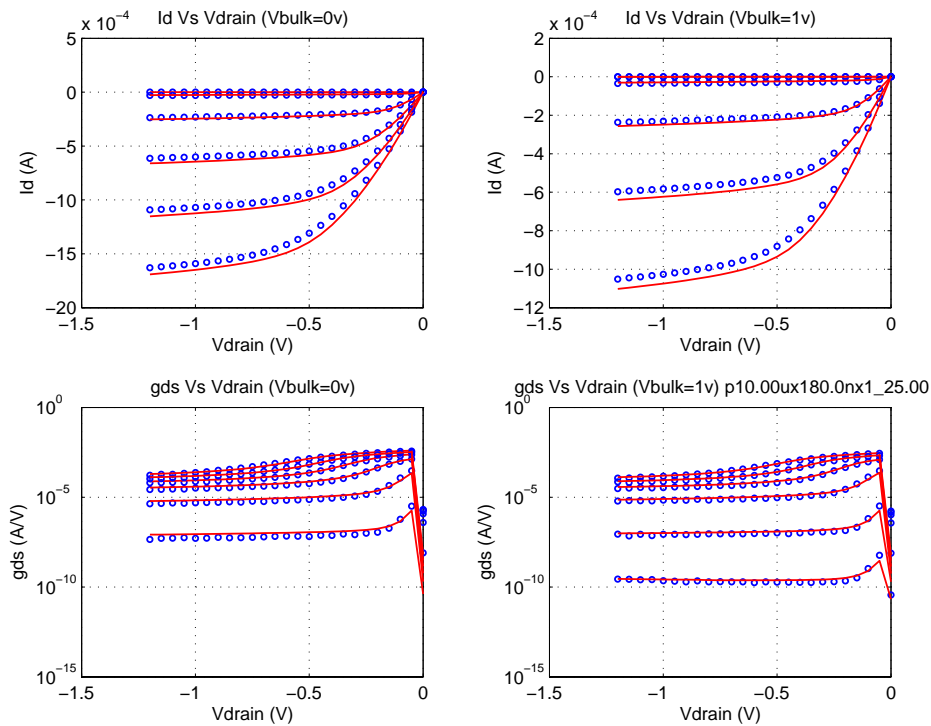


FIGURE 2.36 1p2v_PFET_10x0p18_idvg_25C

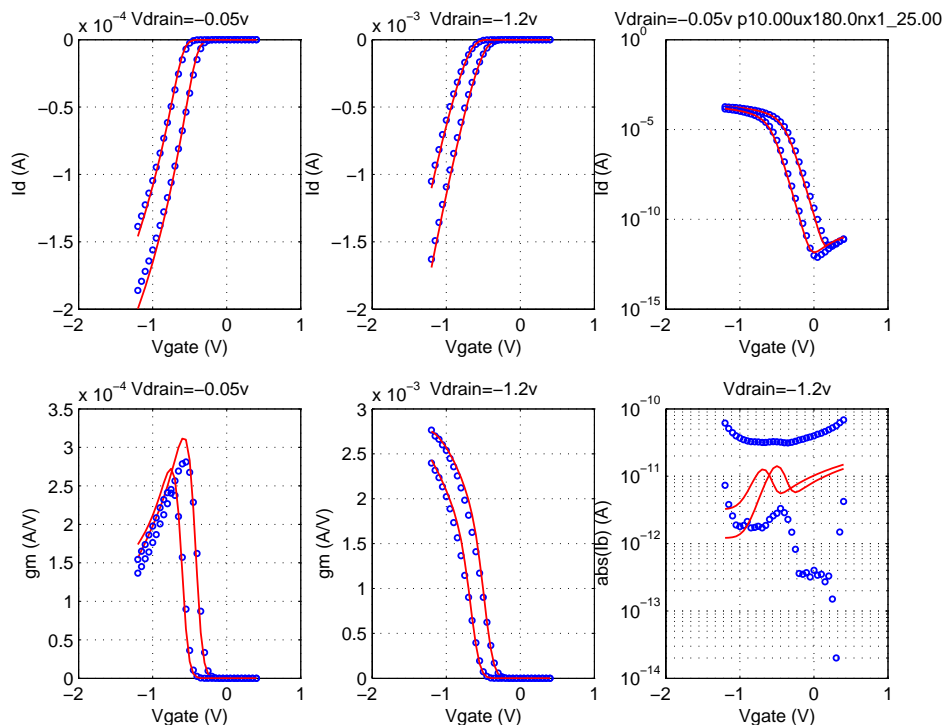


FIGURE 2.37 1p2v_PFET_10x0p12_idvd_-40C

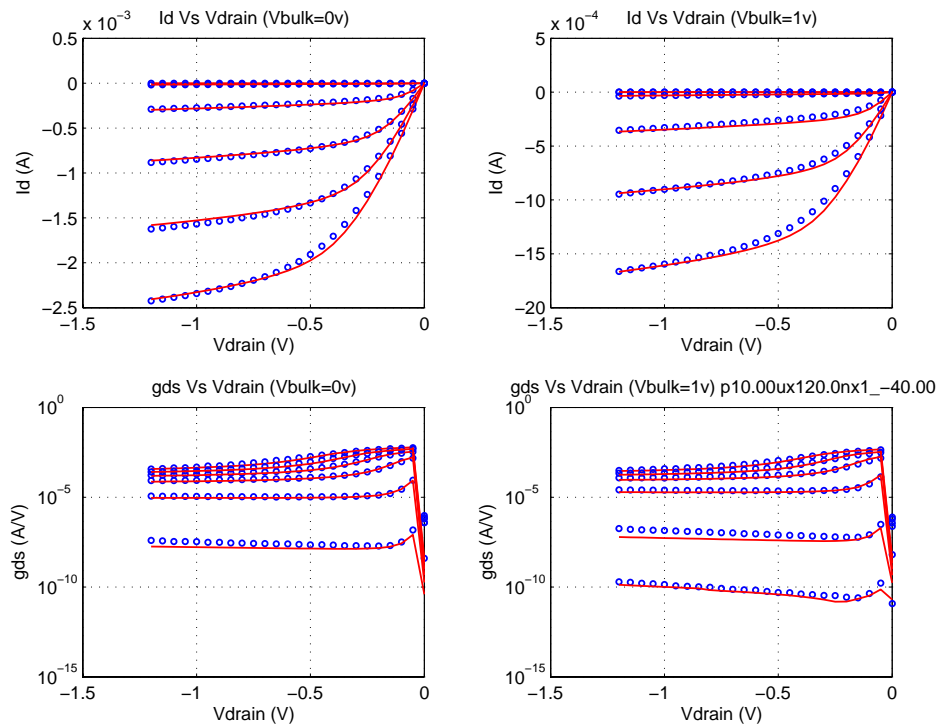


FIGURE 2.38 1p2v_PFET_10x0p12_idvg_-40C

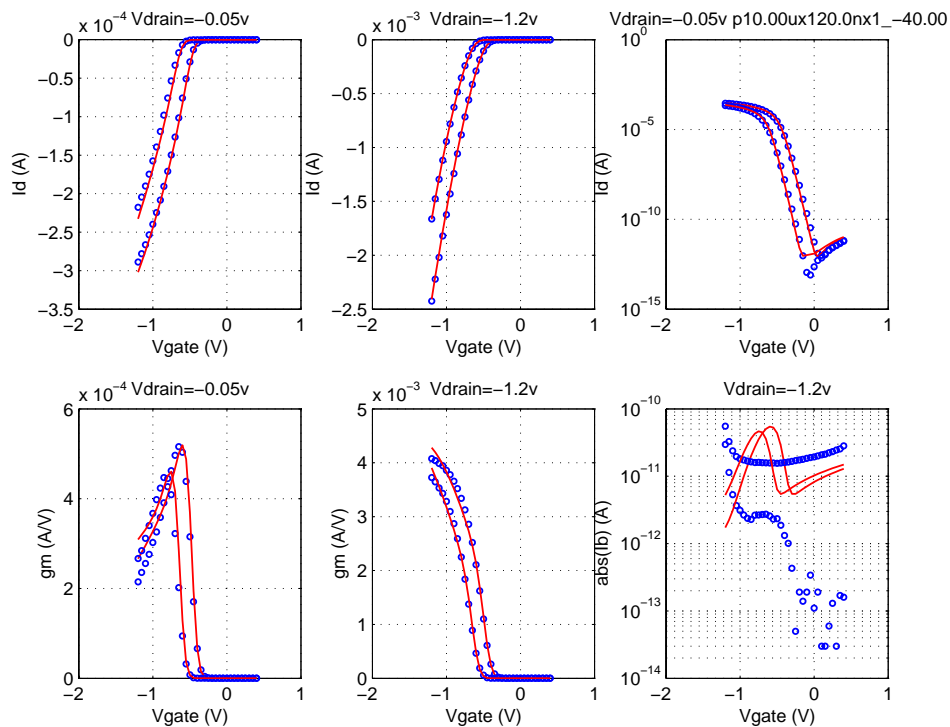


FIGURE 2.39 1p2v_PFET_10x0p12_idvd_125C

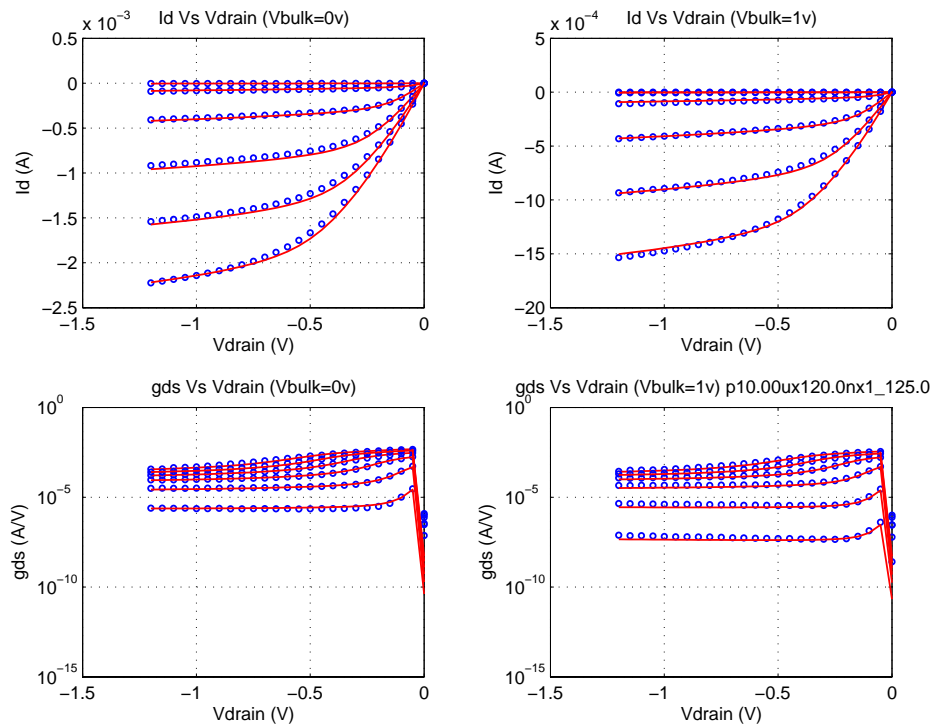


FIGURE 2.40 1p2v_PFET_10x0p12_idvg_125C

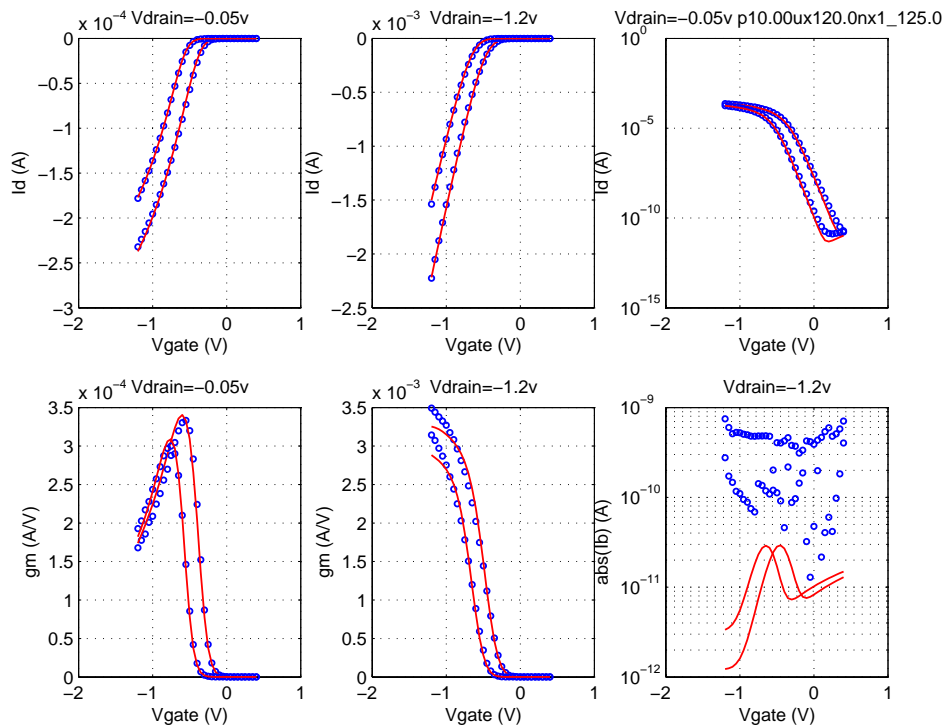
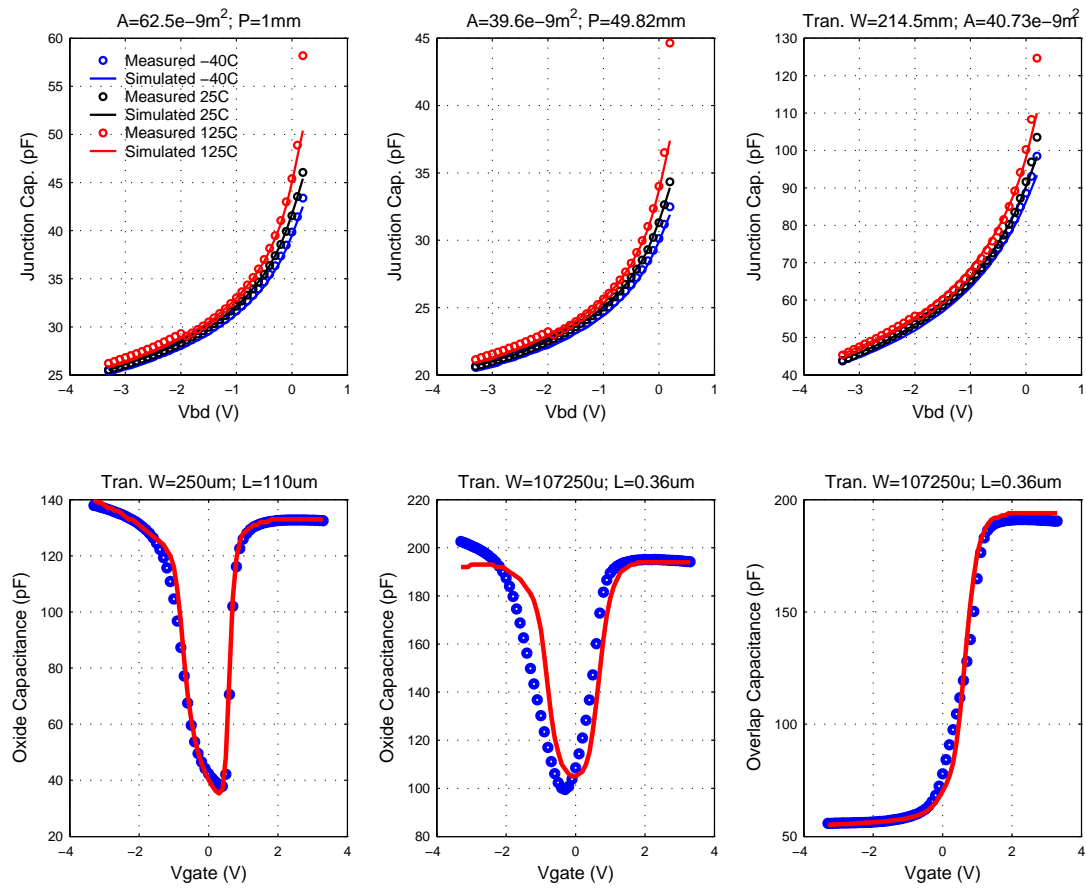


FIGURE 2.41 3p3_NFET_cv_25C



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FIGURE 2.42 3p3v_NFET_vtVsL_25C

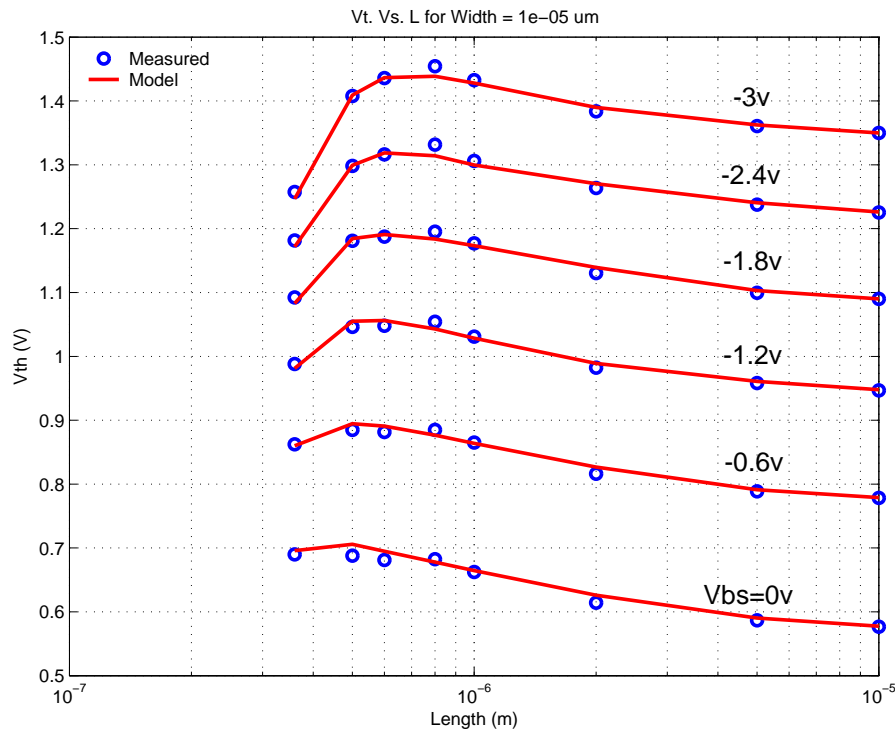


FIGURE 2.43 3p3v_NFET_vtVsW_25C

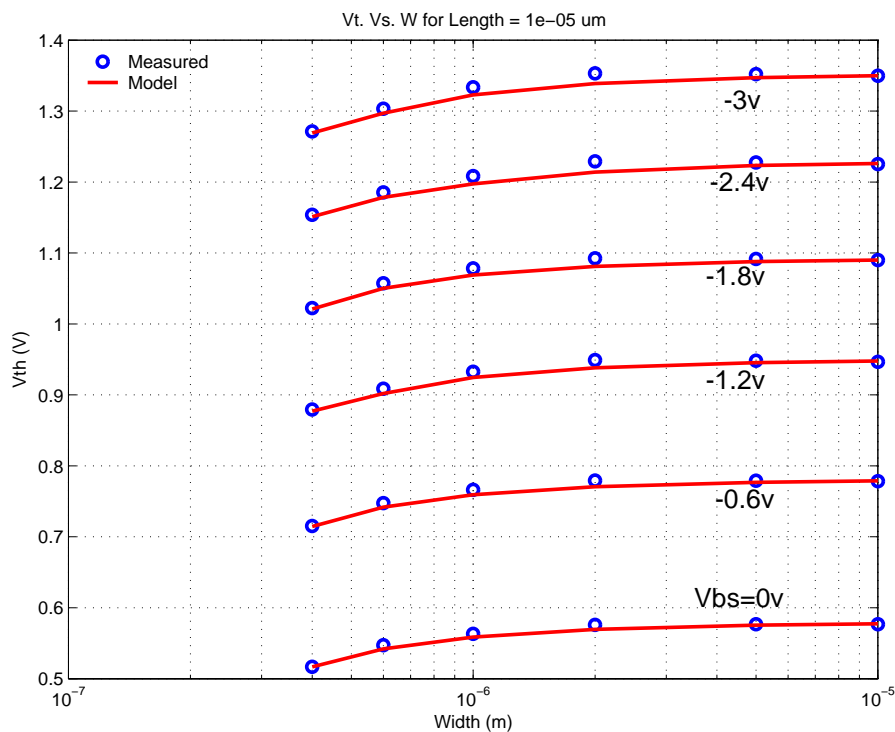


FIGURE 2.44 3p3v_NFET_10x10_idvd_25C

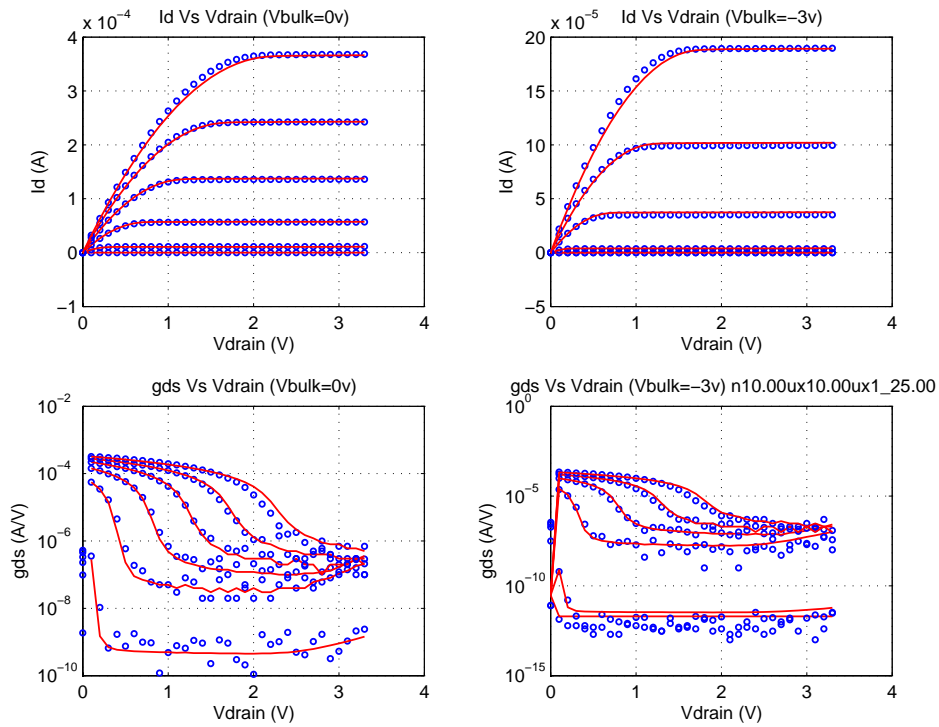


FIGURE 2.45 3p3v_NFET_10x10_idvg_25C

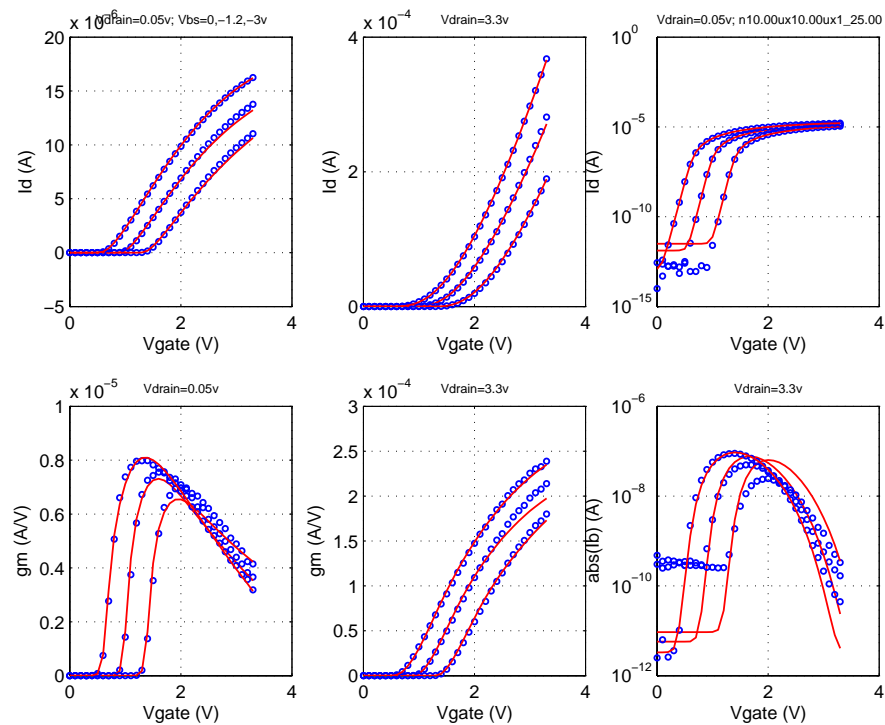


FIGURE 2.46 3p3v_NFET_10x0p36_idvd_25C

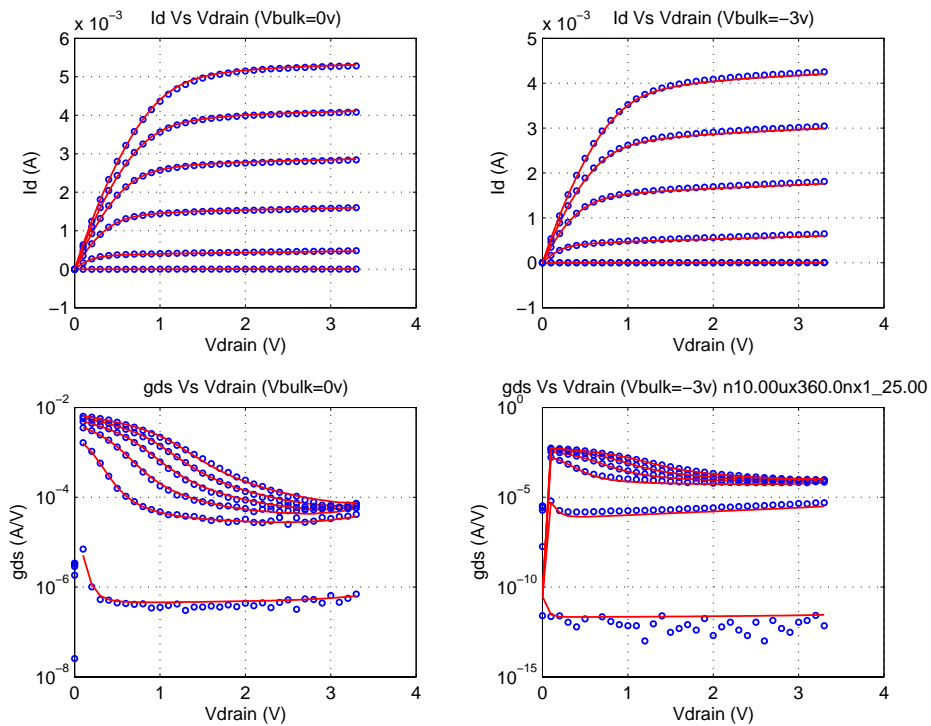


FIGURE 2.47 3p3v_NFET_10x0p36_idvg_25C

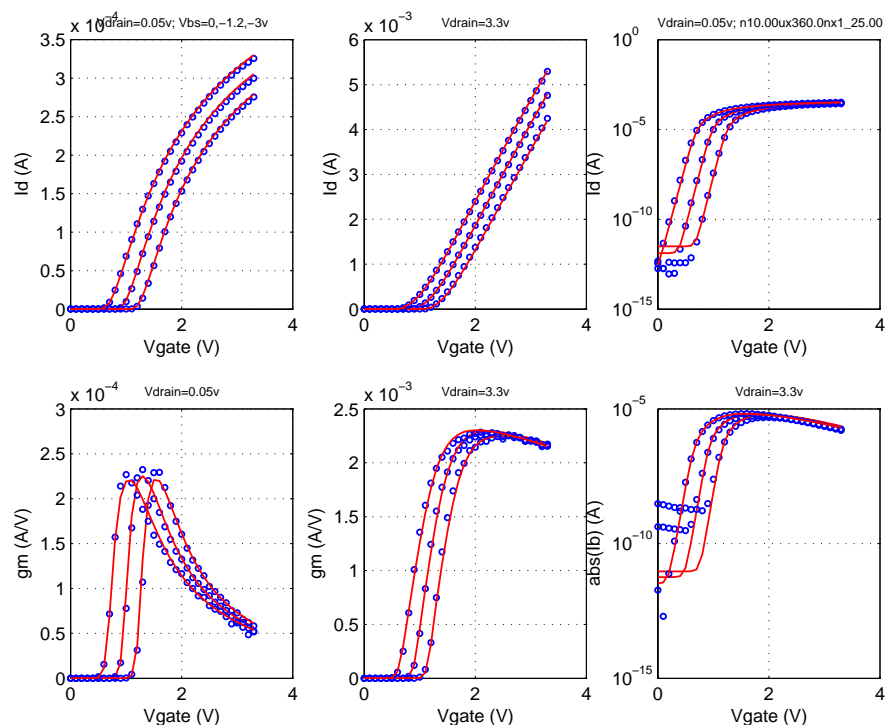


FIGURE 2.48 3p3v_NFET_0p4x10_idvd_25C

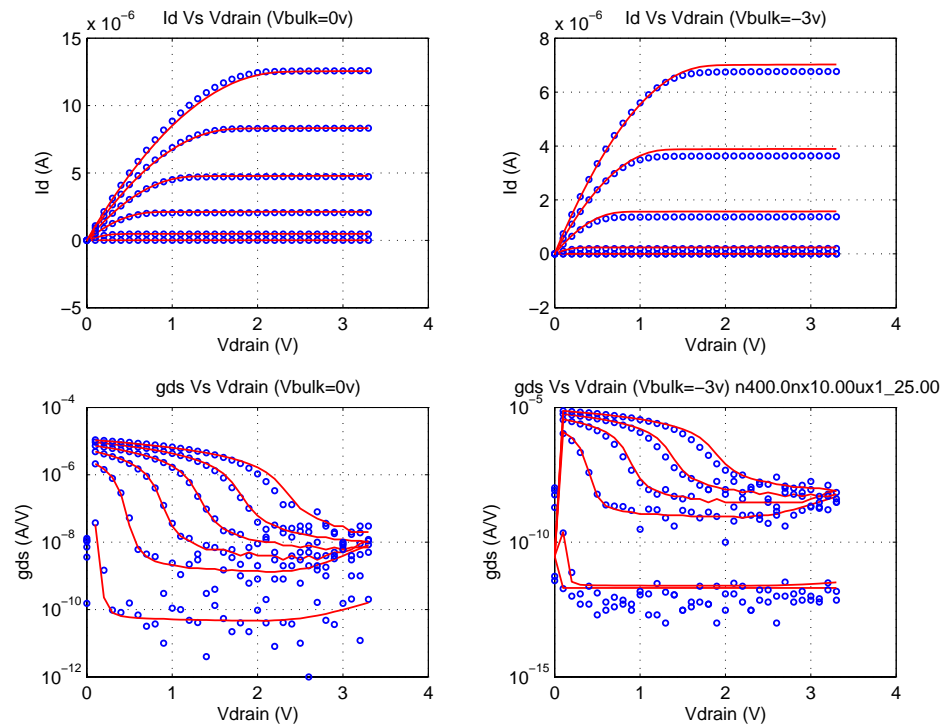


FIGURE 2.49 3p3v_NFET_0p4x10_idvg_25C

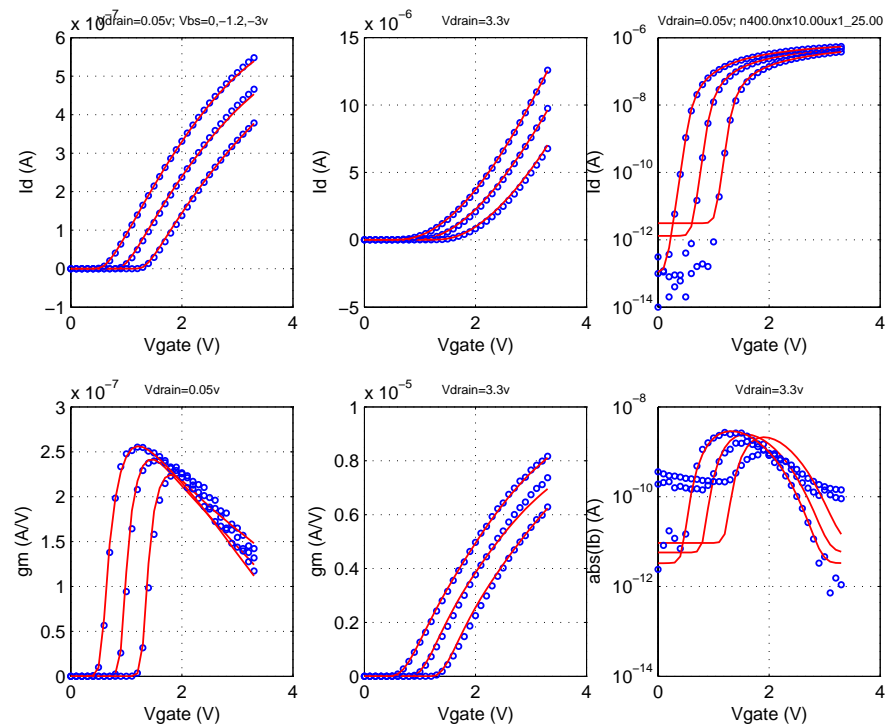


FIGURE 2.50 3p3v_NFET_0p4x0p36_idvg_25C

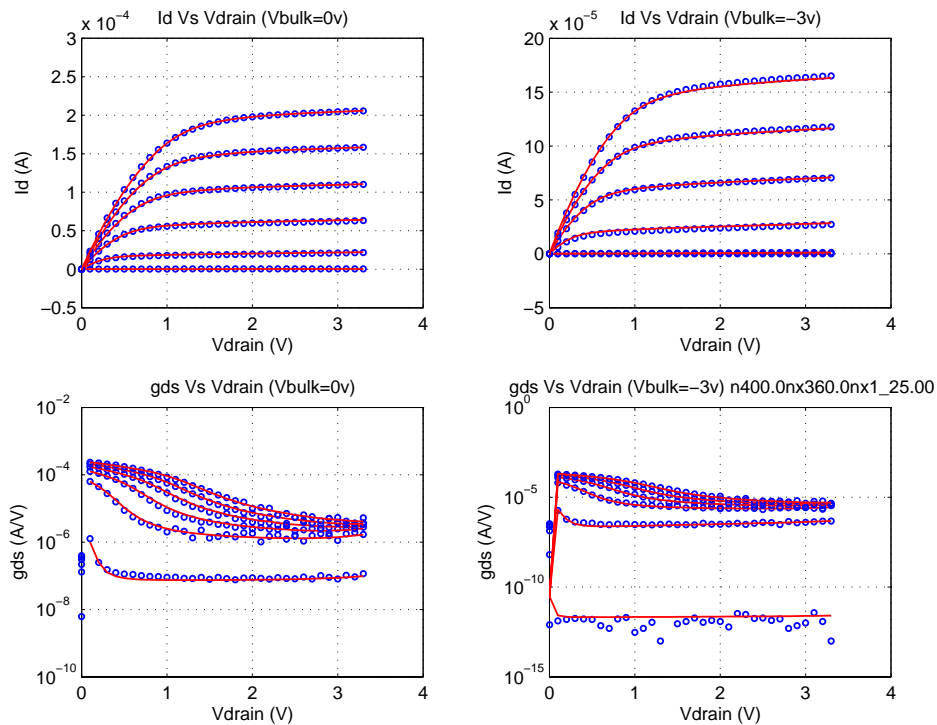


FIGURE 2.51 3p3v_NFET_0p4x0p36_idvd_25C

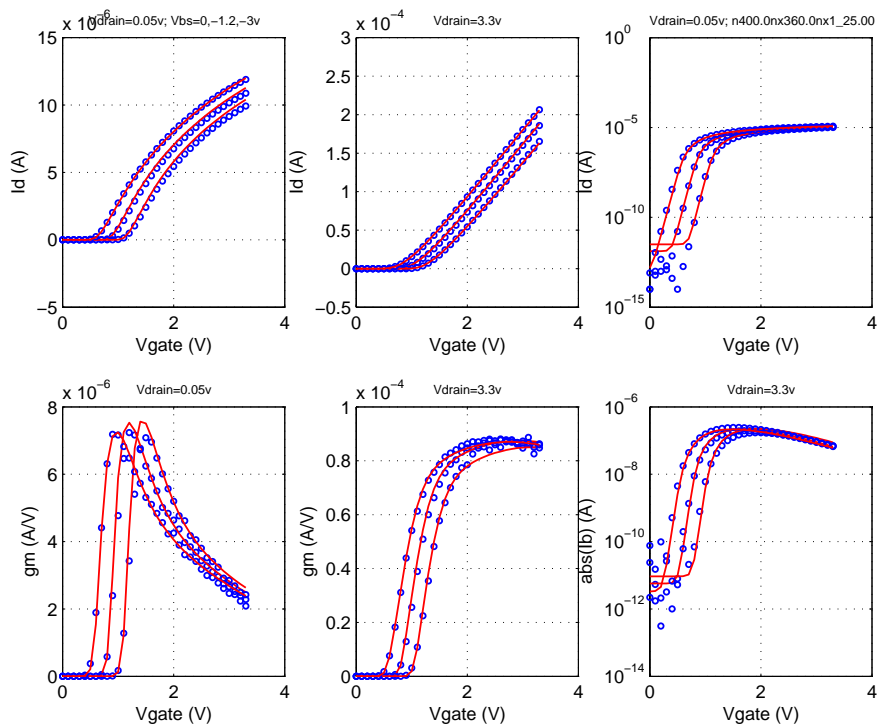


FIGURE 2.52 3p3v_NFET_0p6x0p36_idvd_25C

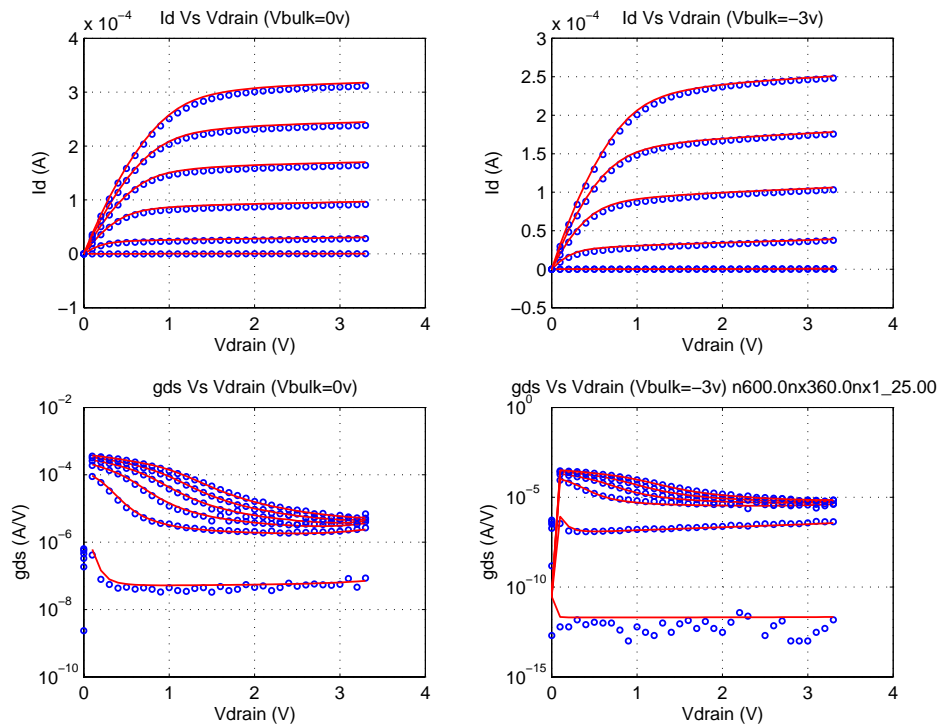


FIGURE 2.53 3p3v_NFET_0p6x0p36_idvg_25C

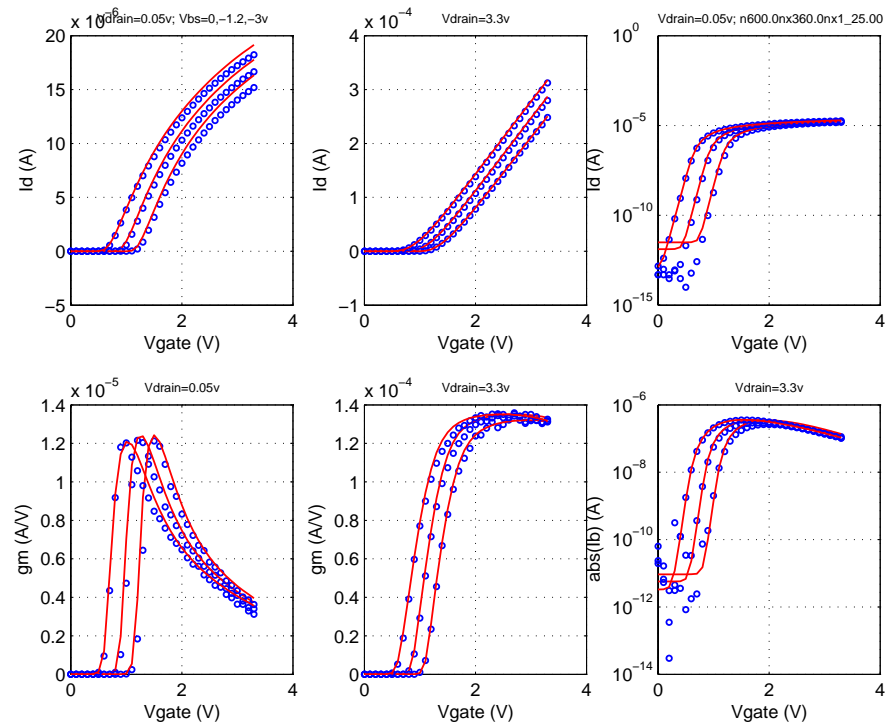


FIGURE 2.54 3p3v_NFET_10x0p5_idvd_25C

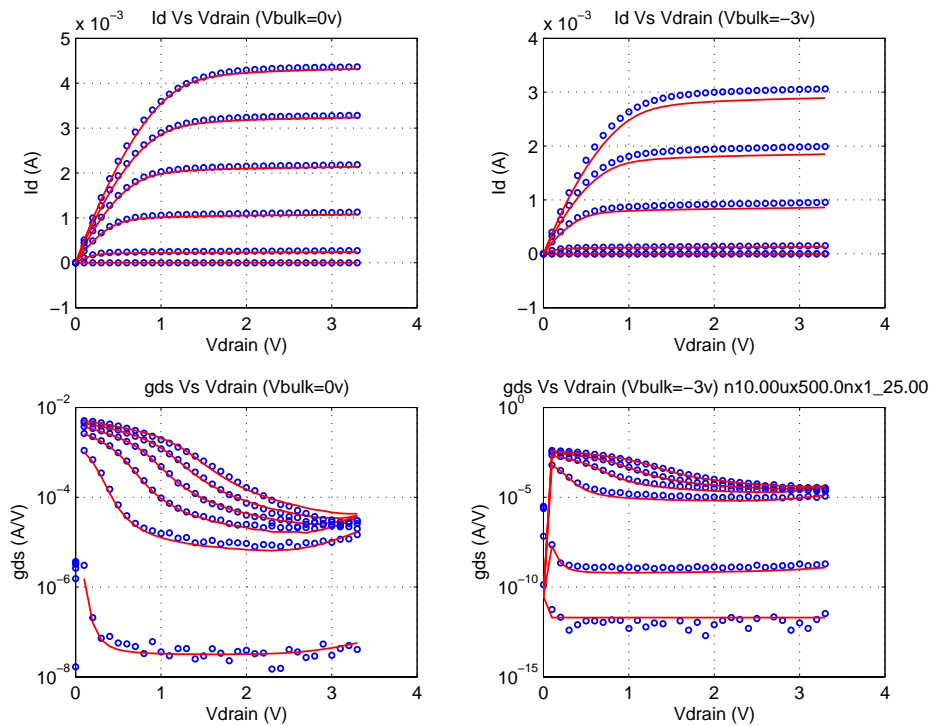


FIGURE 2.55 3p3v_NFET_10x0p5_idvg_25C

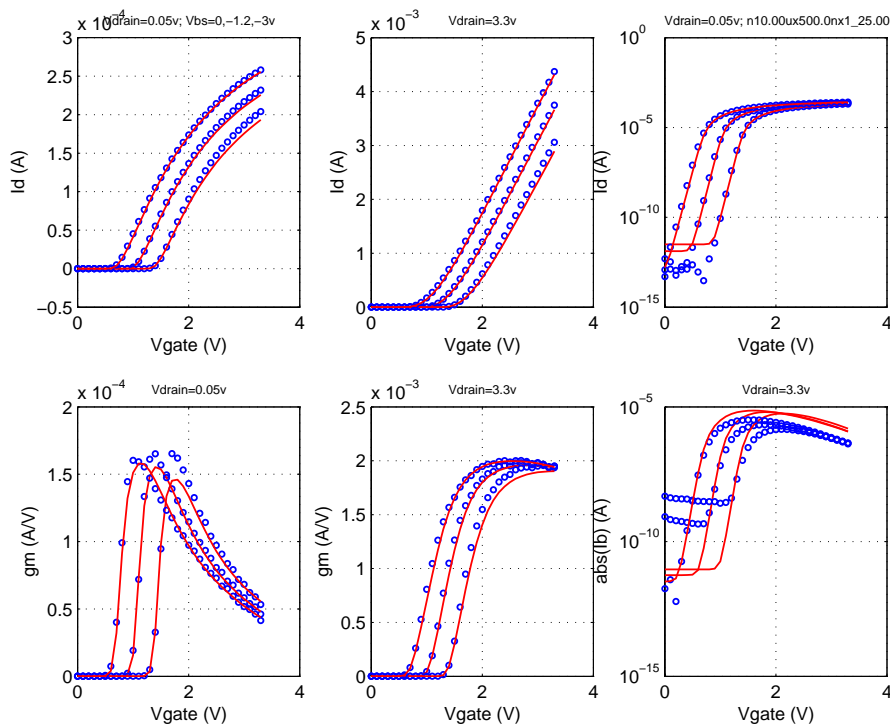


FIGURE 2.56 3p3v_NFET_10x0p36_idvd_-40C

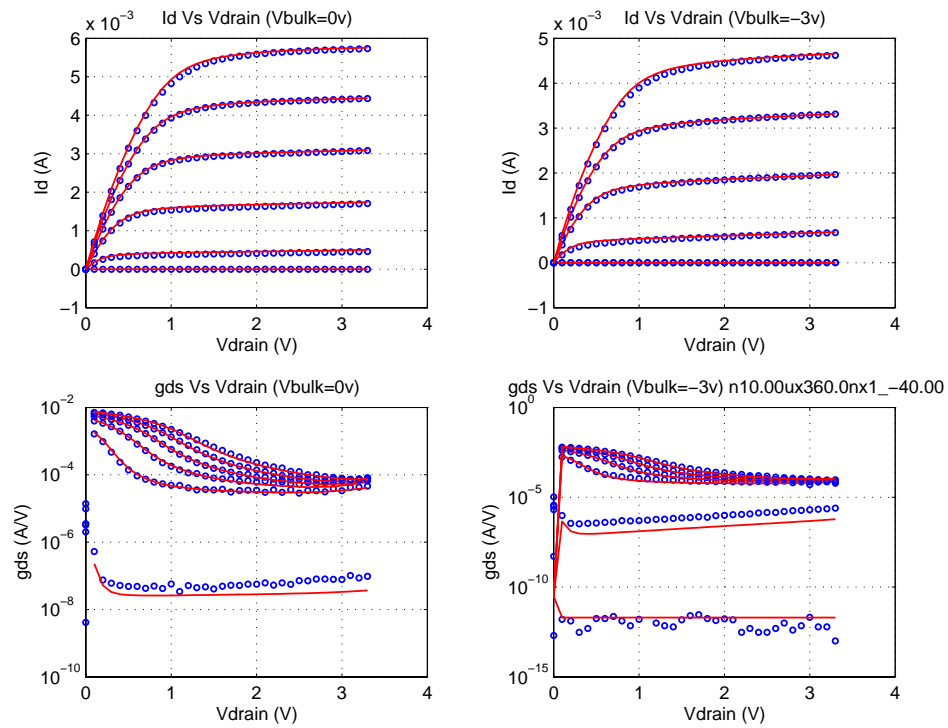


FIGURE 2.57 3p3v_NFET_10x0p36_idvg_-40C

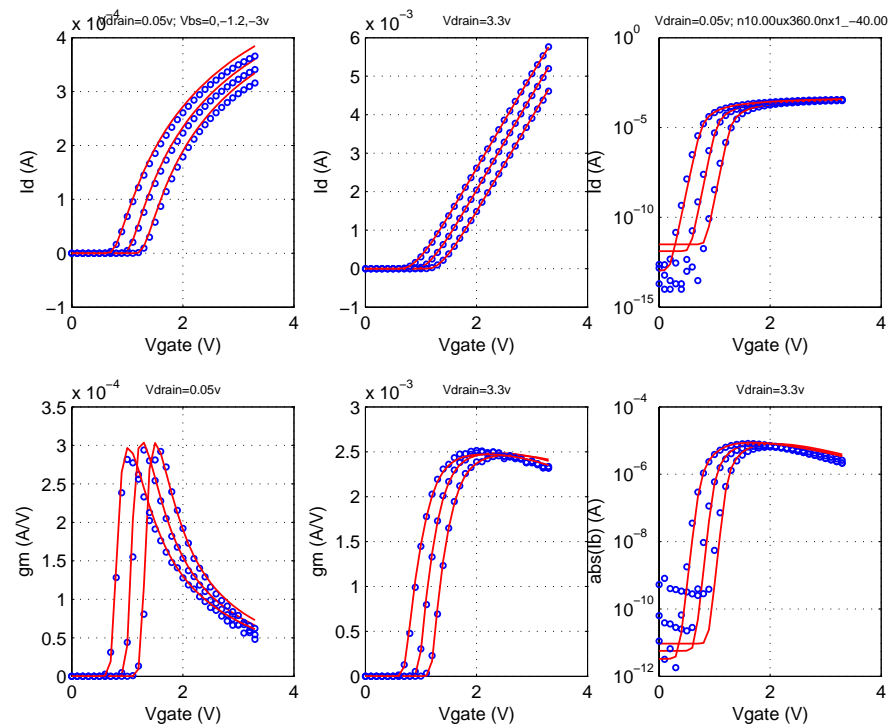


FIGURE 2.58 3p3v_NFET_10x0p36_idvg_125C

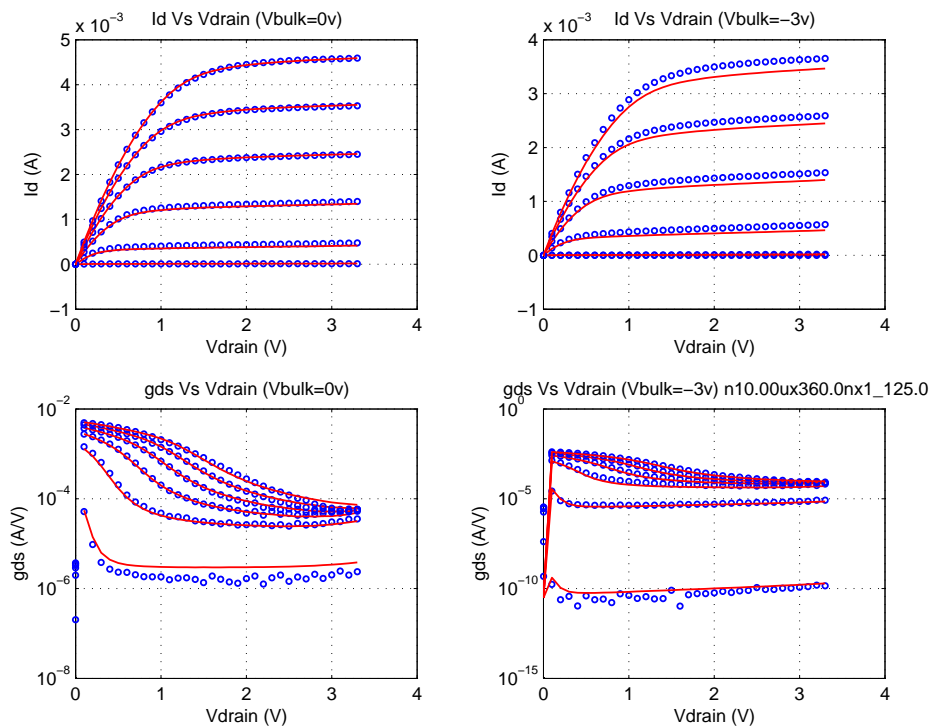


FIGURE 2.59 3p3v_NFET_10x0p36_idvd_125C

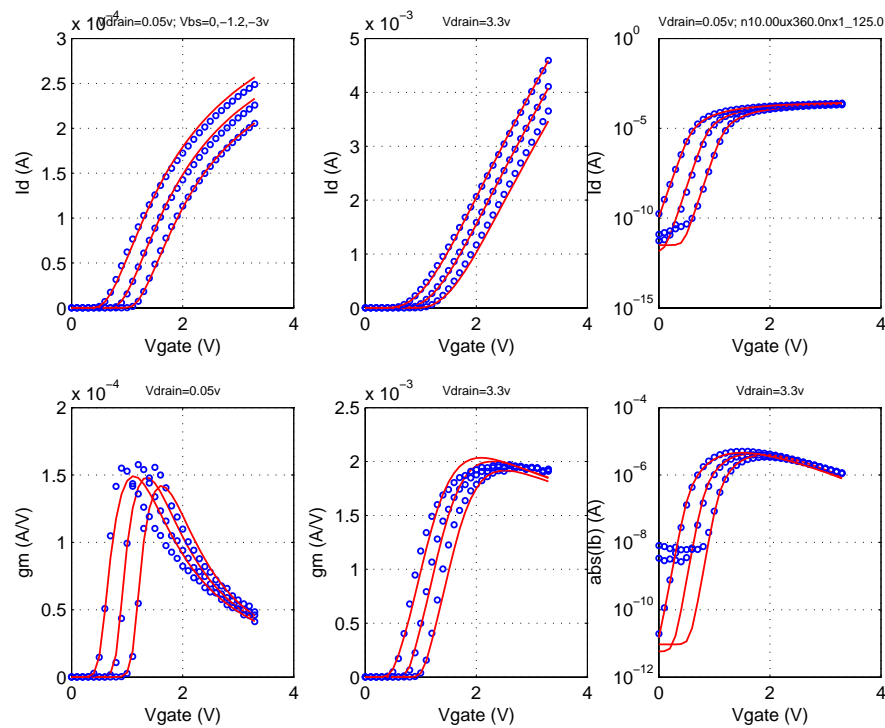


FIGURE 2.60 3p3_PFET_cv_25C

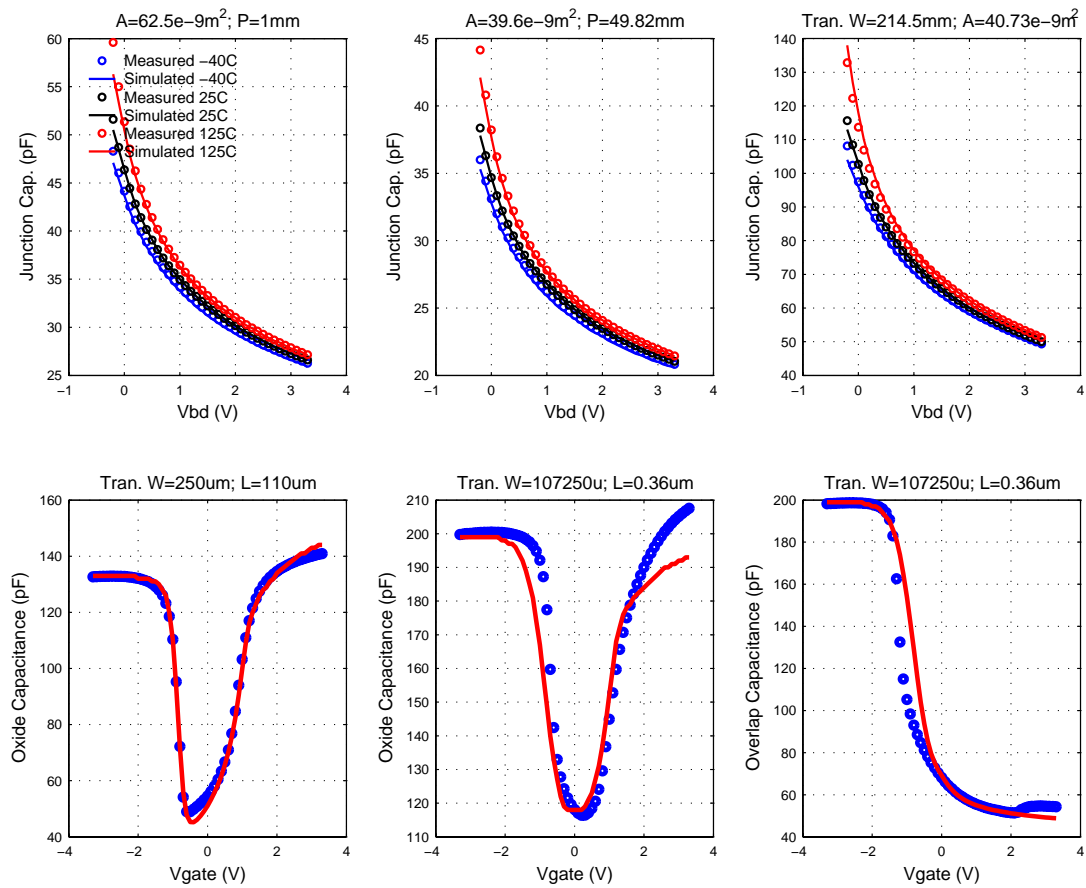


FIGURE 2.61 3p3v_PFET_vtVsL_25C

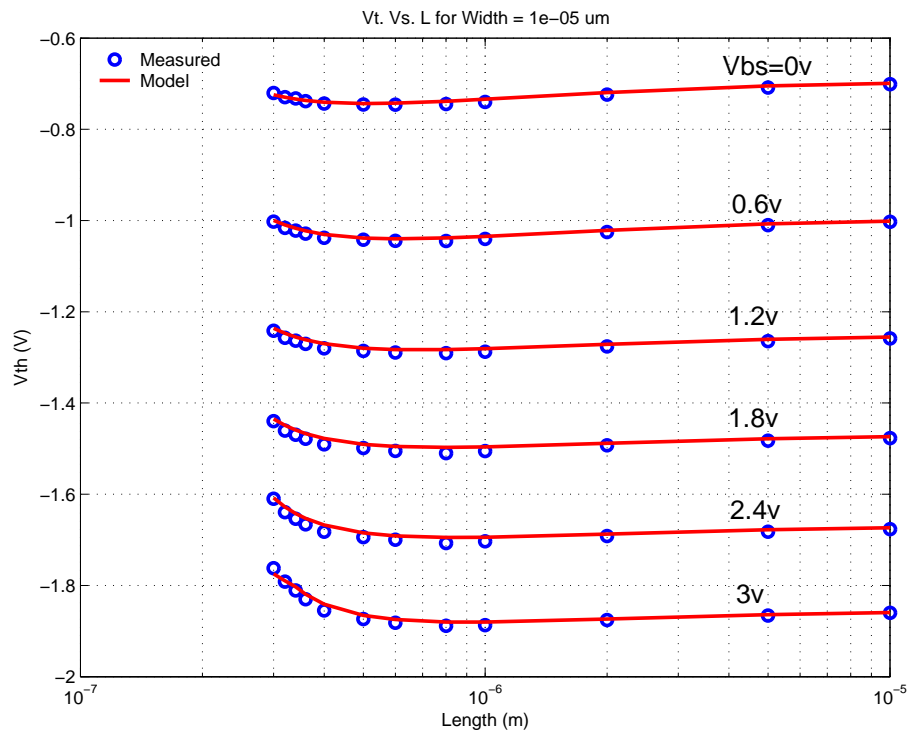


FIGURE 2.62 3p3v_PFET_vtVsW_25C

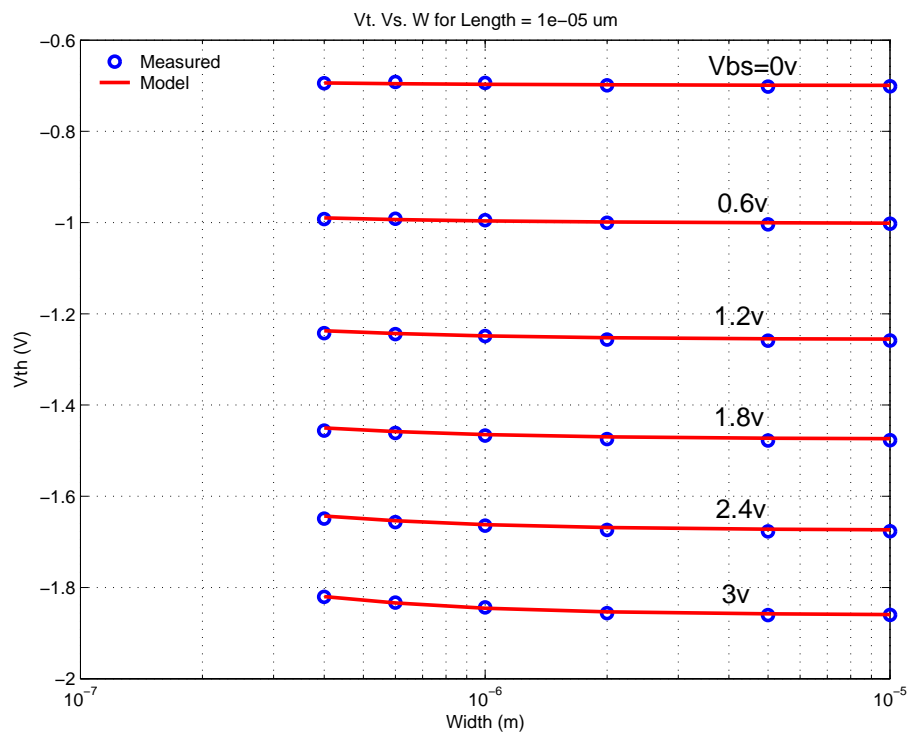


FIGURE 2.63 3p3v_PFET_10x10_idvd_25C

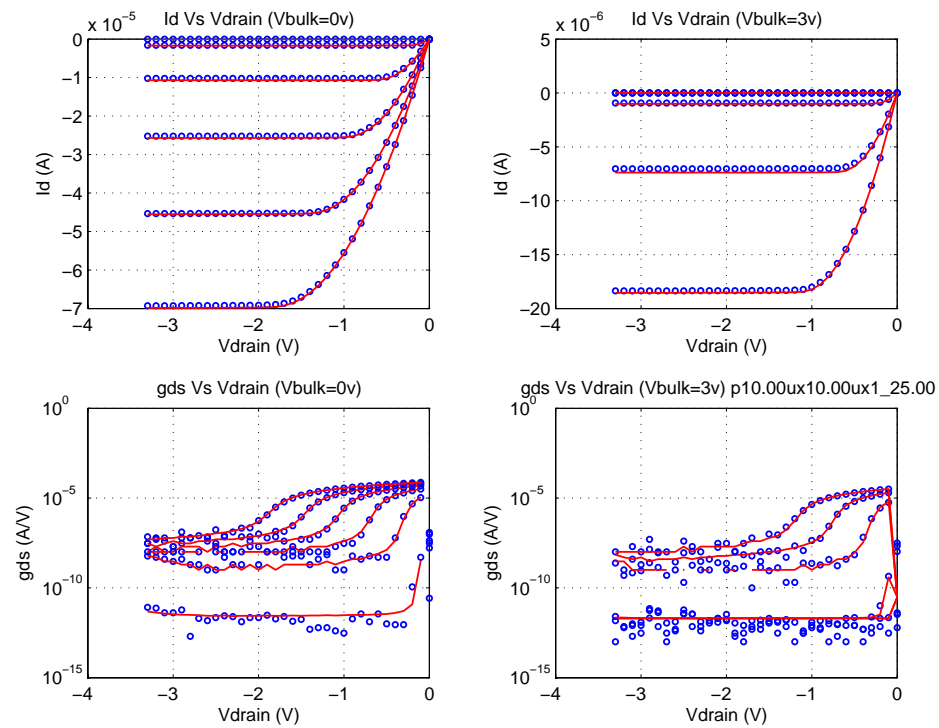


FIGURE 2.64 3p3v_PFET_10x10_idvg_25C

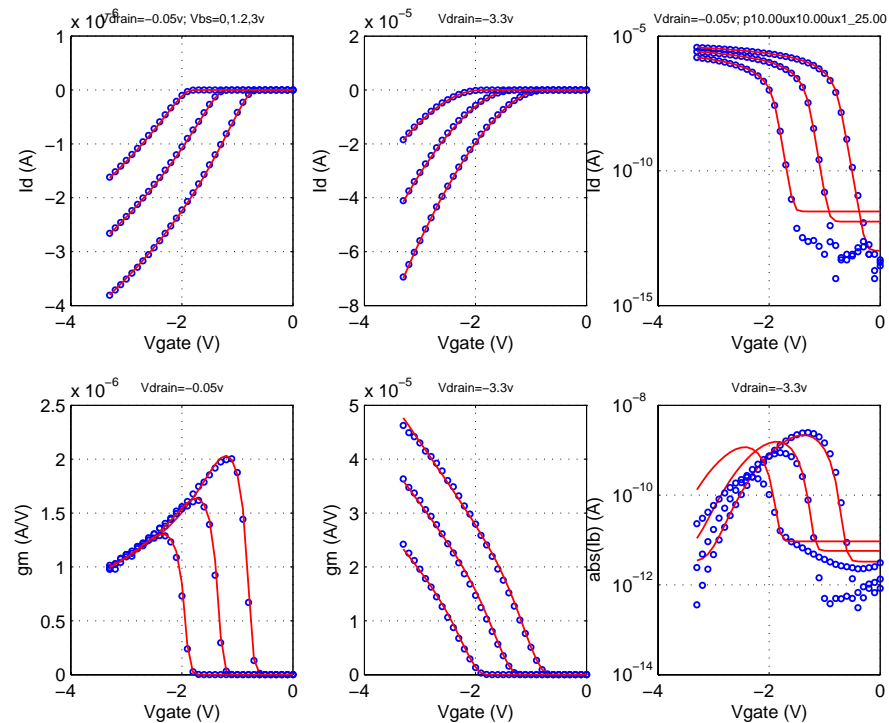


FIGURE 2.65 3p3v_PFET_10x0p3_idvd_25C

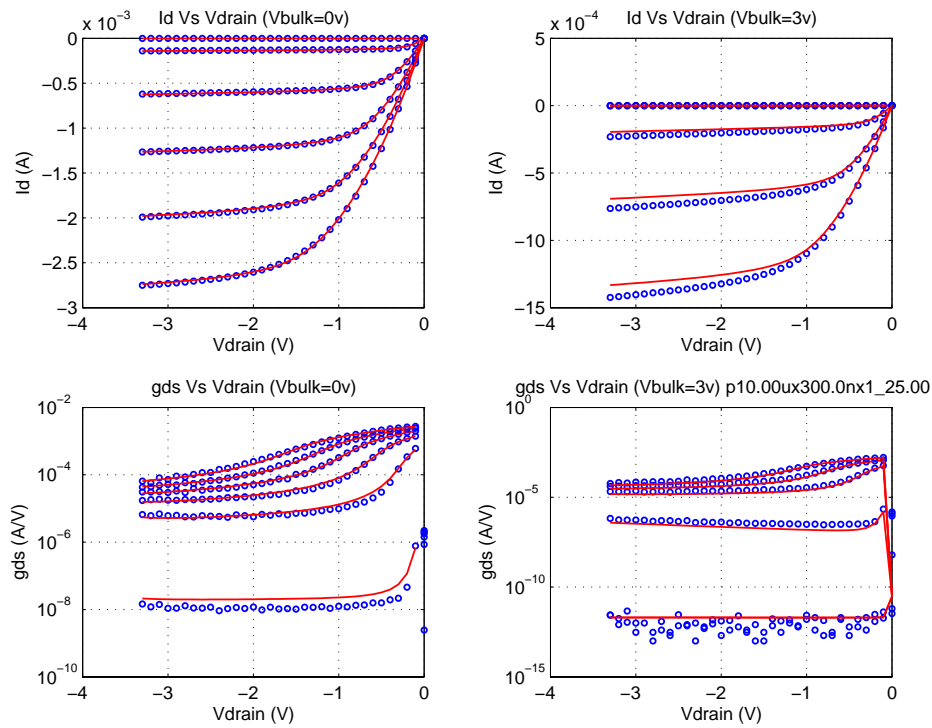


FIGURE 2.66 3p3v_PFET_10x0p3_idvg_25C

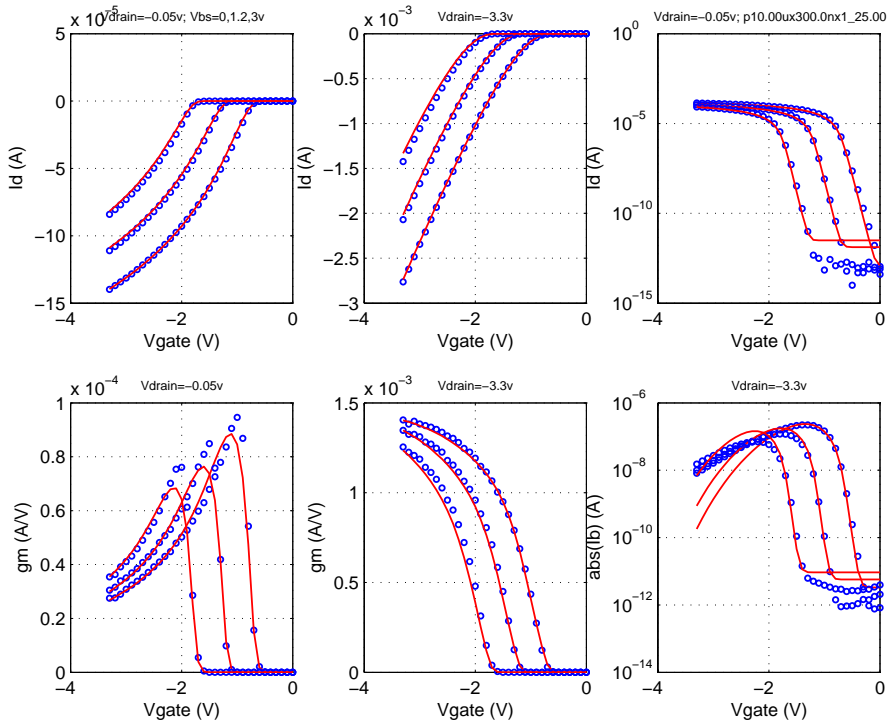


FIGURE 2.67 3p3v_PFET_0p4x10_idvd_25C

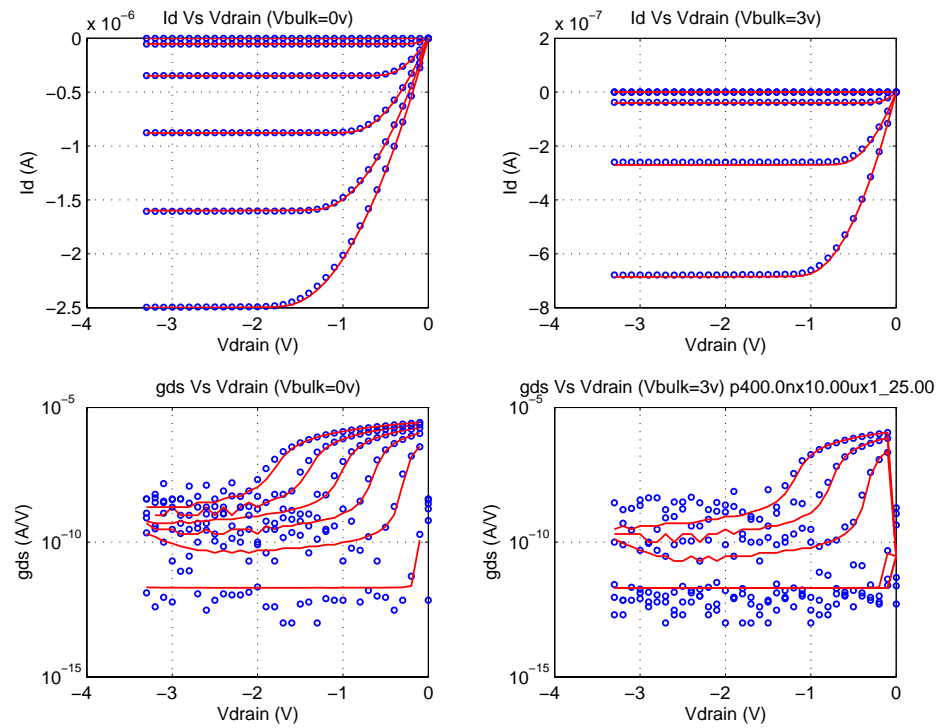


FIGURE 2.68 3p3v_PFET_0p4x10_idvg_25C

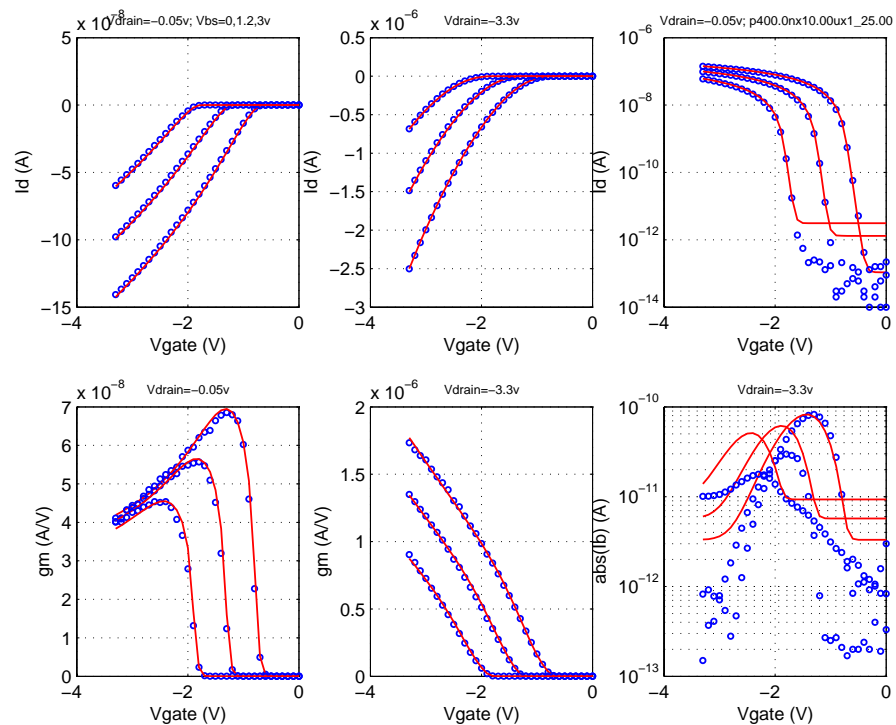


FIGURE 2.69 3p3v_PFET_0p4x0p3_idvd_25C

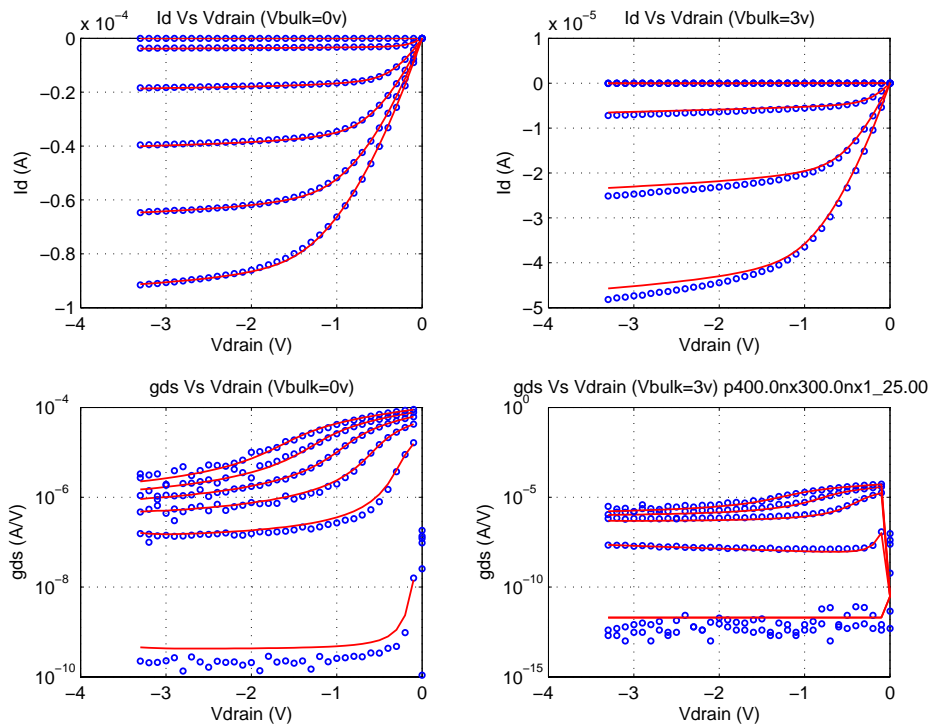


FIGURE 2.70 3p3v_PFET_0p4x0p3_idvg_25C

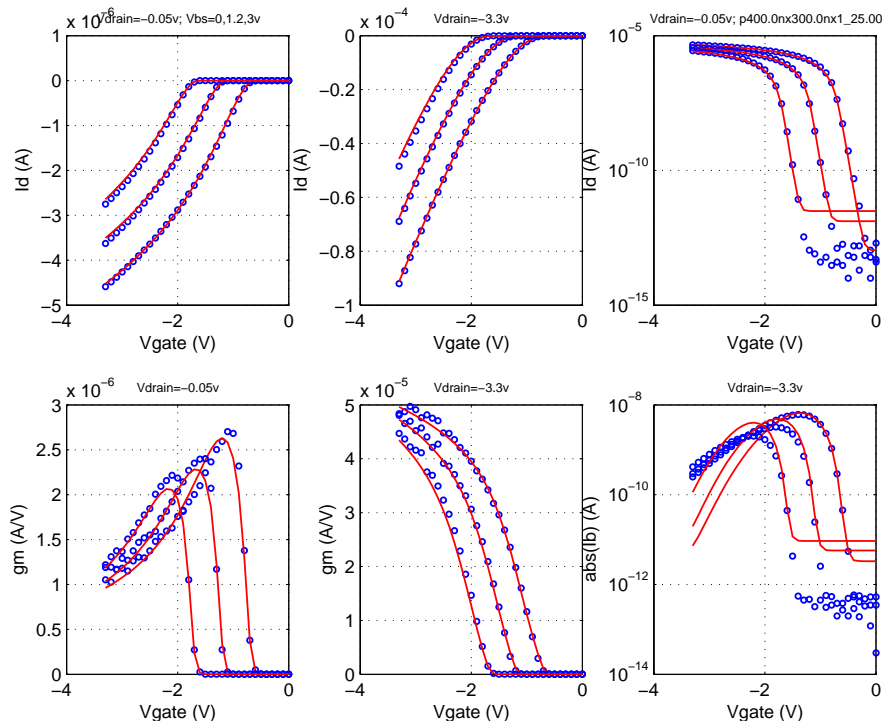


FIGURE 2.71 3p3v_PFET_0p6x0p3_idvd_25C

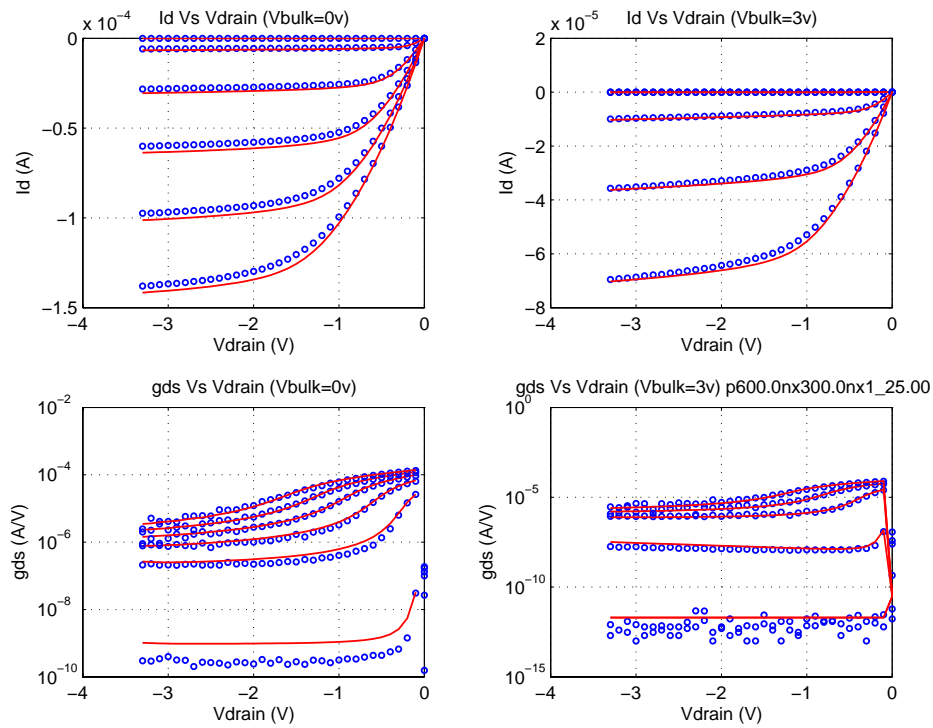


FIGURE 2.72 3p3v_PFET_0p6x0p3_idvg_25C

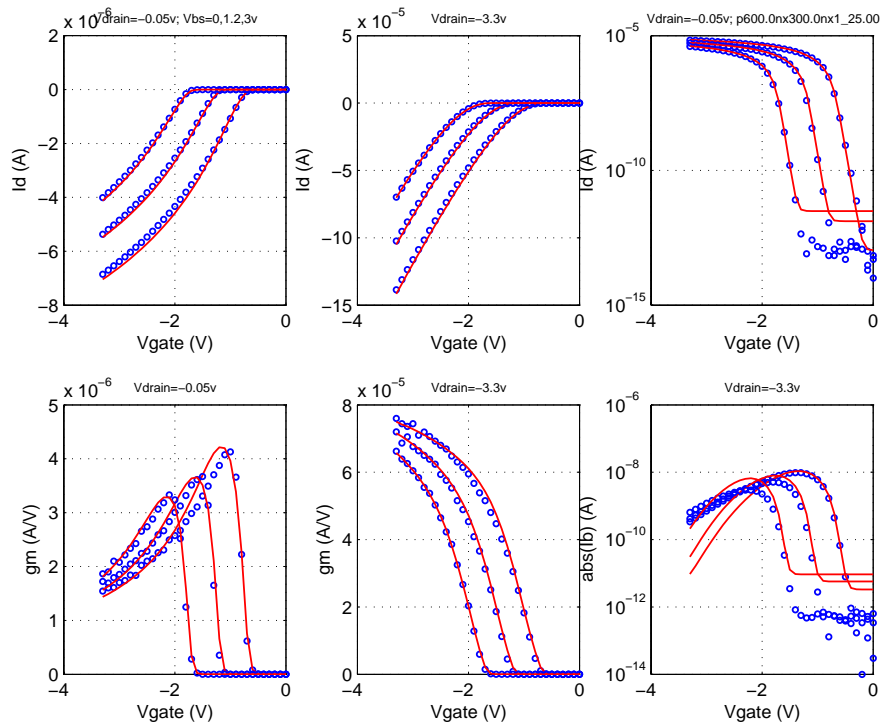


FIGURE 2.73 3p3v_PFET_10x0p5_idvd_25C

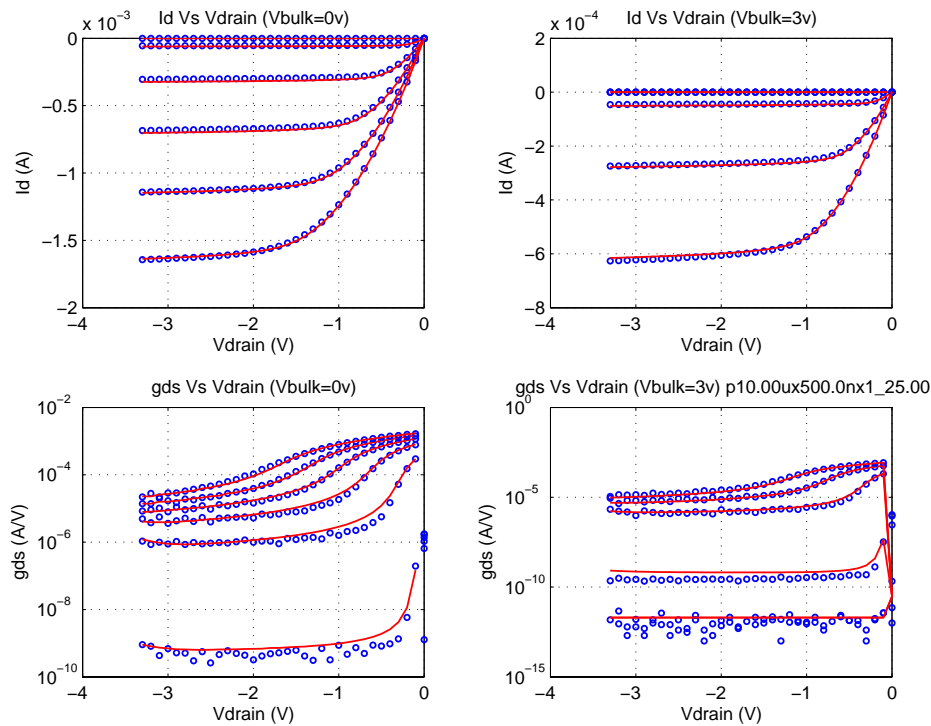


FIGURE 2.74 3p3v_PFET_10x0p5_idvg_25C

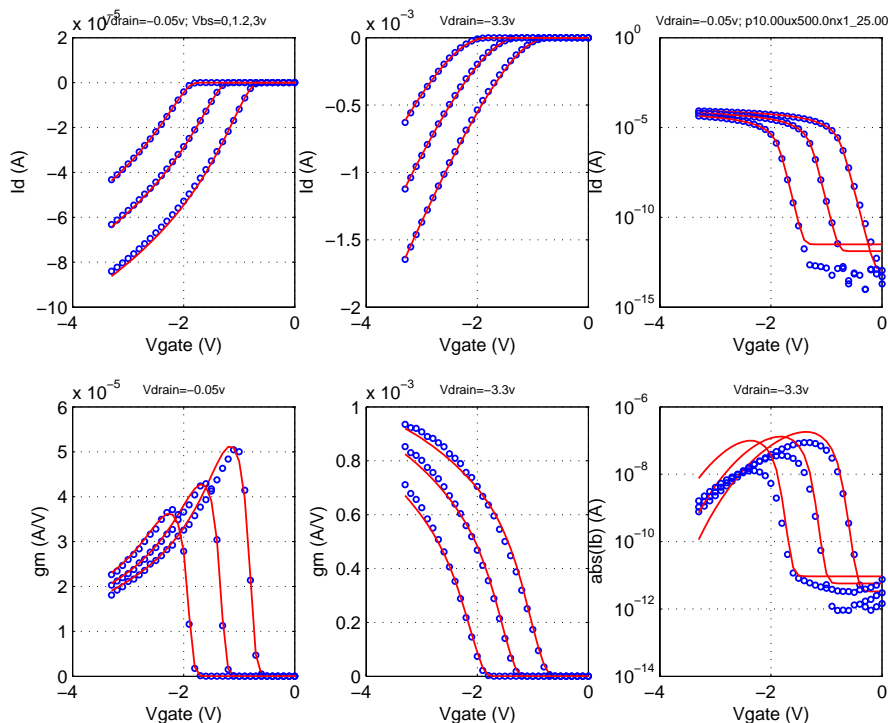


FIGURE 2.75 3p3v_PFET_10x0p3_idvd_-40C

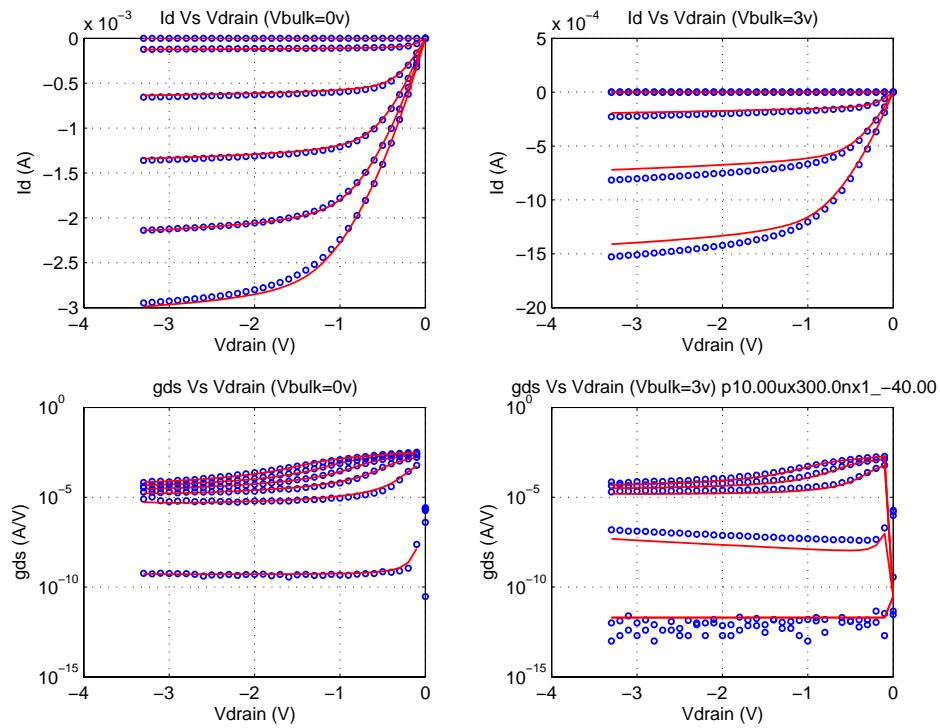


FIGURE 2.76 3p3v_PFET_10x0p3_idvg_-40C

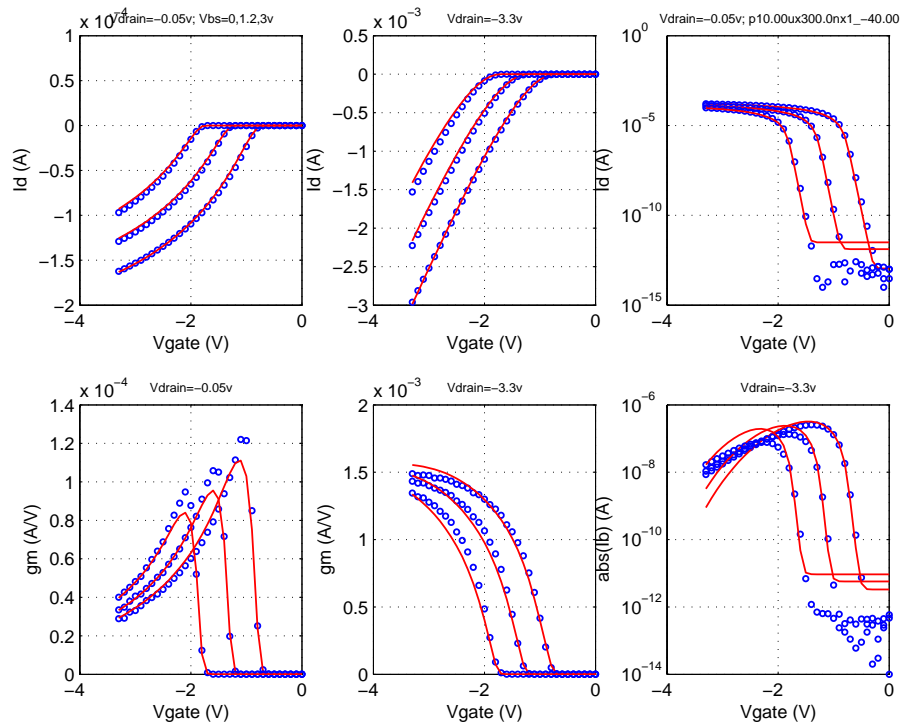


FIGURE 2.77 3p3v_PFET_10x0p3_idvd_125C

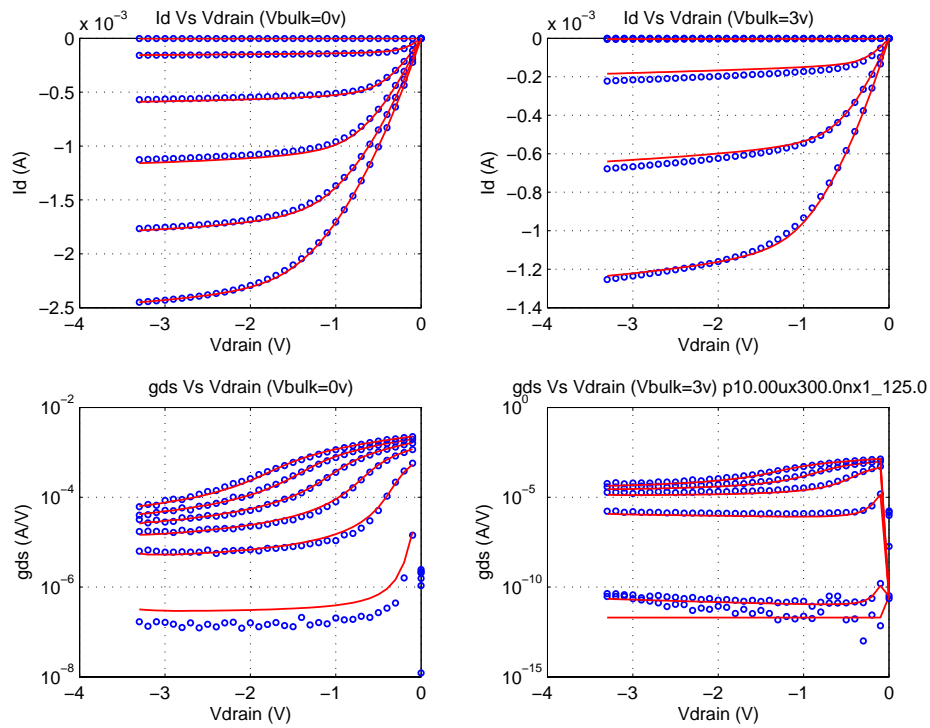
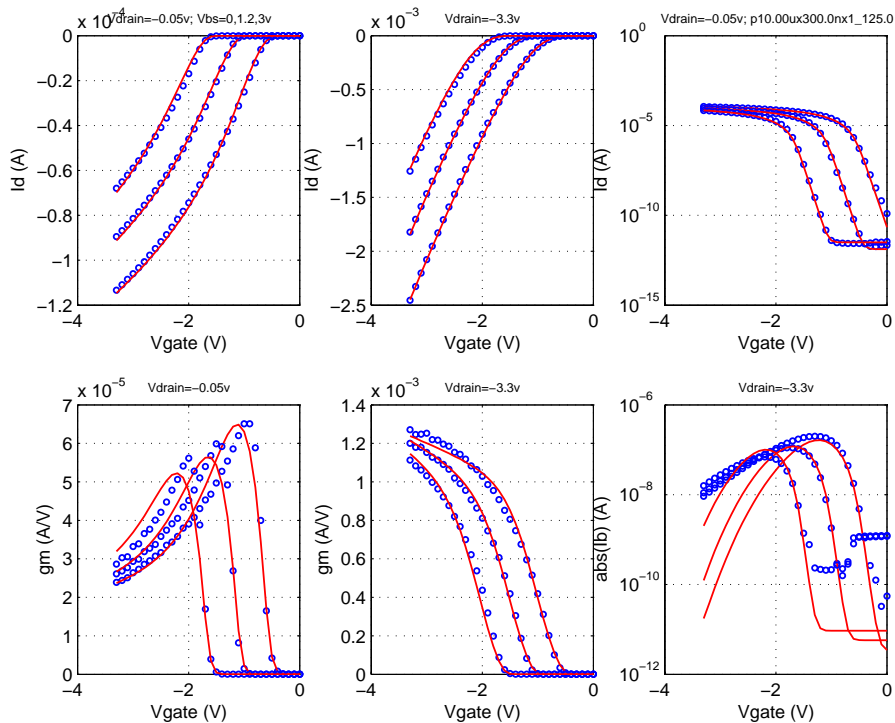


FIGURE 2.78 3p3v_PFET_10x0p3_idvg_125C



2.5 Statistical and Corner Models

Statistical models are generated by specifying 1- σ variations of appropriate model parameters. These variances are generated via a physically based and robust mathematical approach called the “Backward Propagation of Variance (BPV). [3]” The BPV approach is defined by Eq. 3:

$$\sigma_{e_i}^2 = \sum_k \left(\frac{\partial e_i}{\partial p_k} \right)^2 \cdot \sigma_{p_k}^2 \quad (\text{EQ 3})$$

where σ_{e_i} is the standard deviation of the i^{th} Electrical Specification (E-spec), $\frac{\partial e_i}{\partial p_k}$ is the partial derivative of the E-spec w.r.t. to the k^{th} model parameter, and σ_{p_k} is the standard deviation of the model parameter that being solved for. The E-specs for this technology are extracted from Process Control Monitoring (PCM) data and are defined in Jazz document NPB-PS-0577 titled “CA13 Electrical Specification.” This process is termed as the backward propagation of variance, as it takes measurements in variances (E-specs) of important electrical quantities and then calculates the variances in the model process parameters that are necessary to fit the spread in the measured data, rather than taking the measured variations in the model process parameters and forward propagating them to predict the variations in σ_e . Conventional statistical modeling approaches are typically forward propagated, and do not guarantee consistency between model and E-spec corners and miss the real goal of statistical modeling.

The set of partial derivatives on the RHS of Eq. 3 represent the sensitivity matrix of the extracted model, and are directly evaluated using a circuit simulator such as Spectre. These derivatives can depend on the Δp_k values chosen to approximate δp_k . A global optimizer is used to minimize any error associated with the sensitivity matrix evaluation. The maximum deviation between the E-spec. and simulator prediction for the SLOW, NOM, and FAST corners is 1/2- σ , where 6- σ is the total range from the minimum to the maximum value of the E-spec. Typically, this corresponds to < 2% deviation of the model prediction w.r.t the E-spec. Statistical model predictions for the various flavors of FETs in this technology are shown in Tables 2.10 through 2.13.

The statistical model allows un-correlated variations in oxide thickness, flat-band voltage (from oxide-charge and gate work-function), and channel doping as per Eq. 4 and Eq. 5 to impact threshold voltage (BSIM parameter VTH0). Additionally, the channel doping and oxide thickness are used for the body effect (BSIM parameter K1) evaluation as per Eq. 6 and Eq. 7.

$$VTH0 = VFB + 2 \frac{kT}{q} \ln \frac{N_{ch}}{n_i} + \frac{T_{ox}}{E_{ox}} \sqrt{2q \cdot E_{si} \cdot N_{ch} \cdot 2 \frac{kT}{q} \ln \frac{N_{ch}}{n_i}} \quad (\text{EQ 4})$$

$$\Delta VTH0 = \Delta VFB + \frac{\partial}{\partial N_{ch}} VTH0 \cdot \Delta N_{ch} + \frac{\partial}{\partial T_{ox}} VTH0 \cdot \Delta T_{ox} \quad (\text{EQ 5})$$

$$K1 = \frac{T_{ox}}{E_{ox}} \cdot \sqrt{2q \cdot E_{si} \cdot N_{ch}} \quad (\text{EQ 6})$$

$$\Delta K1 = \frac{\partial}{\partial N_{ch}} K1 \cdot \Delta N_{ch} + \frac{\partial}{\partial T_{ox}} K1 \cdot \Delta T_{ox} \quad (\text{EQ 7})$$

The geometry dependence of the threshold voltage and body constant is captured by specifying un-correlated variations in the relevant BSIM parameters such as K3 (narrow width V_{th}), K3B (body effect in narrow device), DVT0 (short channel V_{th}), and DVT2 (body effect of short channel device).

The global variation in active dimensions (active_cd) is propagated into the W_{eff} calculation of FETs to be consistent with other active or passive devices in the circuit. Similarly, global process variations in the gate poly length (poly_cd) are propagated into L_{eff} calculations. Additionally, the L_{eff} depends on the variation in the lateral spread of the LDD (Lightly Doped Drain) under the gate. Oxide thickness and L_{eff} variations are physically propagated into overlap capacitance variation.

The extraction of statistical variations of model parameters is preceded by “Centering” process of the “measured” case. This is described in Section 2.5.1.

2.5.1 Centering

The measured case is “centered” to the E-specs of threshold voltage, body constant, and saturation currents for the devices listed in the E-specs. This is an important part of the model release methodology and generates a nominal model that is aligned to the nominal E-specs of the technology.

The centering is performed using the statistical modeling approach defined in Section 2.5 by modifying Eq. 3 as:

$$\Delta e_i = \sum_k \frac{\partial e_i}{\partial p_k} \cdot \Delta p_k \quad (\text{EQ 8})$$

where Δe_i is the difference between the measured case prediction of the E-spec and nominal E-spec, $\frac{\partial e_i}{\partial p_k}$ is the partial derivative of the e-spec w.r.t the relevant model parameter, and Δp_k is the shift in the model parameter needed to center the measured case to the E-spec. Typical shift in model parameters required to center the measured case are less than 1%, and represent a statistically valid and unique set of shifts in model parameters that are perfectly aligned with the “nominal” process targets of the Fab. It should be noted that these E-specs are targets that the fab continually tries to match, with the results being regularly reported as CPK charts.

2.5.2 Corner model generation

Corner models are generated via an approach identical to the centering model methodology described in Section 2.5.1. The E-spec corners are used to calculate the E-spec delta on the LHS of Eq. 8, which is then solved for the required model parameter shift on the RHS. The maximum allowable deviation between the E-spec. and the model prediction is $1/2 \cdot 6\sigma$, where 6σ is the total range from the minimum to the maximum value of the E-spec. Typically, this corresponds to < 2% deviation of the model prediction w.r.t the E-spec.

The variation in junction area capacitance CJ is +/-10% in corner cases. The junction sidewall capacitance CJSW and gate edge sidewall capacitance CJSWG are skewed for the corner cases by +/- 10% for both FET and diode models.

Conventional corner modeling approaches are typically forward propagated, where measured model parameter deltas (Δp_k in Eq. 8) are used to predict spreads in key electrical properties of the FETs and do not guarantee consistency between corner models and E-spec corners. The extracted corner model parameters for 1.2 and 3.3v FETs are shown in Tables 2.8 and 2.9, respectively.

TABLE 2.8 Corner model parameters for the 1.2v FETs

BSIM4 Parameter	Description	NFET			PFET		
		Slow	Nom	Fast	Slow	Nom	Fast
tox (m)	Elec. Oxide Thickness	2.93e-09	2.88e-09	2.83e-09	2.85e-09	2.80e-09	2.75e-09
tox (m)	Phys. Oxide Thickness	2.35e-09	2.30e-09	2.25e-09	2.35e-09	2.30e-09	2.25e-09
lint (m)	Delta L	3.60e-08	3.74e-08	3.87e-08	7.60e-08	7.78e-08	7.90e-08
k1 ($V^{1/2}$)	Body Effect	3.70e-01	3.37e-01	3.02e-01	4.76e-01	4.34e-01	3.91e-01
k3	Narrow Channel V_t	-2.16e+00	-4.13e+00	-6.34e+00	-5.00e-02	-1.60e+00	-4.21e+00
k3b (1/V)	Narrow Width Body Effect	4.97e-01	8.90e-01	1.47e+00	1.30e+00	2.30e+00	3.48e+00
cjswgd (F/m)	Drain/Channel Junc. Cap.	2.61e-10	2.37e-10	2.13e-10	5.00e-10	4.54e-10	4.09e-10
cjd (F/m ²)	Drain/Well Junc. Cap.	3.42e-04	3.11e-04	2.80e-04	7.49e-04	6.81e-04	6.13e-04
cjswgs (F/m)	Source/Channel Junc. Cap.	2.61e-10	2.37e-10	2.13e-10	5.00e-10	4.54e-10	4.09e-10
wint (m)	Delta W	7.73e-08	6.45e-08	5.18e-08	4.56e-08	3.11e-08	1.90e-08
cjs (F/m ²)	Source/Well Junc. Cap.	3.42e-04	3.11e-04	2.80e-04	7.49e-04	6.81e-04	6.13e-04
vt0 (V)	Long Channel V_t	2.02e-01	1.71e-01	1.43e-01	-2.31e-01	-1.90e-01	-1.53e-01
cgs (F/m)	LDD G/S Overlap Cap.	8.32e-11	8.80e-11	9.27e-11	2.51e-10	2.62e-10	2.71e-10
cgd (F/m)	LDD G/D Overlap Cap.	8.32e-11	8.80e-11	9.27e-11	2.51e-10	2.62e-10	2.71e-10
cgso (F/m)	Non-LDD G/S Overlap Cap.	2.83e-10	3.00e-10	3.16e-10	2.13e-10	2.22e-10	2.29e-10
cgdo (F/m)	Non-LDD G/D Overlap Cap.	2.83e-10	3.00e-10	3.16e-10	2.13e-10	2.22e-10	2.29e-10
cjswd (F/m)	Drain-isolation Junc. Cap.	7.57e-11	6.88e-11	6.19e-11	1.42e-10	1.29e-10	1.16e-10
cjsws (F/m)	Source-isolation Junc. Cap.	7.57e-11	6.88e-11	6.19e-11	1.42e-10	1.29e-10	1.16e-10
lpe0 (m)	Lat. Doping V_t	8.85e-08	7.39e-08	5.83e-08	2.93e-08	2.36e-08	1.79e-08
rdsw (Ω -um)	Bias dep. comp. of R_{ds}	9.45e+01	9.00e+01	8.55e+01	2.10e+03	2.00e+03	1.90e+03
u0 (m ² /Vs)	Low-field Mobility	3.79e-02	3.82e-02	3.88e-02	4.65e-03	4.77e-03	5.01e-03
lpeb (m)	Lat. Doping Body Effect	3.16e-08	2.41e-08	1.40e-08	1.96e-08	1.47e-08	9.13e-09
rdswmin (Ω -um)	Fixed comp. of R_{ds}	1.05e+00	1.00e+00	9.50e-01	1.05e+02	1.00e+02	9.50e+01

TABLE 2.9 Corner model parameters for the 3.3v FETs

BSIM3v3 Parameter	Description	NFET			PFET		
		SLOW	NOM	FAST	SLOW	NOM	FAST
tox (m)	Elec. Oxide Thickness	7.18e-09	7.00e-09	6.82e-09	7.18e-09	7.00e-09	6.82e-09
tox (m)	Phys. Oxide Thickness	6.78e-09	6.60e-09	6.42e-09	6.78e-09	6.60e-09	6.42e-09
lint (m)	Delta L	6.76e-08	8.81e-08	1.02e-07	1.40e-07	1.42e-07	1.46e-07
k1 ($V^{1/2}$)	Body Effect	7.19e-01	6.51e-01	5.88e-01	1.06e+00	9.61e-01	8.62e-01

TABLE 2.9 Corner model parameters for the 3.3v FETs

BSIM3v3 Parameter	Description	NFET			PFET		
		SLOW	NOM	FAST	SLOW	NOM	FAST
cjswgd (F/m)	Drain/Channel Junc. Cap.	1.76e-10	1.60e-10	1.44e-10	3.30e-10	3.00e-10	2.70e-10
cjd (F/m ²)	Drain/Well Junc. Cap.	3.42e-04	3.11e-04	2.80e-04	8.20e-04	7.45e-04	6.71e-04
cjswgs (F/m)	Source/Channel Junc. Cap.	1.76e-10	1.60e-10	1.44e-10	3.30e-10	3.00e-10	2.70e-10
wint (m)	Delta W	8.10e-08	7.03e-08	5.45e-08	1.31e-07	8.89e-08	5.15e-08
cjs (F/m ²)	Source/Well Junc. Cap.	3.42e-04	3.11e-04	2.80e-04	8.20e-04	7.45e-04	6.71e-04
vth0 (V)	Long Channel Vt	6.39e-01	5.55e-01	4.84e-01	-7.83e-01	-6.94e-01	-6.11e-01
cgsi (F/m)	LDD G/S Overlap Cap.	6.74e-11	9.00e-11	1.07e-10	1.25e-10	1.30e-10	1.37e-10
cgdl (F/m)	LDD G/D Overlap Cap.	6.74e-11	9.00e-11	1.07e-10	1.25e-10	1.30e-10	1.37e-10
cgso (F/m)	Non-LDD G/S Overlap Cap.	1.80e-10	2.40e-10	2.84e-10	1.73e-10	1.80e-10	1.90e-10
cgdo (F/m)	Non-LDD G/D Overlap Cap.	1.80e-10	2.40e-10	2.84e-10	1.73e-10	1.80e-10	1.90e-10
cjswd (F/m)	Drain-isolation Junc. Cap.	8.05e-11	7.32e-11	6.59e-11	1.25e-10	1.13e-10	1.02e-10
cjsws (F/m)	Source-isolation Junc. Cap.	8.05e-11	7.32e-11	6.59e-11	1.25e-10	1.13e-10	1.02e-10
rdsw (Ω-um)	Bias dep. comp. of Rds	1.21e+03	1.15e+03	1.09e+03	5.22e+02	4.97e+02	4.73e+02
u0 (m ² /Vs)	Low-field Mobility	2.34e-02	2.50e-02	2.70e-02	1.16e-02	1.30e-02	1.39e-02
rdswmin (Ω-um)	Fixed comp. of Rds	7.84e+00	7.47e+00	7.10e+00	5.54e+02	5.28e+02	5.01e+02

2.5.3 Statistical model usage guidelines

In contrast to the corner models, the statistical models allow “multi-directional” variability in model parameters. For a sufficient number of monte-carlo runs these simulation results converge to the measured (E-spec.) 3-σ variation in key MOSFET device properties (such as I_{dsat} , V_{th}) and in most cases represent a more accurate prediction (over corner models) of expected impact of process variations on circuit-level figures of merit. The statistical model is currently supported only in Spectre, which provides the needed framework for statistical modeling. The “process-only” variation option should be selected when setting up statistical model run. This represents the expected functional (non-defect related) yield, that can be expected for the particular design split. The “numruns” (number of runs) in monte-carlo analysis is an important parameter that controls the accuracy of the statistical model prediction. For single transistor level simulations of V_{th} , I_{dsat} , and body constant a value of a 100 runs gives reasonably stable results. The user should check the mean value of the circuit-level figure of merit that is being simulated and compare it to nominal simulation and decide whether to increase or decrease this value.

2.5.4 Statistical and Corner Model Tables

TABLE 2.10 1.2v NFET corner and statistical model predictions

Device	WxL(μm)	Espec Name (unit)	Slow			Nom			Fast		
			Espec	Corner	Stat	Espec	Corner	Stat	Espec	Corner	Stat
small	0.15x0.12	vt (V)	0.390	0.394	0.376	0.310	0.309	0.307	0.230	0.231	0.238
small	0.15x0.12	idsat (mA)	0.035	0.038	0.040	0.065	0.065	0.065	0.095	0.098	0.090
small	0.15x0.12	kb ($V^{0.5}$)	0.240	0.246	0.248	0.180	0.184	0.184	0.120	0.119	0.121
short	10x0.12	vt (V)	0.450	0.452	0.450	0.390	0.391	0.389	0.330	0.333	0.329
short	10x0.12	idsat (mA)	4.550	4.487	4.550	5.350	5.361	5.334	6.150	6.291	6.118
short	10x0.12	kb ($V^{0.5}$)	0.270	0.270	0.271	0.220	0.222	0.222	0.170	0.170	0.174
large	10x10	vt (V)	0.250	0.252	0.251	0.220	0.220	0.219	0.190	0.192	0.188
large	10x10	β^1 ($\mu\text{A}/V^2$)	180.0	204.4	201.92	200.0	216.40	212.59	220.0	229.9	223.26
large	10x10	kb ($V^{0.5}$)	0.250	0.250	0.252	0.220	0.220	0.221	0.190	0.190	0.190
narrow	0.15x10	v_t^2 (V)	0.160	0.161	0.187	0.120	0.125	0.122	0.080	0.082	0.057
narrow	0.15x10	kb ($V^{0.5}$)	0.230	0.233	0.238	0.180	0.184	0.185	0.130	0.135	0.132

TABLE 2.11 1.2v PFET corner and statistical model predictions

Device	WxL(μm)	Espec Name (unit)	Slow			Nom			Fast		
			Espec	Corner	Stat	Espec	Corner	Stat	Espec	Corner	Stat
small	0.15x0.12	vt (V)	-0.430	-0.437	-0.435	-0.340	-0.344	-0.344	-0.250	-0.253	-0.252
small	0.15x0.12	idsat (mA)	-0.015	-0.017	-0.015	-0.030	-0.030	-0.030	-0.045	-0.047	-0.046
small	0.15x0.12	kb ($V^{0.5}$)	0.360	0.373	0.360	0.280	0.283	0.281	0.200	0.199	0.202
short	10x0.12	vt (V)	-0.420	-0.420	-0.419	-0.360	-0.358	-0.359	-0.300	-0.301	-0.299
short	10x0.12	idsat (mA)	-1.900	-1.892	-1.900	-2.350	-2.349	-2.340	-2.800	-2.856	-2.780
short	10x0.12	kb ($V^{0.5}$)	0.400	0.400	0.402	0.340	0.340	0.340	0.280	0.281	0.278
large	10x10	vt (V)	-0.320	-0.320	-0.317	-0.280	-0.278	-0.279	-0.240	-0.240	-0.241
large	10x10	β^1 ($\mu\text{A}/V^2$)	42.00	43.89	43.10	45.00	46.34	46.30	48.00	49.90	49.50
large	10x10	kb ($V^{0.5}$)	0.380	0.380	0.379	0.340	0.341	0.341	0.300	0.300	0.303
narrow	0.15x10	vt (V)	-0.340	-0.334	-0.340	-0.270	-0.270	-0.270	-0.200	-0.204	-0.200
narrow	0.15x10	kb ($V^{0.5}$)	0.330	0.333	0.333	0.270	0.275	0.274	0.210	0.214	0.215

TABLE 2.12 3.3v NFET corner and statistical model predictions

Device	WxL(μm)	Espec Name (unit)	Slow			Nom			Fast		
			Espec	Corner	Stat	Espec	Corner	Stat	Espec	Corner	Stat
small	0.6x0.3	idsat (mA)	0.255	0.264	0.257	0.330	0.334	0.335	0.405	0.413	0.414
short	10x0.3	vt (V)	0.760	0.773	0.761	0.660	0.656	0.647	0.560	0.547	0.533
short	10x0.3	idsat (mA)	4.600	4.635	4.740	5.500	5.517	5.502	6.400	6.345	6.265
short	10x0.3	kb ($V^{0.5}$)	0.600	0.616	0.622	0.500	0.505	0.497	0.400	0.394	0.373
large	10x10	vt (V)	0.780	0.782	0.782	0.700	0.700	0.698	0.620	0.631	0.614
large	10x10	β^1 ($\mu\text{A}/V^2$)	77.00	74.00	71.22	86.00	82.36	80.88	95.00	92.23	90.54
large	10x10	kb ($V^{0.5}$)	0.680	0.675	0.673	0.610	0.610	0.610	0.540	0.550	0.546

TABLE 2.13 3.3v PFET corner and statistical model predictions

Device	WxL(μm)	Espec Name (unit)	Slow			Nom			Fast		
			Espec	Corner	Stat	Espec	Corner	Stat	Espec	Corner	Stat
small	0.6x0.3	idsat (mA)	-0.100	-0.104	-0.100	-0.150	-0.151	-0.152	-0.200	-0.204	-0.204
short	10x0.3	vt (V)	-0.830	-0.816	-0.816	-0.730	-0.724	-0.723	-0.630	-0.637	-0.630
short	10x0.3	idsat (mA)	-2.400	-2.411	-2.400	-2.900	-2.898	-2.900	-3.400	-3.414	-3.400
short	10x0.3	kb (V ^{0.5})	0.970	0.964	0.964	0.870	0.872	0.870	0.770	0.775	0.776
large	10x10	vt (V)	-0.860	-0.860	-0.859	-0.770	-0.767	-0.766	-0.680	-0.680	-0.673
large	10x10	beta ¹ (μA/V ²)	16.00	17.10	17.30	19.00	20.34	20.30	22.00	23.08	23.30
large	10x10	kb (V ^{0.5})	1.050	1.050	1.050	0.960	0.961	0.960	0.870	0.870	0.868

Notes:

1. Nominal corner and statistical models are not aligned with E-spec., due to tester limitations. Propagating a 3-sigma variation of beta results in > 3-sigma variation in I_{dsat} .
2. Statistical model prediction of narrow/long channel 1.2v NFET V_t spread is larger than E-spec. E-spec. and corner models will be updated once longer-term PCM data is available.
3. Oxide thickness variation in the corner models is less than E-spec. (Table 2.14); propagating a full 3-sigma variation of oxide thickness results in a > 3-sigma variation in I_{dsat} . 3-sigma variation of oxide thickness is included in the statistical models.

TABLE 2.14 Oxide thickness variation in models compared w/ E-spec.

	Espec. (3-sigma)	Corner Models (3-sigma)	Statistical Models (3-sigma)
1,2v FETs	+/- 1A	+/- 0.5A	+/- 1A
3.3v FETs	+/- 3A	+/- 1.8A	+/- 3A

2.6 Mismatch Models

2.6.1 Measurements

The measurement setup is composed of a HP4156 Semiconductor Parameter Analyzer, Keithley 707 switch matrix with 7172 low current matrix cards, and Signatone S485 semi-automatic prober with hot chuck. The test is a two step process. In the first step, the average thresholds of the two transistors in the FET pair are measured via the maximum transconductance method. In the second step, the gate is biased at $V_{gs} = V_{gst} = V_{th} + 0.1, 0.3, 0.5$ and the currents in each transistor measured for multiple drain biases ($V_{ds}=0.2, 0.6, 1.4v$). The mismatch current is then evaluated via Eq. 9:

$$\Delta I_d = 100 \times \frac{I_{d2} - I_{d1}}{I_{d1}} \quad (\text{EQ 9})$$

The mismatch current represents the error between the currents in a simple current mirror. The transistors in the mismatch test-structures are typically $\sim 10\mu m$ apart, representing a worst-case mismatch for most analog layouts, where the transistors in the matched pair can be laid-out in closer proximity to each other.

2.6.2 Mismatch modeling

The mismatch between neighboring FETs is a representation of the local variation of process parameters such as oxide thickness, channel doping, oxide charge, gate work-function, channel length and width. The basic equations used to model such variations are identical to what was described in the section “Statistical and Corner Models” on page 57. To match the measured data, these variations are made geometry dependent as per Eq. 10:

$$\sigma_{local}(X) = \frac{\sigma_X}{\sqrt{W_{eff} \cdot L_{eff}}} \quad (\text{EQ 10})$$

where X is the channel doping N_{ch} , low field mobility $U0$, flat-band voltage VFB , or oxide thickness T_{ox} .

The impact of local lithographic variations is captured via Eq. 11 and Eq. 12:

$$\sigma_{local}(\Delta W) = \frac{\sigma(\Delta W)}{\sqrt{L_{eff}}} \quad (\text{EQ 11})$$

$$\sigma_{local}(\Delta L) = \frac{\sigma(\Delta L)}{\sqrt{W_{eff}}} \quad (\text{EQ 12})$$

whereby a narrower device can be expected to have larger channel length variations, and a shorter device can be expected to have larger channel width variations.

The local variation in these 6 parameters is extracted via a nonlinear least squares global optimization method to best fit the measured data.

2.6.3 Mismatch model usage guidelines

The mismatch model is available in Spectre, which provides the necessary framework to model the local mismatch between transistors. It is implemented inside the “sub-circuit” definition of the FETs allowing for “instance to instance” variations in the process parameters. The “variations” variable inside Spectre should be set equal to “mismatch.” Typically, ~100 monte-carlo runs are sufficient to accurately simulate the local-mismatch between the FETs. The user should, however, increase the “numruns” variable inside Spectre until the improvement in the simulated results is small.

2.6.4 Mismatch model comparison with measurements

Figure 2.79 through Figure 2.82 compare the mismatch model prediction with the measured data for the 3- σ ΔI_d mismatch between a pair of neighboring transistors for low and high voltage N and PFETs. The discrete points are the measured data, while the solid lines represent simulated data.

NOTE: Matching data from the CA18 process technology was used to extract the mismatch model for the SBL13/CA13 FETs.

FIGURE 2.79 1p2_NFET mismatch model vs. measurements

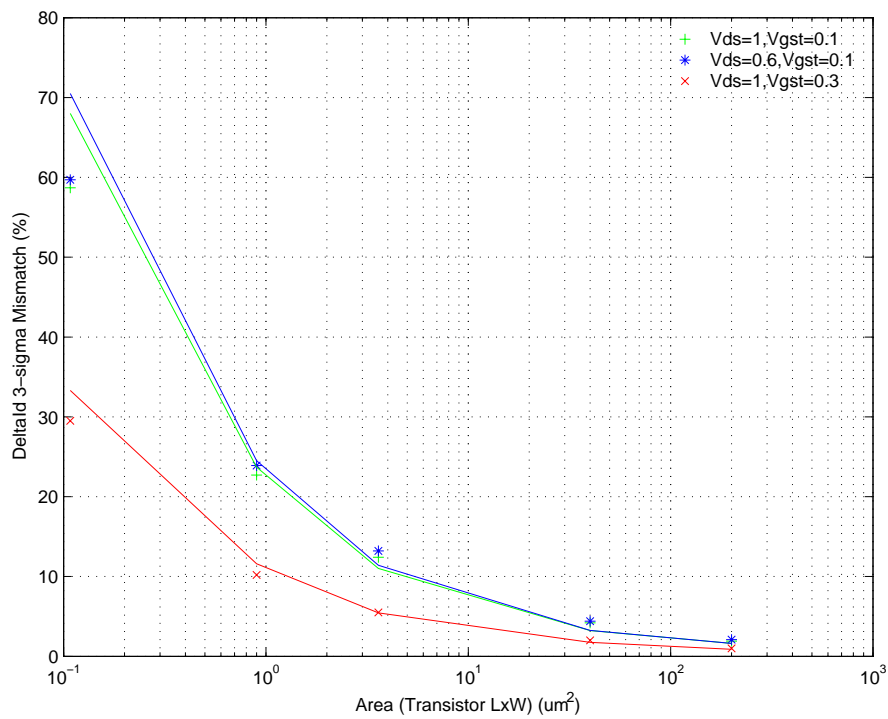


FIGURE 2.80 1p2_PFET mismatch model vs. measurements

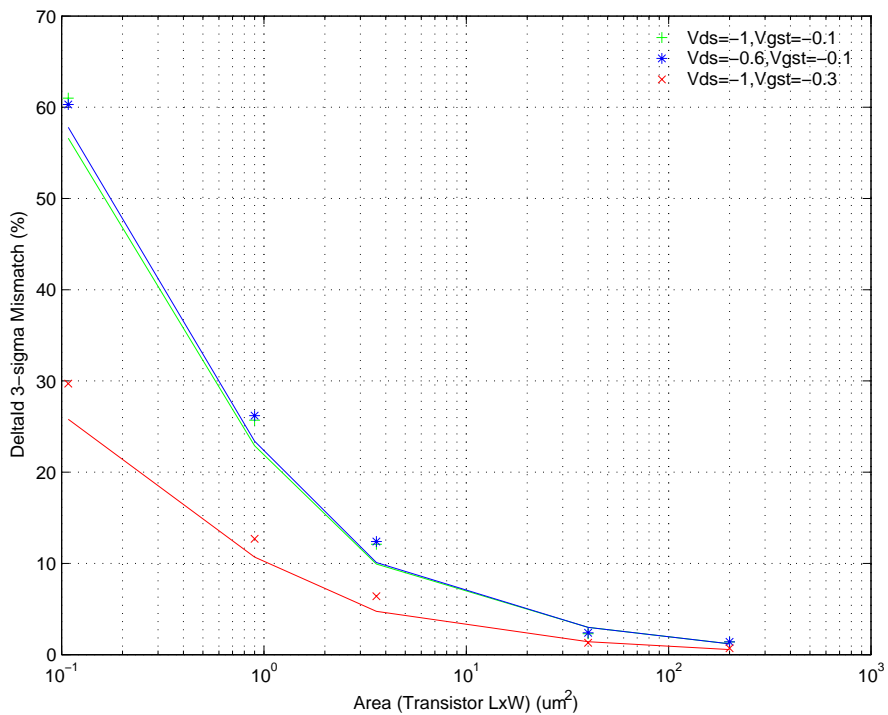


FIGURE 2.81 3p3_NFET mismatch model vs. measurements

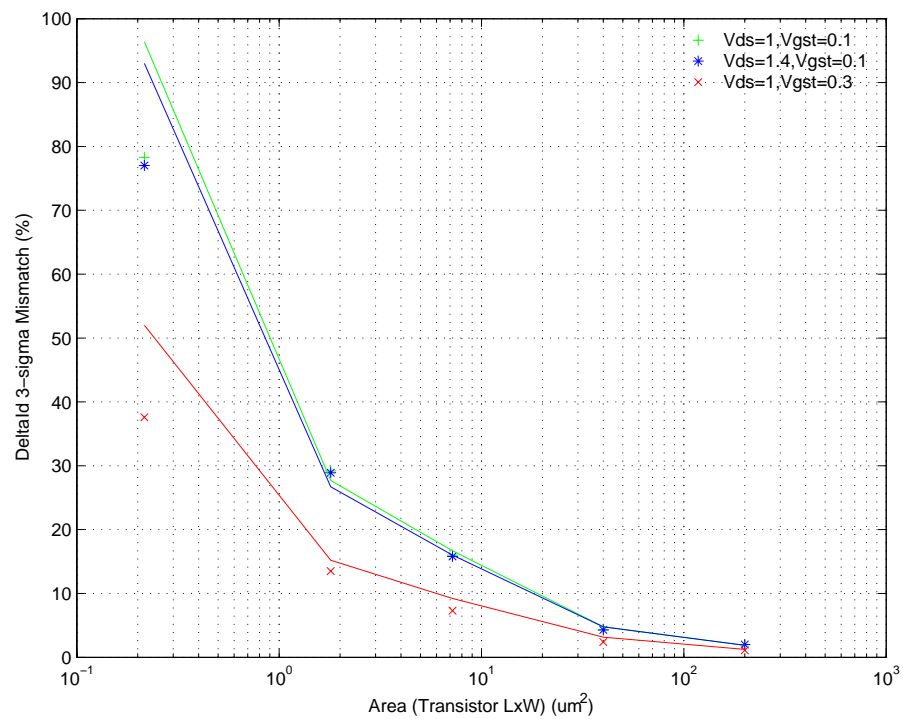
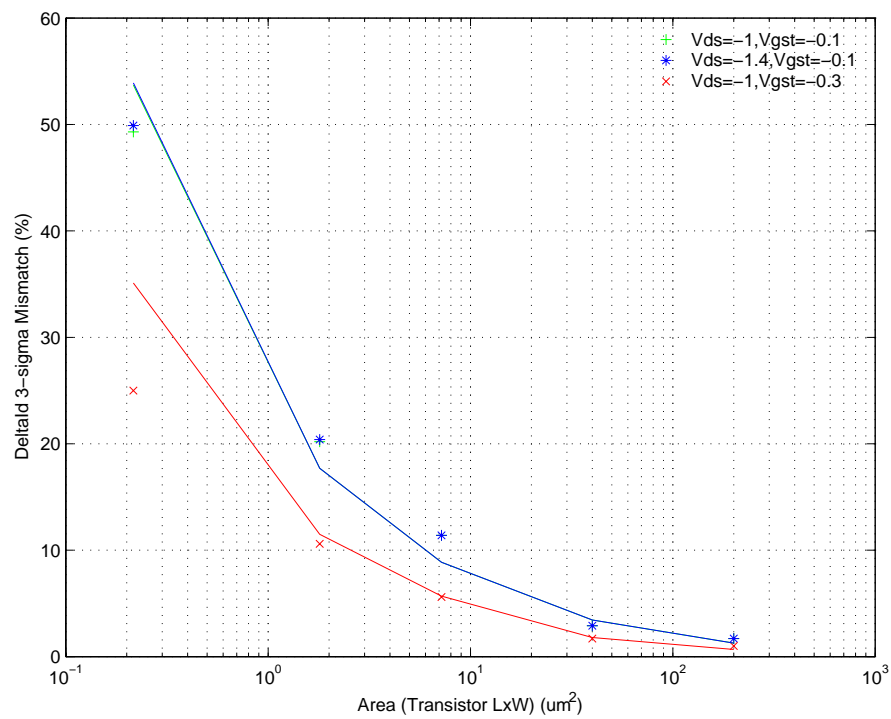


FIGURE 2.82 3p3_PFET mismatch model vs. measurements

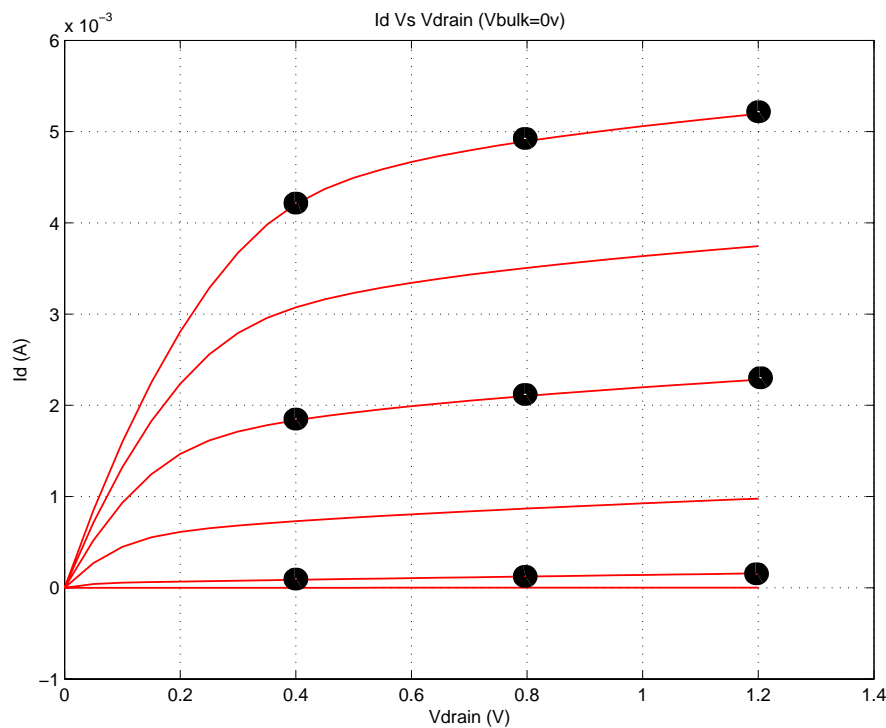


2.7 Flicker Noise

2.7.1 Measurement

Flicker noise ($1/f$ noise) was measured using the BTA9812A noise analyzer system in conjunction with the HP35670A dynamic signal analyzer using an on-wafer probe-station. BTA's Noisepro software was used to automate the measurements. Precautions were taken to electrically isolate the DUT and the RF-transistor (Ground-Signal-Ground) layouts were used to minimize on-wafer ground loops that can corrupt the measurements. Multi-die measurements with the MOSFET biased in saturation were performed to select the worst-case noise site. Measurements were then performed at 9 different biases. The list of biases encompassed both the linear and saturation regions of the FET and are illustrated in Figure 2.83.

FIGURE 2.83 Plot illustrating the bias points at which flicker noise measurements were performed.



2.7.2 Flicker Noise Modeling

The unified flicker noise model in BSIM4 (fnoimod=1) is used to capture the geometry and bias dependence of the measured flicker noise. Fluctuations in mobile carrier concentrations and mobility, caused by charge trapping/de-trapping in oxide traps, are included in this model.

2.7.3 Flicker Noise Model Playbacks

FIGURE 2.84 1p2_NFET_flicker_noise (NF/W/L = 1/10 μ m/0.12 μ m)

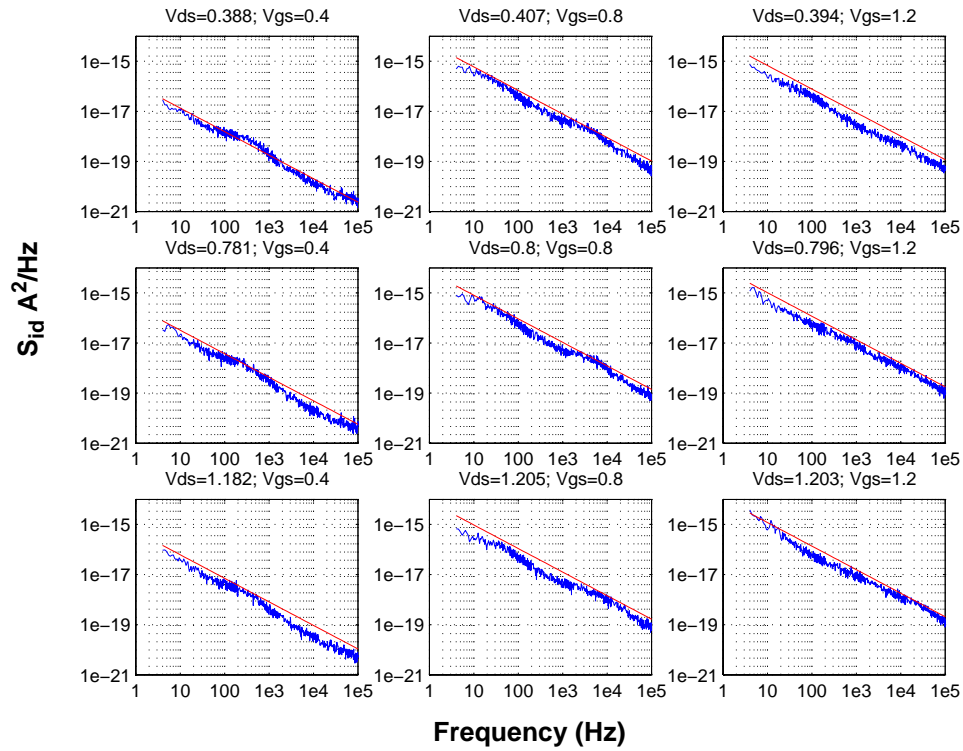


FIGURE 2.85 1p2_NFET_flicker_noise (NF/W/L = 1/20 μ m/0.12 μ m)

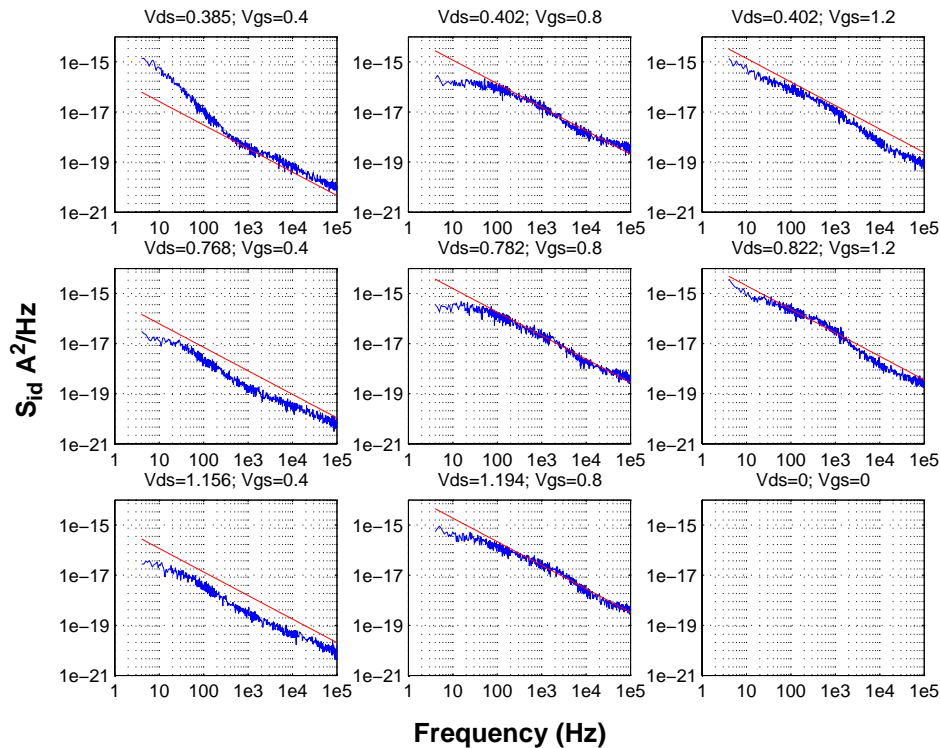


FIGURE 2.86 1p2_NFET_flicker_noise (NF/W/L = 1/2 μ m/0.12 μ m)

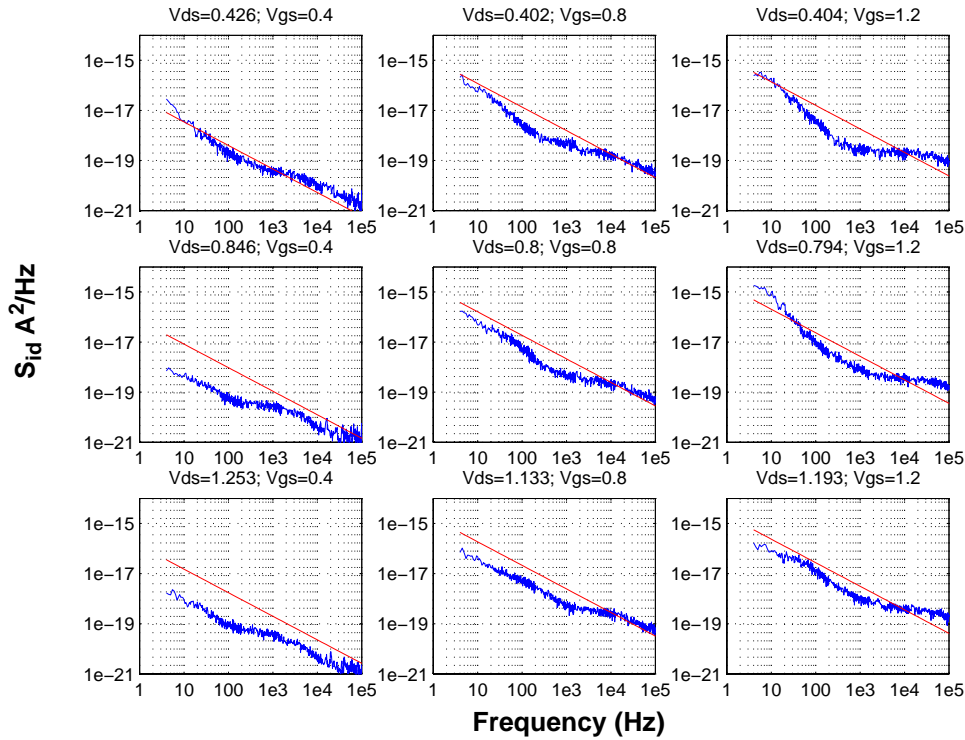


FIGURE 2.87 1p2_NFET_flicker_noise (NF/W/L = 1/10 μ m/0.2 μ m)

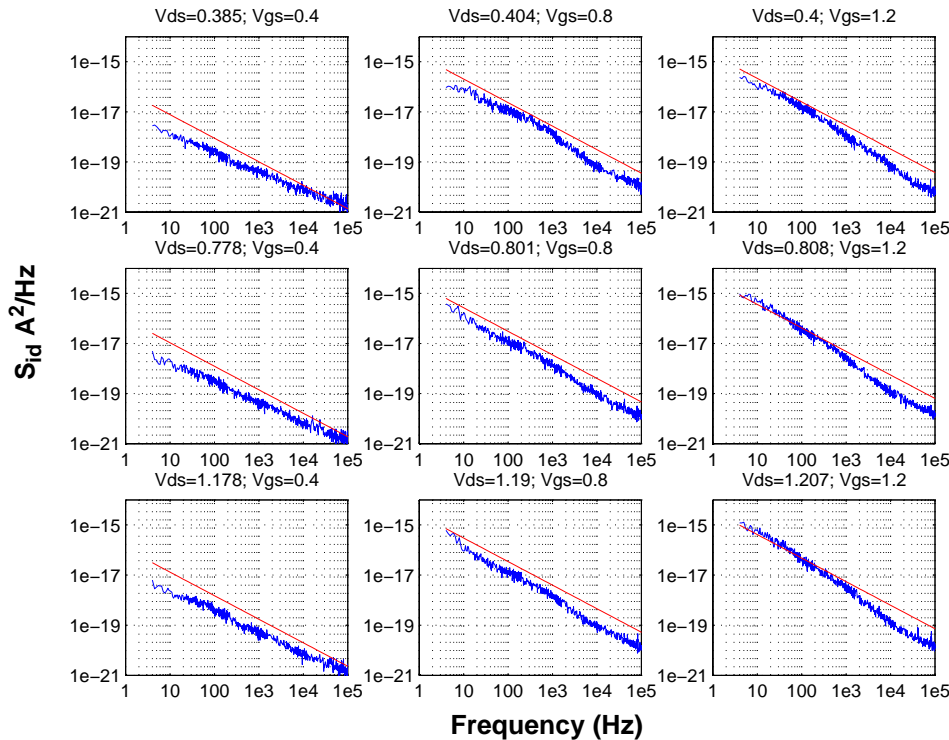


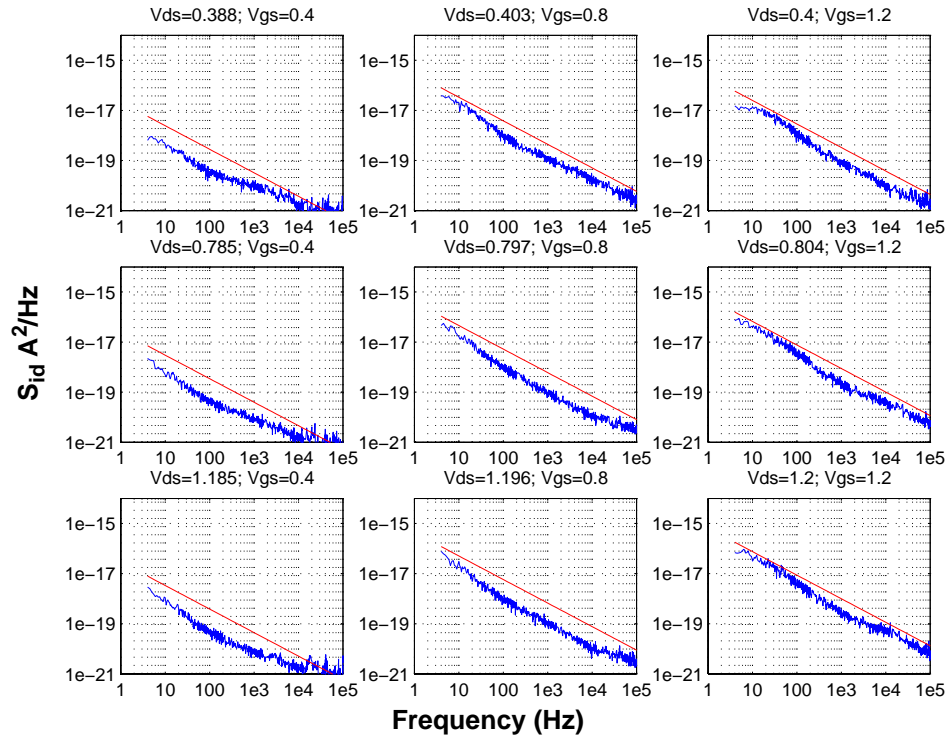
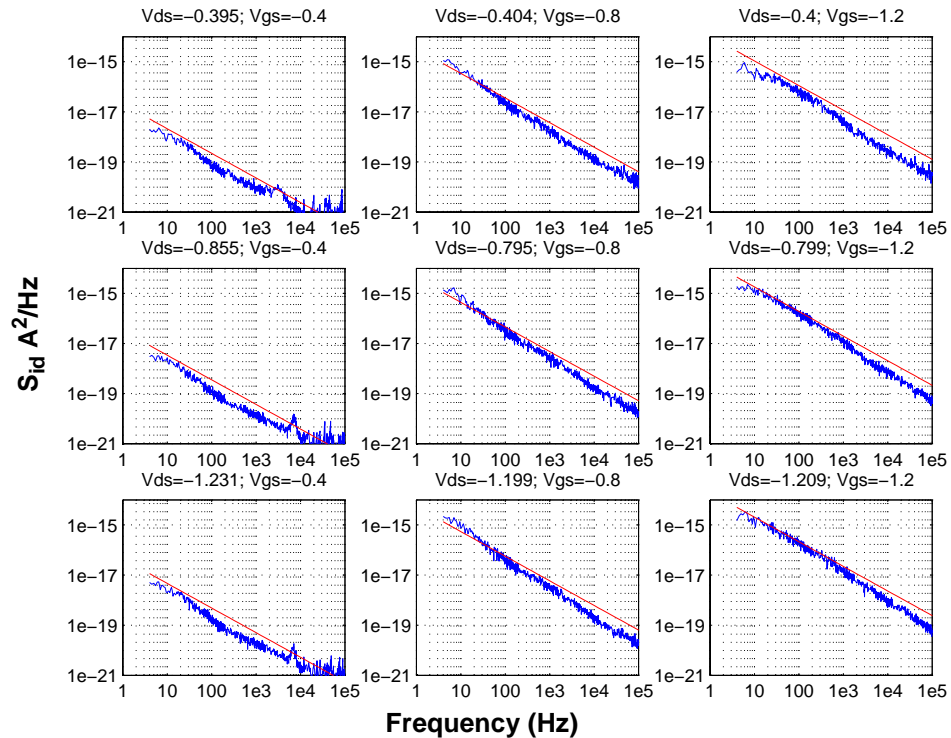
FIGURE 2.88 1p2_NFET_flicker_noise (NF/W/L = 1/10 μ m/0.4 μ m)FIGURE 2.89 1p2_PFET_flicker_noise (NF/W/L = 1/10 μ m/0.12 μ m)

FIGURE 2.90 1p2_PFET_flicker_noise (NF/W/L = 1/20 μ m/0.12 μ m)

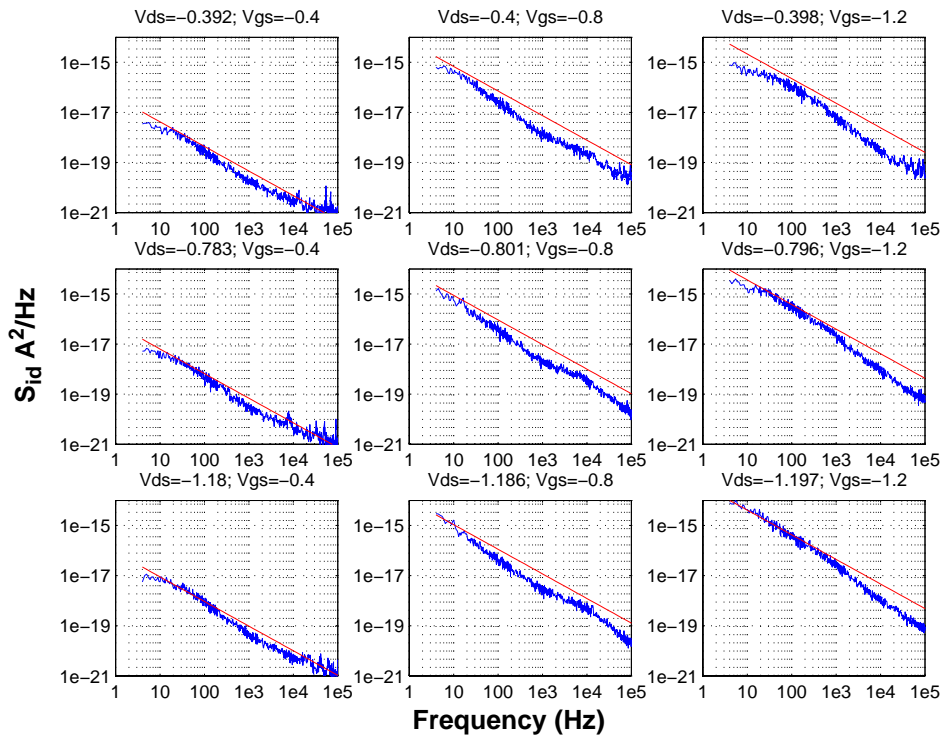


FIGURE 2.91 1p2_PFET_flicker_noise (NF/W/L = 1/2 μ m/0.12 μ m)

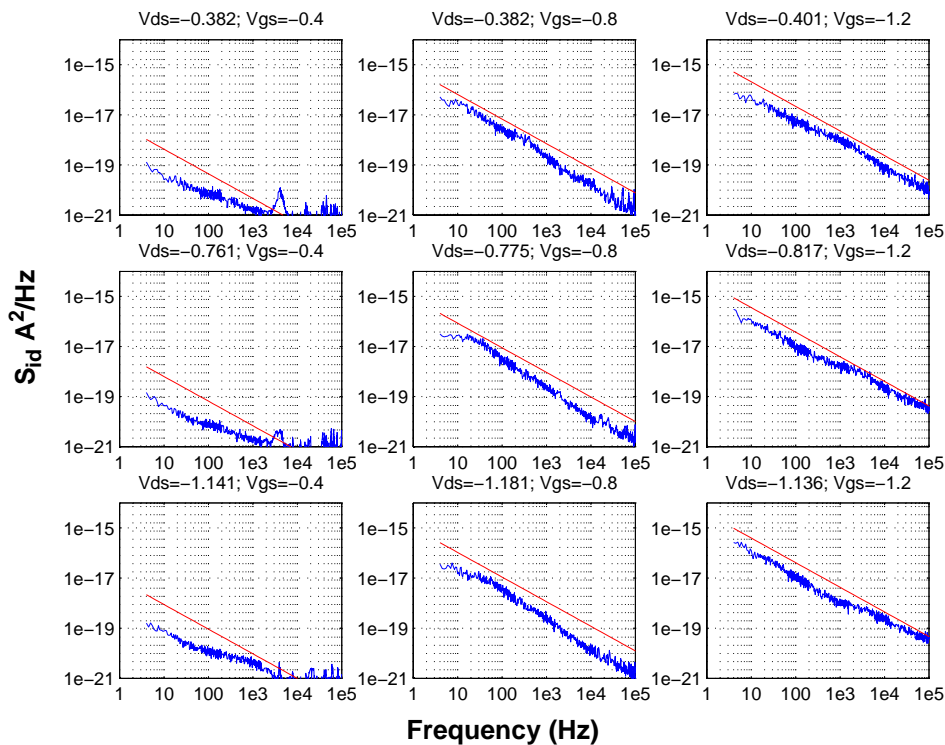


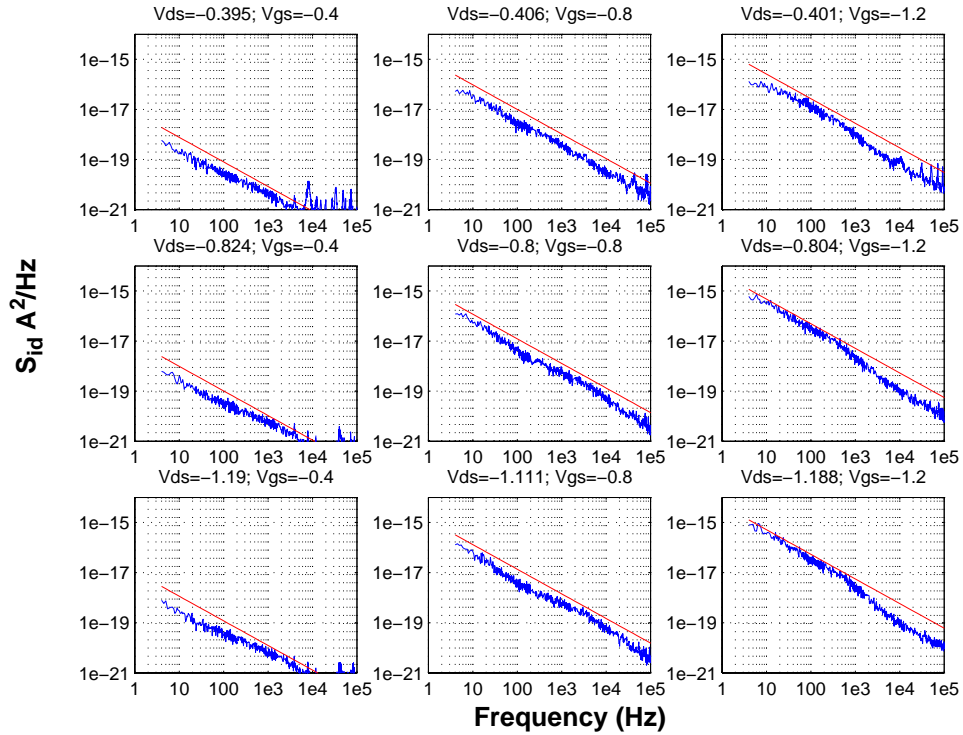
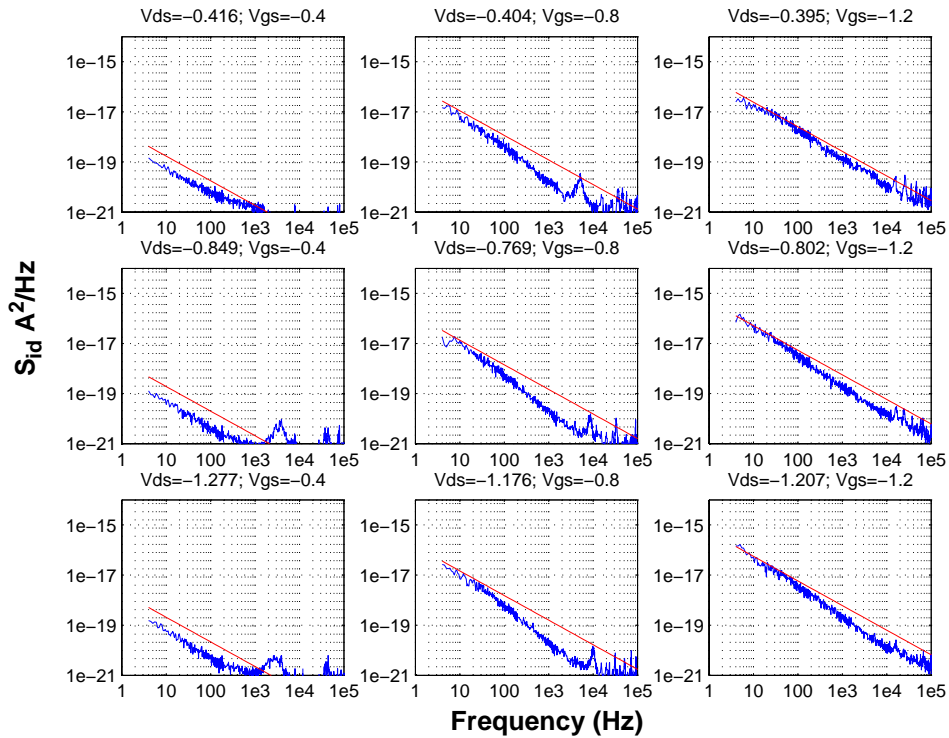
FIGURE 2.92 1p2_PFET_flicker_noise (NF/W/L = 1/10 μ m/0.2 μ m)FIGURE 2.93 1p2_PFET_flicker_noise (NF/W/L = 1/10 μ m/0.4 μ m)

FIGURE 2.94 3p3_NFET_flicker_noise (NF/W/L = 1/10 μ m/0.36 μ m)

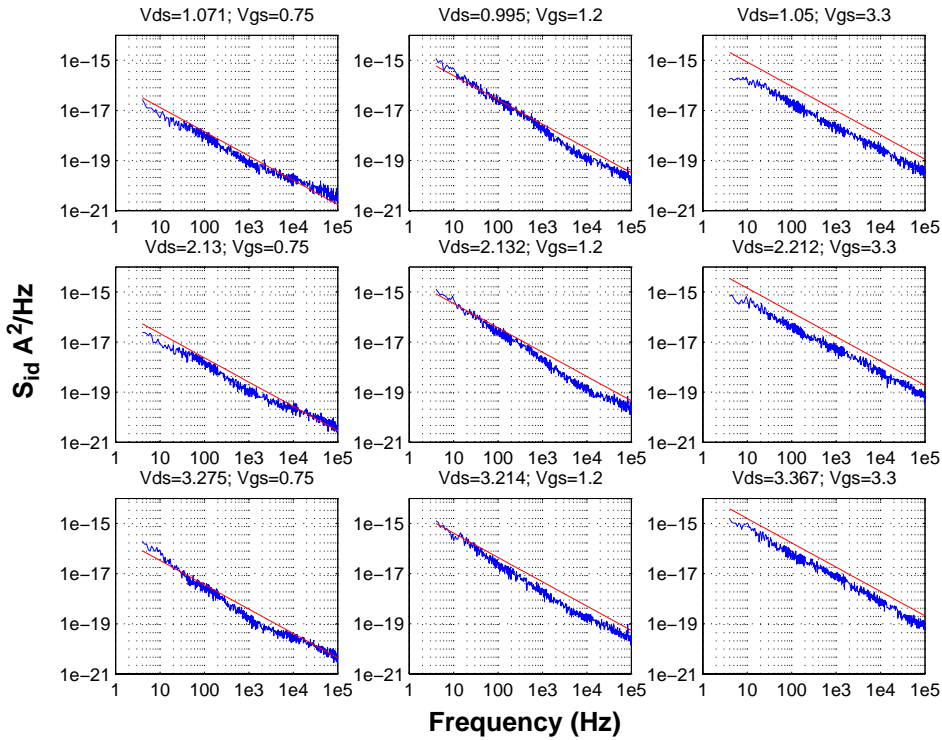


FIGURE 2.95 3p3_NFET_flicker_noise (NF/W/L = 1/2 μ m/0.36 μ m)

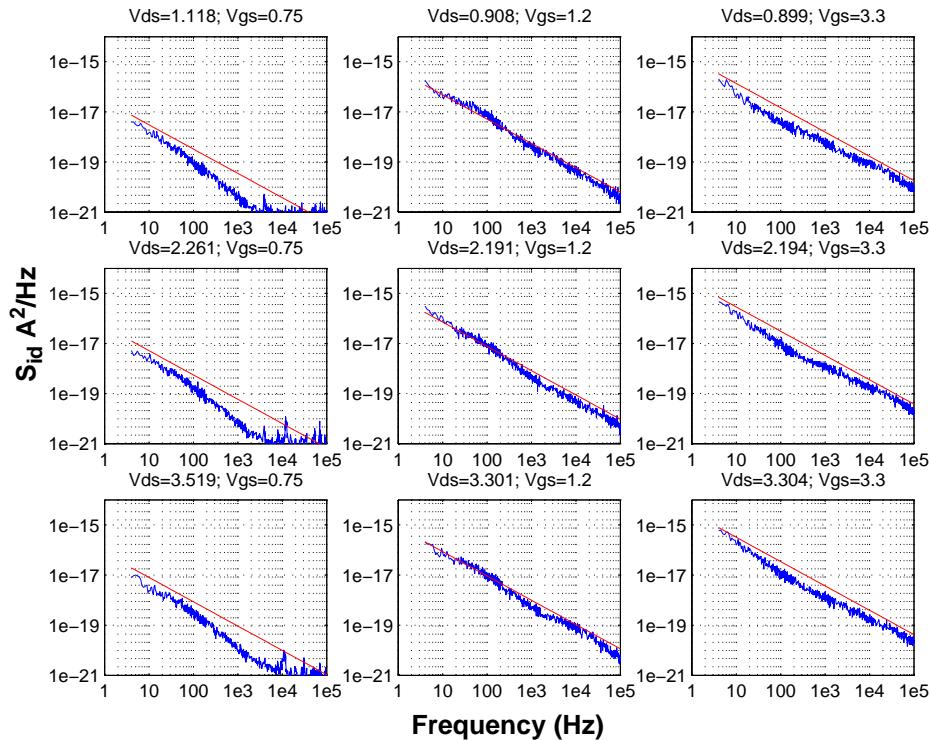


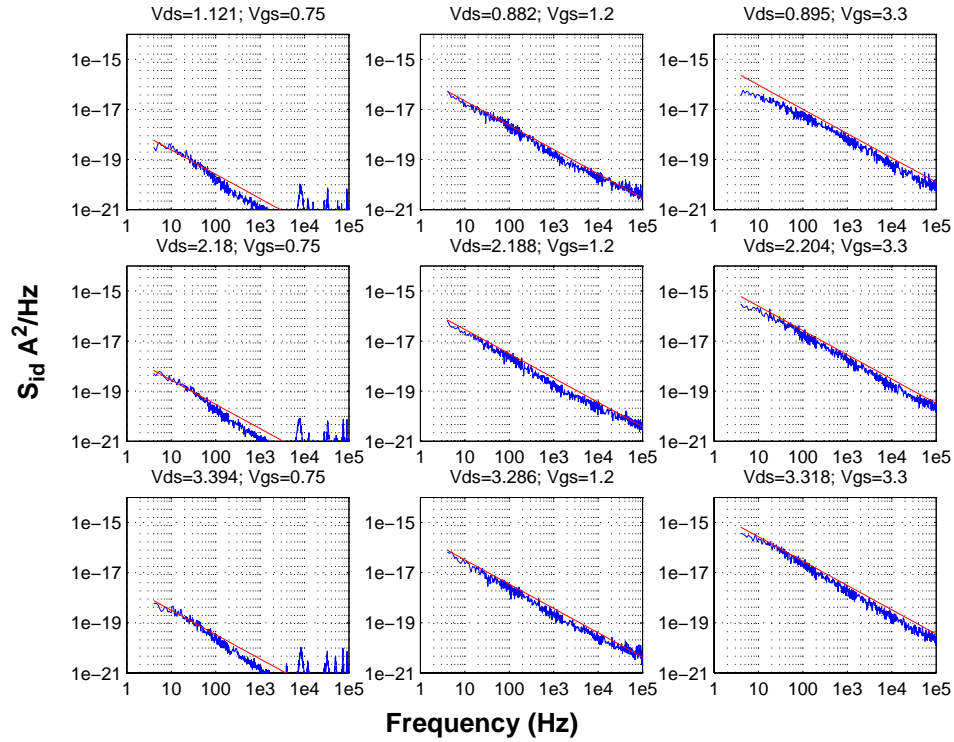
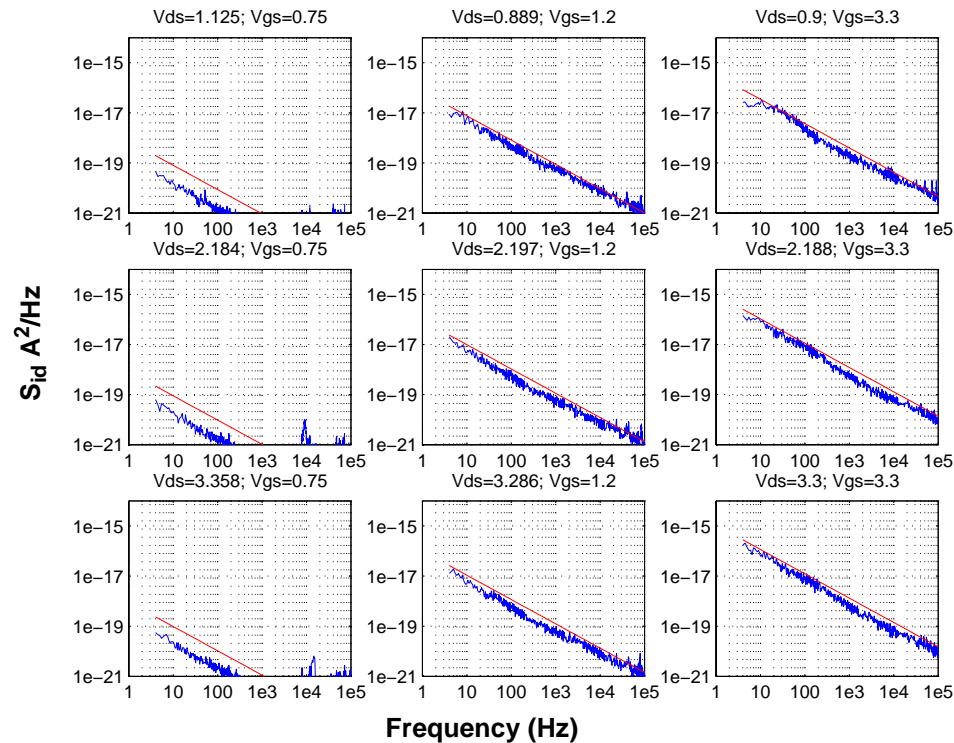
FIGURE 2.96 3p3_NFET_flicker_noise (NF/W/L = 1/10 μ m/0.6 μ m)FIGURE 2.97 3p3_NFET_flicker_noise (NF/W/L = 1/10 μ m/0.8 μ m)

FIGURE 2.98 3p3_PFET_flicker_noise (NF/W/L = 1/10 μ m/0.3 μ m)

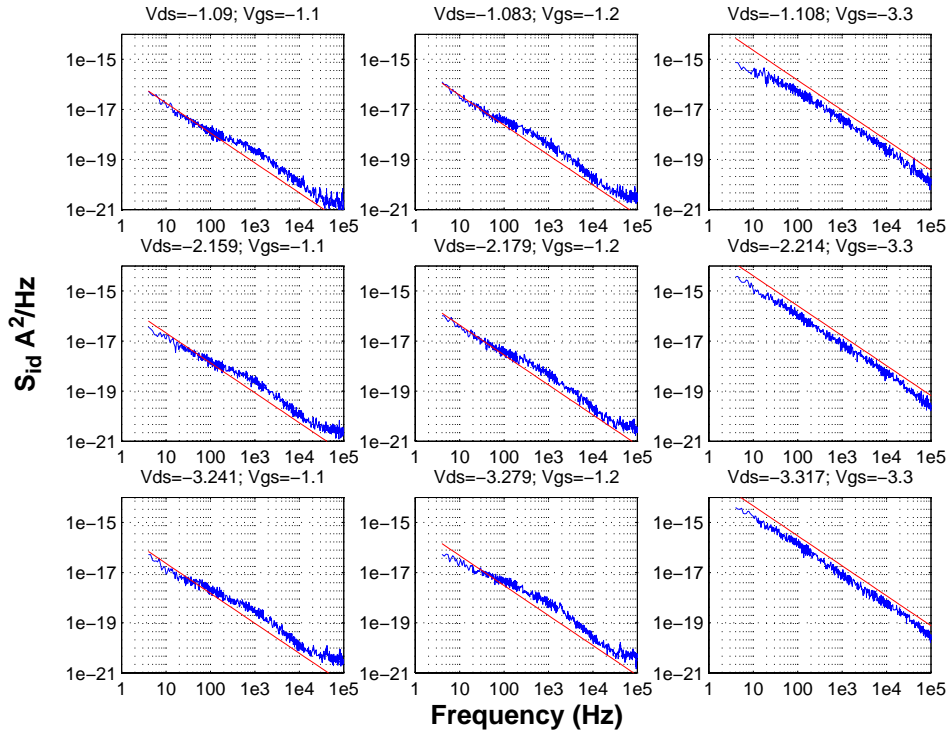


FIGURE 2.99 3p3_NPFET_flicker_noise (NF/W/L = 1/2 μ m/0.3 μ m)

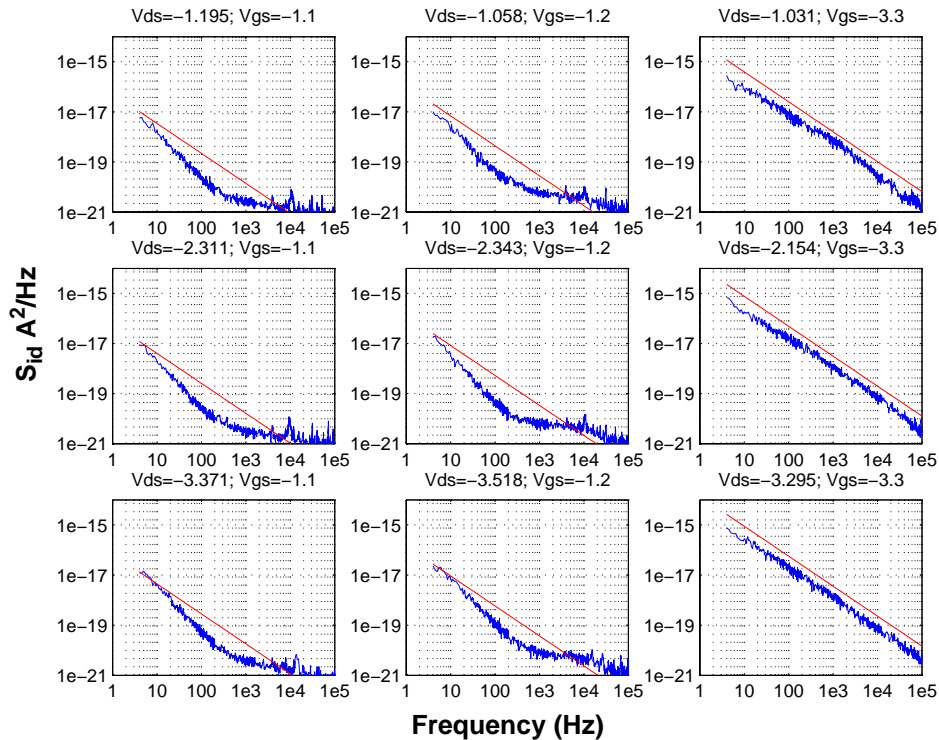
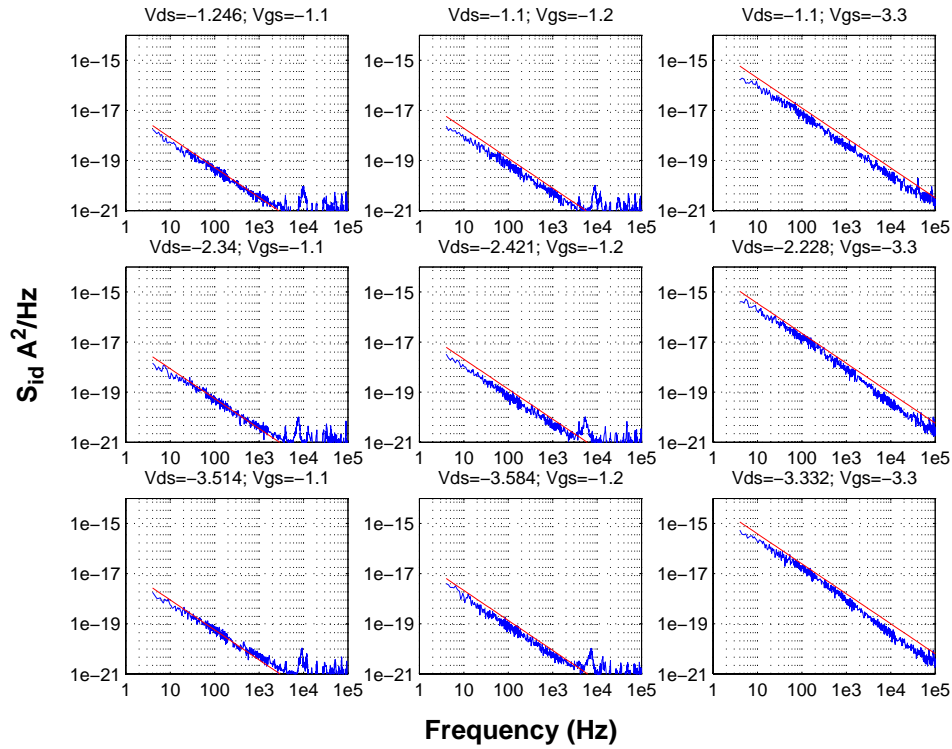
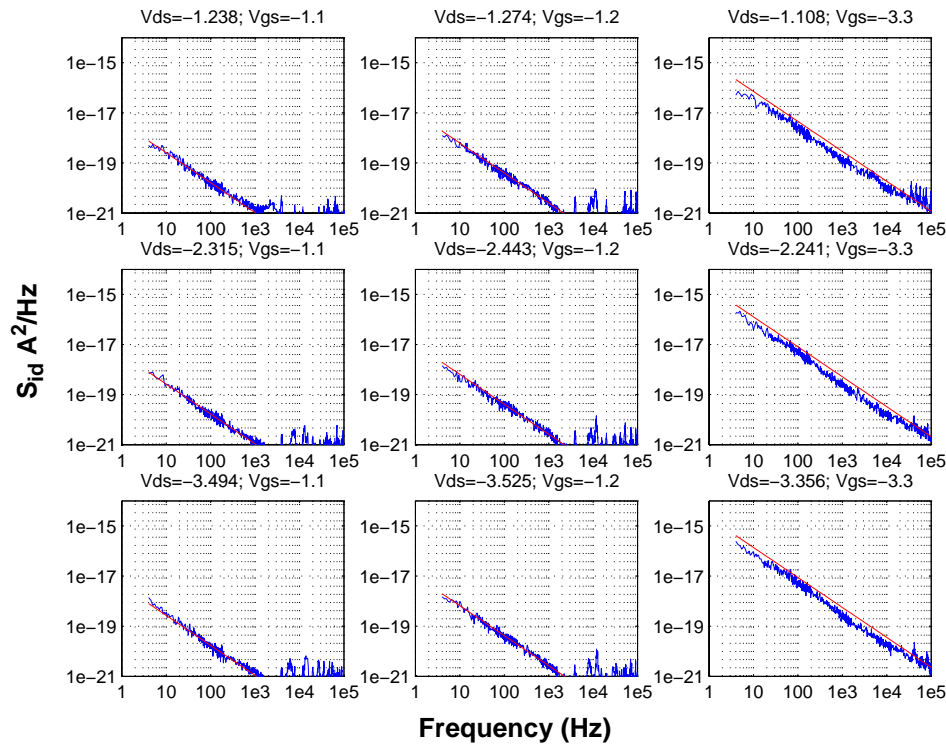


FIGURE 2.100 3p3_PFET_flicker_noise (NF/W/L = 1/10 μ m/0.6 μ m)FIGURE 2.101 3p3_PFET_flicker_noise (NF/W/L = 1/10 μ m/0.8 μ m)

2.8 Released model Quality Assurance (QA)

A rigorous QA procedure is executed before any new model release. The geometry dependence of 9 key device parameters is examined for any non-physical behavior for all 3 cases: Nominal, Fast, and Slow. These parameters are listed in Table 2.15 on page 76.

TABLE 2.15 MOSFET electrical parameters list examined as part of model release QA

Parameter	Description
v_t (V)	Threshold voltage in the linear region
k_b ($V^{0.5}$)	Body constant
i_{dsat} (mA)	Drain current at $V_{gs}=V_{ds}=V_{dd}$
st (mV/dec.)	Sub-threshold slope in the linear region evaluated at $V_{gs}=V_t/5$
β ($\mu A/V^2$)	Extracted from the max. g_m as: $1e6 \cdot (g_{m_max}/2 \cdot \text{abs}(v_d))$, where $\text{abs}(v_d)=0.05$ V is the drain voltage to bias the trans. in the linear region
g_{ds} (mhos)	Output conductance in the saturation region evaluated at $V_{gs}=V_{ds}=V_{dd}$
L_{eff} (μm)	Electrical channel length
W_{eff} (μm)	Electrical channel width
i_{off} (A)	Off-state leakage current at $V_{gs}=0$, $V_{ds}=V_{dd}$

Figures 2.102 through 2.105 illustrate the geometry dependence of these 9 parameters for the 1.2v and 3.3v N and P-FETs. For each devices 4 plots are generated as per Table 2.16. The right-hand most column in the table references the location of the plot. For e.g. the thin oxide NFET, electrical parameter vs. channel length for the 10 μm wide device is on the top-right of Figure 2.102.

TABLE 2.16 MOSFET channel lengths and widths included as part of QA procedure

Variable dimension	Fixed dimension	Location on plots (Figure 2.102 through Figure 2.105)
Channel length (min. design rule $< L < 10\mu m$)	Channel width = $10\mu m$	Top-left
Channel length (min. design rule $< L < 10\mu m$)	Channel width = Min. design rule	Top-right
Channel width (min. design rule $< W < 10\mu m$)	Channel length = $10\mu m$	Bottom-left
Channel width (min. design rule $< W < 10\mu m$)	Channel length = Min. design rule	Bottom-right

FIGURE 2.102 1p2_NFET_qa_plots

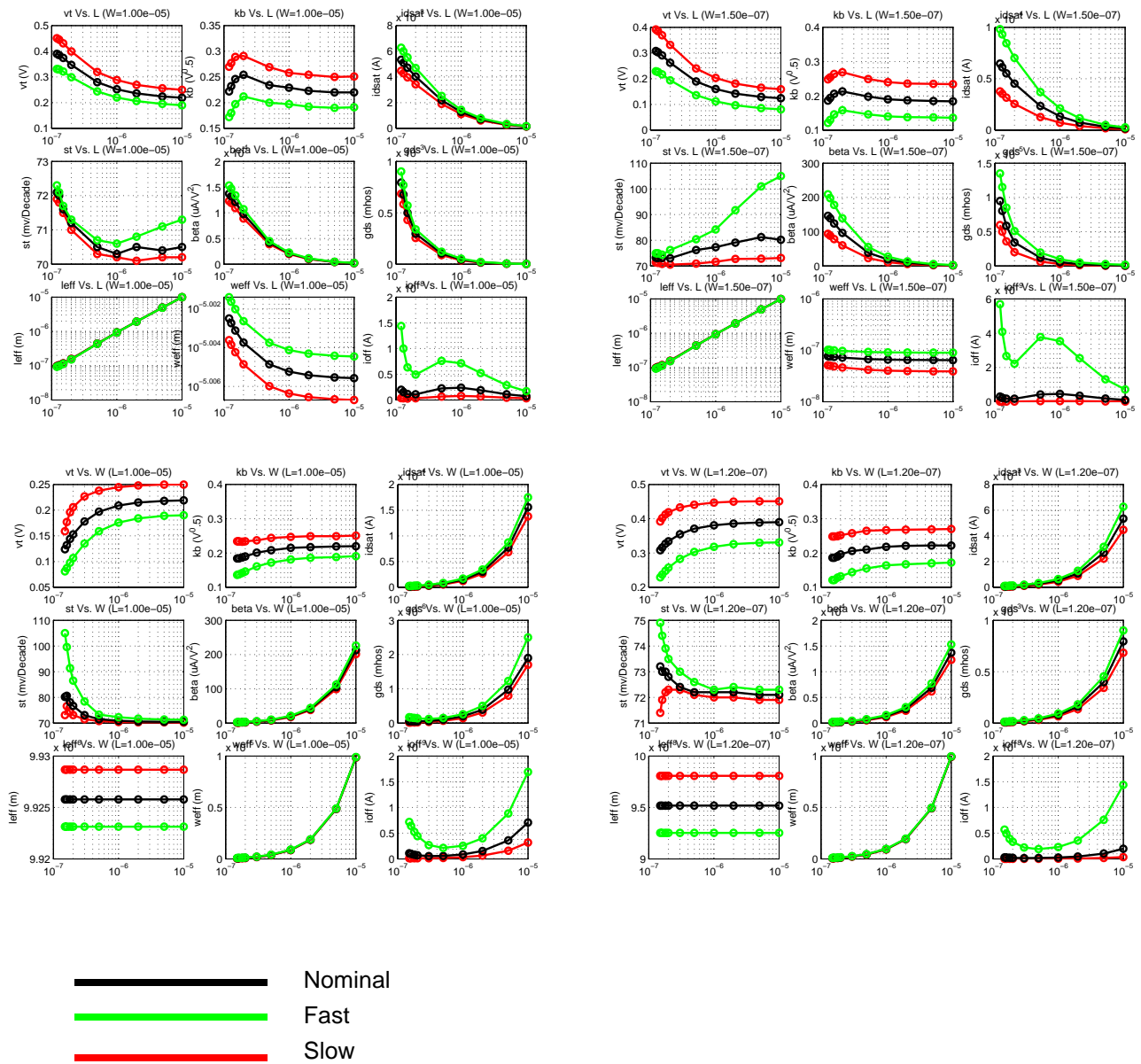


FIGURE 2.103 1p2_PFET_qa_plots

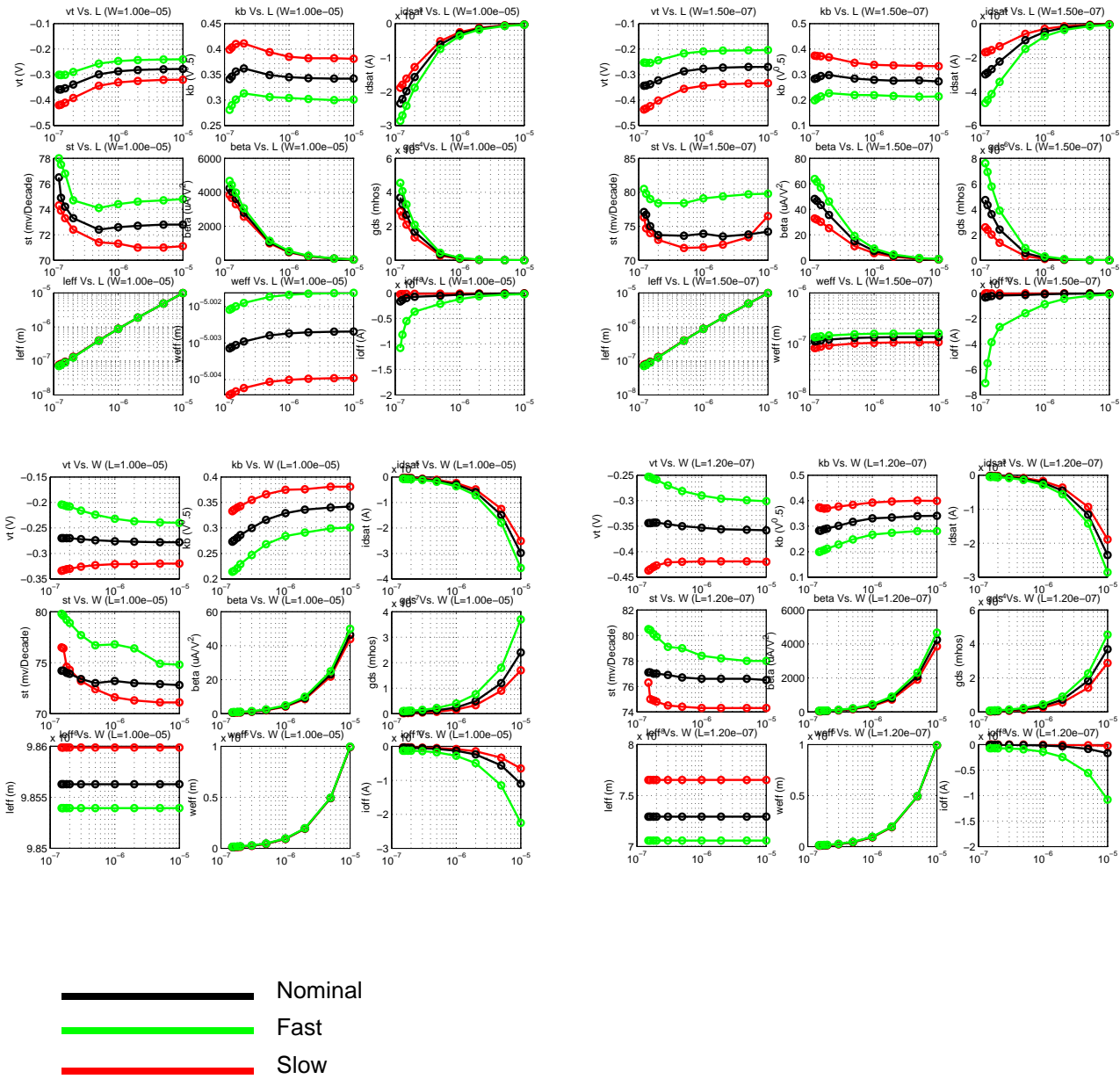


FIGURE 2.104 3p3_NFET_qa_plots

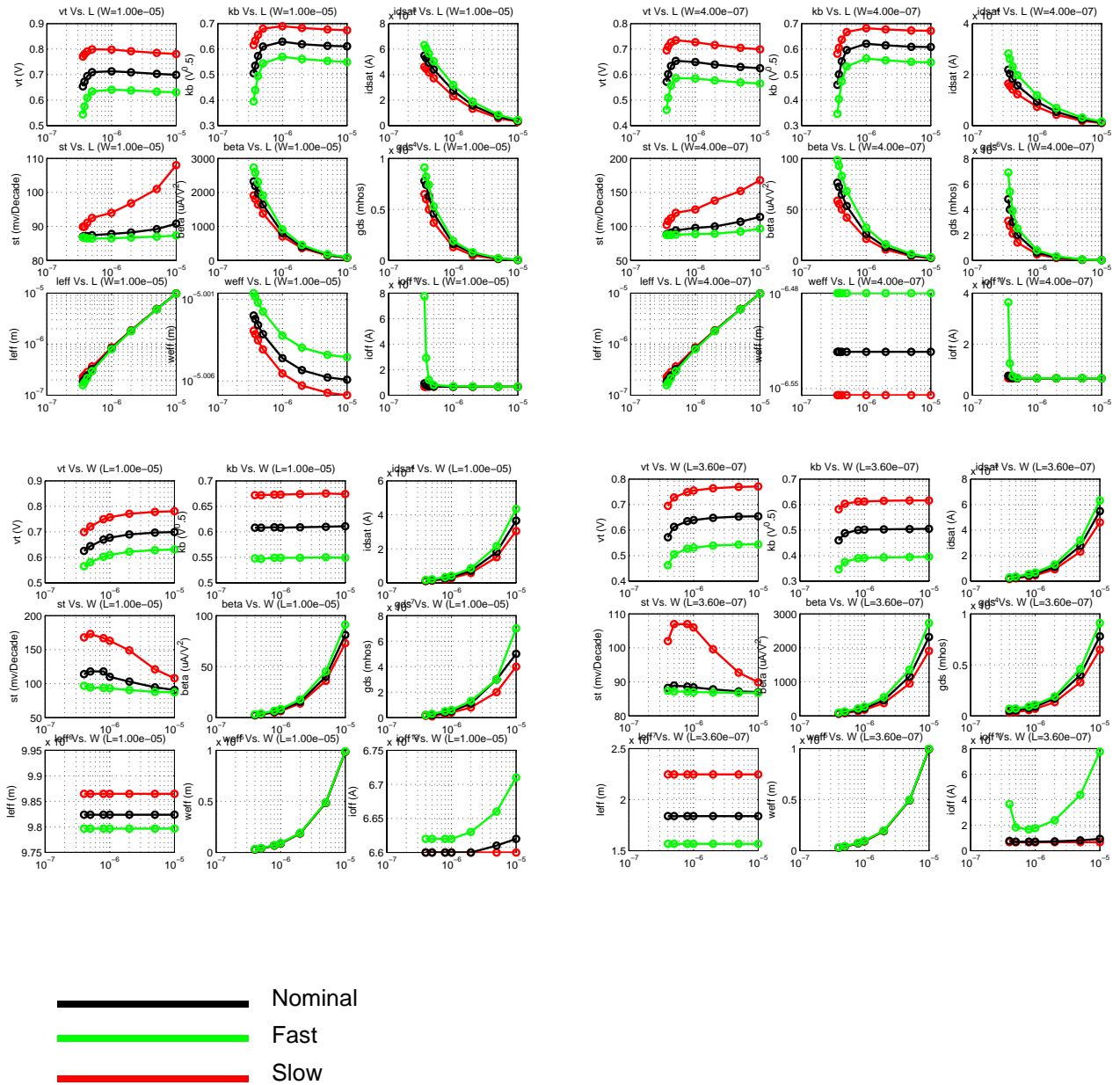
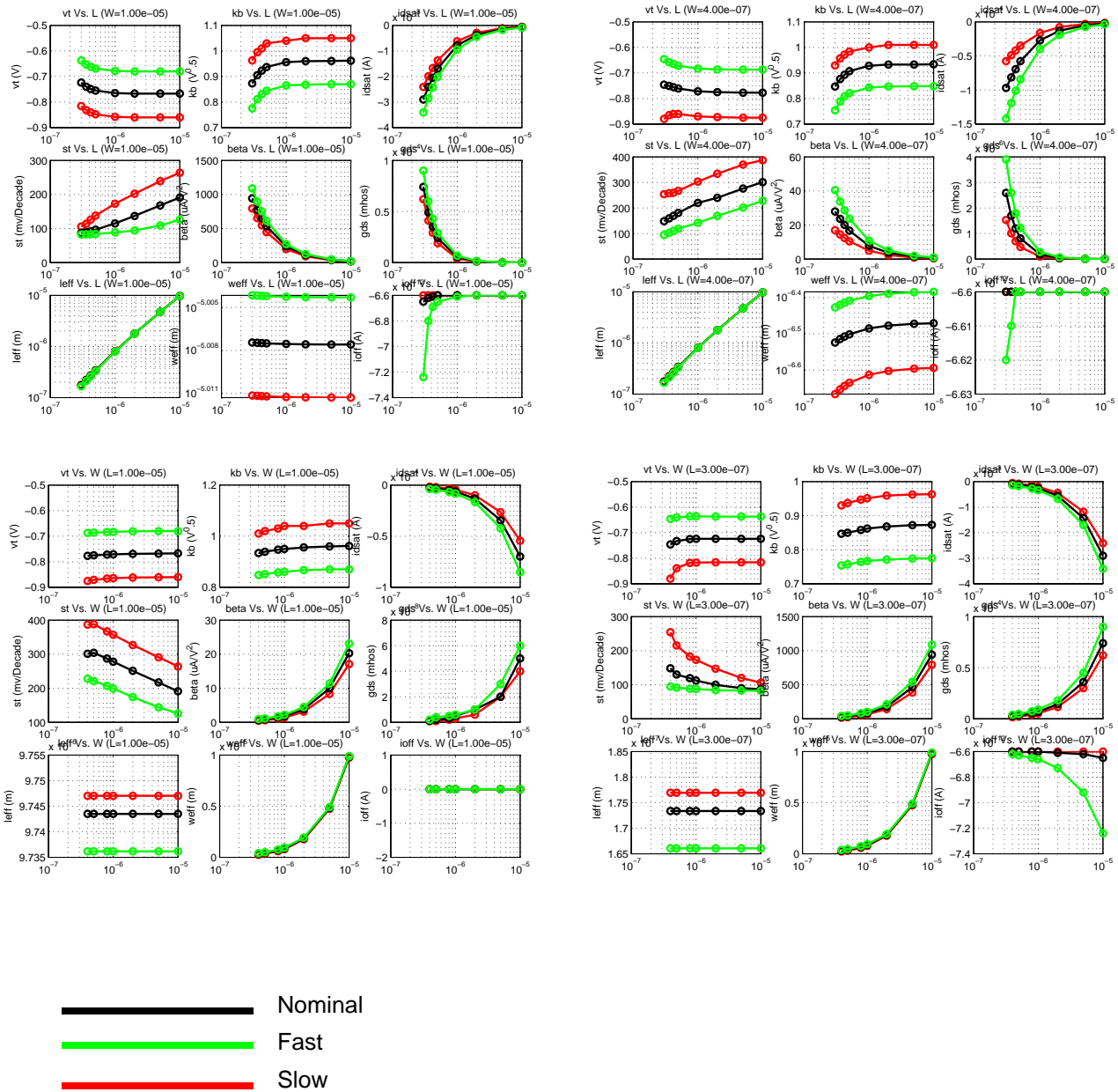


FIGURE 2.105 3p3_PFET_qa_plots



2.9 Model Update History

2.9.1 v1.0

First release of CA13 models.

2.9.2 v1.7

Re-extraction of 1.2v and 3.3v FET models from new silicon:

TABLE 2.17 Mixed-signal model specific updates in model release version 1.7

v1.7 update	Devices	Reason	Impact on user
Mixed-signal (DC) model	All 1.2v FETs	Better silicon available from mature process	Expected shifts in V_t , body effect, g_m and g_{ds} (o/p conductance)
Mixed-signal (DC) model BSIM3v3 -> BSIM4	All 3.3v FETs	Better silicon available from mature process; leverage improved modeling capabilities in BSIM4	Expected shifts in V_t , body effect, g_m and g_{ds} (o/p conductance)
Corner and statistical models	All 1.2 and 3.3v FETs	Aligned to new E-specs.	Shift in corner simulations; expect improved modeling of process variation
BSIM4 unified flicker noise model	All 1.2 and 3.3v FETs	Improved modeling of geometry and bias dependence	Significant shifts in magnitude of flicker noise at certain biases

2.9.3 v1.8

No changes

2.10 References

1. BSIM4 Modeling Package, Agilent 85194E, "<http://www.admos.de/bsim4.html>"
2. T. Gneiting, "A Unified Environment for the Modeling of Ultra Deep Submicron MOS Transistors," Nanotech 2003 Conference
3. Colin C. McAndrew, "Statistical Circuit Modeling," SISPAD 98

3.0 RF CMOS Model

3.1 Model List and Description

The CA13/SBL13 processes supports two different RF models. The first model relates to the thin gate-oxide FETs with a maximum operation voltage of 1.2v. The second model relates to the thick gate-oxide FETs with a maximum operation voltage of 3.3V.

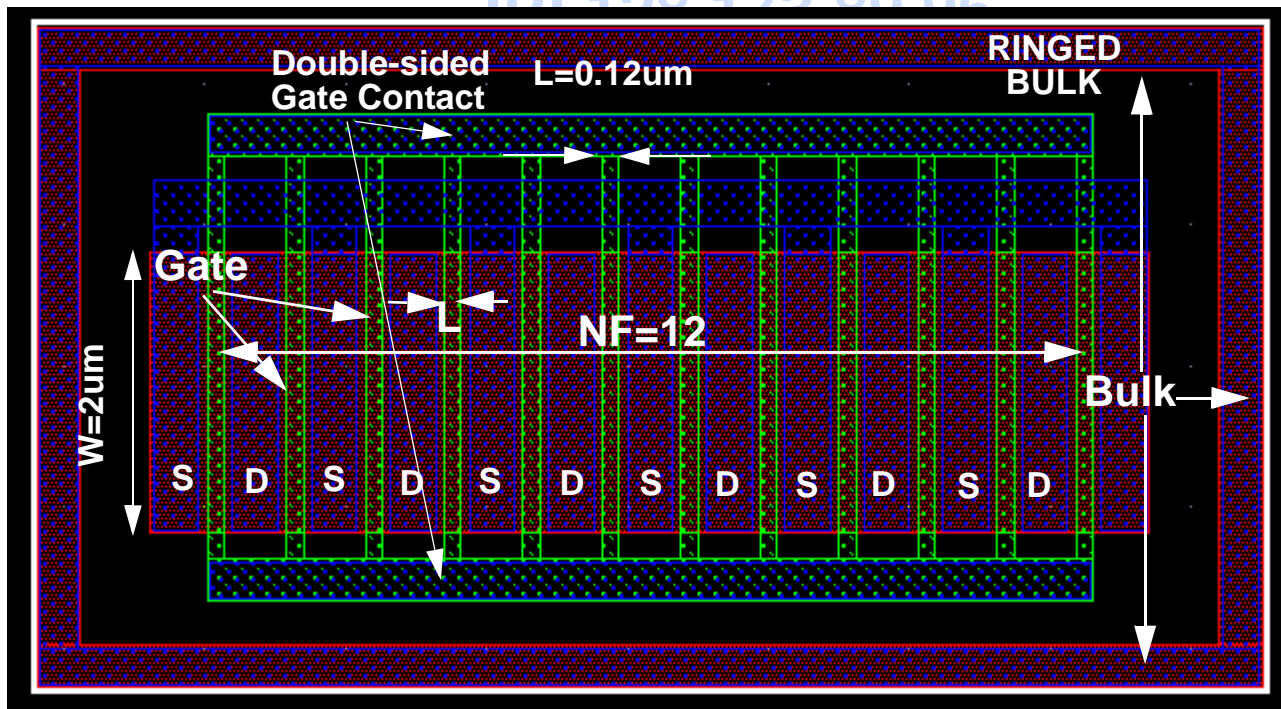
TABLE 3.1 1.2v and 3.3v RF FET model summary

Property	Thin-oxide (1.2v) Fets	Thick-oxide (3.3v) Fets
Model name	nfet_rf, pfet_rf	nfet3p3_rf, pfet3p3_rf
Temperature range	25°C	25°C
Channel length	$0.12\mu\text{m} \leq L < 0.5\mu\text{m}$	$0.36 \text{ (0.3 for pfet3p3)} \mu\text{m} \leq L < 0.5\mu\text{m}$
Channel width	$2\mu\text{m} \leq W < 10\mu\text{m}$	$2\mu\text{m} \leq W < 10\mu\text{m}$
No. of fingers	$1 \leq NF \leq 100$	$1 \leq NF \leq 100$
Bias range	$ V_{gs} : 0 \sim 1.2\text{V}, V_{ds} : 0 \sim 1.2\text{V}, V_{bs} : 0 \sim 1\text{V}$	$ V_{gs} : 0 \sim 3.3\text{V}, V_{ds} : 0 \sim 3.3\text{V}, V_{bs} : 0 \sim 3\text{V}$

Using these models outside of the specified ranges may generate simulation errors. The RF model is based on the core MS model which has been validated for temperatures from -40 to 125°C. Though no RF model validation is performed at temperatures other than 25°C, the RF model should provide a reasonable estimate of RF properties when simulated at temperatures in -40 to 125°C range.

3.2 Layout

FIGURE 3.1 Layout of RF MOSFET. NF= number of fingers, L= channel length, W = channel width, S = Source, D = Drain



The top view of a RF MOSFET is shown in Figure 3.1 with the key design parameters (NF, L, and W). Note that the total width of the RF MOSFETs is equal to NF*W. RF transistors are typically laid out as multi-finger devices to minimize gate resistance and parasitic junction effects. These improvements translate into higher cutoff (f_t) and maximum oscillation frequencies (f_{max}), as well as lower device noise. The gate resistance R_g can further be improved by contacting the gate on multiple sides as per Eq. 1.

$$R_g = W \cdot \frac{R_{polySheet}}{NF \cdot 3 \cdot L \cdot N_{gc}^2} + \frac{\rho_c}{NF \cdot W \cdot L} \quad (\text{Eq. 1})$$

where $R_{polySheet}$ is the silicided poly sheet resistance, N_{gc} is the number of sides that the gate is contacted from, and ρ_c is the contact resistance per unit area between the silicide and the polysilicon gate, and represents an additional component of the gate resistance (Figure 3.2), dominant for narrow widths ($< 3\mu\text{m}$). The factor 3 is due to the distributed nature of this resistance at high frequencies. The p-cell N_{gc} defaults to a value of 1, consistent with the default “top-sided” gate connection. The user can, however, choose a double-sided gate contact by checking the “Both” option under the “**Gate Connection**” cdf variable, as shown in Figure 3.3. The reduced gate resistance might be useful in applications where a large f_{max} or low gate noise is desirable. The interconnect (metal wiring to the intrinsic FET) resistance is not shown in Figure 3.2. This can be an important component of the gate resistance, and should be included in the post-extraction simulation of the FETs. The RF FET model includes any resistance associated with metal wiring inside the active area of the RF FET, consistent with the 2met(RF) or 2met option in the CDF.

Like the gate resistance, the substrate resistance is also layout dependent. The default model for both the 1.2v and 3.3v RF FETs is for a ring of substrate contacts around the active FET, and corresponds to the “**Detached**” Bodytie Type with “lbrt” Tap Style (Left, Right, Top, and Bottom), as shown in Figure 3.3. The 2-sided substrate model is also available corresponding to the “**Detached**” Bodytie Type and “lr” Tap Style (Left and Right). The use of a ringed substrate can significantly reduce the “roll-up” in drain-source conductance g_{ds} (or reduction of output resistance r_o) at high frequencies. One-sided contacts or two-sided contacts on the top and bottom are not supported in the model.

FIGURE 3.2 Components of the gate resistance in a RF-FET

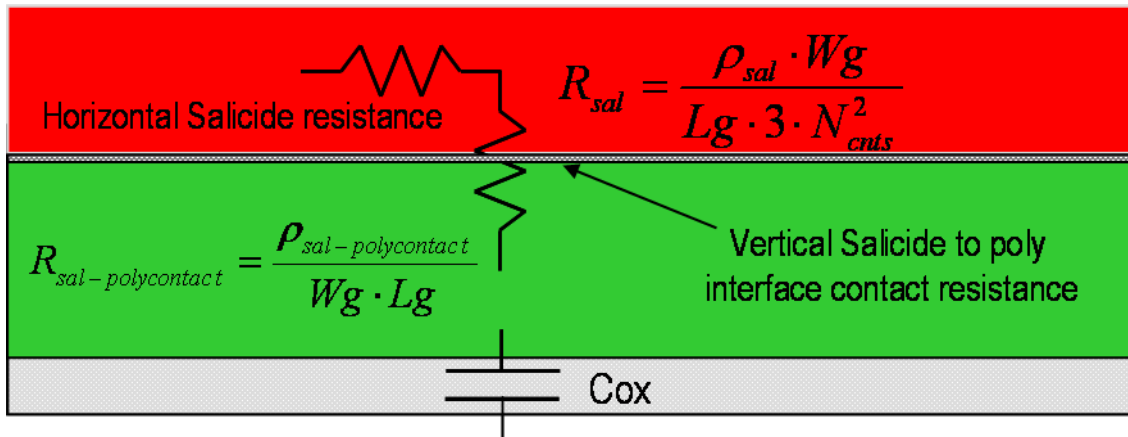


FIGURE 3.3 CDF selection options for RF FETs

Edit Instance Properties

OK Cancel Apply Next Previous Help

☐ Attribute ☐ Connectivity ☒ Parameter ☐ Property ☐ ROD ☐ Common

Multiplier: 1

Length: 120.0

Total Width: 10

Finger Width: 10

Fingers: 1

Threshold: 20

Apply Threshold: ☐

Gate Connection: ☐ None ☒ Top ☐ Bottom ☐ Both ☐ /

Style: ☐ unconnected ☐ 1met ☒ 2met(RF)

Current: 0

Number of Slices: 1

S/D Metal Width: 320.0

use ABLB overplots: ☐

Bodytie Type: Detached

Tap Style: lbrt

Tap Extension: 1

Show Sim Parameters: ☐

Simulation parameters update

Gate connection (Ngc in Eq. 1):
Top: Ngc = 1 (Default)
Bottom: Ngc = 1
Both: Ngc = 2
Alternate: Ngc = 1

Style: RF FETs used for model extraction use the "2met(RF)" options, and include all metal resistance inside the active FETs. Resistance calculation errors introduced when using "1met" and "unconnected" options depend on the wiring scheme used. Metal resistance outside active FET is included in the post-extraction analysis.

Bodytie Type: Layout supports multiple options. Models support only detached option with Tap style either "lbrt" (4-sided "ringed") or "lr" (2-sided left and right).

3.3 Measurements

Transistors with multiple widths, channel lengths and number of fingers were measured to extract a model that is scalable over a large geometry space. Measurements were made on Ground-Signal-Ground test-structures with a 150 μm pitch between the pads. The list of transistors measured for the thin and thick-oxide FETs is shown in Table 3.2. The s-parameters of the RF MOSFETs, were measured on HP 8510C network analyzer. The frequency was swept from 0.1 to 20GHz. The list of biases for the thin and thick-oxide FETs is shown in Table 3.4.

TABLE 3.2 List of 1.2v devices measured for RF model extraction

Type	NF \times W \times L (μm)
Length Scale	16 x 2 x 0.12, 0.14, 0.2, 0.4, 0.6
Width Scale	16 x 1, 2 ^{1,2} , 3, 5, 7, 10 ¹ x 0.12
No. of Finger (NF) Scale	1, 4, 5, 8, 11, 16, 32, 64 ² x 2 x 0.12
Additional Devices	1x10x0.12, 1x10x0.2, 1x10x0.4, 1x10x0.2, 32x2x0.2
Notes: All devices have 2-sided contacts to gate and 4-sided (ringed) substrate contacts, with the following additional layouts for the marked devices: 1. Single-sided gate contact 2. 2-sided "lr" substrate contact	

TABLE 3.3 List of 3.3v devices measured for RF model extraction

Type	NF \times W \times L (μm)
Length scale	16 x 2 x 0.3 (PFET only), 0.36, 0.42, 0.6, 0.8
Width scale	16 x 1, 2, 5, 10 x 0.36 (0.3 for PFET)
No. of finger (NF) scale	1, 5, 8, 16, 32, 64 x 2 x 0.36 (0.3 for PFET)
Additional devices (NFET)	1x10x0.3 (PFET only) 1x10x0.36, 1x10x0.6, 1x10x0.8, 16x5x0.6

TABLE 3.4 List of biases at which s-parameters were measured for the 1.2 and 3.3v NFETs (TYPE=1) and PFETs (TYPE=-1)

1.2v		3.3v	
Vgs(V)	Vds (V)	Vgs (V)	Vds (V)
0	TYPE*0,0.4,0.8,1.2	0	TYPE*0,0.66,1.32,1.98,2.64,3.3
TYPE*0.25	TYPE*0,0.4,0.8,1.2	TYPE*0.825	TYPE*0,0.825,1.65,2.475,3.3
TYPE*0.5	TYPE*0,0.4,0.8,1.2	TYPE*1.65	TYPE*0,0.825,1.65,2.475,3.3
TYPE*0.75	TYPE*0,0.4,0.8,1.2	TYPE*2.475	TYPE*0,0.825,1.65,2.475,3.3
TYPE*1	TYPE*0,0.4,0.8,1.2	TYPE*3.3	TYPE*0,0.825,1.65,2.475,3.3

3.4 Modeling

The BSIM4 model described in the chapter "MOSFET Model" on page 10 is valid at low frequencies (< 200MHz). At higher frequencies, the coupling between the source and drain through the bulk and the distributed resistance and capacitance effects require the gate, substrate and source/drain coupling networks to be explicitly included. The core mixed-signal (MS) model can be extended for use at high frequencies by adding parasitic resistances and capacitances as shown in Figure 3.4. The gate resistance R_g is modeled via Eq. 1 and has a direct impact on the input admittance [1]:

$$Re(Y_{11}) \sim R_g \cdot Im(Y_{11})^2 \quad (\text{EQ 2})$$

where $Im(Y_{11}) \sim \omega \cdot C_{gate}$.

The substrate network consists of 5 resistances:

R_{bpd} and R_{bps} capture the drain/source to internal bulk coupling, and are modeled as:

$$R_{sb} = R_{sbSheet} \times \frac{L}{(2 \times W \times NF)} \quad (\text{EQ 3})$$

$$R_{db} = R_{dbSheet} \times \frac{L}{(2 \times W \times NF)} \quad (\text{EQ 4})$$

where $R_{sbSheet} = R_{dbSheet}$, is the sheet resistance of the region that couples the ac signal from the source to the drain, and is fit to the measured data. The well resistance from the internal bulk to the external bulk contact is modeled via the horizontal and vertical components (Eqs. 5 and 6):

$$R_{dsbv} = R_{dsbSheet} \times \frac{(W/2 + W_{act2act} + W_{act2con})}{2 \times (L + 2 \times (W_{con2gate} + W_{con} + W_{act2con})) \times NF} \quad (\text{EQ 5})$$

where, R_{dsbv} is the vertical component of substrate resistance to the top and bottom taps, $R_{dsbSheet}$ is the sheet resistance of the well and is extracted from the measured s-parameter data, $W_{act2act}$ is the distance between the active regions of the FET and substrate contacts ($1\mu\text{m}$), $W_{act2con}$ is the minimum design rule for the active to contact ($0.07\mu\text{m}$), $W_{con2gate}$ is the distance between contact and gate ($0.11\mu\text{m}$), and W_{con} is the width of the contact ($0.16\mu\text{m}$).

$$R_{dsbh} = R_{dsbSheet} \times \frac{(L/2 + W_{con2gate} + W_{con} + W_{act2con} + W_{sti} + W_{act2con})}{2 \times W} \quad (\text{EQ 6})$$

where R_{dsbh} is the horizontal component of the substrate resistance to the left and right taps, and W_{sti} is the width of the isolation. R_{dsbh} is calculated for the two outermost fingers of the RF FET, as the contribution from the inner fingers has negligible impact on this resistance for layouts with $NF > 4$. The substrate resistance of the RF FETs is either:

$$R_{dsb} = R_{dsbh} \quad (\text{EQ 7})$$

for a 2-sided substrate contact (corresponding to Tap Style "lr" in Figure 3.3), or

$$R_{dsb} = R_{dsbh} \parallel R_{dsbv} \quad (\text{EQ 8})$$

for a 4-sided "ringed" substrate contact (corresponding to Tap Style "lbrt" in Figure 3.3) and is modeled as 3 separate resistors - R_{bpd} , R_{bdb} , and R_{bsb} , representing the well resistance components from the internal bulk, drain, and source to the external bulk contact.

Collectively the substrate network (R_{sub}) impacts the output impedance:

$$R_{sub} \sim Re(Y_{22})/(\omega^2 \cdot C_{db}) \quad (\text{EQ 9})$$

The transmission parameter from gate to drain:

$$Y_{12} \sim -j\omega C_{gd} - \omega^2 \cdot C_{gd} \cdot C_{gg} \cdot R_g \quad (\text{EQ 10})$$

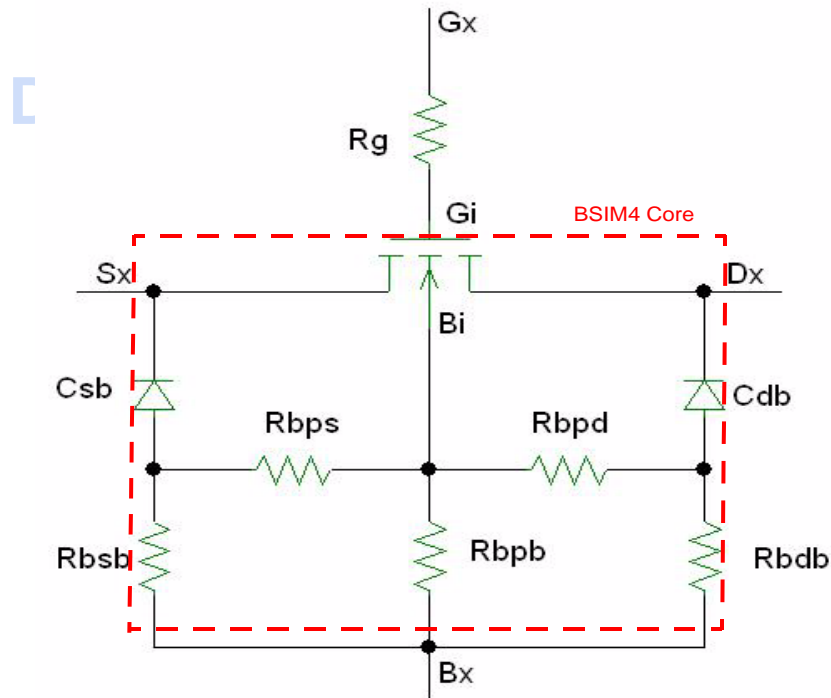
where C_{gd} is the overlap capacitance extracted at low-frequency as described in Section 2.3.2 on page 14. The drain resistance impacts the reverse transmission parameter from drain to gate:

$$Y_{21} \sim -j\omega C_{gd} - \omega^2 \cdot (C_{gd}^2 \cdot R_d + C_{gd} \cdot C_{gg} \cdot R_g) \quad (\text{EQ 11})$$

The drain and source resistances and their associated gate-bias dependencies are included in the core MS model and are not explicitly modeled in the sub-circuit. Modeling these resistors as extrinsic lumped elements in the sub-circuit results in inaccurate predictions of g_m and g_{ds} ; essential in both ac and noise simulations.

The BSIM4 gate resistance model ignores the silicide to poly contact resistance (Section 3.2). This necessitates the use of an external gate resistance, as shown in Figure 3.4 and specified by Eq. 1.

FIGURE 3.4 Circuit schematic of the RF NFET model



3.5 Statistical and Corner Models

The core mixed-signal (DC) corner and statistical model parameters in the RF sub-circuit extension are identical to what was described in Section 2.5 on page 57 respectively, and are valid at higher frequencies. In addition, the sheet resistance of the silicided poly and the contact resistivity of the silicide-polysilicon interface is changed by $\pm 25\%$ for the SLOW/FAST corner cases. Similarly, a $\pm 25\%$ variation is used to model the 3σ variation of these parameter in the statistical models. The 3σ variation of the silicided poly sheet resistance is consistent with E-specs specified for silicided poly resistors in Table 8.3. The variation of the substrate resistance is modeled in a manner consistent with the channel doping variation in the statistical model.

3.6 F_t and Y-parameter Playbacks

The measured F_t as a function of drain current of the RF FETs is compared with the simulated values in Figures 3.5 through 3.8.

The simulated y-parameters are compared with the measured data in Figures 3.9 through 3.28. Two bias regimes are shown; the first is for “cold” MOSFETs with $V_{ds}=V_{gs}=0v$, while second is in saturation with V_{gs} above the threshold voltage of the device. The device description is included in the figure caption using the notation: max_operating_voltage_fetType_NFxWxL. For example, 1p2_NFET_16x2x0p12 represents the 1.2v RF NFET with 16 fingers, each which is $2\mu m$ wide and $0.12\mu m$ long. Y-parameters are shown since they lend better meaning to the device performance than s-parameters. Finally, the blue circles are the measurements and the solid red lines are the simulated model. The measured data has not been de-embedded; simulated data includes the extracted equivalent structure of the GSG pads.

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FIGURE 3.5 1p2_NFET_FtVsId_Vd_1.2v

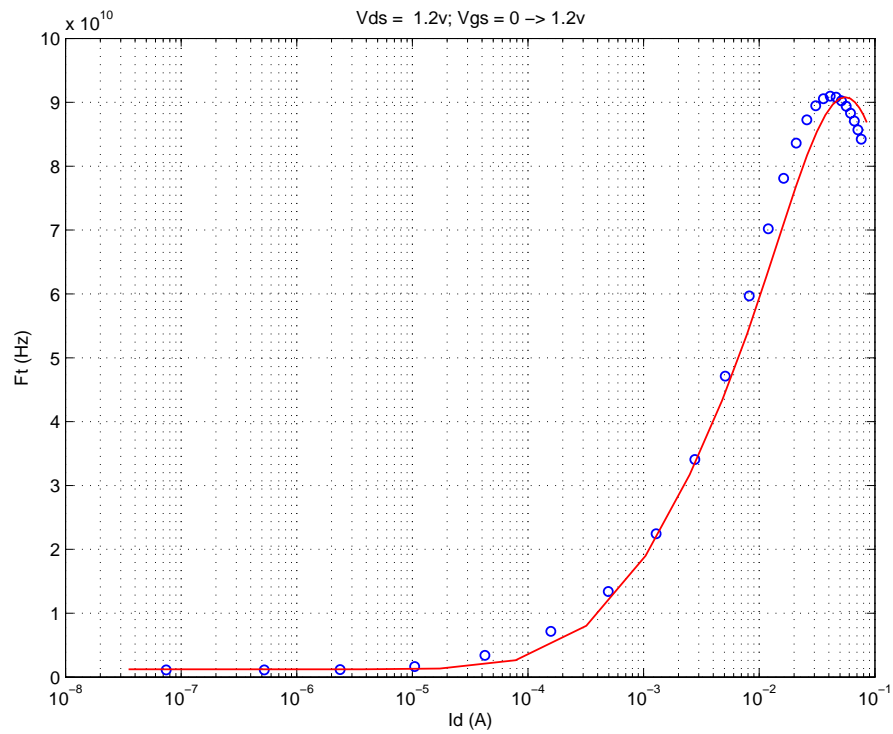


FIGURE 3.6 1p2_PFET_FtVsId_Vd_-1.2v

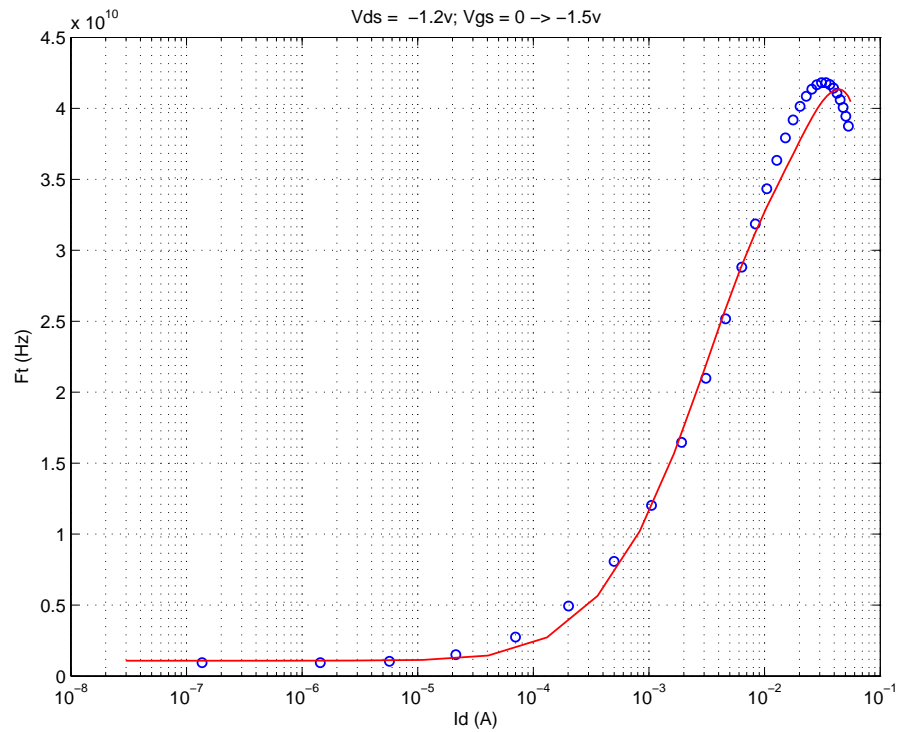


FIGURE 3.7 3p3_NFET_FtVsId_Vd_3.3v

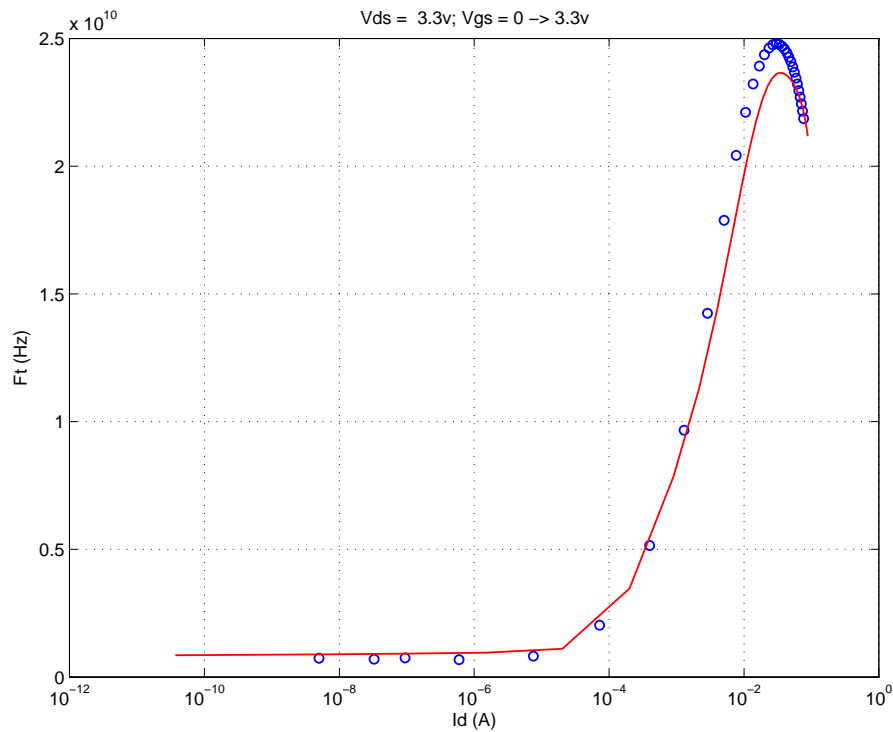


FIGURE 3.8 3p3_PFET_FtVsId_Vd_-3.3v

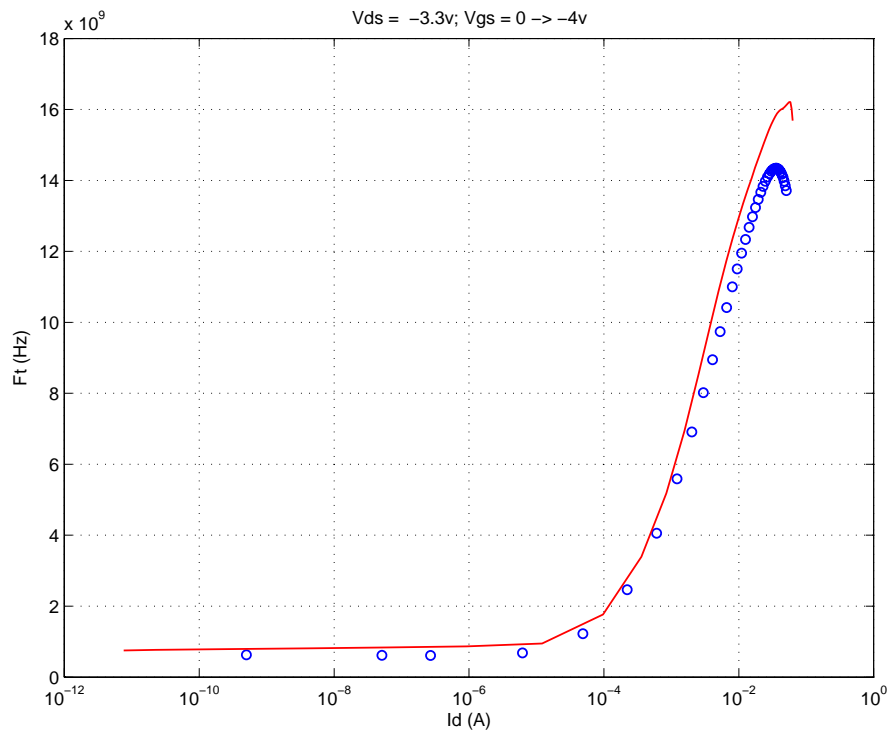


FIGURE 3.9 1p2_NFET_16x2x0p12 with 2-sided gate contact and ringed-substrate

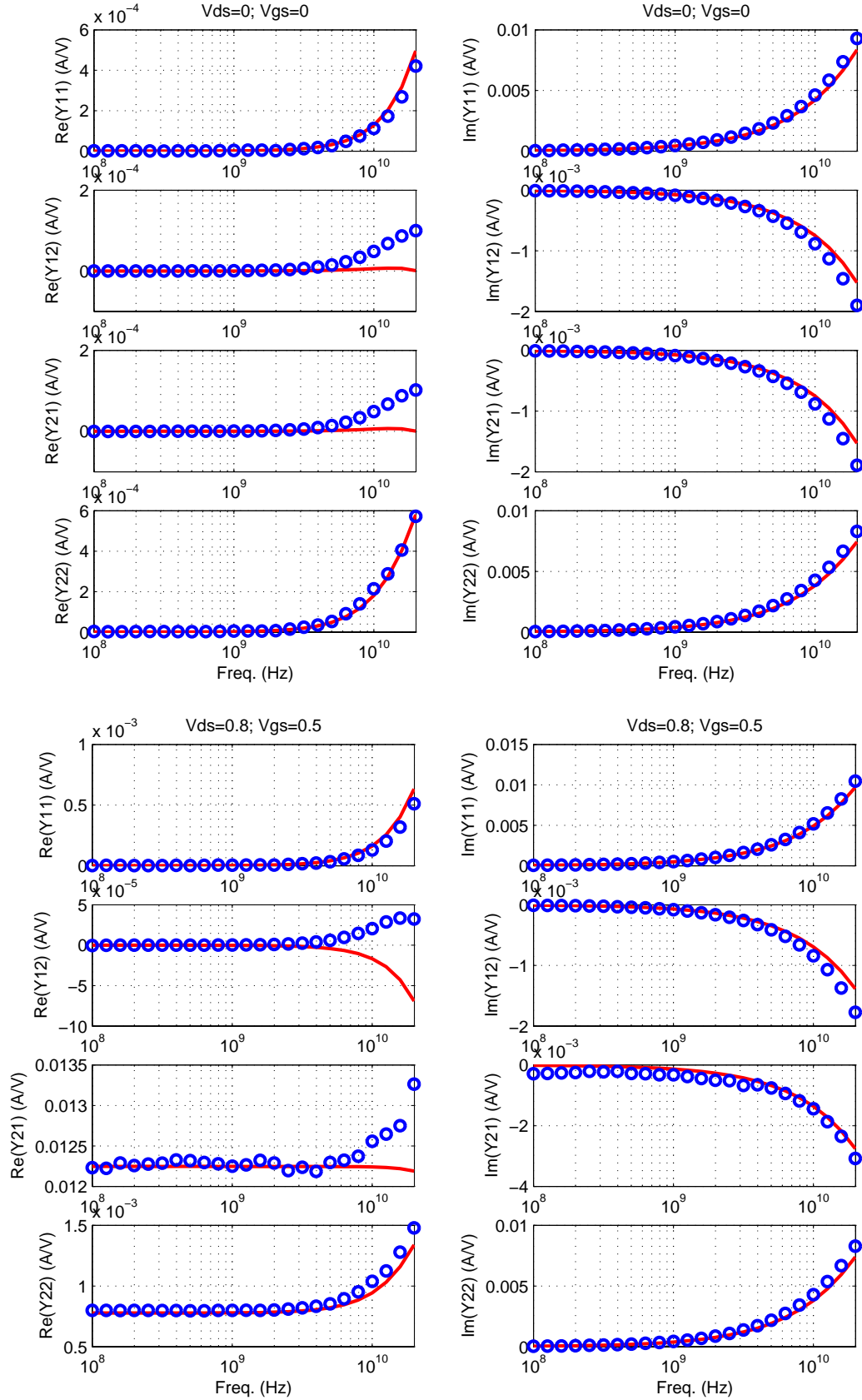


FIGURE 3.10 1p2_NFET_64x2x0p12 with 2-sided gate contact and ringed-substrate

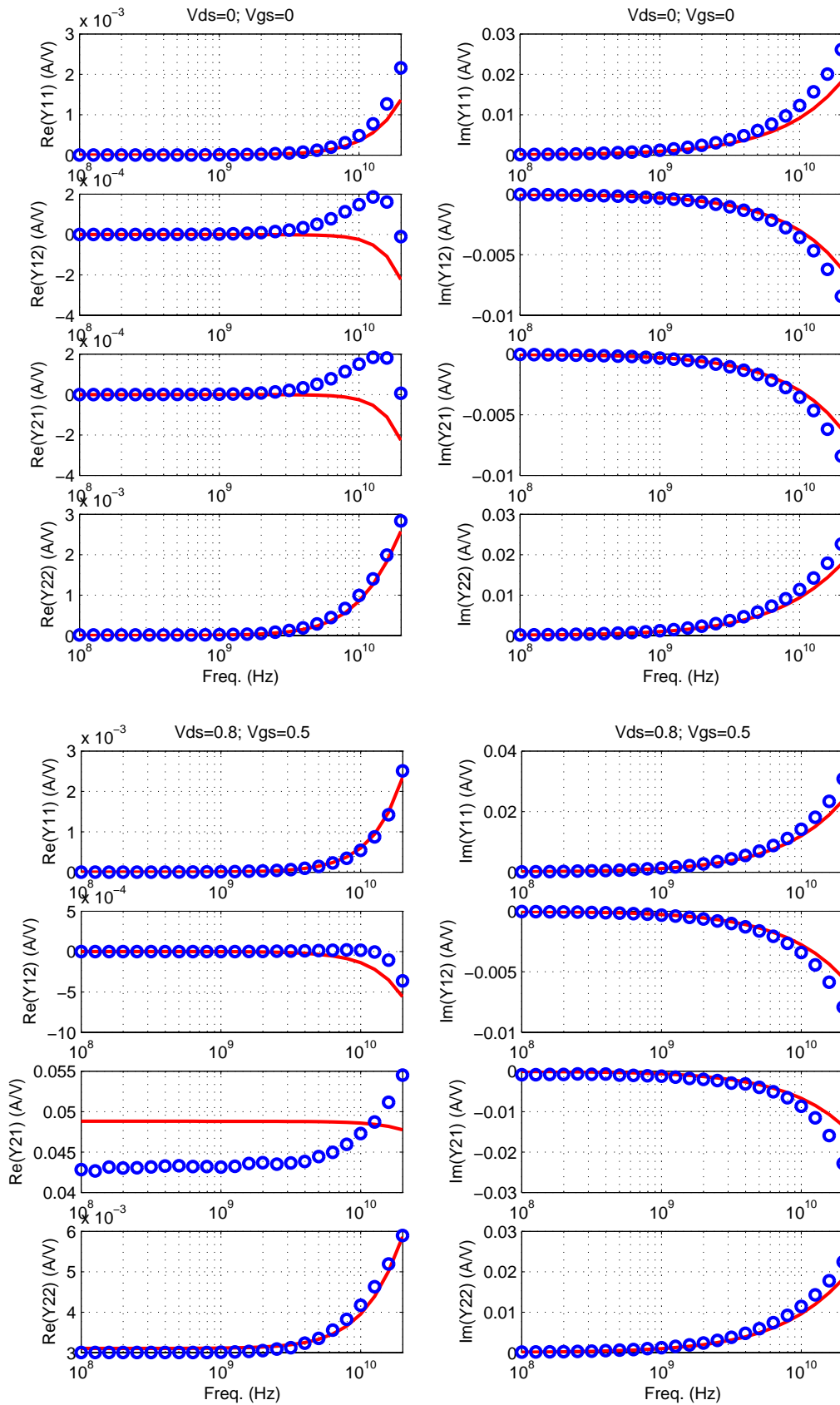


FIGURE 3.11 1p2_NFET_4x2x0p12 with 2-sided gate contact and ringed-substrate

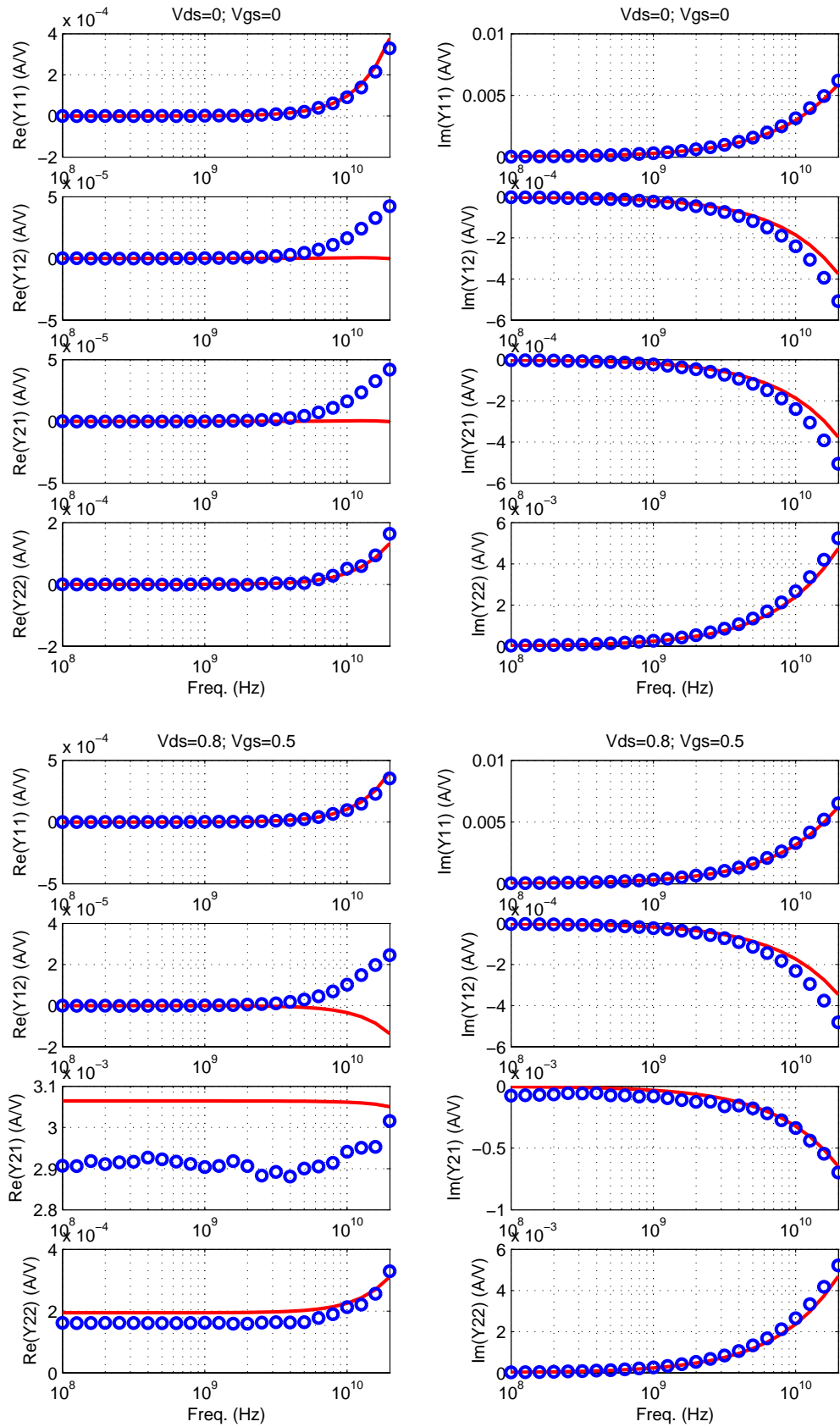


FIGURE 3.12 1p2_NFET_16x2x0p2 with 2-sided gate contact and ringed-substrate

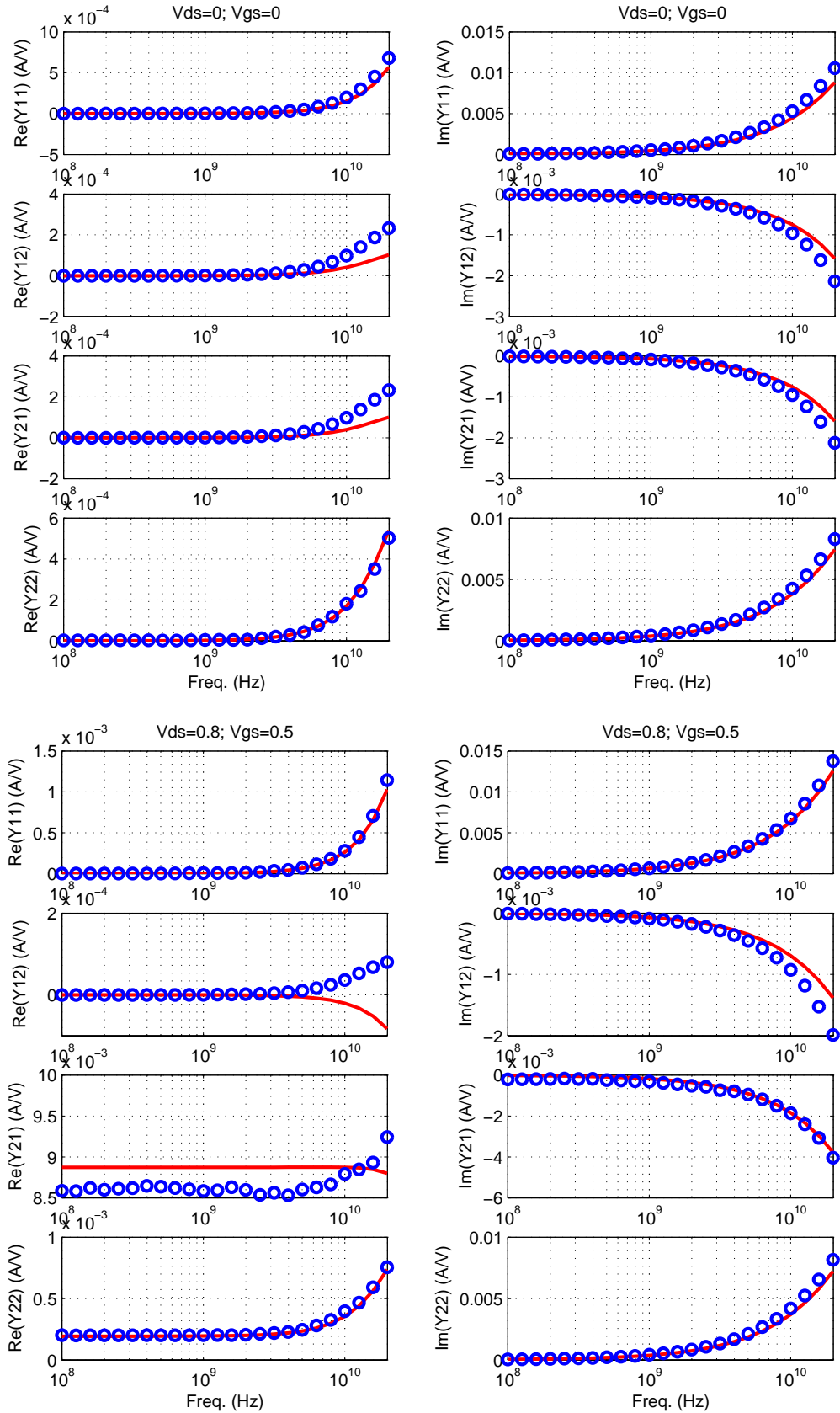


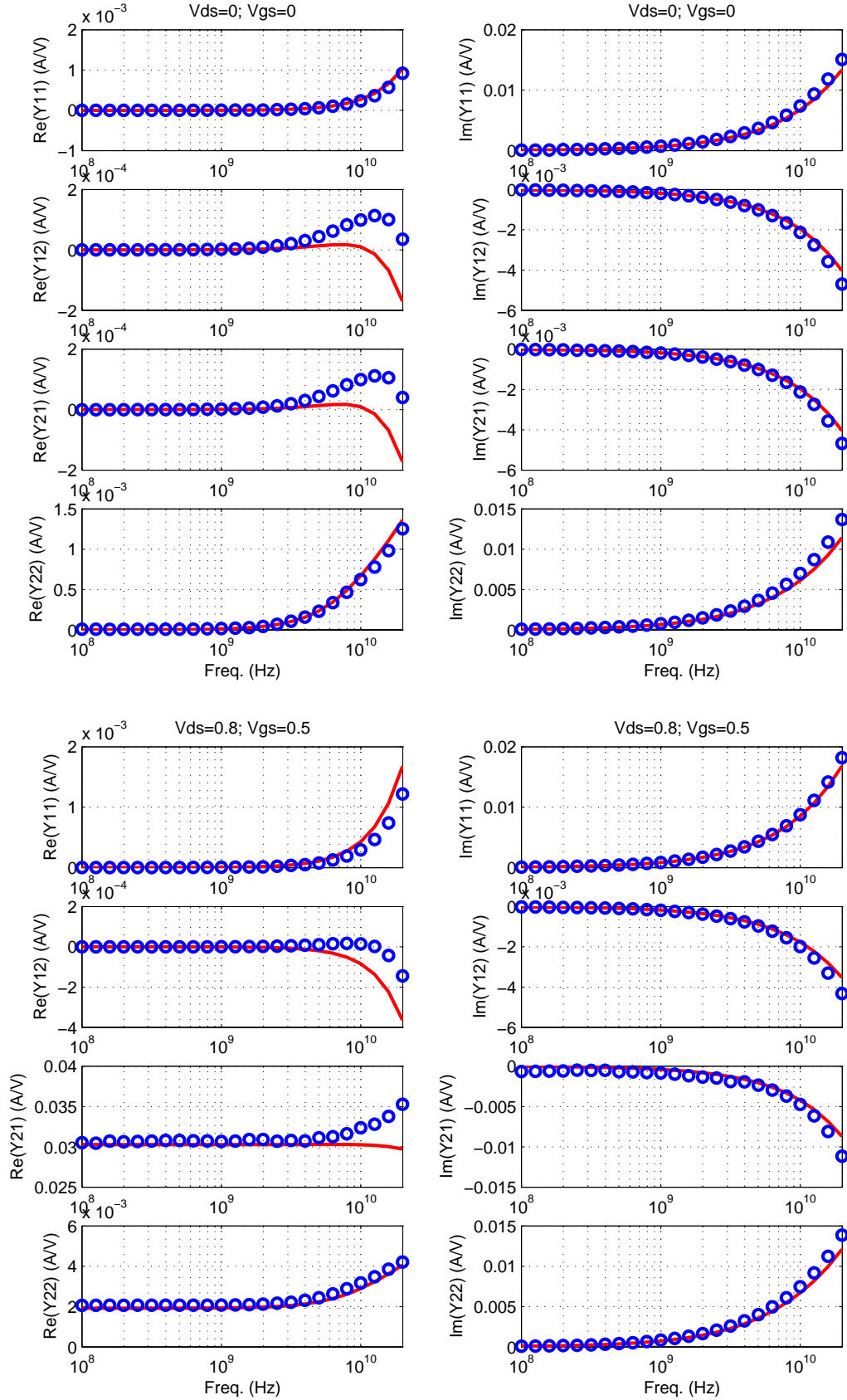
FIGURE 3.13 1p2_NFET_16x5x0p12 with 2-sided gate contact and ringed-substrate

FIGURE 3.14 1p2_PFET_16x2x0p12 with 2-sided gate contact and ringed-substrate

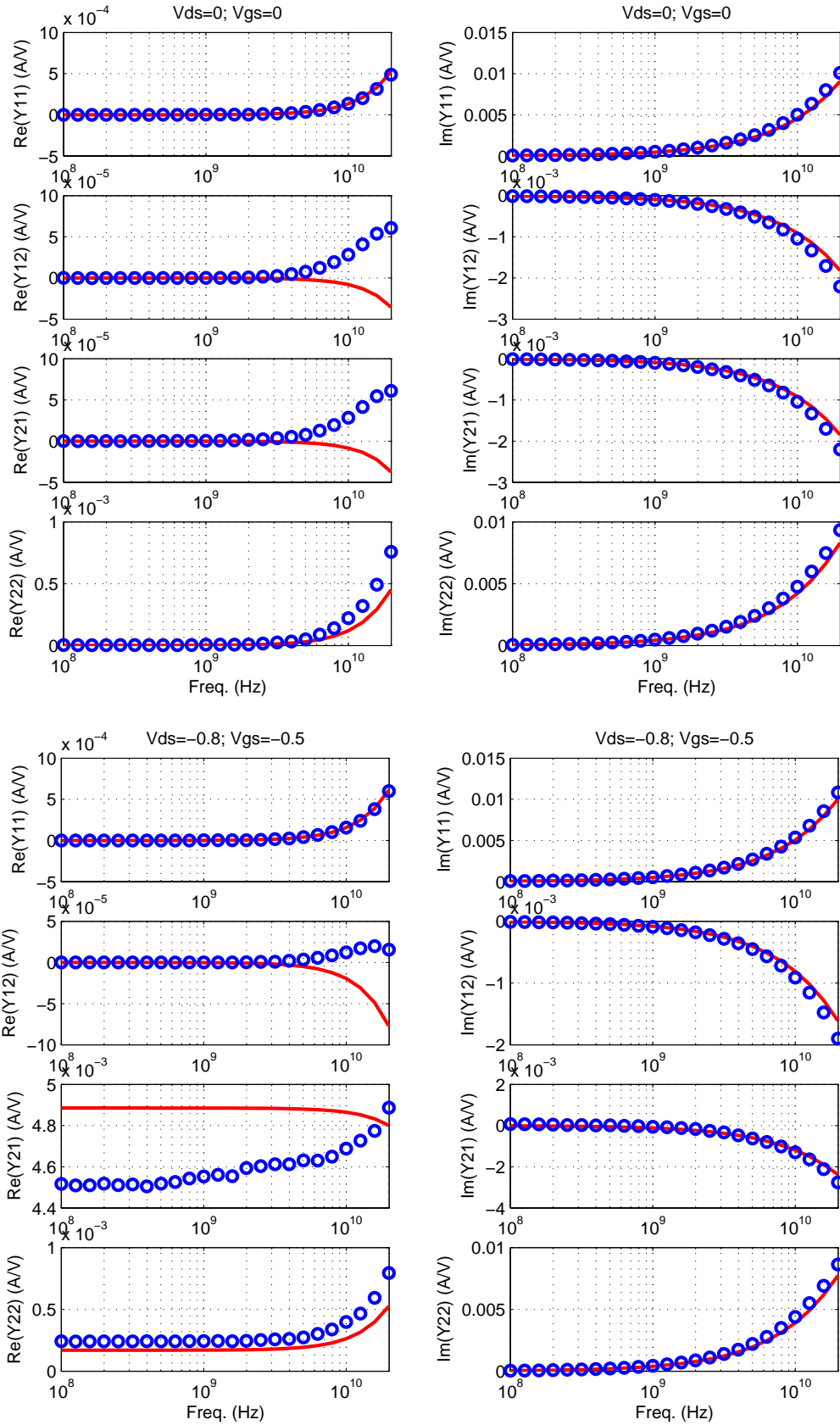


FIGURE 3.15 1p2_PFET_64x2x0p12 with 2-sided gate contact and ringed-substrate

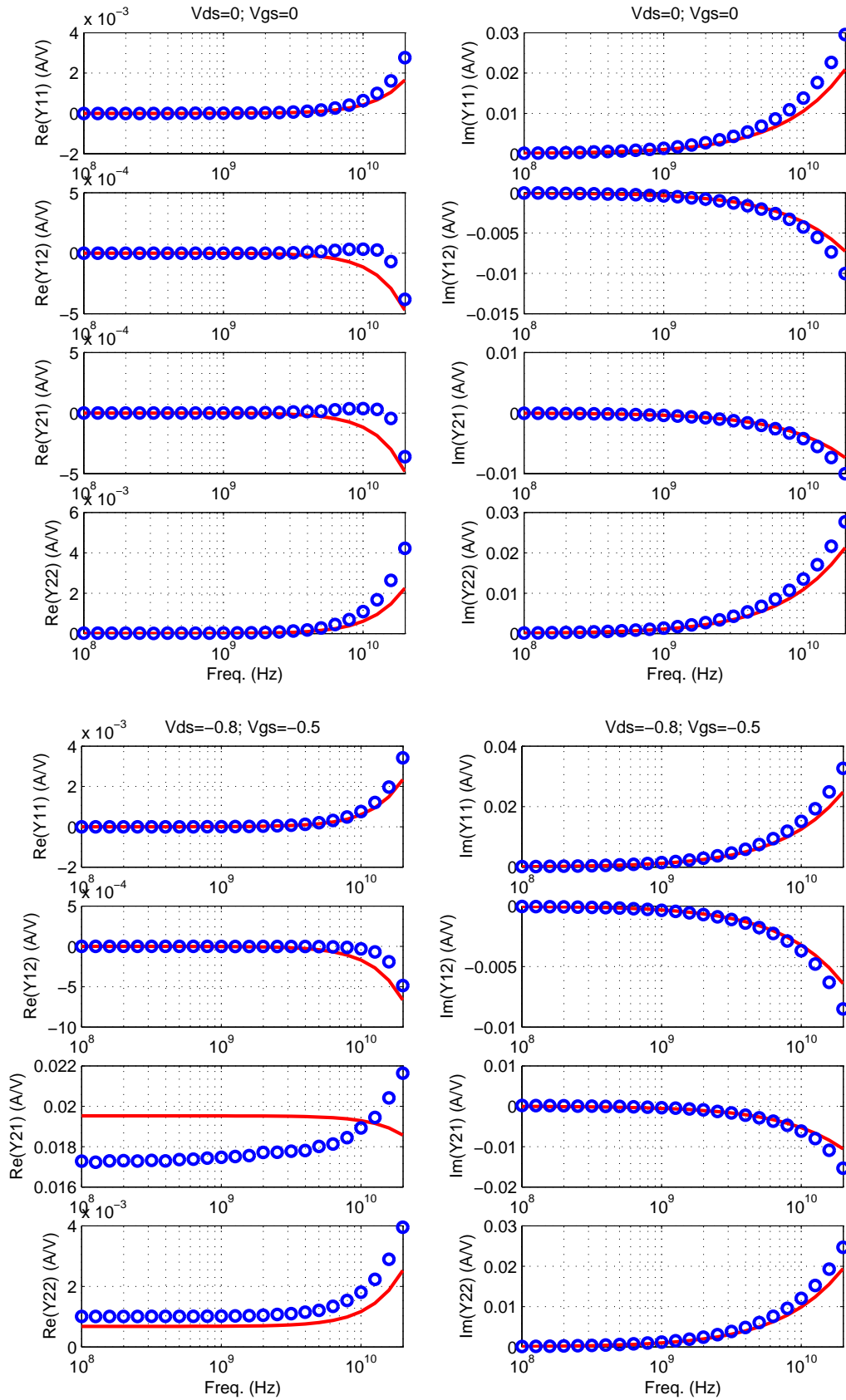


FIGURE 3.16 1p2_PFET_4x2x0p12 with 2-sided gate contact and ringed-substrate

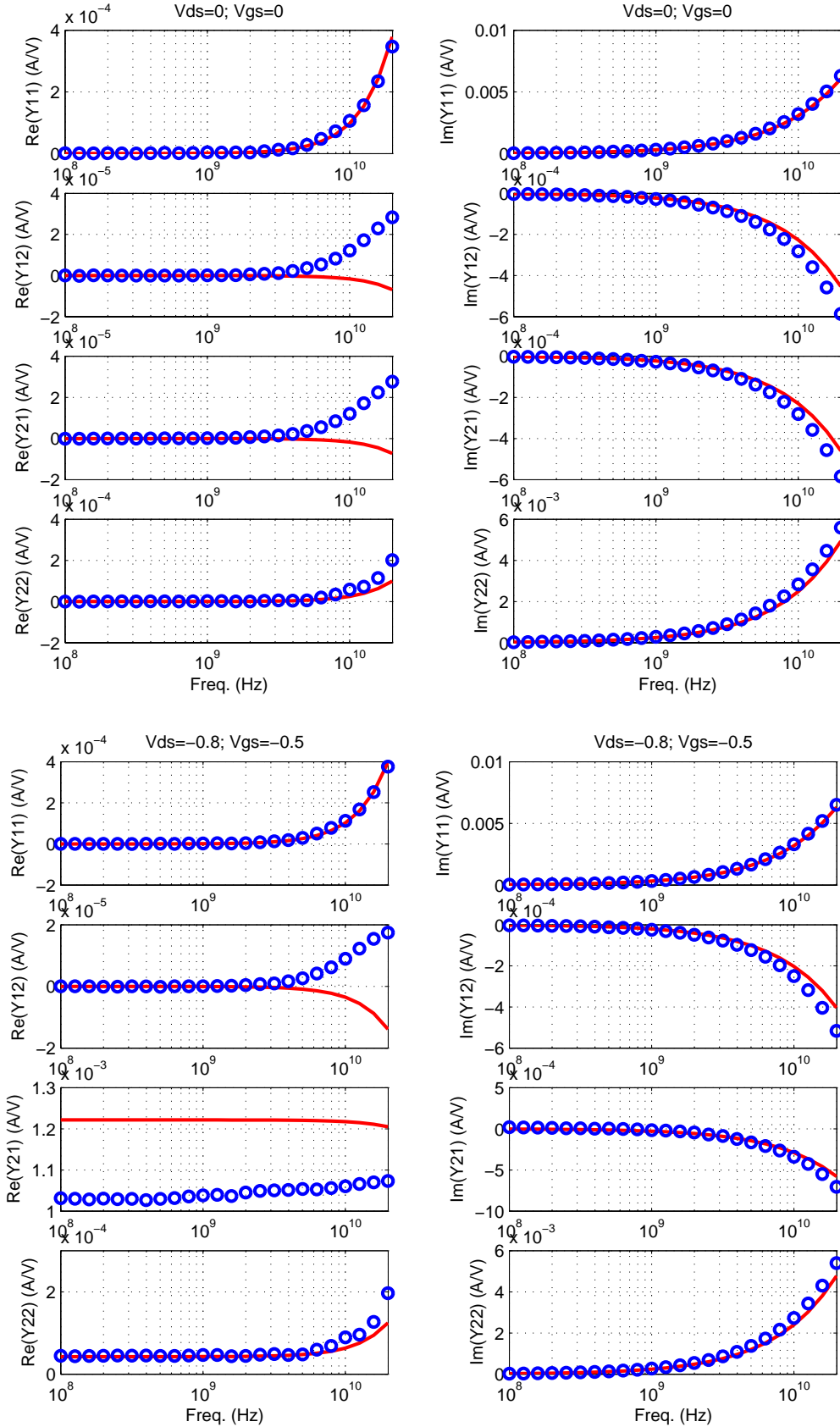


FIGURE 3.17 1p2_PFET_16x2x0p2 with 2-sided gate contact and ringed-substrate

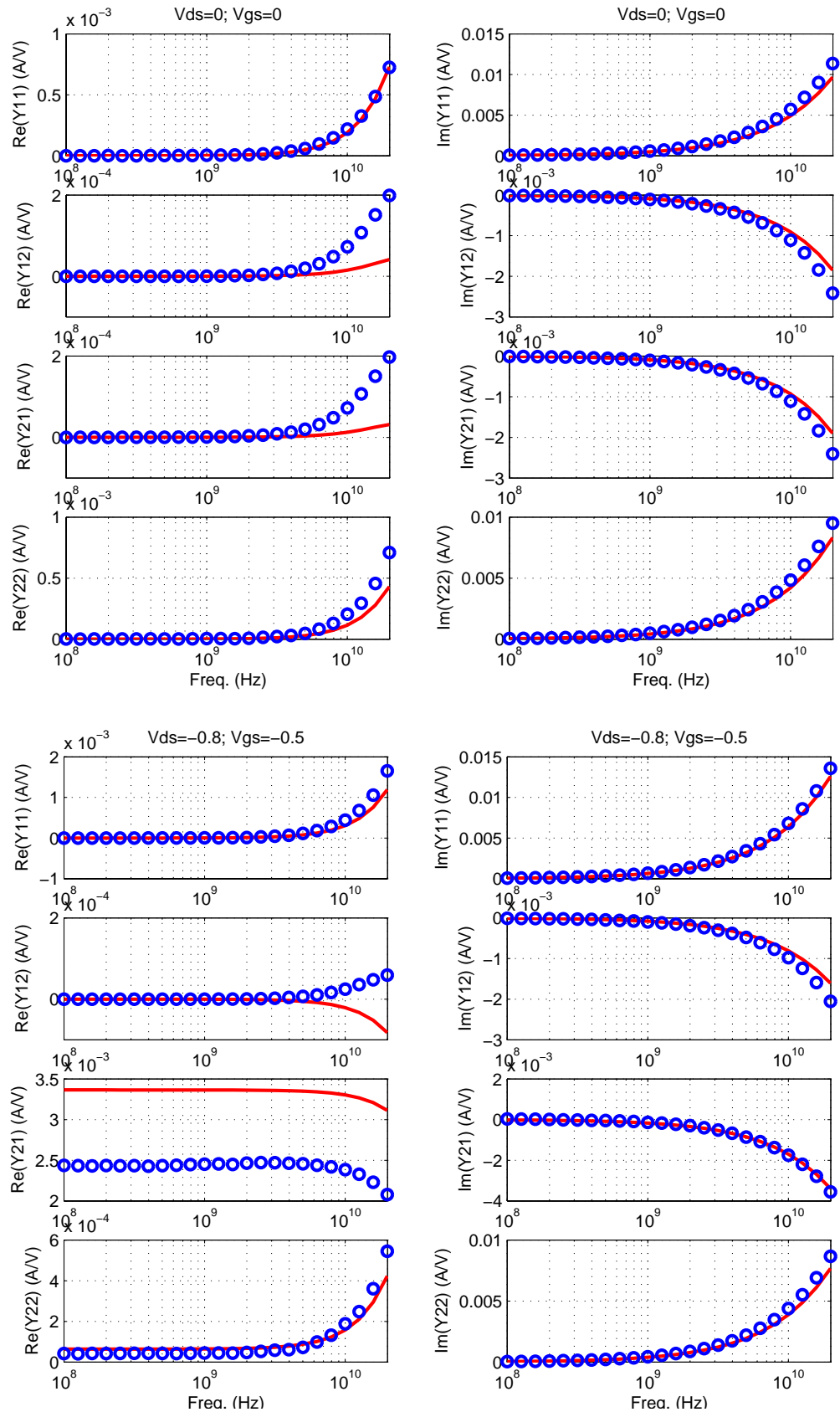


FIGURE 3.18 1p2_PFET_16x5x0p12 with 2-sided gate contact and ringed-substrate

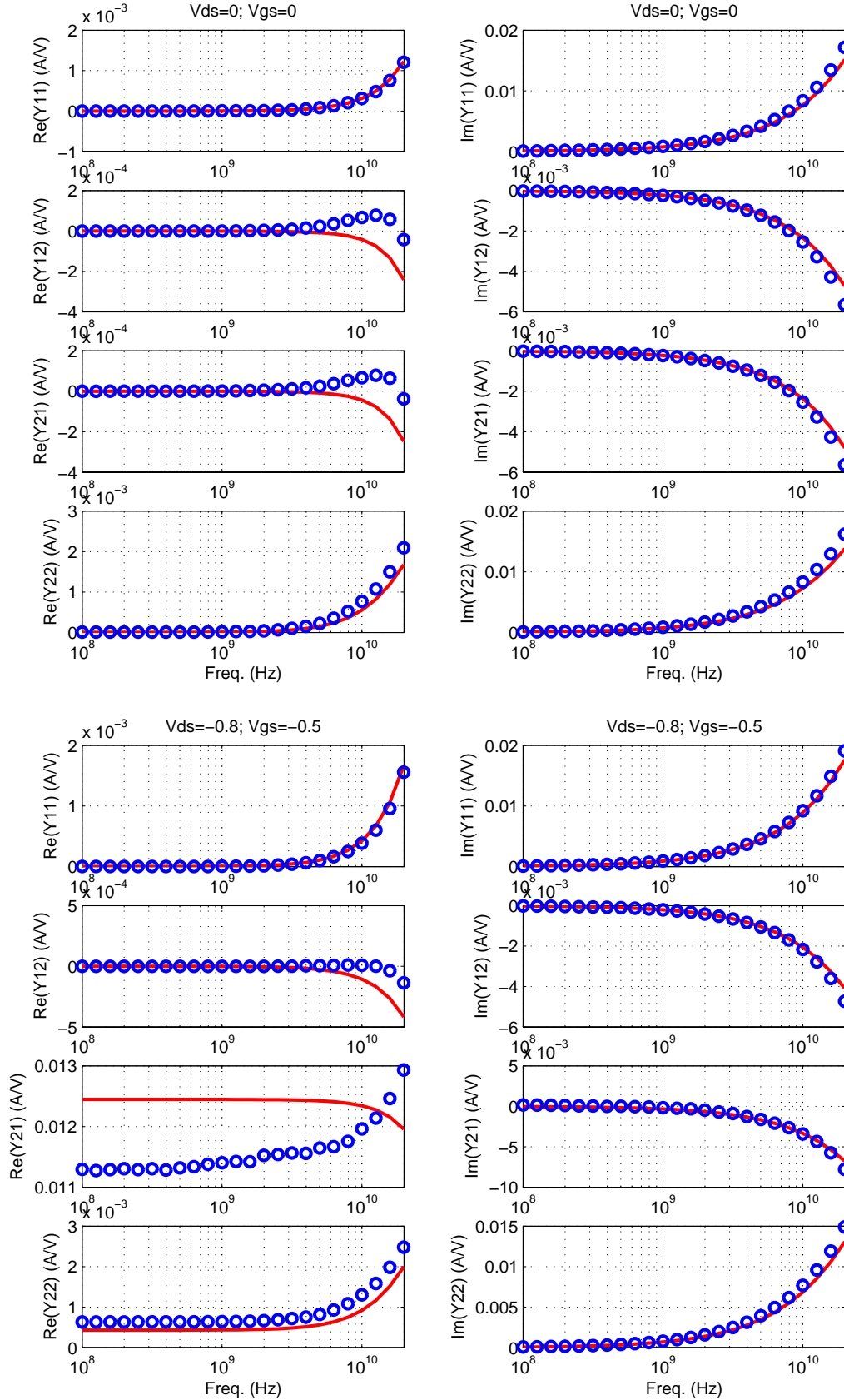


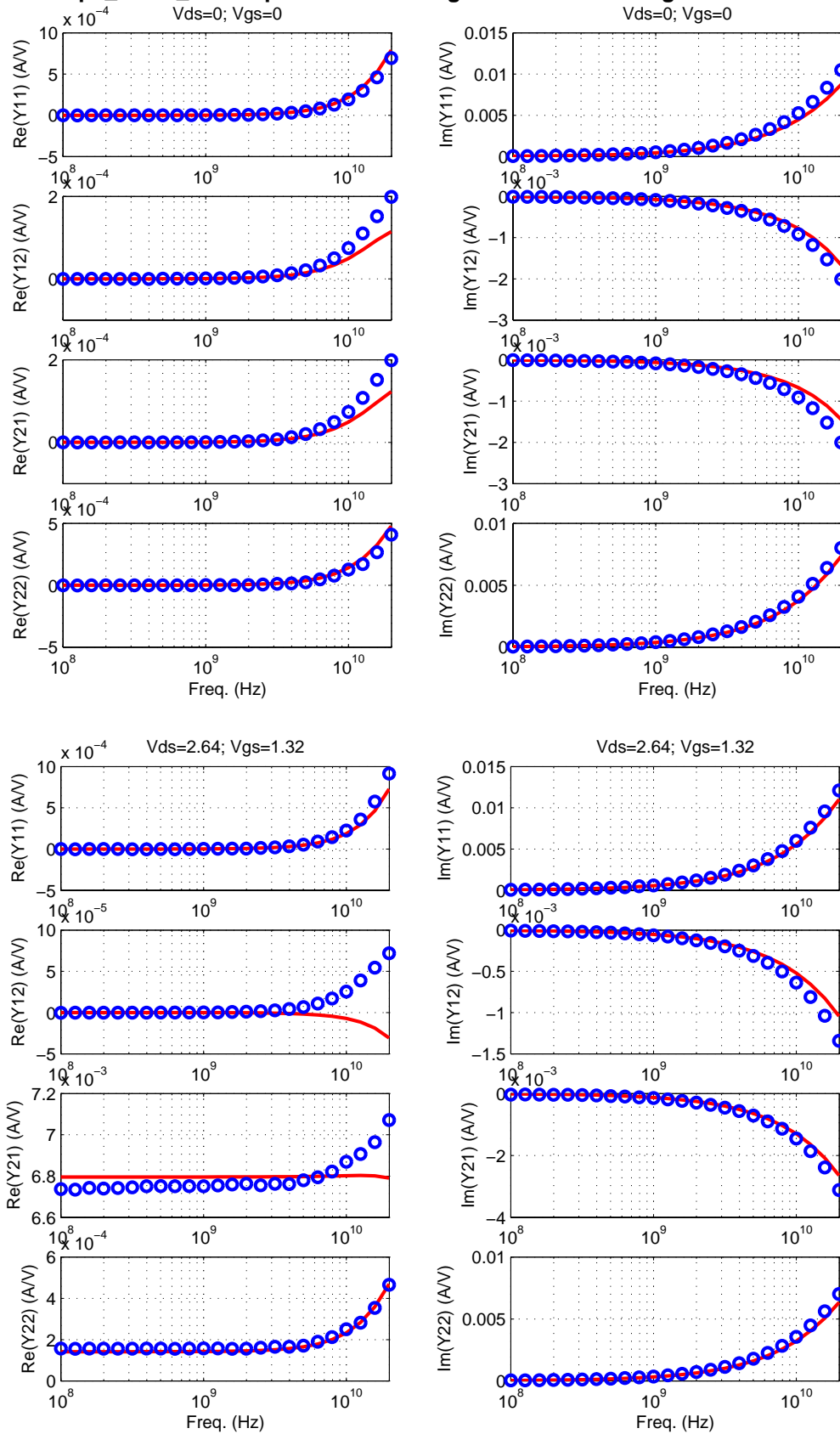
FIGURE 3.19 3p3_NFET_16x2x0p36 with 2-sided gate contact and ringed-substrate

FIGURE 3.20 3p3_NFET_64x2x0p36 with 2-sided gate contact and ringed-substrate

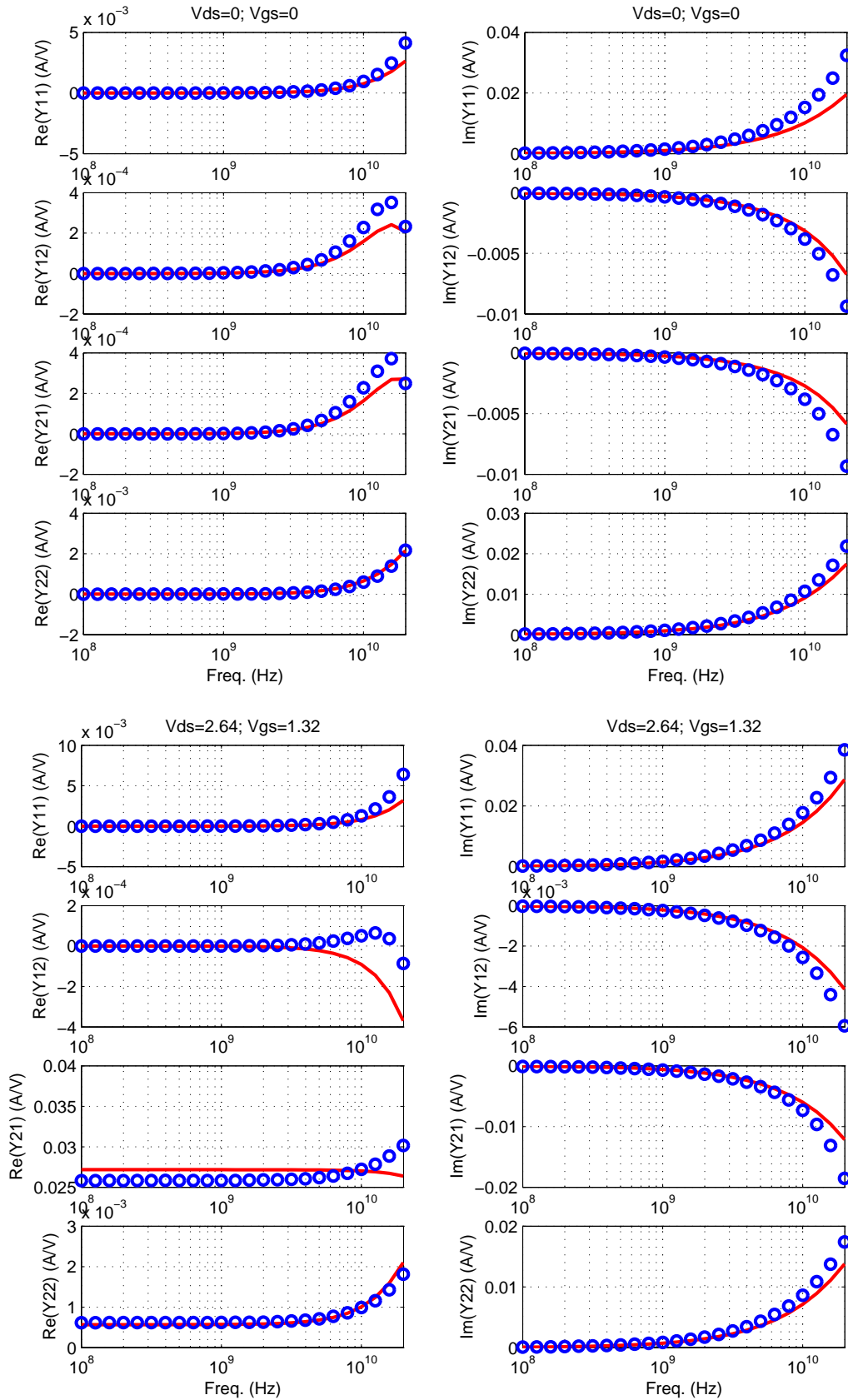


FIGURE 3.21 3p3_NFET_5x2x0p36 with 2-sided gate contact and ringed-substrate

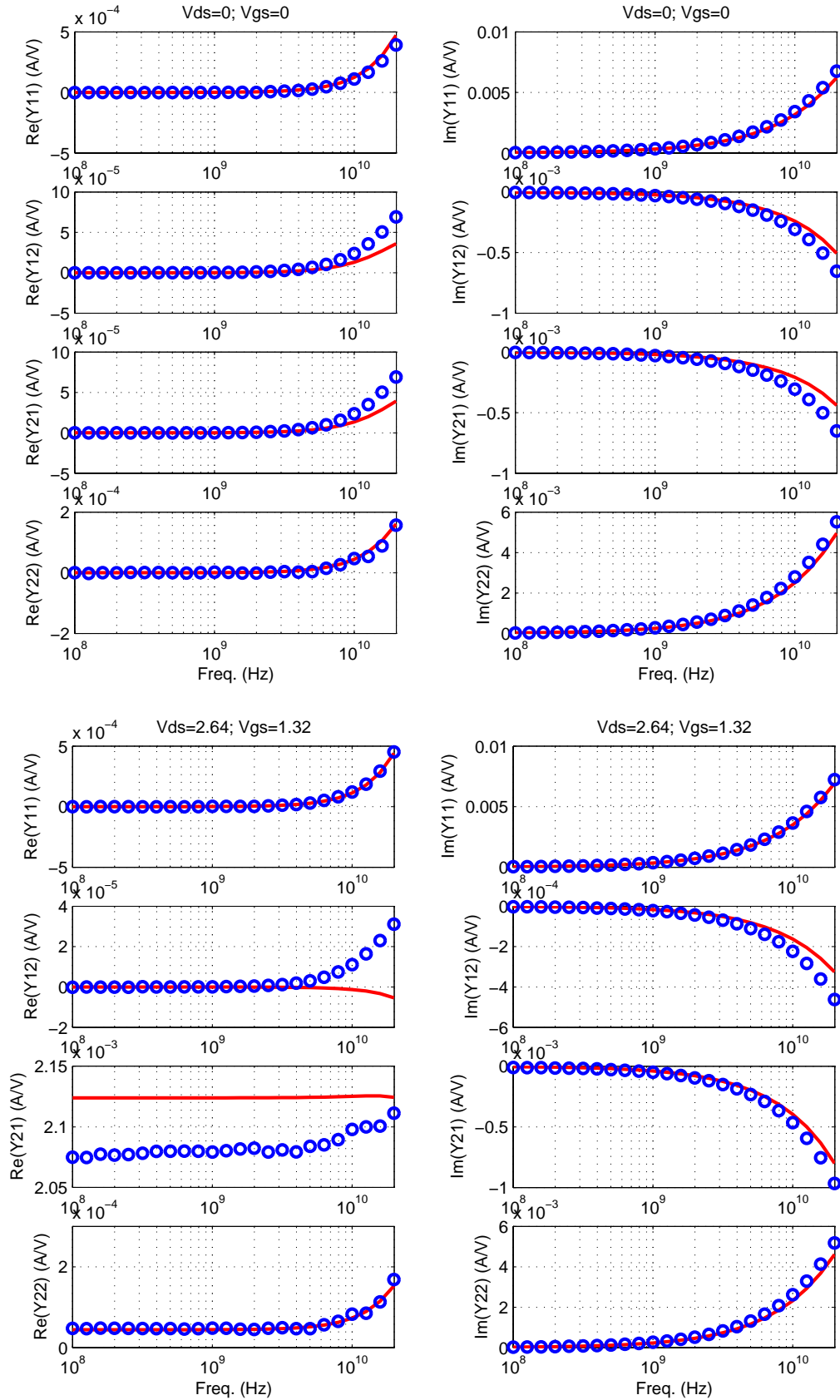


FIGURE 3.22 3p3_NFET_16x2x0p6 with 2-sided gate contact and ringed-substrate

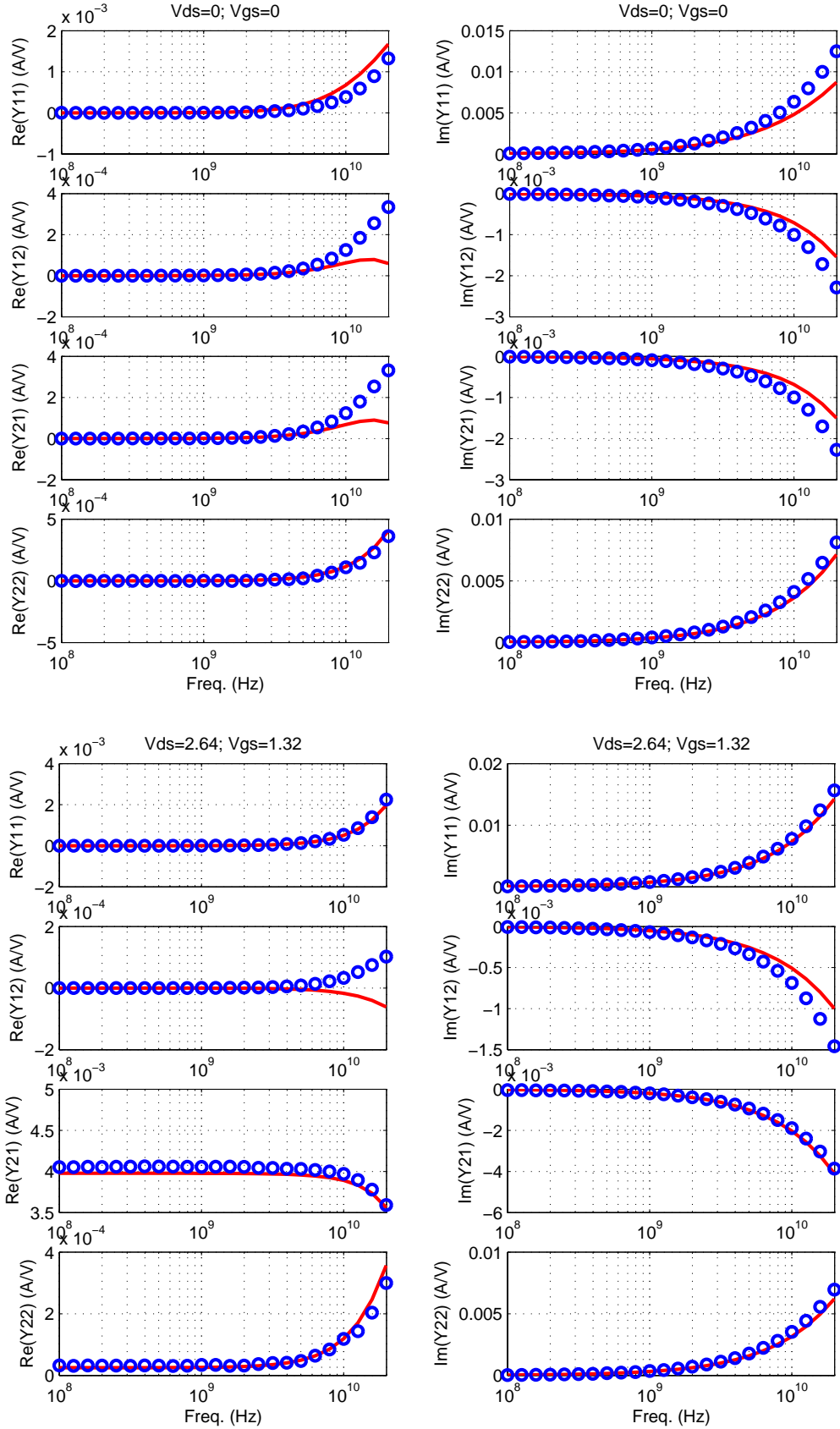


FIGURE 3.23 3p3_NFET_16x5x0p36 with 2-sided gate contact and ringed-substrate

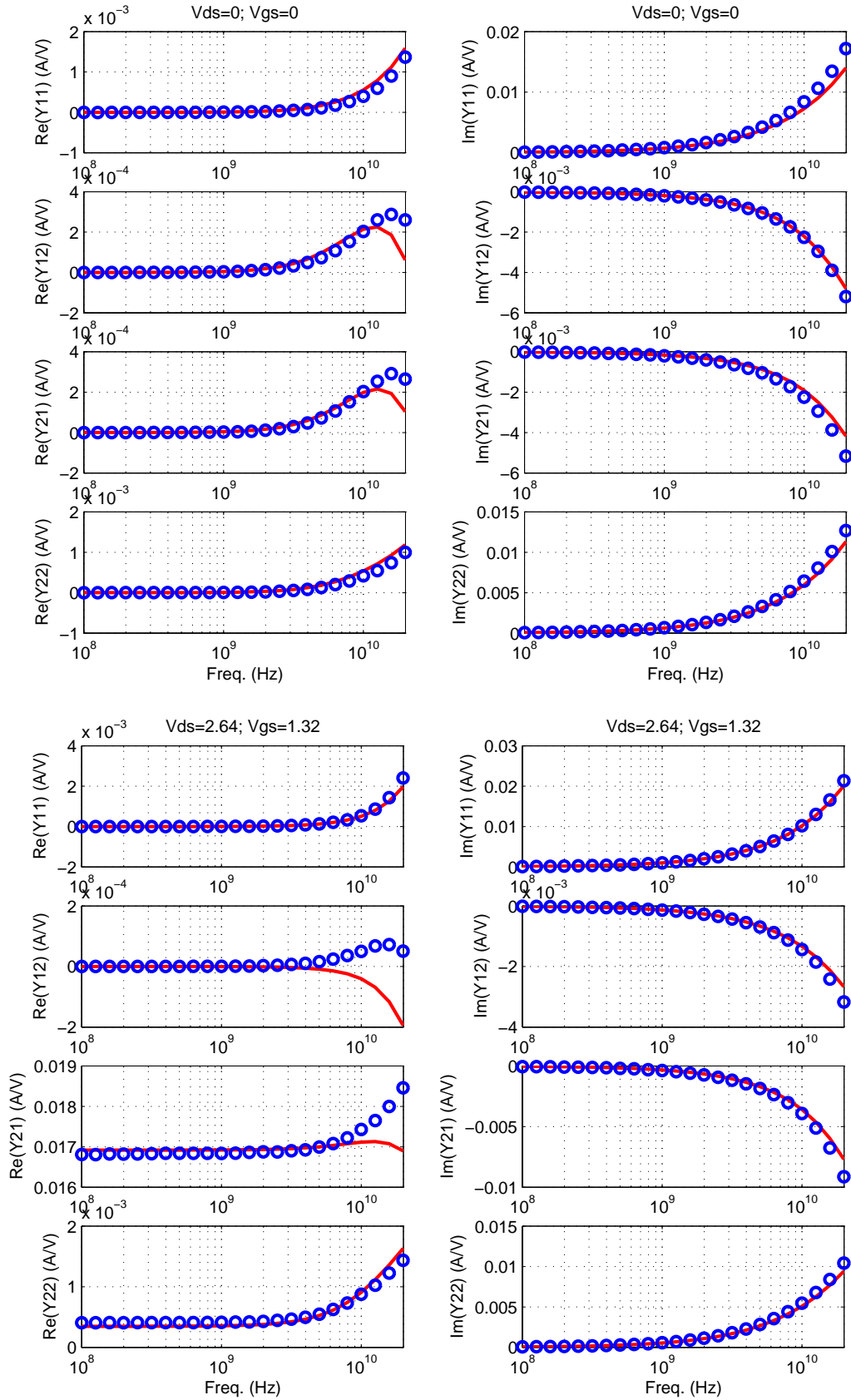


FIGURE 3.24 3p3_PFET_16x2x0p3 with 2-sided gate contact and ringed-substrate

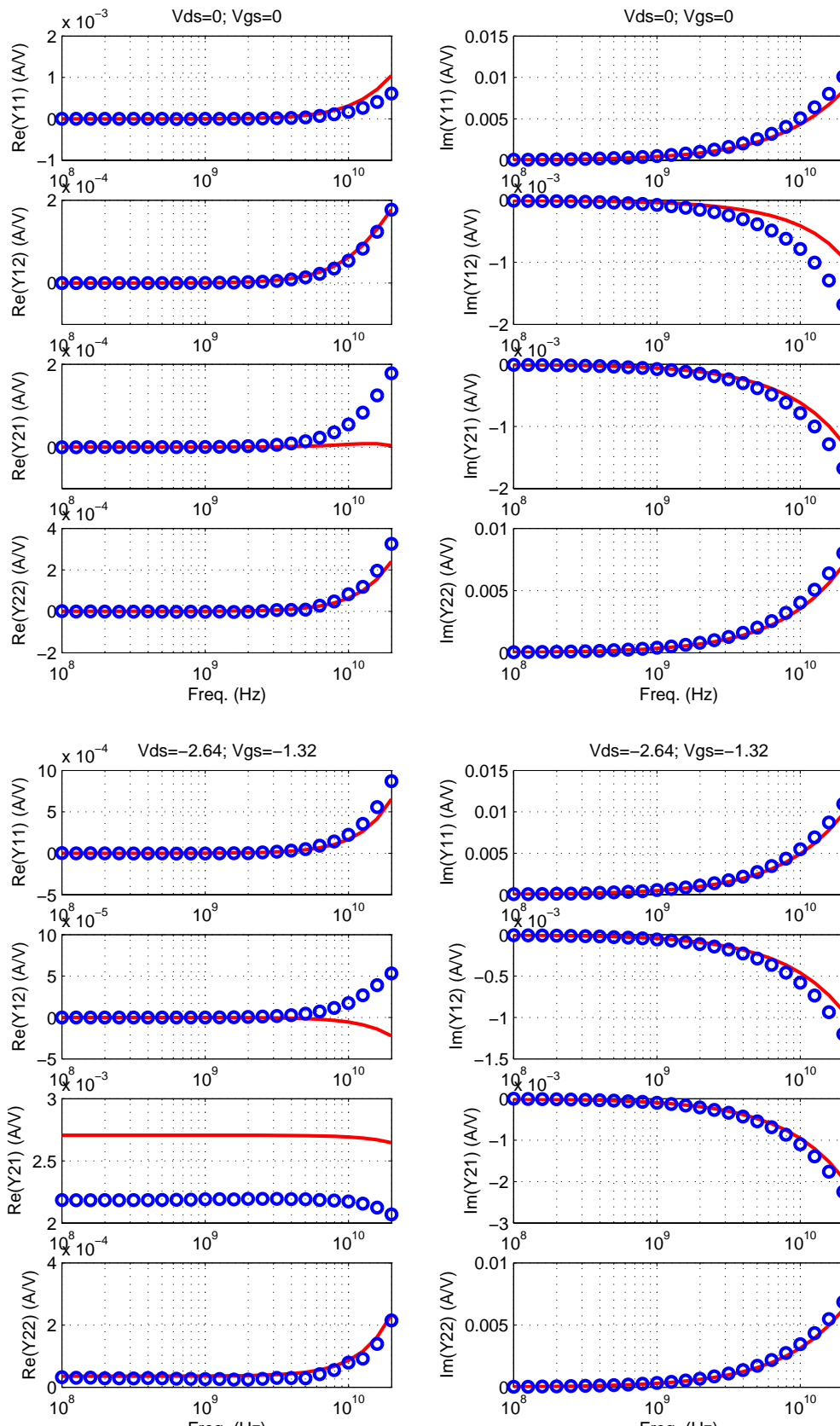


FIGURE 3.25 3p3_PFET_64x2x0p3 with 2-sided gate contact and ringed-substrate

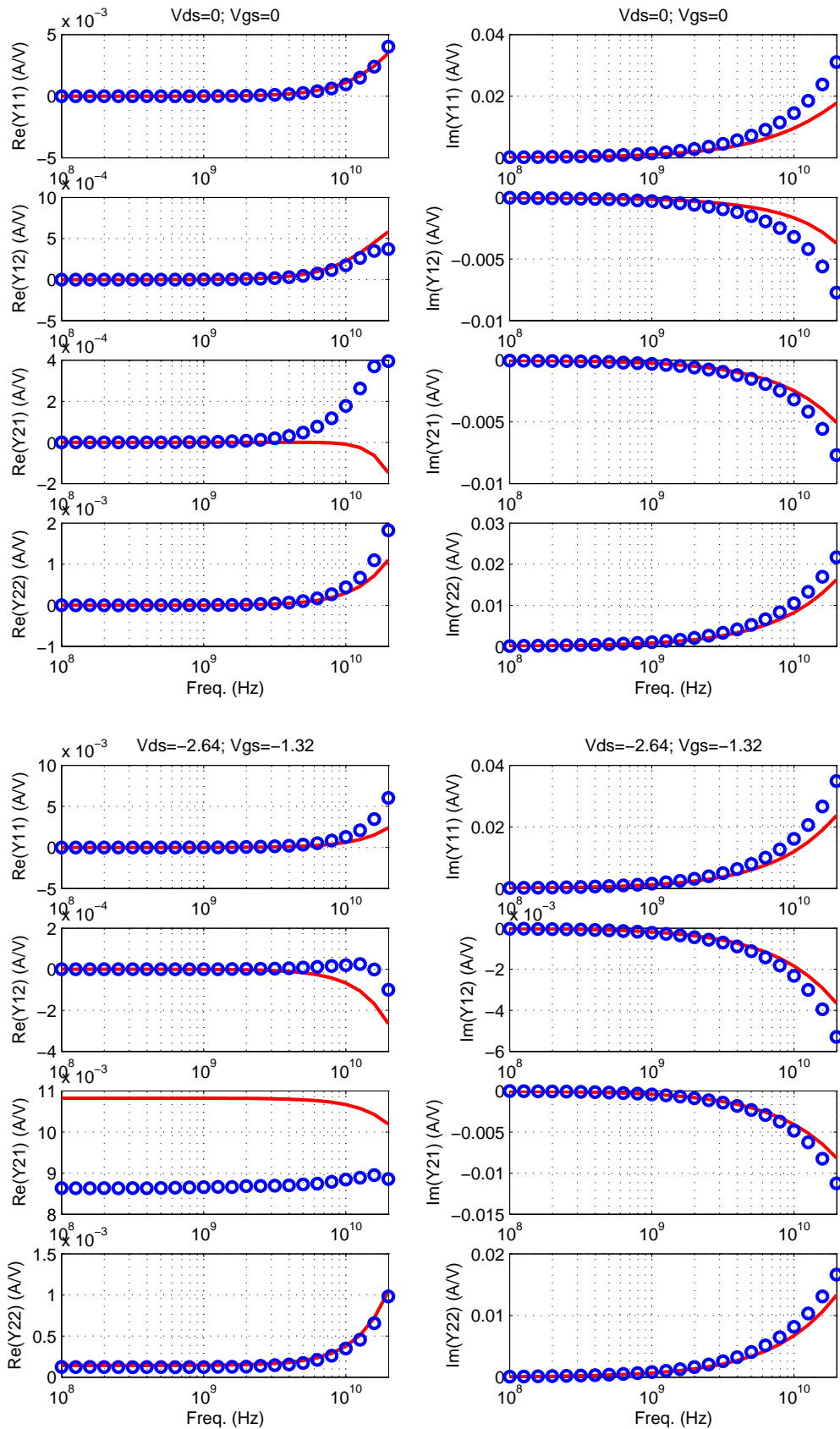


FIGURE 3.26 3p3_PFET_5x2x0p3 with 2-sided gate contact and ringed-substrate

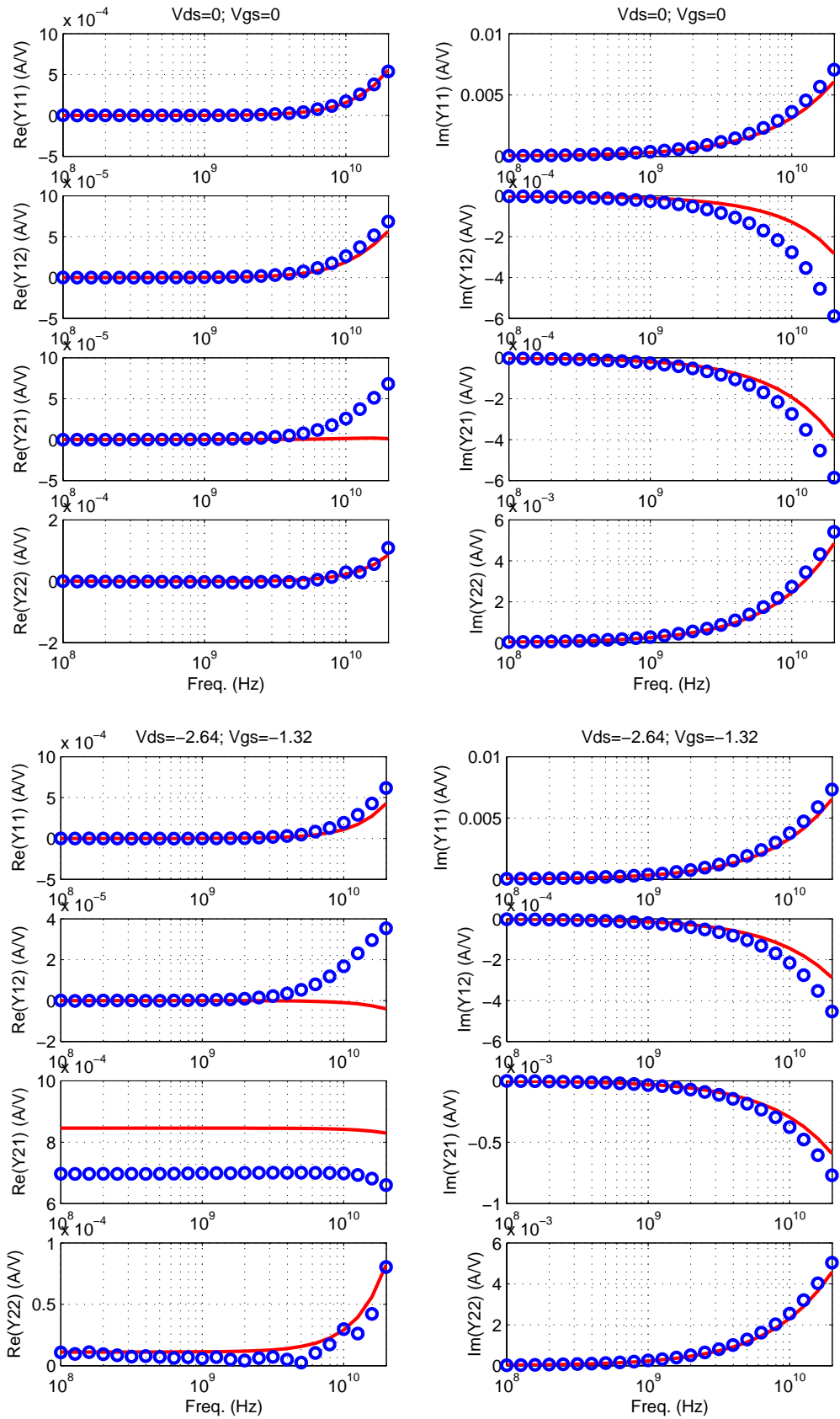


FIGURE 3.27 3p3_PFET_16x2x0p6 with 2-sided gate contact and ringed-substrate

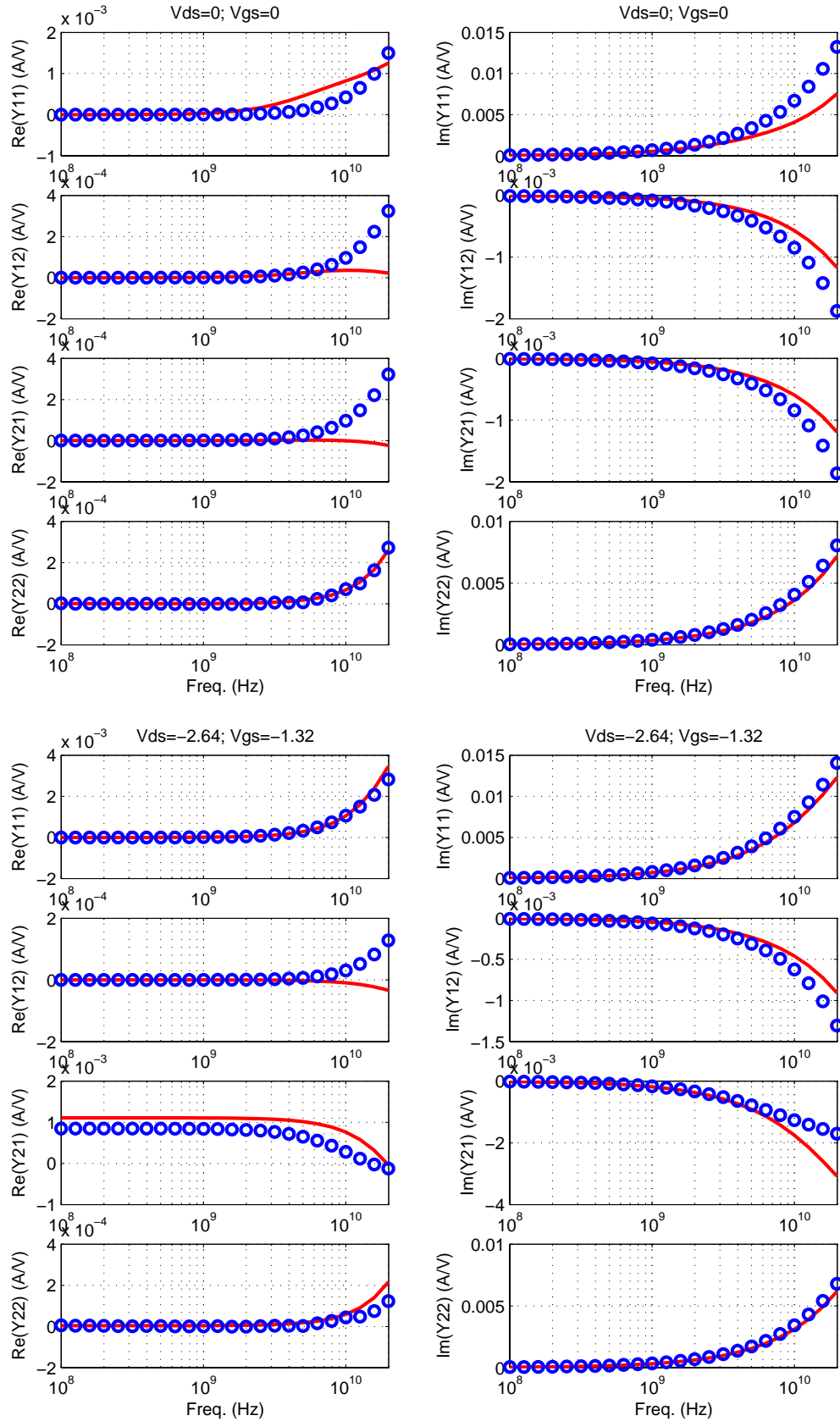
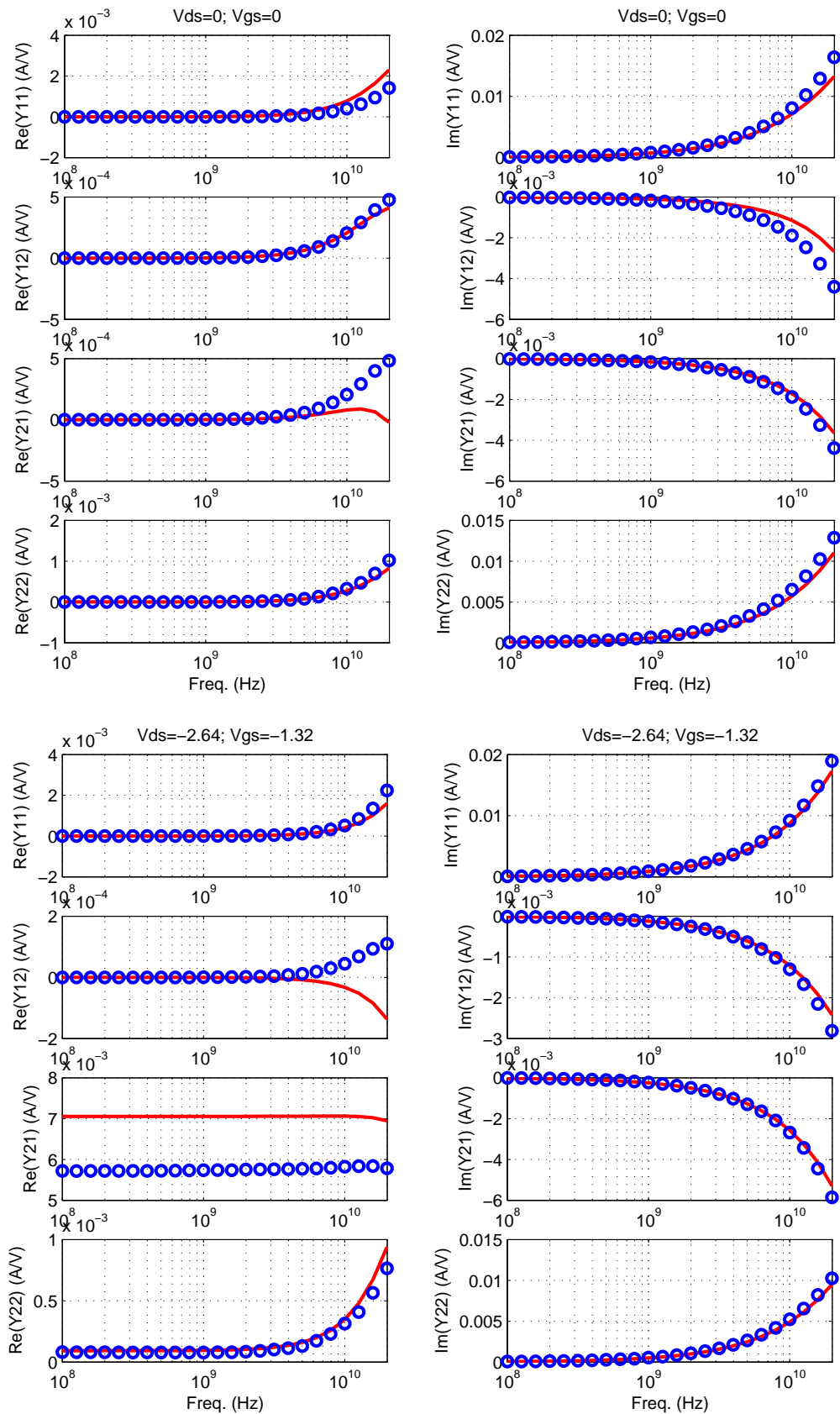


FIGURE 3.28 3p3_PFET_16x5x0p3 with 2-sided gate contact and ringed-substrate



3.7 High frequency Noise Modeling

There are 2 components of thermal noise that are important at high-frequencies (>1GHz): 1. Excess thermal noise in the channel; this is in addition to what can be expected from the resistive channel at a given bias, and 2. Channel induced gate noise, which is caused by the coupling of the channel thermal noise to the gate through the gate oxide. The default BSIM4 model underestimates (1) for velocity saturated short channel devices and does not model (2).

To capture the missing noise components, BSIM4 provides a “holistic” thermal noise model (TNOIMOD=1) as shown in Figure 3.29. The voltage noise source on the source side of the FET accounts for gate correlated portion of the drain noise. The same noise source contributes to the induced gate noise through the gate-source overlap capacitor. The drain current noise source accounts for excess thermal noise observed in short channel devices. The simulated NFmin (minimum Noise Figure) using this holistic noise model for a RF NFET is shown in Figure 3.30.

Note: High-frequency noise measurement data is not yet available for CA13.

FIGURE 3.29 Excess noise source modeling

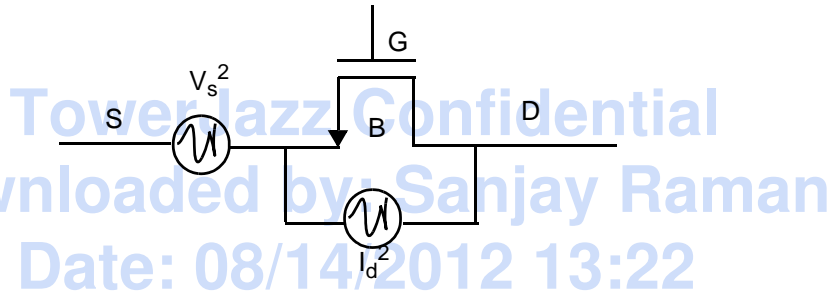
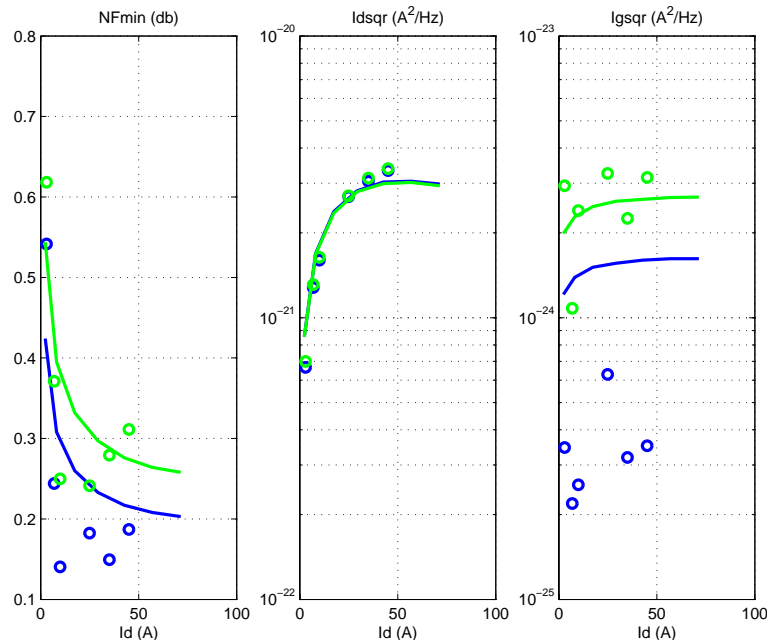


FIGURE 3.30 NFmin, drain and gate noise currents for RF NFET (NFxWxL = 100x2x0.12 μ m)



3.8 Model update History

3.8.1 v1.0

First release of CA13/SBL13 RF FET models.

3.8.2 v1.7

Re-extraction of 1.2v and 3.3v RF FET models from new silicon:

TABLE 3.5 Mixed-signal model specific updates in model release version 1.7

v1.7 update	Devices	Reason	Impact on user
RF Model	All 1.2v RF FETs	Better silicon available from mature process	Shift in o/p admittance (Y22) and transmission (Y12, Y21). Small change in i/p admittance (Y11)
BSIM3v3 -> BSIM4	All 3.3v RF FETs	Better silicon available from mature process; leverage improved modeling capabilities in BSIM4	Improved modeling of i/p resistance Shift in o/p admittance (Y22) and transmission (Y12, Y21)
BSIM4 HF Noise	1.2v RF NFET	NFmin data available	Improved modeling of HF noise
BSIM3v3 -> BSIM4 HF Noise	All 3.3v RF FETs	Leverage improved modeling capabilities in BSIM4	Improved modeling of HF noise

3.8.3 v1.8

No changes

3.9 References

1. Steve Hung-Min Jen, Christian C. Enz, David R. Pehlke, Michael Schroter, and Bing J. Sheu, "Accurate Modeling and Parameter Extraction for MOS Transistors Valid up to 10 GHz," IEEE Trans. on Elec. Dev., Vol. 46, No. 11, November 1999.
2. Chih-Hung Chen, M. Jamal Deen, Yuhua Cheng, and Mishel Matloubian, "Extraction of the Induced Gate Noise, Channel Noise, and Their Correlation in Submicron MOSFETs from RF Noise Measurements," IEEE Trans. on Elec. Dev., Vol. 48, No. 12, December 2001.

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4.0 SiGe Bipolar Model

4.1 Device Description

The SBL13 process contains three NPN device types, low, medium, and high voltage, differentiated by BV_{CEO} and F_t targets listed in Table 4.1. A cross section of an NPN device is shown in Figure 4.1 where the differentiating factor between the device types is the collector implant. Figure 4.2 shows the layout of a 2 emitter, 1 base, 2 collector configuration. Layout configurations are further described in Section 4.3.

TABLE 4.1 SBL13 NPN Specification by BV_{CEO} and F_t

NPN	BV_{CEO}	F_t
low voltage	2.4	91
medium voltage	3.5	67
high voltage	6.6	36.5

FIGURE 4.1 Cross Section of NPN

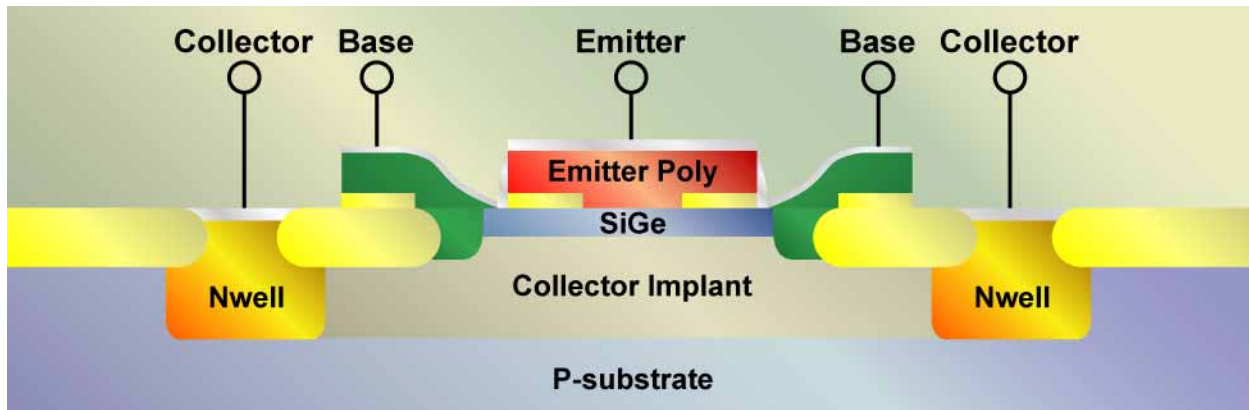
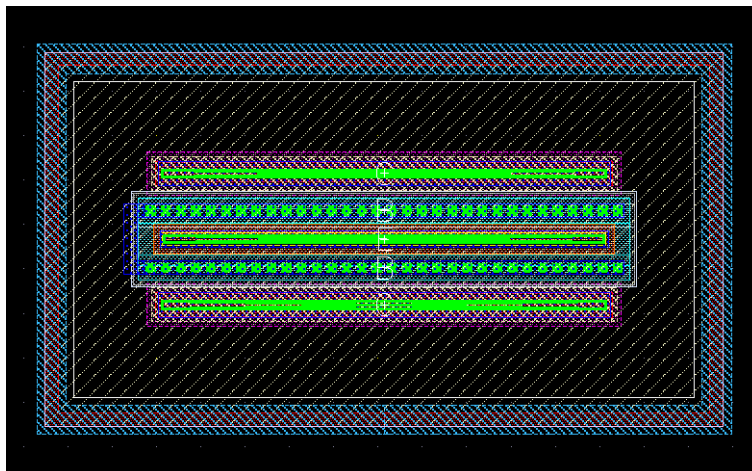


FIGURE 4.2 Layout of NPN



4.2 Model Description

4.2.1 L-Scalable Model

The emitter length can be varied from 0.5 to 20.0 μm within the grid spacing and a corresponding scalable model with emitter length is extracted. Separate models are extracted for the various combinations of emitter width and finger configuration described in Table 4.2. HICUM and GP models are included in the design kit.

4.2.2 HICUM Model

The HICUM model was introduced to overcome the shortcomings of the SGPM. The name of HICUM is derived from “High Current Model”. HICUM was initially developed with special emphasis on the modeling of the high current region, very important for many high-speed applications. Compared with SGPM, HICUM is based on an extended and generalized integral charge control relationship, and approaches the transistor dynamic behaviors in a more physical way. For more detailed information about HICUM, please refer to HICUM official web page (http://www.iese.et.tu-dresden.de/iese/eb/hic_new/hic_start.html).

4.3 Available NPN Configurations and Usage Guidelines

Table 4.2 provides a detailed description of the NPN configurations and parameter ranges.

Narrow vs. Wide Emitters: Two emitter widths (0.28 μm and 0.96 μm) are offered for HV devices to enable trade-offs among base resistance, parasitic capacitance, F_t , and current consumption. For the same device area, 0.96 μm devices will have higher base resistance but lower collector base and collector substrate capacitance than 0.28 μm devices.

Multiple device instances vs. multiple emitter fingers: use of multiple emitter fingers instead of multiple device instances generally results in more efficient footprint and lower parasitic capacitance. The trade-off is collector resistance.

TABLE 4.2 SBL13 NPN Configurations

configuration	device type	emitter width	emitter length	emitters	bases	collectors
	l=low voltage m=medium voltage h=high voltage	n=0.28 μm w=0.96 μm				
122	l, m, h	n	0.5-20.0 μm	1	2	2
232	l, m, h	n	1.0-20.0 μm	2	3	2
342	l, m, h	n	1.0-20.0 μm	3	4	2
452	l, m, h	n	1.0-20.0 μm	4	5	2
122-452	h	w	1.0-20.0 μm	4	5	2

4.4 Model Extraction and Verification

Scalable NPN models are extracted based on DC, CV, and RF measurements over a wide geometry and bias range.

Figures 4.3 through 4.20 display the characterization plots for the low voltage NPN. Figures 4.21 through 4.38 display the characterization plots for the medium voltage NPN. Figures 4.39 through 4.68 display the characterization plots for the high voltage NPN. Multiple devices in parallel are characterized for smaller emitter lengths to reduce de-embedding errors. The device type and size are encoded in the figure caption as “Voltage LxWxM_Configuration.” Thus a MV 0.28x1.0x1_122 captions refers to a medium voltage NPN with a width (W) of 0.28 μ m, a length (L) of 1 μ m, with 10 devices in parallel (M) and 122 emitter/base/collector finger configuration.

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4.4.1 Low Voltage Verification Plots

FIGURE 4.3 Gummel Plot LV 0.28x10.0_122

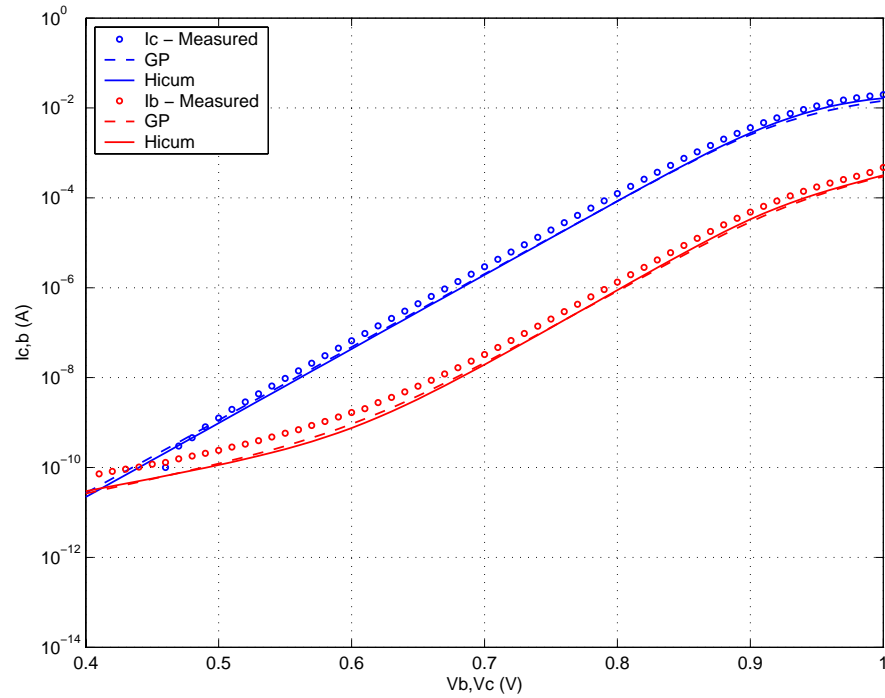


FIGURE 4.4 Beta vs. I_c : LV 0.28x10.0_122

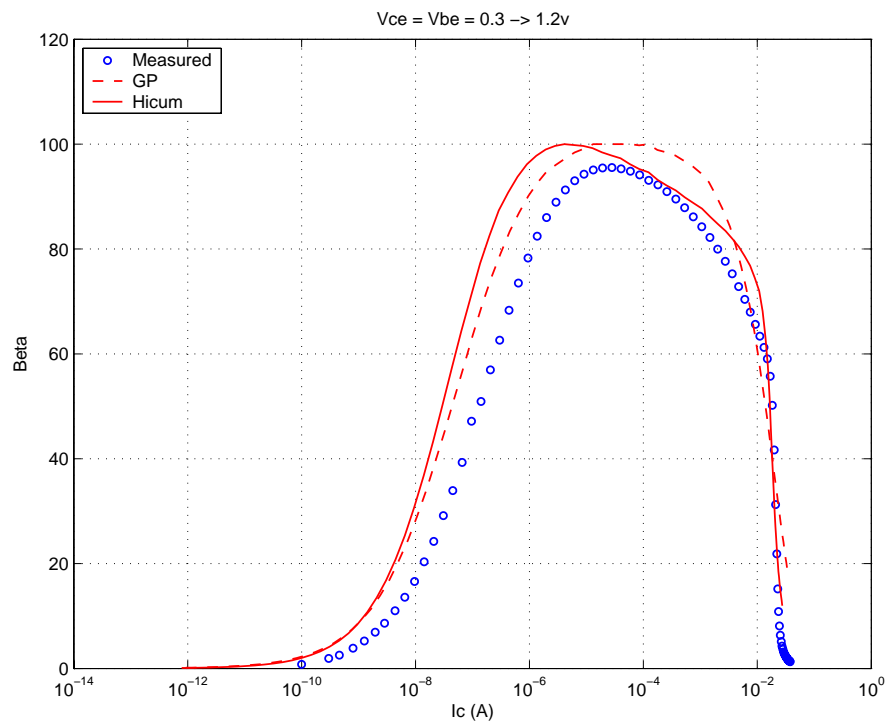


FIGURE 4.5 I_C vs. V_{CE} at constant I_B : LV 0.28x10.0_122

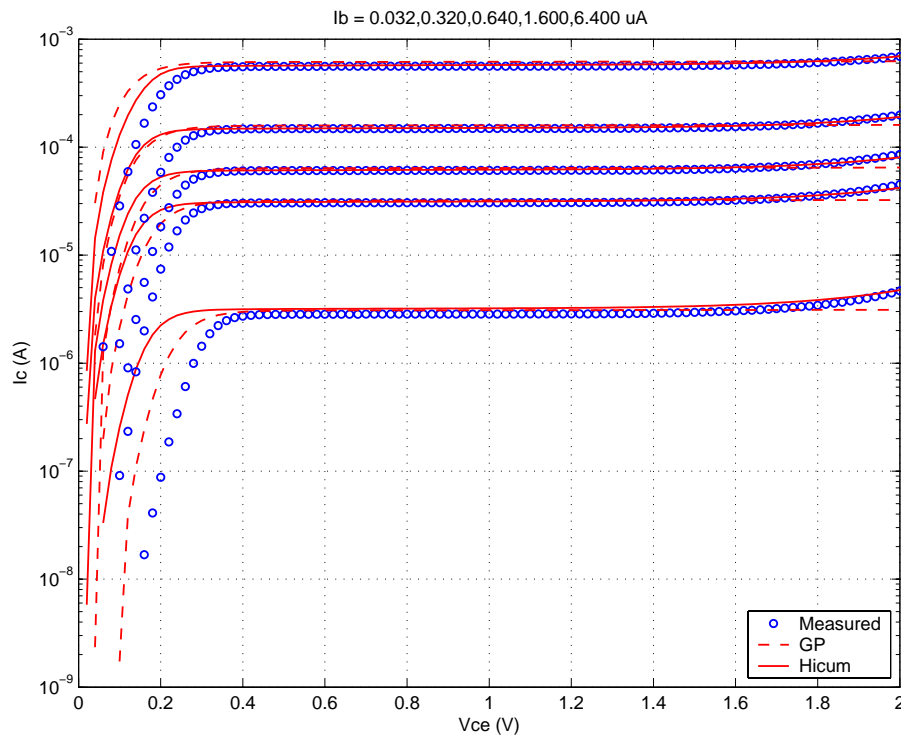


FIGURE 4.6 f_T vs. I_C : LV 0.28x10.0_122

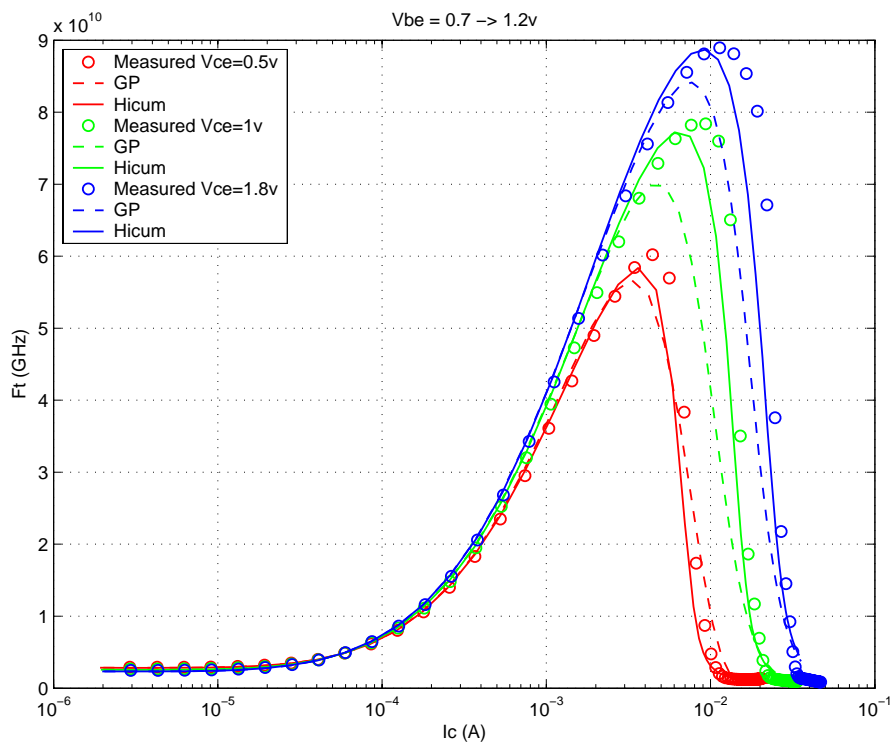
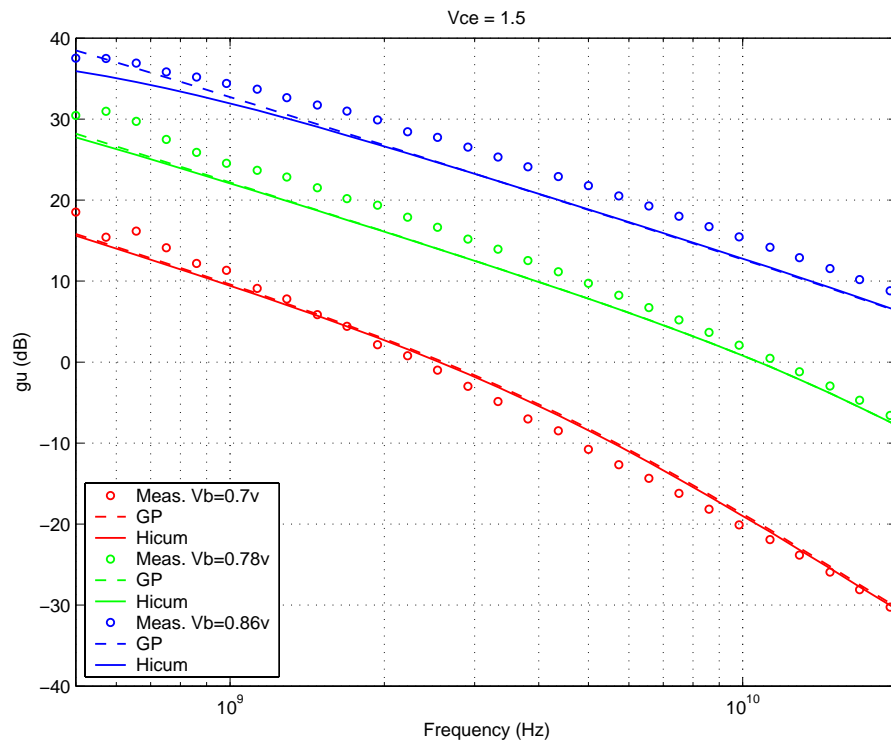


FIGURE 4.7 Power Gain vs. Freq: LV 0.28x10.0_122



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FIGURE 4.8 Y-parameters vs. FREQ: LV 0.28x10.0_122

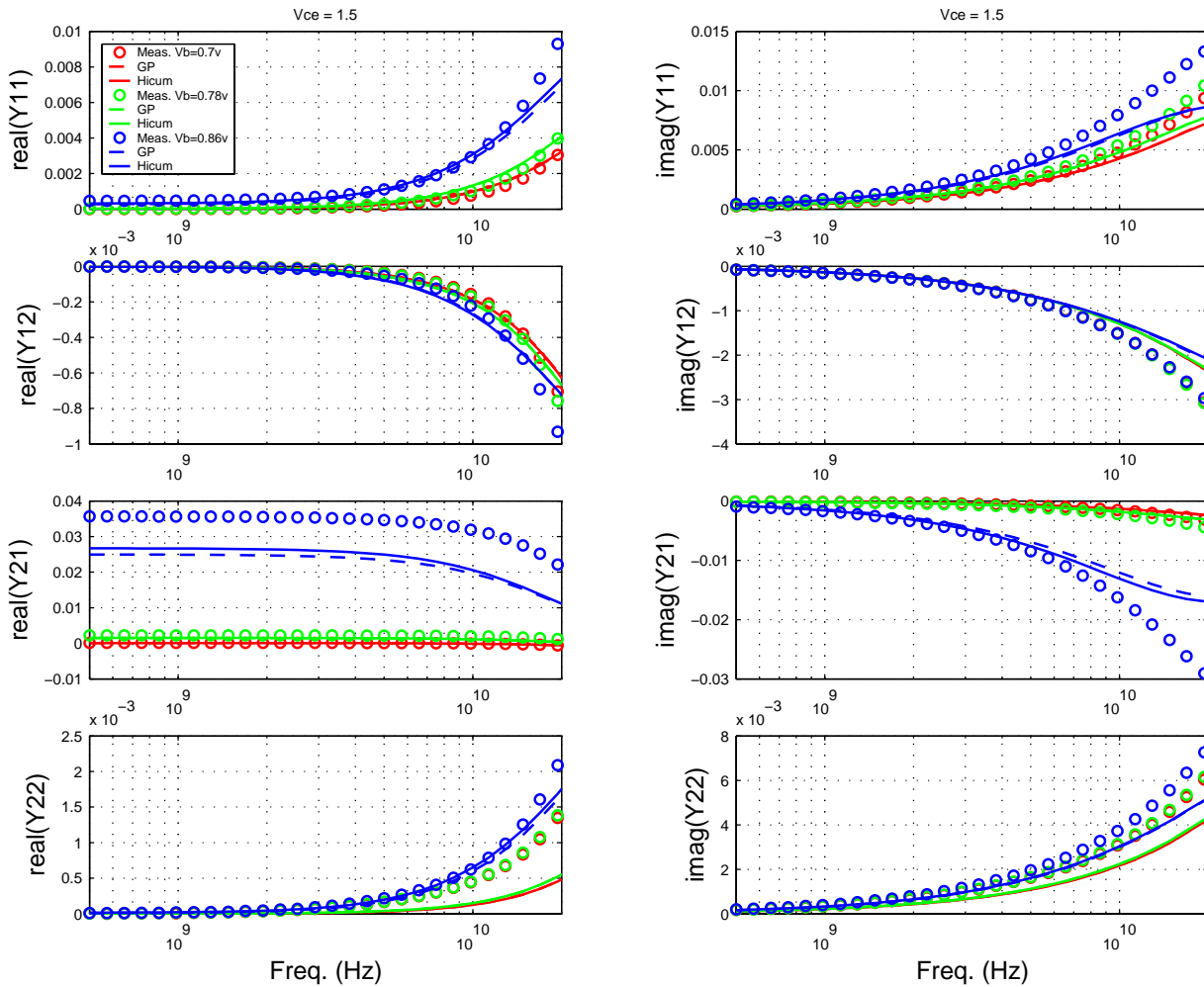


FIGURE 4.9 Gummel Plot: LV 0.28x10.0_232

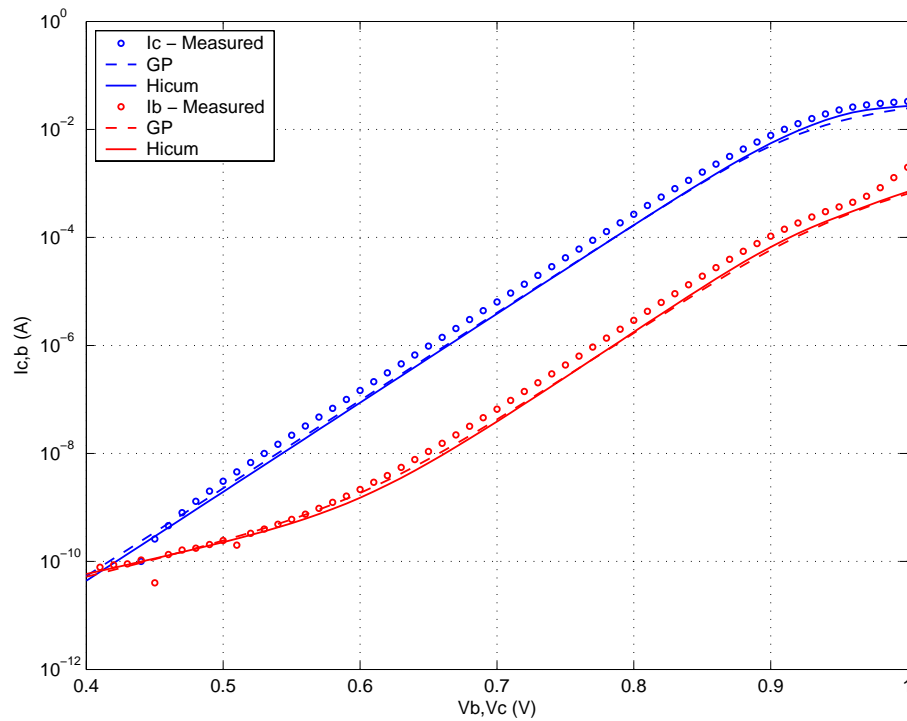
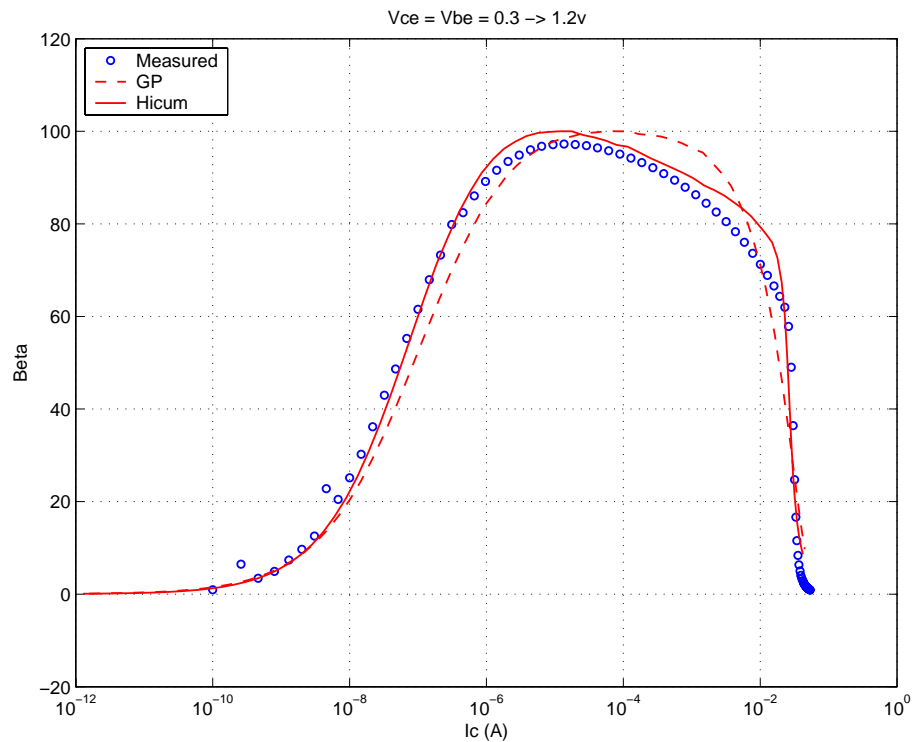
FIGURE 4.10 Beta vs I_c : LV 0.28x10.0_232

FIGURE 4.11 I_C vs. V_{CE} at constant I_B : LV 0.28x10.0_232

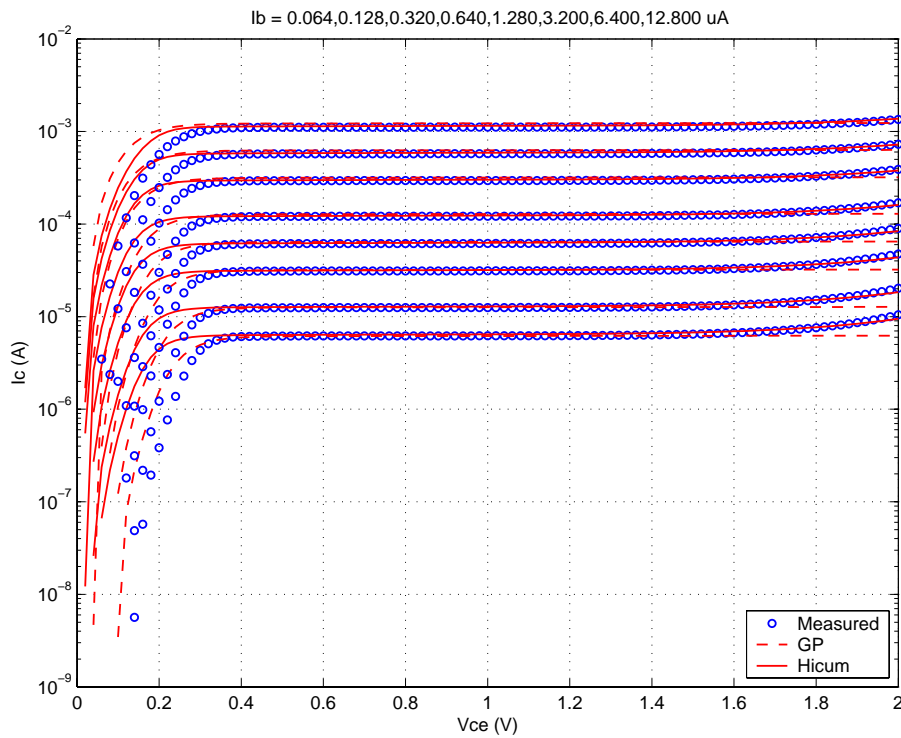


FIGURE 4.12 F_T vs. I_C : LV 0.28x10.0_232

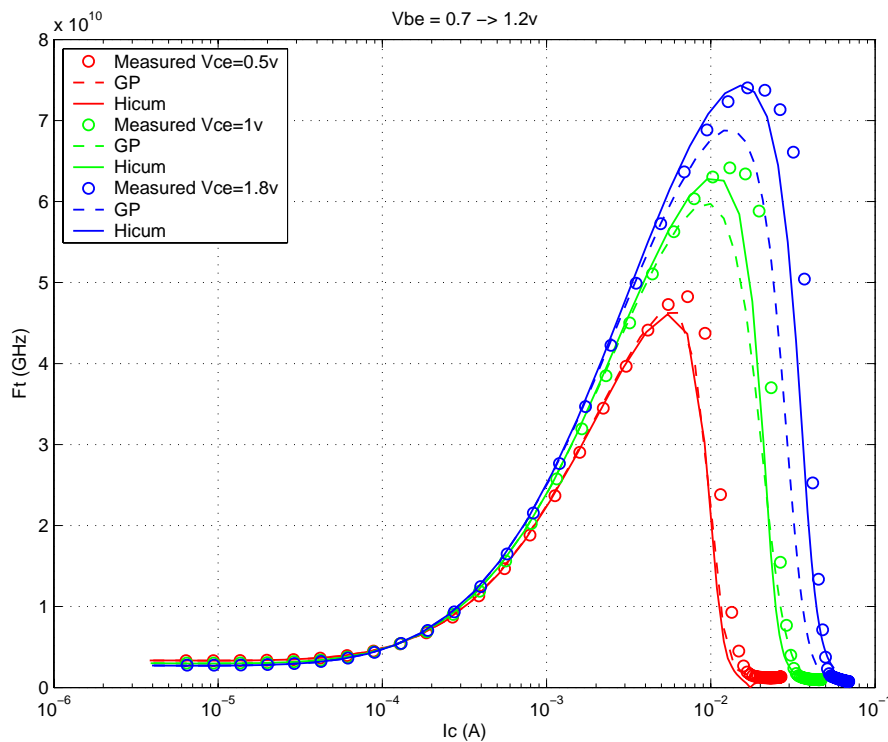
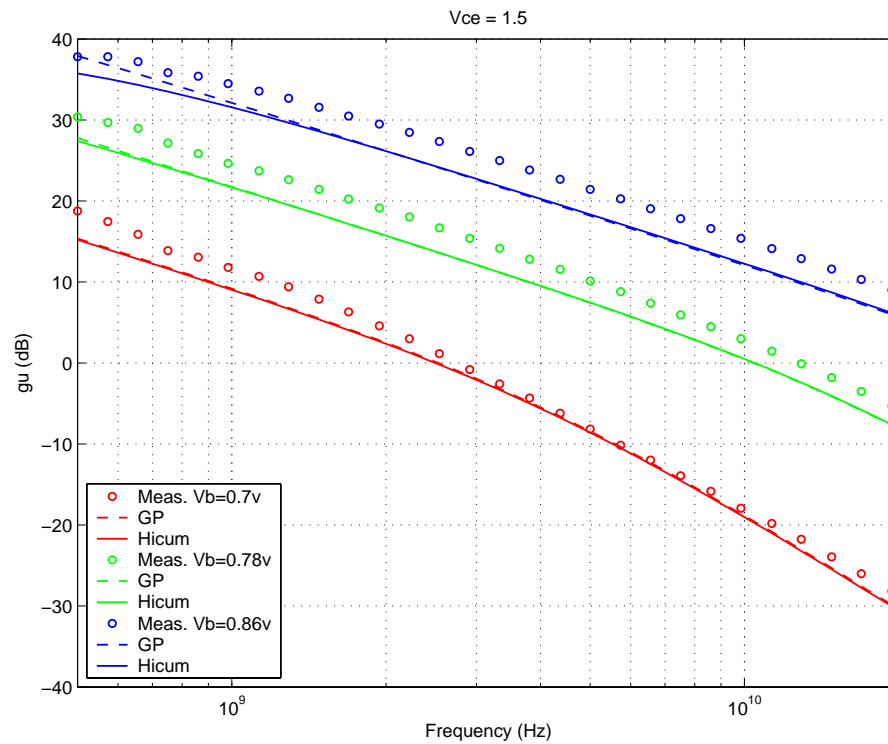


FIGURE 4.13 Power Gain vs. Freq: LV 0.28x10.0_232



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FIGURE 4.14 Y-parameters vs. FREQ: LV 0.28x10.0_232

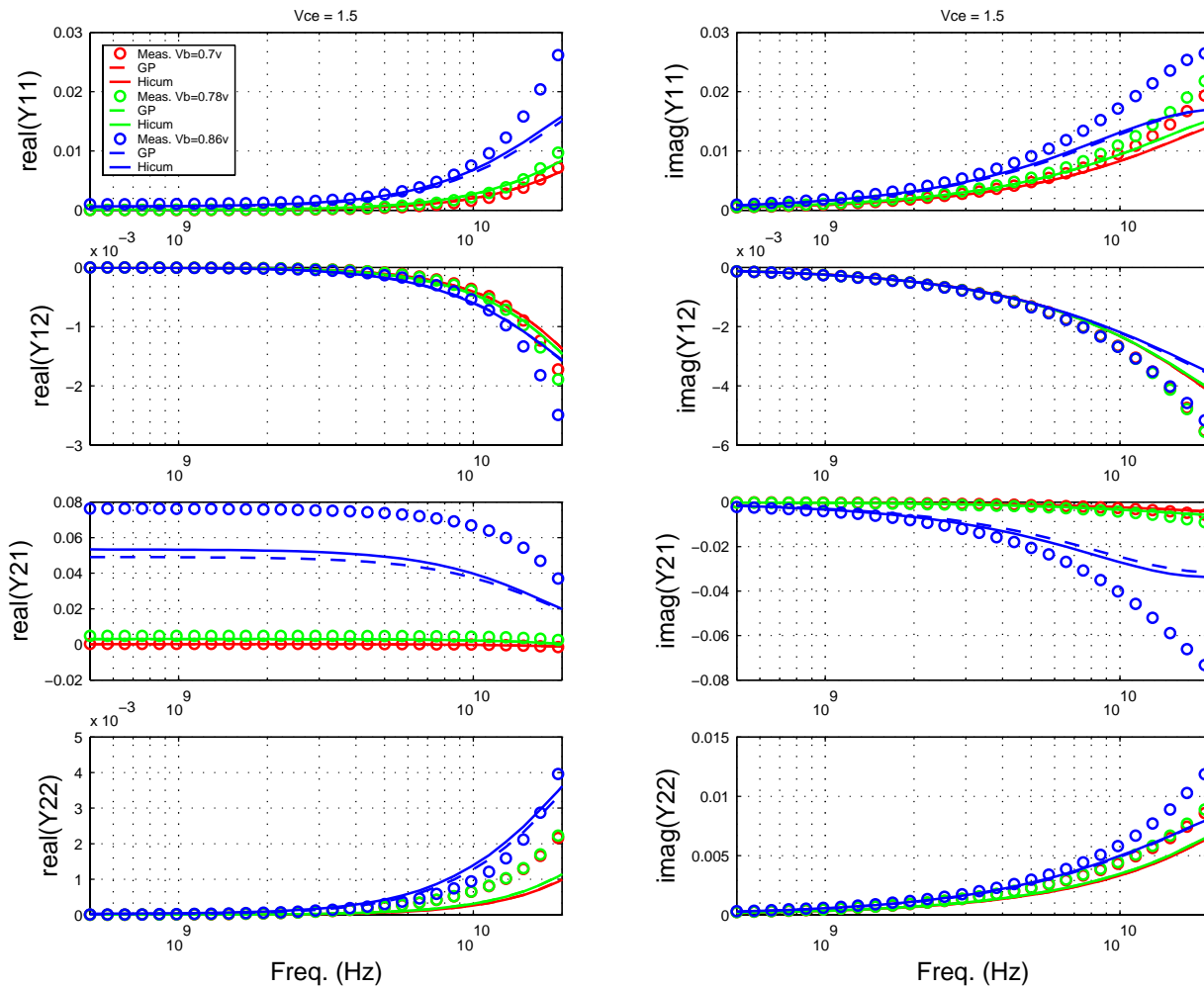


FIGURE 4.15 Gummel Plot: LV 0.28x10.0_452

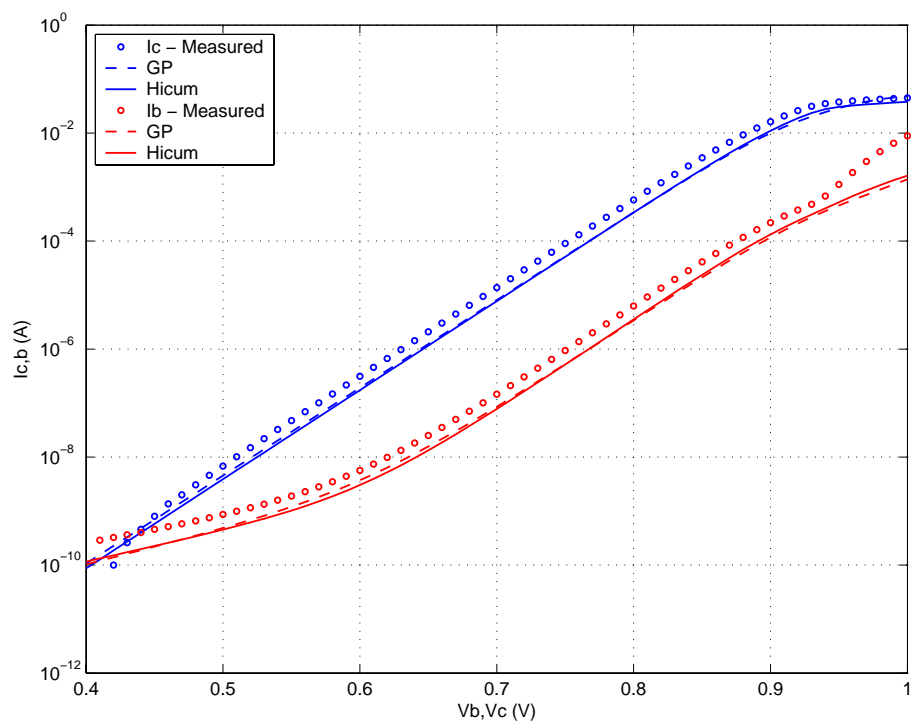


FIGURE 4.16 Beta vs Ic: LV 0.28x10.0_452

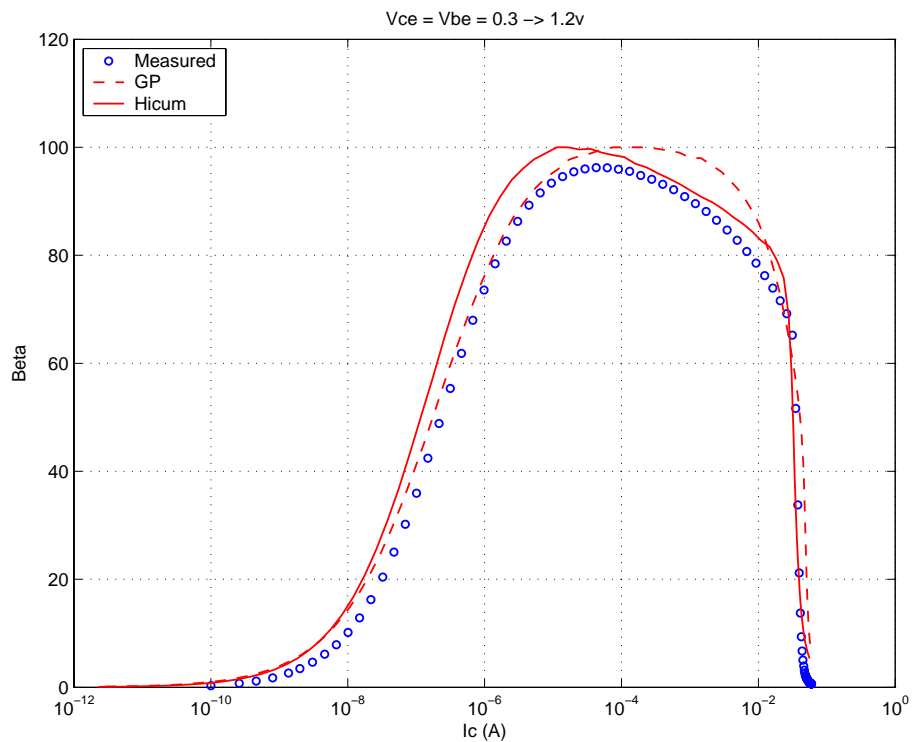


FIGURE 4.17 I_C vs. V_{CE} at constant I_B : LV 0.28x10.0_452

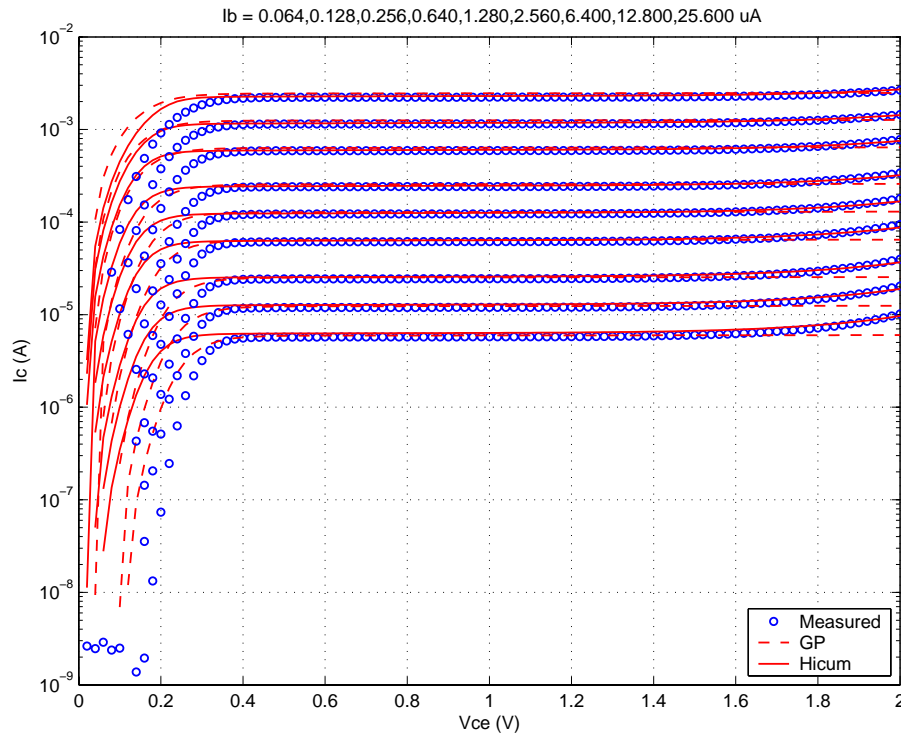


FIGURE 4.18 f_T vs. I_C : LV 0.28x10.0_452

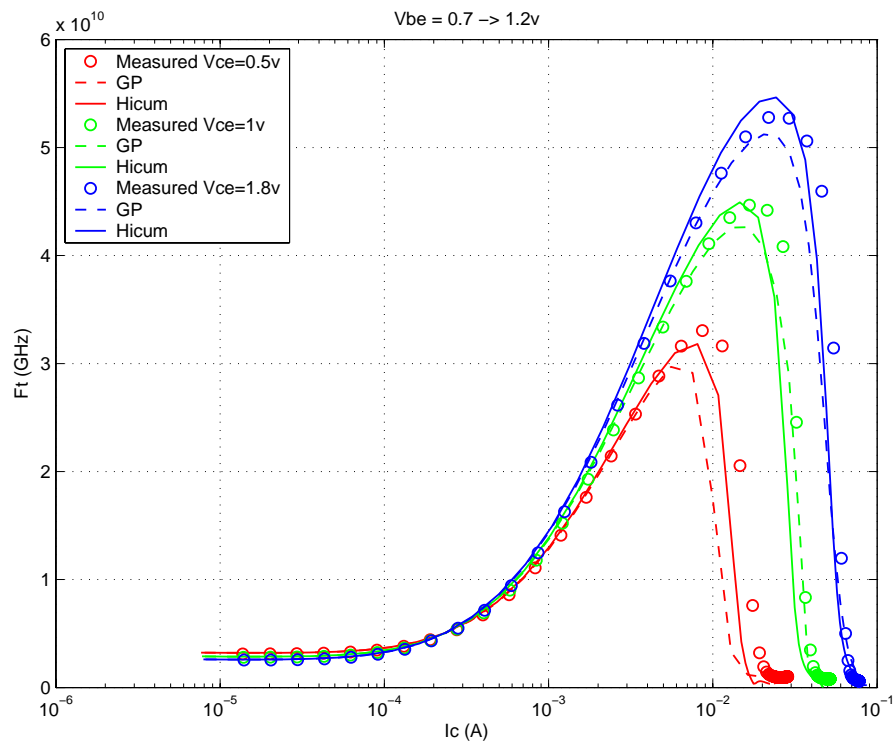
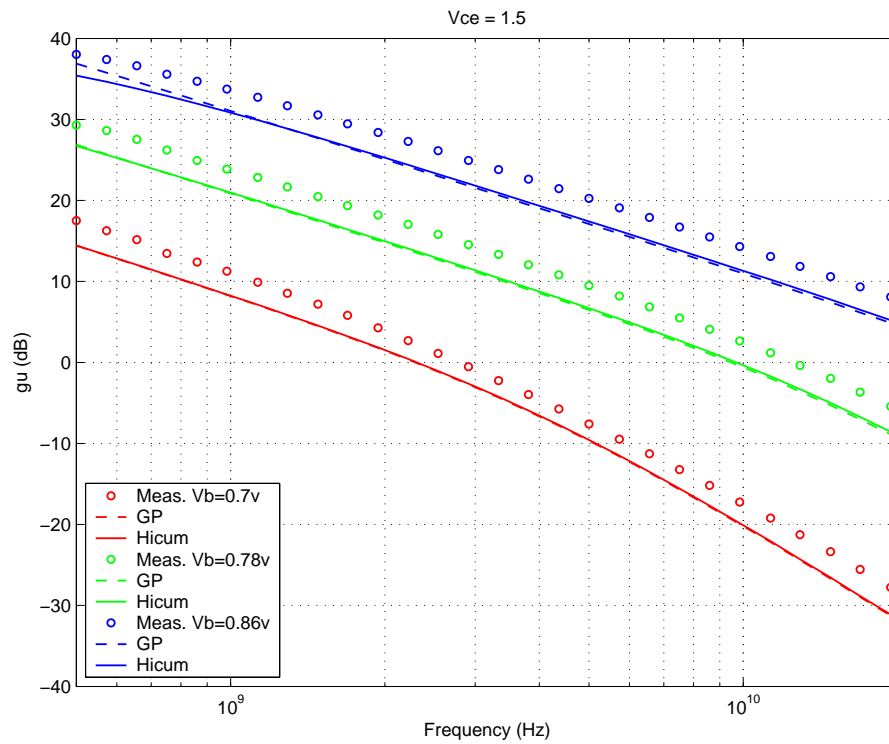
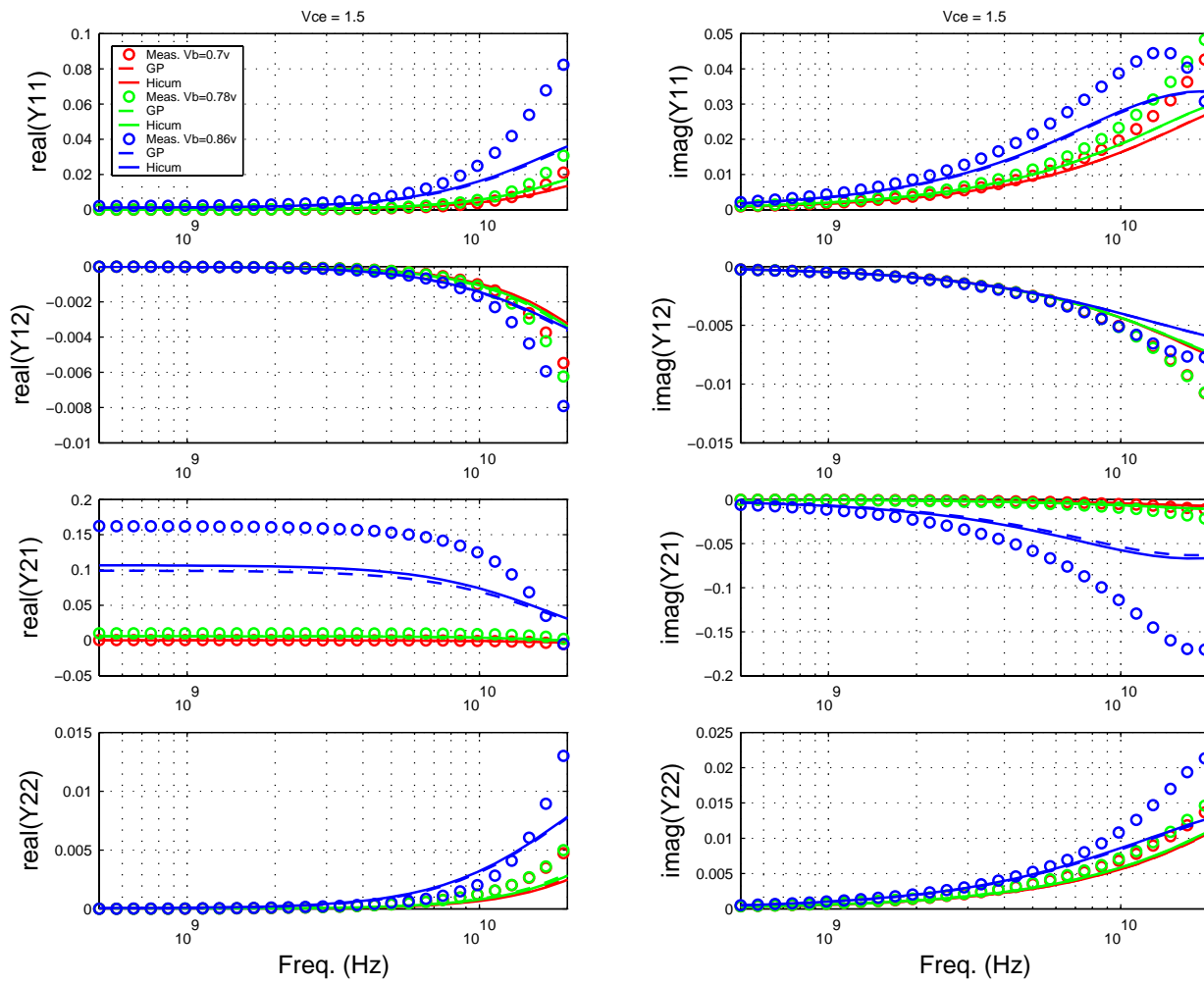


FIGURE 4.19 Power Gain vs. Freq: LV 0.28x10.0_452



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FIGURE 4.20 Y-parameters vs. FREQ: LV 0.28x10.0_452



4.4.2 Medium Voltage Verification Plots

FIGURE 4.21 Gummel Plot: MV 0.28x10.0_122

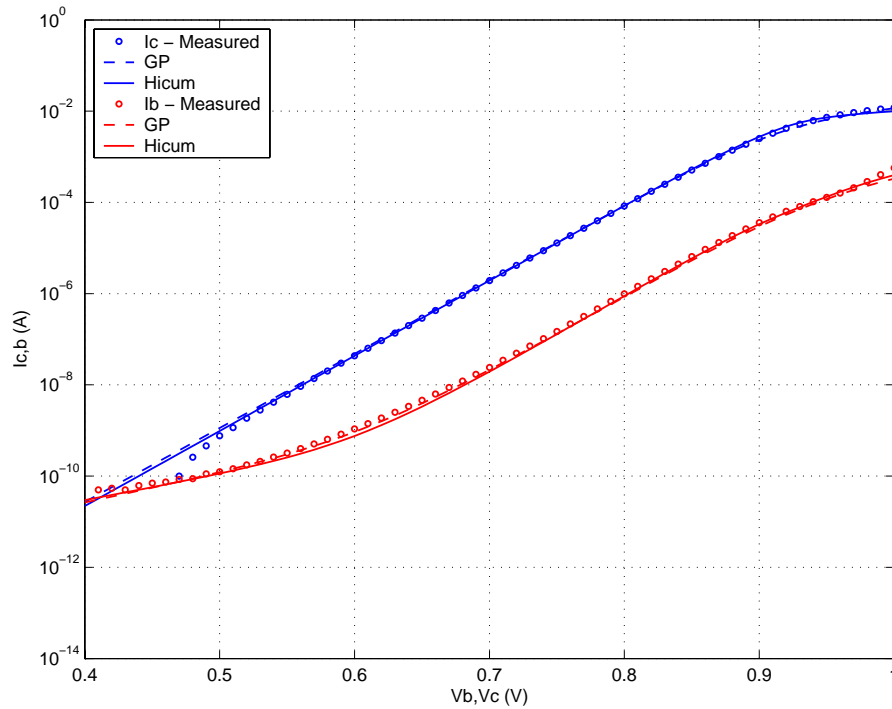
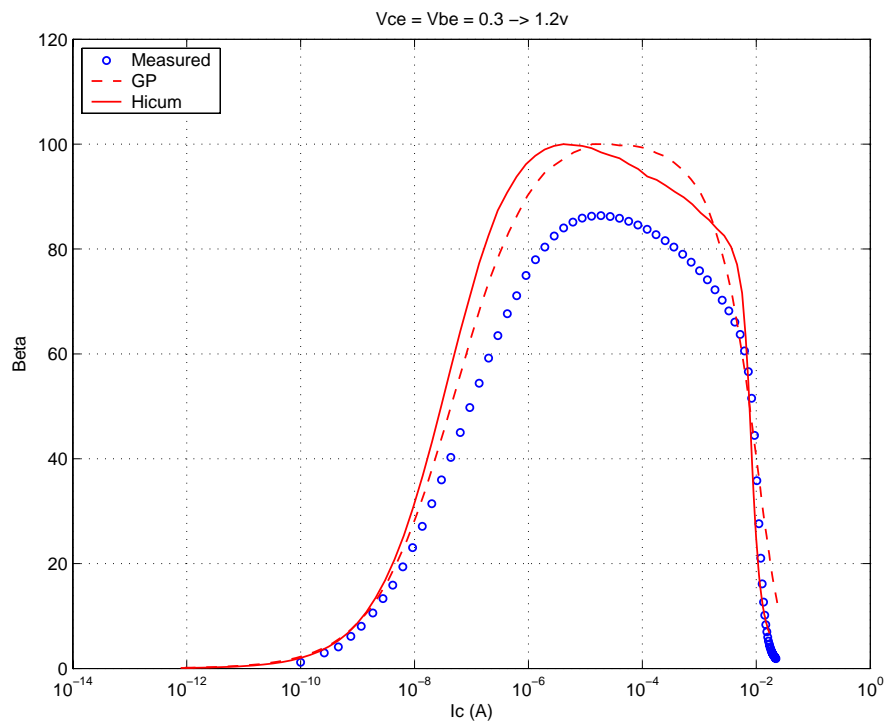
FIGURE 4.22 Beta vs I_c : MV 0.28x10.0_122

FIGURE 4.23 IC vs. VCE at constant IB: MV 0.28x10.0_122

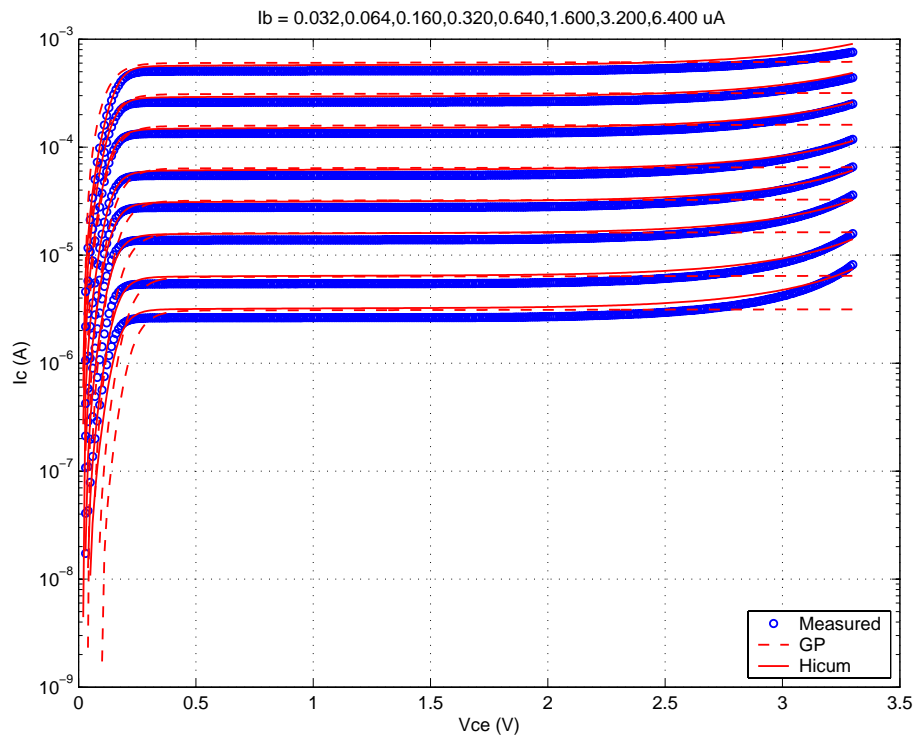


FIGURE 4.24 FT vs. IC: MV 0.28x10.0_122

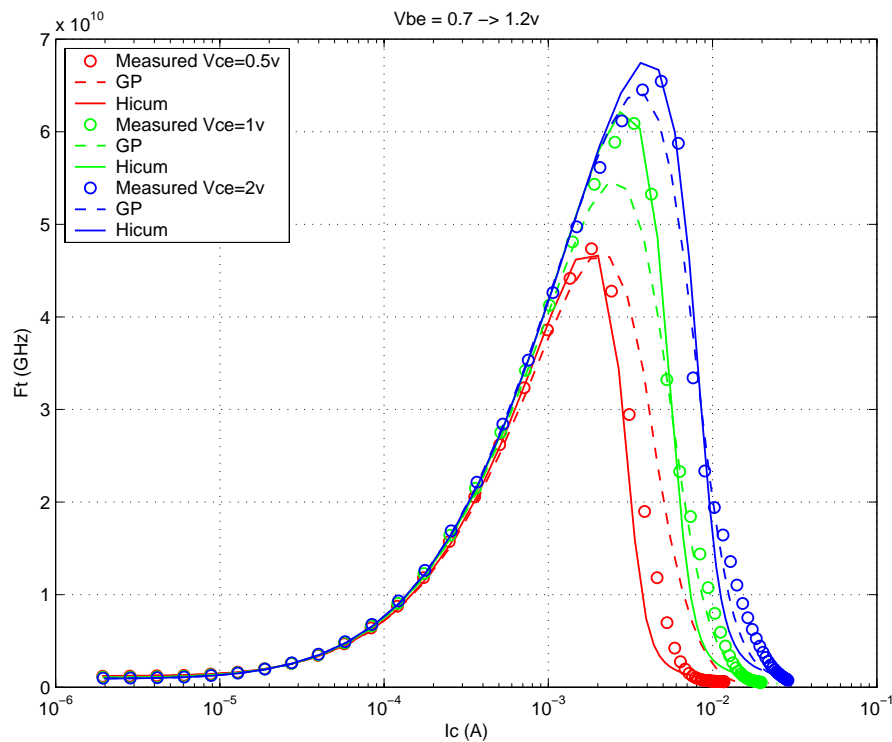
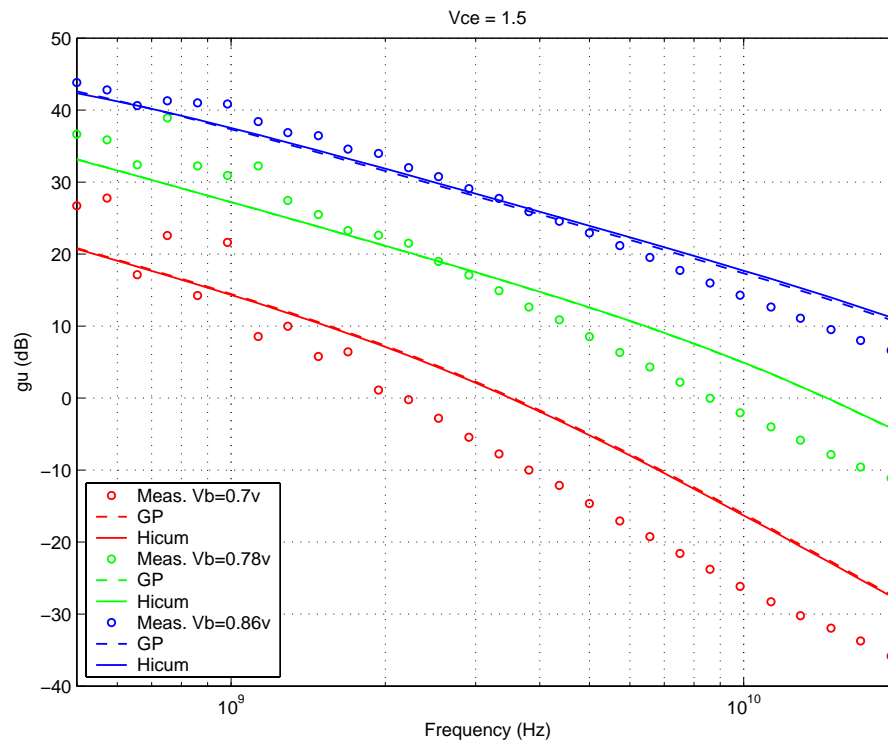


FIGURE 4.25 Power Gain vs. Freq: MV 0.28x10.0_122



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FIGURE 4.26 Y-parameters vs. FREQ: MV 0.28x10.0_122

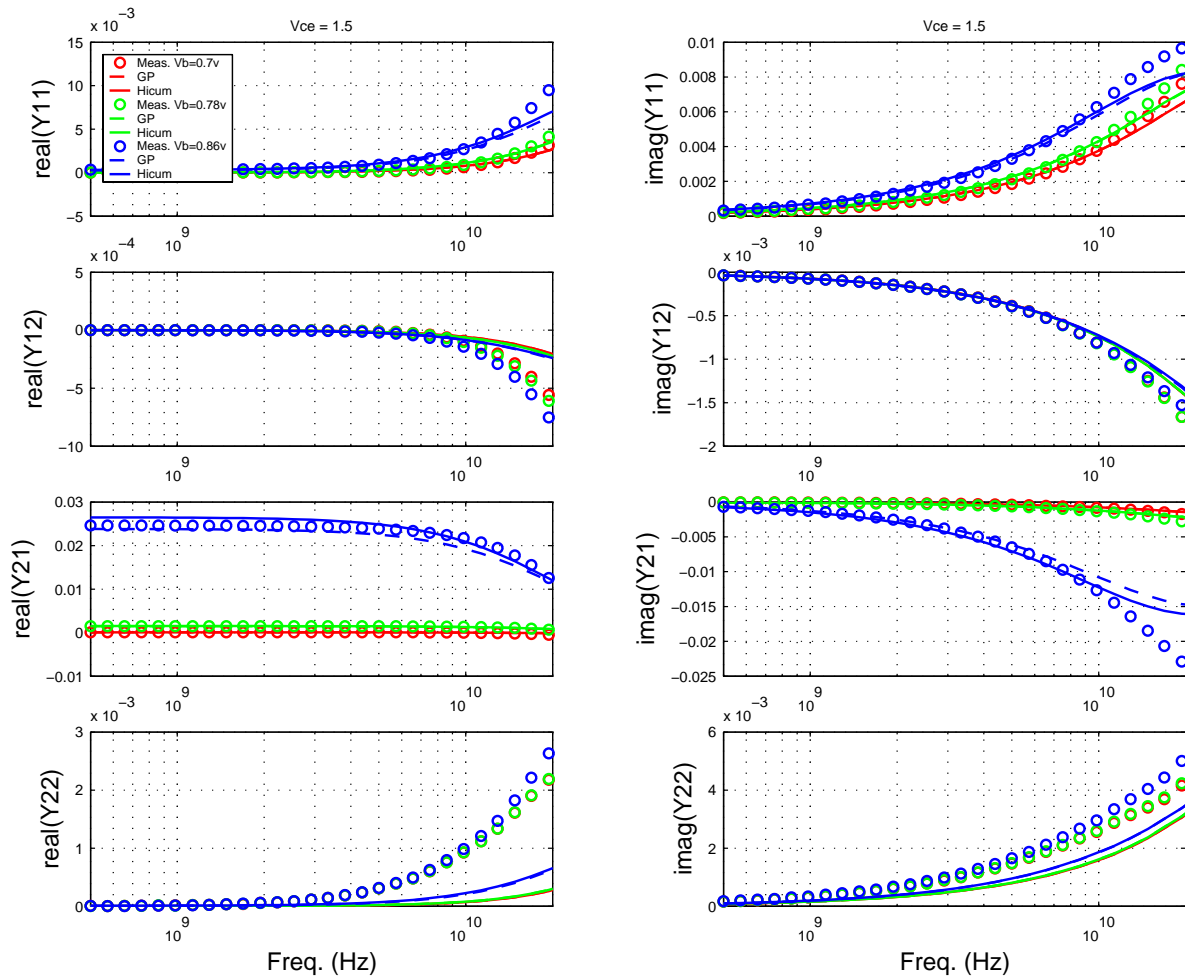


FIGURE 4.27 Gummel Plot: MV 0.28x10.0_232

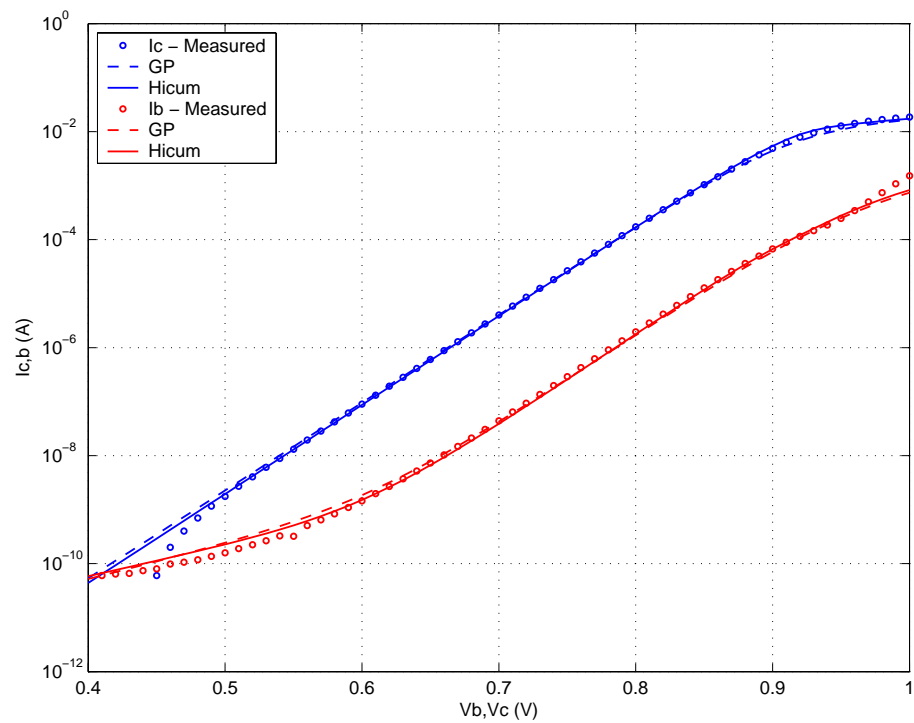
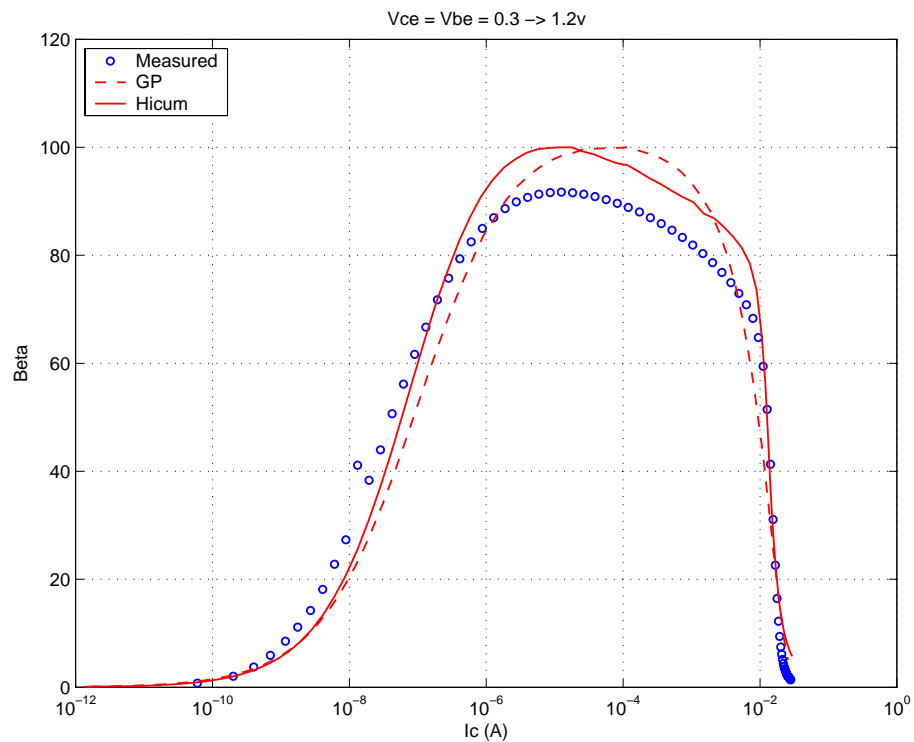
FIGURE 4.28 Beta vs I_c : MV 0.28x10.0_232

FIGURE 4.29 IC vs. VCE at constant IB: MV 0.28x10.0_232

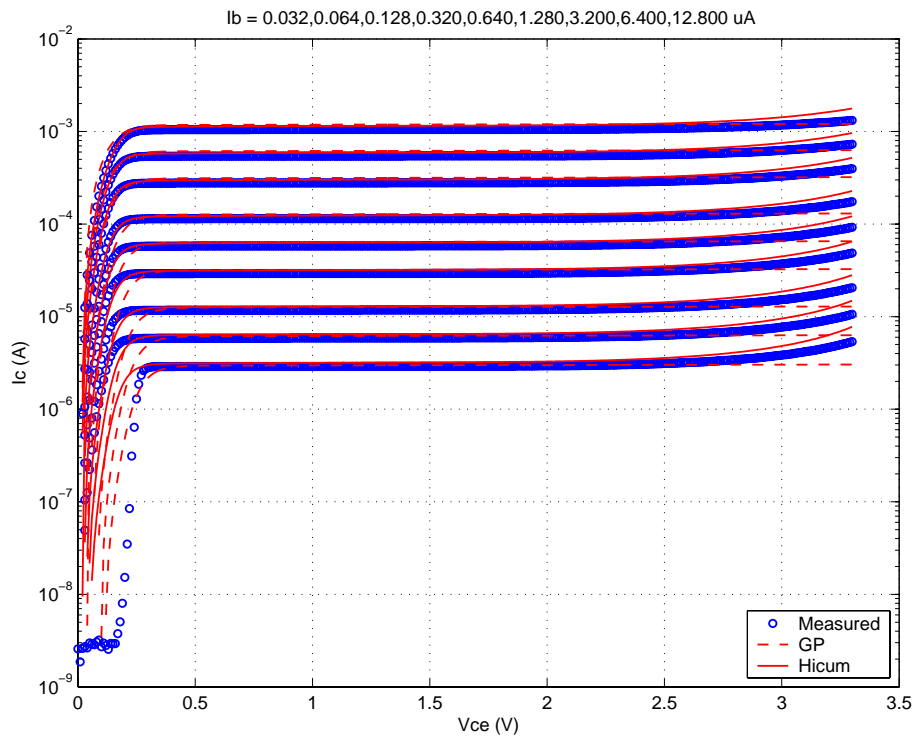


FIGURE 4.30 FT vs. IC: MV 0.28x10.0_232

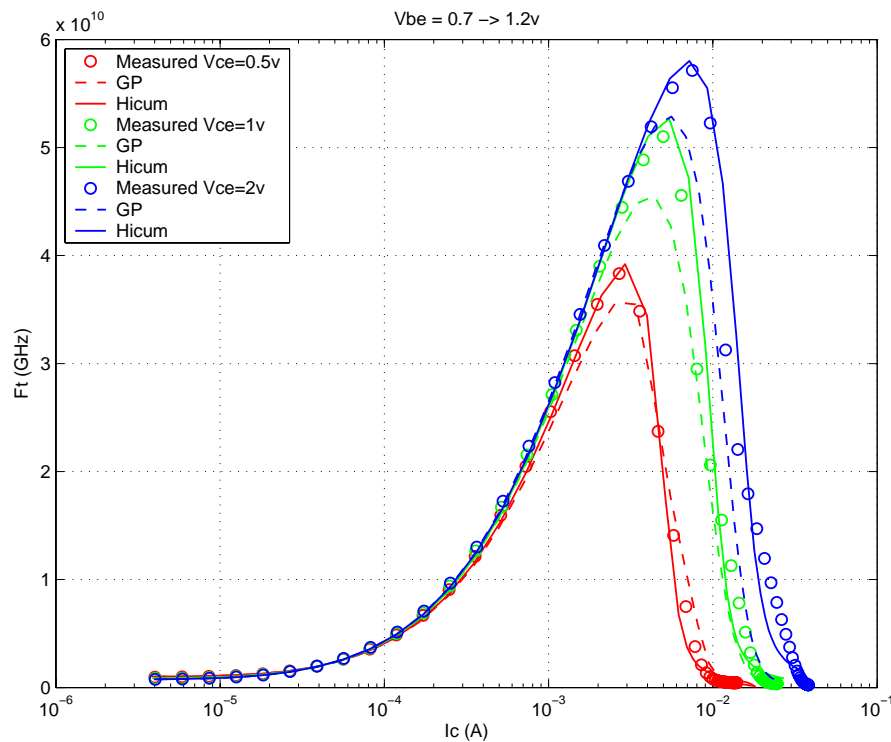
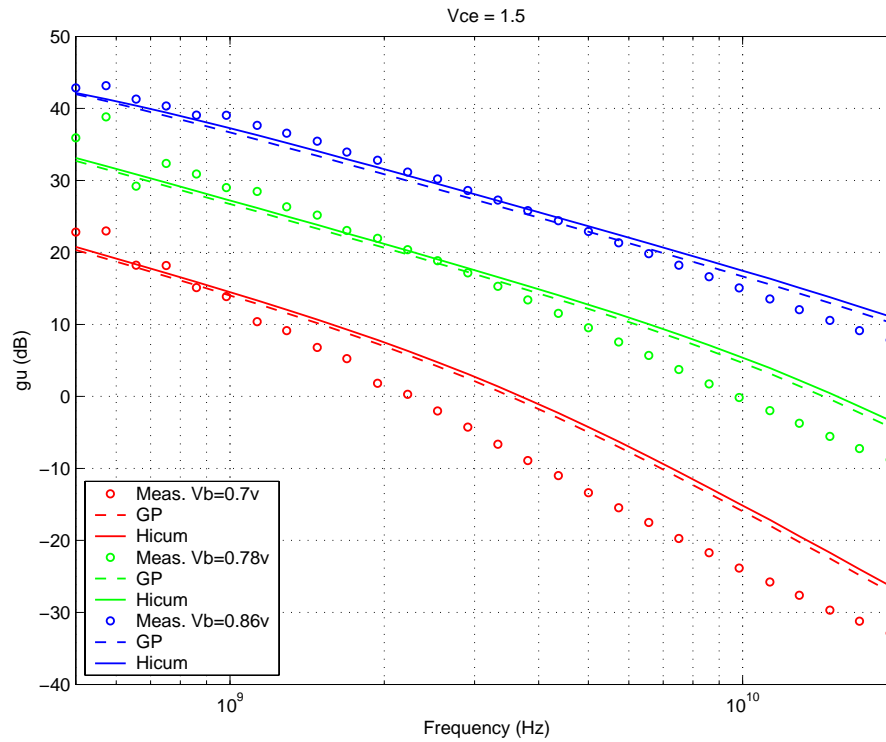


FIGURE 4.31 Power Gain vs. Freq: MV 0.28x10.0_232



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FIGURE 4.32 Y-parameters vs. FREQ: MV 0.28x10.0_232

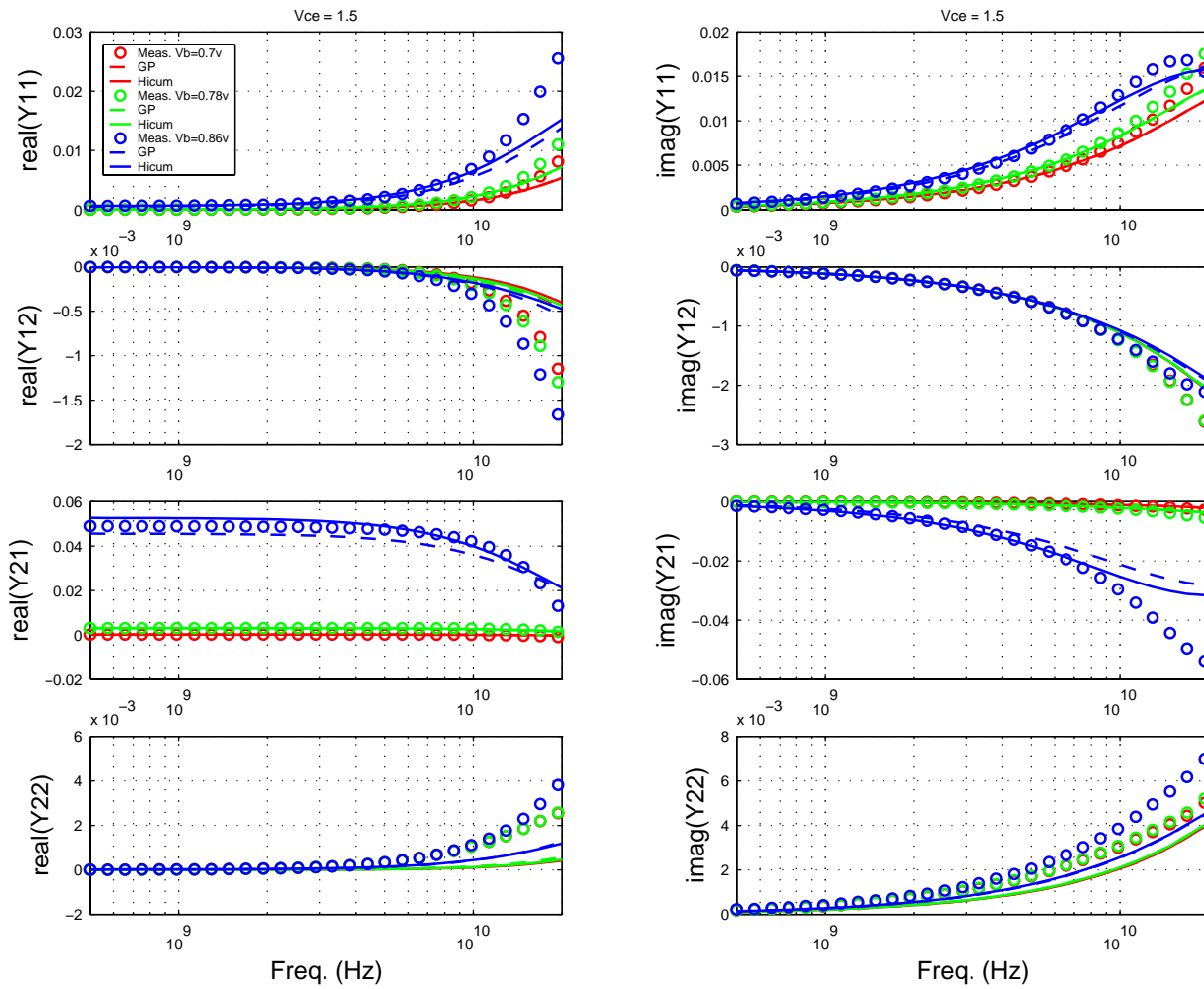


FIGURE 4.33 Gummel Plot: MV 0.28x10.0_452

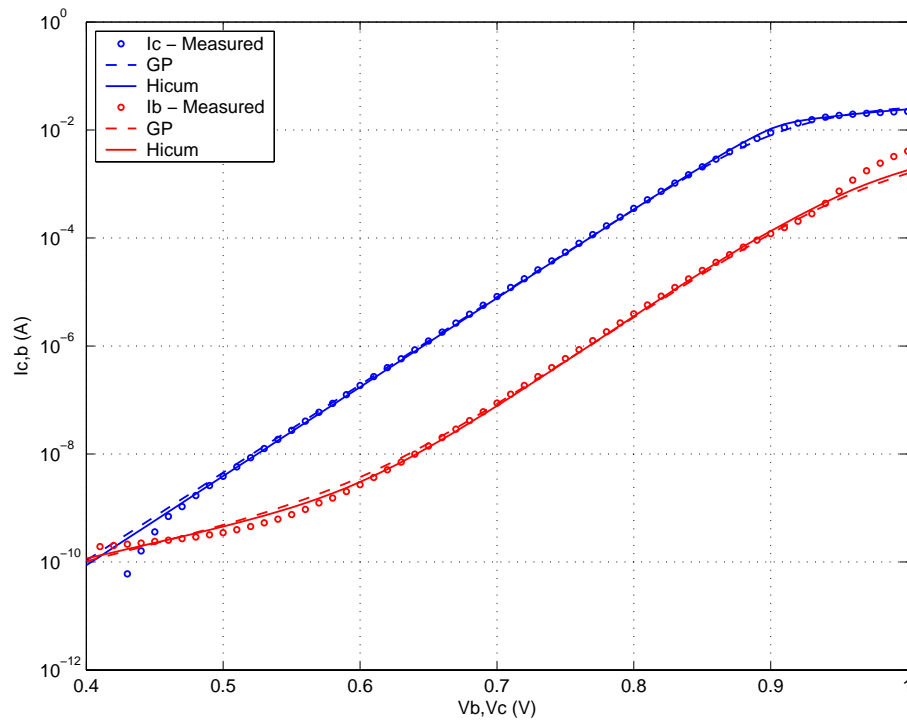
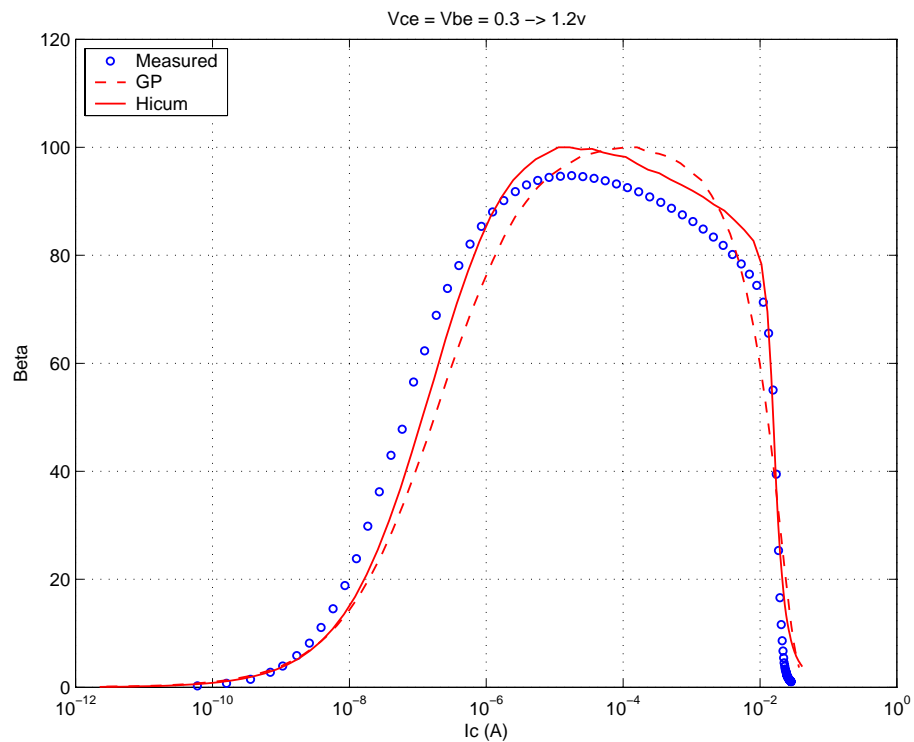
FIGURE 4.34 Beta vs I_c : MV 0.28x10.0_452

FIGURE 4.35 I_C vs. V_{CE} at constant I_B : MV 0.28x10.0_452

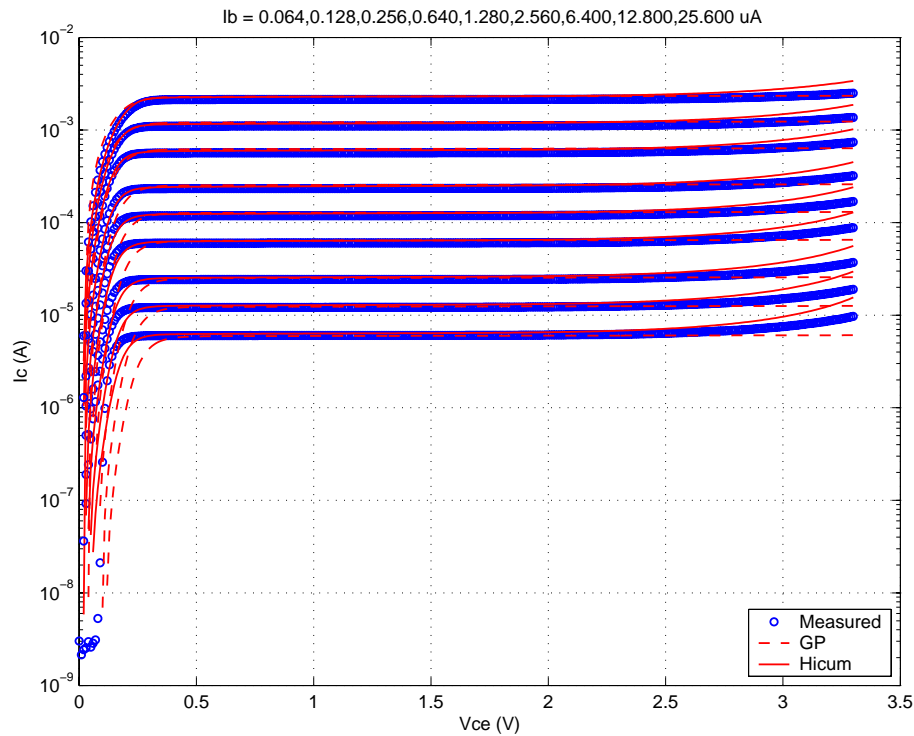


FIGURE 4.36 F_T vs. I_C : MV 0.28x10.0_452

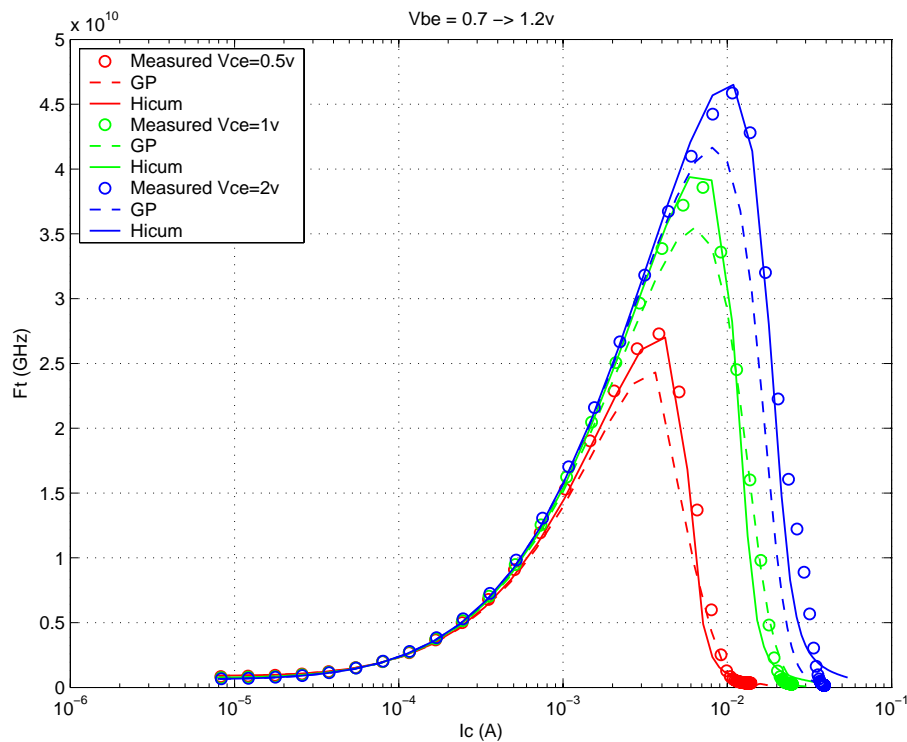
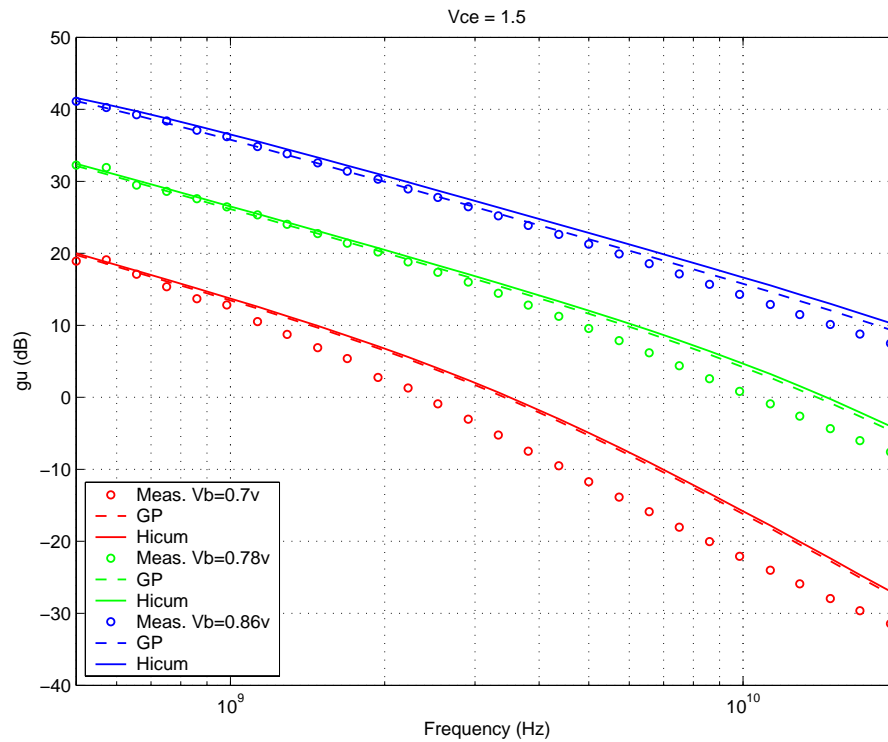
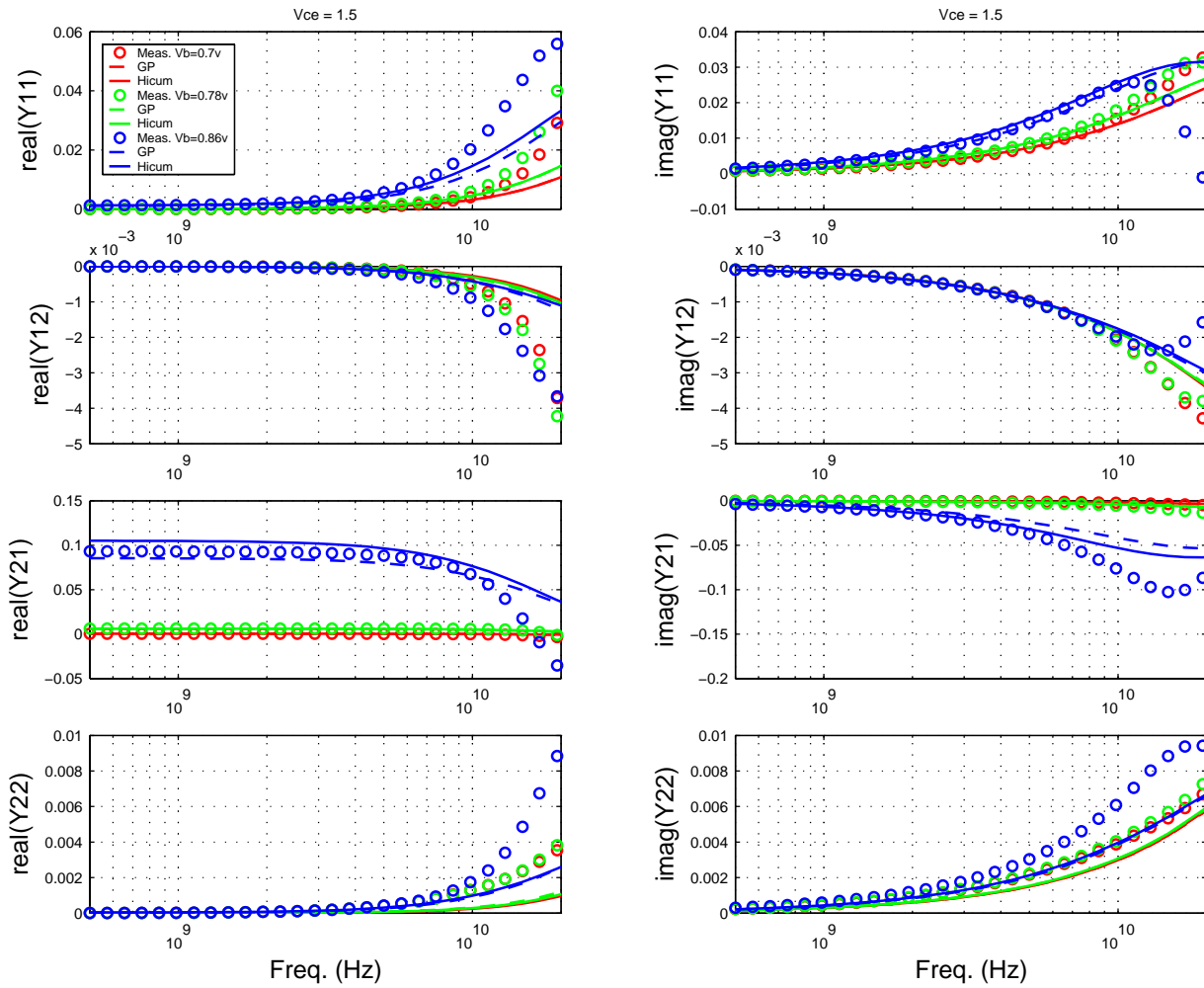


FIGURE 4.37 Power Gain vs. Freq: MV 0.28x10.0_452



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IP: 128.173.89.96

FIGURE 4.38 Y-parameters vs. FREQ: MV 0.28x10.0_452



4.4.3 High Voltage Verification Plots

FIGURE 4.39 Gummel Plot: HV 0.28x10.0_122

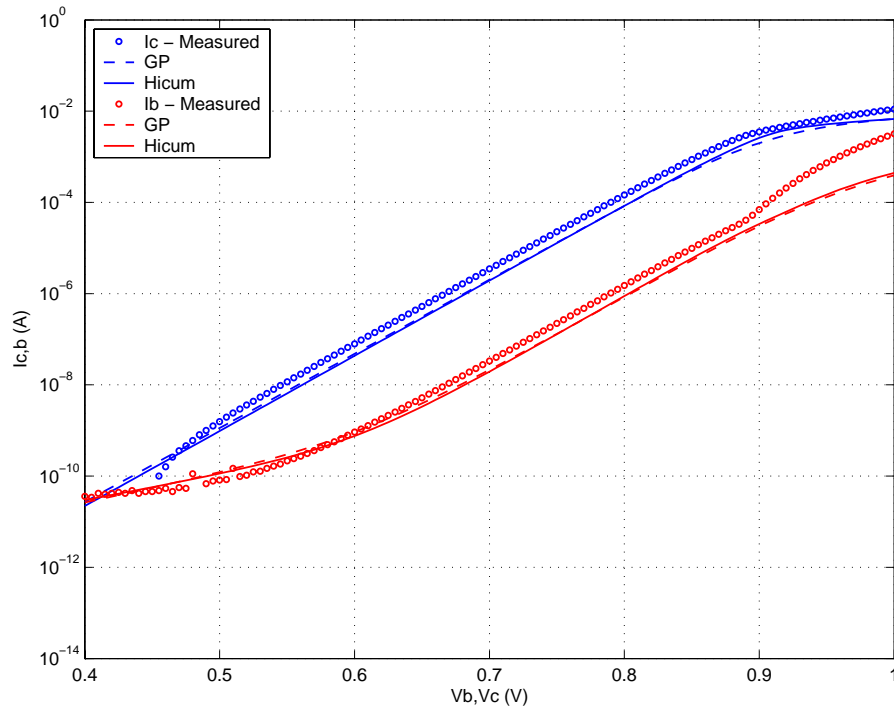


FIGURE 4.40 Beta Vs. I_c : HV 0.28x10.0_122

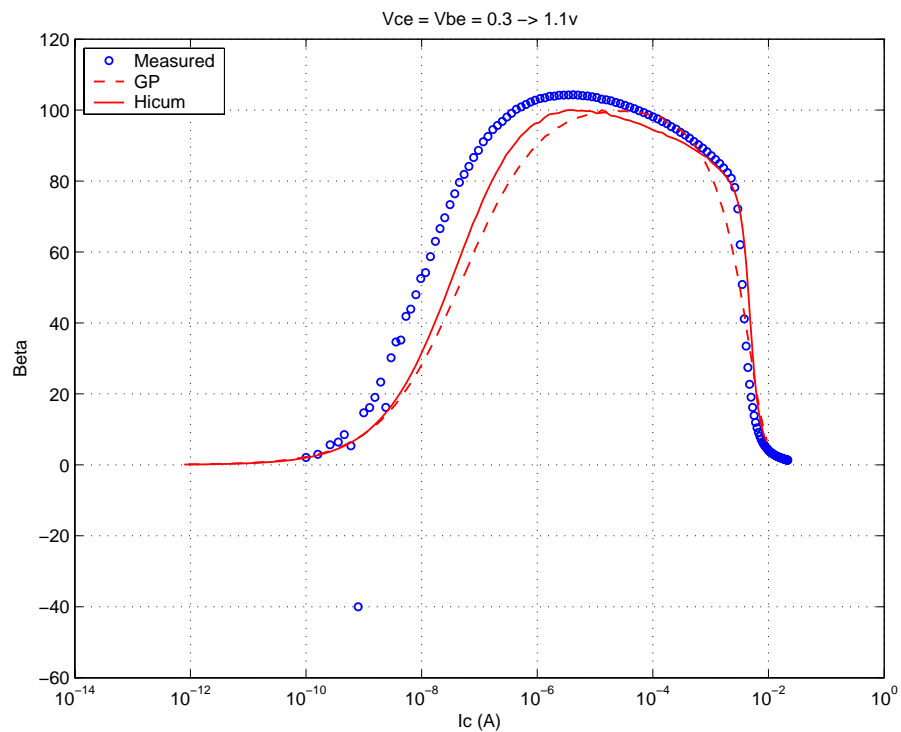


FIGURE 4.41 IC vs. VCE at constant IB: HV 0.28x10.0_122

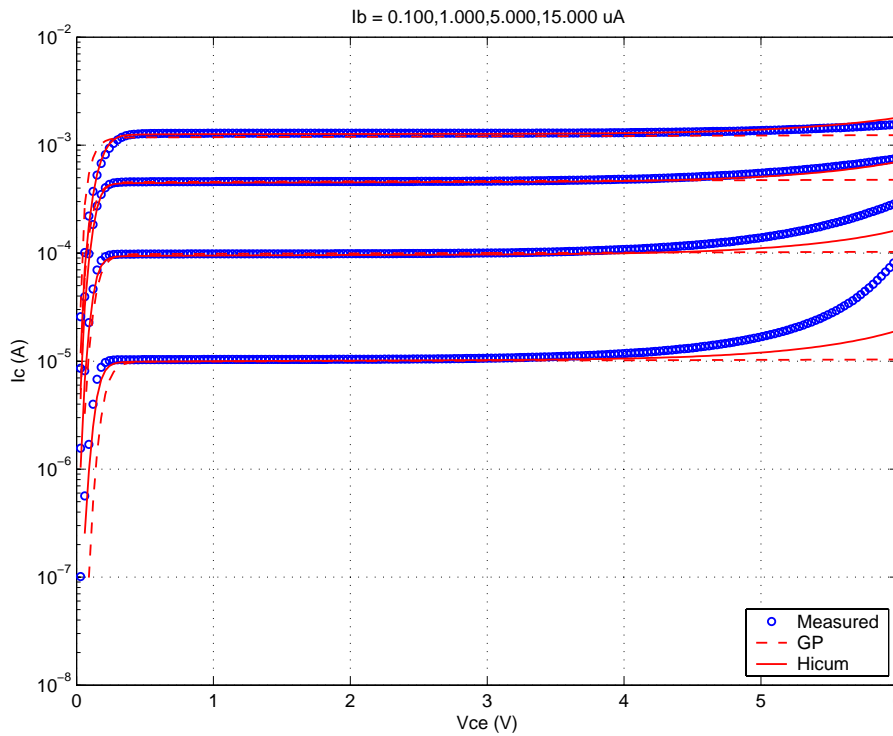


FIGURE 4.42 FT vs. IC: HV 0.28x10.0_122

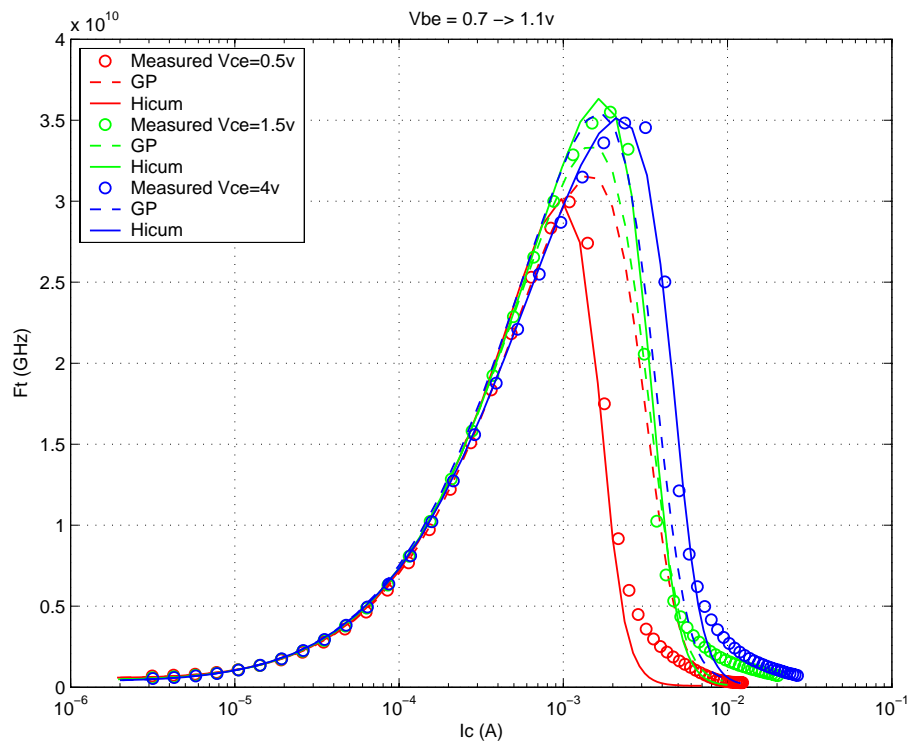
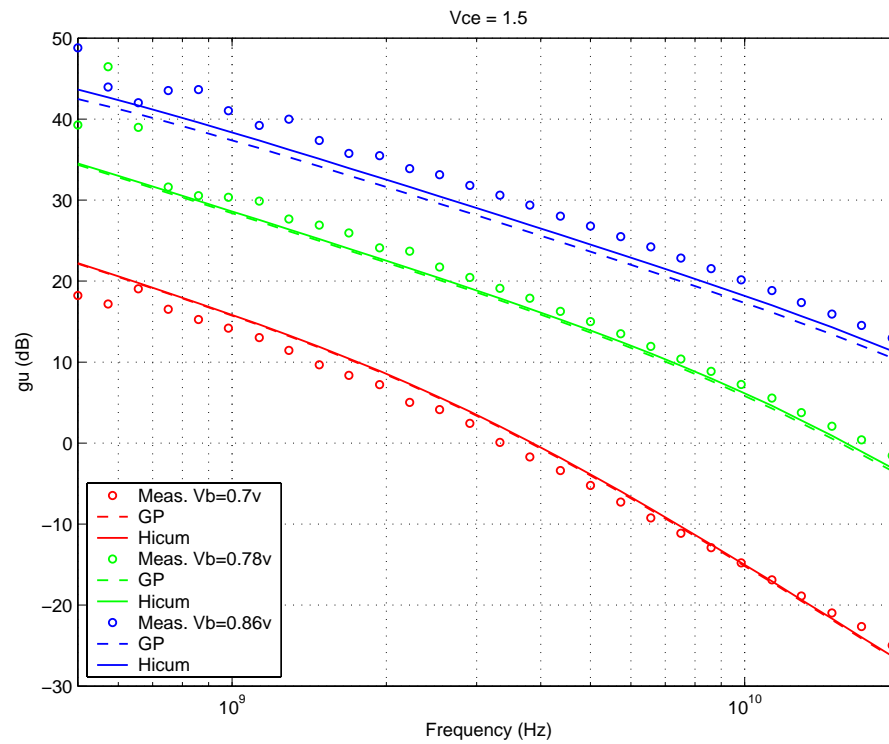


FIGURE 4.43 Power Gain vs. Freq: HV 0.28x10.0_122



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FIGURE 4.44 Y-parameters vs. FREQ: HV 0.28x10.0_122

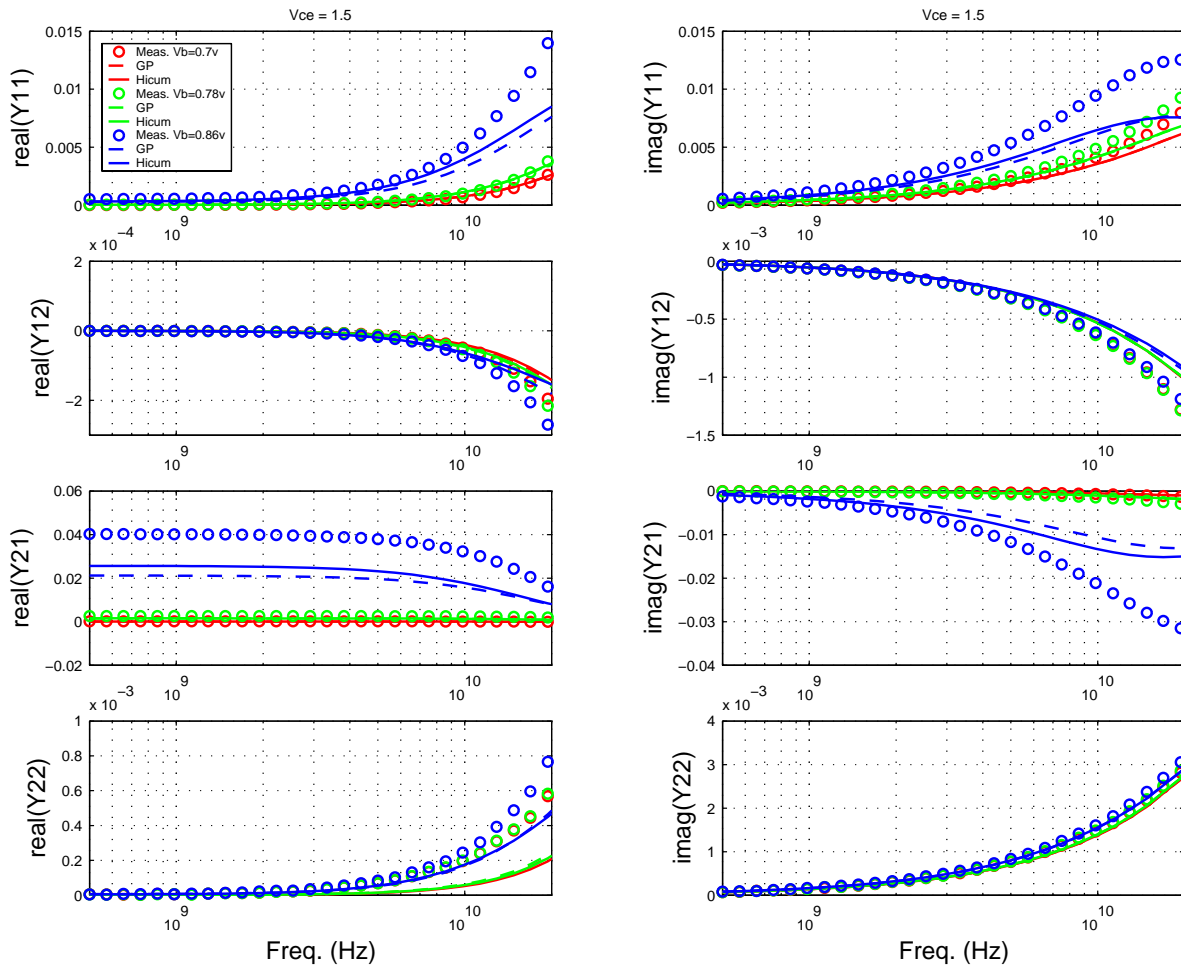


FIGURE 4.45 Gummel Plot: HV 0.28x10.0_232

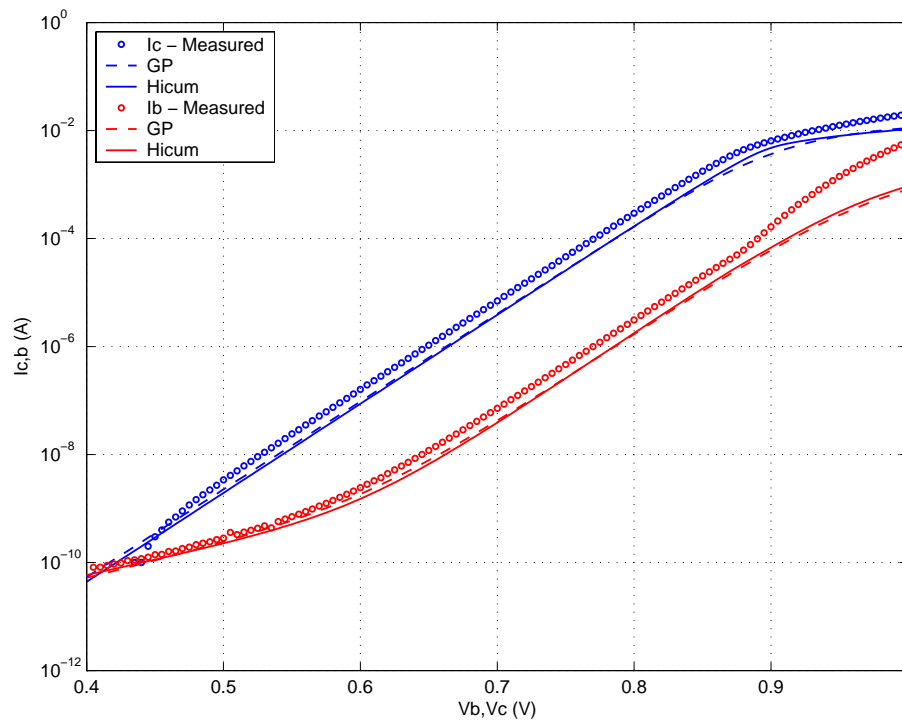
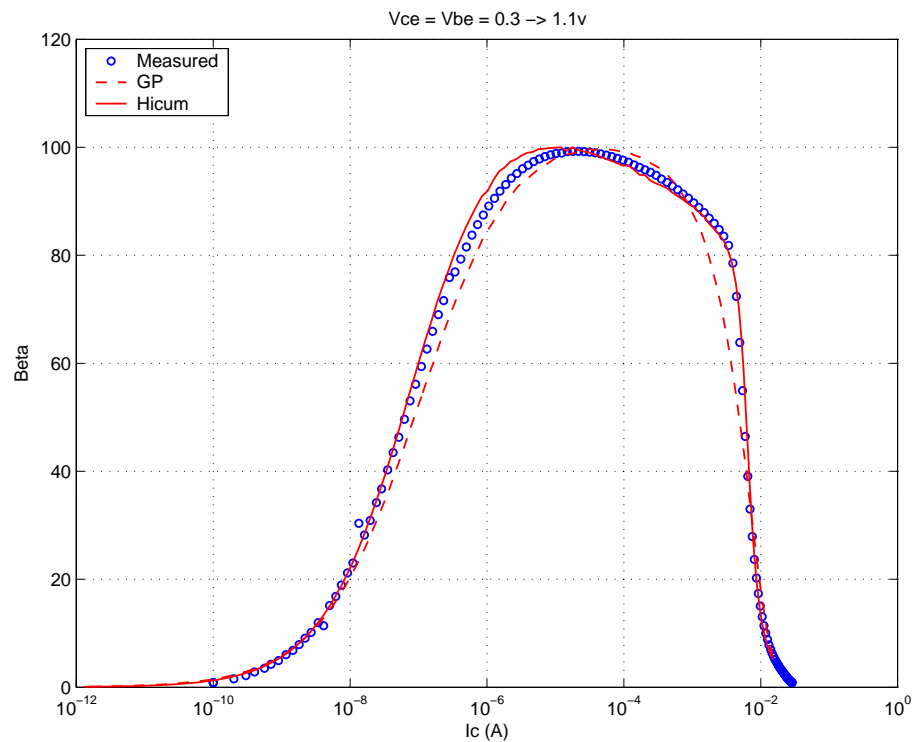
FIGURE 4.46 Beta vs I_c : HV 0.28x10.0_232

FIGURE 4.47 I_C vs. V_{CE} at constant I_B : HV 0.28x10.0_232

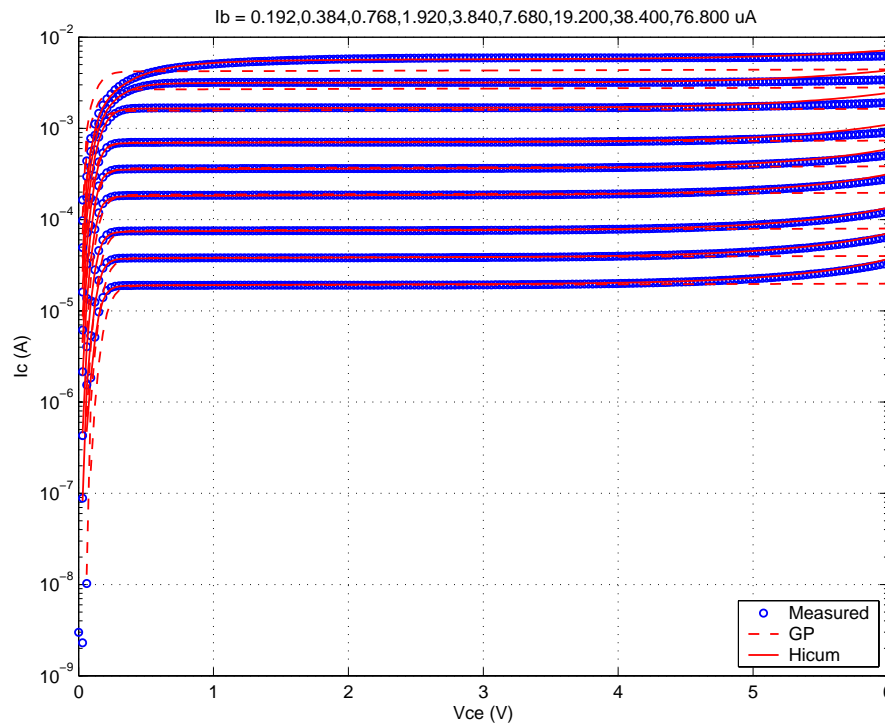


FIGURE 4.48 F_T vs. I_C : HV 0.28x10.0_232

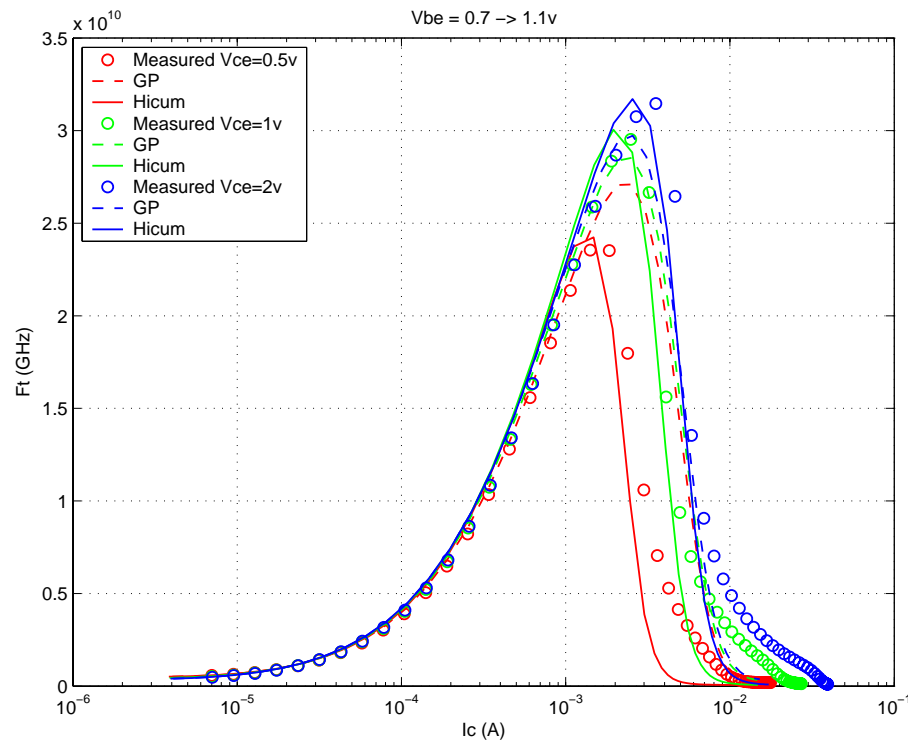
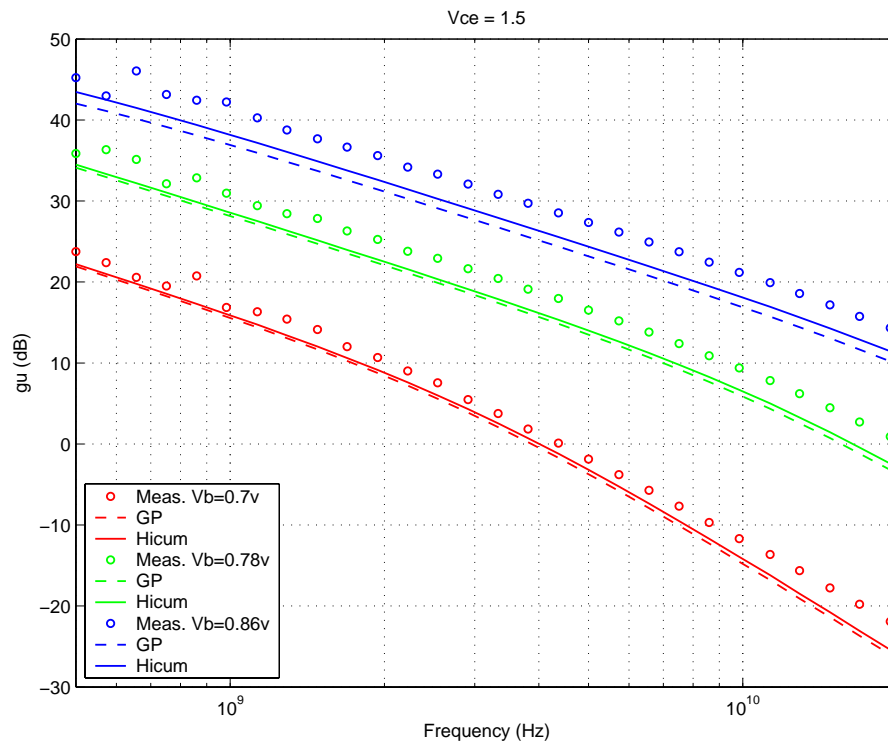


FIGURE 4.49 Power Gain vs. Freq: HV 0.28x10.0_232



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FIGURE 4.50 Y-parameters vs. FREQ: HV 0.28x10.0_232

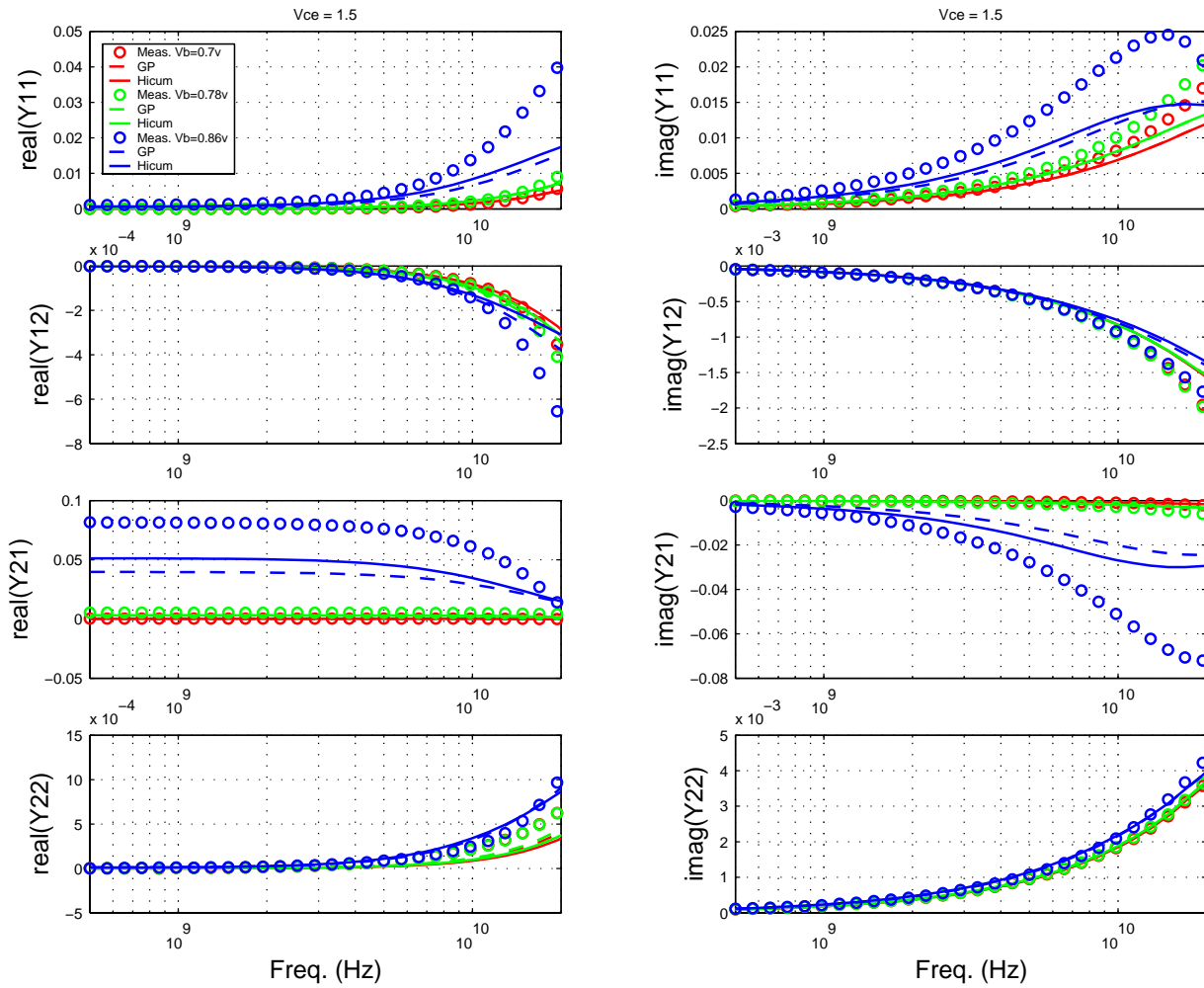


FIGURE 4.51 Gummel Plot: HV 0.28x10.0_452

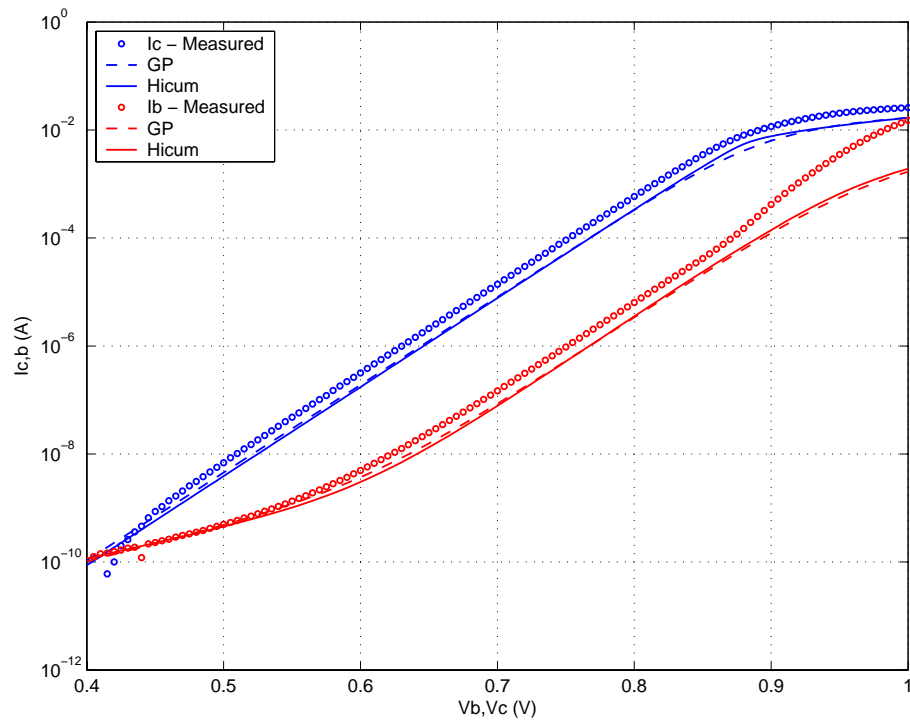
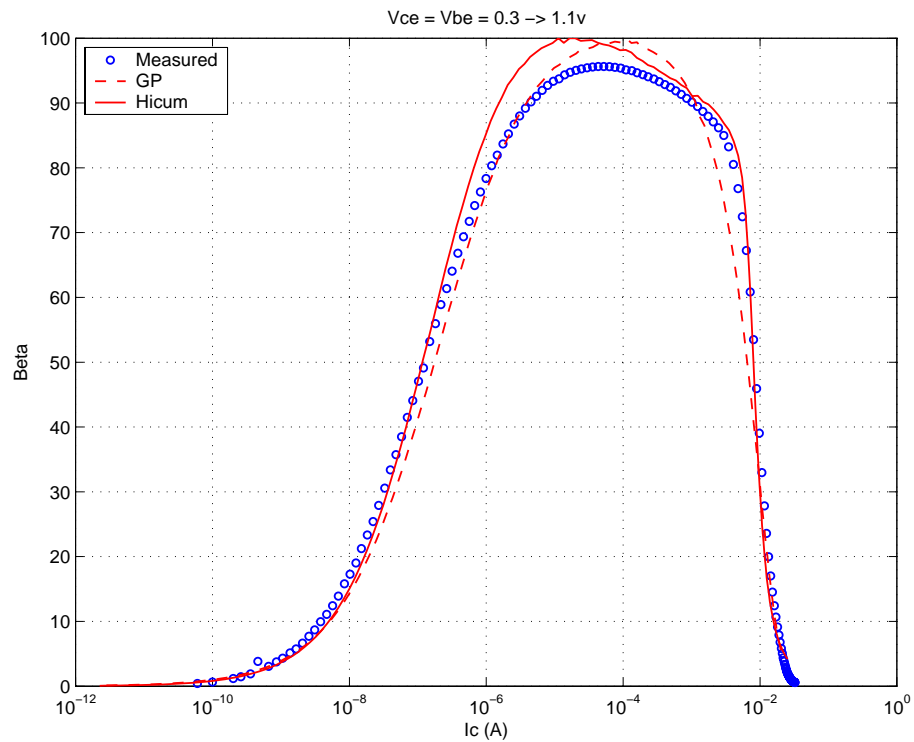
FIGURE 4.52 Beta vs I_c : HV 0.28x10.0_452

FIGURE 4.53 IC vs. VCE at constant IB: HV 0.28x10.0_452

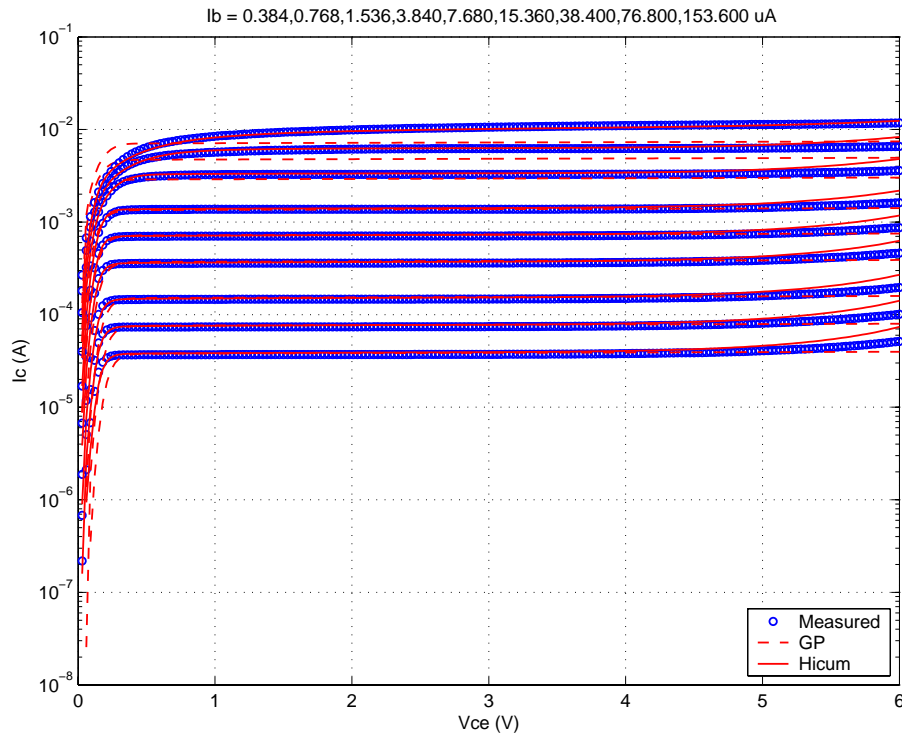


FIGURE 4.54 FT vs. IC: HV 0.28x10.0_452

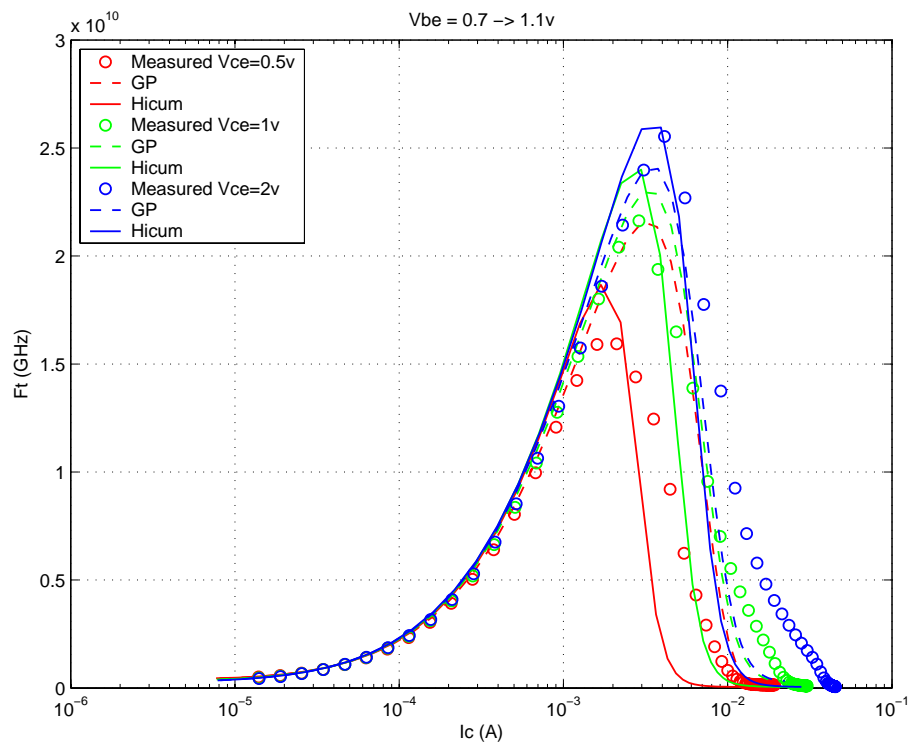
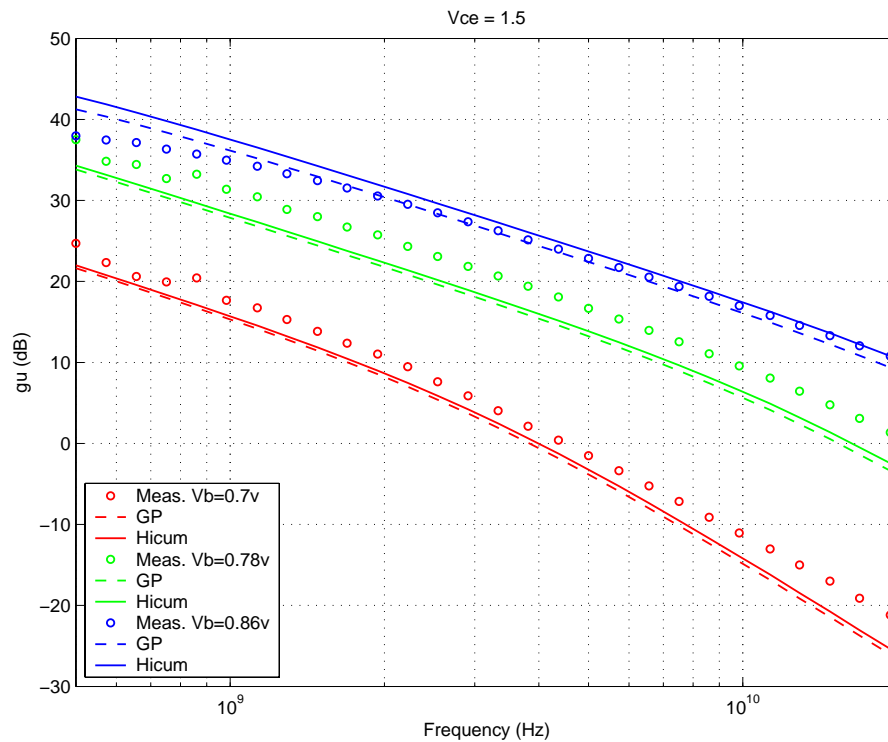


FIGURE 4.55 Power Gain vs. Freq: HV 0.28x10.0_452



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FIGURE 4.56 Y-parameters vs. FREQ: HV 0.28x10.0_452

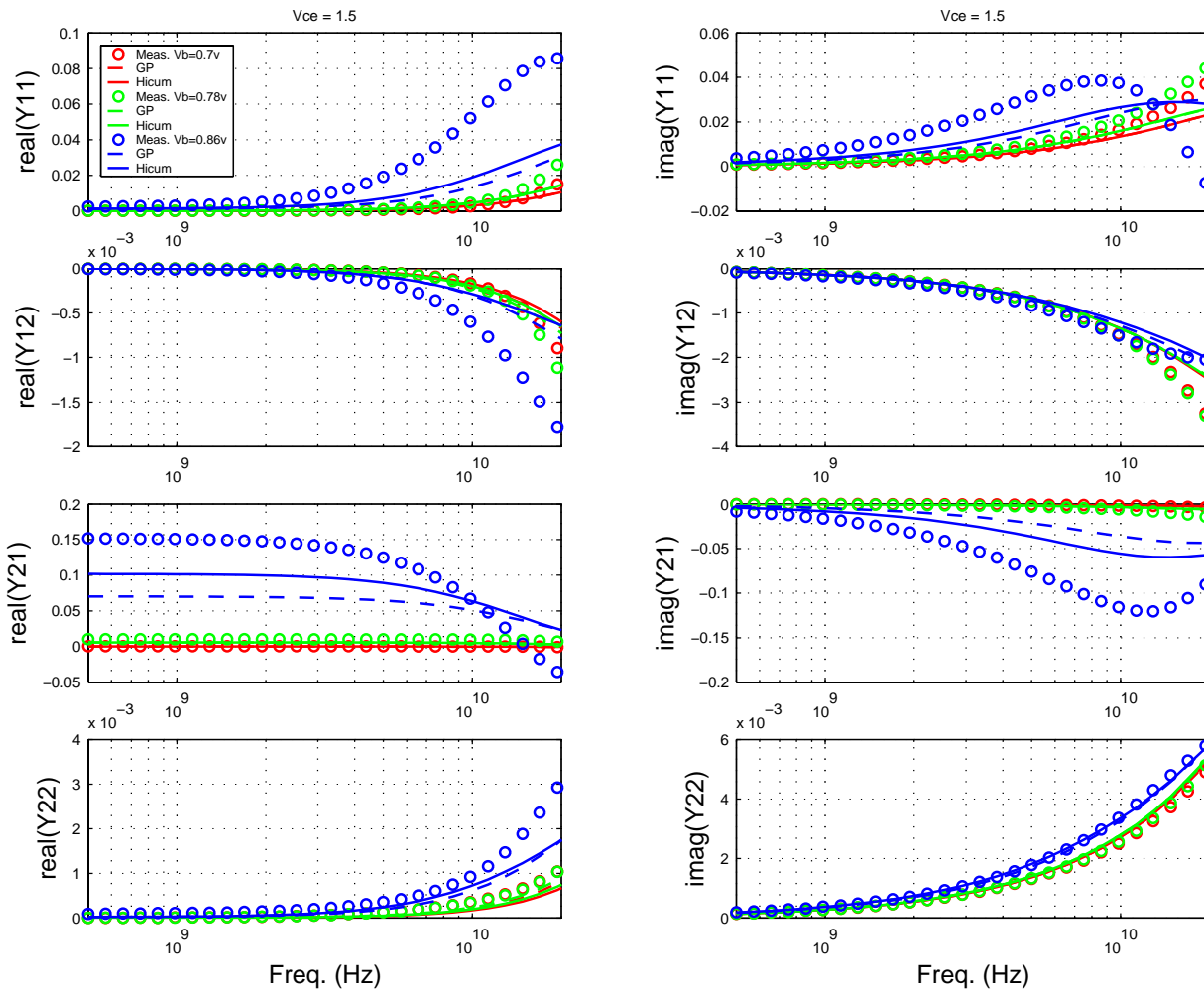


FIGURE 4.57 Gummel Plot: HV 0.96x10.0_232

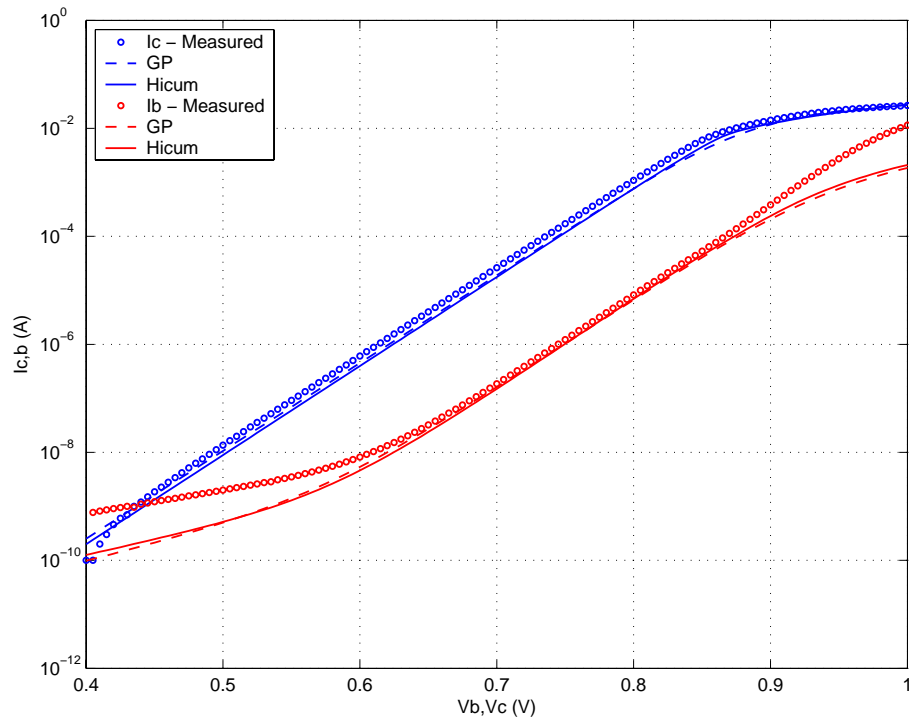
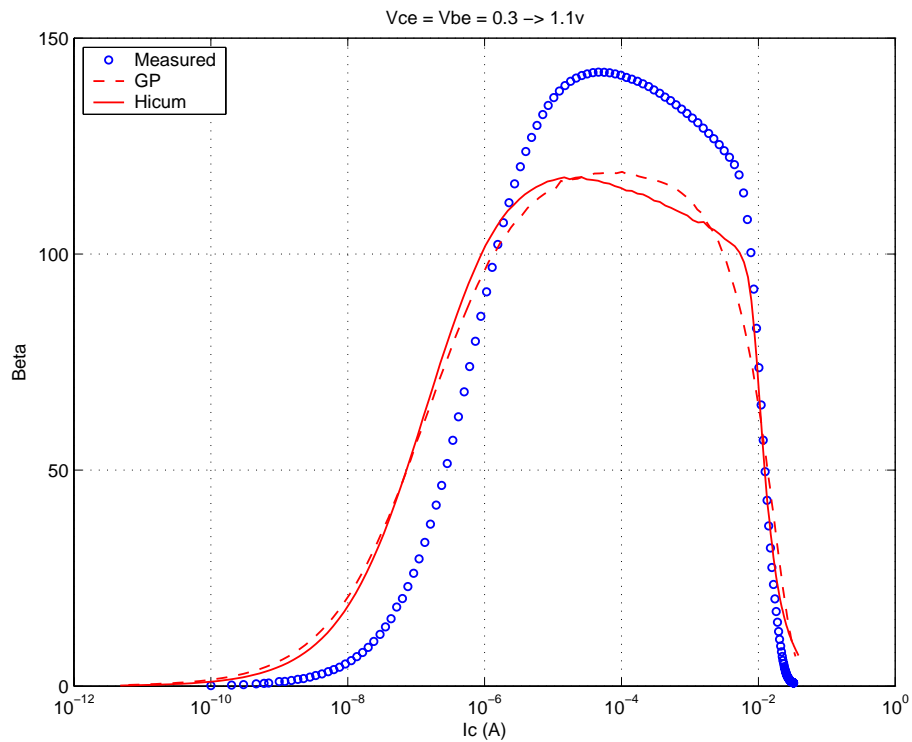
FIGURE 4.58 Beta vs. I_c : HV 0.96x10.0_232

FIGURE 4.59 I_C vs. V_{CE} at constant I_B : HV 0.96x10.0_232

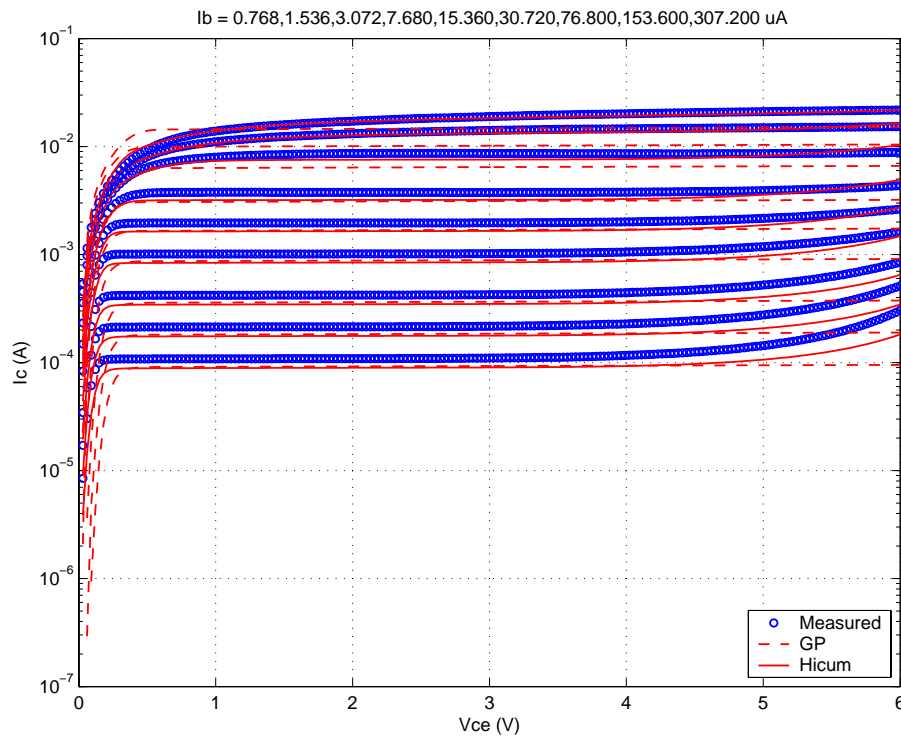


FIGURE 4.60 F_T vs. I_C : HV 0.96x10.0_232

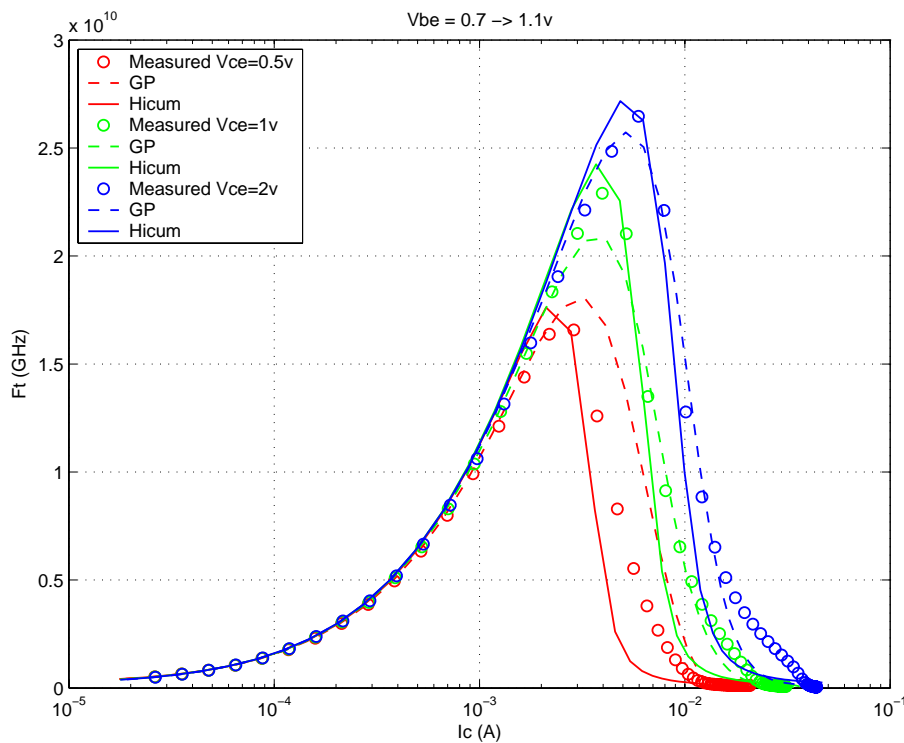
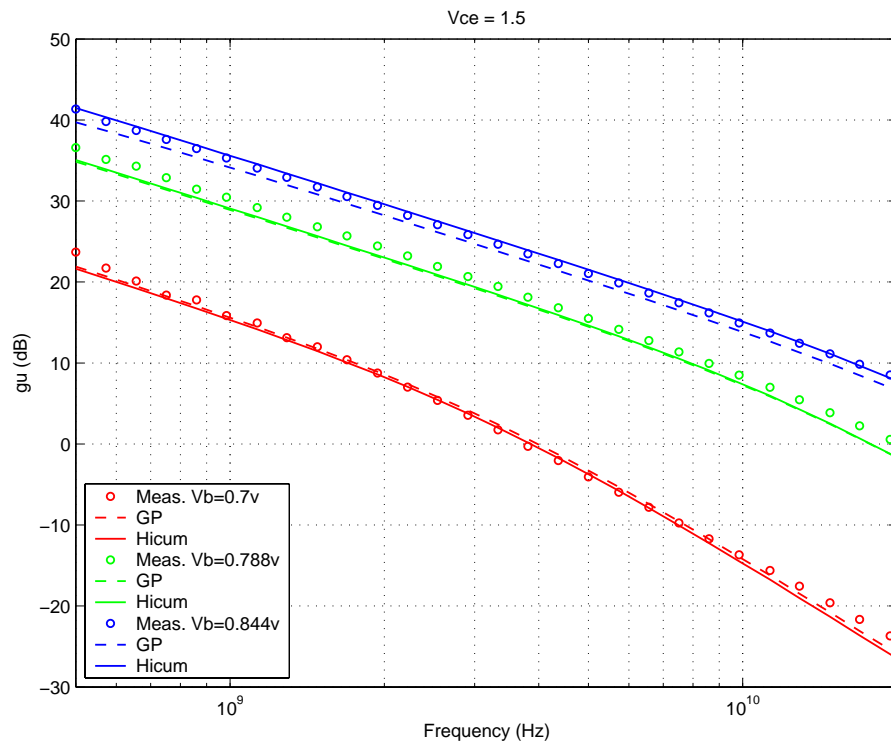


FIGURE 4.61 Power Gain vs. Freq: HV 0.96x10.0_232



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FIGURE 4.62 Y-parameters vs. FREQ: HV 0.96x10.0_232

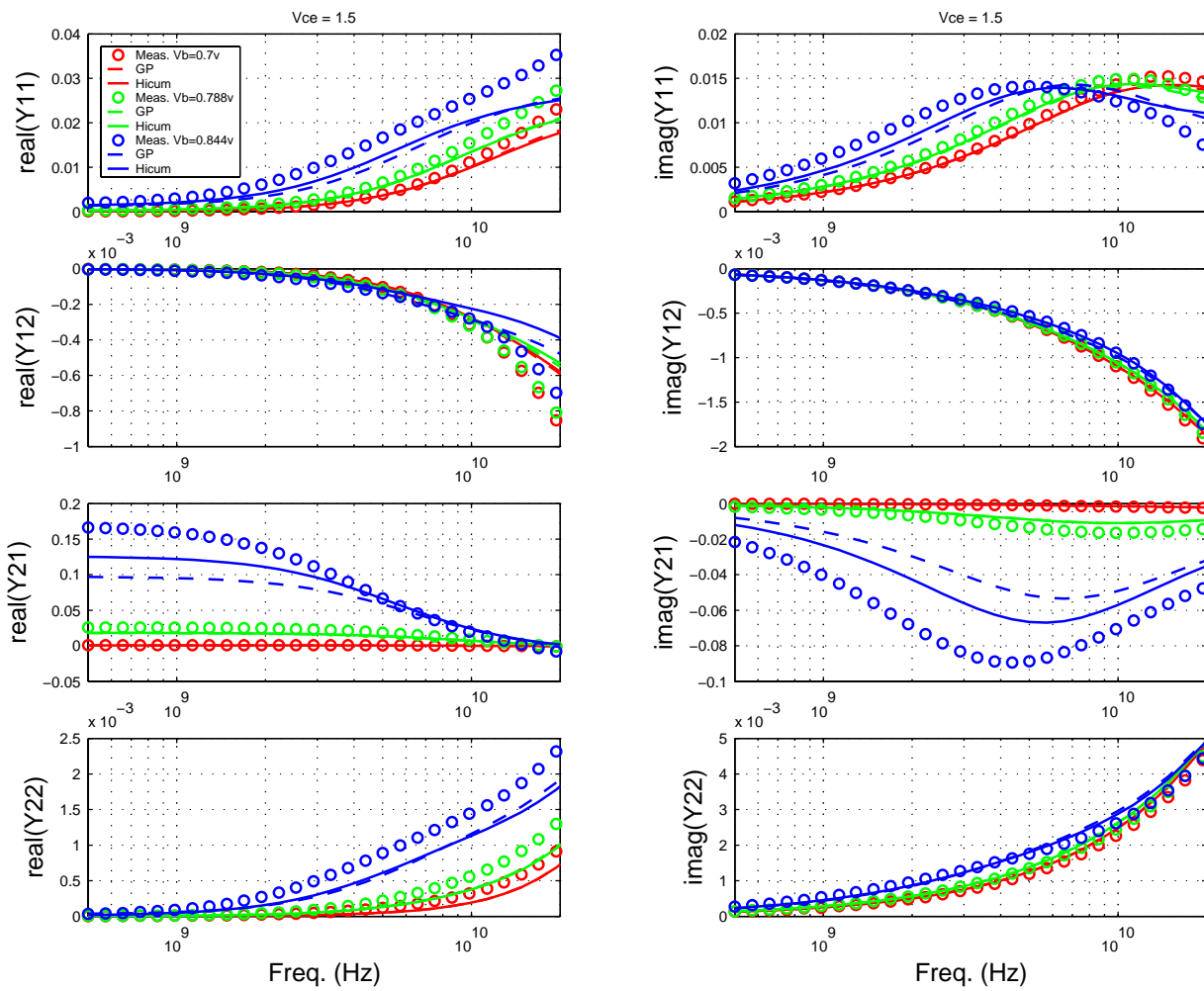


FIGURE 4.63 Gummel Plot: HV 0.96x10.0_452

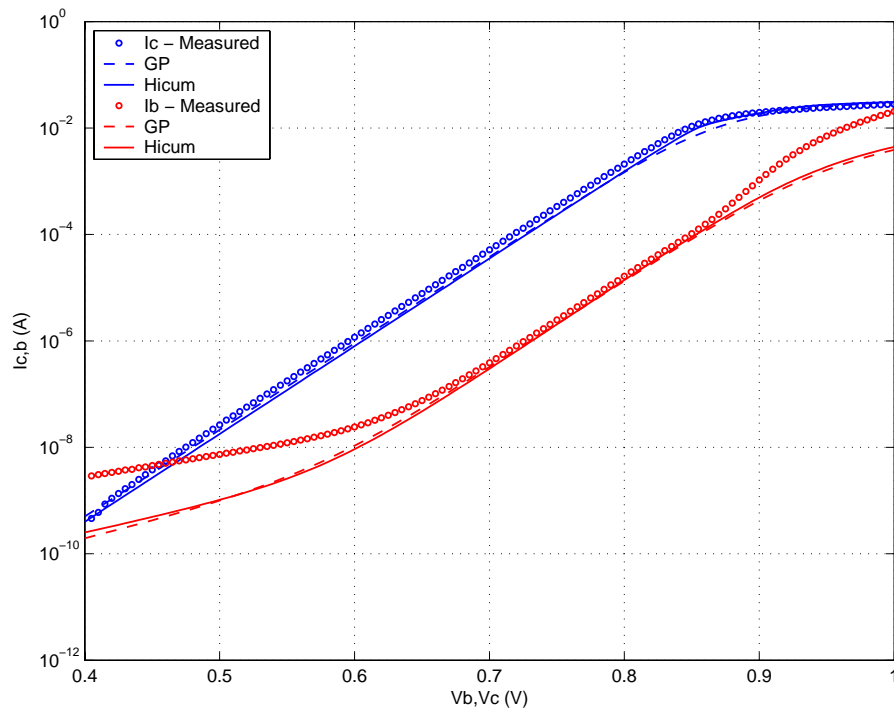
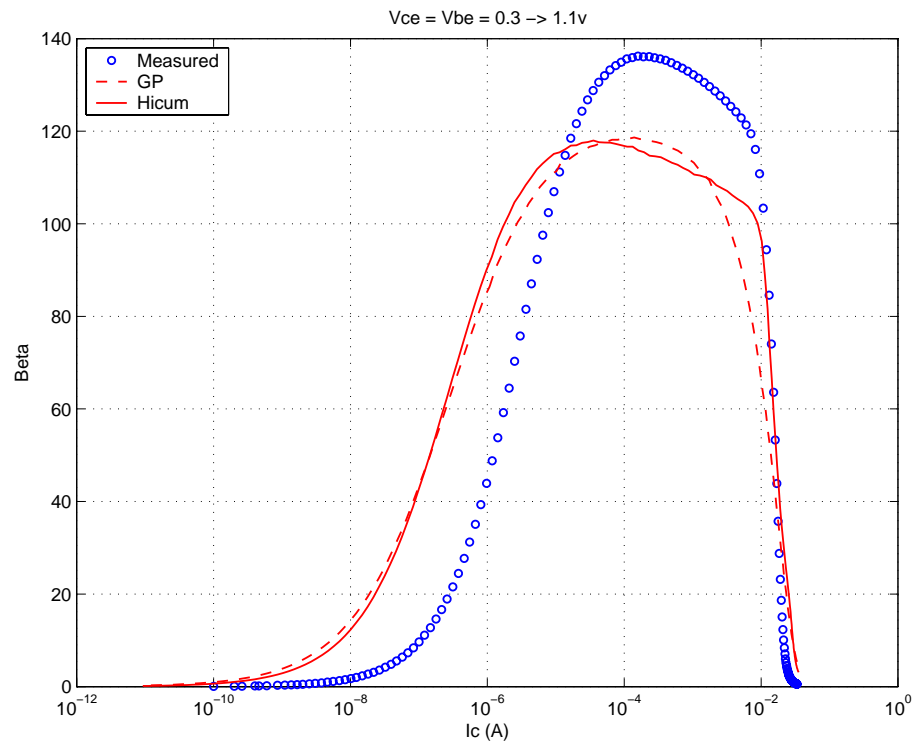
FIGURE 4.64 Beta vs. I_c : HV 0.96x10.0_452

FIGURE 4.65 IC vs. VCE at constant IB: HV 0.96x10.0_452

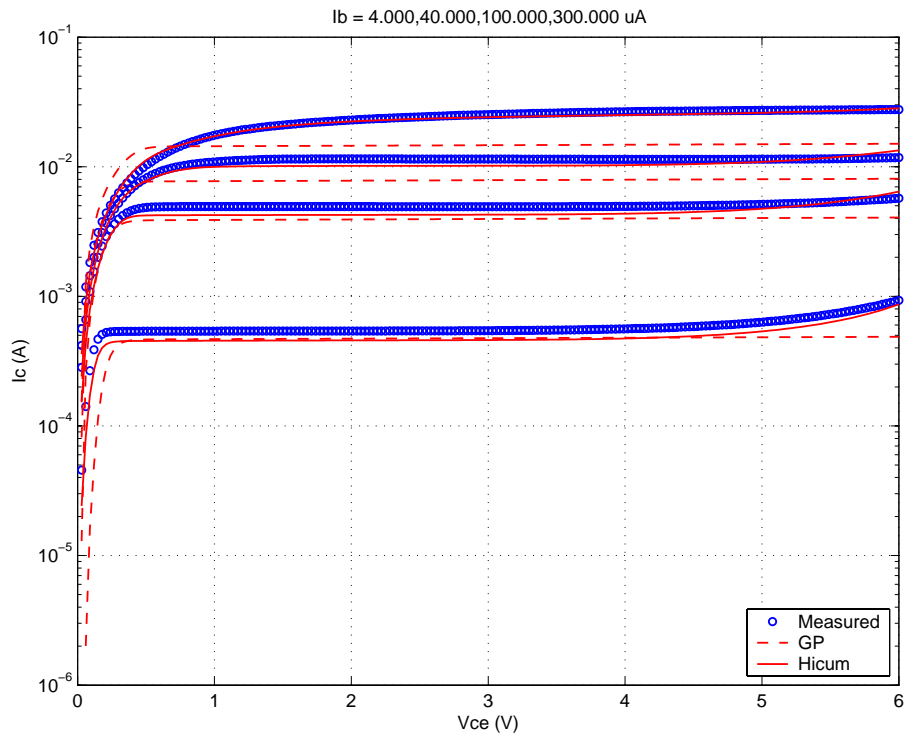


FIGURE 4.66 FT vs. IC: HV 0.96x10.0_452

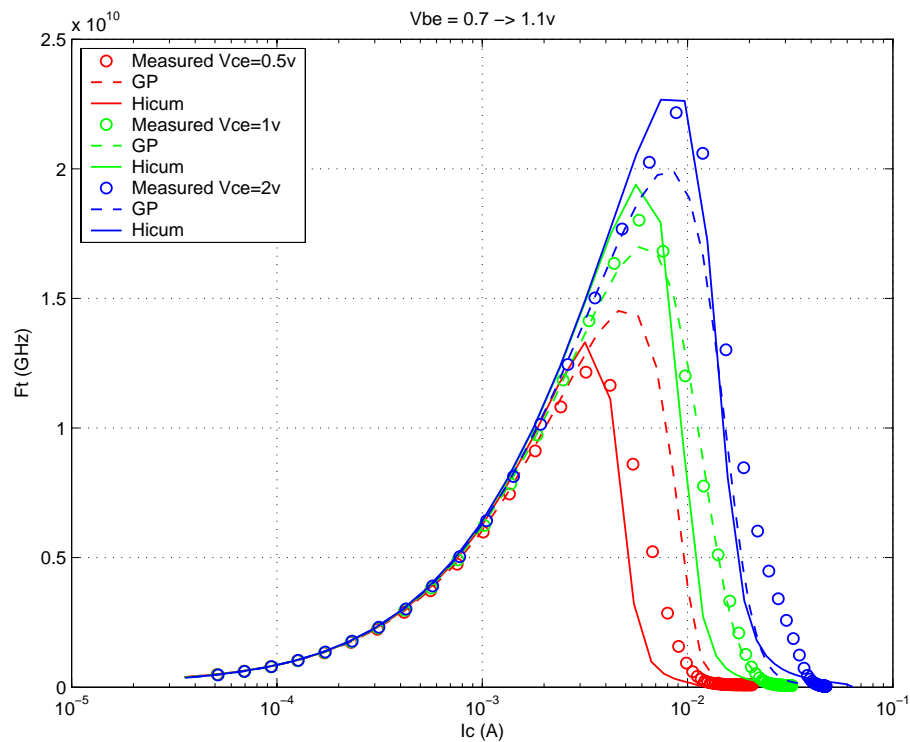
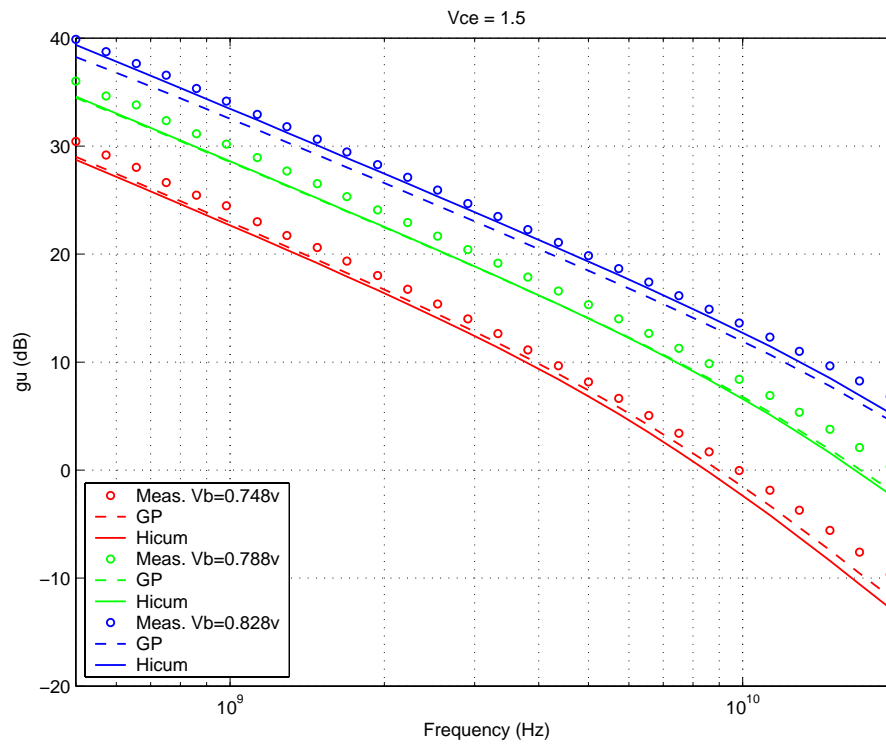
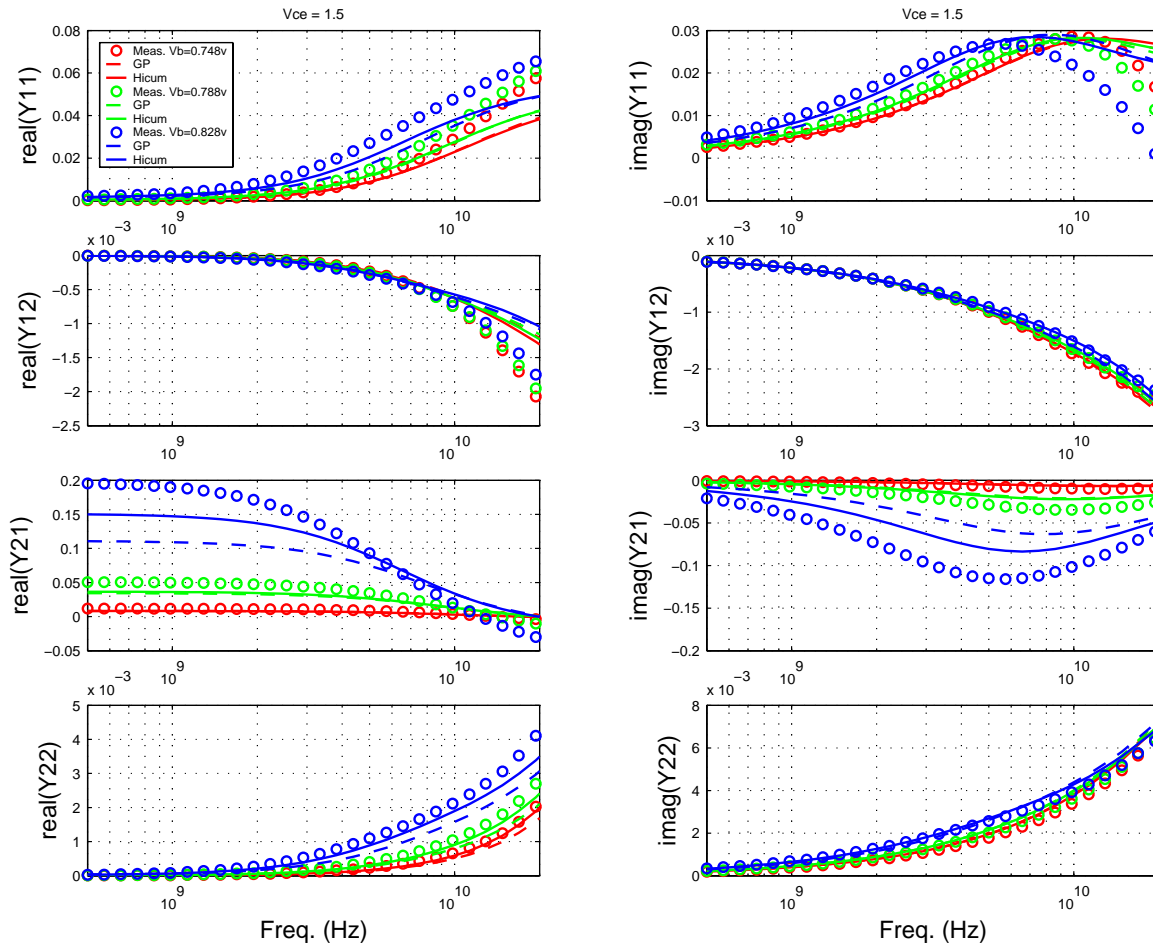


FIGURE 4.67 Power Gain vs. Freq: HV 0.96x10.0_452



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FIGURE 4.68 Y-parameters vs. FREQ: HV 0.96x10.0_452



4.5 NPN Statistical and Corner Models

4.5.1 Statistical Model

A detailed description of the Backward Propagation of Variance (BPV) approach to statistical model generation is given Section 2.6 on page 51 of the MOSFET chapter. Only additional information exclusive to the NPN statistical models is given here. Unlike MOSFET models, the map between process and geometry parameters into model parameters is not well defined for NPN models. Mappings between process parameters, model parameters, and geometry parameters must be developed. The stand alone NPN models (Gummel-Poon, VBIC, Hicum, etc.) do not provide the physical correlation of the model parameters. Thus, a set of independent process parameters, rather than model parameters, are defined as the fundamental statistical variables in the simulator. Mappings for the process and geometry parameters into model parameters are developed based on device physics. A handful of process parameter variances are forward propagated in the BPV infrastructure based on expected variances at the process level such as Emitter-Poly CD variations. The remaining process parameter variances are directly BPV'd based on the variances in the ESPECs. A well conditioned system physically and mathematically results, guaranteeing precise simulation of the ESPEC variances and reasonable and consistent statistical simulation of non ESPEC quantities such as base resistance. The process parameters, the propagation technique, the affected model parameters, and target ESPECs for the Spice Gummel-Poon model (SGPM) are listed in Table 4.3. The affected model parameters in HICUM model are directly correlated with those in SGPM. The statistically simulated ESPECs are listed in Table 4.5. Refer to Section 2.5.3 on page 54 for statistical model usage guidelines.

TABLE 4.3 The Process Variables and the Affected Model Parameters in SGPM.

Process Parameters	BPV or FPV	Affected Model Parameters	Target ESPEC for BPV	Mismatch
Emitter Window CD	FPV	RE, RB, RBX, RC, CEOX, CJE, CJC, IS, ISE, BF (GP), IBEIS (Hicum)	NA	IC, BETA
Emitter Poly CD	FPV	CEOX, RBX	NA	
Base Ge doping concentration	BPV	IS (GP), C10 (Hicum)	Vbe at mod. Ic	
Base Boron doping concentration	BPV	CBE, RBI, RBX, IS (GP), C10 (Hicum)	Cbe	
Emitter Si/Poly interface property	BPV	BF (GP), IBEIS (Hicum), RE	Peak Beta	IB
Emitter/Base Junction Leakage	BPV	ISE (GP), IREIS (Hicum)	Beta @ low Vbe	IB @ low Vbe
Emitter doping concentration	BPV	RE, BF (GP), IBEIS (Hicum)	Ic @ Vbe=1.1v	
Substrate doping concentration	BPV	CJS	Ccs	
Base width	BPV	RBI, TF (GP), T0 (Hicum)	Ft of HS, Std. dev.	
Collector Epi thickness	BPV	RCI, TF (GP), T0 (Hicum)	Ft of HV dev.	
Local Collector Implant (HV dev.)	BPV	CJC of HV dev.	CBC of HV dev.	
Local Collector Implant (Std. dev.)	BPV	CJC of Std. dev.	CBC of Std. dev.	
Nwell Implant (HS dev.)	BPV	CJC of HS dev.	CBC of HS dev.	

4.5.2 Centering

Refer to section 2.6.1 for centering within the BPV framework. The NPN model is extracted from a golden die which measures very close to the nominal of the ESPECs. As a result, the model parameter variation needed to exactly align the model to the nominal ESPECs is small. The simulated NOM ESPECs are listed in Table 4.6.

4.5.3 Corner Models

The goal of the corner models are to capture the device electrical performance limits through appropriate variation of the process parameters. Slow and fast corners are provided. Details of the corner models are given in Table 4.4. All the NPN ESPEC limits can not be captured with 2 corners. The target ESPEC parameters for the corner models are I_C , β , and F_t . The C_{BC} and C_{CS} ESPECs are also aligned to the ESPECs in the corner model. C_{BE} variation in the corner models is reduced from the ESPEC limit in order to retain consistent and physical F_t prediction. The verification of the simulated corner ESPECs are listed in Table 4.6.

TABLE 4.4 Corner model specifications

	FAST	SLOW
Emitter resistance	Component 1 is higher due to lower I_b (high β); Component 2 is lower due to higher emitter doping. Net is ~10% lower	Component 1 is lower due to higher I_b (low β); Component 2 is higher due to lower emitter doping. Net is ~10% higher
Extrinsic base resistance	Component 1 is lower (Nom. - 1σ link dist.); Component 2 is higher due to lower base doping (low C_{be}). Net is ~6% higher	Component 1 is higher (Nom. + 1σ link dist.); Component 2 is lower due to higher base doping (high C_{be}). Net is ~6% lower
Intrinsic base resistance	Component 1 is higher due to shorter base width; Component 2 is higher due to lower base doping (low C_{be}). Net is 10% higher	Component 1 is lower due to longer base width; Component 2 is lower due to higher base doping (high C_{be}). Net is 10% lower
Base emitter junction cap.	95% of NOM case	105% of NOM case
Base collector junction cap.	Max. case of C_{bc}	Min. case of C_{bc}
Collector substrate junction cap.	Min. case of C_{cs}	Max. case of C_{cs}
Intrinsic collector resistance	~20% lower; aligned to higher collector doping (higher C_{bc})	~20% higher; aligned to lower collector doping (lower C_{bc})
Collector saturation current	Min. case of V_{be} for fixed and moderate I_c	Max. case of V_{be} for fixed and moderate I_c
Base current	Max. case of β (lower I_b)	Min. case of β (higher I_b)
Base width	Smaller; aligned to max. F_t E-spec.	Larger; aligned to min. F_t E-spec.

TABLE 4.5 E-spec. vs. Model (Long transistor - 0.28x10µm emitter with 122 configuration)

Device	Espec Name (unit)	Slow			Nom			Fast		
		Espec	Corner	Stat	Espec	Corner	Stat	Espec	Corner	Stat
Low Voltage NPN Gummel-Poon (ln122)	beta ¹	50.00	49.96	46.10	100.00	100.50	101.00	150.00	183.90	156.00
	cbc ² (fF)	22.70	24.20	23.10	25.40	25.41	25.50	28.10	27.00	27.90
	cbe ³ (fF)	30.90	28.90	31.10	27.30	27.25	27.30	23.70	25.20	23.60
	ccs (fF)	22.10	22.08	21.80	18.60	18.65	18.40	15.10	15.11	14.90
	ft (GHz)	82.00	76.02	78.40	91.00	86.76	86.60	100.00	96.54	94.80
	ic (uA)	0.95	1.10	1.12	1.90	2.02	2.00	2.85	2.85	2.88
	Jc ⁴ (Pk. Ft)		2.55		3.32	2.75			3.49	
	fmax ⁵ (GHz)		72.53	68.40	70.00	73.13	73.10		72.15	77.80
	bvceo ⁶ (V)	2.80	100.00	100.00	2.40	100.00	100.00	2.00	100.00	100.00
Low Volt. Hicum (ln122_hicum)	beta ¹	50.00	48.95	46.30	100.00	99.57	100.00	150.00	181.10	154.00
	cbc ² (fF)	22.70	23.24	23.40	25.40	25.41	25.50	28.10	26.83	27.60
	cbe ³ (fF)	30.90	29.40	31.10	27.30	27.25	27.30	23.70	25.20	23.60
	ccs (fF)	22.10	22.08	21.80	18.60	18.65	18.40	15.10	15.11	14.90
	ft (GHz)	82.00	81.32	81.40	91.00	90.53	90.20	100.00	99.69	99.00
	ic (uA)	0.95	0.98	1.03	1.90	1.93	1.91	2.85	2.88	2.79
	Jc ⁴ (Pk. Ft)		2.92		3.32	3.33			3.81	
	fmax ⁵ (GHz)		76.10	83.10	70.00	70.29	91.40		66.27	99.70
	bvceo ⁶ (V)	2.80	3.04	2.75	2.40	2.38	2.38	2.00	1.99	2.01
Medium Volt-age NPN Gummel-Poon (mn122)	beta ¹	50.00	50.06	47.40	100.00	100.80	102.00	150.00	187.90	157.00
	cbc ² (fF)	12.70	13.90	12.80	14.40	14.39	14.30	16.10	15.20	15.80
	cbe ³ (fF)	30.90	28.40	30.60	27.30	27.25	27.30	23.70	25.70	24.00
	ccs (fF)	22.10	22.08	21.80	18.60	18.65	18.40	15.10	15.11	14.90
	ft (GHz)	60.00	53.52	56.00	67.00	63.26	63.00	74.00	70.77	70.00
	ic (uA)	0.95	1.10	1.12	1.90	2.02	2.00	2.85	2.85	2.88
	Jc ⁴ (Pk. Ft)		1.10		1.29	1.37		1.41	1.42	
	fmax ⁵ (GHz)		104.00	103.00	123.00	109.20		135.00	110.10	115.00
	bvceo ⁶ (V)	4.20	100.00	100.00	3.60	100.00	100.00	3.00	100.00	100.00
Medium Volt-age NPN Hicum (mn122_hicum)	beta ¹	50.00	49.07	46.60	100.00	99.92	100.00	150.00	183.90	153.00
	cbc ² (fF)	12.70	13.70	13.80	14.40	14.39	14.40	16.10	15.09	15.00
	cbe ³ (fF)	30.90	28.90	30.60	27.30	27.25	27.30	23.70	25.70	24.00
	ccs (fF)	22.10	22.08	21.80	18.60	18.65	18.40	15.10	15.11	14.90
	ft (GHz)	60.00	59.55	60.00	67.00	67.35	67.20	74.00	74.57	74.40
	ic (uA)	0.95	1.00	1.03	1.90	1.93	1.91	2.85	2.87	2.79
	Jc ⁴ (Pk. Ft)		1.26		1.29	1.30		1.41	1.41	
	fmax ⁵ (GHz)		124.70	143.00	123.00	123.30		135.00	121.60	161.00
	bvceo ⁶ (V)	4.20	4.47	4.14	3.60	3.61	3.62	3.00	2.99	3.10

TABLE 4.5 E-spec. vs. Model (Long transistor - 0.28x10 μ m emitter with 122 configuration)

High Voltage NPN Gummel-Poon (hn122)	beta ¹	50.00	47.06	46.20	100.00	100.60	102.00	150.00	188.40	158.00
	cbc ² (fF)	9.15	9.60	9.37	10.40	10.42	10.40	11.65	11.20	11.40
	cbe ³ (fF)	30.90	28.20	30.60	27.30	27.25	27.30	23.70	26.40	24.00
	ccs (fF)	22.10	22.08	21.80	18.60	18.65	18.40	15.10	15.11	14.90
	ft (GHz)	33.00	31.57	30.60	36.50	34.37	34.00	40.00	38.89	37.40
	ic (uA)	1.60	0.98	1.12	3.20	2.02	2.00	4.80	2.85	2.88
	Jc ⁴ (Pk. Ft)	0.61	0.54	0.00	0.68	0.57	0.00	0.75	0.57	0.00
	fmax ⁵ (GHz)	117.00	88.29	87.10	130.00	89.26	91.60	143.00	93.26	96.10
	bvceo ⁶ (V)	8.40	100.00	100.00	6.70	100.00	100.00	5.00	100.00	100.00
High Voltage NPN Hicup (hn122_hicup)	beta ¹	50.00	48.25	45.50	100.00	99.14	99.80	150.00	184.20	154.00
	cbc ² (fF)	9.15	9.86	9.29	10.40	10.42	10.40	11.65	11.21	11.50
	cbe ³ (fF)	30.90	28.20	30.60	27.30	27.25	27.30	23.70	26.40	24.00
	ccs (fF)	22.10	22.08	21.80	18.60	18.65	18.40	15.10	15.11	14.90
	ft (GHz)	33.00	32.39	33.30	36.50	36.57	36.40	40.00	40.38	39.50
	ic (uA)	1.60	0.99	1.04	3.20	1.93	1.91	4.80	2.86	2.78
	Jc ⁴ (Pk. Ft)		0.53		0.68	0.70		0.74		
	fmax ⁵ (GHz)		99.12	127.00	130.00	104.50	135.00		106.60	143.00
	bvceo ⁶ (V)	8.40	8.45	8.36	6.70	6.72	6.82	5.00	5.31	5.28

Notes:

1. Beta: The E-spec is asymmetrical across the NOM case. The statistical model prediction is +/- 3 sigma and is thus symmetrical across NOM.
2. C_{bc}: Variation in the corner models is reduced from the E-spec limit in order to retain consistent and physical Ft prediction.
3. C_{be}: Variation in the corner models is reduced from the E-spec limit in order to retain consistent and physical Ft prediction.
4. J_c is the current density (mA/mm²) at peak Ft. Only nominal E-spec is specified. This parameter is not a BPV targeted E-spec for corner or statistical model extraction.
5. F_{max}: Only nominal E-spec. is specified. Corner and statistical model predictions are shown for all cases. This parameter is not a BPV targeted E-spec. for corner or statistical model extraction.
6. BV_{ceo}: Gummel-Poon model does not include breakdown effects. Hicup model predictions are shown. This parameter is not a BPV targeted E-spec. for corner or statistical model extraction.

4.6 NPN Mismatch Model

Mismatch characterization is not available. A preliminary model based on local variation of process parameters of the previous generation of NPN technologies is provided in the design kit. The spacing between npns in the mismatch structures was 10 μ m.

4.7 Released Model Quality Assurance (QA)

A rigorous QA procedure is executed before any new model release. The geometry dependence of 9 key device parameters is examined for any non-physical behavior for all 3 cases: Nominal, Fast, and Slow. These parameters are listed in Table 4.6.

TABLE 4.6 NPN electrical parameters list examined as part of model release QA

Parameter	Description
BETA	Current gain
I_C	IC at $V_{be}=0.7v$
F_t	Unity gain cut-off frequency
F_{max}	Unity power gain cut off frequency
C_{BE}	Base-Emitter capacitance
C_{BC}	Base-Collector capacitance
C_{CS}	Collector-Substrate capacitance
R_E	Emitter Resistance
R_B	Base Resistance

Figures 4.69 through 4.71 illustrate the emitter length dependence of these 9 parameters.

FIGURE 4.69 QA Plots: LV 0.28x10.0_122

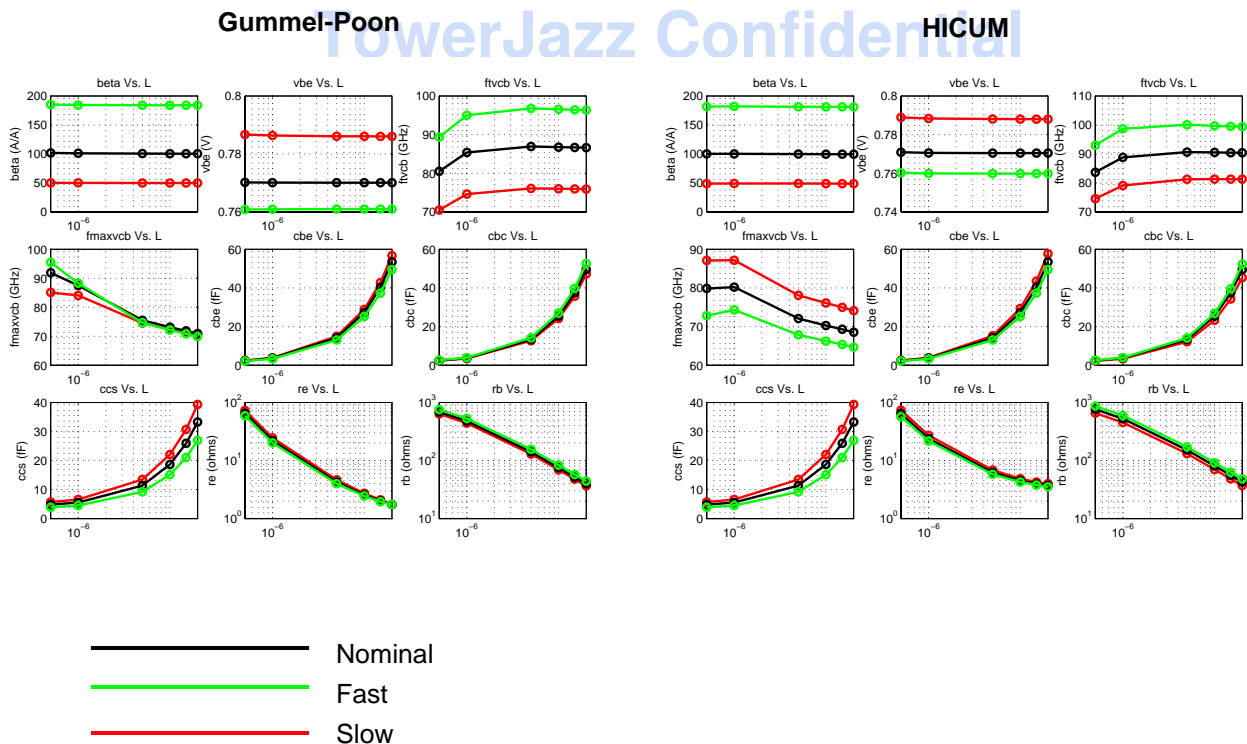


FIGURE 4.70 QA Plots: MV 0.28x10.0_122

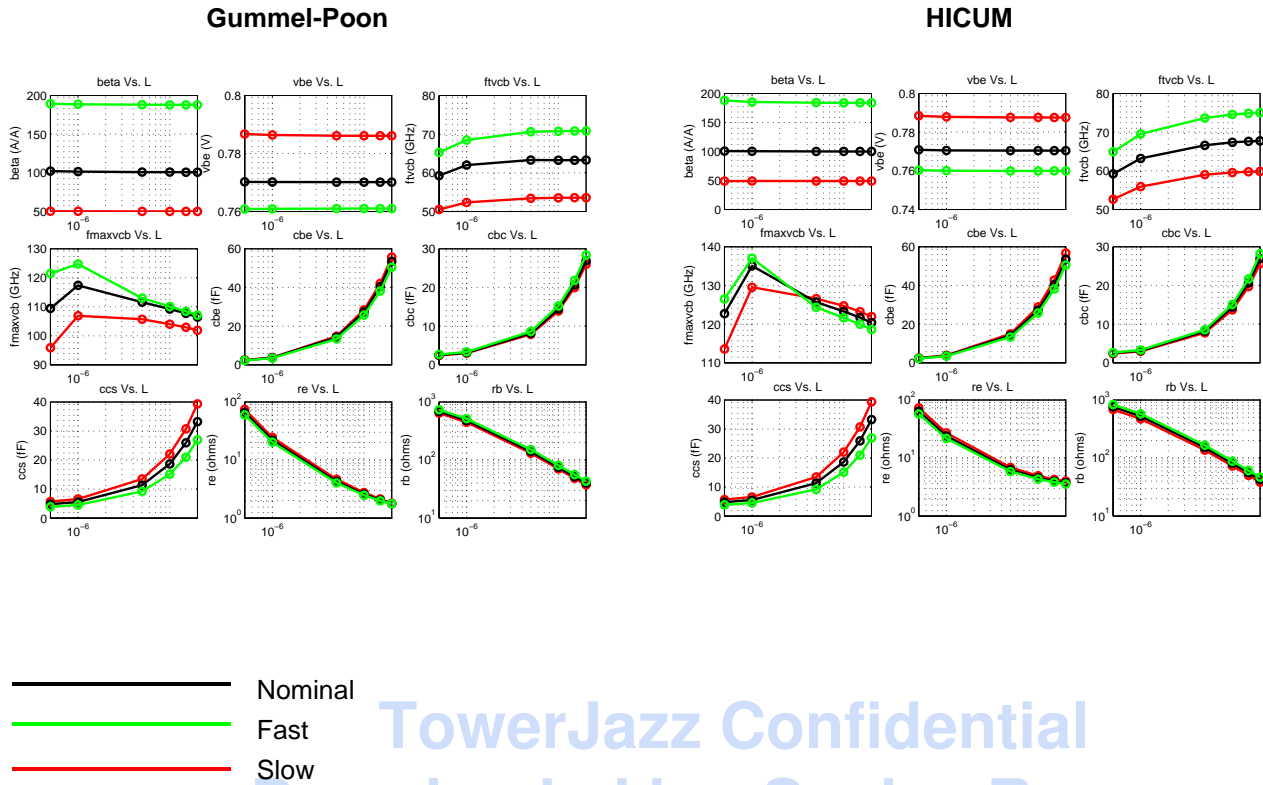
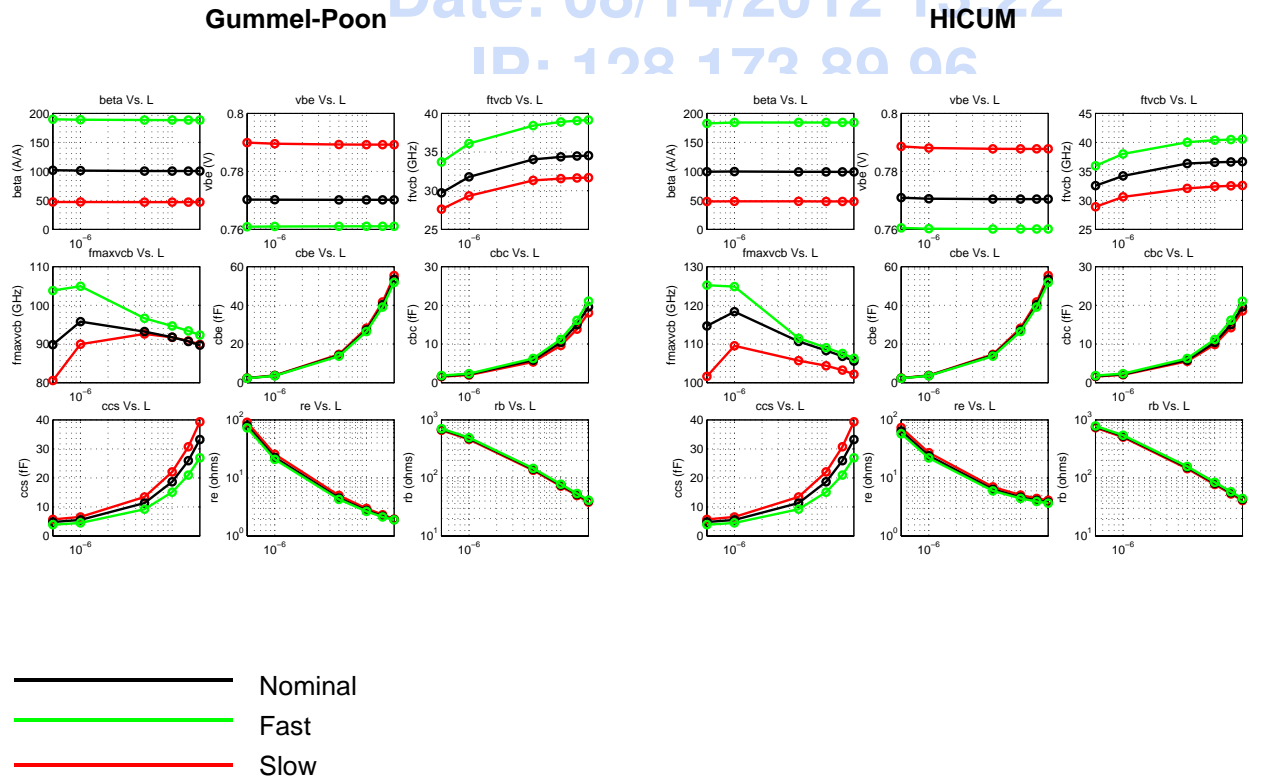


FIGURE 4.71 QA Plots: HV 0.28x10.0_122



4.8 Model Update History

TABLE 4.7 NPN model specific updates in model release version 1.7

v1.7 update	Devices	Reason	Impact on user
Added GP support Added 232, 342, 452 configurations Added ew=0.9 for HV devices	All	Provide increased flexibility	

4.8.1 v1.8

No changes

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5.0 SiGe 200GHz Bipolar Model

5.1 Device Description

The SBC13HA 200GHz process offers 2 NPN device types, low and medium voltage, differentiated by BV_{CEO} and F_t targets listed in Table 5.1. These devices are exclusive to SBC13HA and cannot coexist with the npn devices described in Chapter 4.0. A cross section of an NPN device is shown in Figure 5.1 where the differentiating factor between the device types is the collector implant. Figure 5.2 shows the layout of a 1 emitter, 2 base, 2 collector configuration. Layout configurations are further described in Section 5.2.

TABLE 5.1 SBC13HA NPN Specification by BV_{CEO} and F_t

NPN	BV_{CEO} (V)	F_t (GHz)
low voltage	1.9	200
medium voltage	3.2	75

FIGURE 5.1 Cross Section of NPN

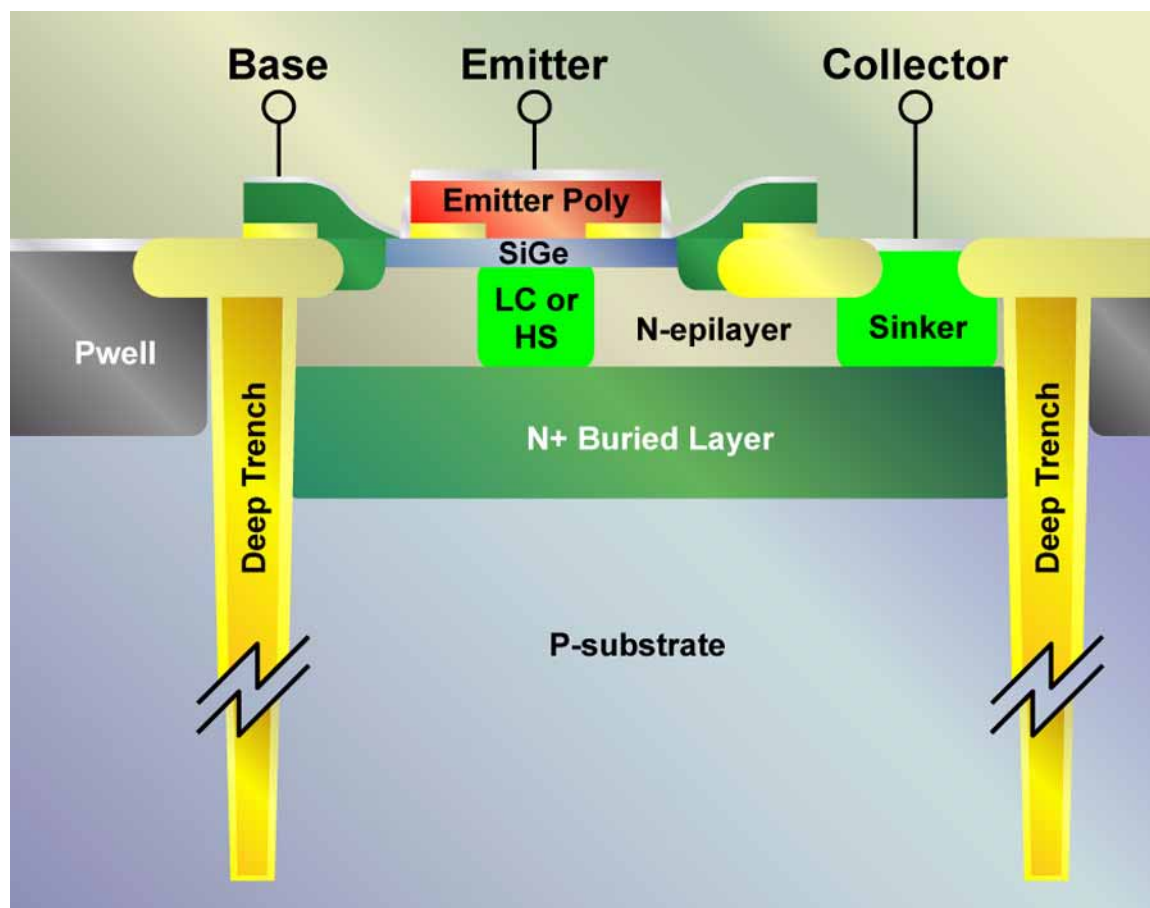
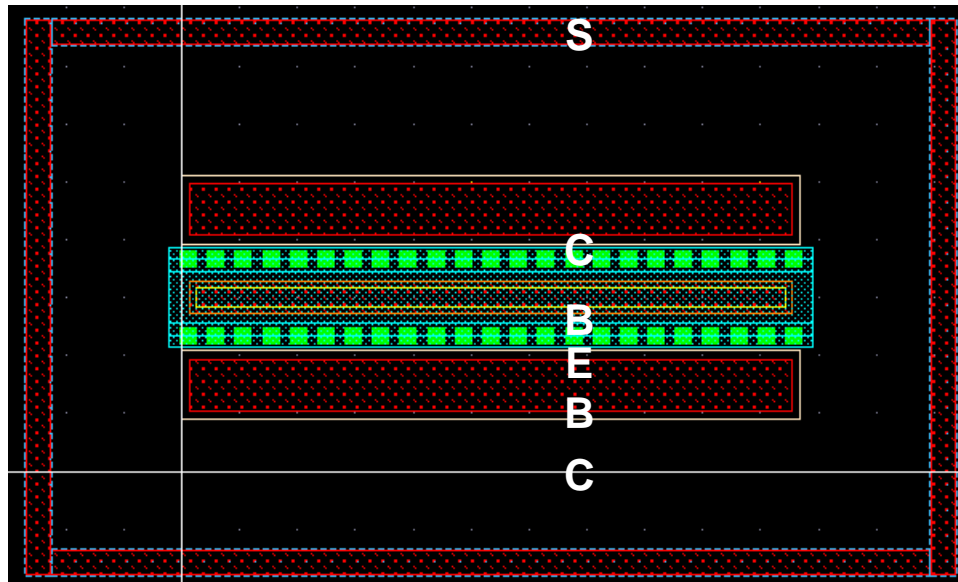


FIGURE 5.2 Layout of NPN: 1 Emitter, 2 Base, and 2 Collector configuration



5.2 Available NPN Configurations and Usage Guidelines

Table 5.2 provides a detailed description of the NPN configurations and parameter ranges.

Emitters Lengths: Scalable, see Table 5.2 for length range.

Emitters Widths: A single emitter width ($0.15\mu\text{m}$) is offered in the SBC13HA technology.

Multiple device instances vs. multiple emitter fingers: use of multiple emitter fingers instead of multiple device instances generally results in more efficient footprint and lower parasitic capacitance. The trade-off is collector resistance.

TABLE 5.2 SiGe200 NPN Configurations

Configuration	Device Type: l=low voltage m=medium voltage	Emitter Width n= $0.28\mu\text{m}$	Emitter Length (μm)	No. of Emitters	No. of Bases	No. of Collectors
121	l, m	n	0.76-20.0	1	2	1
122	l, m	n	0.76-20.0	1	2	2
232	l, m	n	2.84-20.0	2	3	2

5.3 Model Description

5.3.1 L-Scalable Model

The emitter length can be varied within the grid spacing and within the boundaries listed in Table 5.2. Separate models are extracted for the various combinations of emitter width and finger configuration described in Table 5.2.

5.3.2 HICUM Model

The HICUM model was introduced to overcome the shortcomings of the SGPM (Standard Gummel-Poon Model). The name of HICUM is derived from “High Current Model”. HICUM was initially developed with special emphasis on the modeling of the high current region, very important for many high-speed applications. Compared with SGPM, HICUM is based on an extended and generalized integral charge control relationship, and approaches the transistor dynamic behaviors in a more physical way. For more detailed information about HICUM, please refer to HICUM official web page (http://www.iee.et.tu-dresden.de/iee/eb/hic_new/hic_start.html).

5.4 Model Extraction and Verification

Scalable NPN models are extracted based on DC, CV, and RF measurements over a wide geometry and bias range.

Figures 5.3 through 5.44 display the characterization plots for the low voltage NPN. Figures 5.45 through 5.86 display the characterization plots for the medium voltage NPN. Multiple devices in parallel are characterized for smaller emitter lengths to reduce de-embedding errors. The device type and size are encoded in the figure caption as “Voltage LxWxM_Configuration.” Thus a MV 0.15x1x10_122 captions refers to a medium voltage NPN with a width (W) of 0.15 μ m, a length (L) of 1 μ m, with 10 devices in parallel (M) and a 122 emitter/base/collector finger configuration.

5.4.1 Low Voltage Verification Plots

FIGURE 5.3 Gummel Plot LV 0.15x10.16x1_122

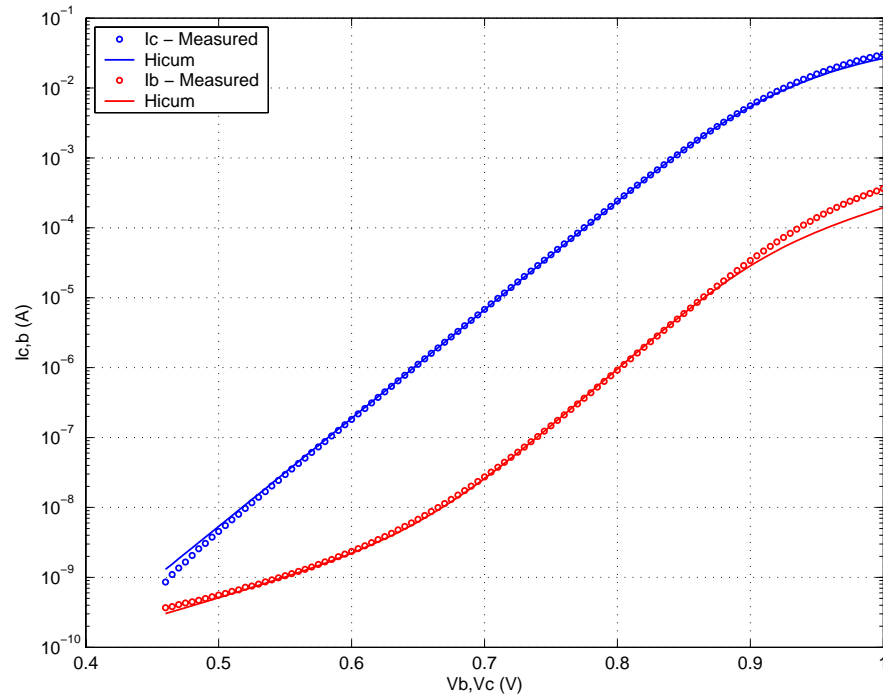


FIGURE 5.4 Beta vs. I_c : LV 0.15x10.16x1_122

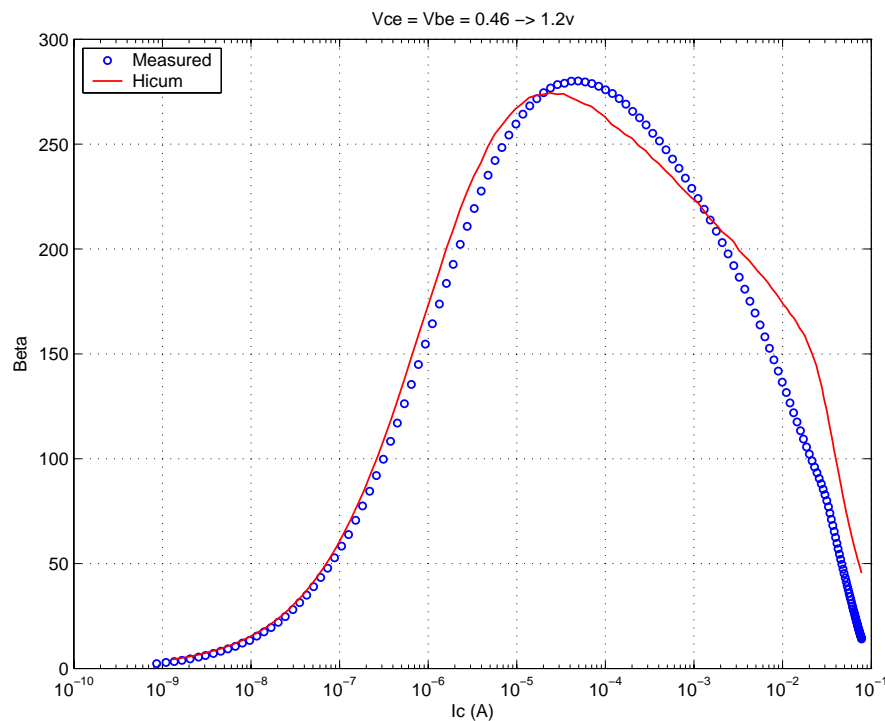


FIGURE 5.5 I_C vs. V_{CE} at constant I_B : LV 0.15x10.16x1_122

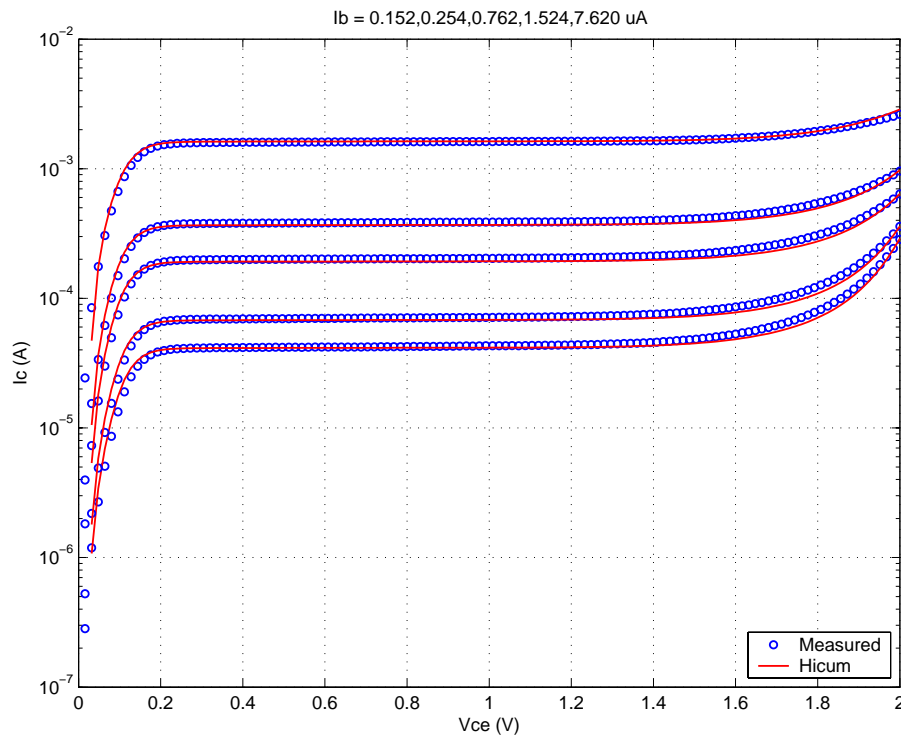


FIGURE 5.6 f_T vs. I_C : LV 0.15x10.16x1_122

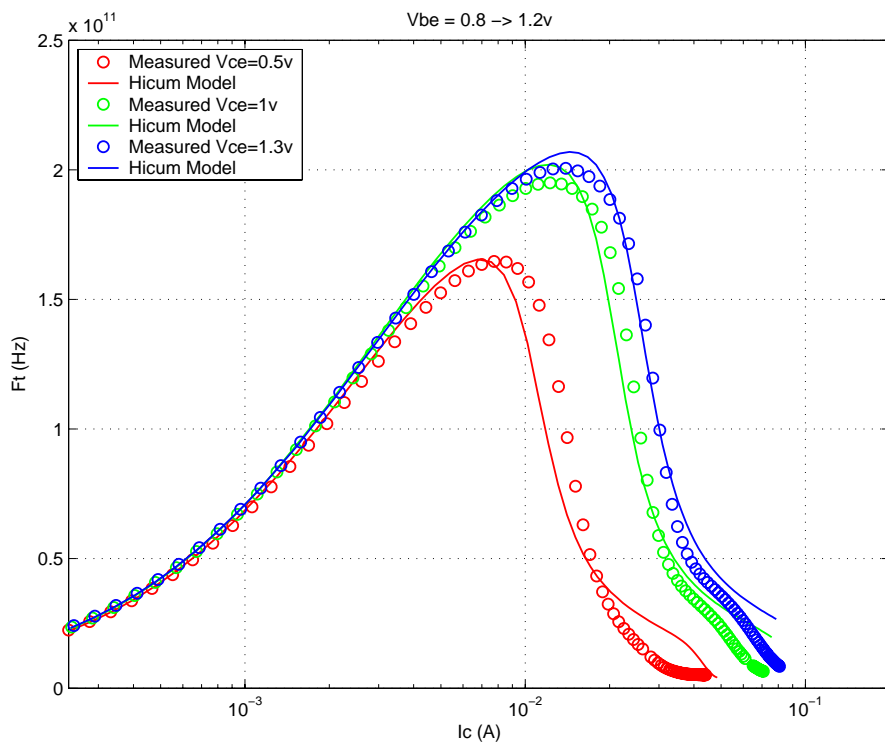
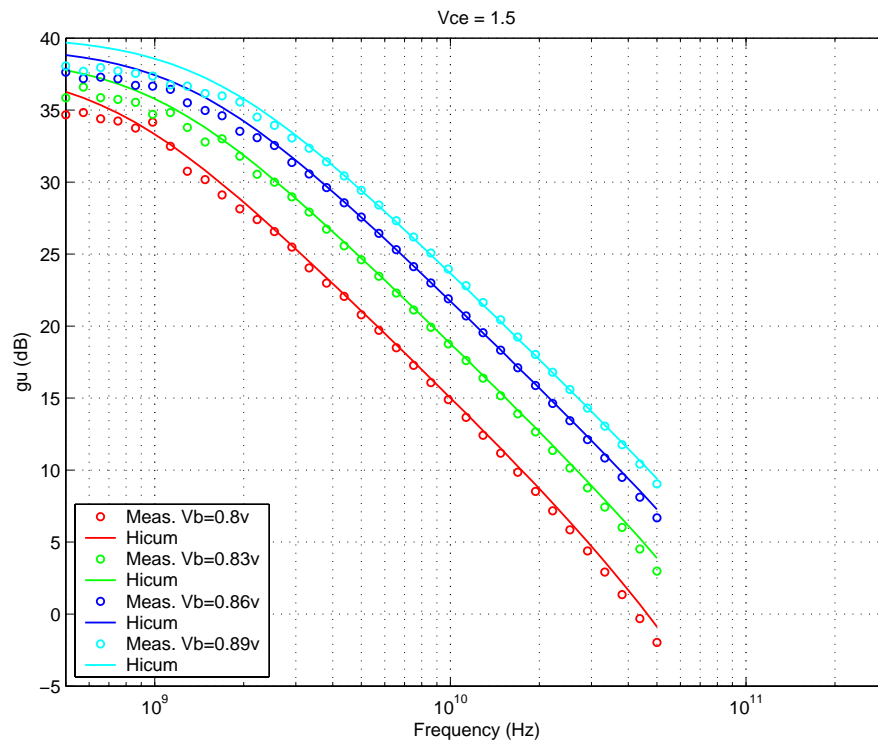


FIGURE 5.7 Power Gain vs. Freq: LV 0.15x10.16x1_122



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FIGURE 5.8 Y-parameters vs. FREQ: LV 0.15x10.16x1_122

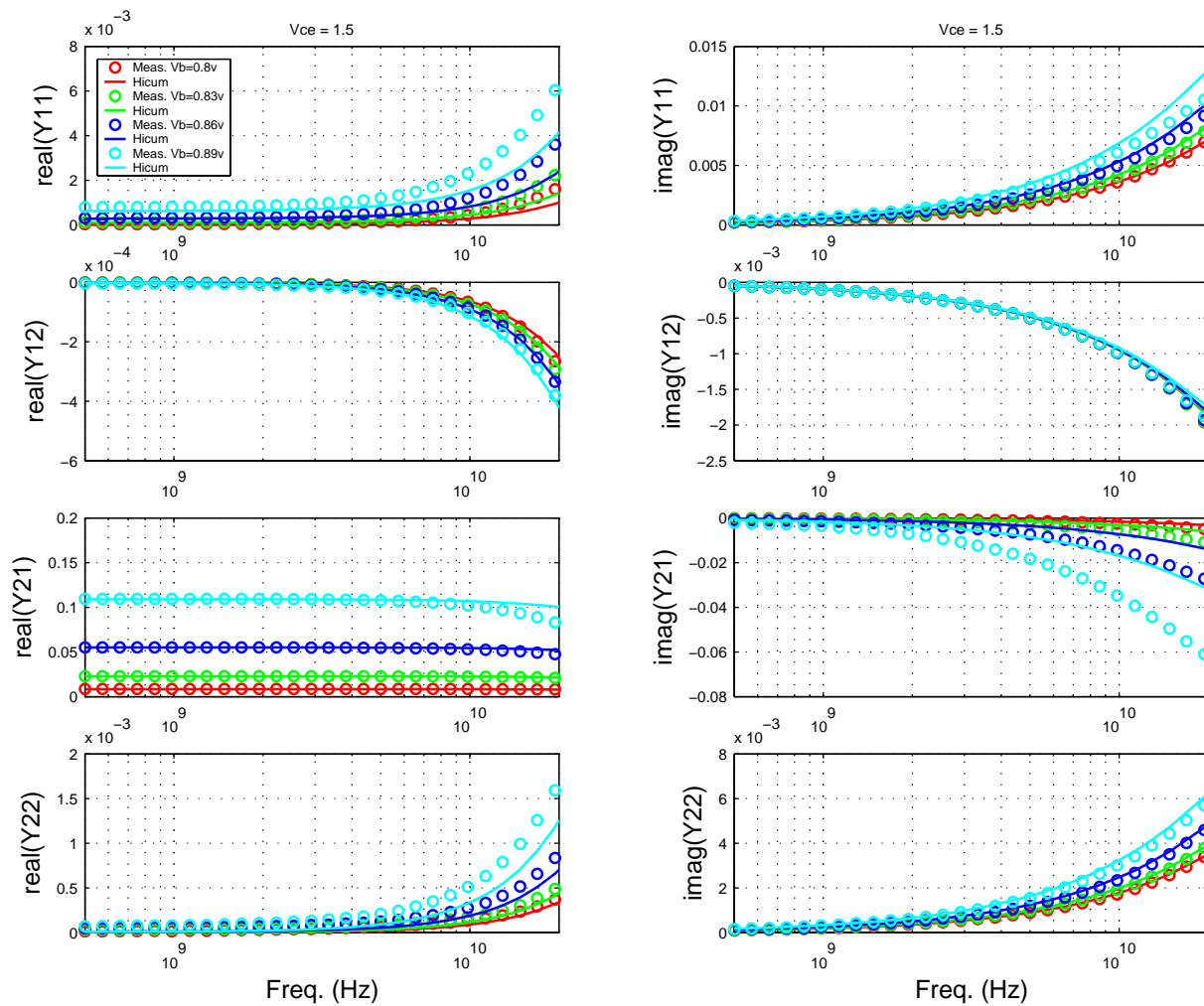


FIGURE 5.9 Gummel Plot LV 0.15x4.52x1_122

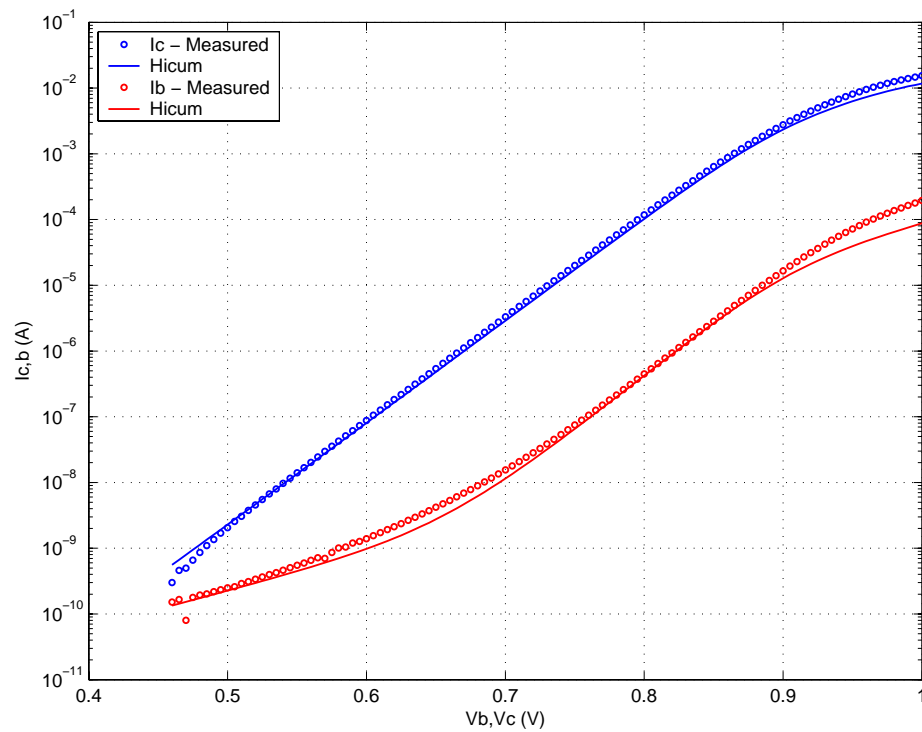
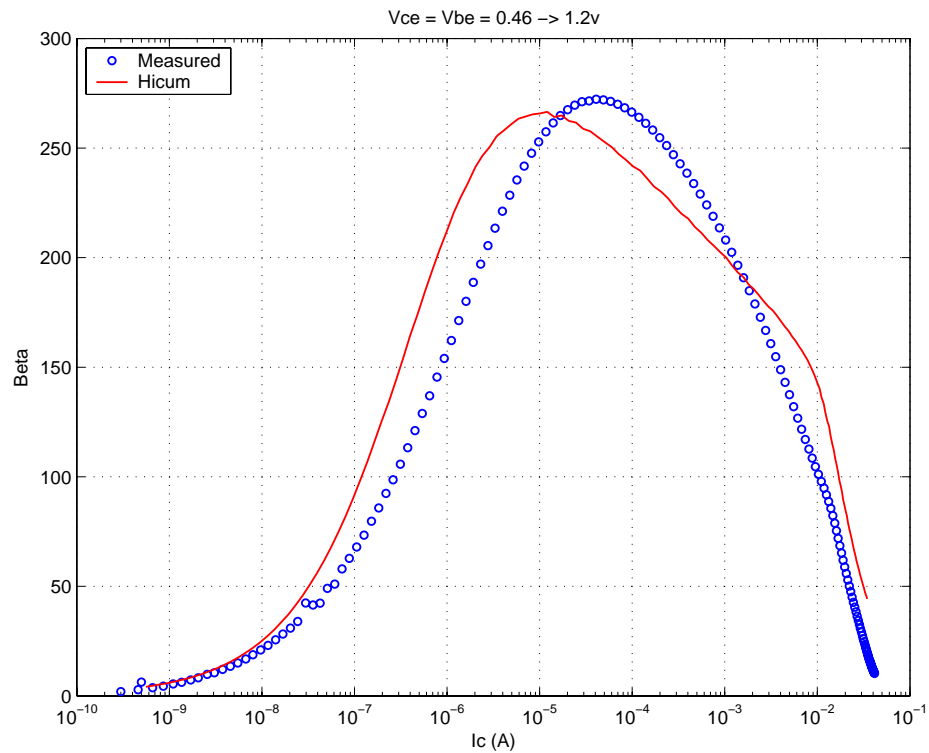
FIGURE 5.10 Beta vs. I_C : LV 0.15x4.52x1_122

FIGURE 5.11 IC vs. VCE at constant IB: LV 0.15x4.52x1_122

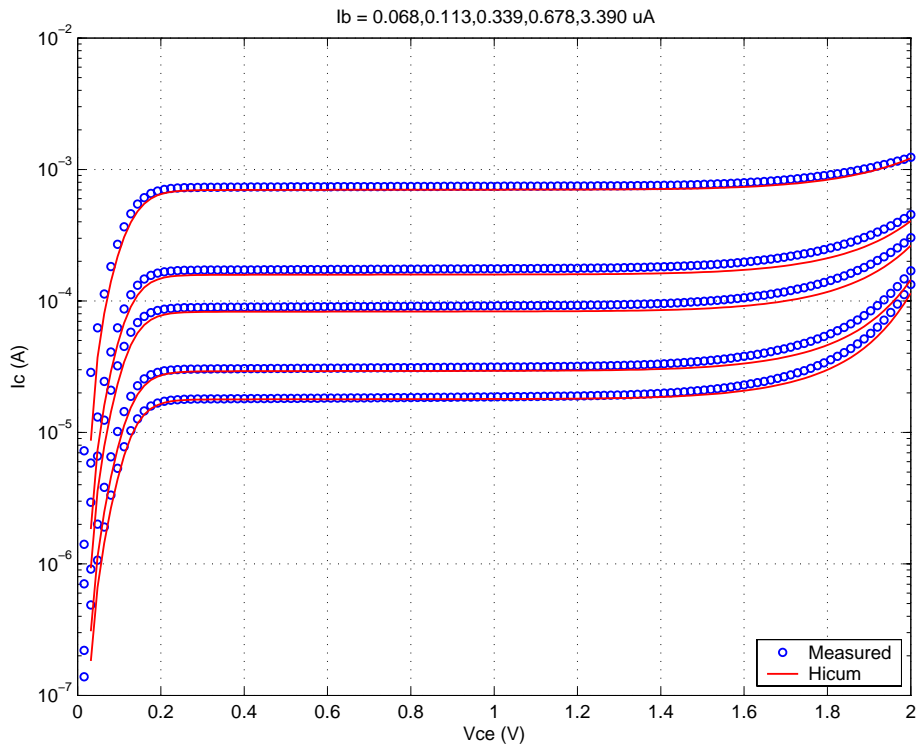


FIGURE 5.12 FT vs. IC: LV 0.15x4.52x1_122

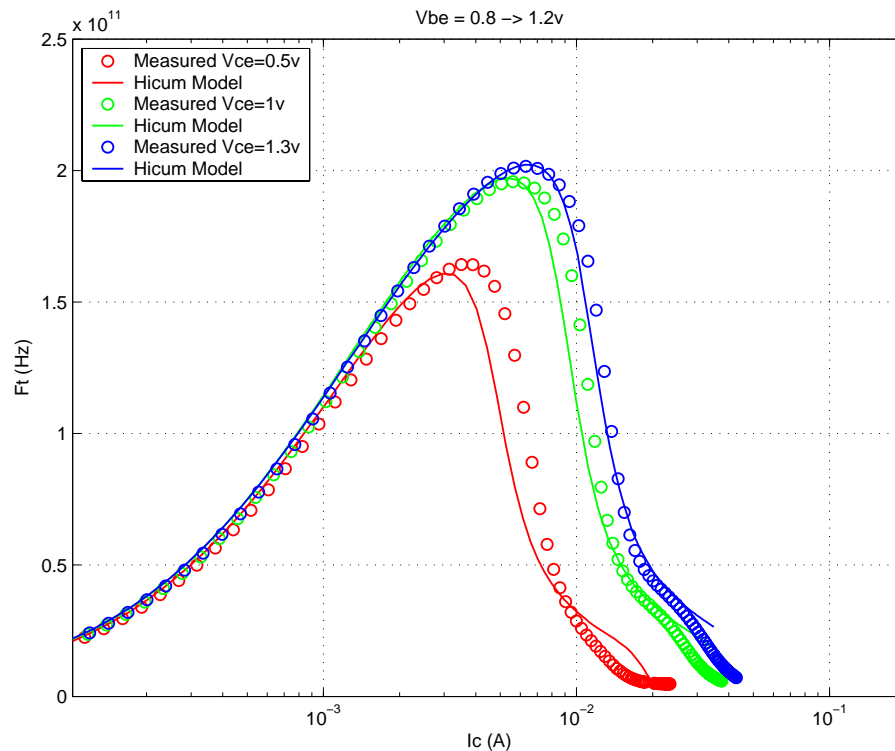
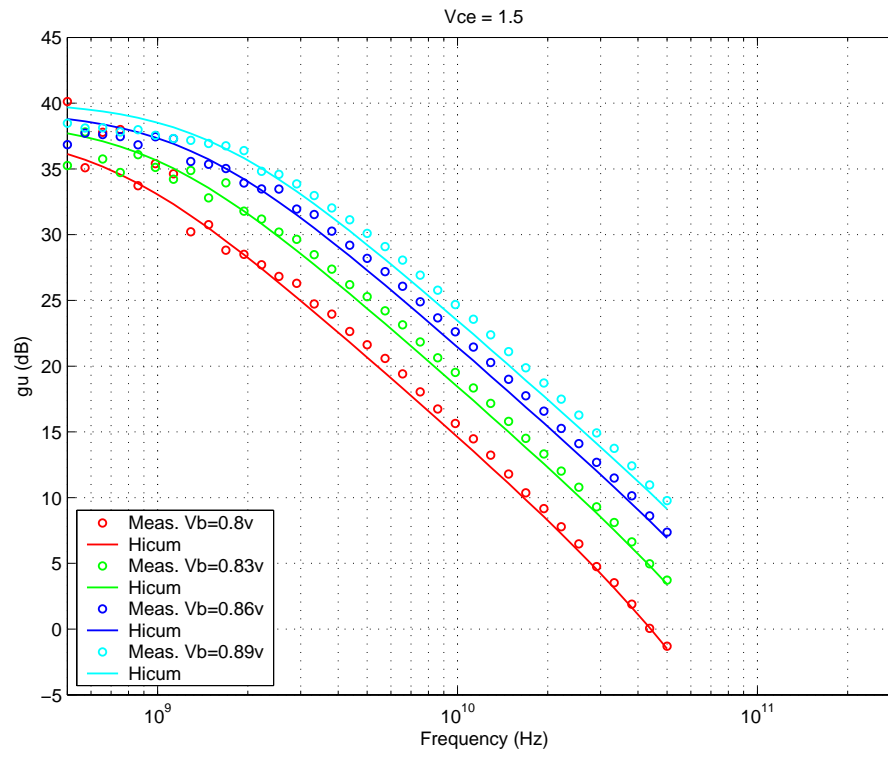


FIGURE 5.13 Power Gain vs. Freq: LV 0.15x4.52x1_122



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FIGURE 5.14 Y-parameters vs. FREQ: LV 0.15x4.52x1_122

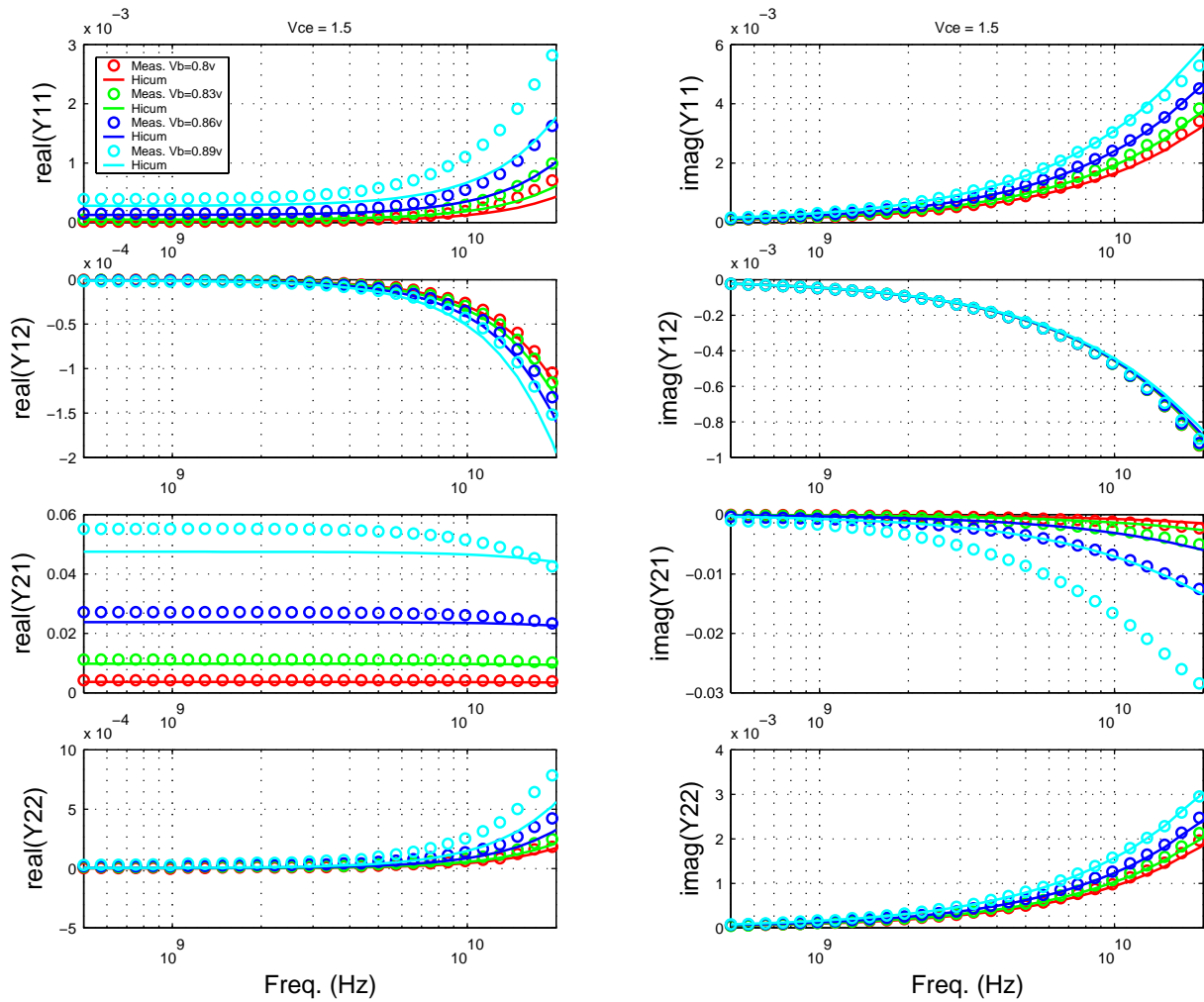


FIGURE 5.15 Gummel Plot: LV 0.15x0.76x10_122

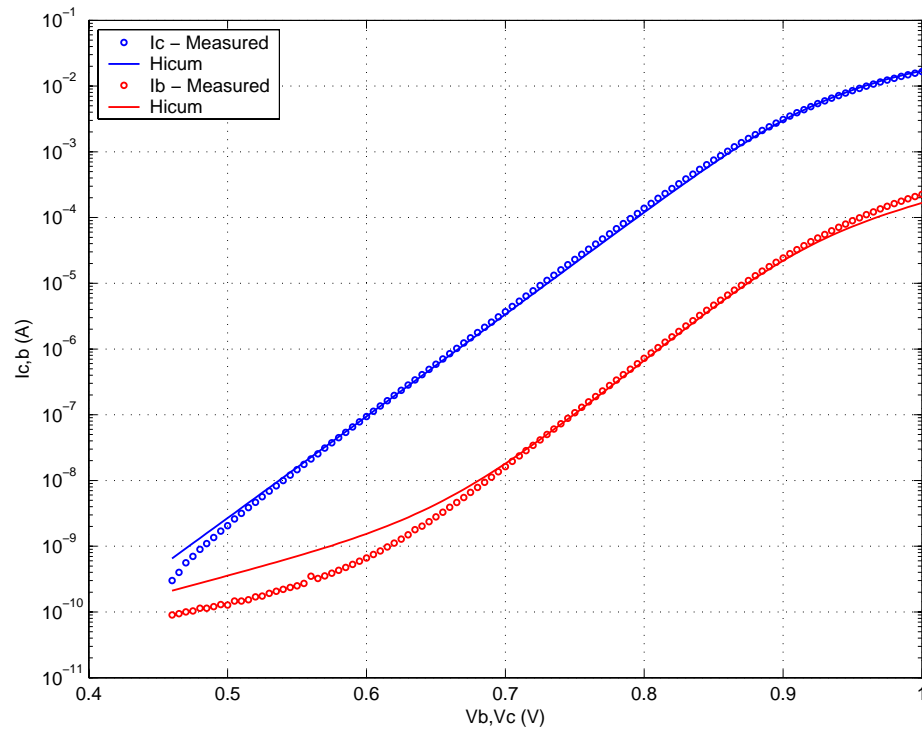
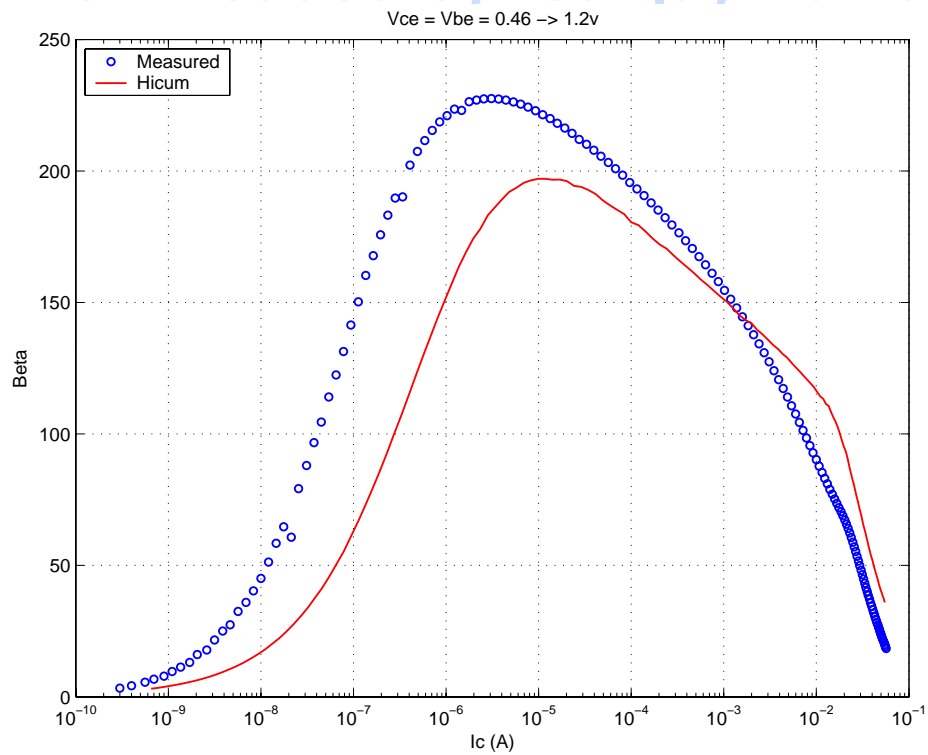
FIGURE 5.16 Beta vs. I_c : LV 0.15x0.76x10_122

FIGURE 5.17 I_C vs. V_{CE} at constant I_B : LV 0.15x0.76x10_122

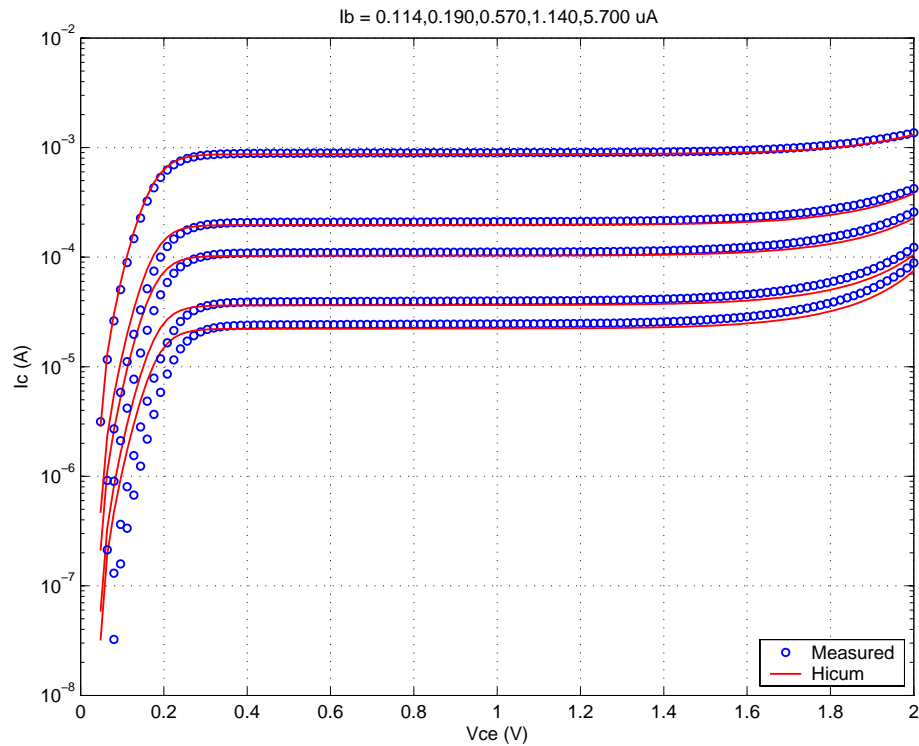


FIGURE 5.18 F_T vs. I_C : LV 0.15x0.76x10_122

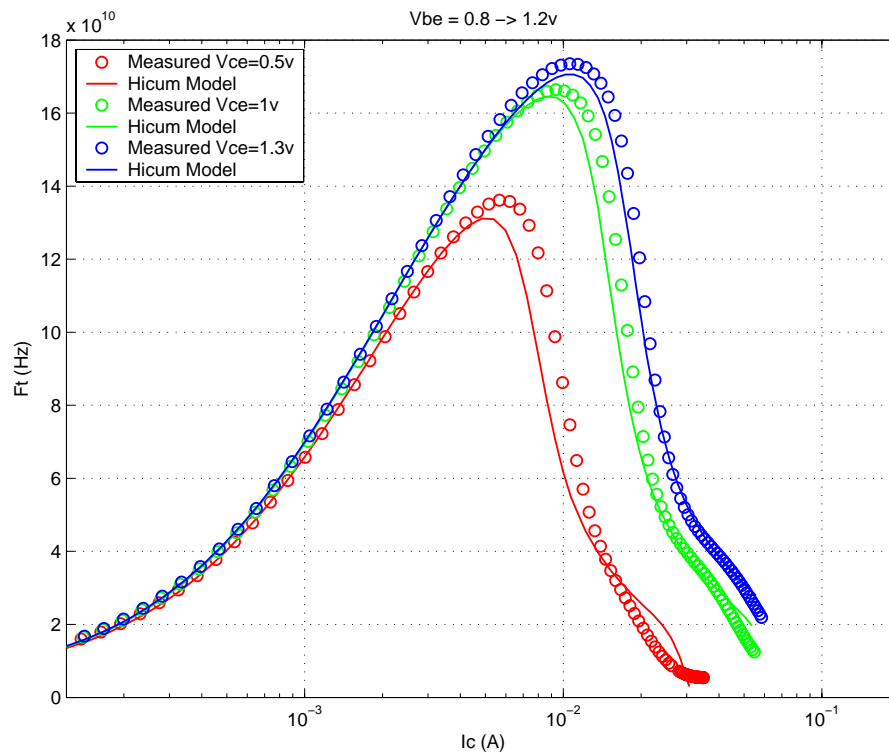
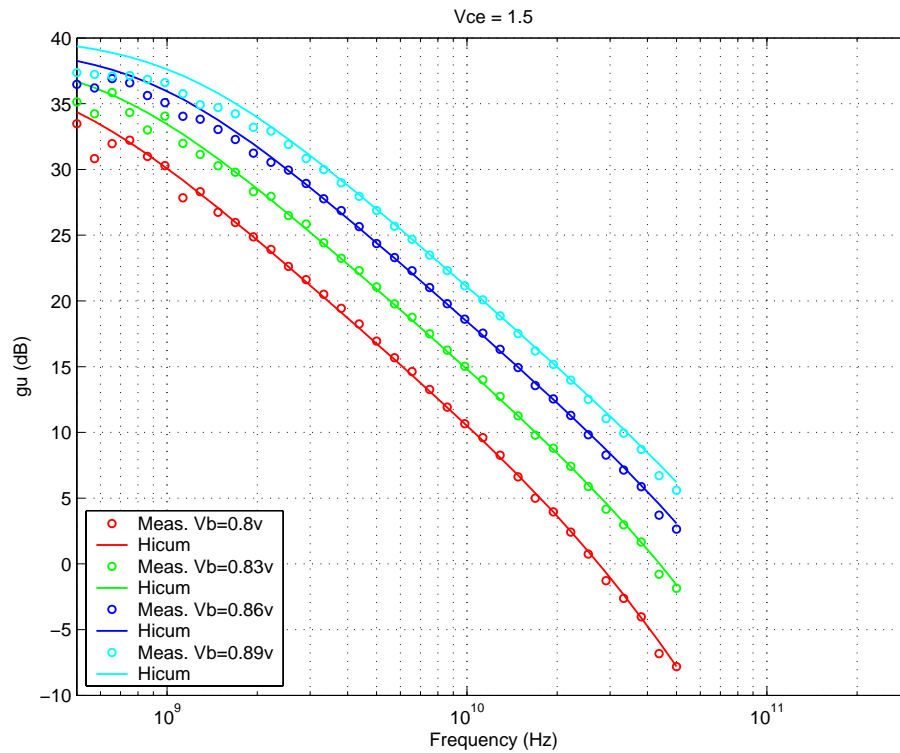


FIGURE 5.19 Power Gain vs. Freq: LV 0.15x0.76x10_122



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FIGURE 5.20 Y-parameters vs. FREQ: LV 0.15x0.76x10_122

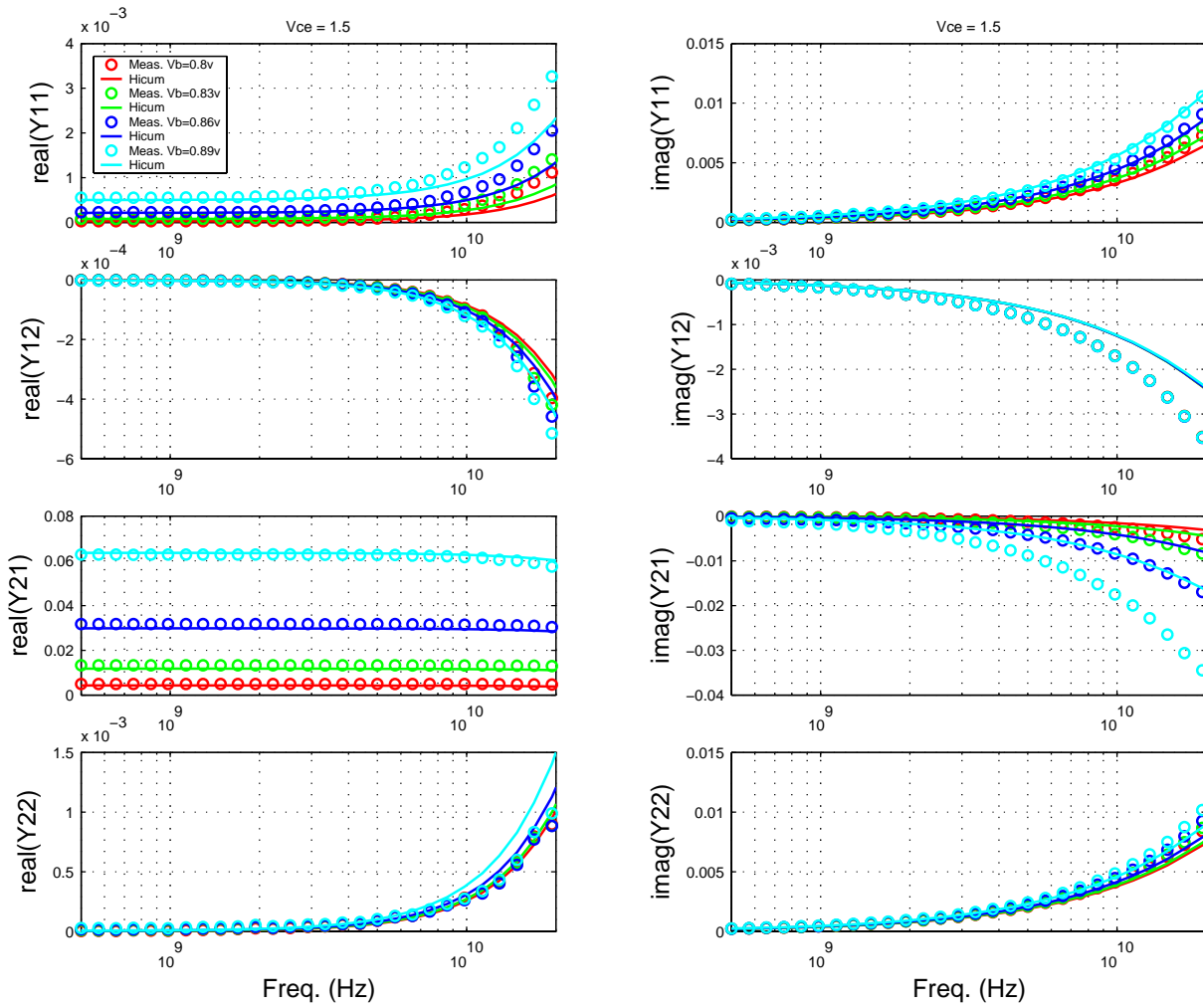


FIGURE 5.21 Gummel Plot LV 0.15x10.16x1_121

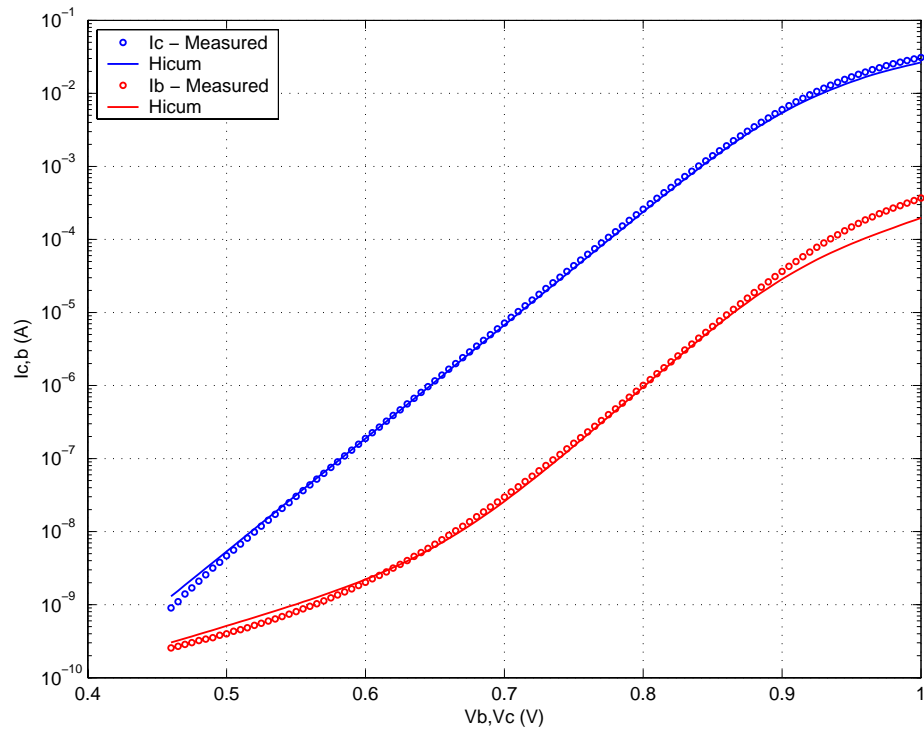
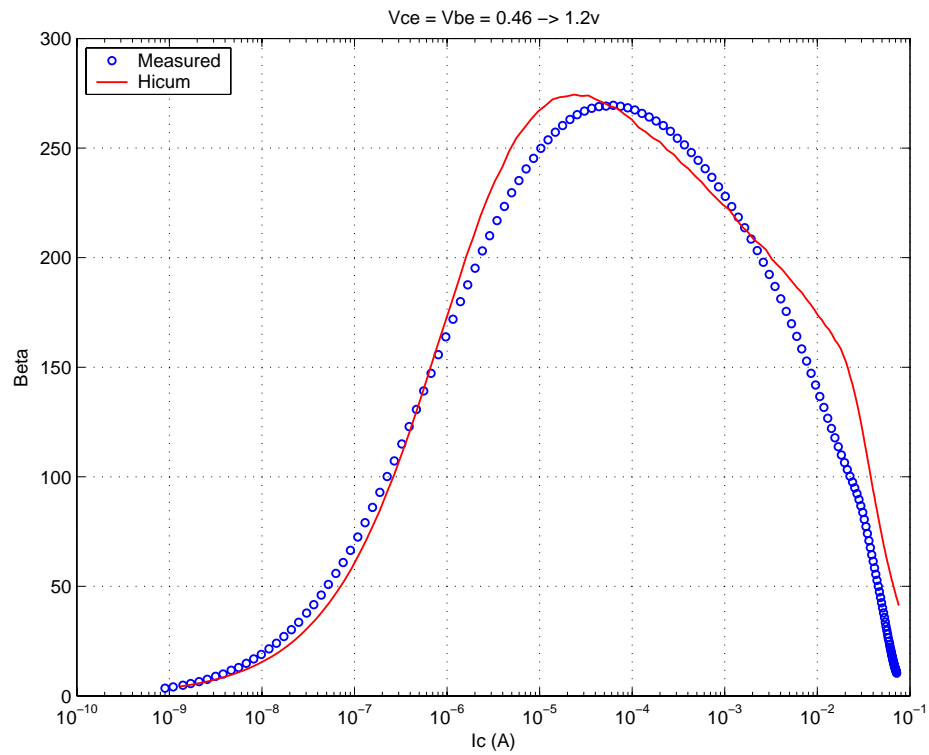
FIGURE 5.22 Beta vs. I_c : LV 0.15x10.16x1_121

FIGURE 5.23 IC vs. VCE at constant IB: LV 0.15x10.16x1_121

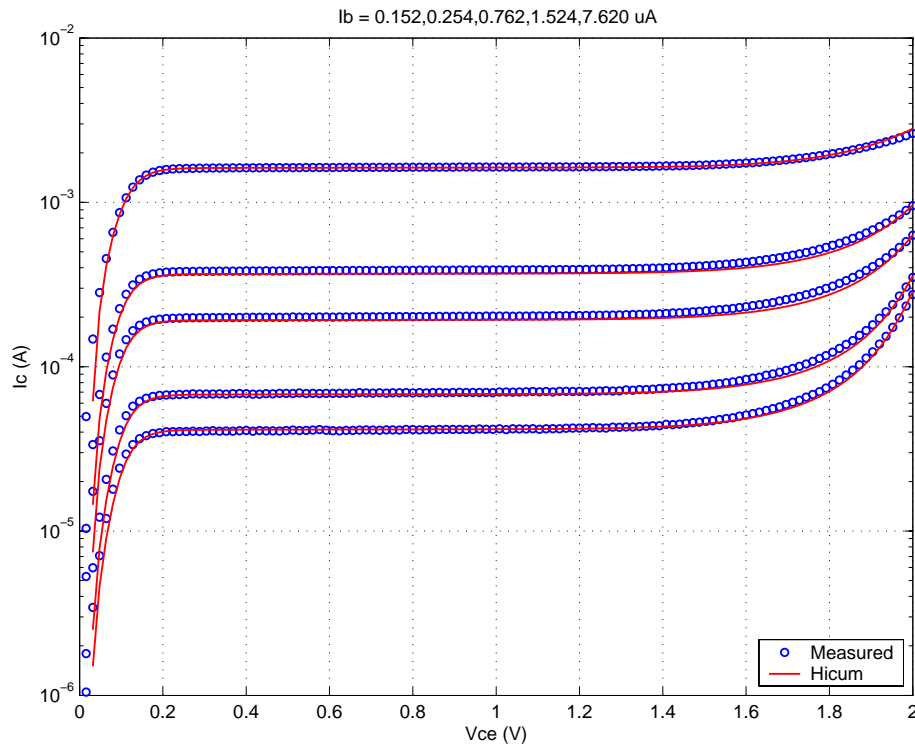


FIGURE 5.24 FT vs. IC: LV 0.15x10.16x1_121

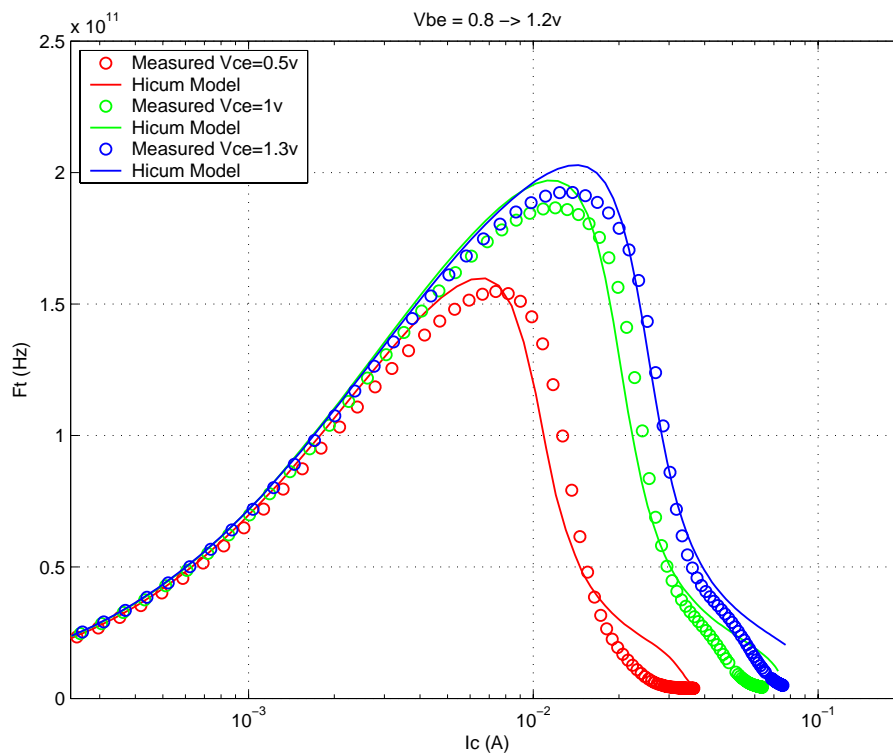
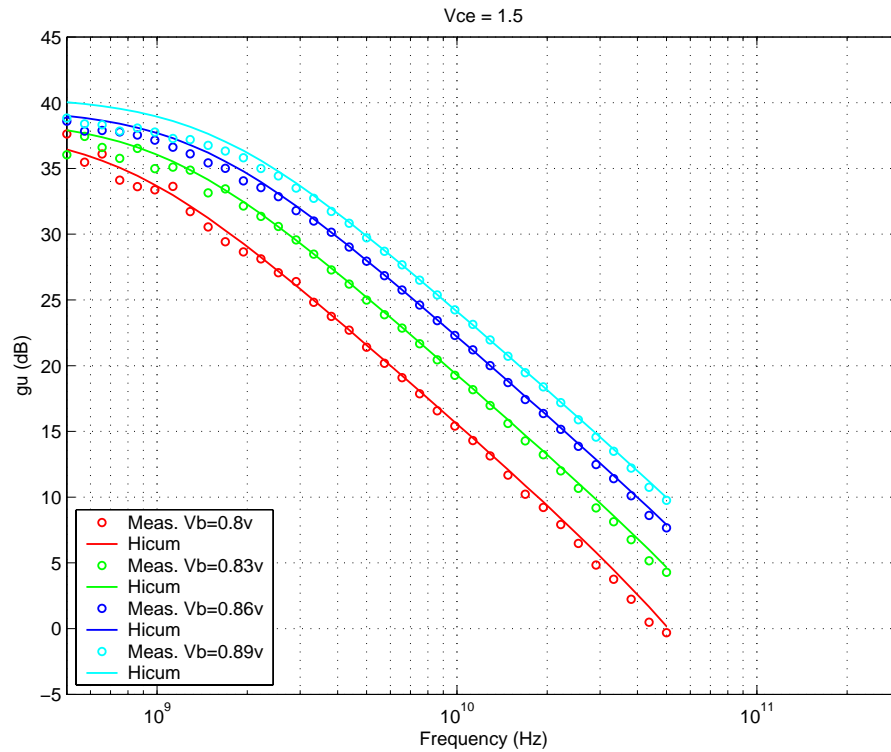


FIGURE 5.25 Power Gain vs. Freq: LV 0.15x10.16x1_121



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FIGURE 5.26 Y-parameters vs. FREQ: LV 0.15x10.16x1_121

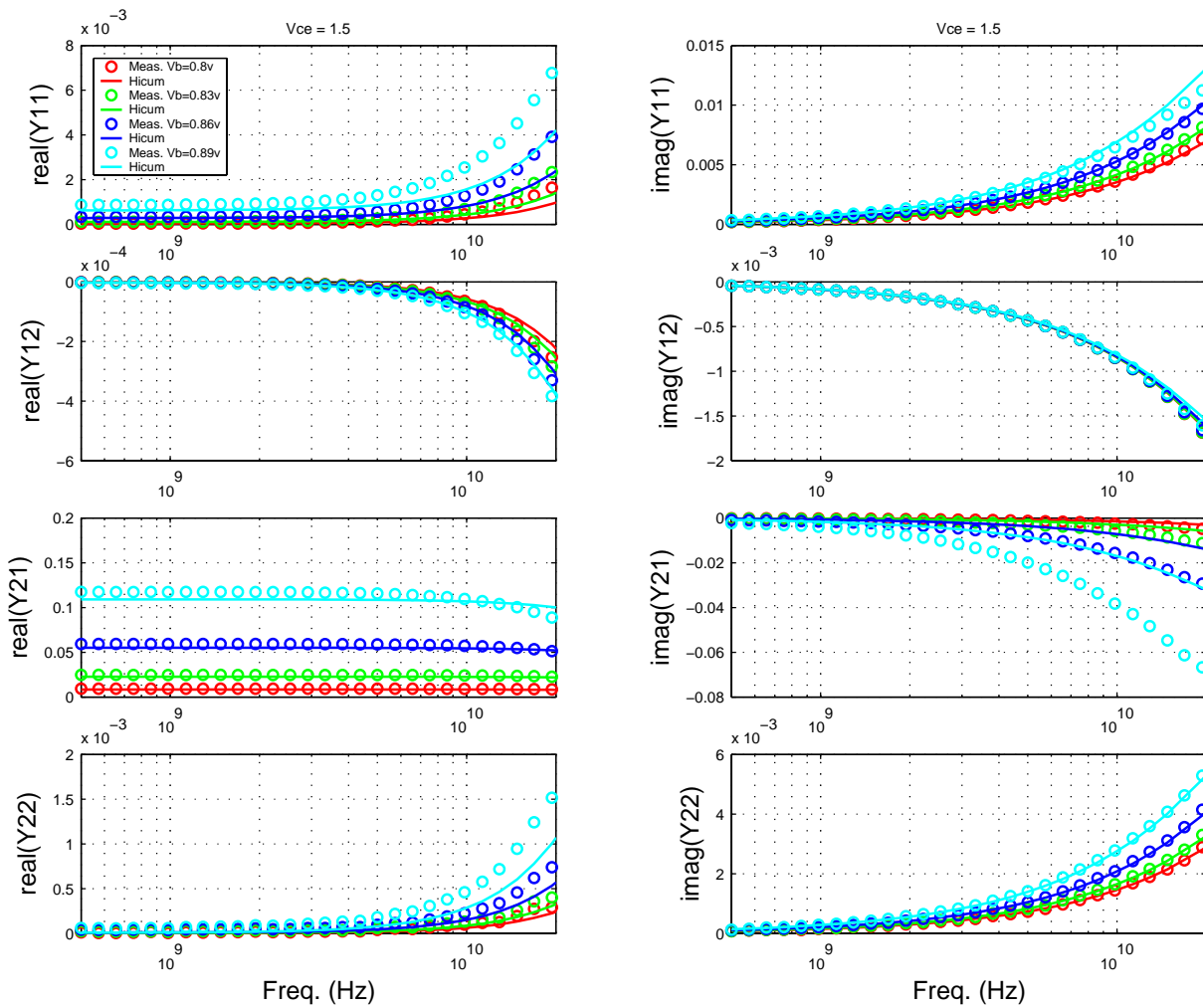


FIGURE 5.27 Gummel Plot LV 0.15x10.16x1_232

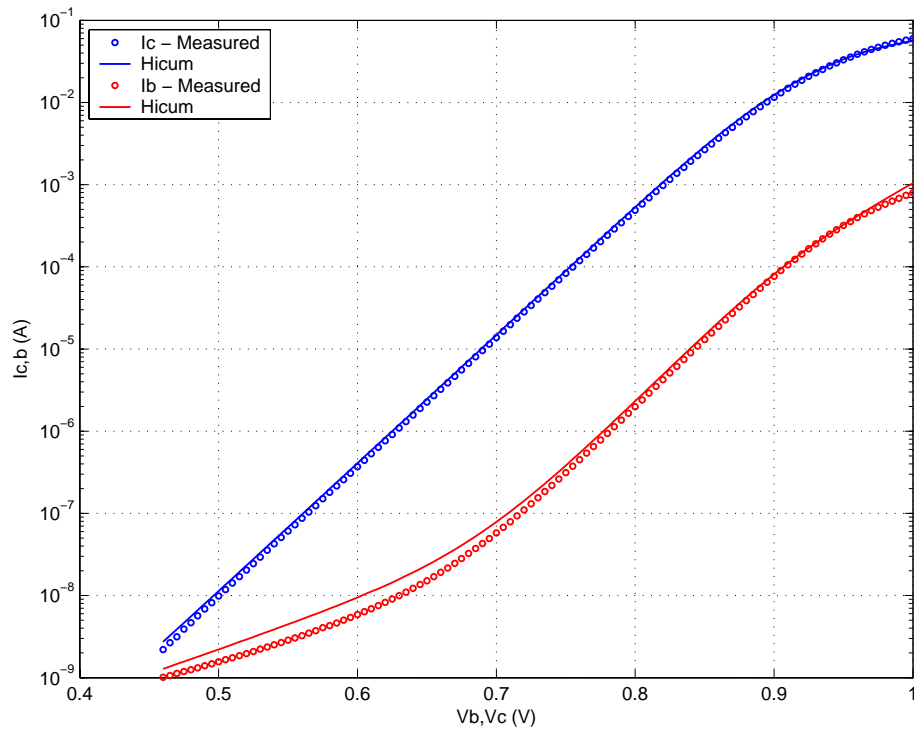
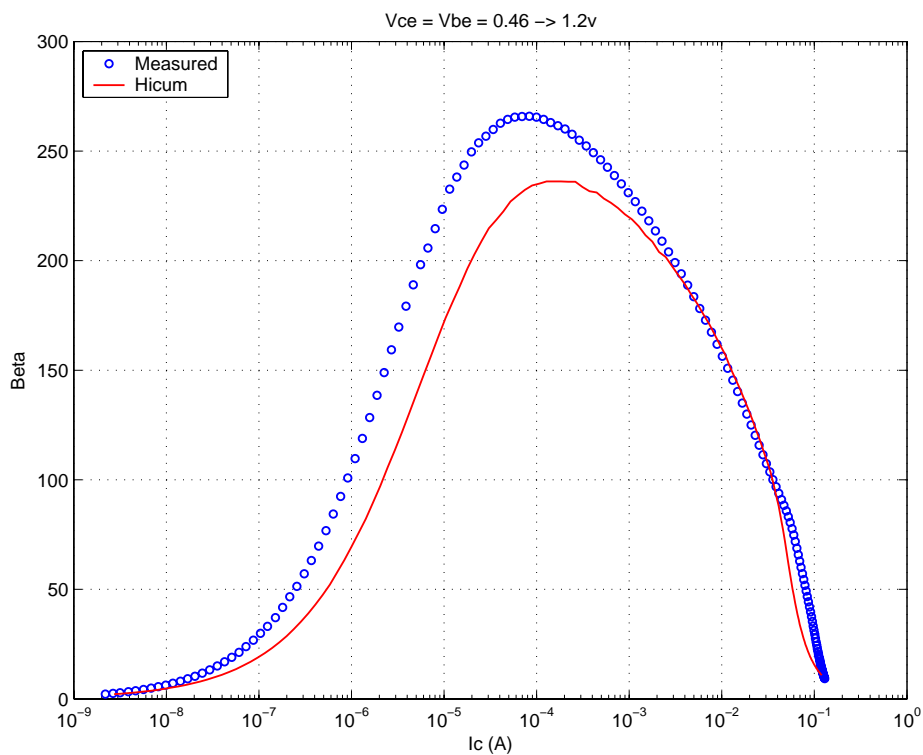
FIGURE 5.28 Beta vs. I_c : LV 0.15x10.16x1_232

FIGURE 5.29 I_C vs. V_{CE} at constant I_B : LV 0.15x10.16x1_232

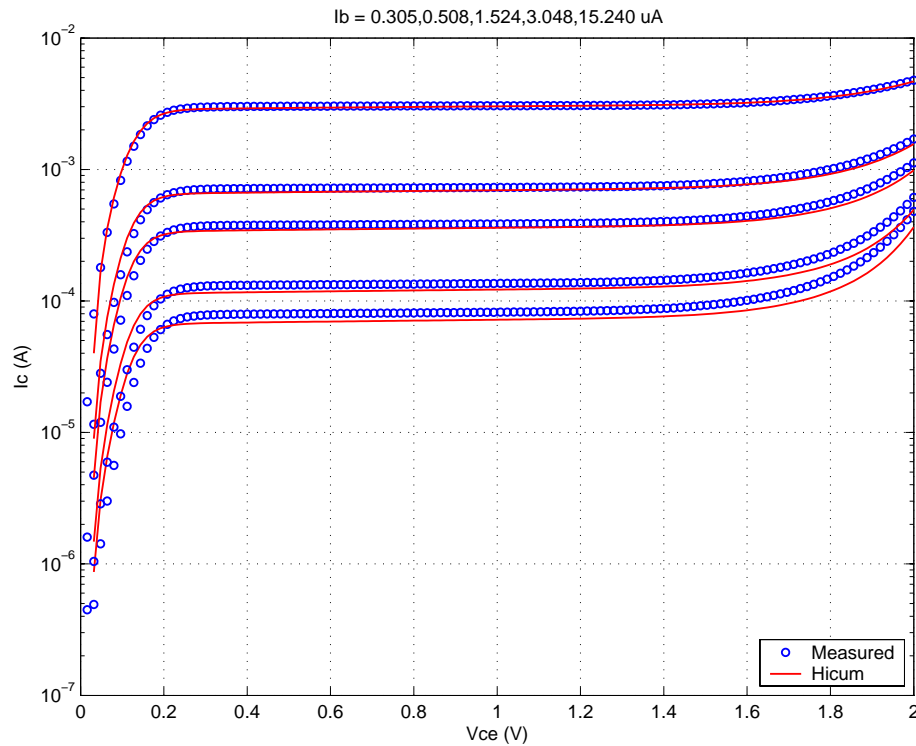


FIGURE 5.30 f_T vs. I_C : LV 0.15x10.16x1_232

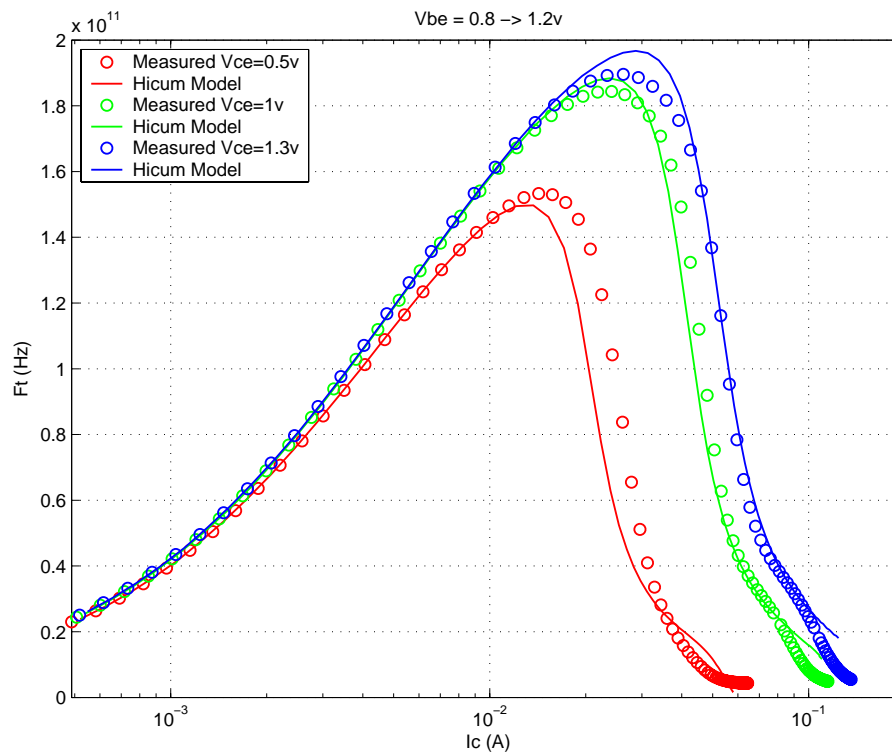
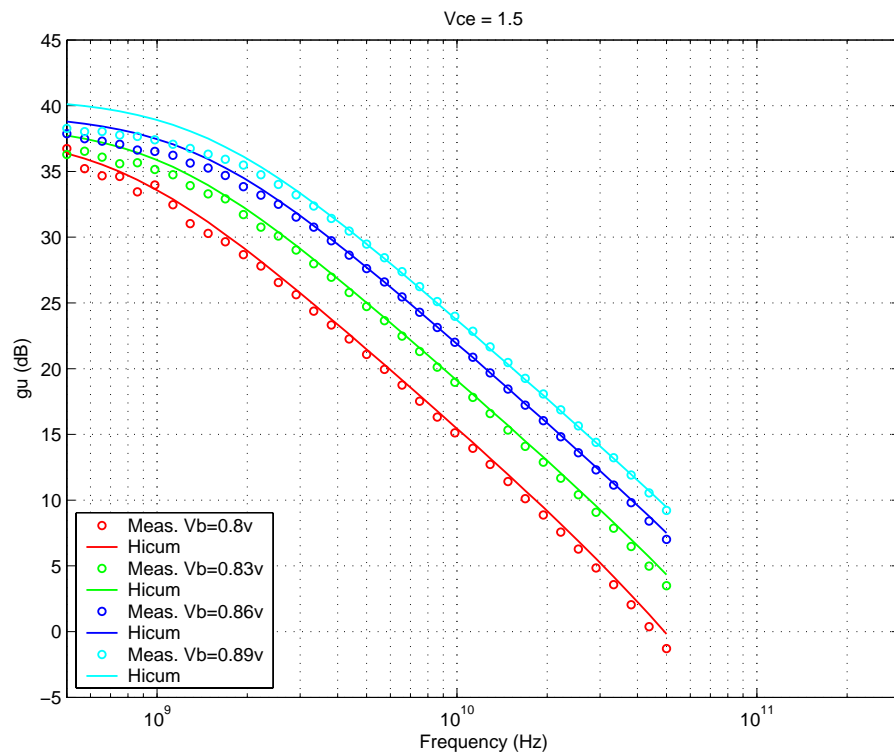


FIGURE 5.31 Power Gain vs. Freq: LV 0.15x10.16x1_232



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FIGURE 5.32 Y-parameters vs. FREQ: LV 0.15x10.16x1_232

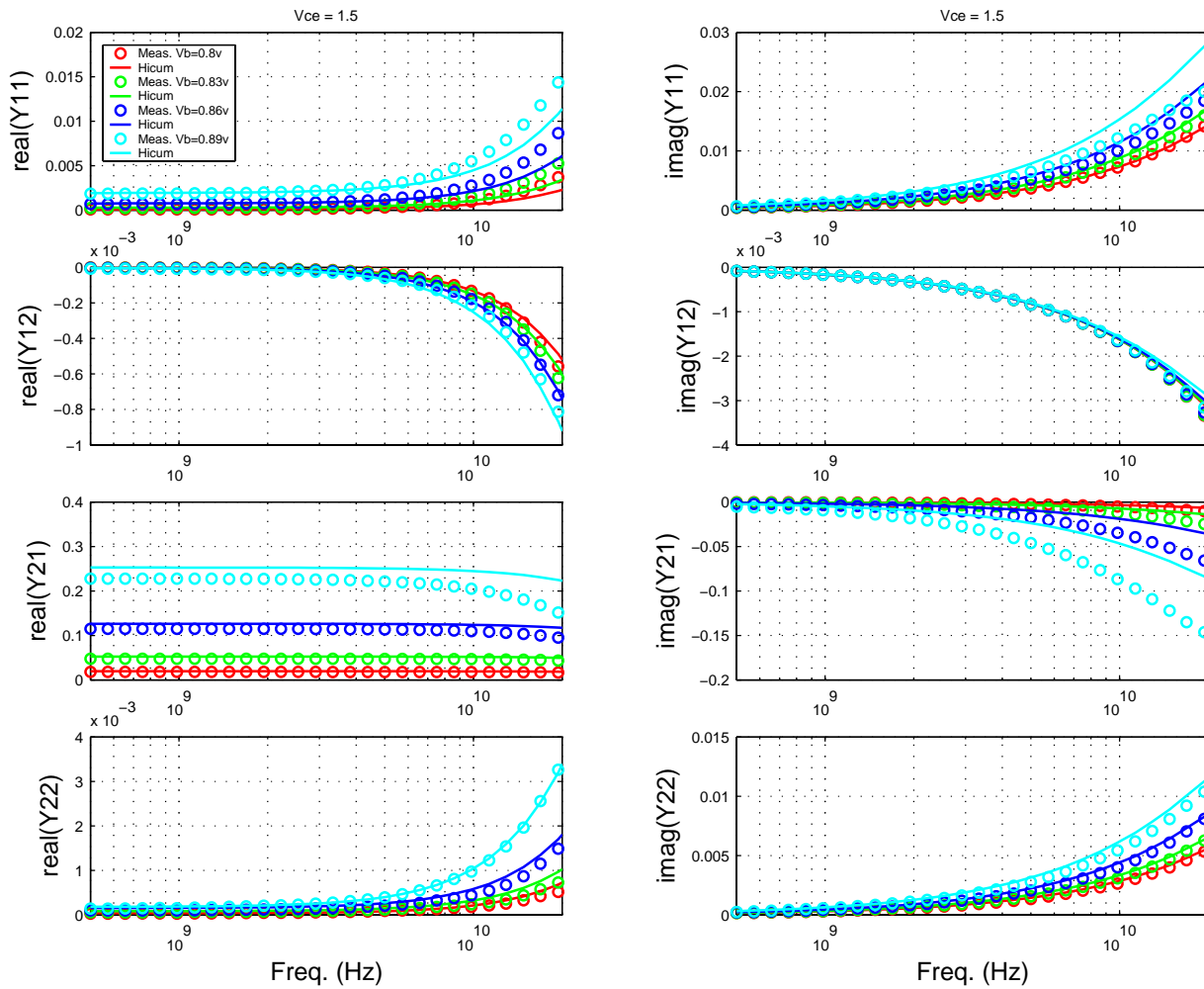


FIGURE 5.33 Gummel Plot LV 0.15x4.52x1_232

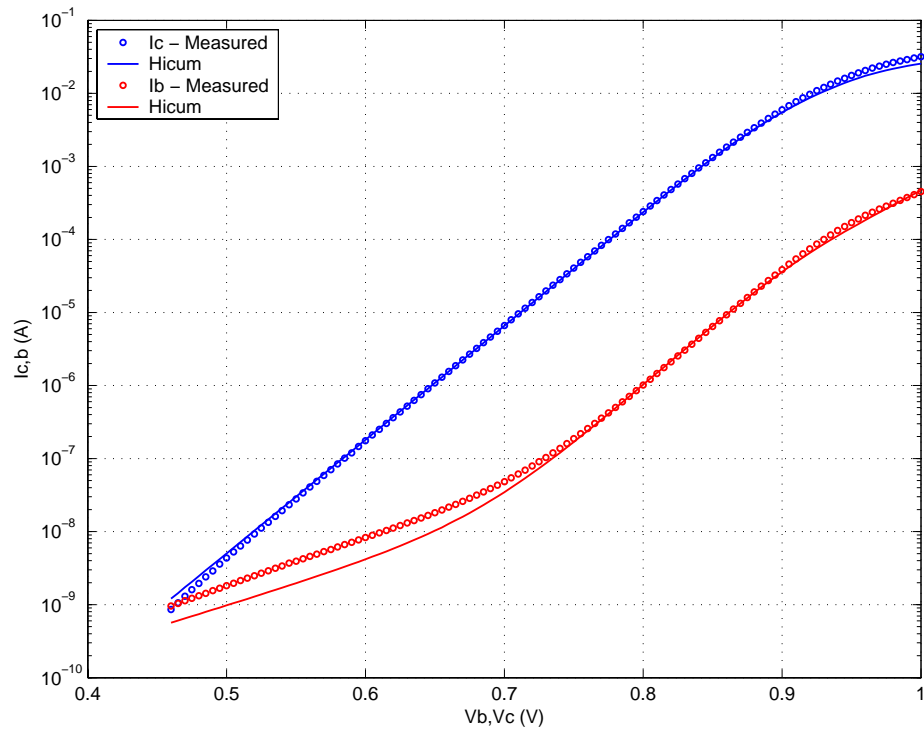
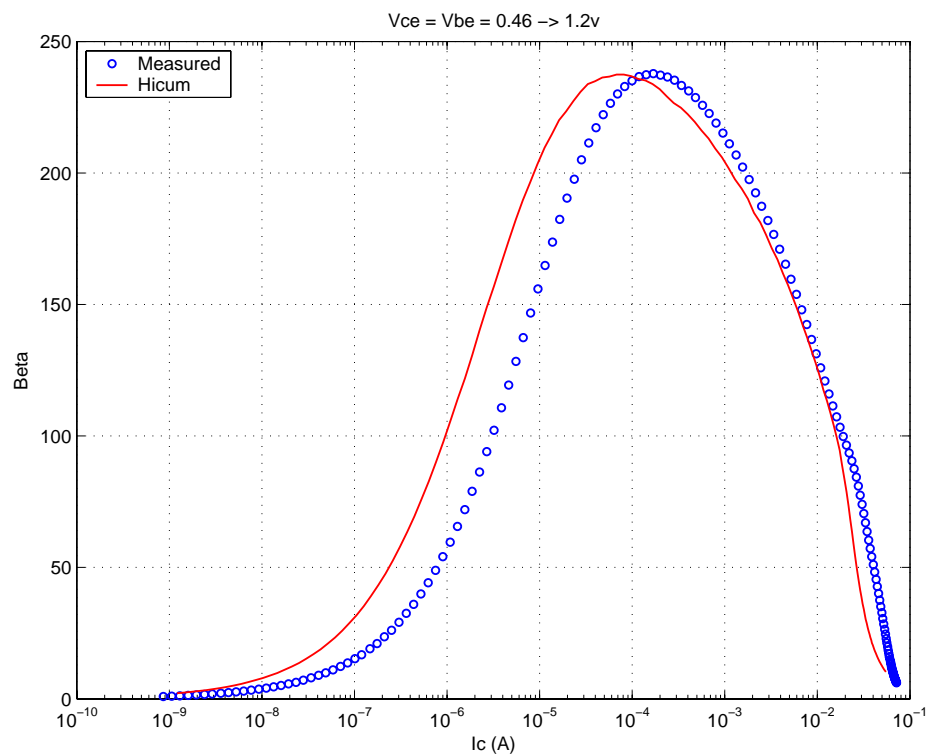
FIGURE 5.34 Beta vs. I_c : LV 0.15x4.52x1_232

FIGURE 5.35 I_C vs. V_{CE} at constant I_B : LV 0.15x4.52x1_232

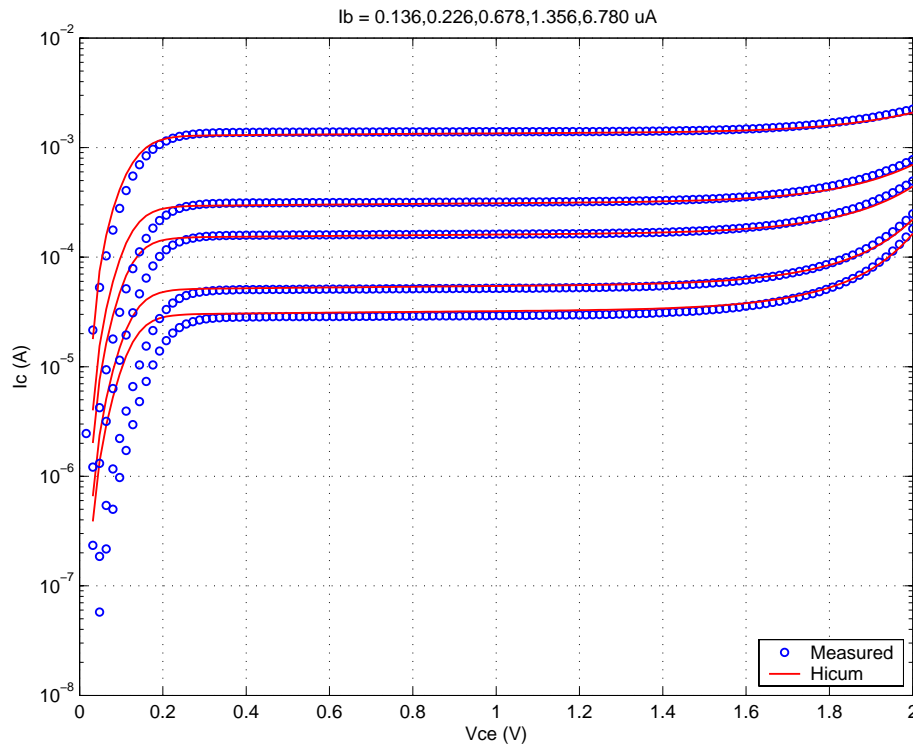


FIGURE 5.36 f_T vs. I_C : LV 0.15x4.52x1_232

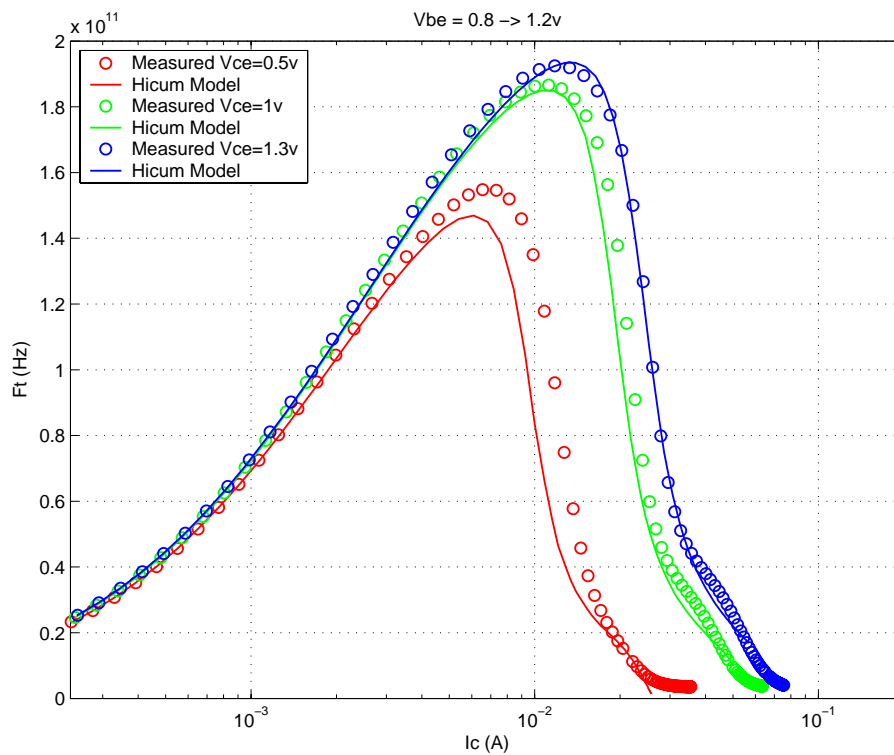
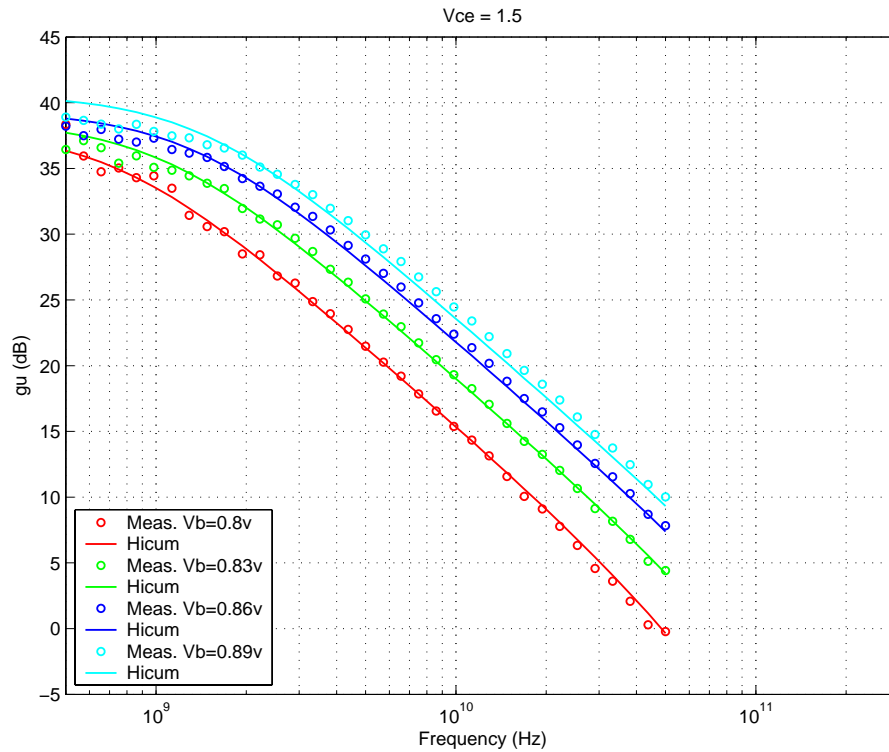


FIGURE 5.37 Power Gain vs. Freq: LV 0.15x4.52x1_232



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FIGURE 5.38 Y-parameters vs. FREQ: LV 0.15x4.52x1_232

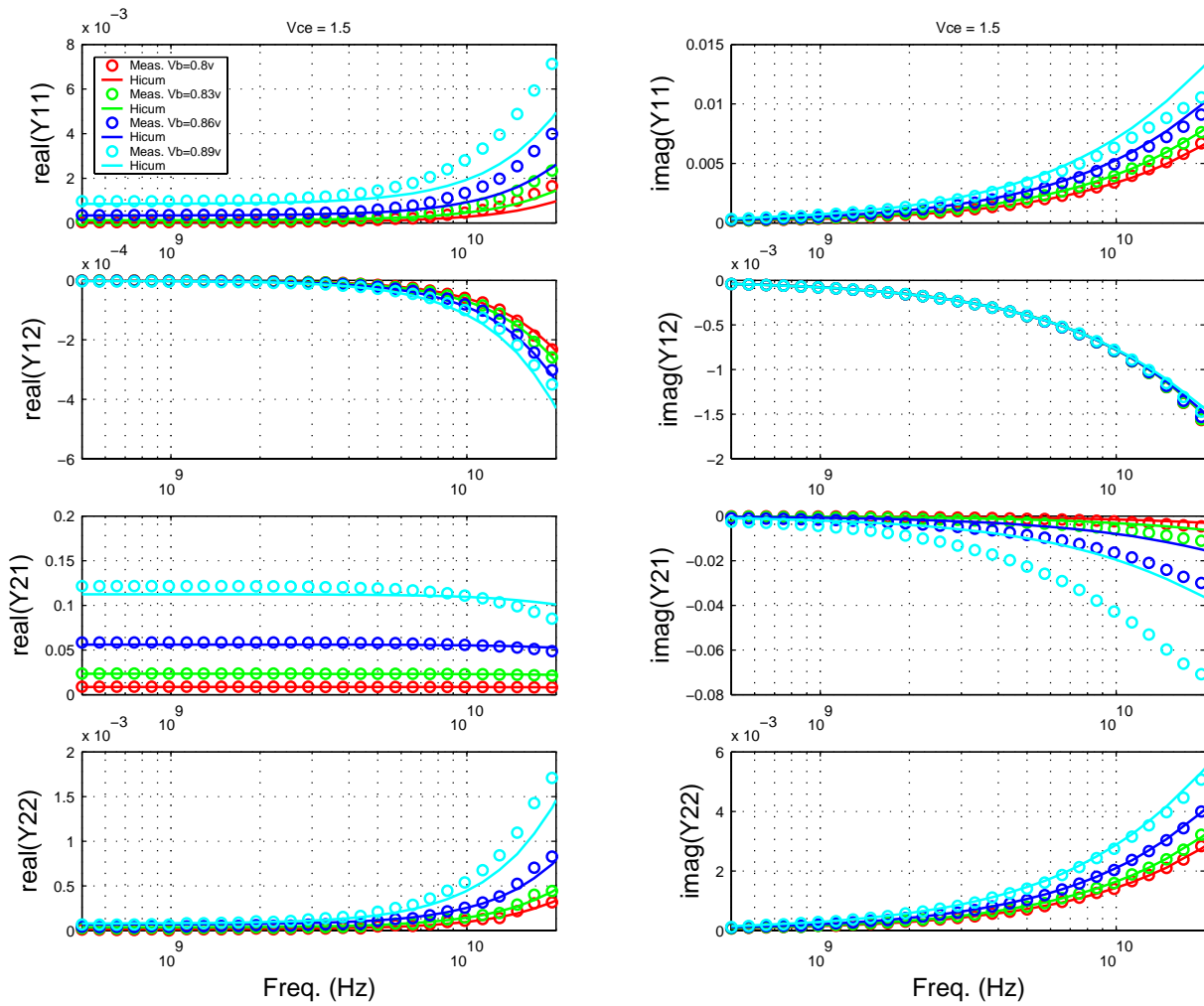


FIGURE 5.39 Gummel Plot LV 0.15x2.84x1_232

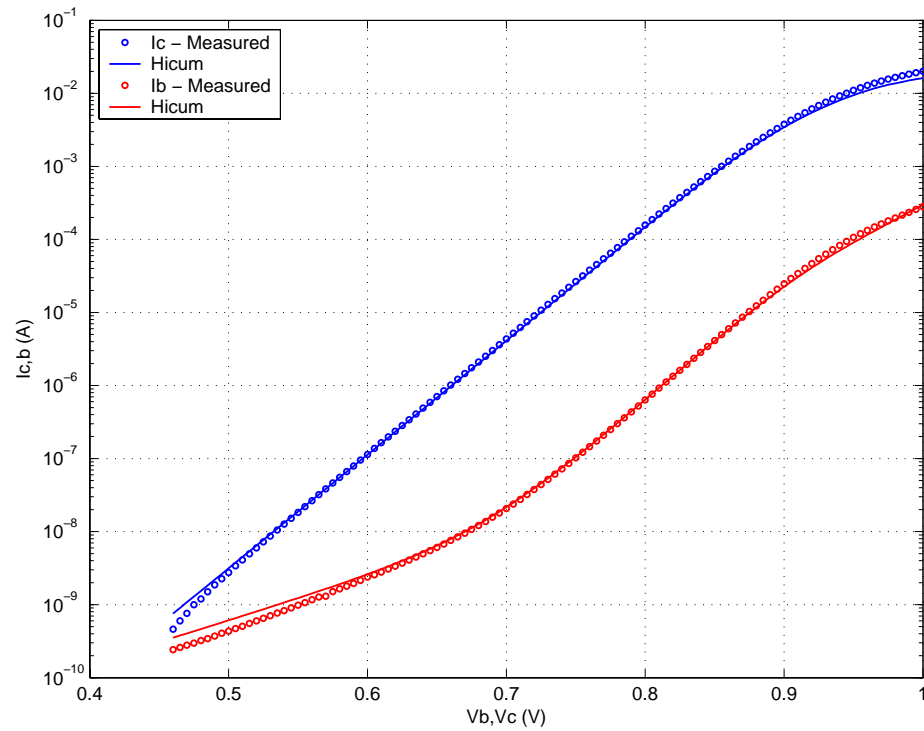
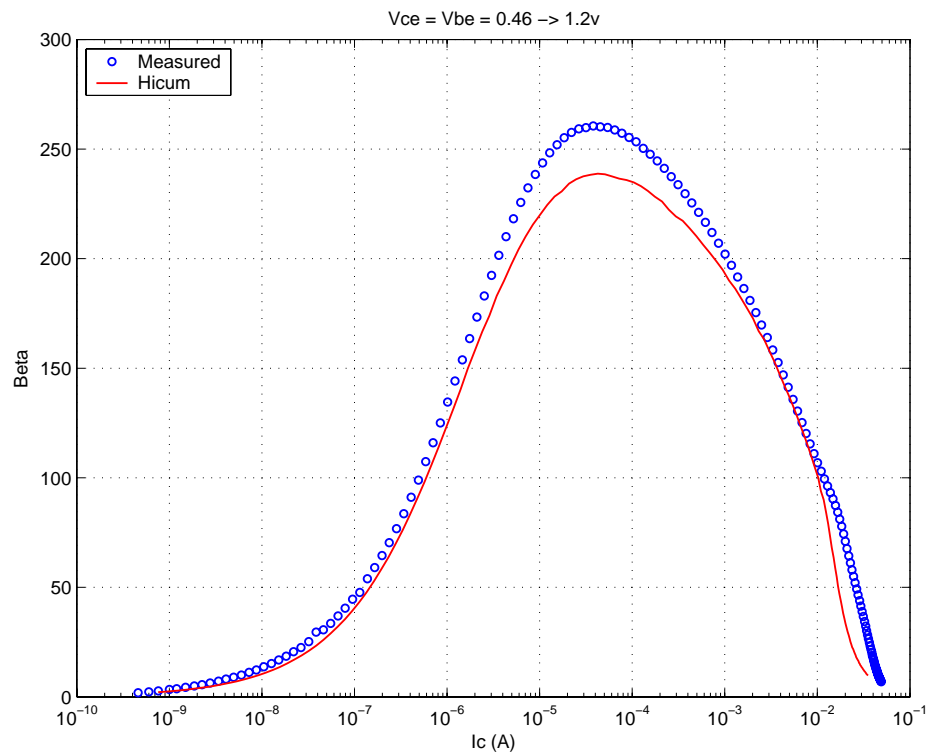
FIGURE 5.40 Beta vs. I_c : LV 0.15x2.84x1_232

FIGURE 5.41 IC vs. VCE at constant IB: LV 0.15x2.84x1_232

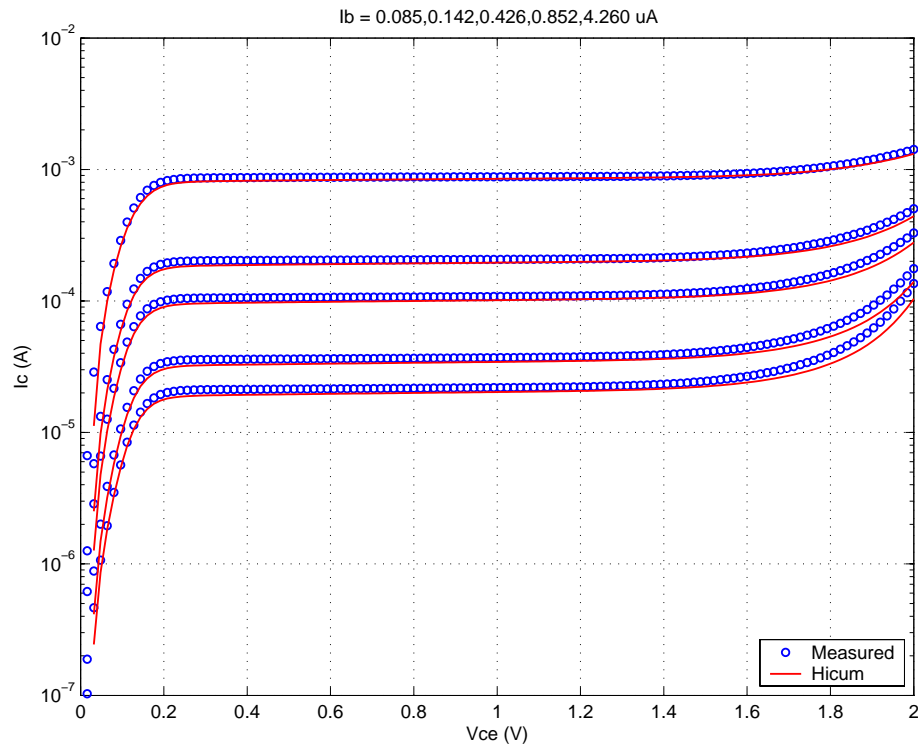


FIGURE 5.42 FT vs. IC: LV 0.15x2.84x1_232

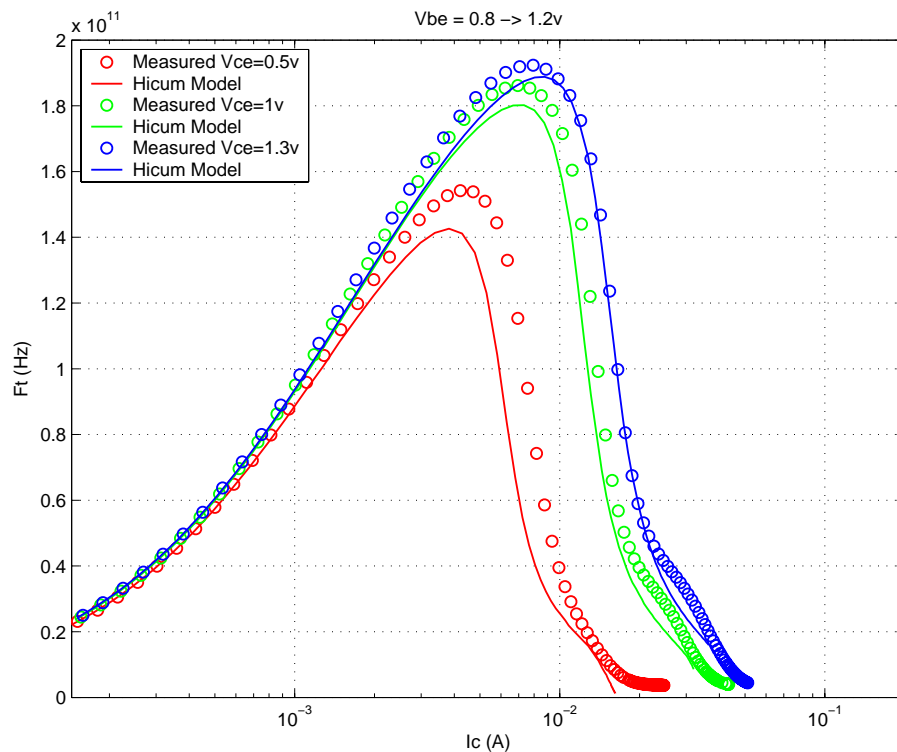
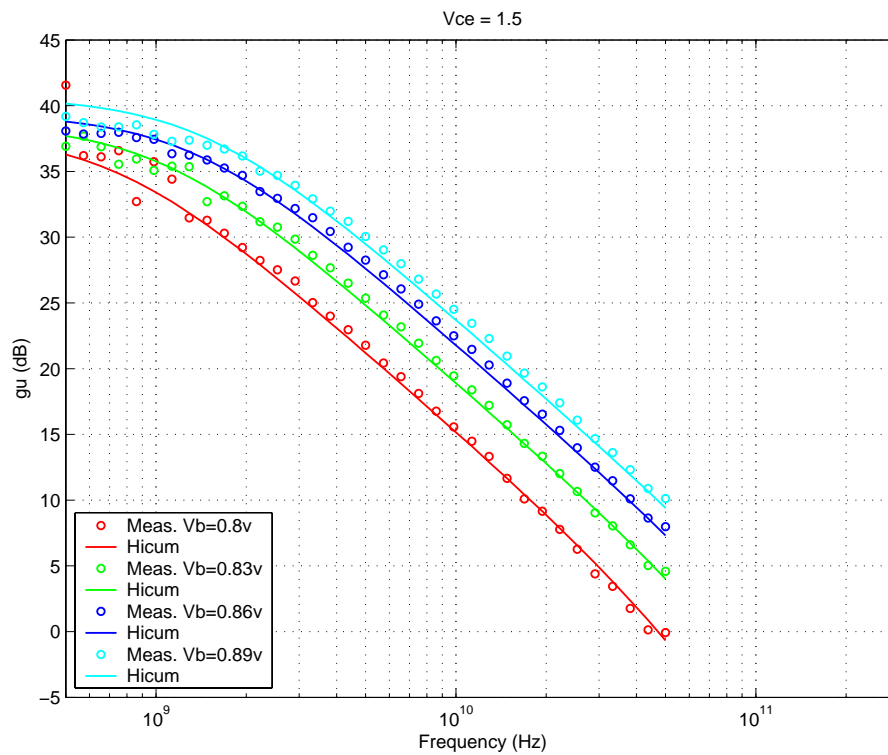
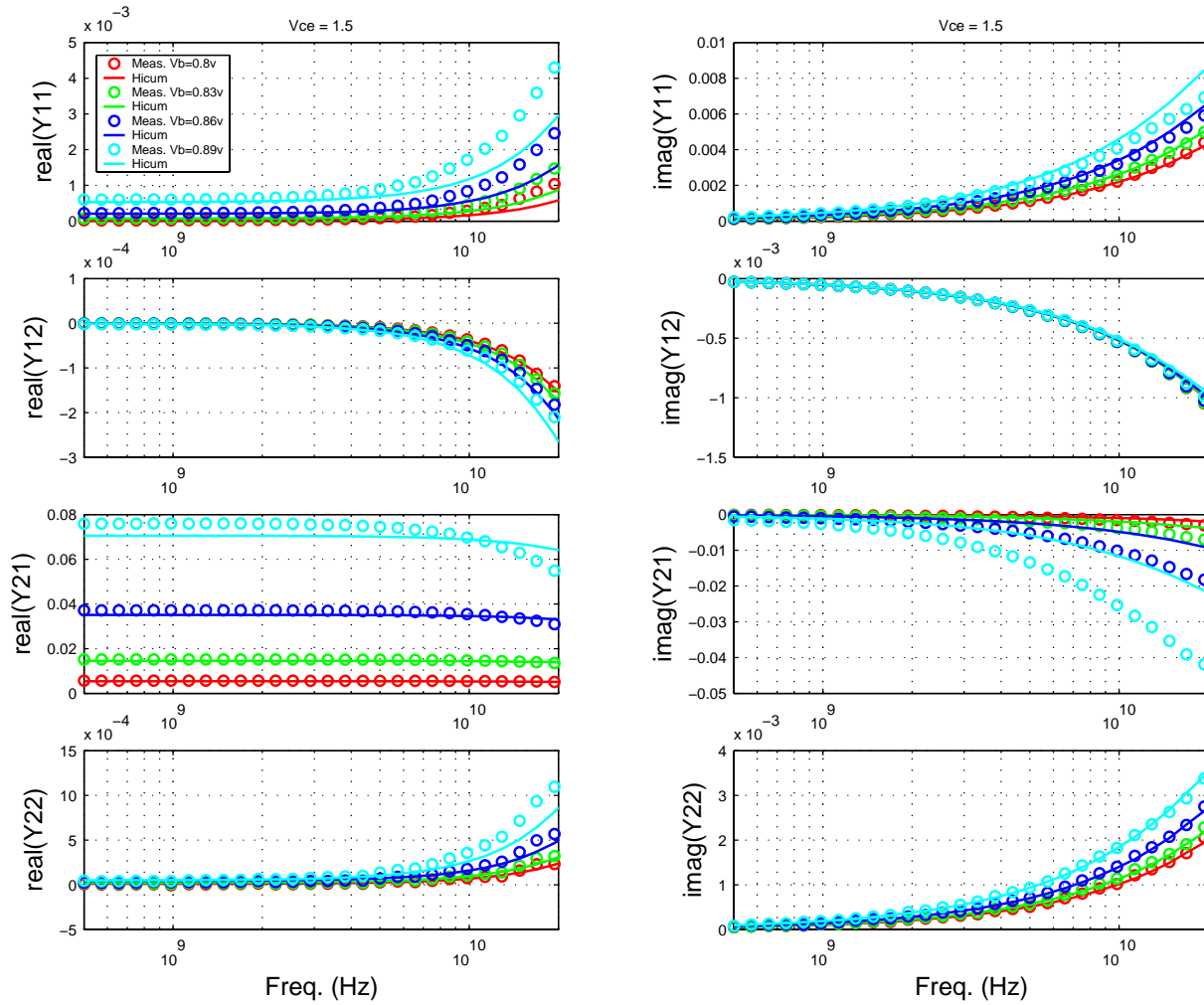


FIGURE 5.43 Power Gain vs. Freq: LV 0.15x2.84x1_232



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FIGURE 5.44 Y-parameters vs. FREQ: LV 0.15x2.84x1_232



5.4.2 Medium Voltage NPN Verification Plots

FIGURE 5.45 Gummel Plot MV 0.15x8.28x1_122

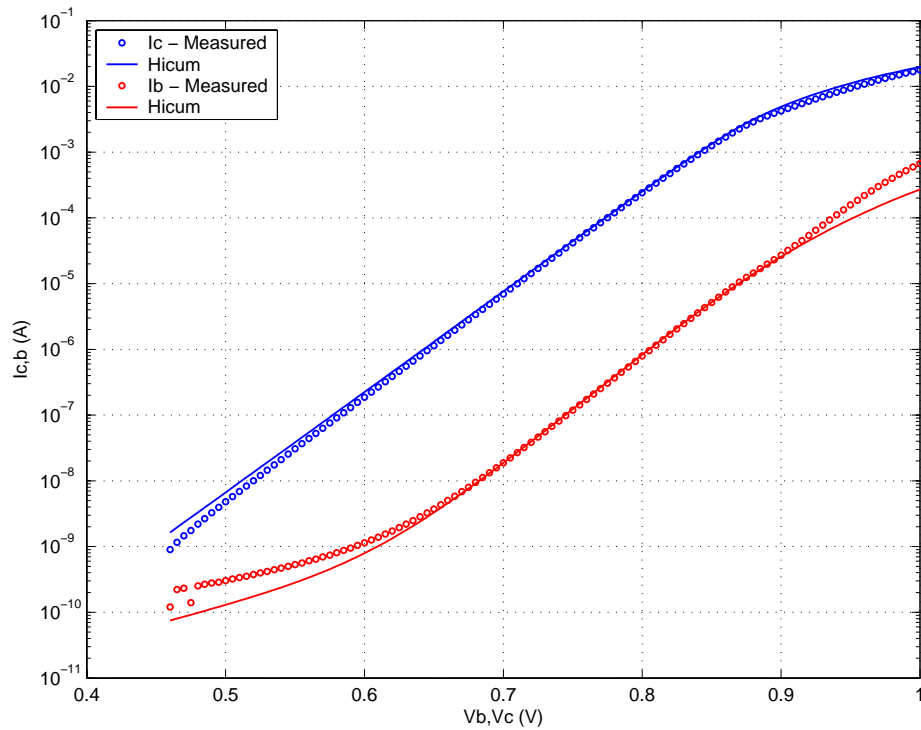


FIGURE 5.46 Beta vs. I_c : MV 0.15x8.28x1_122

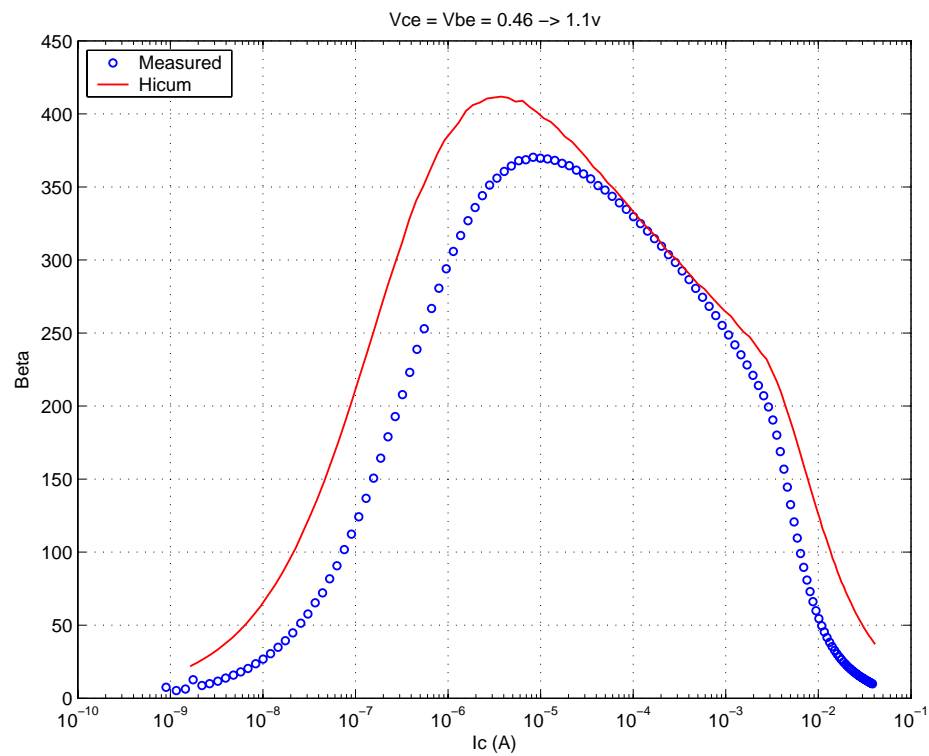


FIGURE 5.47 I_C vs. V_{CE} at constant I_B : MV 0.15x8.28x1_122

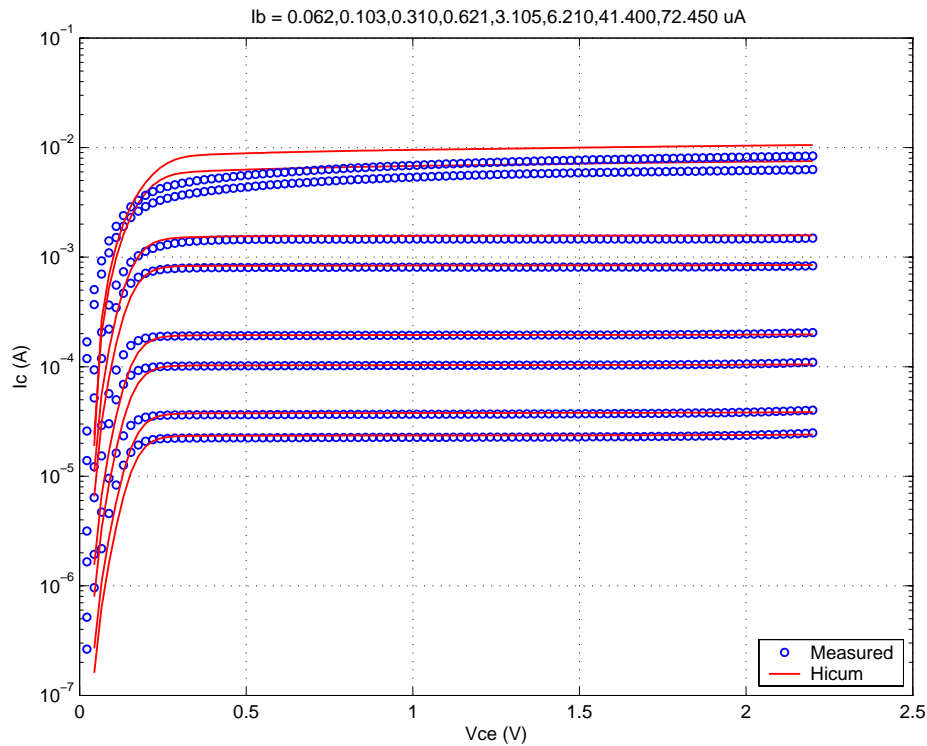


FIGURE 5.48 f_T vs. I_C : MV 0.15x8.28x1_122

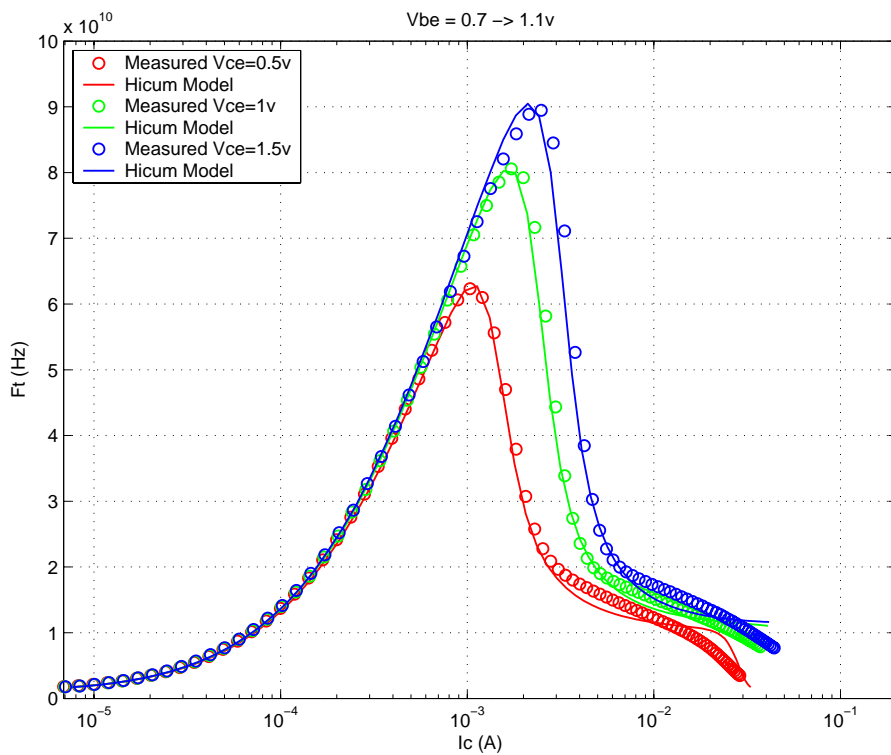
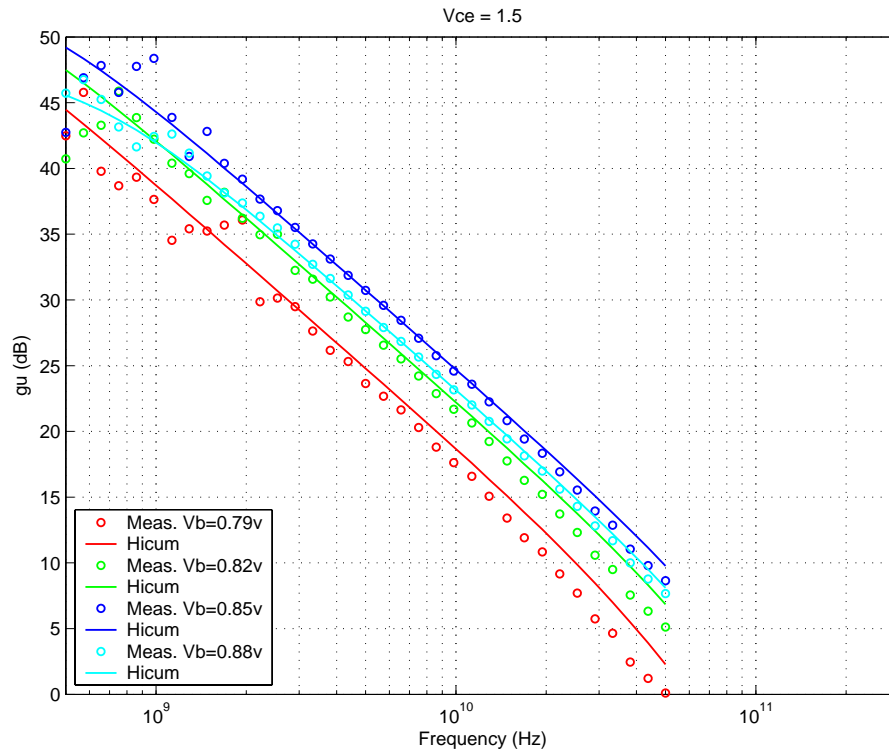


FIGURE 5.49 Power Gain vs. Freq: MV 0.15x8.28x1_122



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FIGURE 5.50 Y-parameters vs. FREQ: MV 0.15x8.28x1_122

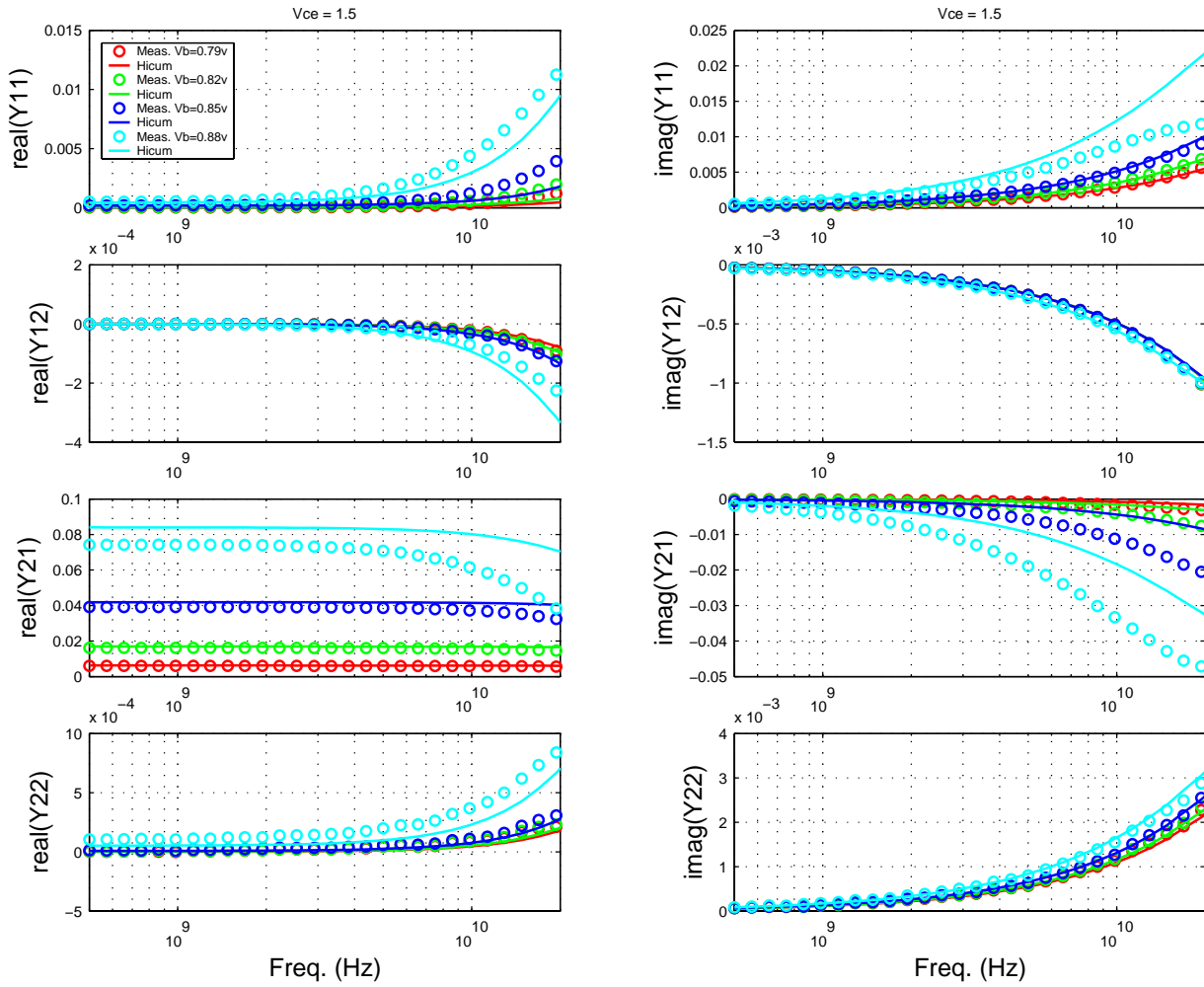


FIGURE 5.51 Gummel Plot MV 0.15x4.52x1_122

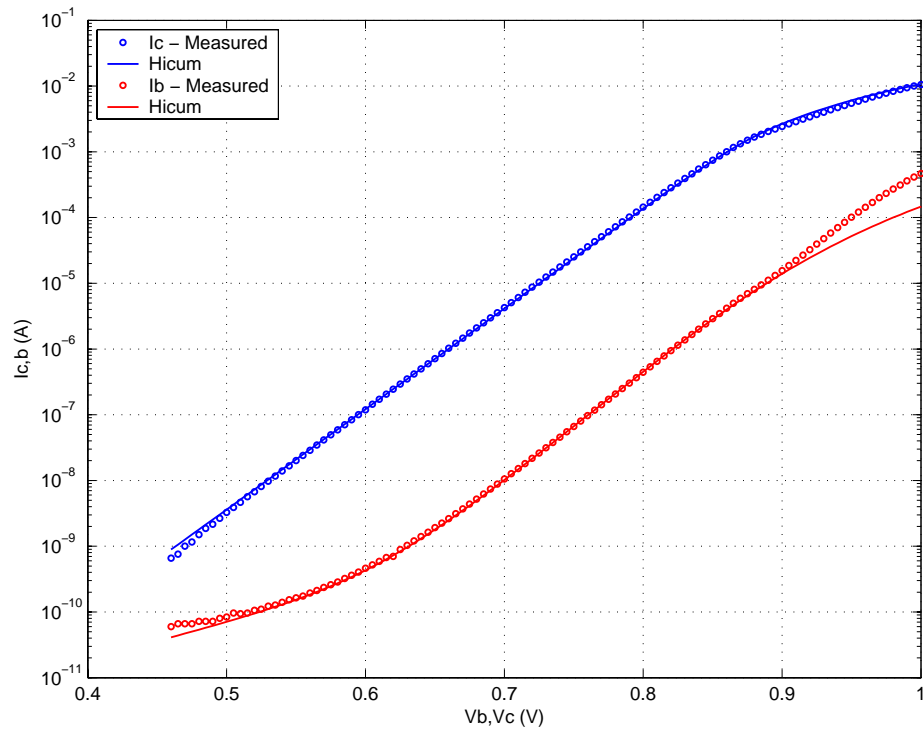
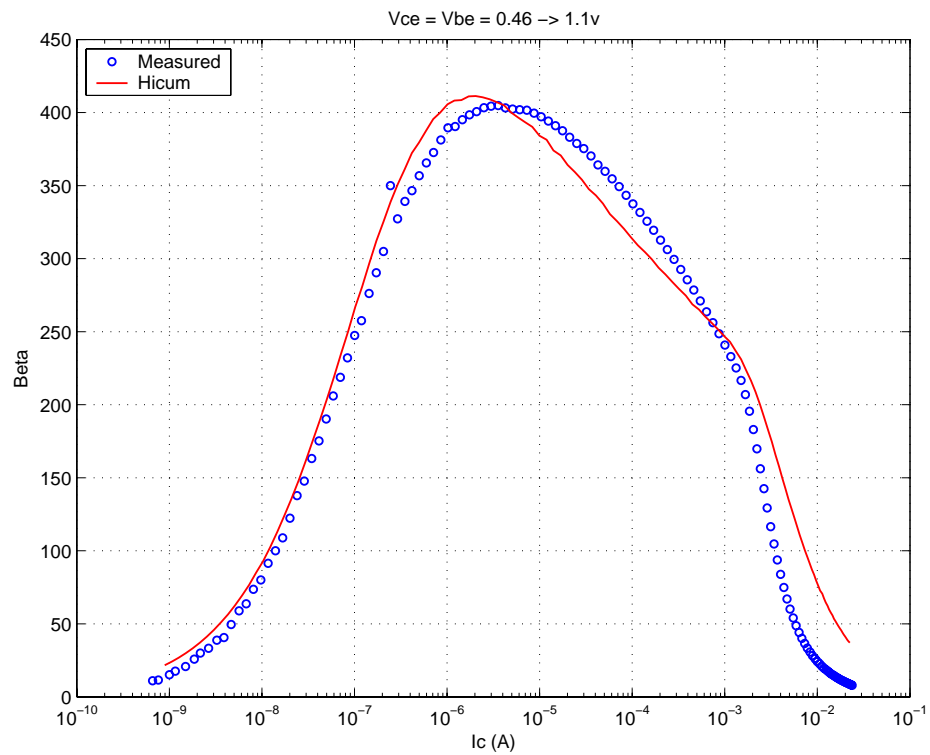
FIGURE 5.52 Beta vs. I_c : MV 0.15x4.52x1_122

FIGURE 5.53 IC vs. VCE at constant IB: MV 0.15x4.52x1_122

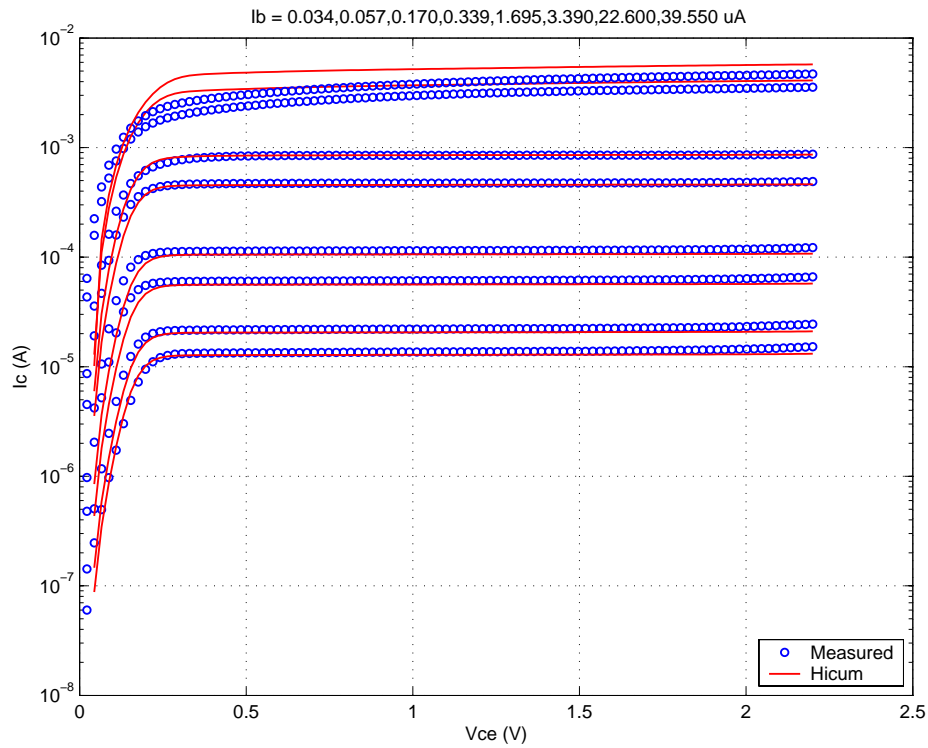


FIGURE 5.54 FT vs. IC: MV 0.15x4.52x1_122

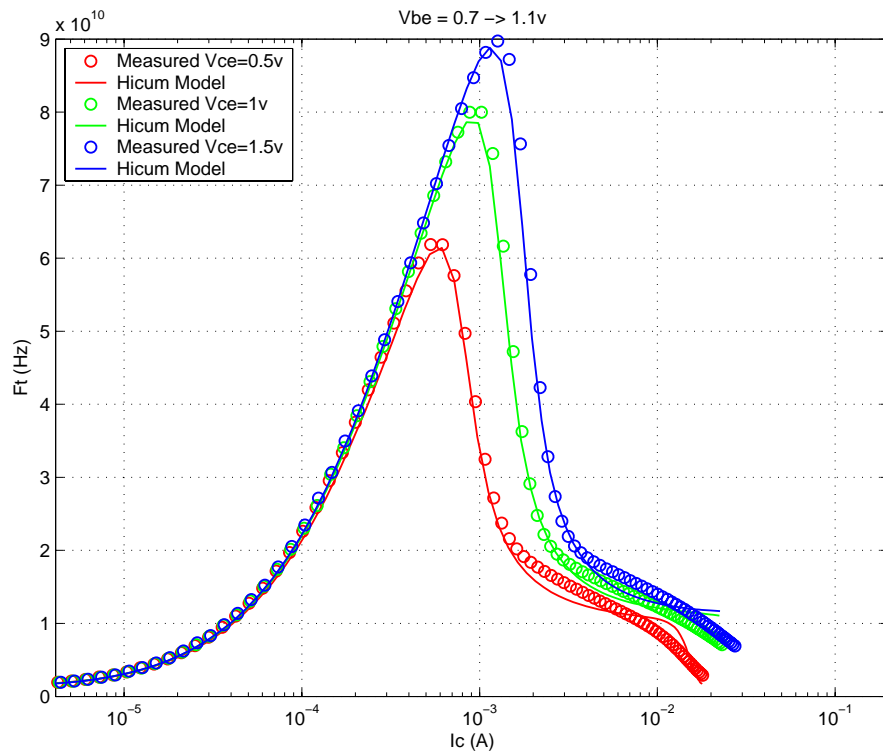
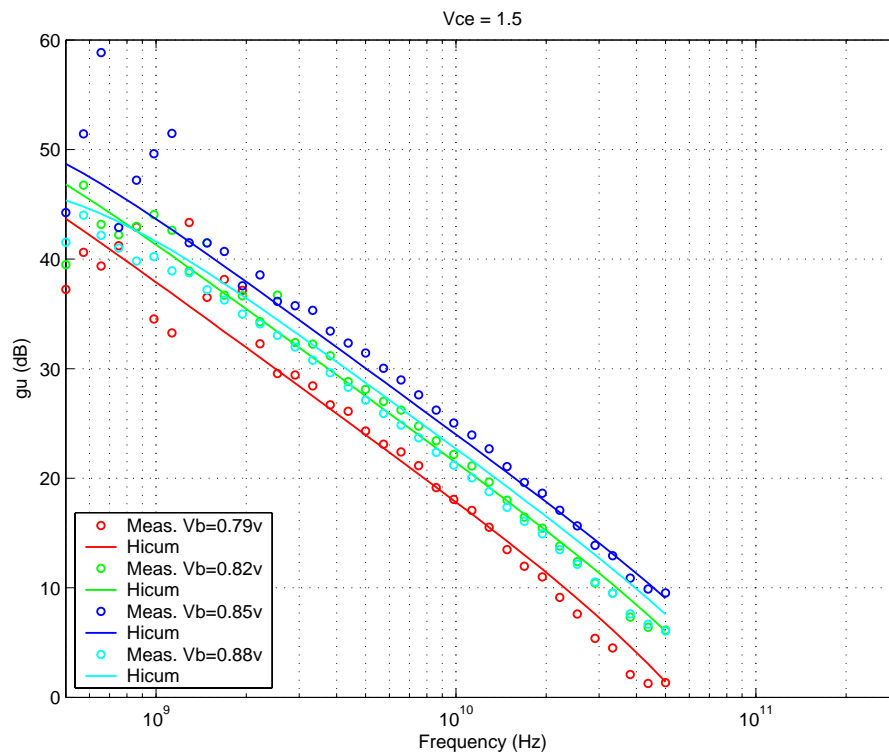


FIGURE 5.55 Power Gain vs. Freq: MV 0.15x4.52x1_122



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FIGURE 5.56 Y-parameters vs. FREQ: MV 0.15x4.52x1_122

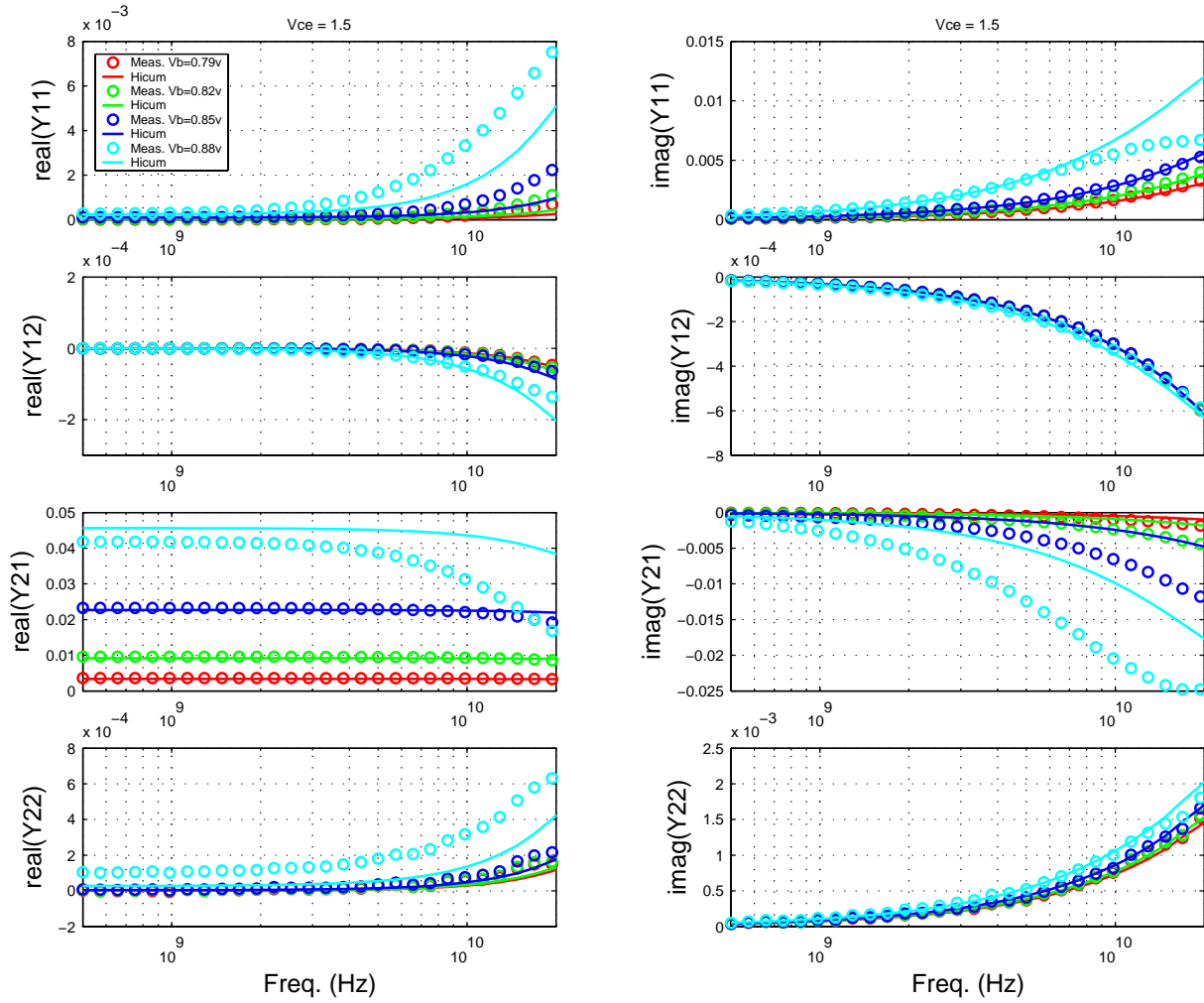


FIGURE 5.57 Gummel Plot: MV 0.15x0.76x10_122

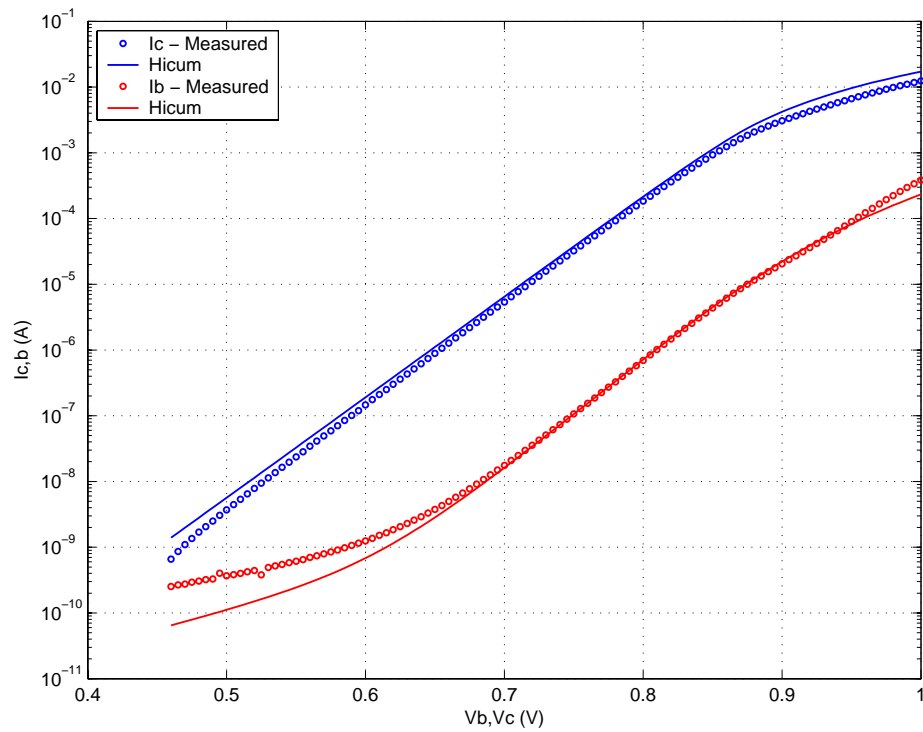
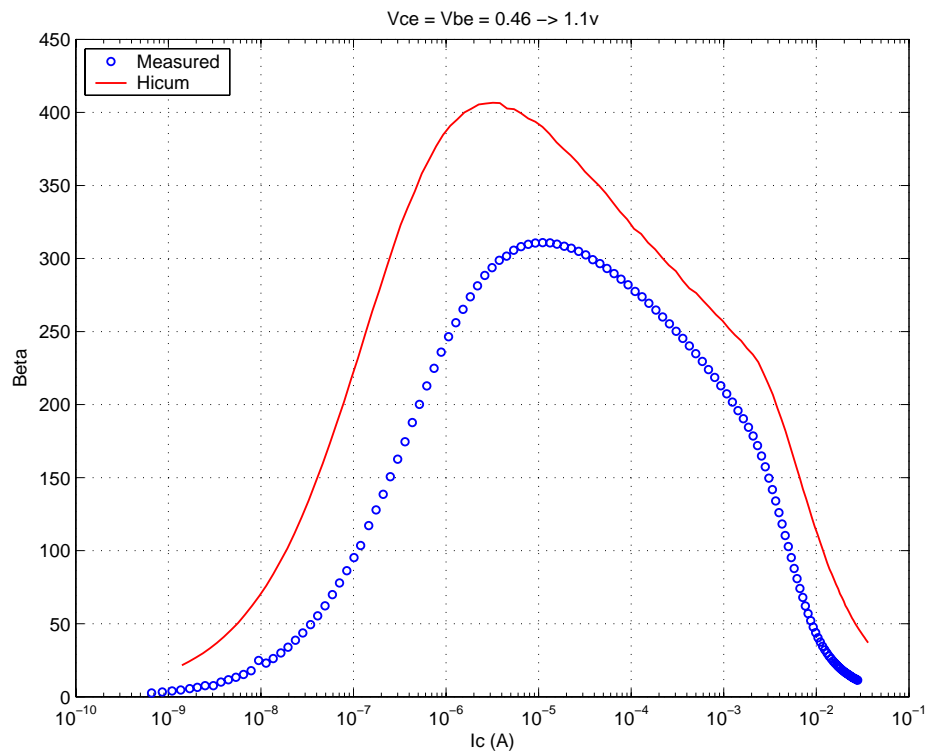
FIGURE 5.58 Beta vs. I_c : MV 0.15x0.76x10_122

FIGURE 5.59 I_C vs. V_{CE} at constant I_B : MV 0.15x0.76x10_122

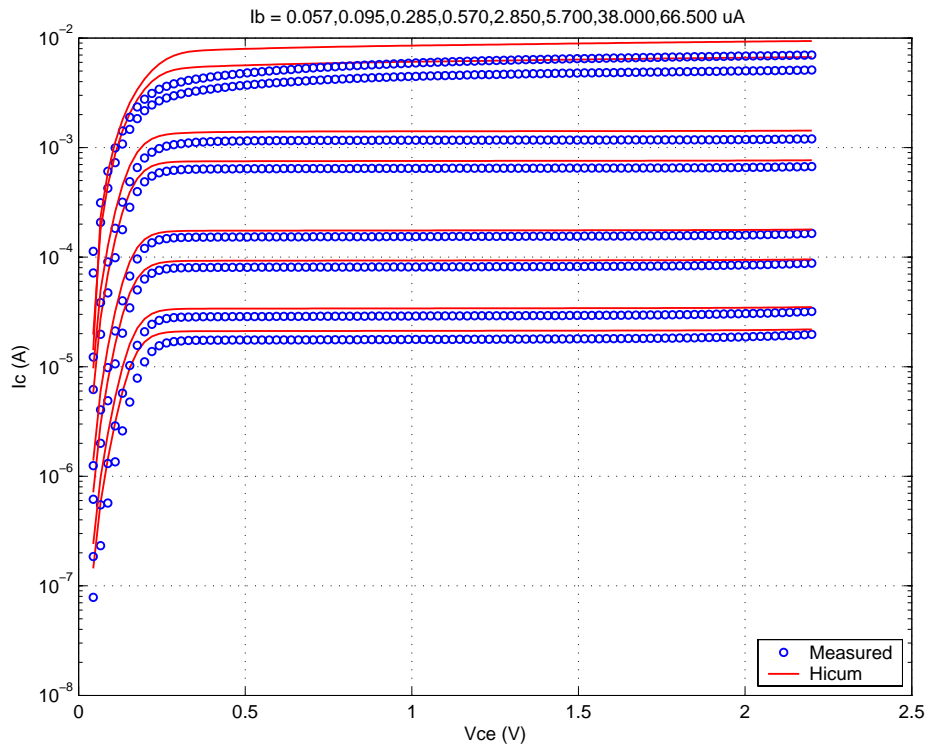


FIGURE 5.60 F_T vs. I_C : MV 0.15x0.76x10_122

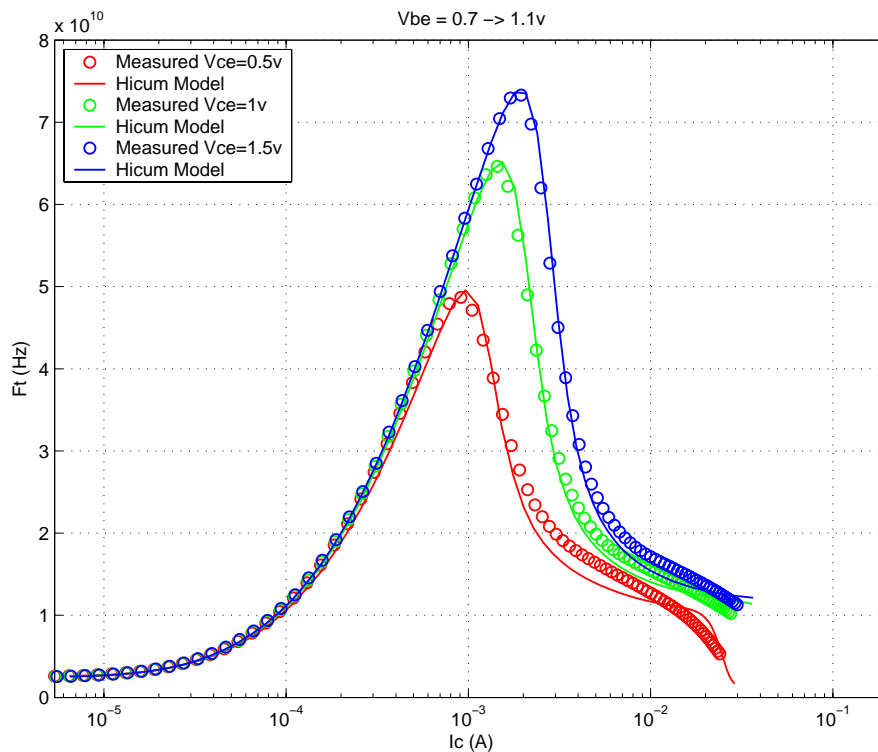
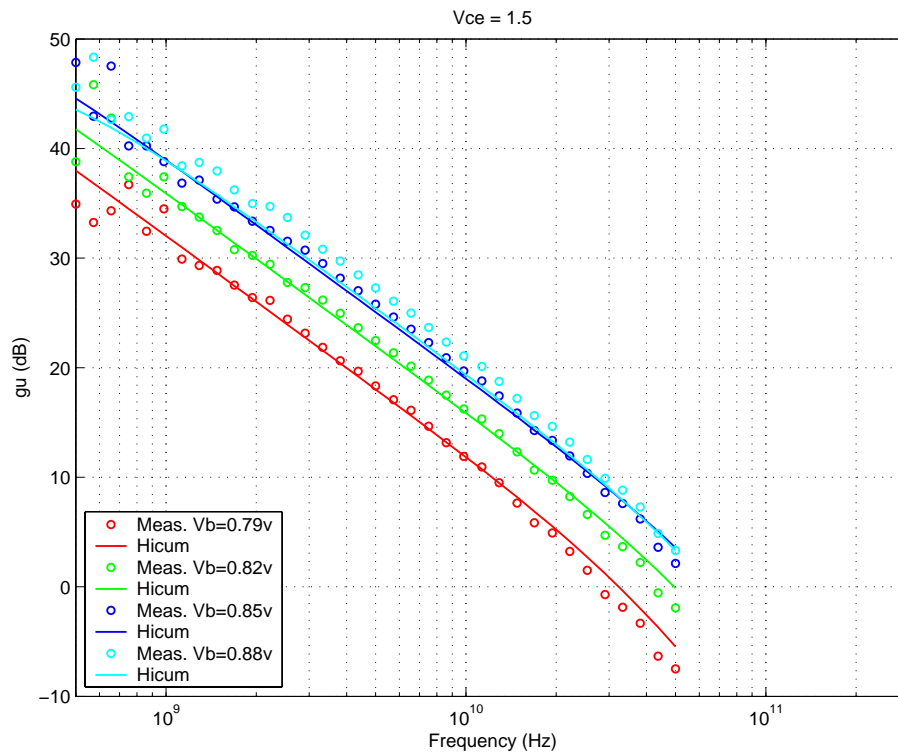


FIGURE 5.61 Power Gain vs. Freq: MV 0.15x0.76x10_122



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FIGURE 5.62 Y-parameters vs. FREQ: MV 0.15x0.76x10_122

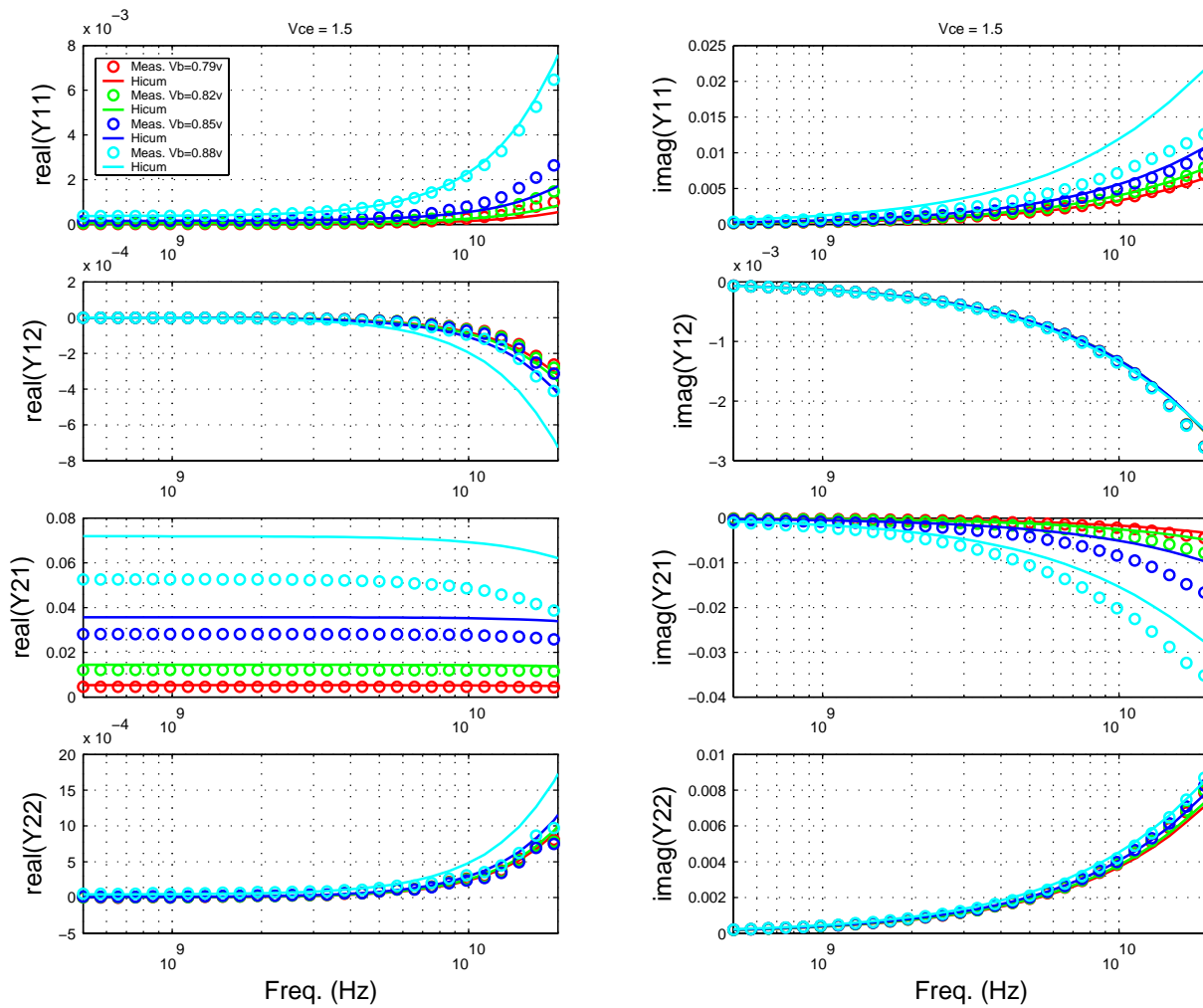


FIGURE 5.63 Gummel Plot MV 0.15x10.16x1_121

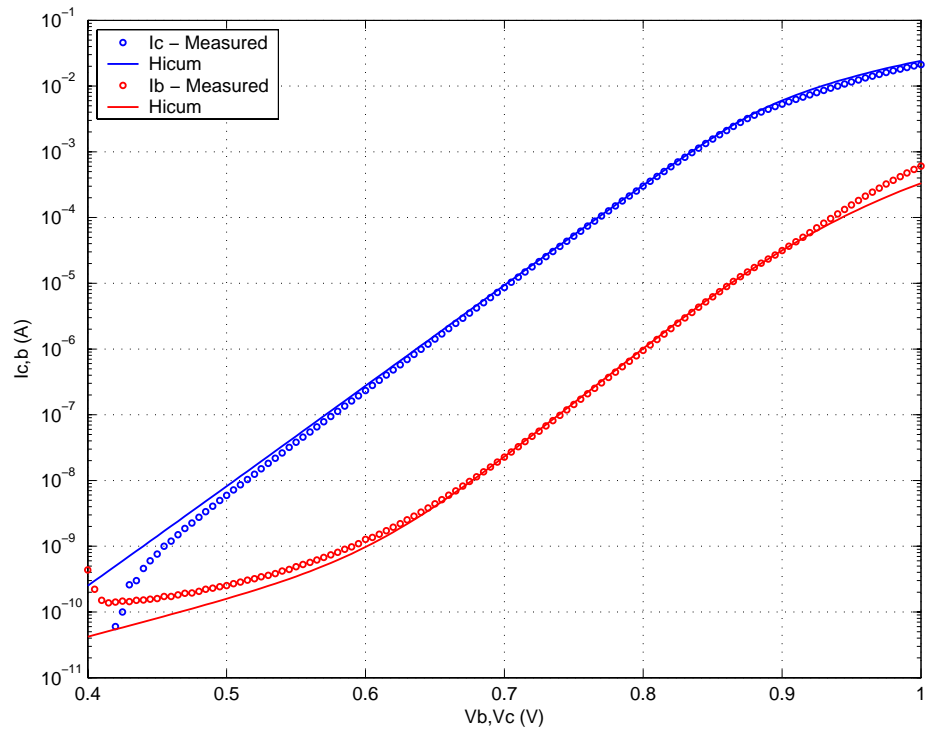
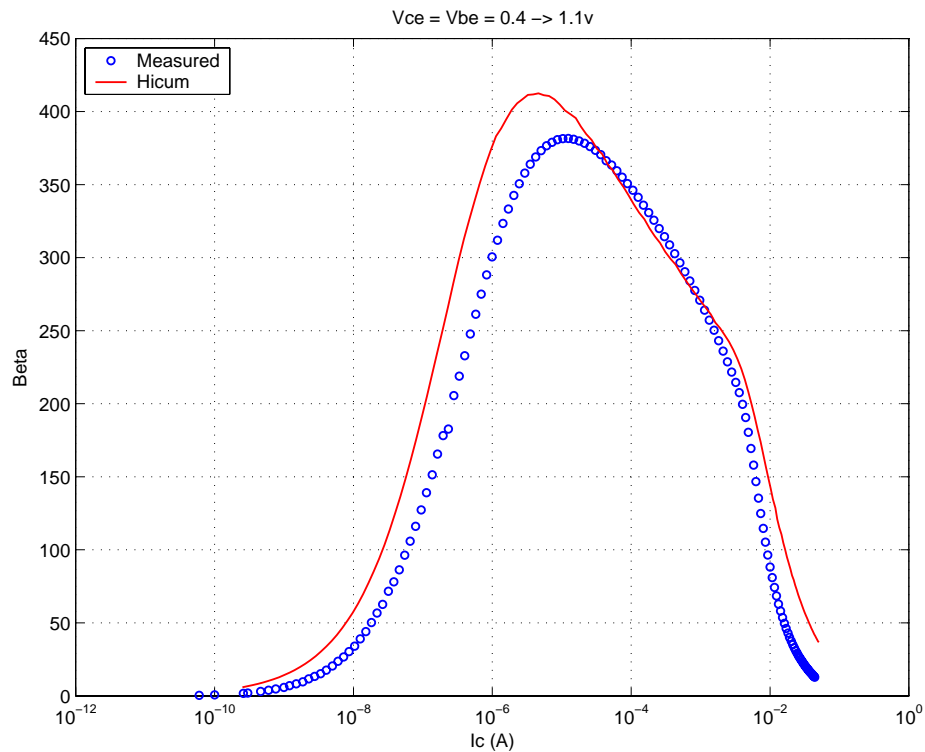
FIGURE 5.64 Beta vs. I_c : MV 0.15x10.16x1_121

FIGURE 5.65 I_C vs. V_{CE} at constant I_B : MV 0.15x10.16x1_121

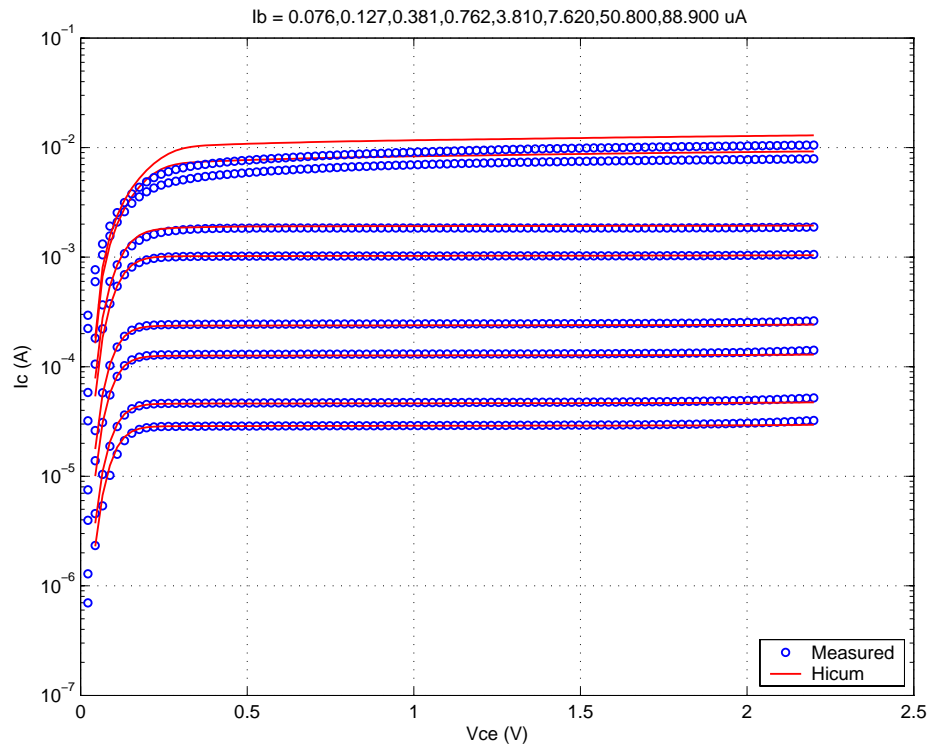


FIGURE 5.66 f_T vs. I_C : MV 0.15x10.16x1_121

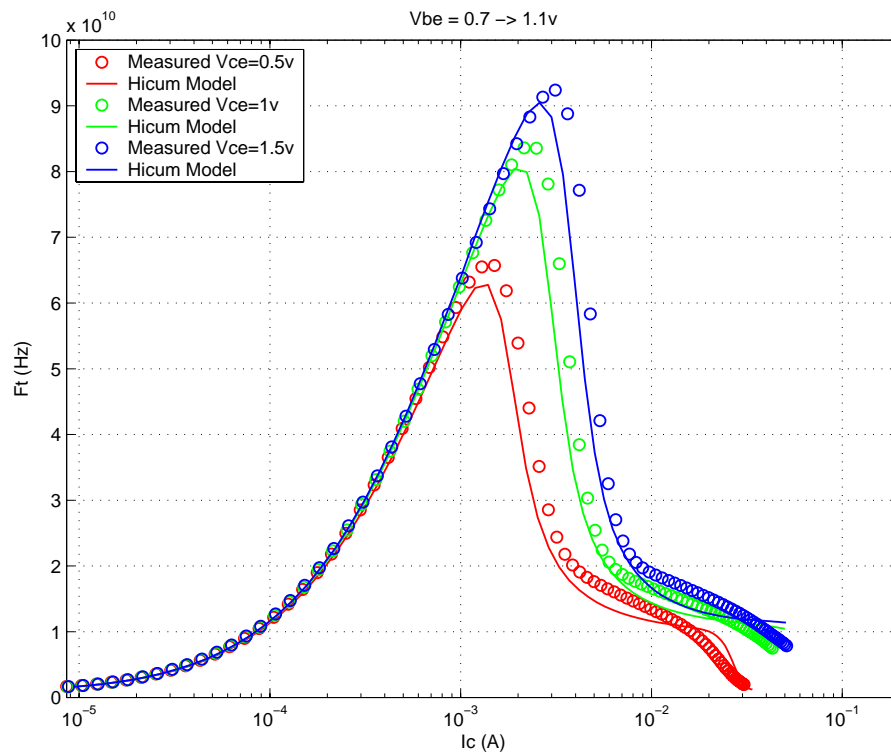
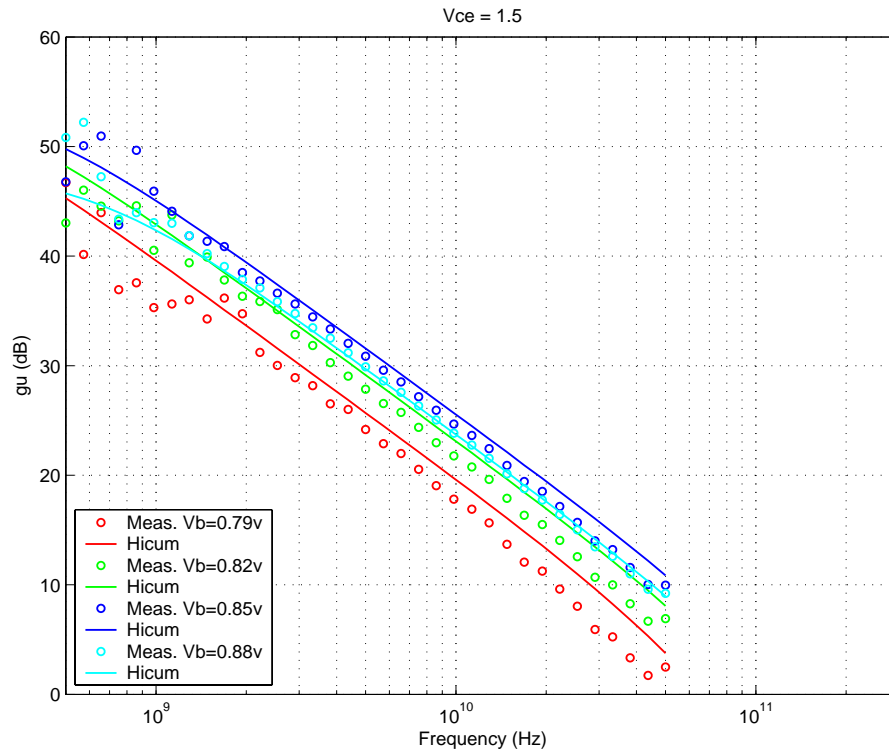


FIGURE 5.67 Power Gain vs. Freq: MV 0.15x10.16x1_121



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FIGURE 5.68 Y-parameters vs. FREQ: MV 0.15x10.16x1_121

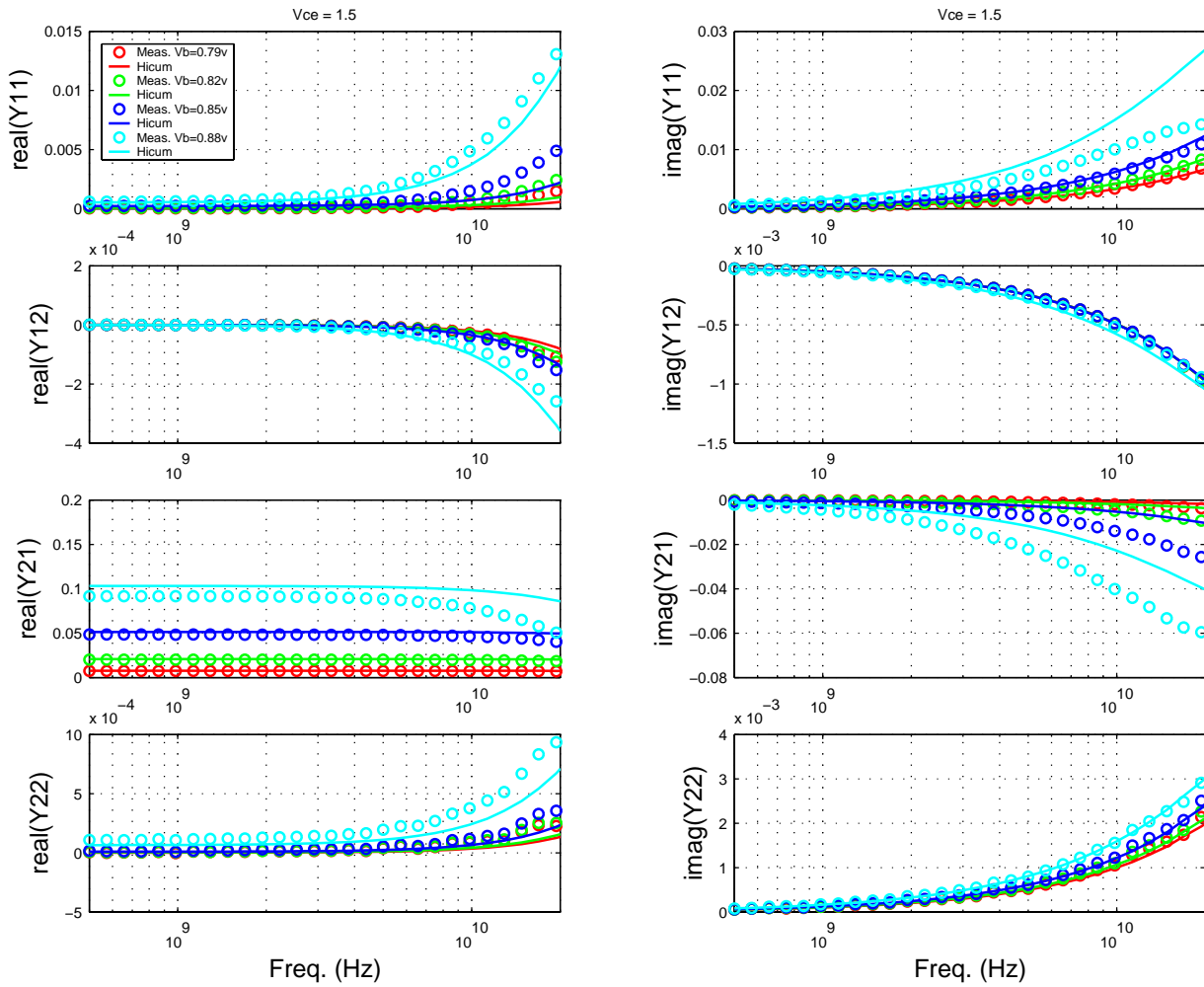


FIGURE 5.69 Gummel Plot MV 0.15x10.16x1_232

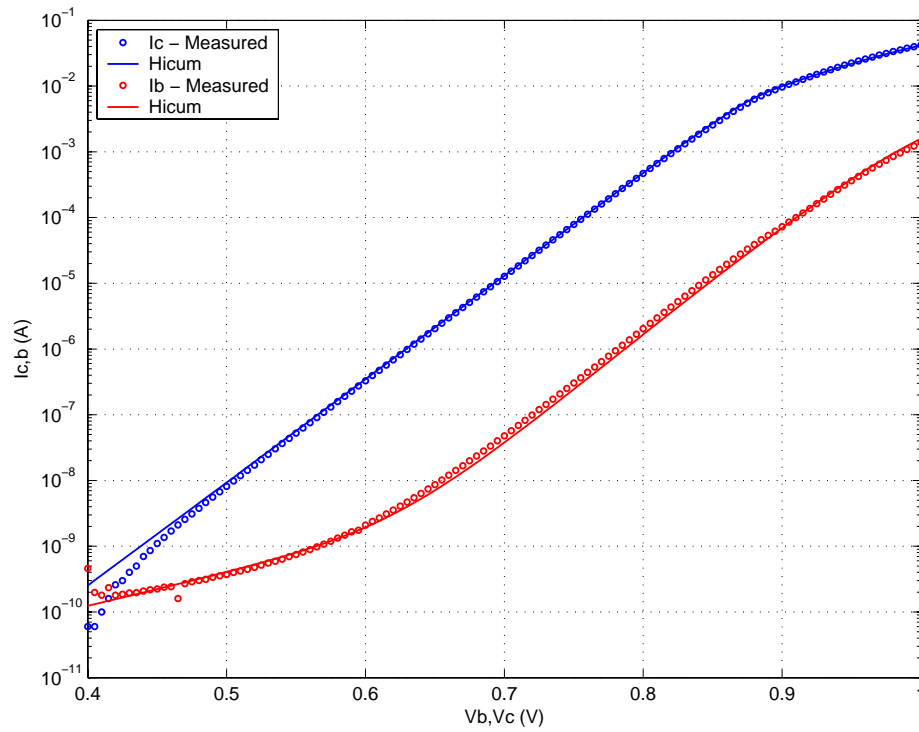
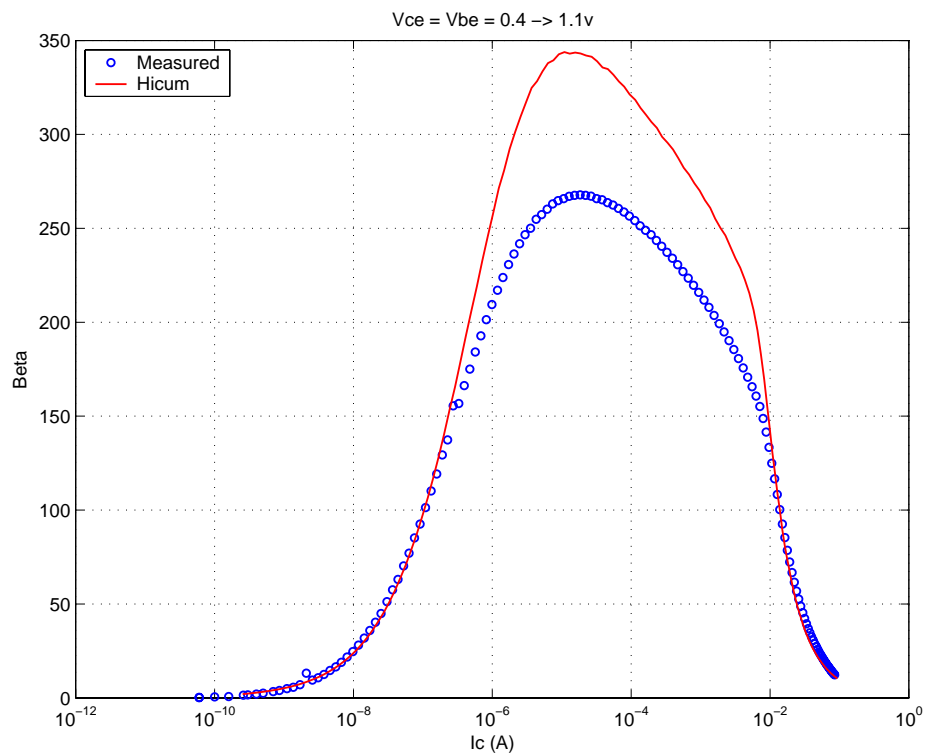
FIGURE 5.70 Beta vs. I_c : MV 0.15x10.16x1_232

FIGURE 5.71 I_C vs. V_{CE} at constant I_B : MV 0.15x10.16x1_232

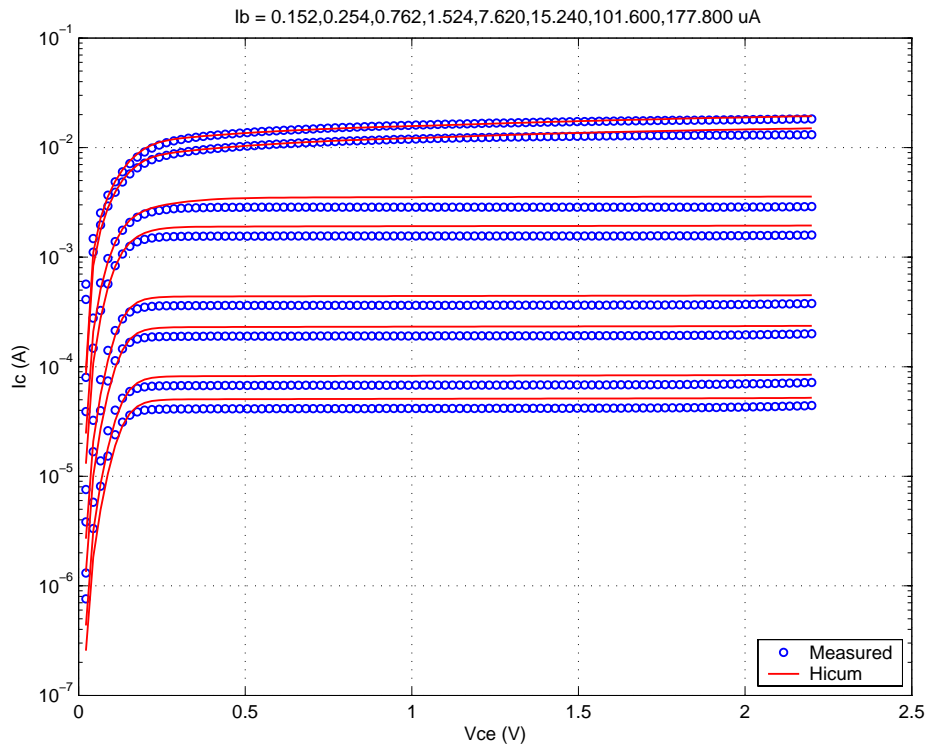


FIGURE 5.72 f_T vs. I_C : MV 0.15x10.16x1_232

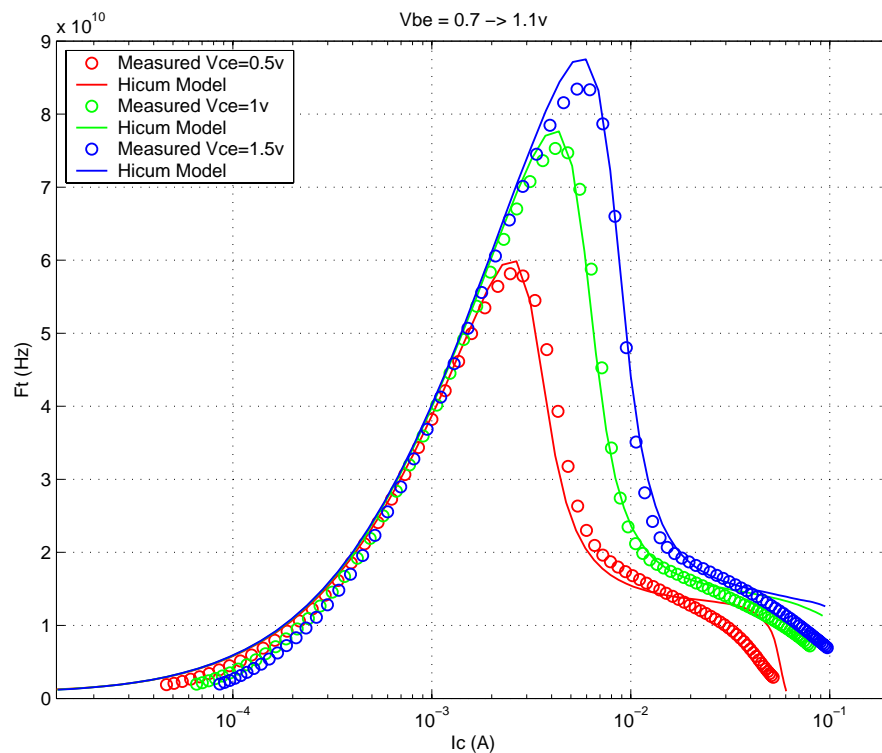
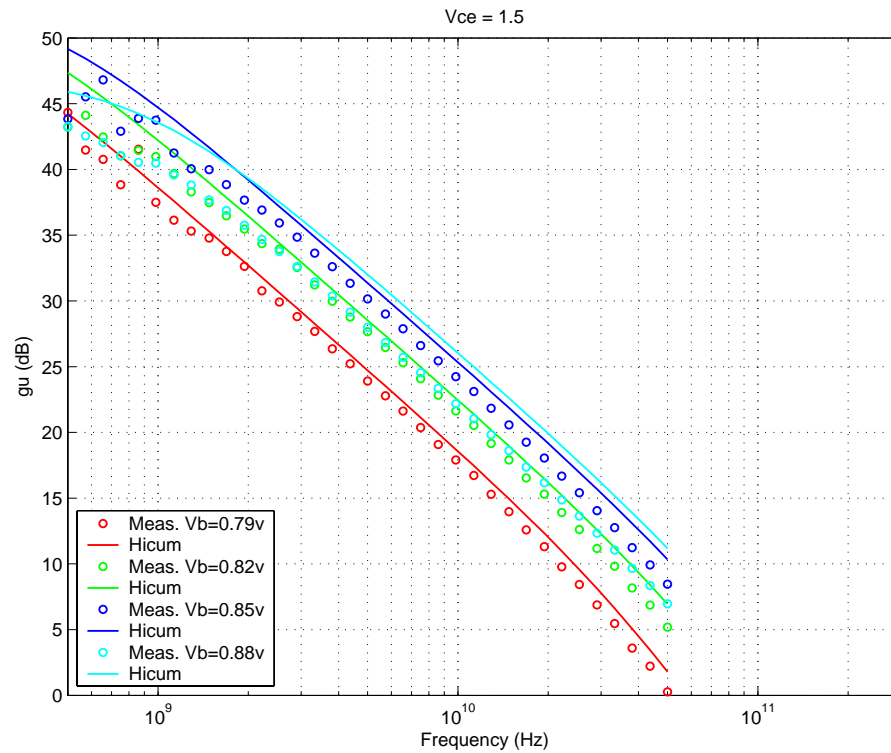


FIGURE 5.73 Power Gain vs. Freq: MV 0.15x10.16x1_232



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FIGURE 5.74 Y-parameters vs. FREQ: MV 0.15x10.16x1_232

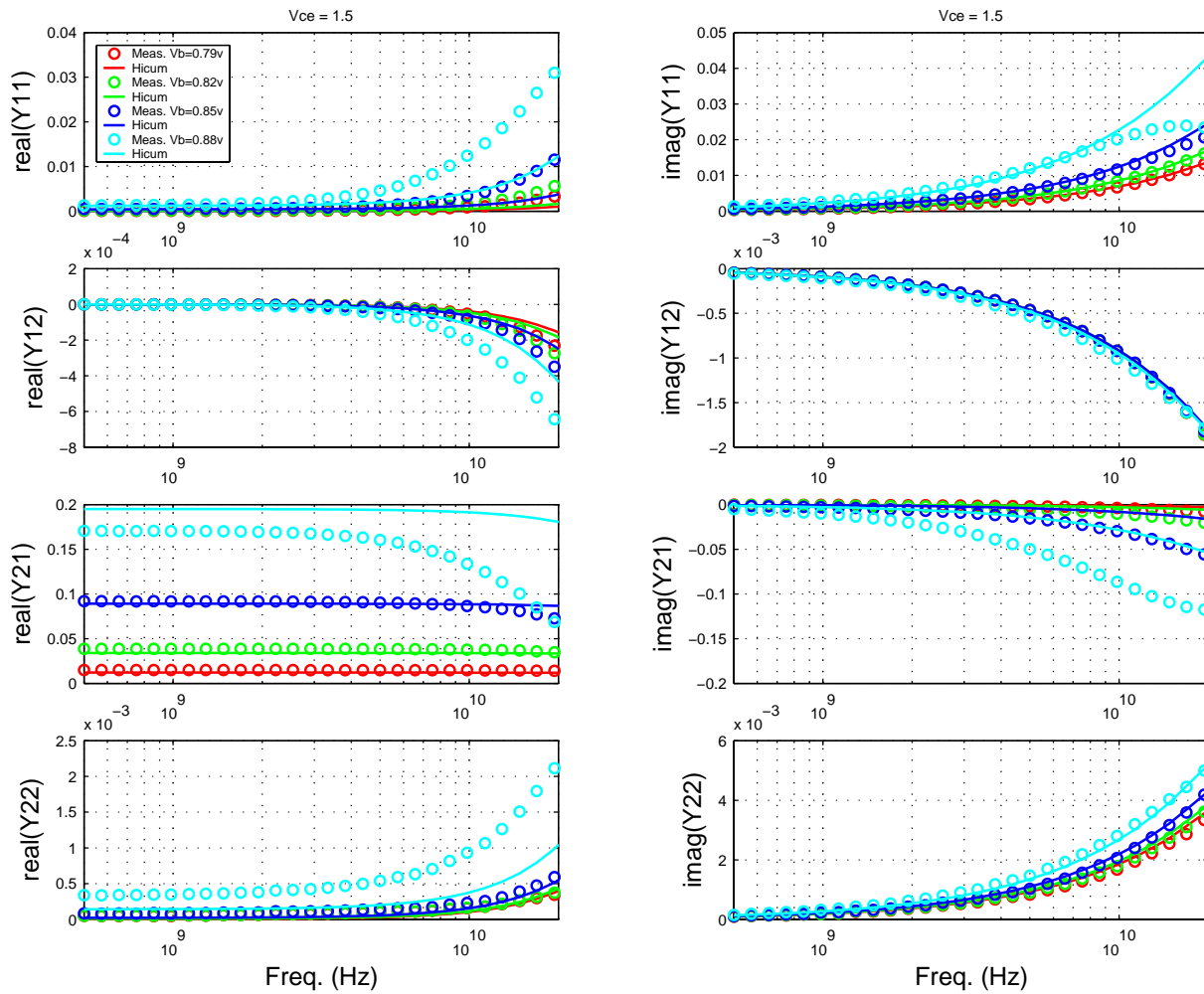


FIGURE 5.75 Gummel Plot MV 0.15x4.52x1_232

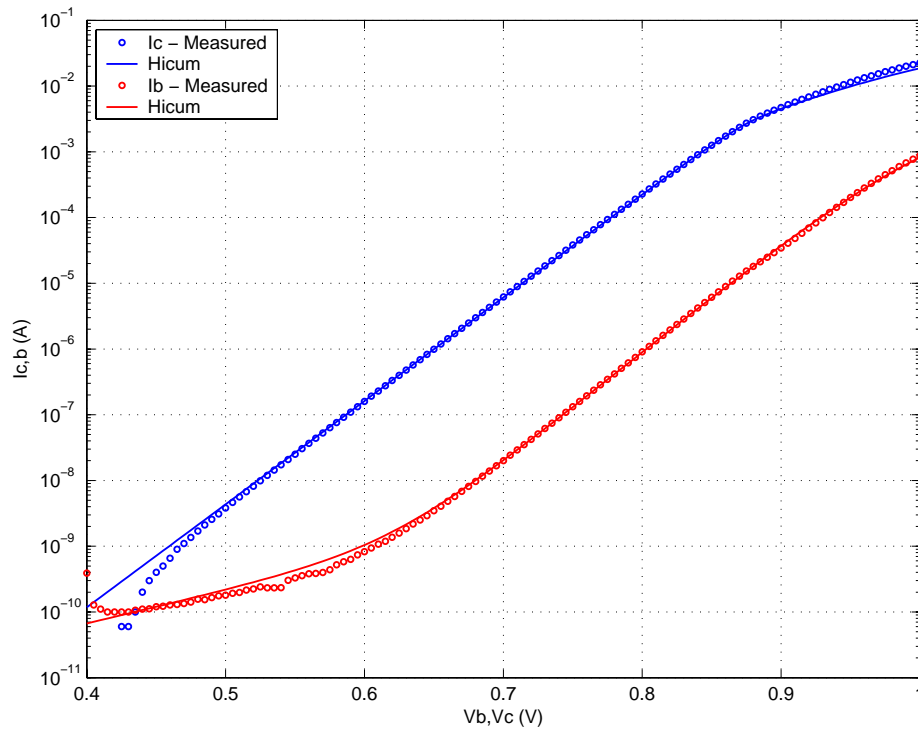
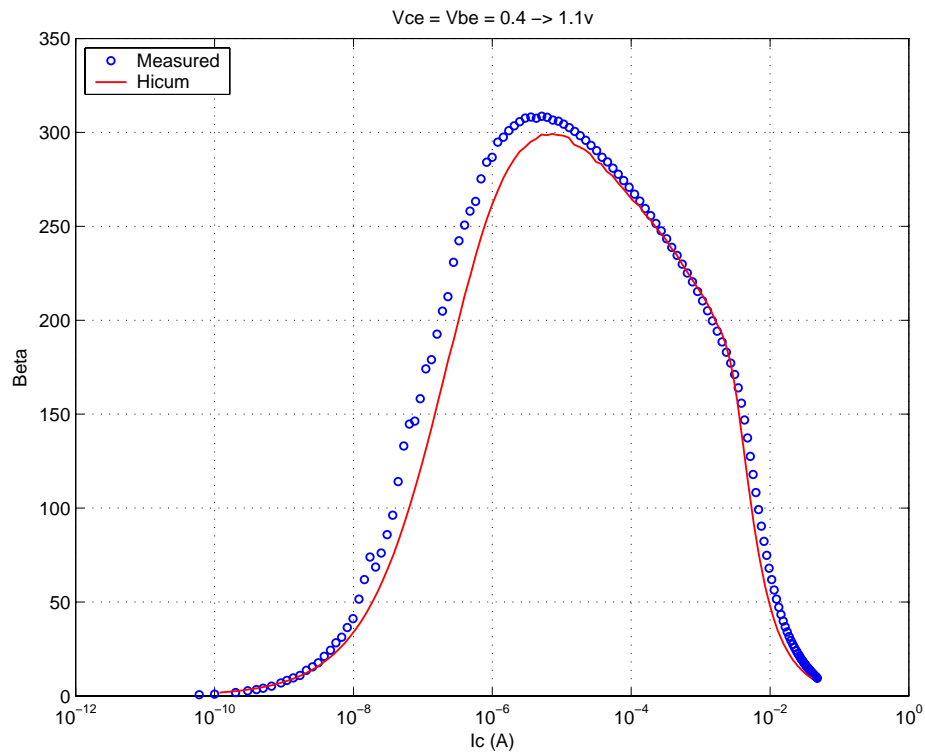
FIGURE 5.76 Beta vs. I_c : MV 0.15x4.52x1_232

FIGURE 5.77 IC vs. VCE at constant IB: MV 0.15x4.52x1_232

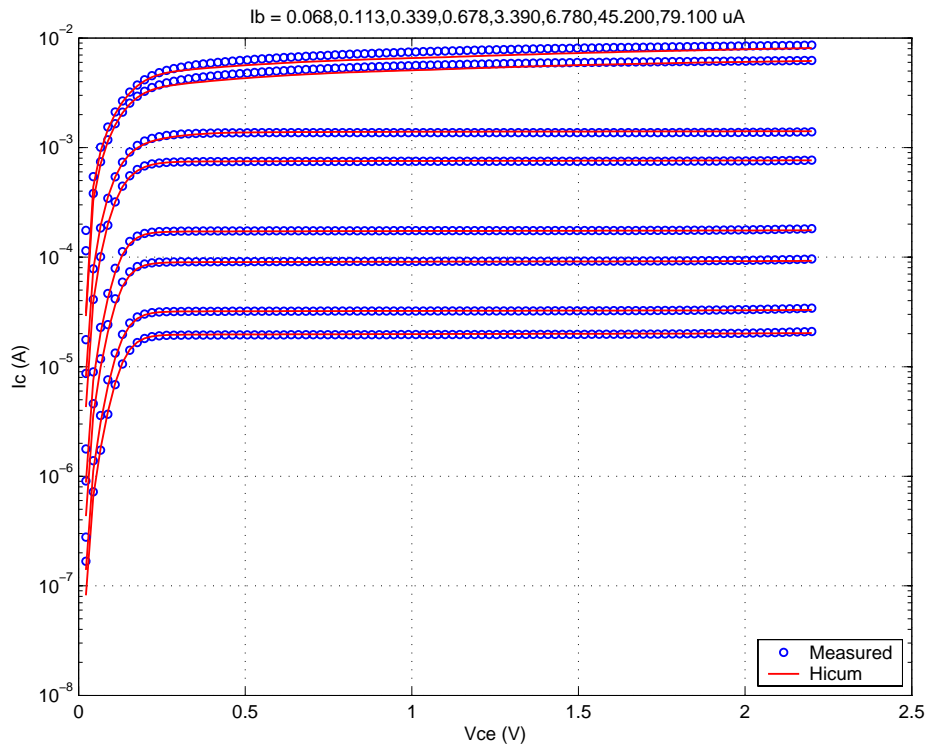


FIGURE 5.78 FT vs. IC: MV 0.15x4.52x1_232

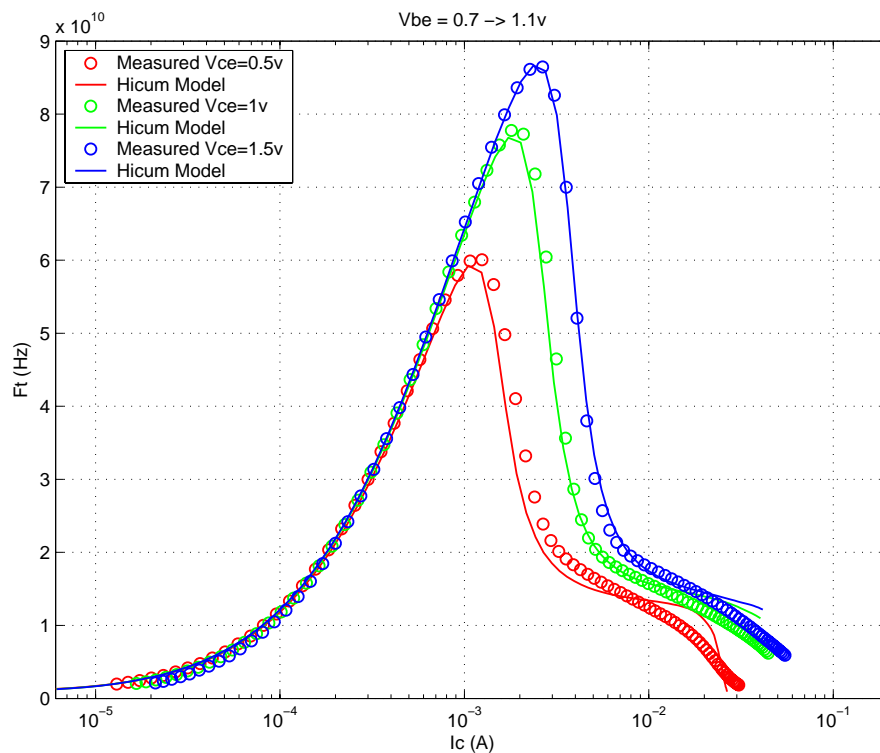
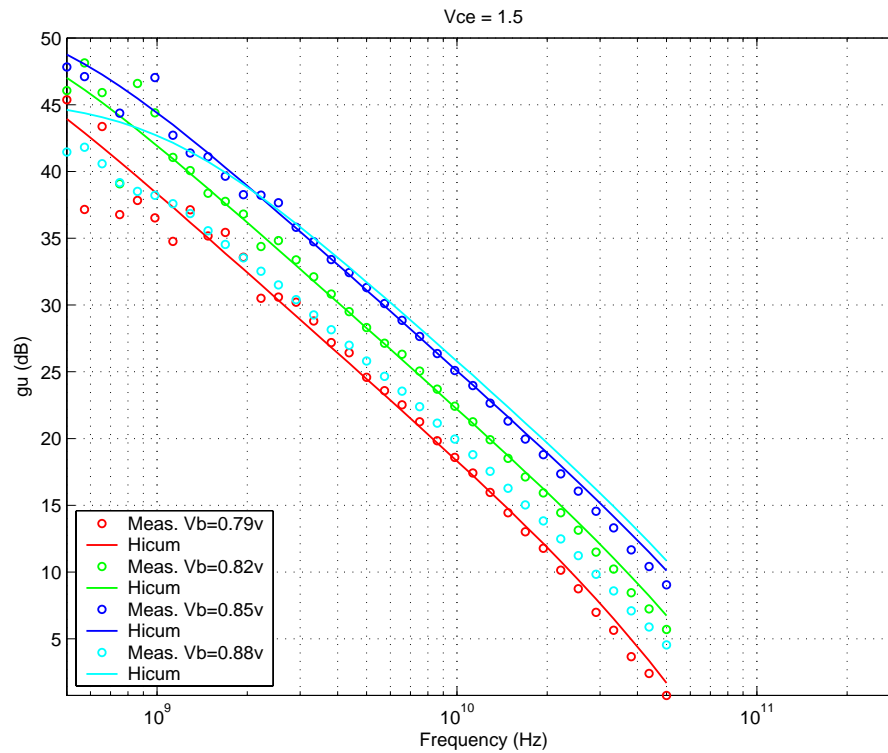


FIGURE 5.79 Power Gain vs. Freq: MV 0.15x4.52x1_232



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FIGURE 5.80 Y-parameters vs. FREQ: MV 0.15x4.52x1_232

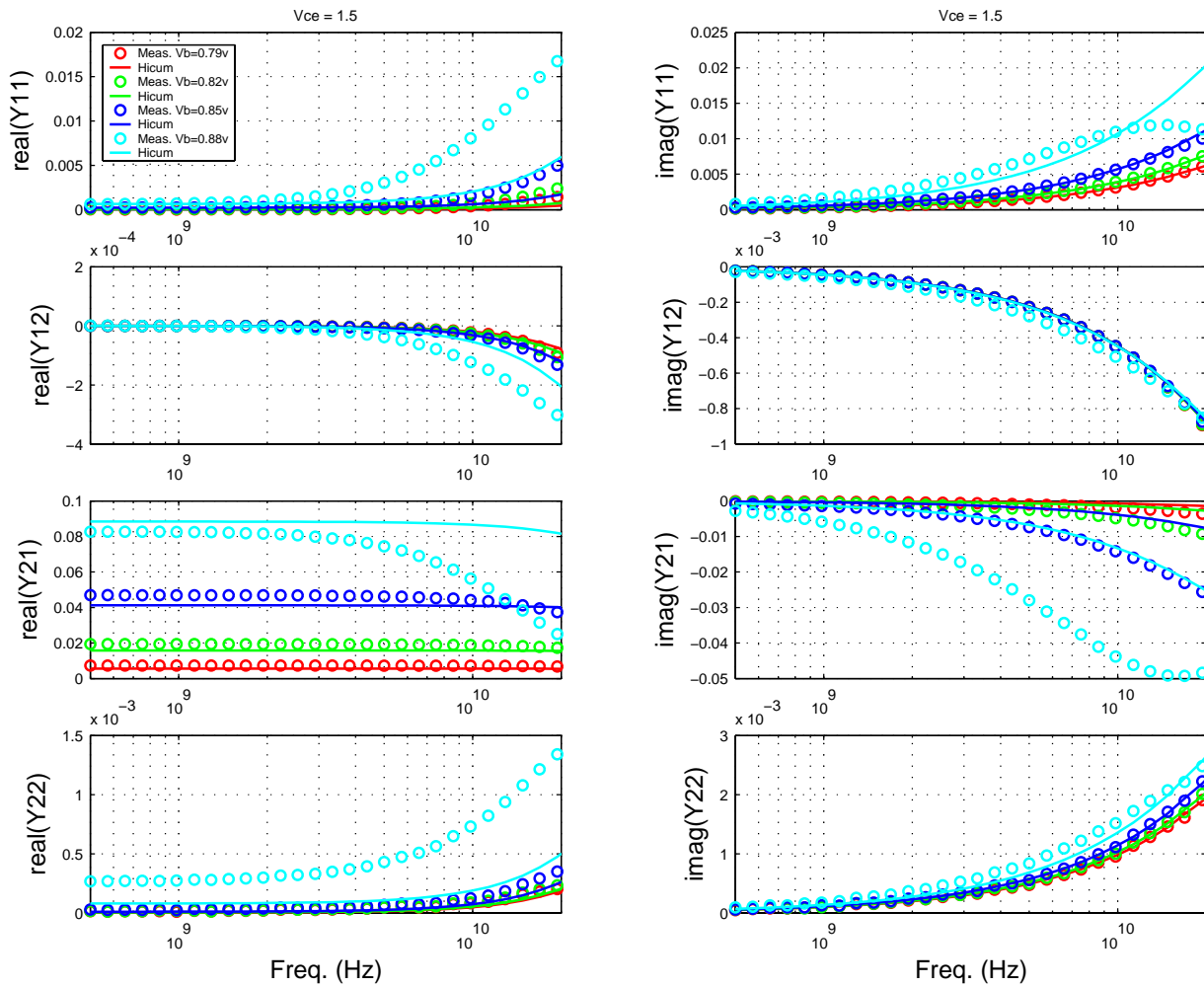


FIGURE 5.81 Gummel Plot MV 0.15x2.84x1_232

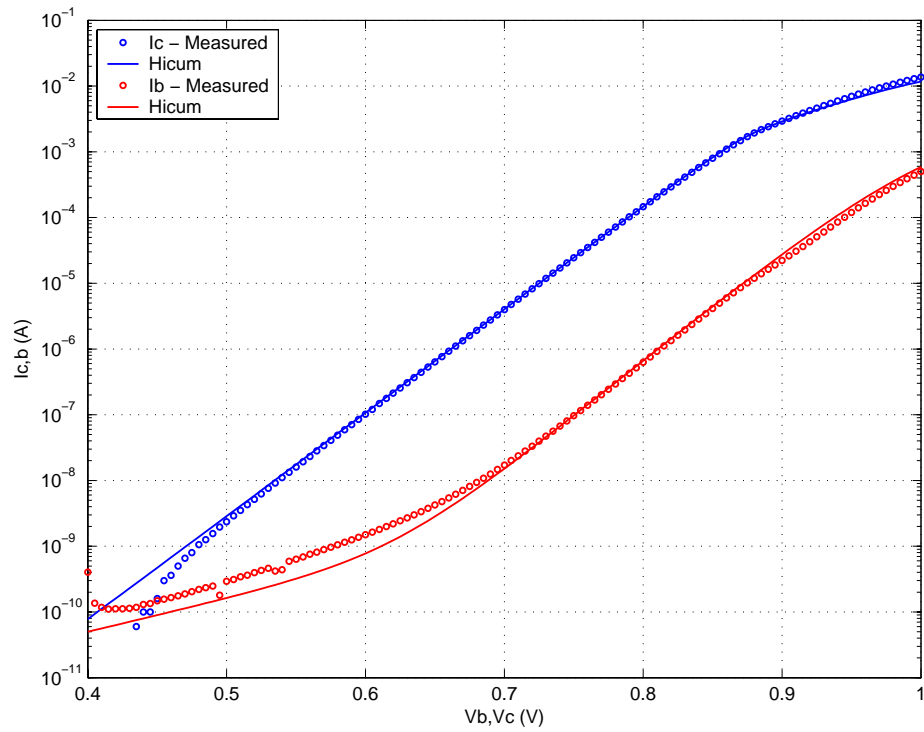
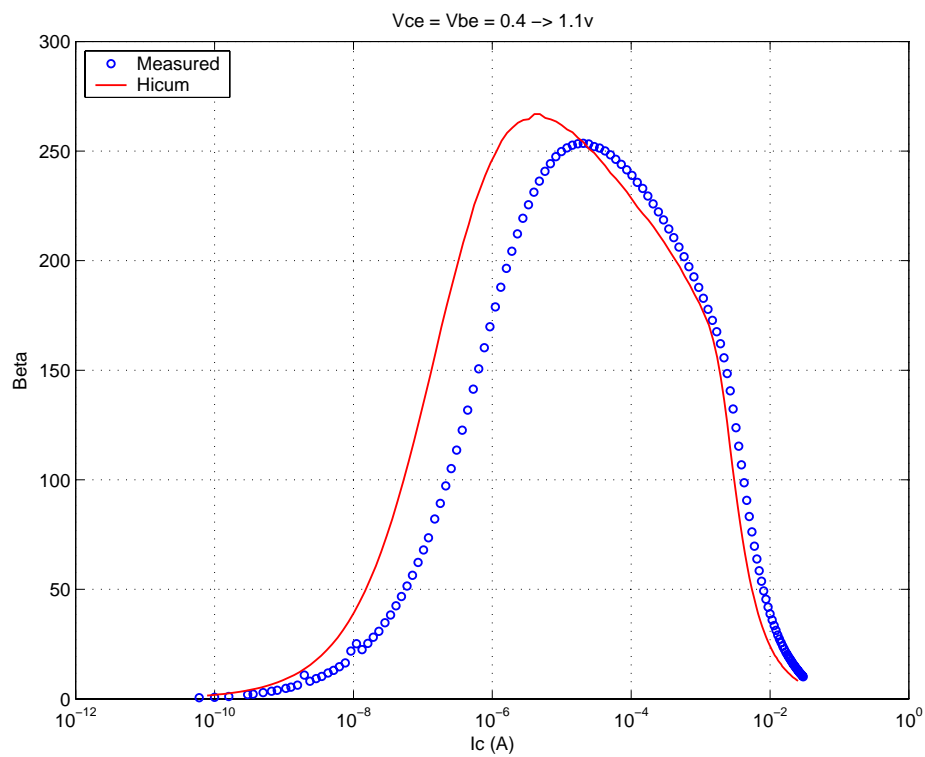
FIGURE 5.82 Beta vs. I_c : MV 0.15x2.84x1_232

FIGURE 5.83 I_C vs. V_{CE} at constant I_B : MV 0.15x2.84x1_232

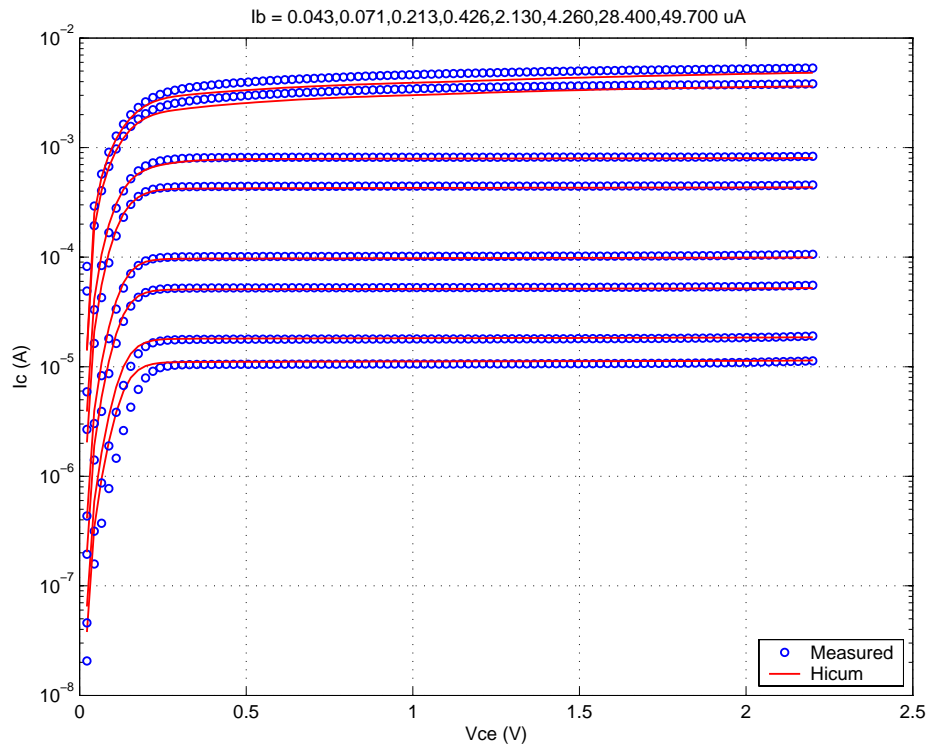


FIGURE 5.84 f_T vs. I_C : MV 0.15x2.84x1_232

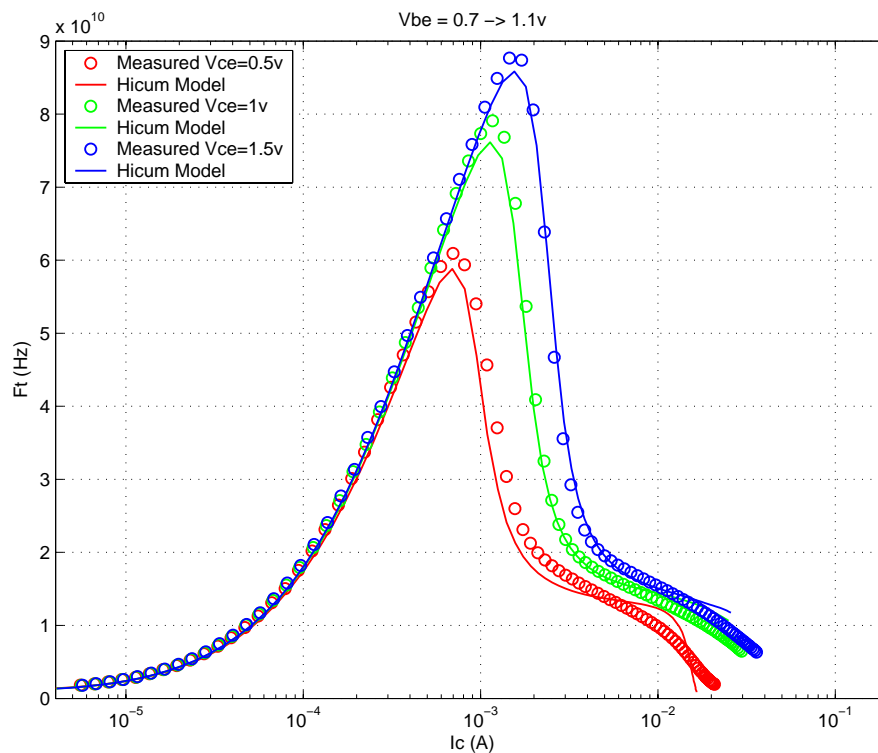
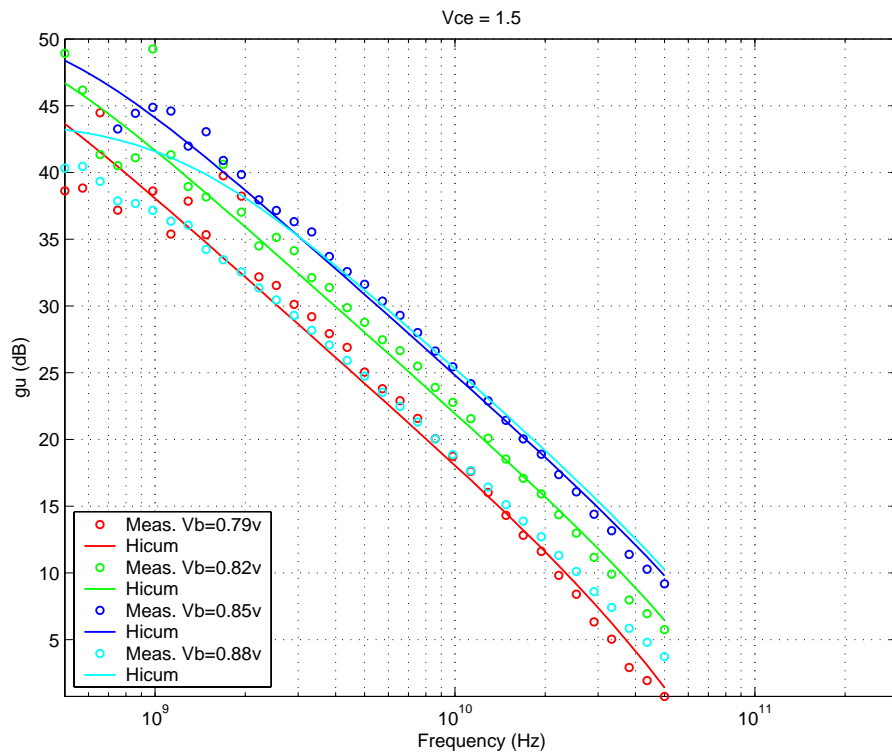


FIGURE 5.85 Power Gain vs. Freq: MV 0.15x2.84x1_232

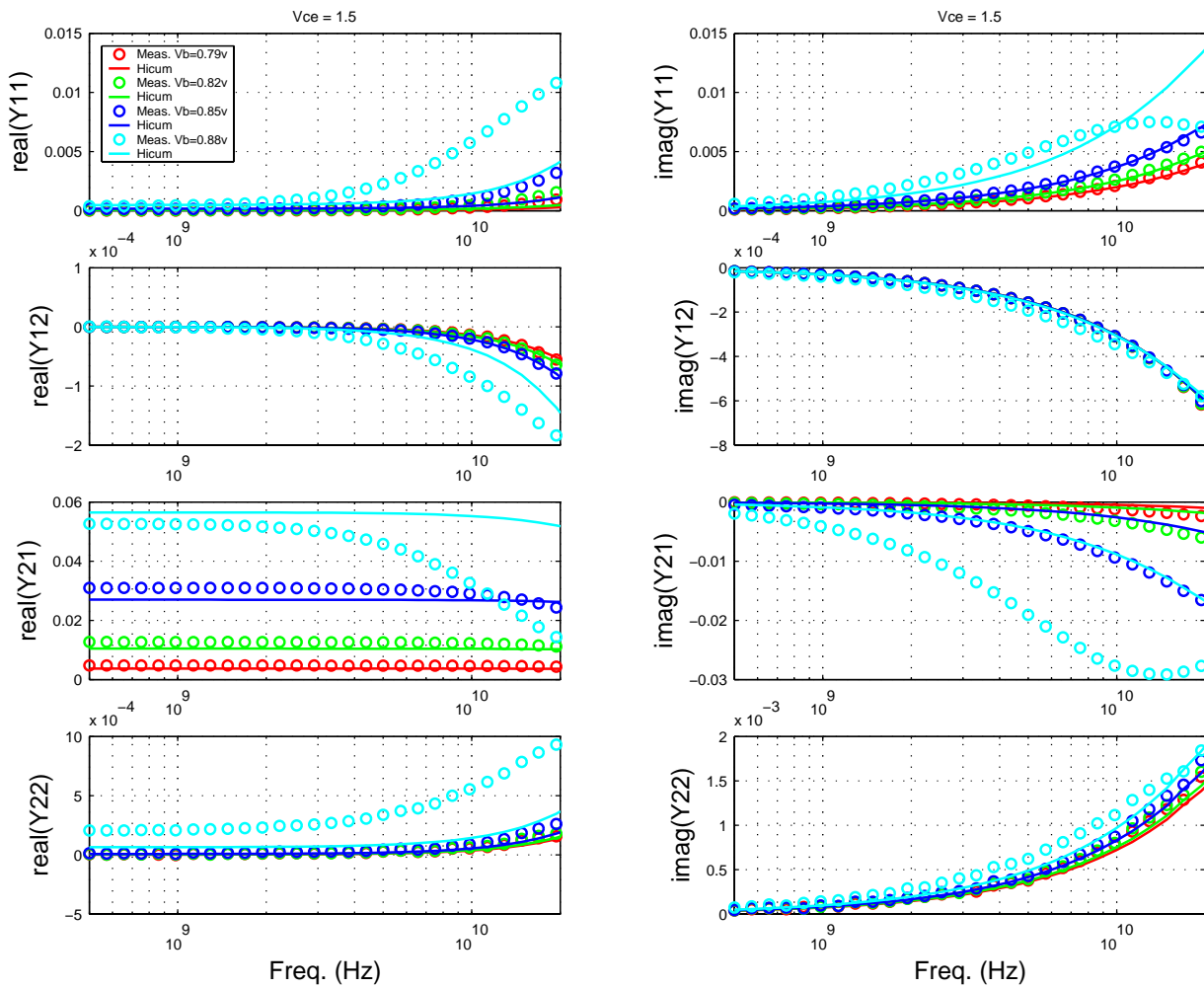


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FIGURE 5.86 Y-parameters vs. FREQ: MV 0.15x2.84x1_232



5.5 NPN Statistical and Corner Models

5.5.1 Statistical Model

A detailed description of the Backward Propagation of Variance (BPV) approach to statistical model generation is given in the MOSFET chapter. Only additional information exclusive to the NPN statistical models is given here. Unlike MOSFET models, the map between process and geometry parameters into model parameters is not well defined for NPN models. Mappings between process parameters, model parameters, and geometry parameters must be developed. The stand alone NPN models (Gummel-Poon, VBIC, Hicup, etc.) do not provide the physical correlation of the model parameters. Thus, a set of independent process parameters, rather than model parameters, are defined as the fundamental statistical variables in the simulator. Mappings for the process and geometry parameters into model parameters are developed based on device physics. A handful of process parameter variances are forward propagated in the BPV infrastructure based on expected variances at the process level such as Emitter-Poly CD variations. The remaining process parameter variances are directly BPV'd based on the variances in the ESPECs. A well conditioned system physically and mathematically results, guaranteeing precise simulation of the ESPEC variances and reasonable and consistent statistical simulation of non ESPEC quantities such as base resistance. The process parameters, the propagation technique, the affected model parameters, and target ESPECs for the Spice Gummel-Poon model (SGPM) are listed in Table 5.3. The statistically simulated ESPECs are listed in Table 5.5. Refer to the MOSFET chapter for statistical model usage guidelines.

TABLE 5.3 The Process Variables and the Affected Model Parameters in SGPM.

Process Parameters	BPV or FPV	Affected Model Parameters	Target ESPEC for BPV	Mismatch
Emitter Window CD	FPV	RE, RB, RBX, RC, CEOX, CJE, CJC, IS, ISE, BF (GP), IBEIS (Hicup)	NA	IC, BETA
Emitter Poly CD	FPV	CEOX, RBX	NA	
Base Ge doping concentration	BPV	IS (GP), C10 (Hicup)	Vbe at mod. Ic	
Base Boron doping concentration	BPV	CBE, RBI, RBX, IS (GP), C10 (Hicup)	Cbe	
Emitter Si/Poly interface property	BPV	BF (GP), IBEIS (Hicup), RE	Peak Beta	IB
Emitter/Base Junction Leakage	BPV	ISE (GP), IREIS (Hicup)	Beta @ low Vbe	IB @ low Vbe
Emitter doping concentration	BPV	RE, BF (GP), IBEIS (Hicup)	Ic @ Vbe=1.1v	
Substrate doping concentration	BPV	CJS	Ccs	
Base width	BPV	RBI, TF (GP), T0 (Hicup)	Ft of LV & HV dev.	
Local Collector Implant (LV dev.)	BPV	CJC of LV dev.	CBC of LV dev.	
Local Collector Implant (MV dev.)	BPV	CJC of MV dev.	CBC of MV dev.	

5.5.2 Centering

Refer to section 2.6.1 for centering within the BPV framework. The NPN model is extracted from a golden die which measures very close to the nominal of the ESPECs. As a result, the model parameter variation needed to exactly align the model to the nominal ESPECs is small. The simulated NOM ESPECs are listed in Table 5.6.

5.5.3 Corner Models

The goal of the corner models are to capture the device electrical performance limits through appropriate variation of the process parameters. Slow and fast corners are provided. Details of the corner models are given in Table 5.4. All the NPN ESPEC limits can not be captured with 2 corners. The target ESPEC parameters for the corner models are I_C , BETA, and F_t . The C_{BE} and C_{CS} ESPECs are also aligned to the ESPECs in the corner model. C_{BC} variation in the corner models is reduced from the ESPEC limit in order to retain consistent and physical F_t prediction. The verification of the simulated corner ESPECs are listed in Table 5.5.

TABLE 5.4 Corner model specifications

	FAST	SLOW
Emitter resistance	Component 1 is higher due to lower I_b (high Beta); Component 2 is lower due to higher emitter doping. Net is ~15% lower	Component 1 is lower due to higher I_b (low Beta); Component 2 is higher due to lower emitter doping. Net is ~15% higher
Extrinsic base resistance	Component 1 is lower (Nom. - 1σ link dist.); Component 2 is higher due to lower base doping (low Cbe). Net is ~10% higher	Component 1 is higher (Nom. + 1σ link dist.); Component 2 is lower due to higher base doping (high Cbe). Net is ~10% lower
Intrinsic base resistance	Component 1 is higher due to shorter base width; Component 2 is higher due to lower base doping (low Cbe). Net is 30% higher	Component 1 is lower due to longer base width; Component 2 is lower due to higher base doping (high Cbe). Net is 30% lower
Base emitter junction cap.	90% of NOM case	110% of NOM case
Base collector junction cap.	Max. case of Cbc	Min. case of Cbc
Collector substrate junction cap.	Min. case of Ccs	Max. case of Ccs
Intrinsic collector resistance	~15% lower; aligned to higher collector doping (higher Cbc)	~15% higher; aligned to lower collector doping (lower Cbc)
Collector saturation current	Min. case of V_{be} for fixed and moderate I_c	Max. case of V_{be} for fixed and moderate I_c
Base current	Max. case of beta (lower I_b)	Min. case of beta (higher I_b)
Base width	Smaller; aligned to max. F_t E-spec.	Larger; aligned to min. F_t E-spec.

TABLE 5.5 E-spec. vs. Model (Long transistor - 0.15x10 μ m emitter with 122 configuration)

Device	Espec Name (unit)	Slow			Nom			Fast		
		Espec	Corner	Stat	Espec	Corner	Stat	Espec	Corner	Stat
Low Voltage NPN Hicup (ln122_hicup)	β ¹	100.00	108.20	104.00	300.00	300.60	300.00	550.00	546.80	496.00
	c_{bc} ² (fF)	15.60	16.35	16.40	17.10	17.17	17.10	18.60	18.10	17.80
	c_{be} (fF)	22.00	22.00	22.10	20.00	20.00	20.00	18.00	18.00	17.90
	c_{cs} (fF)	17.50	17.56	17.60	14.60	14.65	14.50	11.70	11.74	11.40
	f_t (GHz)	180.00	179.10	179.00	200.00	200.00	200.00	220.00	219.20	221.00
	i_c (uA)	4.00	4.10	4.30	10.00	10.05	9.94	16.00	15.82	15.60
	J_c^3 (Pk. Ft)		5.36	4.29	5.51	5.51	5.57		6.29	6.86
	f_{max} ⁴ (GHz)		186.10	167.00	180.00	180.60	181.00		174.90	195.00
	bv_{ceo} ⁵ (V)	2.40	2.26	2.41	2.00	1.89	1.91	1.60	1.53	1.41

TABLE 5.5 E-spec. vs. Model (Long transistor - 0.15x10 μ m emitter with 122 configuration)

Medium Volt- age NPN Hicum (mn122_hicum)	beta ¹	100.00	109.20	113.00	300.00	300.50	297.00	500.00	563.70	481.00
	cbc ² (fF)	9.00	9.50	9.02	9.90	9.89	9.85	10.80	10.30	10.70
	cbe (fF)	22.00	22.00	21.80	20.00	20.00	20.00	18.00	18.00	18.20
	ccs (fF)	17.50	17.56	17.60	14.60	14.65	14.50	11.70	11.74	11.40
	ft (GHz)	65.00	65.14	64.90	75.00	75.00	74.50	85.00	84.47	84.10
	ic (uA)	4.00	4.07	4.39	10.00	10.00	9.88	16.00	16.49	15.40
	Jc ³ (Pk. Ft)		0.71	0.59	0.85	0.85	0.986		0.98	1.14
	fmax ⁴ (GHz)		168.10	157.00	170.00	171.10	171.00		172.10	185.00
	bvceo ⁵ (V)	3.30	3.80	3.84	2.80	3.18	3.23	2.30	2.77	2.62

Notes:

1. Beta: The E-spec is asymmetrical across the NOM case. The statistical model prediction is +/- 3 sigma and is thus symmetrical across NOM.
2. C_{bc}: Variation in the corner models is reduced from the E-spec limit in order to retain consistent and physical Ft prediction.
3. J_c is the current density (mA/ μ m²) at peak Ft. Only nominal E-spec is specified. This parameter is not a BPV targeted E-spec for corner or statistical model extraction.
4. F_{max}: Only nominal E-spec. is specified. Corner and statistical model predictions are shown for all cases. This parameter is not a BPV targeted E-spec. for corner or statistical model extraction.
5. BV_{ceo}: Gummel-Poon model does not include breakdown effects. Hicum model predictions are shown. This parameter is not a BPV targeted E-spec. for corner or statistical model extraction.

5.6 NPN Mismatch Model

Mismatch characterization is not available. A preliminary model based on local variation of process parameters of the previous generation of NPN technologies is provided in the design kit. The spacing between npns in the mismatch structures was 10 μ m.

5.7 Released Model Quality Assurance (QA)

A rigorous QA procedure is executed before any new model release. The geometry dependence of 9 key device parameters is examined for any non-physical behavior for all 3 cases: Nominal, Fast, and Slow. These parameters are listed in Table 5.6.

TABLE 5.6 NPN electrical parameters list examined as part of model release QA

Parameter	Description
BETA	Current gain
I _C	IC at Vbe=0.7v
Ft	Unity gain cut-off frequency
Fmax	Unity power gain cut off frequency
C _{BE}	Base-Emitter capacitance
C _{BC}	Base-Collector capacitance
C _{CS}	Collector-Substrate capacitance
R _E	Emitter Resistance
R _B	Base Resistance

Figures 5.87 through 5.88 illustrate the emitter length dependence of these 9 parameters.

FIGURE 5.87 QA Plots: LV 0.15x10.0_122

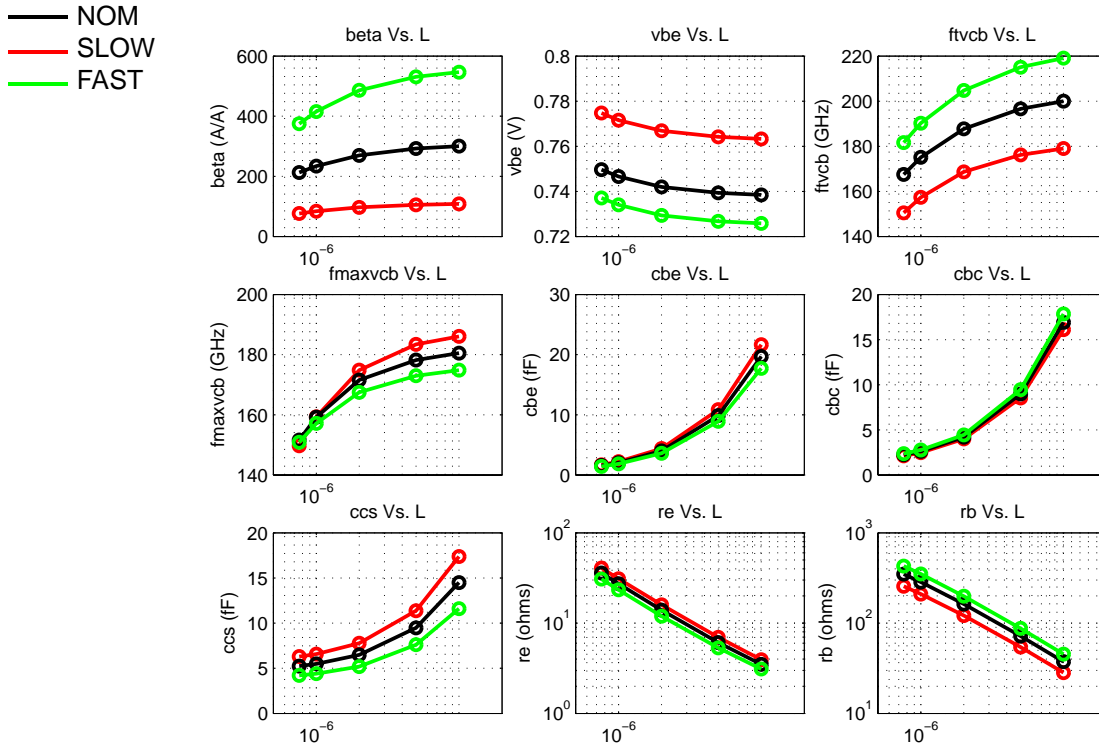
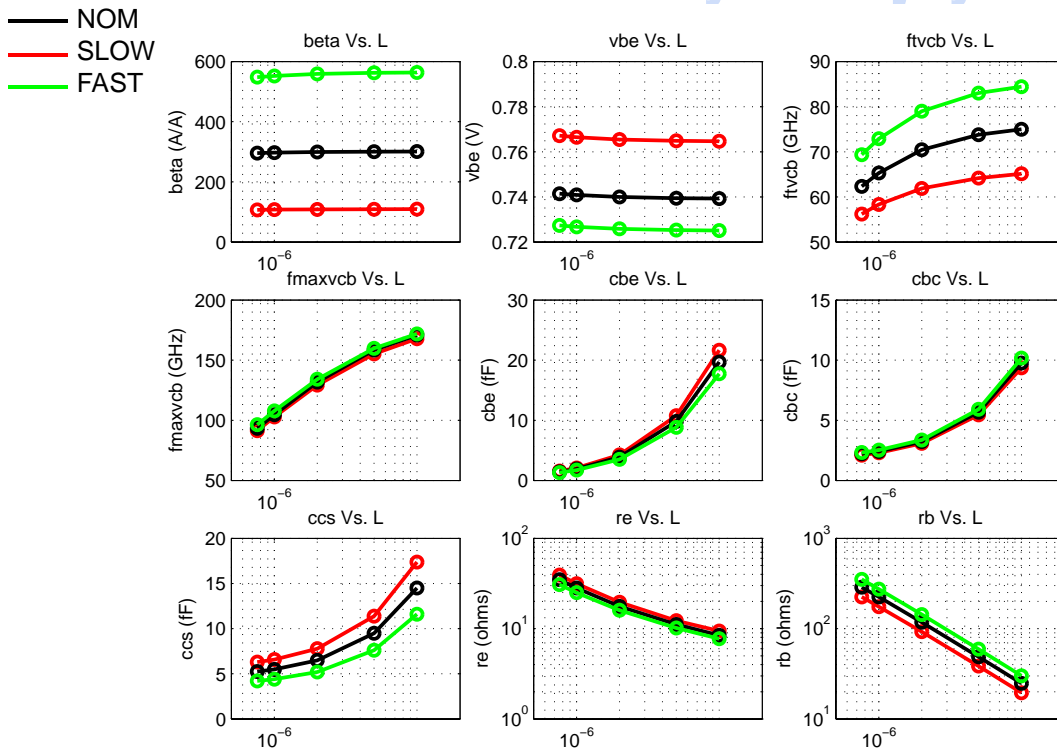


FIGURE 5.88 QA Plots: MV 0.15x10.0_122



5.8 Model Update History

5.8.1 Model Release 2.0

TABLE 5.7 NPN model specific updates in model release version v2.0

v6.0b update	Devices	Reason	Impact on user
Updated low-voltage (lnxxx) and medium-voltage (mnxxx) hicum models based on recent silicon	All	New models extracted from extensive set of test structures from more mature process	Improved accuracy
NOM Beta increased from 200 to 300	All	Align to recent silicon and updated E-spec.	Increased current gain
Peak Ft of the medium voltage npn increased from 70 to 85 GHz	MV	Align to recent silicon and updated E-spec.	Higher cut-off frequency for current gain
BVceo of medium voltage npn lowered to new E-spec (3v)	MV	Align to recent silicon and updated E-spec.	Lower breakdown voltage

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6.0 Vertical PNP

The vertical pnp is included in CA13/SBL13 design kits released after October 2006.

6.1 Device Description

The vertical PNP transistor formed by a p+ emitter, Nwell base, and psub collector is shown in Figure 6.1. There are four discrete vertical PNP transistors in the model library given in Table 6.1. The top layout view is shown in Figure 6.2.

FIGURE 6.1 Cross Section of the Vertical PNP

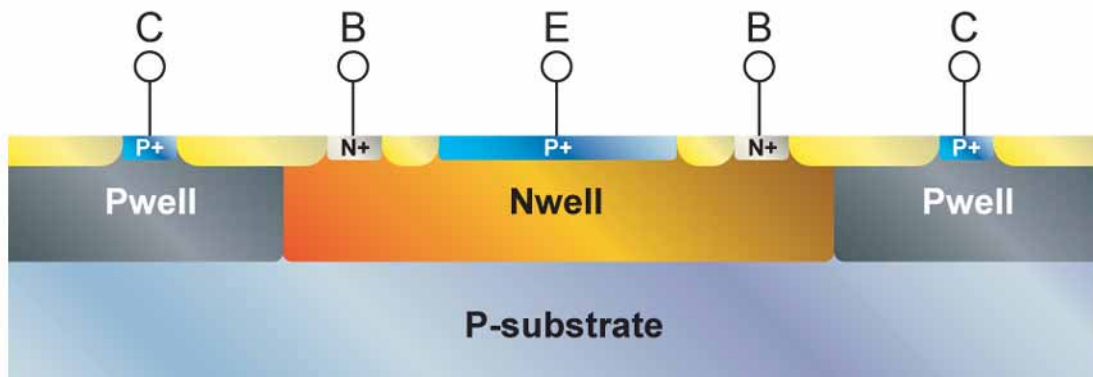
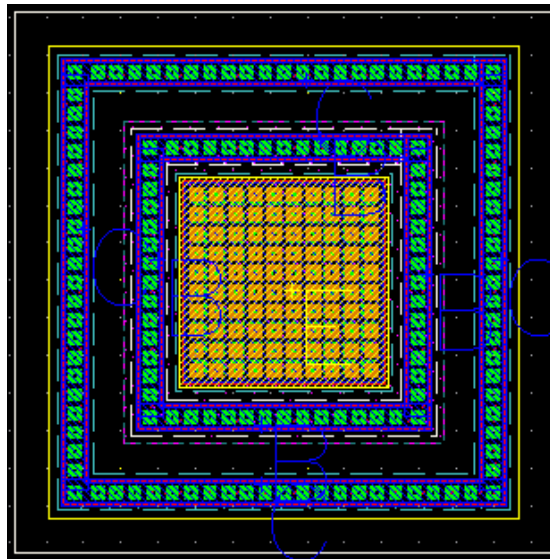


TABLE 6.1 VPNP Devices

Device Name	Emitter Area
PNPa	25x25 μm^2
PNPb	11x11 μm^2
PNPc	5.4x5.4 μm^2
PNPd	3x3 μm^2

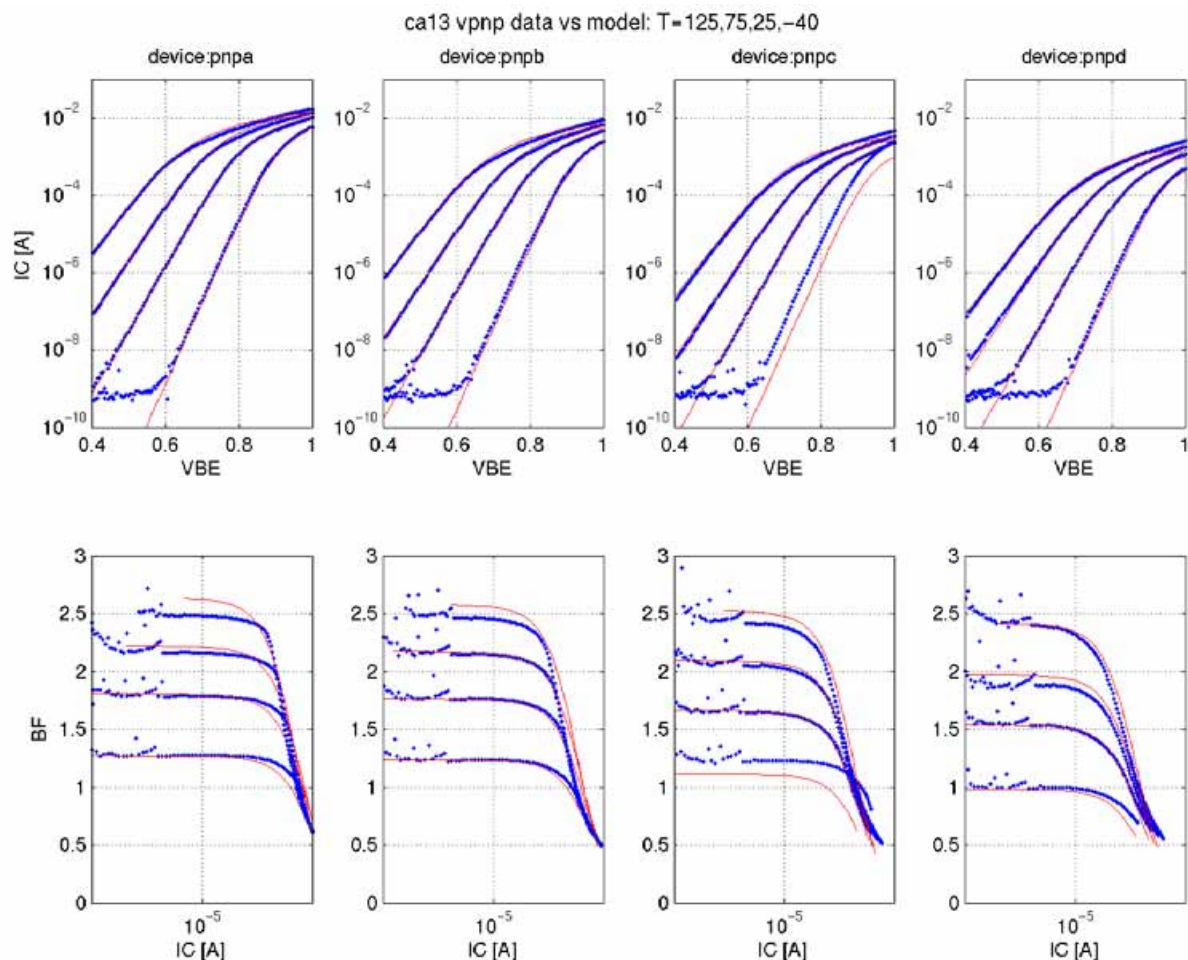
FIGURE 6.2 Top view of the vertical PNP transistor

6.2 Model Description

The VPNP is modeled with a standard Gummel-Poon model. Four discrete model cards are extracted for the four different emitter sizes given in Table 6.1.

6.2.1 Model Verification

Figure 6.3 displays vertical PNP performance across different temperatures. The -40 data for pnp_c is corrupt and will be re-measured at a future date.

FIGURE 6.3 Verification Plots for VPNP


6.2.2 VPNP Statistical and Corner Models

The primary process parameter that controls the statistical behavior of the VPNP is the Nwell doping. The current gain (β), saturation current (I_s), and Early Voltage (V_{AF}) are affected by the Nwell doping. See Section 13.0 for further explanation of the device interdependencies in the corner models and use of the X-Sigma corner models. Table 6.2 lists the VPNP specific ESPECs compared to simulated corner and statistical values.

TABLE 6.2 Espec, Corner and Statistical model comparison for VPNP

Device	name	units	slow			nomi			fast		
			Espec	Corner	Stat	Espec	Corner	Stat	Espec	Corner	Stat
pnpa	beta ($I_e=10\mu A$)		1.3	1.3	1.3	1.8	1.8	1.8	2.3	2.3	2.3
	Va	V	100	93	94		196	194			

6.2.3 VPNP Mismatch Models

Mismatch is not supported for the VPNP device.

6.3 Model Update History

TABLE 6.3 PNP models specific updates in model release version v1.8

v1.8 update	Devices	Reason	Impact on user
Initial Release	VPNP		

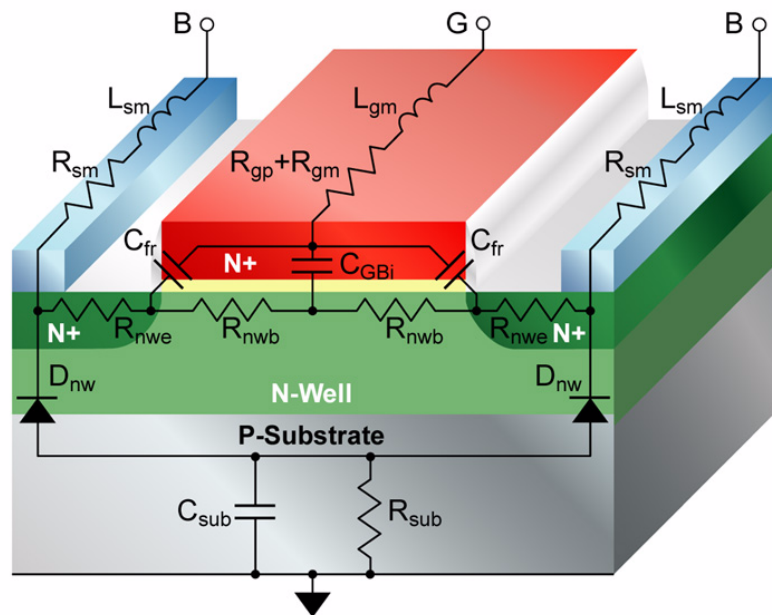
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7.0 MOS Varactor Model

7.1 Device Description

The MOS varactor is formed by 3.3V gate-oxide over Nwell, with N+ implant at both source/drain regions to form ohmic contacts with varactor Nwell region. The cross section of this device is shown in Figure 7.1. The device is the same in cross section to the poly capacitors.

FIGURE 7.1 MOS Varactor Cross Section: n+ poly to Nwell capacitor as MOS Varactor



7.1.1 Layout Options

The MOS varactor pcell offers several design parameters to allow optimization of device performance. Table 7.1 provides detailed information on the pcell variables. The gate width (W_g) and length (L_g) control the capacitance (C) tuning range and quality factor (Q). Increased W_g and L_g provide higher tuning range as the contribution of fixed capacitance is reduced. However, the Q is reduced due to increased Nwell and poly gate resistance. Section 6.3 provides further validation of C vs. Q trade-offs.

The C is scaled through arraying the device as *slices* (N_s) and *fingers* (N_f). There is no break in the poly or metal 1 between successive slices. There is a break in the active to allow for metal 1 contact to the poly gate in order to minimize the gate resistance. Two different *metal style* options (metal 1 and metal 2) are offered for the MOS varactor in the CA13HC design kit. The metal one option is shown in Figure . Metal 1 fingers are drawn parallel to the gate poly and Nwell contacts. The metal 2 option exists as *unconnected* and *connected*. The metal 2 *connected* option is shown in Figure . In the *unconnected* option, the vertical metal bars are removed. In the metal 2 option, the metal 2 fingers are drawn orthogonal to the metal 1 fingers with vias dropped to connect to the gate and Nwell metal 1 fingers. The metal 2 option provides for lower metal resistance for larger

N_s layouts ($N_s > 5$) at the expense of increased parasitic metal 1 to metal 2 capacitance which degrades the tuning range.

TABLE 7.1 MOS Varactor Parameter Description

Variable	Description	Typical	Min		Max
			met 1	met 2	
L_g	gate length for each var_mos cell	0.5 μm	0.5 μm	0.36 μm	1 μm
W_g	gate width for each var_mos cell	3.0 μm	2 μm	2 μm	8 μm
N_s (slices)	number of slices which controls the number of var_mos cells in series	4	1	1	10
N_f (fingers)	number of fingers connected in parallel for each slices	scaled to give C	1	1	40
Metal Style	metal connection type	metal 1, metal 2, metal 2 connected			

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8.0 Resistor Models

8.1 Device Description

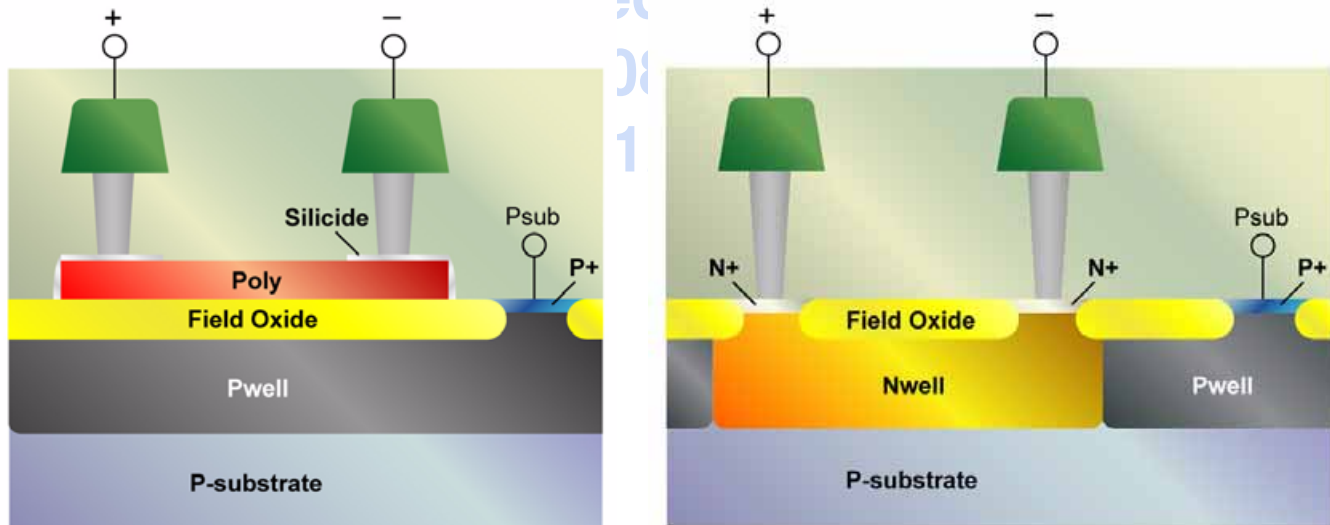
CA13/SBL13 processes support three types of resistor devices. These include low and high value unsalicyded polysilicon and Nwell resistors as shown in Figure 8.1 and listed in Table 8.1. The poly resistors are very linear for reasonable length geometries ($>3\mu\text{m}$) and are thus modeled by linear resistors. Short resistors ($<3\mu\text{m}$) can experience velocity saturation for larger biases which is not modeled. Due to the lower doping of the Nwell non linear effects due to JFET pinching are significant for all geometries. This JFET effect is included in the model. For all resistors, the resistance can be changed through choice of Finger Width “W”, length “L” and number of fingers “Strips” in the component property window. A calculation callback updates the resistance value using the nominal electrical specification. For the Nwell resistor, this result corresponds to zero bias at the terminals.

TABLE 8.1 CA13/SBL13 Supported Resistors

Resistor	Description	sheet rho
<i>rppoly_lo</i>	Low value unsalicyded poly resistor	310
<i>rppoly_hi</i>	High value unsalicyded poly resistor	1K
<i>rnwell</i>	Nwell resistor	890

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FIGURE 8.1 Unsalicyded poly resistor, low and high value (left), and Nwell resistor (right)



8.2 Model Description

The equivalent circuit representation of the poly resistor (rf-version) is shown in Figure 8.2. The individual components are based on physical models and are computed using geometrical and electrical process spec information. The base resistance equation is given by

$$R = \frac{\rho_{\square} \cdot L + R_{end}}{W + \Delta W} \tag{EQ 1}$$

where ΔW is the change in effective width, ρ_{\square} is the sheet resistance, and R_{end} is the end resistance. Please note that poly resistors are supported either full inside or fully outside nwell. No modeling effects are included for the nwell-psub junction if placed in nwell. The equivalent circuit for an Nwell resistor is shown in Figure 8.3 where R_{nwell} is described by a voltage dependent resistance implemented in Verilog-A. Rn is given by (EQ 1) at zero bias.

FIGURE 8.2 Sub-Circuit model for resistor (rf-version)

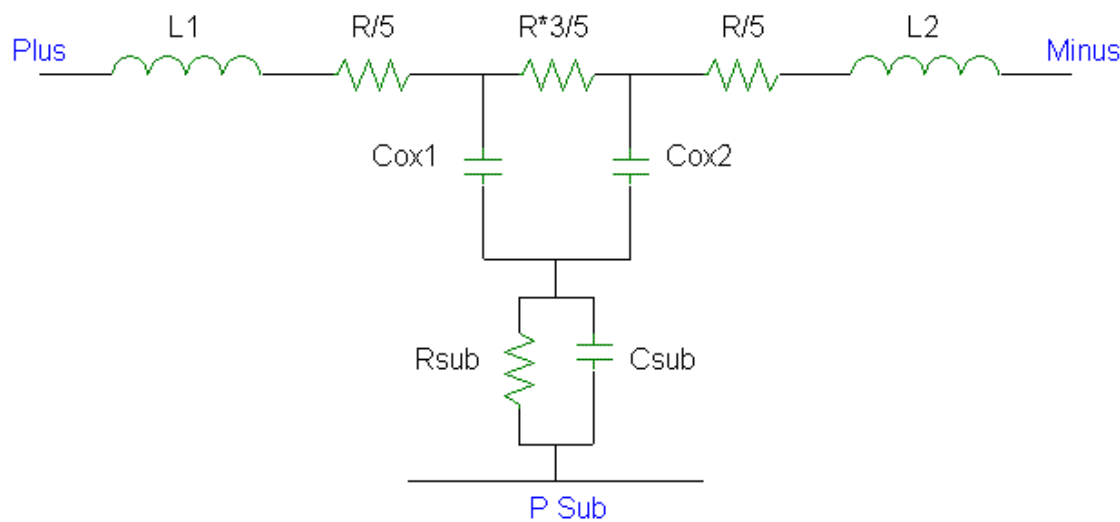


FIGURE 8.3 Sub-Circuit model for Nwell resistor

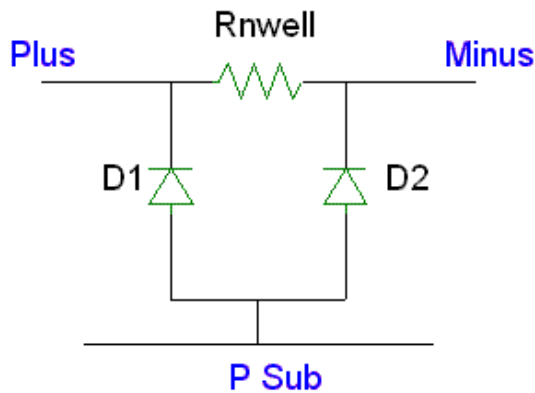


TABLE 8.2 Model Sub-circuit Component Names

Circuit Components	
R	Poly resistance
L1, L2	Resistor self-inductance
Cox1, Cox2	Oxide capacitance

Circuit Components

Rnwell	Resistance of Nwell
D1, D2	Diodes associated with Nwell
Csub	Substrate capacitance
Rsub	Substrate resistance

8.3 Model Verification

DC measurements are performed over temperature for the poly and nwell resistors. The temperature coefficients TC1 and TC2 are extracted based from measurements with ranging from -40 to 125 C. The temperature model equation is

$$R(T) = R_{T25} \cdot [1 + TC1 \cdot (T - T25) + TC2 \cdot (T - T25)^2] \quad (\text{EQ 2})$$

Figures Figure 8.4 through Figure 8.6 show the measured data and the simulated results for temperature range from -40C to 125C for the poly resistor and nwell resistor respectively. Figure 8.7 shows the nwell resistor model validation over voltage.

FIGURE 8.4 rppoly_lo temperature characteristics comparison between data and model

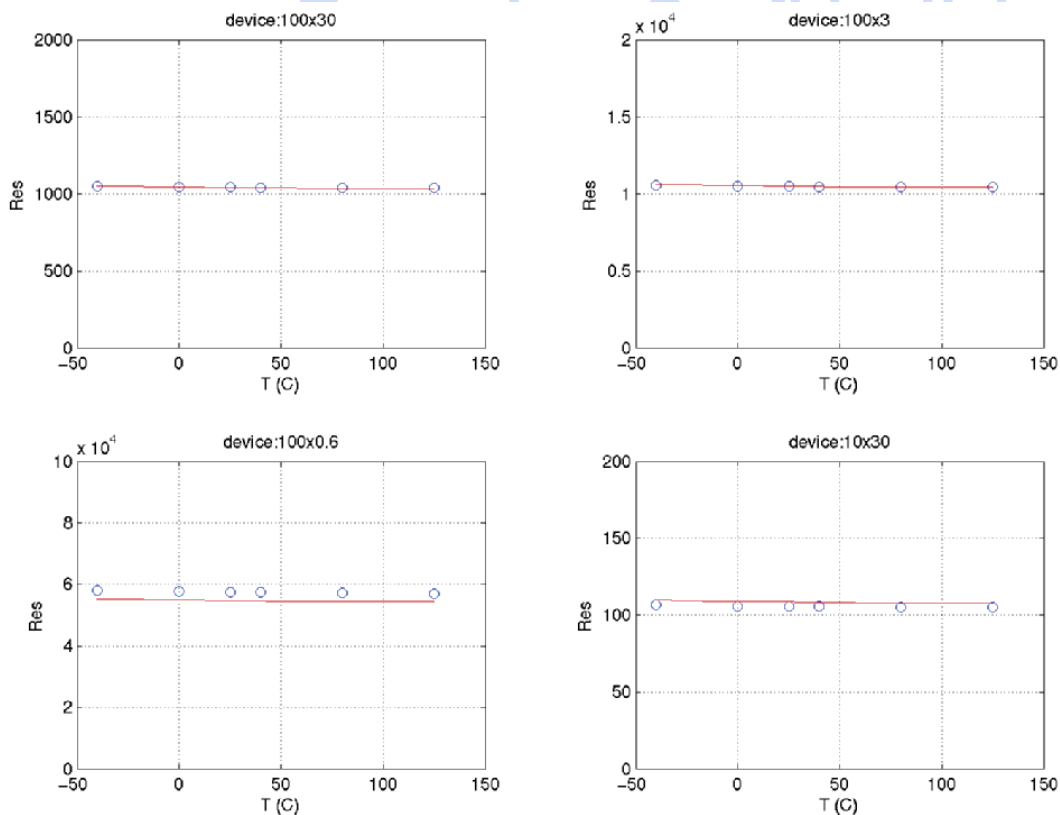


FIGURE 8.5 rppoly_hi temperature characteristics comparison between data and model

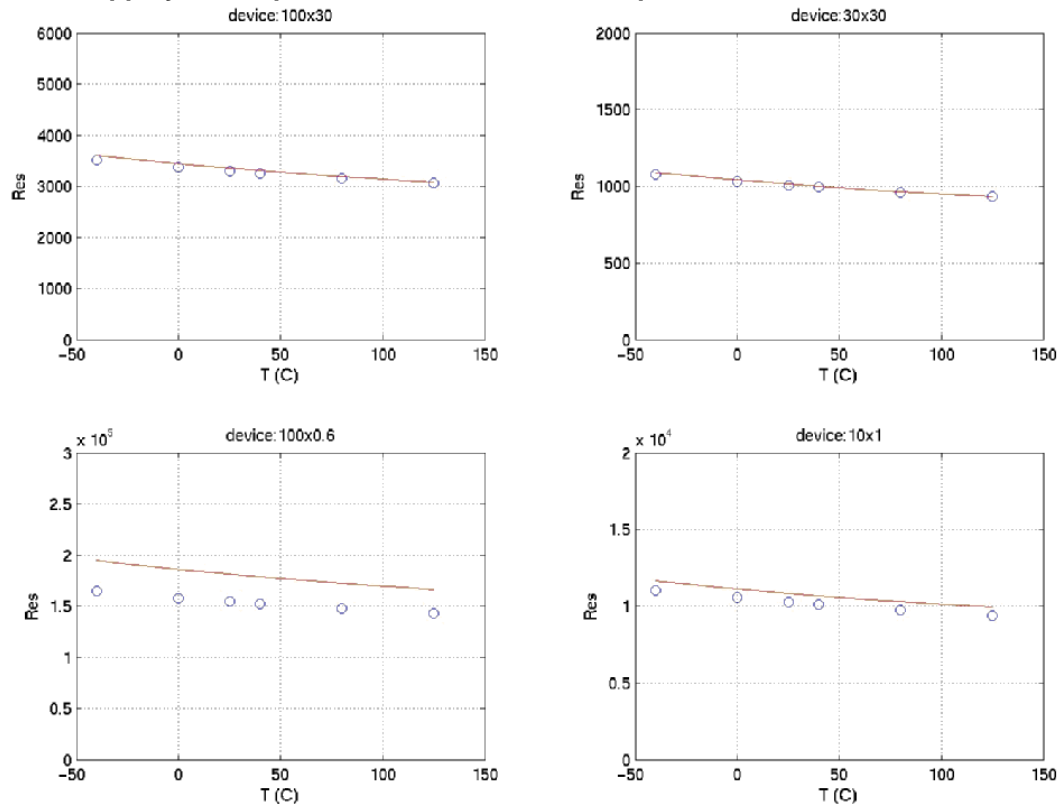


FIGURE 8.6 rnwell temperature characteristics comparison between data and model

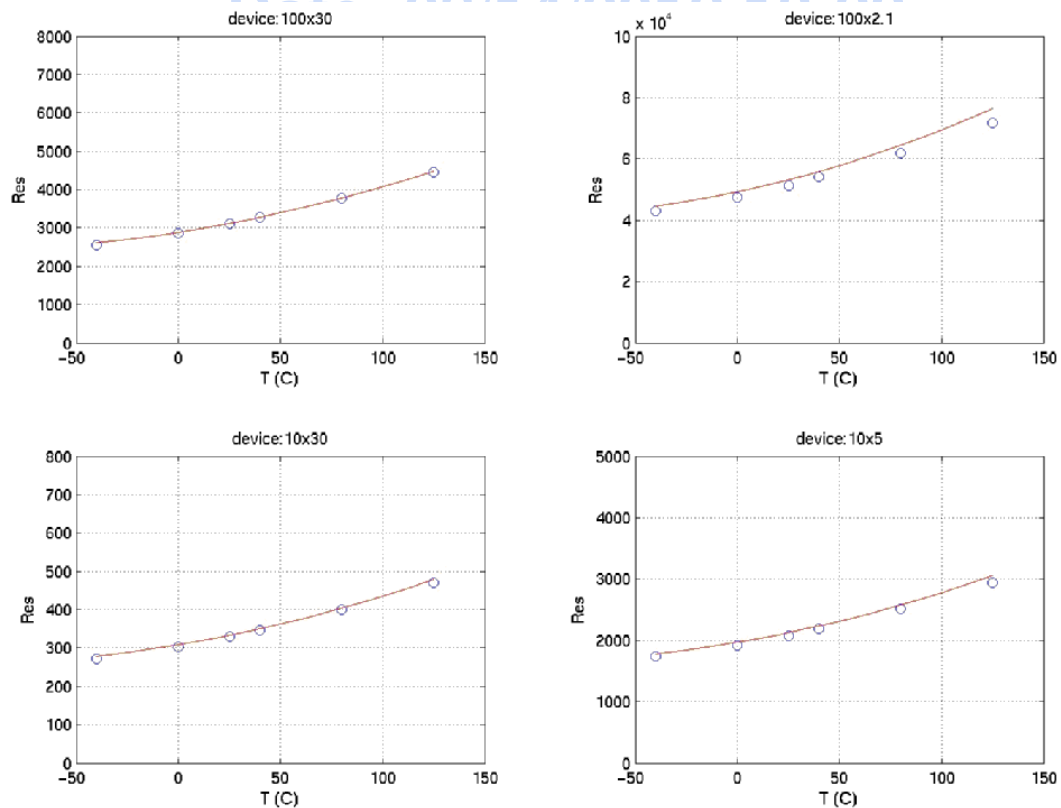
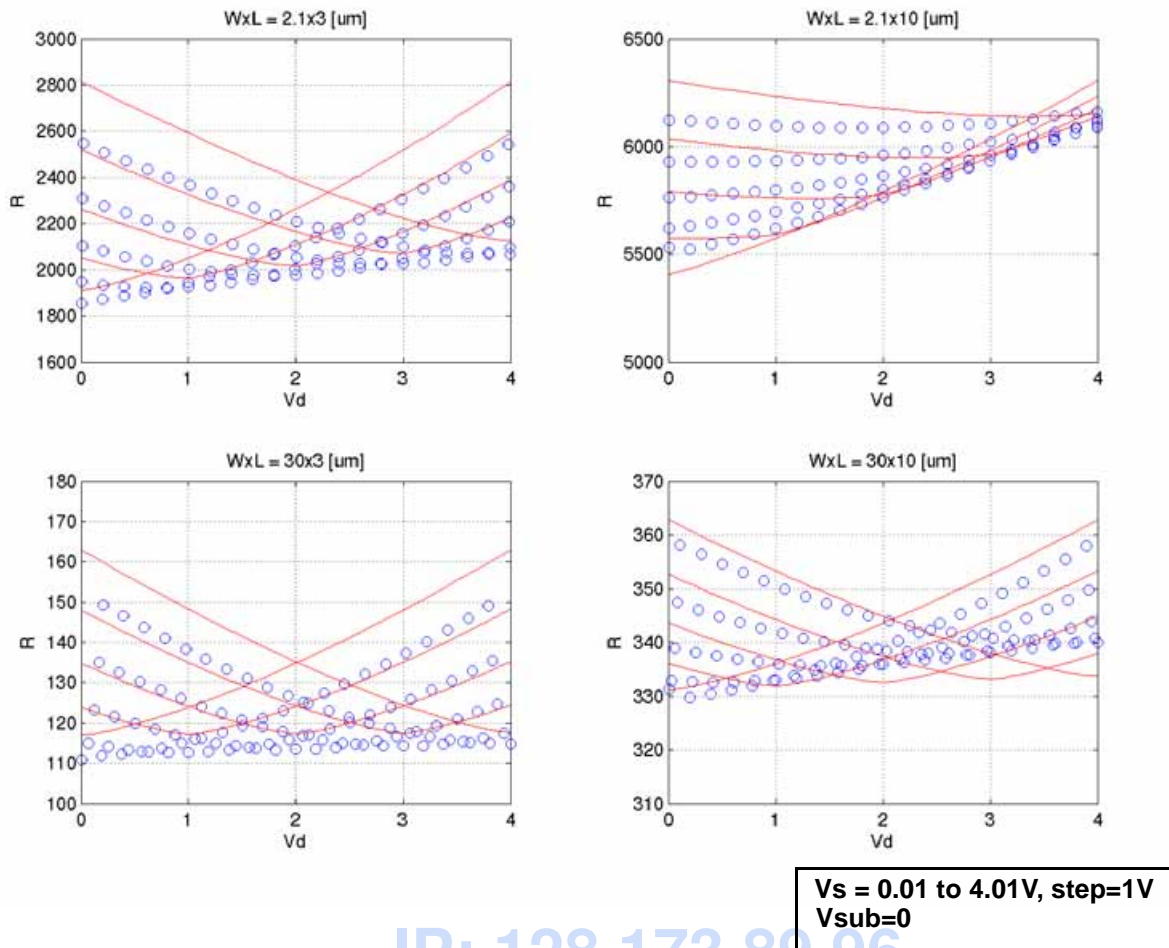


FIGURE 8.7 r_{nwell} – Over voltage



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8.4 Resistor Statistical and Corner Models

The resistor statistical and corner models account for process variation of the ΔW , sheet resistance ρ_{\square} , end resistance R_{end} , and STI thickness derived directly from the process ESPECs. The Resistor model parameters are directly correlated with the process parameters. The corner performance is determined using the min and max values in the ESPECs. See Section 13.0 for further explanation of the device interdependencies in the corner models and use of the X-Sigma corner models. Table 8.3 lists the resistor specific ESPECs compared to simulated corner and statistical values

TABLE 8.3 Resistor ESPEC, Corner, and Statistical Model Simulation

Device	name	units	Slow			Nom			Fast		
			Espec	Corner	Stat	Espec	Corner	Stat	Espec	Corner	Stat
rps	rend ²	ohm-um	23.6	23.4	23.2	19.0	18.9	18.8	14.5	14.4	14.5
	dw ²	um	0.02	0.02	0.02	0.03	0.03	0.03	0.04	0.04	0.04
	rs ¹	ohm/sq	8.13	8.08	8.06	6.50	6.46	6.43	4.88	4.85	4.81
rppoly_lo	rend ²	ohm-um	110	111	109	85	85	85	60	60	60
	dw ²	um	-0.06	-0.06	-0.06	-0.05	-0.05	-0.05	-0.04	-0.04	-0.04
	rs ¹	ohm/sq	357	357	353	310	310	311	264	264	269
rppoly_hi	rend ²	ohm-um	379	380	377	316	317	316	253	253	255
	dw ²	um	-0.056	-0.056	-0.056	-0.046	-0.046	-0.046	-0.036	-0.036	-0.036
	rs ¹	ohm/sq	1150	1150	1150	1000	1000	1000	850	850	850
rnwell	rend ²	ohm-um	1050	1050	1050	875	871	868	700	697	690
	dw ²	um	-0.38	-0.38	-0.38	-0.28	-0.28	-0.28	-0.18	-0.18	-0.185
	rs ¹	ohm/sq	1070	1090	1080	890	909	913	710	727	743

PCM notes:

1. PCM and ESPEC share the same limits.
2. There is no PCM monitoring.

8.5 Resistor Mismatch Models**8.5.1 Mismatch Measurements**

For resistor mismatch characterization, the basic set-up is a kelvin measurement of 2 matched pairs. Resistor mismatch characterization is only available for poly resistors.

8.5.1.1 Resistor Mismatch Modeling

The resistor mismatch included in the design kit takes into account area and perimeter capacitance mismatch variations. Mismatch due to spacing variation is not included in the model. The mismatch models for the ΔW , sheet resistance ρ_q , end resistance R_{end} are given by

$$\rho_{\square mm} = \rho_{\square nom} \left(1 - \frac{\sigma_A}{\sqrt{LW}} \right) \quad (\text{EQ 3})$$

$$R_{end mm} = R_{end nom} \left(1 - \frac{\sigma_B}{\sqrt{LW}} \right) \quad (\text{EQ 4})$$

$$\Delta W_{mm} = \Delta W_{nom} \left(1 - \frac{\sigma_C}{\sqrt{W}} \right) \quad (\text{EQ 5})$$

where σ_A , σ_B , and σ_C are the mismatch coefficients extracted via a nonlinear least squares global optimization method to best fit the measured data.

8.6 Mismatch Model Usage Guidelines

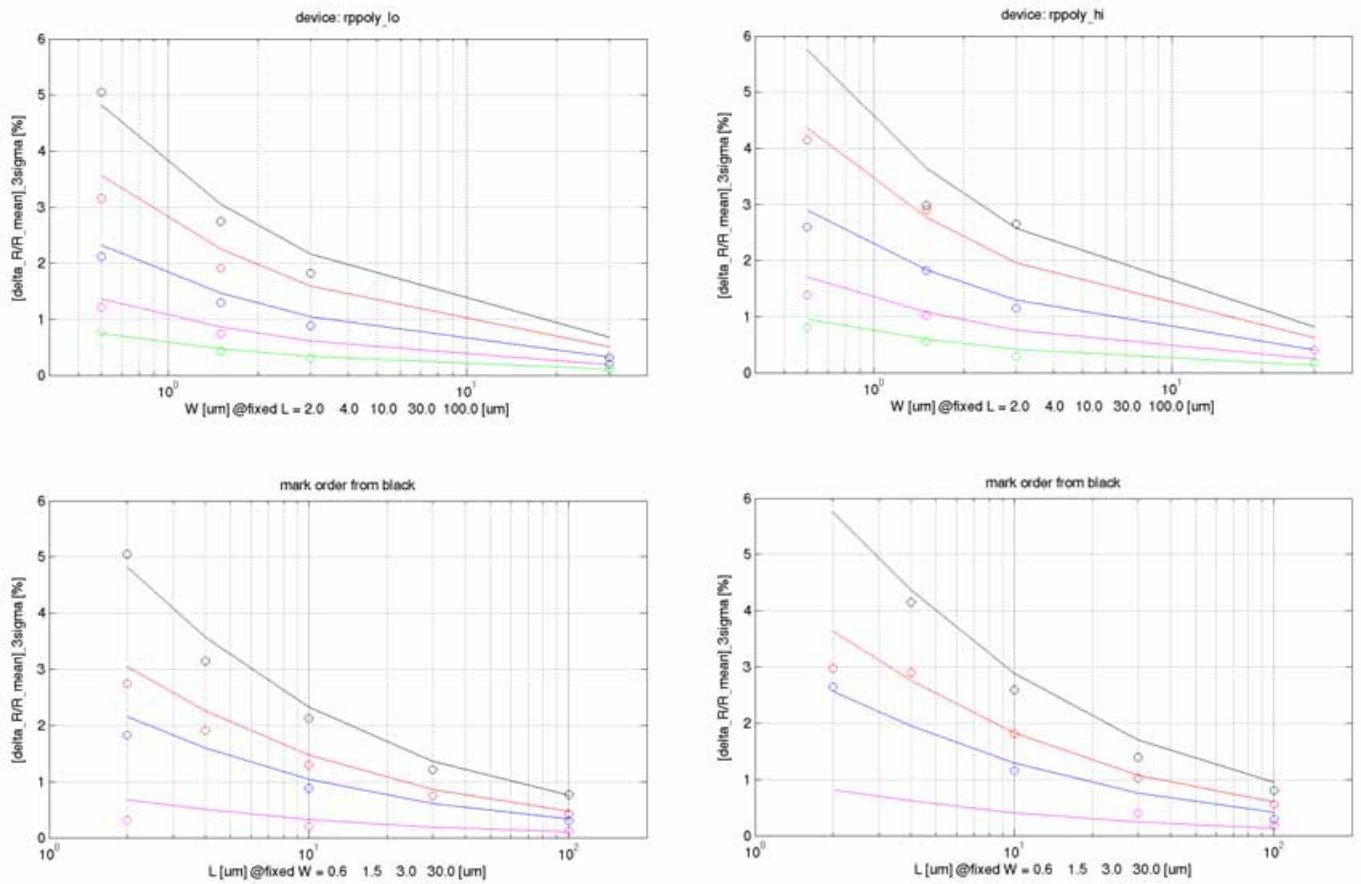
The mismatch model is available in Spectre, which provides the necessary framework to model the local mismatch between resistors. It is implemented inside the “sub-circuit” definition of the resistors allowing for “instance to instance” variations in the process parameters. The “variations” variable inside Spectre should be set equal to “mismatch.” Typically, ~100 monte-carlo runs are sufficient to accurately simulate the local-mismatch between the resistors. The user should, however, increase the “numruns” variable inside Spectre until the improvement in the simulated results is small.

8.6.1 Mismatch Model Verification

The mismatch between closely spaced resistor pairs follows a geometric dependence. An extraction process was performed to determine the mismatch coefficients for resistor parameters of ΔW , ρ_{\square} , and R_{end} . These coefficients are used in the statistical model card. The Spectre to measurement mismatch results is shown in Figure 8.8. To obtain good matching results, it is preferable to not use minimum dimension but larger size resistors.

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FIGURE 8.8 Low-Value and High-Value Poly resistor mismatch



8.7 Low Value Poly Resistor Flicker Noise (1/f Noise) Model and Verification

Poly-silicon resistors exhibit current noise that is at lower frequencies inversely proportional to frequency and area of the resistor. At higher frequencies the 1/f dependence is replaced by thermal noise which is described by

$$\sqrt{S_{th}} = \sqrt{\frac{4 \cdot k \cdot T}{R}} \quad \left[\frac{A}{\sqrt{Hz}} \right] \quad (EQ 6)$$

The 1/f noise is caused by charge trapping and de-trapping events at the poly-silicon grain boundaries. These events change the energetic barrier and thus modulate the resistance or current over the grain boundary. A physics based equation was proposed in IEEE Transactions on Electron Devices, Vol48, No.6, June 2001 by Brederlow et al.

$$S_I = \frac{I^2}{W \cdot L} \cdot \frac{\alpha}{f} \quad \left[\frac{A^2}{Hz} \right] \quad (EQ 7)$$

where S_I is the noise current per frequency band width and α is the parameter extracted to measured data.

This equation was implemented in the Spectre model cards for **rpoly_lo** device by matching it with the coefficients of the Spectre provided noise equation.

$$\sqrt{S_I} = \sqrt{\frac{KF \cdot I_r^{AF}}{f}} \quad \left[\frac{A}{\sqrt{Hz}} \right] \quad (EQ 8)$$

where $I_r = I$, $AF = 2$, and $KF = \alpha/(WL)$.

The model verification plots for two **rpoly_lo** devices at biases 0.25, 0.5 and 2 V are shown in figures Figure 8.9 and Figure 8.10. The model verification plot for a **rpoly_hi** at the same bias points is shown in Figure 8.11.

FIGURE 8.9 Flicker Noise (rppoly_lo) – W=3um, L=10um

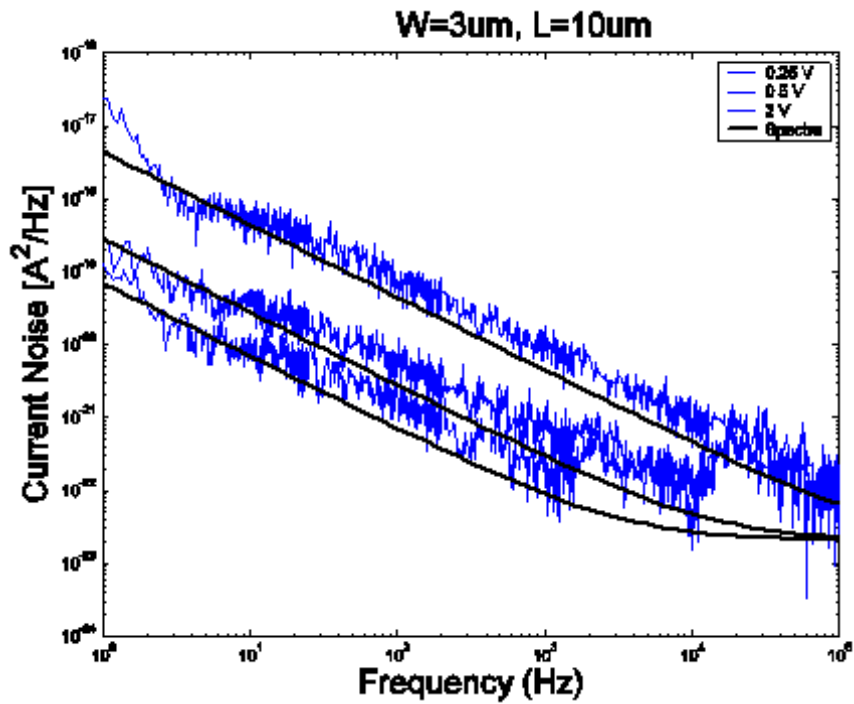


FIGURE 8.10 Flicker Noise (rppoly_lo) – W=10um, L=10um

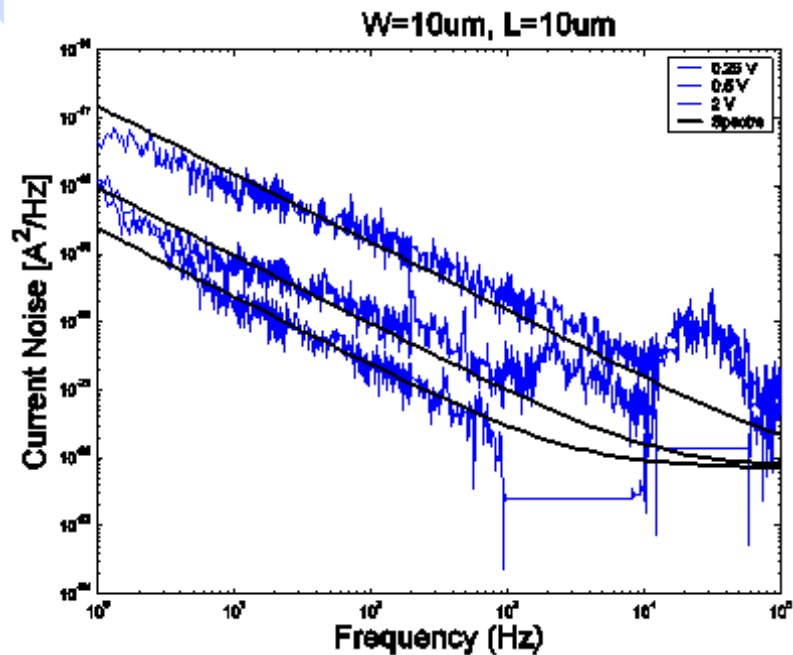
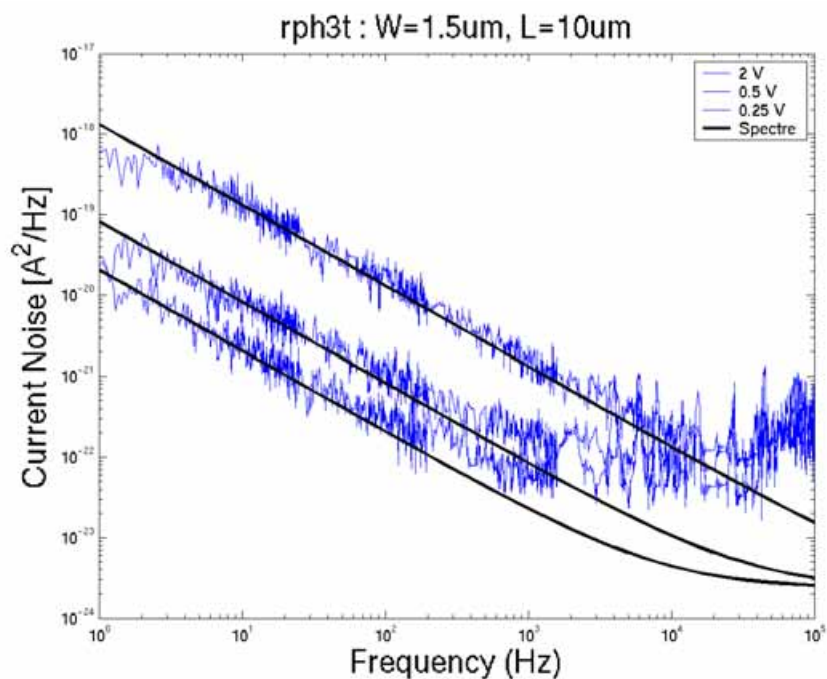


FIGURE 8.11 Flicker Noise (rppoly_hi) - W=1.5um, L=10um



8.8 Model Update History

TABLE 8.4 Resistor model specific updates in model release version 1.8

v1.8 update	Devices	Reason	Impact on user
Update model to tightened EPEC for sheet rho	low value poly resistor	ESPEC variation for sheet rho tightened	See ESPEC differences.

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9.0 Capacitor Models

9.1 MiM capacitor model

9.1.1 Device description

The CA13/SBL13 technology offers vertical MiM capacitor densities and metal layer configurations given in Table 9.1.

TABLE 9.1 CA13/SBL13 MIM Capacitors

Technology	Metal Layers	MiM Definition	Model Name
CA13HC, SBL13	6	2.8fF between M4-M5	cmim3, cmimw3_4
CA13HC, SBL13	6	2.8fF between M5-M6	cmim3_m5, cmimw3_4_m5
CA13HC, SBL13	6	5.6fF stacked between M4-M6	csmim6, csmimw6_4

MiM capacitors can be placed over Nwell ("w" in device name) or over P-substrate. MiM capacitors over Nwell have an additional Nwell to P-substrate junction isolation between the bottom plate and P-substrate which is included in the model. The 3rd terminal is the Nwell and 4th terminal is the P-substrate. Table 9.2 provides a description of the terminal connections. In order to obtain better isolation between the MiM capacitors over Nwell and nearby devices, it is recommended to tie the Nwell to AC ground (VDD for example). Figure 9.1 illustrates a cross section of a MiM capacitor over Nwell.

FIGURE 9.1 MIM Capacitor cross section (CMIM3 - between M4 and M5)

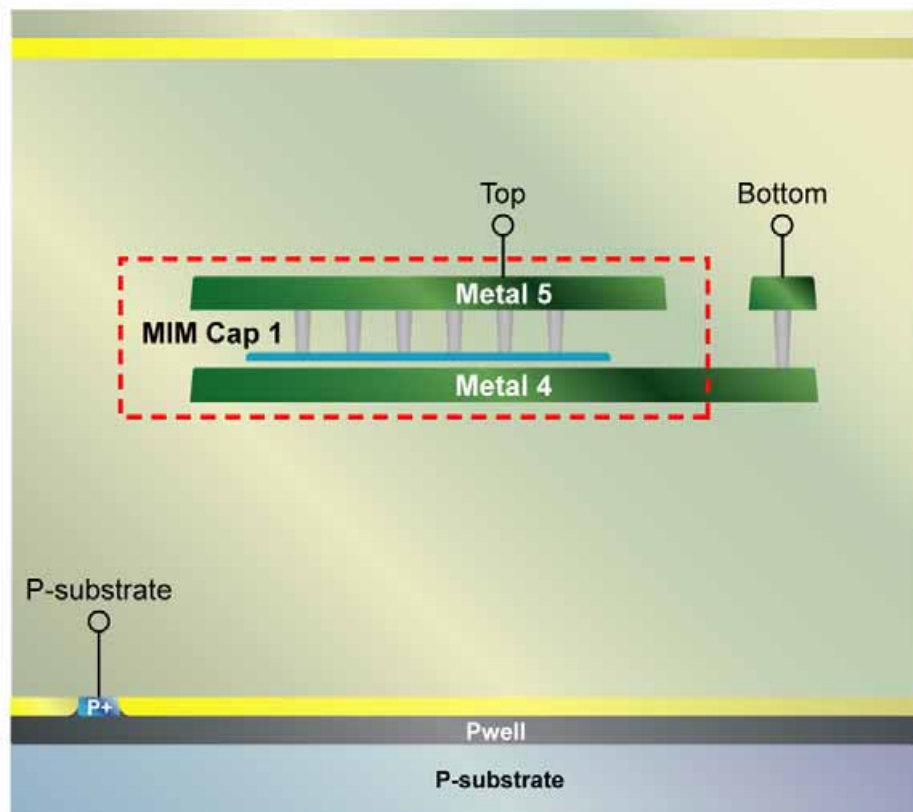
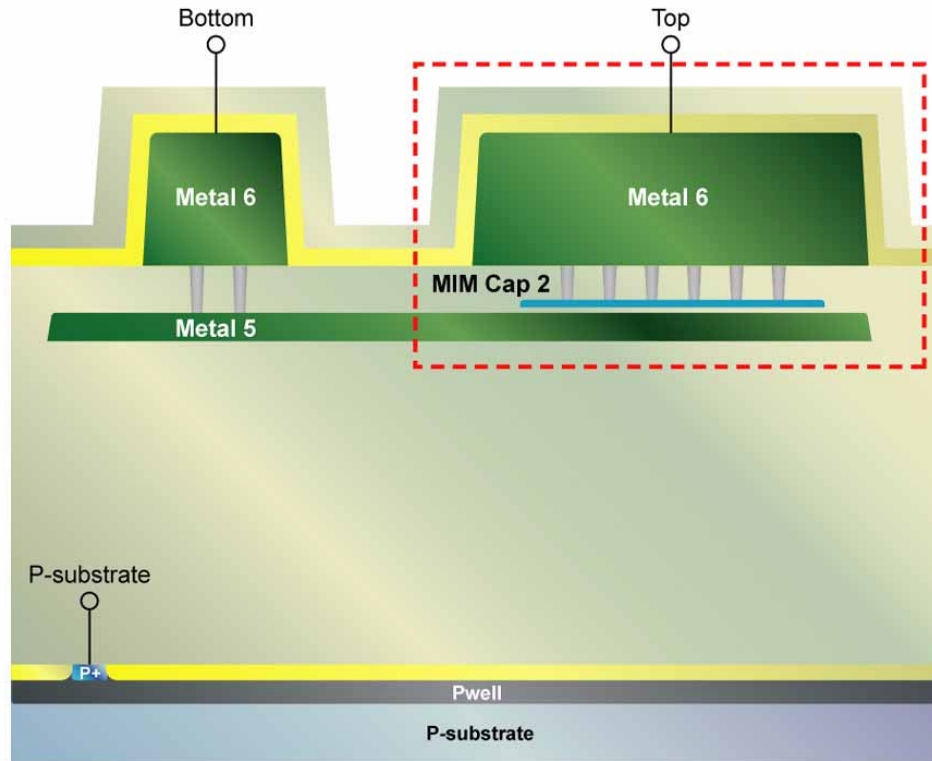


FIGURE 9.2 MIM Capacitor cross section (CMIM3_M5 - between M5 and M6)

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FIGURE 9.3 Stacked MIM Capacitor cross section

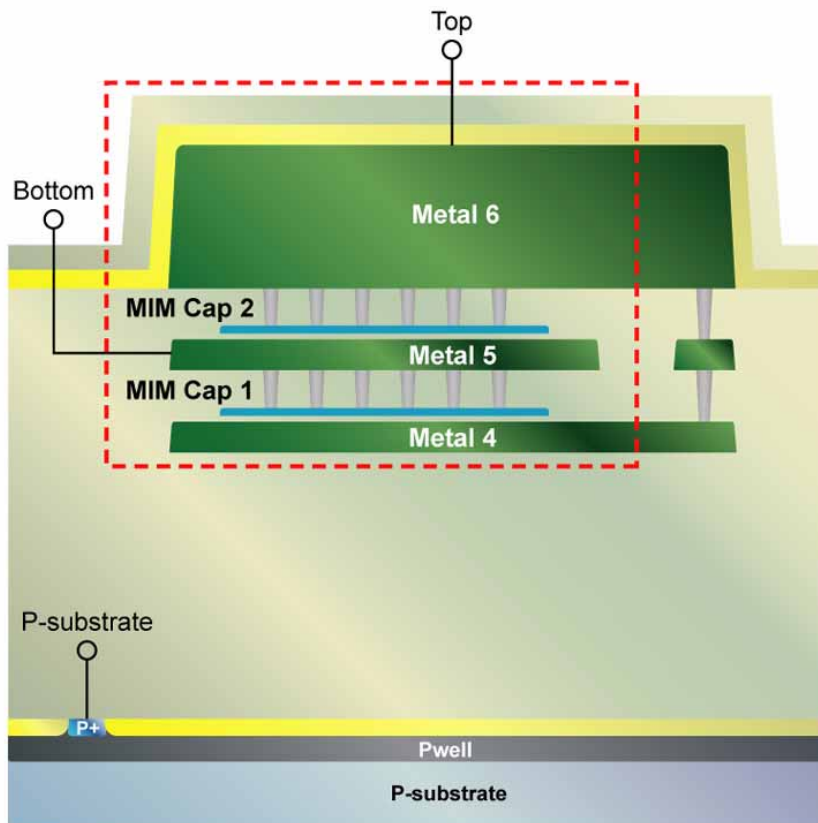


TABLE 9.2 MiM NWELL and SUB Terminal Connections

Terminals	SUB Terminal	NWELL Terminal	Models
3	3rd terminal	none	cmim3, cmim3_m5, csmim6
4	4th terminal	3rd terminal	cmimw3_4, cmimw3_4_m5, csmimw6_4

9.1.2 Model Description

Figure 9.4 through Figure 9.7 show the sub circuits used to model the MiM and stacked MiM devices respectively. Please refer to Table 9.3 for sub circuit component names and physical descriptions. The model includes all elements within the dashed box shown in Figure 9.1 including metal and via parasitics. The bottom plate access is not included in the model since it's placement is controlled by the pcell with various options available. The model assumes one sided bottom and top plate routing which is a worst case scenario. Accurate simulations of the bottom plate access are achieved through parasitic extraction and simulation. See Appendix A for more information on layout parasitics. The device over Nwell model includes the Nwell/psub diode. All models scale with MiM length (L) and width (W).

FIGURE 9.4 Sub-circuit and component description of a MIM capacitor over Nwell.

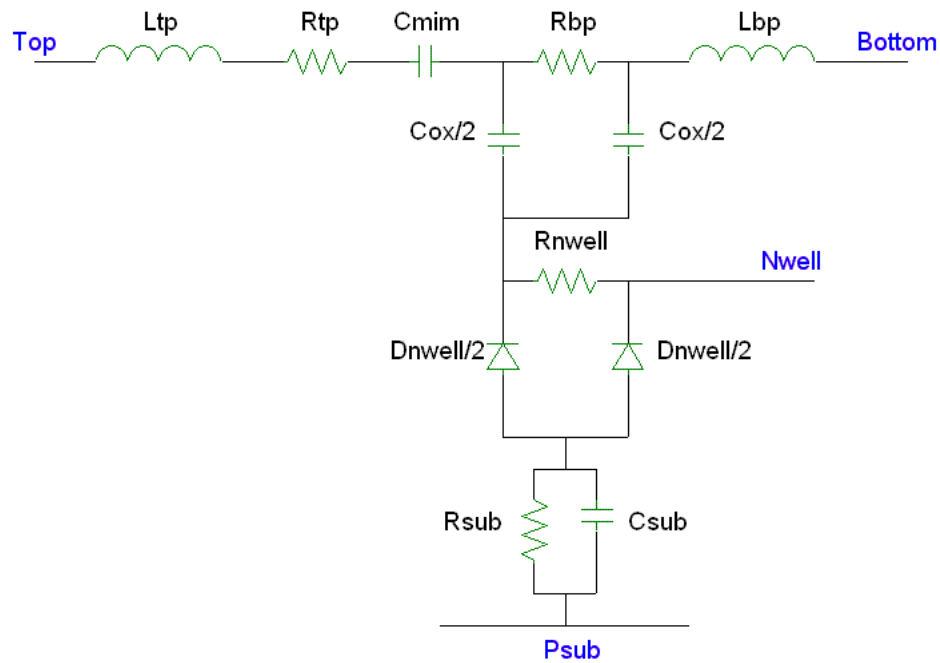


FIGURE 9.5 Sub-circuit and component description of a MIM capacitor over P substrate.

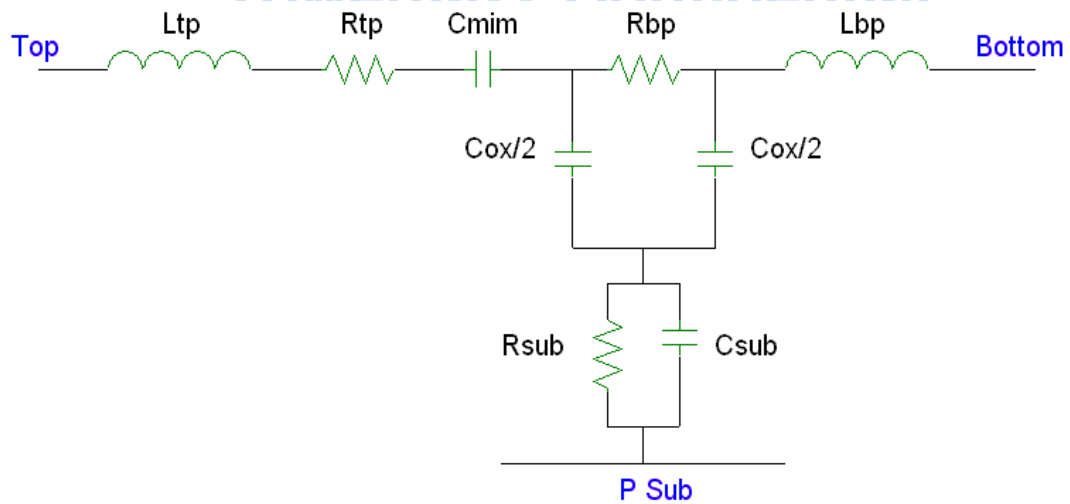


FIGURE 9.6 Sub-circuit and component description of a Stacked MIM capacitor over Nwell.

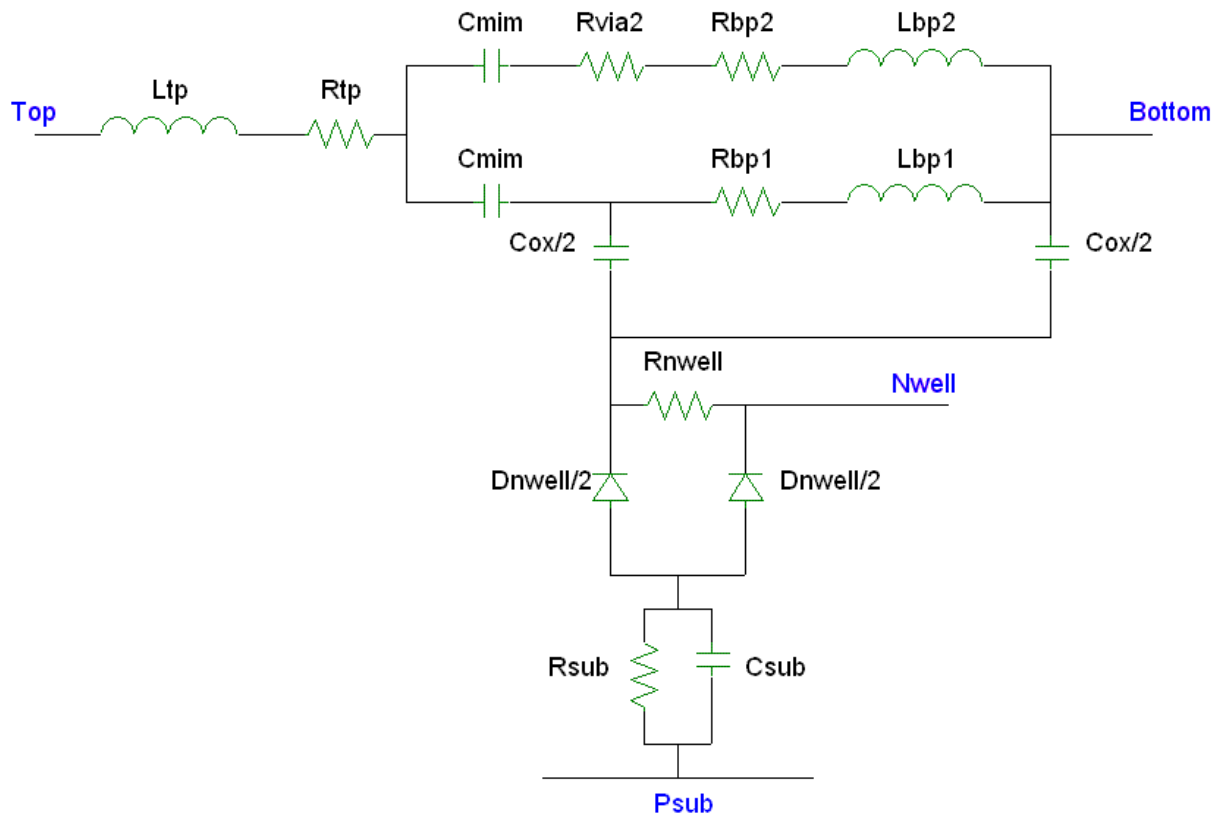


FIGURE 9.7 Sub-circuit and component description of a Stacked MIM capacitor over P substrate.

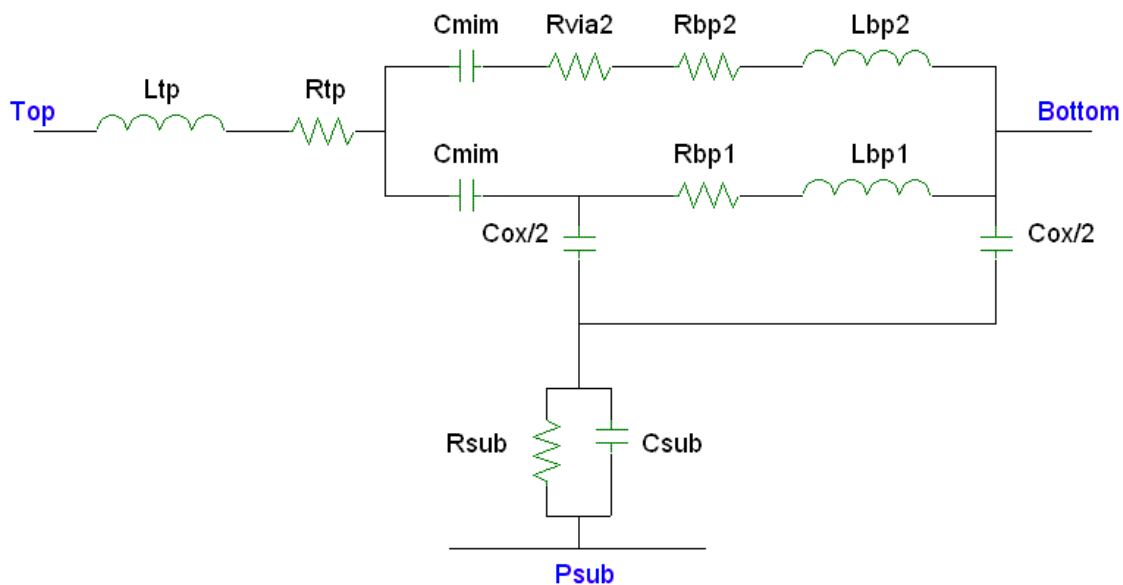


TABLE 9.3 Capacitor Model Sub-circuit component names

Circuit Components		Characterization Method
cmim	MIM Capacitance	Verified by low frequency s-parameters
Ltp	Top Plate Inductance	Calculated by Greenhouse equation, verified by SRF characteristics from high frequency s-parameters
Rtp	Top Plate Metal and VIA Resistance	Calculated directly from geometry and sheet p
Rbp	Bottom Plate Resistance	Calculated directly from geometry and sheet p
Lbp	Bottom Plate Inductance	Calculated by Greenhouse equation, verified by SRF characteristics of Ceff data
Cox	Oxide Capacitance	Calculated directly from ESPEC
RNwell	Nwell Resistance	Calculated directly from ESPEC
DNwell	Nwell to P Sub junction diode	Calculated directly from ESPEC
Csub	Substrate Capacitance	Estimated
Rsub	Substrate Resistance	Estimated
Rvia	Via Resistance	Calculated directly from ESPEC

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9.1.3 Model Verification

Figure 9.8 and Figure 9.9 show the simulated results for the 2.8 and 5.6fF capacitors respectively.

FIGURE 9.8 2.8fF/ μm^2 MIM capacitance and Q characteristics

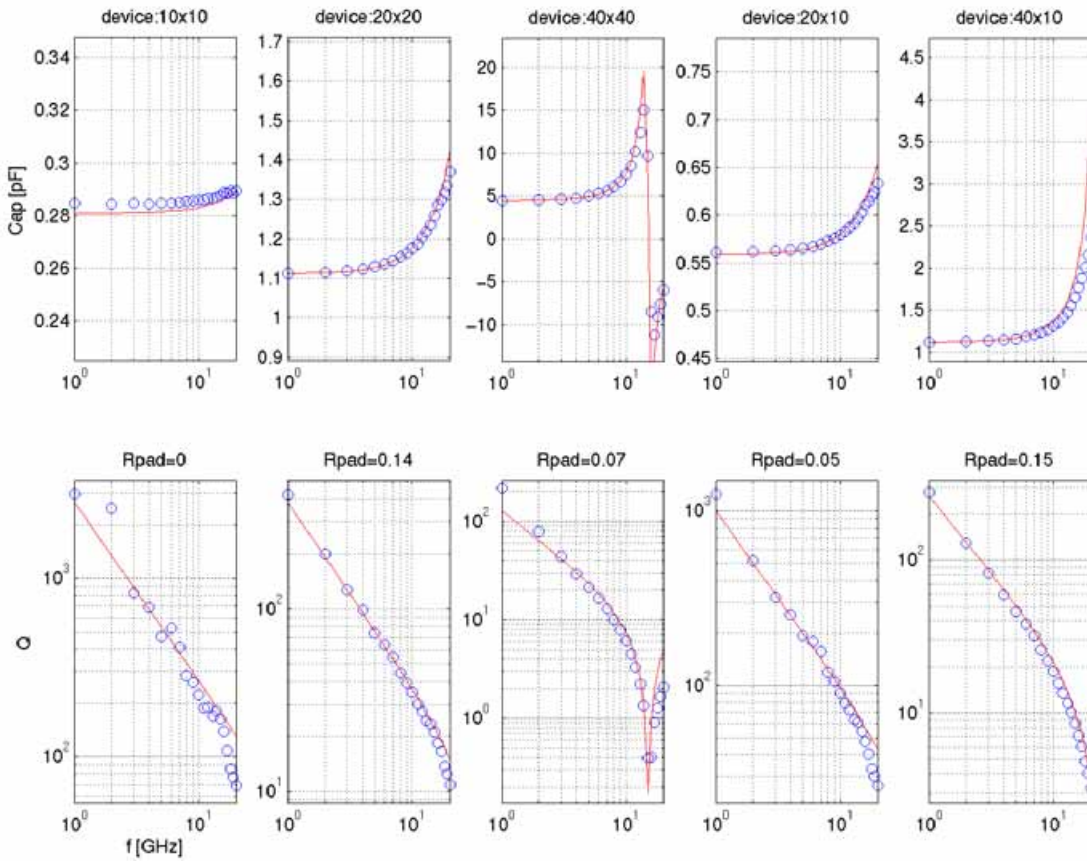
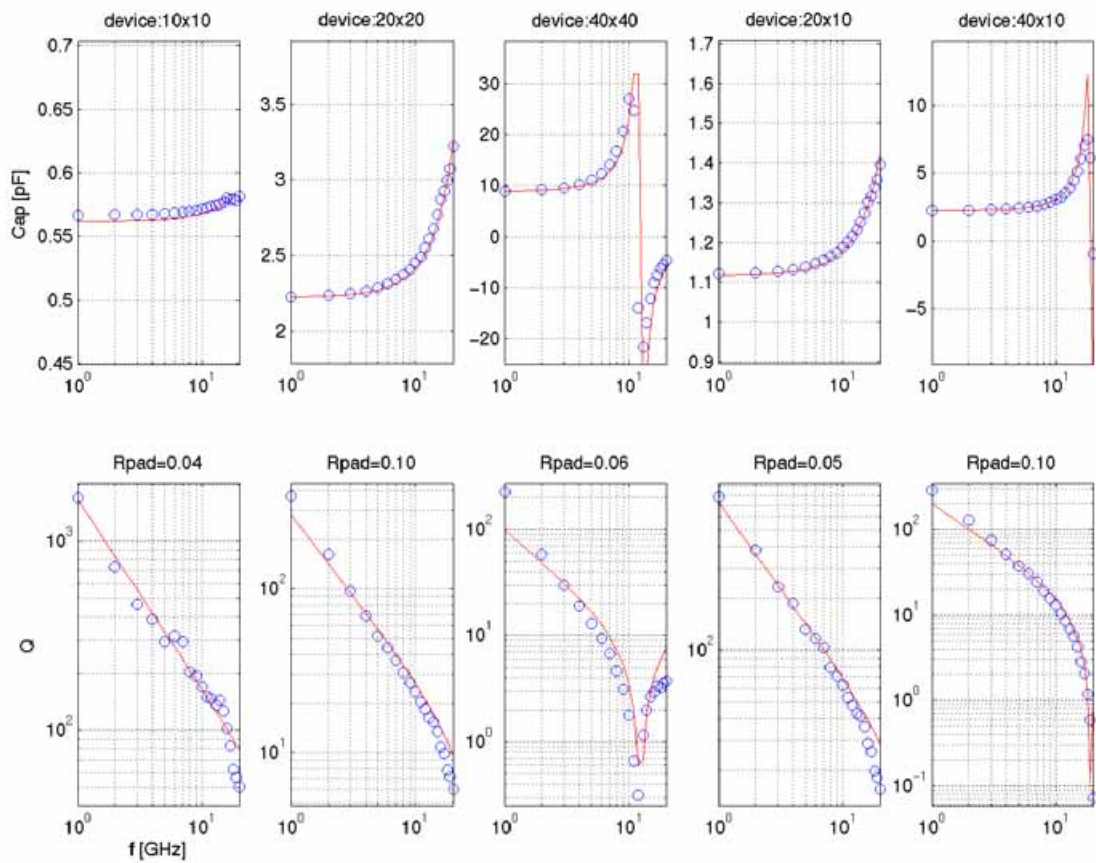


FIGURE 9.9 5.6fF/ μm^2 MiM capacitance and Q characteristics

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9.1.4 MiM Statistical and Corner Models

The MiM statistical and corner models account for process variation of the MiM dielectric, metal thickness (sheet resistivity), and ILD thickness derived directly from the process ESPECs. The MiM model parameters are directly correlated with the process parameters. See Section 13.0 for further explanation of the device interdependencies in the corner models and use of the X-Sigma corner models. Table 9.4 lists the MiM specific ESPECs compared to simulated corner and statistical values for three MiM capacitor devices.

TABLE 9.4 ESPEC, Corner and Statistical Model Comparison for MiM Capacitor Model

Device	name	units	slow			nomi			fast		
			Espec	Corner	Stat	Espec	Corner	Stat	Espec	Corner	Stat
cmim3	cp ²	fF/ μm	0.25	0.25	0.25	0.15	0.15	0.15	0.05	0.05	0.05
	ca ¹	fF/ μm^2	3.16	3.16	3.17	2.75	2.75	2.76	2.34	2.34	2.34
	tc ²	ppm/v		20	20	20	20	20		20	20

TABLE 9.4 ESPEC, Corner and Statistical Model Comparison for MiM Capacitor Model

Device	name	units	slow			nomi			fast		
			Espec	Corner	Stat	Espec	Corner	Stat	Espec	Corner	Stat
cmim6	cp ²	fF/um	0.5	0.5	0.5	0.3	0.3	0.3	0.05	0.1	0.1
	ca ¹	fF/um ²	6.32	6.33	6.34	5.5	5.5	5.5	4.68	4.68	4.68
	tc ²	ppm/v		20	20	20	20	20		20	20

PCM notes:

1. PCM and ESPEC share the same limits.
2. There is no PCM monitoring.

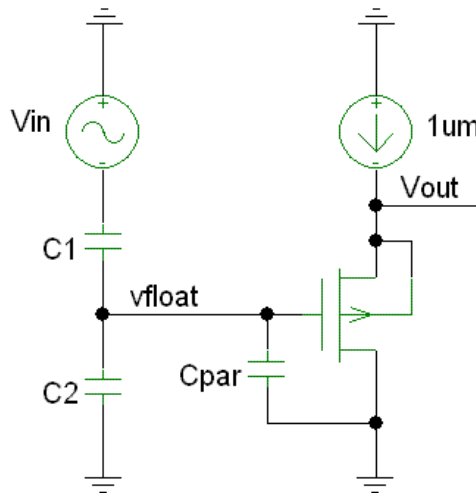
9.1.5 MiM Mismatch Models

9.1.5.1 Mismatch Measurements

For capacitor mismatch characterization, the basic set-up is a voltage divider circuit as shown in Figure 9.10. By reversing the terminals of the capacitor pairs, the mismatch can be calculated independent of the circuit parasitics, given by

$$\frac{\Delta C}{C} = 2 \cdot \left(\frac{C1 - C2}{C1 + C2} \right) \quad (\text{EQ 1})$$

FIGURE 9.10 MiM Mismatch Measurement Schematic



9.1.5.2 MiM Mismatch Modeling

The MiM mismatch included in the design kit takes into account area and perimeter capacitance mismatch variations. Mismatch due to spacing variation is not included in the model. The mismatch models for area and perimeter effects are given by

$$CA_{mm} = CA_{nom}(1 - \sigma_A[LW]^{\delta_A}) \quad (\text{EQ 2})$$

$$CP_{mm} = CP_{nom}(1 - \sigma_P[LW]^{\delta_P}) \quad (\text{EQ 3})$$

where σ_A , σ_P , δ_A , and δ_P are the area and perimeter coefficients and exponents extracted via a nonlinear least squares global optimization method to best fit the measured data.

9.1.5.3 Mismatch Model Usage Guidelines

The mismatch model is available in Spectre, which provides the necessary framework to model the local mismatch between capacitors. It is implemented inside the “sub-circuit” definition of the MiMs allowing for “instance to instance” variations in the process parameters. The “variations” variable inside Spectre should be set equal to “mismatch.” Typically, ~100 monte-carlo runs are sufficient to accurately simulate the local-mismatch between the MiMs. The user should, however, increase the “numruns” variable inside Spectre until the improvement in the simulated results is small.

9.1.5.4 Mismatch Model Verification

Figure 9.8 and Figure 9.9 show the mismatch model prediction of the measured data for the minimum spacing (4 μm) 3- σ $\frac{\Delta C}{C}$ vs. capacitance value which is scaled through geometry variation. For smaller devices, the mismatch increases due to perimeter effect dominance. For larger devices, the mismatch increases due to area effect dominance. The model accurately predicts the trends and can be used to design for minimum mismatch between 2 capacitor pairs.

9.1.6 Model Update History

The following tables list the model updates with each revision. Unlisted model revisions indicate that no changes have occurred in that revision.

TABLE 9.5 MiM model specific updates in model release version 1.7

v1.7 update	Devices	Reason	Impact on user
Updated Models to POR	All	Prior models based on CA18HR	Minimal model changes

FIGURE 9.11 2.8fF MiM Matching Data (circles) vs. Model (solid line) (spacing=4 μ m)

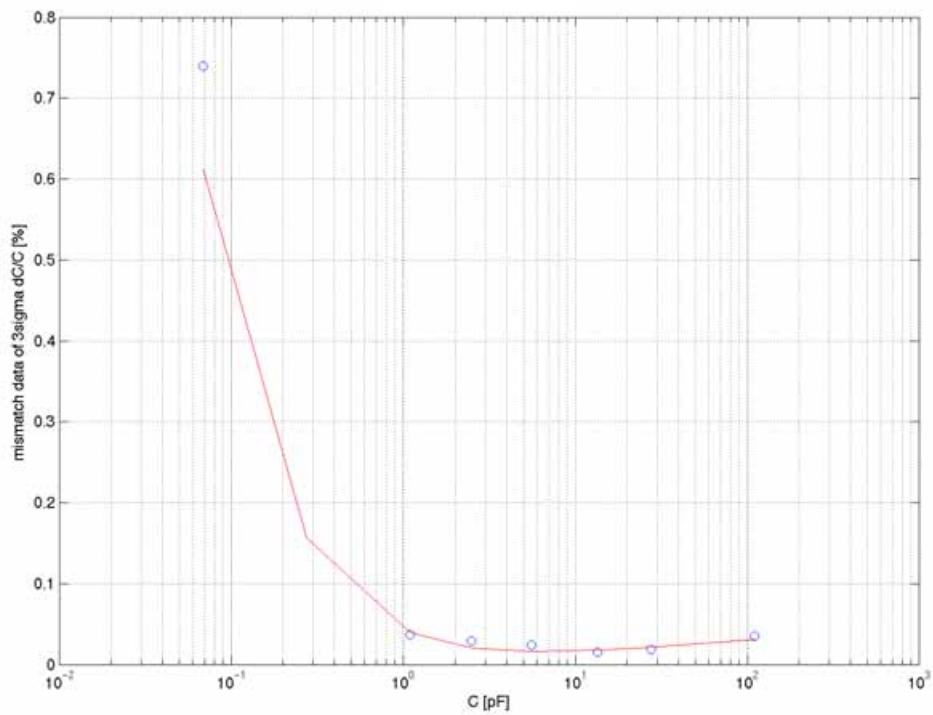
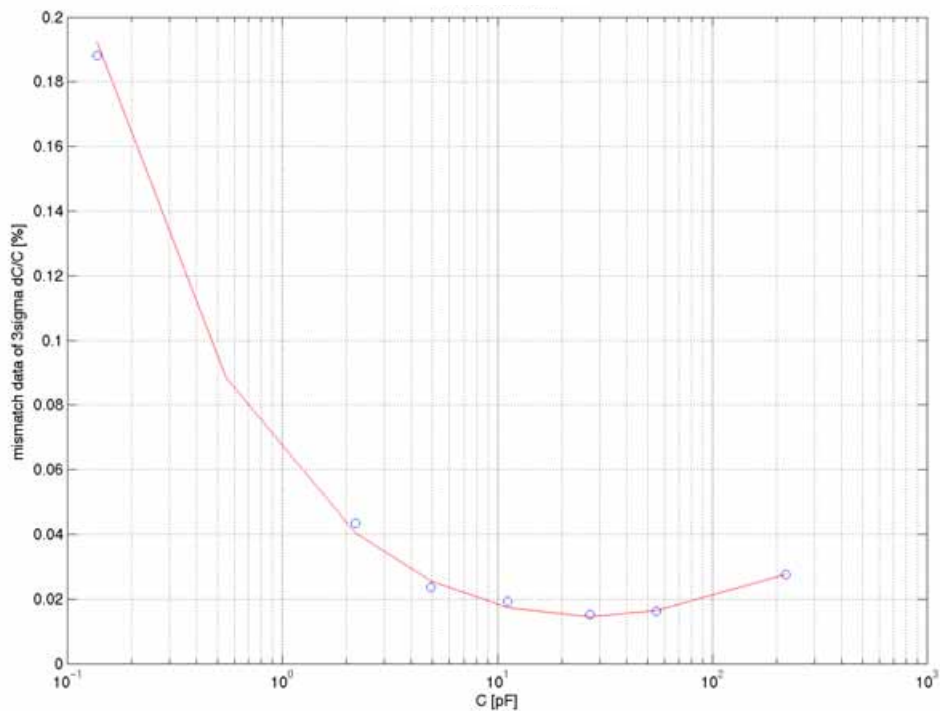


FIGURE 9.12 5.6fF MiM Matching Data (circles) vs. Model (solid line) (spacing=4 μ m)

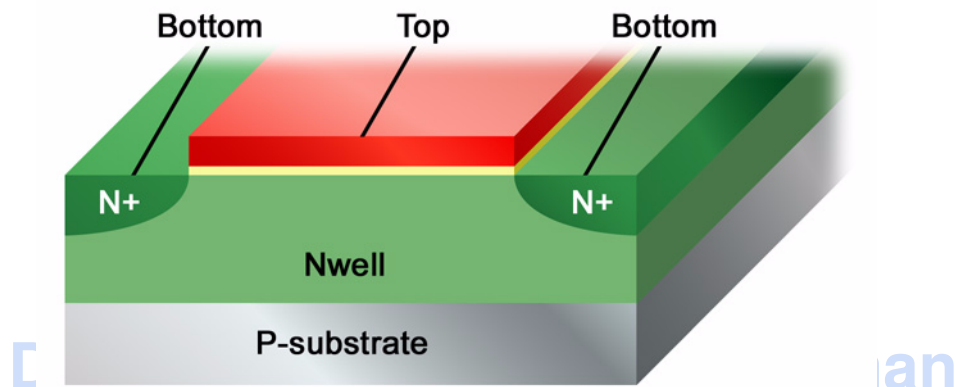


9.2 Poly Capacitor (CPOLY, CPOLY3P3) model

9.2.1 Device Description

Poly capacitors are formed by MOS structures with Nwell beneath the n+ poly gate and n+ Nwell contacts as shown in Figure 9.13. Without p+ source/drains, there is no source for inversion charge, resulting in depletion capacitance in inversion. Maximum capacitance is achieved in accumulation when the poly gate is positively biased with respect to the Nwell. The device is available in thin oxide (library name: **cpoly**) and thick oxide (library name: **cpoly3p3**) versions. The **cpoly** device is exactly the same in cross section to the MOS varactor. The difference between the **cpoly** device and the MOS Varactor is in layout and modeling.

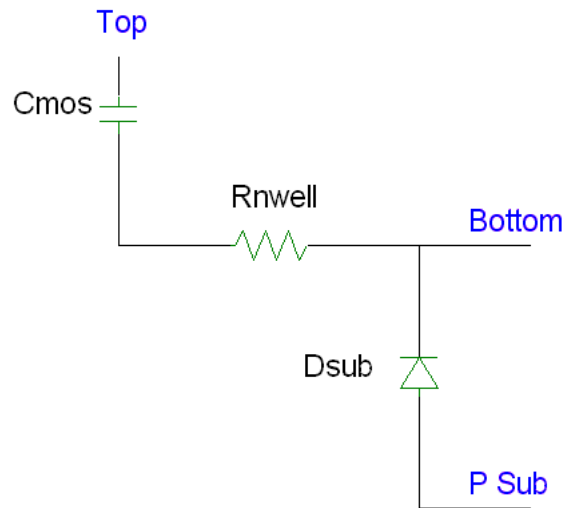
FIGURE 9.13 Poly Capacitor cross-section



9.2.2 Model Description

Figure 9.14 shows the sub circuit model for the **cpoly** device. The model consists of MOS capacitance (emulated through a BSIM element) in series with a Nwell resistance. The parasitic Nwell/Psub junction diode is also included. **The capacitance model is accurate for large plate geometries ($L > 2\mu\text{m}$, $W > 2\mu\text{m}$).** The Nwell resistance is estimated in order to give reasonable simulations of RC effects. **The *cpoly* or *cpoly3p3* devices should not be used in varactor applications.** For varactor applications which require accurate capacitance and parasitic modeling over bias, frequency and geometry, the **varactor_mos** device should be used.

FIGURE 9.14 Poly Capacitor Sub-circuit description



9.2.3 Model Verification

Figures 9.15 through 9.18 show the measured and simulated CV data for **cpoly** and **cpoly3p3** devices.

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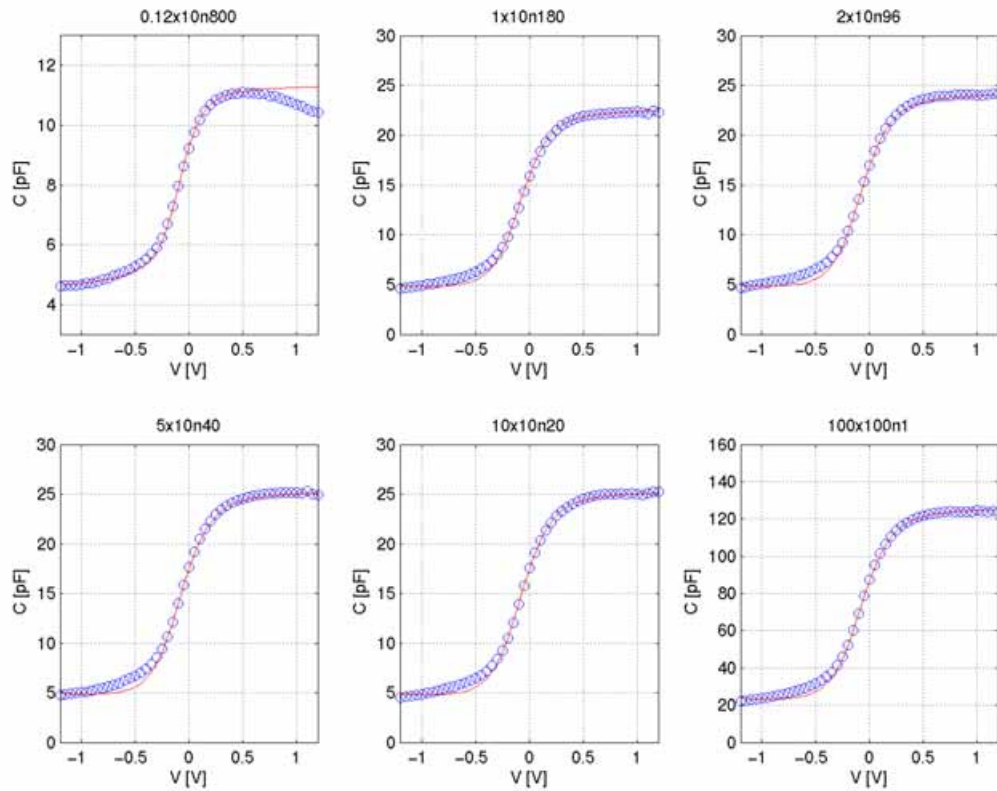
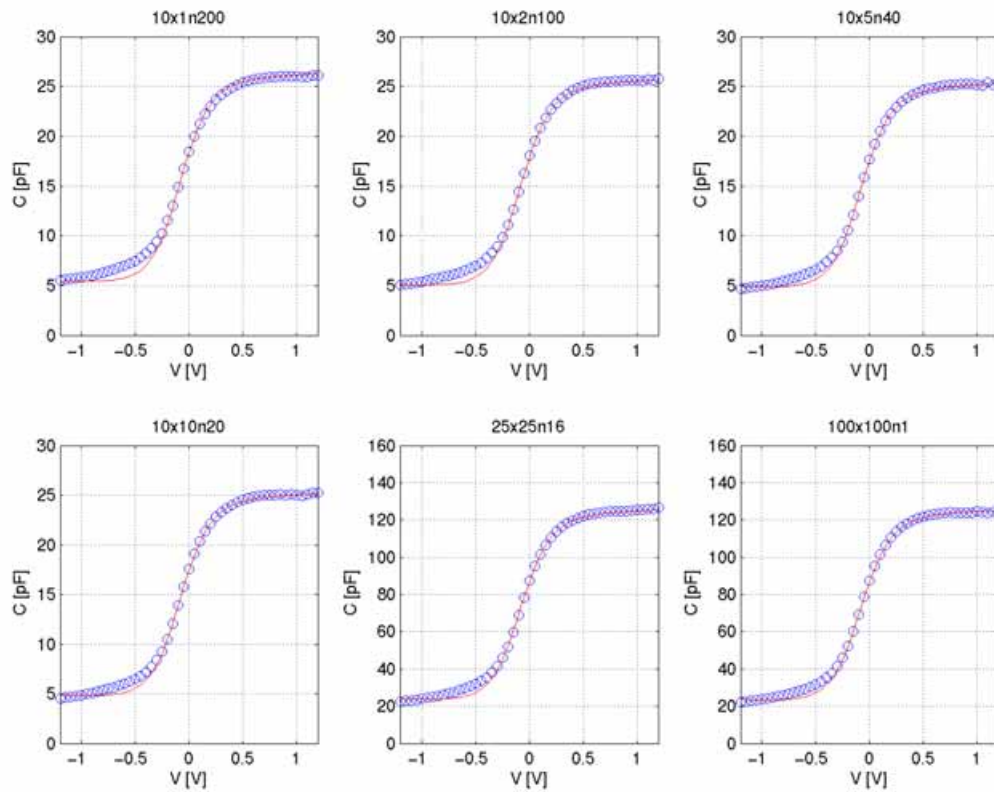
FIGURE 9.15 *cpoly* - varying L_g FIGURE 9.16 *cpoly* - varying W_g 

FIGURE 9.17 *c3p3poly* - varying L_g

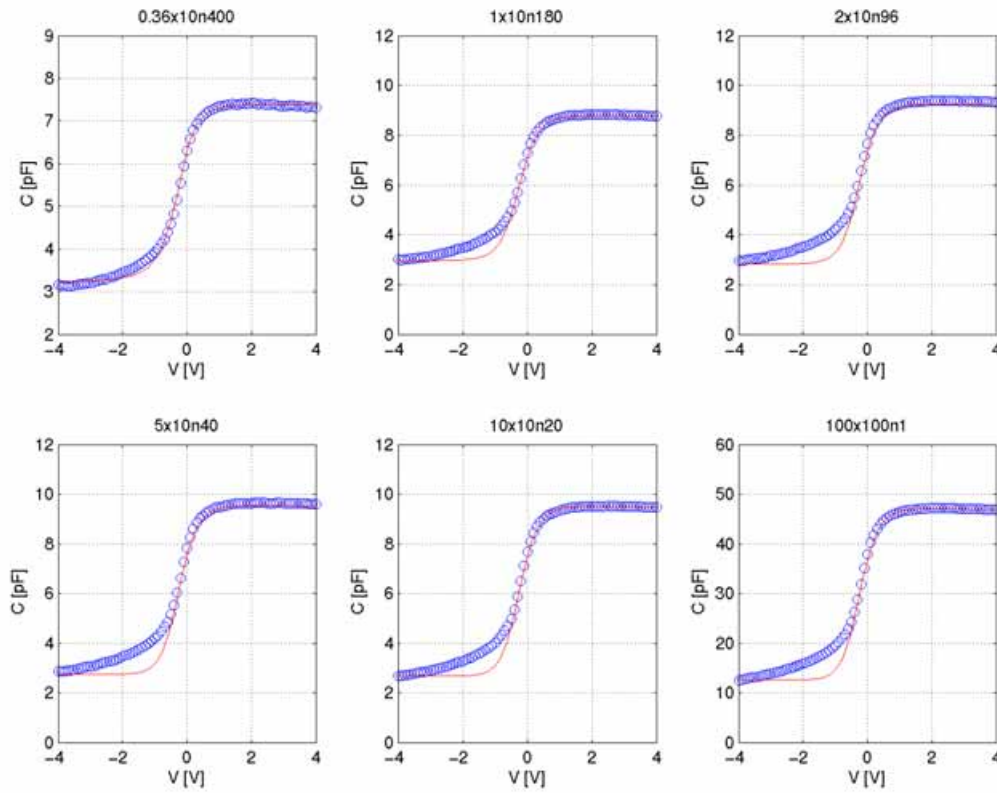
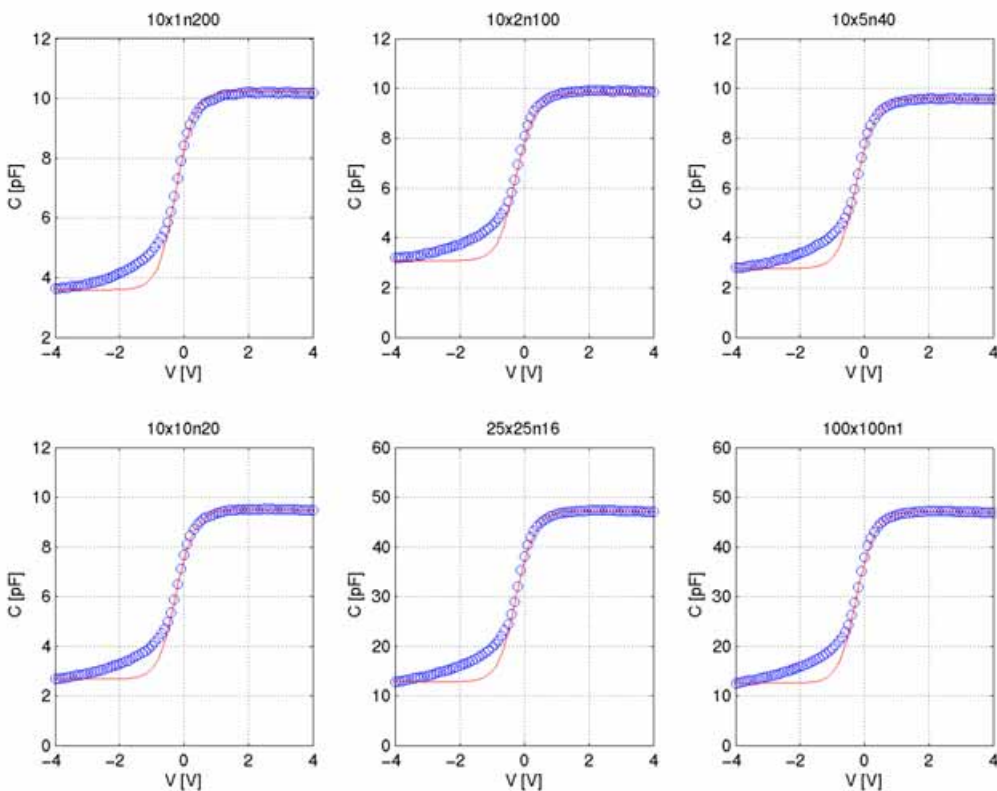


FIGURE 9.18 *c3p3poly* - varying W_g



9.2.4 Poly Capacitor Statistical and Corner Models

The statistical and corner models for the **cpoly** devices are correlated directly with the MOSFETs through the parameters T_{ox} , V_{TH} , ΔW , and ΔL .

9.2.5 Poly Capacitor MisMatch Models

Mismatch models for **cpoly** and **cpoly3p3** are not supported.

9.3 Model Update History

TABLE 9.6 Poly Capacitor model specific updates in model release version 1.7

v1.7 update	Devices	Reason	Impact on user
Re-extraction of the model to include full geometry ranges and POR silicon	All	Previous models based on large plate, causing inaccuracies for dimensions below 2 μ m	Increased accuracy over entire design space

9.3.1 v1.8

No changes

10.0 Inductor Model

10.1 Device Description

The SBL13 design kit provides single-ended and differential inductors with square and octagonal spiral geometry in a 2.81 μm metal process. For single-ended inductors, the kit offers an optional ground shield drawn in silicided active. The capacitive effect of the packaging compound can be taken into account by selecting the dielectric constant of the compound through the inductor Component Description Format (CDF). An inductor instance is defined by its dimensions and can be modified through the CDF. The minimum metal width and metal space is 2.5 μm and 2.0 μm , respectively. A schematic cross section and layout snap shots of single-ended and differential inductors are shown in Figure 10.1 through Figure 10.5. The substrate ties in the cross section view are drawn for completeness of the example. Further information on substrate contacts is given in Section 10.2.6.1 on page 276.

FIGURE 10.1 Cross section view of inductor

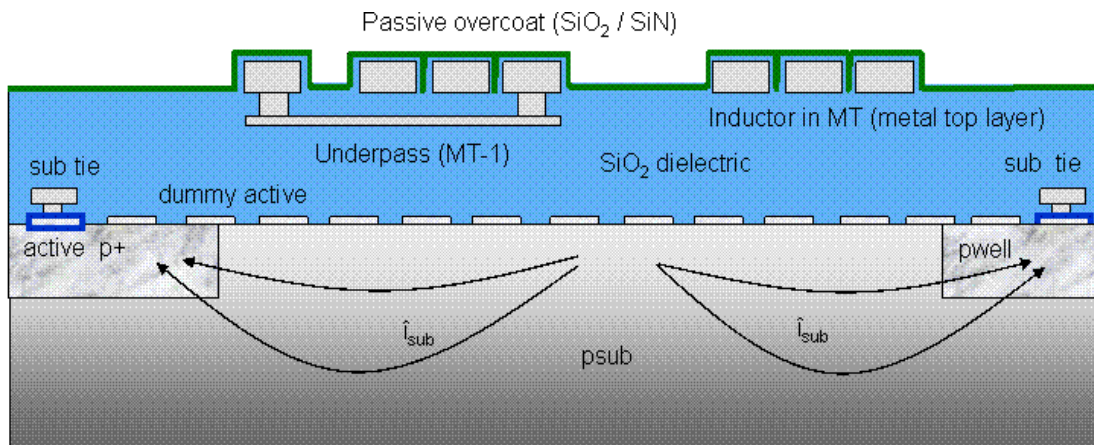


FIGURE 10.2 Square Single-Ended Inductor

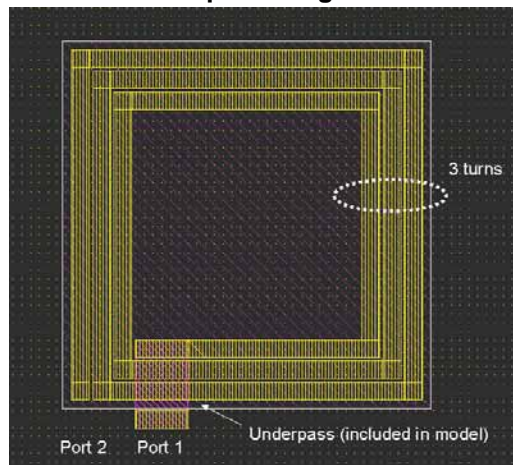


FIGURE 10.3 Square Differential Inductor

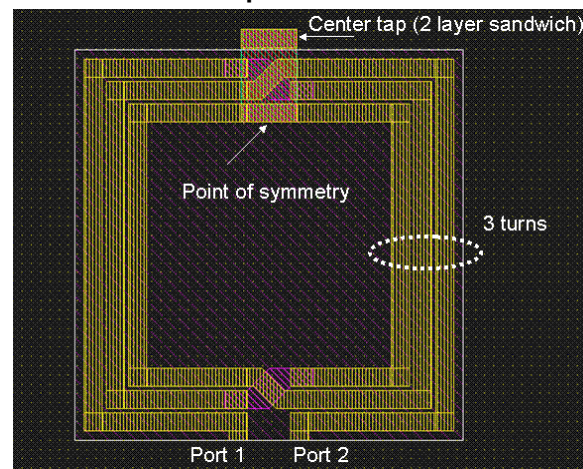
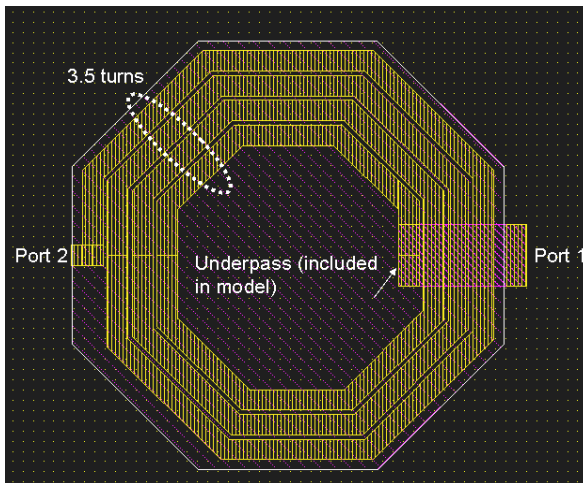
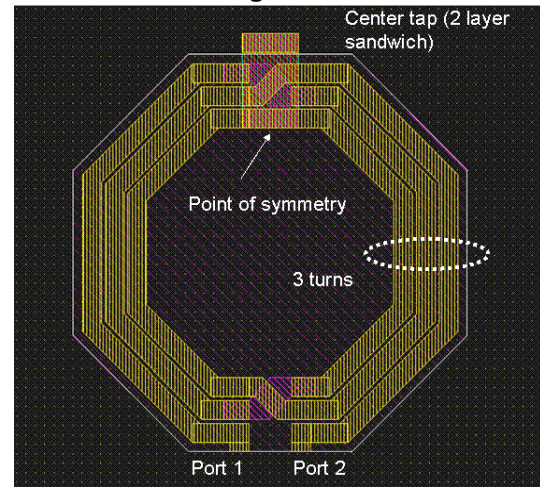


FIGURE 10.4 Octagon Single-Ended Inductor**FIGURE 10.5 Octagon Differential Inductor**

10.1.1 Inductor Layout Generator (PCELL) Confidential

The inductor layout generator creates the layout using the information entered through the CDF properties window. For singled-ended inductors, the inner end is connected to port 1 by an underpass, that is included in the model. The underpass exit can be chosen between “straight” and “perpendicular” which refers to the angle of the underpass to the last spiral segment. While both exit orientations are available on the square inductor for all full and fractional turn numbers, on the octagonal inductor the exit is forced to perpendicular for the fractional quarter turns and can only be chosen between “straight” and “perpendicular” for the full turn layout. The width of the underpass is scaled by a factor 3 with respect to the inductor linewidth. The maximum scaled width is $30\mu\text{m}$, beyond which the underpass width is set equal to the inductor line width.

Differential inductors offer the choice of a center tab through the CDF property. To minimize the dc resistance, the tab width is scaled by 3 to a maximum width of $30\mu\text{m}$. For line width greater $30\mu\text{m}$ the tab width is set equal to the inductor line width. To reduce the parasitic of the tab connection, the tab exit from the symmetric point in the core of the inductor is routed vertically down and then sandwiched in the 2 metal layers beneath the crossover layer. In case that greater flexibility is needed in designing the tab, the layout pcell can be flattened and the tab can be customized. However it should be avoided to run the tab through the core of the inductor to avoid increasing the ac resistance and degrading quality factor Q of the inductor.

The designer must verify that the number of vias drawn at the cross-overs or underpass connections are sufficient to carry the current in the inductor. For allowable current densities please refer to the electrical specifications document. If additional vias are required, the layout pcell can be flattened and vias be added manually.

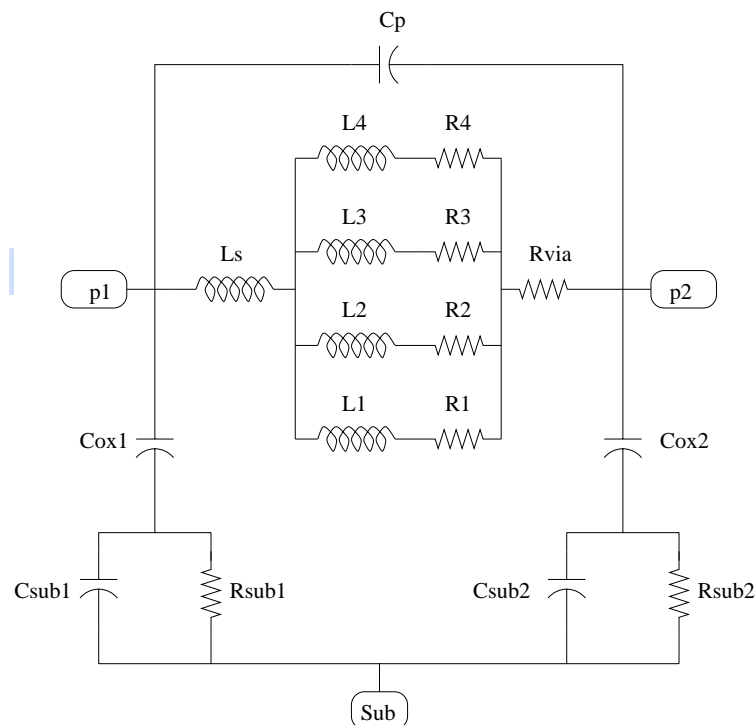
10.2 Model Description

The inductor modeling within the design kit is enabled through the JAZZ Inductor ToolBox (JIT). The JIT is a matlab program which takes as inputs inductor layout parameters and produces netlist component values for the inductor sub circuit model. The layout parameters entered through the inductor CDF in the design kit are outer dimension, line width, line space and number of turns.

10.2.1 Sub-circuit representation

The equivalent circuit representations of single-ended and differential inductors are shown in Figure 10.6 and Figure 10.7, respectively. The individual model components which are listed in Table 10.1, are based on physical models and are computed using geometrical and electrical process specification (espec) information.

FIGURE 10.6 Sub-Circuit Model for Single-Ended Inductor



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FIGURE 10.7 Sub-Circuit Model for Differential Inductor

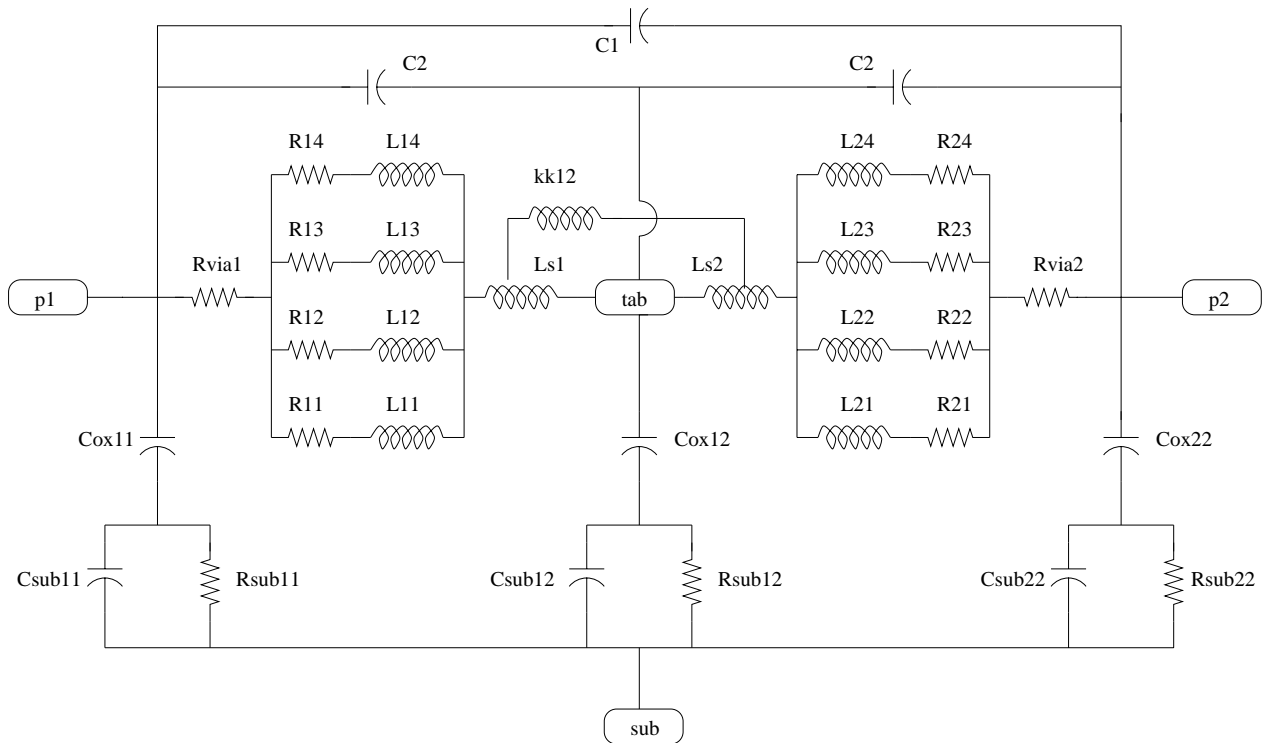


TABLE 10.1 Inductor Model Components

Component	Description
Csub	Substrate capacitance
Rsub	Substrate resistance
Cox	Oxide capacitance
Cp / C1, C2	Interwinding and cross-over capacitance
Rvia	Underpass / cross-over via resistance
Ls	Inductor series inductance
R1 - R4	Ladder resistance components (equal to R of spiral and underpass / cross-over)
L1 - L4	Ladder inductance components (circuit phase equal to phase at low frequency)
kk	Mutual inductance

The radiofrequency (RF) skin effect pushes the current at higher frequencies to the surface of the metal line, effectively increasing the resistance of the inductor (AC resistance). This effect is modeled using a ladder circuit comprised of resistors and inductors that approximate the conductor as 4 concentric shells. The parallel combination of resistors in the ladder circuit resistance corresponds to the DC resistance of the inductor, while the inductance of the ladder corresponds to the internal inductance of the metal trace. This internal inductance is due to the flux linkage of the current to itself and is gradually turned off as the current conducting cross-

section is restricted with increasing frequency. For this reason, a droop of the inductance from the DC value is observed on inductors that are affected by the skin effect.

Series inductance and mutual coupling are calculated using the Grover - Greenhouse formulations [1]. The ac resistance model and the series inductance describe the rising section of the Q curve and determine the peak Q value that is achievable with a particular inductor design.

The interwinding capacitance or feedforward capacitance, electrically couples the ports of the inductors. The oxide capacitance couples the inductor to the substrate. Both capacitances are significant in determining the self-resonant frequency of the inductor. Their values are calculated using a 2 dimensional interconnect solver. The packaging compound material affects primarily the interwinding capacitance whose value will increase with the dielectric constant of the material.

The substrate parasitic resistance is empirically fit to inductor RF measurements. The substrate capacitance is calculated using a simple fringing capacitance formulation. These parasitic affect the roll-off section and the shape of the Q curve.

Single-ended inductors can be drawn over active ground shield to improve the Q value. The subcircuit topology is identical to the case of unshielded inductor in Figure 10.6. Using a ground shield lowers the substrate resistance by moving the ground return path from bulk silicon to the shield structure. The reduced ground return resistance is absorbed into the substrate resistance component, leaving the circuit topology unchanged.

10.2.2 Model selection

The inductor CDF allows for selection of geometric information of “Xsize”, “Ysize”, “Width”, “Spacing”, “Number of Turns” and information on operating frequency and frequency range. After modification of these properties, the inductor performance results and sub circuit component values for the nominal case at the nominal temperature of the circuit simulator are calculated and displayed. For proper simulation results it is necessary to include a substrate pin connected to ac ground into the schematic. The substrate pin name must be identical to the CDF parameter name defined under “Substrate Node”.

For differential inductors, the center tap connection point is included in the model. Simulated results returned from the RF simulation engine and inductor performance CDF results listed in Table 10.2 must match closely.

TABLE 10.2 Inductor CDF Performance Results

Performance	Description
PeakQ / PeakqDiff	maximum Q value
FPeakQ / FPeakqDiff	frequency at Peak Q
SRF / SRFDiff	self resonance frequency
Qinterest / QinterestDiff	Q value at operating frequency
Linterest / LinterestDiff	effective inductance at operating frequency
Rinterest / RinterestDiff	effective resistance at operating frequency

TABLE 10.2 Inductor CDF Performance Results

Performance	Description
Lfgoes0 / Lfgoes0Diff	effective inductance as frequency approaches zero (Ldc)
Rfgoes0 / Rfgoes0Diff	effective resistance as frequency approaches zero (Rdc)

The performance data for single ended and differential inductors are calculated differently. In single-ended configuration, the port 1 terminal at the inner end of the spiral inductor is connected to ac ground. The resulting impedance seen at the outer terminal port 2 is:

$$R + j \cdot X = \frac{1}{Y_{22}} \quad (\text{EQ 1})$$

In differential configuration, the ground connection of the equivalent circuit is assumed a virtual, floating ground and the resulting impedance from port 1 to port 2 is:

$$R + j \cdot X = Z_{11} + Z_{22} - 2 \cdot Z_{12} \quad (\text{EQ 2})$$

The reported metrics in the differential inductor CDF use the impedance from port to center tab, which is half the value from port 1 to port 2 or:

$$R + j \cdot X = \frac{1}{2} \cdot (Z_{11} + Z_{22} - 2 \cdot Z_{12}) \quad (\text{EQ 3})$$

The inductor Q, L and R as reported in the inductor CDF are calculated from the single-ended or differential impedance Z_L :

$$Q = \frac{\text{imag}(Z_L)}{\text{real}(Z_L)} \quad (\text{EQ 4})$$

$$L = \frac{\text{imag}(Z_L)}{2 \cdot \pi \cdot \text{freq}} \quad (\text{EQ 5})$$

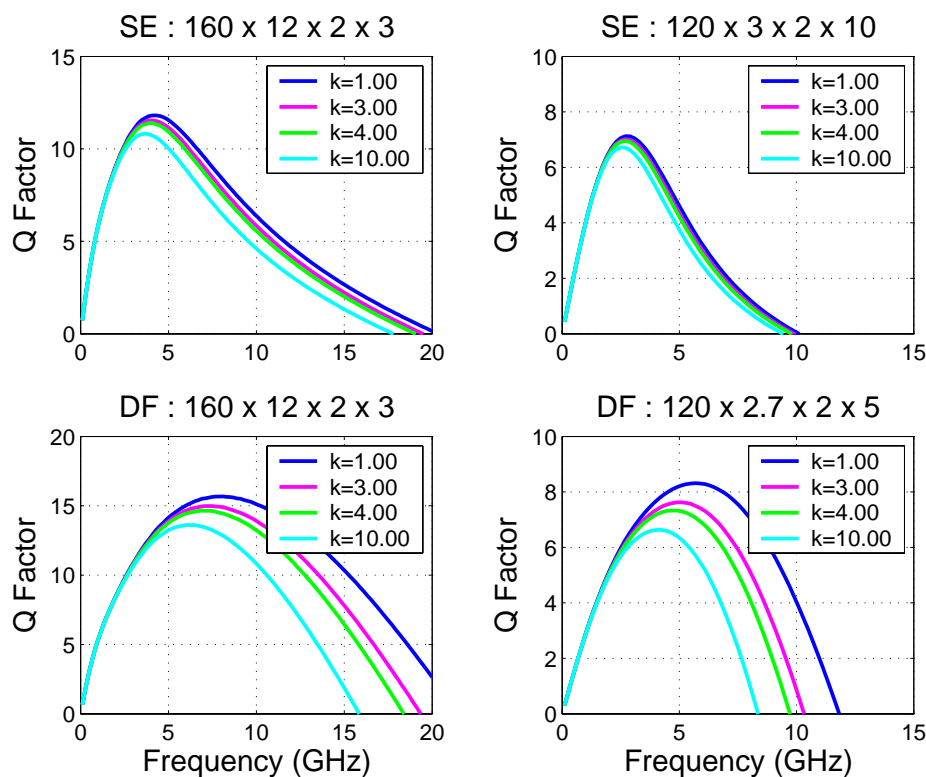
$$R = \text{real}(Z_L) \quad (\text{EQ 6})$$

Since the parasitic capacitance of the underpass exit of the single-ended inductor is associated with the inner terminal port 1, the Q at port 2 is higher than the Q at port 1. In single-ended analysis, the admittance Y_{22} in the impedance equation is replaced by admittance Y_{21} to extract series inductance and series resistance.

10.2.3 Packaging Compound Material

The packaging compound material affects the interwinding capacitance and its value will increase with the dielectric constant of the material. Through the CDF a relative permittivity ϵ_r in the range from 1 to 10 can be entered to account for the effect of the packaging dielectric on the inductor performance. The default value is 1 which represents air. Increasing ϵ_r will reduce the Q and self-resonant frequency of the inductor. Due to its stronger sensitivity to the interwinding capacitance, the differential inductor performance is more affected by the packaging material than the single-ended inductor. An example of the Spectre simulated Q curve on 4 inductors in the sbl13 process as a function of various packaging dielectric permittivities is provided with Figure 10.8.

FIGURE 10.8 Effect of Packaging Compound on Inductor Q

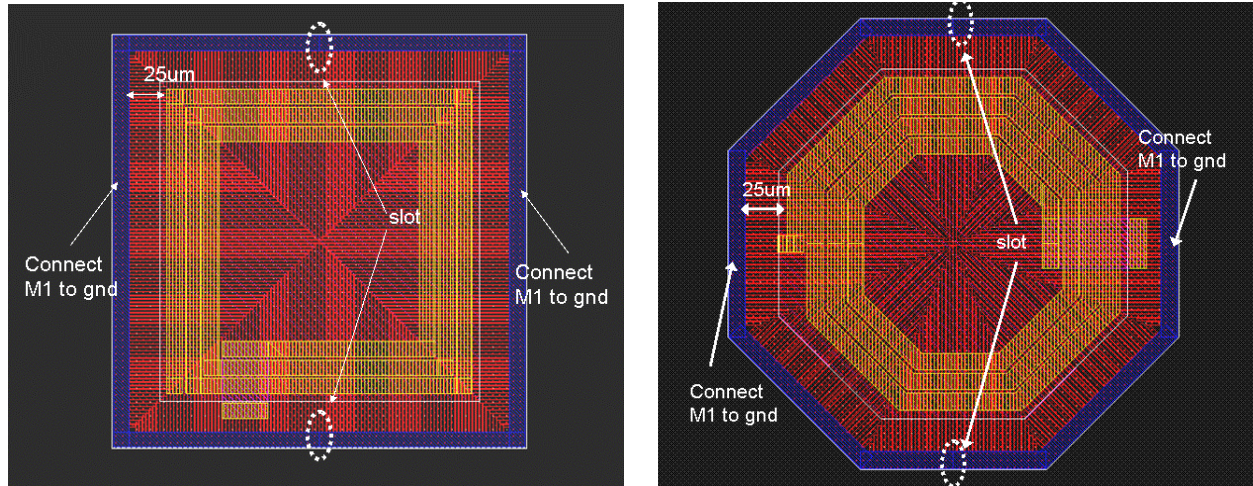


10.2.4 Ground Shield in Silicided Active

For single-ended inductors the Q performance can be boosted and noise isolation improved by inserting a ground shield below the inductor. A layout snapshot of square and octagonal inductors with shield is shown in Figure 10.9. The shield is by default 25 μ m per side larger than the inductor (outside edge of inductor to inside edge of shield metal 1). A metal 1 frame at the perimeter of the shield connects the shield fingers which are drawn in active, keeping the resistive loss over the shield small. This frame is slotted at the top and bottom to

prevent a closed current loop and should be connected to ac gnd at the 2 sides of the frame segment. The connection however must not short out the slots.

FIGURE 10.9 Single-Ended Inductors with Gnd Shield



The shield fingers are drawn in silicided p+ active and are located in a n-epi layer (weak nwell). This configuration isolates the shield from the silicon substrate through a “pn”-junction. A schematic drawing of the shield and associated junctions is shown in Figure 10.10. This configuration was used for silicon model validation.

To improve noise isolation, the n-epi can be connected to vdd to minimize any diode current by keeping the “pn” –junctions zero or reverse biased as shown in Figure 10.11. The substrate noise will be shunted to ac ground reducing RF noise coupling with the neighboring area. This configuration has not been silicon validated. Not connecting the substrate, i.e. leaving it floating does not impair the function of the active shield

FIGURE 10.10 Shield Connection

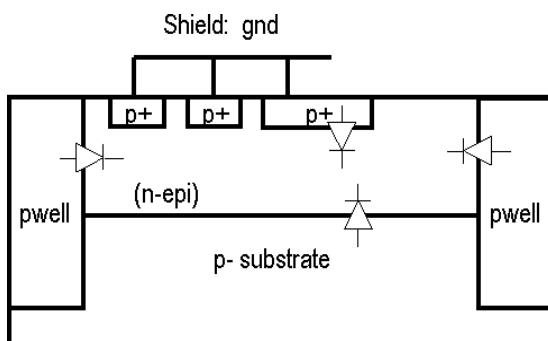
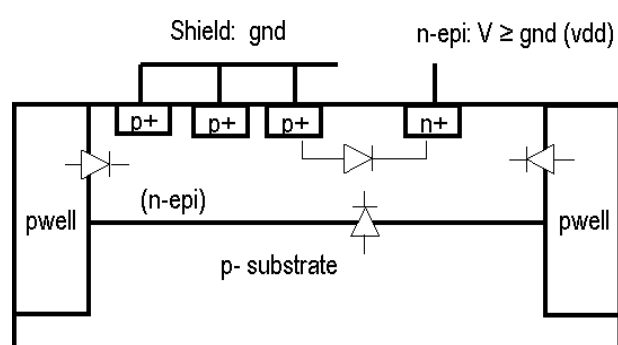


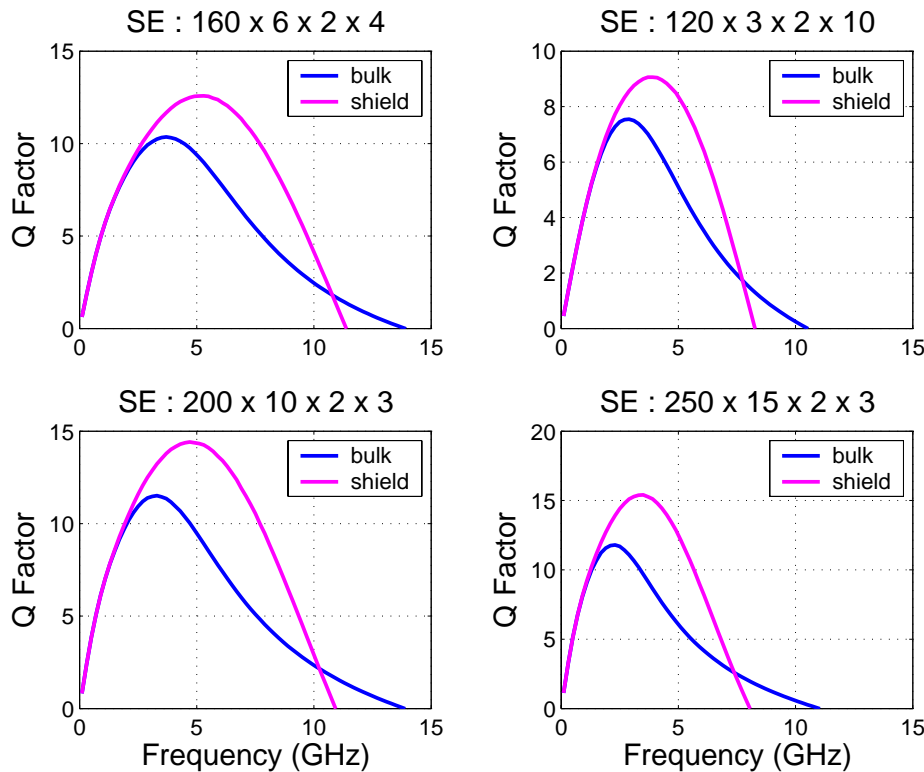
FIGURE 10.11 Shield with Noise Shunt



The ground shield structure defines an alternative current return path at a lower resistance than the return path through silicon to substrate contacts for the unshielded case. Since the resulting substrate resistance is much

lower, a very different dome-like shape Q curve is obtained, rendering the Q more broadband. The effective capacitance to the substrate is increased, approaching C_{ox} as the return path resistance decreases, reducing the self-resonant frequency. An example of the Spectre simulated Q curve on 4 square inductors in the sb113 process with and without shield is shown in Figure 10.12.

FIGURE 10.12 Effect of Shield on Inductor Q



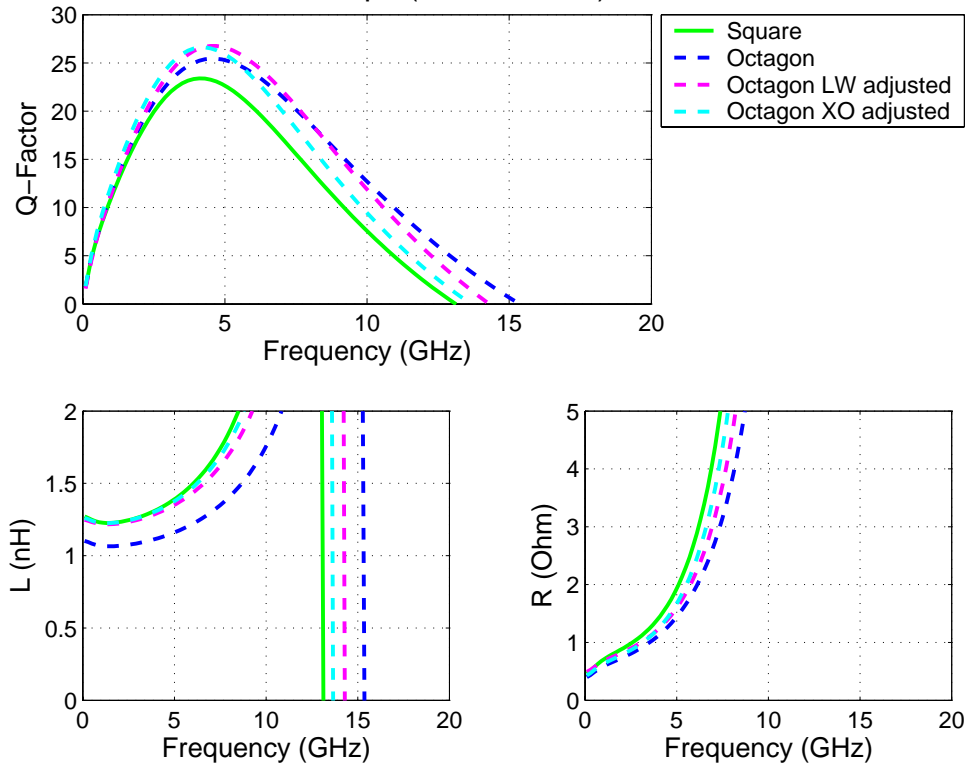
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10.2.5 Octagonal Geometry

The performance of the inductor Q can be improved by using an octagonal geometry over the square geometry. When comparing a differential inductor with the same dimensions in square and octagon shape, the trace of the octagon is 17.2 % shorter than the square leading to a higher Q and SRF with lower L and R (EM simulated Q on 5.26 μm M5 inductor in Figure 10.13). If the octagonal design is adjusted by reducing the line width or by increasing the outer dimension to match the same low frequency inductance and resistance as the square design, it can be seen that the octagon has an inherently better Q than the square inductor.

The differential inductor layout pcell allows a minimum of 1 turn for the octagon while the square differential requires a minimum of 2 turns. The single-ended device starts with 1.25 turns for both octagon and square layouts. A layout snapshot of minimum turn octagonal inductors is shown Figure 10.14 and Figure 10.15. The single-ended octagon is asymmetric in its layout with the lower left quadrant sides forming the “step-in” turn. A symmetric layout 1 turn single-ended device can be realized by using the 1 turn differential inductor without the center tab.

FIGURE 10.13 Q-Performance for Octagon versus Square
 DF : 240x15x3x3p0 (sbc18m5-5u)



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FIGURE 10.14 Single-Ended Octagon
 N=1.25

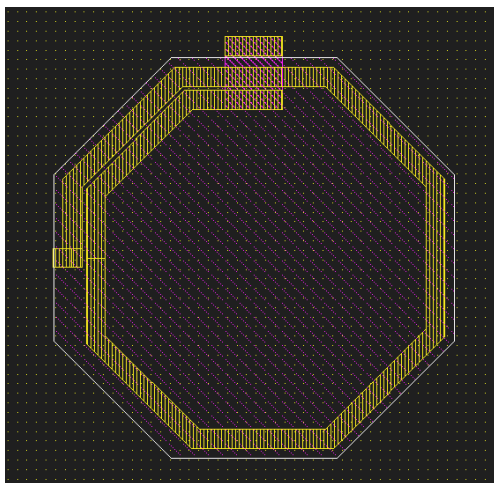
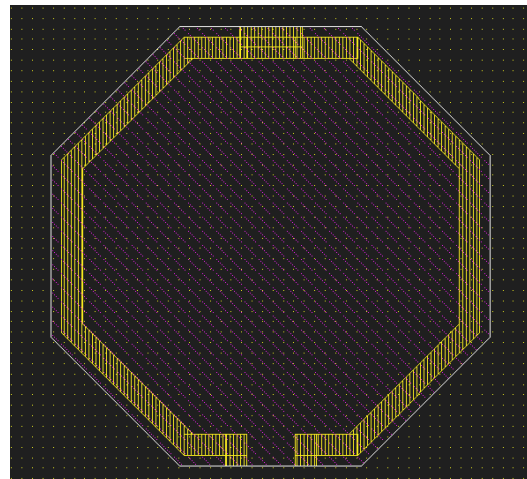


FIGURE 10.15 Differential Octagon N=1



10.2.6 Model Accuracy

10.2.6.1 Substrate Contacts

The ground-signal-ground 2-port test structure used for RF measurement on the intrinsic inductor structure, ties the silicon substrate to the equipment ground of the RF probestation and network analyzer. These substrate ties are at a distance of 75 μm - 100 μm from the inductor. To provide balanced ground return [3], the ground pads are connected between both S-parameter ports by a 100 μm wide bar in top metal which is surrounding the inductor, rendering the structure essentially into a coplanar waveguide. This configuration provides an ideal return path for the signal current to flow back through this bar to the ground probes of the port from which the signal originated. In an actual chip design this bar may not be present, but the measurement obtained on the structure with ideal return path will correspond to the intrinsic inductor as used in the design.

Substrate contacts are not included in the layout PCELL and need to be carefully considered when manually added in the vicinity to the inductor [4]. For a single-ended inductor, substrate ties within approximately 75 μm will affect the Q of the inductor. Generally an increase in Q is observed by reducing the substrate resistance. Concurrently, the effective capacitance to the substrate is increased, approaching C_{ox} in the limit of $R_{sub}=0$ (see Figure 10.6). Thus, the self resonance decreases due to the added capacitance. For differential inductors, substrate ties within 75 μm can cause asymmetry, degrading the Q [4]. In both cases the tie ring should not be a closed loop to avoid an induced current loop from lowering the inductor L through negative mutual coupling.

10.2.6.2 Inductor Q and Current Crowding

The models are verified for inductors using a line space of 2 μm and inductance values greater than 0.3 nH. Inductors with a high layout density suffer from excessive ac resistance due to the proximity or current crowding effect [5]. This effect is not included in the models and such inductors will not be modeled accurately in terms of ac resistance and Q factor. The JIT warns the user of poor inductor designs with a message prompting to reduce the layout density to below 75 %. The inductor search tool that can be accessed through the inductor CDF offers a database of approximately 5000 single-ended inductors and 1800 differential inductors that are modeled well and do not exhibit the proximity effect issue.

10.2.6.3 Inductor Q Extraction

The traditional approach to Q extraction which is used for the design manual plots and for the JIT reporting in the unix background window from which the design kit was invoked, defines Q as the ratio of imaginary part of impedance to the real part of impedance

$$Q = \frac{\text{imag}(Z_L)}{\text{real}(Z_L)} \quad (\text{EQ } 7)$$

This arbitrary definition has the awkward property that the Q is zero at self-resonance when the reactive terms of capacitance and inductance cancel and the impedance is purely real. In some applications when the inductor is used as a resonant tank, a more appropriate method of defining Q would be to use the 3 dB

bandwidth of impedance or the rate of change of phase of admittance when the inductor is shunted with a capacitor to resonate it at the frequency of interest [6]. The resulting admittance of inductor and shunt capacitor is

$$Y = \frac{1}{Z_L} + j \cdot \omega \cdot C_{Shunt} \quad (\text{EQ 8})$$

The shunt capacitance will resonate the device at the frequency of interest ω_0 canceling the admittance of the inductor.

$$C_{Shunt} = -\frac{\text{imag}\left(\frac{1}{Z_L}\right)}{\omega_0} \quad (\text{EQ 9})$$

For each frequency, the device is shunted to resonate. The Q at this frequency is calculated by dividing the frequency point f_0 by the 3dB frequency bandwidth of the magnitude of impedance of the shunted device.

$$Q = \frac{f_0}{\Delta f_{3dB}} \quad (\text{EQ 10})$$

Alternatively, the incremental change in phase of admittance at the frequency point f_0 can be used to calculate Q.

$$Q = \frac{f_0}{2} \cdot \left(\frac{\angle Y(f_0 + \Delta f) - \angle Y(f_0 - \Delta f)}{2 \cdot \Delta f} \right) \quad (\text{EQ 11})$$

Both methods return the same result but are fundamentally different to the result using equation [7]. These alternative methods are more computational intensive and require a finer frequency stepsize for the impedance vector to lead to a stable converged Q result. A resolution on the order of 10 MHz was found suitable and can be generated from the measurement or simulation data using cubic spline fitting. An example of shunt capacitance over frequency, tuned inductor and the Q results obtained with the different methods on measurement data of 2.81 μm M4 single-ended and differential inductors is shown in Figure 10.16 and Figure 10.17, respectively.

FIGURE 10.16 Q Methods on Single-Ended Inductor

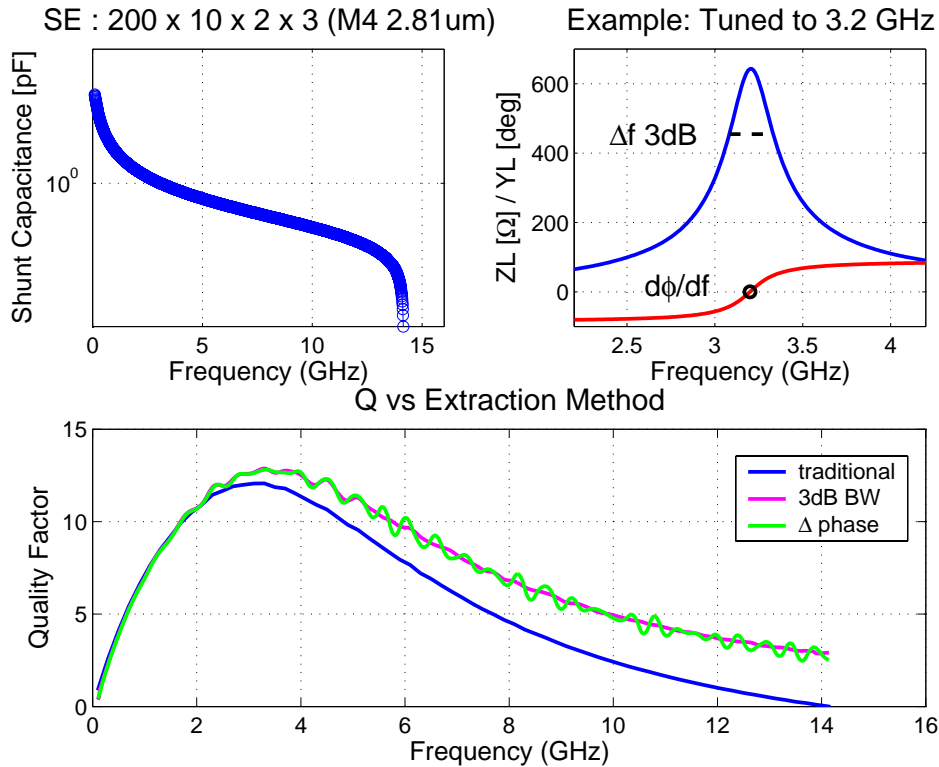
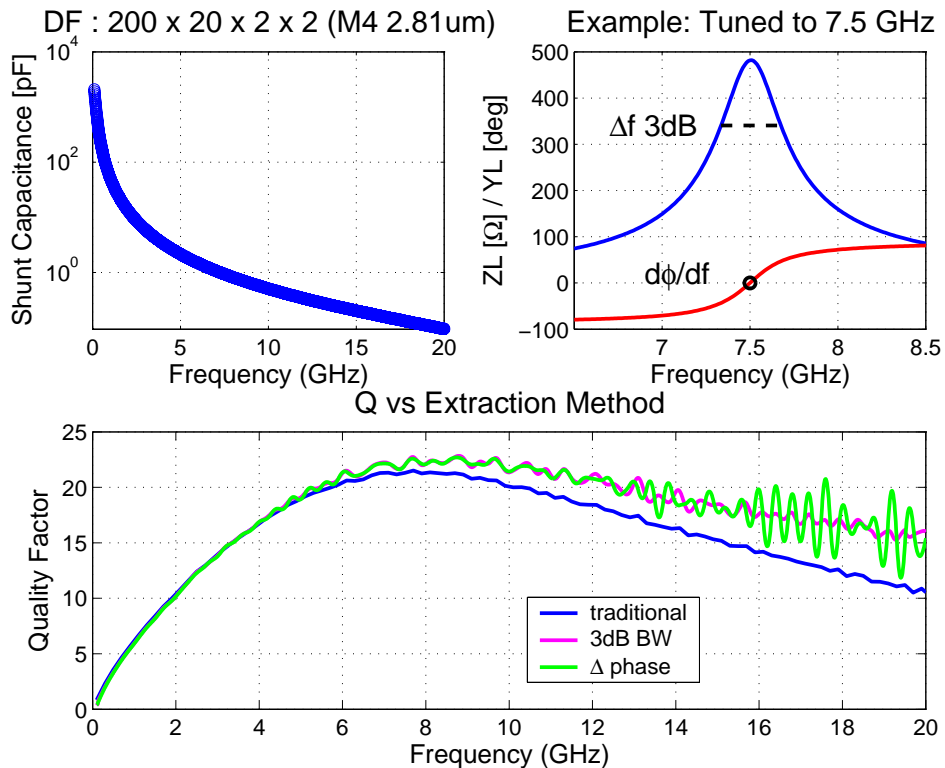


FIGURE 10.17 Q Methods on Differential Inductor

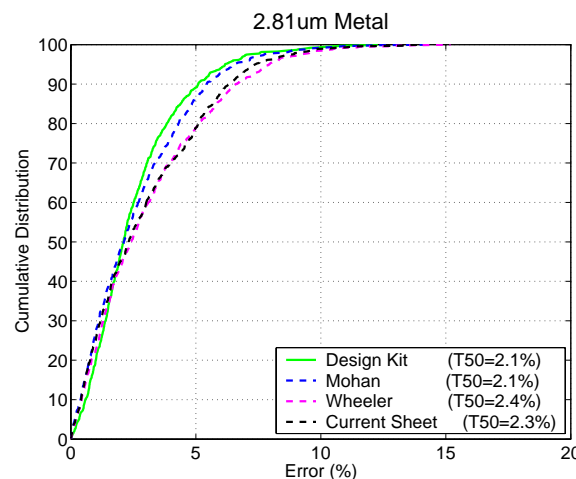


10.2.6.4 Inductance Accuracy

10.2.6.4.1 Square Geometry Inductors

Since it is difficult to obtain an accurate inductance result for the intrinsic device due to inherently small inductance on most inductor designs and contributing effects from the signal feeds, the accuracy of dc inductance was determined through comparison to electromagnetic simulations. The design kit model results on a set of 750 inductors with inductances ranging from 0.3 nH to 12 nH were bench marked against ASITIC [7] numerical simulations, similar to the study described by Mohan et.al [8]. The model inductance is calculated with the JIT using the Grover - Greenhouse equations on the inductor layout as generated by the design kit layout PCELL. ASITIC constructs and solves inductance and capacitance matrices if a low frequency, for example 1 kHz is chosen, which is the electrical analog to solving Maxwell's equation. For comparison, the inductance was also computed using Mohan's empirical equation, modified Wheeler and modified current sheet equations, all described by Mohan et.al. Figure 10.18 shows the cumulative inductance error distributions with respect to the ASITIC result for 2.81 μm metal square inductors. From the cumulative error plots, a typical inductance error of 2.1 % (median or T50) is obtained demonstrating the accuracy of the design kit equations. The JIT results are slightly better than the alternatives provided by Mohan. The connecting feed lines to the inductor are not included in the design kit model and need to be accounted for separately by inductance extraction on the actual layout.

FIGURE 10.18 Cumulative Error of DC Inductance (Square Inductors)



10.2.6.4.2 Octagonal Geometry Inductors

The accuracy of the inductance models for octagonal single-ended and differential inductors were benchmarked against MIT's FastHenry [9]. FastHenry is a three-dimensional inductance extraction program that computes the frequency dependent self and mutual inductances and resistances between conductors of complex shape.

The difference of the inductance result between design kit model and FastHenry is shown on a large set of 4455 octagonal single-ended inductors and 1485 octagonal differential inductors in 2.81 μm metal process in Figure 10.19 and Figure 10.20. The geometry space covered by the histograms ranges from 3 to 35 μm line width, 2 to 10 μm line space and 1 to 9 turns. The JIT results are well within 2 % of the FastHenry result. The connecting feed lines to the inductor are not included in the design kit model and need to be accounted for separately by inductance extraction on the actual layout.

FIGURE 10.19 Inductance Calculation Accuracy (Octagonal Single-Ended Inductor)

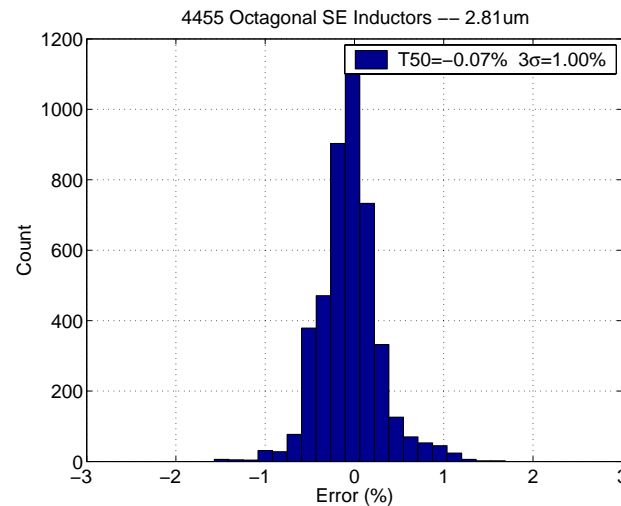
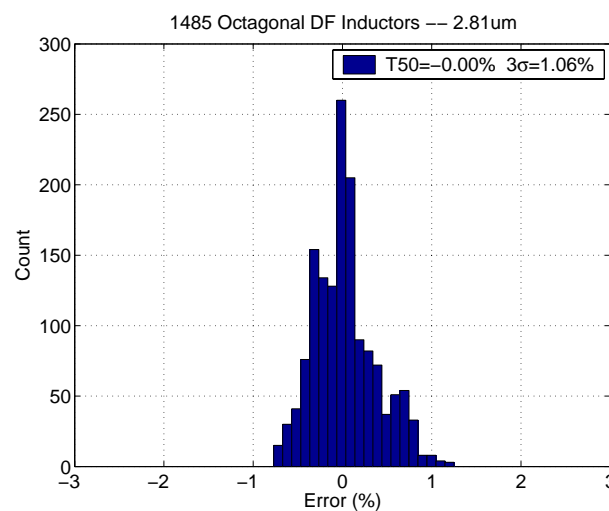


FIGURE 10.20 Inductance Calculation Accuracy (Octagonal Differential Inductor)



10.3 Model Verification

10.3.1 Silicon Validation

The inductor models have been verified by comparing measured high frequency characteristics at 25°C temperature with the Spectre simulation on the corresponding intrinsic device. Since the inductor verification in silicon requires the use of ground-signal-ground pads and feed lines to connect the device, the measurement results are afflicted with considerable parasitic capacitances, inductances and resistances. These parasitic effects were removed from the measured data to yield the intrinsic device by subtracting the pad admittance followed by an ABCD matrix multiplication to remove the feed lines. Any deembedding approach is imperfect and the result will only be the approximate true device. Substrate contacts are located in the ground-signal-ground test fixture which is generally at a distance of 75µm to 100µm to the inductor.

Silicon data is not available yet for sbl13 inductors. In lieu, model verification plots from a M4 process that is fairly close in process specs are shown. The distance from inductor to substrate is 6.98 µm for M6 sbl13 and 7.03 µm for the M4 process. The major difference in both processes is the interlevel dielectric thickness between top and top-1 level metals of 0.70 µm for sbl13 and 2.0 µm for M4. Since the JIT models are fully scaleable over a wide range of foundry processes, accurate model fits similar to the shown data is expected for sbl13.

Examples of Spectre simulated and measured Q, L, R results for various single-ended inductors over silicon substrate and over shield and for square and octagonal differential inductors over bulk silicon are shown in subsequent Figure 10.21 through Figure 10.51. The title describes the inductor type with “SE” for single-ended or “DF” for differential inductor and indicates in parentheses where a shield was used and whether square or octagonal layout for the differential inductors. The geometry information is following the inductor type information in sequence of outer dimension, line width, line space and turns. The specific process and JIT information is marked in the legend.

FIGURE 10.21 Inductor Model Verification

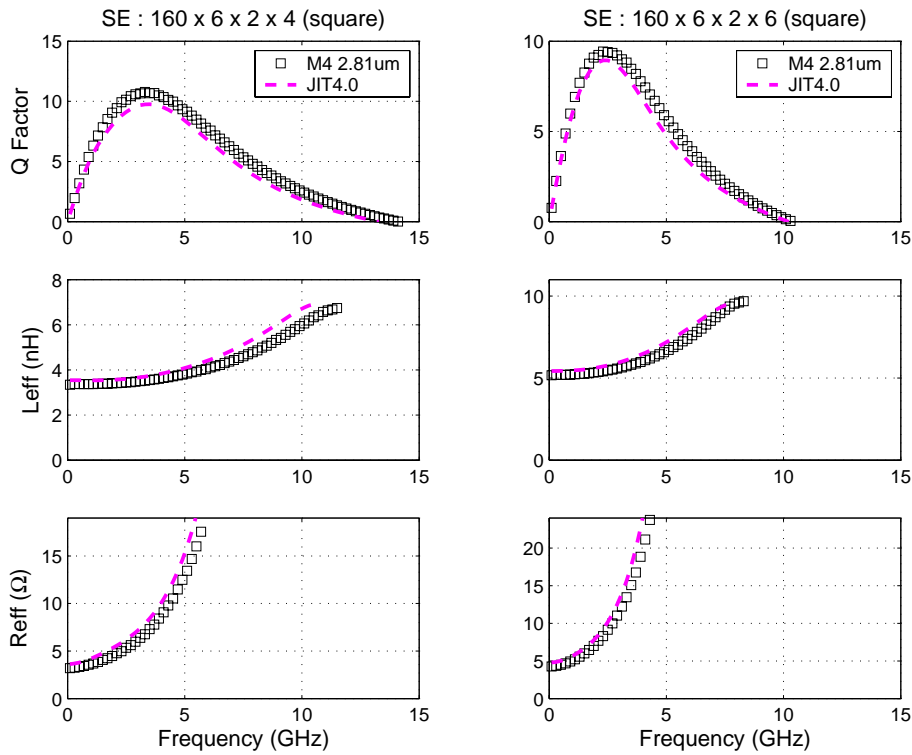


FIGURE 10.22 Inductor Model Verification

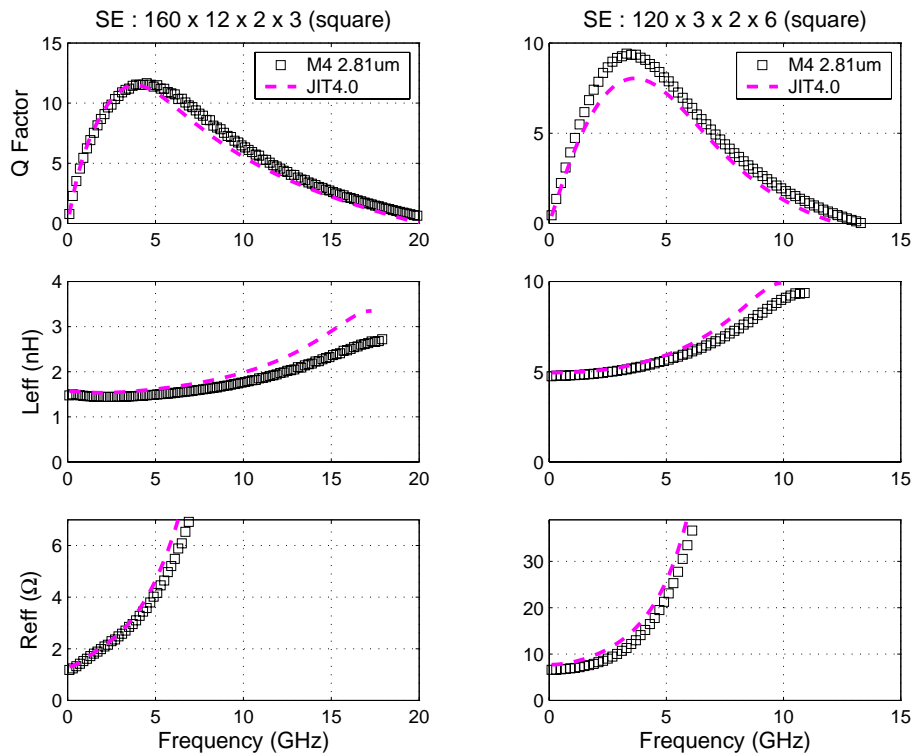


FIGURE 10.23 Inductor Model Verification

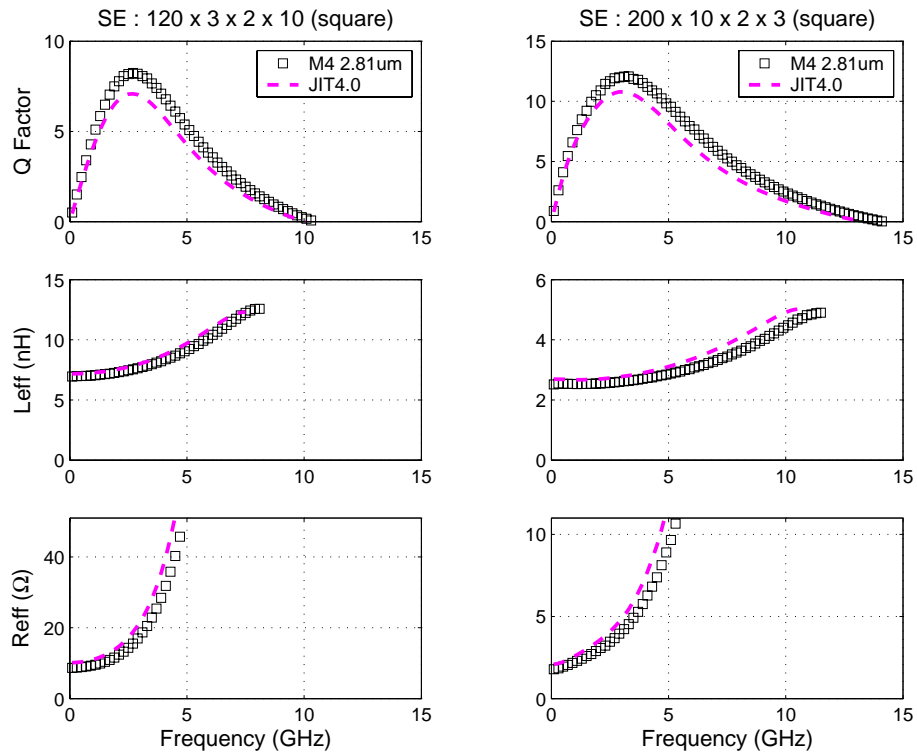


FIGURE 10.24 Inductor Model Verification

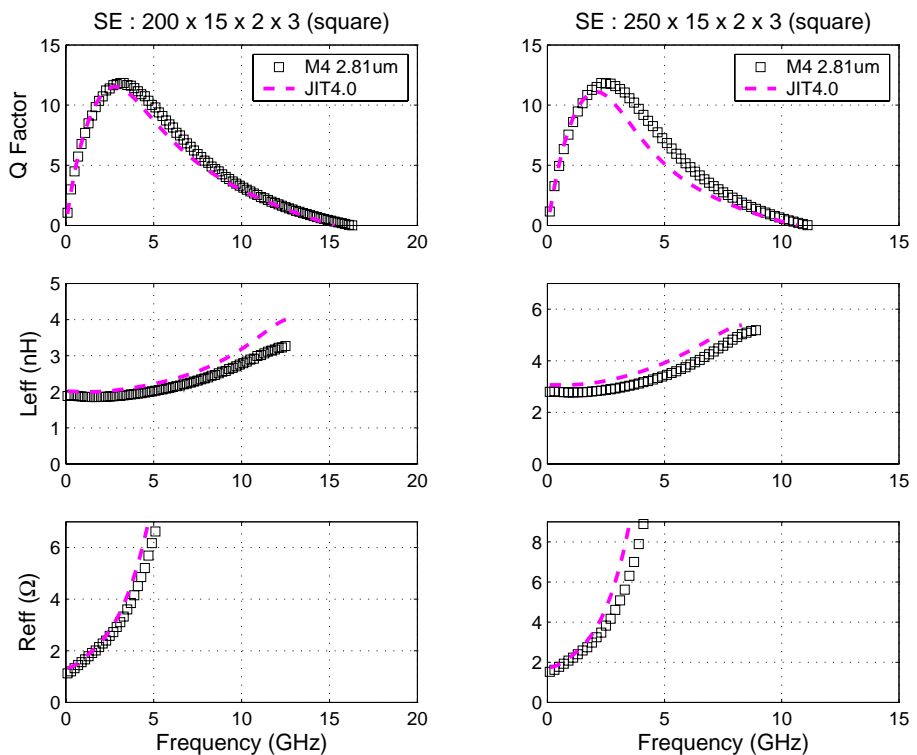


FIGURE 10.25 Inductor Model Verification

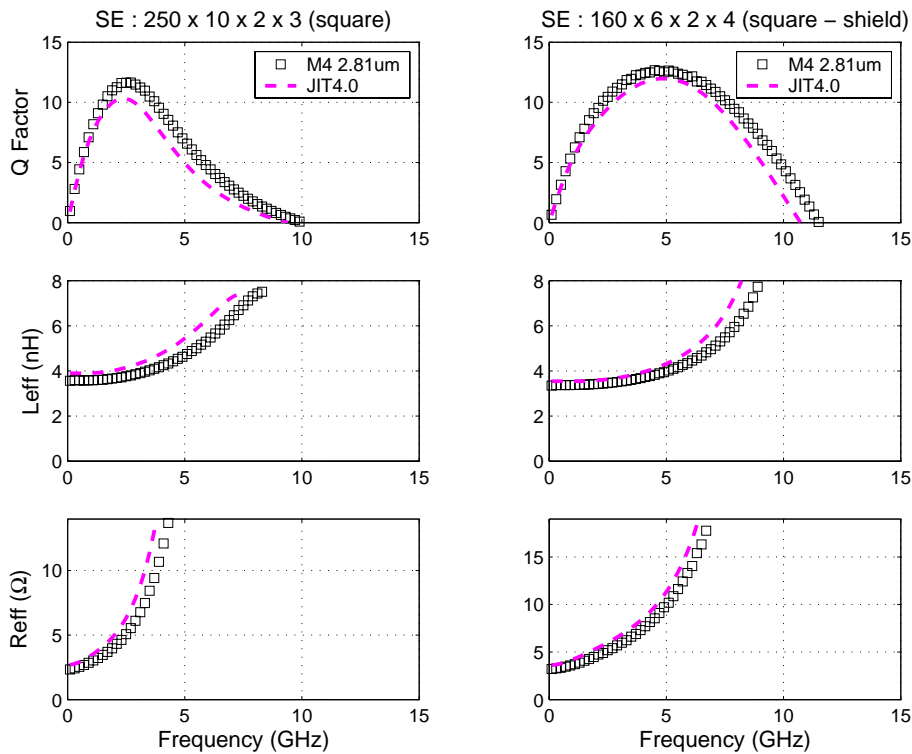


FIGURE 10.26 Inductor Model Verification

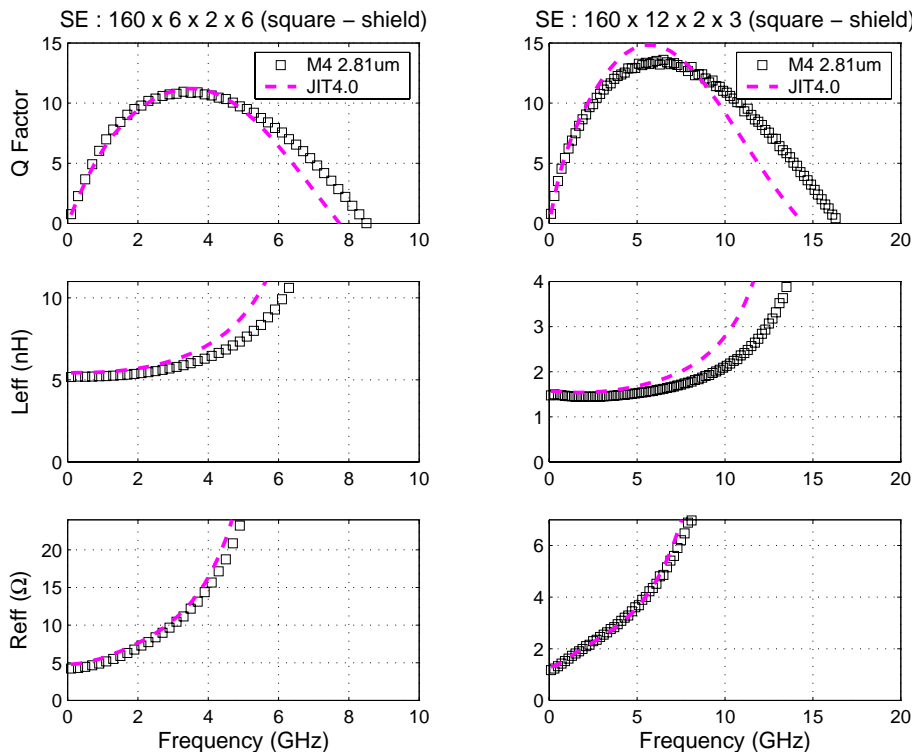


FIGURE 10.27 Inductor Model Verification

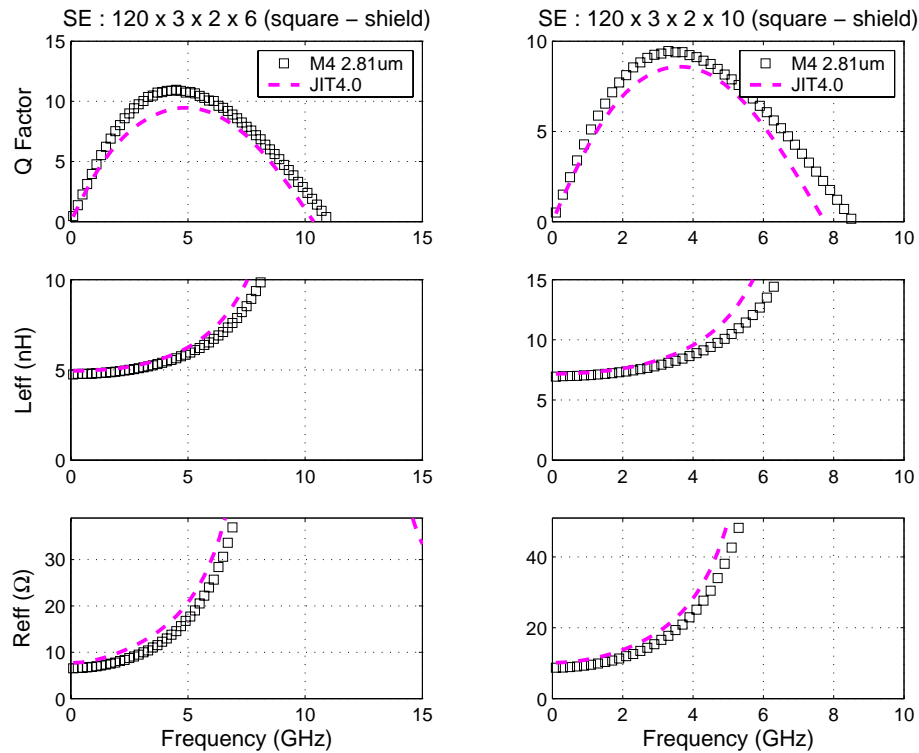


FIGURE 10.28 Inductor Model Verification

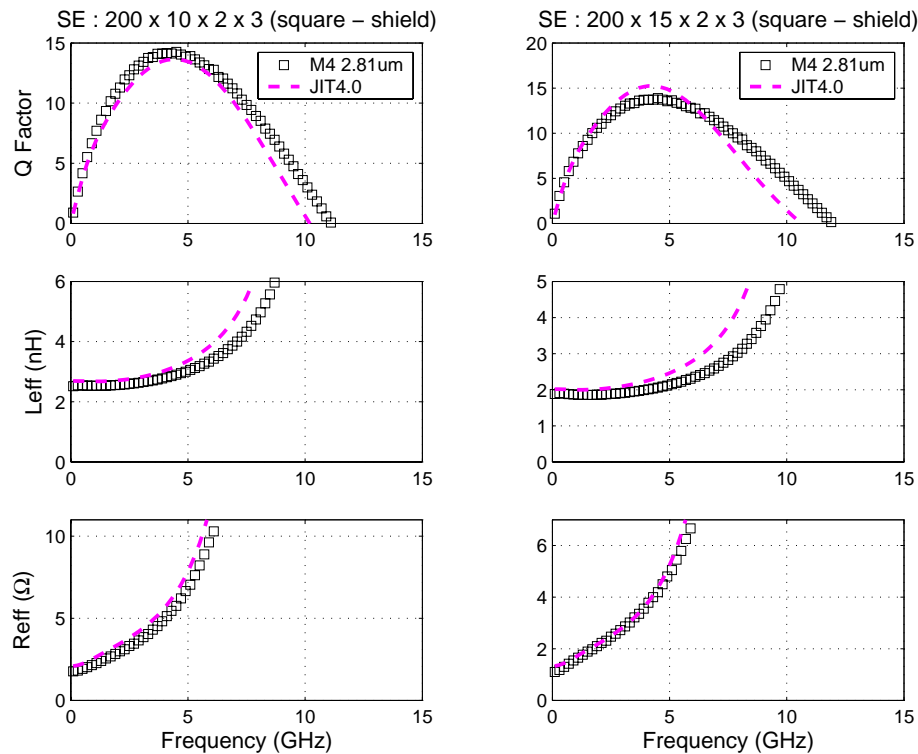


FIGURE 10.29 Inductor Model Verification

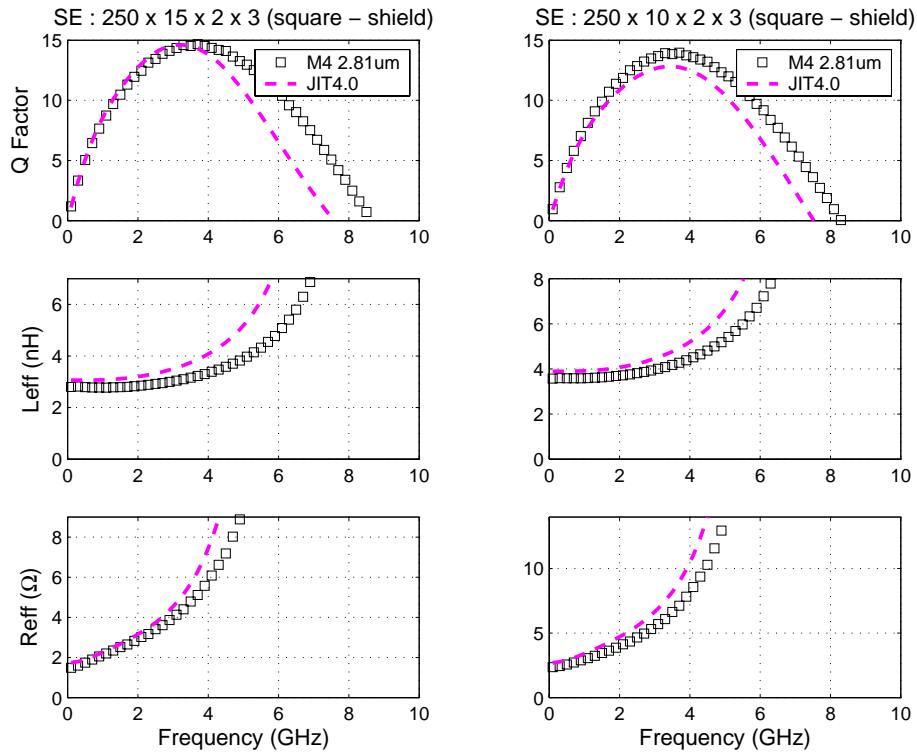


FIGURE 10.30 Inductor Model Verification

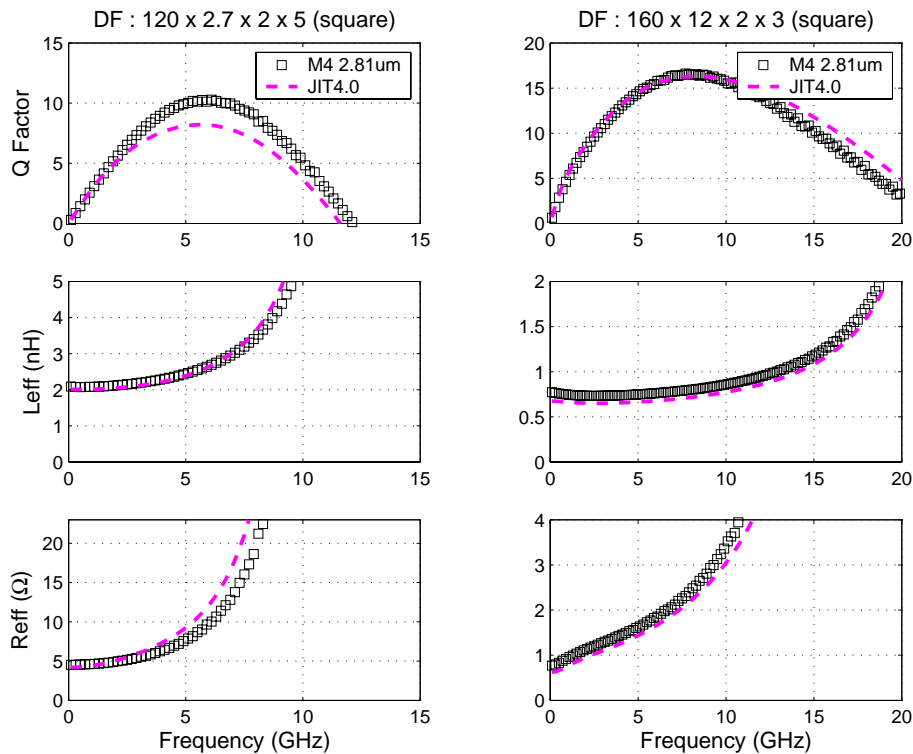


FIGURE 10.31 Inductor Model Verification

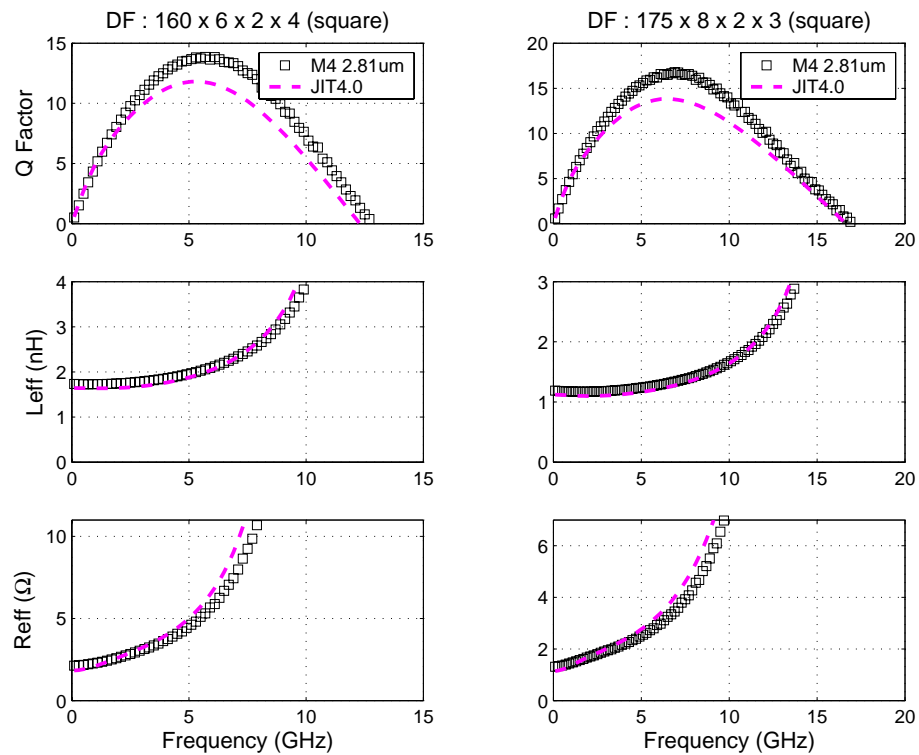


FIGURE 10.32 Inductor Model Verification

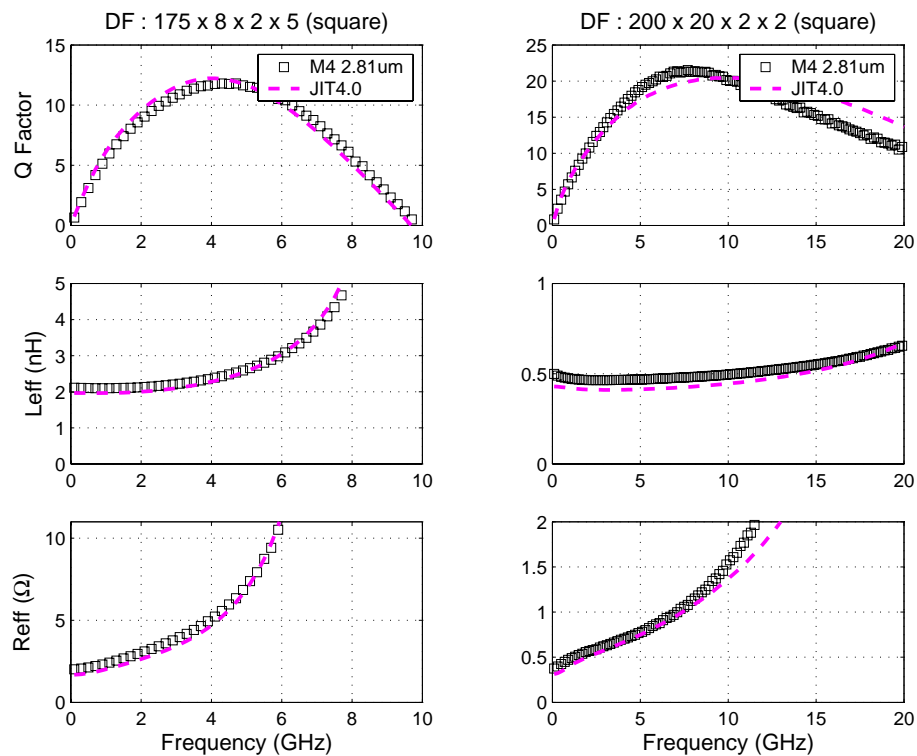


FIGURE 10.33 Inductor Model Verification

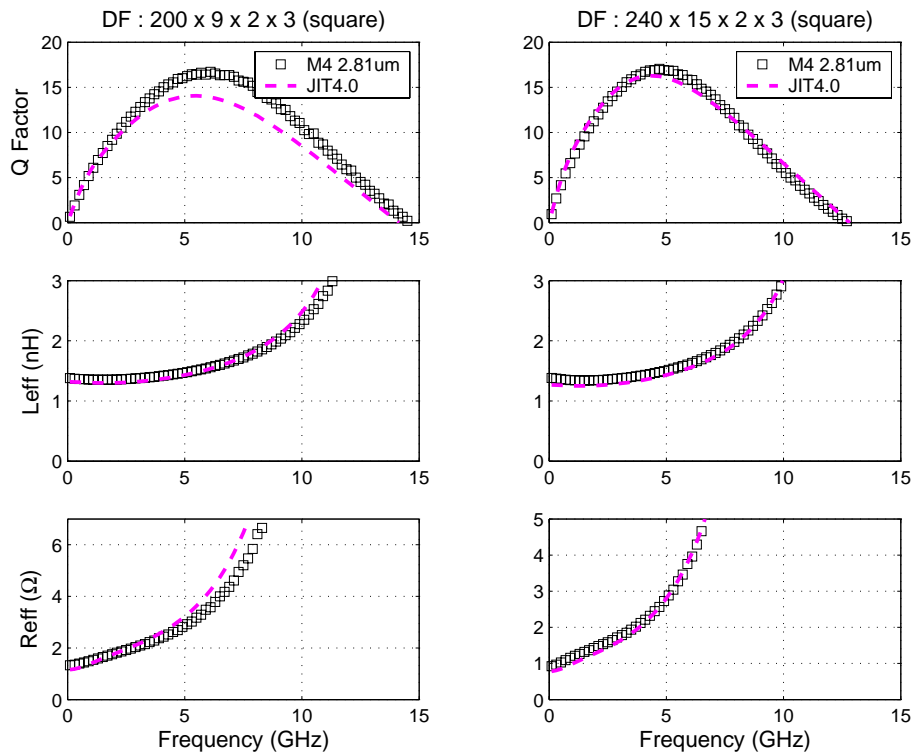


FIGURE 10.34 Inductor Model Verification

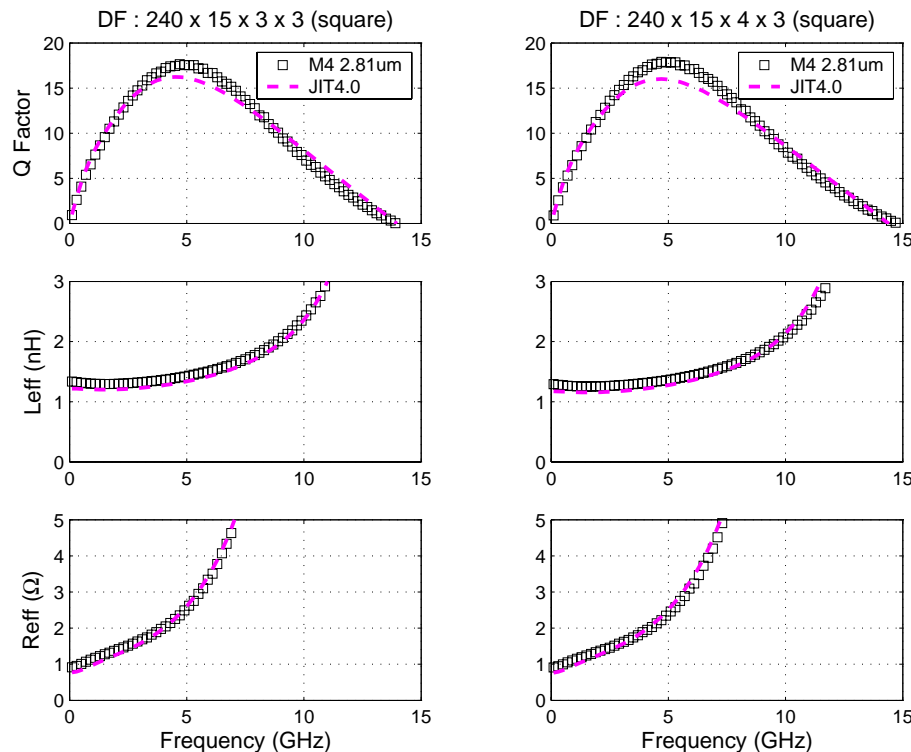


FIGURE 10.35 Inductor Model Verification

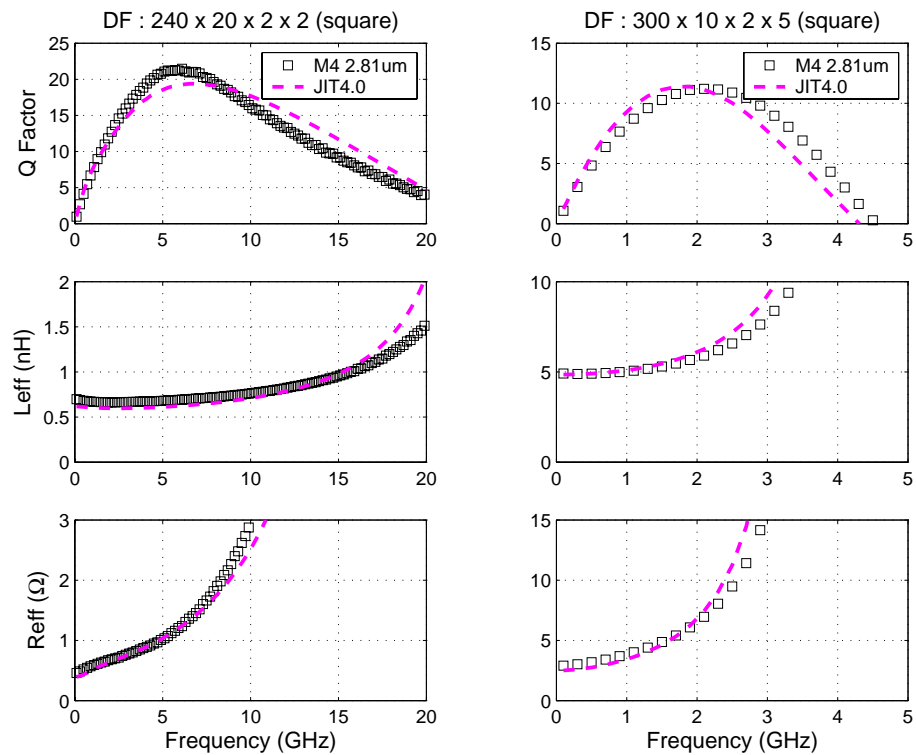


FIGURE 10.36 Inductor Model Verification

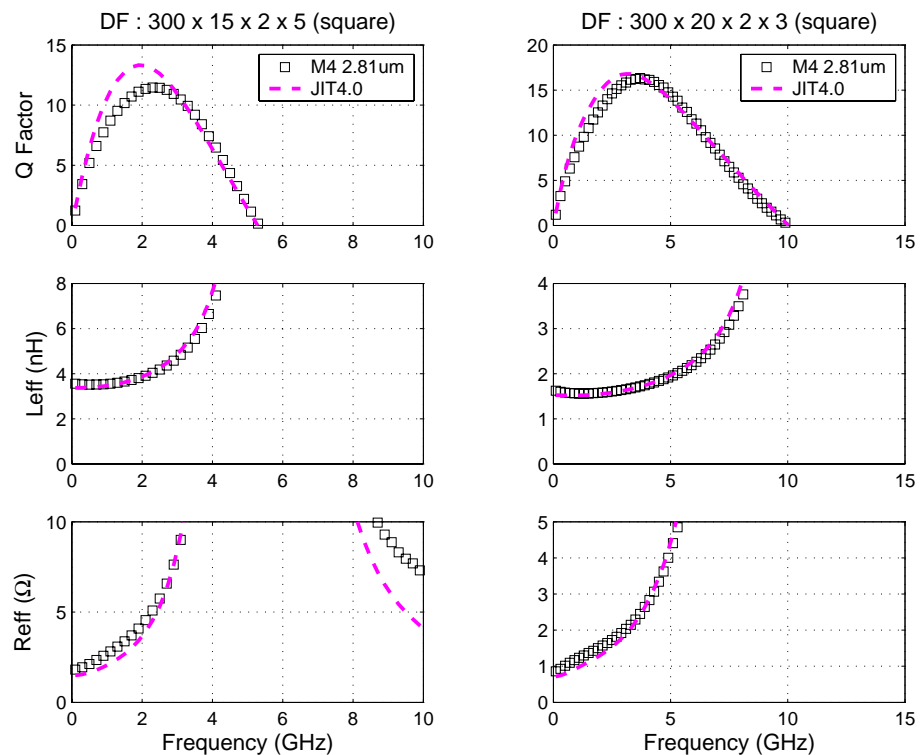


FIGURE 10.37 Inductor Model Verification

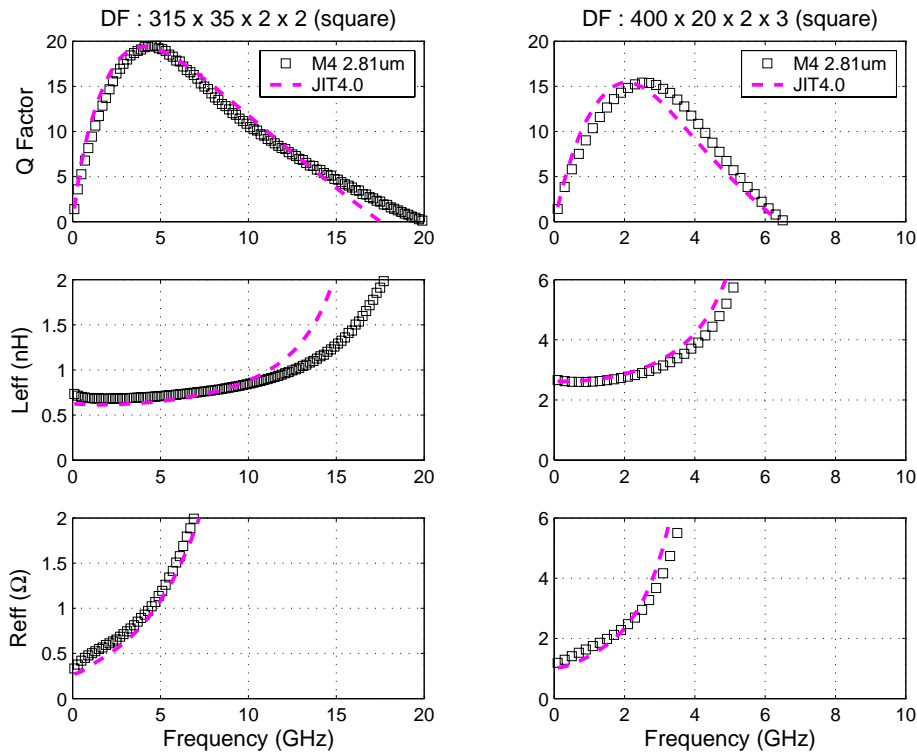


FIGURE 10.38 Inductor Model Verification

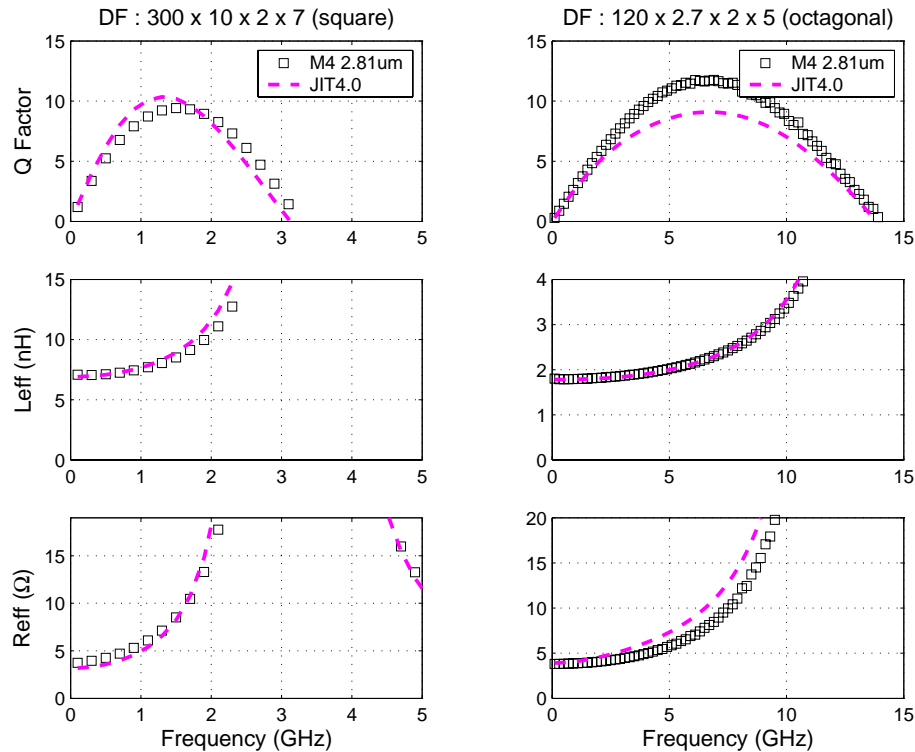


FIGURE 10.39 Inductor Model Verification

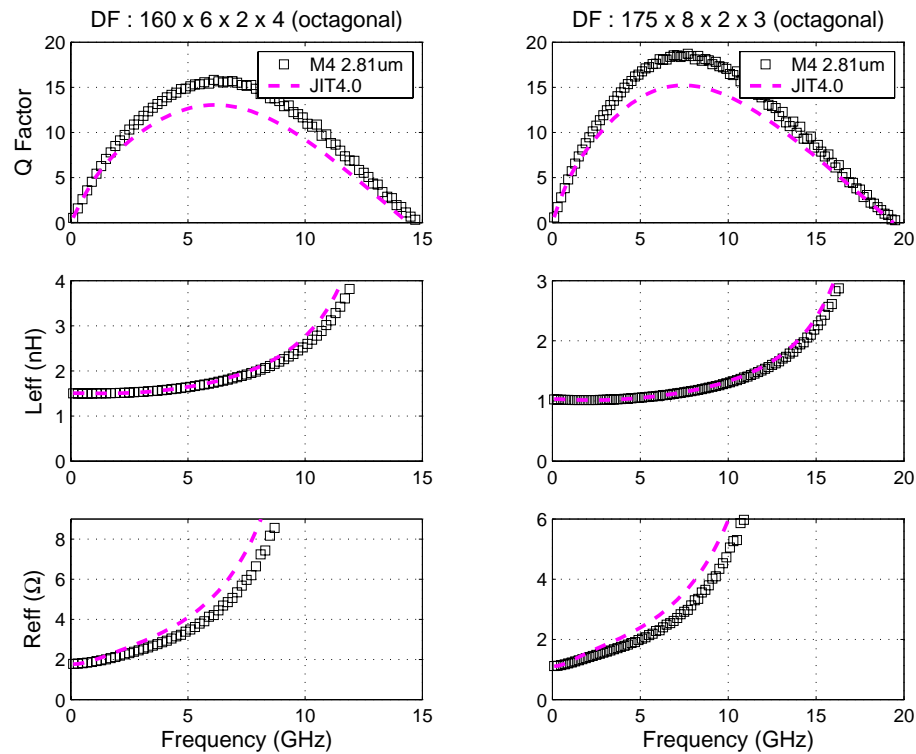


FIGURE 10.40 Inductor Model Verification

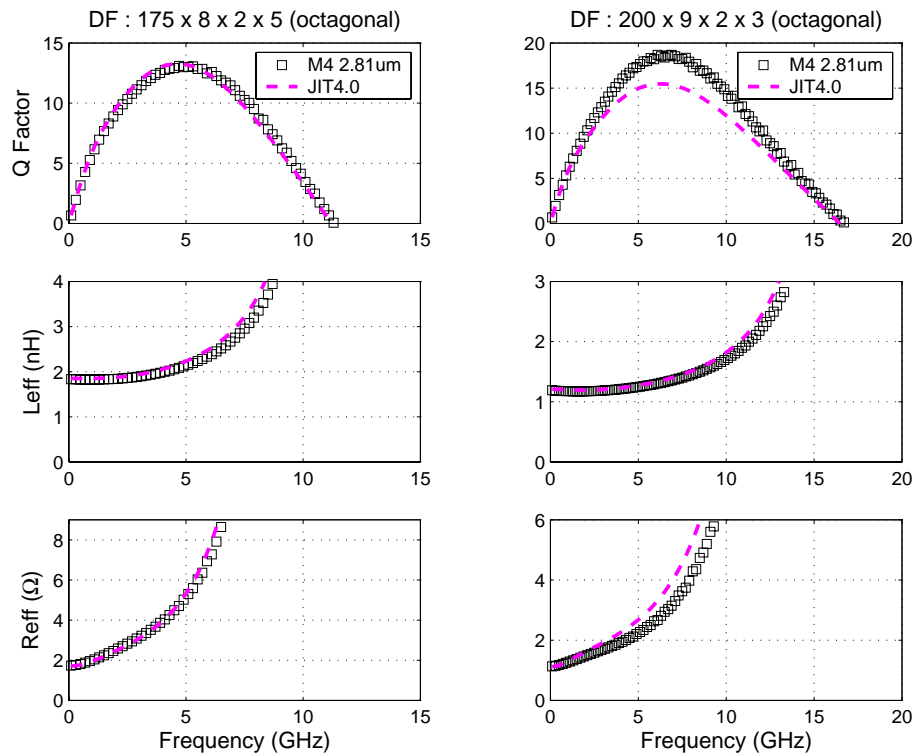


FIGURE 10.41 Inductor Model Verification

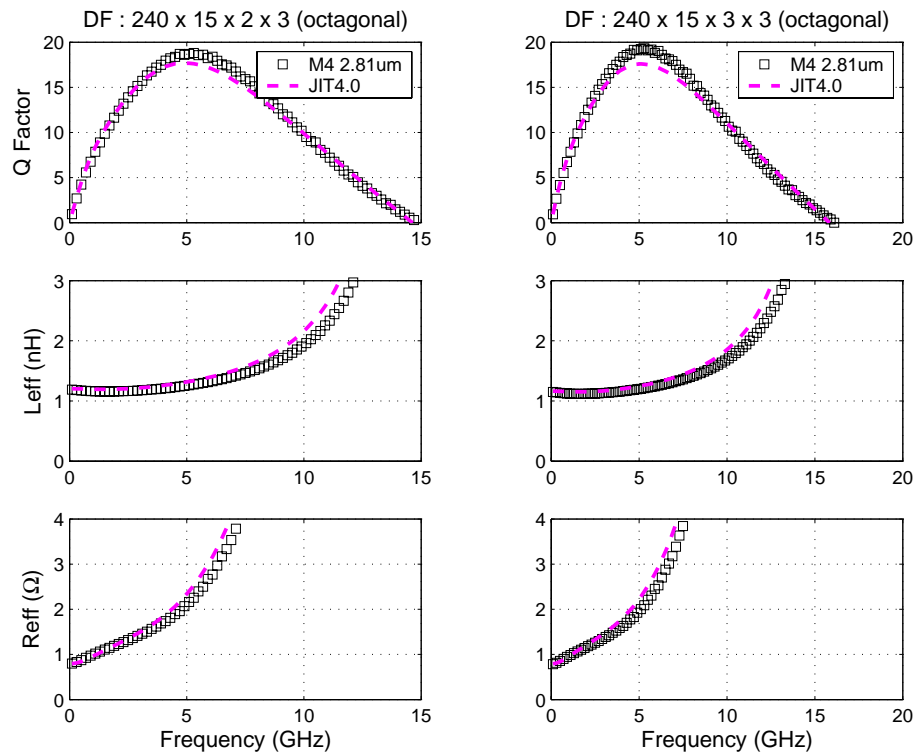


FIGURE 10.42 Inductor Model Verification

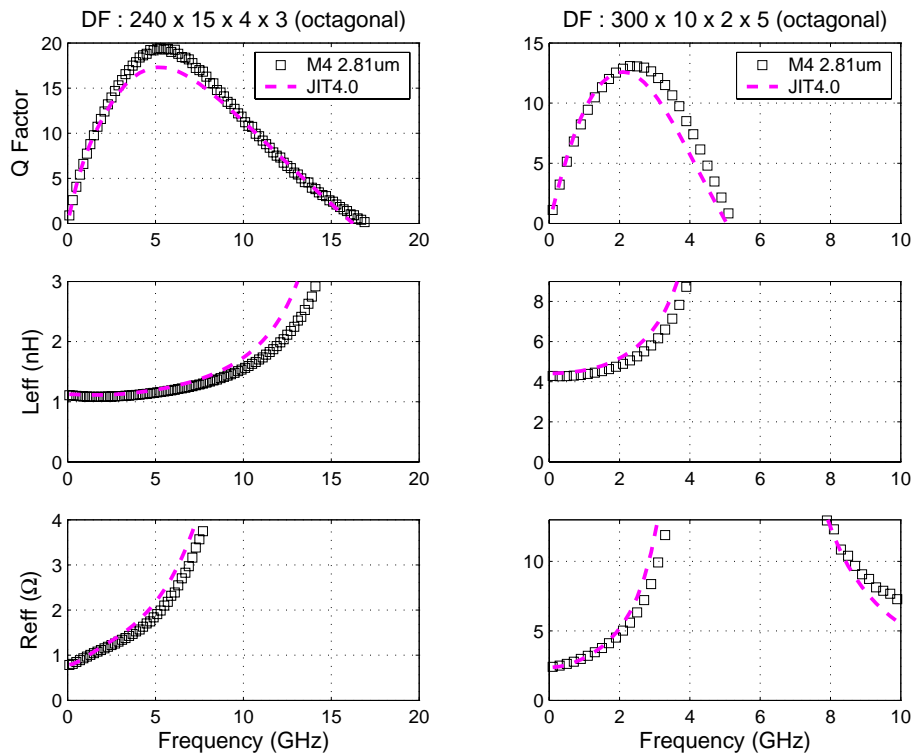


FIGURE 10.43 Inductor Model Verification

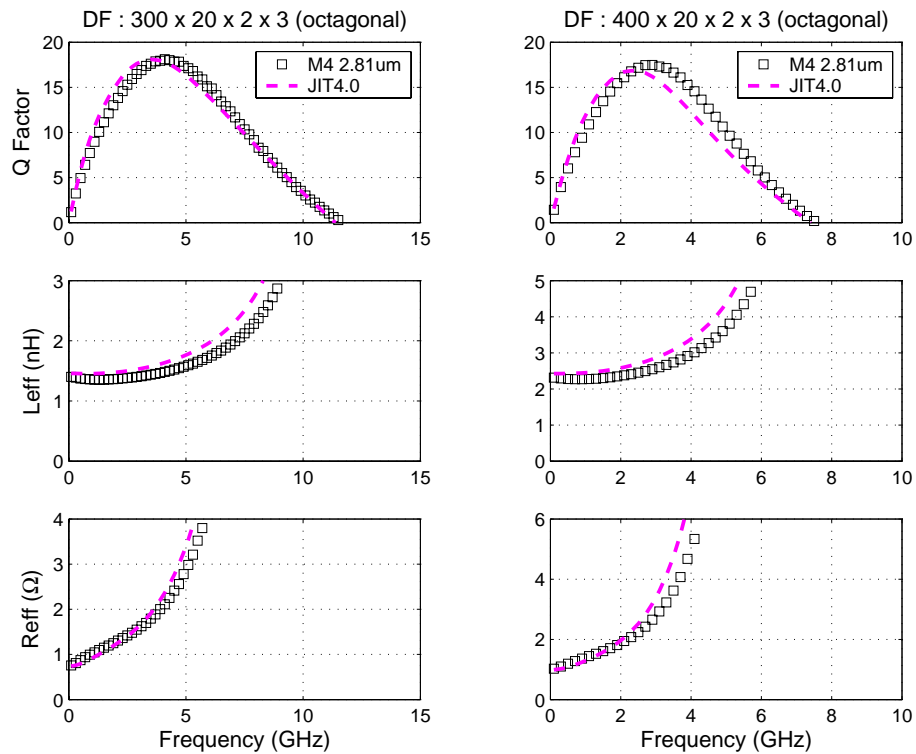


FIGURE 10.44 Inductor Model Verification

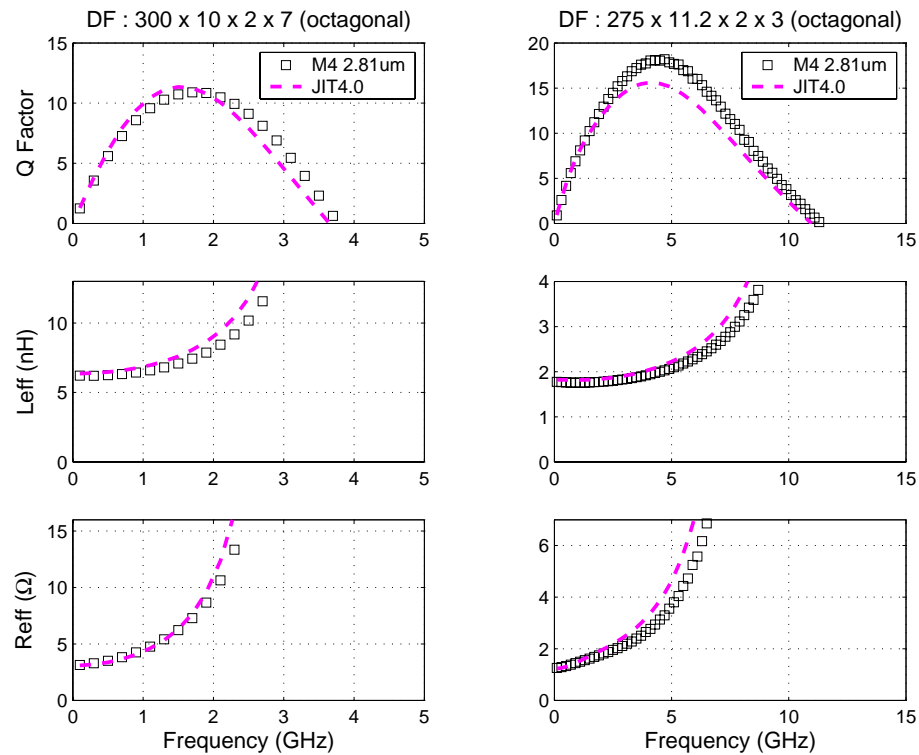


FIGURE 10.45 Inductor Model Verification

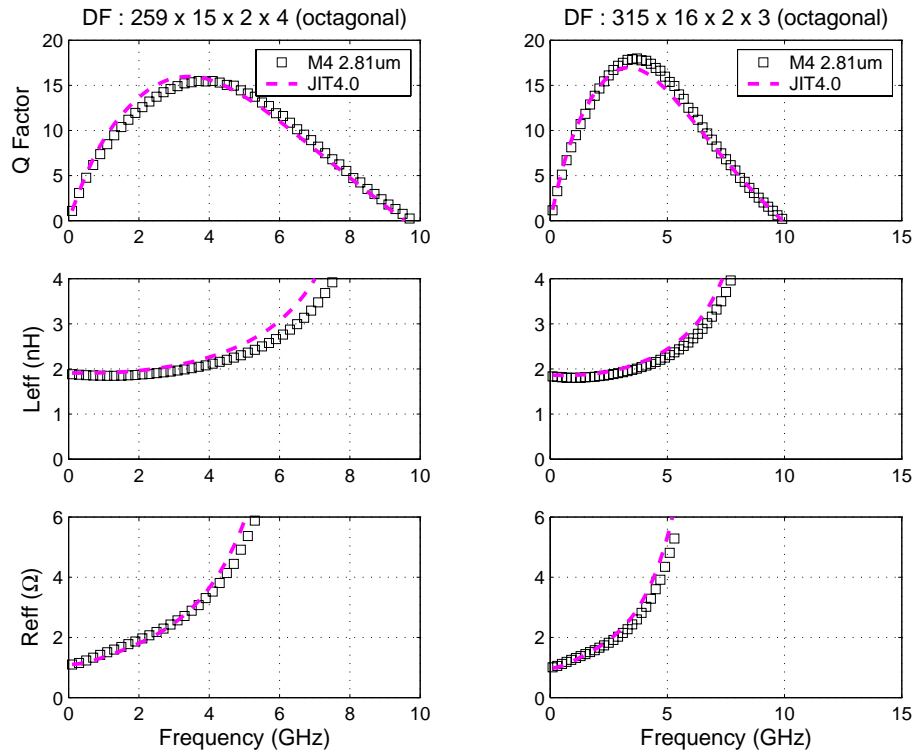


FIGURE 10.46 Inductor Model Verification

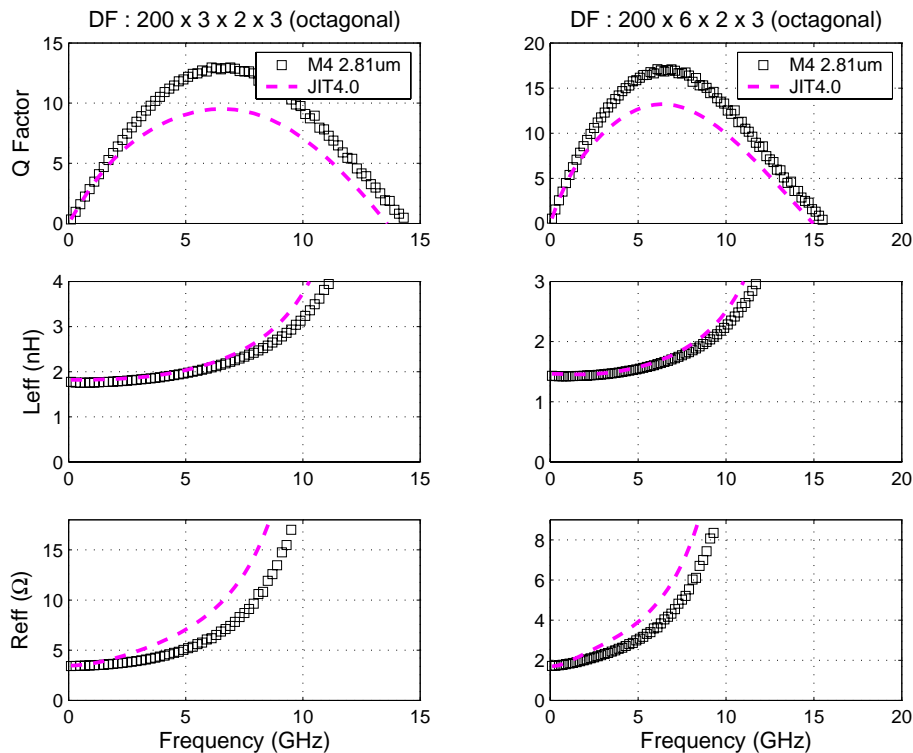


FIGURE 10.47 Inductor Model Verification

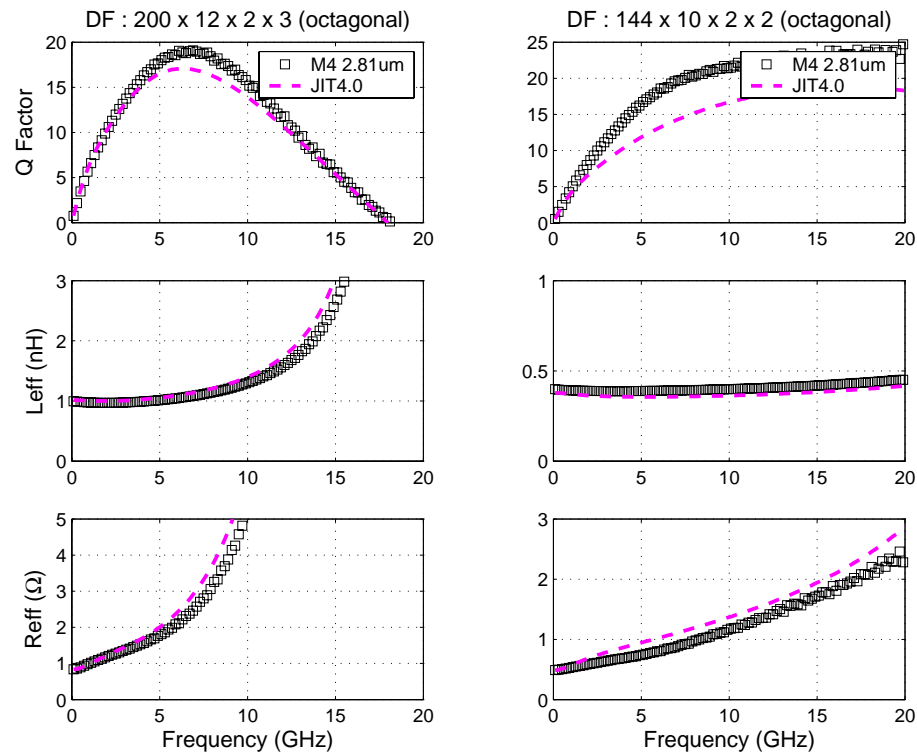


FIGURE 10.48 Inductor Model Verification

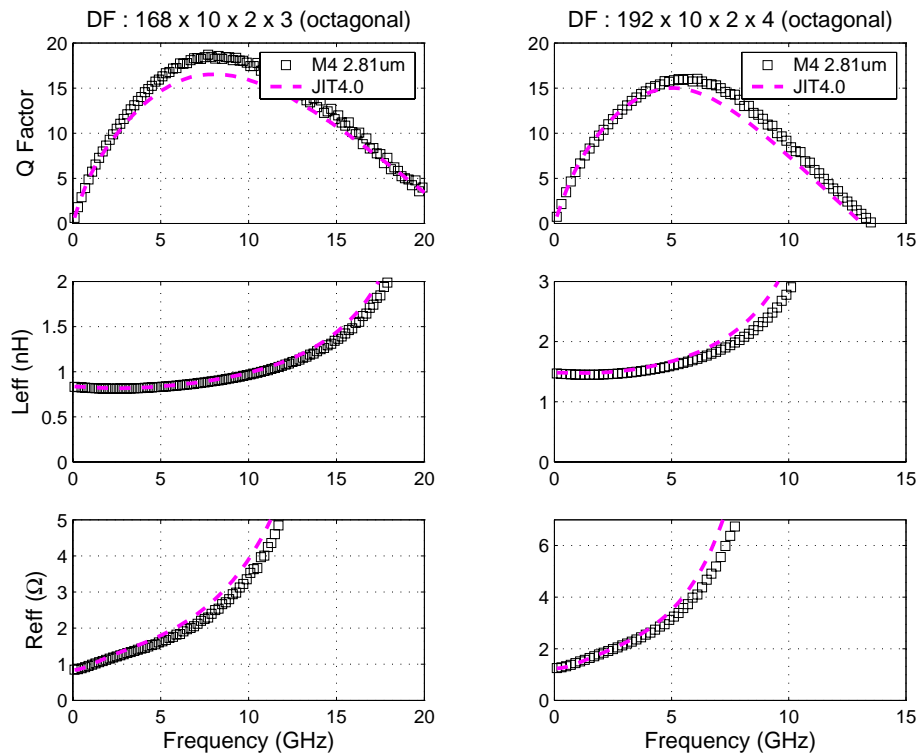


FIGURE 10.49 Inductor Model Verification

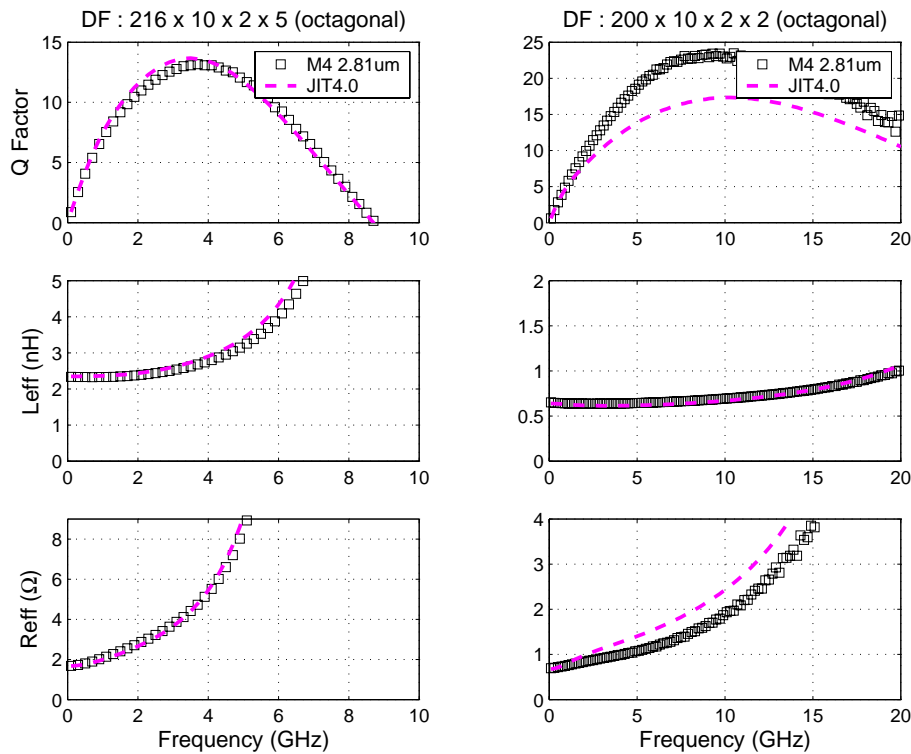


FIGURE 10.50 Inductor Model Verification

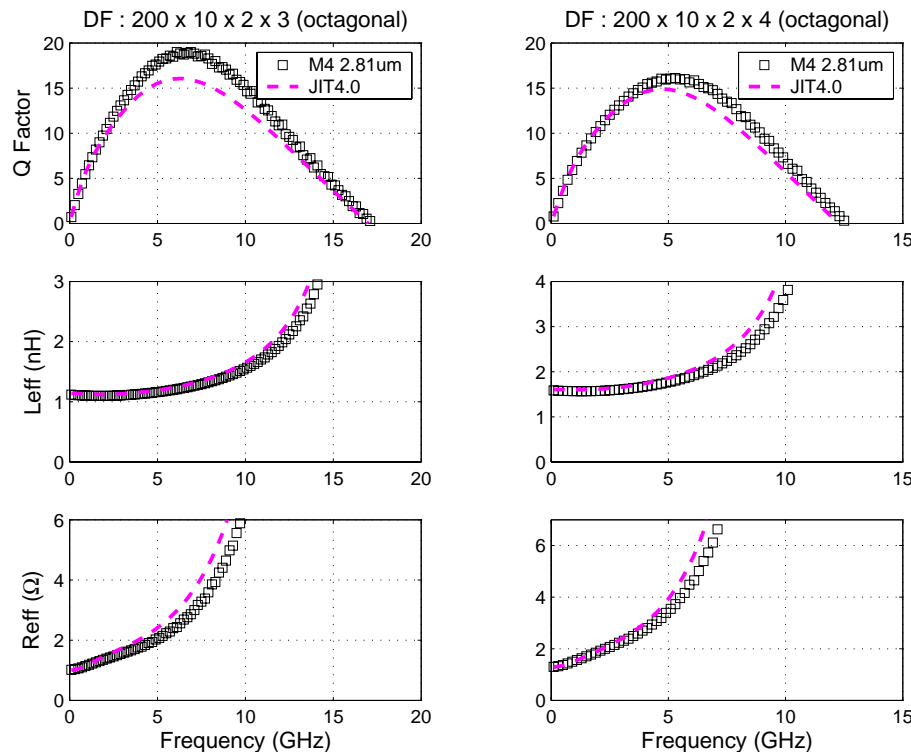
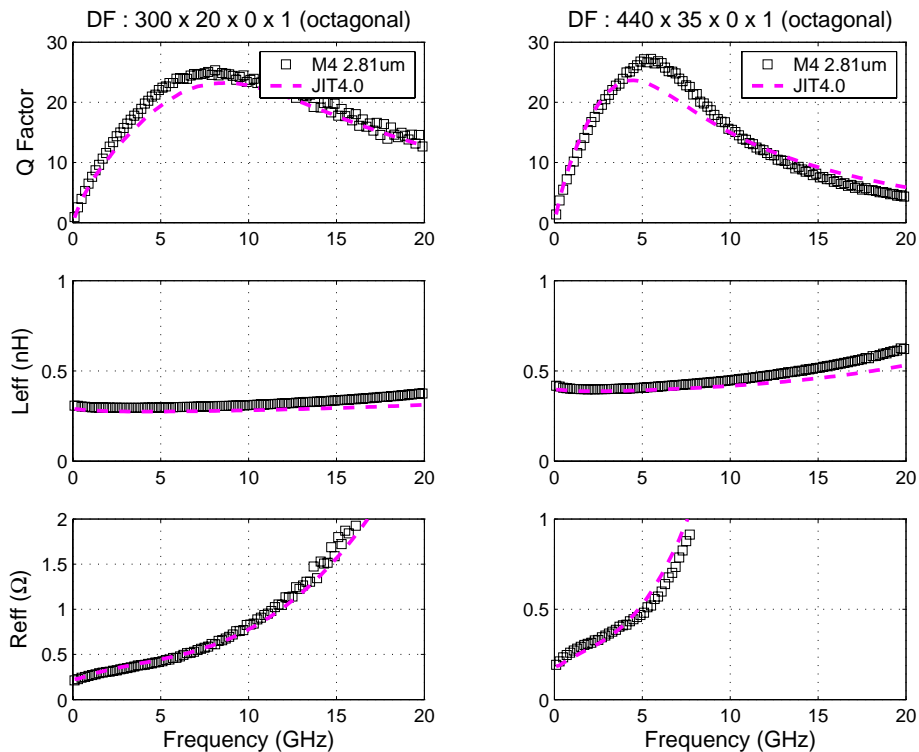


FIGURE 10.51 Inductor Model Verification

10.3.2 Validation with EM Simulation

The single-ended octagonal inductors is the newest addition to the JIT. Since there is no silicon data yet, the QLR models have been compared to ADS Momentum 2.5 EM simulations. The accuracy of the inductance models has already been established using FastHenry (Section 10.2.6.4.2 on page 279). Several examples in 5.26 μm metal 5 from the SBC18PT process are shown in Figure 10.52 through Figure 10.57. The title of each Q,L,R plots contains geometry and special layout information with “UPV” for vertical underpass exit, “UPH” for horizontal underpass exit and “gnd” for ground shield configuration.

FIGURE 10.52 Inductor Model Verification - EM Simulation

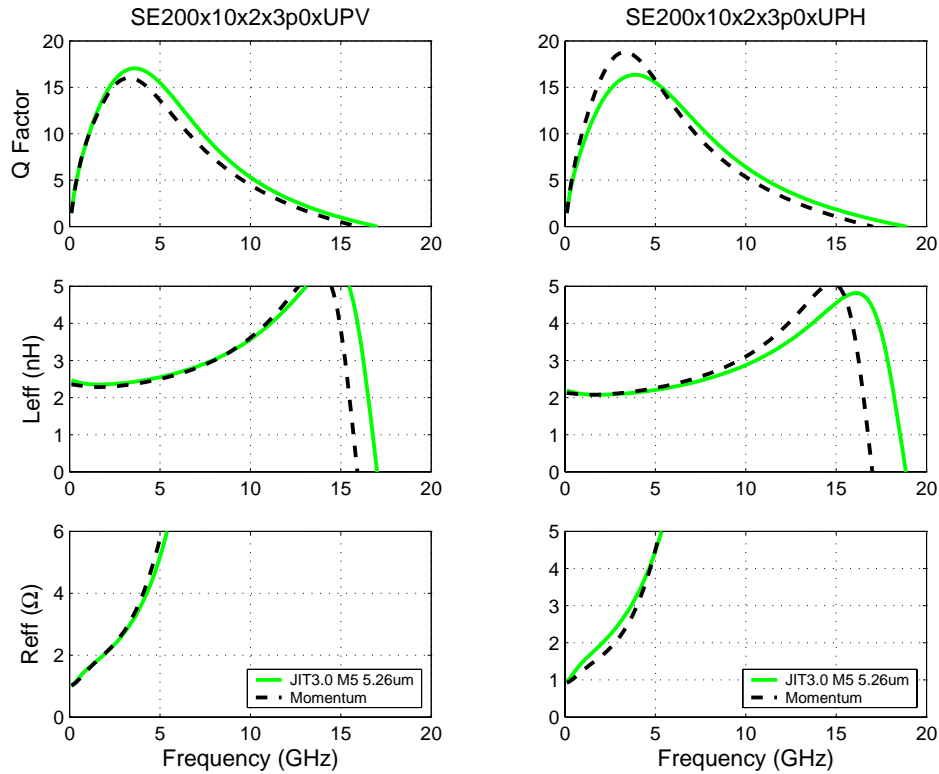


FIGURE 10.53 Inductor Model Verification - EM Simulation

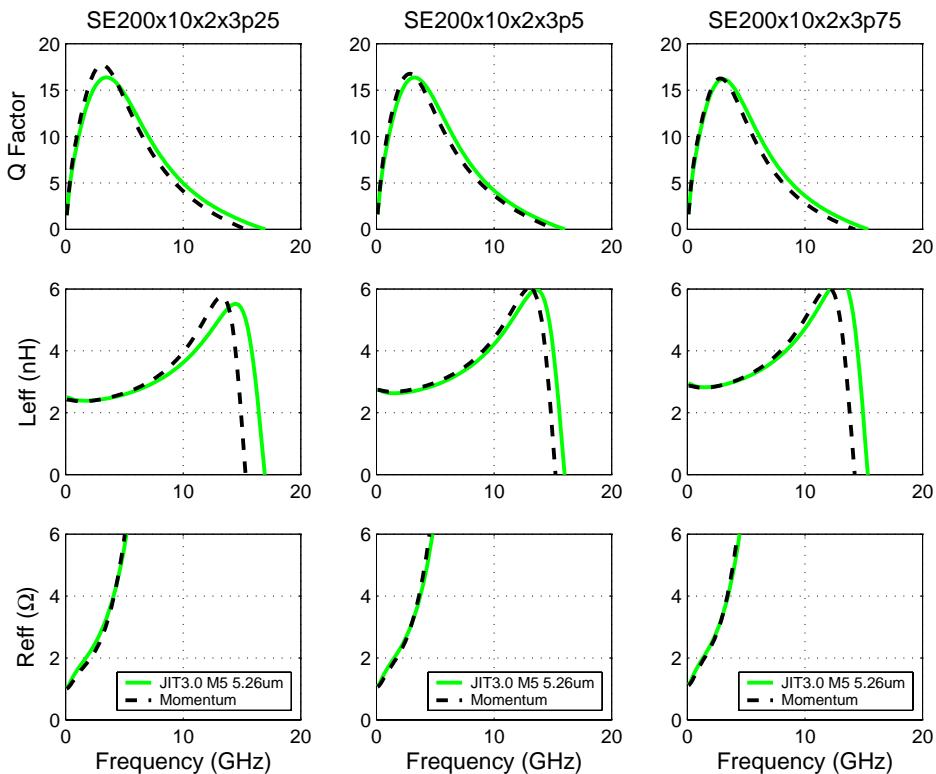


FIGURE 10.54 Inductor Model Verification - EM Simulation

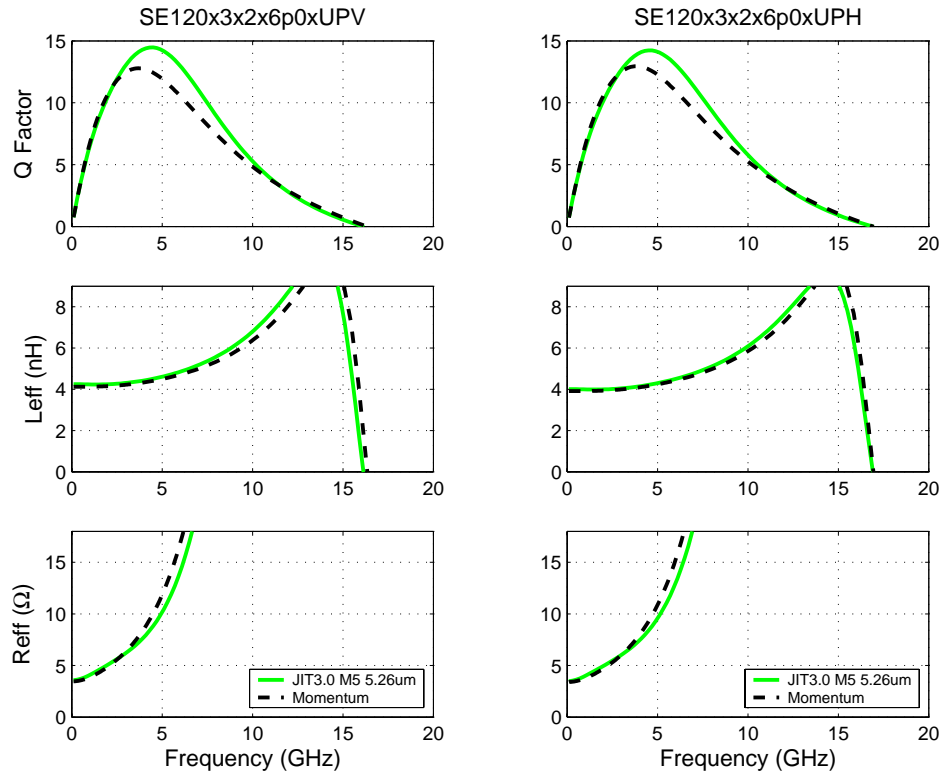


FIGURE 10.55 Inductor Model Verification - EM Simulation

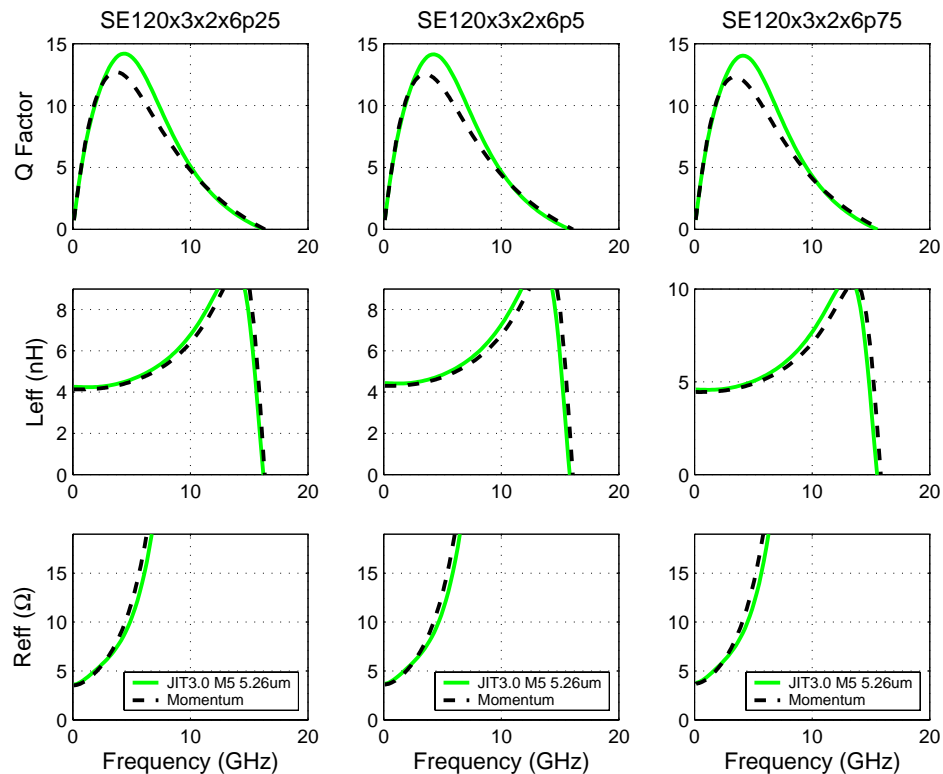


FIGURE 10.56 Inductor Model Verification - EM Simulation

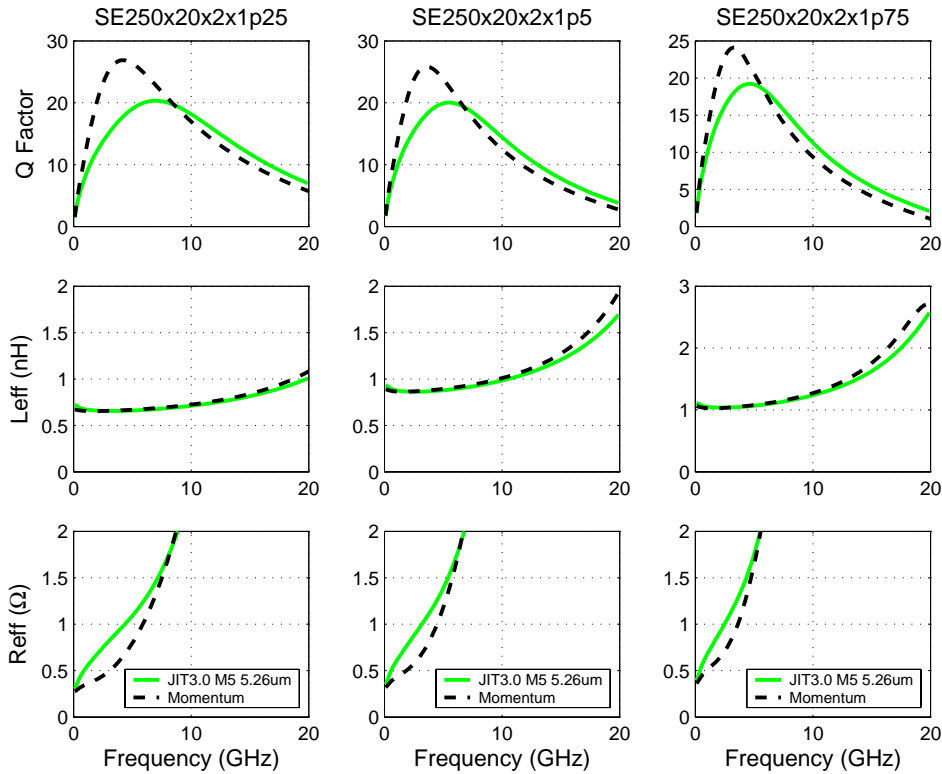
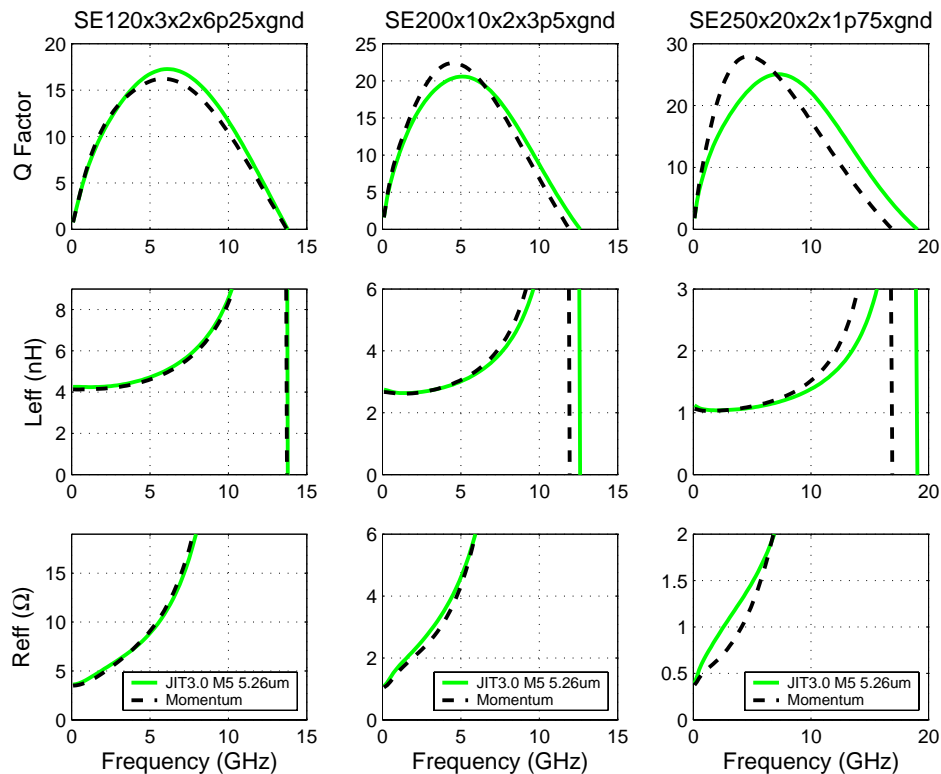


FIGURE 10.57 Inductor Model Verification - EM Simulation



10.4 Inductor Statistical and Corner Models

10.4.1 Corner Models

The corner performance is simulated using the corner model card in the design kit. The equivalent circuit component values are provided by the JIT through the CDF with their nominal value. These nominal values are then multiplied by a factor within the model card to obtain the corner case which was optimized to maximize (fast corner) or minimize (slow corner) the peak Q value of the inductor. The multiplier factors are based on the $\pm 3\sigma$ electrical spec limits of the parameters that affect the value of the individual circuit components. The corner case can be simulated by changing the inductor corner from “NOM” to either “SLOW” or “FAST” under the “Set Active Library” menu in the Spectre “Analog Environment”. The multiplier factors are tabulated in Table 10.3.

The component Cx is not represented by an individual element in the subcircuit diagram but is rather a part of the interwinding capacitance Cp. It is representing the capacitance between spiral trace and cross-overs. In its corners, the cross-over and turn-to-turn capacitances move opposite while they are both part of the feedforward capacitance Cp shown in Figure 10.6 and Figure 10.7. The corner value of component Cp is calculated in the subcircuit model card from these 2 parts resulting in an improved corner model.

TABLE 10.3 Corner Component Multipliers

Component	Multiplier	Fast	Nominal	Slow
L_s^2	lsig	0.980	1.00	1.020
R_s^1 (2.81 um metal)	rsmsig_3u	0.790	1.00	1.210
C_{ox}^2	coxsig	0.930	1.00	1.070
C_p^2 (2.81 um metal)	cpsig_3u	1.200	1.00	0.800
C_x^2	cxsig	0.740	1.00	1.260
R_{sub}^2	rsbsig	0.710	1.00	1.290
C_{sub}^2	csbsig	0.990	1.00	1.010

PCM notes:

1. The Rs multiplier is consistent with the common PCM and ESPEC limits.
2. There is no PCM monitoring.

10.4.2 Statistical Model

The statistical models allow simulation of inductors as affected by the variation of process parameters. These variations are on a global scale affecting the variation of inductors over a larger set of wafers or wafer lots rather than within a given wafer. Generally it is observed that the performance variation between a particular inductor over a wafer is below the resolution of the RF measurements. Therefore, the mismatch of 2 closely located inductor structures is negligible; however mismatch is enabled within the statistical model card and set

to an empirical number of 0.1σ . In comparison to the corner model card, the statistical model is not optimized under the constraint of maximizing or minimizing a particular figure of merit such as Q peak. Consequently, the statistical model is more meaningful in exploring the inductor performance space as dictated by the espec.

Since inductors are fairly large devices and their measurement involves a RF network analyzer, inductors don't lend itself to inline process control. Thus these structures are not monitored like process variables that are defined in the espec. Consequently, there is no data available on an inductor population to enable statistical modeling. Instead, the statistical models are based indirectly on the ESPEC via the corner multipliers of the component values described in the previous section. This method corresponds to the forward propagation of variance. The $\pm 3 \sigma$ variations in the component multipliers propagate through the Spectre model to simulate the device electrical behavior [2].

The statistical model cards were verified for the convergence of the average Qpeak to the nominal Qpeak obtained with the corner model card. Convergence to within 0.1σ is typically achieved with a sample size of less than 100 Monte Carlo simulations.

10.5 Model Update History

Table 10.4 and Table 10.5 lists the model updates with each revision after JIT1.4. Unlisted model revisions indicate that no changes have occurred in that revision. The JIT3.0 uses a "place-holder" inductor from technology ca18hr for sbl13. In JIT4.0 the sbl13 process technology was included and the inductors are now modeled using the proper electrical specs information. Toolbox JIT4.0 represents a major change over JIT1.4 with added new functionality, simplified corner subcircuits and more accurate models.

TABLE 10.4 Model Updates JIT4.0

JIT4.0 Update Detail	Devices	Reason	Impact on User
New inductor technologies	All	New processes	New models for sbl13 inductors.

TABLE 10.5 Model Updates JIT3.0

JIT3.0 Update Detail	Devices	Reason	Impact on User
Active ground shield	Single-Ended Inductor	Improve Q.	Inductors with higher Q.
Modeling of packaging compound	All	Improved accuracy.	Model takes into account the capacitance increase through the packaging material.
New substrate resistance model	All	Improved accuracy, models are calibrated to Jazz silicon.	Better models for roll-off section of Q curve.
Cox and Cp account for distributed effect	All	Improved accuracy.	Better models for roll-off section of Q curve and self-resonant frequency.
Additional interwinding capacitance from port to center-tab	Differential Inductor	Improved accuracy.	More accurate prediction of self-resonant frequency.
Interchange of ports 1 and 2	Single-Ended Inductor	Align models with layout PCELL.	Q performance of port1 and port2 shifts. Port2 identifies the outer (non-underpass) port and has the higher Q due to lower Cox.

TABLE 10.5 Model Updates JIT3.0

JIT3.0 Update Detail	Devices	Reason	Impact on User
Proximity effect warning	Differential Inductor	Prevent usage of devices that are not modeled well.	The warning alerts users of dense inductor designs, whose Q is overpredicted by the model.
New subcircuit model cards and optimized corner multipliers	All	Simplify kit maintenance and improve corner accuracy.	Corner results changed. The inductance corner flipped.
New octagonal inductors	All	Improve Q	Inductors with higher Q

10.6 References

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11.0 Diode Models

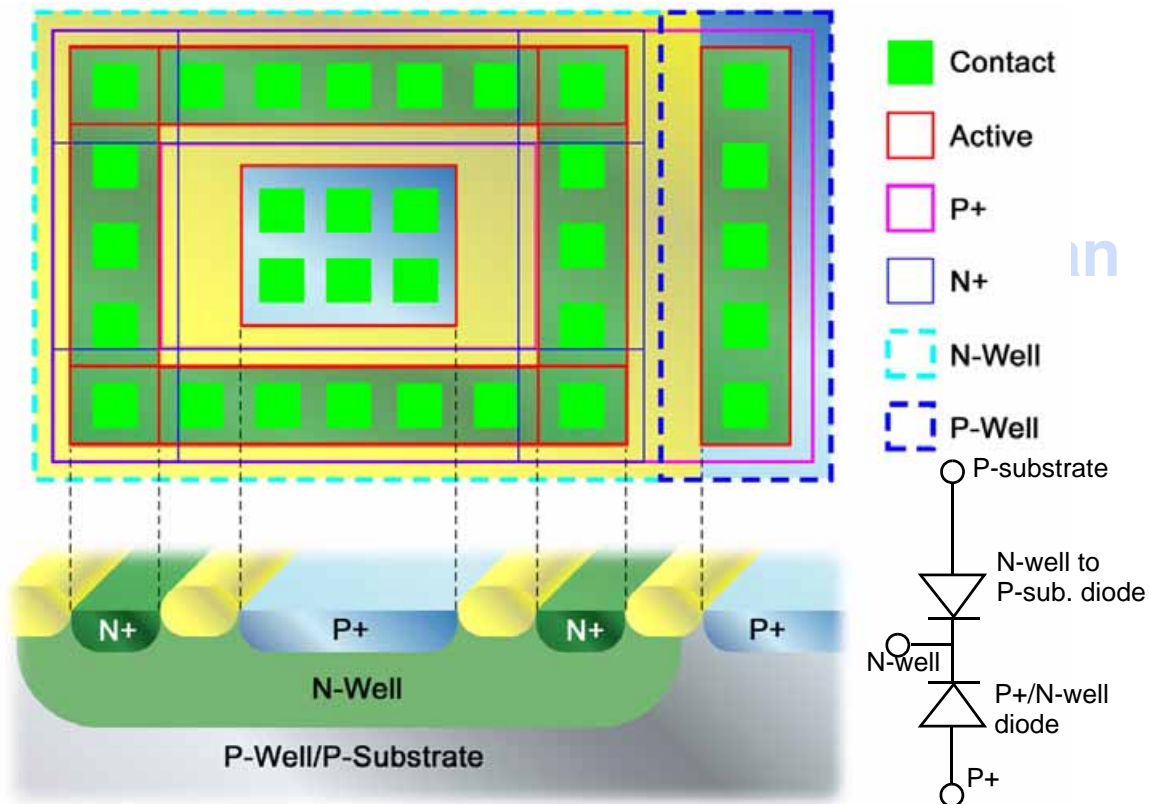
11.1 Device Description

The CA13/SBL13 processes offer four diodes: dn, dn3p3, dp_3 and dp3p3_3 listed in Table 11.1. A typical diode layout, cross-section and schematic for a p+/n-well diode is shown in Figure 11.1.

TABLE 11.1 CA13/SBL13 Diodes

Diode	Description	3rd terminal
dn	1.2V N+/Pwell diode	none
dn3p3	3.3V N+/Pwell diode	none
dp_3	1.2V P+/Nwell diode	P-substrate
dp3p3_3	3.3V P+/Nwell diode	P-substrate

FIGURE 11.1 Layout and cross-section of a typical p+/n-well diode



11.2 Model Description and Verification

The diode models are extracted from two different structures. The first is an area intensive structure with $W \times L = 250\mu\text{m} \times 250\mu\text{m}$. The second is a perimeter intensive structure with 99 fingers of $W \times L = 1.6\mu\text{m} \times 250\mu\text{m}$. The capacitances were measured via a CV meter @ 100 KHz for biases ranging from a small forward bias of 0.2v to a reverse bias of 1.2v (3.5v for the 3.3v diodes). The area and perimeter capacitance densities and their bias

dependencies were extracted simultaneously from measurements of the two test structures described above. The junction capacitance model is valid for reverse biases for a small forward bias of 0.2v to a reverse bias of 1.5v diodes (3.3v for the 3.3v diodes) at -40, 25, and 125°C. The measurements are compared with the model playbacks are plotted in Figures 11.2 through 11.5.

Similarly, the diode current as a function of reverse and forward bias was measured for the two flavors of diodes, allowing simultaneous extraction of saturation current densities for the bulk (area) and sidewall (perimeter) components for the forward bias. The junction leakage current for the reverse bias characteristics is not modeled. The dc current diode model is valid up to a 0.6v forward bias. The measurements along with model playbacks are shown in Figures 11.6 through 11.9.

11.3 Statistical and Corner Models

The area and perimeter components of the capacitance are varied by to give 3- σ values of +/- 10% based on typical expected variation. The numbers have not been verified through process monitoring or electrical data of ring oscillators.

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FIGURE 11.2 Measured junction capacitance and model playbacks for 1.2v n+/pwell diode

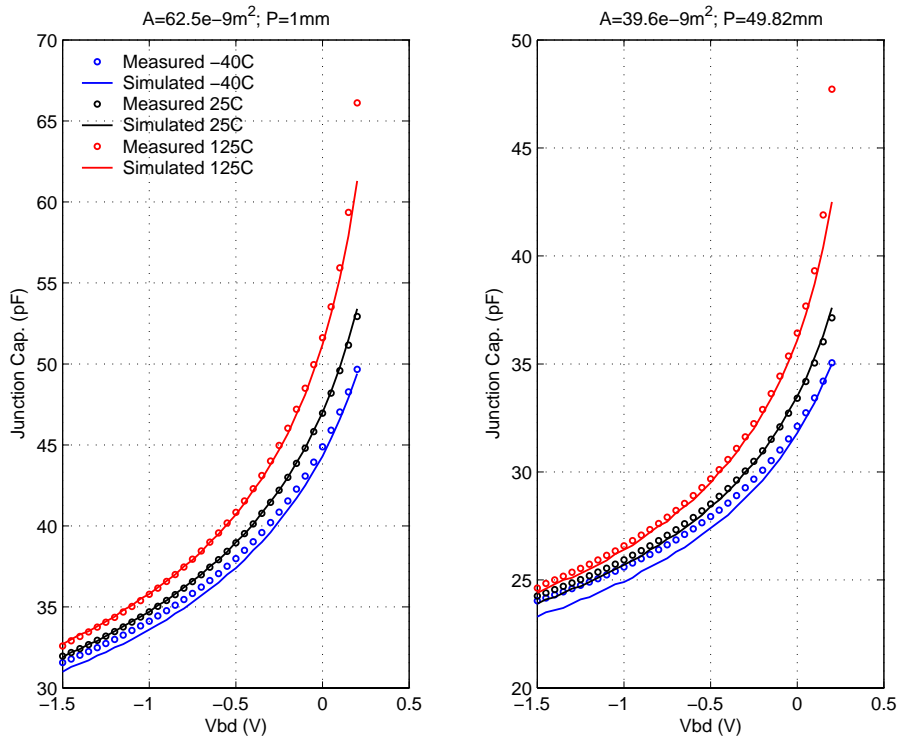


FIGURE 11.3 Measured junction capacitance and model playbacks for 1.2v p+/nwell diode

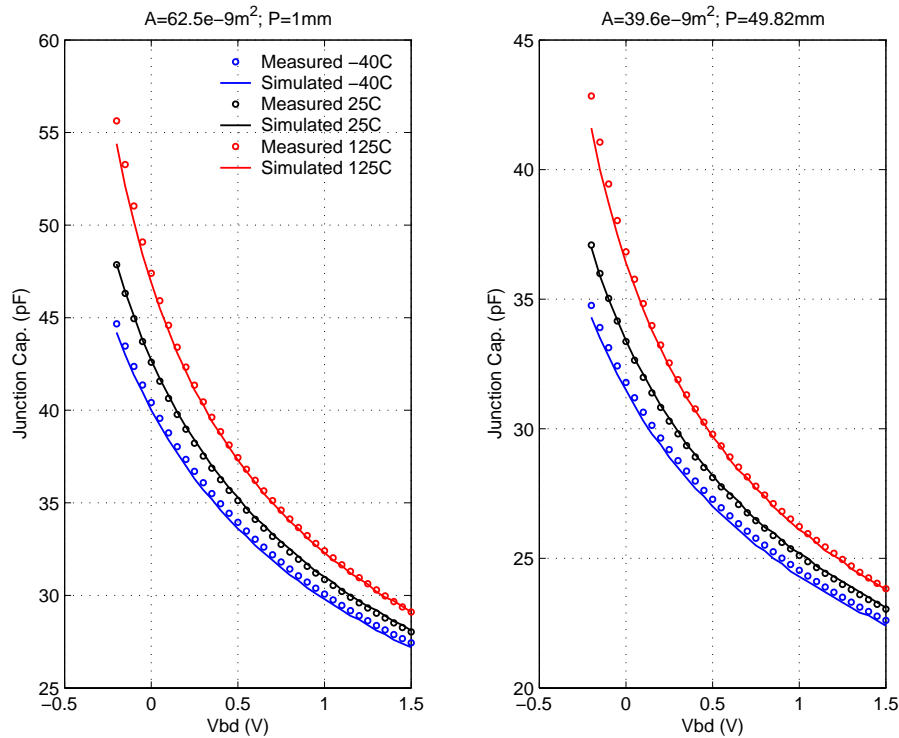


FIGURE 11.4 Measured junction capacitance and model playbacks for 3.3v n+/pwell diode

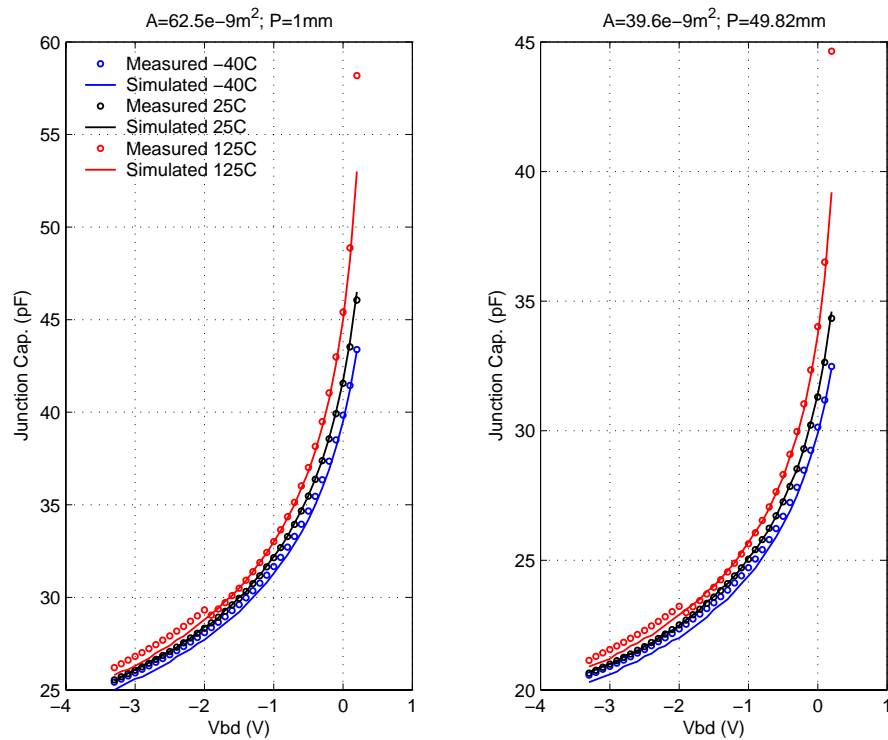


FIGURE 11.5 Measured junction capacitance and model playbacks for 3.3v p+/nwell diode

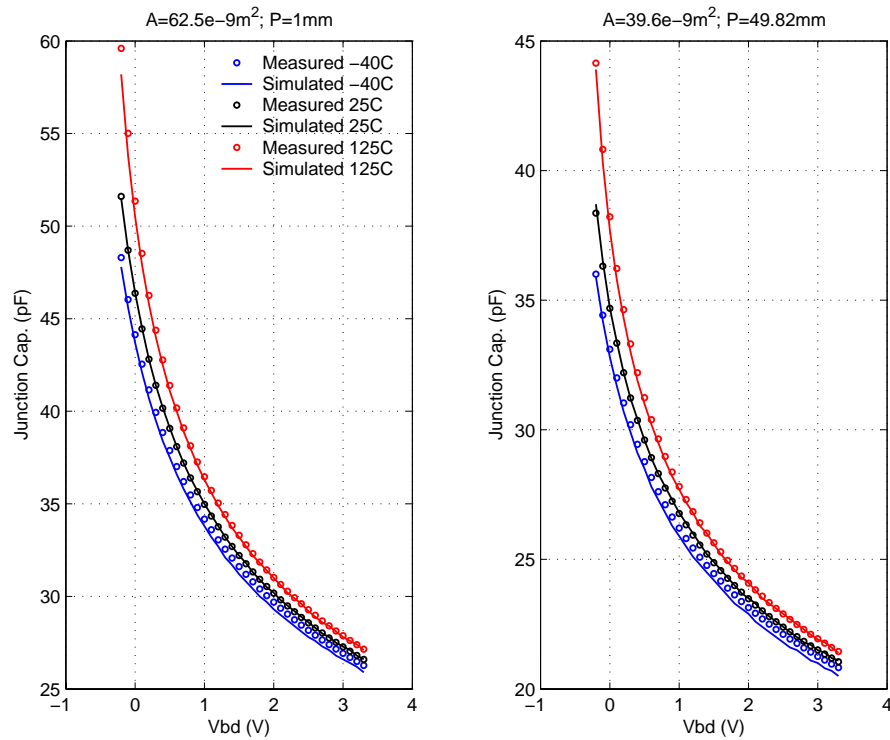


FIGURE 11.6 Measured junction diode current and model playbacks for 1.2v n+/pwell diode

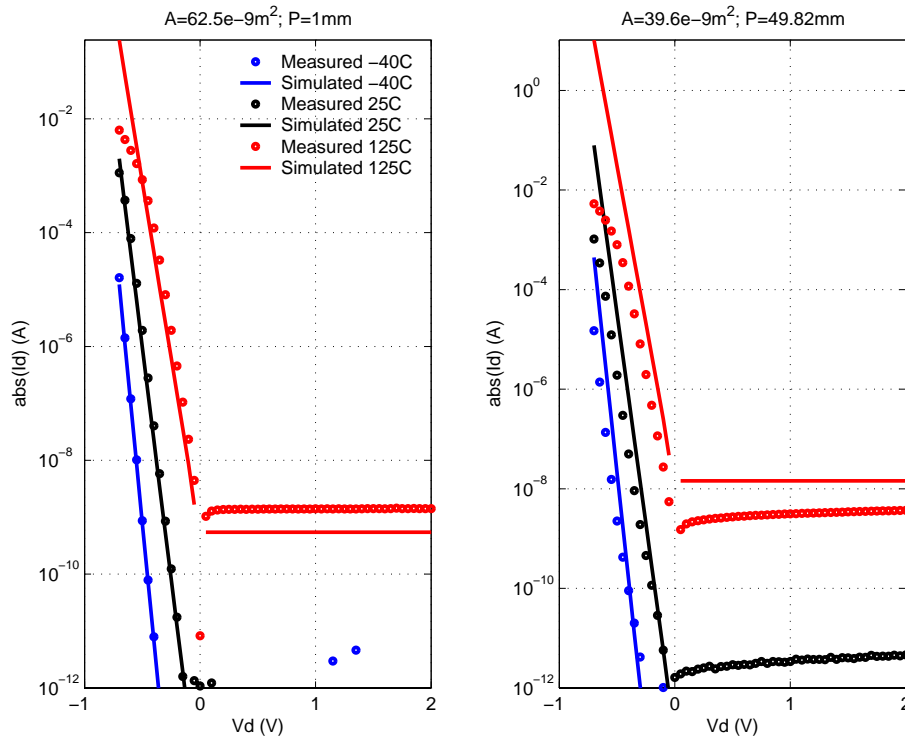


FIGURE 11.7 Measured junction diode current and model playbacks for 1.2v p+/nwell diode

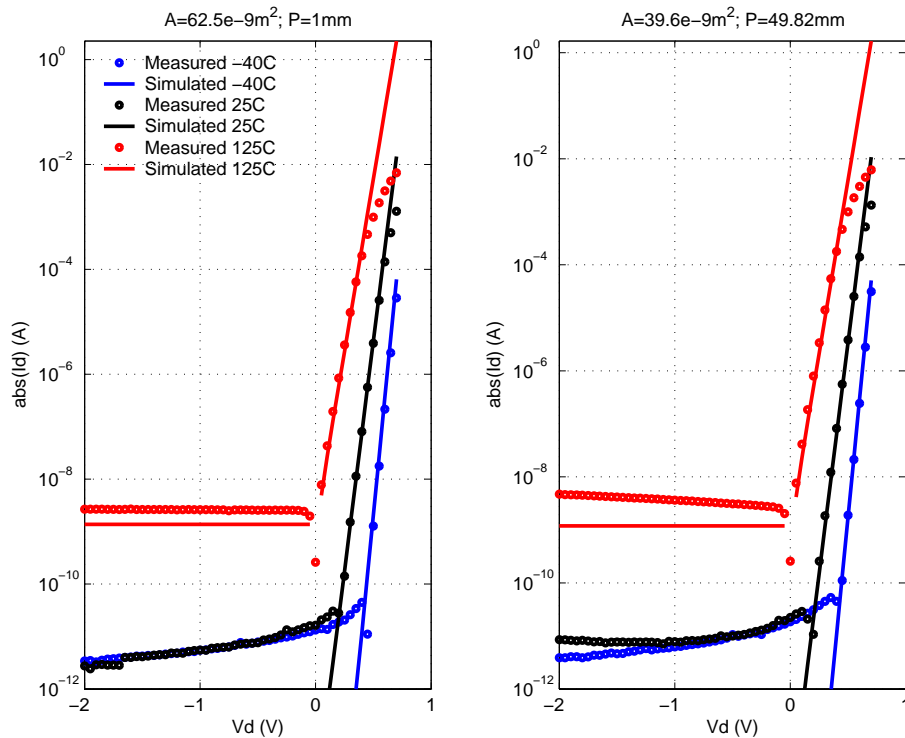


FIGURE 11.8 Measured junction diode current and model playbacks for 3.3v n+/p-well diode

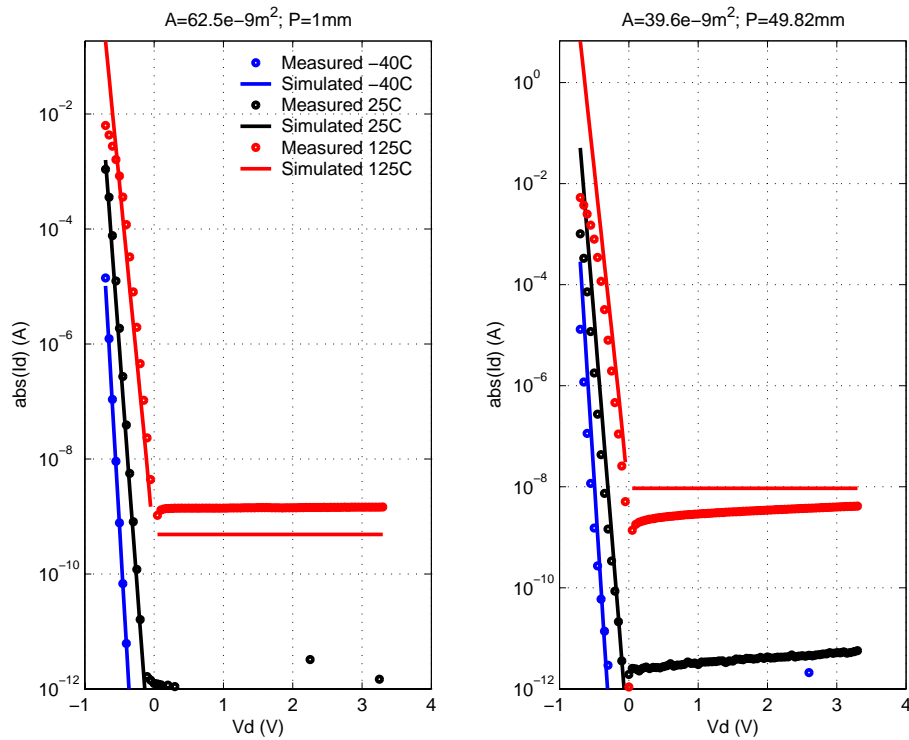
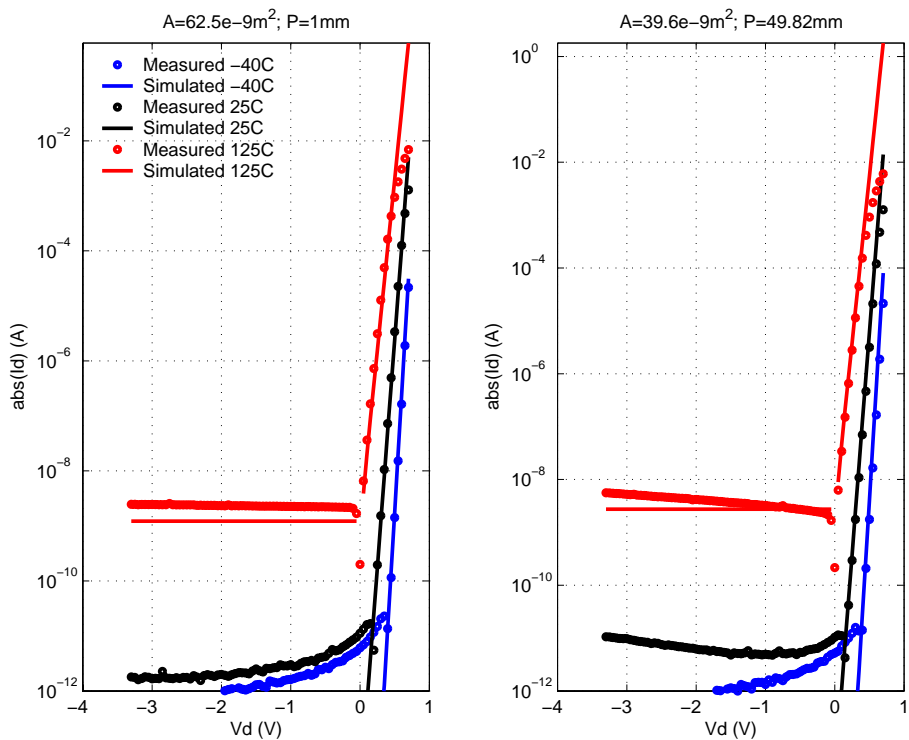


FIGURE 11.9 Measured junction diode current and model playbacks for 3.3v p-/nwell diode



11.4 Model Update History

11.4.1 v1.8

No changes

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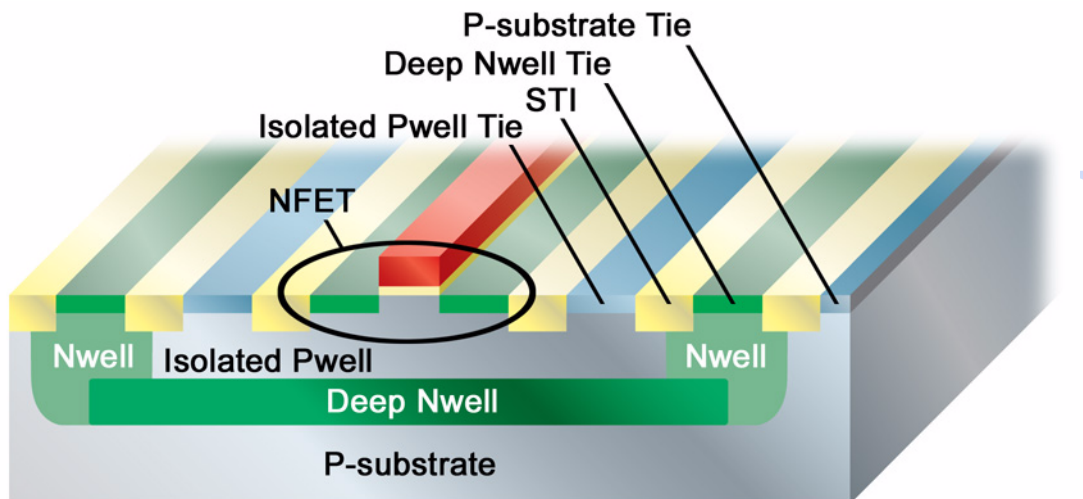
12.0 Deep Nwell

12.1 Introduction

The purpose of this section is to describe the use of the Deep Nwell module to provide additional substrate isolation for nfet_rf library devices. This chapter describes how the Jazz design system accounts for the Deep Nwell process module. This document will cover the modeling, schematic, layout, and verification aspects of this technology. For details on Deep Nwell process availability and specifications please refer to the respective design rules and electrical specification documents.

The current Deep Nwell implementation provides a methodology that allows for robust connectivity and verification and provides a basic model. Among some of the benefits, this methodology allows the designer to bias the isolated Pwell separately from the outer P-substrate. It will also prevent the improper biasing (such as forward bias) of the junctions formed by the Deep Nwell by reporting design rule and LVS violations. Please refer to Figure 12.1 and Figure 12.3 for Deep Nwell silicon cross section, top views, and legend.

FIGURE 12.1 Deep Nwell Silicon Cross Section including isolated NFET.



12.2 Modeling

The addition of Deep Nwell will form two PN junction diodes across the physical circuit area. The Jazz design environment models these junctions as separate diodes **diso** and **ddnw** as seen in Figure 12.2. The first diode **diso** is formed by the Deep Nwell/Nwell to Isolated Pwell junction. The second diode, **ddnw**, is formed by the the P-substrate to Deep Nwell/Nwell junction. Table 12.1 lists the ESPEC and NOM model simulation of the area and perimeter capacitances. Corner and statistical models are not supported. Investigation of the DC and RF effects of the Deep Nwell is given in Section 12.6.

TABLE 12.1 Deep Nwell Diode ESPEC vs. NOM Model

Capacitance	units	Espec	NOM
Pwell to DNW CA ¹	$\mu\text{F}/\text{m}^2$	546.6	546.7
Pwell to DNW CP ¹	nF/m	1.346	1.346
DNW to P-Sub CA ¹	$\mu\text{F}/\text{m}^2$	126.7	126.8
DNW to P-Sub CP ¹	nF/m	3.124	3.122

PCM notes:

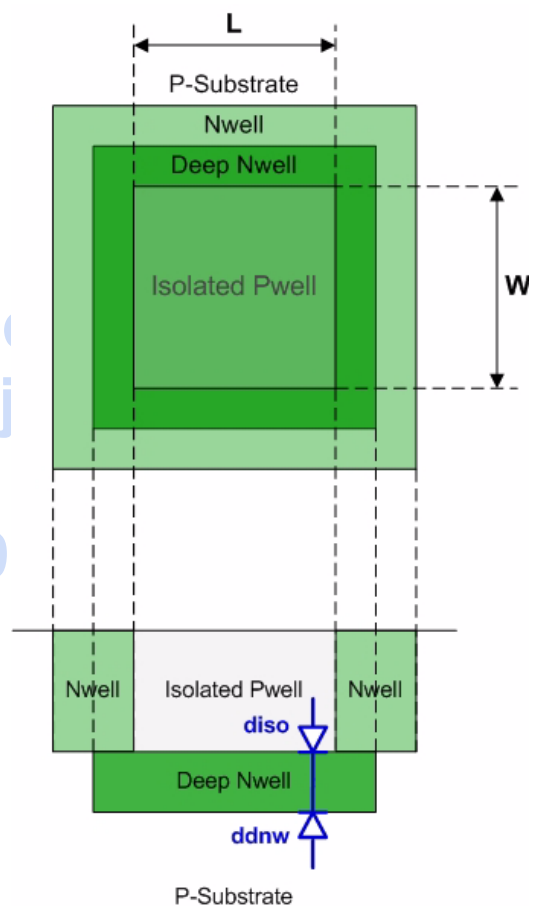
1. PCM and ESPEC share the same limits.

12.3 Schematic Entry

The two diodes, **ddnw** and **diso**, are shown in Figure 12.2.

FIGURE 12.2 ddnw Device Schematic**12.3.1 Device Attributes**

The geometry of each of the diodes can be entered by A/P (area and perimeter), L/W (length and width), or A/R (area and aspect ratio). For the **diso**, the geometry is a measure of the isolated Pwell. For the **ddnw**, the geometry is a measure of the drawn deep Nwell layer. Typically these devices can be used during schematic entry and simulation to give an estimate of the Deep Nwell construction.

FIGURE 12.3 Deep Nwell Top view and Cross section

Once layout is completed, the schematic should be updated to reflect the final geometries. Section 10.5.2 will describe how these parameters are included in LVS.

FIGURE 12.4 *ddnw* device attributes

CDF Parameter	Value
Model name	dnw_psub
Specify	<input checked="" type="radio"/> A/P <input type="radio"/> WL <input type="radio"/> A/R
Width	5u M
Length	5u M
Area	25.0p M
Perimeter	20u M
Aspect - Ratio	1
Count	1

12.3.2 Connectivity

The *diso* and *ddnw* devices allow the designer to connect and bias the Isolated Pwell and P-substrate independently. By default, the Jazz three terminal FETs come embedded with an inherited substrate connection “sub_inh” set to “sub”. The value of the sub_inh property may be changed through the object properties page as shown in Figure 12.5. Four terminal FETs allow for more explicit definition of the substrate connection. Finally, for all other devices allowed in deep nwell such as diodes, poly resistors, and capacitors, the user may edit the **Substrate Node** property directly through the CDF.

FIGURE 12.5 How to define a FET substrate name

Edit Object Properties

OK Cancel Apply Defaults Previous Next Help

Apply To:

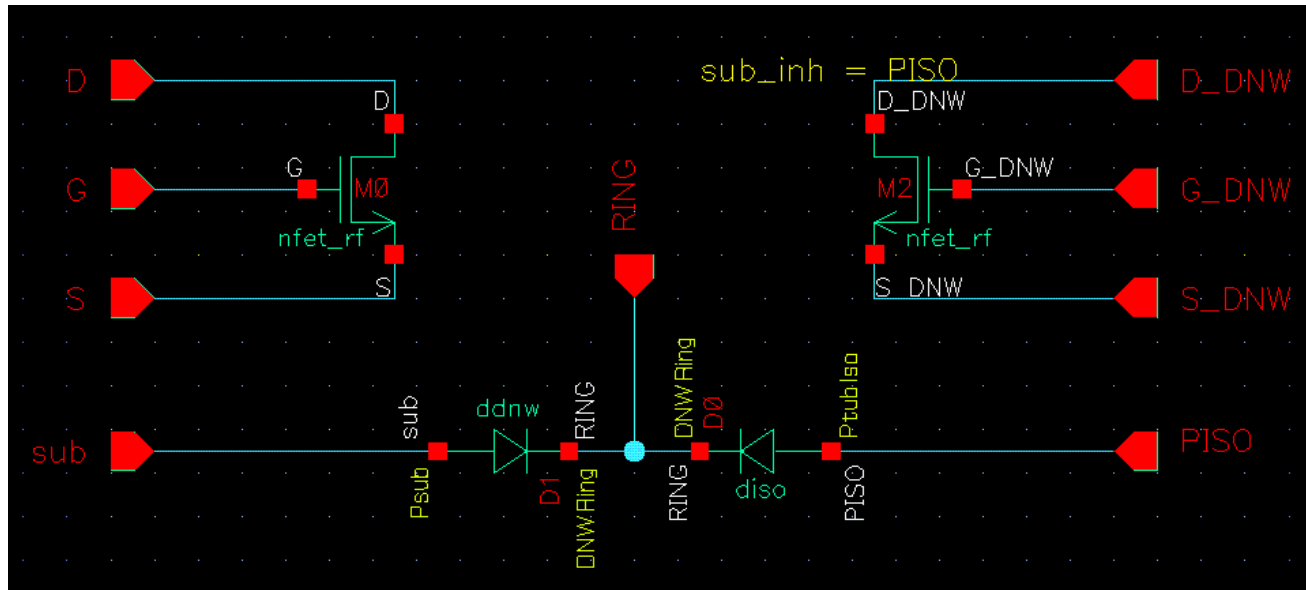
Show: ☐ system ☒ user ☒ CDF

Property	Value	Display
Library Name	sbcl8ptf	off
Cell Name	nfet_rf	value
View Name	symbol	off
Instance Name	M2	off

User Property	Master Value	Local Value	Display
sub_inh		PISQ	off

Figure 12.6 illustrates the schematic view of two NFET transistors. The right hand side NFET (M2) will be placed over Deep Nwell, while the left hand side device (M0) will be placed over P-substrate. The schematic also shows how the *ddnw* device can be properly connected to each transistor.

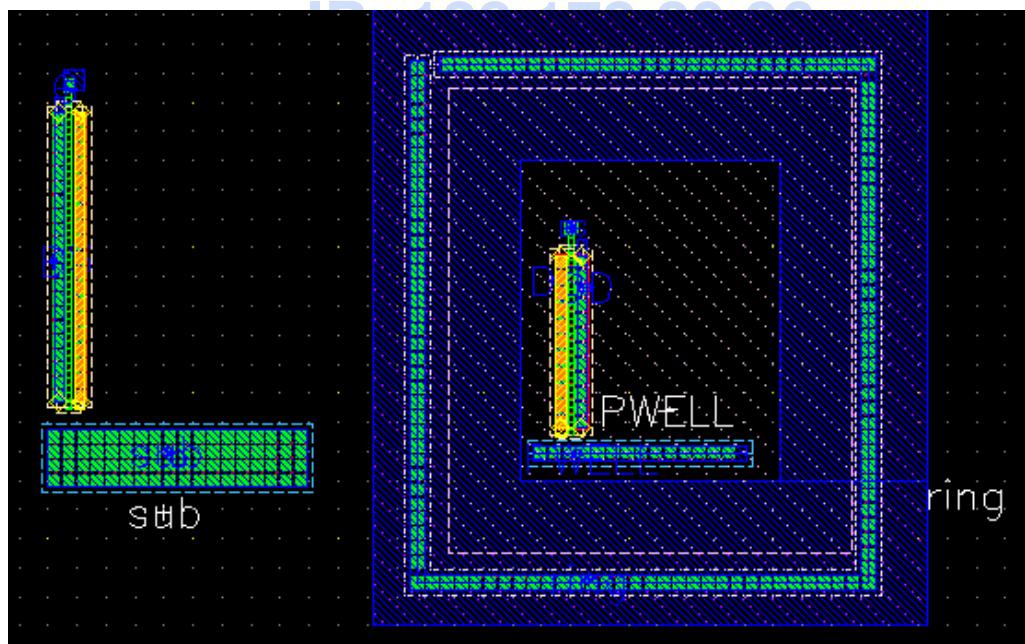
FIGURE 12.6 Deep Nwell connectivity example



12.4 Layout

The Deep Nwell (Cadence layer “dnw”, number 36) can be drawn around a circuit block or an element. At this point, no layout view is provided to generate the Deep Nwell/Nwell ring structure. The user must draw the Deep Nwell, Nwell layers, and ntap and ptap contacts when applicable. The figure below pictures the layout view of the example given in the proceeding section.

FIGURE 12.7 Deep Nwell layout example



12.5 Verification

12.5.1 Design Rules

Please refer to the design rule document for complete details.

12.5.2 LVS

The LVS routine will check for accurate connectivity matching. In addition, the LVS deck provides the “**CompareDnwDiode**” switch. Once enabled, this switch will trigger the comparison of the **Area** and **Perimeter** properties defined in the **ddnw** and **diso** schematic elements with the physical properties, as defined by layout, of the Isolated Pwell.

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12.6 RF and DC Measurement Validation

The deep n-well structure can greatly improve the device isolation from substrate. On the modeling side, in order to provide an accurate RF SPICE model, the impact on both DC and RF performance from the deep n-well must be studied. This section focuses on the deep n-well impact on the *nfet* in the SBC18 technologies. Verification data for CA13/SBL13 is currently unavailable.

12.6.1 Test Structure and Experiment Description

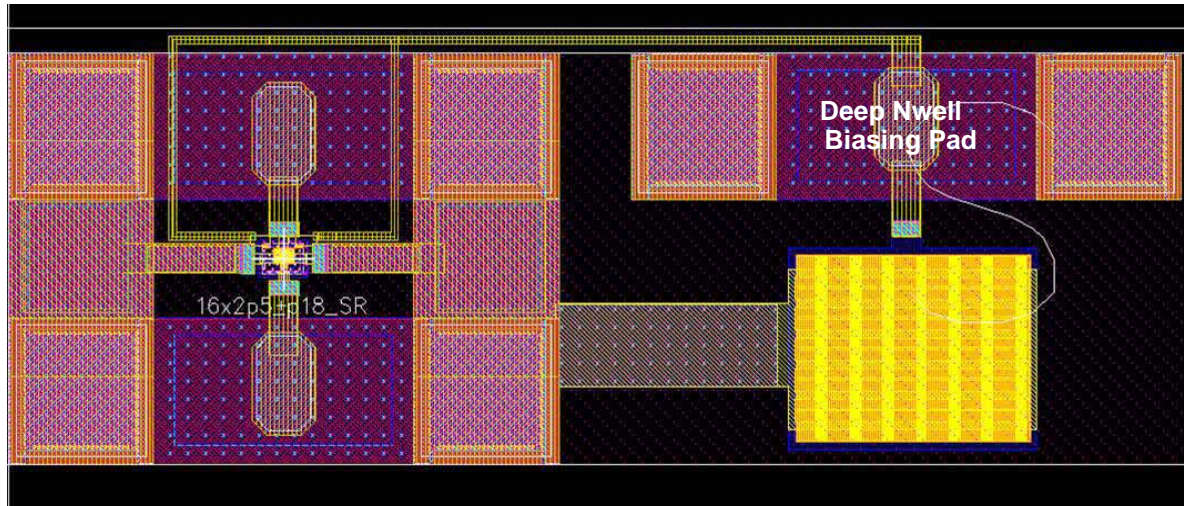
Test structures are fabricated in order to compare the DC and RF performance of deep nwell and standard devices. Table 12.2 lists the 4 types of tests along with test structure description and WELL connections. For all tests, the *gate* is port 1, the *drain* is port 2, and the *source* is connected to ground of the GSG probe.

TABLE 12.2 Test Descriptions

Test Name	Test Structure Description	PWELL	Deep Nwell	P-Sub
<i>NDNW</i>	standard device in P-Substrate	G (of GSG)	NA	G
<i>DNWA</i>	deep Nwell device with isolated PWELL, deep Nwell, and P-Substrate all tied to ground of GSG.	G	G	G
<i>DNWB</i>	deep Nwell device with isolated PWELL and P-Substrate all tied to ground of GSG. Deep Nwell connected to separate DC bias with large de-coupling capacitor.	G	0 V	G
<i>DNWB3</i>	deep Nwell device with isolated PWELL and P-Substrate all tied to ground of GSG. Deep Nwell connected to separate DC bias with large de-coupling capacitor.	G	3 V	G

The DC and S-parameters are measured at different bias conditions. For the RF characterization, the measured raw S-parameters are de-embedded from the *Open* and *Short* S-parameters. After the de-embedding, the Y-parameters are plotted against frequency. We compared Y-parameters with *NDNW* vs. *DNWA*, *DNWA* vs. *DNWB*, and *DNWB* vs. *DNWB3*. The purpose of the *DNWA* vs. *DNWB* comparison is to verify that the DC biasing scheme for the deep Nwell is correct. The Y-parameters for these two cases should be identical since the deep Nwell is grounded in both. The purpose of the *DNWB3* test is to investigate any "pinching" effects of the depletion region into the isolated PWELL. In normal circuit operation, the deep Nwell is biased to the VDD of the circuit. This test will illuminate any requirement to modify the substrate network in the RF MOSFET model for deep Nwell devices. Figure 12.8 shows the layout for the *DNWB* and *DNWB3* measurements. A GSGGSG probe is used to contact the deep Nwell and *drain* at port 2, assuring consistent DC and AC grounding.

FIGURE 12.8 DNWB Layout



12.6.2 DC Measurements and Analysis

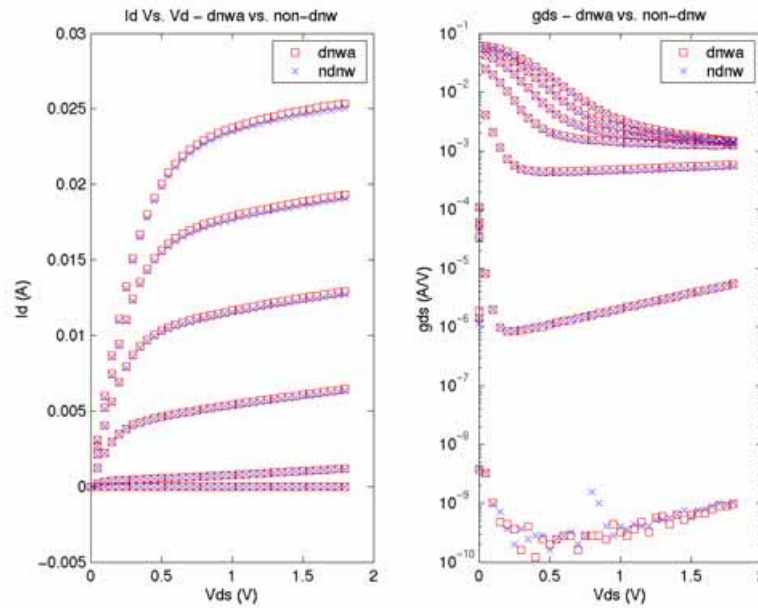
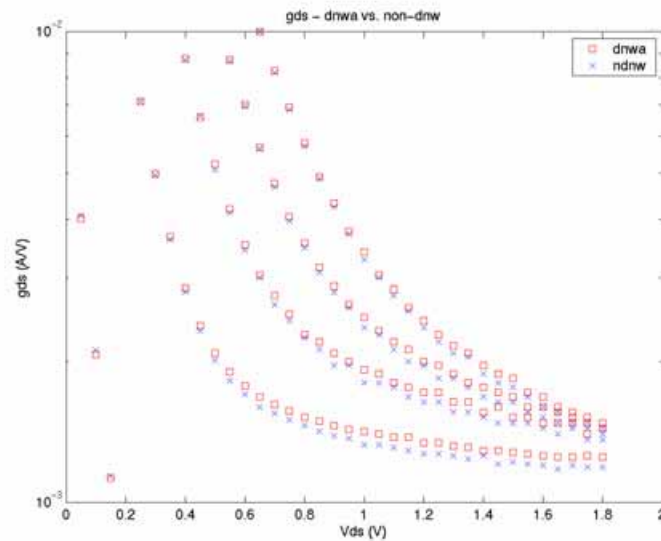
In all 4 cases the DC Output characteristic are measured. The bias conditions are listed Table 12.3.

TABLE 12.3 DC Measurement Conditions

Sweep	Start	Stop	Step
VD	0	1.8	0.05
VG	0	1.8	0.3
VS	0	0	0
VB	0	0	0

In the case of *DNWB* and *DNWB3*, additional DC biases of $V_{dnw}=0$ and $V_{dnw}=3V$ are applied respectively to the Deep Nwell to monitor the change of the drain current I_d and output conductance g_{ds} . The output conductance g_{ds} is derived numerically from the drain current data where a small step = 50mV is applied to keep the g_{ds} smooth. The DC measurement is performed by the Agilent E5270A parametric Measurement Unit.

Figure 12.9 compares the *NDNW* and *DNWA* drain current I_d and output conductance g_{ds} . Figure 12.10 shows a zoom in of the output conductance. The differences seen are on the same order of measurements on exact devices (both without deep Nwell) in different die. Therefore the differences can be attributed to process variation. Furthermore, comparisons of *DNWB* and *DNWB3* yield the same results as expected.

FIGURE 12.9 NDNW vs. DNWA Drain Current I_d FIGURE 12.10 NDNW vs. DNWA Output Conductance g_{ds} 

At $V_G=0.9$, $V_D=1.8$, $\Delta g_{ds}=15\%$

12.6.3 Y-parameter Measurements and Analysis

S-parameter measurements are performed by the Agilent network analyzer E8376B with the frequency sweep from 100MHz to 10.1 GHz. Two step, open-short de-embedding is performed and the results converted to Y-parameters. The DC bias conditions are listed in Table 12.4. Figure through Figure 12.12 display the *NDNW* vs. *DNWA* comparisons for a device with $NF_xW_g \times L_g = 16 \times 2.5 \times 0.18$. The expected potential difference is in $Real(Y_{22})$ where the bulk resistance affects the high frequency data. At low frequencies, $Real(Y_{22})$ is proportional to g_{ds} . The shifts in $Real(Y_{22})$ can be attributed to the difference in the DC output conductance shown in Figure 12.10. Similarly, shifts in the $Real(Y_{21})$ are a result of small differences in the transconductance g_m . The Y-parameters are all close in value and frequency dependence except for $Real(Y_{11})$ and $Real(Y_{12})$ whose values are all close to the dynamic range limit of the NWA¹. It was also discovered that there are minor differences between the gate connection in the layout between the *NDNW* and *DNWA* which can be amplified when operating close to the dynamic range limit. Figure 12.13 through Figure 12.15 show the Y-parameter *NDNW* vs. *DNWA* comparisons for a device with $NF_xW_g \times L_g = 16 \times 2.5 \times 0.3$. All the Y-parameters match, including $Real(Y_{11})$ and $Real(Y_{12})$, whose values are now well above the dynamic range limit due to the increased channel resistance.

To investigate the effects of applying a DC bias to the deep Nwell, the test structures previously described in Figure 12.8 are measured. The first step is to ensure the measurements are accurate. This is achieved by comparing a 0V bias applied to the deep Nwell (*DNWB* test) with the hard wired ground applied to the deep Nwell (*DNWA* test). Figure 12.16 shows the comparison where the Y-parameters are the same except for slight differences in conductances due to different devices. The scale of the plot is very small, thus the differences are very small. The next step is to apply a DC bias of 3V to the deep Nwell (*DNWB3*). Figure 12.17 shows the *DNWB* vs. *DNWB3* comparison where the Y-parameters are exact (no DC difference since the measurements are performed on the same device).

TABLE 12.4 DC Measurement Conditions for S-parameter Sweeps

	VG	VD
sweep 1	1.8	0
sweep 2	0.9	1.8
sweep 3	1.8	1.8

12.6.4 Conclusions

The experiments performed show that the deep Nwell has no influence on the DC or RF performance of the *nfet* devices. Therefore, the MS and RF models are not altered in the presence of deep Nwell. The junction

1. Improved test structures are under development to eliminate measurement error seen in $Real(Y_{11})$ and $Real(Y_{21})$.

isolation effects of the deep Nwell and added terminals are modeled by the **ddnw** component as described in Section 12.2. $W_g=2.5\mu\text{m}$, $L_g=0.18\mu\text{m}$, $NF=16$, $V_d=0$, $V_g=1.8\text{V}$

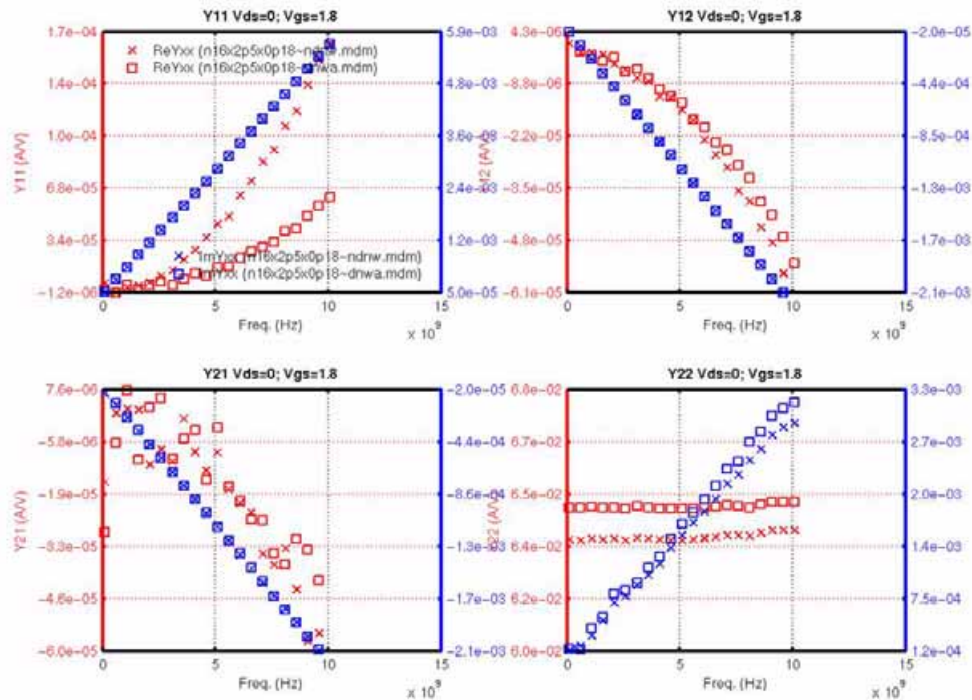


FIGURE 12.11 $W_g=2.5\mu\text{m}$, $L_g=0.18\mu\text{m}$, $NF=16$, $V_d=1.8\text{V}$, $V_g=0.9\text{V}$

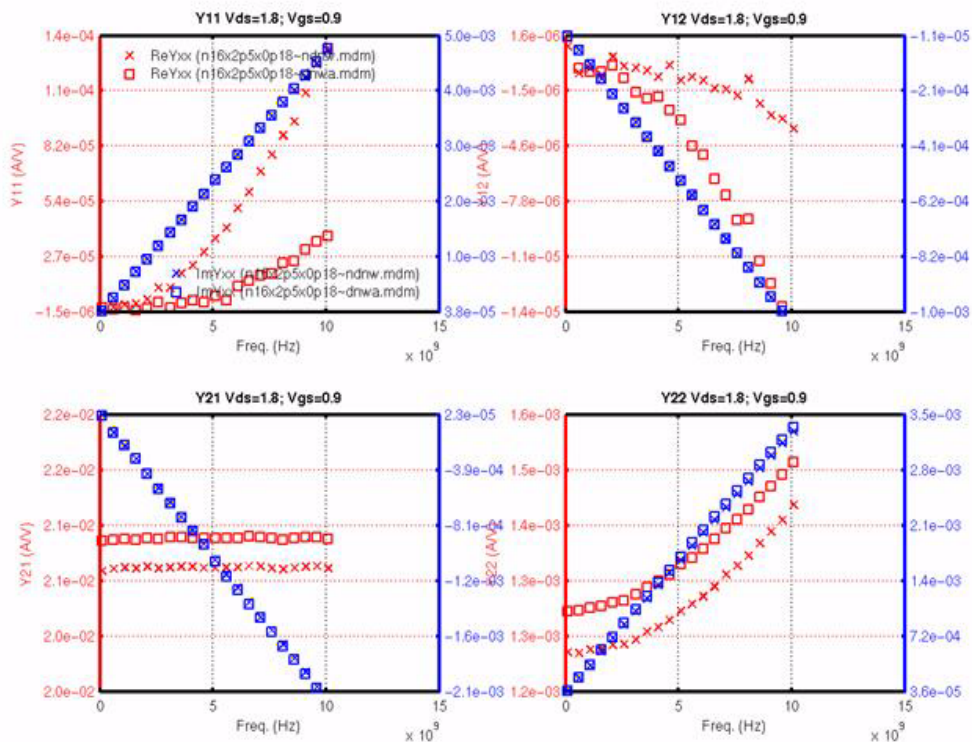


FIGURE 12.12 $W_g=2.5\mu\text{m}$, $L_g=0.18\mu\text{m}$, $NF=16$, $V_d=1.8\text{V}$, $V_g=1.8\text{V}$

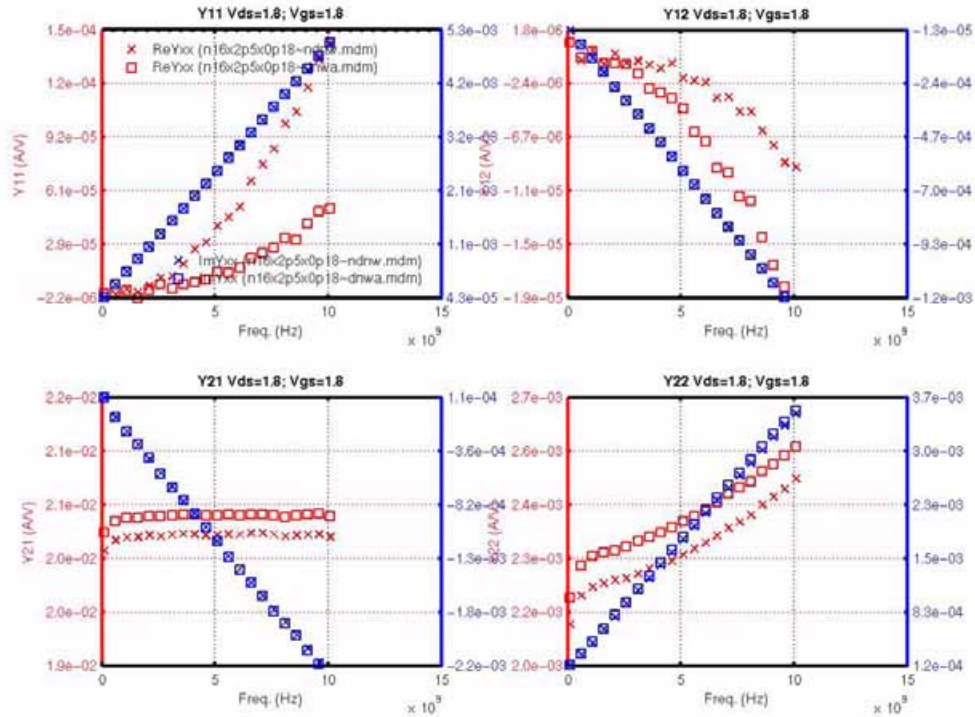


FIGURE 12.13 $W_g=2.5\mu\text{m}$, $L_g=0.3\mu\text{m}$, $NF=16$, $V_d=0$, $V_g=1.8\text{V}$

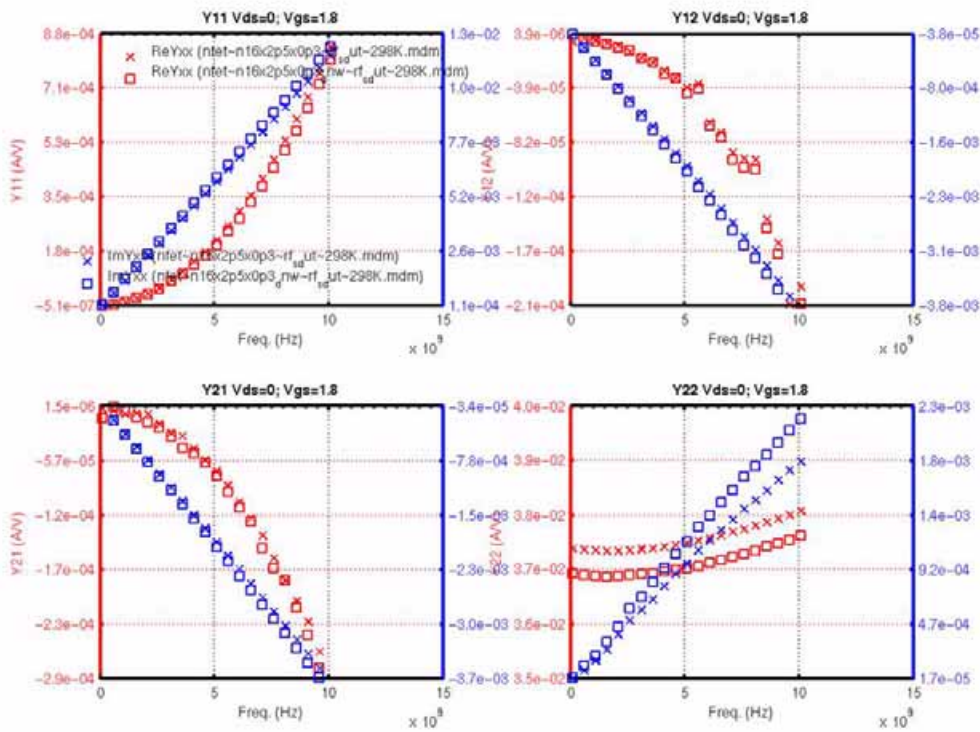


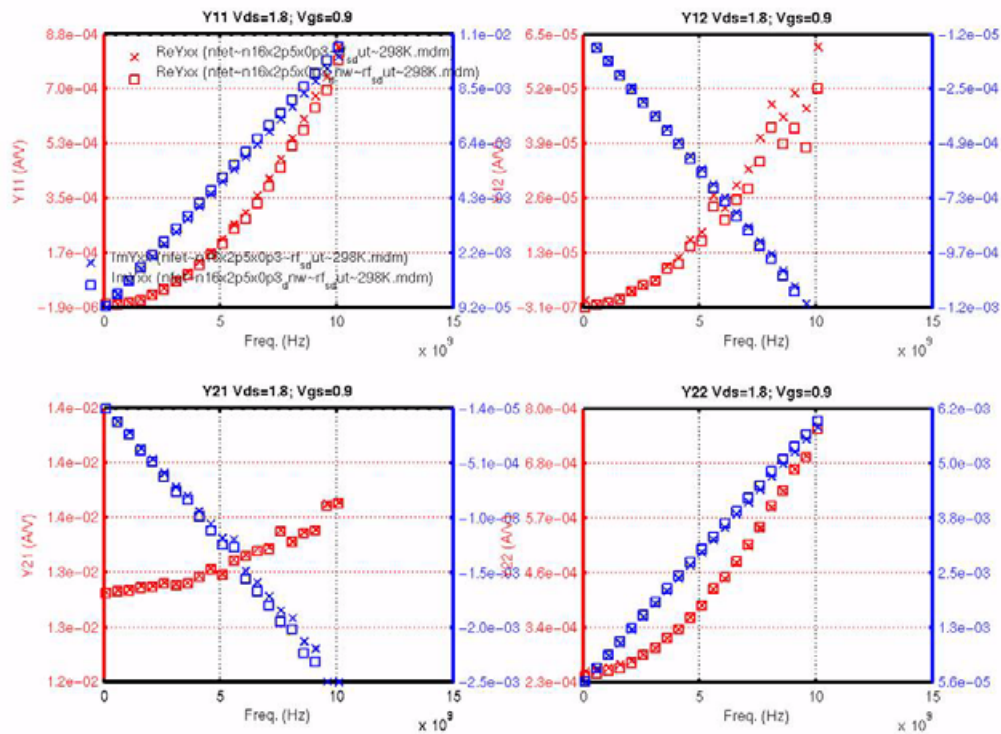
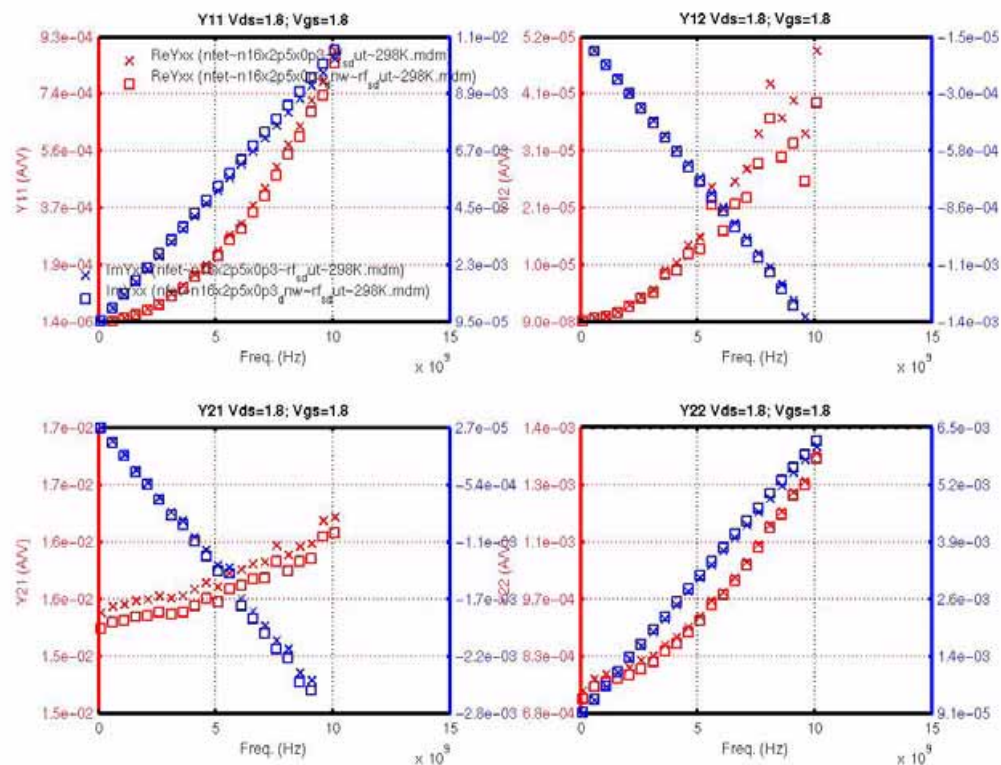
FIGURE 12.14 $W_g=2.5\mu\text{m}$, $L_g=0.3\mu\text{m}$, $NF=16$, $V_d=1.8\text{V}$, $V_g=0.9\text{V}$ FIGURE 12.15 $W_g=2.5\mu\text{m}$, $L_g=0.3\mu\text{m}$, $NF=16$, $V_d=1.8\text{V}$, $V_g=1.8\text{V}$ 

FIGURE 12.16 DNWA vs. DNWB ($W_g=2.5\mu\text{m}$, $L_g=0.18\mu\text{m}$, $NF=16$, $V_d=1.8\text{V}$, $V_g=0.9\text{V}$)

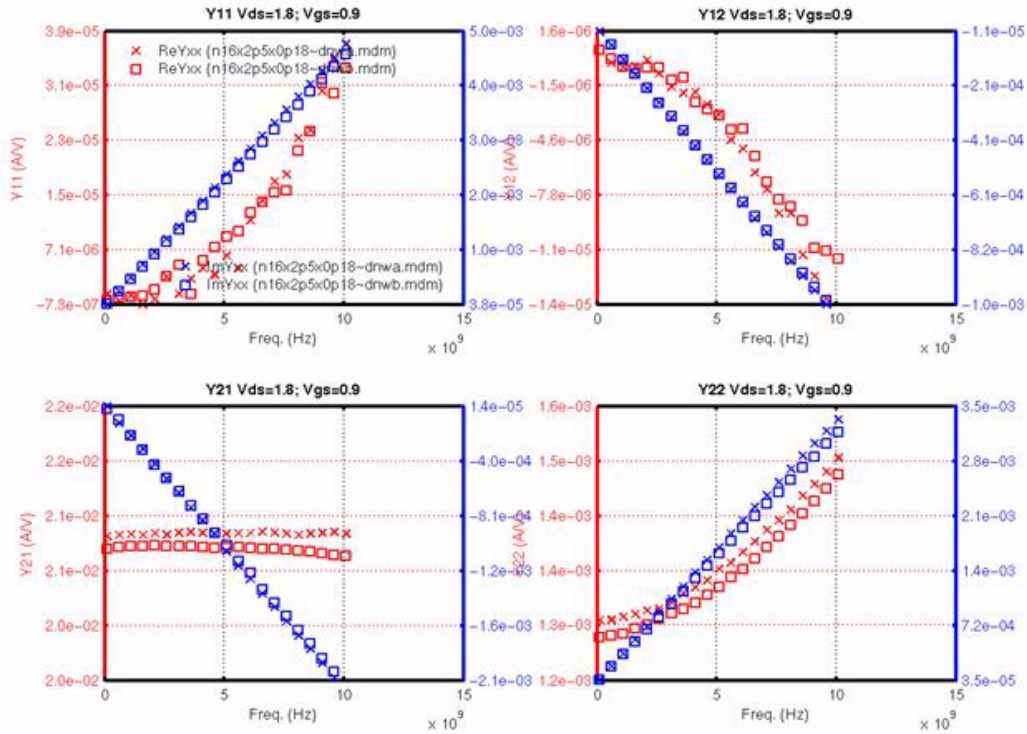
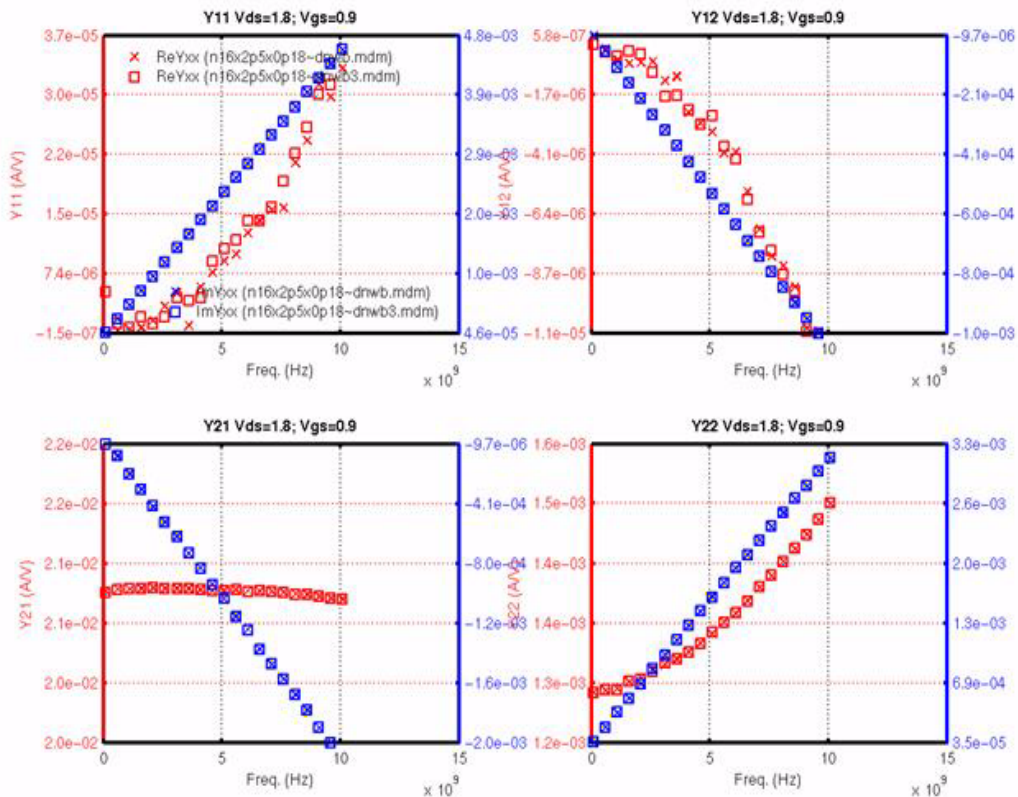


FIGURE 12.17 DNWB vs. DNWB3 ($W_g=2.5\mu\text{m}$, $L_g=0.18\mu\text{m}$, $NF=16$, $V_d=1.8\text{V}$, $V_g=0.9\text{V}$)



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13.0 X-Sigma Corner and Statistical Models

13.1 X-Sigma Corner Models

X-Sigma corner models allow for process variation settings different than conventional corner models which typically set the process variation to worst case ± 3 sigma. Process sigmas, classified into device types, are variable inputs. In their limits, the X-Sigma models align to the limits of the ESPECs. The ESPECs limits are mostly aligned with the PCM limits. Typically, the process may run tighter than the PCM limits. Combined with PCM data tracking, the X-Sigma models allow design to a more aggressive process variation than is predicted by the ESPECs. The added flexibility provides for direct insight into circuit sensitivities previously hidden by the fixed corner settings.

13.1.1 Device Correlation

The X-Sigma models provide 100% correlation among device types. Table 13.1 shows the device class groupings and the related independent process variables which fall under their control. The individual devices are listed in the horizontal axis of the table. Table entries indicate variation caused by the given process variable on the particular device. Some horizontal device names represent groups of devices (e.g. all mosfets in the technology such as nfet, pfet, n3p3fet, p3p3fet are grouped under MOSFET; hs, std and hv npns under NPN). When a process variable affects more than one device type, a judgement is made on the relative significance of the process variable. This in turn determines which class controls the sigma variation. A master slave approach is used where the secondary device, or slave device, follows the variation determined by the master device. For example, the poly CD affects the MOSFETs through ΔL variation and the poly resistors through ΔW variation. Typical channel lengths, on the order of $0.12\mu\text{m}$, are smaller than typical resistor widths on the order of a few microns. Thus the poly CD variation has more impact on the MOSFET and thus is listed under and controlled by the FET device class. A FET sigma set to $+3$ sigma results in a smaller poly CD, yielding higher I_D and a “faster” FET. Conversely, the smaller poly CD yields a larger poly resistance which is considered a “slower” RES. If the RES class is set to $+3$ in this case, the other process variables affecting the poly resistors, sheet rho and end resistance, are set to their $+3$ case, tending towards the “faster”, lower resistance. Combined with the $+3$ FET setting, the poly resistors will not be at their fastest setting due to the smaller width set by the poly CD. The “fastest” poly resistor is only realized when the RES is set to $+3$ and the FET is set to -3 . Figure 13.1 shows a graphical representation of this case. Figure 13.2 shows the X-Sigma variation of some key ESPECs for the STD NPN device.

13.1.2 Design Kit Implementation

Figure 13.3 shows the Cadence analog environment implementation of the X-Sigma models. Entry fields for the sigma number are given for each device class. The legacy corner model buttons are listed for backward compatibility and can not be used in unison with the X-Sigma or STAT models. Once X-Sigma is selected for a device class, all device classes are switched to X-Sigma. When the X-Sigma models are chosen, the device class sigma variables become design variables as shown in the Figure 13.3. Users are then free to access these variables within the environment, enabling custom parametric sweeping for example. Figure 13.4 shows an example VCO circuit and plots resulting from a sweep of the FET global sigma with a parametric CAP global sigma sweep.

TABLE 13.1 X-Sigma Model Matrix

Device Class	Independent Process Variables	Devices							
		NPN	MOSFET	RPOLY	RNWE LL	MI	IND BAL	VARMOS	VPNP
FET	active CD		✓		✓				
	nwell doping				✓			✓	✓
	poly CD		✓	✓					
	LV tox		✓					✓	
	LV NFET channel doping		✓						
	LV NFET flatband voltage		✓						
	LV NFET short channel body effect		✓						
	LV NFET 2nd order body constant		✓						
	LV NFET narrow width effect on VT		✓						
	LV NFET body effect of k3		✓						
	LV NFET Idd impact on Leff		✓						
	LV NFET low field mobility		✓						
	LV PFET channel doping		✓					✓	
	LV PFET flatband voltage		✓					✓	
	LV PFET 2nd order body constant		✓						
	LV PFET narrow width effect on VT		✓						
	LV PFET body effect of k3		✓						
	LV PFET Idd impact on Leff		✓						
	LV PFET low field mobility		✓						
	3.3V HV Tox		✓						
	HV NFET channel doping		✓						
	HV NFET flatband voltage		✓						
	HV NFET short channel body effect		✓						
	HV NFET Idd impact on Leff		✓						
	HV NFET low field mobility		✓						
	HV PFET channel doping		✓						
	HV PFET flatband voltage		✓						
	HV PFET Idd impact on Leff		✓						

TABLE 13.1 X-Sigma Model Matrix

Device Class	Independent Process Variables	Devices							
		NPN	MOSFET	RPOLY	RNWELL	MIM	INDIBAL	VARMOS	VPNP
BJT	emitter window CD	✓							
	emitter-base oxide thickness	✓							
	emitter doping concentration	✓							
	emitter poly CD	✓							
	emitter poly/Si interface	✓							
	base boron doping concentration	✓							
	base thickness	✓							
	collector epi doping concentration	✓							
	collector epi thickness	✓							
	low voltage NPN selective collector implantation dosage	✓							
	high speed NPN selective collector implantation dosage	✓							
	base Ge doping concentration	✓							
	emitter-base recombination concentration	✓							
	buried layer resistance/doping								
	STI thickness	✓		✓					
RES	high value poly doping			✓					
	silicide thickness/sheet rho		✓	✓					
	low value poly doping			✓					
IND	ILD thickness	✓				✓	✓		
	substrate doping	✓							
	contact resistance	✓							
	Metal CD	✓							
	metal thickness/sheet rho	✓				✓	✓		
CAP	MiM tox (area cap)					✓			
	MiM peripheral cap					✓			

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FIGURE 13.1 Example FET and RES X-Sigma Correlation Plots

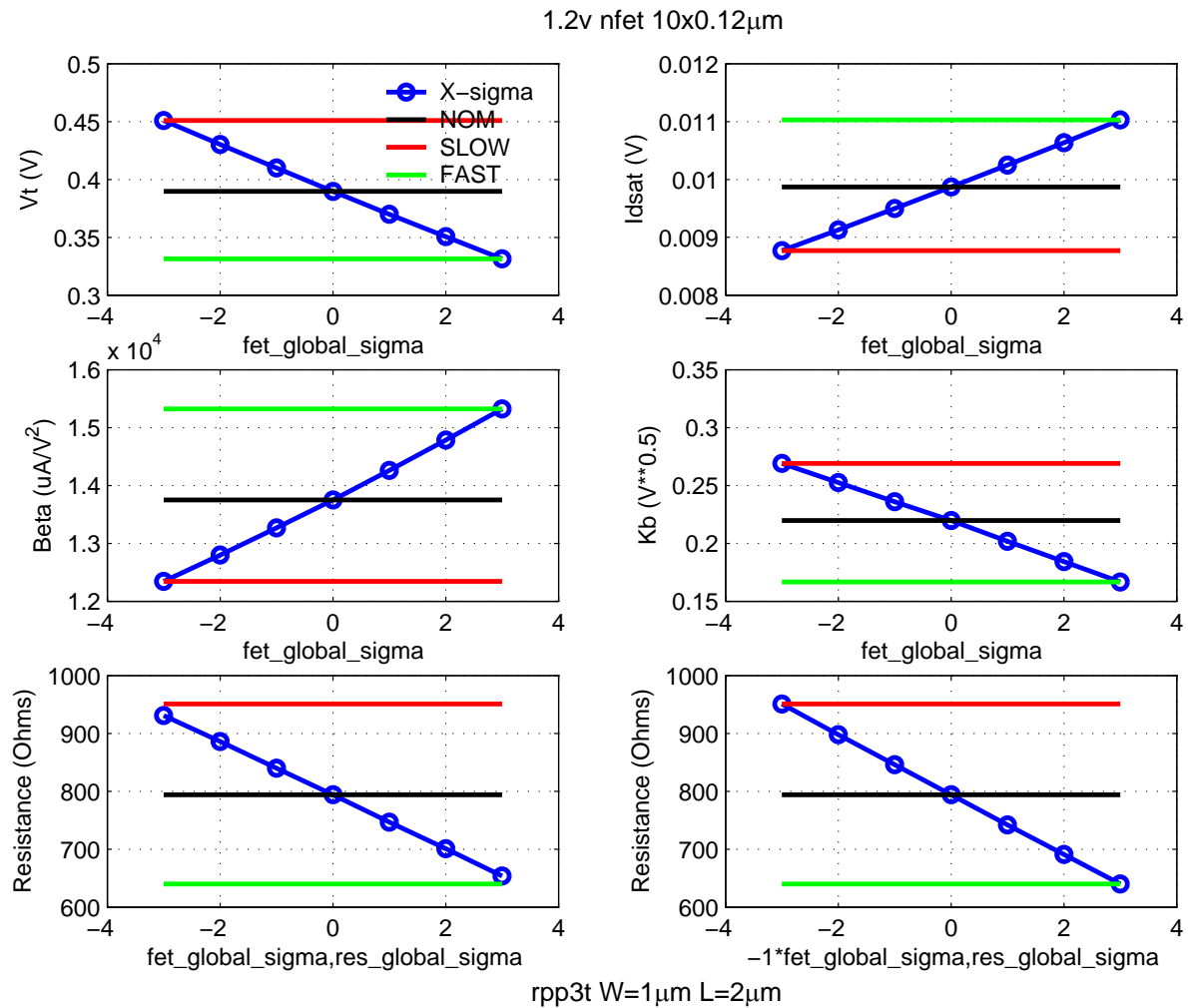
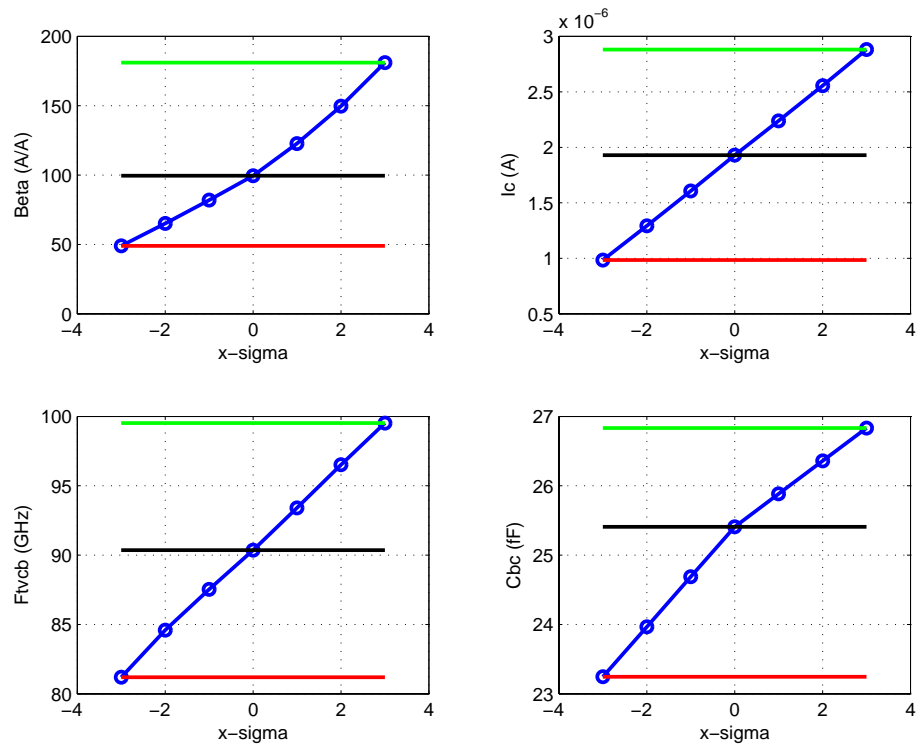


FIGURE 13.2 Example NPN X-Sigma Plots for the LV 0.28x10.0_122 Device



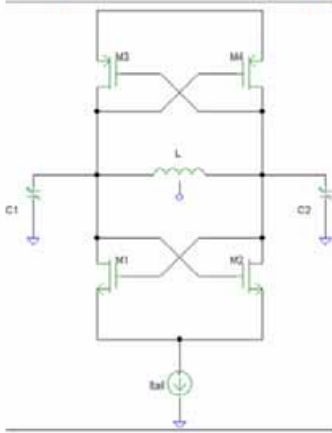
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FIGURE 13.3 JAZZ Design Kit Model Library Selection Form

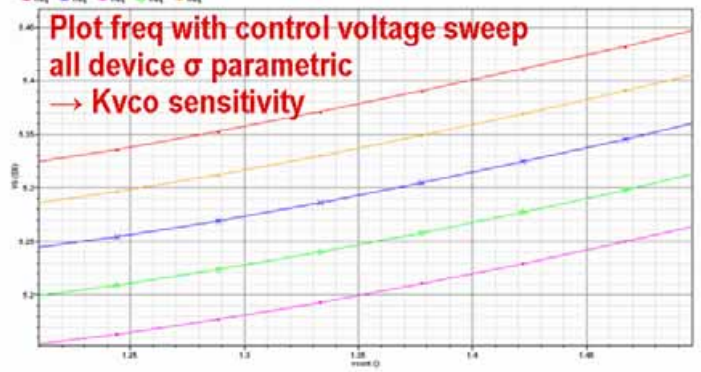
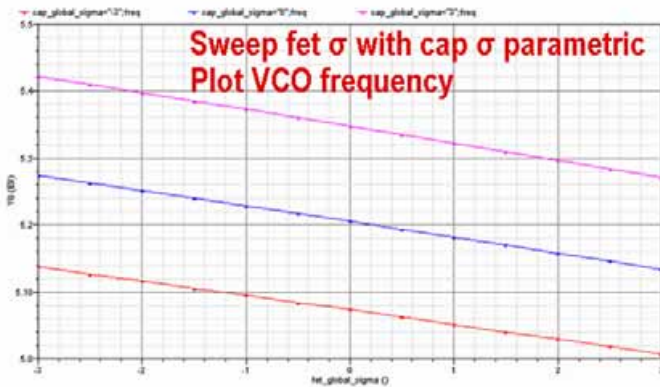
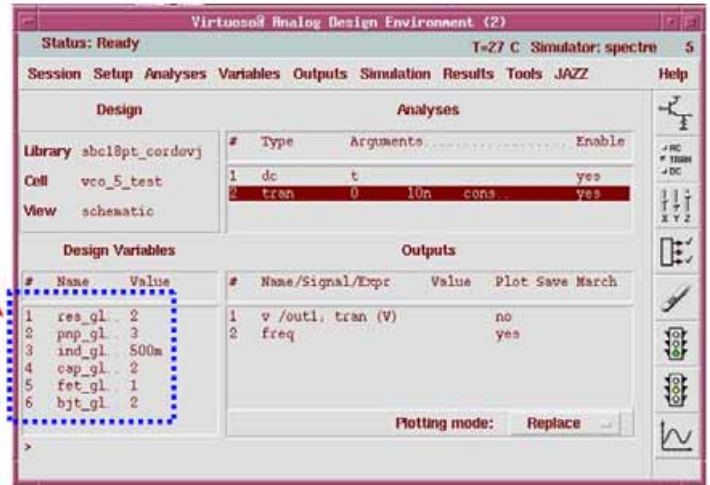
The screenshot shows the 'Jazz Model Libraries' dialog box. The 'Library' is set to 'sbc18pt' and 'Versions' to 'v6.0 (default)'. The 'statistics comers' section is highlighted with a blue dashed box and labeled 'Provided for backward compatibility'. The 'res comers' section is also highlighted. The 'fet comers' section has a 'STAT' radio button selected, and the 'X_SIGMA' value is set to 1.5. The 'bjt comers' section has a 'STAT' radio button selected, and the 'X_SIGMA' value is set to -2. The 'hpvar comers' section has a 'STAT' radio button selected, and the 'X_SIGMA' value is set to 0. The 'cap comers' section has a 'STAT' radio button selected, and the 'X_SIGMA' value is set to -3. The 'ind comers' section has a 'STAT' radio button selected, and the 'X_SIGMA' value is set to 0. A red arrow points to the 'STAT' radio button in the 'bjt comers' section, labeled 'Set σ_s '. Another red arrow points to the 'STAT' radio button in the 'res comers' section, labeled 'Run stat on device class basis'.

FIGURE 13.4 X-Sigma Parametric Sweep Example

Simple VCO Example



Access σ_s as design variables



IP: 128.173.89.96

13.2 Statistical Models

Statistical models provide the most accurate simulation of the process variation at the expense of simulation time. The random nature of Monte-Carlo simulation emulates the true process variation. The statistical and X-Sigma models use the same model libraries and statistical mappings. Thus, Table 13.1 applies fully to the statistical models. The difference lies in the amount of sigma variation (simulator defined for statistical simulation, user defined for the X-Sigma model simulation). In the V6.0 model and related design kit release, the statistical simulation is set by device class as shown in Figure 13.3. Prior releases required simultaneous statistical simulation of all devices. Isolated statistical simulation provides more direct access to circuit sensitivities to particular devices. Statistical simulation of one device (or multiple) device class can be combined with X-Sigma simulation of another (or multiple) device class. The statistical models are not compatible with the legacy corner models.

13.3 Verification

Tables for each device type showing the corner and statistical simulation match to the technology ESPECs are contained in the relevant device chapters of this design manual.

14.0 Layout Parasitics

Jazz supports Calibre and Assura parasitic extraction in the CA13/SBL13 design kit. Table 12.4 gives a detailed device by device breakdown of what parasitics are included in the model compared to parasitics extracted by Calibre and Assura.

TABLE 14.1 Parasitic Extraction Reference Table

Device Model	Included in Model	Included in Extraction Deck
NPN	<ul style="list-style-type: none"> ✓ M1, via1, and M2 on E and C ✓ M1 on B 	<ul style="list-style-type: none"> ✓ via2 and M3
MS MOSFET	<ul style="list-style-type: none"> ✓ When the mos primitive is used alone (i.e. nfet instead of nfets), it represents a single "finger" of a device with nominal source/drain area/perimeter. HDIF parameter helps estimate multiple finger scaling. ✓ When the sub circuit wrapper is used (i.e. nfets), the source/drain is calculated to be shared between the fingers and also scaled based on the "current" parameter. The default source/drain size uses the minimum design rule size for the gate/source/drain. ✓ No gate or contact resistance is modeled. 	<ul style="list-style-type: none"> ✓ Gate resistance, contact resistance, etc. even in active region ✓ Each finger is extracted separately with the proper shared source/drain also calculated. ✓ All metal interconnect.
RF MOSFET	<ul style="list-style-type: none"> ✓ all source/drain area and perimeter calculations ✓ gate poly resistance and metal interconnect over active 	<ul style="list-style-type: none"> ✓ source, drain, and gate connections on the ends of the fingers including gate poly resistance over STI and contact resistance ✓ number of gate fingers extracted and passed to the model

Device Model	Included in Model	Included in Extraction Deck
Resistors/Fuse	<ul style="list-style-type: none"> ✓ Head resistance/capacitance on poly. This is an Espec value that includes the contact resistance. Head resistance scales inversely with width because more contacts are included with a wider resistor. ✓ Body resistance/capacitance on poly. ✓ Well-to-sub resistance and diode. 	<ul style="list-style-type: none"> ✓ All metal and interconnect except contact. Contact is part of the head resistance and is NOT extracted.
MIM Capacitor	<ul style="list-style-type: none"> ✓ bottom metal resistance and capacitance ✓ topmm resistance and capacitance ✓ top metal resistance including via to topmm ✓ Well-to-sub resistance and diode. 	<ul style="list-style-type: none"> ✓ bottom metal access resistance (see Section 11.1.1 on page 347)
Varactor_MOS	<ul style="list-style-type: none"> ✓ All M1, M2, via1, poly, and contacts over device area inside Nwell ✓ fingers (nf) and slices (ns) included ✓ 1 Nwell per device which scales with w,l, ns and nf. 	<ul style="list-style-type: none"> ✓ nf and ns extracted and passed to the model ✓ metal interconnect of end regions connecting up fingers outside of Nwell
Inductor/Balun	<ul style="list-style-type: none"> ✓ All metal parasitics 	<ul style="list-style-type: none"> ✓ Any interconnect outside of the inductor marking layer LCELL ✓ Connection metal not included with pcell but drawn on LCELL is ignored.
VPNP	<ul style="list-style-type: none"> ✓ No metal or contact parasitics 	<ul style="list-style-type: none"> ✓ All metal interconnect ✓ All contact resistance