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**Design Kit:** IBM BiCMOS8HP

**Version**: 1.2.3.0

**Date:** MAY 21st, 2012.

**ADS Versions supported**: ADS 2011.01 and above

**Description:** ADS Front End (Schematic & Layout Artwork) Design kit for the IBM BiCMOS8HP process. This design kit provides components and parameters specific to schematic & layout flow only.

## List of components (SChematic)

All the components provided along with this design kit are divided into 4 palette groups:

1. IBM BiCMOS8HP Passives.
2. IBM BiCMOS8HP Actives.
3. IBM BiCMOS8HP InterConnects.
4. IBM BiCMOS8HP ESD

The tables below list all the available components. The table name represents

“Component Group” (“Palette containing the component”)

### *PROCESS (IBM BiCMOS8HP Passives)*

|  |  |
| --- | --- |
| Component Name | Description |
| IBM\_bicmos8hp\_Process | Technology process include: Used for selecting corners and setting variables to setup simulation |

### *RESISTORS (IBM BiCMOS8HP Passives*)

|  |  |
| --- | --- |
| Component Name | Description |
| IBM\_bicmos8hp\_kqres | TaN BEOL Resistor. |
| IBM\_bicmos8hp\_kqres\_inh | TaN BEOL Resistor with implicit pin. |
| IBM\_bicmos8hp\_nsres | N+ Subcollector Resistor. |
| IBM\_bicmos8hp\_nsres\_inh | N+ Subcollector Resistor with implicit pin. |
| IBM\_bicmos8hp\_opppcres | P+ Poly Resistor. |
| IBM\_bicmos8hp\_opppcres\_inh | P+ Poly Resistor with implicit pin. |
| IBM\_bicmos8hp\_oprrpres | RR Poly Resistor. |
| IBM\_bicmos8hp\_oprrpres\_inh | RR Poly Resistor with implicit pin. |

### *CAPACITORS (IBM BiCMOS8HP Passives)*

|  |  |
| --- | --- |
| Component Name | Description |
| IBM\_bicmos8hp\_mim | MIM Capacitor. |
| IBM\_bicmos8hp\_mim\_inh | MIM Capacitor with implicit pin. |
| IBM\_bicmos8hp\_dgncap | Thick-Oxide (2.5 V) nMOS Varactor. |
| IBM\_bicmos8hp\_dgncap\_inh | Thick-Oxide (2.5 V) nMOS Varactor with implicit pin. |
| IBM\_bicmos8hp\_ncap | Thin-Oxide (1.2 V) nMOS Varactor. |
| IBM\_bicmos8hp\_ncap\_inh | Thin-Oxide (1.2 V) nMOS Varactor with implicit pin. |
| IBM\_bicmos8hp\_diffncap | Thin-oxide Varactor. |
| IBM\_bicmos8hp\_diffncap\_inh | Thin-oxide Varactor with implicit pin. |

### *INDUCTORS (IBM BiCMOS8HP Passives)*

|  |  |
| --- | --- |
| Component Name | Description |
| IBM\_bicmos8hp\_ind | Single level octagonal spiral Inductor. |
| IBM\_bicmos8hp\_ind\_inh | Single level octagonal spiral Inductor, with implicit pin. |
| IBM\_bicmos8hp\_symind | Octagonal Inductor, with two coupled spirals. |
| IBM\_bicmos8hp\_symind\_inh | Octagonal Inductor, with two coupled spirals and an implicit pin. |

### *DIODES (IBM BiCMOS8HP Actives)*

|  |  |
| --- | --- |
| Component Name | Description |
| IBM\_bicmos8hp\_divpnp | DI diode (BJT Model). |
| IBM\_bicmos8hp\_havar | Hyper-Abrupt Junction Varactor Diode. |
| IBM\_bicmos8hp\_havar\_inh | Hyper-Abrupt Junction Varactor Diode, with implicit pin. |

### *LVS (IBM BiCMOS8HP Passives)*

|  |  |
| --- | --- |
| Component Name | Description |
| IBM\_bicmos8hp\_diodenwx | Nwell to Substrate Junction Diode. |
| IBM\_bicmos8hp\_diodenx | N+ to Substrate Junction Diode. |
| IBM\_bicmos8hp\_diodepisx | N-isolation(PI) to Substrate(SX) Junction Diode. |
| IBM\_bicmos8hp\_diodepnw | P+ Diffusion to Nwell Junction Diode. |
| IBM\_bicmos8hp\_diodepwpi | Pwell to N-isolation(PI) Junction Diode. |
| IBM\_bicmos8hp\_tdndsx | N+ Tiedown. |
| IBM\_bicmos8hp\_tdpdnw | P+ Tiedown. |
| IBM\_bicmos8hp\_pcapc | Extracted parasitic capacitance. |
| IBM\_bicmos8hp\_rcnet | Extracted parasitic resistance/capacitance |
| IBM\_bicmos8hp\_lvsres | LVS Resistor. |

### *CHIP (IBM BiCMOS8HP Passives)*

|  |  |
| --- | --- |
| Component Name | Description |
| IBM\_bicmos8hp\_bondpad | Top metal bondpad C4 or WB over backplate NS or M1. |
| IBM\_bicmos8hp\_bondpad\_inh | Top metal bondpad C4 or WB over backplate NS or M1,implicit third terminal. |

### *INTERCONNECTS (IBM BiCMOS8HP InterConnects)*

|  |  |
| --- | --- |
| Component Name | Description |
| IBM\_bicmos8hp\_gap | Gap model. |
| IBM\_bicmos8hp\_tee | Tee model AM/MQ and AM/MQ-1 with/without side shields. |
| IBM\_bicmos8hp\_bend | Bend model. |
| IBM\_bicmos8hp\_open | Microstrip open stub model. |
| IBM\_bicmos8hp\_short | Microstrip short stub model. |
| IBM\_bicmos8hp\_step | Step model. |
| IBM\_bicmos8hp\_taper | Taper model. |
| IBM\_bicmos8hp\_yjunction | Yjunction model AM/MQ and AM/MQ-1 with/without side shields. |
| IBM\_bicmos8hp\_radialstub | Microstrip radial stub model. |
| IBM\_bicmos8hp\_coupledcpw | Coupled coplanar T-line model. |
| IBM\_bicmos8hp\_coupledwires | Coupled wires T-line model. |
| IBM\_bicmos8hp\_singlecpw | Single coplanar T-line model. |
| IBM\_bicmos8hp\_singlewire | Single wire T-line model. |
| IBM\_bicmos8hp\_rfline | Transmission line model for AM line over substrate. |
| IBM\_bicmos8hp\_rfline\_inh | Transmission line model for AM line over substrate, with implicit pin. |
| IBM\_bicmos8hp\_langecoupler | Langecoupler model. |
| IBM\_bicmos8hp\_ratracehybrid | Ratracehybrid model (subcircuit uses basic InterConnects). |
| IBM\_bicmos8hp\_meanderline1 | Meanderline model (subcircuit uses basic InterConnects). |
| IBM\_bicmos8hp\_meanderline2 | Meanderline model (subcircuit uses basic InterConnects). |
| IBM\_bicmos8hp\_branchcoupler0 | Branchcoupler model (subcircuit uses basic InterConnects). |
| IBM\_bicmos8hp\_branchcoupler1 | Branchcoupler model (subcircuit uses basic InterConnects). |
| IBM\_bicmos8hp\_branchcoupler2 | Branchcoupler model (subcircuit uses basic InterConnects). |
| IBM\_bicmos8hp\_powerdivider0 | Powerdivider model (subcircuit uses basic InterConnects). |
| IBM\_bicmos8hp\_powerdivider1 | Powerdivider model (subcircuit uses basic InterConnects). |
| IBM\_bicmos8hp\_powerdivider2 | Powerdivider model (subcircuit uses basic InterConnects). |

### *FUSE (IBM BiCMOS8HP Passives)*

|  |  |
| --- | --- |
| Component Name | Description |
| IBM\_bicmos8hp\_efuse | Polysilicide Electrically Programmable Fuse. |

### *CONTACTS (IBM BiCMOS8HP Passives)*

|  |  |
| --- | --- |
| Component Name | Description |
| IBM\_bicmos8hp\_subc | Substrate contact |
| IBM\_bicmos8hp\_subc\_inh | Substrate contact |

### *FETS (IBM BiCMOS8HP Actives)*

|  |  |
| --- | --- |
| Component Name | Description |
| IBM\_bicmos8hp\_nfet | 1.5V NFET. |
| IBM\_bicmos8hp\_nfet\_inh | 1.5V NFET, with implicit pin. |
| IBM\_bicmos8hp\_pfet | 1.5V PFET. |
| IBM\_bicmos8hp\_pfet\_inh | 1.5V PFET, with implicit pin. |
| IBM\_bicmos8hp\_dgnfet | 2.5V DG NFET. |
| IBM\_bicmos8hp\_dgnfet\_inh | 2.5V DG NFET, with implicit pin. |
| IBM\_bicmos8hp\_dgpfet | 2.5V DG PFET. |
| IBM\_bicmos8hp\_dgpfet\_inh | 2.5V DG PFET, with implicit pin. |
| IBM\_bicmos8hp\_nfet\_rf | 1.5V NFET RF subcircuit. |
| IBM\_bicmos8hp\_dgnfet\_rf | 2.5V DG NFET. |
| IBM\_bicmos8hp\_pfet\_rf | 1.5V PFET RF subcircuit. |
| IBM\_bicmos8hp\_dgpfet\_rf | 2.5V DG PFET. |
| IBM\_bicmos8hp\_nfettw | 1.5V Triple Well NFET. |
| IBM\_bicmos8hp\_dgnfettw | 2.5V Triple Well NFET. |
| IBM\_bicmos8hp\_nfettw\_rf | 1.5V Triple Well NFET RF subcircuit. |
| IBM\_bicmos8hp\_dgnfettw\_rf | 2.5V Triple Well NFET RF subcircuit. |

### *NPN (IBM BiCMOS8HP Actives)*

|  |  |
| --- | --- |
| Component Name | Description |
| IBM\_bicmos8hp\_npn | NPN Bipolar Junction Transistor. |
| IBM\_bicmos8hp\_npn \_inh | NPN Bipolar Junction Transistor, with implicit pin. |
| IBM\_bicmos8hp\_npncbe |  |
| IBM\_bicmos8hp\_npncbe\_inh |  |
| IBM\_bicmos8hp\_vpnpsx | Vertical PNP Subcircuit w/ Parasitic Diode. |

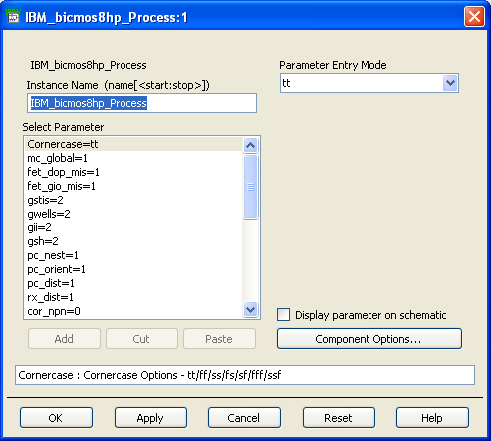
### ESD (*IBM BiCMOS8HP ESD)*

|  |  |
| --- | --- |
| Component Name | Description |
| IBM\_bicmos8hp\_esdndsx | N- diff to Substrate Junction Diode. |
| IBM\_bicmos8hp\_esdnwsx | N-Well to Substrate Junction Diode. |
| IBM\_bicmos8hp\_esdvpnp | ESD diode - P+ Nwell or P+ Nwell plus NS. |
| IBM\_bicmos8hp\_antiparallel\_diodes | Anti parallel Diodes. |
| IBM\_bicmos8hp\_darlington\_clamp | Darlington Clamp. |
| IBM\_bicmos8hp\_double\_diode\_n | ESD Double Diode. |
| IBM\_bicmos8hp\_rc\_clamp | RC Clamp. |
| IBM\_bicmos8hp\_rc\_clamp25 | 2.5V RC Clamp. |

## Setting up Simulation

Before you begin to simulate, you need to place the component: “**IBM\_bicmos8hp\_Process”** on the schematic. This is to ensure that all model directories needed to simulate components are included.

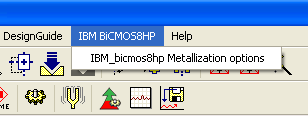
All corners and global switches can be set using this component as shown below:



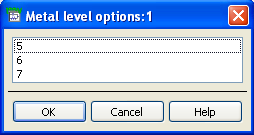
## Setting the Metal Option

The Metal option in this PDK can be set through a toolbar menu “IBM BiCMOS8HP” in the Schematic window. Setting the metal option (nlev) is a two step process as explained below.

1. Click on the toolbar menu “IBM BiCMOS8HP” and select the only sub-menu option “IBM\_bicmos8hp Metallization options”.



1. Clicking on the sub-menu option opens up a new window, where the user can select one of the three available metal options for the PDK. Once the option is selected, click “OK” to exit.



## Known Issues

Listed below are some known issues:

1. The values of the calculated “Parasitics” in the FETs might not be correct in case of ‘Interdigited Layout = Yes’.
2. The calculated Segment lengths for components ‘branchcoupler1’ & ‘branchcoupler2’ might not be correct for higher values of ‘wh’ or ‘wv’ (approximately, > 38um).
3. The component ‘langecoupler’ would fail to simulate in the latest available ADS (2011.10).

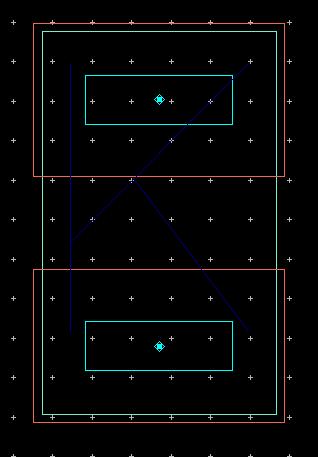
\*\*This problem would be addressed in the future release of ADS.

# Layout Flow

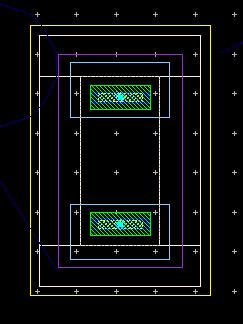
## Available Layout Artworks

List of Layout components in the PDK (screenshot provided)

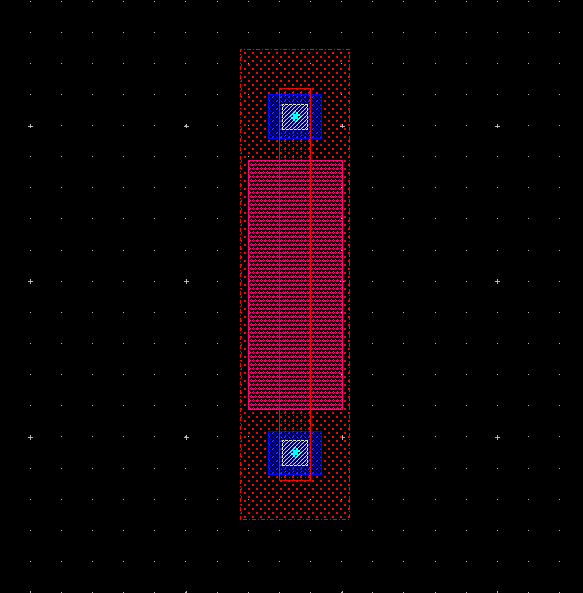
1. kqres



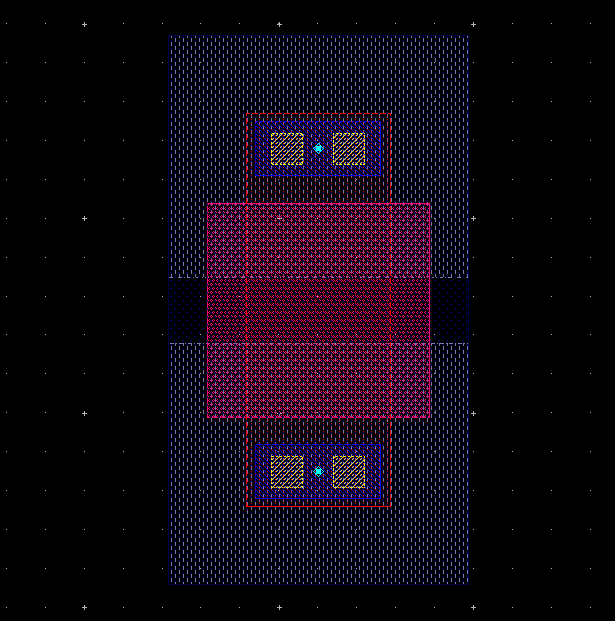
1. kqres\_inh
2. nsres



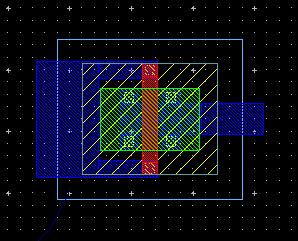
1. nsres\_inh
2. opppcres



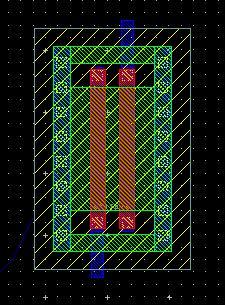
1. opppcres\_inh
2. oprrpres



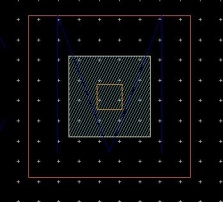
1. oprrpres\_inh
2. dgncap



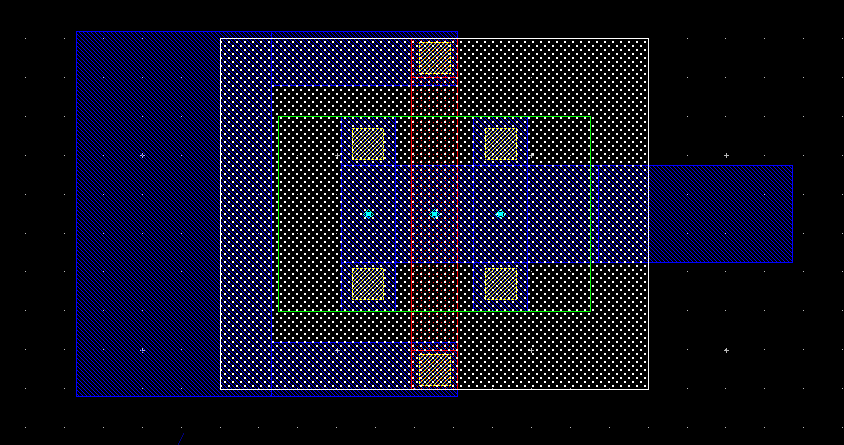
1. dgncap\_inh
2. diffncap



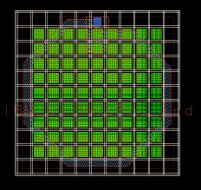
1. diffncap\_inh
2. mim



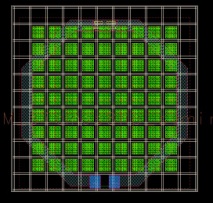
1. mim\_inh
2. ncap



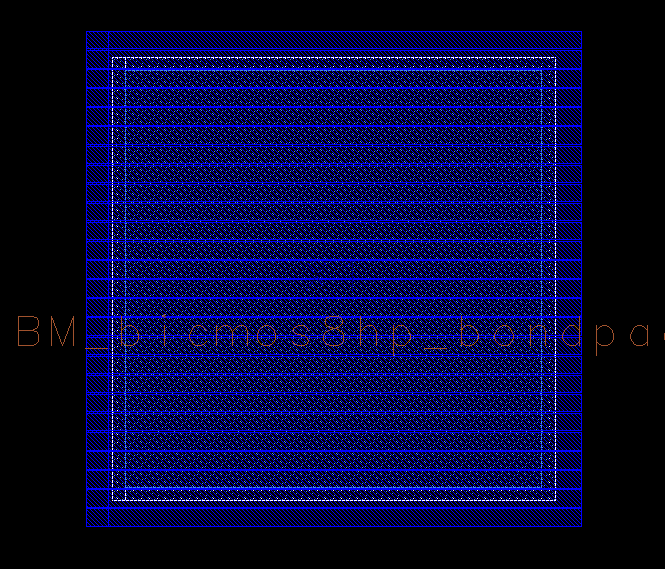
1. ncap\_inh
2. ind



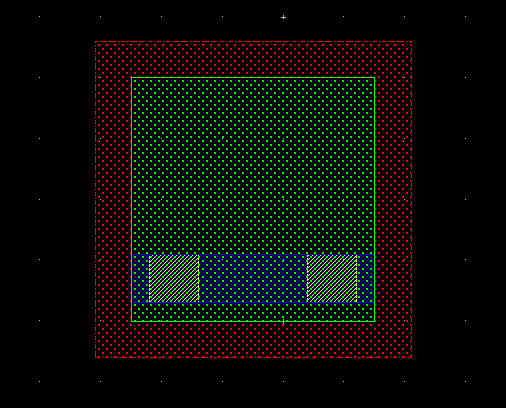
1. ind\_inh
2. symind



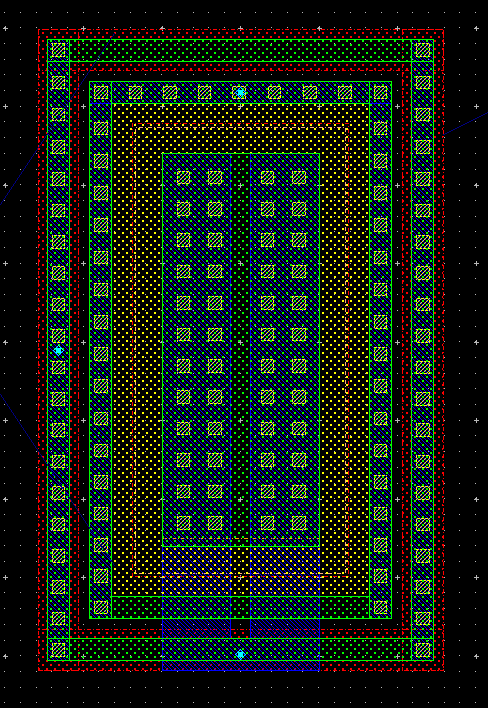
1. symind\_inh
2. bondpad



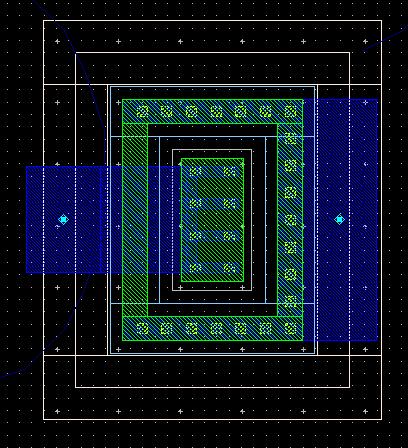
1. bondpad\_inh
2. subc



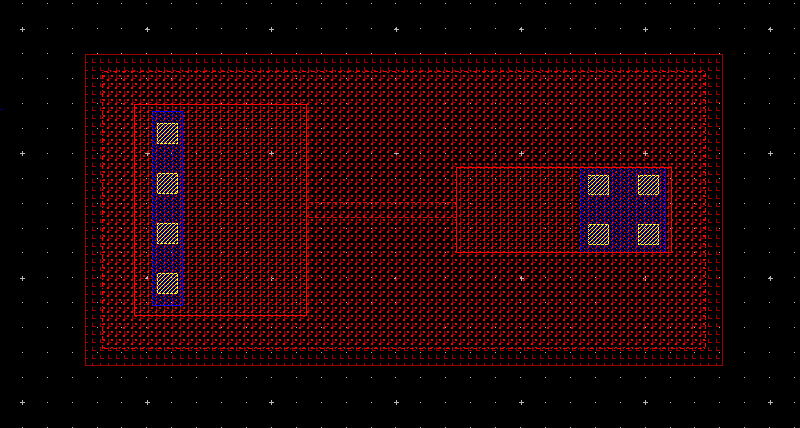
1. subc\_inh
2. divpnp



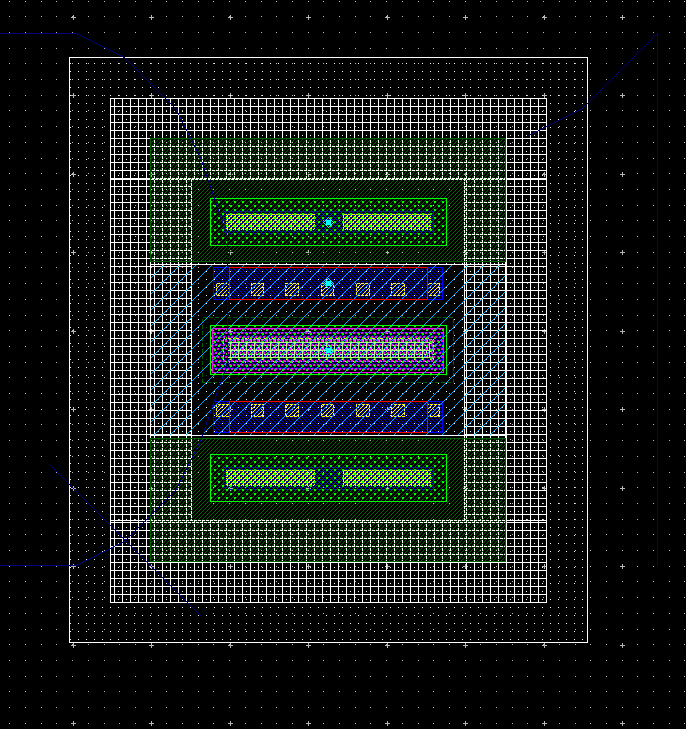
1. havar



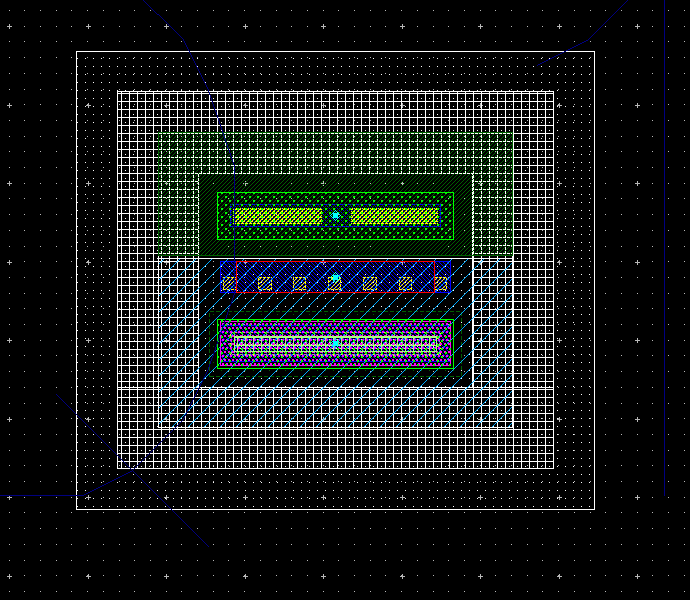
1. havar\_inh
2. efuse



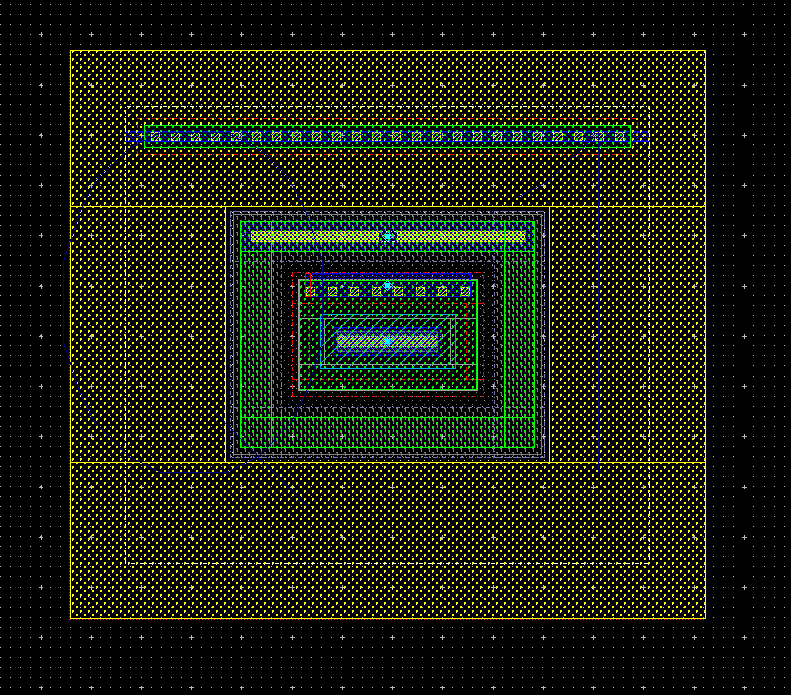
1. npn



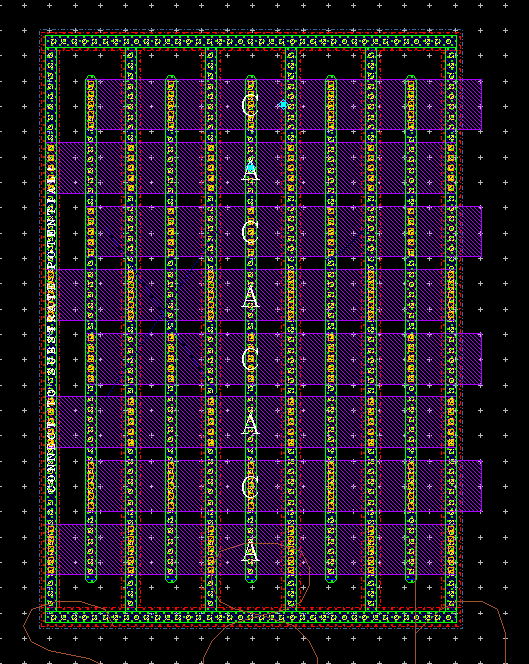
1. npn\_inh
2. npncbe



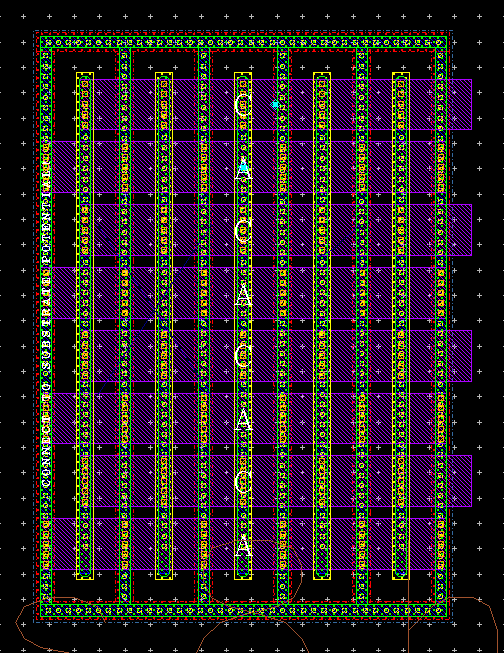
1. npncbe\_inh
2. vpnpsx



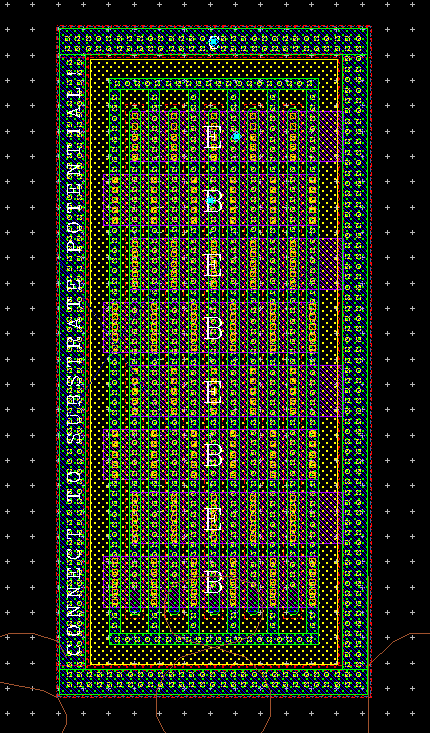
1. esdndsx



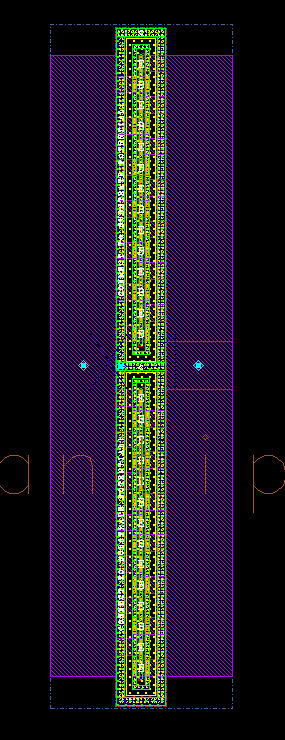
1. esdnwsx



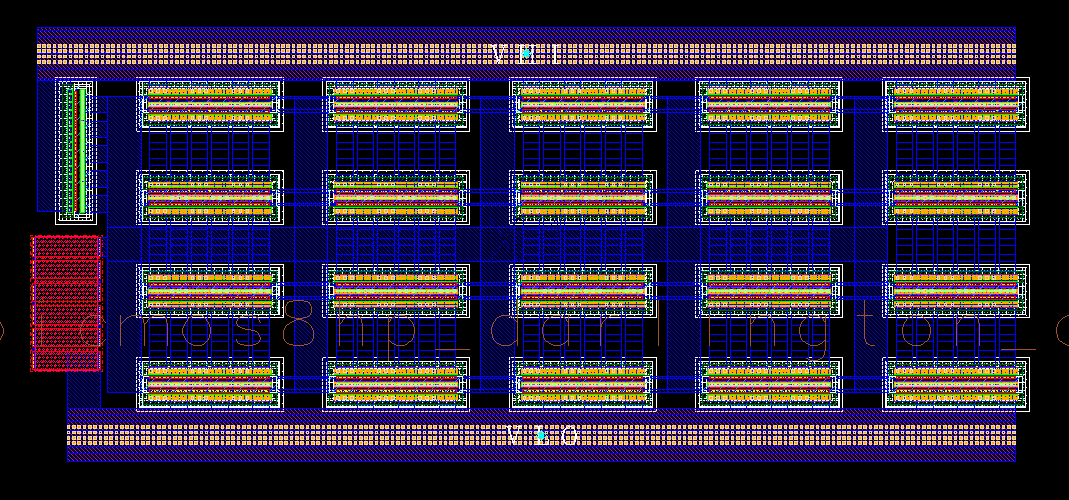
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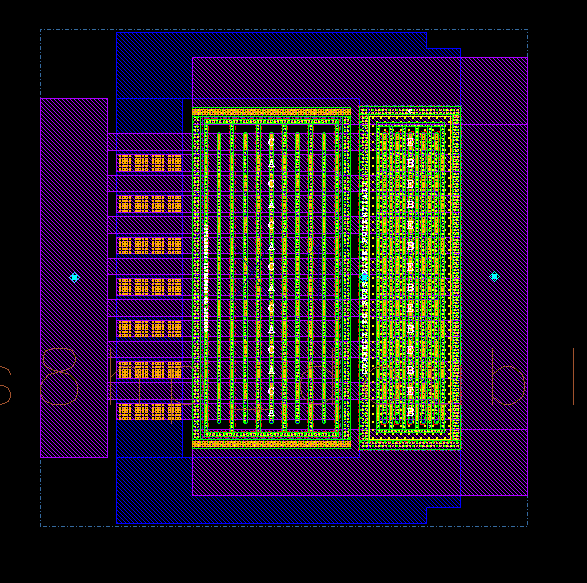
1. antiparallel\_diodes



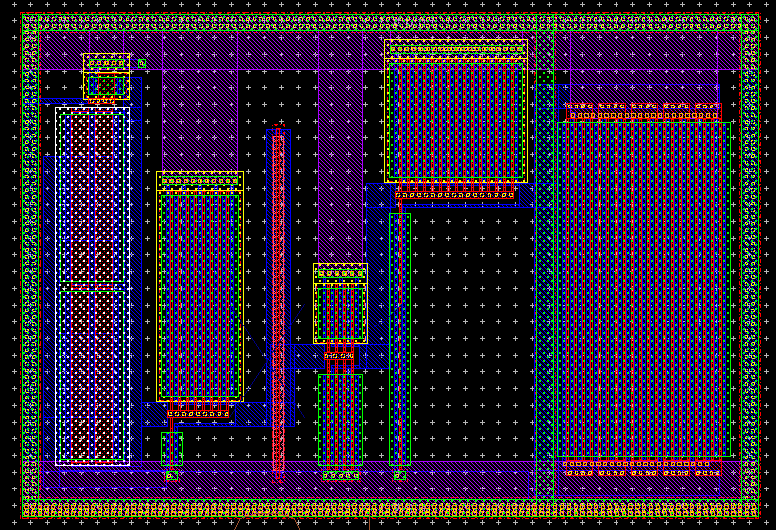
1. darlington\_clamp



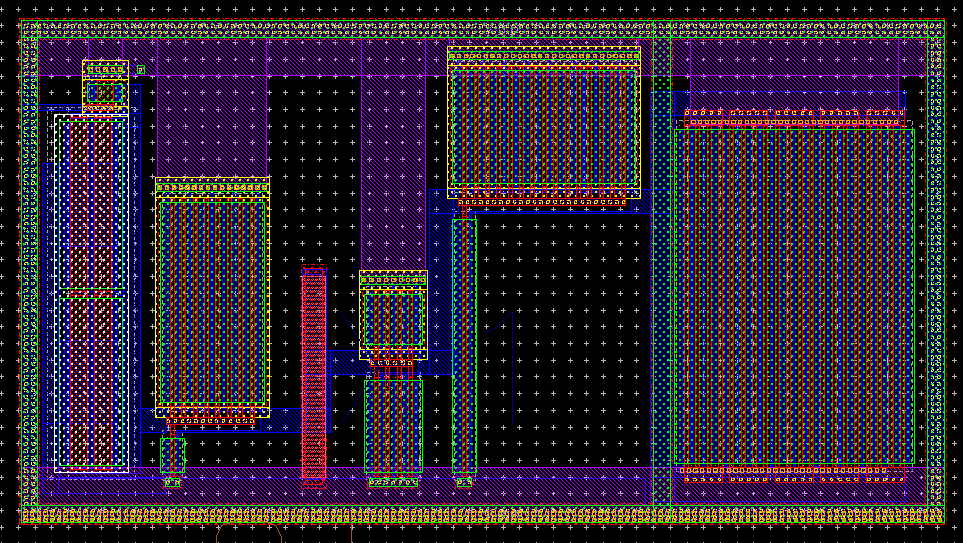
1. double\_diode\_n



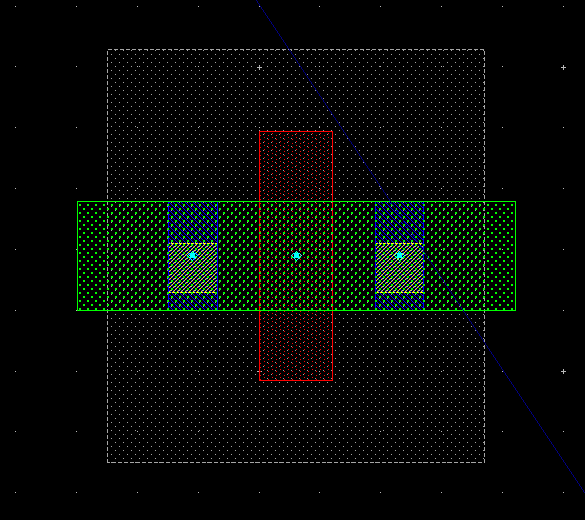
1. rc\_clamp



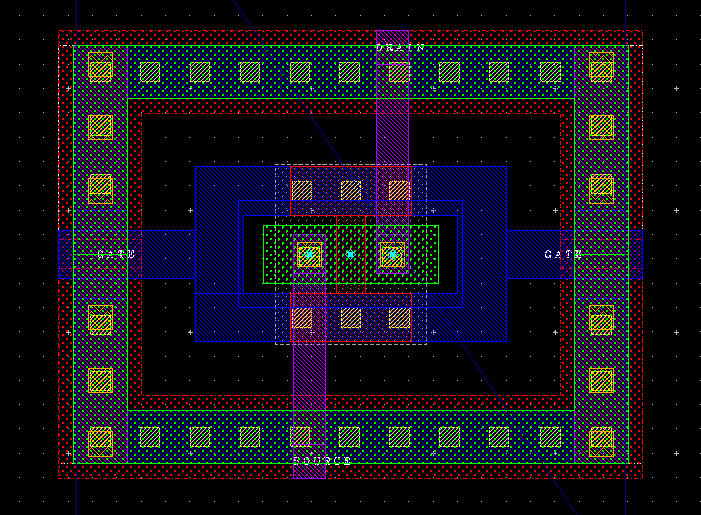
1. rc\_clamp25



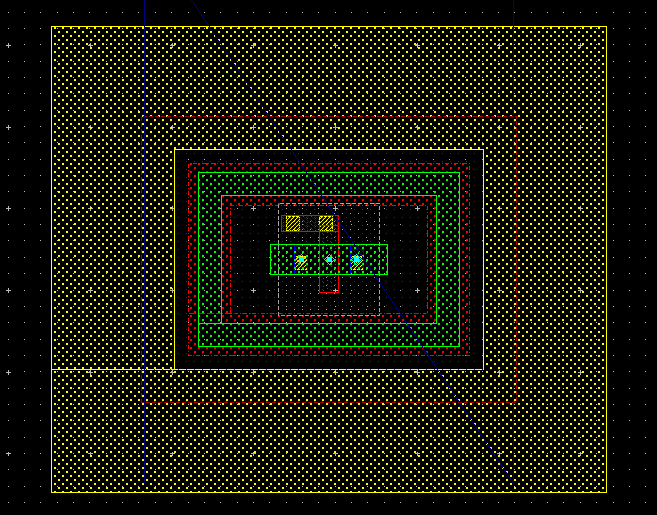
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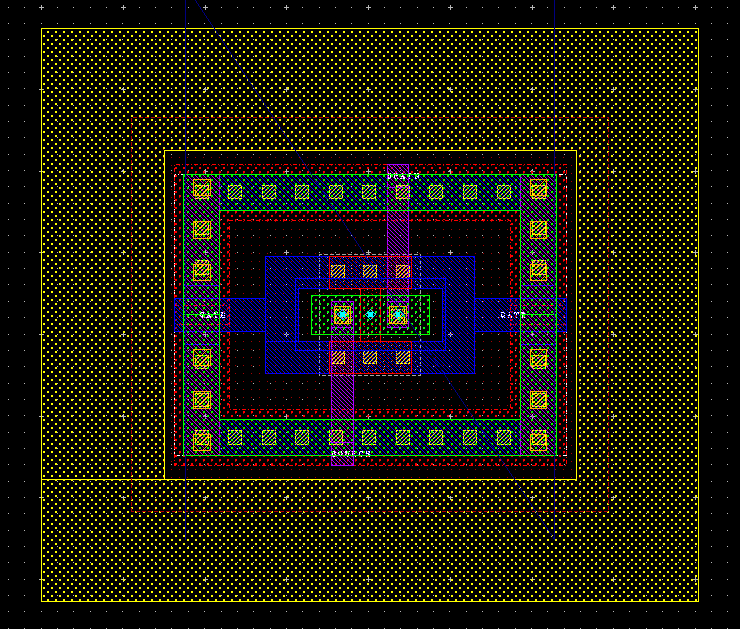
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2. dgnfet\_rf



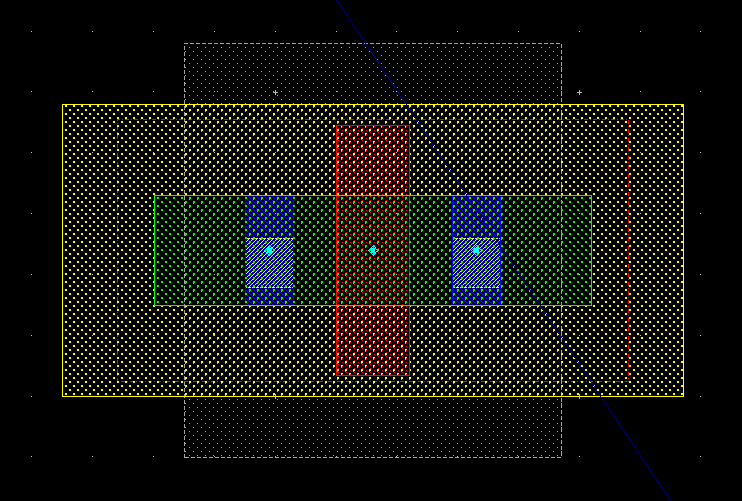
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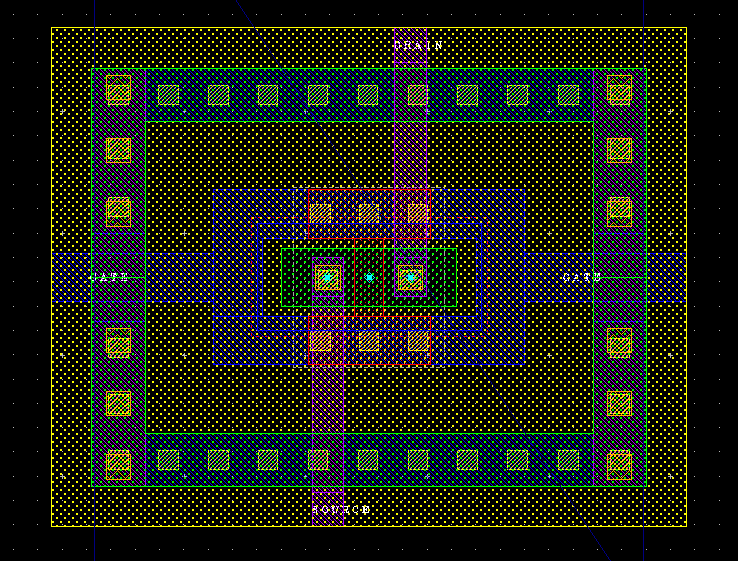
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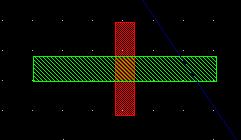
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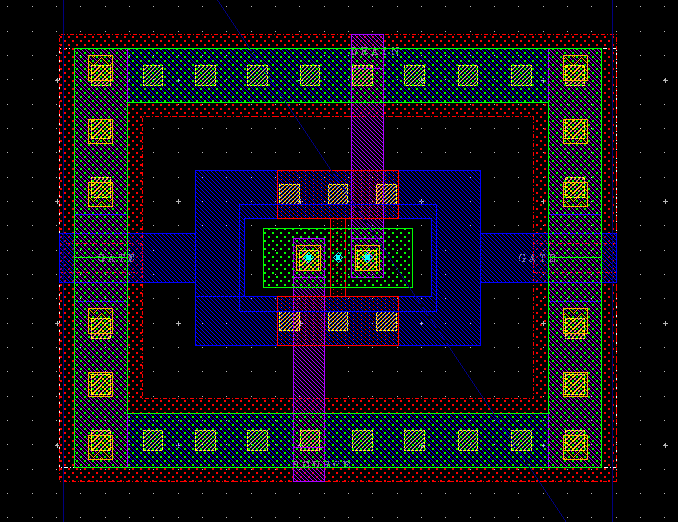
1. dgpfet\_inh
2. dgpfet\_rf



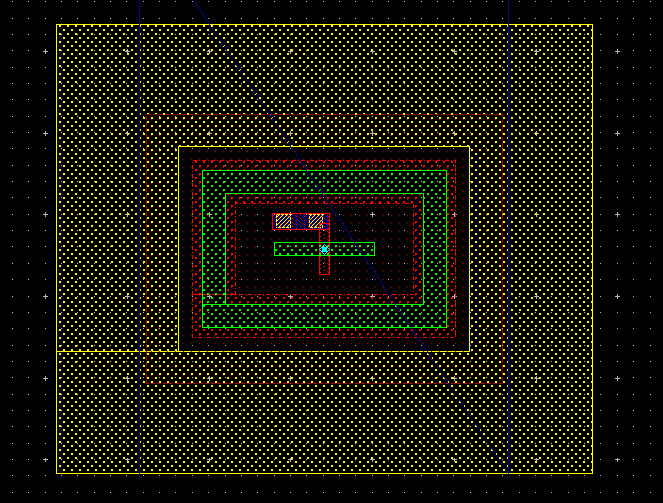
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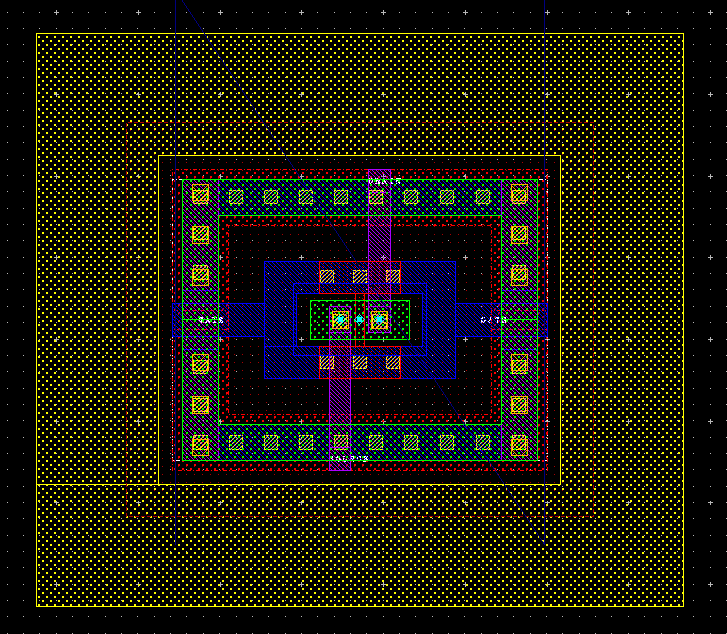
1. nfet\_inh
2. nfet\_rf



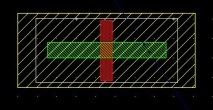
1. nfettw



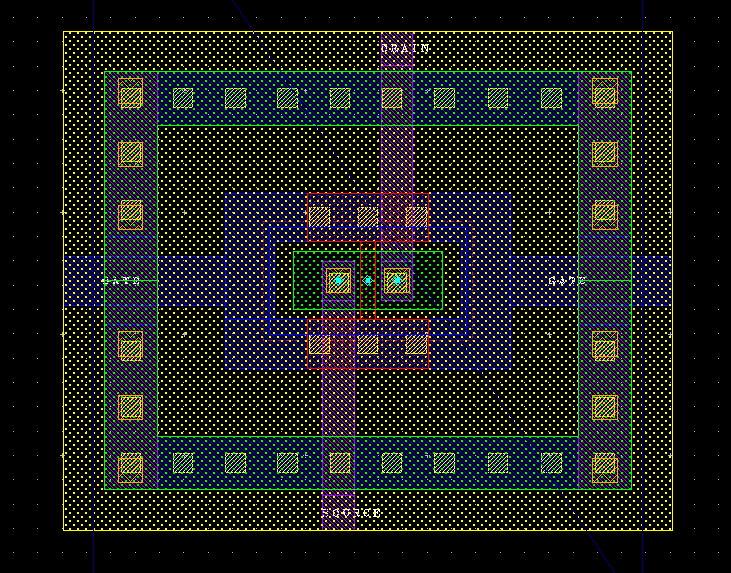
1. nfettw\_rf



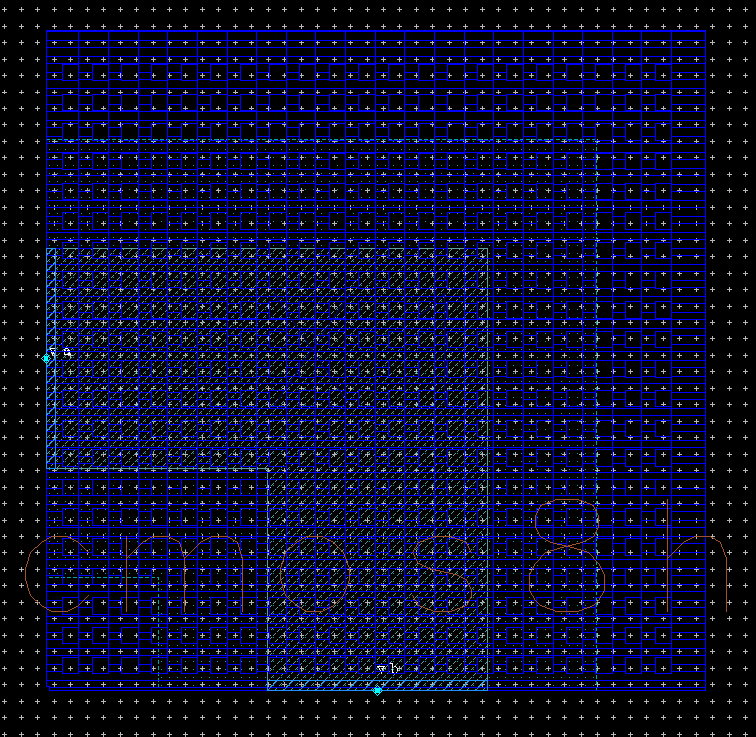
1. pfet



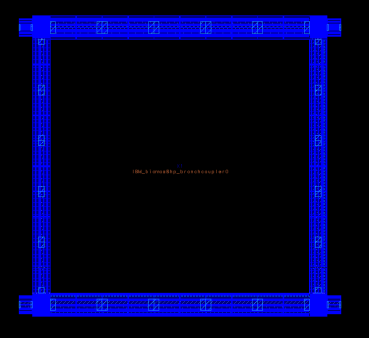
1. pfet\_inh
2. pfet\_rf



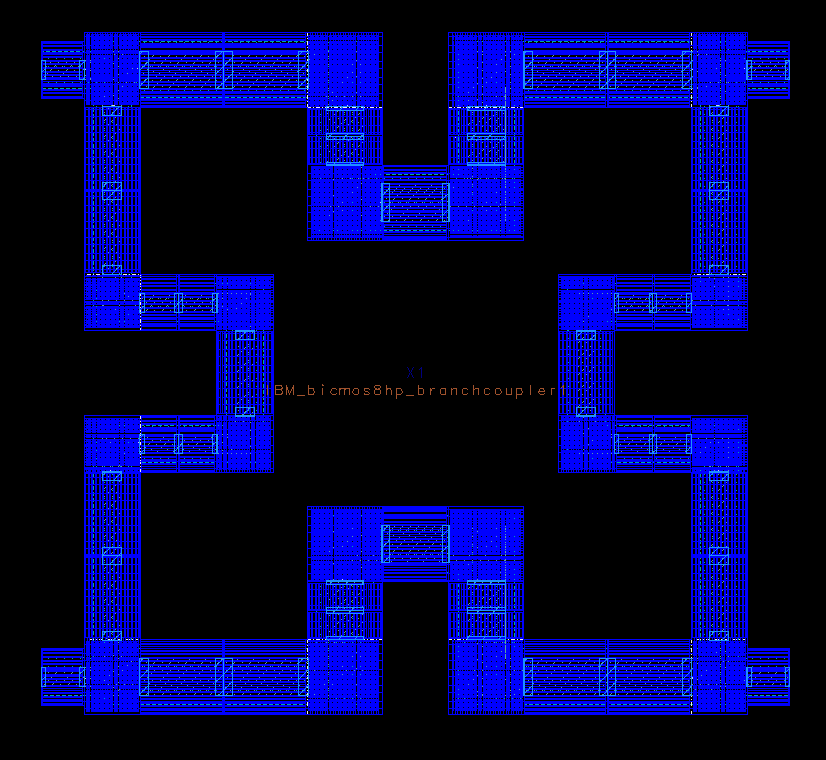
1. bend



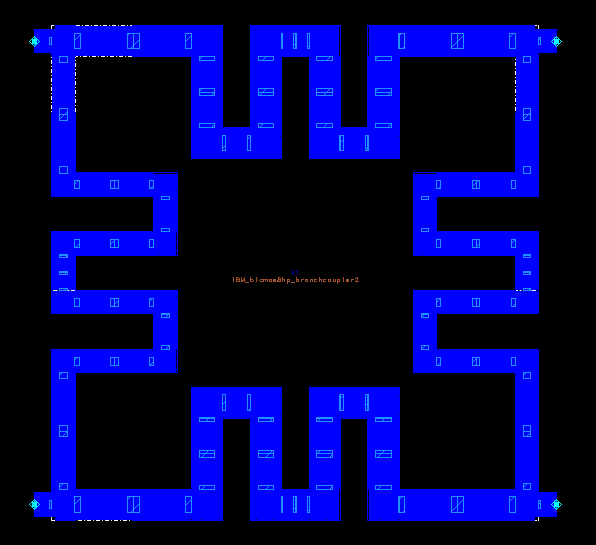
1. branchcoupler0



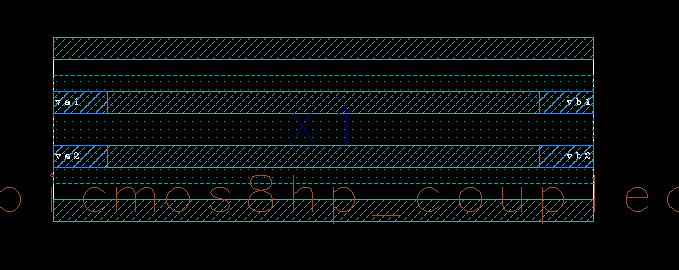
1. branchcoupler1



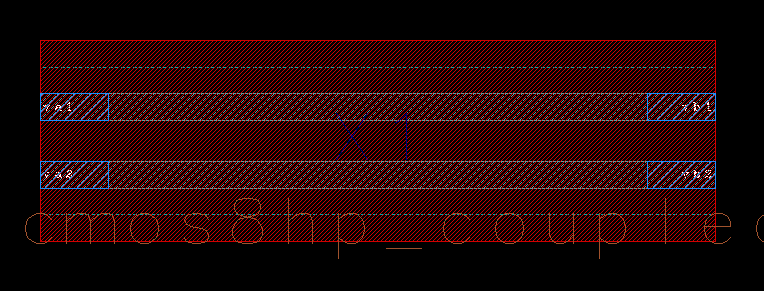
1. branchcoupler2



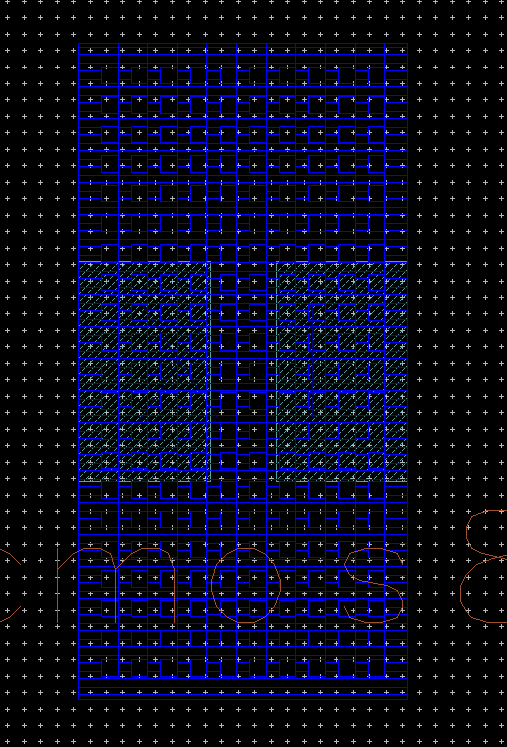
1. coupledcpw



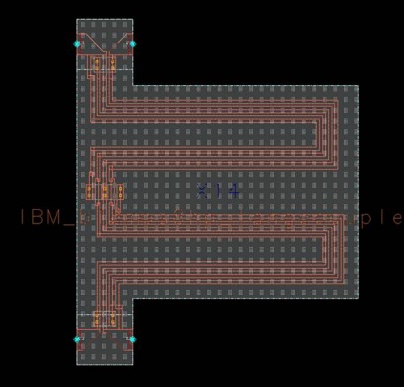
1. coupledwires



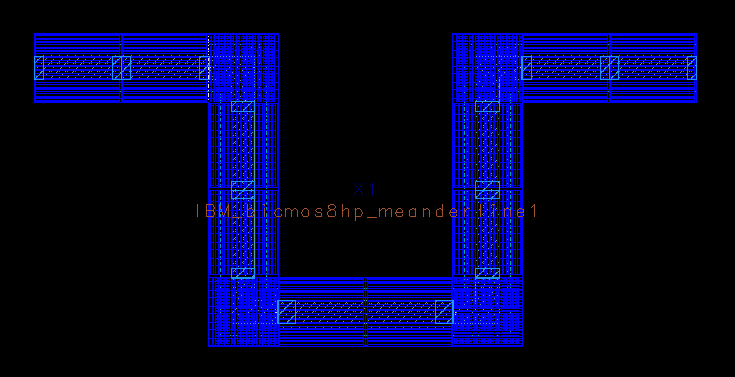
1. gap



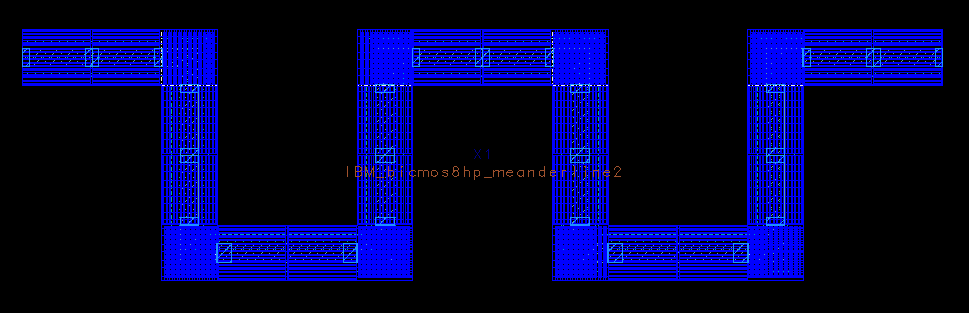
1. langecoupler



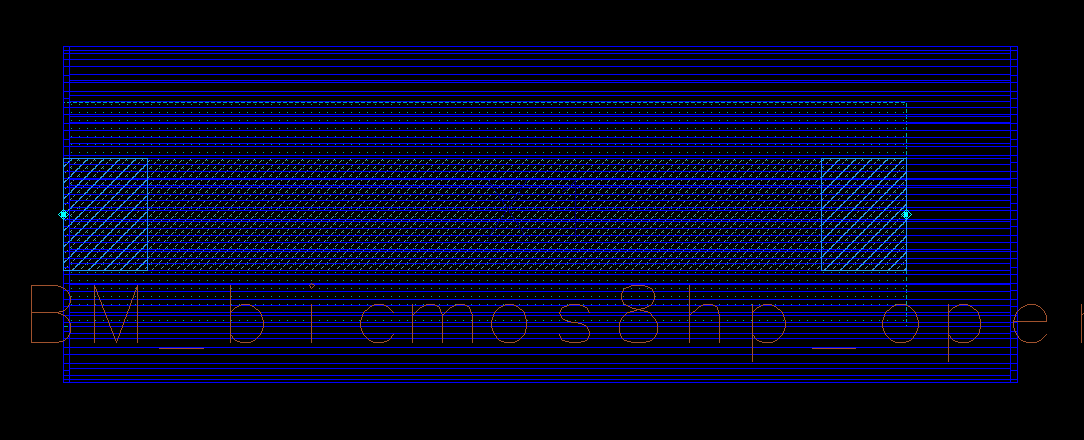
1. meanderline1



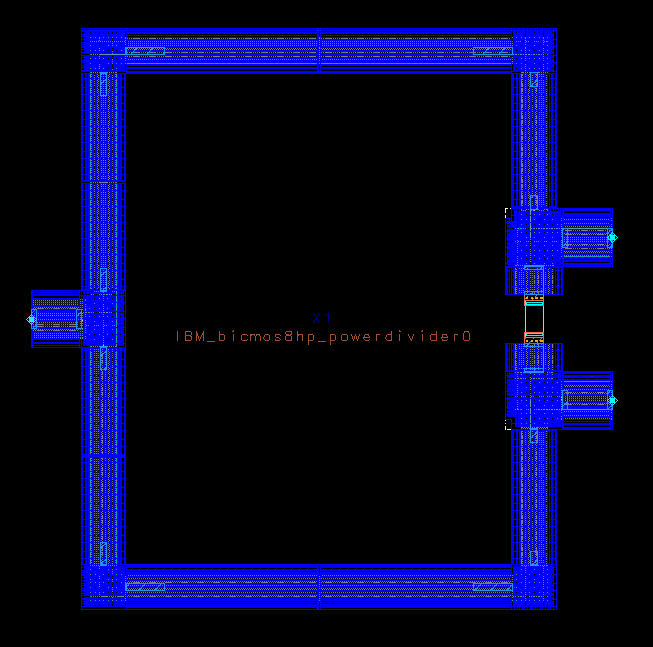
1. meanderline2



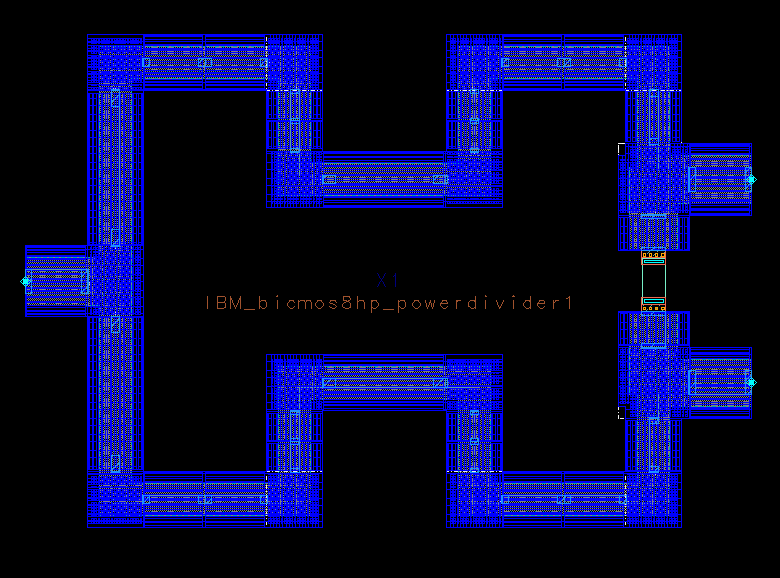
1. open



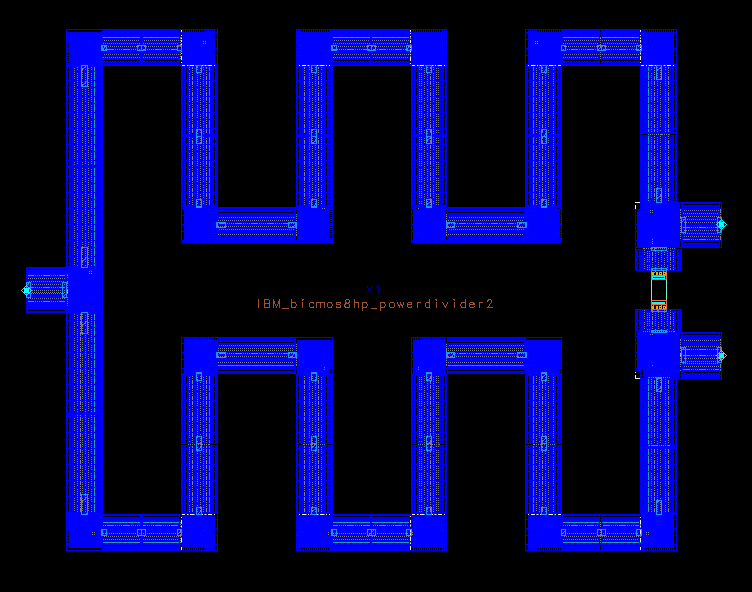
1. powerdivider0



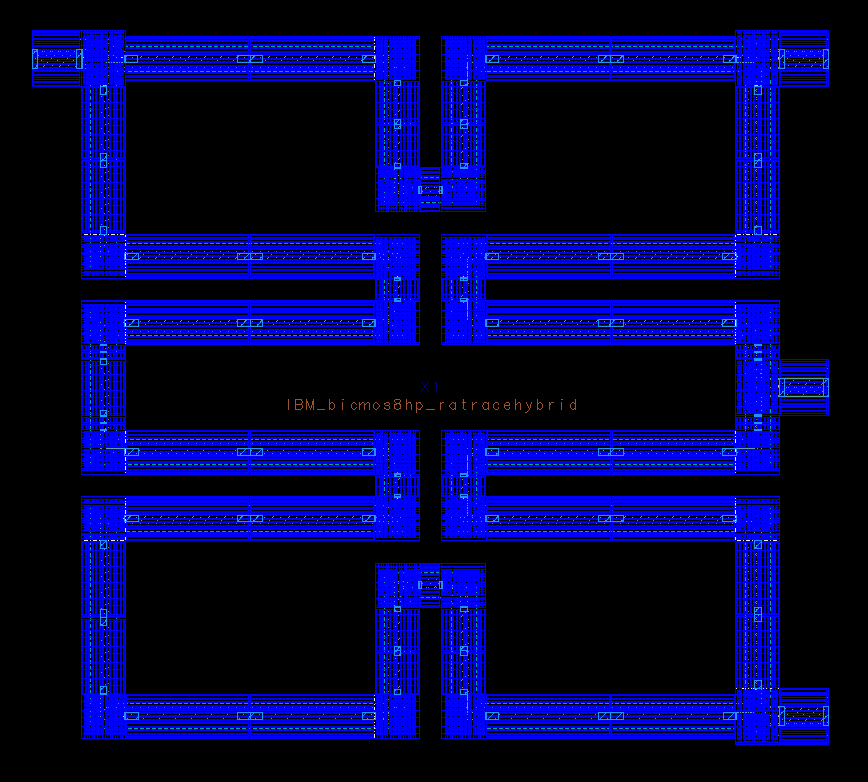
1. powerdivider1



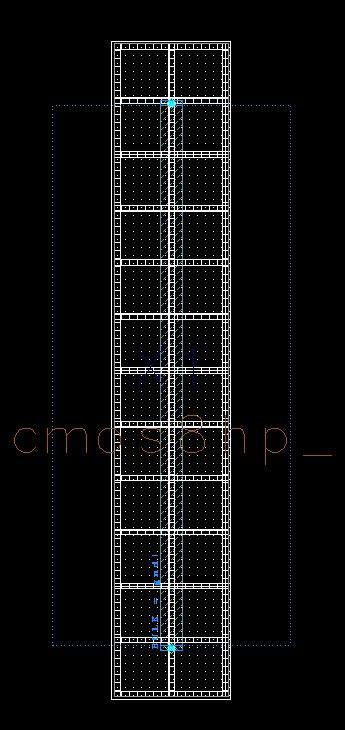
1. powerdivider2



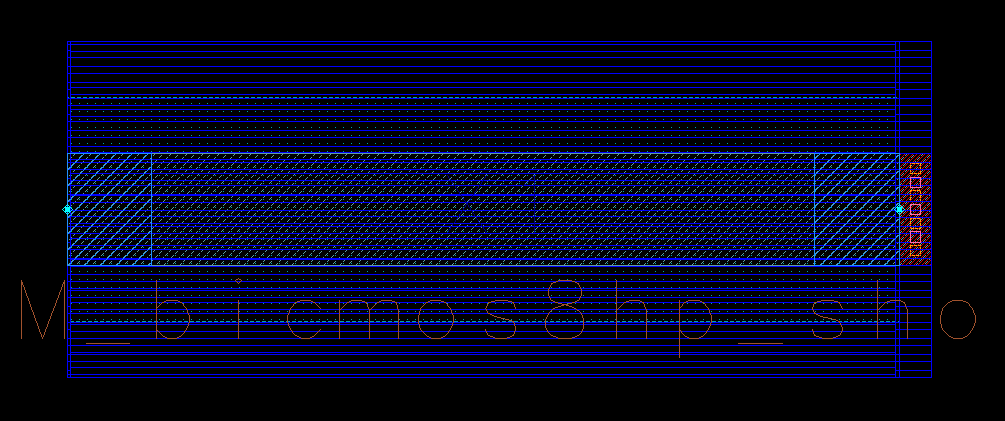
1. ratracehybrid



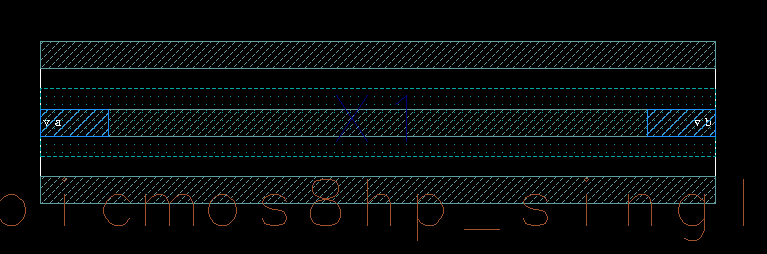
1. rfline



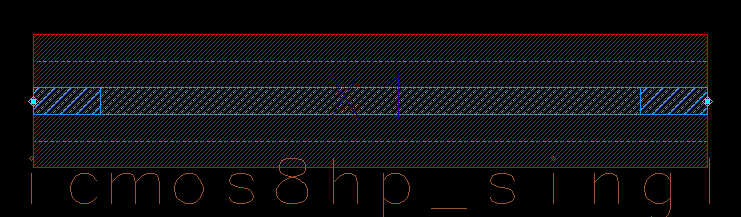
1. rfline\_inh
2. short



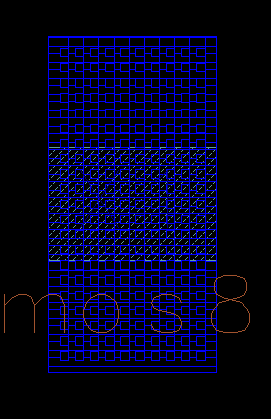
1. singlecpw



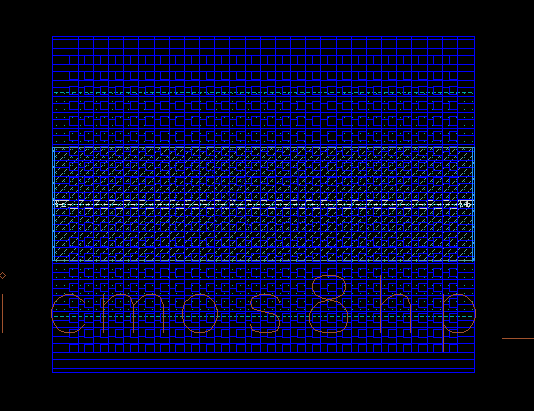
1. singlewire



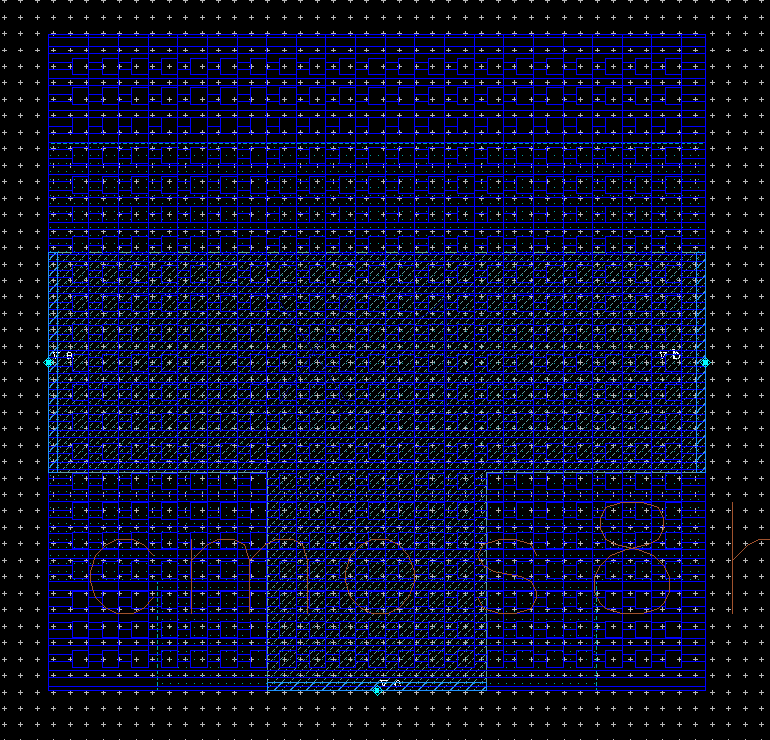
1. step



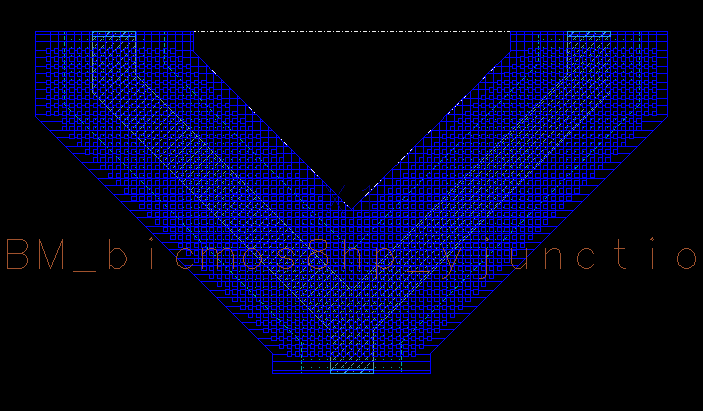
1. taper



1. tee



1. yjunction



# Known Issues(Layout)

Listed below are some known issues in the current version of the kit:

1. The ’45 degree’ mitre bend is not supported in the current version of the kit. However, this would be included in the next version.
2. The ‘low current’ marking layers are currently not provided
3. The ‘radialstub’ is not present in this iteration of the kit and will be available in the next iterations of the kit.
4. Some complex layouts, like the ‘langecoupler’, may take a while to instantiate.