
BiCMOS-8HP

Model Reference Guide

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V1.2.3.0HP (December 2011)

This edition of the BiCMOS-8HP Model Reference Guide applies to the V1.2.3.0HP version of the models.

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1.0 Model Reference Guide Introduction

The main purpose of this reference guide is to provide the designer with information on the BiCMOS-8HP models beyond that which is currently available in other documentation (see “Additional References” below).

1.1 Scope

This version of the guide contains the following types of information:

- A brief overview of the IBM BiCMOS modeling methodology.
- A description of the statistical process distributions and corner simulation methodology.
- Model-to-Hardware correlation plots. Be aware that these plots use the models before the process by which they are "centered" to match the design manual.
- Model features, limitations and/or restrictions.
- Possible differences between any of the supported simulators (e.g. HSPICE vs SPECTRE).
- Details on conditions used for device characterization or model extraction.

Note: Technology and device use conditions, such as maximum voltage or temperature limits, for all of the devices documented here are as specified in the BiCMOS-8HP Design Manual. Model verification and/or correlation plots may depict data beyond these limits to illustrate robust model behavior.

1.2 Additional References

Other modeling information can also be found in the following sources:

- Model syntax, input parameter options and basic topology diagrams are included as comment lines at the top of each individual model file.
- Device performance specifications, layout groundrules, use restrictions and some basic model equations are contained in the “Electrical Design Rules and Models” section of the BiCMOS-8HP Design Manual.

1.3 On-line Guide Viewing

This document has been created in PDF format to provide for easy hardcopy printing or on-line viewing. For on-line viewing, the guide has built-in Hyper Text links to each main document section as well as to all of the correlation plots. Clicking on any of the entries in the “Contents” list will bring up the page where that heading appears. For sections where there are multiple pages of plots, tables may be provided near the beginning of that section. Clicking on the figure numbers in the table cells will also link to the specified plot.

1.4 Model Overview

This section gives a brief overview of IBM's BiCMOS modeling methodology. IBM's BiCMOS models are physics-based, scalable compact models, in contrast to models based on fitting a discrete device. This allows the greatest amount of flexibility for designers and provides excellent model accuracy over a broad range of applications. Below is a brief description of this scalability concept followed by specific comments for each device in the design kit offering.

1.4.1 Scalability and Physics-Based Models

Scalable models provide circuit designers with an extra degree of freedom for circuit optimization compared to discrete elements or model library approaches. Also, using device physics allows the models to easily incorporate realistic statistics and process changes. Within the model files, a complete set of parameters for arbitrary device geometries is generated from a single set of technology specific electrical and process data. For this, each value of the required model elements is related to a function describing the dependence on the specific electrical data (such as capacitance per area, sheet resistivities), technology data (layout design rules), operating point and temperature. This type of physics-based model also allows us to leverage the large volumes of in-line test data and provides a realistic approach to statistical modeling.

Other important features:

1. The models match key process parameter control specifications
2. Electrical data is extracted using near-nominal process hardware
3. Statistical variation is measured using process split hardware

The electrical data comes from DC characterization (over voltage and temperature), AC characterization (S-parameters), characterization of bridge structures and current mirrors for device matching and CV characterization.

The electrical and technology parameters are contained in a "skew" file that allows process parameters shared between various devices to be included in one file. The model parameters are calculated from these process parameters and the device geometry. Finally, correlation is obtained among devices as a result of sharing common process parameters. The device models support Monte Carlo analysis since the skew file parameters are coded for both global and local mis-match. This gives the best predictions of what happens in the manufacturing line.

1.4.2 NPN Models

Layout information is combined with process information to generate models for arbitrary emitter lengths through the use of scaling equations. The model parameters are expressed semi-empirically in terms of independent process parameters through a set of device equations, allowing ready integration of the manufacturing line process monitor data into the device models.

This technology uses the VBIC model as the core device model. This model overcomes a number of long recognized deficiencies in the standard Gummel-Poon model (self-heating and impact ionization are built-in, parasitic PNP is included, quasi-saturation and Early effect treatments are improved and it is fully supported in multiple circuit simulators).

For further details on NPN model features and limitations, see Section 3.0 , "NPN Models" on page 48.

1.4.3 MOSFET Models

The MOSFET models are scalable, based on the standard PSP 103.1 model and include process-based statistics. Additional gate resistance, S/D diode, parasitic capacitance, wiring resistance and substrate resistance elements have been included to obtain better accuracy at high frequencies. For further details on the MOSFET model features and limitations, **see Section 5.0 , “MOSFET Models” on page 184.**

1.4.4 Passive Device Models

The models for passives and other devices (resistors, capacitors, varactors, inductors, and diodes) are also developed using the same physics-based principles as discussed above. These devices are generally modeled using distributed subcircuits to account for the effects of parasitics necessary for accurate high frequency modeling.

1.4.5 Design Application Caution

All of the device models are extracted with some emphasis on the expected range of operation for device characteristics of general interest. There may be specific design applications that are sensitive to regions where the model has not been fully characterized or optimized. Please review the range of bias conditions, device geometries and characteristics shown in this guide to ensure that the model accuracy demonstrated will cover the design of interest. Please contact your IBM Foundry Application engineering team with any questions or concerns in this regard.

1.4.6 Substrate Resistance Modeling

Most of the device models have substrate as one of the terminals. This terminal is usually connected to ground through substrate contacts in most applications. There can be a significant amount of resistance between the substrate terminal of the device and the substrate contact itself. This resistance depends on the size and shape of the device and the substrate contact, the distance between them, whether there are other devices between the device and the substrate contact, etc. Since this resistance is very dependent on the layout of the circuit, the models provide only an estimate of substrate resistance that may be off substantially.

Models based on the MOSFET RF pcells that contain well defined substrate contacts avoid this problem by providing the circuit designer the opportunity to use the same layout as used in the modeling. The use of these pcell-based models in conjunction with the RF pcells for layout will give the greatest accuracy. The effect of the substrate resistance depends upon the device and the characteristics being looked at. The high frequency MOSFET model to hardware plots in this guide were generated using the RF pcell layouts.

For many of the other devices, an instance parameter "rsx" is provided. This parameter defaults to a value of 50 ohms and can be overridden by the designer just like other model input parameters. The model to hardware plots in this guide were generated using empirical estimates of the substrate resistance for the layout of the test structures.

1.4.7 Multiplicity and Mis-match

For any of the models which incorporate the prediction of device mis-match (e.g. resistors, MOSFETs), there is an instance parameter ("par") which is netlisted and set equal to the value of the implicit multiplicity parameter ("m"). This explicit parameter is used by the calculations within the model subcircuit code so that the mis-match properly accounts for cases where multiplicity is used, e.g. $m(\text{par}) > 1$.

1.4.8 Double-Counted Parasitic Metal Capacitance

When making high frequency measurements on individual devices, we de-embed the metal parasitic capacitance, resistance, and inductance that is not part of the device itself. After de-embedding, the resultant data represents our best knowledge of the device, and is used to fit the parameters of our scalable models.

All metal parasitic effects within the Pcell boundary of a device, however, cannot be perfectly de-embedded from the measured data due to the constraints of open and short calibration structure design and test methods. Consequently, the model could include a very small amount of Pcell metal parasitic capacitance. This parasitic would be inherent in the model fit and not an explicit capacitance between the metal terminals of the Pcell. The quality of our model-to-hardware correlation results supports the use of this approach.

When the parasitic capacitance of a circuit layout is extracted for final simulation, the M1-to-substrate capacitance within the Pcell instance boundary is blocked, but the capacitance between the metal terminals of the Pcell instance is not. Because this is already part of the model fit, this inter-electrode capacitance could be, in effect, double-counted.

To a first order approximation, the error is between 0.050 fF/um and 0.055 fF/um for typical base-to-collector metal lines in the BiCMOS-8HP npn (a percent or so of junction capacitance). Also note that there are two collectors per Pcell in BiCMOS-8HP which doubles the error. An error of this magnitude is typically not a concern for a single instantiation of a device. Designers that use large arrays of devices in a design -- for instance, an array of npns in a power amplifier or an array of varactors in a VCO -- may wish to take this effect into consideration.

1.5 General Model Notes

Additional information and details on the setup of the simulation environment can be found in the CDS design kit User's Guide.

Reference Temperature

The nominal (or reference) temperature for all of the device models is 25degC. The simulator options must be consistent with this definition.

For HSPICE, the following entry should appear as a part of the ".option" line in the netlist:

```
.option tnom=25
```

For Spectre, the following line can be included in the environment file (.cdsenv):

```
spectre.opts tnom string "25.0"
```

Geometric Units

Device dimensions for all of the model files are in meters. To specify typical device geometries (in microns), the proper unit suffix or exponent must be included, e.g. w=0.5u or w=0.5e-6.

1.5.1 HSPICE Simulation Setup

The HSPICE model directory contains example setup files:

design.inc	File to specify all global switch and process corner parameter overrides.
allModels.inc	File to specify all model include statements to support nominal, fixed process corner and Monte Carlo simulation analysis options.

The syntax for inclusion of the models using these files is:

```
.inc '<PDK model directory path>/design.inc'
.lib '<PDK model directory path>/allModels.inc' XX
```

where XX represents one of these analysis options:

tt	Nominal process (typical mean corner) and Monte Carlo
fff	Fixed MOSFET process corner: Functional Fast NMOS, Fast PMOS
ssf	Fixed MOSFET process corner: Functional Slow NMOS, Slow PMOS
fs	Fixed MOSFET process corner: Fast NMOS, Slow PMOS
sf	Fixed MOSFET process corner: Slow NMOS, Fast PMOS
ff	Fixed MOSFET process corner: Fast NMOS, Fast PMOS
ss	Fixed MOSFET process corner: Slow NMOS, Slow PMOS

If a custom "design.inc" file is to be used and is located outside of the intalled model directory, the directory path for the file must be specified explicitly.

1.5.2 Spectre Simulation Setup

The Spectre Direct simulation environment requires the input of the following files which are located in the Spectre model directory path:

design.scs	File to specify all global switch and process corner parameter overrides.
allModels.scs	File to specify all model include statements to support nominal, fixed process corner and Monte Carlo simulation analysis options.

The syntax for inclusion of the models using these files is:

```
include "<PDK model directory path>/design.scs"
```

```
include "<PDK model directory path>/allModels.scs" section=XX
```

where XX represents one of these analysis options:

tt	Nominal process (typical mean corner) and Monte Carlo
fff	Fixed MOSFET process corner: Functional Fast NMOS, Fast PMOS
ssf	Fixed MOSFET process corner: Functional Slow NMOS, Slow PMOS
fs	Fixed MOSFET process corner: Fast NMOS, Slow PMOS
sf	Fixed MOSFET process corner: Slow NMOS, Fast PMOS
ff	Fixed MOSFET process corner: Fast NMOS, Fast PMOS
ss	Fixed MOSFET process corner: Slow NMOS, Slow PMOS

If a custom "design.scs" file is to be used and is located outside of the installed model directory, the directory path for the file must be specified explicitly.

2.0 The Process Model

Ideally every device built in a given technology would vary from any other device of the same type in a purely deterministic way due to device parameters chosen by the circuit designer. In reality, every wafer lot that is manufactured differs in many random ways from the ideal “nominal process”. In addition, different wafers within a lot and chips at different locations on the same wafer experience slightly different process conditions. These variations are referred to as **chip mean variations**.

There are also factors, both systematic and random, that cause individual devices within a chip to vary from the chip mean of that chip. This instance specific variation includes geometric **across chip variation** (acv) and **mis-match** due to doping and film thickness fluctuations. Instance specific variation is modeled in the skew file and in the include files (*.inc) in HSPICE, and through the mis-match keyword in the Spectre process.scs file.

By default, a single run will simulate every device in the circuit as if it were perfectly nominal and a Monte Carlo run will apply a randomly selected chip mean variation to each device parameter for which a distribution is supplied in the skew file. In addition, each instance of a given device type will receive a random across chip variation for each parameter for which across chip variation is supplied in the skew file. Physically, some of these variations are correlated between different device types and between different instances of the same device type. This physical correlation is captured in the models and is used in calculating skewed parameters during Monte Carlo runs.

2.1 Process Model User Controls

The process model supports two basic approaches to simulating process variation; Monte Carlo and process corner simulation. It also allows certain specific hybridizations of these two approaches for the FET devices. A standard Monte Carlo simulation with all of the variations turned on is the most accurate representation of process variation available from the model. However, statistical simulations require a lot of CPU time which is not always feasible for large circuits or complete libraries of many small circuits. A less CPU intensive method is to skew the process to a set of particular corners and run a single simulation at each selected corner. In general, it is recommended that Monte Carlo analysis be used with a representative set of small circuits to select specific corners to be used for the bulk of the design work.

There are a number of switches which the user can specify to control which sources of device variation are included and how they are calculated. The first table (Table 1) lists each process model switch with a brief statement of the effect of each possible setting. The next table (Table 2) gives a brief listing of the function of the various process model parameters. User controls are contained in the design.inc file (HSPICE) and the design.scs file (Spectre). These files are to be copied and edited for simulation with non-default settings.

Note: The IBM PDK does not support the Cadence Monte-Carlo form based “Process Only” or “Mismatch Analysis Only” variation options. For all Monte-Carlo simulations, the “Process and Mismatch” option should be selected. Separate fet_*_mis switches (described below) allow the user to turn the MOSFET mis-match on/off instead.

Table 1. Process Model Switches

Switch	Function	Default
mc_global	= 1 for Monte Carlo variation of chip mean parameters = 0 for FET chip mean parameters set by corner parameters = 2 for FET chip mean and across chip variation moving together	1
fet_dop_mis	= 1 to enable FET V_t and mobility variation due to dopant mis-match = 0 to disable this effect	1
fet_geo_mis	= 1 to enable FET variation due to across chip variation in delta L and delta W. = 0 to disable this effect	1
gstis	STI Stress effect switch. Calculations use instance parameters (sa, sb, sd). = 2 to enable FET STI stress effect for all devices = 0 to disable this effect for all devices = 1 effect enabled based on local instance switch setting (Istis) for each device	2
gwells	NWell proximity switch. Calculations use instance parameters (panw1-panw10). = 2 to enable FET NW proximity effect for all devices = 0 to disable this effect for all devices = 1 effect enabled based on local instance switch setting (Inws) for each device	2
gii	NPN and VPNP impact ionization switch. = 2 Impact ionization enabled for all NPN and VPNP devices = 0 to disable this effect for all NPNs and VPNP = 1 effect enabled based on local instance switch setting (ii) for each device	2

Table 1. Process Model Switches

Switch	Function	Default
gsh	NPN and VPNP self-heating effect switch. = 2 Self-heating enabled for all NPNs and VPNPs = 0 to disable this effect for all NPNs and VPNPs = 1 effect enabled based on local instance switch setting (sh) for affected devices	2
gbv (Spectre only)	MOSFET and NPN breakdown warning checks. = 2 to enable breakdown warning checks for all MOSFET and NPN devices = 0 to disable these checks = 1 NPN (only) check enabled based on instance switch (bv) for each device	2
pc_nest	= 1 to enable FET length variation due to nesting. = 0 to disable this effect = 2 if the user is supplying a magnitude for nested to isolated variation to be used for all FETs in the simulation (pc_nest_add).	1
pc_orient	= 1 to enable FET length variation due to gate orientaion = 0 to disable this effect = 2 if the user is supplying a magnitude for vertical to horizontal variation to be used for all FETs in the simulation (pc_orient_add).	1
pc_dist	= 1 to enable additional FET length variation for spaced more than 200 um apart. = 0 to disable this effect = 2 if the user is supplying a magnitude for near to far variation to be used for all FETs in the simulation (pc_dist_add).	1
rx_dist	= 1 to enable additional width variation for FETs spaced more than 100 um apart. = 0 to disable this effect = 2 if the user is supplying a magnitude for near to far variation to be used for all FETs in the simulation (rx_dist_add).	1

Table 2. Process Model Parameters

Parameter	Function	Default
cor_npn	Skews device type specific process parameters for the NPNs	0
cor_pnp	Skews device type specific process parameters for the VPNP	0
cor_nmos	Skews device type specific process parameters of N-type FETs	0
cor_pmos	Skews device type specific process parameters of P-type FETs	0
cor_noin	Skews flicker (1/f) noise for N-type FETs	0
cor_noip	Skews flicker (1/f) noise for P-type FETs	0
cor_res	Skews resistance parameters of passive devices	0
cor_cap	Skews capacitance parameters of passive devices	0
cor_tox	Skews tox for all thin oxide devices	0
cor_toxd	Skews tox for all thick oxide devices	0

Table 2. Process Model Parameters

Parameter	Function	Default
cor_pc	Skews chip mean delta L for all FETs	0
cor_rx	Skews chip mean delta W for all FETs	0
cor_ind	Skews inductance of inductors	0
pc_nest_add	Specifies the difference in delta L between FETs with instance parameter plnest=0 and those with plnest=1	0 (m)
pc_orient_add	Specifies the difference in delta L between FETs with instance parameter plorient=0 and those with plorient=1	0 (m)
pc_dist_add	Specifies the difference in delta L between FETs with instance parameter pld200=0 and those with pld200=1	0 (m)
rx_dist_add	Specifies the difference in delta L between FETs with instance parameter pwd100=0 and those with pwd100=1	0 (m)
vcepd (Spectre only)	Specifies C-E voltage limit used in breakdown check for HP NPNs.	2.0 (V)
vcehb (Spectre only)	Specifies C-E voltage limit used in breakdown check for HB NPNs.	4.75 (V)
fwdlim (Spectre only)	Specifies voltage limit used in the forward-bias check of S/D junctions.	0 (V)

Note: These parameters are real valued and can take values from a continuum of values. It is the user's responsibility to ensure that the values specified are physically reasonable.

Some model parameters, such as delta L ($2 \cdot \text{lint}$), have process variation from more than one source. During Monte Carlo simulation these sources vary independently and when the various effects are summed the resulting total variation is the root mean sum of the individual variations. When these distributions are controlled by corner parameters, the individual contributions move together and summing would produce an excessive total distribution.

User-Defined Corner Parameter Notes

The following applies to the use of the corner parameters in the design input file:

- These parameters are real valued and can take values from a continuum of values. It is the user's responsibility to ensure that the values specified are physically reasonable.
- The MOSFET-related parameter (cor_tox^* , cor_pc , cor_rx , cor_nmos , cor_pmos) values in the design input file will be ignored whenever a fixed corner, other than the nominal process (tt), is selected. The parameter settings from these pre-defined MOSFET fixed corners will take precedence over any values in the design input file. The user input parameters can be set when using the nominal process (tt) corner.
- The MOSFET 1/f noise, bipolar, resistor, capacitor and inductor corner parameters in the design input file can be used in conjunction with the MOSFET fixed corners.

2.1.1 FET Specific User Control Notes

By default, all process variations are turned on and all correlations specified in the design manual are included for Monte Carlo runs. This provides the most complete and accurate description of the process variation available from the model and is obtained by setting `mc_global=1`. In some cases it may be of interest to examine events which have a less than 3 sigma probability of occurrence (3 out of 1000). The reason for this may be needed if a chip has 1000 copies of a circuit, as the circuit on every chip can be expected to have a three sigma fast and another 3 sigma slow ACLV. In order to see the behavior of the 3 sigma fast circuit on the 3 sigma fast chip approximately 1 million Monte Carlo cases of that circuit would need to be run.

The skew/process file provides two ways to estimate the 3 sigma circuit on the 3 sigma chip with fewer simulations. One method is to set `mc_global=0`. The chip mean variation can then be set to a 3 sigma condition by setting the appropriate corner parameters. The other method is to set `mc_global=2`. In this case, the across chip variations are not independent but are set to the same fraction of their maximum value along with the corresponding chip mean variations. In this way, a 3 sigma chip / 3 sigma circuit simulation is expected 3 times out of 1000 rather than a few times out of a million.

ACLV variation comes from a number of sources, some of which are under the control of the circuit designer. For example, delta L variation can be reduced during layout by having all FETs oriented so that current flows along the same axis (i.e. all vertical or all horizontal). Two mechanisms are provided to help the circuit designer estimate the magnitude of these effects. Switches are provided to turn these effects on or off. First, switches are provided to individually turn these effects on and off as listed in Table 1. When one or more of these switches is set to zero, the corresponding effect is set to zero **and** the total variation is reduced.

A second method is to specify on the device instance call in the netlist the layout information for that FET with respect to that effect. The FET subcircuits accept 4 instance parameters for layout dependent FET variation. For each effect, the instance parameters divide all FETs on the chip into two groups. The skew file picks an independent random number for each of these groups which is used for all members of that group. In this way, FETs with the same value are more similar to one another than are two FETs, one from each group. However, total L variation is the same for all FETs and equal to the variation specified in the design manual.

If one of these instance parameters is not specified, or is specified as a -1, during Monte Carlo it is randomly assigned to one or the other of the groups. This gives an estimate of the possible impact of these effects on circuits where these variables are not controlled during layout.

plnest: This specifies whether an FET is surrounded by space empty of PC shapes (`plnest=0`) or by many other FETs (or dummy poly shapes) (`plnest=1`).

plorient: This specifies whether an FET gate is oriented horizontally (`plorient=0`) or vertically (`plorient=1`).

pld200: This divides all FETs in the netlist into two groups, those that are within a 200 by 200 μm square on the chip (`pld200=0`) and those that are outside that square (`pld200=1`).

pwd100: This divides all FETs in the netlist into two groups, those that are within a 100 by 100 μm square on the chip (`pwd100=0`) and those that are outside that square (`pwd100=1`).

The process switches (shown in Table 1) for one or more of these effects can also be set to 2, meaning the magnitude of this effect is being supplied by the user. This is useful for model to hardware correlation. For example if it is known that nested FETs are longer than isolated FETs by a 4nm, that information can be incorporated into the simulation by setting `pc_nest=2` and `pc_nest_add=-4e-9`. The skew file will make all nested FETs 2nm longer than they would otherwise be and all isolated FET 2nm shorter than they would otherwise be.

2.2 Process Parameter Description

The process (skew) parameter files in the model directory contain the parameters with distributions and the variation of those parameters. Many process parameters are varied in Monte Carlo simulations. A subset of these parameters are varied in corner simulations. The following tables contain a general description of the parameters controlled by corner parameters, grouped by device type.

The UP column shows the direction that the indicated distribution is varied in order to get to an "UP" value for the following device characteristics:

- NPNs, VPNNs, and MOSFETs: High current / high speed
- Resistors: High resistance
- MIM, HA varactor, and nMOS varactors: High capacitance
- MIM, inductor, transmission lines, and RFlne: High quality factor

Most of the process parameters (with the exception of Lint, Wint, tox and vth0) are independent in Monte Carlo simulations. Multiple parameters are controlled by one of the corner parameters in corner runs. The CORNER column in these tables indicates the direction the corner parameter moves to achieve the "UP" condition described above.

In Monte Carlo mode, each oxide thickness is controlled by its own distribution which effects all devices with that same thickness. For example, the tox for an nfet and an lppfet would move together but the tox for a dgnfet would move independently of these two. For chip mean wint (one half of delta W), all devices share the same distribution. The magnitude of delta W variation is not the same for all FET types so the wint is scaled with each FET type moving by the same fraction of its chip mean tolerance in a give Monte Carlo run.

Note that the "UP" column indicates the direction the distribution parameter moves to achieve the "UP" condition noted above. For example, the NFET threshold voltage and capacitances are reduced with positive cor_nmos, for the high speed corner. The NFET mobility, however, increases with positive cor_nmos.

Table 3. NPN Process Distributions

Parameter**	Description	UP	CORNER
exwx exlx	EX image bias Effective emitter width, length	+	+ cor_npn
rxwx rxlx	RX image bias Effective base width, length	+	+ cor_rx
nrea	Emitter resistance	+	+ cor_npn
nrdb<npn>	Pinch Rs (intrinsic Rb), Forward collector current	+	+ cor_npn
nrbl<npn>	Extrinsic base resistance	+	+ cor_npn
prsi	Silicided base poly Rs	-	+ cor_npn
nrnr<npn>	Extrinsic collector resistance	-	+ cor_npn
nbnsr<npn>		-	+ cor_npn
nvpd<npn>	Intrinsic collector resistance	-	+ cor_npn
nisa<npn> nisp<npn>	Forward collector current (area, perimeter)	+	+ cor_npn
nibeia<npn> nibeip<npn>	Forward base current (area, perimeter)	-	+ cor_npn
nvef<npn> nver<npn>	Early and reverse Early voltages	-	+ cor_npn
navc<npn>	Weak avalanche voltage parameter	-	+ cor_npn
ntf<npn>	Base transit time	-	+ cor_npn
ncjea<npn> ncjep<npn>	E-B junction capacitance (area, perimeter)	-	+ cor_npn
cnpba, cnpbp	E-B overlap capacitance (area, perimeter)	-	+ cor_npn
ncjcua<npn> ncjcup<npn>	Intrinsic C-B capacitance (area, perimeter)	-	+ cor_npn
ncjcx<npn> ncjcp<npn>	Extrinsic C-B capacitance (area, perimeter)	-	+ cor_npn
oppcdwn<npn> oppcfrng<npn>	B-C overlap capacitance (area, perimeter)	-	+ cor_ind
ncjsa, ncjsp	C-S junction capacitance (area, perimeter)	-	+ cor_npn

** <npn> refers to the device type, e.g. "hb" represents the High-Breakdown NPN.

Table 4. VPNP Process Distributions

Parameter	Description	UP	CORNER
evwx, evlx	EV image bias Effective emitter width, length	+	+ cor_pnp
rxwx rxlx	RX image bias Effective base width, length	+	+ cor_rx
vprea vprea8	Emitter resistance (0.4 μ m width) Emitter resistance (0.8 μ m width)	+	+ cor_pnp
vprdb	Pinch Rs (intrinsic Rb), Forward collector current	+	+ cor_pnp
vprbi	Extrinsic base resistance	+	+ cor_pnp
prsi	Silicided base poly Rs	-	+ cor_npn
vpozr	Extrinsic collector resistance	-	+ cor_pnp
vprcv		-	+ cor_pnp
vpisa, vpisp	Forward collector current (area, perimeter)	+	+ cor_pnp
vpibei	Forward base current	-	+ cor_pnp
vpvef vpver	Early and reverse Early voltages	-	+ cor_pnp
vpavc2	Weak avalanche voltage parameter	-	+ cor_pnp
vptf	Base transit time	-	+ cor_pnp
vpcjea, vpcjep	E-B junction capacitance (area, perimeter)	-	+ cor_pnp
vcppb	E-B overlap capacitance	-	+ cor_pnp
vpcjc	Intrinsic C-B capacitance	-	+ cor_pnp
vpcjcp, vpcjcx vpcjcl	Extrinsic C-B capacitance (area, perimeter)	-	+ cor_pnp
vpcbco, vpcbcp	B-C overlap capacitance (area, perimeter)	-	+ cor_pnp
vpcia, vpcip	C-PI junction capacitance (area, perimeter)	-	+ cor_pnp

Table 5. *n-channel MOSFETs (nfet, nfettw, dgnfet, dgnfettw) Process Distributions*

Parameter**	Description	UP	CORNER
wint_<fet>	RX image bias (one half of) Effective width (delta-W)	-	+ cor_rx, + cor_nmos for acwv
lint_<fet>	PC image bias (one half of) Effective length (delta-L)	+	+ cor_pc, + cor_nmos for aclv
tox_<fet>	Gate oxide thickness	-	+ cor_tox, for thin oxide + cor_toxd for thick oxide
vfb_<fet>	Base V_t	-	+ cor_nmos
u0_<fet> thesatl_<fet>	Mobility	+	+ cor_nmos
rsw_<fet>	Series resistance	-	+ cor_nmos
nsubo_<fet>	Channel doping	-	+ cor_nmos
fol1_<fet> fol2_<fet>	Short channel roll-off and body effect	+	+ cor_nmos
cj_<fet>	S/D Junction area cap	-	+ cor_nmos
cjsw_<fet>	S/D junction STI sidewall cap	-	
cjsg_<fet>	S/D gate sidewall junction cap	-	
dnoi_<fet>	Low frequency or flicker (1/f) noise	-	+ cor_noin

Table 6. *p-channel MOSFETs (pfet, dgpfet) Process Distributions*

Parameter**	Description	UP	CORNER
wint_<fet>	RX image bias (one half of) Effective width (delta-W)	-	+ cor_rx, + cor_pmos for acwv
lint_<fet>	PC image bias (one half of) Effective length (delta-L)	+	+ cor_pc, + cor_pmos for aclv
tox_<fet>	Gate oxide thickness	-	+ cor_tox, for thin oxide + cor_toxd for thick oxide
vfb_<fet>	Base V_t	+	+ cor_pmos
u0_<fet> thesatl_<fet>	Mobility	+	+ cor_pmos
rsw_<fet>	Series resistance	-	+ cor_pmos
nsubo_<fet>	Channel doping	-	+ cor_pmos
fol1_<fet> fol2_<fet>	Short channel roll-off and body effect	-	+ cor_pmos
cj_<fet>	S/D Junction area cap	-	+ cor_pmos
cjsw_<fet>	S/D junction STI sidewall cap	-	
cjsg_<fet>	S/D gate sidewall junction cap	-	
dnoi_<fet>	Low frequency or flicker (1/f) noise	-	+ cor_noip

** <fet> refers to the device type, e.g. “dgp” represents the DG thick oxide pfet.

Table 7. Resistor (opppcrsf, oprrrsf, nsres, kqres) Process Distributions

Parameter	Description	UP	CORNER
oppcrsf	Poly sheet rho	+	+ cor_res
oppcrenf	Poly end resistance	+	+ cor_res
oppcdwf	Poly resistor delta W	-	+ cor_pc
oprrrsf	RR Poly sheet rho	+	+ cor_res
opdlbnf	BN image bias	-	+ cor_res
oprrdwf	RR poly delta W	-	+ cor_pc
nbnsr	NS sheet rho	-	+ cor_npn
nsrenf	NS end resistance	+	+ cor_res
nsdwf	NS resistor delta W	-	+ cor_res
kqrsf	Kq sheet rho	+	+ cor_res
kqrenf	Kq end resistance	+	+ cor_res
kqdwf	Kq resistor delta W	-	+ cor_res

Table 8. nMOS Varactor and Differential NMOS Varactor (ncap, dgncap, diffncap) Process Distributions

Parameter	Description	UP	CORNER
co_mv co_mvdbg	Unit oxide capacitance ¹	-	+ cor_tox (ncap) + cor_toxd (dgncap)
plf	Effective PC length	+	- cor_pc
pwf	Effective RX width	+	+ cor_rx
nrnw qs_mv, qs_mvdbg	NW series resistance Depletion capacitance	-	+ cor_res
delm1	M1 width bias	+	+ cor_cap
m1rs	M1 sheet rho	-	+ cor_ind

1. In Monte Carlo simulations, this parameter is linked to the NFET or DG NFET Tox for each case in the run

Table 9. HA Varactor (havar) Process Distributions

Parameter	Description	UP	CORNER
nrnr	Series resistances	-	- cor_npn
nvrsl		-	- cor_npn
ncahav	Unit area capacitance	+	+ cor_cap
ncjsa, ncjsp	Area, perimeter capacitance to SX	+	- cor_cap

Table 10. MIM Capacitor (mim) Process Distributions

Parameter	Description	UP	CORNER
cmima, cmimp	Unit area, perimeter capacitance	+	+ cor_cap
prvav	AV via resistance	-	+ cor_cap
amrs	AM sheet resistance	-	+ cor_cap
lyrs	LY sheet resistance	-	+ cor_cap

Table 11. Inductors, Transmission Lines, Bondpad and vertical parallel plate capacitor (vncap) Process Distributions

Parameter	Description	UP	CORNER
numerous	Metal Thicknesses	+	+ cor_ind
numerous	Dielectric Thicknesses	+	+ cor_ind
delmq, delly, delam	Metal mask bias (upper metal levels)	+	+ cor_ind
mqr, lyrs, amrs	Metal sheet resistance (upper metal levels)	-	+ cor_ind
delmx, x=1-4	Metal mask bias (lower metal levels)	+	+ cor_cap

Table 12. Voltage Reference and Parasitic Diodes Process Distributions

Parameter	Description	UP	CORNER
delrx	RX bias in anode (cathode) dimensions: all	+	+ cor_rx
js_p, jsw_p	Forward bias current density: divpnp	+	+ cor_res
nw_rs	NWell resistance: divpnp	-	- cor_res
pwrs	PWell resistance: divpnp	-	- cor_res
m1rs	M1 resistance:divpnp	-	+ cor_ind
cj_n, cjsw_n	N+ S/D to substrate capacitance: diodenx	-	+ cor_nmos
cj_p, cjsw_p	P+ S/D to substrate capacitance: diodepnw, divpnp	-	+ cor_pmos

2.3 Corner Simulation Methodology

A group of corner parameters have been defined to provide quasi-independent variations of the device characteristics. Each of these corner parameter flags affects the skew parameters for a group of devices. If a skew parameter is shared between different groups, it is varied by the corner parameter for the group where it has a dominant effect in order to maintain the proper physical relationships. Set these flags between -3 and +3 to get the corresponding *magnitude* of three sigma variations in the multiple skew parameters of the devices affected.

The proper selection and *direction* of the change in the process skew parameters to get an 'up' value should be made by sensitivity analysis of the circuit performance on the skew parameters. It should be emphasized that the selection and direction of the changes in the parameters of the process skew files provided are only an example and are not necessarily inclusive for each application.

Table 13. Single Device Group Corner Parameters

Corner Parameter	Affected Parameter	Devices Affected in a Dominant Manner	Positive Corner Parameter Yields
cor_npn	several	nnp, npncbe, nsres	High current, high speed
cor_pnp	several	vpnp	High current, high speed
cor_nmos	several	nfet(tw), dgnfet(tw)	High current, high speed
cor_pmos	several	pfet, dgpfet	High current, high speed
cor_res	several	opppcres, oprpres, nsres, kqres, ncap, dgncap, diffncap, divpnp	High resistance, Low capacitance (MOS varactors)
cor_cap	several	havar, mim	High capacitance
cor_ind	several	ind, symind, rfline, singlewire, singlecpw, coupledwires, coupledcpw, bondpad, bend, gap, open, radialstub, short, step, tee, yjunction	High Q

A few additional corner parameters have been provided to skew the process parameters that are known to affect more than one group of devices in a potentially dominant manner, as defined in the following table:

Table 14. Multiple Device Group Corner Parameters

Corner Parameter	Primary Affected Parameter	Devices Affected in a Dominant Manner	Positive Corner Parameter Yields
cor_tox	thin tox (oxide thickness)	nfet(tw), pfet, ncap, diffncap	High current and high capacitance
cor_toxd	thick tox (oxide thickness)	dgnfet(tw), dgpfet, dgncap	High current and high capacitance
cor_pc	lint (polysilicon width)	nfet(tw), dgnfet(tw), pfet, dgpfet	High current
cor_rx	wint (STI width)	nfet(tw), dgnfet(tw), pfet, dgpfet	High current
cor_noin	NMOS flicker noise	nfet(tw), dgnfet(tw)	Low 1/f noise
cor_noip	PMOS flicker noise	pfet, dgpfet	Low 1/f noise

2.3.1 Corner Specification and Analysis

The corner parameters (cornr_*) described in the previous tables can be controlled within the design.inc (hspice) or the design.scs file (spectre) during simulation setup. Running corner simulations can serve different purposes as described by the following examples:

Device Type Sensitivity Analysis

To determine whether a circuit is more sensitive to a particular device group, skew one of the corner parameters while setting all others to zero. Repeat the simulation analysis in this manner for each of the device group corner parameters.

Multiple Device Group Analysis

It is also possible to simulate various combinations of extreme values across the different device groups simultaneously. For example, if a circuit is sensitive to bipolar devices, resistors and capacitors, each combination of 'up' and 'down' corners can be simulated to assess the effects on the circuit performance.

Best and Worst Case Analysis

Any of the best and worst case combinations of corner parameters should be *calibrated* against the Monte Carlo simulation results. It should be noted that the direction of corner parameters and their magnitude for the best and worst cases will depend on the class of circuit as well as the specific performance being analyzed.

The directions of the corner parameters for best and worst case performances can be set through sensitivity analysis for various device types. Setting the corner parameters to a magnitude of 3 may give a highly improbable case. Therefore, it is highly recommended that the best and worst case combinations be calibrated to the 3-sigma limits of the circuit performance by first finding the 3-sigma variation in the performance using a full Monte Carlo Analysis and then setting the magnitude of the corner parameters appropriately to match these limits.

2.3.2 Corner Parameter vs Monte Carlo Results

As mentioned above, the corner parameter settings must be calibrated against statistical Monte Carlo results for each class of circuits and performance metrics under consideration. The appropriate direction and magnitude of the multiple corner parameters depends not only on the topology of the circuit, the devices chosen, the design dimensions and the bias conditions, but also whether speed, power, noise sensitivity or other performance consideration is of prime concern.

The figures which follow show a sample of device level characteristics simulated with Monte Carlo statistical process variations and corner parameter variations. An understanding of the device parametric sensitivities to the statistical process variation and corner parameter settings may aid designers in the selection of devices (including design dimensions and bias conditions) and in establishing a simulation methodology for a particular class of circuits and performance metrics.

Note that in some cases, multiple process or model parameters are controlled by a single corner parameter. If the device parametric is highly sensitive to multiple independent process or model parameters, corner parameter settings of +/- 3 may result in values that far exceed what is expected from the long-term manufacturing environment, which is best represented by the statistical Monte Carlo simulations. As described previously, other process parameters, such as active width bias, polysilicon gate bias and gate oxide thickness, are controlled by separate corner parameters (cor_rx, cor_pc, cor_tox and cor_toxd) because of their influence on many device types. Taking multiple corner parameters to a +/- 3 value may also result in overly pessimistic values since the process parameters are not correlated.

For each figure, the device level Monte Carlo results are shown as histograms with the left y-axis of the plot denoting the frequency of occurrence for the device parameter plotted on the x-axis. The Monte Carlo simulations included 1000 cases with global process variation applied (“process only”). The right y-axis of each plot reflects a corner parameter value which results in the x-axis value of that same device parameter. In curves where multiple corner parameters are referenced, these parameters are varied together. In addition, the sign of some parameters are reversed so that their effects are maximized. All simulation results are for 25C. Where applicable, scribe-line (kerf) targets for the minimum and maximum device parameter values are shown as dashed vertical lines. If scribe-line targets are not available, the dashed lines represent the +/- 3 sigma values as calculated from the Monte Carlo results (assuming a Gaussian distribution). The device parametrics and corner parameter sensitivities from the figures are summarized in the table below.

Note: The MOSFET simulations were done with the STI stress effect disabled (gstis=0) as this corresponds to the larger RX length (3μm) found in the physical layout of the kerf devices used to provide the inline monitor data and the target spec limits shown in the figure. The behavior of the regular-Vt devices in this example should be consistent for all thin oxide device types. Similarly, the DG device plots are representative of the behavior for all of the thick oxide devices.

Table 15. Device Parametrics and Corner Sensitivities

Figure	Device Parametric	Corner Parameter(s) and Direction Setting	Corner(s) Value
1	High- f_T NPN Vbe (npn), $I_c=10\mu A$, $V_{cb}=0V$	cor_npn vs Kerf/Monte Target Limit	-2.15
	High- f_T NPN Beta (npn), $V_{be}=0.72V$, $V_{cb}=0V$		1.5
	High-Breakdown NPN Vbe (npn), $I_c=10\mu A$, $V_{cb}=0V$		-2.05
	High-Breakdown NPN Beta (npn), $V_{be}=0.72V$, $V_{cb}=0V$		1.4
2	Vertical PNP Beta (vpnp) $V_{be}=-0.78V$, $W=0.4\mu m$, $L=2.5\mu m$	cor_pnp vs Kerf Target Limit	2.55
	Vertical PNP Vbe (vpnp) $I_c=10\mu A$, $W=0.4\mu m$, $L=2.5\mu m$		-2.7
	Vertical PNP Beta (vpnp) $V_{be}=-0.78V$, $W=0.8\mu m$, $L=5\mu m$	cor_pnp vs Monte Carlo Limit	2.75
	Vertical PNP Vbe (vpnp) $I_c=10\mu A$, $W=0.8\mu m$, $L=5\mu m$		-2.95
3	NFET IDSAT @ $V_{gs}=V_{ds}=1.2V$, $L=0.12\mu m$, $W=5\mu m$	cor_nmos, cor_pc, cor_tox vs Kerf Target Limit	1.0
	NFET IDLIN @ $V_{gs}=1.2V$, $V_{ds}=0.05V$, $L=5\mu m$, $W=5\mu m$		1.9
	PFET IDSAT @ $V_{gs}=V_{ds}=1.2V$, $L=0.12\mu m$, $W=5\mu m$	cor_pmos, cor_pc, cor_tox vs Kerf Target Limit	0.95
	PFET IDLIN @ $V_{gs}=1.2V$, $V_{ds}=0.05V$, $L=5\mu m$, $W=5\mu m$		1.6

Table 15. Device Parametrics and Corner Sensitivities

Figure	Device Parametric	Corner Parameter(s) and Direction Setting	Corner(s) Value
4	DGNFET IDSAT @ Vgs=Vds=2.5V, L=0.24μm, W=5μm	cor_nmos, cor_pc, cor_toxd vs Kerf Target Limit	1.05
	DGNFET IDLIN @ Vgs=2.5V, Vds=0.05V, L=5μm, W=5μm		2.35
	DGPFET IDSAT @ Vgs=Vds=2.5V, L=0.24μm, W=5μm	cor_pmos, cor_pc, cor_toxd vs Kerf Target Limit	1.25
	DGPFET IDLIN @ Vgs=2.5V, Vds=0.05V, L=5μm, W=5μm		2.55
5	NFET 1/f Noise @ Vds=1.0V, Vgs=0.7V L=0.12μm, W>=10μm, nf=1	cor_noin, -cor_pc, cor_tox vs Monte Carlo Limit	-1.85
	NFET 1/f Noise @ Vds=1.0V, Vgs=0.7V L=0.12μm, W>=10μm, nf=10		-1.85
	PFET 1/f Noise @ Vds=1.0V, Vgs=0.7V L=0.12μm, W>=10μm, nf=1	cor_noip, -cor_pc, cor_tox vs Monte Carlo Limit	-2.05
	PFET 1/f Noise @ Vds=1.0V, Vgs=0.7V L=0.12μm, W>=10μm, nf=10		-2.15
6	P+ Polysilicon Resistance (oppccres), W=1μm, L=2μm	cor_res, cor_pc vs Monte Carlo limit	1.85
	P+ Polysilicon Resistance (oppccres), W=10um, L=40um		2.9
	NS Resistance (nsres), W=3um, L=3um	cor_res, cor_rx, cor_npn vs Monte Carlo limit	1.95
	NS Resistance (nsres), W=10um, L=40um		1.9
7	RR Polysilicon Resistance (oprrpres), W=1μm, L=2μm	cor_res, cor_pc vs Monte Carlo limit	1.5
	RR Polysilicon Resistance (oprrpres), W=10μm, L=40μm		2.7
	KQ Resistance (kqres), W=5um, L=5um	cor_res vs Monte Carlo limit	1.85
	KQ Resistance (kqres), W=10um, L=40um		2.45
8	Thin Oxide nMOS Varactor Cap (ncap) @ 1V, L=2μm, W=2μm, nf=16, rep=25	cor_tox, cor_rx, -cor_res, -cor_pc vs Monte Carlo limit	2.3
	Thin Oxide nMOS Varactor Cap (ncap) @ -0.5V, L=2μm, W=2μm, nf=16, rep=25		2.15
	Thick Oxide nMOS Varactor Cap (dgncap) @ 3.3V, L=2μm, W=2μm, nf=16, rep=25	cor_toxd, cor_rx, -cor_res, -cor_pc vs Monte Carlo limit	2.2
	Thick Oxide nMOS Varactor Cap (dgncap) @ -0.5V, L=2μm, W=2μm, nf=16, rep=25		1.9

Table 15. Device Parametrics and Corner Sensitivities

Figure	Device Parametric	Corner Parameter(s) and Direction Setting	Corner(s) Value
9	HA Varactor Capacitance (havar) @ 0V, W=2μm, L=10μm, #anodes=20	cor_cap, cor_rx vs Monte Carlo limit	1.85
	HA Varactor Capacitance (havar) @ -3V, W=2μm, L=10μm, #anodes=20		1.6
	Single MIM Capacitance (mim) @ 0V W = L = 25μm	cor_cap vs Monte Carlo limit	2.7
	Forward-Biased Diode Voltage (divpnp) @ 10μA W=1.4μm, L=20μm, nf=4	-cor_rx, cor_res vs Monte Carlo limit	-2.55
10	AM Inductor Q @ 3.5GHz x=200μm, w=15μm, s=5μm, n=1.5	cor_ind vs Monte Carlo limit	2.1
	AM Inductor Q @ 3.5GHz x=200μm, w=10μm, s=3μm, n=5.5		1.7
	AM Inductor Q @ 3.5GHz x=200μm, w=5μm, s=3μm, n=8.5		1.45
11	AM Inductor L @ 3.5GHz x=200μm, w=15μm, s=5μm, n=1.5	cor_ind vs Monte Carlo limit	-2.1
	AM Inductor L @ 3.5GHz x=200μm, w=10μm, s=3μm, n=5.5		-2.1
	AM Inductor L @ 3.5GHz x=200μm, w=5μm, s=3μm, n=8.5		-2.1

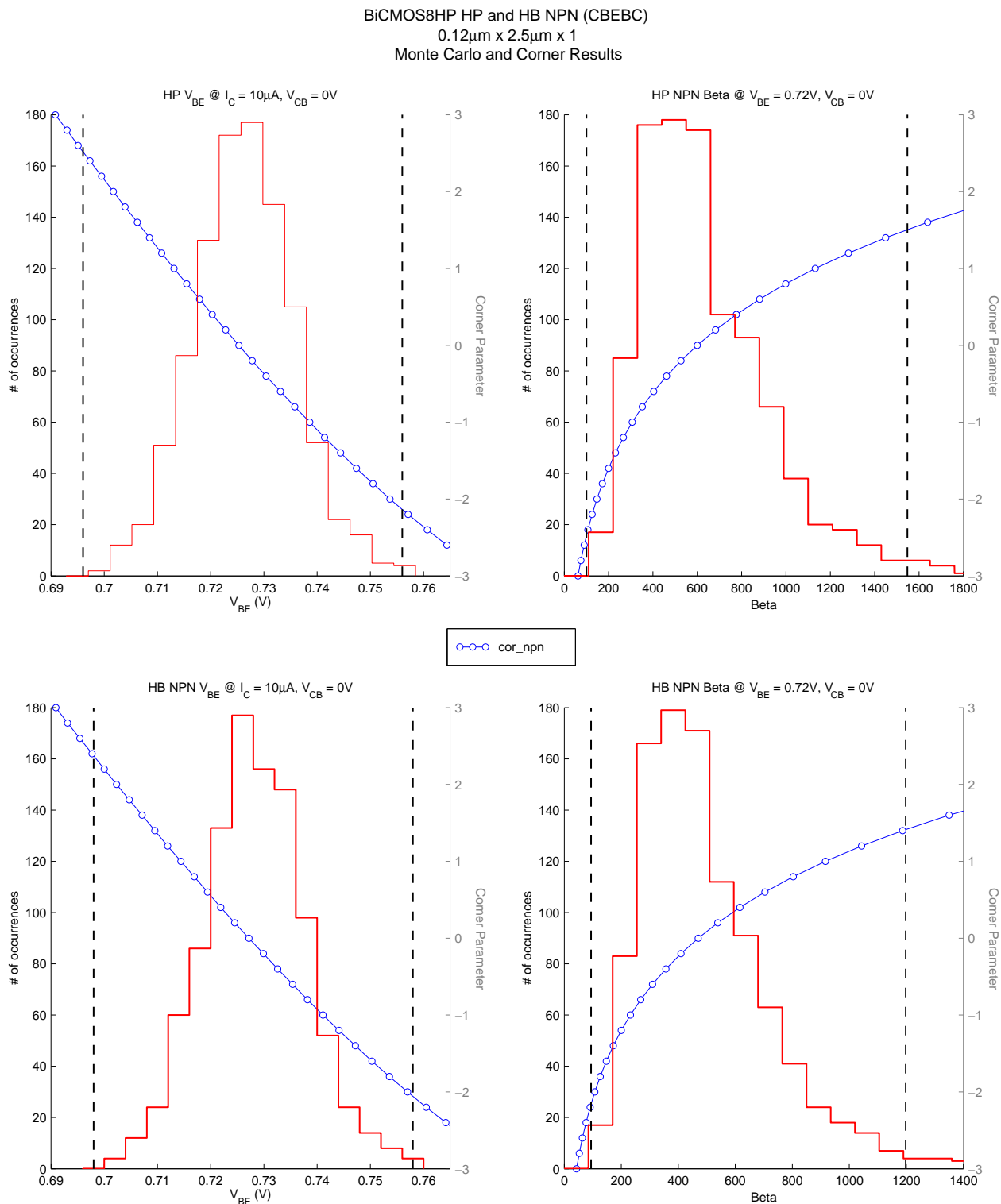


Figure 1. Corner vs Monte Carlo Results : NPNs

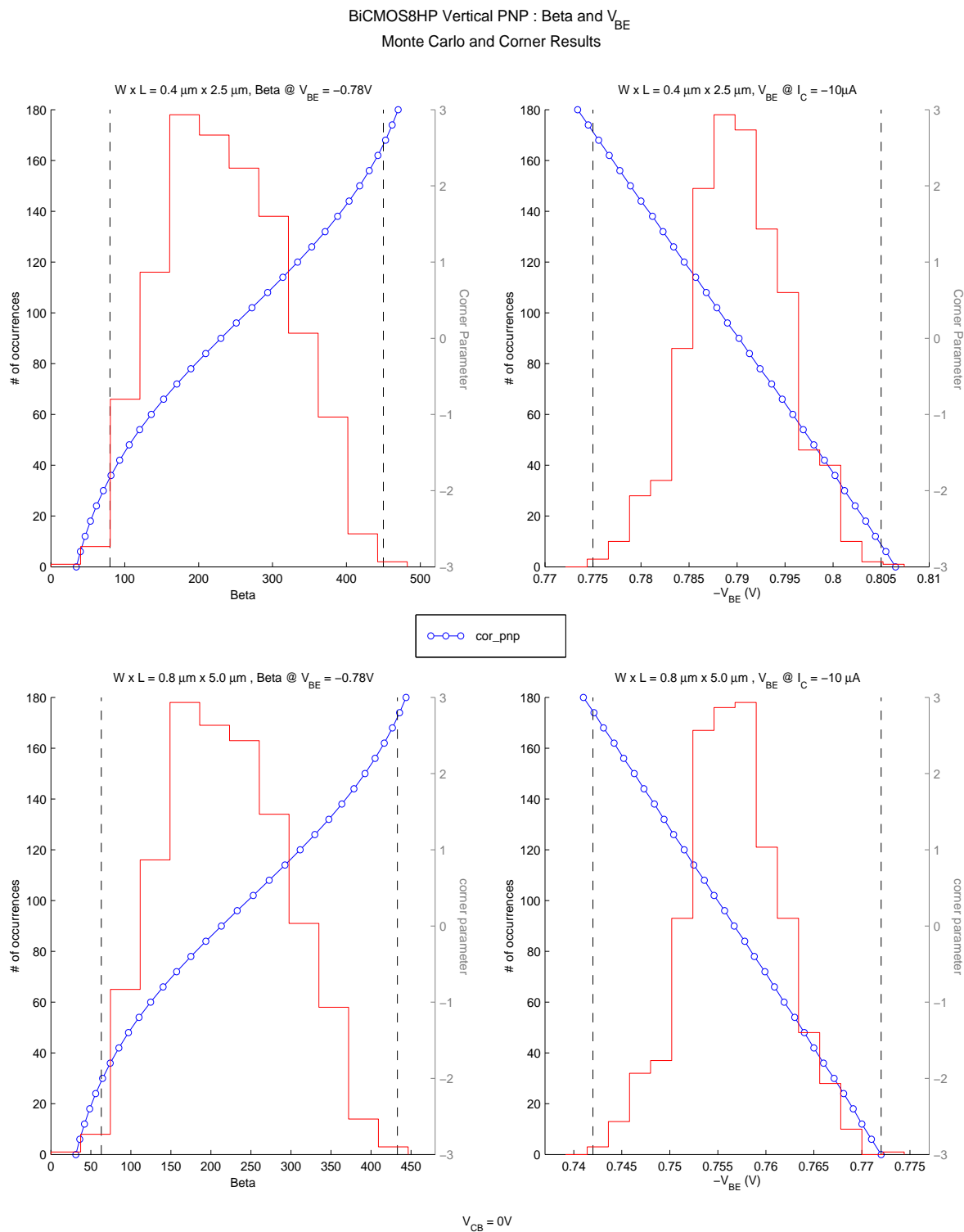


Figure 2. Corner vs Monte Carlo Results : VPNP

BiCMOS8HP NFET and PFET
Monte Carlo and Corner Results

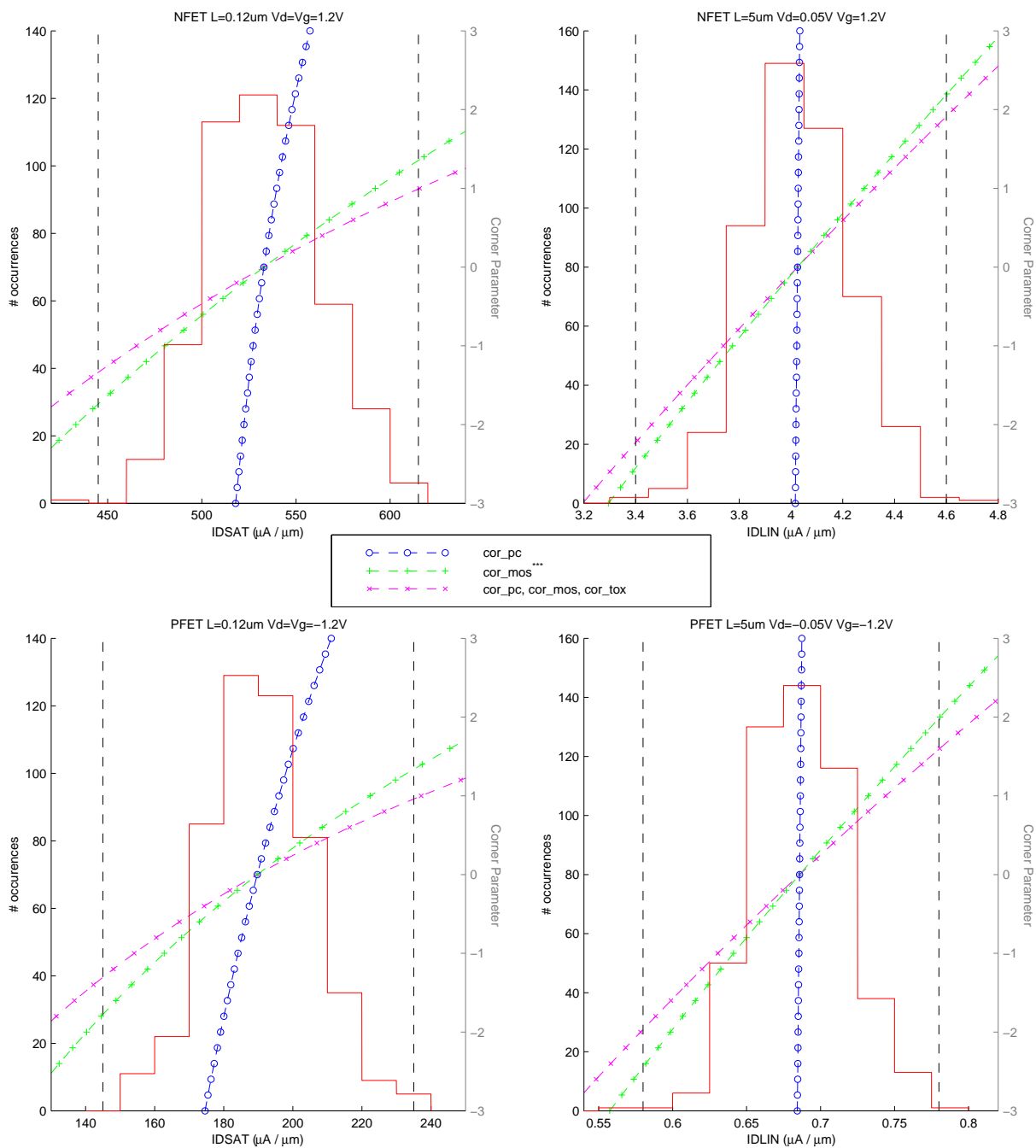
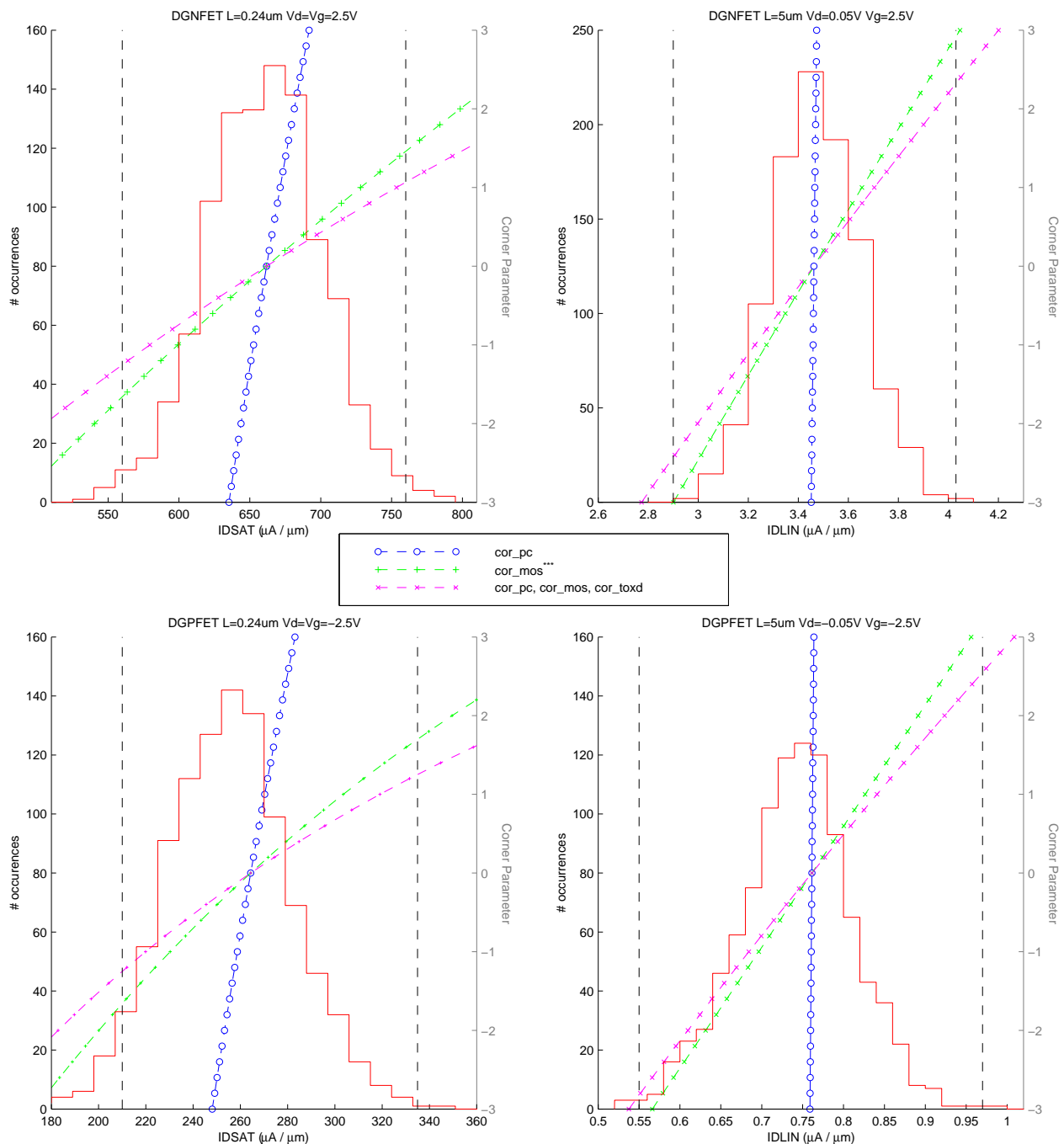


Figure 3. Corner vs Monte Carlo Results : NFET and PFET

BiCMOS8HP DGNFET and DGPFET
Monte Carlo and Corner Results



*** "cor_mos" represents "cor_nmos" and "cor_pmos" for the DGNFET and DGPFET plots, respectively

Figure 4. Corner vs Monte Carlo Results : DGNFET and DGPFET

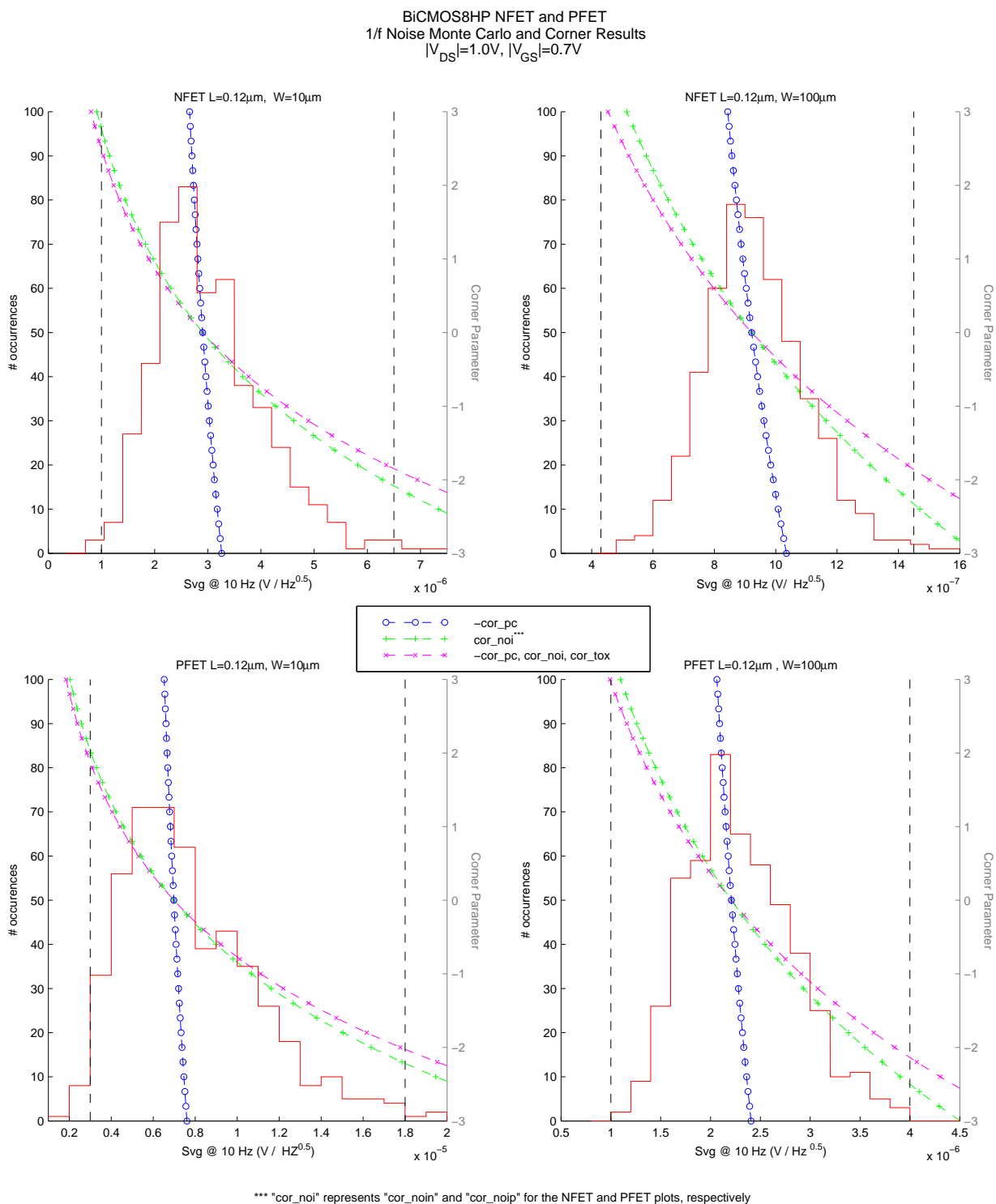


Figure 5. Corner vs Monte Carlo Results : MOSFET Statistical Flicker (1/f) Noise

BiCMOS8HP P+ Polysilicon and NS Resistors
Monte Carlo and Corner Results

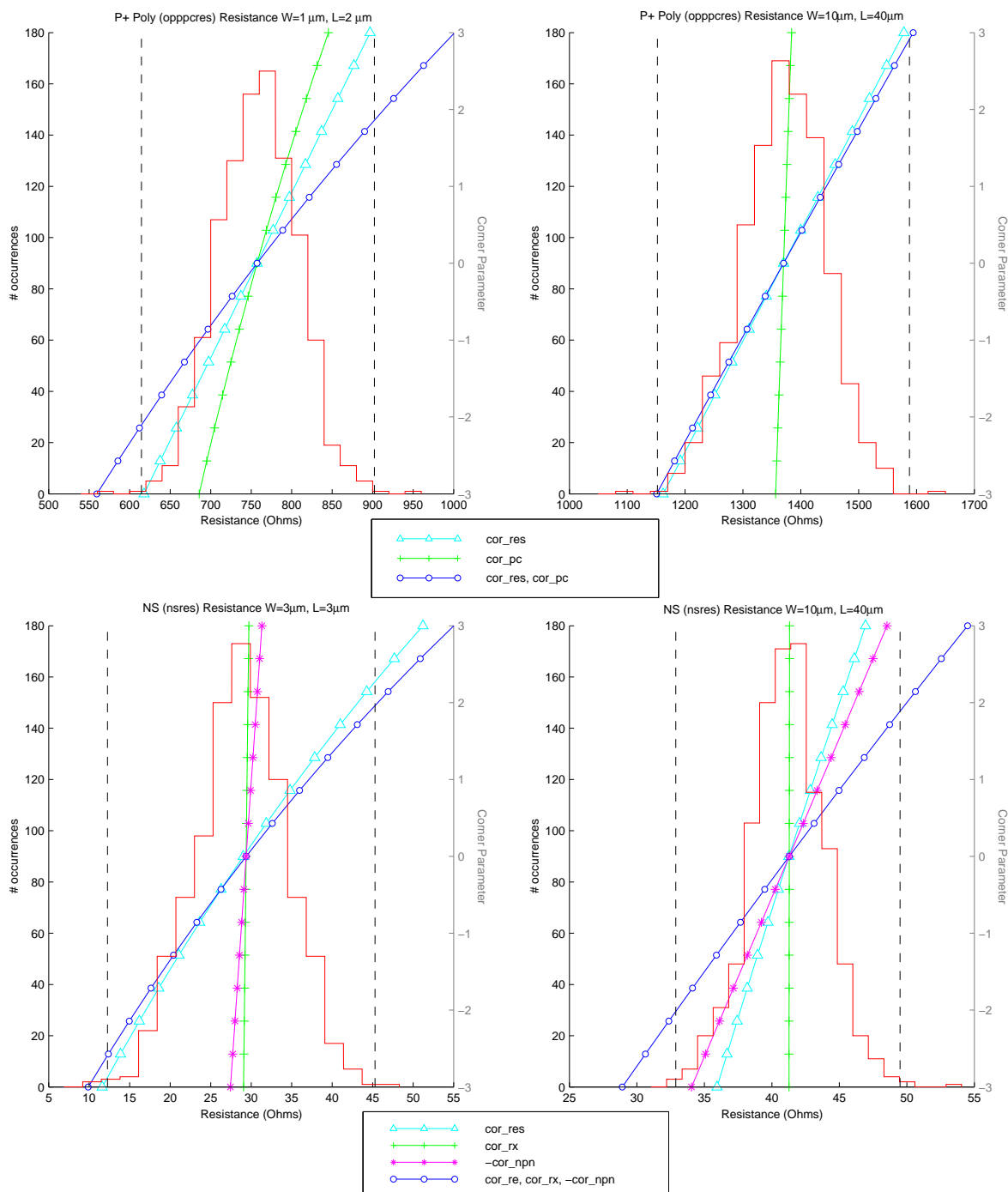


Figure 6. Corner vs Monte Carlo Results : P+ Poly and NS Resistors

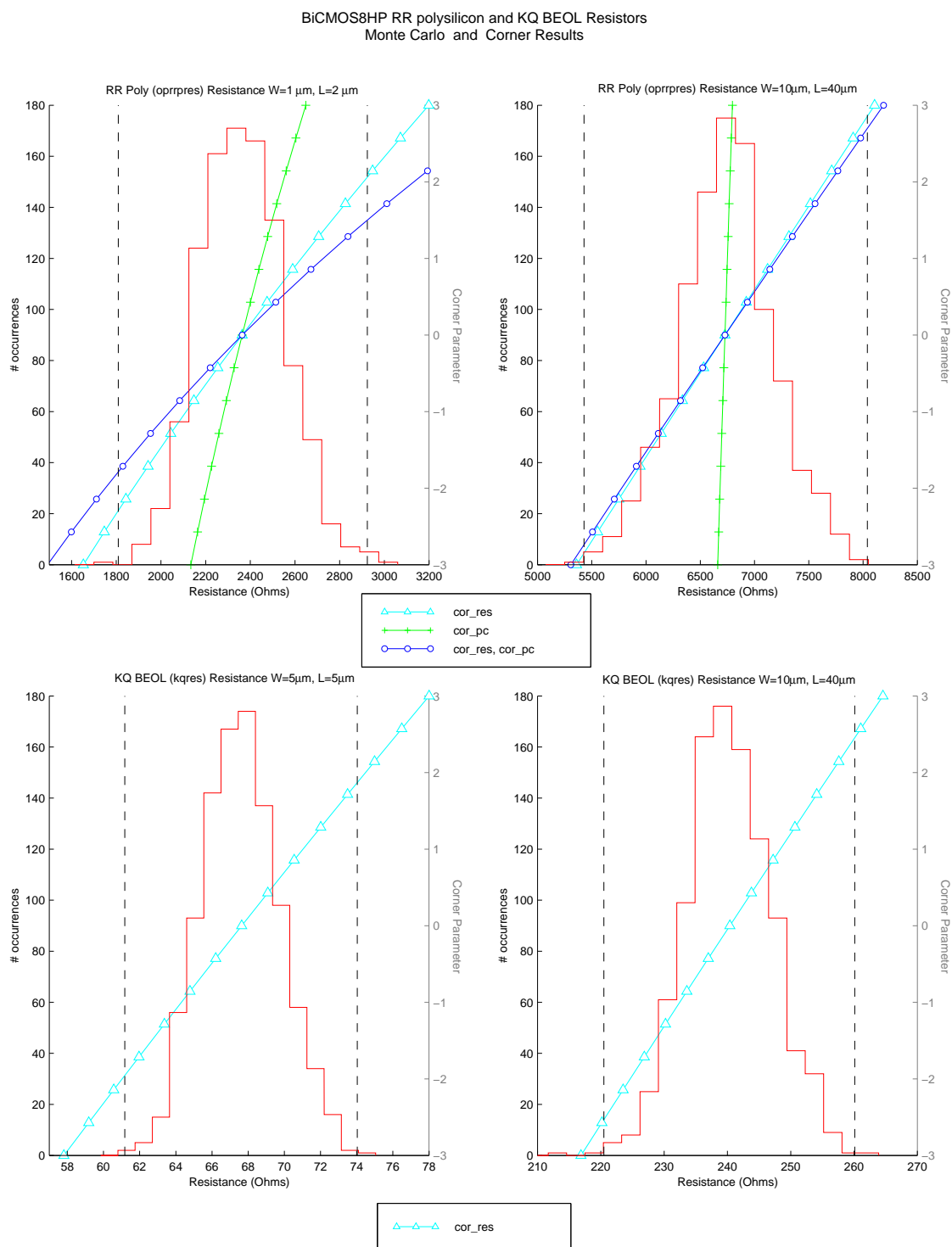


Figure 7. Corner vs Monte Carlo Results : RR Poly and KQ Resistors

BiCMOS8HP NCAP and DGNCAP Varactors
Monte Carlo and Corner Results

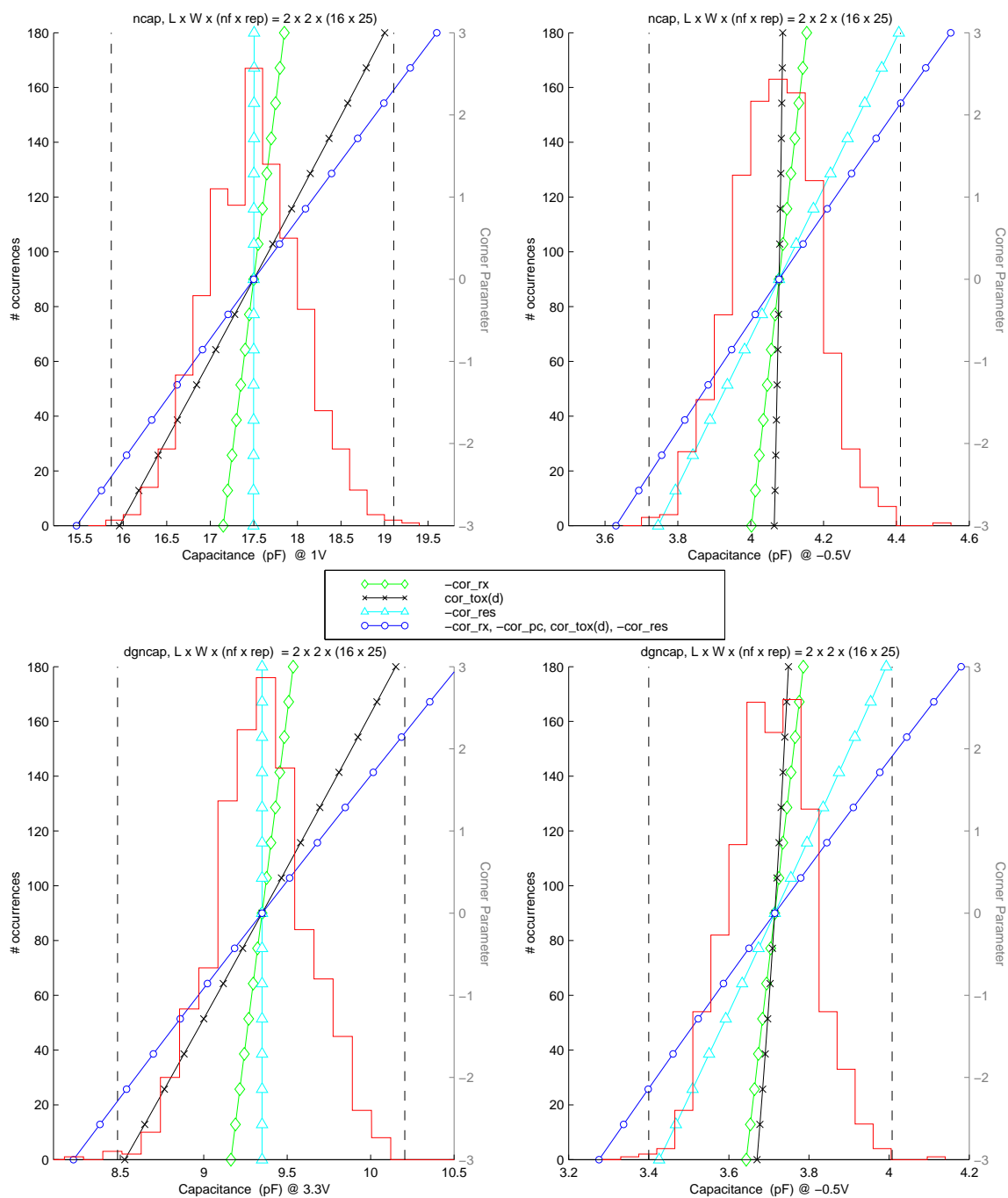


Figure 8. Corner vs Monte Carlo Results : nMOS Varactors

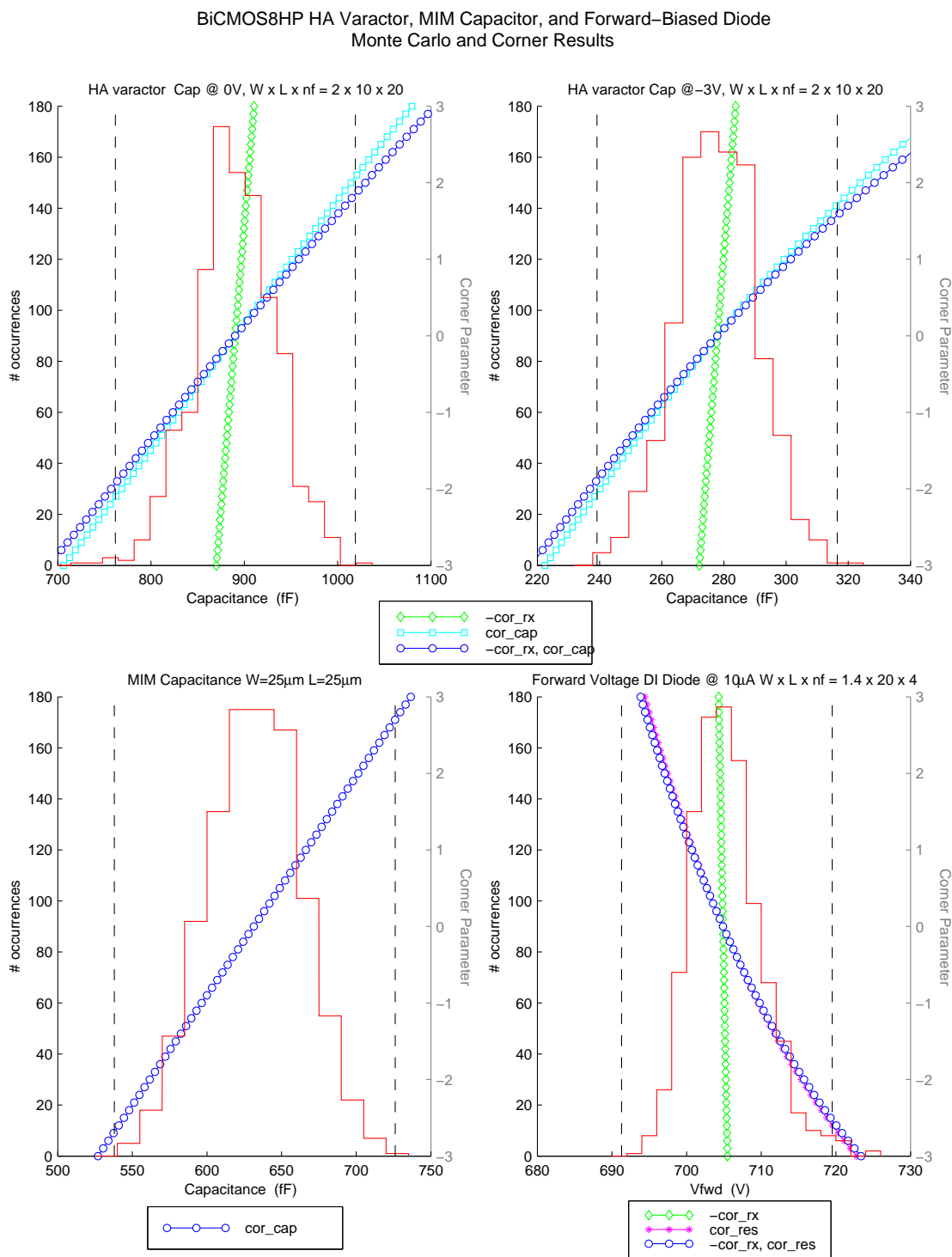


Figure 9. Corner vs Monte Carlo Results : HA Varactor, MIM Capacitor and Forward-Biased Diode

BiCMOS8HP Inductor Q
Monte Carlo and Corner Results

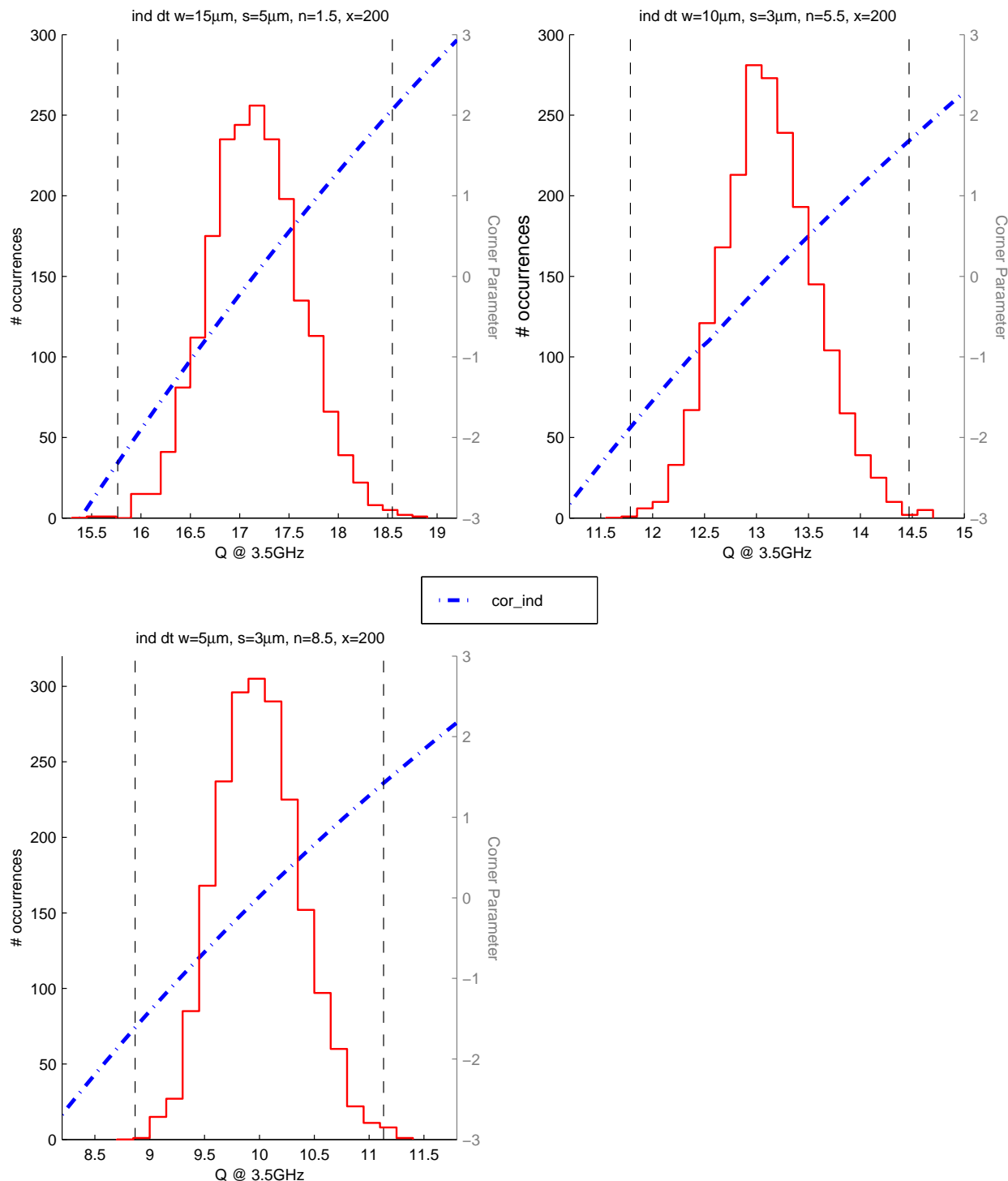


Figure 10. Corner vs Monte Carlo Results : Inductor -- Q

BiCMOS8HP Inductor: Inductance
Monte Carlo and Corner Results

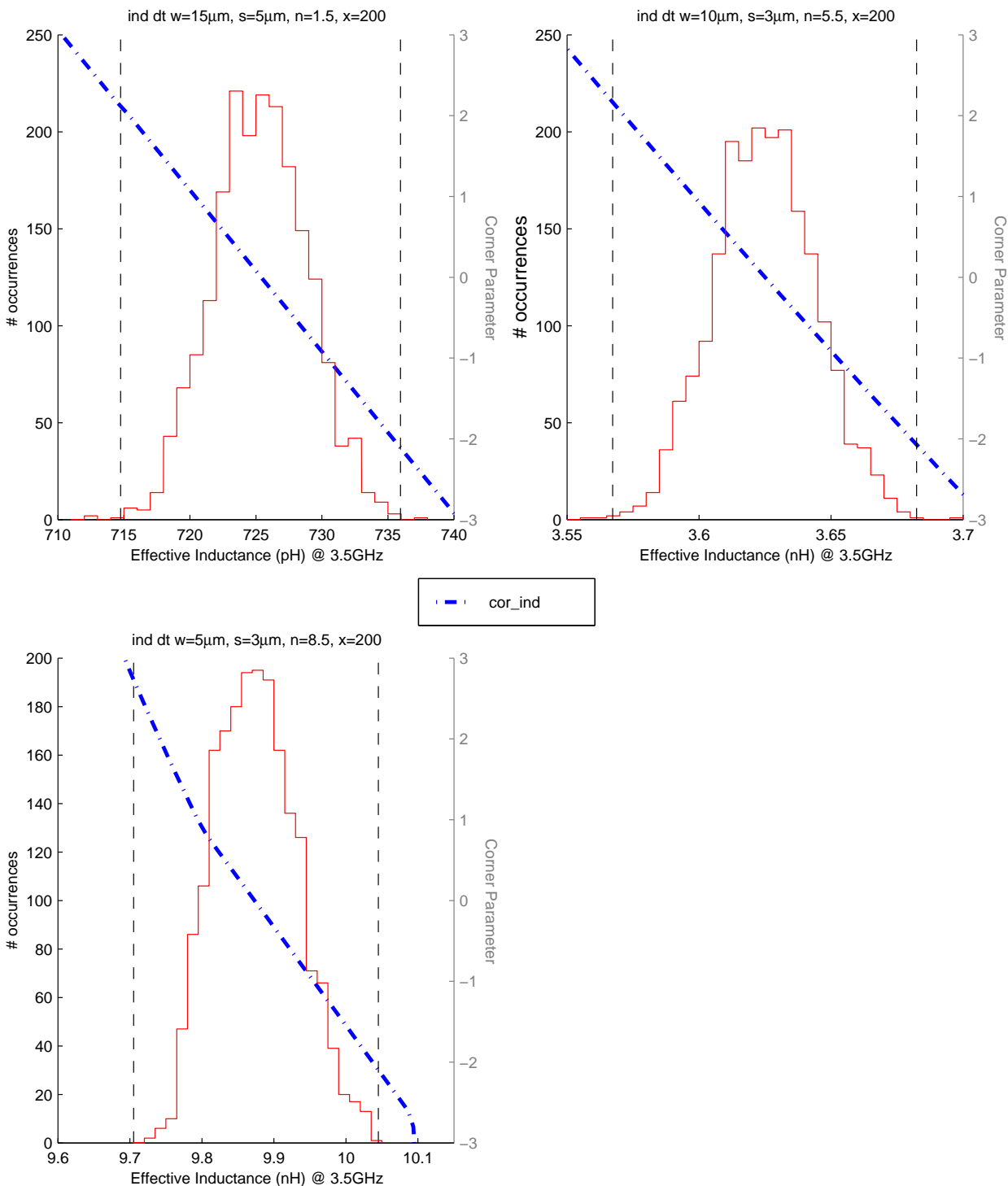


Figure 11. Corner vs Monte Carlo Results : Inductor -- Inductance Value

2.4 Fixed Corner Analysis for MOSFETs

This section discusses the definition of fixed corner parameters supplied for the MOSFET models: nfet, pfet, dgnfet, and dgpfet. The passive and BEOL device models are not included in the pre-defined set of fixed corners.

There are many ways to define process skew corners. Process corners for a particular circuit are related to how sensitive the circuit is to the various process parameters. Hence, it is not possible to provide corners for all possible circuit applications. The MOSFET corner parameters provided here are primarily for predicting static logic circuit delays. However, override capability is provided to allow users to pick and choose their own corners which can be different than the ones discussed here.

2.4.1 MOSFET Fixed Corner Definitions

For digital applications, seven fixed corners are defined as listed in Table 16 and illustrated in Figure 12.

Table 16. Corner Definition for Digital Circuit Application		
Corner Name	Definition	Purpose
TT	Nominal process	Estimate typical performance
FF	Match fast circuit delay as measured on ring oscillators during inline testing.	Best case timing of static cmos circuits
SS	Match slow circuit delay as measured on ring oscillators during inline testing.	Worst case timing of static cmos circuits
FS	Match I_{dsat} and V_t skew between NFETs and PFETs based on line data and design manual specifications.	Circuit operation under N to P mismatch, for fast Nfet and slow Pfet
SF	Match I_{dsat} and V_t skew between NFETs and PFETs based on line data and design manual specifications	Circuit operation under N to P mismatch, for slow Nfet and fast Pfet
FF-FUNCTIONAL (FFF)	Bound design manual extreme I_{dsat} and V_t for wide and narrow short channel FETs	Verify circuit robustness under extreme process condition with fast Nfet and fast Pfet
SS-FUNCTIONAL (SSF)	Bound design manual extreme I_{dsat} and V_t for wide and narrow short channel FETs	Verify circuit robustness under extreme process condition with slow Nfet and slow Pfet

Typical Corner

The typical (TT) corner corresponds to a nominal process simulation where all corner parameters are set to zero and all model parameter values represent the nominal process specifications.

Functional Corners

A “functional corner” is defined as a group of corner parameter values that will predict the +/- 3-sigma limit of a critical electrical parameter, such as I_{dsat} or V_{tsat} . The fast-fast functional (FFF) and slow-slow function (SSF) corners predict the best case and worst case design manual limits (+/- 3-sigma), respectively, for I_{dsat} and V_{tsat} values for all NFET and PFET devices in the circuit simultaneously. Device geometries used in setting the functional corners included both wide $\times L_{min}$ and $W_{min} \times L_{min}$. For the purposes of these functional corners, other electrical parameters were not considered for determining the specific corner parameter values.

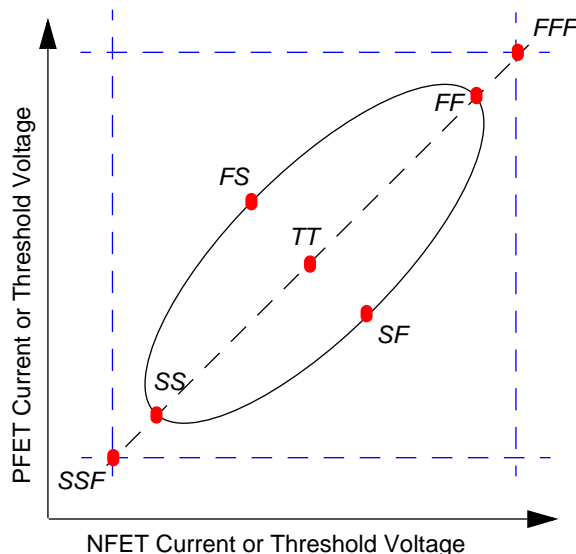


Figure 12. Graphical Representation of MOSFET Fixed Corners. Specification limits are shown as dashed blue lines, and the various fixed corners are shown as red dots. The ellipse represents a cloud of statistical data.

Performance Corners

The physical nature of the process makes it possible for an NFET to run faster than nominal and, at the same time, for a PFET to run slower than nominal, and vice versa. The main factors that cause this behavior are an offset in delta-L (N to P), V_t dopant mis-matches and other random variations. Note that while it is possible for N and P type devices to behave in opposite ways, they would not go to the 3-sigma limits simultaneously due to the many shared process steps. For this reason, a less than 3-sigma skew of the NFET and PFET devices in opposite directions has been assumed in the "performance corners", the fast-fast (FF), slow-slow (SS), fast-slow (FS) and slow-fast (SF) corners.

To generate the performance corner values, Monte Carlo simulations were run on a suite of circuits to establish 3-sigma limits for static CMOS logic delays for setting FF and SS performance corners. The suite of circuits includes inverters, NAND, and NOR circuits with varying device widths, fan-out, and stage configurations. Monte Carlo runs included both chip mean and across chip variations of V_t , L, and W. The circuits contained 12 delay stages. Delay per stage was calculated by the average rising and falling delays across the center 8 stages of the circuits so some averaging of $AC \cdot V$ is achieved.

The NFET to PFET mismatch corners were determined by matching the NFET and PFET I_{dsat} values at the 3-sigma mismatch extremes.

Note that the fixed corner variations in the models do not include device reliability degradation mechanisms such as threshold voltage shifts caused by ionics, NBTI, etc.

2.4.2 MOSFET Fixed Corner Implementation

Each fixed corner is specified as a particular set of values for the corner parameters (cor_nfet, cor_pc, etc.). As described in Section 2.1 on page 13, corner models are invoked through the specification of a particular analysis option, which then sets the cor_* parameters for the models to a set of defined values for that corner.

The d<param>_<fet>_fc parameters listed in Table 17 are the adders to the RVT and DG FET PSP model parameters to achieve the corner values.

Table 17. MOSFET PSP Parameters Controlled by Corner Parameters	
Corner Parameter	PSP Parameter affected
dvfbo_<fet>_fc	vfbo
dcjorsti_<fet>_fc	cjorsti
dcjorgat_<fet>_fc	cjorgat
dvfbl_<fet>_fc	vfbl
dlov_<fet>_fc	lov
dcjorbot_<fet>_fc	cjorbot
dthesatl_<fet>_fc	thesatl
dtoxo_<fet>_fc	toxo
dfol1_<fet>_fc	fol1
dlap_<fet>_fc	lap
dvfblw_<fet>_fc	vfblw
duo_<fet>_fc	uo
drsw1_<fet>_fc	rsw1
dwot_<fet>_fc	wot
For PSP models where <fet> = n, p, dgn or dgp	

Note: The device parametric values shown in these sections were determined without N-well proximity or STI stress effects. N-well proximity and STI stress effects are layout dependent. When these effects are included, additional adders may be applied, and the final device parametric values will be changed.

2.4.3 MOSFET Corner Model Plots

This section shows the I_{dsat} and V_{tsat} characteristics for the different FET pairs at the various fixed corners.

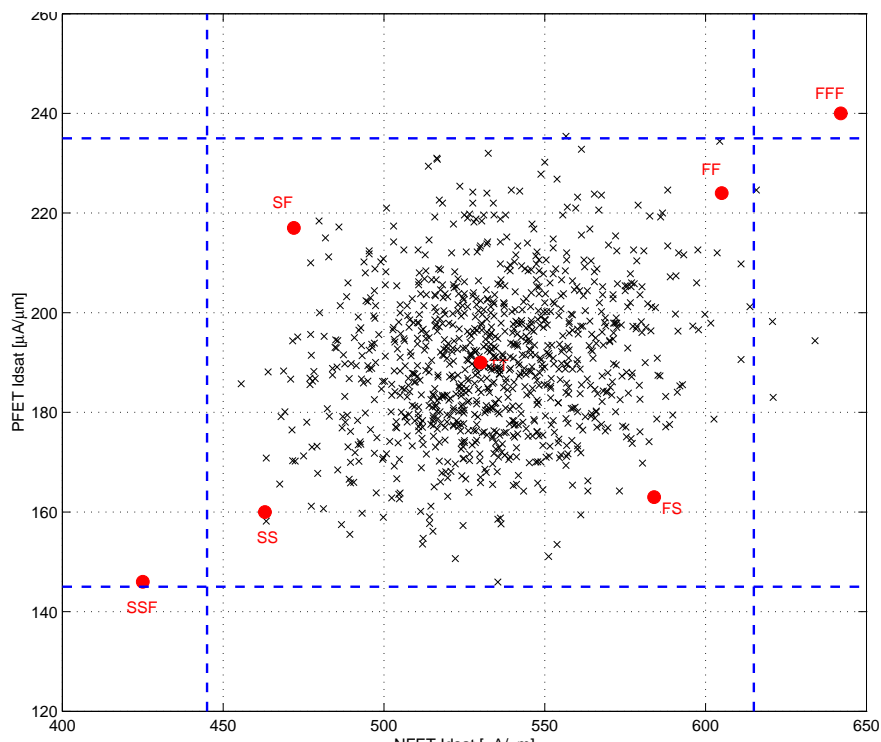


Figure 13. PFET I_{dsat} vs. NFET I_{dsat} .

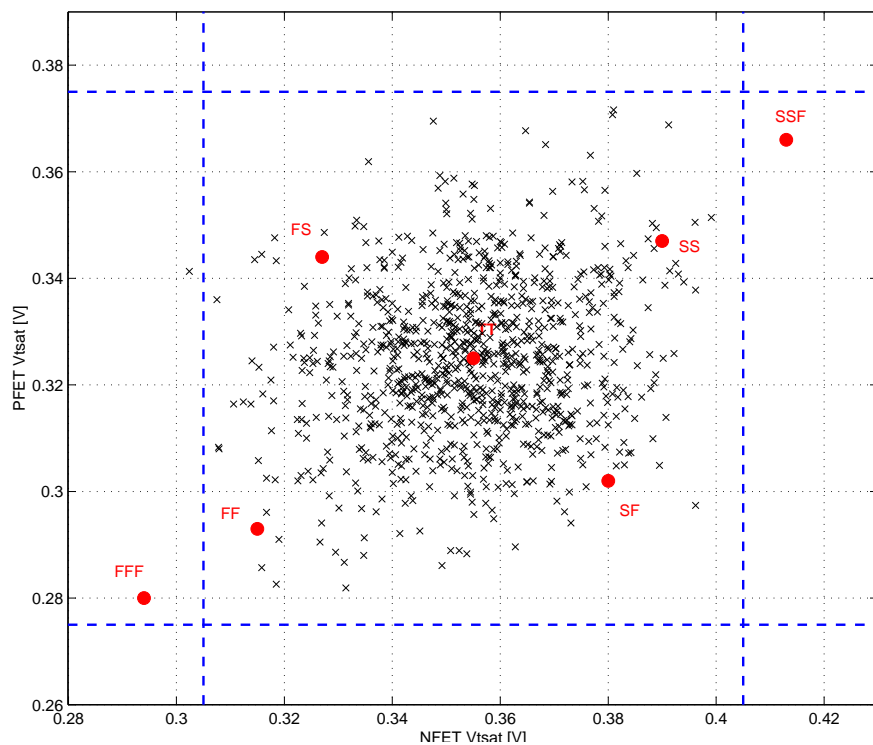


Figure 14. PFET V_{tsat} vs. NFET V_{tsat} .

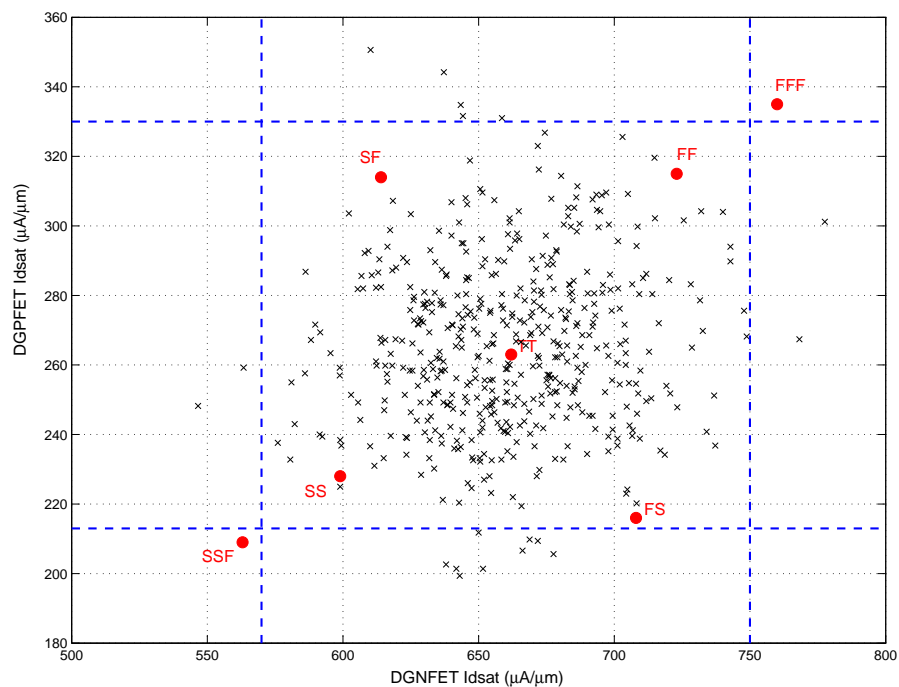


Figure 15. DGNFET I_{dsat} vs. DGNFET I_{dsat} .

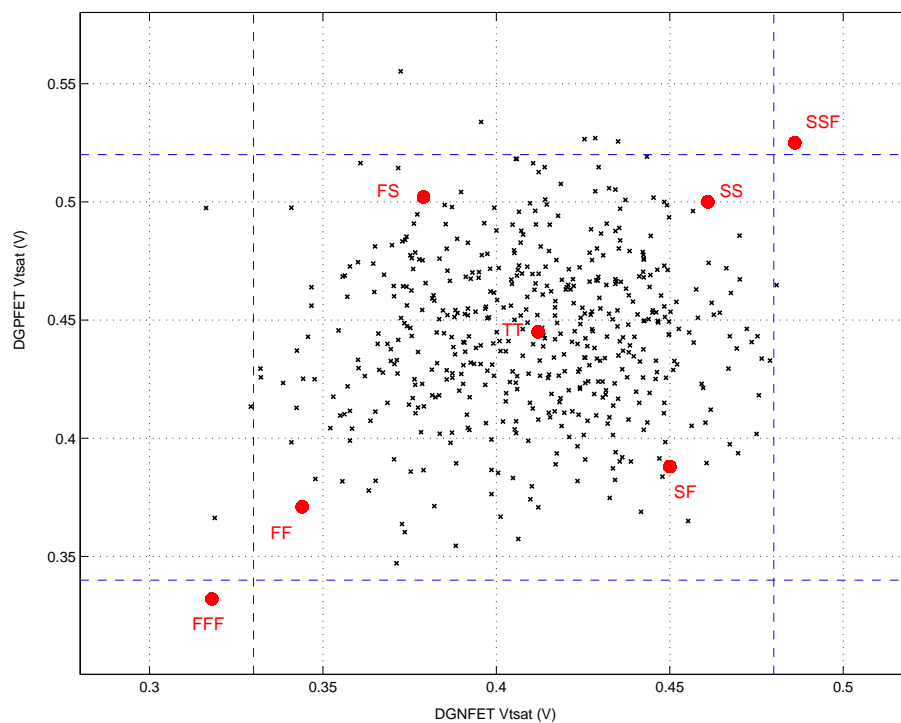


Figure 16. DGNFET V_{tsat} vs. DGNFET V_{tsat} .

2.5 Example Simulation Settings

As described earlier, user controlled settings may be specified through the design.inc (HSPICE) or design.scs file (Spectre). A few common examples are shown below.

2.5.1 Monte Carlo Simulations

Note: The IBM PDK does not support the Cadence Monte-Carlo form based "Process Only" or "Mismatch Analysis Only" variation options. For all Monte-Carlo simulations, the "Process and Mismatch" option should be selected.

Instance specific variation is always included in the non-FET devices which include mis-match effects in the model. No switch setting in the design.inc or design.scs file controls the instance specific variation of non-FET devices. FET devices have instance specific variations applied depending on the settings of the fet_geo_mis (geometric ACV effects) and fet_dop_mis (doping mis-match) switches.

When performing a mis-match only analysis on a well-designed layout, use switch settings: mc_global=0, fet_dop_mis=1, fet_geo_mis=0 (turning off the ACV effects). For a more pessimistic estimate of mis-match for a non-ideal layout, set fet_geo_mis=1 (as shown in the 2nd example below).

Table 18. Example with all global and instance specific variations enabled (DEFAULT)

Control	Setting	Effect
mc_global	1	Full statistical process variation enabled, best representation of long term manufacturing performance. cor_* parameters have no effect
fet_dop_mis	1	
fet_geo_mis	1	
pc_nest	1	
pc_orient	1	
pc_dist	1	
rx_dist	1	
corner option	tt	
cor_*	0	

Table 19. Example with chip mean values controlled by corner parameters, only instance specific statistical variations

Control	Setting	Effect
mc_global	0	Statistical variation enabled only for instance specific variations. Chip mean distributions for FETs and nonFETs are controlled by the cor_* parameters. Useful for looking at extreme process corners for circuits sensitivite to device mis-match.
fet_dop_mis	1	
fet_geo_mis	1	
pc_nest	1	
pc_orient	1	
pc_dist	1	
rx_dist	1	
corner option	tt	
cor_*	-3 to +3	

Table 20. Example with FET chip mean values extended to include ACV effects

Control	Setting	Effect
mc_global	2	Full statistical variation enabled, however the FET channel length and width chip mean variation is extended to include ACV effects (not instance specific) . Useful for looking at extreme process corners for circuits not sensitivite to fet geometric mis-match. Instance specific variation for FETs is only through the non-geometric (doping) variation. Non-FET devices are treated the same for the default mc_global = 1.
fet_dop_mis	1	
fet_geo_mis	1	
pc_nest	1	
pc_orient	1	
pc_dist	1	
rx_dist	1	
corner option	tt	
cor_*	0	

Table 21. Example with all global and sub-set of instance specific variations enabled

Control	Setting	Effect
mc_global	1	Full statistical process variation for chip means enabled ACV variation due to FET spacing disabled, resulting in tighter FET tracking. Appropriate for circuits with a total size less than 100x100um. cor_* parameters have no effect.
fet_dop_mis	1	
fet_geo_mis	1	
pc_nest	1	
pc_orient	1	
pc_dist	0	
rx_dist	0	
corner option	tt	
cor_*	0	

Note: Similar results may also be obtained by setting the netlisted parameters pld200 and pwd100 to zero for every fet in the circuit. Fet to Fet tracking will be the same with either method, but more accurate results for the total Across Chip Variation will be obtained through the netlisted instance parameters.

2.5.2 Non-Statistical Simulations

Table 22. Example of non-statistical simulation with custom user corner parameters enabled

Control	Setting	Effect
mc_global	0	Non-statistical simulation. Parameter values are skewed in accordance with the cor_* settings. Cor_rx and cor_pc move all FET channel length and widths together.
fet_dop_mis	0	
fet_geo_mis	0	
pc_nest	1	
pc_orient	1	
pc_dist	1	
rx_dist	1	
corner option	tt	
cor_*	-3 to + 3	

Table 23. Example of non-statistical simulation for MOSFET fixed process corners enabled

Control	Setting	Effect
mc_global	0	Non-statistical simulation. Parameter values are skewed in accordance with the cor_* settings provided in the "fixed_corner" file. Cannot be used in conjunction with any other MOSFET corner parameter settings.
fet_dop_mis	0	
fet_geo_mis	0	
pc_nest	1	
pc_orient	1	
pc_dist	1	
rx_dist	1	
corner options	fff, ssf, ff, ss, fs or sf	
cor_*	0	

Table 24. Example of non-statistical simulation with ACV user-overrides

Control	Setting	Effect
mc_global	0	Non-statistical simulation. skewed fast by one sigma through the cor_pc, cor_rx and cor_tox* settings. NFET to PFET tracking is controlled by cor_nmos and cor_pmos to represent a slow nfet, fast pfet.
fet_dop_mis	0	
fet_geo_mis	1	
pc_nest	1	
pc_orient	1	
pc_dist	1	
rx_dist	1	
corner option	tt	
cor_pc	+ 1.0	
cor_rx	+1.0	
cor_tox	+1.0	
cor_toxd	+1.0	
cor_nmos	- 0.5	
cor_pmos	+ 0.5	

Table 25. Example of non-statistical simulation with ACV user-overrides

Control	Setting	Effect
mc_global	0	<p>Non-statistical simulation. ACV variation due to FET gate nesting is over-ridden to a user-supplied value (0.005um in this example). FETs with the instance parameter plnest = 1 become shorter and instances with plnest= 0 become longer, each by pc_nest_add/2. Other ACV effects are disabled. Useful for simulations when hardware information is available.</p>
fet_dop_mis	0	
fet_geo_mis	1	
pc_nest	2	
pc_orient	0	
pc_dist	0	
rx_dist	0	
pc_nest_add	+0.005e-6	
corner option	tt	
cor_*	-3 to +3	

3.0 NPN Models

3.1 Model Features

The HSPICE and SPECTRE npn subcircuit includes the more advanced VBIC model as the core element which provides built-in support for the following features:

- Parasitic vertical PNP to substrate
- Weak avalanche multiplication (impact ionization)
- Self-heating approximation (dV_{be}/dT)
- Fixed oxide capacitances for the emitter-base and collector-base junctions
- Quasi-saturation modeling
- Improved Early effect modeling (as compared to the standard Gummel-Poon model)

The models have optional switches to turn-off the self-heating and impact ionization effects. By default, these options are active and the model was optimized using these features. If the switches are not enabled, the output characteristics of the model will not accurately represent hardware measurements. The switches may help improve simulation time by allowing the designer to de-activate these options for non-critical devices.

The SPECTRE model also includes breakdown voltage warning parameters which have been set to junction voltage limits, documented in the technology design manual, as follows:

- bv_{be} (B-E breakdown voltage) = nominal BV_{ebo}
- bv_{bc} (B-C breakdown voltage) = nominal BV_{cbo}
- bv_{ce} (C-E breakdown voltage) = nominal BV_{ceo}
- bv_{sub} (Substrate junction breakdown voltage) = minimum BV_{cso}

The following is an example of the warning message that will be generated during simulation if any of these parameter limits are exceeded:

```
Warning from spectre at dc = 10 uA during DC analysis 'xxx'.
xxx.x2.q: The collector-emitter voltage exceeded breakdown voltage.
```

The simulation results are not affected by these warnings, but designers should review the bias conditions of all devices that are identified as violating any of these voltage limits. Note that for the C-E voltage, the nominal (rather than minimum) BV_{ceo} value is used as the default in an effort to avoid unnecessary warnings on all devices. This is due to the fact that most circuit applications do not make use of an open base condition. The designer can also use the include or design.scs file override parameters provided to specify an alternate C-E voltage limit for the High- f_T (HP) and High-Breakdown (HB) devices that may be more suitable for their application.

3.2 Model Limitations and Restrictions

Modeling of the reverse base-emitter junction breakdown is not included in the npn models as it is not supported by the VBIC equations.

The npn models support single stripe emitter geometries only. The models support either a c-b-e-b-c or c-b-e layout for the High- f_T device and c-b-e-b-c layout for the High-Breakdown device as represented in the device library pcells within the design kit environment. The reasons for this limitation are:

- At the high current densities allowed in this technology, center fingers of a multi-emitter device would be at a higher temperature than the outer fingers. With the exponential dependence of the collector current, the center fingers would conduct more current and could cause reliability concerns (or catastrophic failure in extreme cases).
- The difference in collector resistance between emitters at various distances from the collector can also lead to significant bias differences between inner and outer fingers.

3.3 Device Parameter Reference Tables

The following tables provide a quick reference for designers to assess the device parasitics associated with several sample device sizes, as listed. These geometries contain examples across varying length and, for the High- f_T device, compare c-b-e-b-c with c-b-e configurations.

The first table reflects the High- f_T device parameters:

Table 28. High- f_T (HP) NPN Device Parameter Comparison (c-b-e-b-c and c-b-e configurations)						
Device Parameter	Drawn Emitter Dimensions (μm)					
	.12 x .52 c-b-e-b-c	.12 x .52 c-b-e	.12 x 3 c-b-e-b-c	.12 x 3 c-b-e	.12 x 12 c-b-e-b-c	.12 x 12 c-b-e
Extrinsic Re (ohms)	37.9	37.9	4.93	4.93	1.53	1.53
Extrinsic Rb (ohms)	236.0	236.0	52.3	52.3	13.7	16.2
Intrinsic Rb (ohms)	125.3	125.3	21.1	21.1	5.80	5.80
Extrinsic Rc (ohms)	51.4	77.8	14.7	22.4	4.10	6.25
Intrinsic Rc (ohms)	198.3	198.3	25.8	25.8	6.20	6.20
BE Intrinsic Cap (fF)	0.673	0.673	4.44	4.44	18.1	18.1
BE Oxide Cap (fF)	0.842	0.842	4.67	4.67	18.6	18.6
BC Extrinsic Cap (fF)	0.144	0.144	0.411	0.411	1.38	1.38
BC Intrinsic Cap (fF)	0.549	0.549	2.49	2.49	9.52	9.52
BC Oxide Cap (fF)	1.064	0.730	2.80	1.917	9.11	6.22
CS Intrinsic Cap (fF)	0.075	0.047	0.197	0.124	0.642	0.403
Peak f_T I_C (mA)	0.75	0.69	4.32	3.96	17.28	15.84

This second table reflects the High-Breakdown device parameters:

<i>Table 29. High-Breakdown (HB) NPN Device Parameter Comparison</i>					
Device Parameter	Drawn Emitter Dimensions (μm)				
	.12 x .52 c-b-e-b-c	.12 x 1 c-b-e-b-c	.12 x 2.5 c-b-e-b-c	.12 x 5 c-b-e-b-c	.12 x 10 c-b-e-b-c
Extrinsic Re (ohms)	37.9	16.5	5.97	2.90	1.53
Extrinsic Rb (ohms)	286.9	170.7	75.3	39.0	19.9
Intrinsic Rb (ohms)	125.3	64.5	25.3	12.57	6.54
Extrinsic Rc (ohms)	581.3	391.7	194.1	105.5	55.2
Intrinsic Rc (ohms)	7932	3457	1251	606	299
BE Intrinsic Cap (fF)	0.540	1.144	3.03	6.18	12.5
BE Oxide Cap (fF)	0.842	1.583	3.90	7.75	15.5
BC Extrinsic Cap (fF)	0.072	0.103	0.197	0.356	0.672
BC Intrinsic Cap (aF)	0.0006	0.001	0.0022	0.0043	0.0084
BC Oxide Cap (fF)	1.117	1.435	2.43	4.09	7.41
CS Intrinsic Cap (fF)	0.075	0.098	0.172	0.296	0.543
Peak f_T I_C (mA)	0.0905	0.174	0.435	0.87	1.74

3.4 Device Mis-Match Reference Tables

The following tables provide a comparison of adjacent device Vbe and Beta mis-match for a select set of emitter sizes. The tables also show hardware data results used to set the mis-match scaling in the models.

The data results are based on a sample of 28 sites from 19 wafers from 4 standard process technology hardware lots. The mis-match results, as quoted in the table and used to set the model mis-match, are based on the three sigma values as extrapolated on a normal probability plot. Forced current is approximately $0.1 \cdot I_{peak}$ and I_{peak}

Note that the general trend of the models is to predict a slightly higher mis-match than the calculated data results. The models have been set to be conservative in this manner due to the relatively small sample size of data available, as reflected in some of the larger sigmas observed in the data. Also note that there is no bias dependence associated with the Beta mis-match as there is with the Vbe mis-match.

Table 30. NPN Adjacent Device Vbe Mis-Match			
Emitter Dimensions (W x L x #stripes)	I _{bias}	Model Vbe Mis-match	Data Mis-Match
0.12 μ m x 0.52 μ m x 1	78 μ A	12.9 mV	12.1 mV
	780 μ A	43.8 mV	40.5 mV
0.12 μ m x 0.75 μ m x 1	112 μ A	9.1 mV	10.1 mV
	1.12 mA	33.9 mV	41.7 mV
0.12 μ m x 1 μ m x 1	150 μ A	7.5 mV	9.1 mV
	1.5 mA	31.9mV	16.2 mV
0.12 μ m x 3 μ m x 1	450 μ A	4.87 mV	5.6 mV
	4.5 mA	24.6 mV	8.1 mV
0.12 μ m x 6 μ m x 1	900 μ A	4.6 mV	4.5 mV
	9.5 mA	23.4 mV	7.7 mV
0.12 μ m x 12 μ m x 1	1.8 mA	3.1 mV	3.7 mV
	18 mA	11.4 mV	6.3 mV
0.12 μ m x 18 μ m x 1	2.7 mA	2.6 mV	3.2 mV
	27 mA	8.4 mV	6.0 mV

Table 31. NPN Adjacent Device Beta Mis-Match		
Emitter Dimensions (W x L x #stripes)	Model Beta Mis-match	Data Mis-Match
0.12 μ m x 0.52 μ m x 1	54%	47%
0.12 μ m x 0.75 μ m x 1	42.6%	39%
0.12 μ m x 1 μ m x 1	33.6%	32%
0.12 μ m x 3 μ m x 1	19.8%	25%
0.12 μ m x 6 μ m x 1	14.9%	18.6%
0.12 μ m x 12 μ m x 1	12.3%	12.6%
0.12 μ m x 18 μ m x 1	11.6%	12%

3.5 DC Correlation Plots

The following series of plots compares the DC characteristics of the npn model with measurements from qualification hardware. As the model supports a range of emitter lengths, the plots show the model correlation for a few select device sizes.

Table 32. NPN DC Correlation Plots

Device Emitter Size	High- f_T (HP) c-b-e-b-c	High- f_T (HP) c-b-e	High-Breakdown (HB) c-b-e-b-c
Width = 0.12 μ m, Length = 0.52 μ m	Fig 17	Fig 24	Fig 31
Width = 0.12 μ m, Length = 0.75 μ m	Fig 18	Fig 25	data not available
Width = 0.12 μ m, Length = 1.0 μ m	Fig 19	Fig 26	Fig 32
Width = 0.12 μ m, Length = 2.5 μ m	data not available	data not available	Fig 33
Width = 0.12 μ m, Length = 3.0 μ m	Fig 20	Fig 27	data not available
Width = 0.12 μ m, Length = 5.0 μ m	data not available	data not available	Fig 34
Width = 0.12 μ m, Length = 6.0 μ m	Fig 21	Fig 28	data not available
Width = 0.12 μ m, Length = 10 μ m	data not available	data not available	Fig 35
Width = 0.12 μ m, Length = 12 μ m	Fig 22	Fig 29	data not available
Width = 0.12 μ m, Length = 18 μ m	Fig 23	Fig 30	data not available
Note: DC Correlation Plots reflect the SPECTRE VBIC model characteristics.			

Each of the figures contains the following:

- The plots in the top row of the figure are generated from forward (V_{be} sweep, $V_{cb}=0V$) and reverse (V_{bc} sweep, $V_{eb}=0V$) gummel measurements. The left and right plots depict the node currents vs voltage. The center plot shows the forward and reverse current gain (beta) vs current. Note that the apparent leakage in the base and collector currents shown in the forward gummel plots for the High-Breakdown device is a measurement anomaly due to the fact these data were measured using an S-Parameter measurement system. This also affects the low current roll off in the forward current gain.
- The remaining plots in the figure are generated from a sweep of V_{ce} for a series of fixed base currents which are defined on each page for the respective device size. The left plot in the middle row shows collector current vs V_{ce} . Impact ionization effects can be observed in both model and data curves. The middle plot in this row depicts the effective Early voltage (I_C/g_0). The region from low-to-mid V_{ce} biases illustrates the quasi-saturation effects in the device. The plots in the bottom row show base-emitter voltage vs V_{ce} and the substrate current at low V_{ce} (saturation region). The decrease in V_{be} with increasing V_{ce} , prior to the onset of breakdown effects, is due to the self-heating.

In addition to the nominal temperature (25C) plots, DC characteristics vs temperature are shown for the following devices:

<i>Table 33. NPN DC Temperature Plots</i>			
Device Emitter Size	High- f_T (HP) c-b-e-b-c	High- f_T (HP) c-b-e	High-Breakdown (HB) c-b-e-b-c
Width = 0.12 μ m, Length = 2.5 μ m	data not available	data not available	Fig 38
Width = 0.12 μ m, Length = 3.0 μ m	Fig 36	Fig 37	data not available
Note: DC Temperature Plots reflect the SPECTRE VBIC model characteristics.			

Note: All of the DC simulation curves were created with some adjustments to the skew file parameters, as noted in each figure, to center the model near the mean of the measured data.

BiCMOS8HP "High- f_T NPN" – Typical Characteristics (25C)

Emitter Size: $0.12\mu\text{m} \times 0.52\mu\text{m} \times 1$, Topology: CBEBC

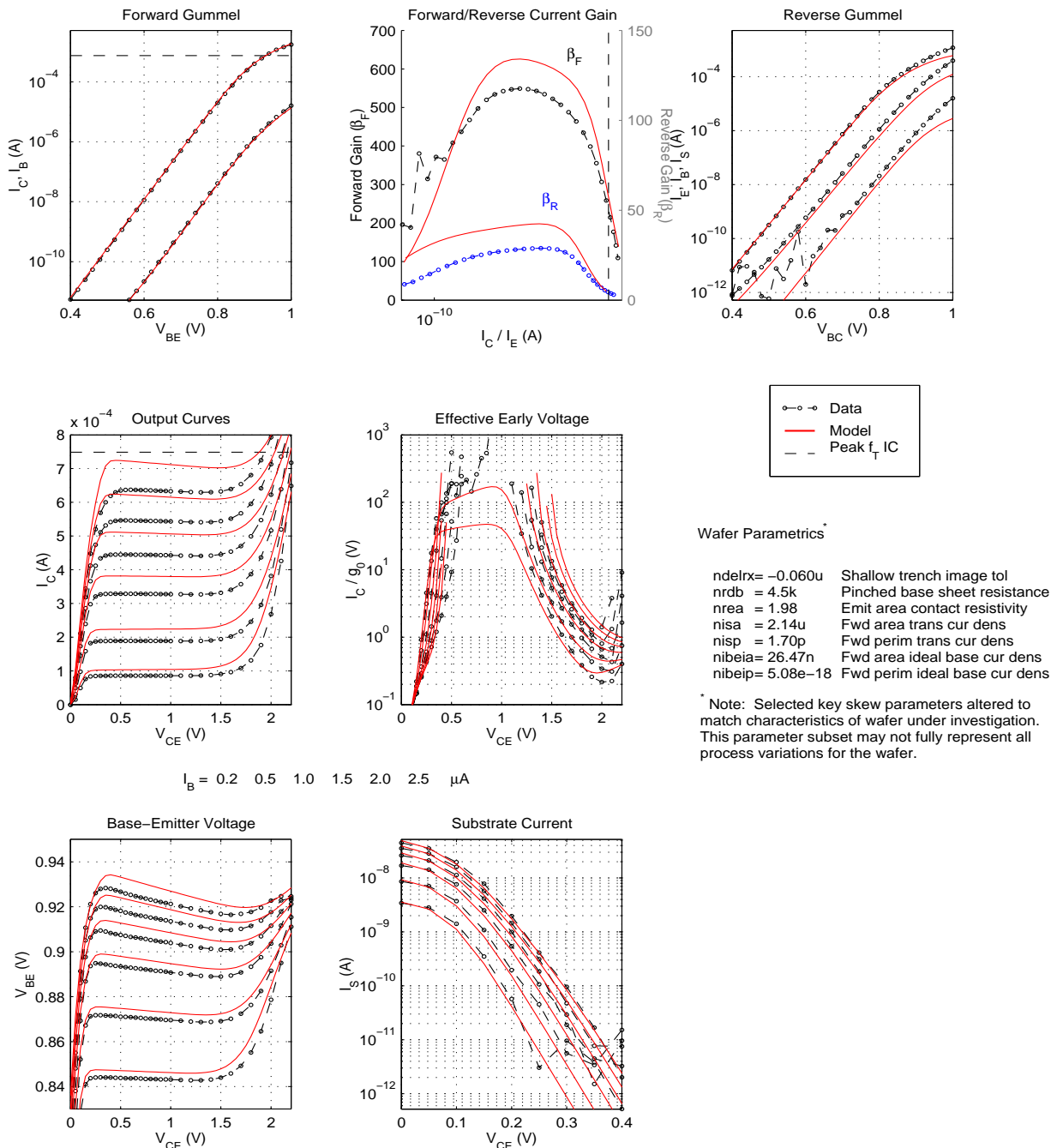


Figure 17. HP NPN DC Characteristics for $0.12\mu\text{m} \times 0.52\mu\text{m}$, c-b-e-b-c

BiCMOS8HP "High- f_T NPN" – Typical Characteristics (25C)

Emitter Size: $0.12\text{ }\mu\text{m} \times 0.75\text{ }\mu\text{m} \times 1$, Topology: CBEB

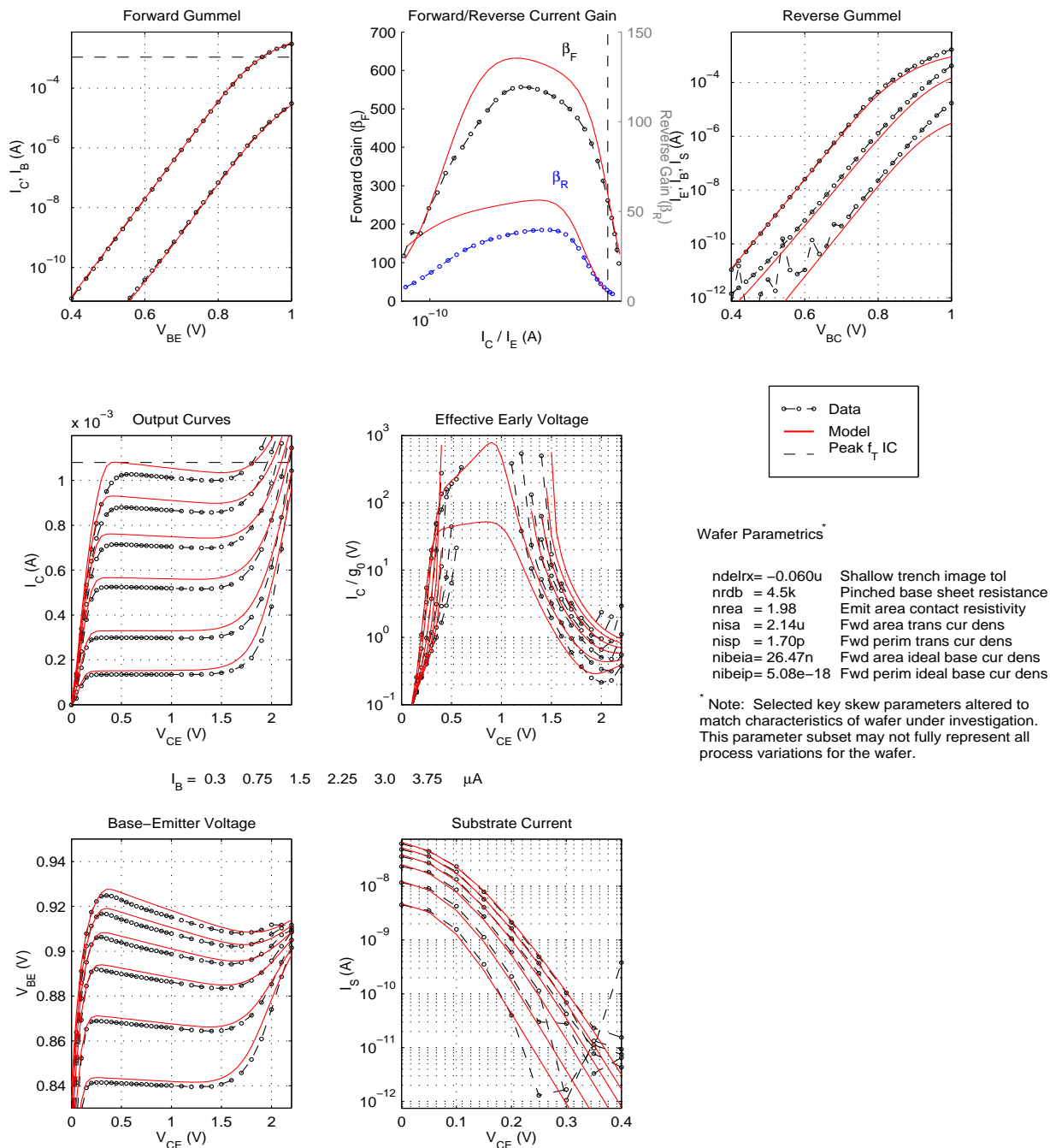


Figure 18. HP NPN DC Characteristics for $0.12\text{ }\mu\text{m} \times 0.75\text{ }\mu\text{m}$, c-b-e-b-c

BiCMOS8HP "High- f_T NPN" – Typical Characteristics (25C)

Emitter Size: $0.12\ \mu\text{m} \times 1.0\ \mu\text{m} \times 1$, Topology: CBECB

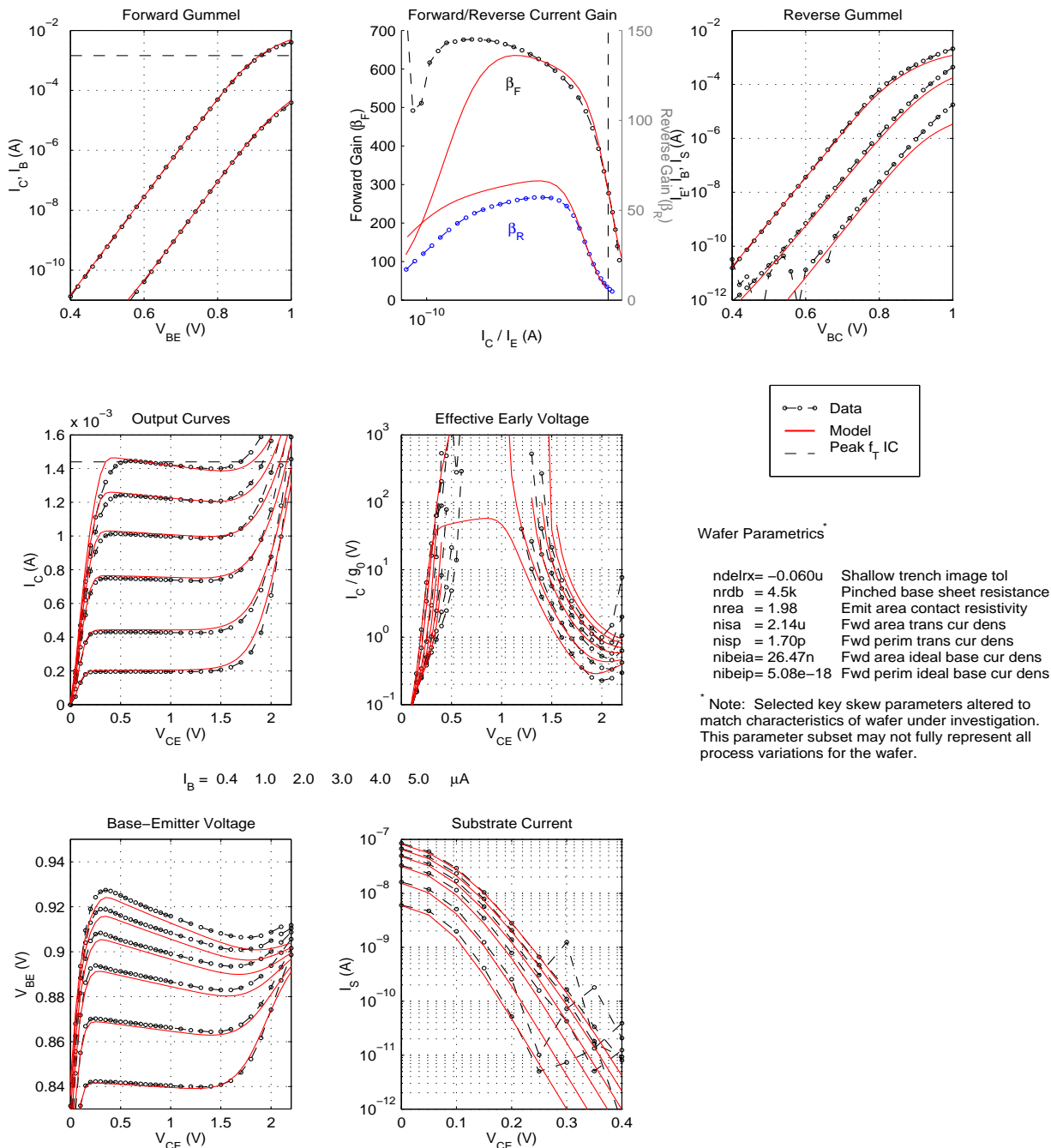


Figure 19. HP NPN DC Characteristics for $0.12\ \mu\text{m} \times 1\ \mu\text{m}$, c-b-e-b-c

BiCMOS8HP "High- f_T NPN" – Typical Characteristics (25C)

Emitter Size: 0.12 μm x 3.0 μm x 1, Topology: CBEBc

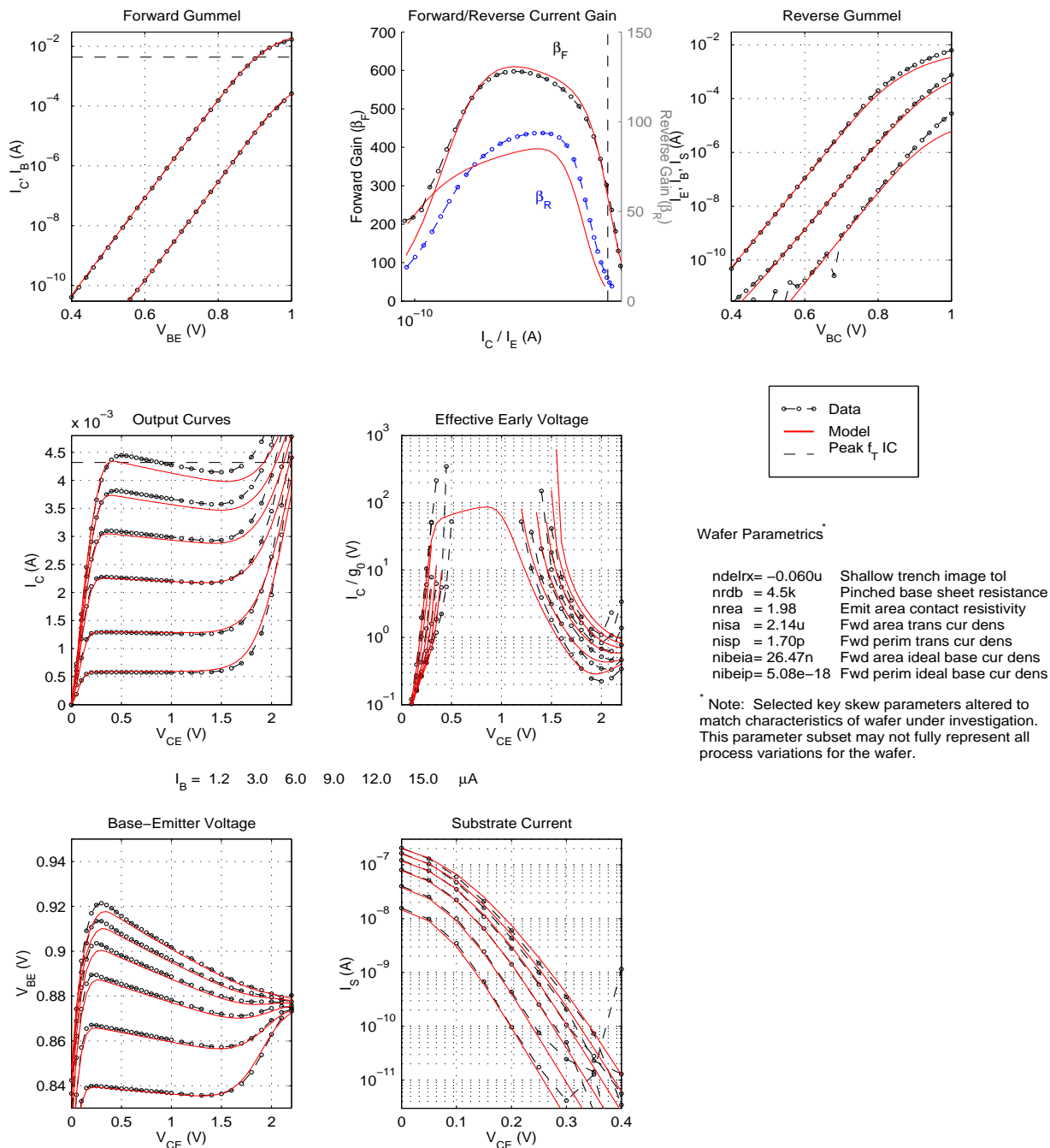


Figure 20. HP NPN DC Characteristics for 0.12 μm x 3 μm , c-b-e-b-c

BiCMOS8HP "High- f_T NPN" – Typical Characteristics (25C)
Emitter Size: $0.12\ \mu\text{m} \times 6.0\ \mu\text{m} \times 1$, Topology: CBECB

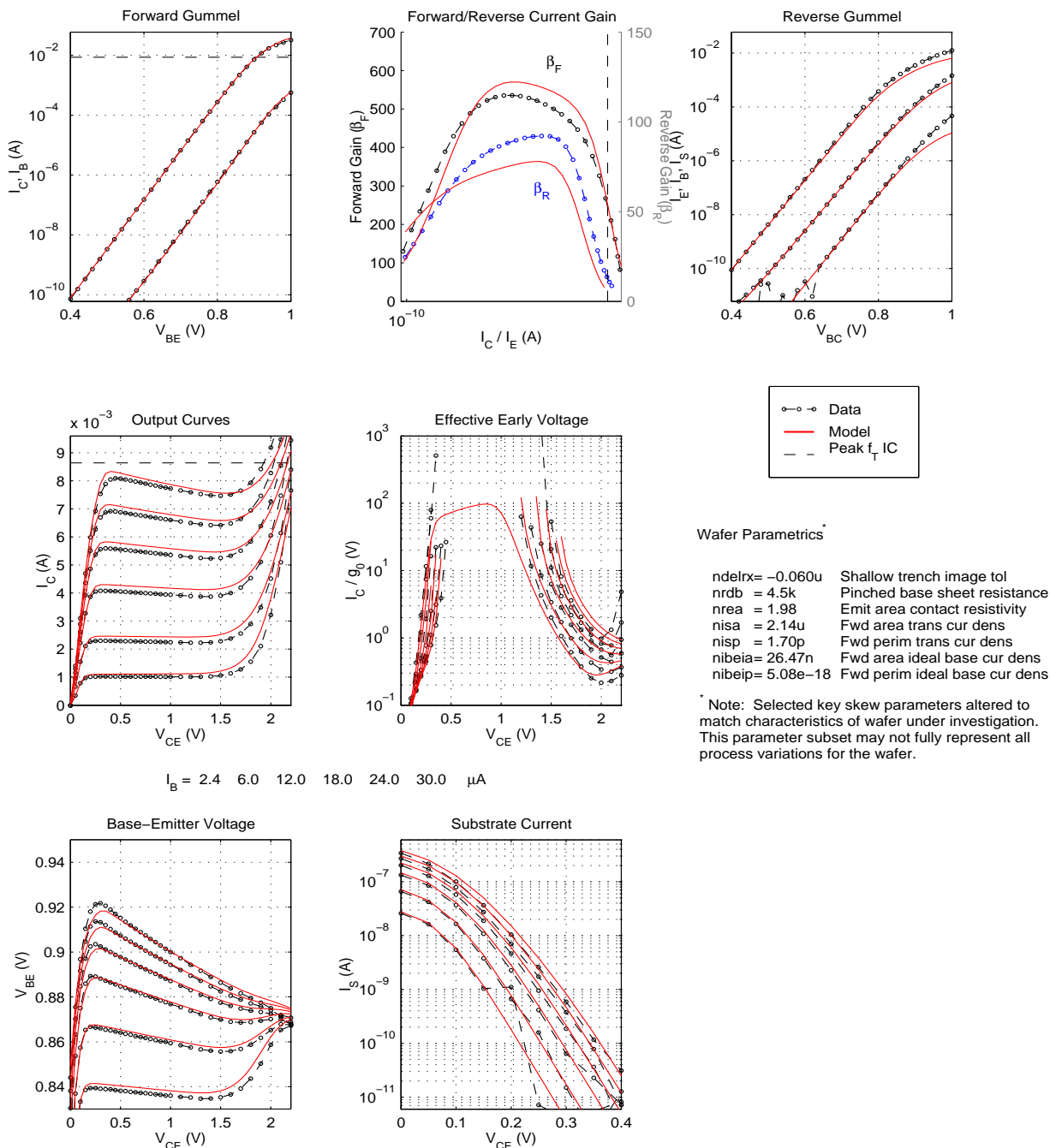


Figure 21. HP NPN DC Characteristics for $0.12\ \mu\text{m} \times 6\ \mu\text{m}$, c-b-e-b-c

BiCMOS8HP "High- f_T NPN" – Typical Characteristics (25C)

Emitter Size: 0.12 μm x 12.0 μm x 1, Topology: CBEB

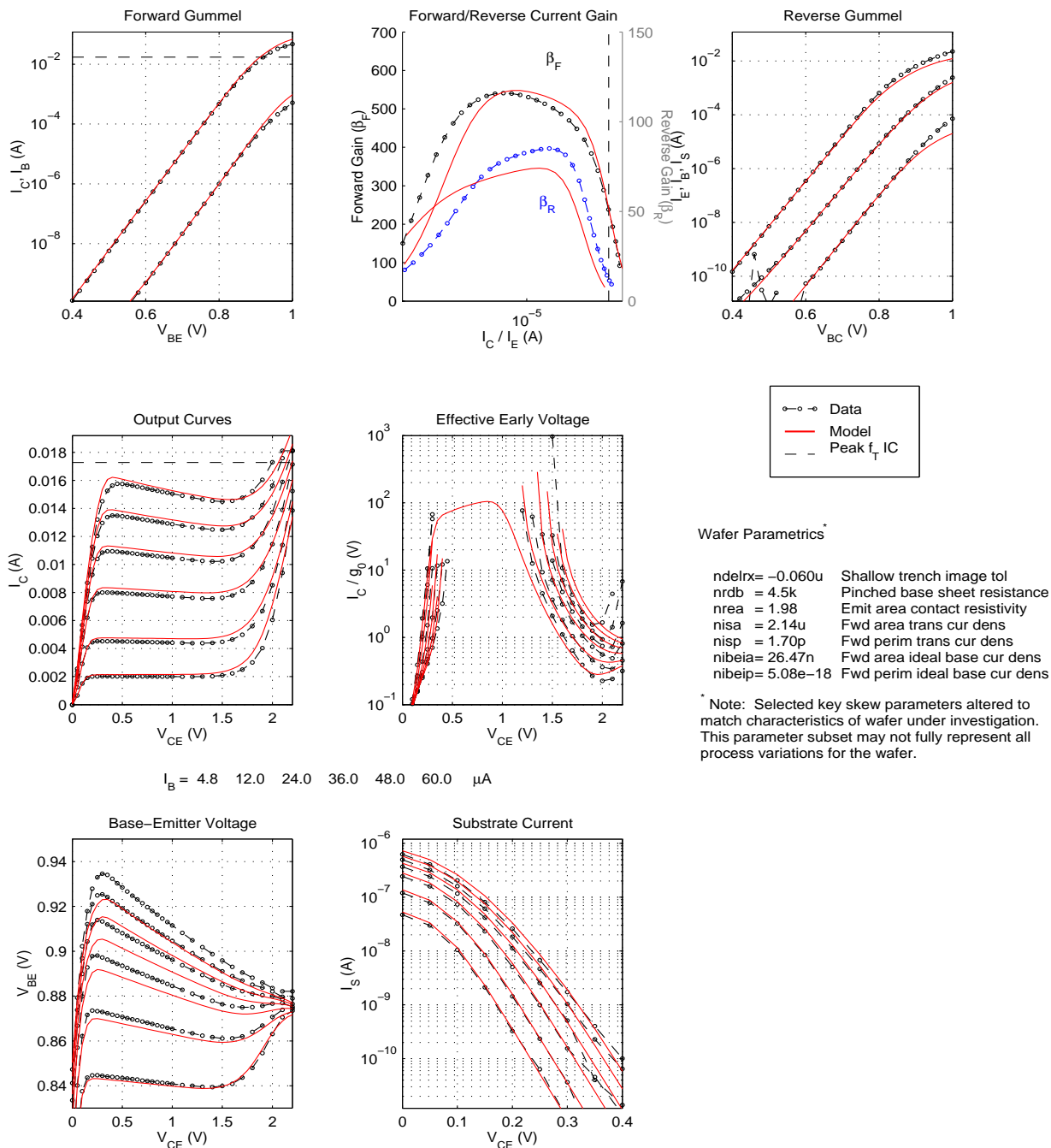


Figure 22. HP NPN DC Characteristics for 0.12 μm x 12 μm , c-b-e-b-c

BiCMOS8HP "High- f_T NPN" – Typical Characteristics (25C)

Emitter Size: $0.12\mu\text{m} \times 18.0\mu\text{m} \times 1$, Topology: CBEBc

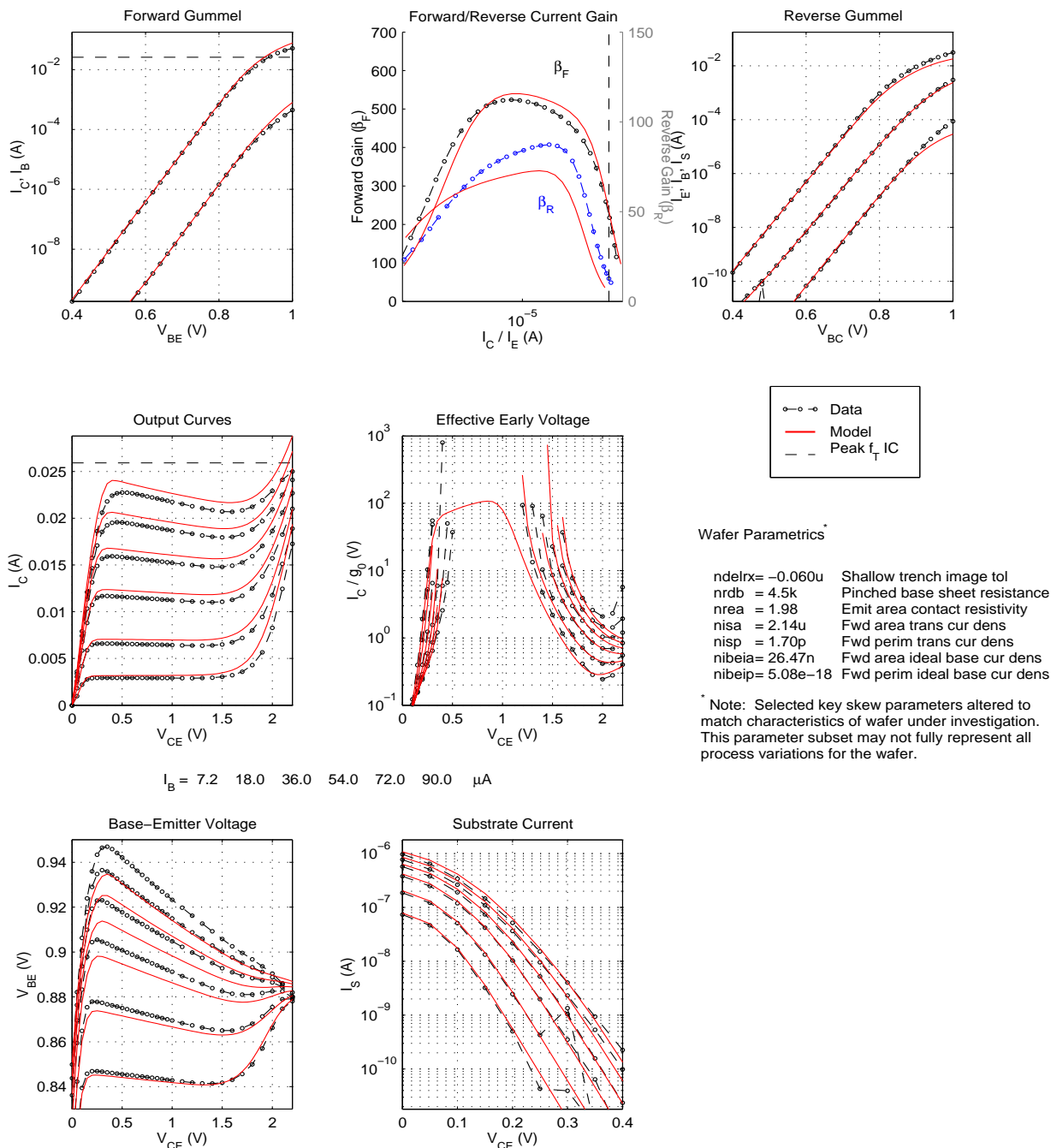


Figure 23. HP NPN DC Characteristics for $0.12\mu\text{m} \times 18\mu\text{m}$, c-b-e-b-c

BiCMOS8HP "High- f_T NPN" – Typical Characteristics (25C)

Emitter Size: $0.12\mu\text{m} \times 0.52\mu\text{m} \times 1$, Topology: CBE

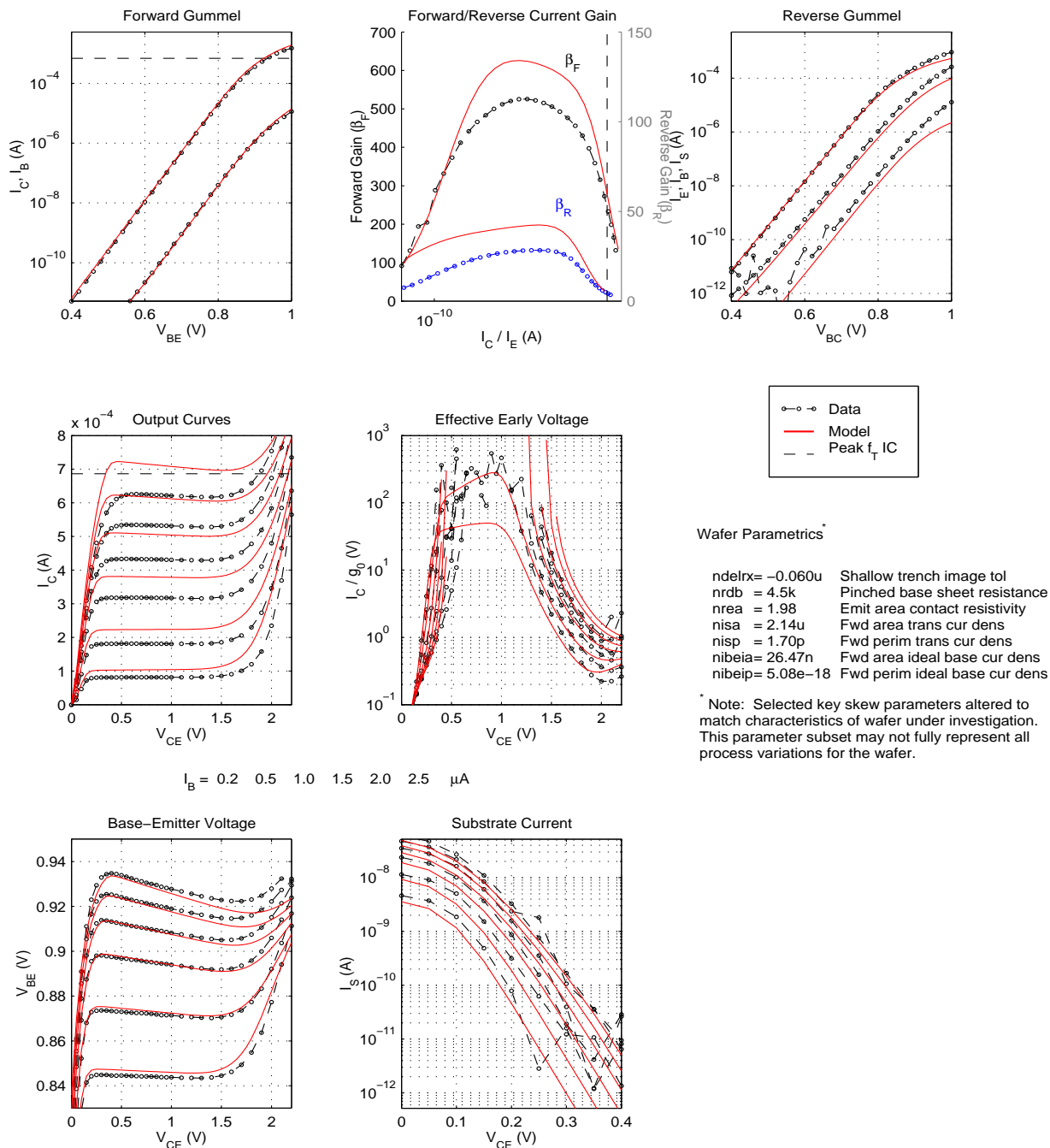


Figure 24. HP NPN DC Characteristics for $0.12\mu\text{m} \times 0.52\mu\text{m}$, c-b-e

BiCMOS8HP "High- f_T NPN" – Typical Characteristics (25C)

Emitter Size: $0.12\mu\text{m} \times 0.75\mu\text{m} \times 1$, Topology: CBE

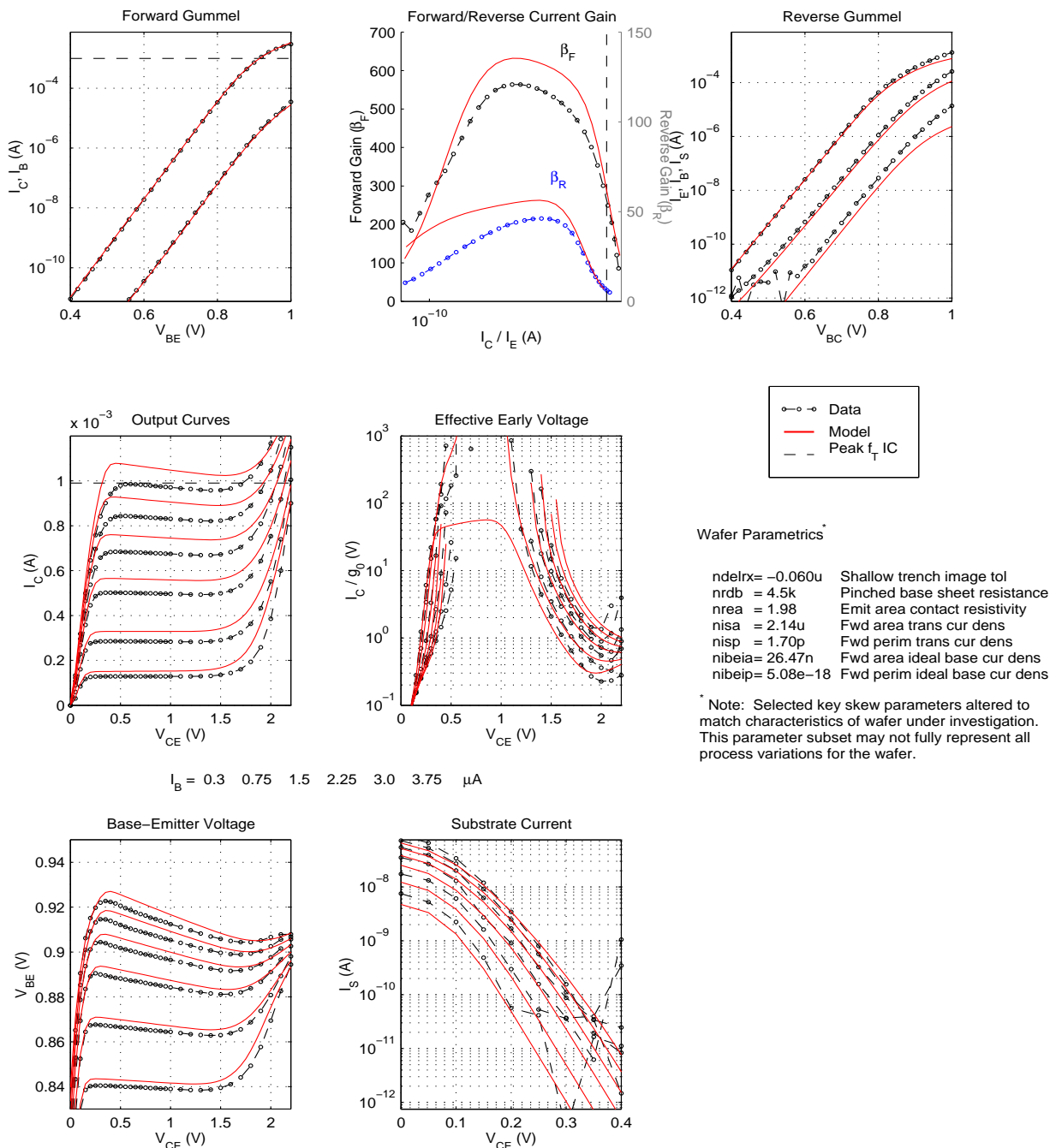


Figure 25. HP NPN DC Characteristics for $0.12\mu\text{m} \times 0.75\mu\text{m}$, c-b-e

BiCMOS8HP "High- f_T NPN" – Typical Characteristics (25C)

Emitter Size: 0.12 μm x 1.0 μm x 1, Topology: CBE

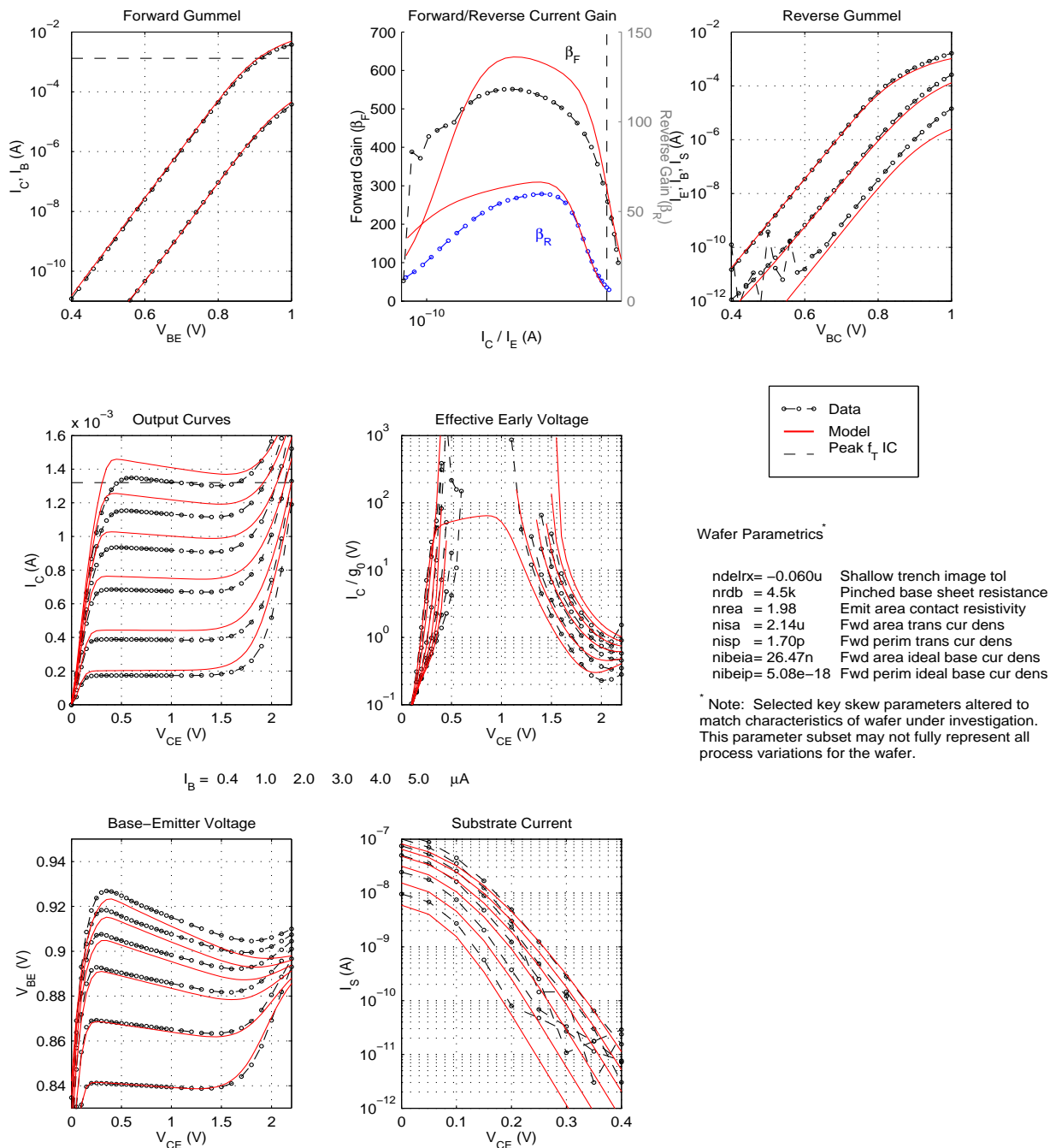


Figure 26. HP NPN DC Characteristics for 0.12 μm x 1 μm , c-b-e

BiCMOS8HP "High- f_T NPN" – Typical Characteristics (25C)

Emitter Size: $0.12\mu\text{m} \times 3.0\mu\text{m} \times 1$, Topology: CBE

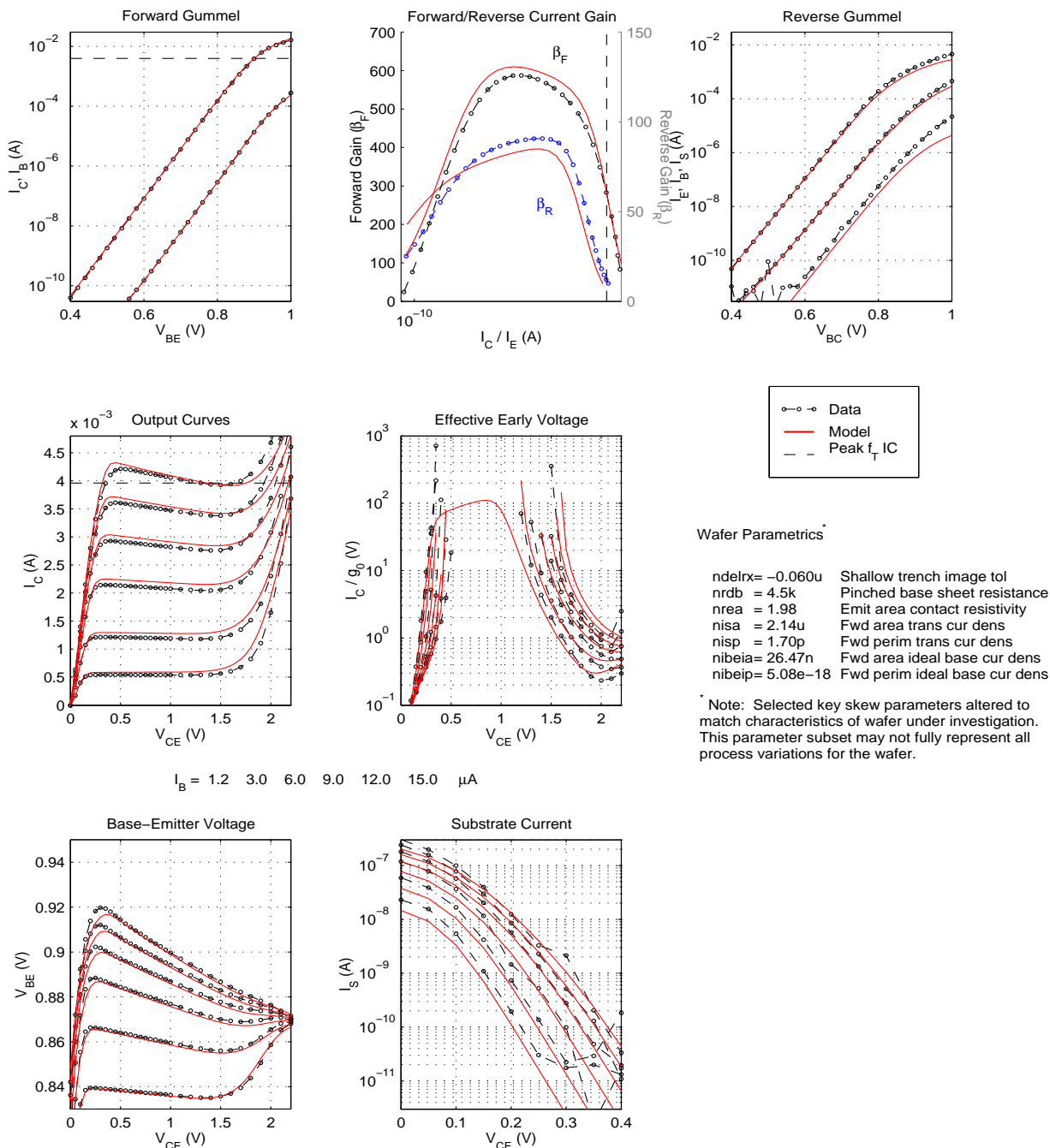


Figure 27. HP NPN DC Characteristics for $0.12\mu\text{m} \times 3\mu\text{m}$, c-b-e

BiCMOS8HP "High- f_T NPN" – Typical Characteristics (25C)

Emitter Size: $0.12\ \mu\text{m} \times 6.0\ \mu\text{m} \times 1$, Topology: CBE

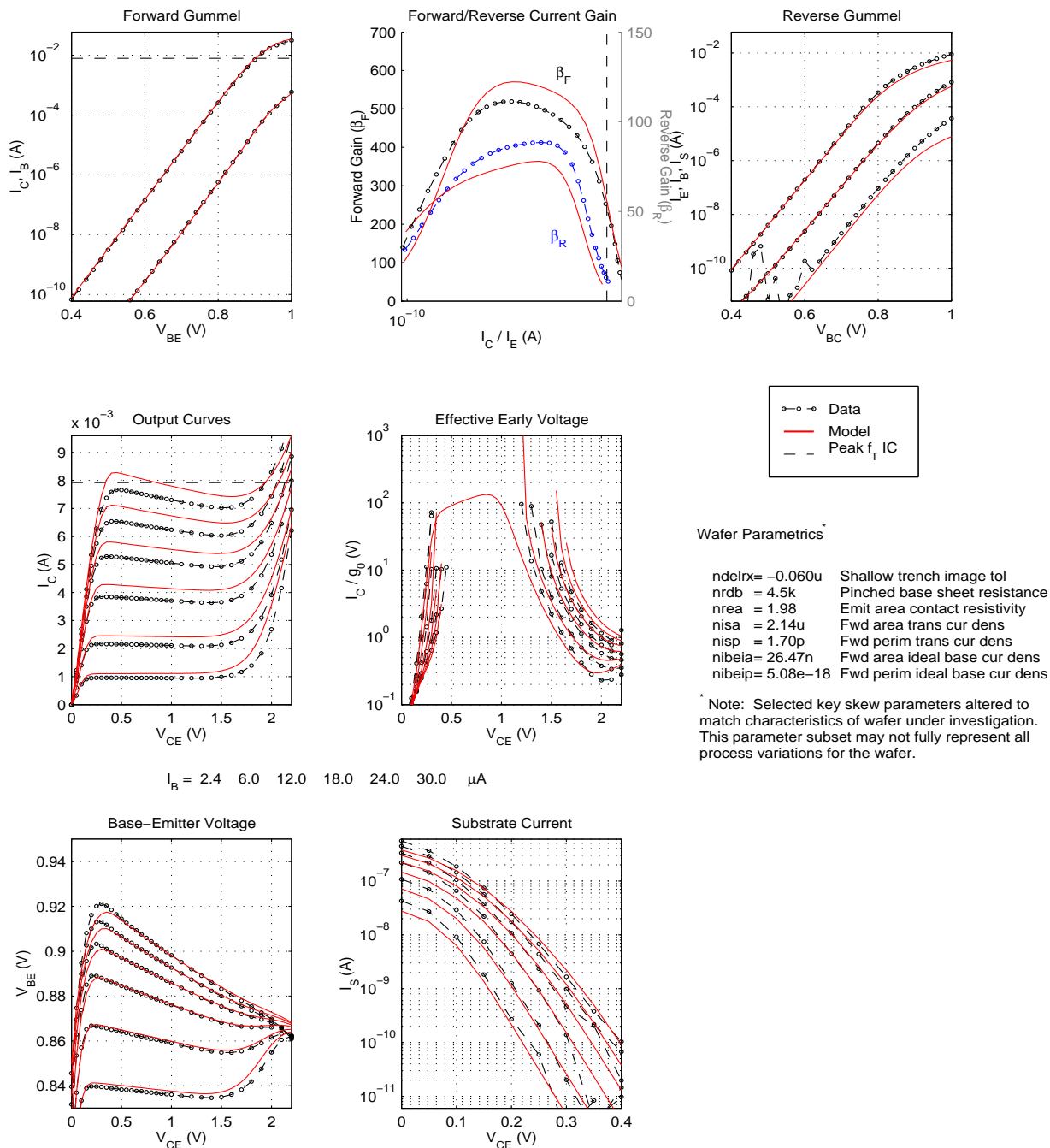


Figure 28. HP NPN DC Characteristics for $0.12\ \mu\text{m} \times 6\ \mu\text{m}$, c-b-e

BiCMOS8HP "High- f_T NPN" – Typical Characteristics (25C)

Emitter Size: $0.12\mu\text{m} \times 12.0\mu\text{m} \times 1$, Topology: CBE

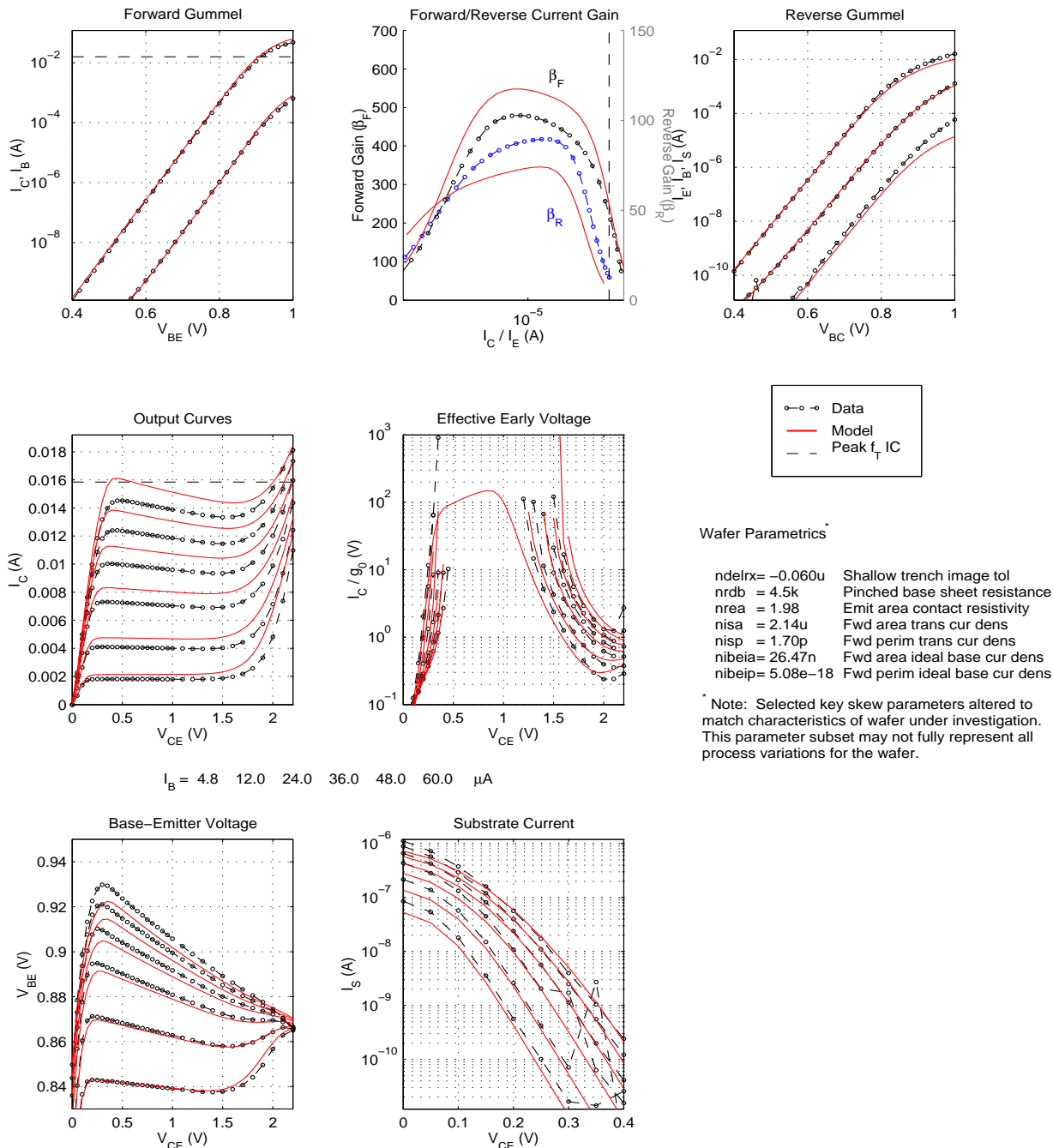


Figure 29. HP NPN DC Characteristics for $0.12\mu\text{m} \times 12\mu\text{m}$, c-b-e

BiCMOS8HP "High- f_T NPN" – Typical Characteristics (25C)

Emitter Size: $0.12\mu\text{m} \times 18.0\mu\text{m} \times 1$, Topology: CBE

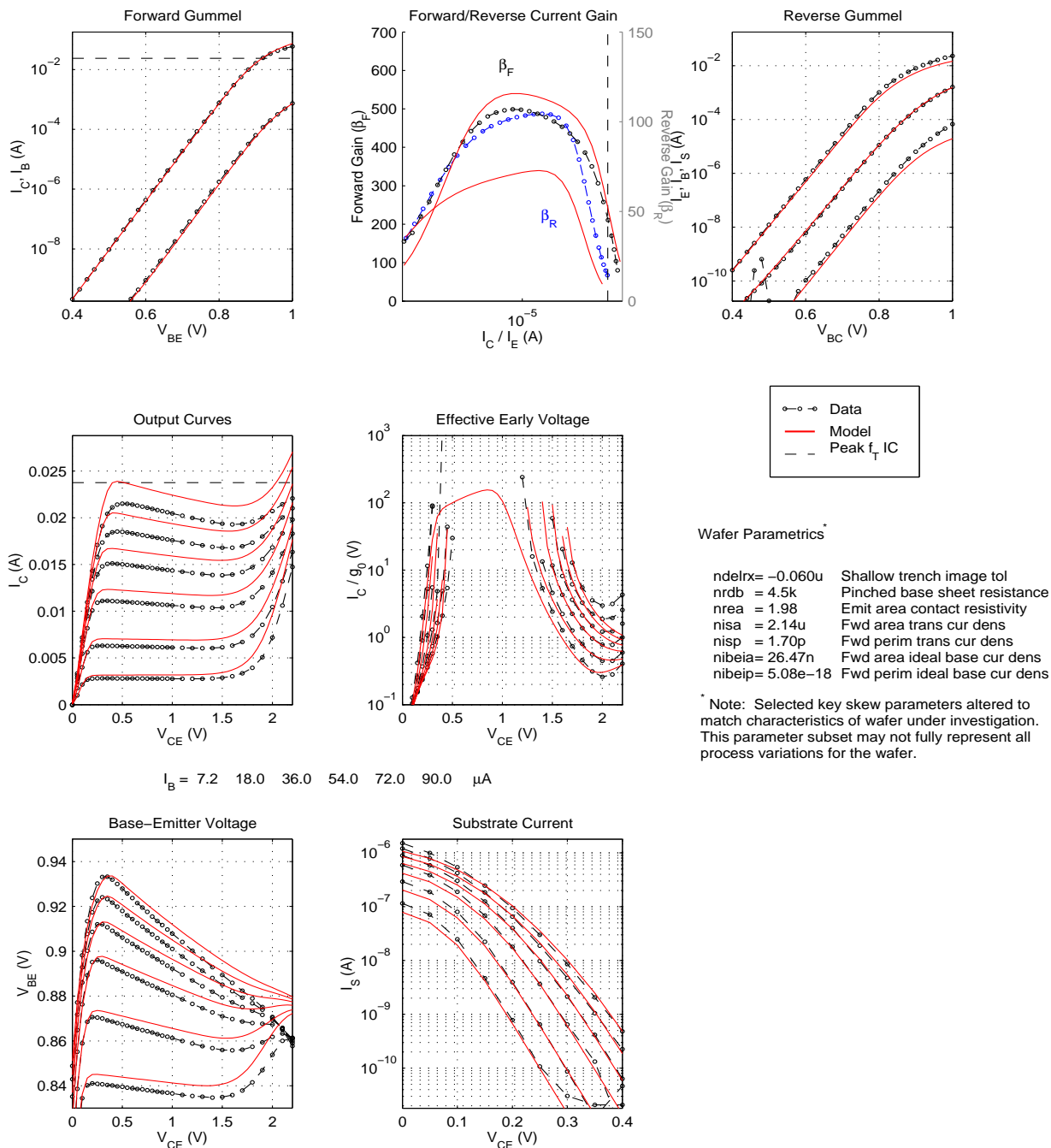


Figure 30. HP NPN DC Characteristics for $0.12\mu\text{m} \times 18\mu\text{m}$, c-b-e

BiCMOS8HP "High-Breakdown NPN" – Typical Characteristics (25°C)
Emitter Size: 0.12 μm x 0.52 μm x 1, Topology: CBEBC

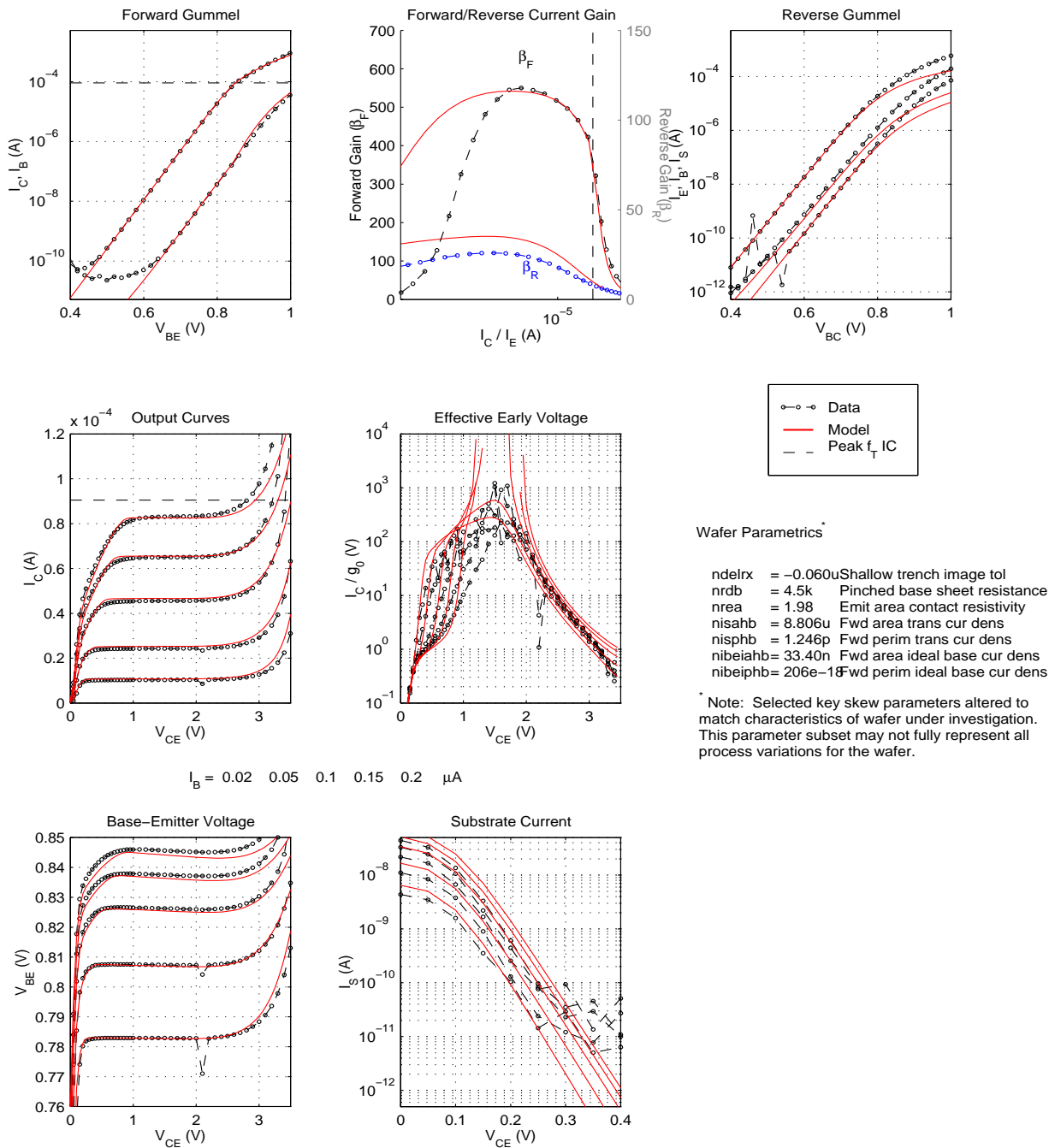


Figure 31. HB NPN DC Characteristics for 0.12 μm x 0.52 μm , c-b-e-b-c

BiCMOS8HP "High-Breakdown NPN" – Typical Characteristics (25°C)
Emitter Size: 0.12 μm x 1.0 μm x 1, Topology: CBEB

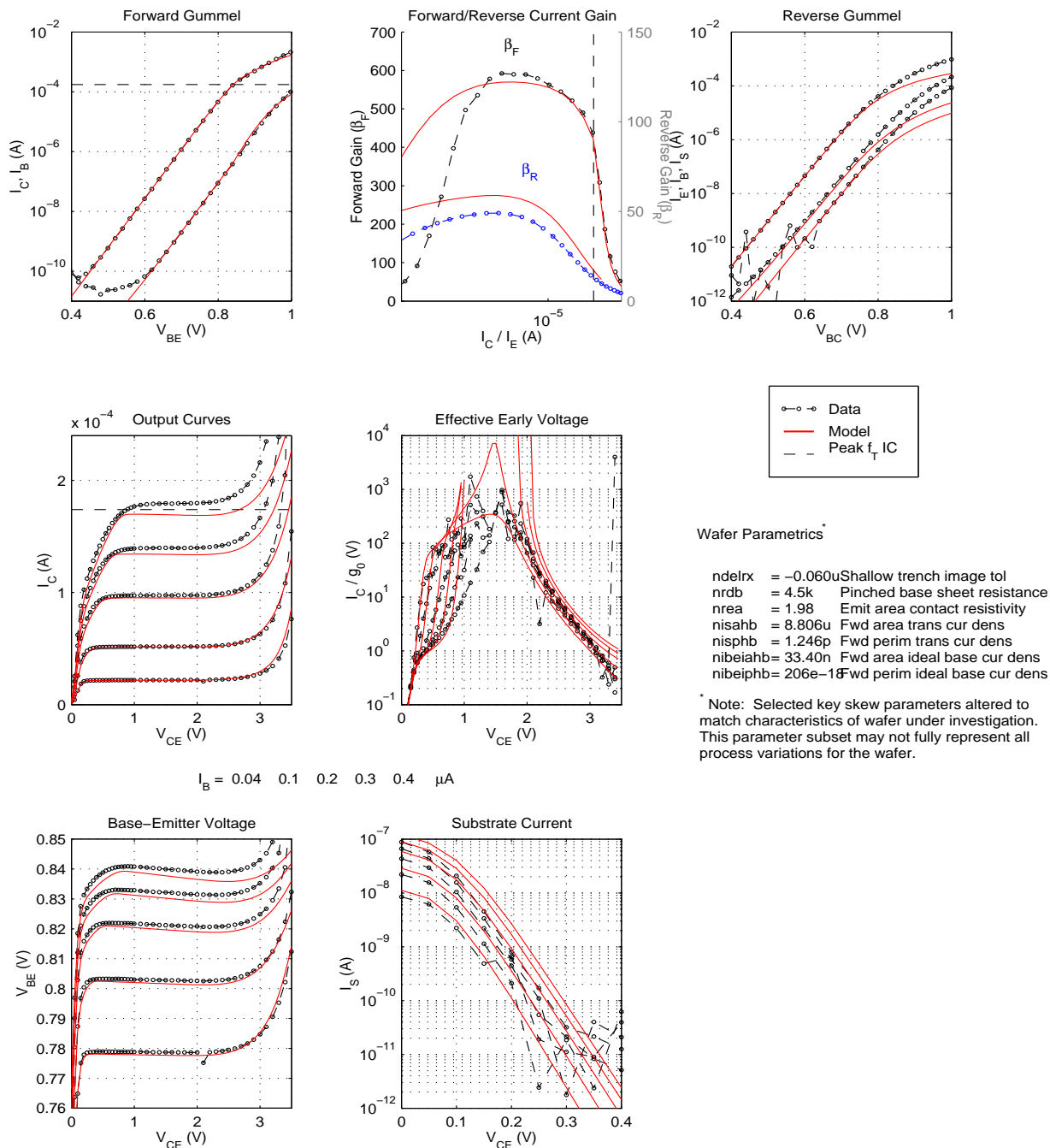


Figure 32. HB NPN DC Characteristics for 0.12 μm x 1 μm , c-b-e-b-c

BiCMOS8HP "High-Breakdown NPN" – Typical Characteristics (25C)
Emitter Size: $0.12\ \mu\text{m} \times 2.5\ \mu\text{m} \times 1$, Topology: CBECB

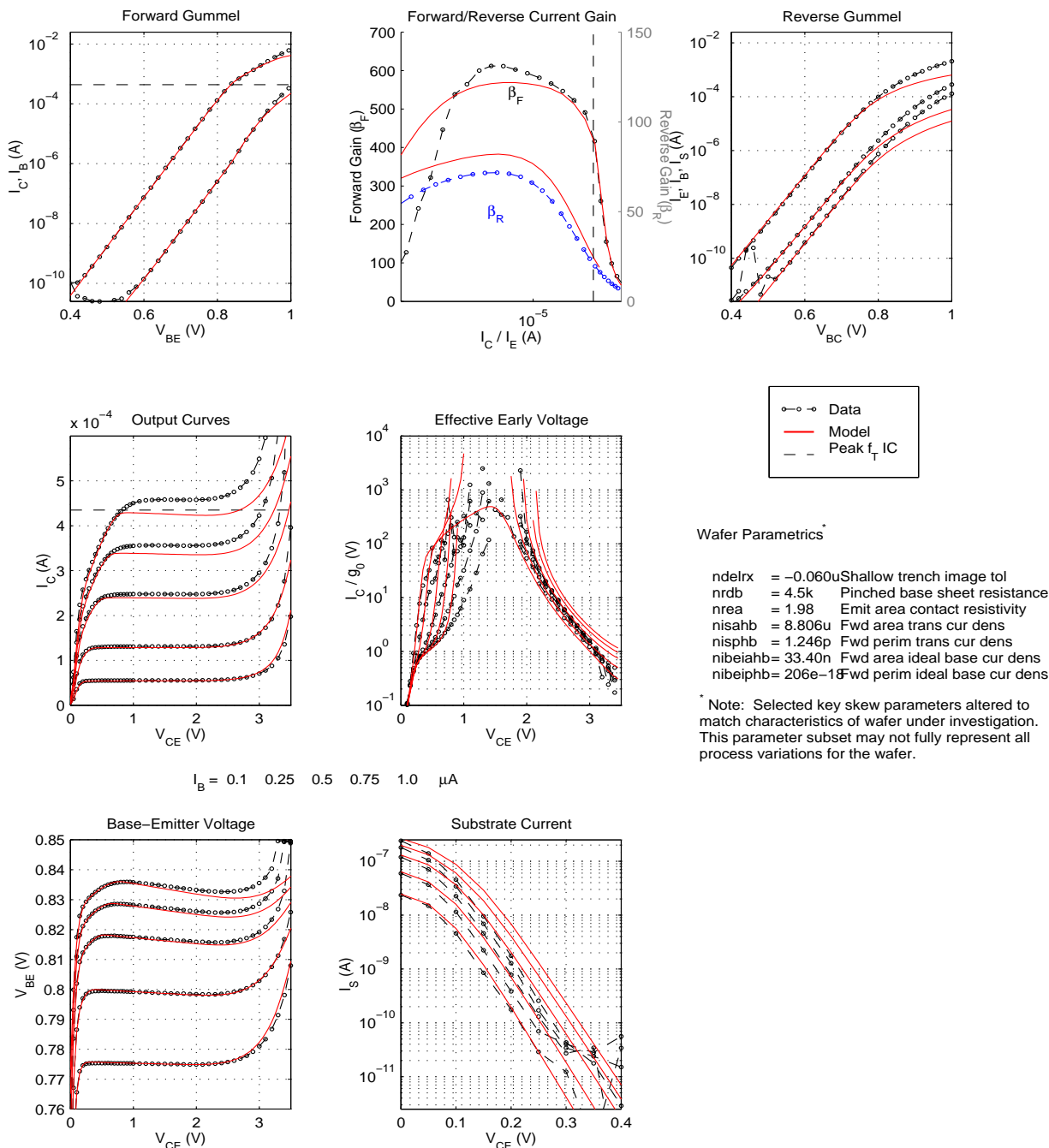


Figure 33. HB NPN DC Characteristics for $0.12\ \mu\text{m} \times 2.5\ \mu\text{m}$, c-b-e-b-c

BiCMOS8HP "High-Breakdown NPN" – Typical Characteristics (25C)
Emitter Size: 0.12 μm x 5.0 μm x 1, Topology: CBEB

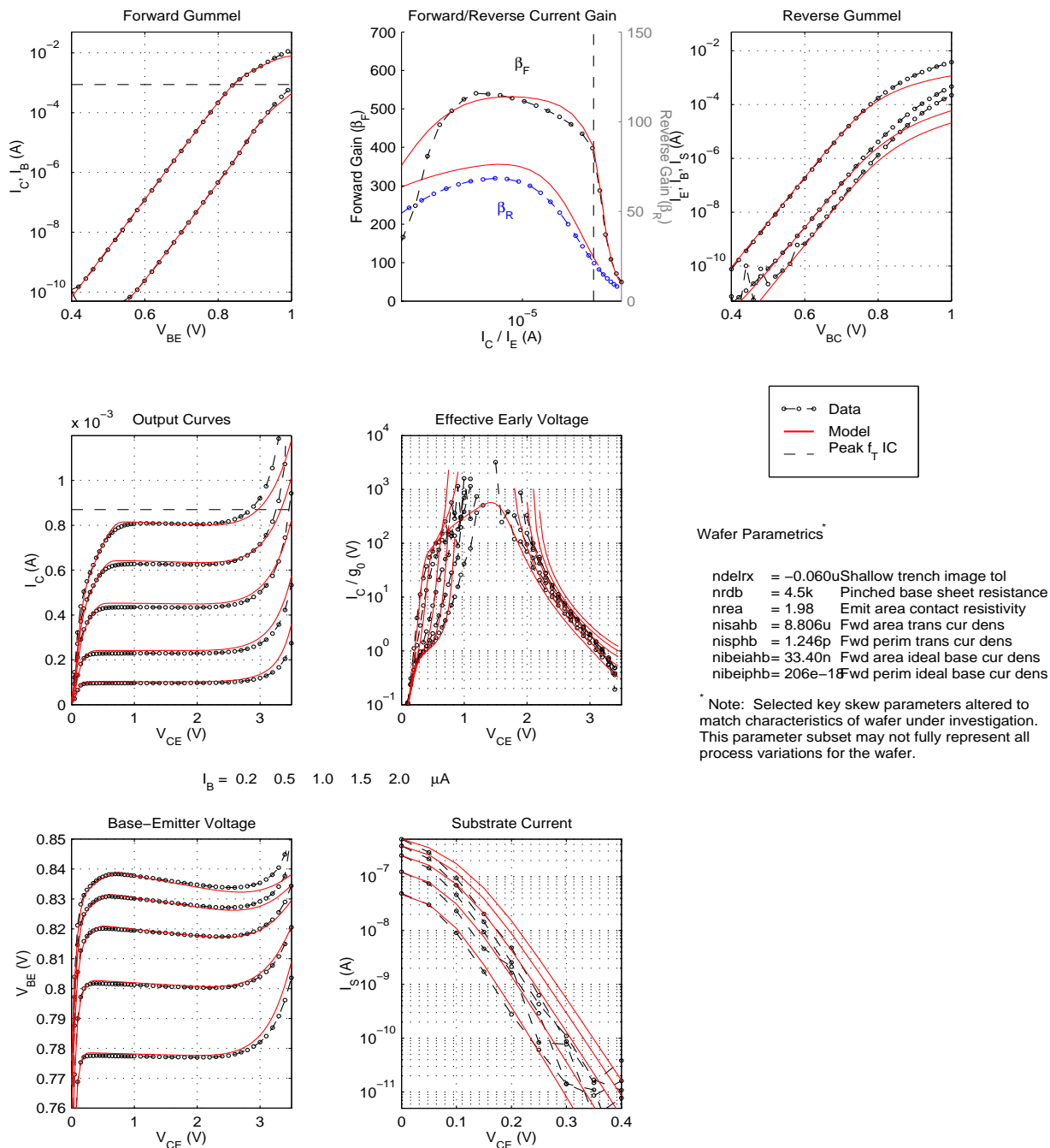


Figure 34. HB NPN DC Characteristics for 0.12 μm x 5 μm , c-b-e-b-c

BiCMOS8HP "High-Breakdown NPN" – Typical Characteristics (25°C)
Emitter Size: 0.12 μm x 10.0 μm x 1, Topology: CBEBc

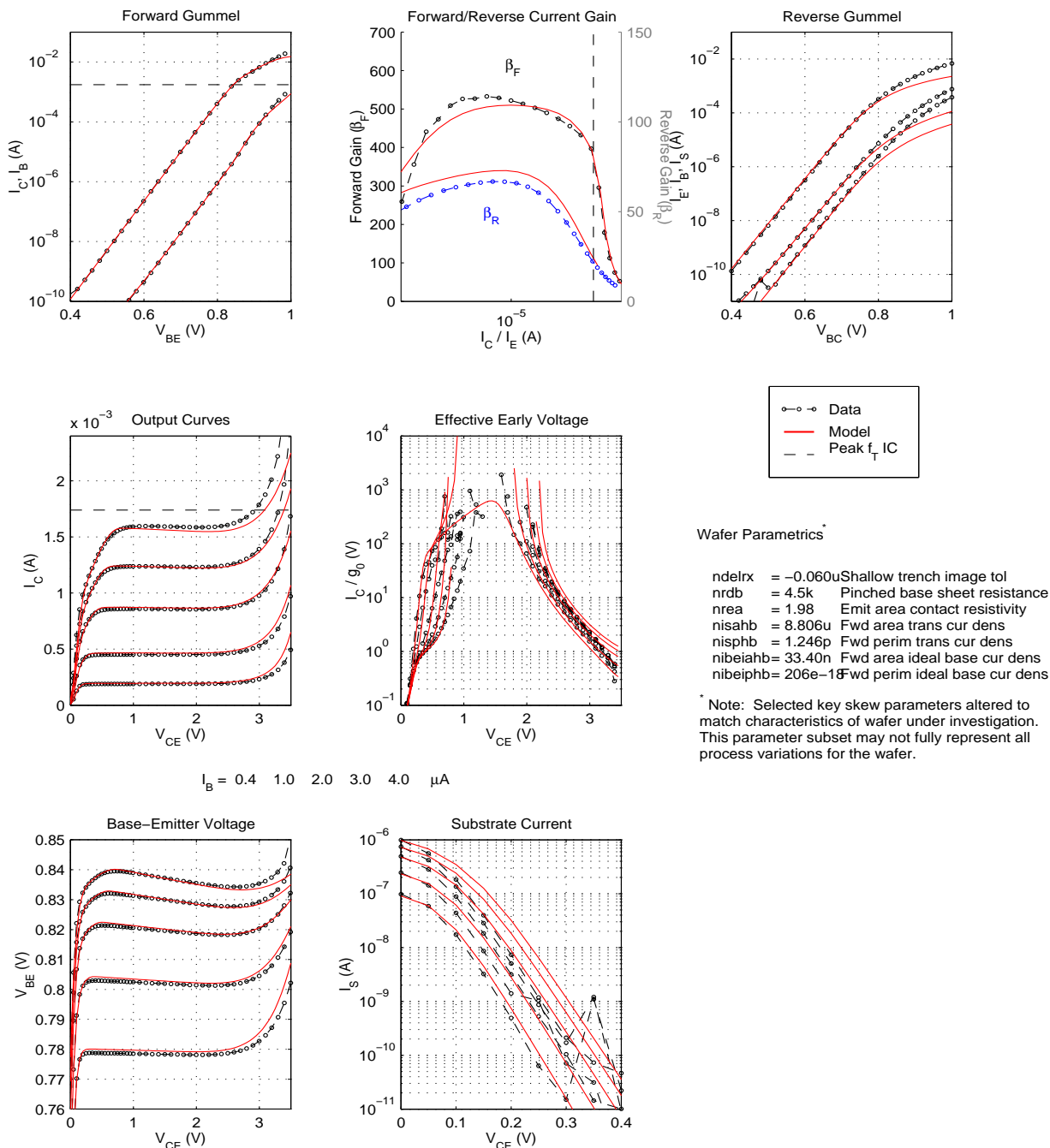
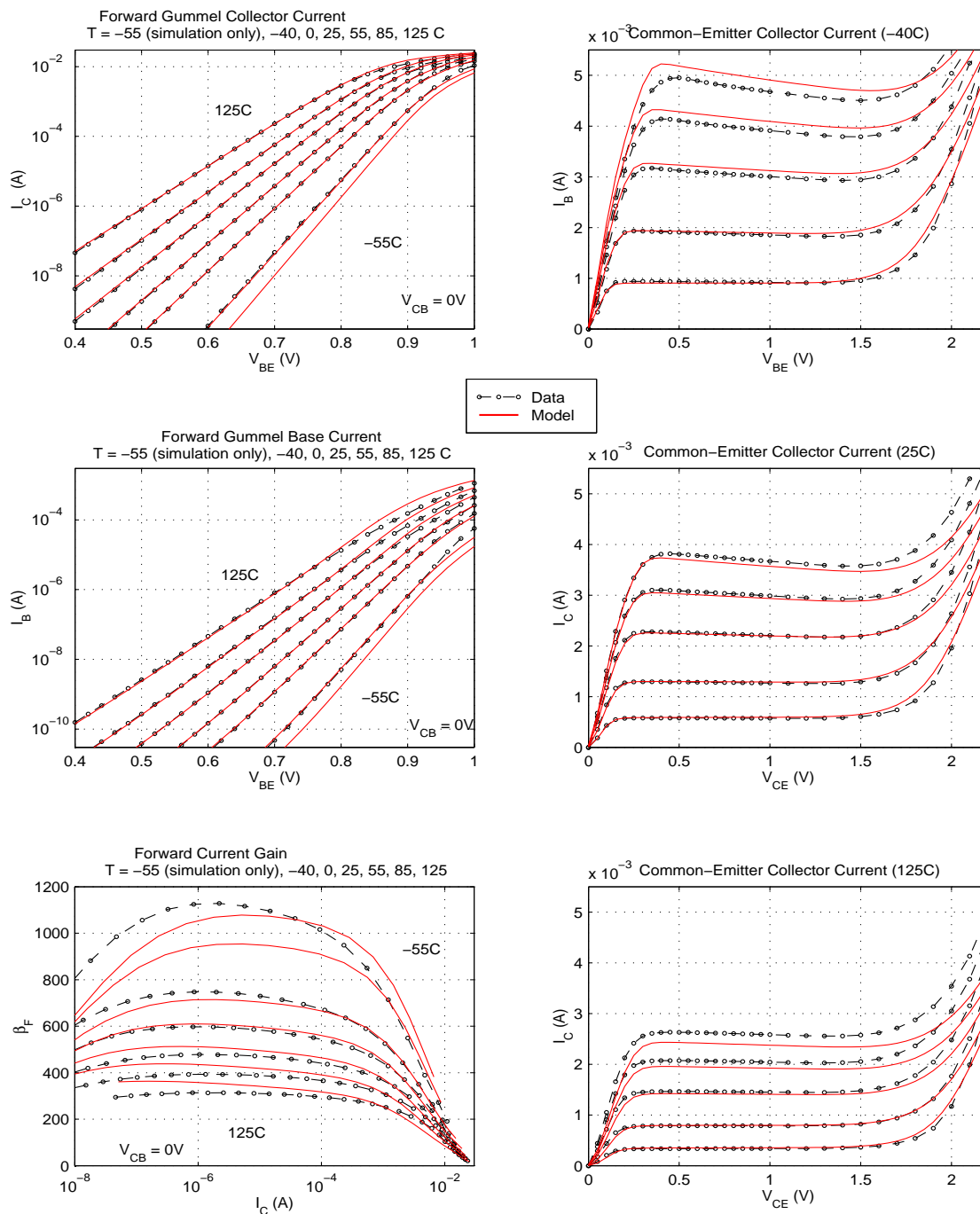


Figure 35. HB NPN DC Characteristics for 0.12 μm x 10 μm , c-b-e-b-c

BiCMOS8HP "High- f_T NPN" – Typical DC Characteristics vs. Temperature

Emitter Size: $0.12\ \mu\text{m} \times 3.0\ \mu\text{m} \times 1$, Topology: CBEBc



Wafer Parametrics: $\text{ndelrx} = -0.060\text{u}$, $\text{nrdb} = 4.5\text{k}$, $\text{nrea} = 1.98$, $\text{nisa} = 2.14\text{u}$, $\text{nisp} = 1.70\text{p}$, $\text{nibeia} = 26.47\text{n}$, $\text{nibeip} = 5.08\text{e-18}$

Figure 36. HP NPN DC vs Temperature for $0.12\ \mu\text{m} \times 3\ \mu\text{m}$, c-b-e-b-c

BiCMOS8HP "High- f_T NPN" – Typical DC Characteristics vs. Temperature

Emitter Size: $0.12\mu\text{m} \times 3.0\mu\text{m} \times 1$, Topology: CBE

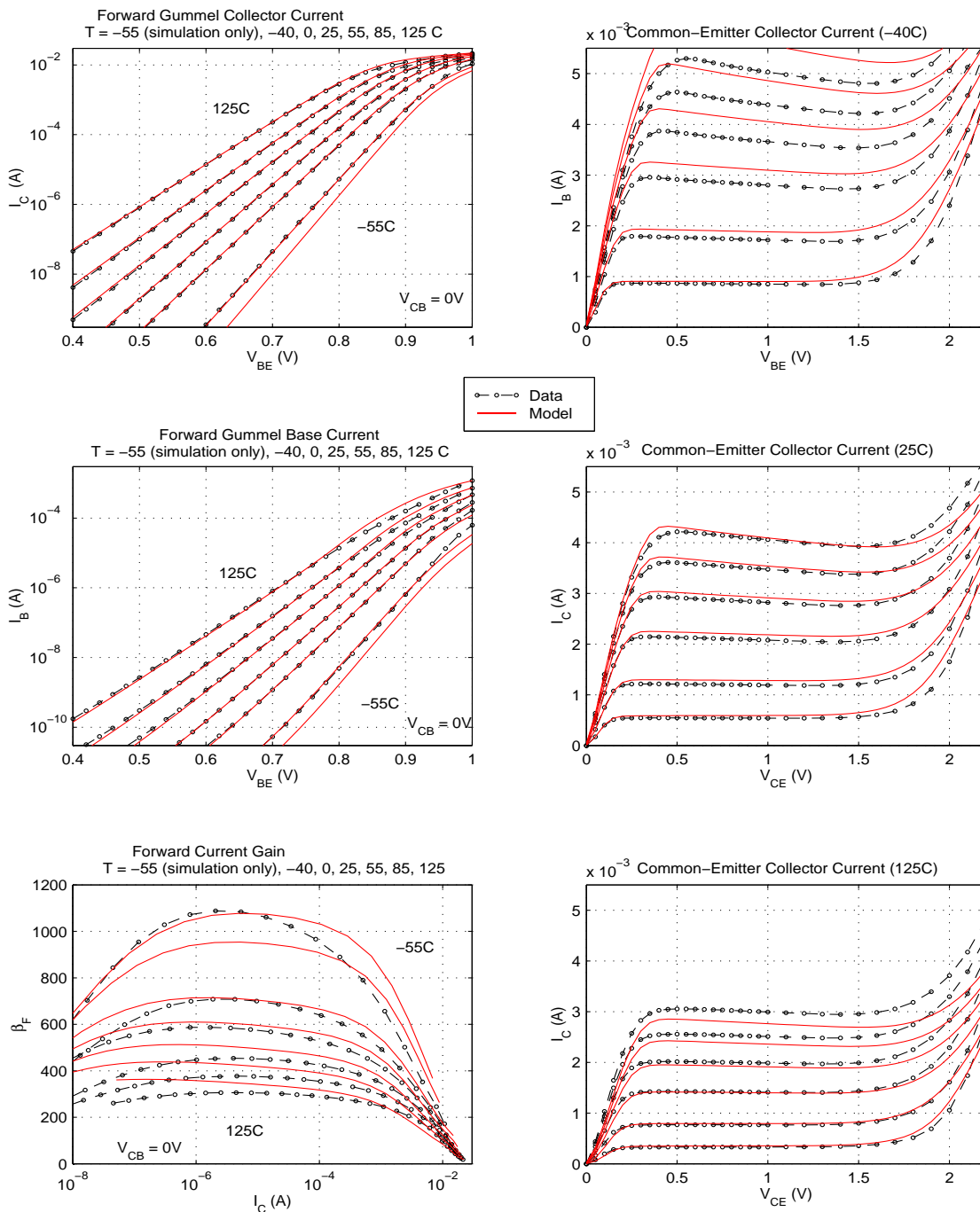
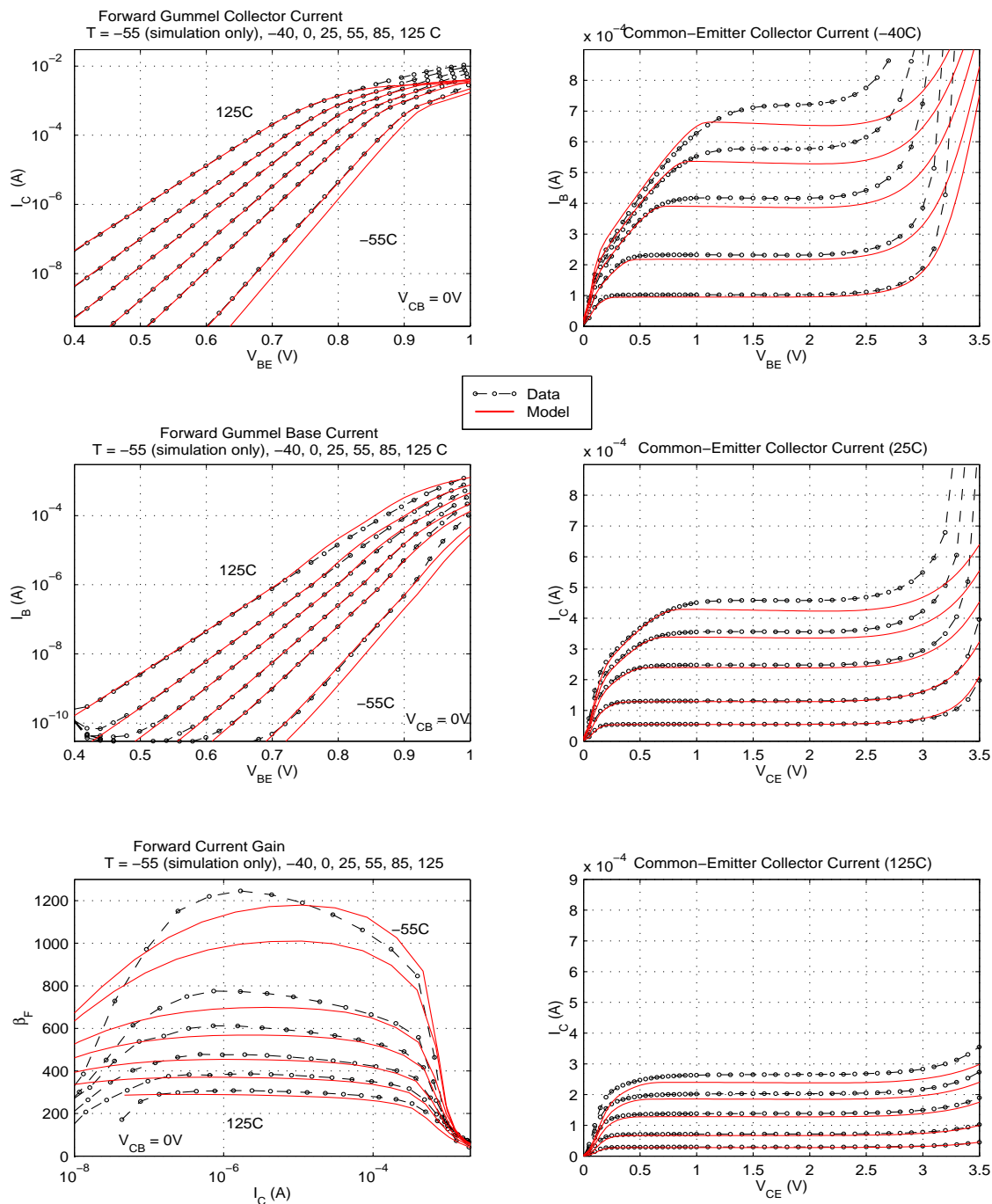


Figure 37. HP NPN DC vs Temperature for $0.12\mu\text{m} \times 3\mu\text{m}$, c-b-e

BiCMOS8HP "High-Breakdown NPN" – Typical DC Characteristics vs. Temperature
Emitter Size: $0.12\text{ }\mu\text{m} \times 2.5\text{ }\mu\text{m} \times 1$, Topology: CBEBc



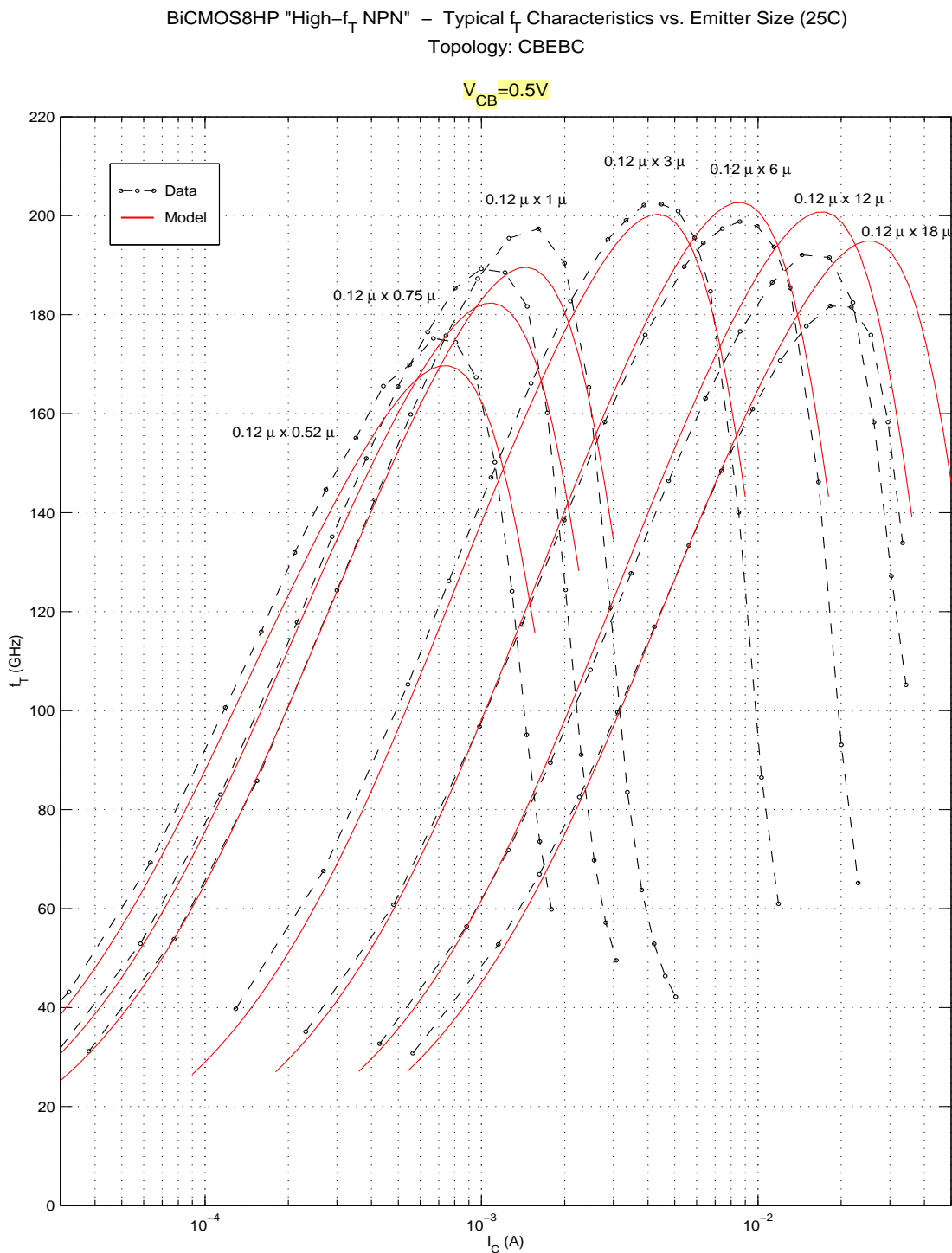
Wafer Parametrics: $\text{ndelrx} = -0.060\text{u}$, $\text{nrdb} = 4.5\text{k}$, $\text{nrea} = 1.98$, $\text{nisahb} = 8.806\text{u}$, $\text{nispbh} = 1.246\text{p}$, $\text{nibeiahb} = 33.40\text{n}$, $\text{nibeipbh} = 206\text{e-18}$

Figure 38. HB NPN DC vs Temperature for $0.12\text{ }\mu\text{m} \times 2.5\text{ }\mu\text{m}$, c-b-e-b-c

3.6 f_T Correlation Plots

The following plots compare the f_T vs I_c characteristics of the npn model with measurement data from the qualification hardware. As the model supports a range of emitter lengths, the plots show the model correlation for a few select device sizes.

<i>Table 34. NPN f_T Correlation Plots</i>			
Characteristic	High- f_T (HP) c-b-e-b-c	High- f_T (HP) c-b-e	High-Breakdown (HB) c-b-e-b-c
f_T vs I_c - Geometry Scaling	Fig 39	Fig 41	Fig 43
f_T vs I_c - V_{cb} and Temperature Dependence	Fig 40	Fig 42	Fig 44
Note: f_T Correlation Plots reflect the SPECTRE VBIC model characteristics.			



Wafer Parametrics: $\text{ndelrx} = -0.060u$, $\text{nrd b} = 4.5k$, $\text{nrea} = 1.98$, $\text{nisa} = 2.14u$, $\text{nisp} = 1.70p$, $\text{nibeia} = 26.47n$, $\text{nibeip} = 5.08e-18$

Figure 39. HP NPN f_T vs I_C - Emitter Scaling Comparison for c-b-e-b-c

BiCMOS8HP "High- f_T NPN" – Typical f_T Characteristics
Emitter Size: $0.12\ \mu\text{m} \times 3.0\ \mu\text{m} \times 1$, Topology: CBECB

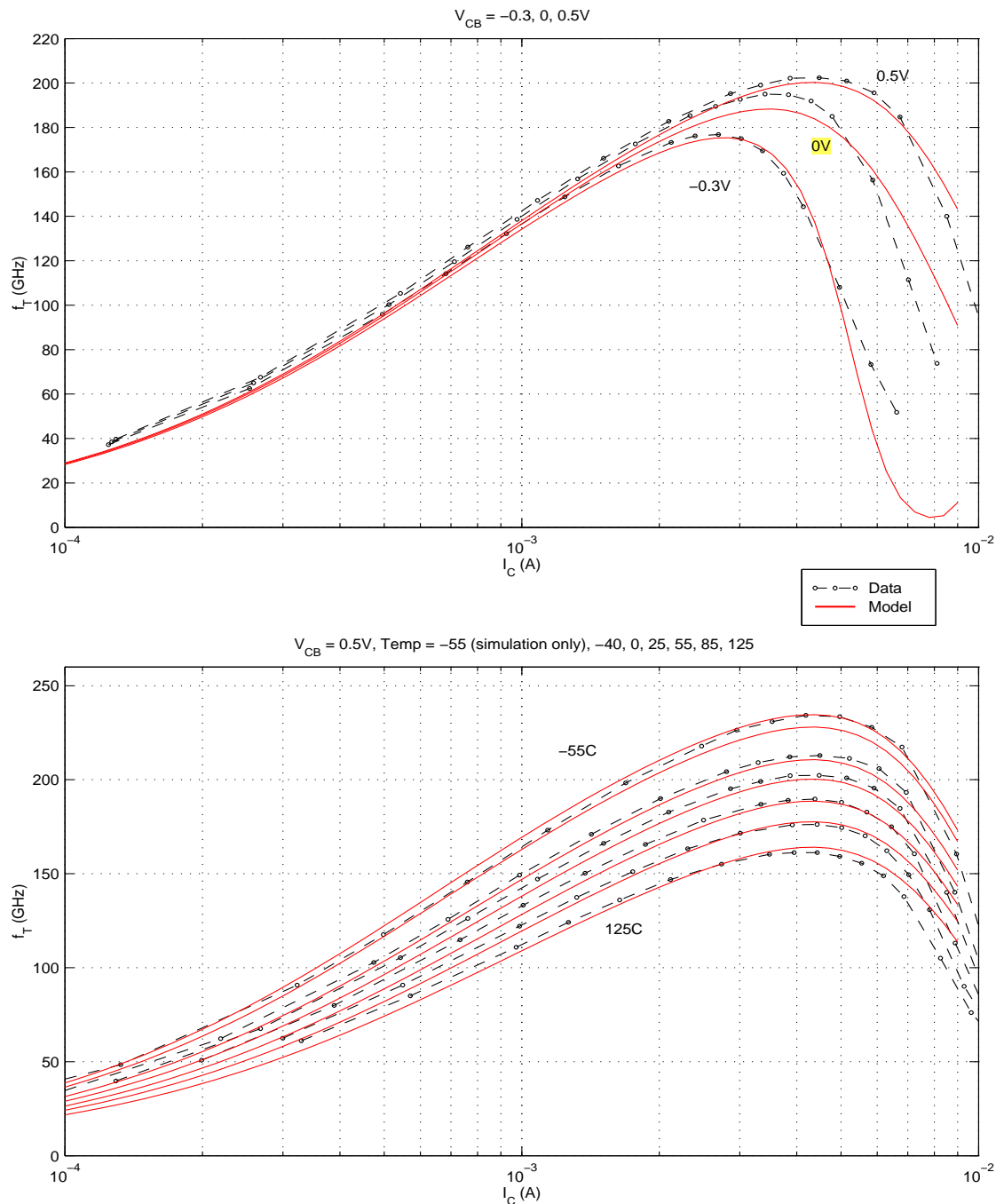


Figure 40. HP NPN f_T vs I_C - V_{cb} and Temperature Dependence for c-b-e-b-c

BiCMOS8HP "High-f_T NPN" – Typical f_T Characteristics vs. Emitter Size (25°C)

Topology: CBE

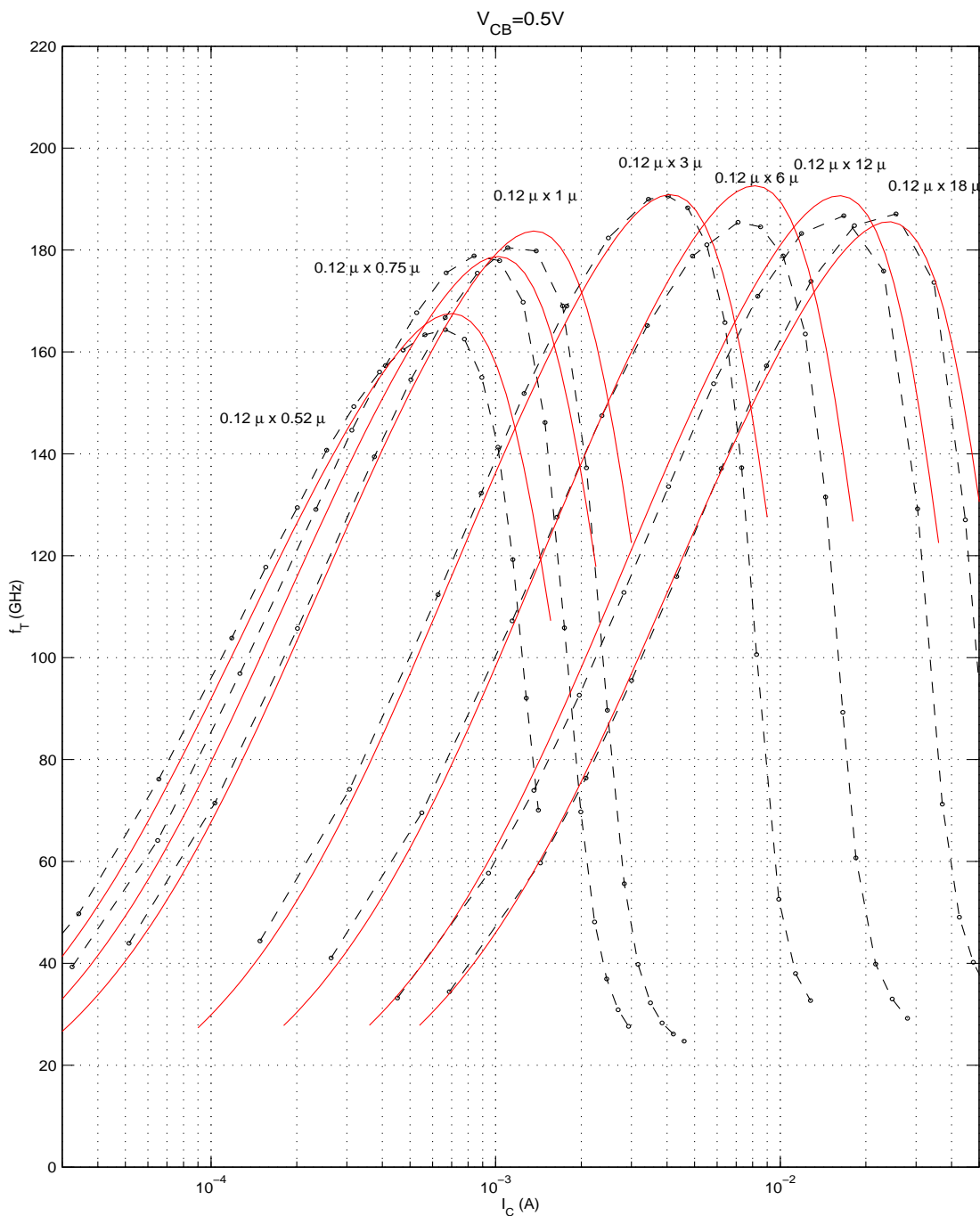


Figure 41. HP NPN f_T vs I_C - Emitter Scaling Comparison for c-b-e

BiCMOS8HP "High-f_T NPN" – Typical f_T Characteristics
Emitter Size: 0.12 μm x 3.0 μm x 1, Topology: CBE

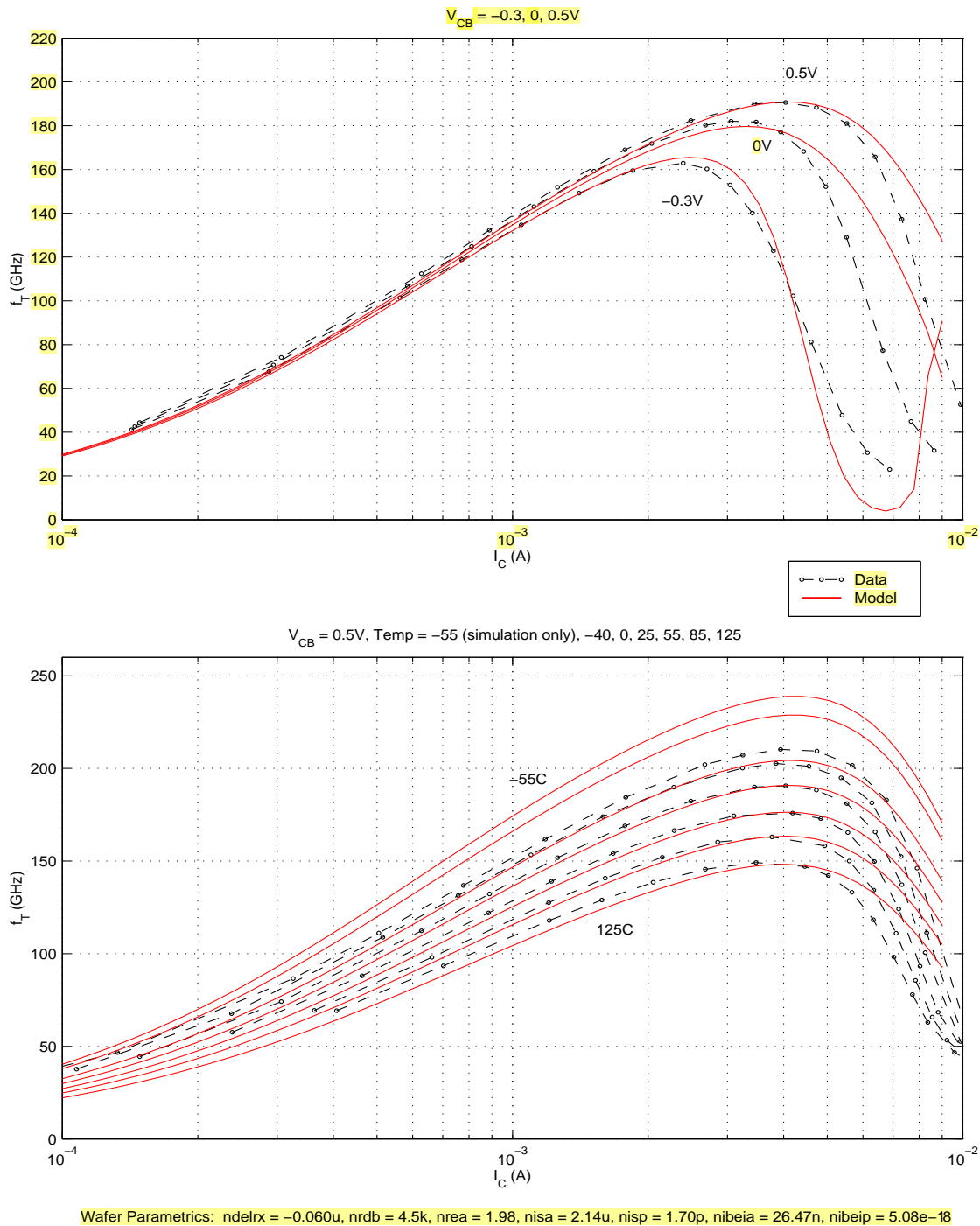
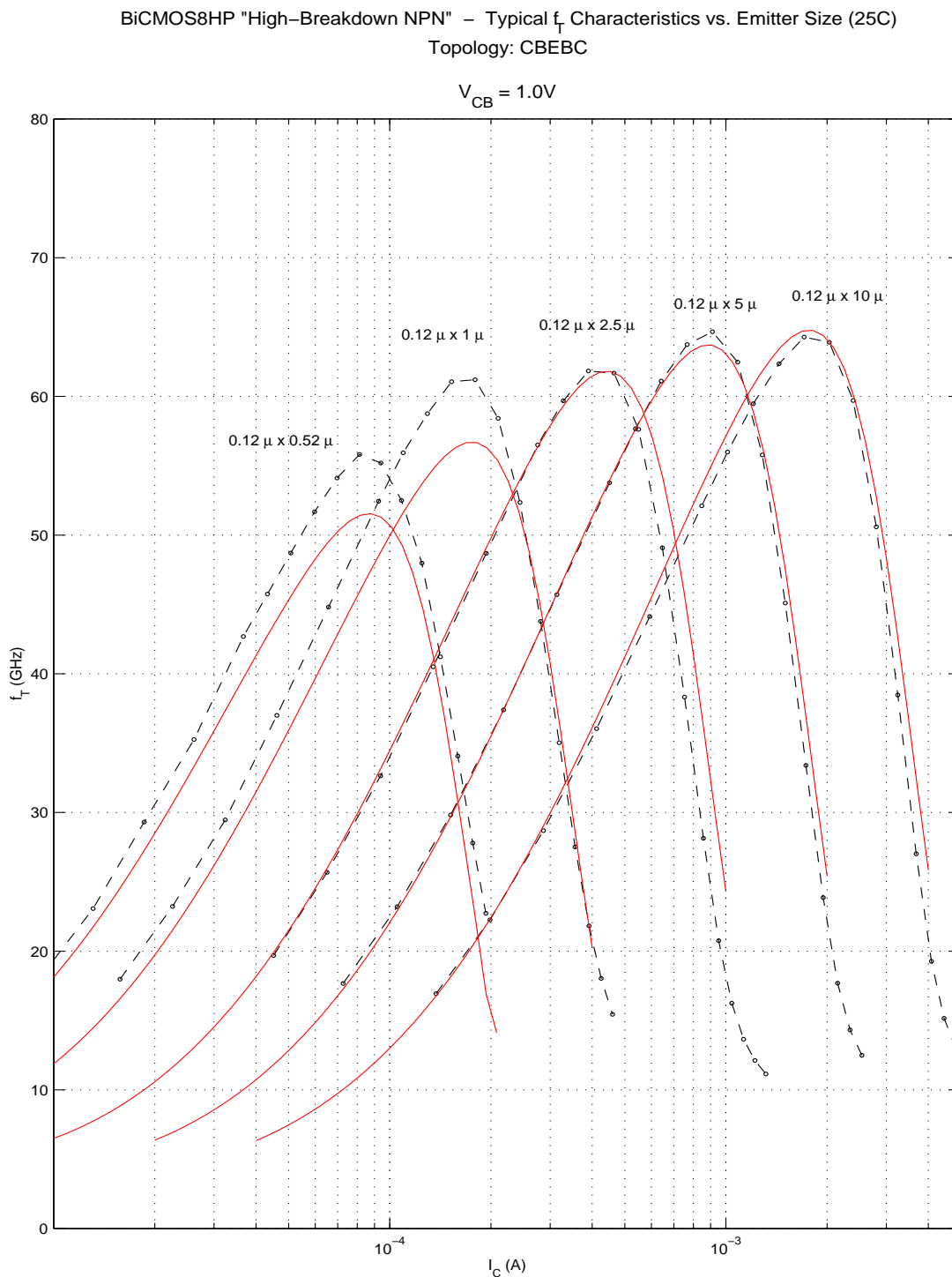
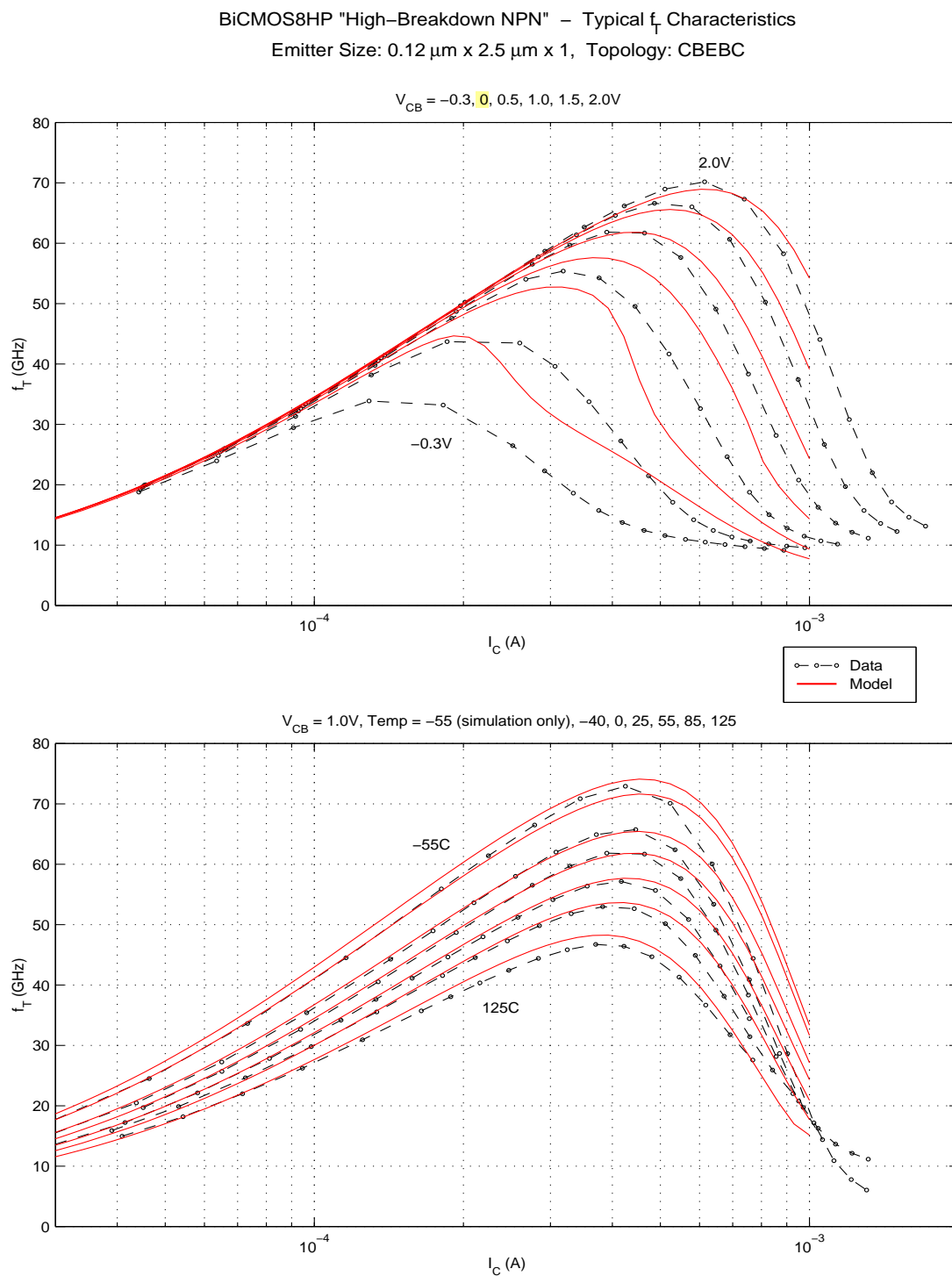


Figure 42. HP NPN f_T vs I_C - V_{cb} and Temperature Dependence for c-b-e



Wafer Parametrics: $ndelrx = -0.060u$, $nrd b = 4.5k$, $nrea = 1.98$, $nisahb = 8.806u$, $nisp h b = 1.246p$, $nibeia h b = 33.40n$, $nibeip h b = 206e-18$, $ntf h b = 1.00p$

Figure 43. HB NPN f_T vs I_C - Emitter Scaling Comparison for c-b-e-b-c



Wafer Parametrics: $\text{ndelrx} = -0.060\text{u}$, $\text{nrdb} = 4.5\text{k}$, $\text{nrea} = 1.98$, $\text{nisahb} = 8.806\text{u}$, $\text{nisphb} = 1.246\text{p}$, $\text{nibeiahb} = 33.40\text{n}$, $\text{nibeipb} = 206\text{e-18}$, $\text{ntfbb} = 1.00\text{p}$

Figure 44. HB NPN f_T vs I_C - V_{cb} and Temperature Dependence for c-b-e-b-c

3.7 S-Parameter Correlation Plots

The following plots compare the S-Parameter characteristics of the npn model with measurement data from qualification hardware. As the model supports a range of emitter lengths, the plots show the model correlation for a few select device sizes at 25C.

Table 35. NPN S-Parameter Correlation Plots

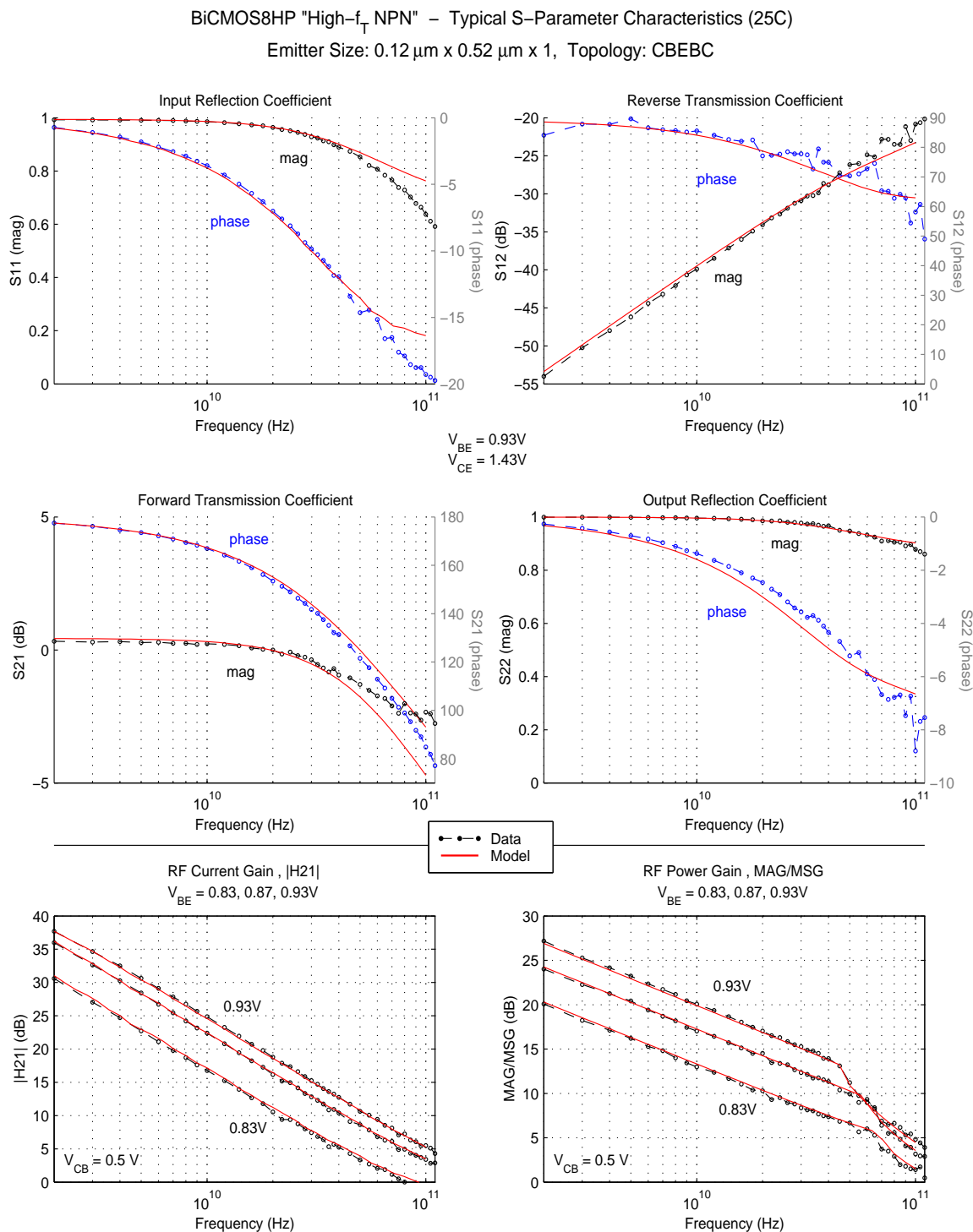
Device Emitter Size	High- f_T (HP) c-b-e-b-c	High- f_T (HP) c-b-e	High-Breakdown (HB) c-b-e-b-c
Width = 0.12 μ m, Length = 0.52 μ m	Fig 45	Fig 52	Fig 59
Width = 0.12 μ m, Length = 0.75 μ m	Fig 46	Fig 53	data not available
Width = 0.12 μ m, Length = 1.0 μ m	Fig 47	Fig 54	Fig 60
Width = 0.12 μ m, Length = 2.5 μ m	data not available	data not available	Fig 61
Width = 0.12 μ m, Length = 3.0 μ m	Fig 48	Fig 55	data not available
Width = 0.12 μ m, Length = 5.0 μ m	data not available	data not available	Fig 62
Width = 0.12 μ m, Length = 6.0 μ m	Fig 49	Fig 56	data not available
Width = 0.12 μ m, Length = 10 μ m	data not available	data not available	Fig 63
Width = 0.12 μ m, Length = 12 μ m	Fig 50	Fig 57	data not available
Width = 0.12 μ m, Length = 18 μ m	Fig 51	Fig 58	data not available
Note: S-Parameter Correlation Plots reflect the SPECTRE VBIC model characteristics.			

- The top four plots show the magnitude and phase for the S-Parameters from 2GHz to 110GHz at a single Vbe, Vce bias which is near the peak Ft for the device.
- The “RF Current Gain” plot in the lower left of the page depicts the magnitude, in dB, of the Current Gain (H_{21}) for a group of three (3) Vbe biases, as shown. Extrapolation of H_{21} down to zero gives Ft value.
- The “RF Power Gain” plot in the lower right of the page depicts the magnitudes, in dB, of the Maximum Available/Maximum Stable Power Gain (MAG/MSG) for a group of three (3) Vbe biases, as shown. Extrapolation of MAG/MSG down to zero gives f_{MAX} value.

In addition to the nominal temperature (25C) plots, S-Parameter characteristics vs temperature are shown for the 0.12μm x 3.0μm High- f_T devices and the 0.12μm x 2.5μm High-Breakdown device at -40C and 125C.

<i>Table 36. NPN S-Parameter Temperature Plots</i>			
Device Emitter Size	High- f_T (HP) c-b-e-b-c	High- f_T (HP) c-b-e	High-Breakdown (HB) c-b-e-b-c
Width = 0.12μm, Length = 2.5μm, -40C	data not available	data not available	Fig 68
Width = 0.12μm, Length = 2.5μm, 125C	data not available	data not available	Fig 69
Width = 0.12μm, Length = 3.0μm, -40C	Fig 64	Fig 66	data not available
Width = 0.12μm, Length = 3.0μm, 125C	Fig 65	Fig 67	data not available
Note: S-Parameter Temperature Plots reflect the SPECTRE VBIC model characteristics.			

Note: All of the S-Parameter simulation curves were created with some adjustments to the skew file parameters, as noted in each figure, to center the model near the mean of the measured data.



Wafer Parametrics: ndelrx = -0.060u, nrdb = 4.5k, nrea = 1.98, nisa = 2.14u, nisp = 1.70p, nibeia = 26.47n, nibeip = 5.08e-18

Figure 45. HP NPN S-Parameter Characteristics for 0.12 μm x 0.52 μm , c-b-e-b-c

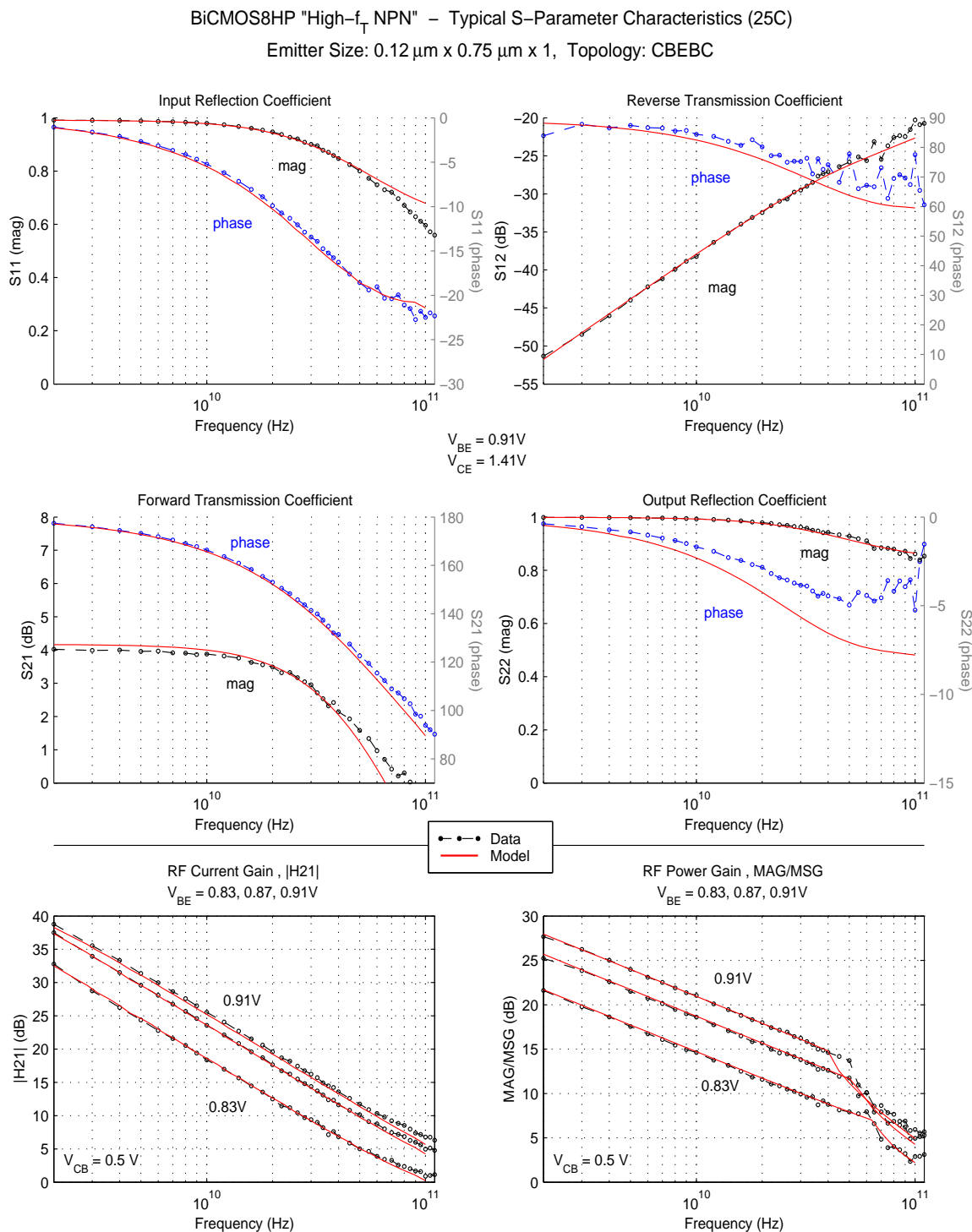
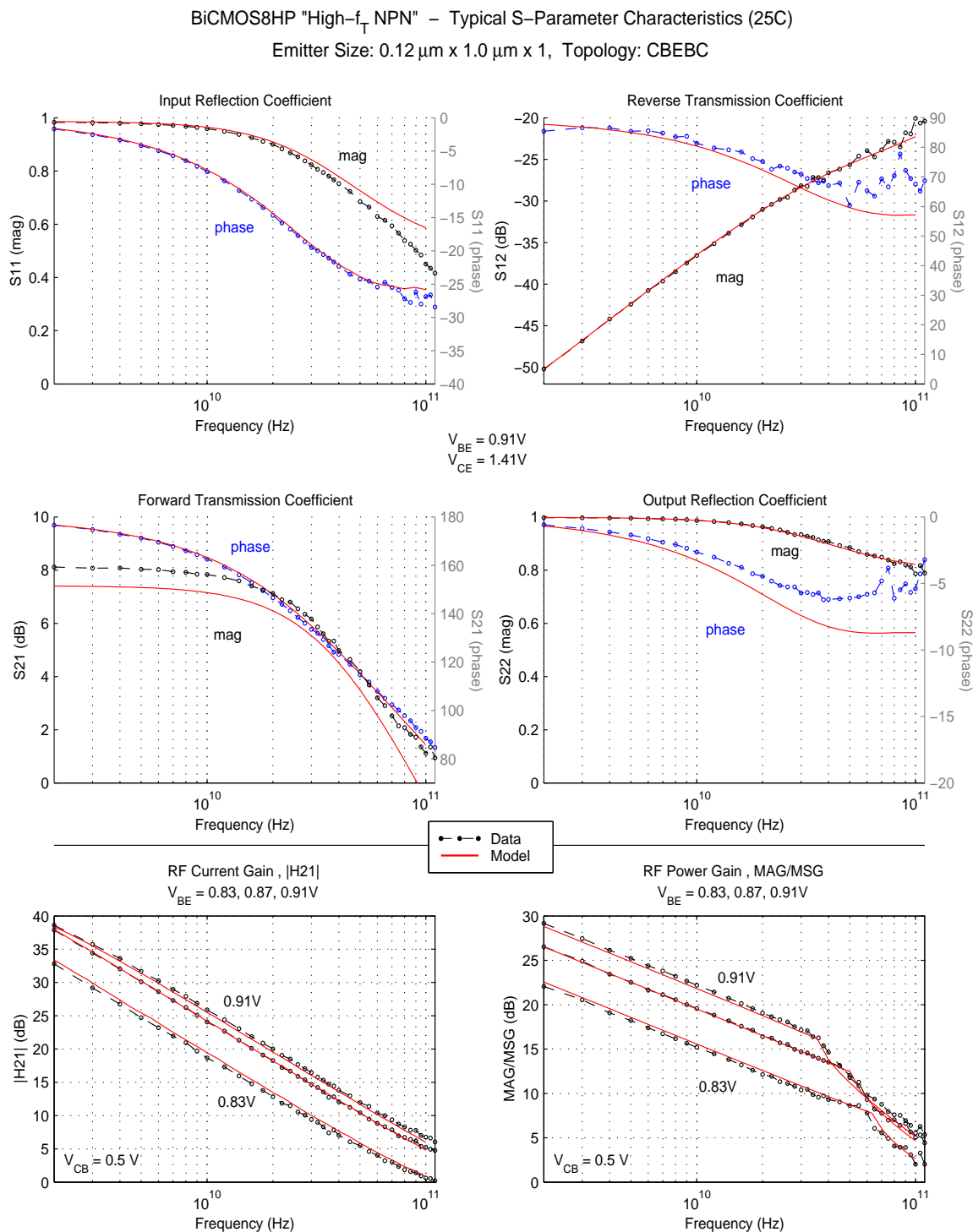


Figure 46. HP NPN S-Parameter Characteristics for $0.12\ \mu\text{m} \times 0.75\ \mu\text{m}$, c-b-e-b-c



Wafer Parametrics: $\text{ndelrx} = -0.060\text{u}$, $\text{nrd b} = 4.5\text{k}$, $\text{nrea} = 1.98$, $\text{nisa} = 2.14\text{u}$, $\text{nisp} = 1.70\text{p}$, $\text{nibeia} = 26.47\text{n}$, $\text{nibeip} = 5.08\text{e-18}$

Figure 47. HP NPN S-Parameter Characteristics for $0.12\ \mu\text{m} \times 1\ \mu\text{m}$, c-b-e-b-c

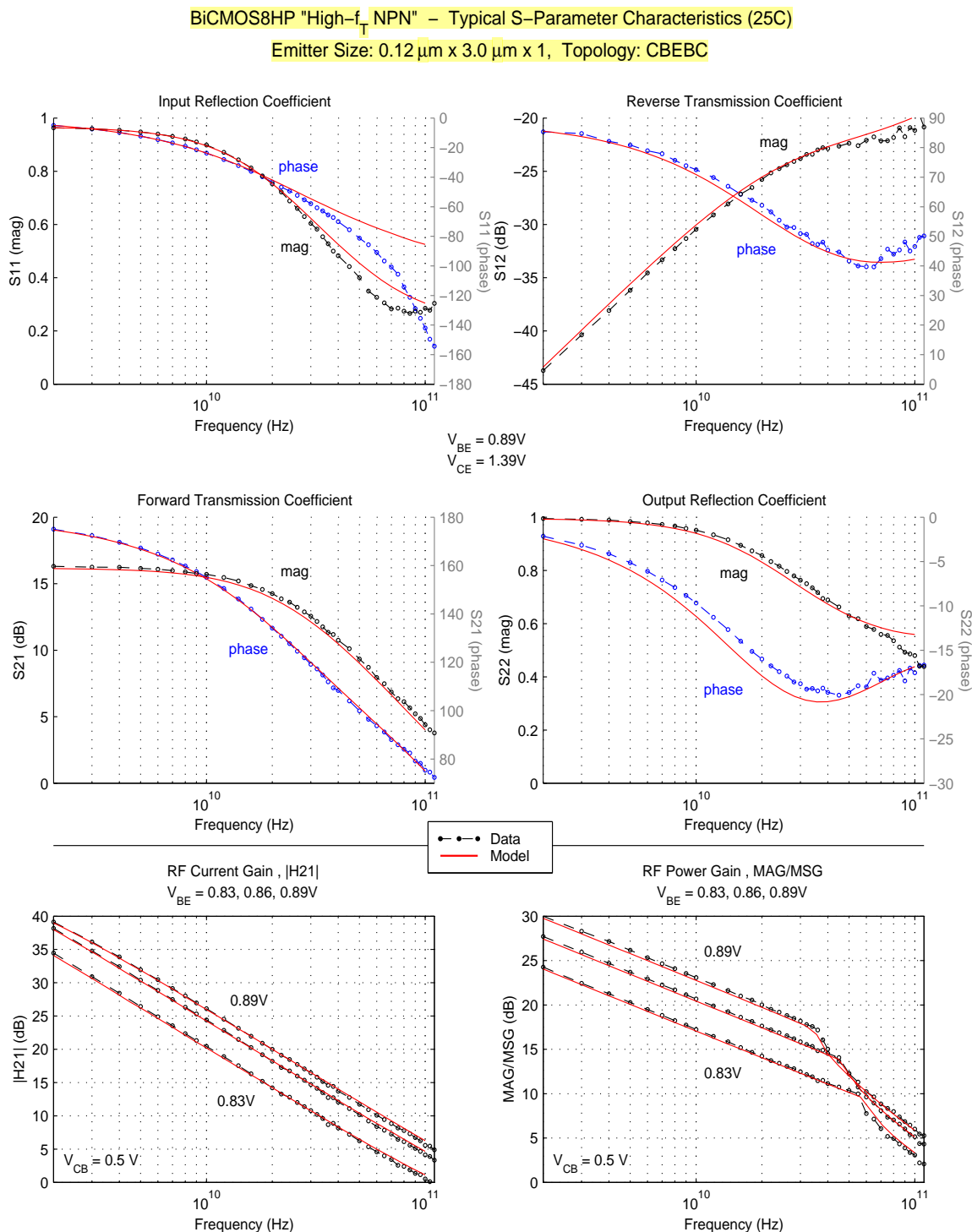
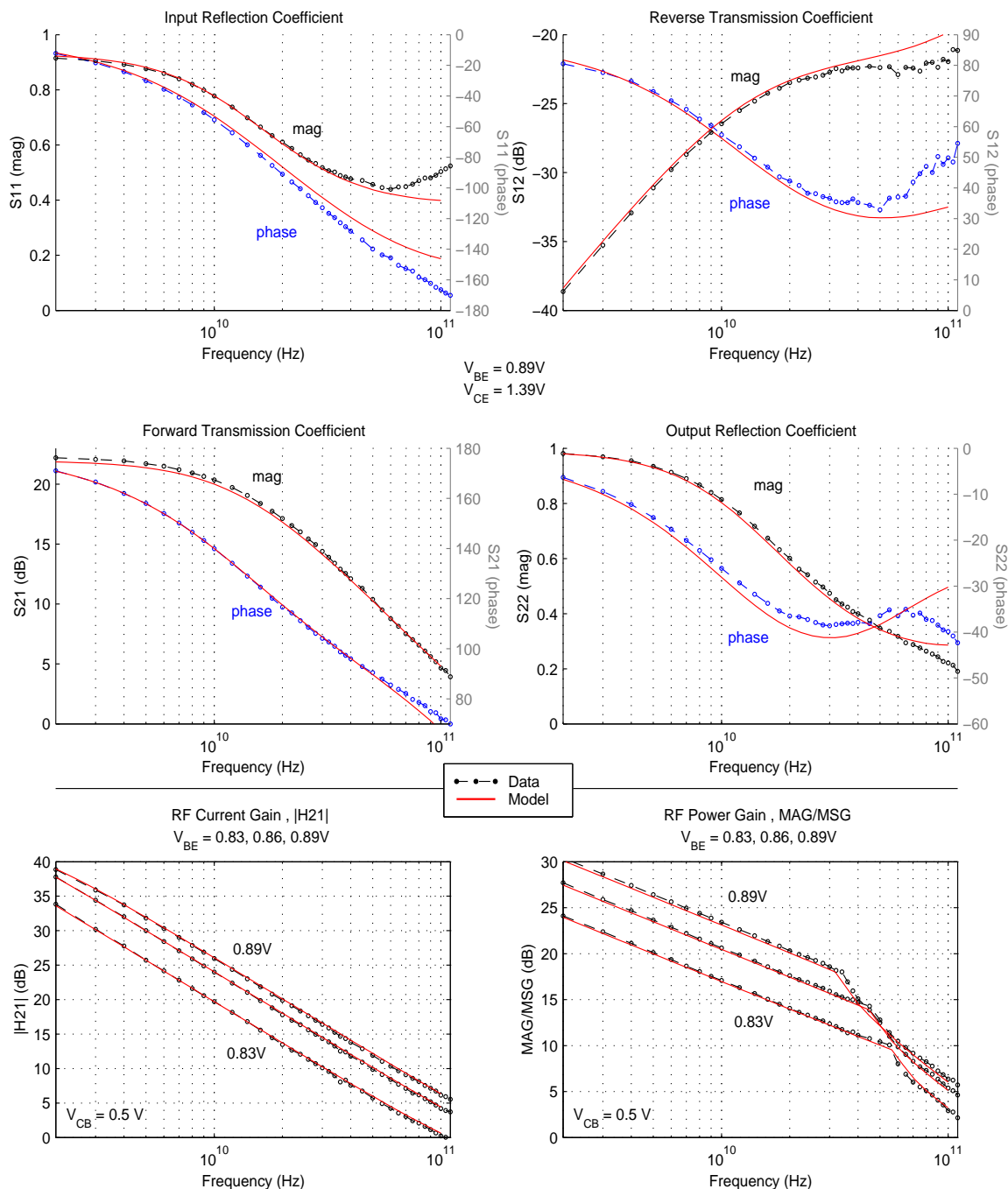


Figure 48. HP NPN S-Parameter Characteristics for 0.12 μm x 3 μm , c-b-e-b-c

BiCMOS8HP "High- f_T NPN" – Typical S-Parameter Characteristics (25C)

Emitter Size: 0.12 μm x 6.0 μm x 1, Topology: CBEB



Wafer Parametrics: $\text{ndelrx} = -0.060\text{u}$, $\text{nrd} = 4.5\text{k}$, $\text{nrea} = 1.98$, $\text{nisa} = 2.14\text{u}$, $\text{nisp} = 1.70\text{p}$, $\text{nibeia} = 26.47\text{n}$, $\text{nibeip} = 5.08\text{e-18}$

Figure 49. HP NPN S-Parameter Characteristics for 0.12 μm x 6 μm , c-b-e-b-c

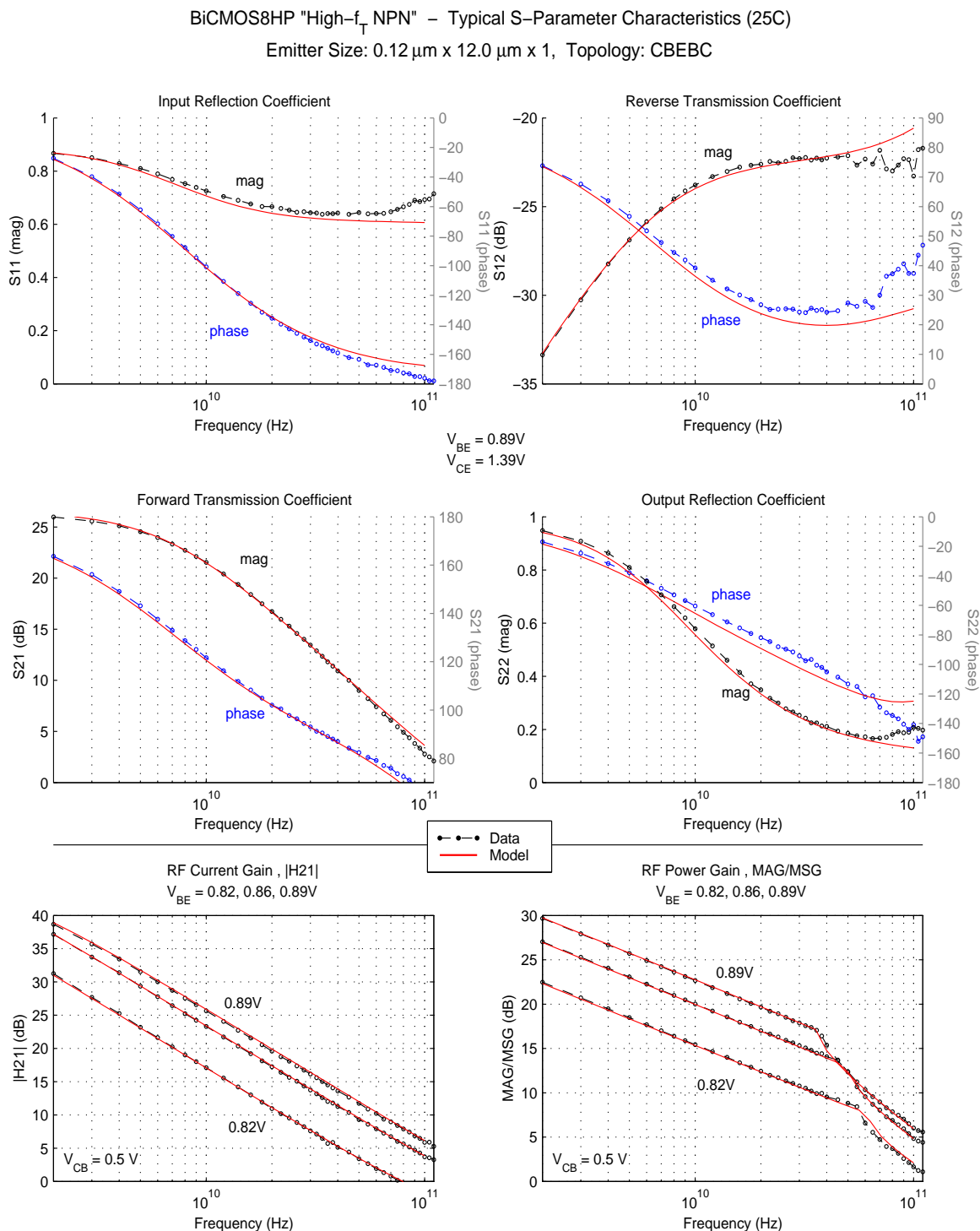
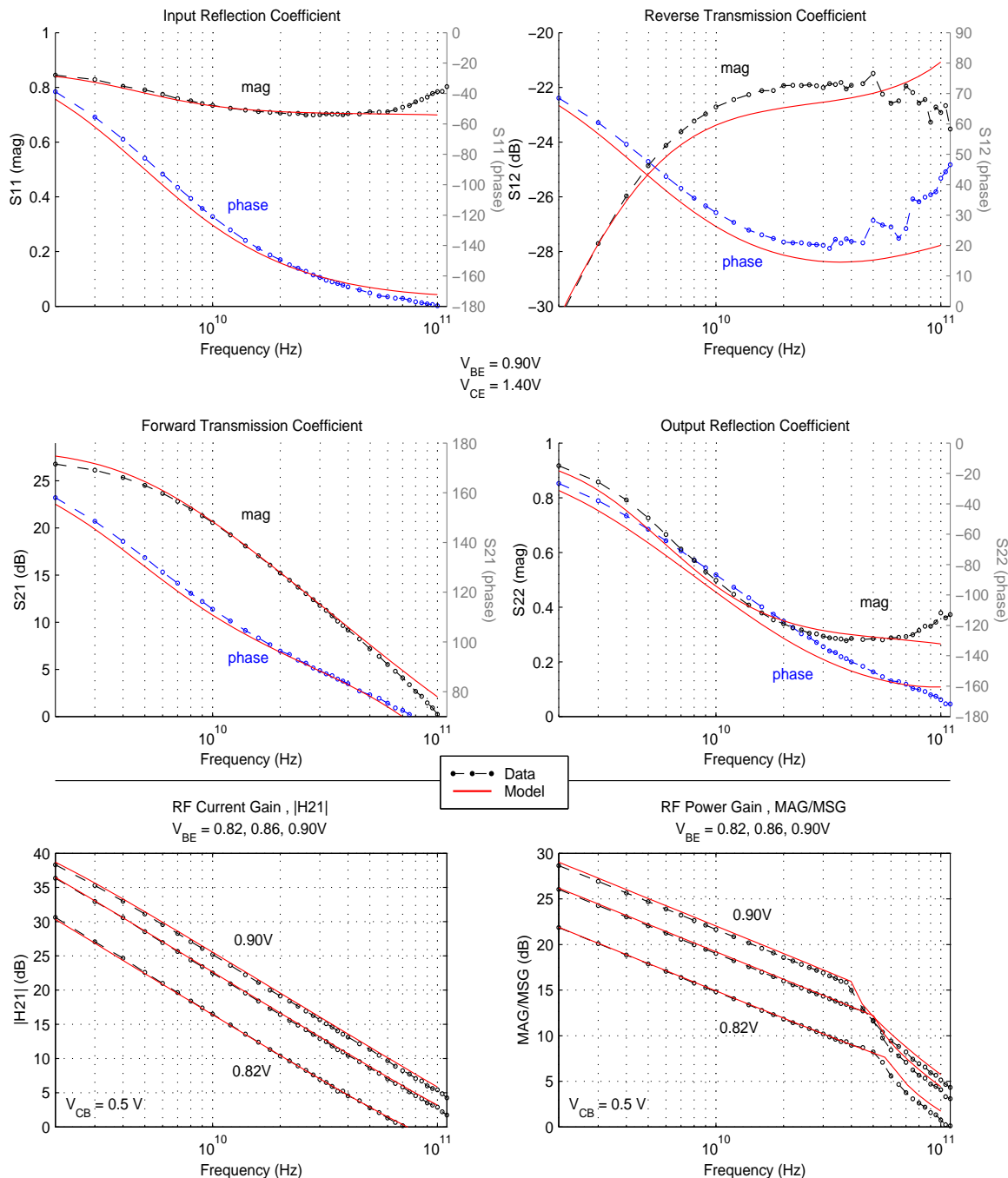


Figure 50. HP NPN S-Parameter Characteristics for 0.12 μm x 12 μm , c-b-e-b-c

BiCMOS8HP "High- f_T NPN" – Typical S-Parameter Characteristics (25C)

Emitter Size: 0.12 μm x 18.0 μm x 1, Topology: CBECB



Wafer Parametrics: ndelrx = -0.060u, nrdb = 4.5k, nrea = 1.98, nisa = 2.14u, nisp = 1.70p, nibeia = 26.47n, nibeip = 5.08e-18

Figure 51. HP NPN S-Parameter Characteristics for 0.12 μm x 18 μm , c-b-e-b-c

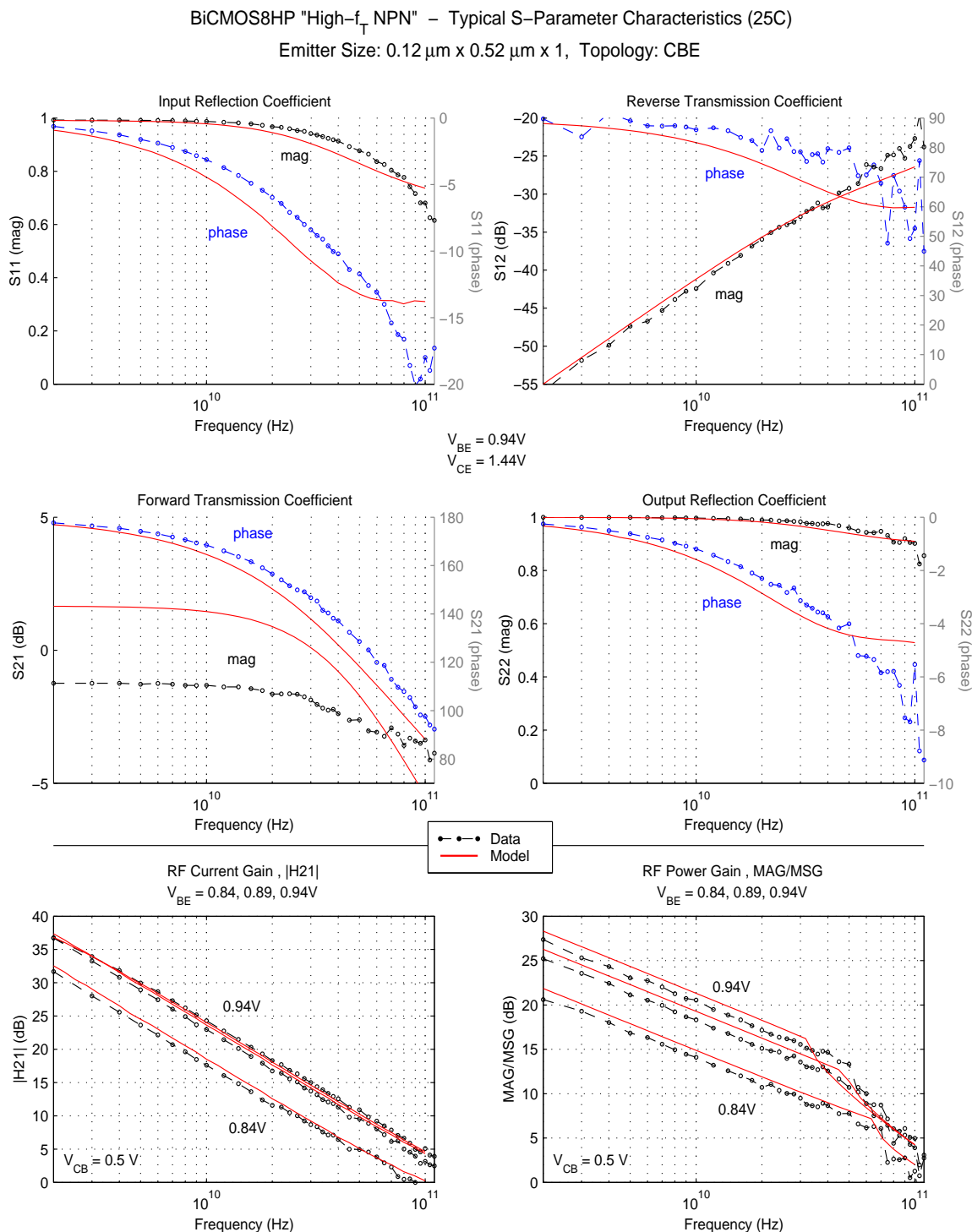
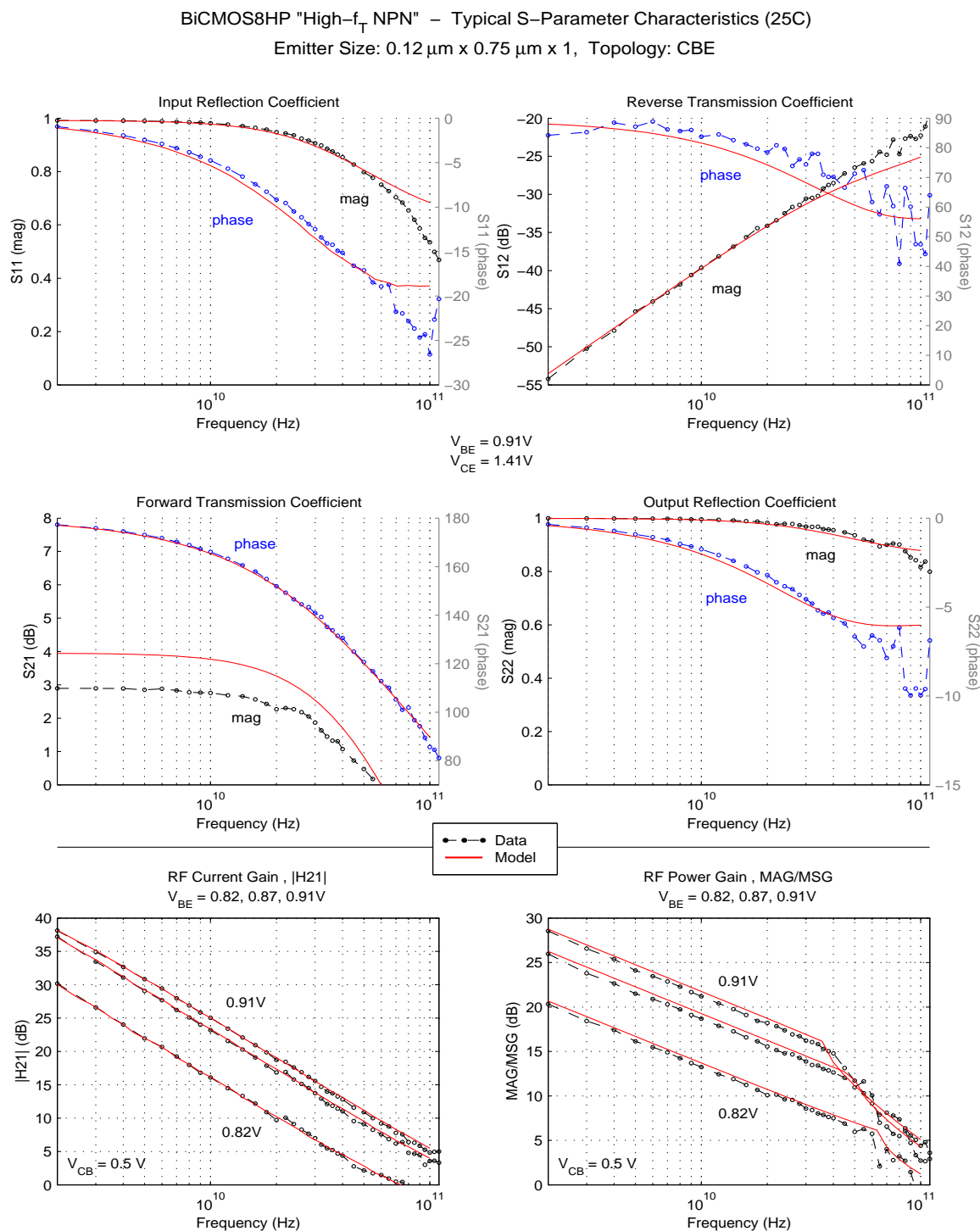


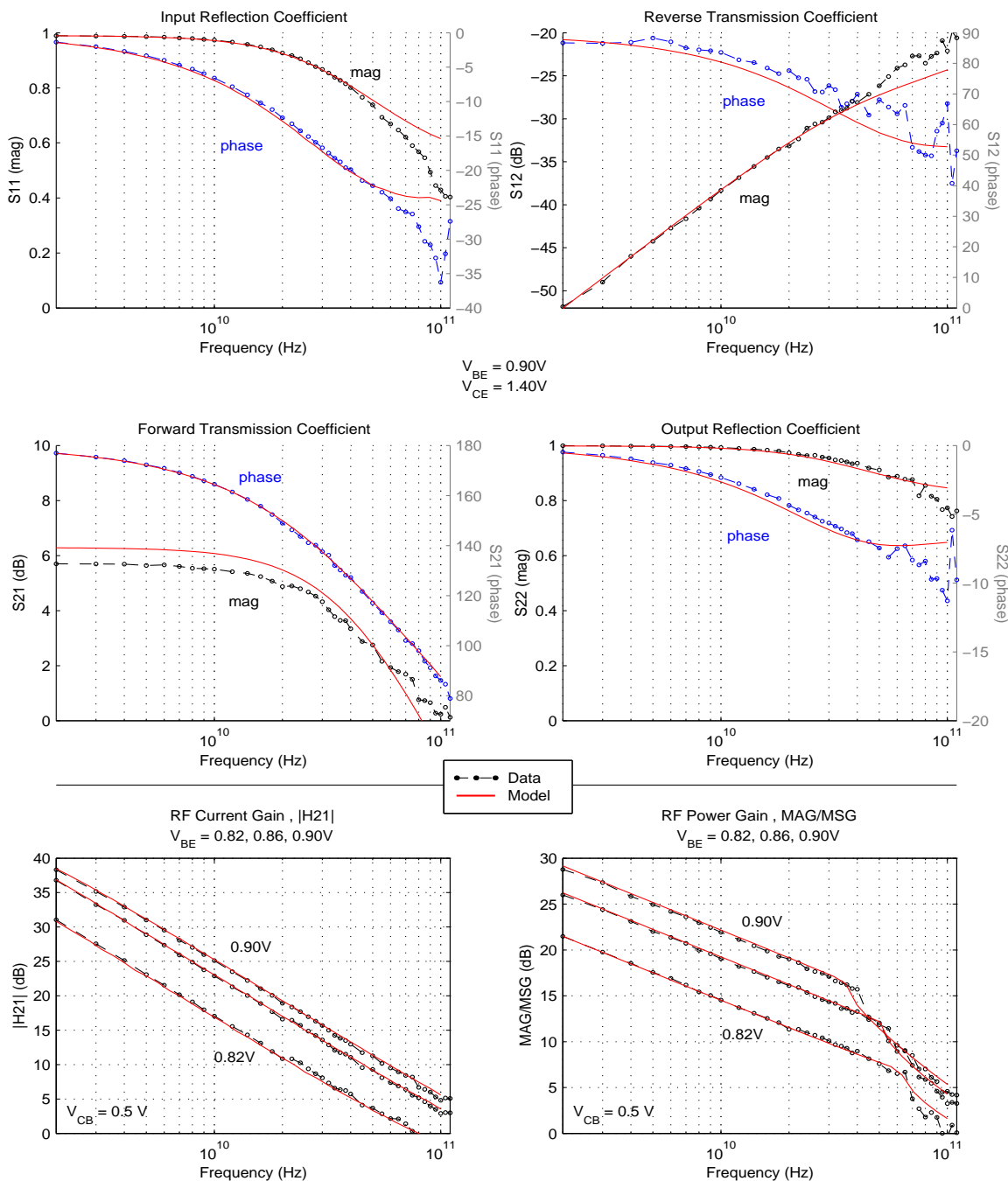
Figure 52. HP NPN S-Parameter Characteristics for $0.12\ \mu\text{m} \times 0.52\ \mu\text{m}$, c-b-e



Wafer Parametrics: ndelrx = -0.060u, nrdb = 4.5k, nrea = 1.98, nisa = 2.14u, nisp = 1.70p, nibeia = 26.47n, nibeip = 5.08e-18

Figure 53. HP NPN S-Parameter Characteristics for 0.12 μm x 0.75 μm , c-b-e

BiCMOS8HP "High- f_T NPN" – Typical S-Parameter Characteristics (25C)
Emitter Size: 0.12 μm x 1.0 μm x 1, Topology: CBE

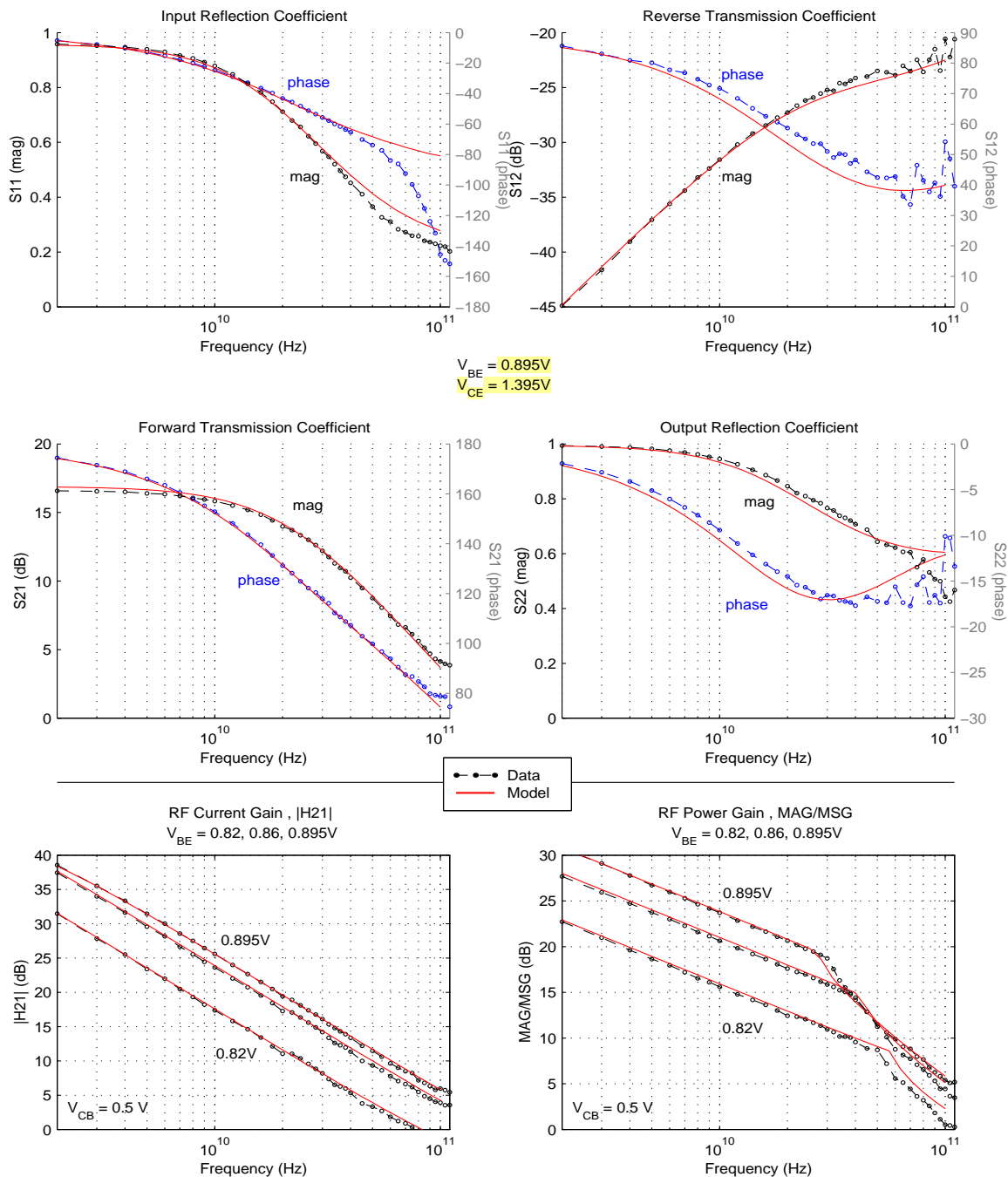


Wafer Parametrics: ndelrx = -0.060u, nrdb = 4.5k, nrea = 1.98, nisa = 2.14u, nisp = 1.70p, nibeia = 26.47n, nibeip = 5.08e-18

Figure 54. HP NPN S-Parameter Characteristics for 0.12 μm x 1 μm , c-b-e

BiCMOS8HP "High- f_T NPN" – Typical S-Parameter Characteristics (25C)

Emitter Size: $0.12\ \mu\text{m} \times 3.0\ \mu\text{m} \times 1$, Topology: CBE



Wafer Parametrics: $\text{ndelrx} = -0.060\text{u}$, $\text{nrdb} = 4.5\text{k}$, $\text{nrea} = 1.98$, $\text{nisa} = 2.14\text{u}$, $\text{nisp} = 1.70\text{p}$, $\text{nibeia} = 26.47\text{n}$, $\text{nibeip} = 5.08\text{e}-18$

Figure 55. HP NPN S-Parameter Characteristics for $0.12\ \mu\text{m} \times 3\ \mu\text{m}$, c-b-e

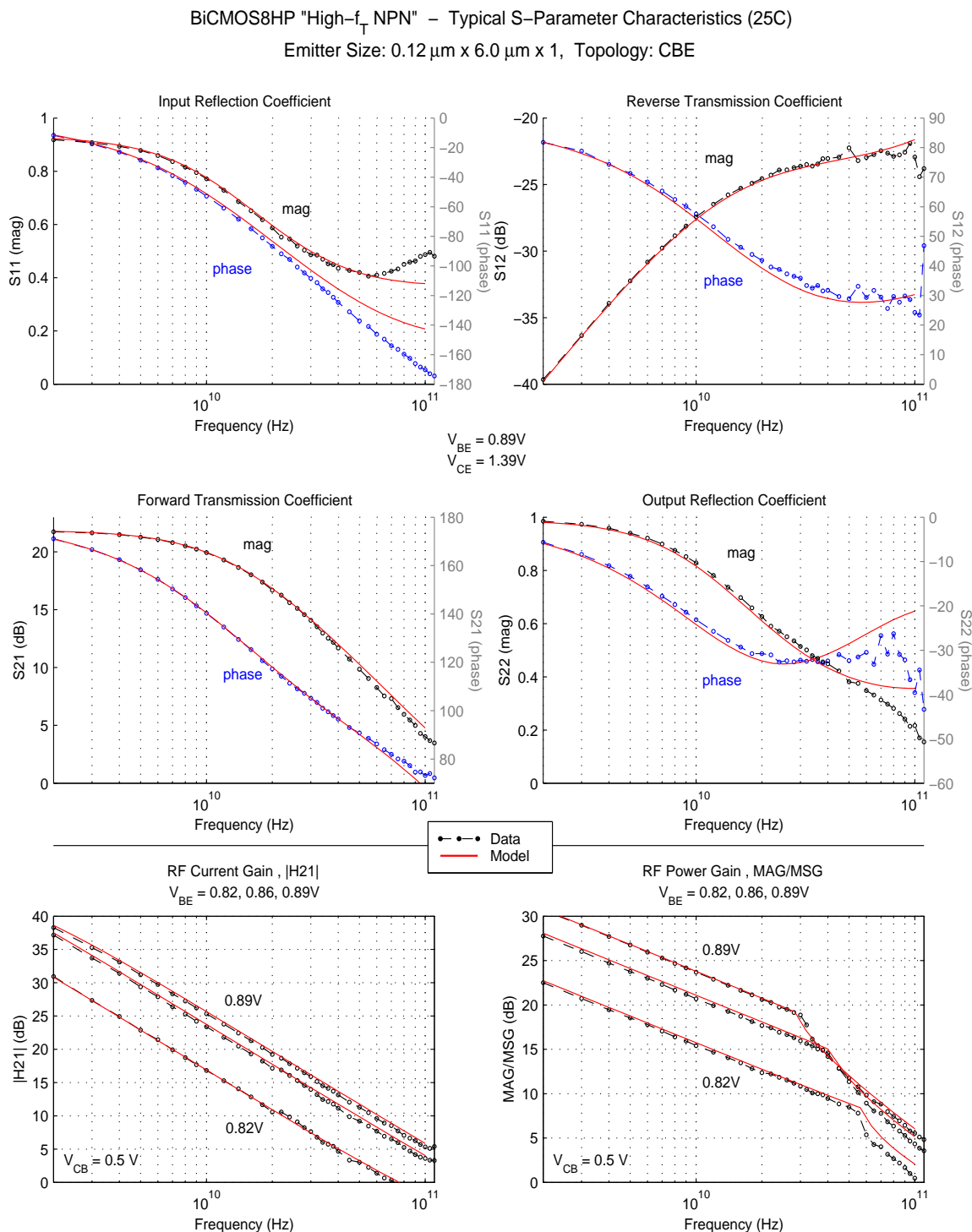
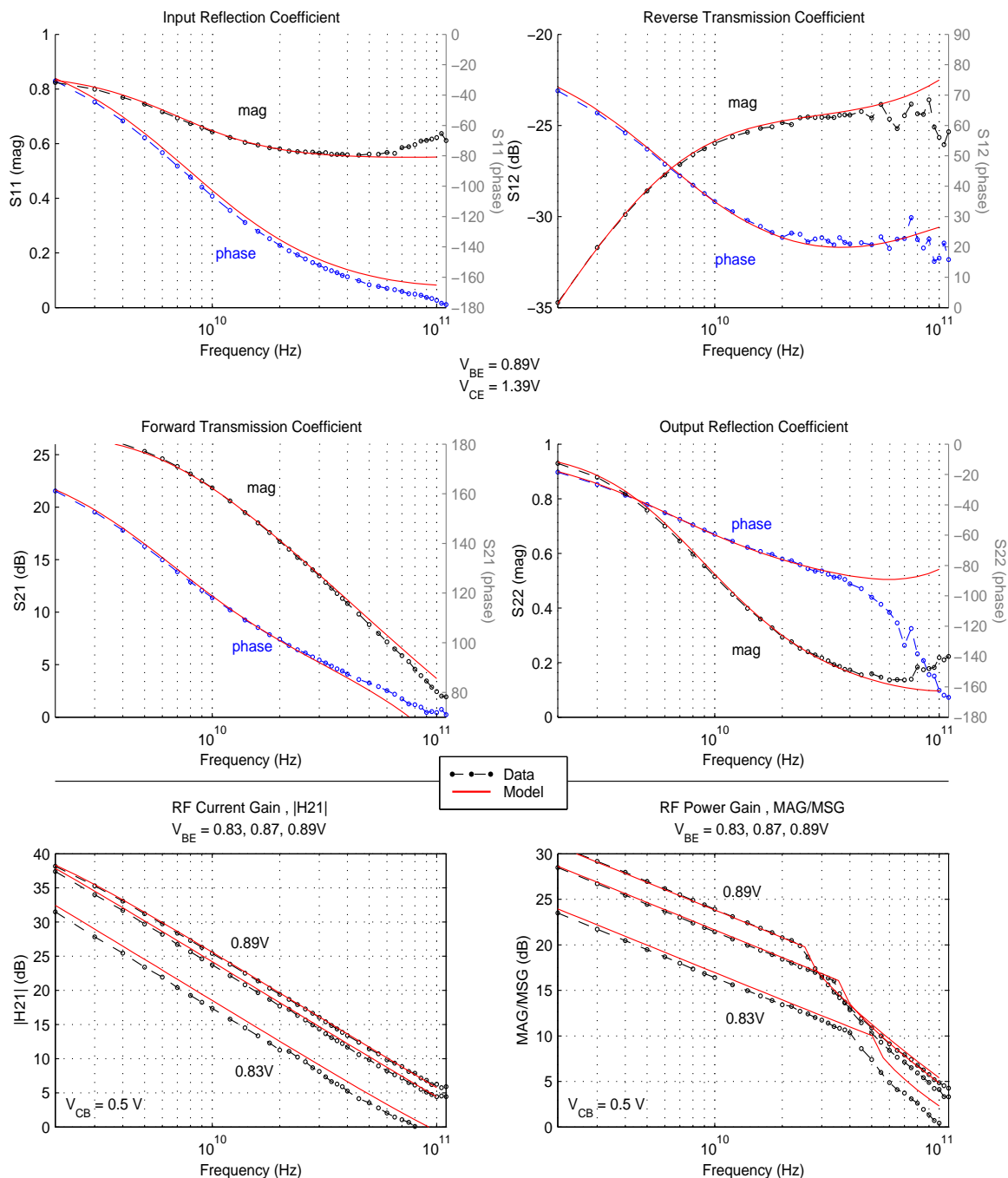


Figure 56. HP NPN S-Parameter Characteristics for $0.12\ \mu\text{m} \times 6\ \mu\text{m}$, c-b-e

BiCMOS8HP "High- f_T NPN" – Typical S-Parameter Characteristics (25C)

Emitter Size: $0.12\mu\text{m} \times 12.0\mu\text{m} \times 1$, Topology: CBE



Wafer Parametrics: $\text{ndelrx} = -0.060\text{u}$, $\text{nrdB} = 4.5\text{k}$, $\text{nrea} = 1.98$, $\text{nisa} = 2.14\text{u}$, $\text{nisp} = 1.70\text{p}$, $\text{nibeia} = 26.47\text{n}$, $\text{nibeip} = 5.08\text{e-18}$

Figure 57. HP NPN S-Parameter Characteristics for $0.12\mu\text{m} \times 12\mu\text{m}$, c-b-e

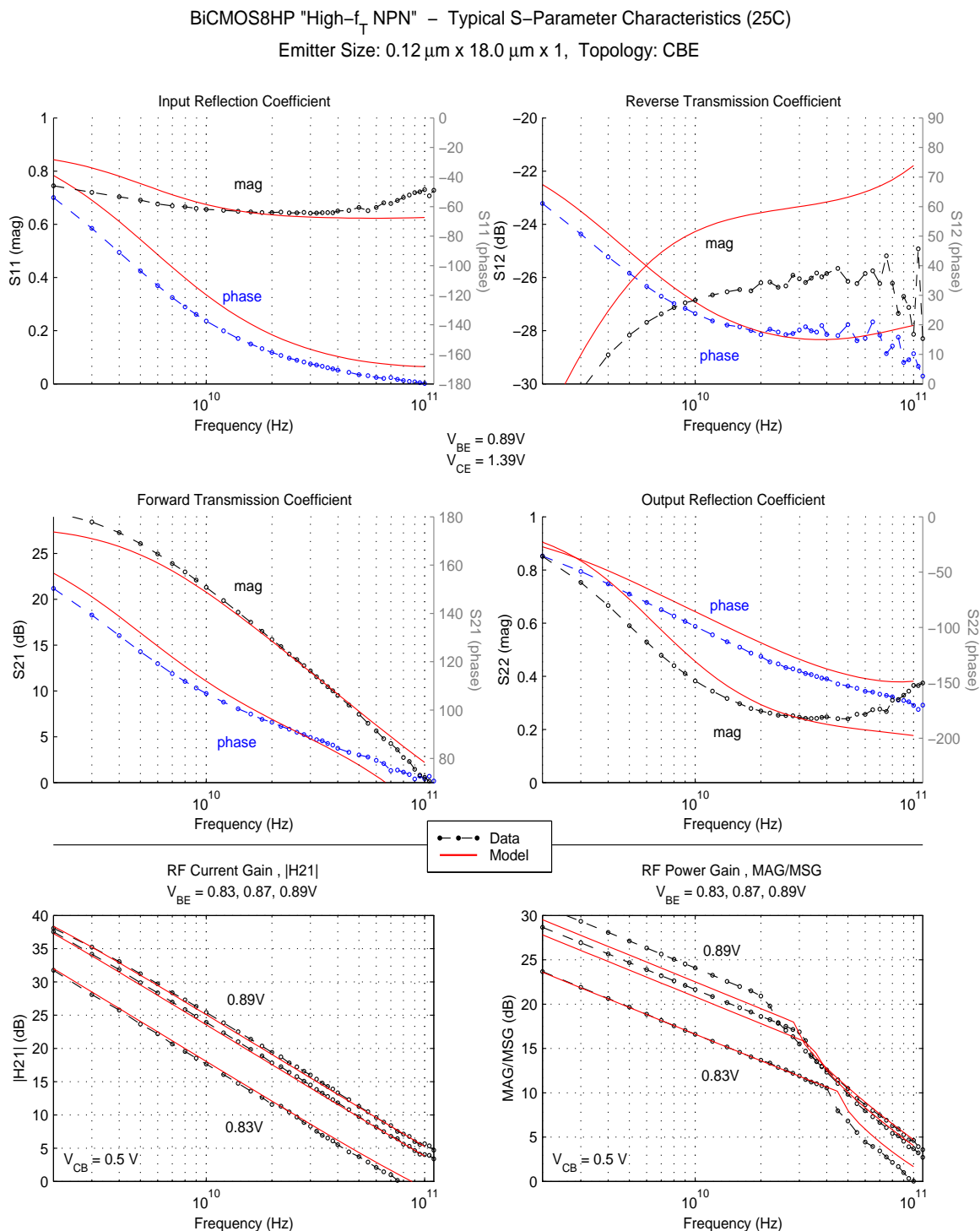
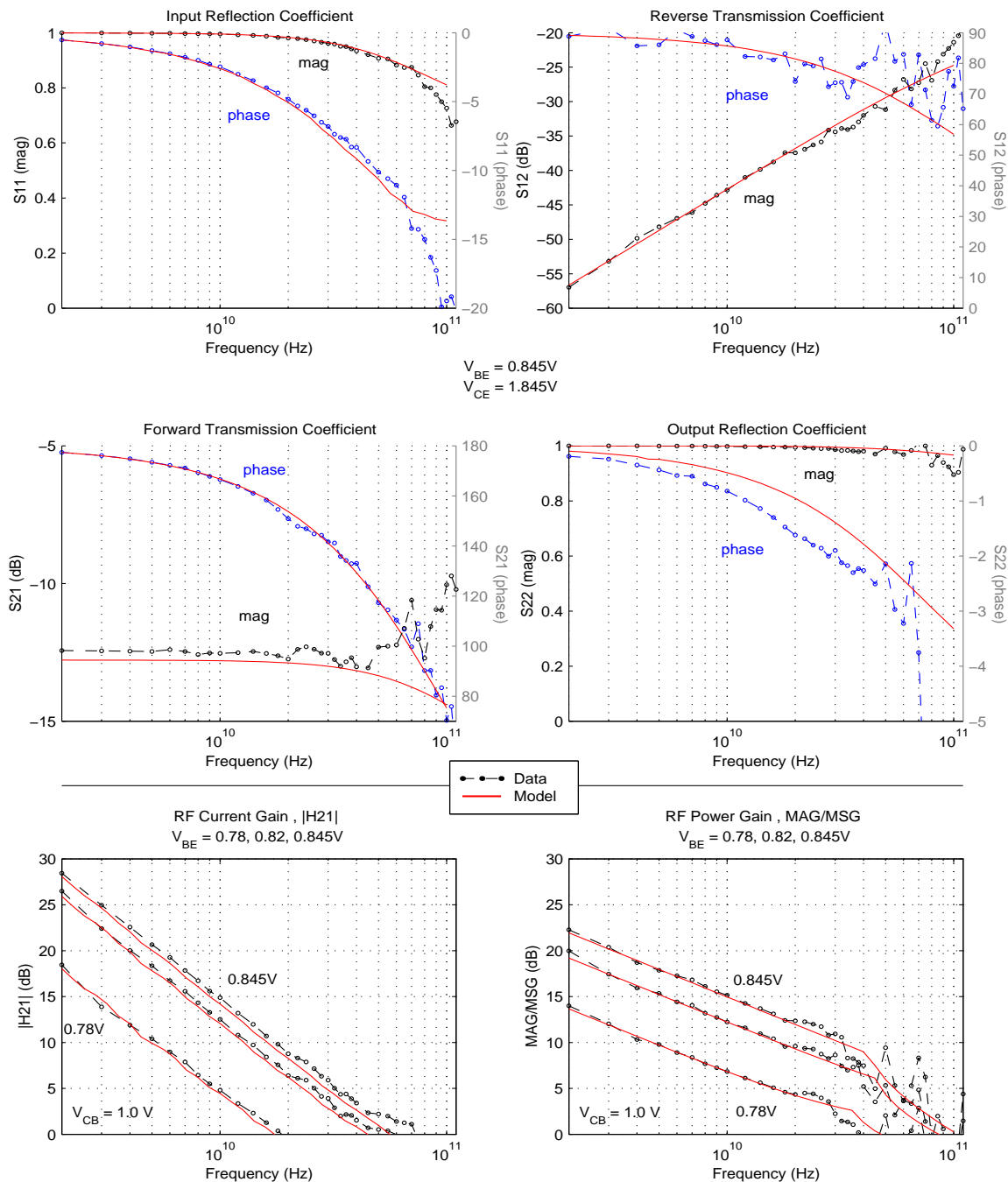


Figure 58. HP NPN S-Parameter Characteristics for $0.12\mu\text{m} \times 18\mu\text{m}$, c-b-e

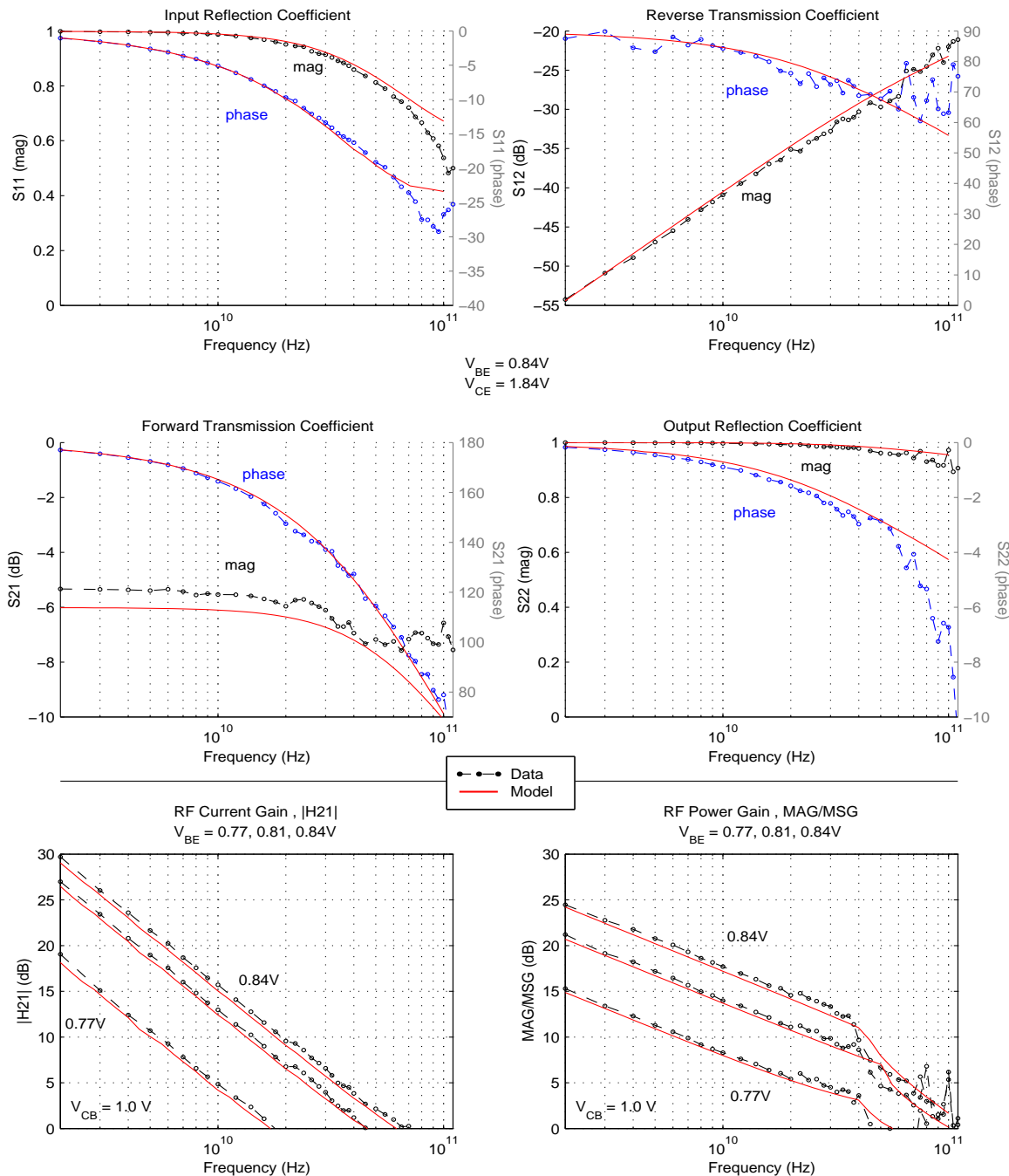
BiCMOS8HP "High-Breakdown NPN" – Typical S-Parameter Characteristics (25C)
Emitter Size: $0.12\ \mu\text{m} \times 0.52\ \mu\text{m} \times 1$, Topology: CBEBEC



Wafer Parametrics: $\text{ndelrx} = -0.060\text{u}$, $\text{nrdb} = 4.5\text{k}$, $\text{nrea} = 1.98$, $\text{nisahb} = 8.806\text{u}$, $\text{nisphb} = 1.246\text{p}$, $\text{nibeiahb} = 33.40\text{n}$, $\text{nibeiphb} = 206\text{e}-18$, $\text{ntfthb} = 1.00\text{p}$

Figure 59. HB NPN S-Parameter Characteristics for $0.12\ \mu\text{m} \times 0.52\ \mu\text{m}$, c-b-e-b-c

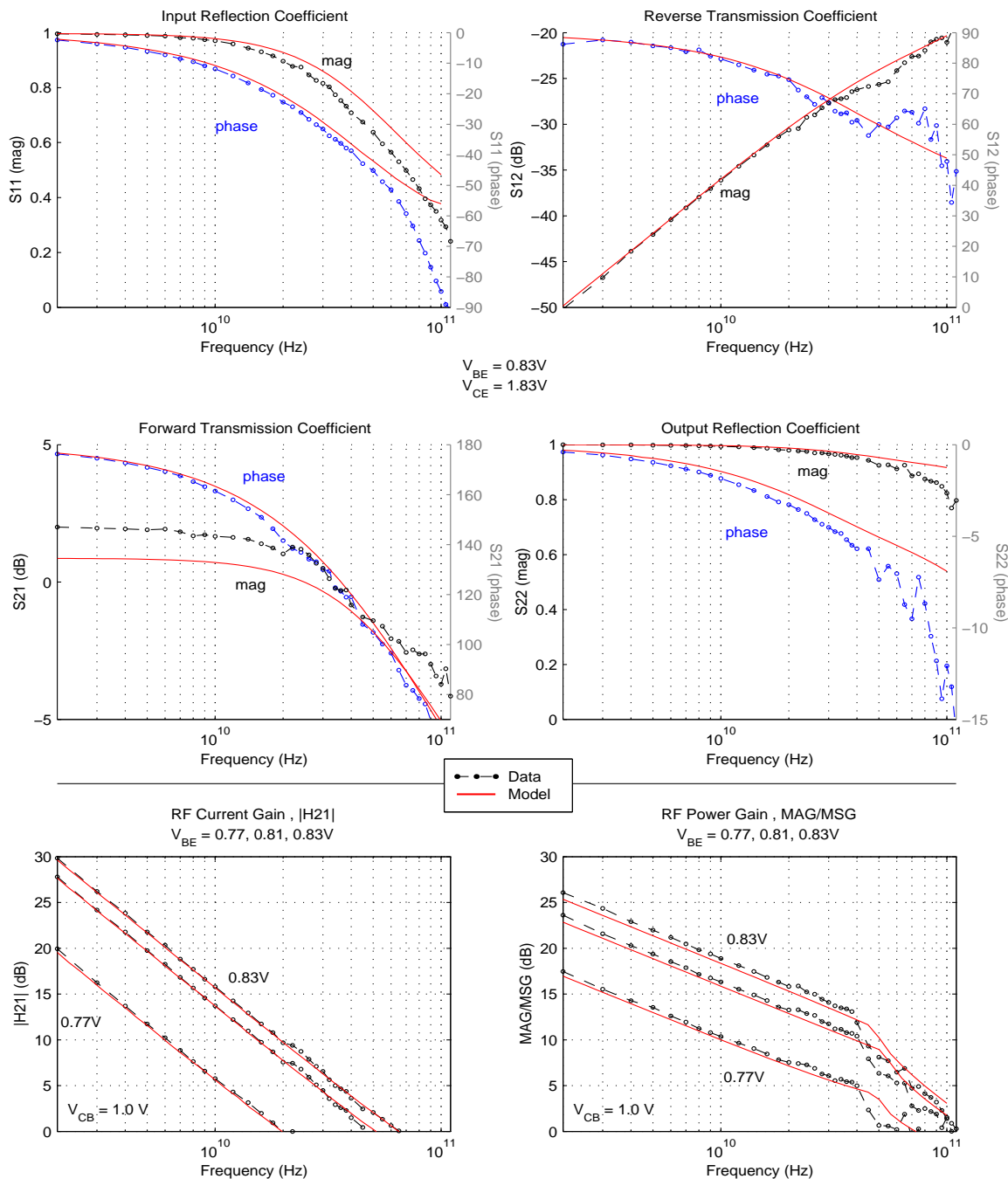
BiCMOS8HP "High-Breakdown NPN" – Typical S-Parameter Characteristics (25C)
Emitter Size: $0.12\ \mu\text{m} \times 1.0\ \mu\text{m} \times 1$, Topology: CBEB



Wafer Parametrics: $\text{ndelrx} = -0.060\text{u}$, $\text{nrd} = 4.5\text{k}$, $\text{nrea} = 1.98$, $\text{nisahb} = 8.806\text{u}$, $\text{nispbh} = 1.246\text{p}$, $\text{nibeiahb} = 33.40\text{n}$, $\text{nibeipbh} = 206\text{e-18}$, $\text{ntfthb} = 1.00\text{p}$

Figure 60. HB NPN S-Parameter Characteristics for $0.12\ \mu\text{m} \times 1\ \mu\text{m}$, c-b-e-b-c

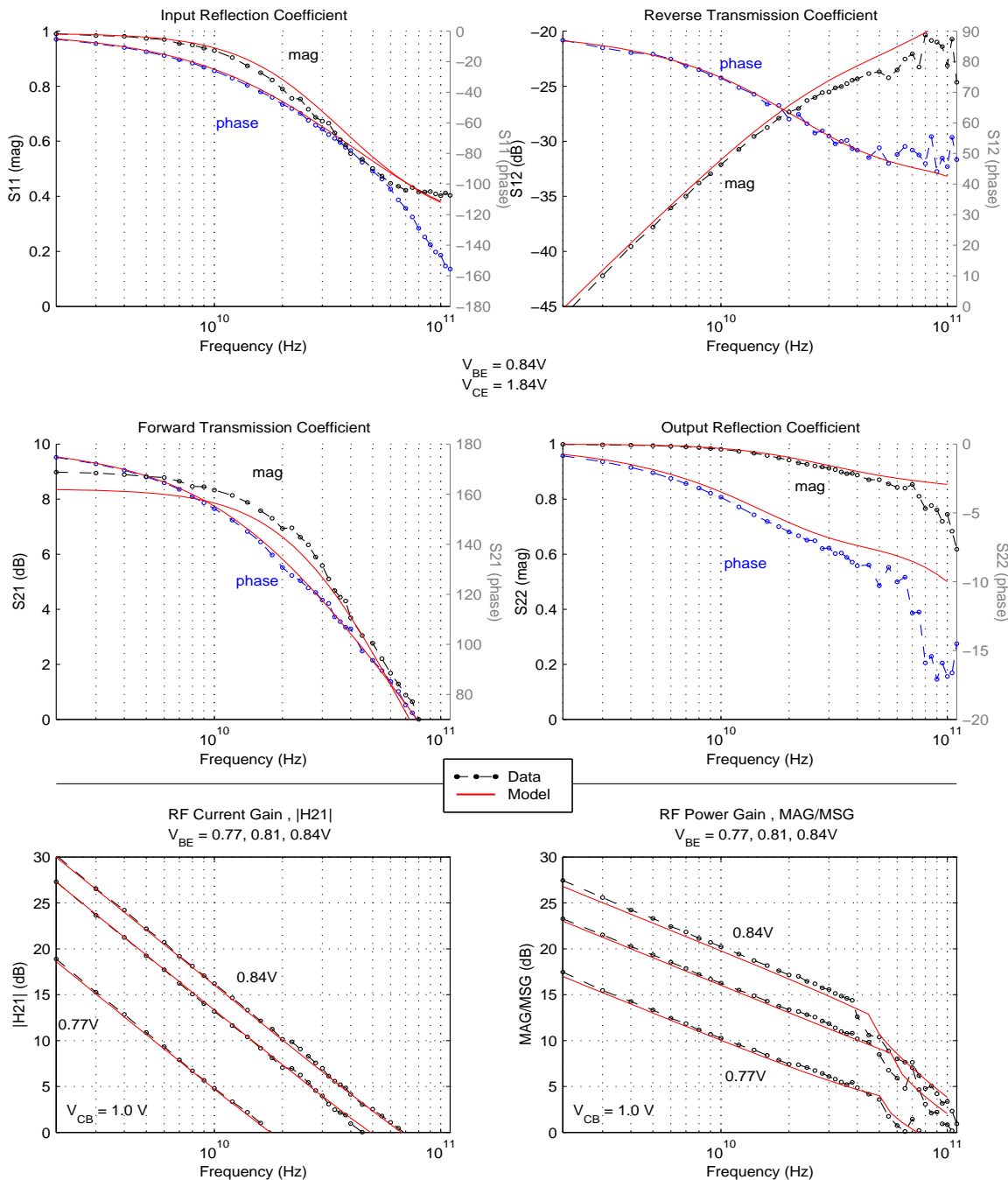
BiCMOS8HP "High-Breakdown NPN" – Typical S-Parameter Characteristics (25C)
Emitter Size: $0.12\ \mu\text{m} \times 2.5\ \mu\text{m} \times 1$, Topology: CBEBc



Wafer Parametrics: ndelrx = -0.060u, nrdb = 4.5k, nrea = 1.98, nisahb = 8.806u, nisphb = 1.246p, nibeiahb = 33.40n, nibeipbh = 206e-18, ntffhb = 1.00p

Figure 61. HB NPN S-Parameter Characteristics for $0.12\ \mu\text{m} \times 2.5\ \mu\text{m}$, c-b-e-b-c

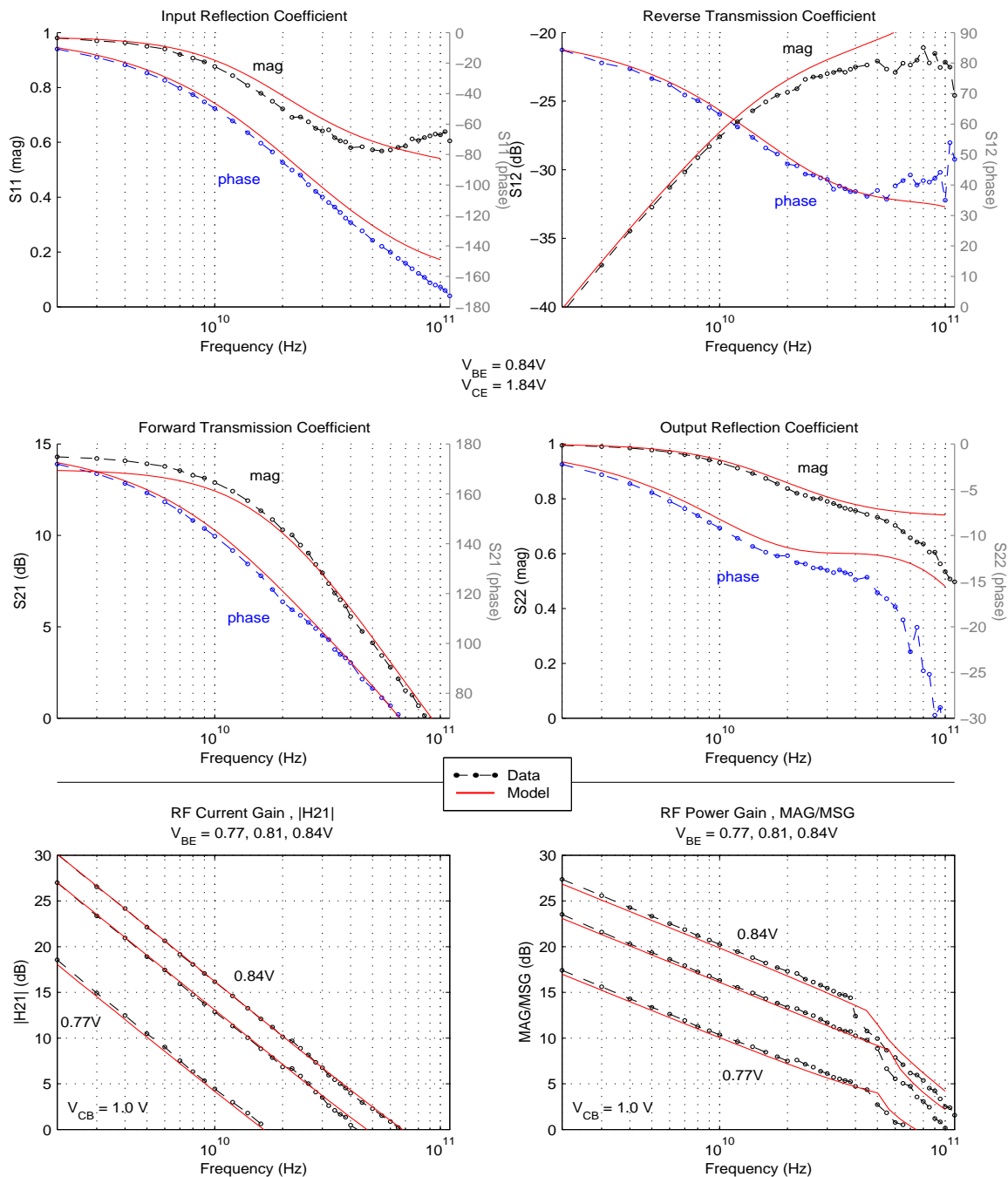
BiCMOS8HP "High-Breakdown NPN" – Typical S-Parameter Characteristics (25C)
Emitter Size: 0.12 μm x 5.0 μm x 1, Topology: CBEB



Wafer Parametrics: ndelrx = -0.060u, nrdb = 4.5k, nrea = 1.98, nisahb = 8.806u, nisphb = 1.246p, nibeiahb = 33.40n, nibeipbh = 206e-18, ntfhb = 1.00p

Figure 62. HB NPN S-Parameter Characteristics for 0.12 μm x 5 μm , c-b-e-b-c

BiCMOS8HP "High-Breakdown NPN" – Typical S-Parameter Characteristics (25C)
Emitter Size: $0.12\ \mu\text{m} \times 10.0\ \mu\text{m} \times 1$, Topology: CBEBc



Wafer Parametrics: $\text{ndelrx} = -0.060\text{u}$, $\text{nrdb} = 4.5\text{k}$, $\text{nrea} = 1.98$, $\text{nisahb} = 8.806\text{u}$, $\text{nisphb} = 1.246\text{p}$, $\text{nibeiahb} = 33.40\text{n}$, $\text{nibeiphb} = 206\text{e}-18$, $\text{ntfthb} = 1.00\text{p}$

Figure 63. HB NPN S-Parameter Characteristics for $0.12\ \mu\text{m} \times 10\ \mu\text{m}$, c-b-e-b-c

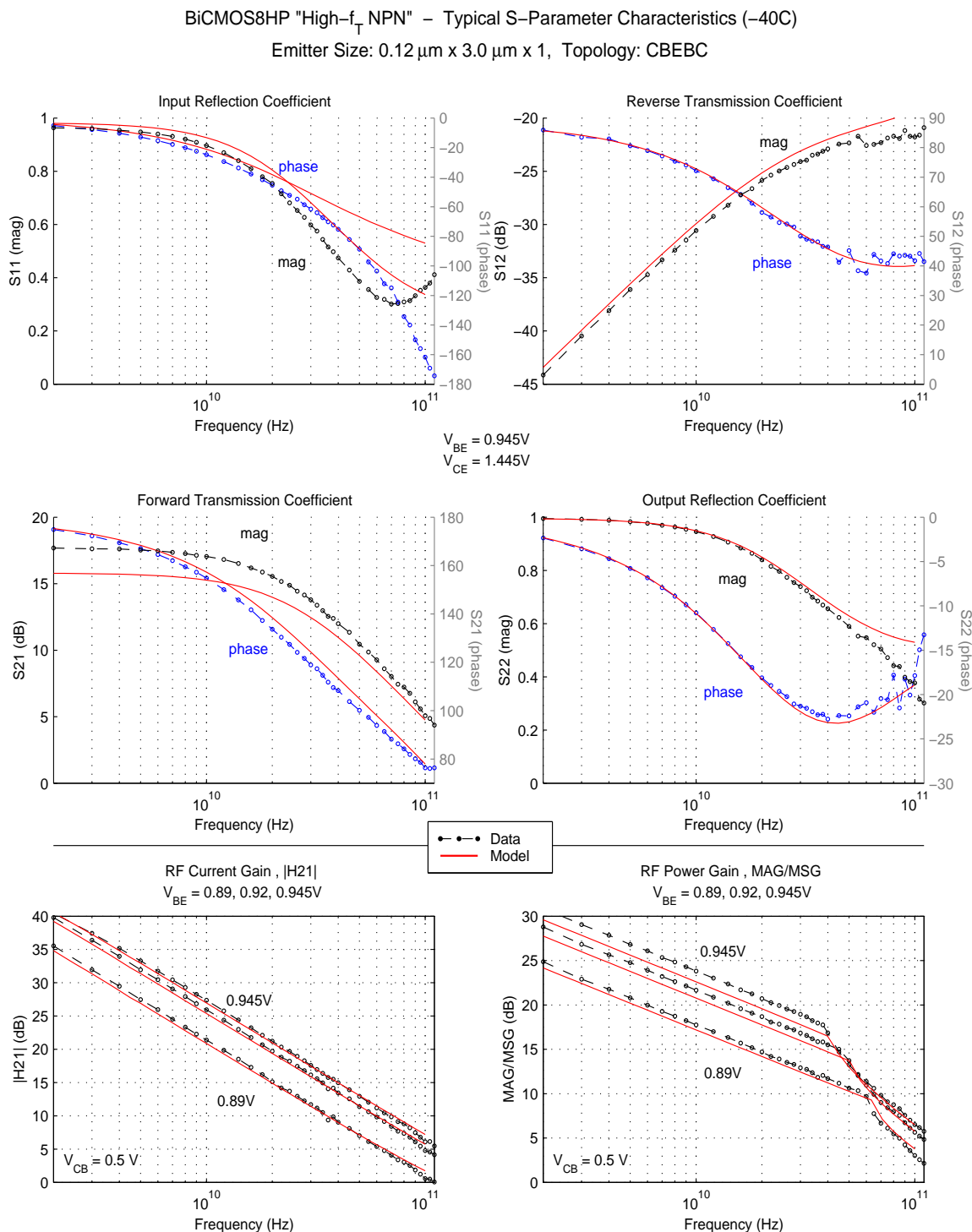
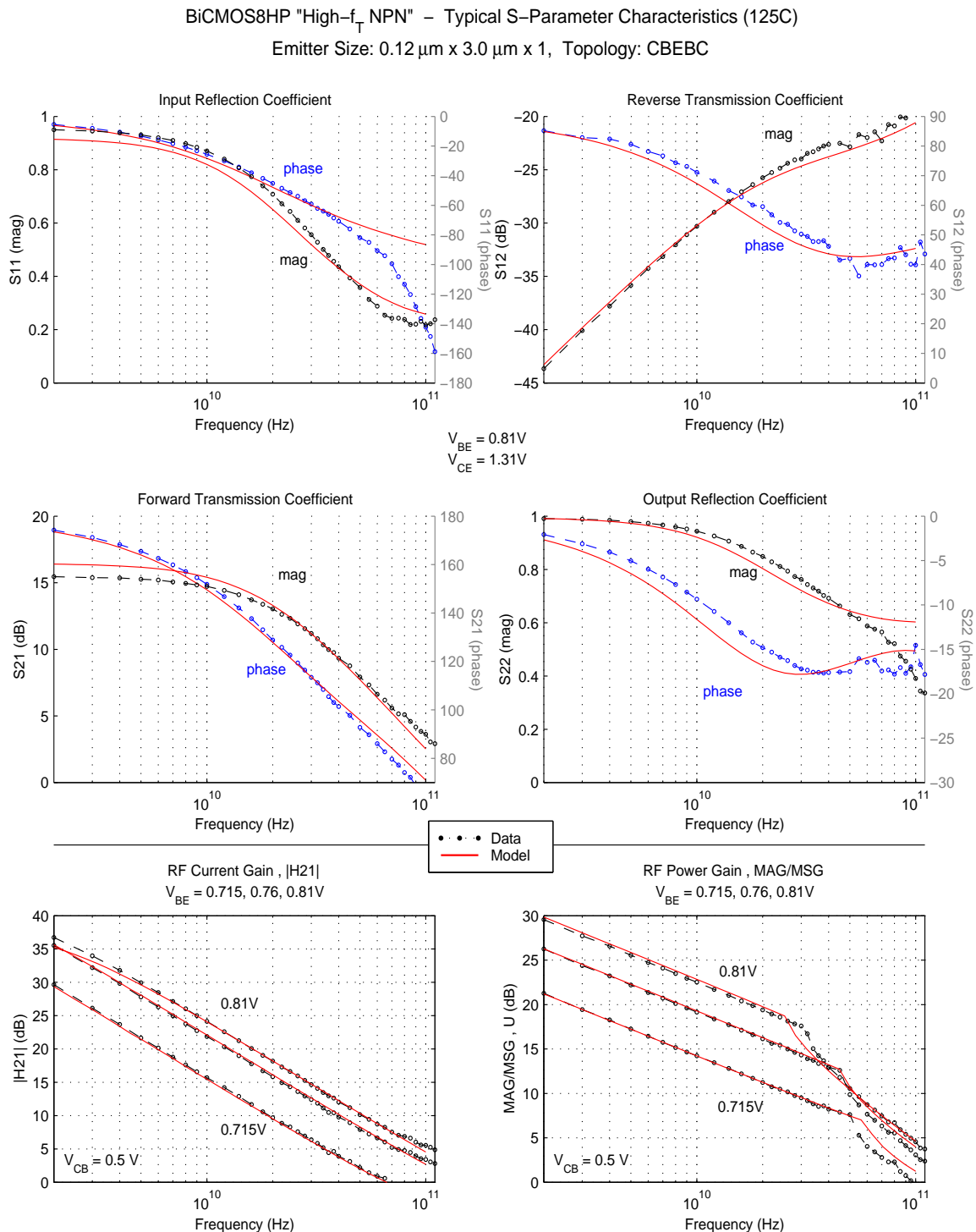


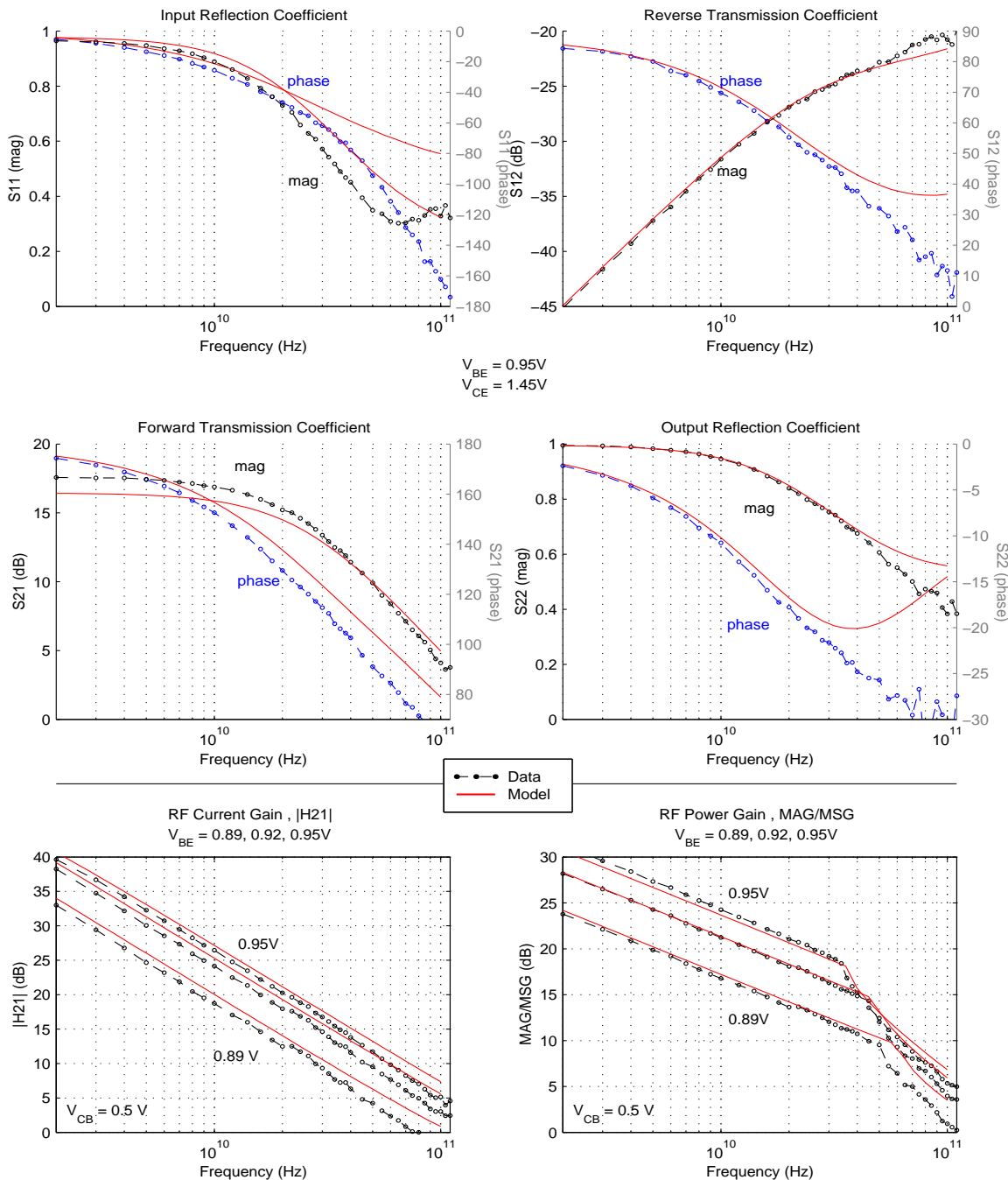
Figure 64. HP NPN S-Parameter Characteristics for 0.12 μm x 3 μm , c-b-e-b-c at -40C



Wafer Parametrics: $\text{ndelrx} = -0.060\text{u}$, $\text{nrd b} = 4.5\text{k}$, $\text{nrea} = 1.98$, $\text{nisa} = 2.14\text{u}$, $\text{nisp} = 1.70\text{p}$, $\text{nibeia} = 26.47\text{n}$, $\text{nibeip} = 5.08\text{e-18}$

Figure 65. HP NPN S-Parameter Characteristics for $0.12\ \mu\text{m} \times 3\ \mu\text{m}$, c-b-e-b-c at 125C

BiCMOS8HP "High- f_T NPN" – Typical S-Parameter Characteristics (-40C)
Emitter Size: 0.12 μm x 3.0 μm x 1, Topology: CBE



Wafer Parametrics: ndelrx = -0.060u, nrdb = 4.5k, nrea = 1.98, nisa = 2.14u, nisp = 1.70p, nibeia = 26.47n, nibeip = 5.08e-18

Figure 66. HP NPN S-Parameter Characteristics for 0.12 μm x 3 μm , c-b-e at -40C

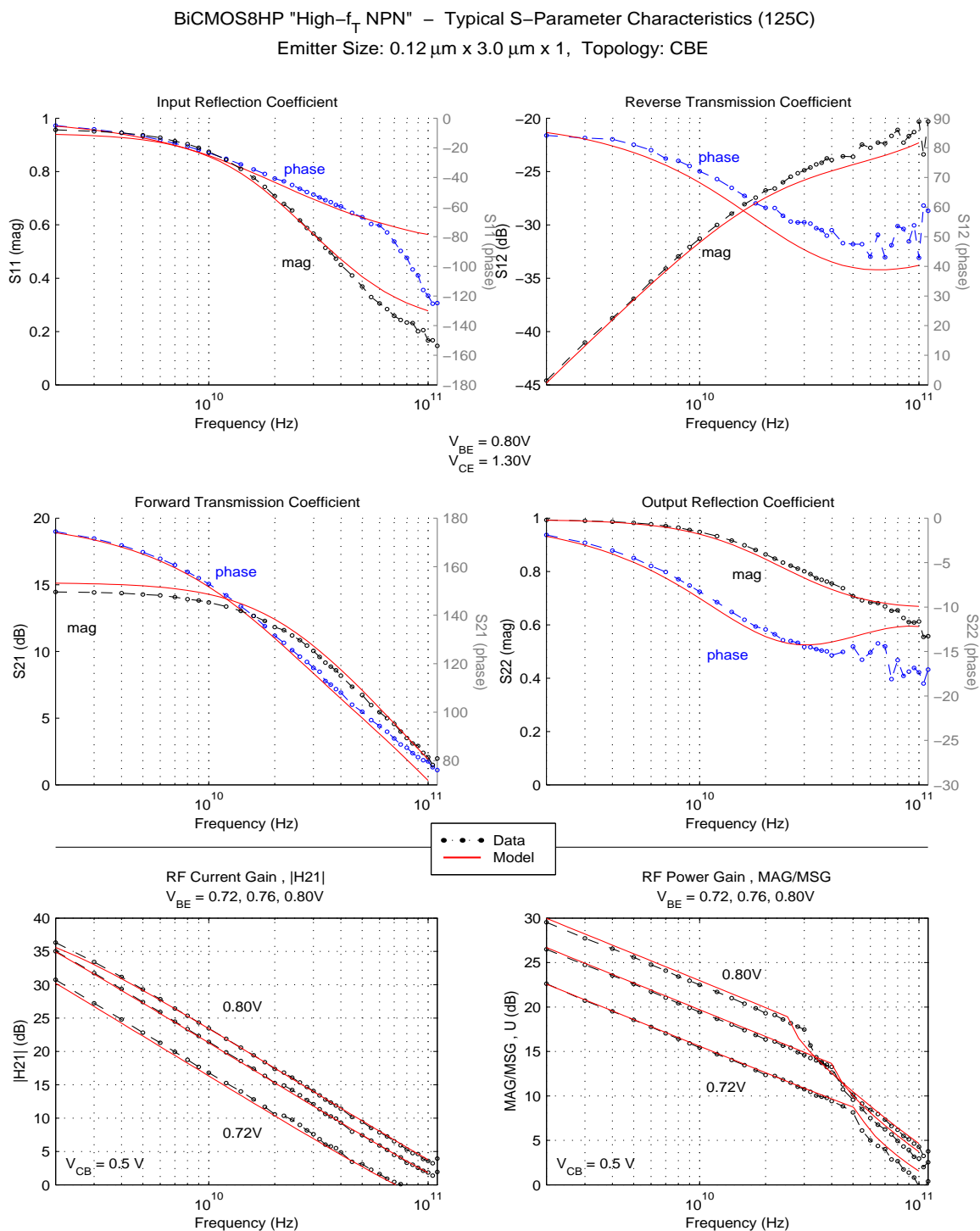
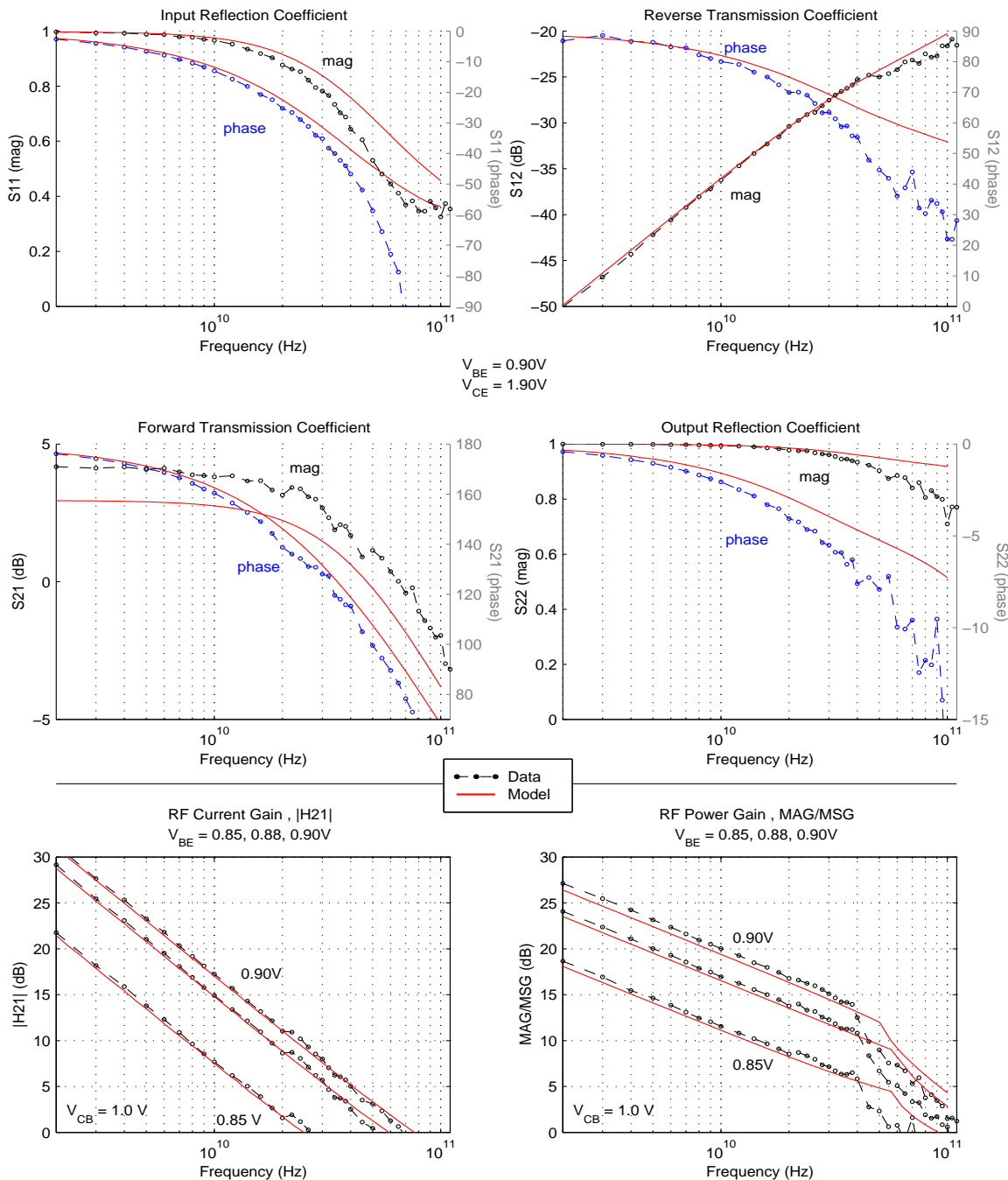


Figure 67. HP NPN S-Parameter Characteristics for $0.12\ \mu\text{m} \times 3\ \mu\text{m}$, c-b-e at 125C

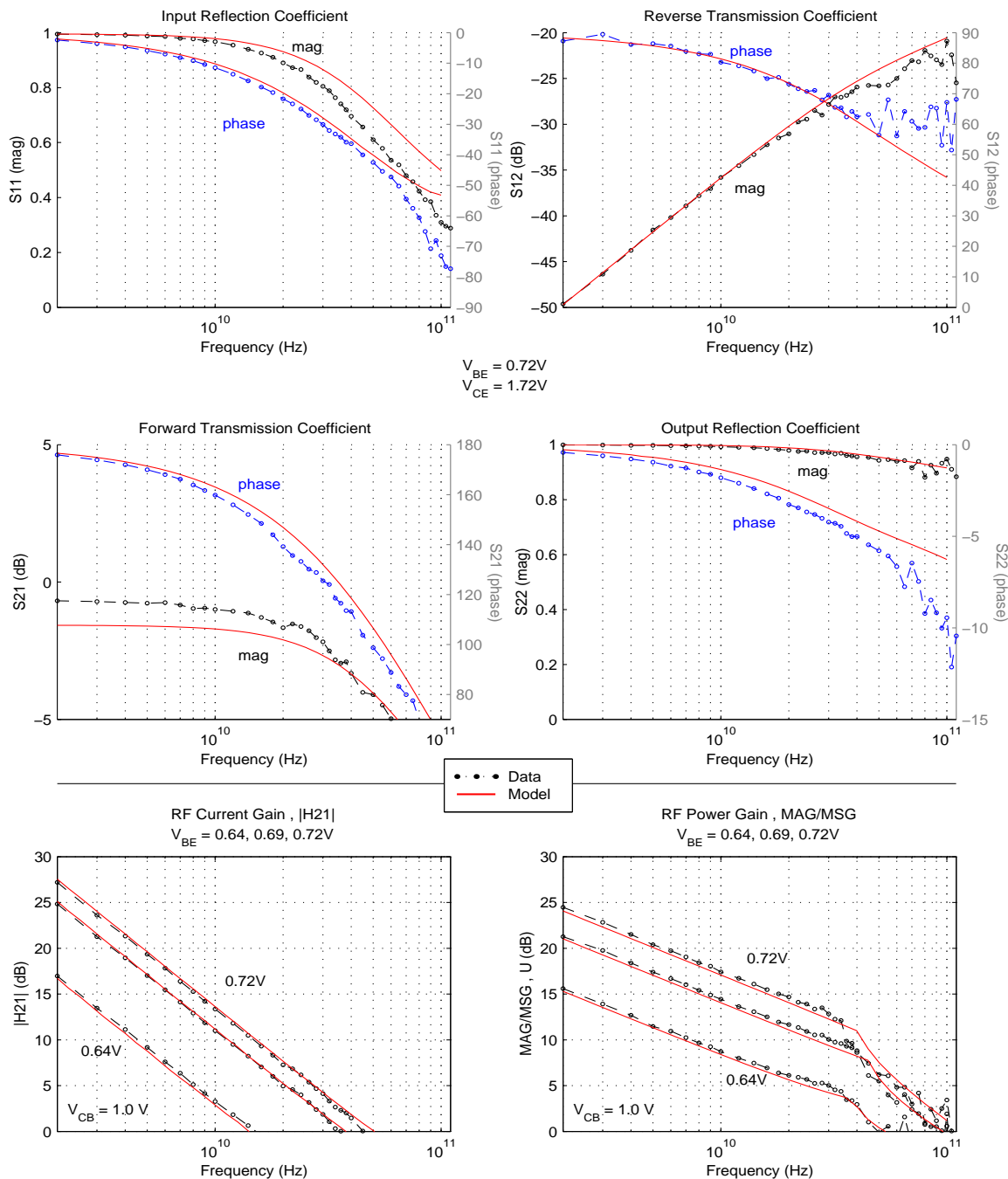
BiCMOS8HP "High-Breakdown NPN" – Typical S-Parameter Characteristics (–40C)
Emitter Size: 0.12 μm x 2.5 μm x 1, Topology: CBECB



Wafer Parametrics: ndelrx = -0.060u, nrdb = 4.5k, nrea = 1.98, nisahb = 8.806u, nisphb = 1.246p, nibeiahb = 33.40n, nibeiphb = 206e-18, ntfhb = 1.00p

Figure 68. HB NPN S-Parameter Characteristics for 0.12 μm x 2.5 μm , c-b-e-b-c at -40C

BiCMOS8HP "High-Breakdown NPN" – Typical S-Parameter Characteristics (125C)
Emitter Size: 0.12 μm x 2.5 μm x 1, Topology: CBEBc



Wafer Parametrics: ndelrx = -0.060u, nrdb = 4.5k, nrea = 1.98, nisahb = 8.806u, nisphb = 1.246p, nibeiahb = 33.40n, nibeipbh = 206e-18, ntffhb = 1.00p

Figure 69. HB NPN S-Parameter Characteristics for 0.12 μm x 2.5 μm , c-b-e-b-c at 125C

3.8 Minimum Noise Figure Data Plots

Noise figure is defined as:

$$NF = \frac{\text{Input S/N ratio}}{\text{Output S/N ratio}}$$

which provides a convenient measure of the signal-to-noise ratio degradation caused by the circuit under investigation.

The noise figure of a circuit can be optimized through careful selection of an appropriate source impedance. The resulting value is referred to as the *minimum noise figure* (NF_{min}). It should be noted that the source impedance resulting in a minimum noise figure does not, in general, coincide with the source impedance providing maximum power gain. Therefore, a trade-off often exists between design for maximum power gain and design for minimum noise figure.

These initial plots show the minimum noise figure for a single geometry HP NPN device:

Table 37. NPN Minimum Noise Figure Plots		
Device Type and Emitter Size	Frequency sweep	Ic sweep
High- f_T (HP): 0.12 x 18, c-b-e-b-c	Fig 70	Fig 71
Note: Noise Figure Plots reflect the SPECTRE model characteristics.		

For the “Ic” frequency sweep figures, the plots are defined as follows:

- The upper left plot shows minimum noise figure.
- The upper right plot shows the associated gain at minimum noise figure.
- The lower left plot shows the noise resistance.
- The lower right plot shows the optimum source reflection coefficient (magnitude and phase) required to obtain minimum noise figure.

The data was obtained using an Agilent 4142 to bias the device through an ATN NP5 Noise parameter measurement system. The raw noise figure was measured at 8 impedance points and the noise parameters were then extracted. Note that the sensitivity of the noise figure meter is quoted at about +/- 0.2 dB. As a result, there is a certain percentage of error in the extracted noise parameters as well.

At low frequencies, the reflection coefficient being close to 1, good impedance matching could not be achieved. Another source of error in the data is that the de-embedding of pads is currently incomplete, so the data shown is almost identical to that measured from the NP5 system.

BiCMOS8HP "High- f_T NPN" – Typical Minimum Noise Figure Characteristics (21C)

Emitter Size: $0.12\ \mu\text{m} \times 18.0\ \mu\text{m} \times 1$, Topology: CBEB

$V_{CB} = 0.5\text{V}$

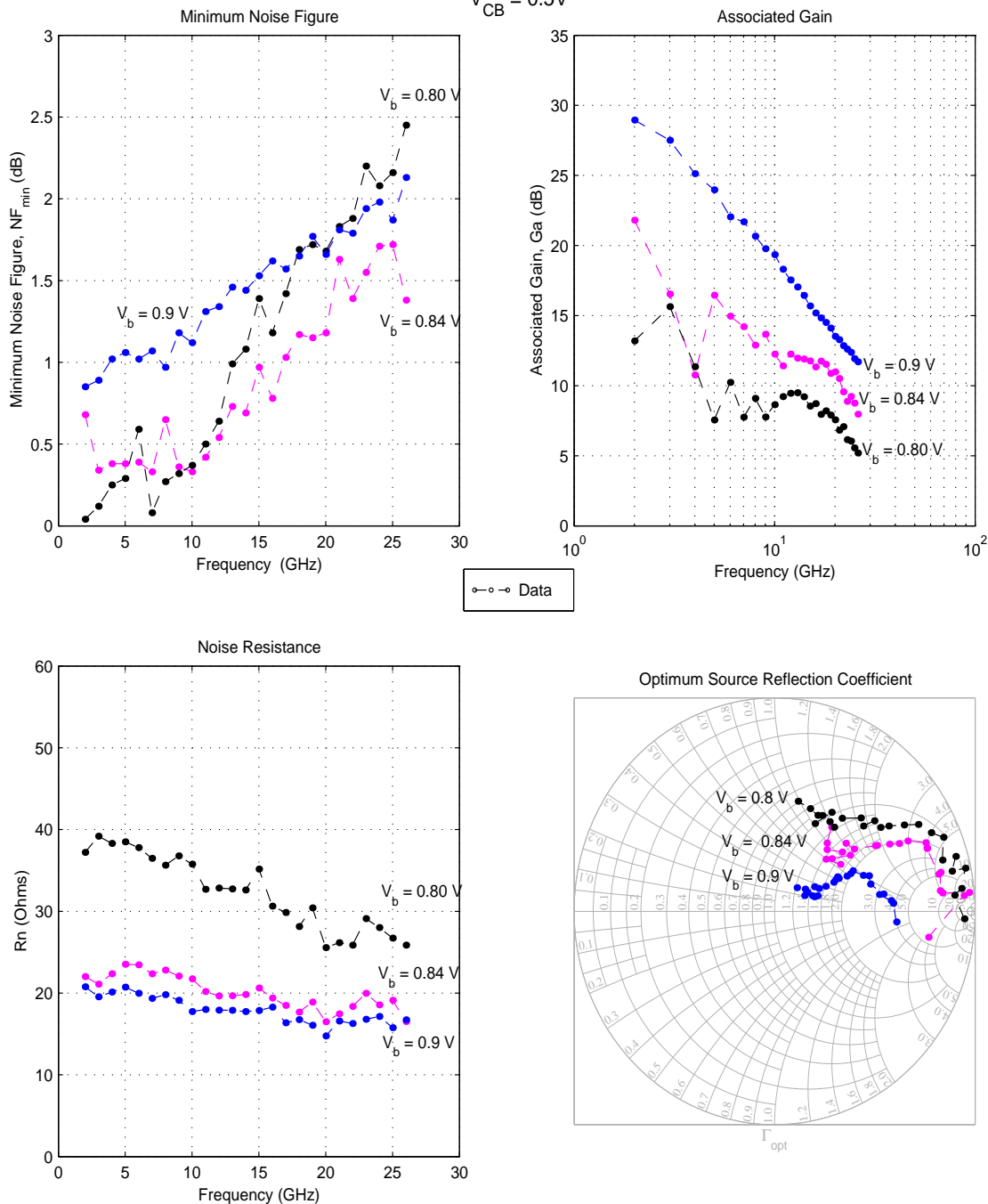


Figure 70. HP NPN Minimum Noise Figure: Frequency Sweep for $0.12\ \mu\text{m} \times 18\ \mu\text{m}$, c-b-e-b-c

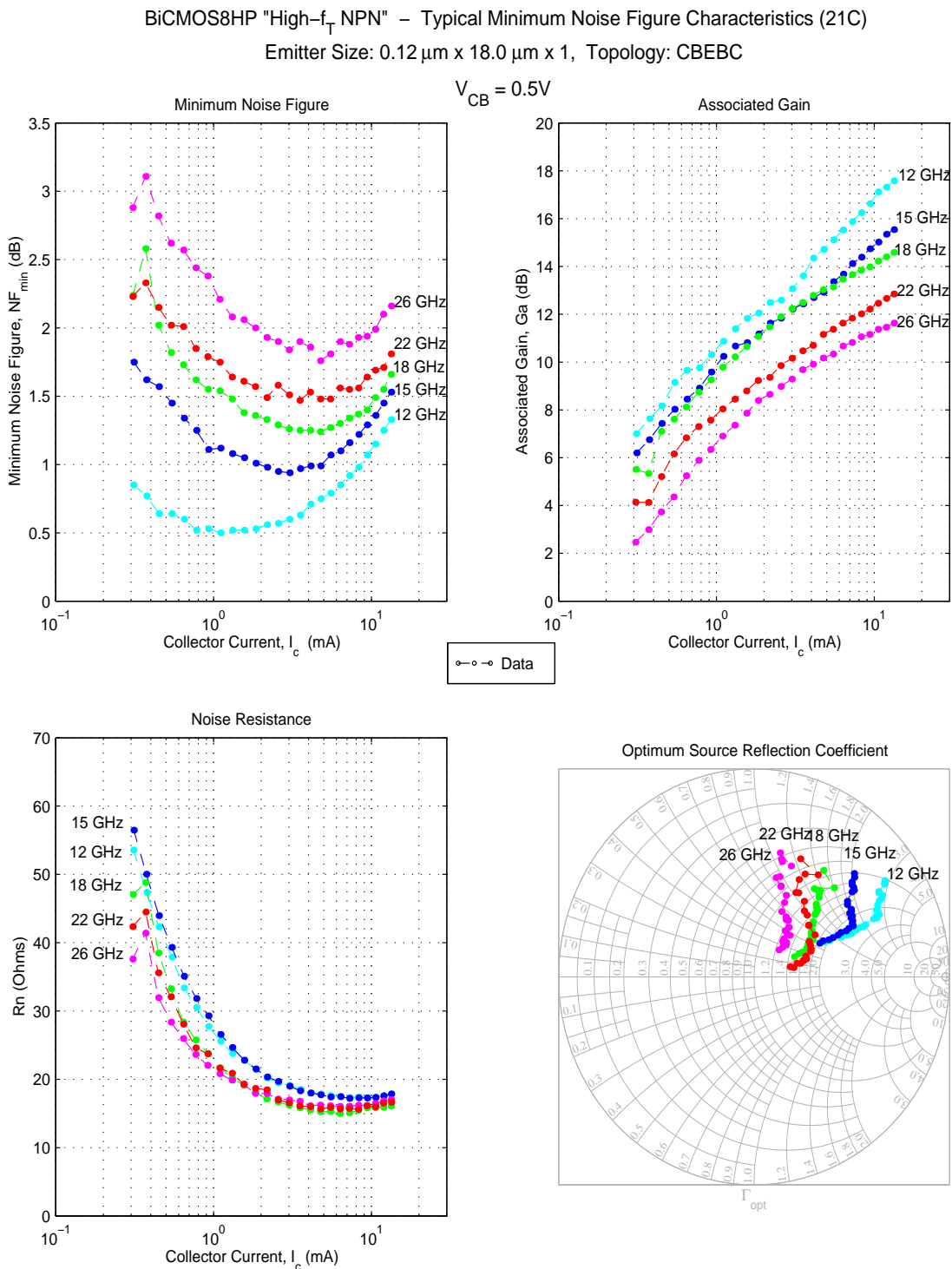


Figure 71. HP NPN Minimum Noise Figure: Bias Sweep for $0.12\ \mu\text{m} \times 18\ \mu\text{m}$, c-b-e-b-c

3.9 1/f Noise Correlation Plots

The data measurements for npn 1/f noise were made on single device test structures with the BTA 9812A Noise Analyzer System. The output noise spectrum plots were generated at fixed base current biases, as noted in each figure.

The following plots illustrate the model-to-hardware correlation for 1/f noise:

Table 38. NPN 1/f Noise Plots			
Characteristic	High- f_T (HP) c-b-e-b-c	High- f_T (HP) c-b-e	High-Breakdown (HB) c-b-e-b-c
1/f Noise vs. Ib and Vcb Bias	Fig 72	Fig 73	Fig 74
1/f Noise vs. Emitter Geometry	data not available	data not available	data not available
Note: 1/f Noise Plots reflect the SPECTRE model characteristics.			

Note that the model gives a reasonable fit across base current bias for all device types and is also able to predict the slight increase observed in the output noise spectrum as the Vce bias nears the weak avalanche region for the high-breakdown (HB) npn.

3.10 BVcer Measurements

While the DC correlation plots shown earlier in this chapter contain output characteristics at various forced base currents and the BiCMOS-8HP Design Manual lists the open base C-E breakdown voltage (BVceo) spec, many circuit applications use a common emitter with forced Vbe configuration and an external base resistance in series with the device.

It is interesting to note that the breakdown voltage for this configuration decreases with increasing current level due to the debiasing effect, which gets more pronounced as the emitter current level increases, leading to a steeper slope and thus a lower breakdown voltage. In addition, the ratio between the amount of holes exiting the device and those recombining with the electrons depends on the external base impedance attached to the device. A lower base impedance tends to increase the amount of holes coming out of the device resulting in a decrease in the C-E breakdown voltage as the base impedance increases.

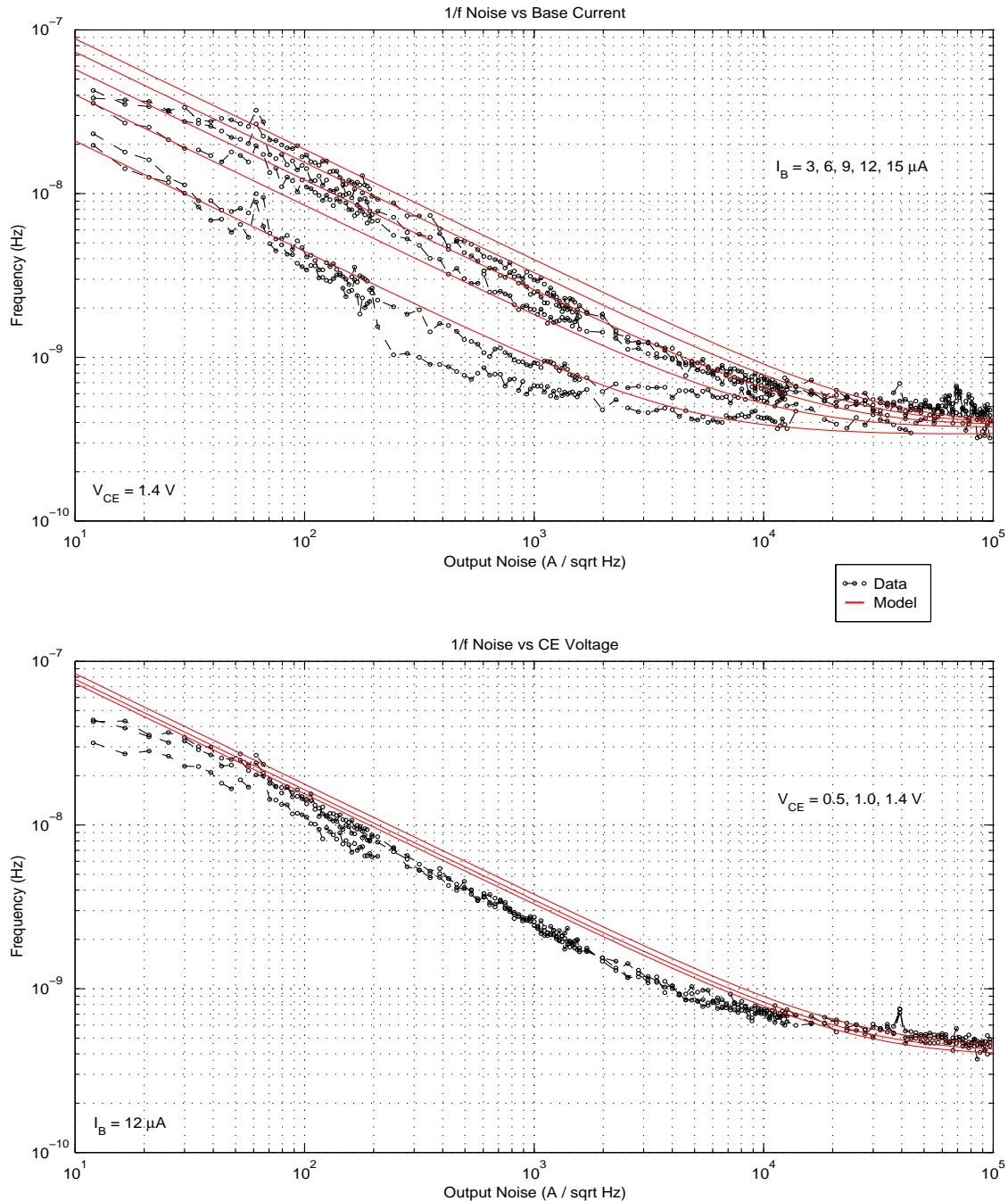
The plots in **Fig 75** contain BVcer measurement data for a single emitter geometry High- f_T , and High-Breakdown NPN. Each device was measured with a 500 ohm current limiting collector resistor and a series of Vbe biases (0.72, 0.74, 0.76V).

- The left hand figures show a comparison of the data vs model simulation for the case of an external base resistance of 1kohm and a 0.12 μ m x 3.0 μ m x 1 emitter size.
- The right hand figures contain measurement data only for each device type with a series of external base resistance values (100, 1k, and 10k ohms) for the same emitter size.

Note that the expected dependence between the external base resistance and C-E breakdown voltage can be observed in each of the plots and that this breakdown voltage is approaching BVceo for the case where Rb=10 kohm.

BiCMOS8HP "High- f_T NPN" – Typical 1/f Noise Characteristics (25°C)

Emitter Size: 0.12 μm x 3.0 μm x 1, Topology: CBEB

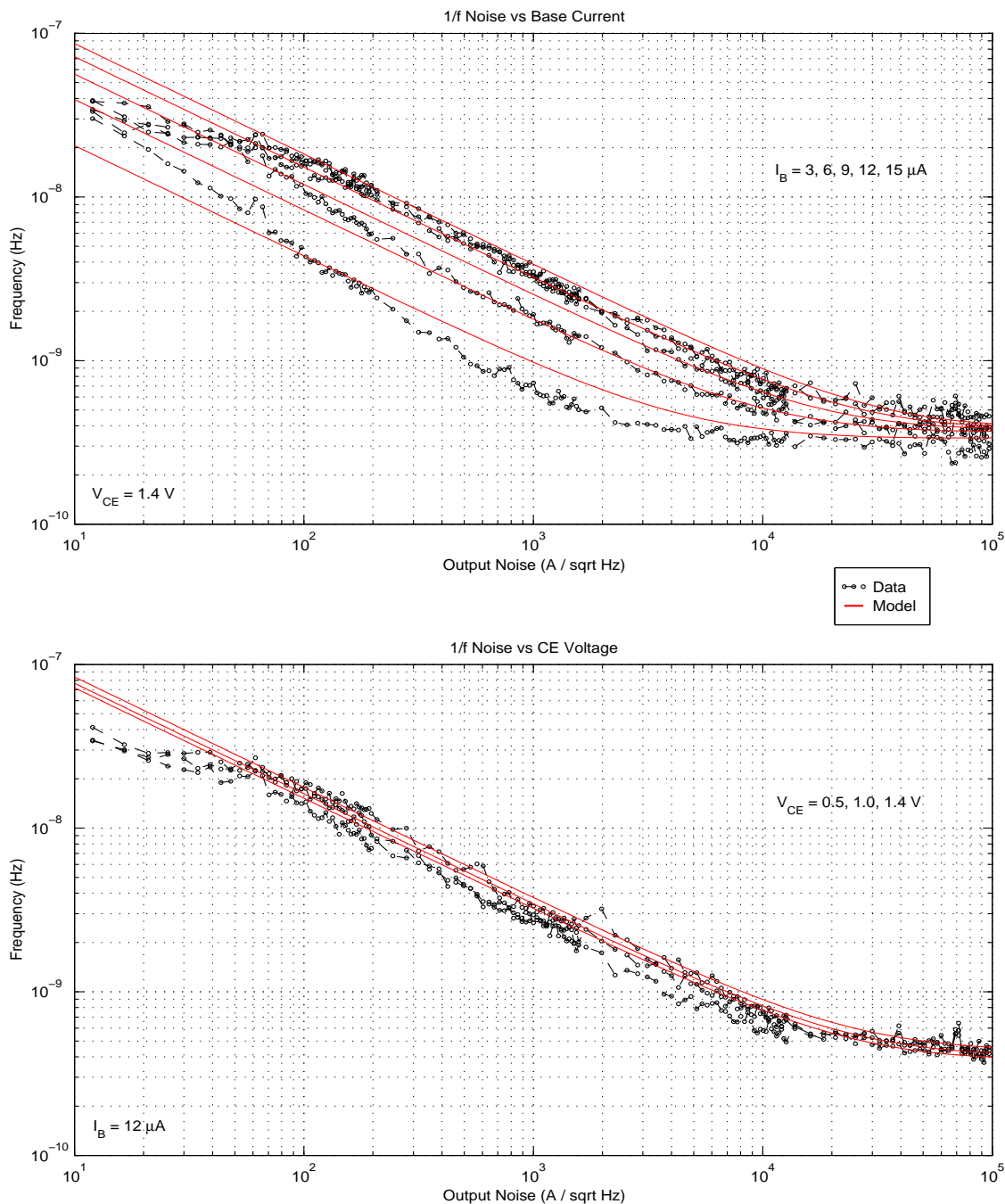


Wafer Parametrics: $\text{ndelrx} = -0.060\text{u}$, $\text{nrdb} = 4.5\text{k}$, $\text{nrea} = 1.98$, $\text{nisa} = 2.14\text{u}$, $\text{nisp} = 1.70\text{p}$, $\text{nibeia} = 26.47\text{n}$, $\text{nibeip} = 5.08\text{e-18}$

Figure 72. HP NPN 1/f Noise Characteristics

BiCMOS8HP "High- f_T NPN" – Typical 1/f Noise Characteristics (25C)

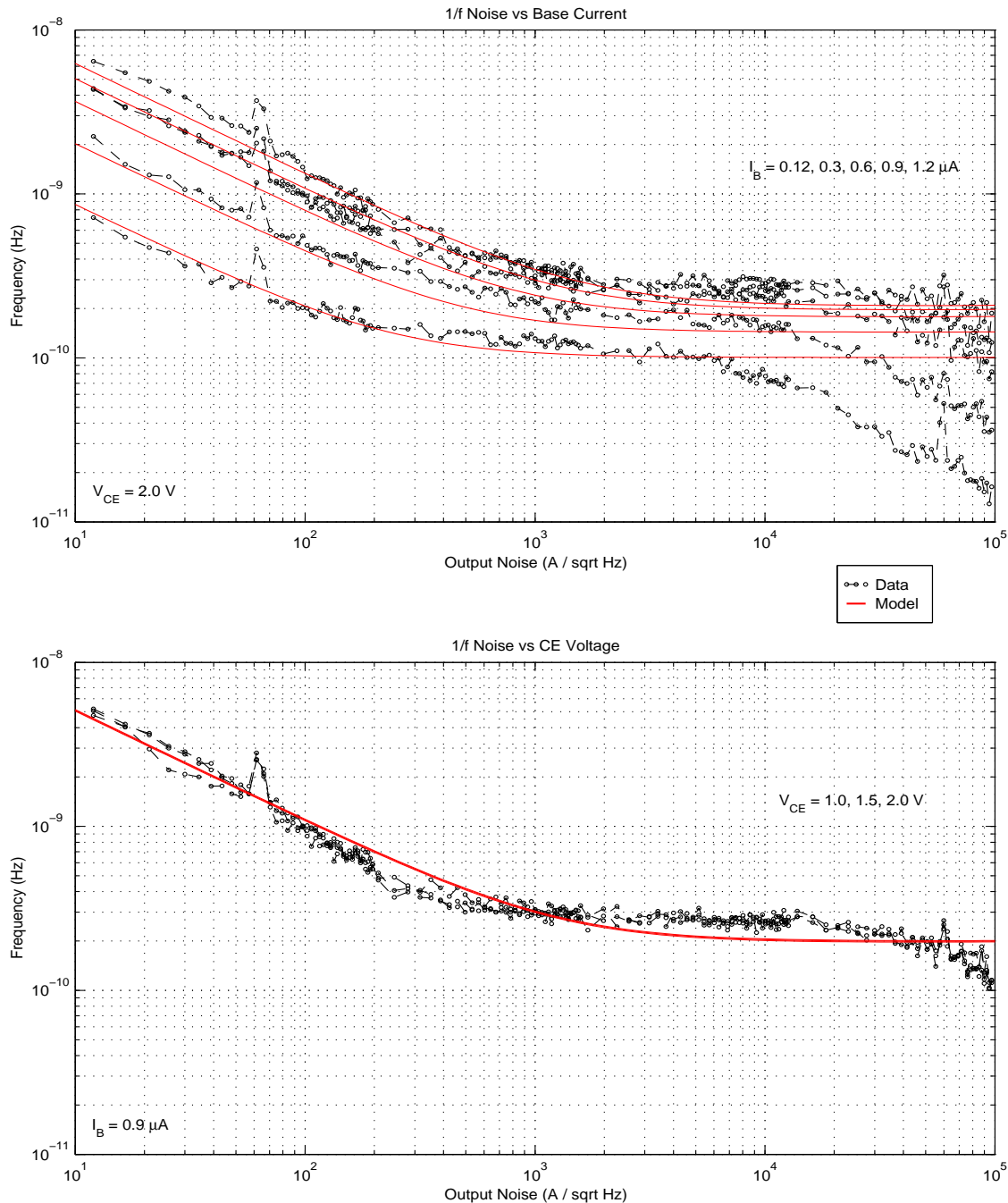
Emitter Size: 0.12 μm x 3.0 μm x 1, Topology: CBE



Wafer Parametrics: $\text{ndelrx} = -0.060\text{u}$, $\text{nrd b} = 4.5\text{k}$, $\text{nrea} = 1.98$, $\text{nisa} = 2.14\text{u}$, $\text{nisp} = 1.70\text{p}$, $\text{nibeia} = 26.47\text{n}$, $\text{nibeip} = 5.08\text{e-18}$

Figure 73. MP NPN 1/f Noise Characteristics

BiCMOS8HP "High-Breakdown NPN" – Typical 1/f Noise Characteristics (25C)
Emitter Size: 0.12 μm x 3.0 μm x 1, Topology: CBECB



Wafer Parametrics: $\text{ndelrx} = -0.060\text{u}$, $\text{nrd} = 4.5\text{k}$, $\text{nrea} = 1.98$, $\text{nisahb} = 8.806\text{u}$, $\text{nisphb} = 1.246\text{p}$, $\text{nibeiahb} = 33.40\text{n}$, $\text{nibeipbh} = 206\text{e-18}$, $\text{ntfbb} = 1.00\text{p}$

Figure 74. HB NPN 1/f Noise Characteristics

BiCMOS8HP NPN – Typical BV_{CER} Characteristics (25C)

Emitter Size: 0.12 μm x 3.0 μm x 1, Topology: CBEBc

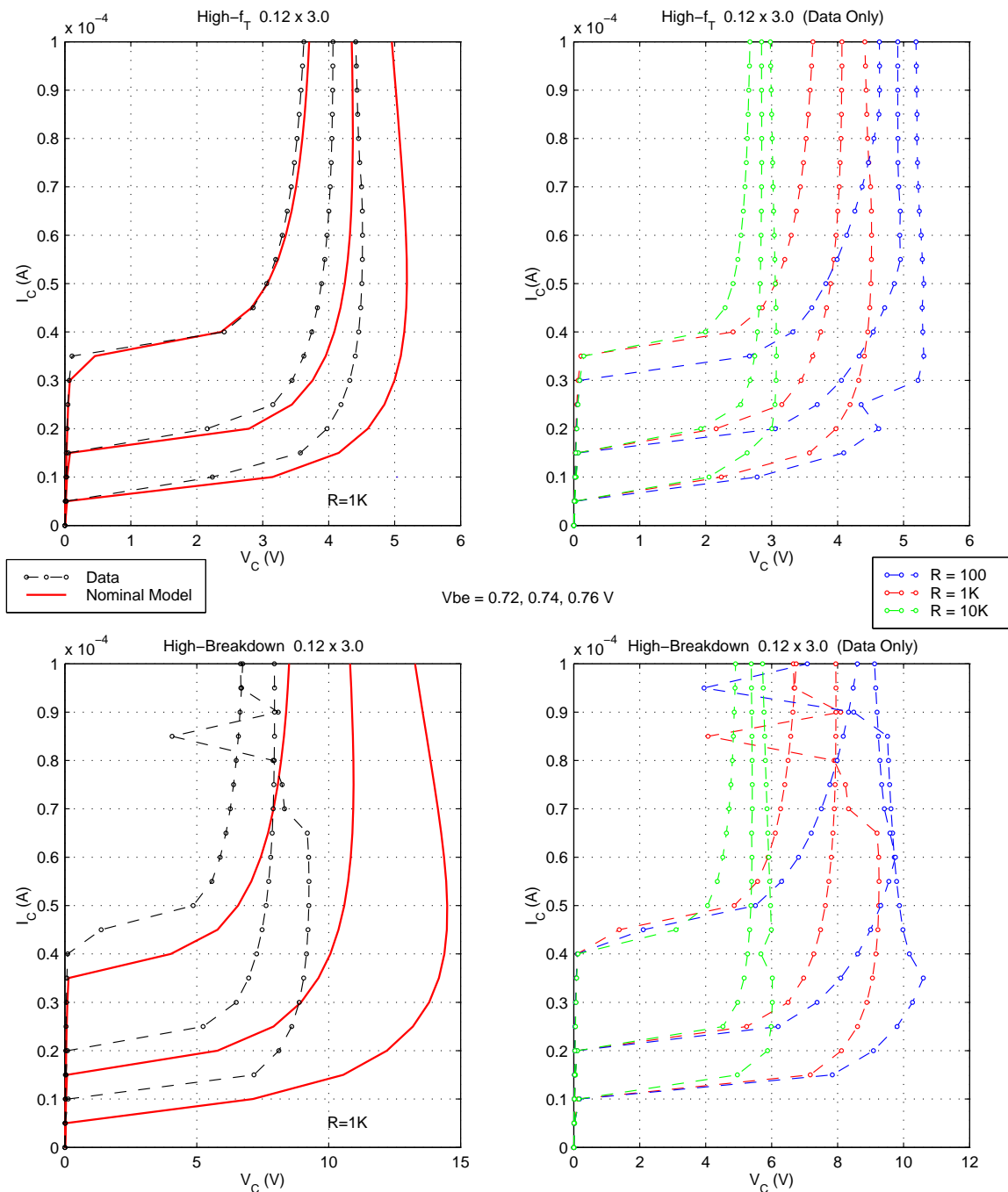


Figure 75. HP and HB NPN BV_{cer} Characteristics for 0.12 μm x 3.0 μm , c-b-e-b-c

4.0 VPNP Models

4.1 Model Features

The HSPICE and Spectre vnp subcircuit includes the VBIC model as the core element which provides built-in support for the following features:

- Parasitic vertical NPN to substrate
- Weak avalanche multiplication (impact ionization)
- Self-heating approximation (dV_{be}/dT)
- Fixed oxide capacitances for the emitter-base and collector-base junctions
- Quasi-saturation modeling
- Improved Early effect modeling (as compared to the standard Gummel-Poon model)

The models have optional switches to turn-off the impact ionization effect. By default, this option is active and the model was optimized using this feature. If the switch is not enabled, the output characteristics of the model will not represent hardware measurements as accurately. The switch may help improve simulation time by allowing the designer to de-activate this option for non-critical devices.

4.2 Model Limitations and Restrictions

Modeling of the reverse base-emitter junction breakdown is not included in the vnp models as it is not supported by the VBIC equations.

The vnp models support single and dual stripe emitter geometries only. The models assume a c-b-e single emitter layout and a c-b-e-b-c-b-e-b-c dual emitter device layout as represented in the device library pcells within the design kit environment. The reasons for this limitation are:

- At the high current densities allowed in this technology, center fingers of a multi-emitter device would be at a higher temperature than the outer fingers. With the exponential dependence of the collector current, the center fingers would conduct more current and could cause reliability concerns (or catastrophic failure in extreme cases).

4.3 Device Parameter Reference Tables

The following table provides a quick reference for designers to assess the device parasitics associated with several sample device sizes, as listed. The geometries include examples of both emitter widths with the same emitter length, and single and dual emitter stripes for a given width/length.

Table 39. VPNP Device Parameter Comparison

Device Parameter	Drawn Emitter Dimensions (μm)						
	0.4 x 1.2 x 1	0.4 x 2.5 x 1	0.4 x 20 x 1	0.4 x 20 x 2	0.8 x 2.5 x 1	0.8 x 5 x 1	0.8 x 20 x 1
Extrinsic Re (ohms)	85.7	39.2	4.7	2.36	20.6	10.2	2.55
Extrinsic Rb (ohms)	208.1	137.8	24.8	6.2	123.5	78.0	24.3
Intrinsic Rb (ohms)	179.2	96.3	13.0	6.5	169.2	94.5	25.5
Extrinsic Rc (ohms)	267.5	216.8	68.7	56.6	210.0	158.9	67.8
Intrinsic Rc (ohms)	1.90k	1.14k	176.1	88.1	921.3	519.1	143.0
BE intrinsic cap (fF)	3.18	6.47	50.7	101.4	10.1	19.4	75.3
BE oxide cap (fF)	0.95	1.42	7.75	15.5	1.56	2.46	7.9
BC extrinsic cap (fF)	1.58	2.29	12.0	23.9	2.5	3.9	12.2
BC intrinsic cap (fF)	0.39	0.78	6.1	12.1	1.17	2.22	8.5
BC oxide cap (fF)	1.10	1.49	6.8	17.8	1.57	2.33	6.9
CS intrinsic cap (fF)	43.1	51.3	161.6	266.4	54.5	71.1	171.0

4.4 Device Mis-Match Reference Tables

The following tables provide a comparison of adjacent device Vbe and Beta mis-match for a select set of emitter sizes. The tables also show hardware data results used to set the mis-match scaling in the models.

The data results are based on a sample of 30 sites from 20-24 wafers from 12 separate hardware lots. The data analysis programs first calculate the “per wafer 3-sigma” mis-match for each wafer measured. The “typical” mis-match results, as quoted in the table and used to set the model mis-match, are based on the mean of these “per wafer 3-sigma” values. The “data variation sigma” column represents the 1-sigma variation observed in the “per wafer 3-sigma” values (sample size=20, or 24).

Note: The general trend of the models is to predict a slightly higher 3-sigma mis-match than the calculated data results. The models have been set in this conservative manner due to the relatively small sample size of data available.

<i>Table 40. VPNP Adjacent Device Vbe Mis-Match</i>				
Emitter W x Lx #E	I_{bias}	Model Vbe mis-match (mV)	Data Typical (mV)	Data variation 1-sigma (mV)
0.4 x 1.2 x 1	1.44 μ A	1.28	1.03	+/- 0.29
	144 μ A	2.88	2.44	+/- 1.08
0.4 x 2.5 x 1	1.8 μ A	0.94	0.71	+/- 0.22
	180 μ A	1.96	1.38	+/- 0.37
0.4 x 5 x 1	6.0 μ A	0.70	0.54	+/- 0.11
	600 μ A	1.40	1.0	+/- 0.26
0.4 x 10 x 1	12 μ A	0.53	0.38	+/- 0.08
	1.2 mA	1.02	0.76	+/- 0.27
0.4 x 20 x 1	24 μ A	0.40	0.37	+/- 0.12
	2.4 mA	0.75	0.68	+/- 0.18
0.8 x 2.5 x 1	6.0 μ A	0.50	0.44	+/- 0.09
	600 μ A	1.31	1.0	+/- 0.34
0.8 x 3 x 1	7.2 μ A	0.46	0.45	+/- 0.07
	720 μ A	1.23	0.94	+/- 0.27
0.8 x 5 x 1	12 μ A	0.39	0.35	+/- 0.04
	1.2 mA	1.02	0.80	+/- 0.24
0.8 x 10 x 1	24 μ A	0.31	0.27	+/- 0.04
	2.4 mA	0.80	0.67	+/- 0.20
0.8 x 20 x 1	48 μ A	0.24	0.21	+/- 0.05
	4.8 mA	0.63	0.62	+/- 0.17

Table 41. VPNP Adjacent Device Beta Mis-Match

Emitter W x Lx #E	I_{bias}	Model Beta mis-match	Data Typical	Data variation 1-sigma
0.4 x 1.2 x 1	1.44 μ A	12.6 %	11.8 %	+/- 3.1 %
0.4 x 2.5 x 1	3.0 μ A	8.36 %	7.15 %	+/- 1.3 %
0.4 x 5 x 1	6.0 μ A	5.76 %	4.93 %	+/- 1.05 %
0.4 x 10 x 1	12 μ A	4.0 %	3.5 %	+/- 0.53 %
0.4 x 20 x 1	24 μ A	2.8 %	2.62 %	+/- 0.46 %
0.8 x 2.5 x 1	6.0 μ A	5.48 %	4.96 %	+/- 0.56 %
0.8 x 3 x 1	7.2 μ A	5.03 %	4.59 %	+/- 0.73 %
0.8 x 5 x 1	12 μ A	4.0 %	3.5 %	+/- 0.50 %
0.8 x 10 x 1	24 μ A	2.91 %	2.63 %	+/- 0.53 %
0.8 x 20 x 1	48 μ A	2.12 %	2.0 %	+/- 0.53 %

4.5 DC Correlation Plots

The following series of plots compares the DC characteristics of the vnp model with measurements from the initial device hardware. As the model supports a range of emitter widths and lengths, the plots show the model correlation for a few select device sizes.

Table 42. VNP DC Correlation Plots					
Emitter Length and # Stripes L x #E	Emitter Width = 0.40 μ m		Emitter Length and # Stripes L x #E	Emitter Width = 0.80 μ m	
	I _B bias	Figure		I _B bias	Figure
1.2 x 1	1.73 μ A	Fig 76	2.5 x 1	7.2 μ A	Fig 83
2.5 x 1	3.6 μ A	Fig 77	3 x 1	8.6 μ A	Fig 84
4.2 x 1	6.05 μ A	Fig 78	5 x 1	14.4 μ A	Fig 85
10 x 1	14.4 μ A	Fig 79	10 x 1	28.8 μ A	Fig 86
10 x 2	28.8 μ A	Fig 80	10 x 2	57.6 μ A	Fig 87
20 x 1	28.8 μ A	Fig 81	20 x 1	57.6 μ A	Fig 88
20 x 2	57.6 μ A	Fig 82	20 x 2	115.2 μ A	Fig 89

Each of the figures contains the following:

- The plots in the top row of the figure are generated from forward (V_{be} sweep, V_{cb}=0V) and reverse (V_{bc} sweep, V_{eb}=0V) gummel measurements. The left and right plots depict the node currents vs voltage. The center plot shows the forward and reverse current gain (beta) vs current.
- The remaining plots in the figure are generated from a sweep of V_{ce} for a series of fixed base currents, which are defined as 0.05, 0.25, 0.5, 0.75, 1.0 and 1.25 x the I_B bias value listed in the table.
- The left plot in the middle row shows collector current vs V_{ce}. The middle plot in this row depicts the output conductance (g₀). The region from low-to-mid V_{ce} biases illustrates the quasi-saturation effects in these devices. Plots located in the bottom row show base-emitter voltage vs V_{ce} and substrate current at low V_{ce} (saturation region). The decrease in V_{be} with increasing V_{ce} is due to the self-heating.

Along with the nominal temperature (25C) plots, DC characteristics vs temperature are shown as follows:

Table 43. VNP DC Temperature Plots			
Device Emitter Size (W x L x #E)	vs. Varying Temp	@ 125C	@ -40C
0.4 x 2.5 x 1	Fig 90	Fig 91	Fig 92
0.4 x 20 x 2		Fig 93	Fig 94
0.8 x 5 x 1	Fig 95	Fig 96	Fig 97
0.8 x 20 x 2		Fig 98	Fig 99

Note: All of the DC simulation curves were created with some adjustments to the process parameters, as noted in each figure, to center the model near the mean of the measured data.

BiCMOS8HP "Vertical PNP" – Typical Characteristics (25C)
Emitter Size : 0.4 μm x 1.2 μm x 1

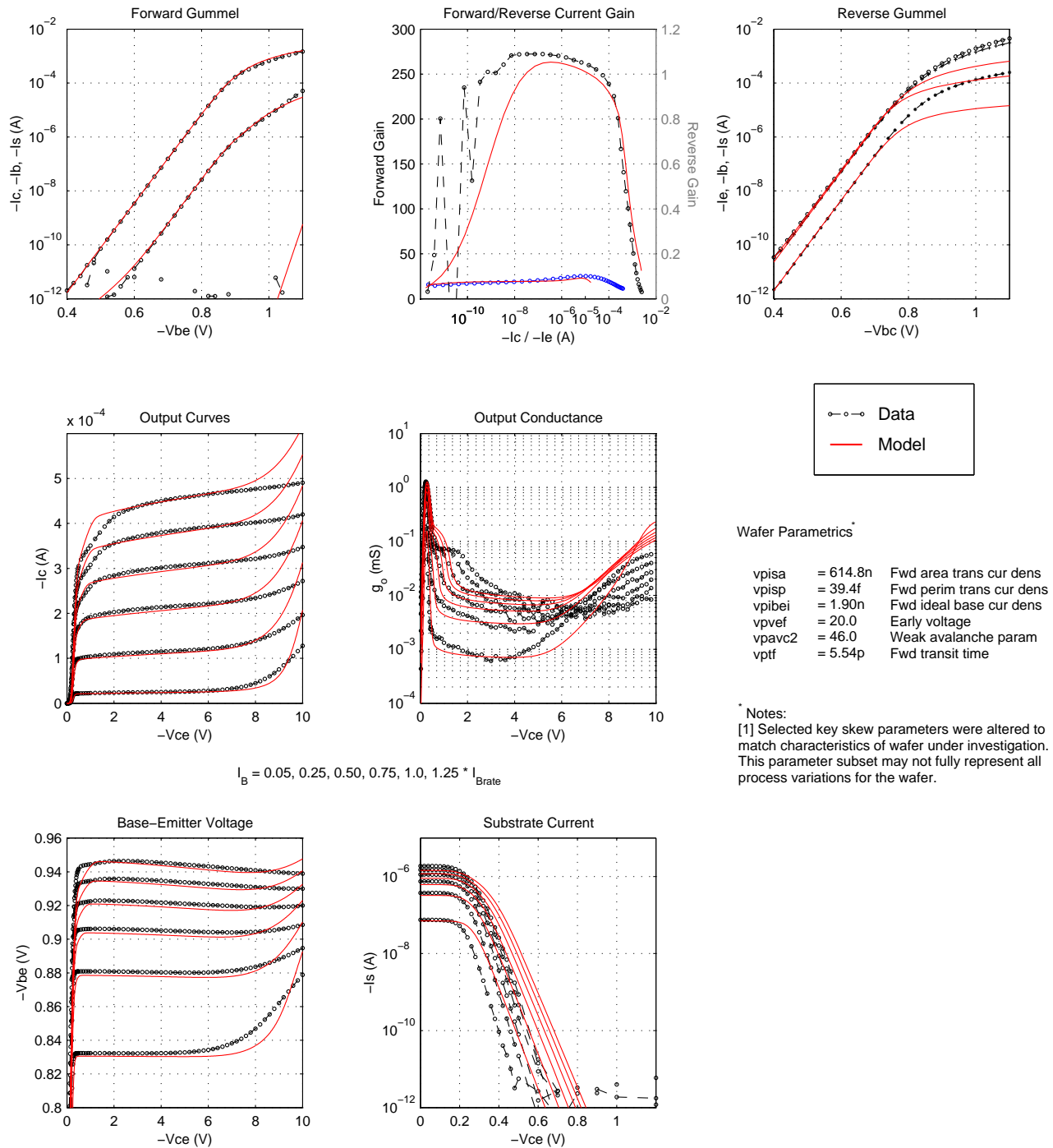


Figure 76. VPNP DC Characteristics for 0.4 μm x 1.2 μm x 1 Emitter

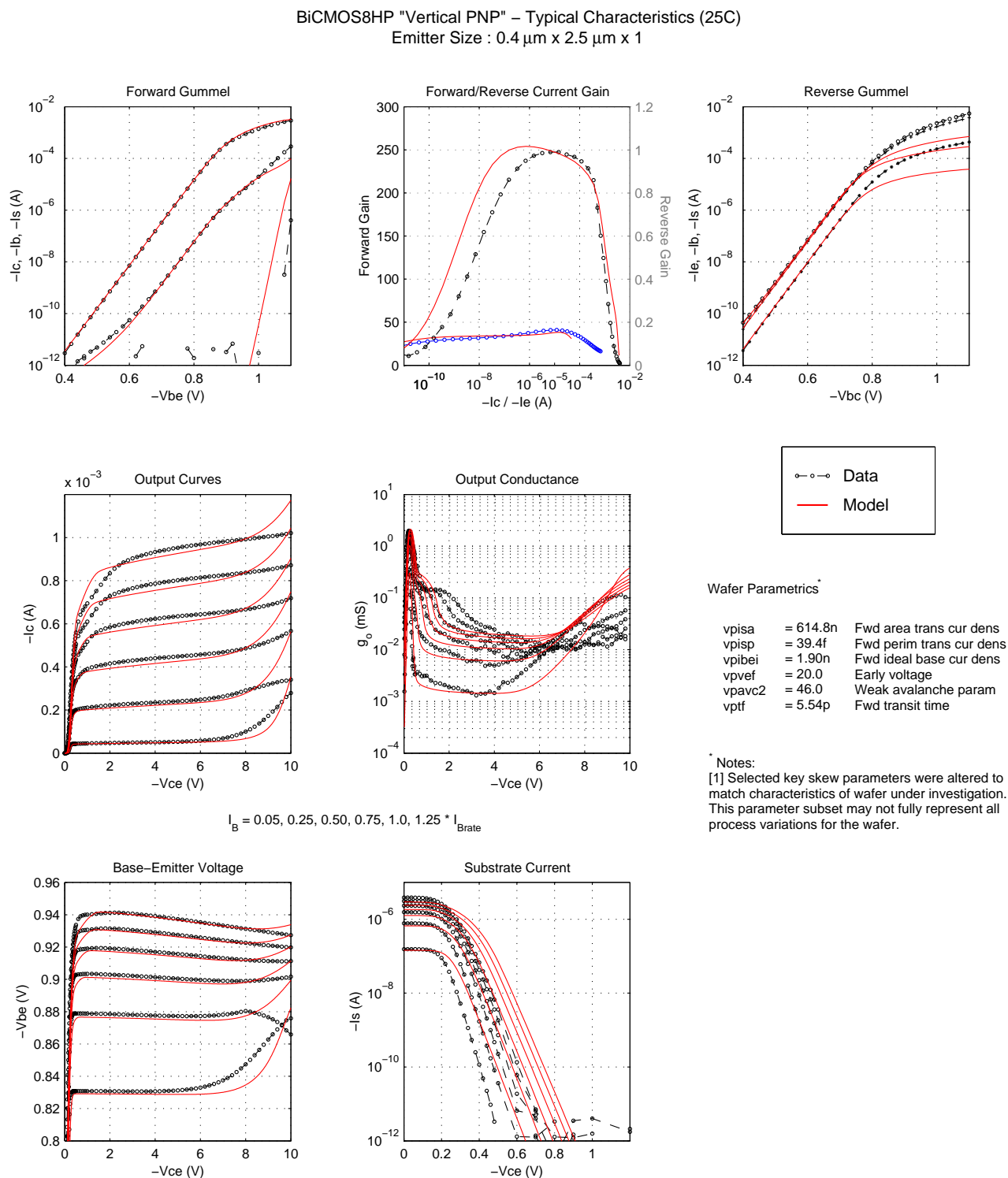


Figure 77. VPNP DC Characteristics for 0.4 μm x 2.5 μm x 1 Emitter

BiCMOS8HP "Vertical PNP" – Typical Characteristics (25C)
Emitter Size : 0.4 μm x 4.2 μm x 1

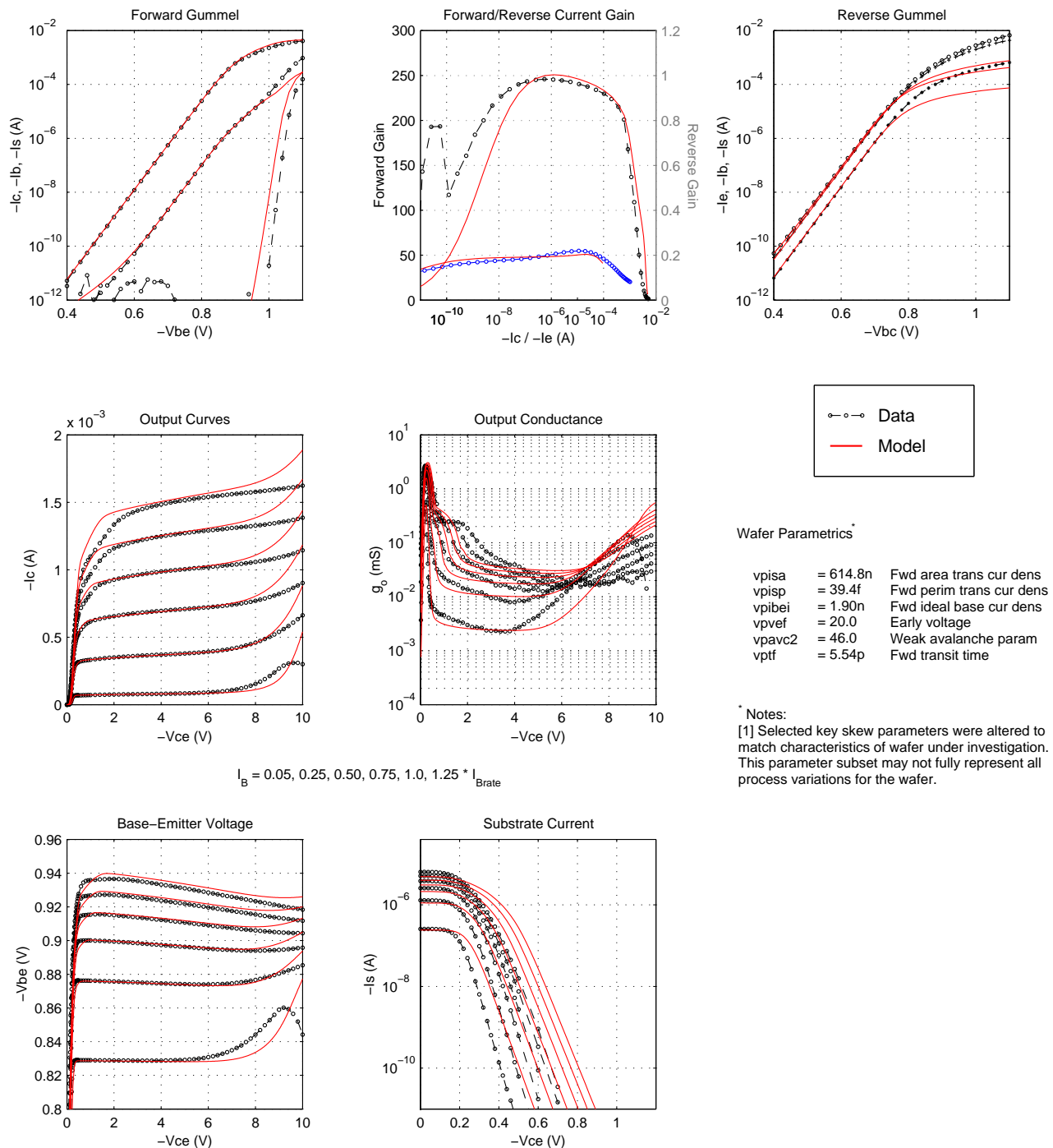


Figure 78. VPNP DC Characteristics for 0.4 μm x 4.2 μm x 1 Emitter

BiCMOS8HP "Vertical PNP" – Typical Characteristics (25C)
 Emitter Size : 0.4 μm x 10.0 μm x 1

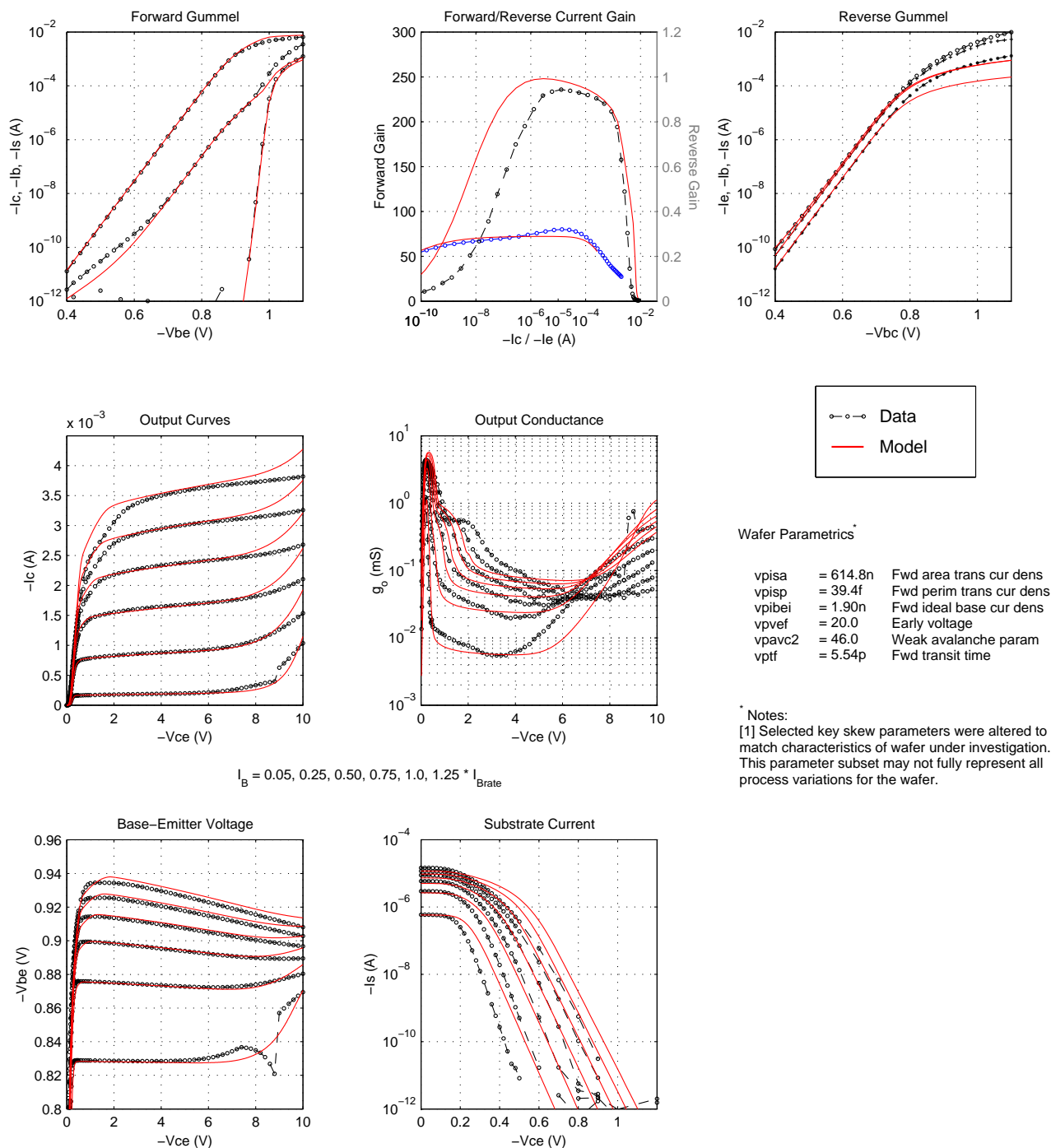


Figure 79. VPNP DC Characteristics for 0.4 μm x 10 μm x 1 Emitter

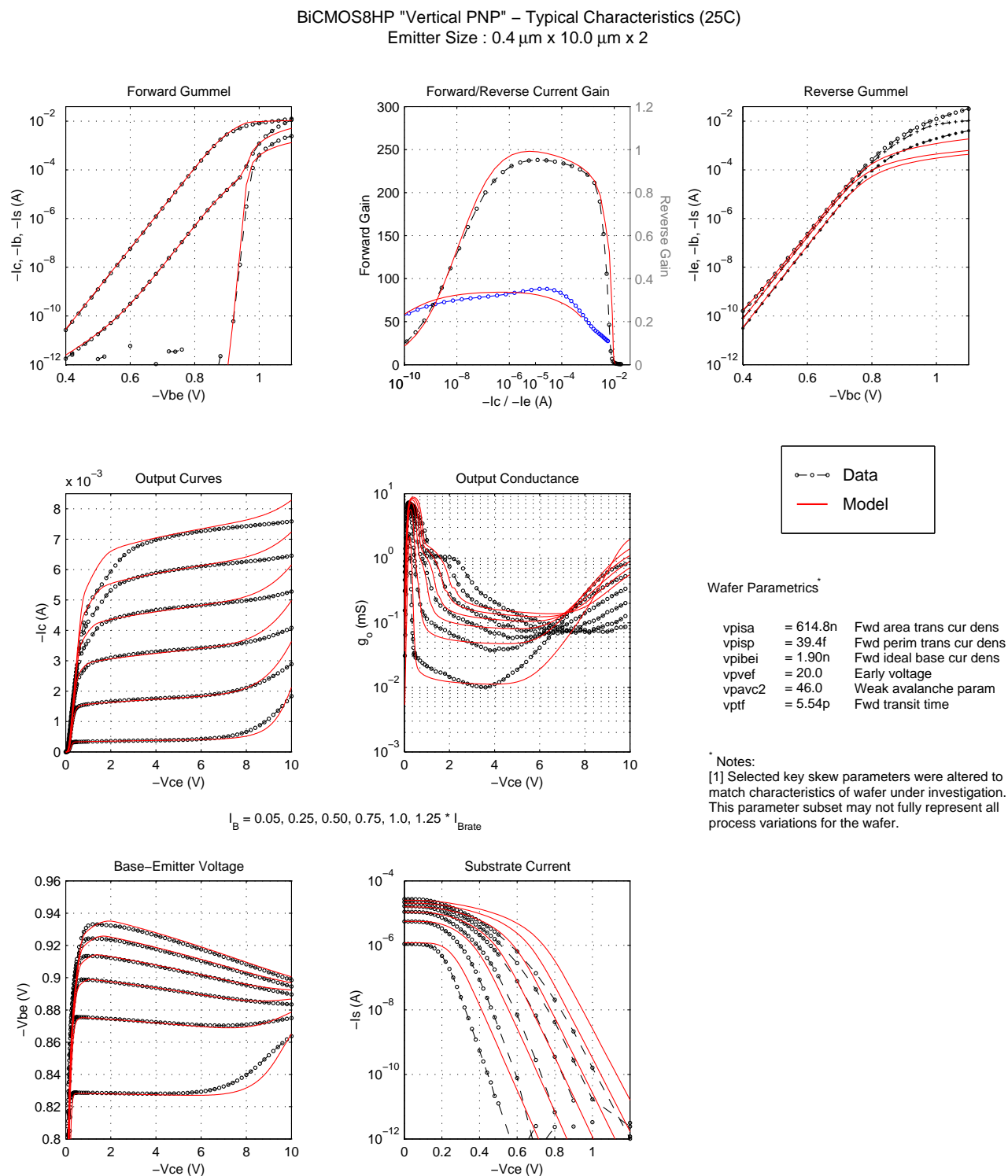


Figure 80. VPNP DC Characteristics for 0.4 μm x 10 μm x 2 Emitter

BiCMOS8HP "Vertical PNP" – Typical Characteristics (25C)
Emitter Size : 0.4 μm x 20.0 μm x 1

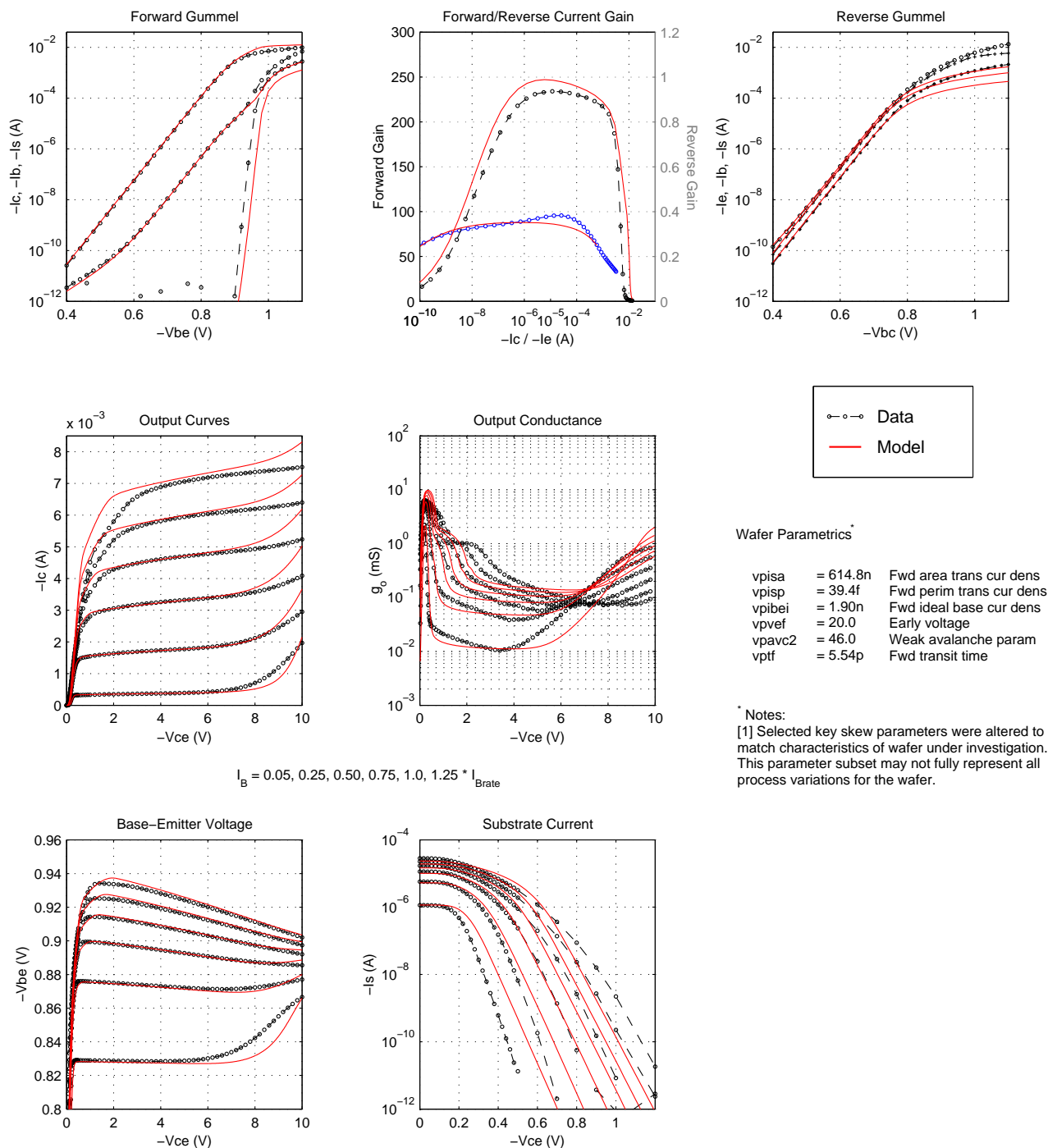


Figure 81. VPNP DC Characteristics for 0.4 μm x 20 μm x 1 Emitter

BiCMOS8HP "Vertical PNP" – Typical Characteristics (25C)
Emitter Size : 0.4 μm x 20.0 μm x 2

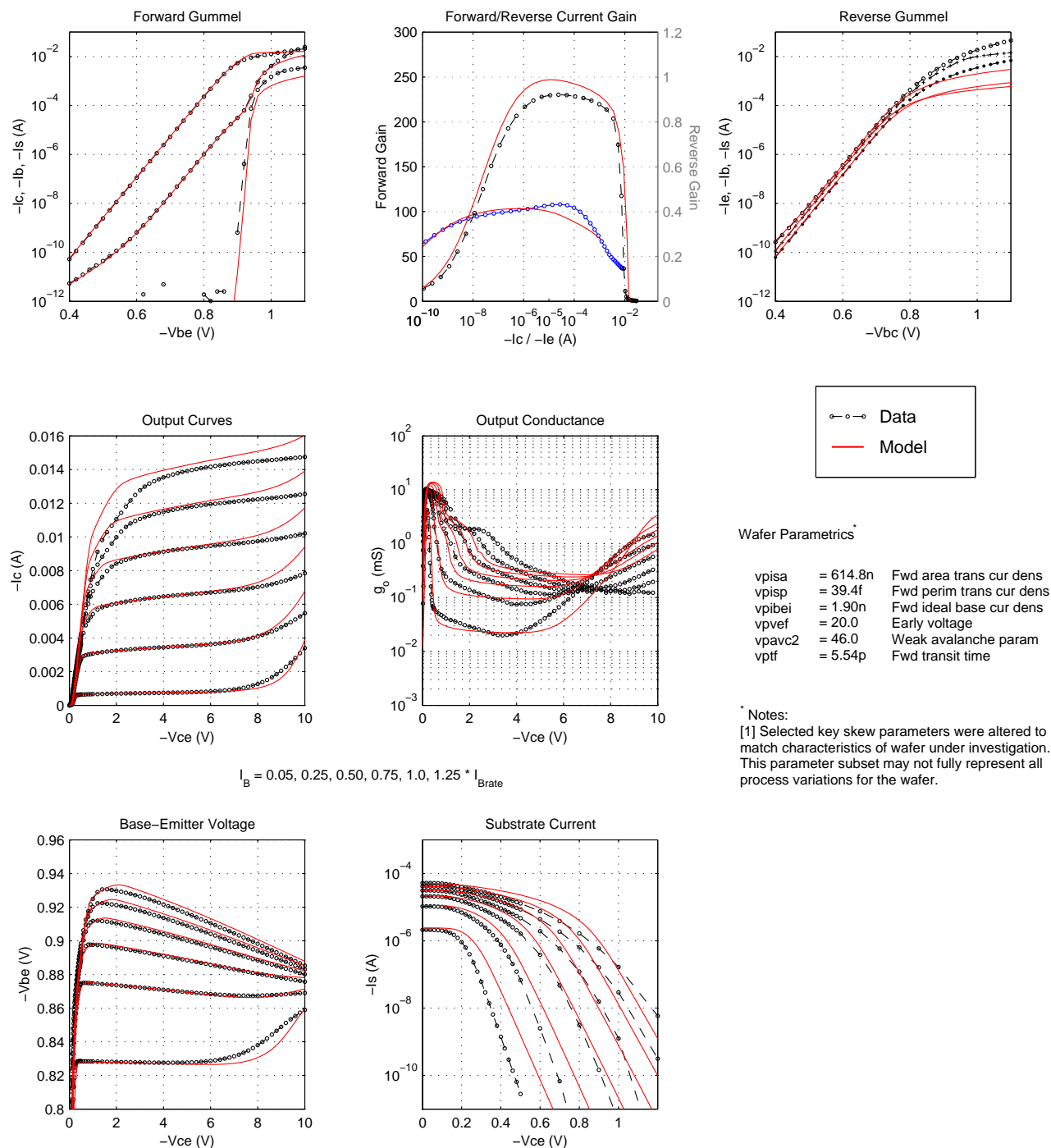


Figure 82. VPNP DC Characteristics for 0.4 μm x 20 μm x 2 Emitter

BiCMOS8HP "Vertical PNP" – Typical Characteristics (25C)
 Emitter Size : 0.8 μm x 2.5 μm x 1

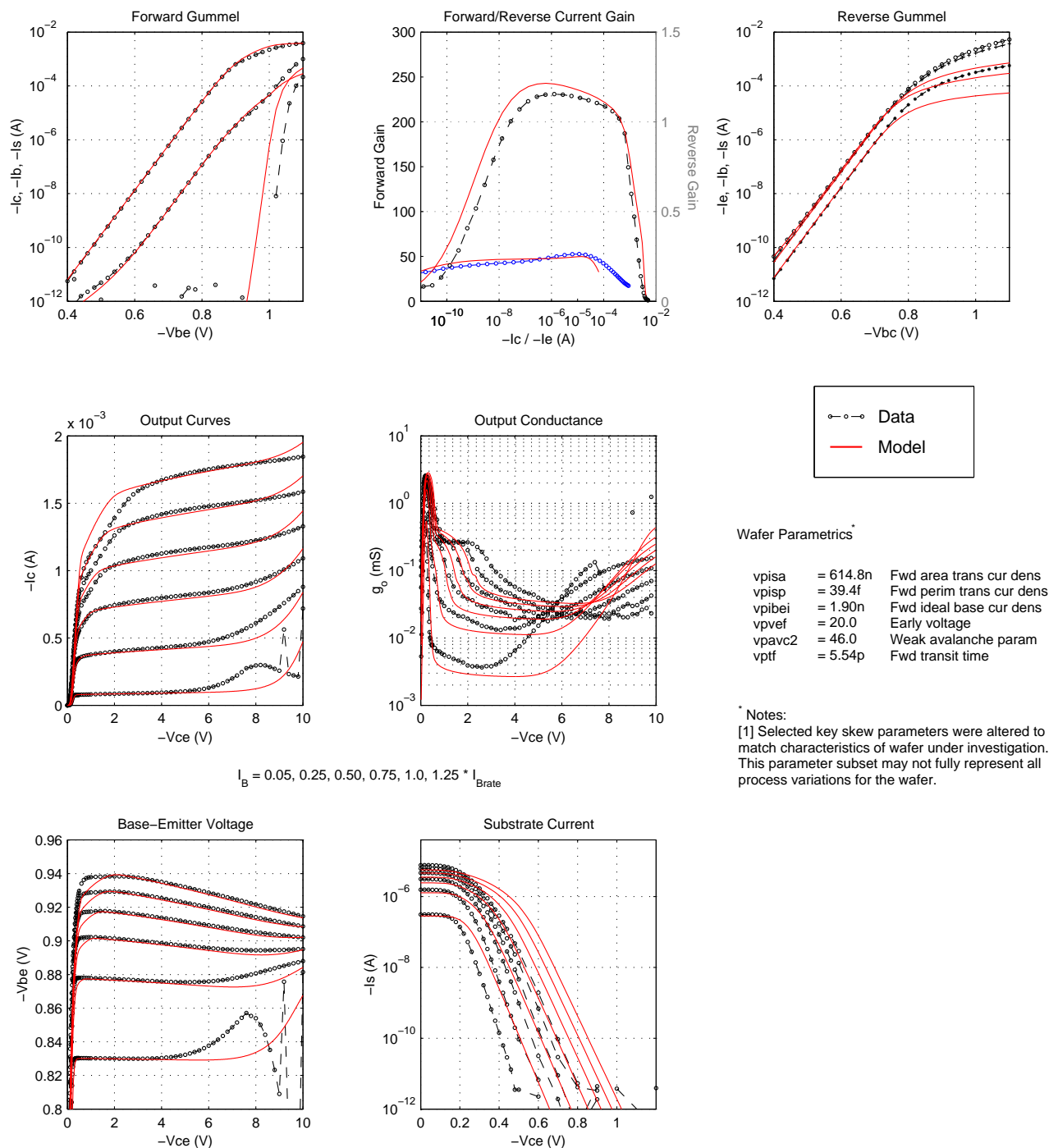


Figure 83. VPNP DC Characteristics for 0.8 μm x 2.5 μm x 1 Emitter

BiCMOS8HP "Vertical PNP" – Typical Characteristics (25C)
Emitter Size : 0.8 μm x 3.0 μm x 1

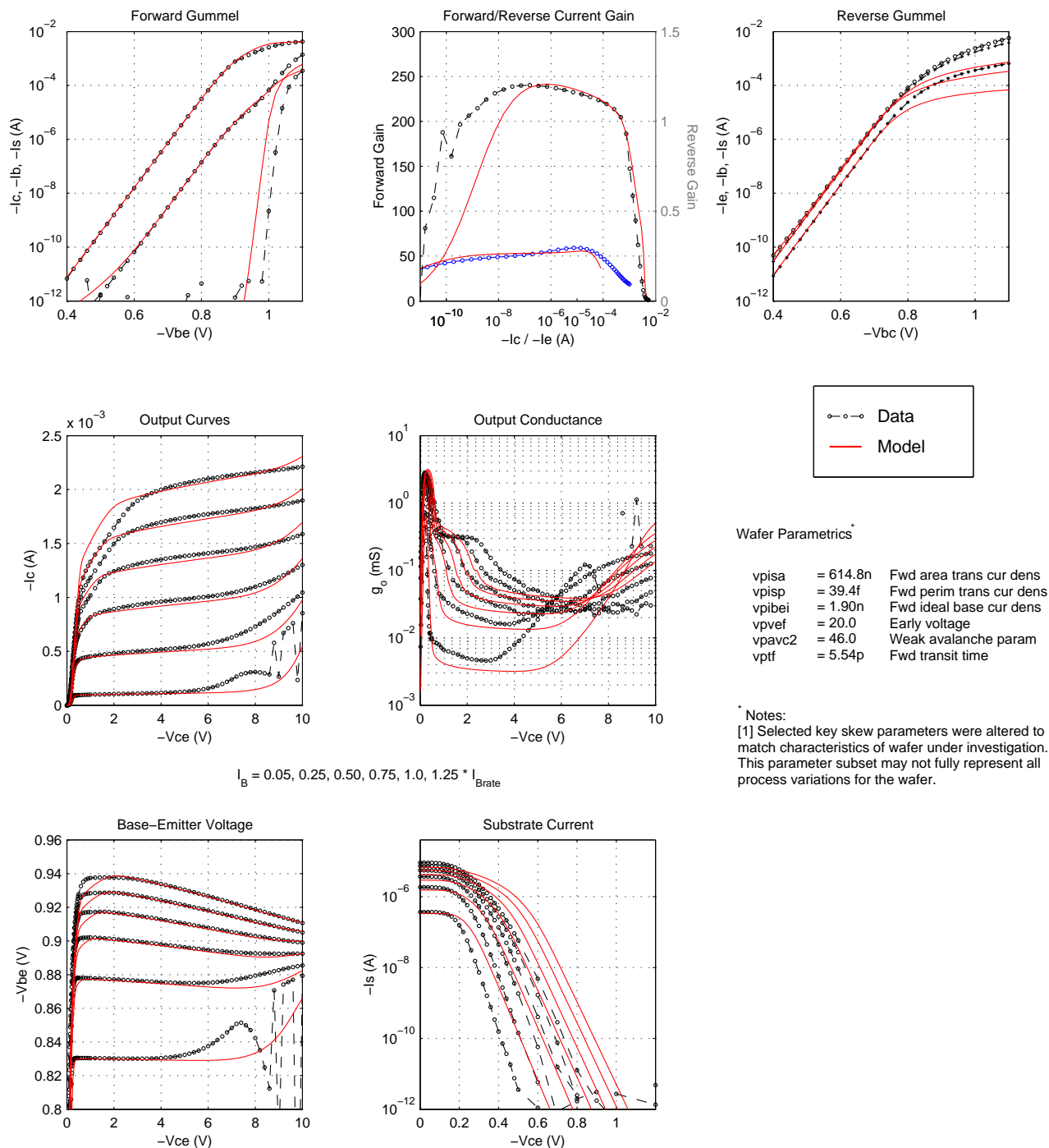


Figure 84. VPNP DC Characteristics for 0.8 μm x 3 μm x 1 Emitter

BiCMOS8HP "Vertical PNP" – Typical Characteristics (25C)
Emitter Size : 0.8 μm x 5.0 μm x 1

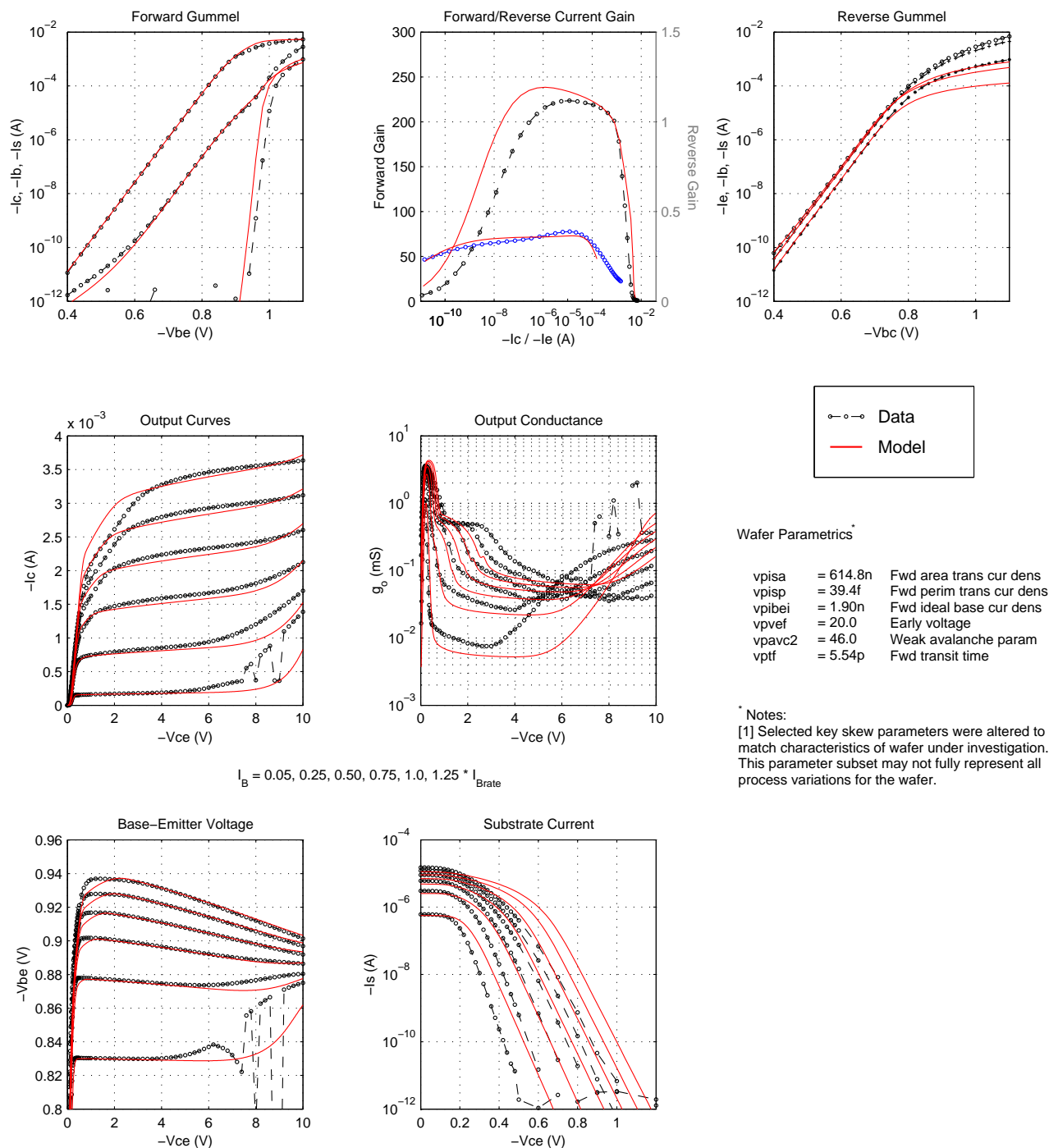


Figure 85. VPNP DC Characteristics for 0.8 μm x 5 μm x 1 Emitter

BiCMOS8HP "Vertical PNP" – Typical Characteristics (25C)
Emitter Size : 0.8 μm x 10.0 μm x 1

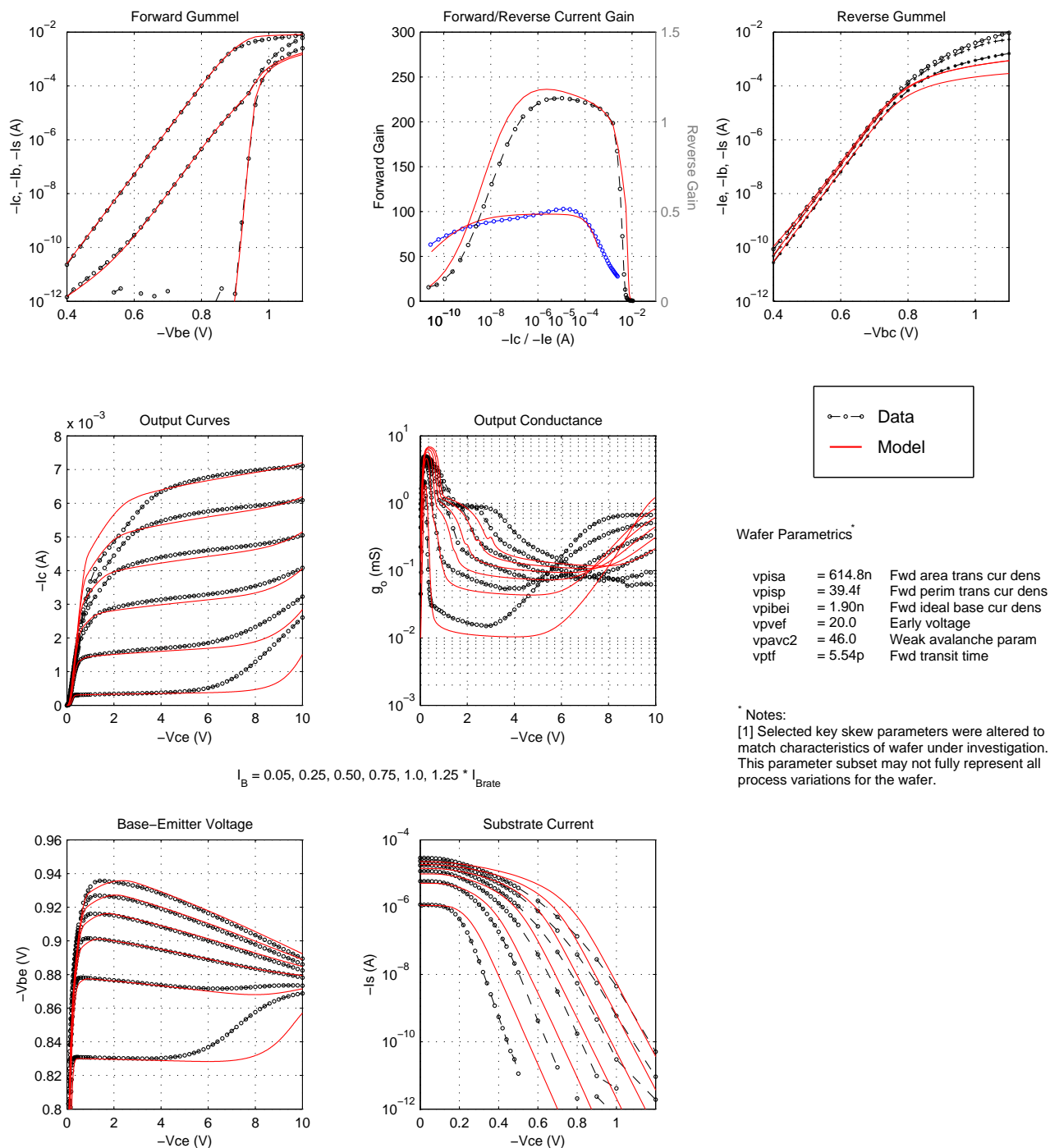


Figure 86. VPNP DC Characteristics for 0.8 μm x 10 μm x 1 Emitter

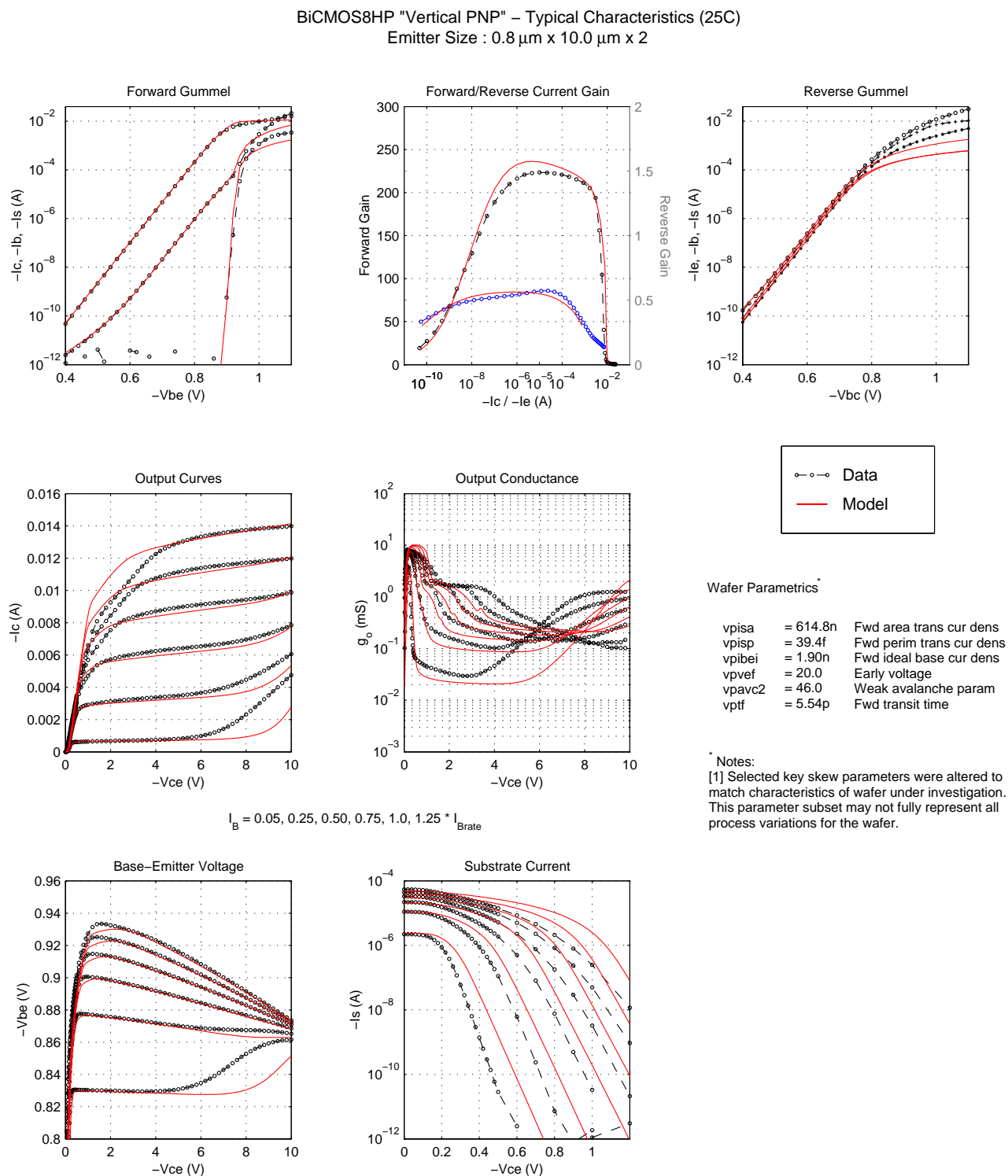


Figure 87. VPNP DC Characteristics for 0.8 μm x 10 μm x 2 Emitter

BiCMOS8HP "Vertical PNP" – Typical Characteristics (25C)
Emitter Size : 0.8 μm x 20.0 μm x 1

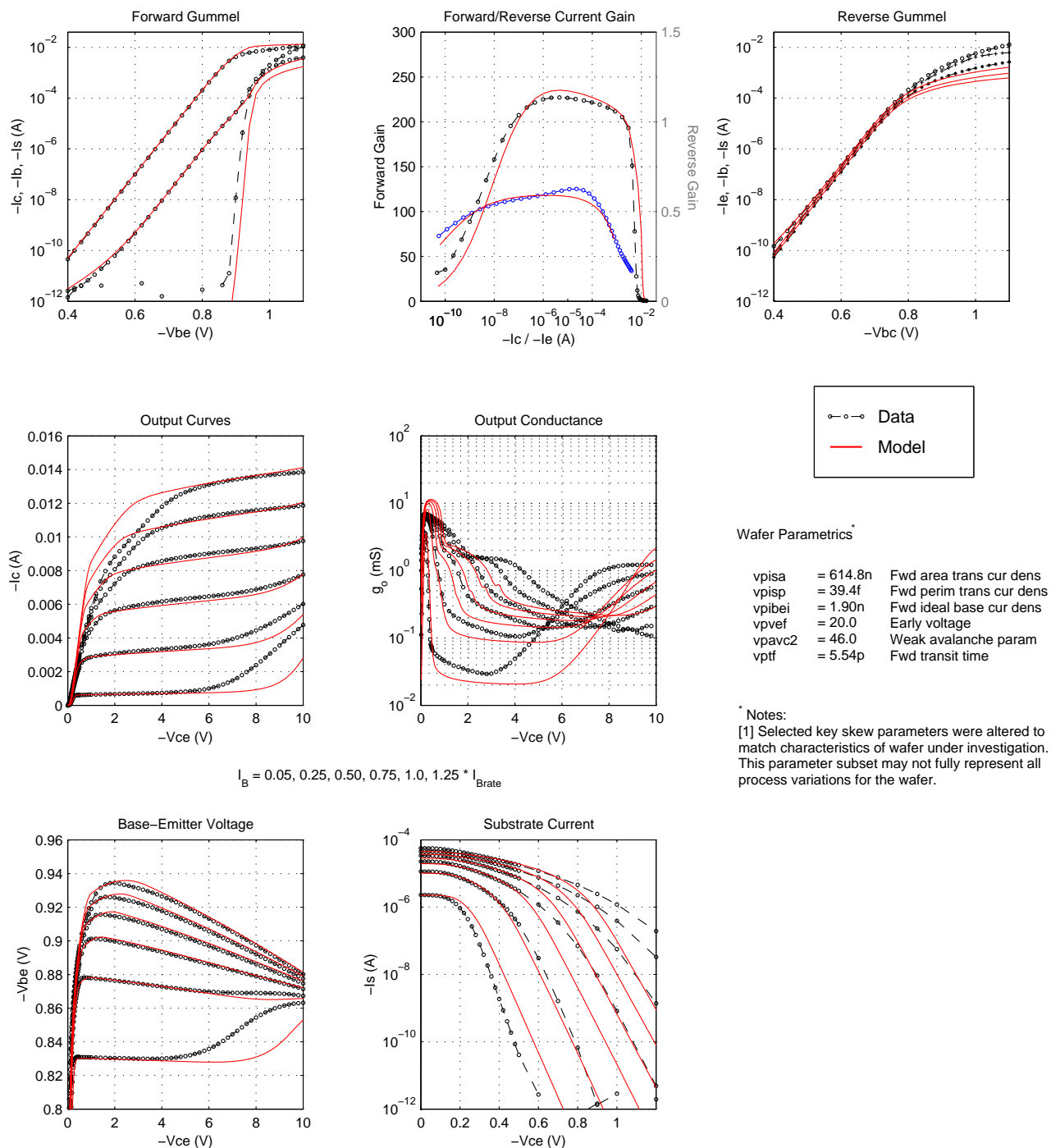


Figure 88. VPNP DC Characteristics for 0.8 μm x 20 μm x 1 Emitter

BiCMOS8HP "Vertical PNP" – Typical Characteristics (25C)
Emitter Size : 0.8 μ m x 20.0 μ m x 2

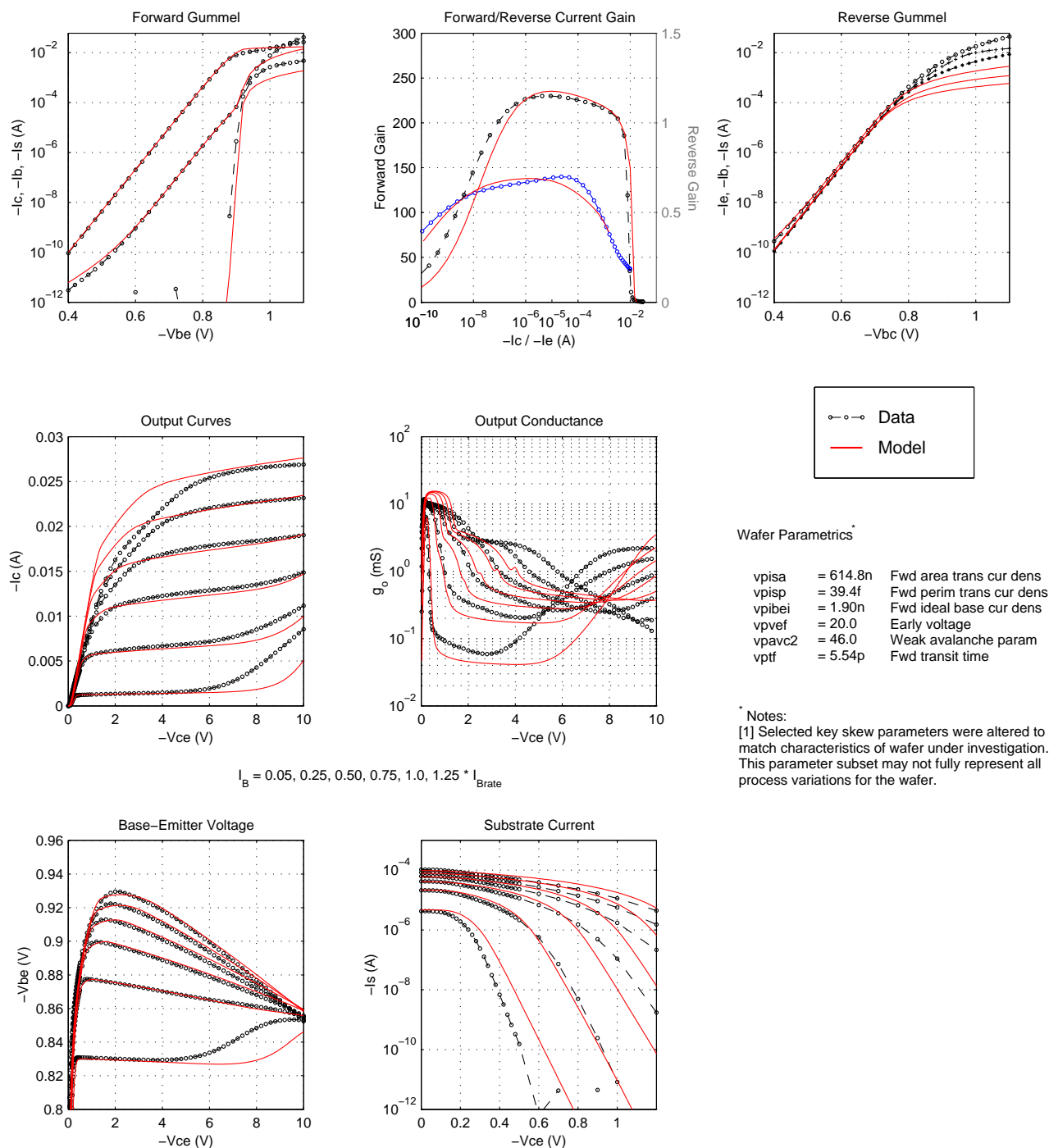


Figure 89. VPNP DC Characteristics for 0.8 μ m x 20 μ m x 2 Emitter

BiCMOS8HP "Vertical PNP" – Typical DC Characteristics vs. Temperature
 Emitter Size: $0.4\mu\text{m} \times 2.5\mu\text{m} \times 1$

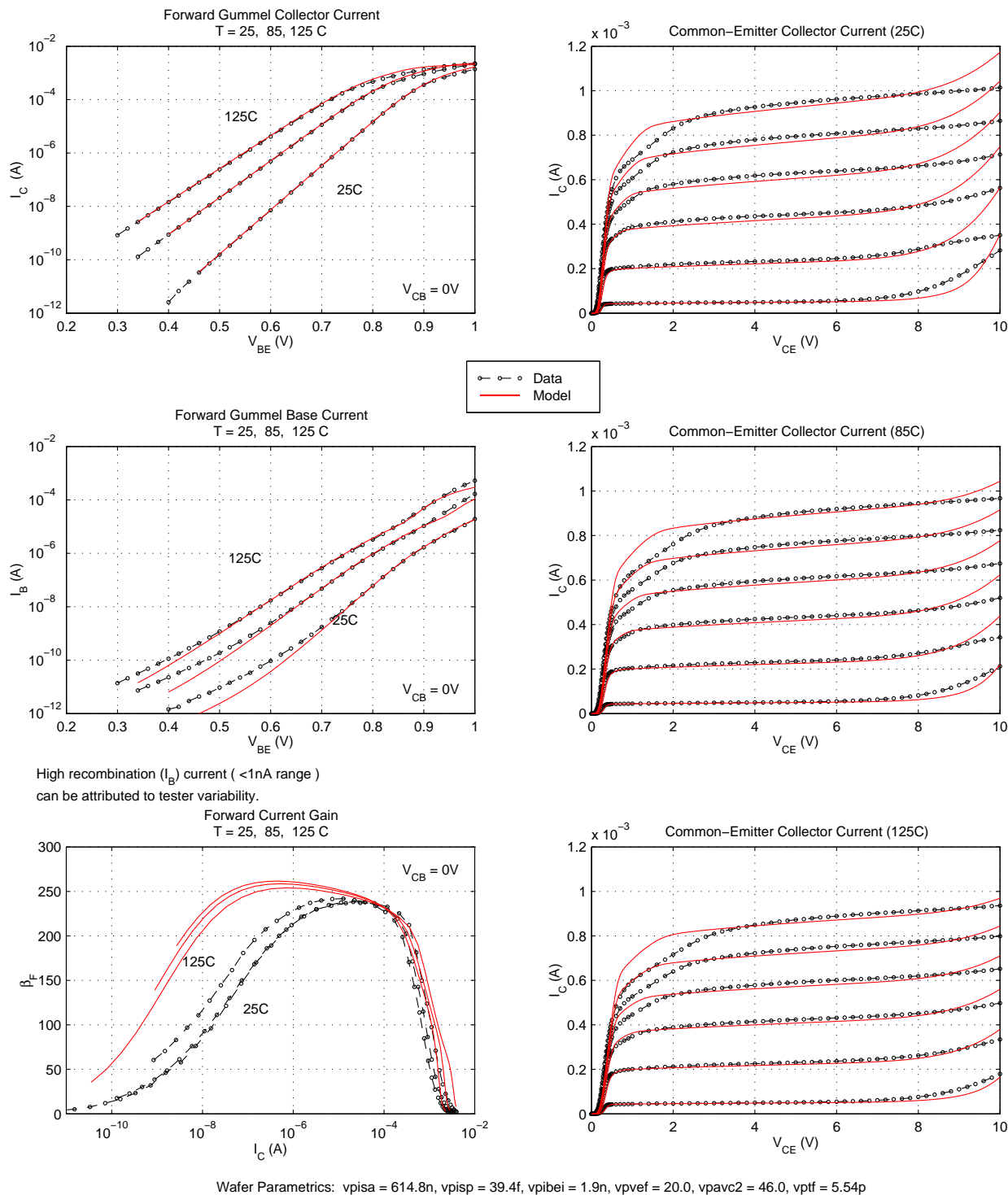


Figure 90. VNP DC vs Temperature for $0.4\mu\text{m} \times 2.5\mu\text{m} \times 1$ Emitter

BiCMOS8HP "Vertical PNP" – Typical Characteristics (125C)
Emitter Size : 0.4 μm x 2.5 μm x 1

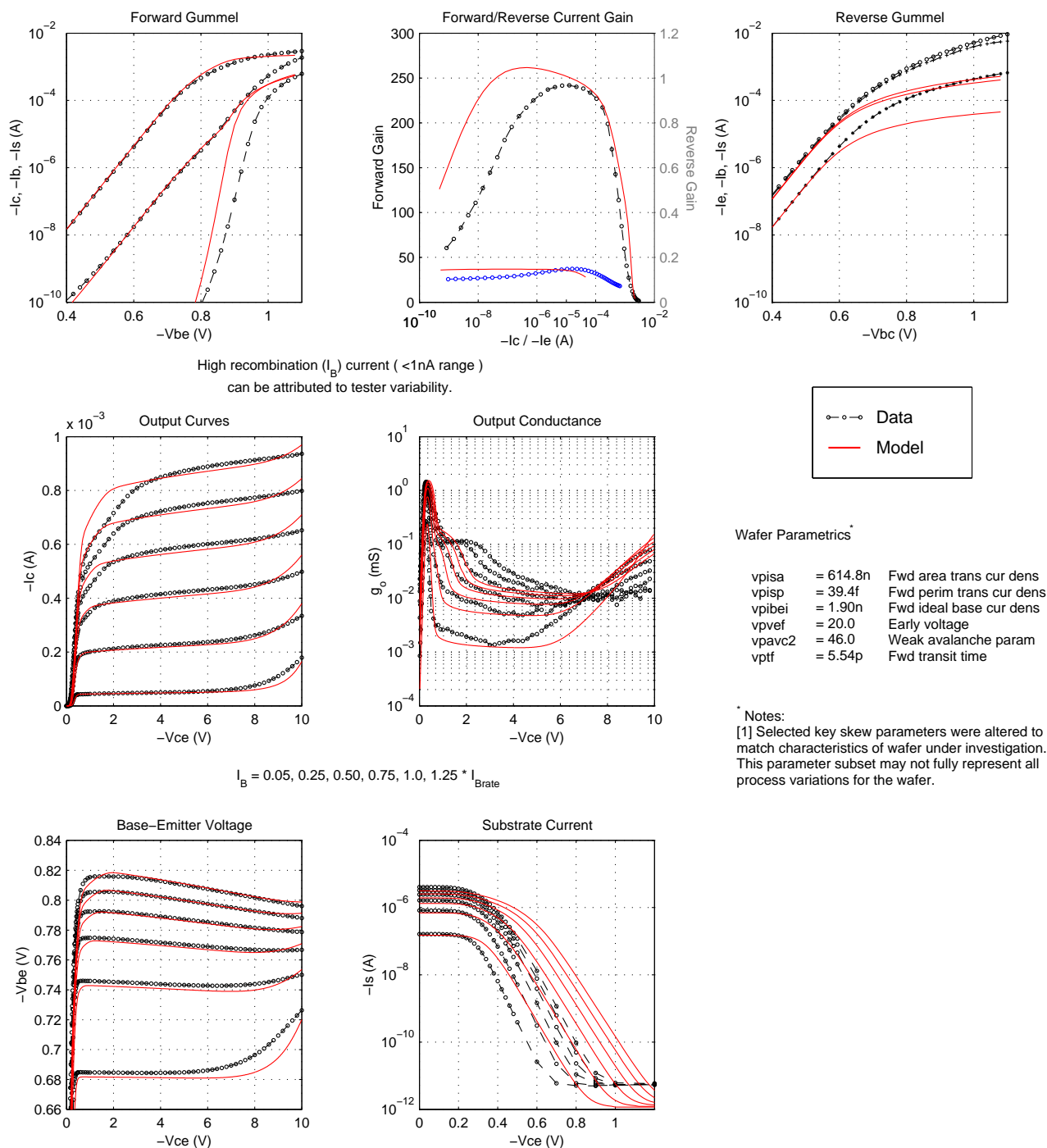


Figure 91. VPNP DC Characteristics for 0.4 μm x 2.5 μm x 1 Emitter (125C)

BiCMOS8HP "Vertical PNP" – Typical Characteristics (–40C)
Emitter Size : 0.4 μm x 2.5 μm x 1

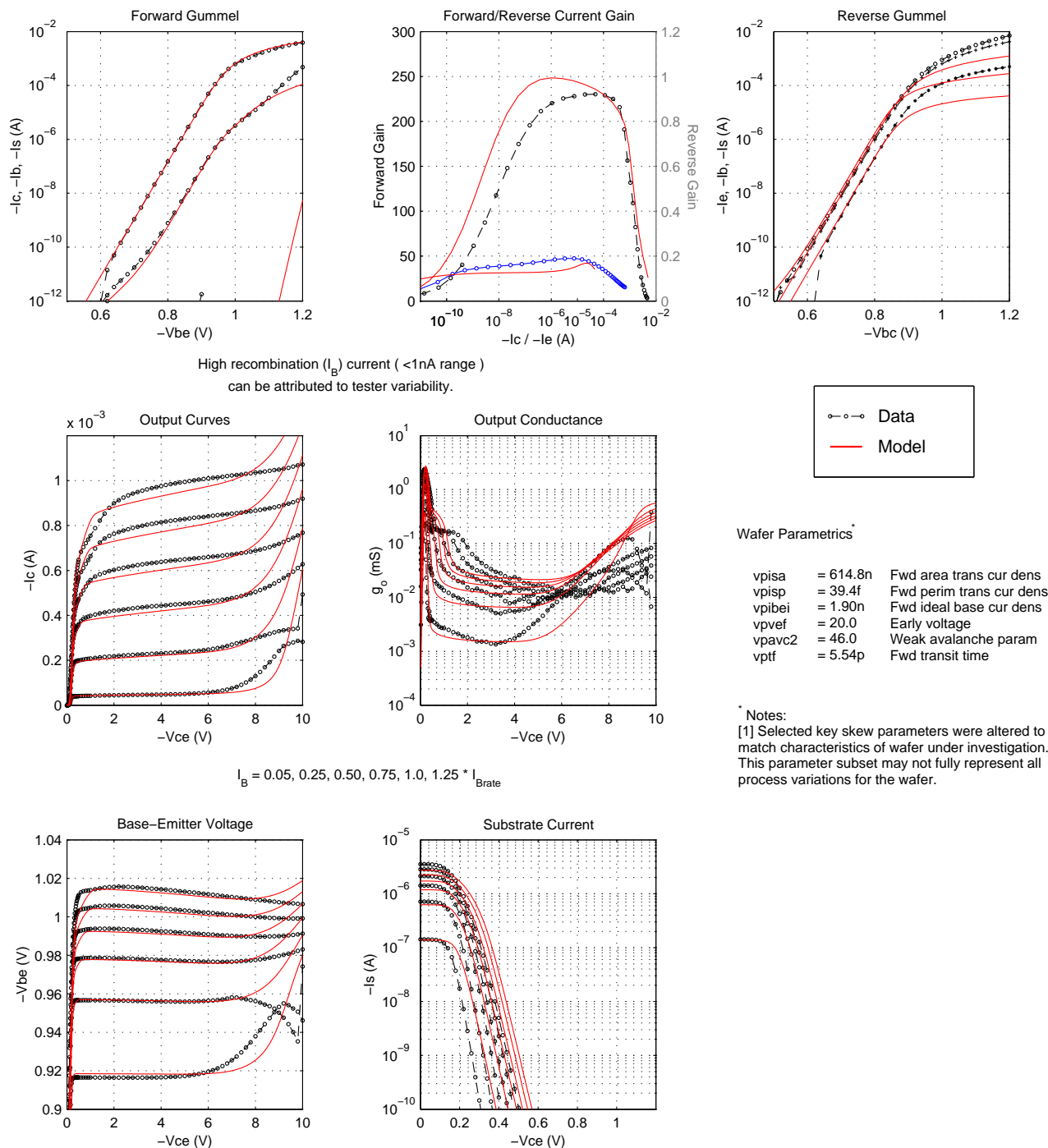


Figure 92. VPNP DC Characteristics for 0.4 μm x 2.5 μm x 1 Emitter (–40C)

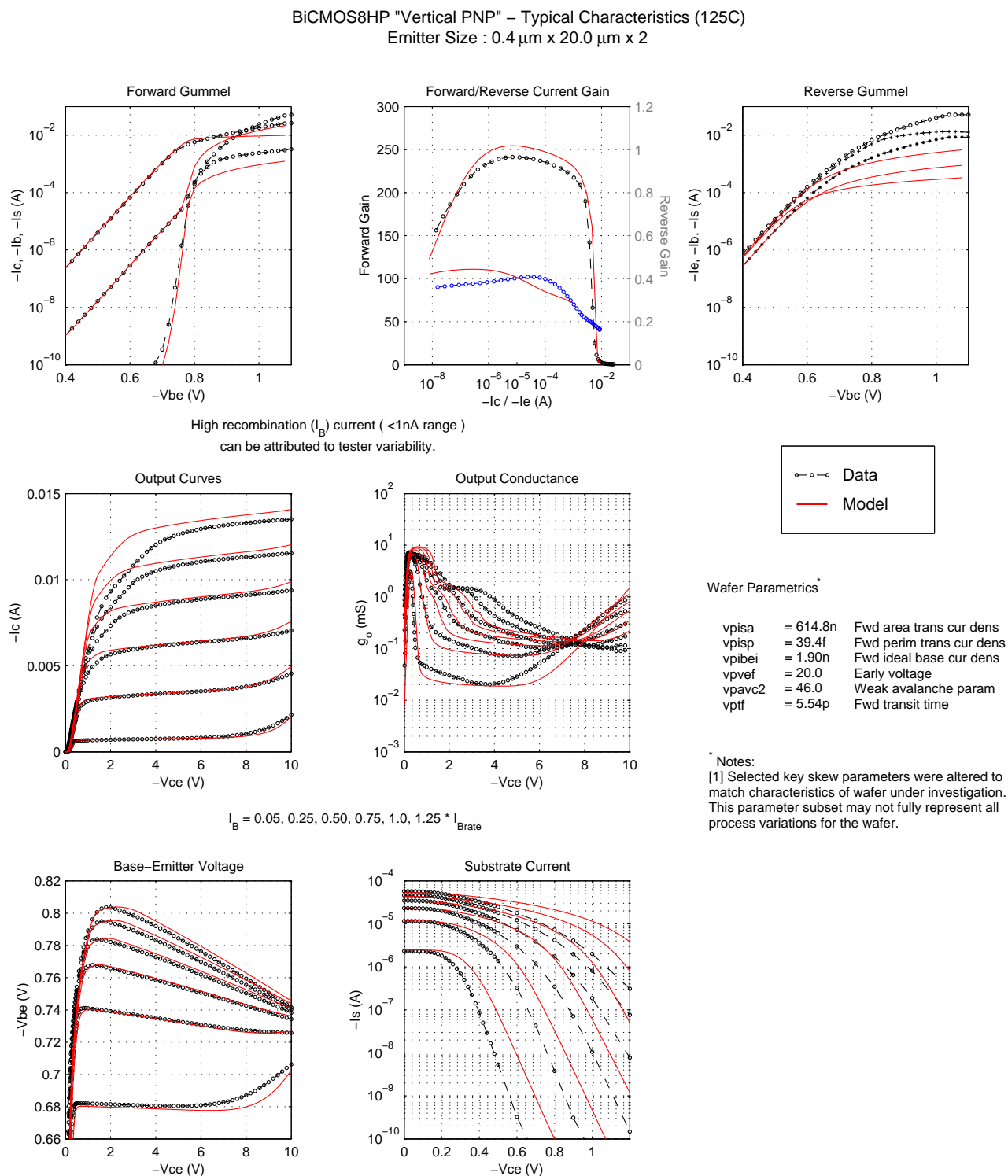


Figure 93. VNP DC Characteristics for 0.4 μm x 20 μm x 2 Emitter (125C)

BiCMOS8HP "Vertical PNP" – Typical Characteristics (–40C)
Emitter Size : 0.4 μm x 20.0 μm x 2

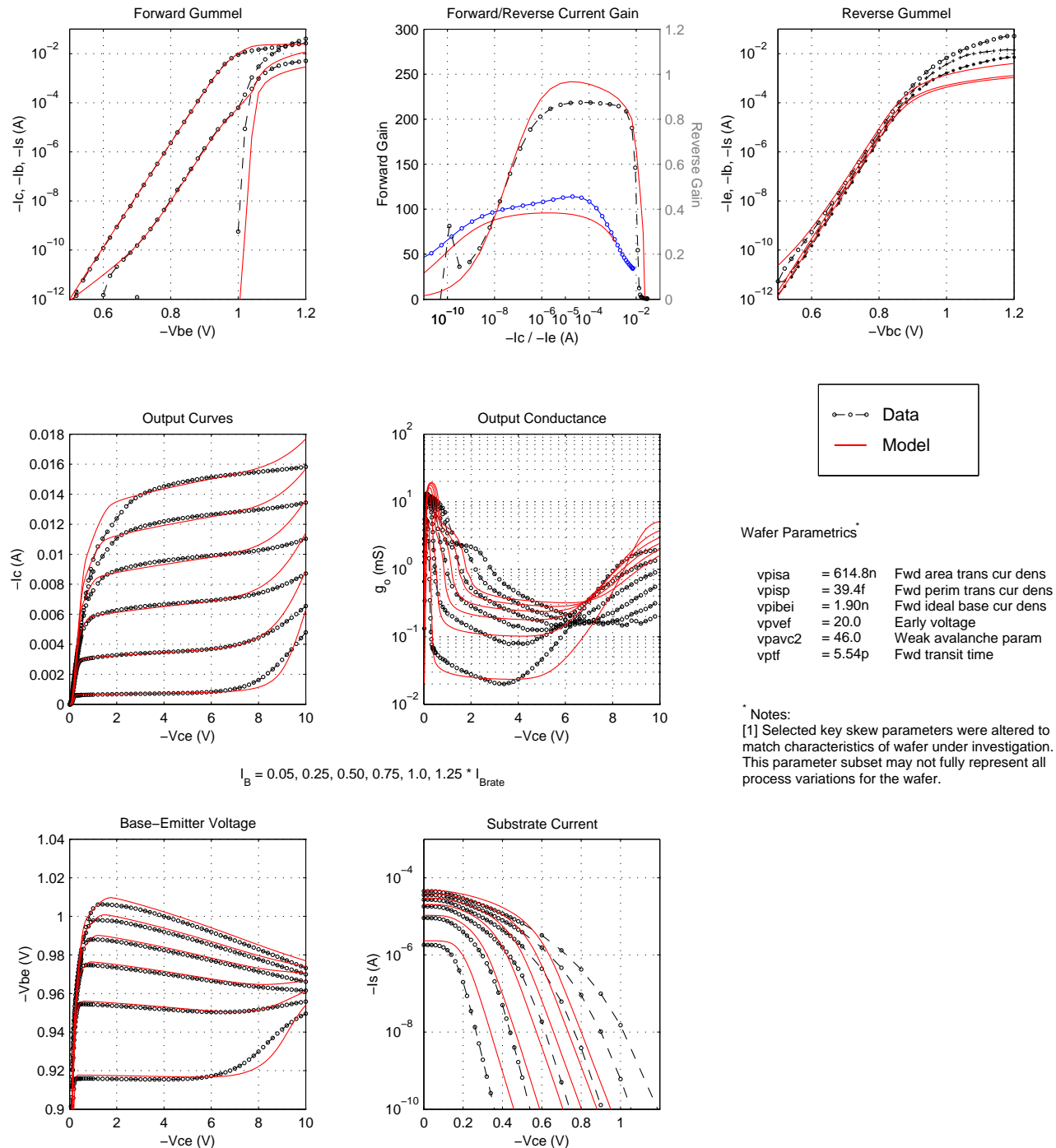


Figure 94. VPNP DC Characteristics for 0.4 μm x 20 μm x 2 Emitter (–40C)

BiCMO8HP "Vertical PNP" – Typical DC Characteristics vs. Temperature
Emitter Size: 0.8 μ m x 5 μ m x 1

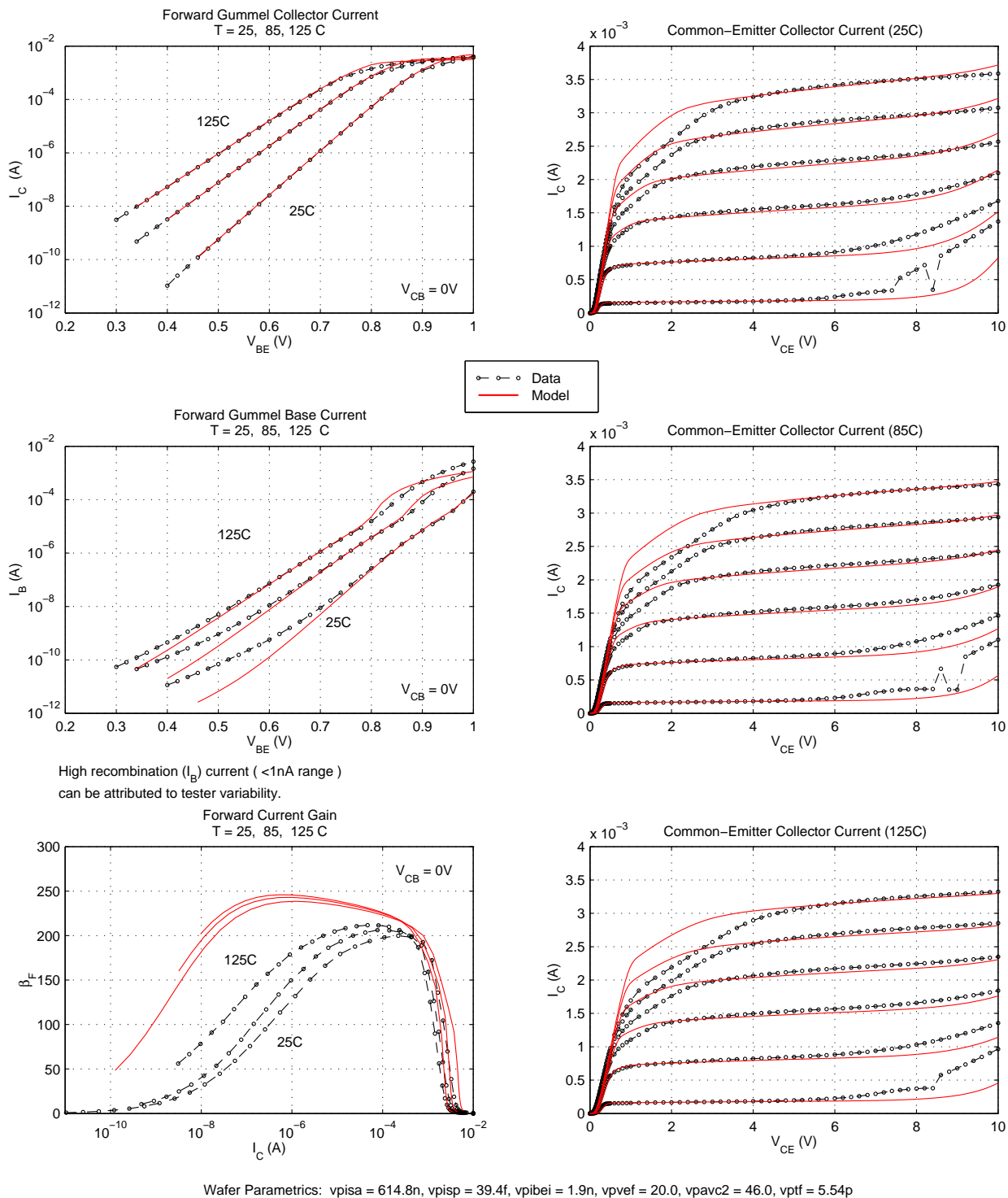


Figure 95. VPNP DC vs Temperature for 0.8 μ m x 5 μ m x 1 Emitter

BiCMOS8HP "Vertical PNP" – Typical Characteristics (125C)
Emitter Size : 0.8 μm x 5.0 μm x 1

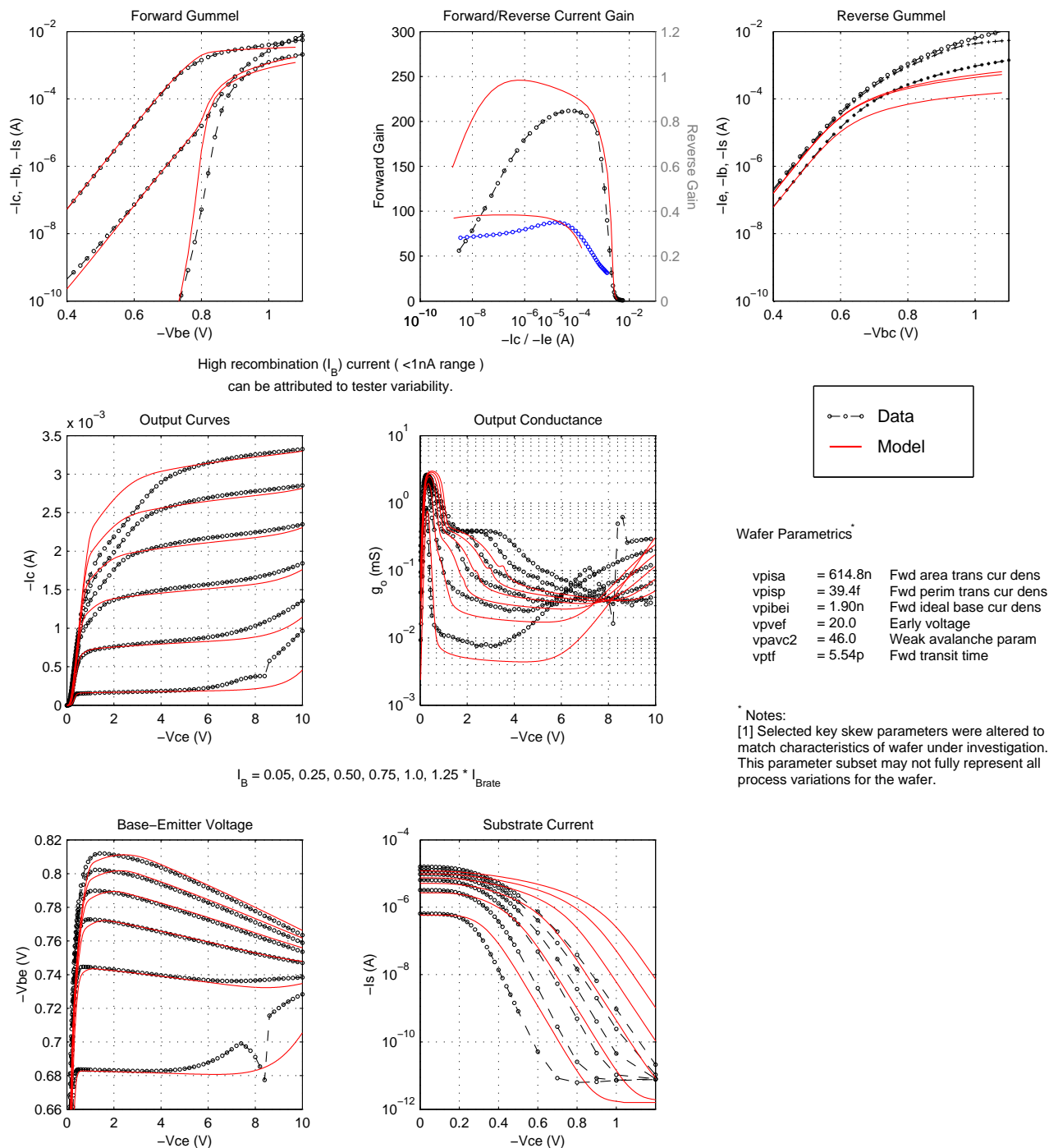


Figure 96. VPNP DC Characteristics for 0.8 μm x 5 μm x 1 Emitter (125C)

BiCMOS8HP "Vertical PNP" – Typical Characteristics (–40C)
Emitter Size : 0.8 μ m x 5.0 μ m x 1

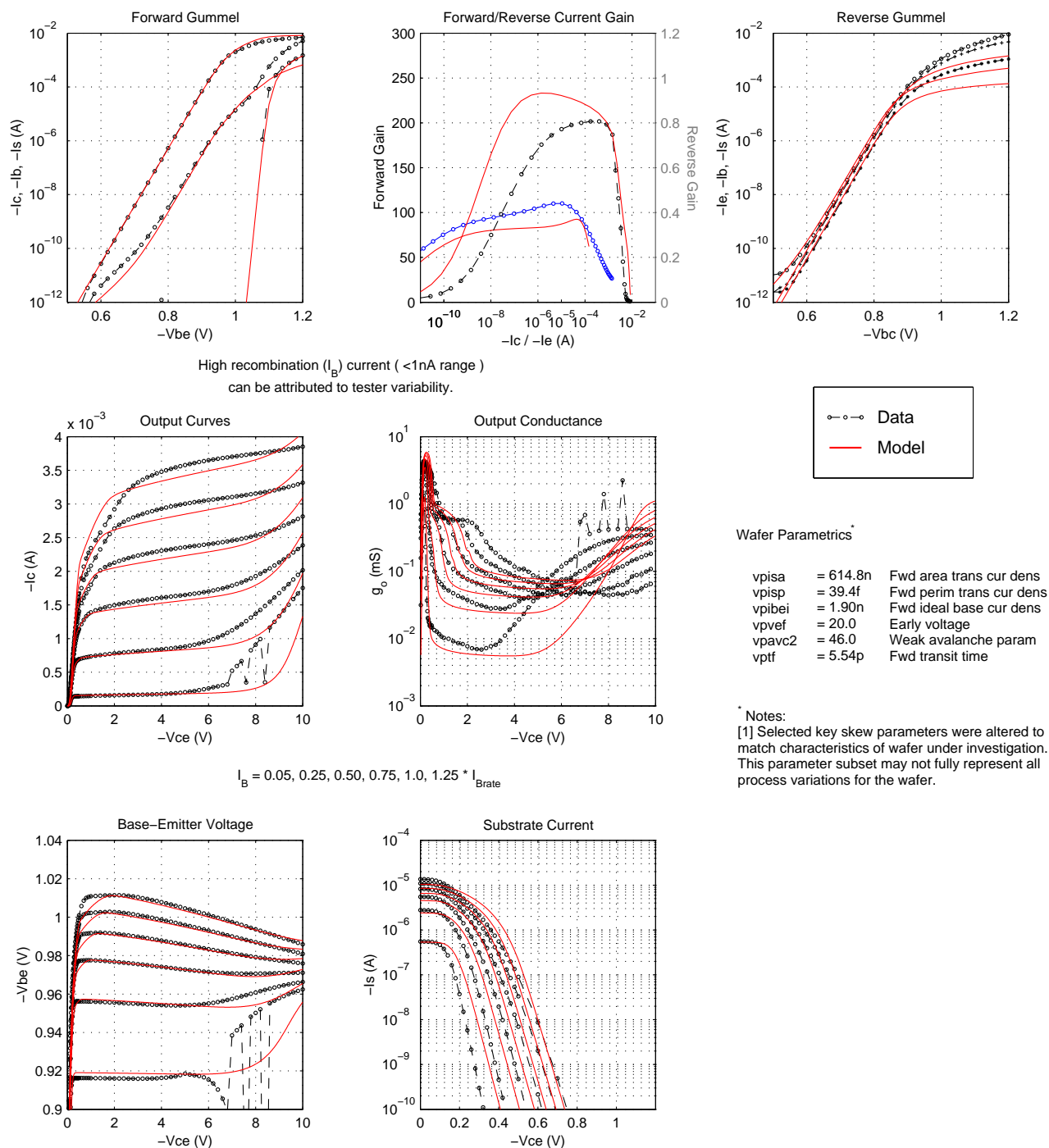


Figure 97. VPNP DC Characteristics for 0.8 μ m x 5 μ m x 1 Emitter (–40C)

BiCMOS8HP "Vertical PNP" – Typical Characteristics (125C)
Emitter Size : 0.8 μm x 20.0 μm x 2

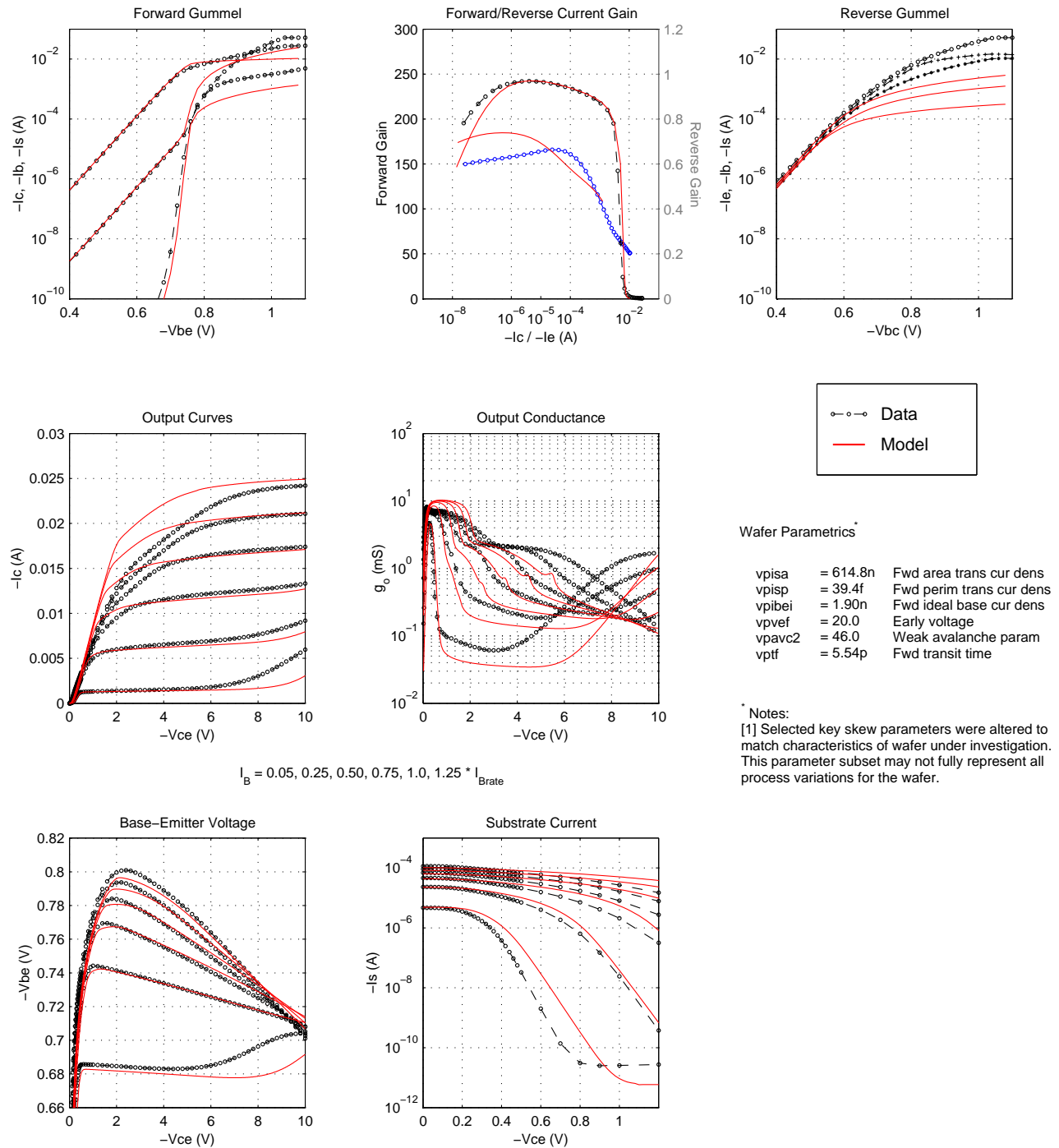


Figure 98. VPNP DC Characteristics for 0.8 μm x 20 μm x 2 Emitter (125C)

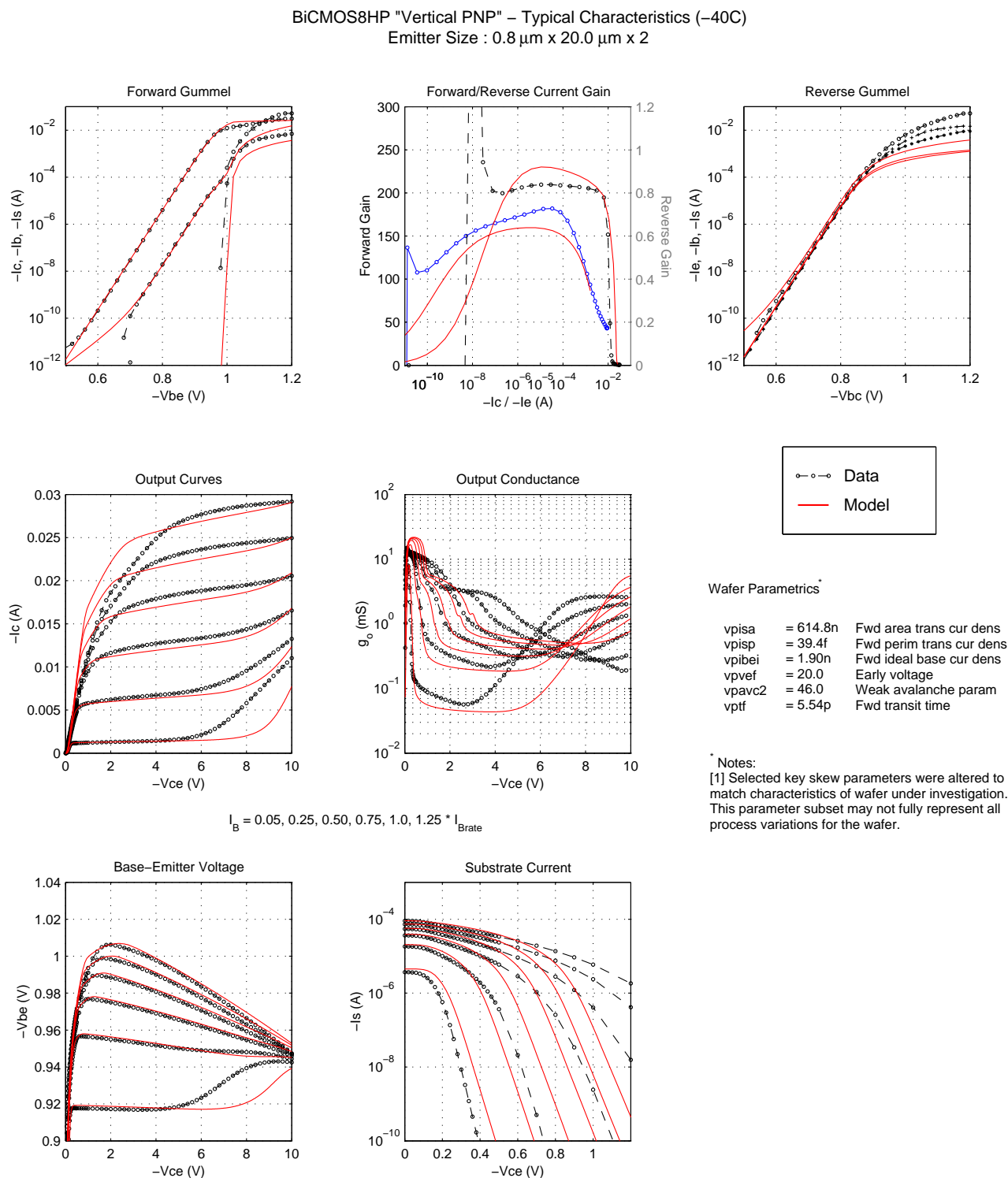


Figure 99. VNP DC Characteristics for 0.8 μm x 20 μm x 2 Emitter (–40C)

4.6 f_T Correlation Plots

The following plots compare the f_T vs I_C characteristics of the vpn model with measurement data from the initial device hardware. As the model supports a range of emitter widths and lengths, the plots show the model correlation for a few select device sizes.

<i>Table 44. VPNP f_T Correlation Plots</i>		
f_T vs I_C Characteristic	Emitter Width = 0.40 μ m	Emitter Width = 0.80 μ m
Emitter Length Scaling	Fig 100	Fig 100
V_{cb} , Temp Dependence	Fig 101	Fig 102

At this point, the model is limited in its ability to predict the following:

- The model will overpredict the f_T value in the higher current roll-off region (beyond peak).
- The model will underpredict the peak f_T value when the device is operated in saturation ($V_{cb} > 0$).

BiCMOS8HP Vertical PNP – Typical f_T Characteristics vs. Emitter Size (25°C)

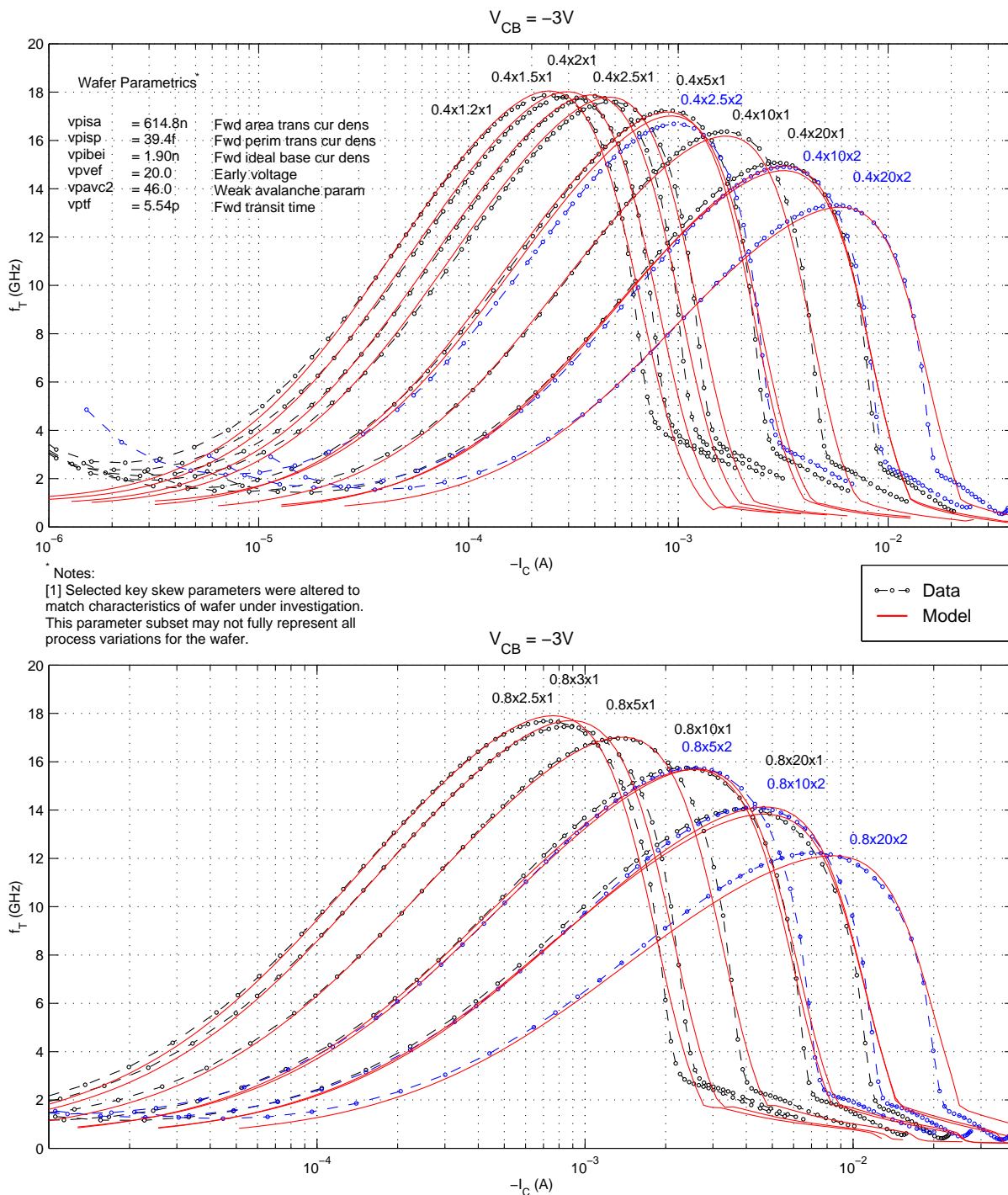


Figure 100. VPNP f_T vs I_C - Emitter Length Scaling, Width=0.4 μ m, 0.8 μ m

BiCMOS8HP Vertical PNP – Typical f_T Characteristics

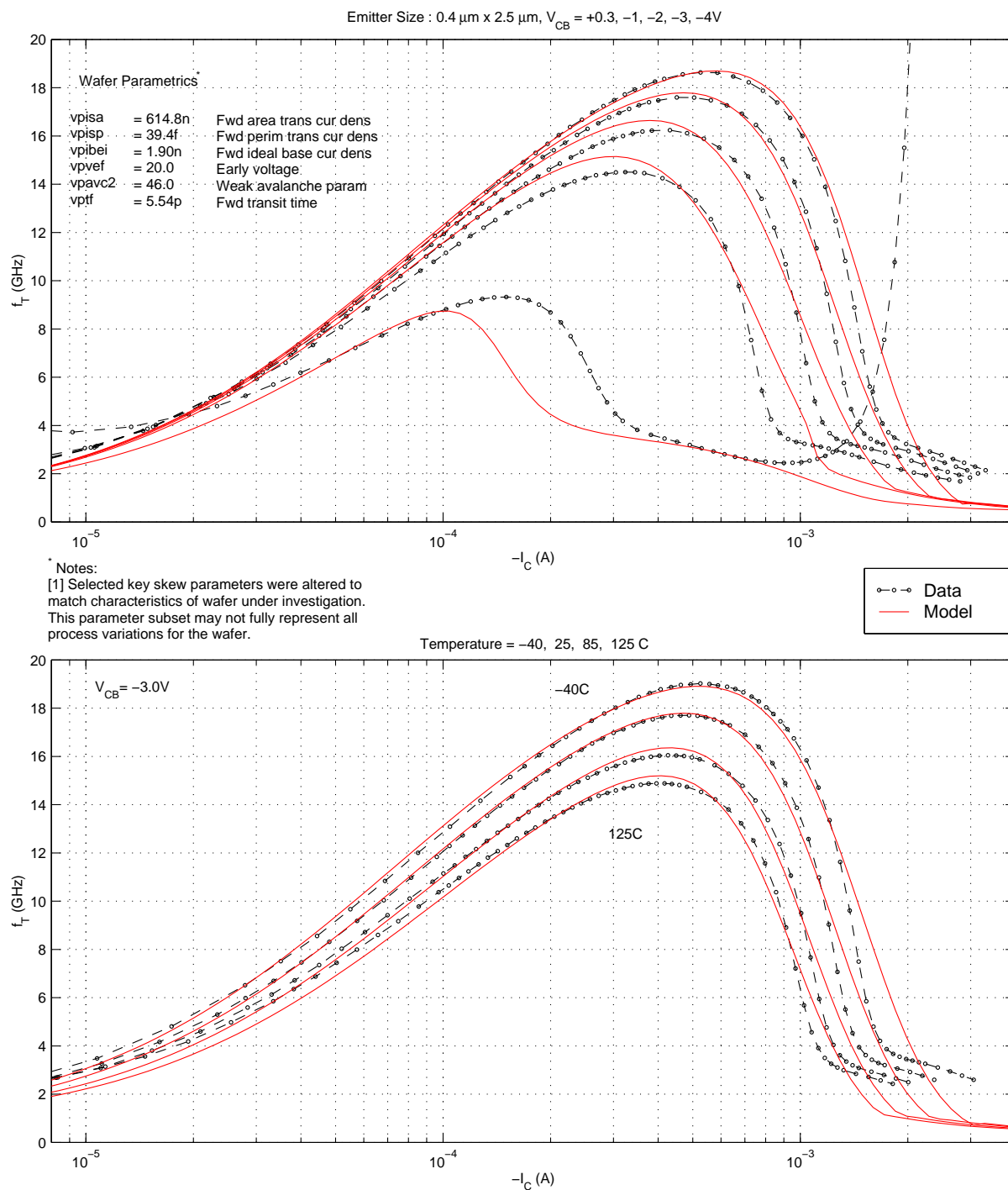


Figure 101. VPNP f_T vs I_C - V_{cb} and Temperature Dependence for $0.4\ \mu\text{m} \times 2.5\ \mu\text{m} \times 1$ Emitter

BiCMOS8HP Vertical PNP – Typical f_t Characteristics

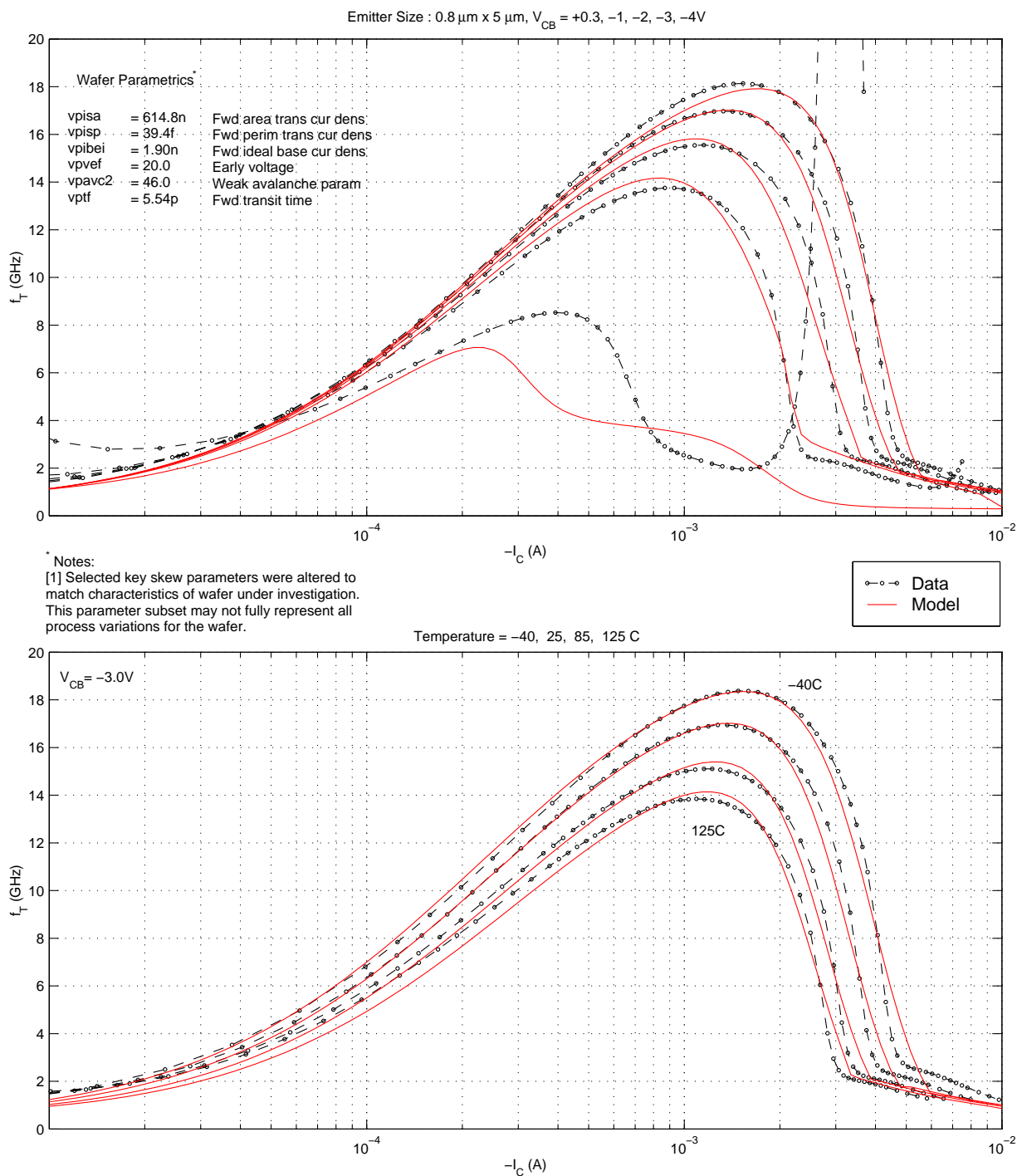


Figure 102. VPNP f_t vs I_C - V_{cb} and Temperature Dependence for $0.8\ \mu\text{m} \times 5\ \mu\text{m} \times 1$ Emitter

4.7 S-Parameter Correlation Plots

The following plots compare the S-Parameter characteristics of the vnp model with measurement data from the initial device hardware. As the model supports a range of emitter widths and lengths, the plots show the model correlation for a few select device sizes.

Table 45. VNP S-Parameter Correlation Plots

Emitter Length and # Stripes L x #E	Emitter Width = 0.40 μ m		Emitter Length and # Stripes L x #E	Emitter Width = 0.80 μ m	
	I _B bias	Figure		I _B bias	Figure
1.2 x 1	1.73 μ A	Fig 103	2.5 x 1	7.2 μ A	Fig 110
2.5 x 1	3.6 μ A	Fig 104	3 x 1	8.6 μ A	Fig 111
5 x 1	7.2 μ A	Fig 105	5 x 1	14.4 μ A	Fig 112
10 x 1	14.4 μ A	Fig 106	10 x 1	28.8 μ A	Fig 113
10 x 2	28.8 μ A	Fig 107	10 x 2	57.6 μ A	Fig 114
20 x 1	28.8 μ A	Fig 108	20 x 1	57.6 μ A	Fig 115
20 x 2	57.6 μ A	Fig 109	20 x 2	115.2 μ A	Fig 116

- The top four plots in each figure show the magnitude and phase for the S-Parameters from 100MHz to 40GHz at a base current equal to 0.167 x the I_B bias value listed in the table, which is near the peak f_T for the device.
- The “RF Current Gain” plot in the lower left of the page depicts the magnitude, in dB, of the Current Gain (H₂₁) for a series of fixed base currents, which are defined as 0.033, 0.167 and 0.64 x the I_B bias value listed in the table. Extrapolation of H₂₁ down to zero gives the f_T value.
- The “RF Power Gain” plot in the lower right of the page depicts the magnitudes, in dB, of the Maximum Available/Maximum Stable Power Gain (MAG/MSG) for a series of fixed base currents, which are defined as 0.033, 0.167 and 0.64 the I_B bias value listed in the table. Extrapolation of MAG/MSG down to zero gives the f_{MAX} value.

Along with the nominal temperature (25C) plots, S-parameter characteristics at high and low temperatures are shown as follows:

Table 46. VNP S-Parameter Temperature Plots

Device Emitter Size (W x L x #E)	@ 125C	@ -40C
0.4 x 2.5 x 1	Fig 117	Fig 118
0.8 x 5 x 1	Fig 119	Fig 120

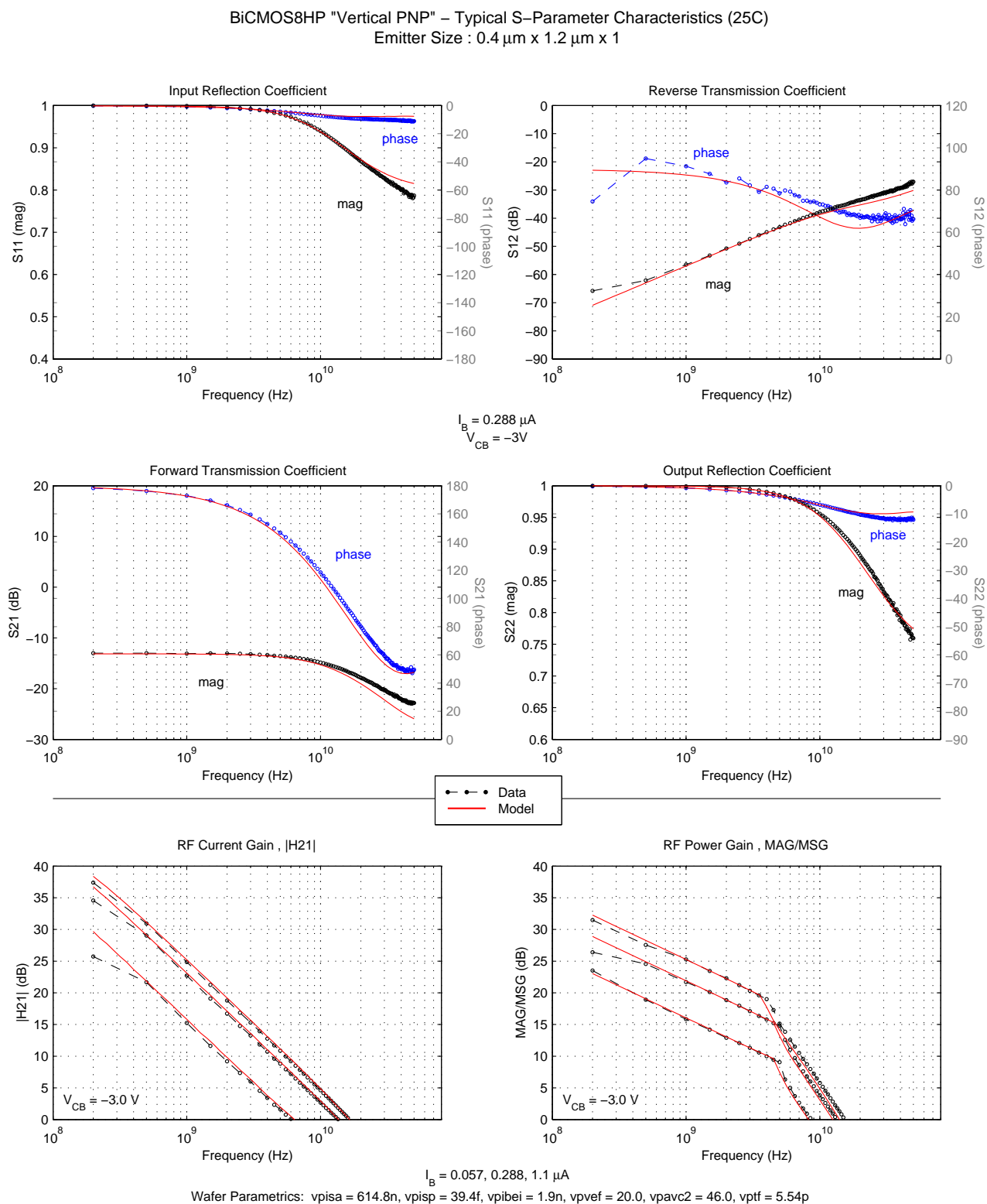


Figure 103. VPNP S-Parameter Characteristics for 0.4 μm x 1.2 μm x 1 Emitter

BiCMOS8HP "Vertical PNP" – Typical S-Parameter Characteristics (25C)
Emitter Size : 0.4 μm x 2.5 μm x 1

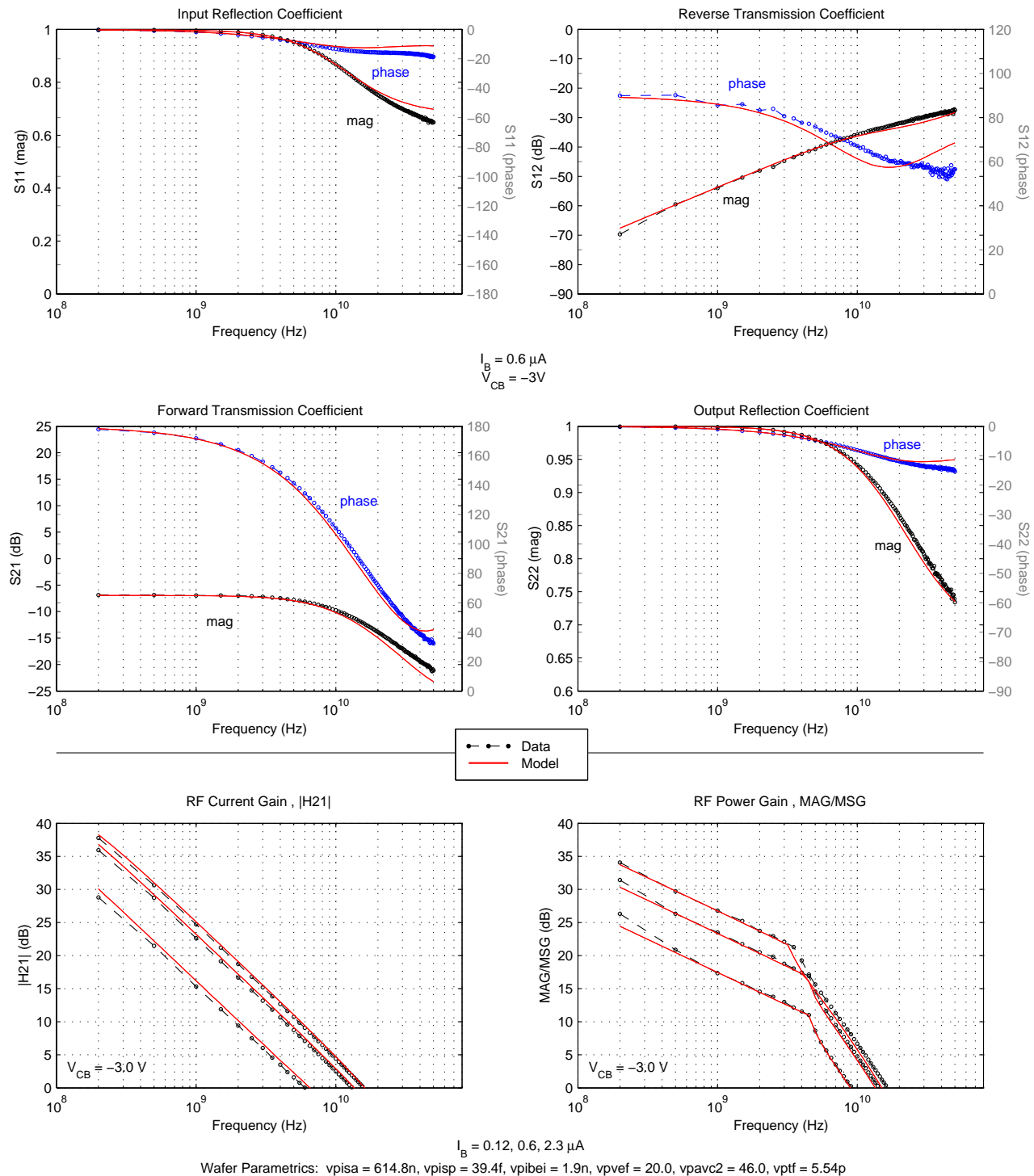


Figure 104. VPNP S-Parameter Characteristics for 0.4 μm x 2.5 μm x 1 Emitter

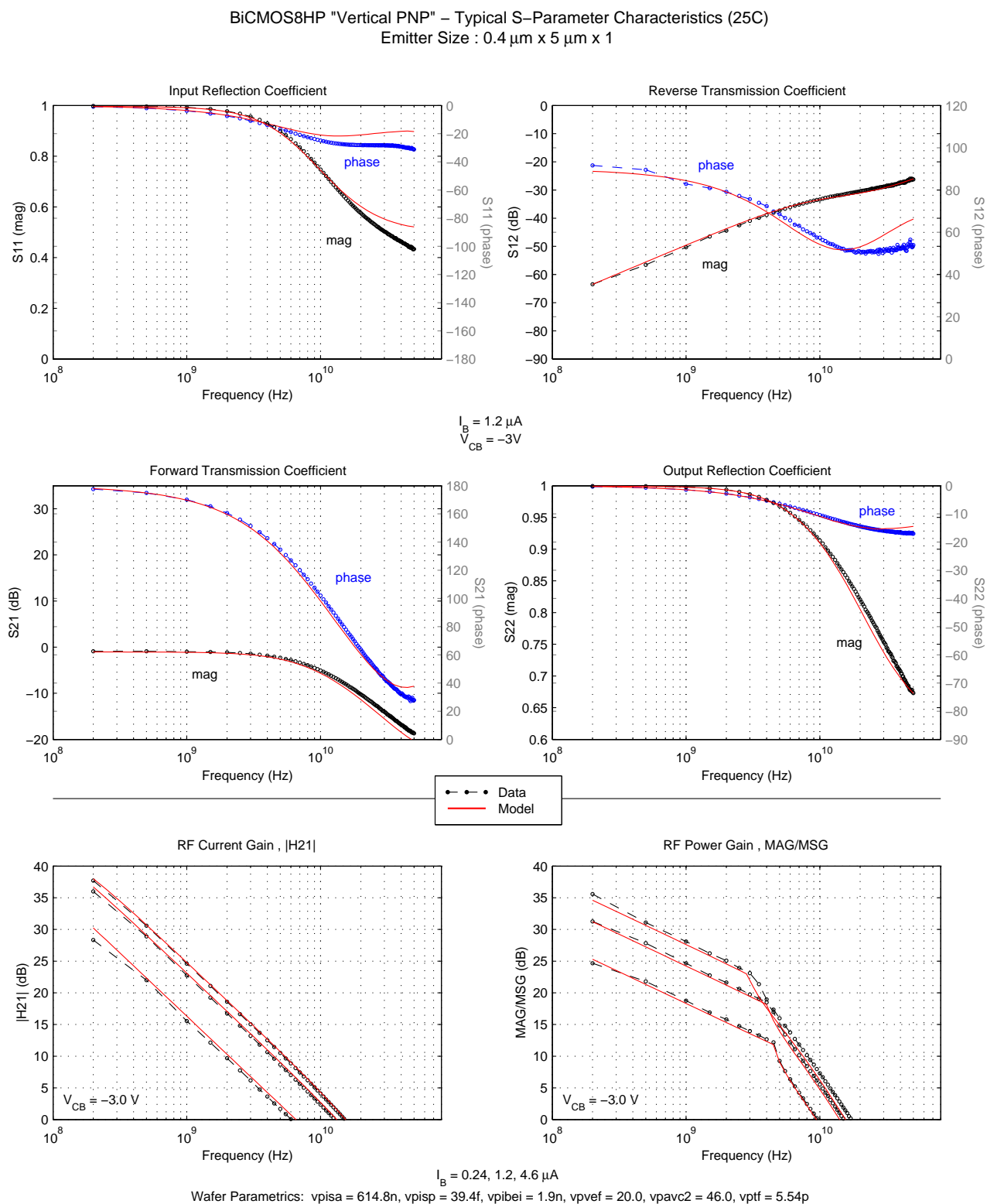


Figure 105. VPNP S-Parameter Characteristics for 0.4 μm x 5 μm x 1 Emitter

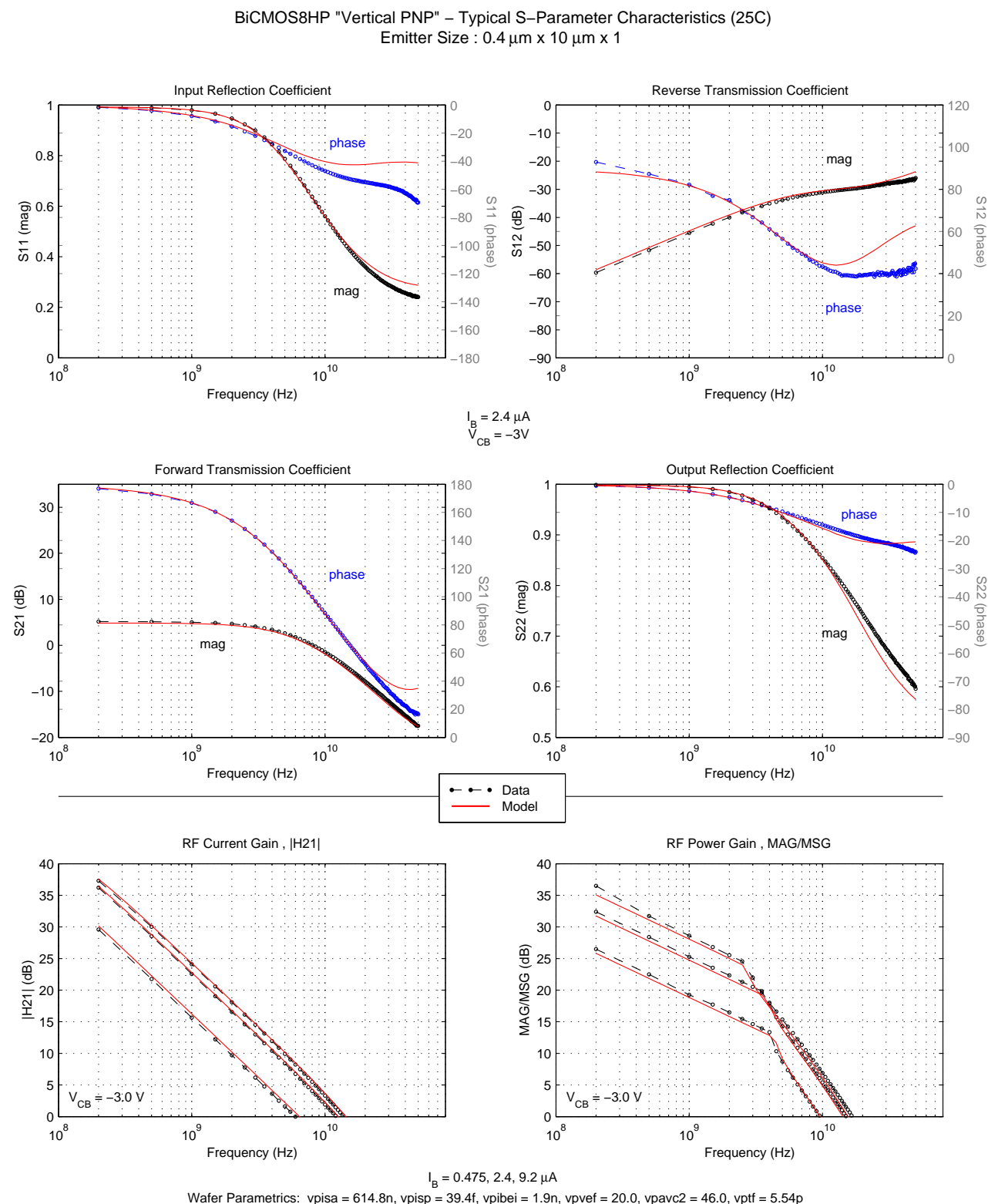


Figure 106. VPNP S-Parameter Characteristics for 0.4 μm x 10 μm x 1 Emitter

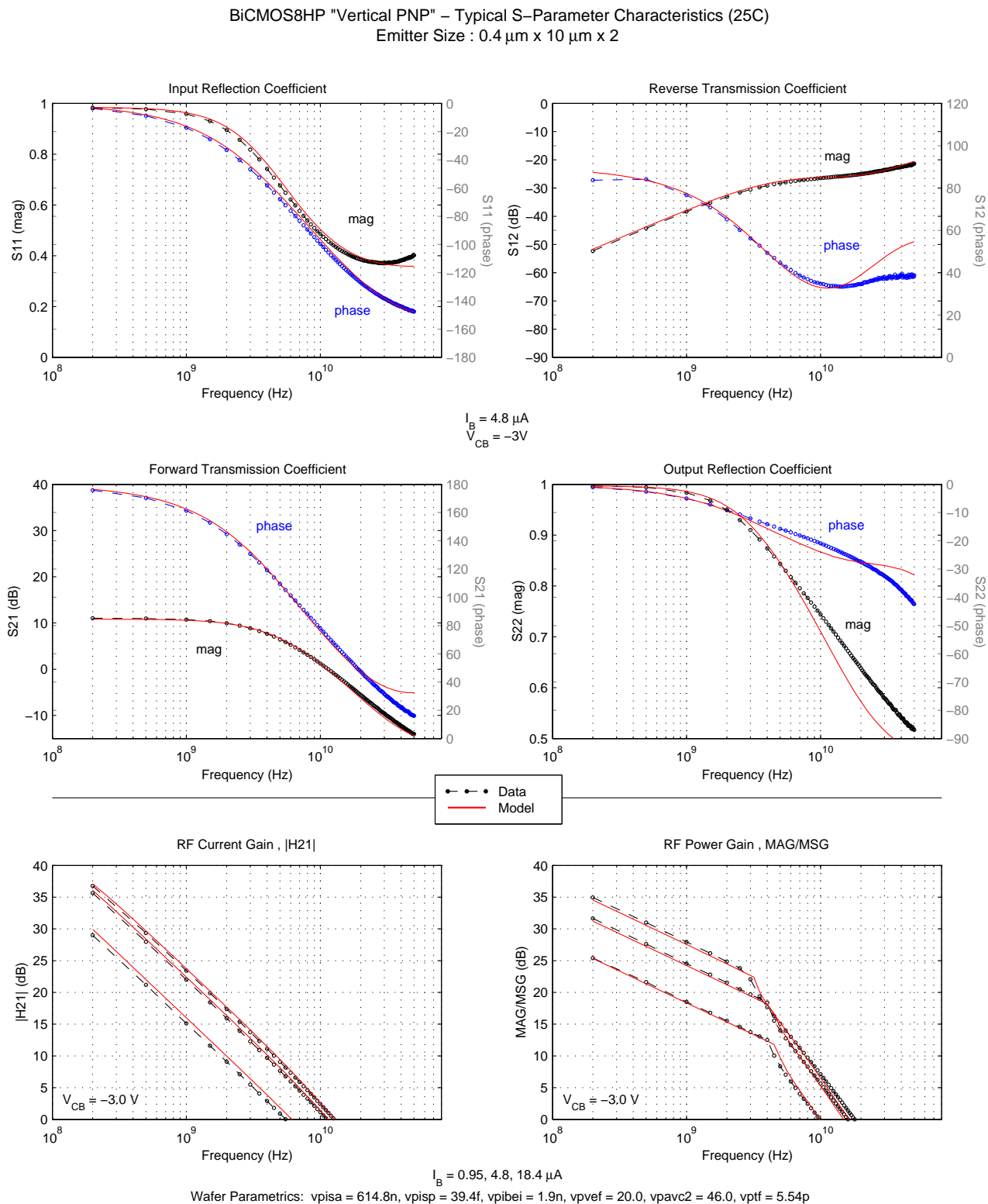


Figure 107. VPNP S-Parameter Characteristics for 0.4 μm x 10 μm x 2 Emitter

BiCMOS8HP "Vertical PNP" – Typical S-Parameter Characteristics (25C)
Emitter Size : 0.4 μm x 20 μm x 1

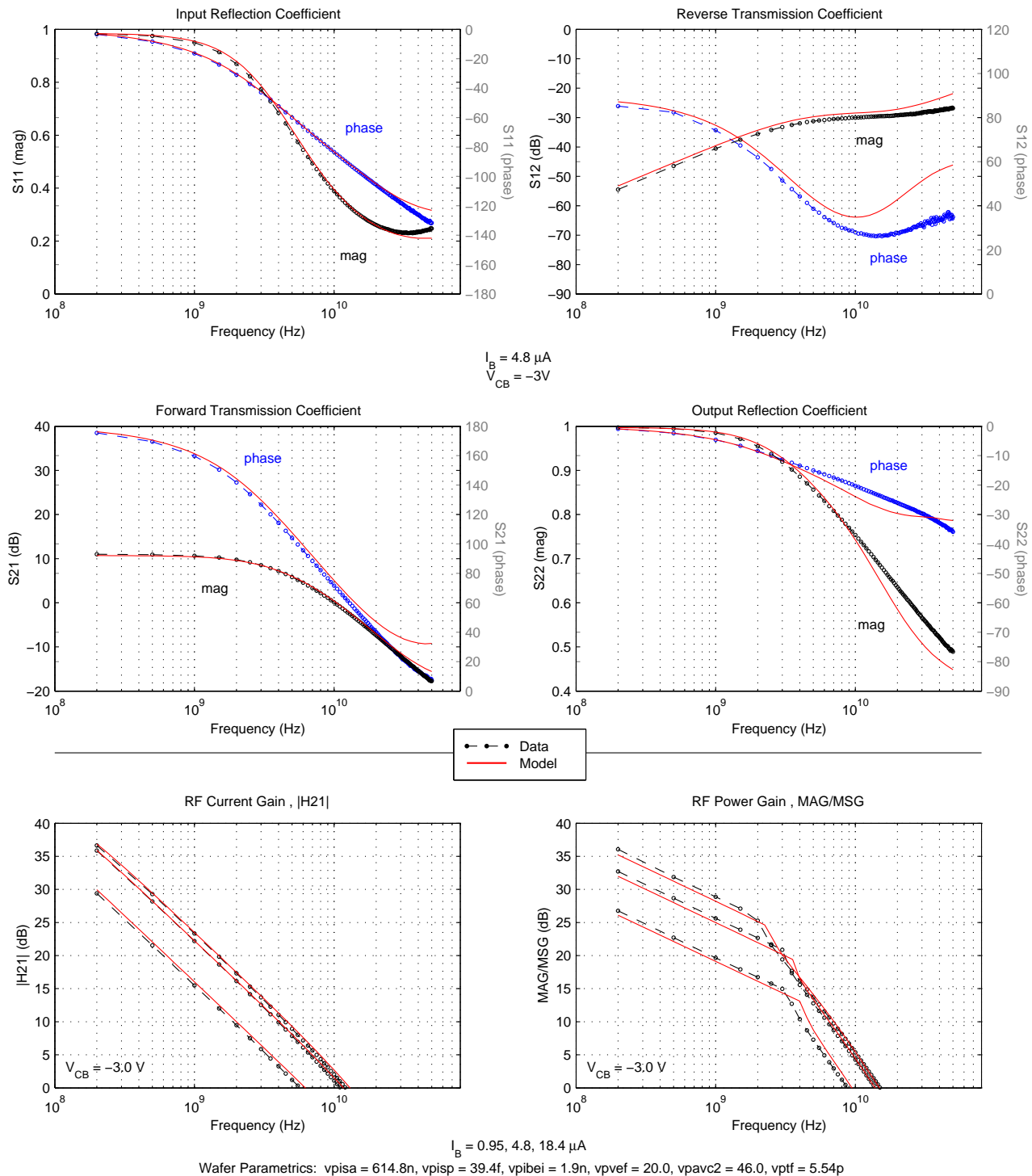


Figure 108. VPNP S-Parameter Characteristics for 0.4 μm x 20 μm x 1 Emitter

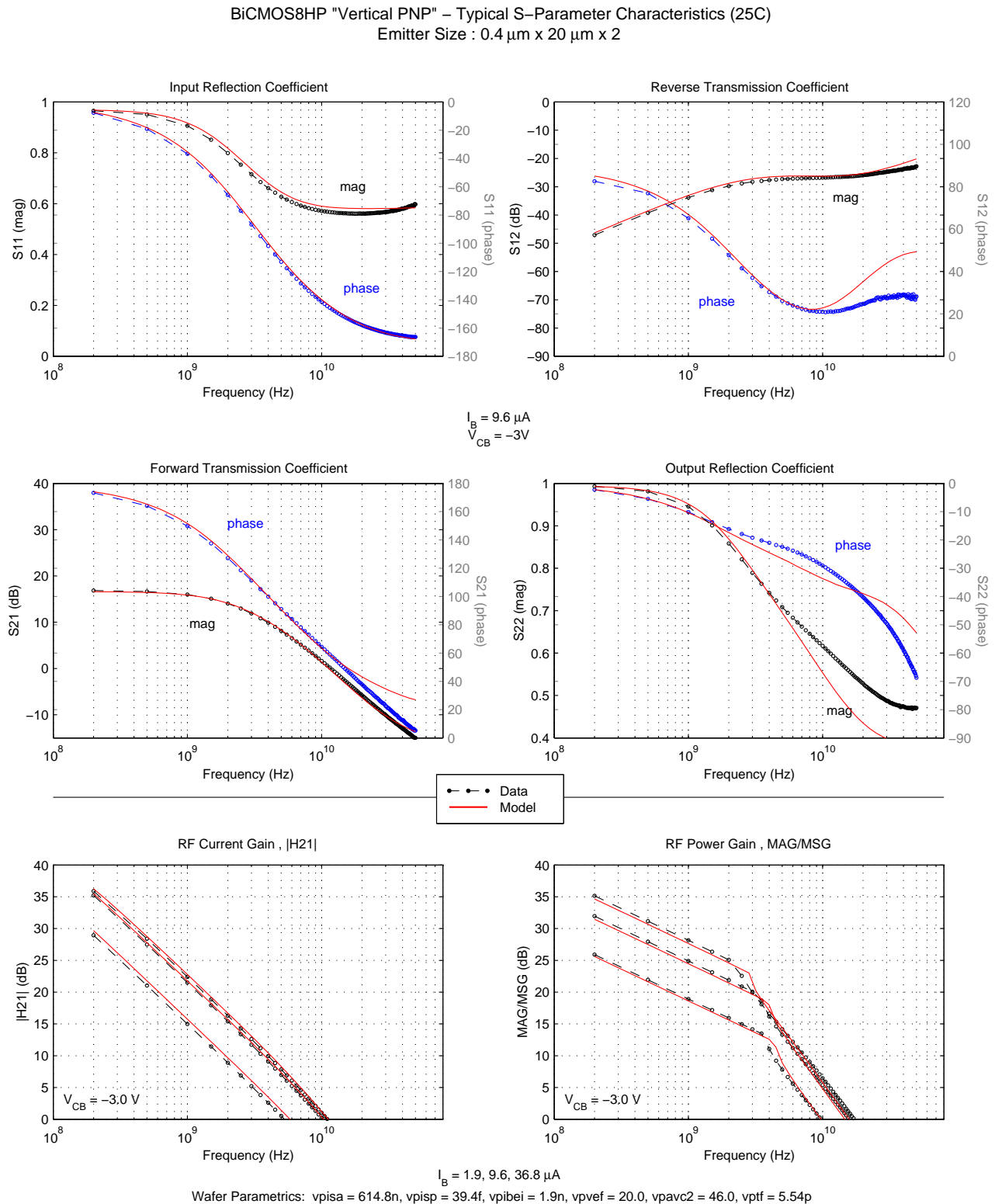


Figure 109. VPNP S-Parameter Characteristics for 0.4 μm x 20 μm x 2 Emitter

BiCMOS8HP "Vertical PNP" – Typical S-Parameter Characteristics (25C)
Emitter Size : 0.8 μm x 2.5 μm x 1

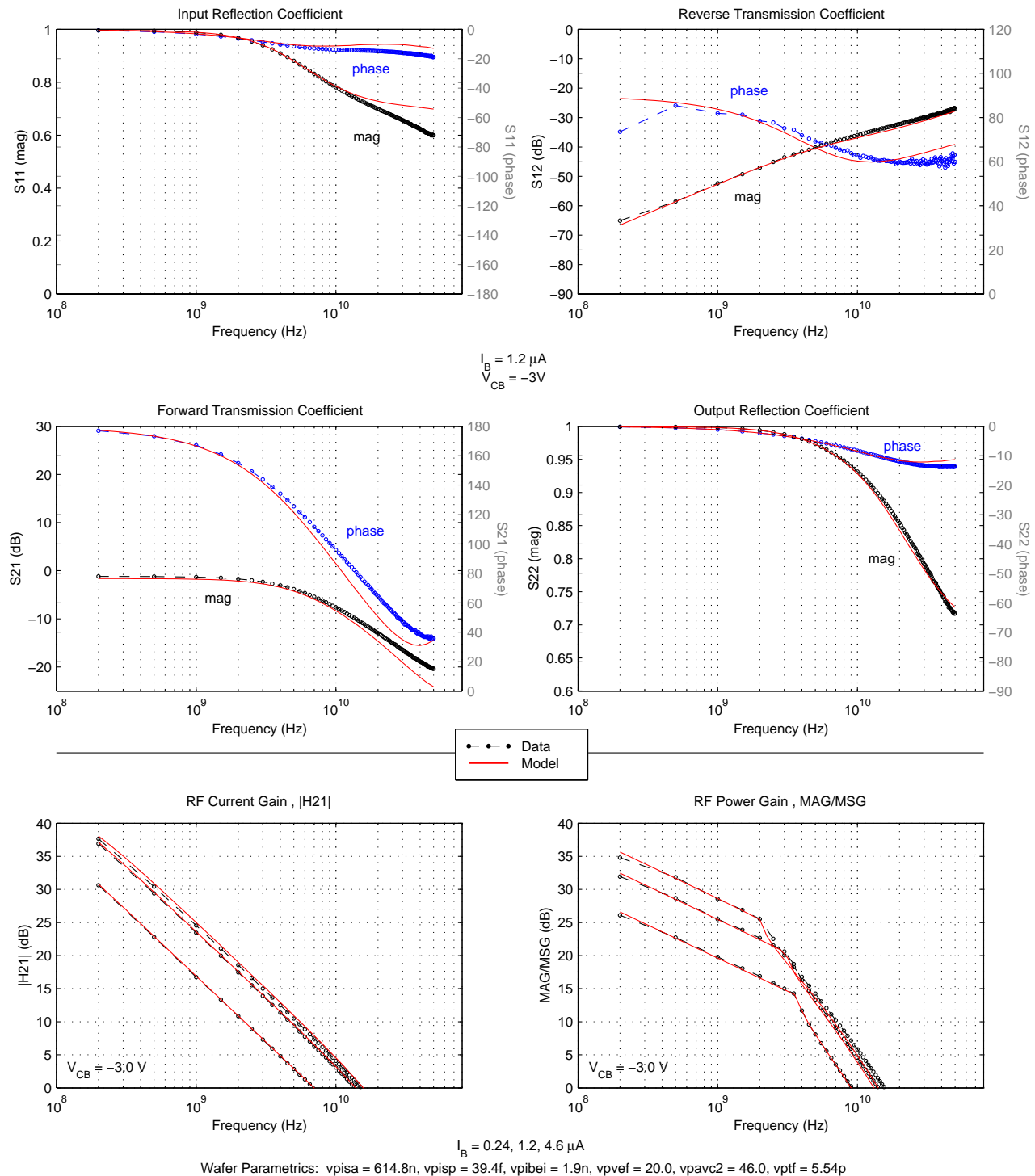


Figure 110. VPNP S-Parameter Characteristics for 0.8 μm x 2.5 μm x 1 Emitter

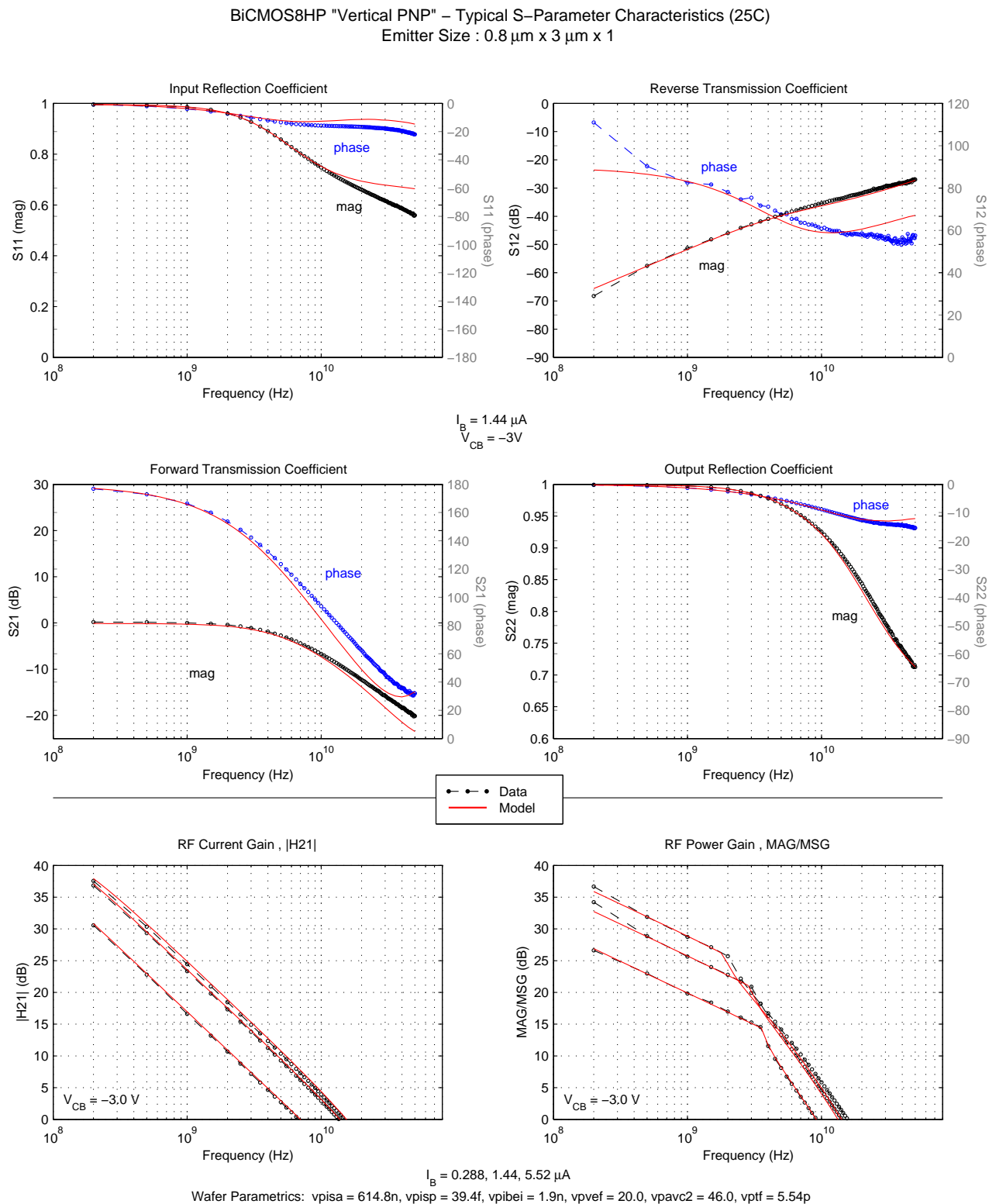


Figure 111. VPNP S-Parameter Characteristics for 0.8 μm x 3 μm x 1 Emitter

BiCMOS8HP "Vertical PNP" – Typical S-Parameter Characteristics (25C)
Emitter Size : 0.8 μm x 5 μm x 1

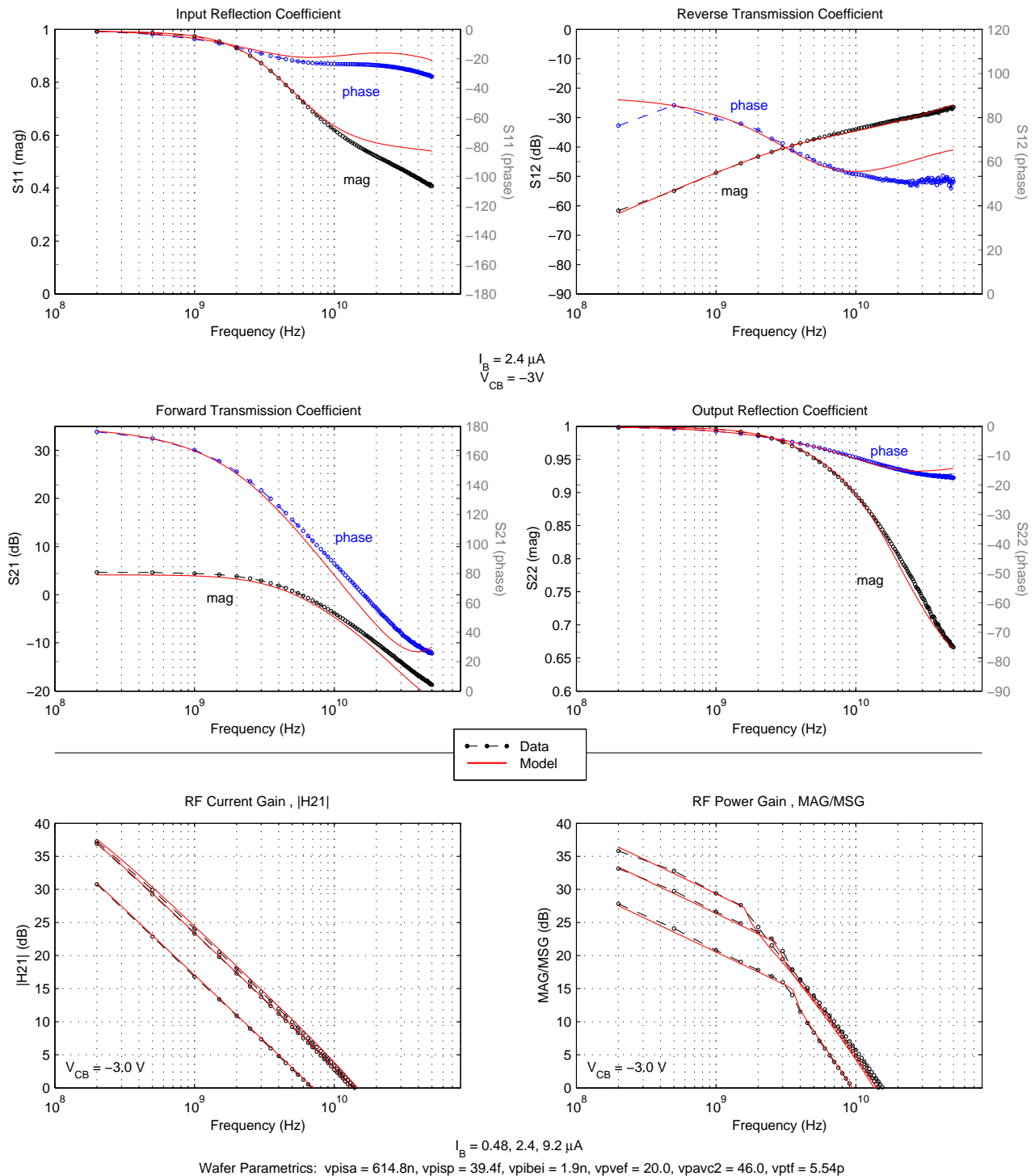


Figure 112. VPNP S-Parameter Characteristics for 0.8 μm x 5 μm x 1 Emitter

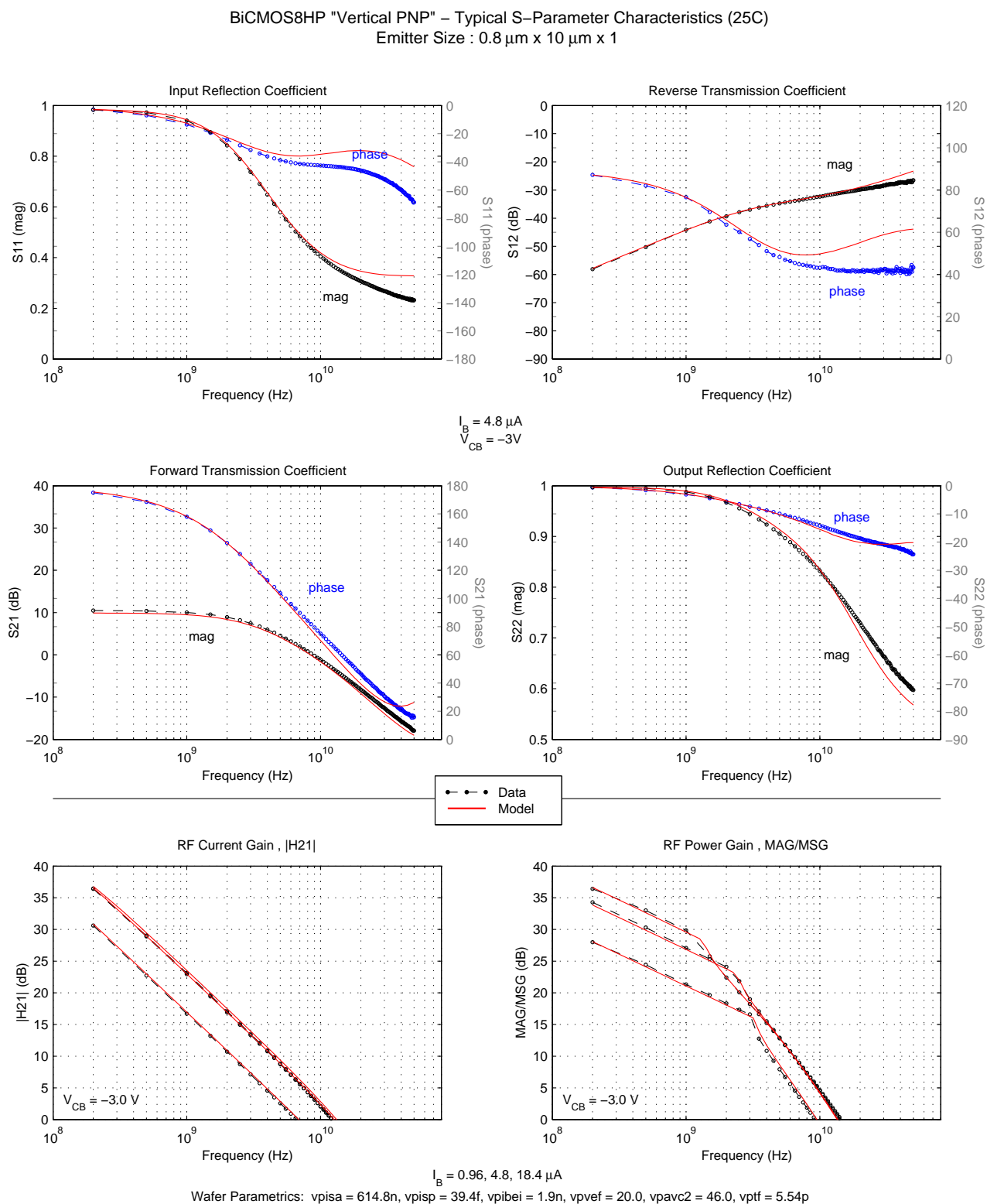


Figure 113. VPNP S-Parameter Characteristics for 0.8 μm x 10 μm x 1 Emitter

BiCMOS8HP "Vertical PNP" – Typical S-Parameter Characteristics (25C)
Emitter Size : 0.8 μm x 10 μm x 2

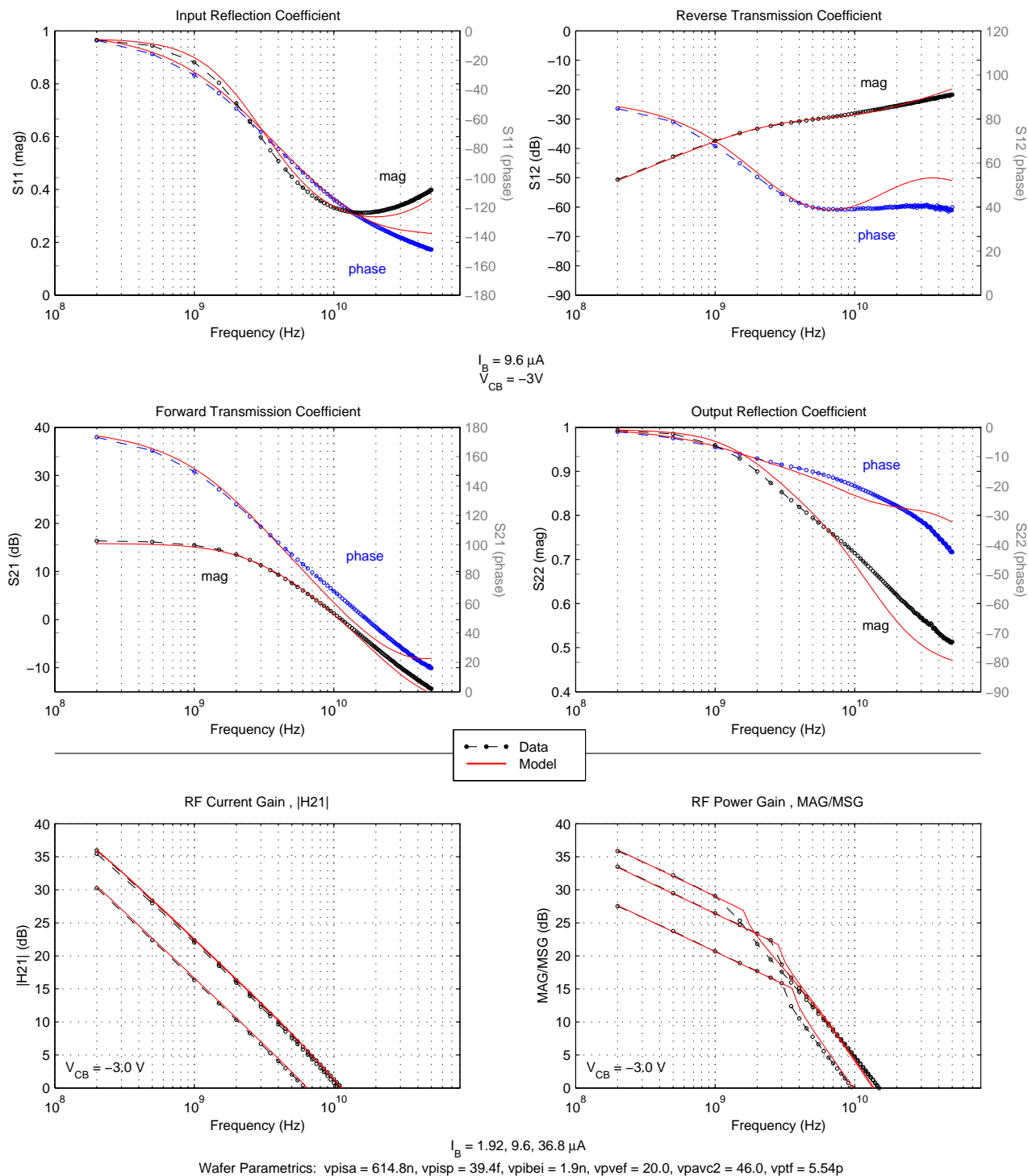


Figure 114. VPNP S-Parameter Characteristics for 0.8 μm x 10 μm x 2 Emitter

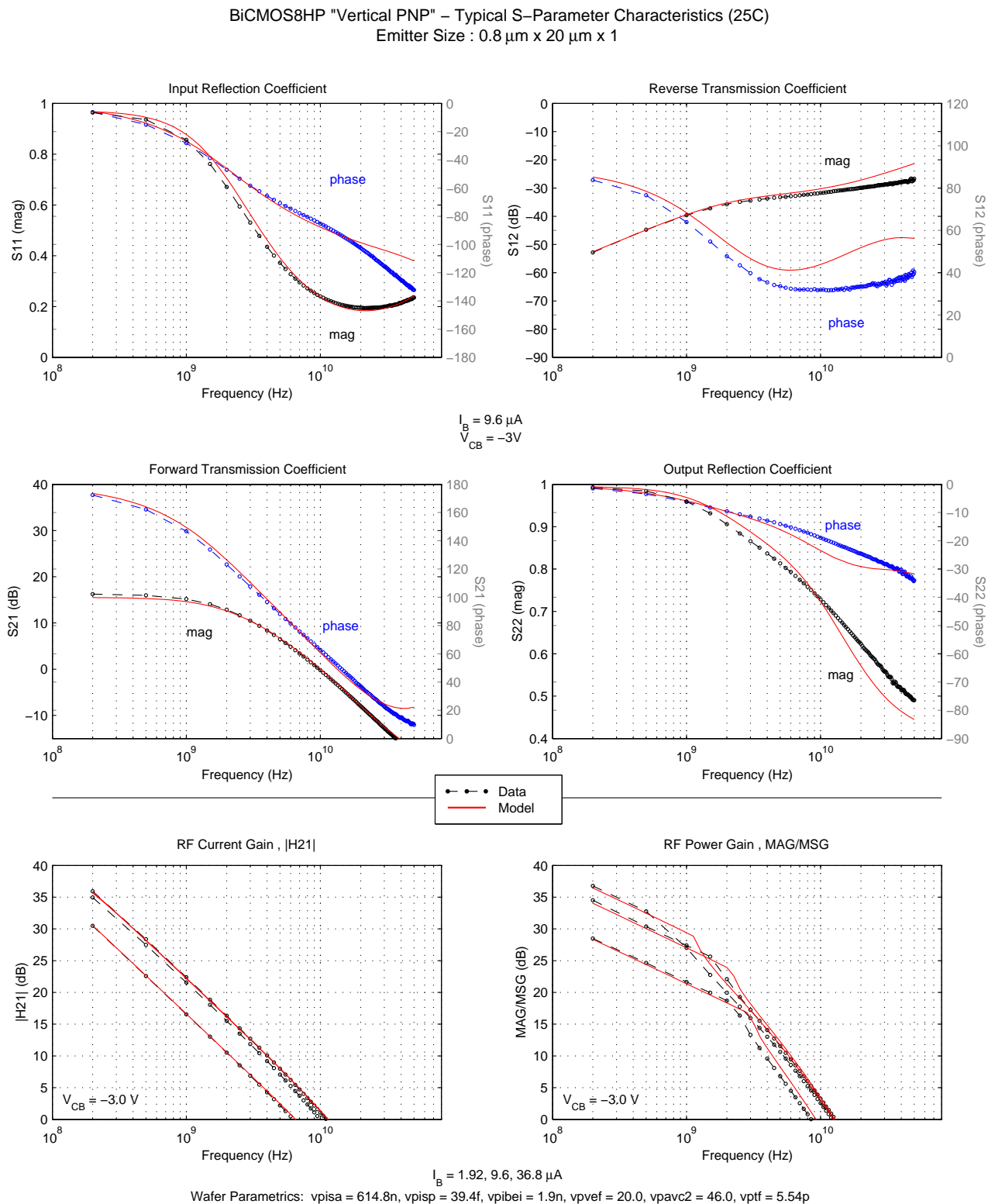


Figure 115. VPNP S-Parameter Characteristics for 0.8 μm x 20 μm x 1 Emitter

BiCMOS8HP "Vertical PNP" – Typical S-Parameter Characteristics (25C)
Emitter Size : 0.8 μm x 20 μm x 2

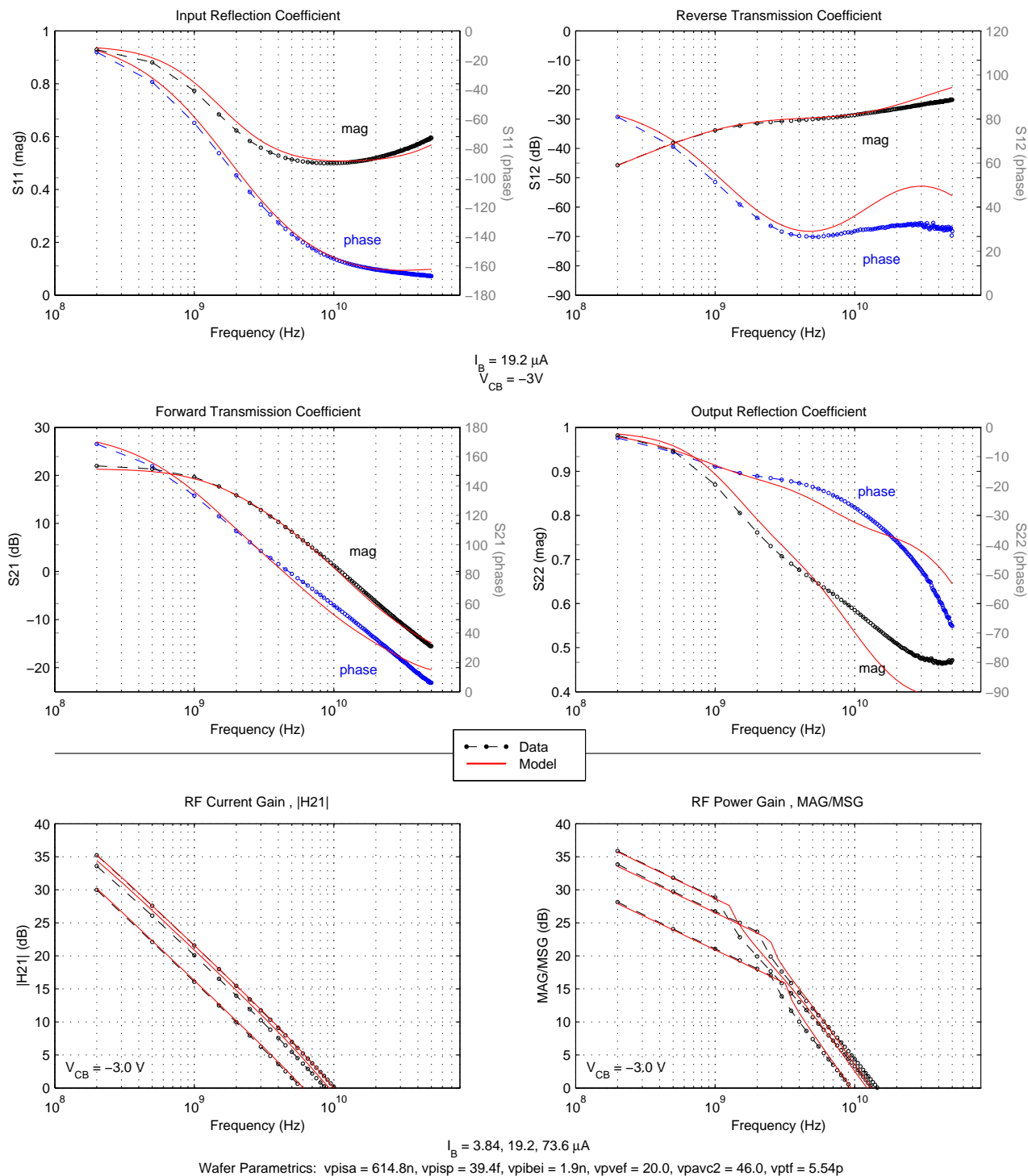


Figure 116. VPNP S-Parameter Characteristics for 0.8 μm x 20 μm x 2 Emitter

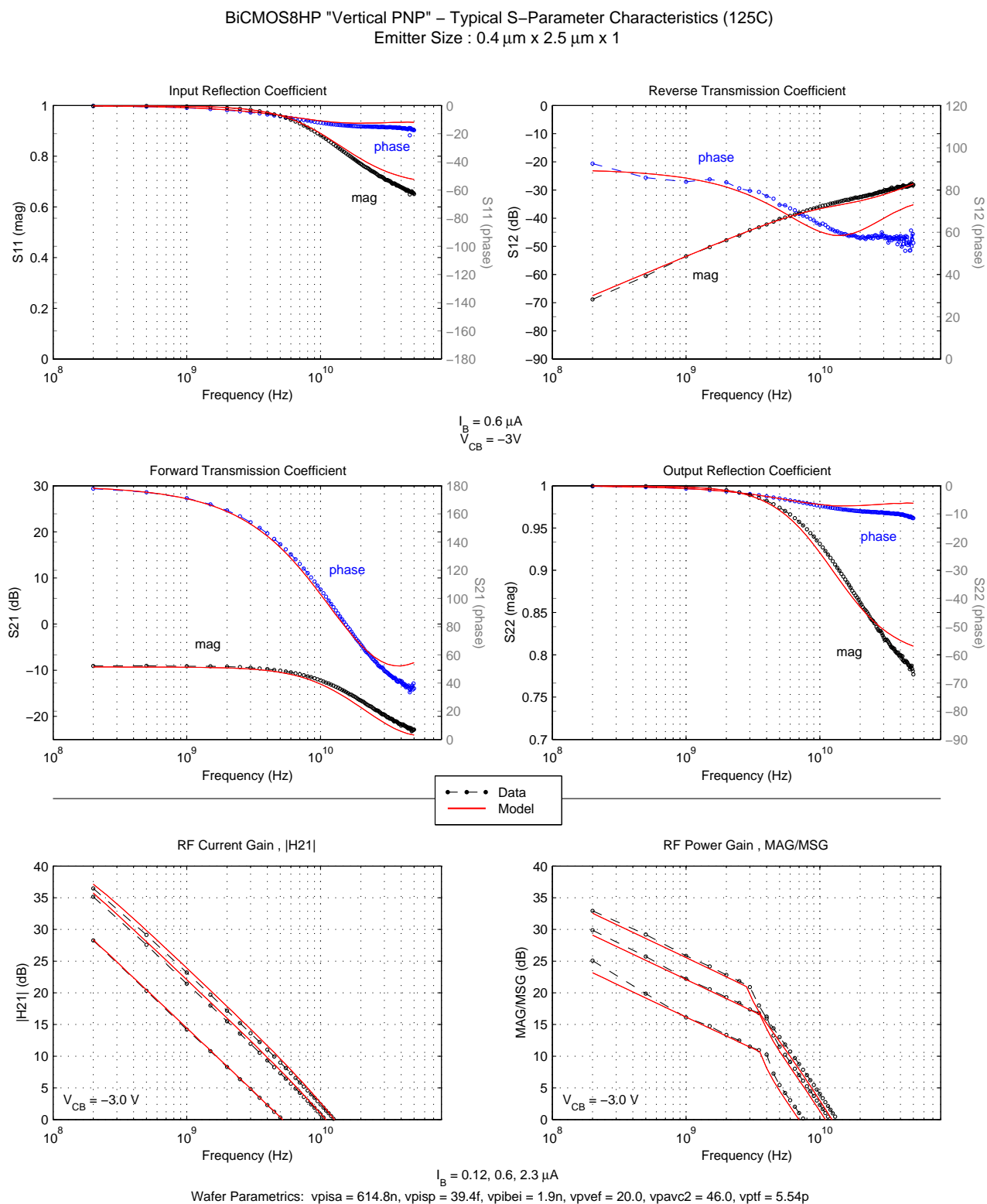


Figure 117. VNP S-Parameter Characteristics for 0.4 μm x 2.5 μm x 1 Emitter (125C)

BiCMOS8HP "Vertical PNP" – Typical S-Parameter Characteristics (–40C)
Emitter Size : 0.4 μm x 2.5 μm x 1

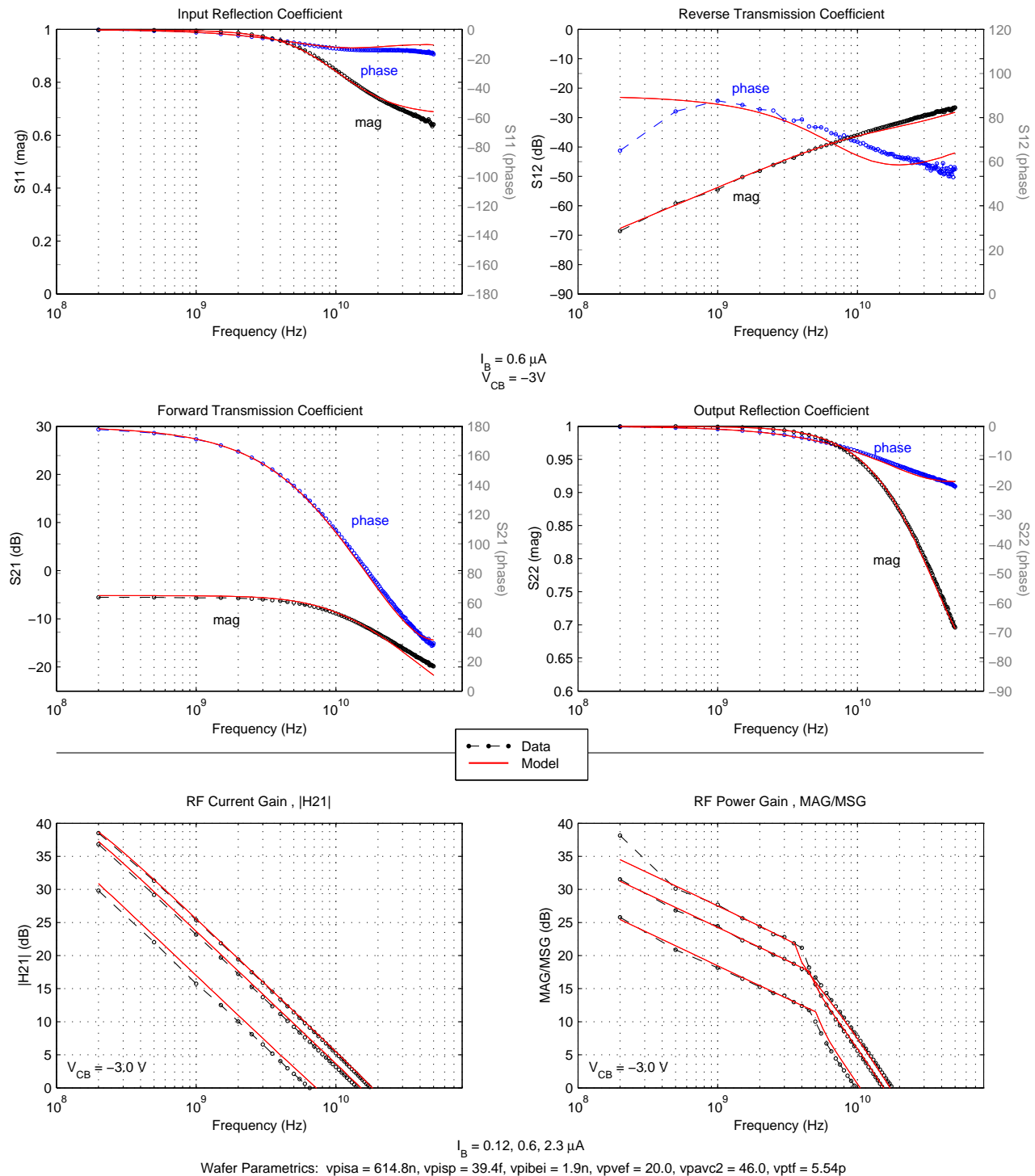


Figure 118. VPNP S-Parameter Characteristics for 0.4 μm x 2.5 μm x 1 Emitter (–40C)

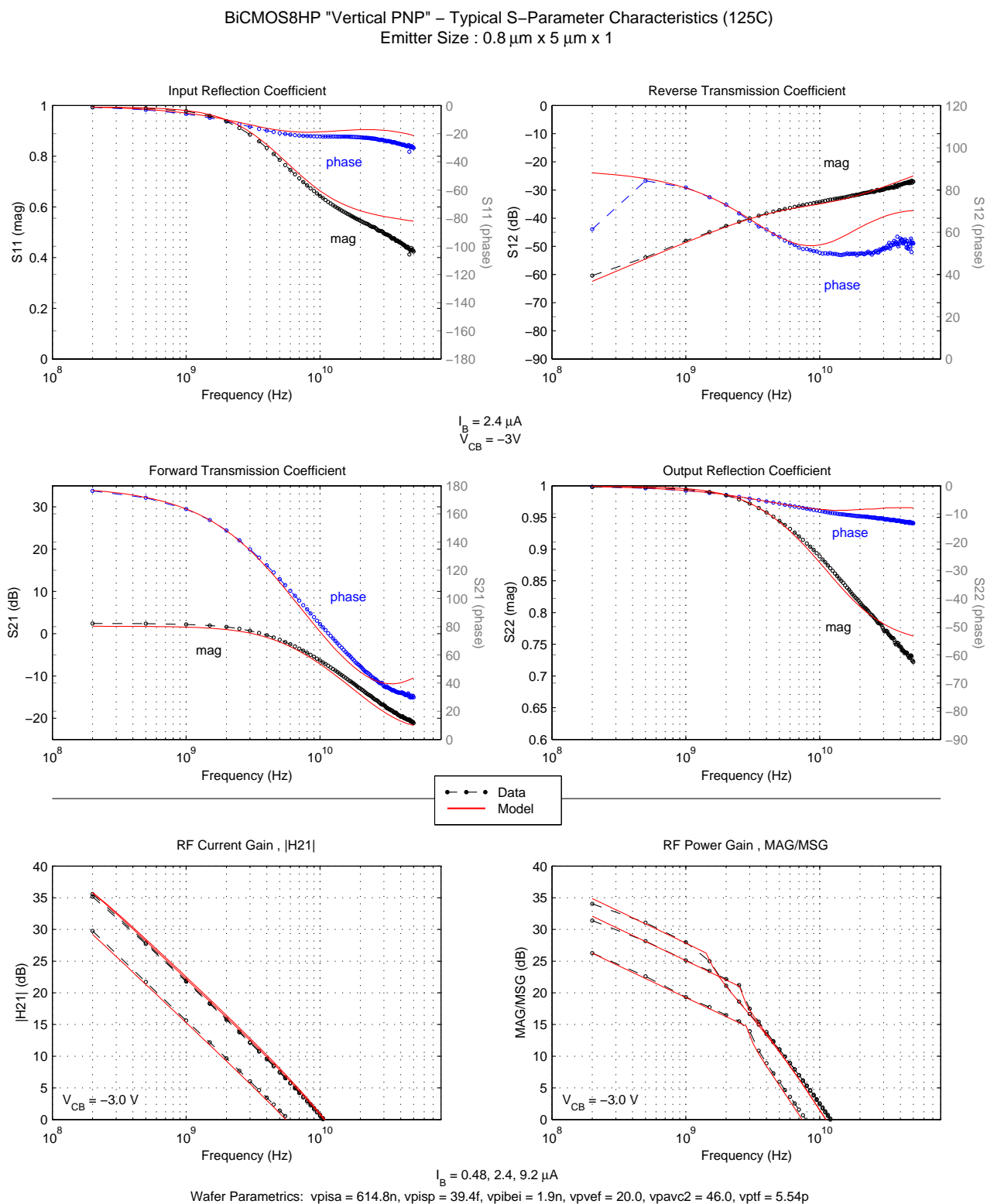


Figure 119. VPNP S-Parameter Characteristics for 0.8 μm x 5 μm x 1 Emitter (125C)

BiCMOS8HP "Vertical PNP" – Typical S-Parameter Characteristics (–40C)
Emitter Size : 0.8 μm x 5 μm x 1

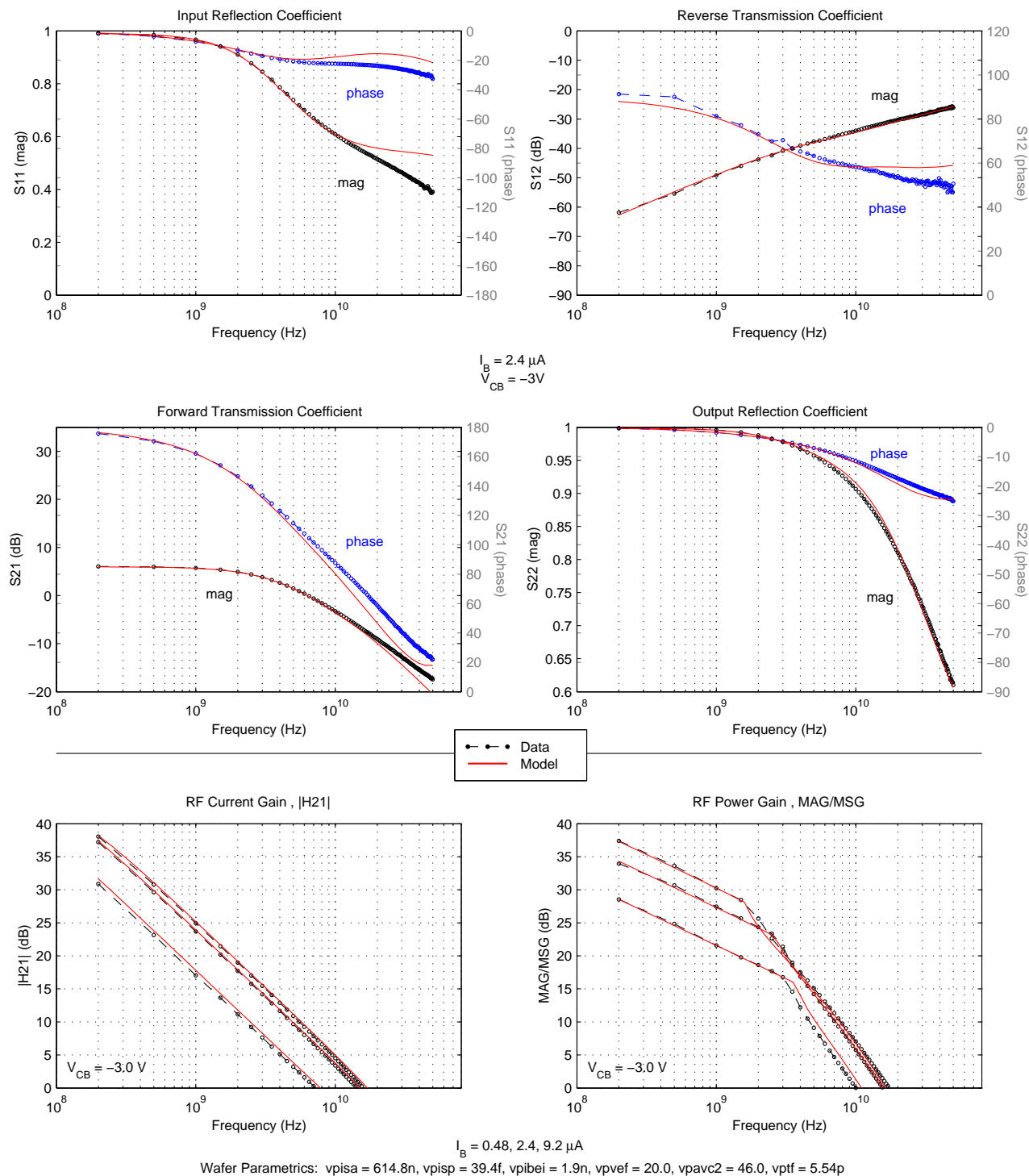


Figure 120. VPNP S-Parameter Characteristics for 0.8 μm x 5 μm x 1 Emitter (–40C)

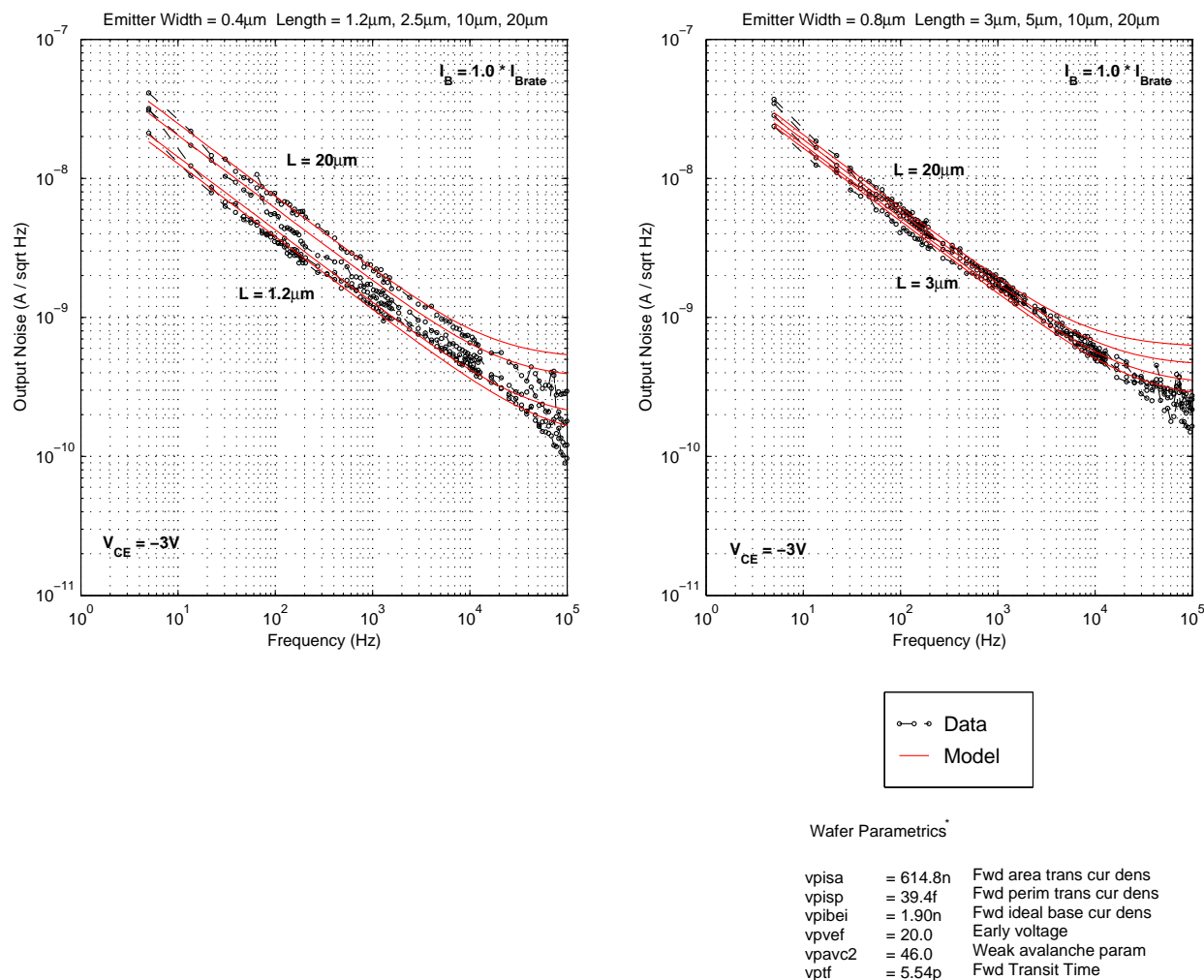
4.8 1/f Noise Correlation Plots

The data measurements for vnp 1/f noise were made on single device test structures with the BTA 9812A Noise Analyzer System. The output noise spectrum plots were generated at fixed base current biases for several device sizes, as noted in each figure.

The following plots illustrate the model-to-hardware correlation for 1/f noise:

<i>Table 47. VPNP Flicker Noise Plots</i>		
1/f Noise Characteristic	Emitter Width = 0.40μm	Emitter Width = 0.80μm
Emitter Length Scaling	Fig 121	Fig 121
Ib Bias Dependence	Fig 122	Fig 122
Vce Bias Dependence	Fig 123	Fig 123

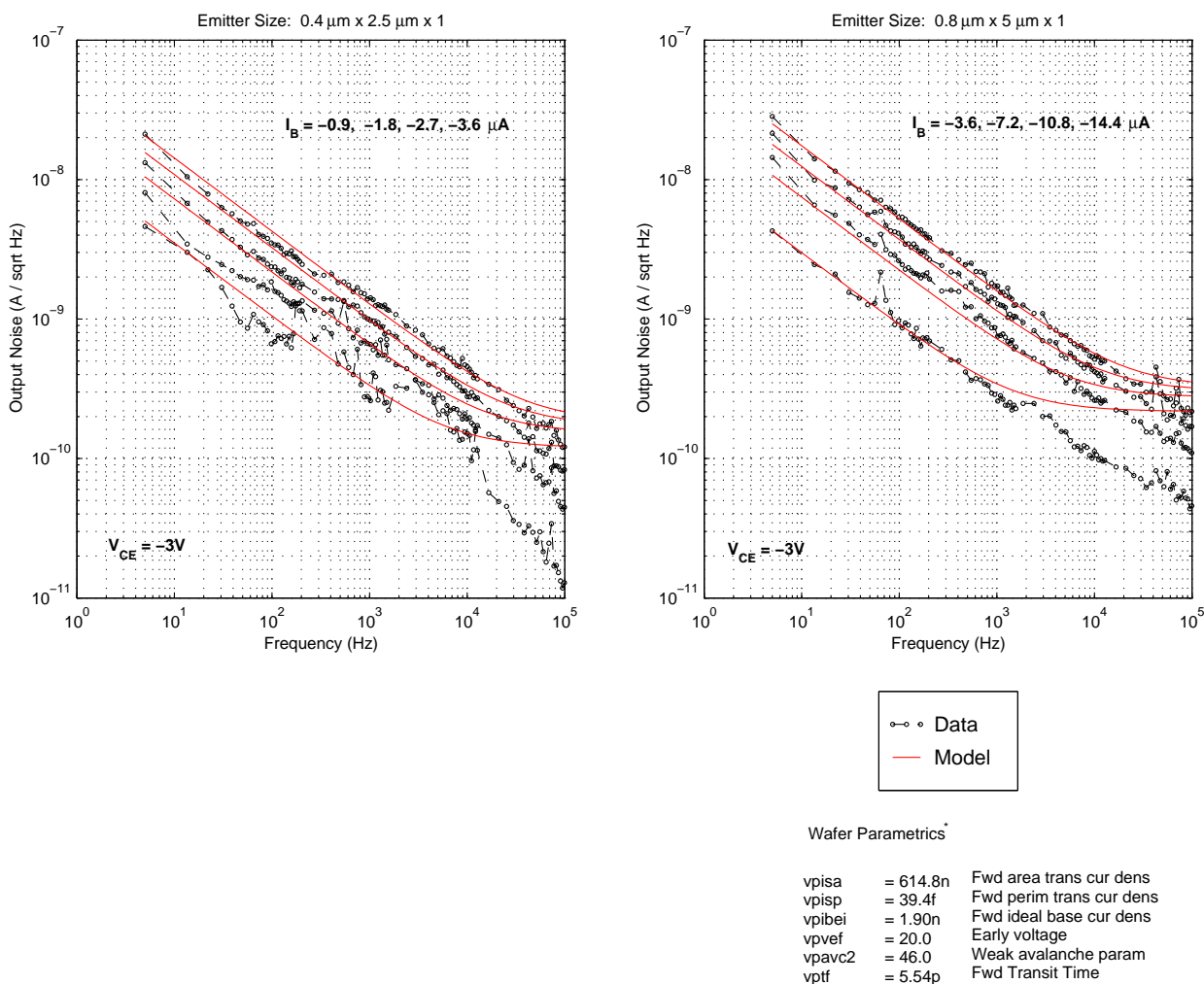
BiCMOS8HP VPNP – Typical 1/f Noise Characteristics vs Emitter Length (25C)



* Notes:
[1] Selected key skew parameters were altered to match characteristics of wafer under investigation. This parameter subset may not fully represent all process variations for the wafer.

Figure 121. VPNP 1/f Noise Characteristics - Emitter Length Scaling

BiCMOS8HP VPNP – Typical 1/f Noise Characteristics vs Base Current (25C)



* Notes:
 [1] Selected key skew parameters were altered to match characteristics of wafer under investigation. This parameter subset may not fully represent all process variations for the wafer.

Figure 122. VPNP 1/f Noise Characteristics - I_b Bias Dependence

BiCMOS8HP VPNP – Typical 1/f Noise Characteristics vs CE Voltage (25C)

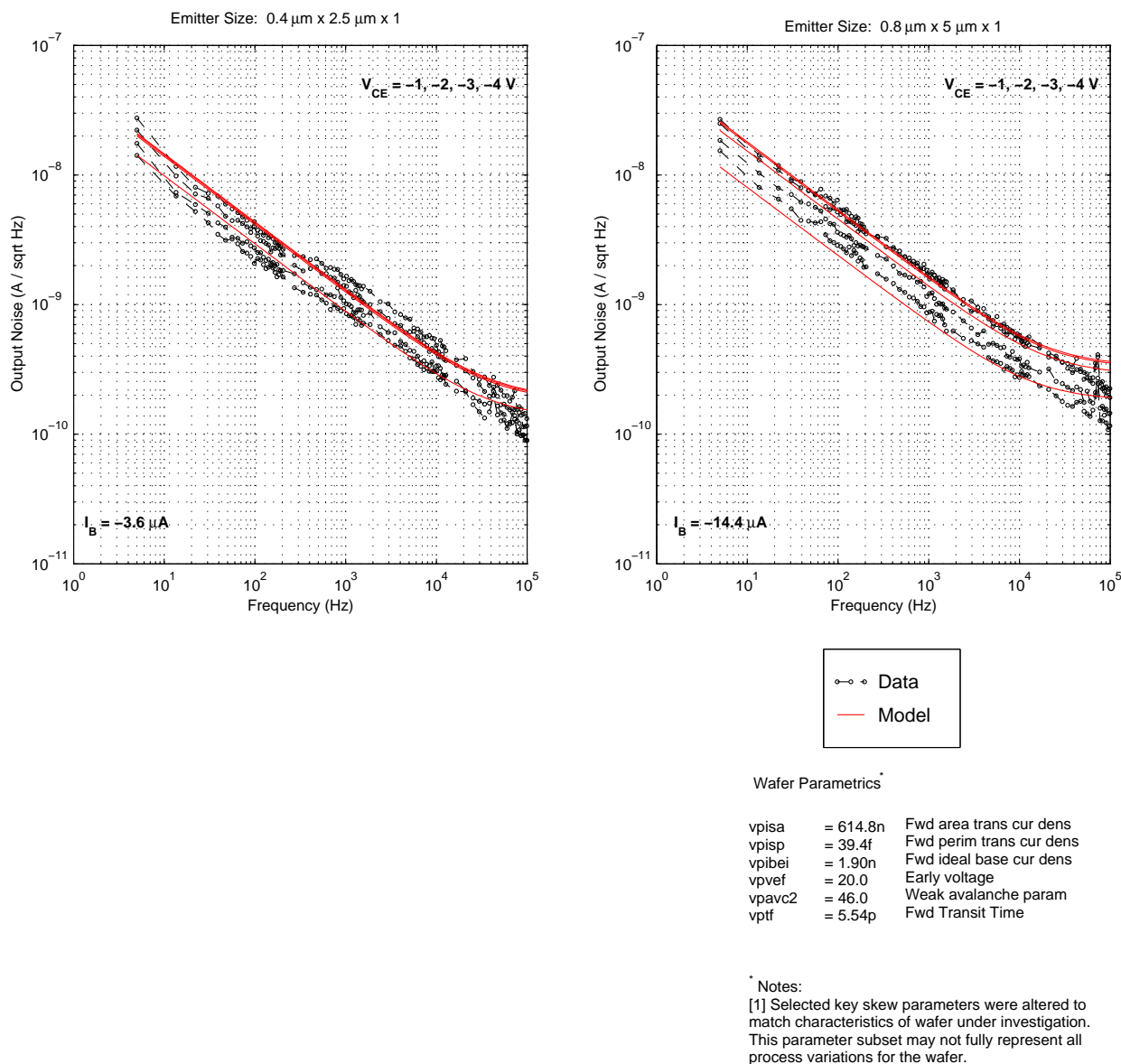


Figure 123. VPNP 1/f Noise Characteristics - Vce Bias Dependence

4.9 Minimum Noise Figure Correlation Plots

Noise figure is defined as:

$$NF = \frac{\text{Input S/N ratio}}{\text{Output S/N ratio}}$$

which provides a convenient measure of the signal-to-noise ratio degradation caused by the circuit under investigation.

The noise figure of a circuit can be optimized through careful selection of an appropriate source impedance. The resulting value is referred to as the *minimum noise figure* (NF_{min}). It should be noted that the source impedance resulting in a minimum noise figure does not, in general, coincide with the source impedance providing maximum power gain. Therefore, a trade-off often exists between design for maximum power gain and design for minimum noise figure.

These initial plots show the minimum noise figure for a sample of vnp device geometries:

Table 48. VNP Minimum Noise Figure Plots				
Emitter Size	Frequency sweep		Ic sweep	
	Ic Bias	Figure	@ 5 GHz	@ 9 GHz
0.4 x 20 x 1	1.06 mA	Fig 124	Fig 126	Fig 127
0.4 x 20 x 2	2.74 mA	Fig 125		
0.8 x 20 x 1	2.11 mA	Fig 128	Fig 130	Fig 131
0.8 x 20 x 2	3.74 mA	Fig 129		

For these figures, the plots are defined as follows:

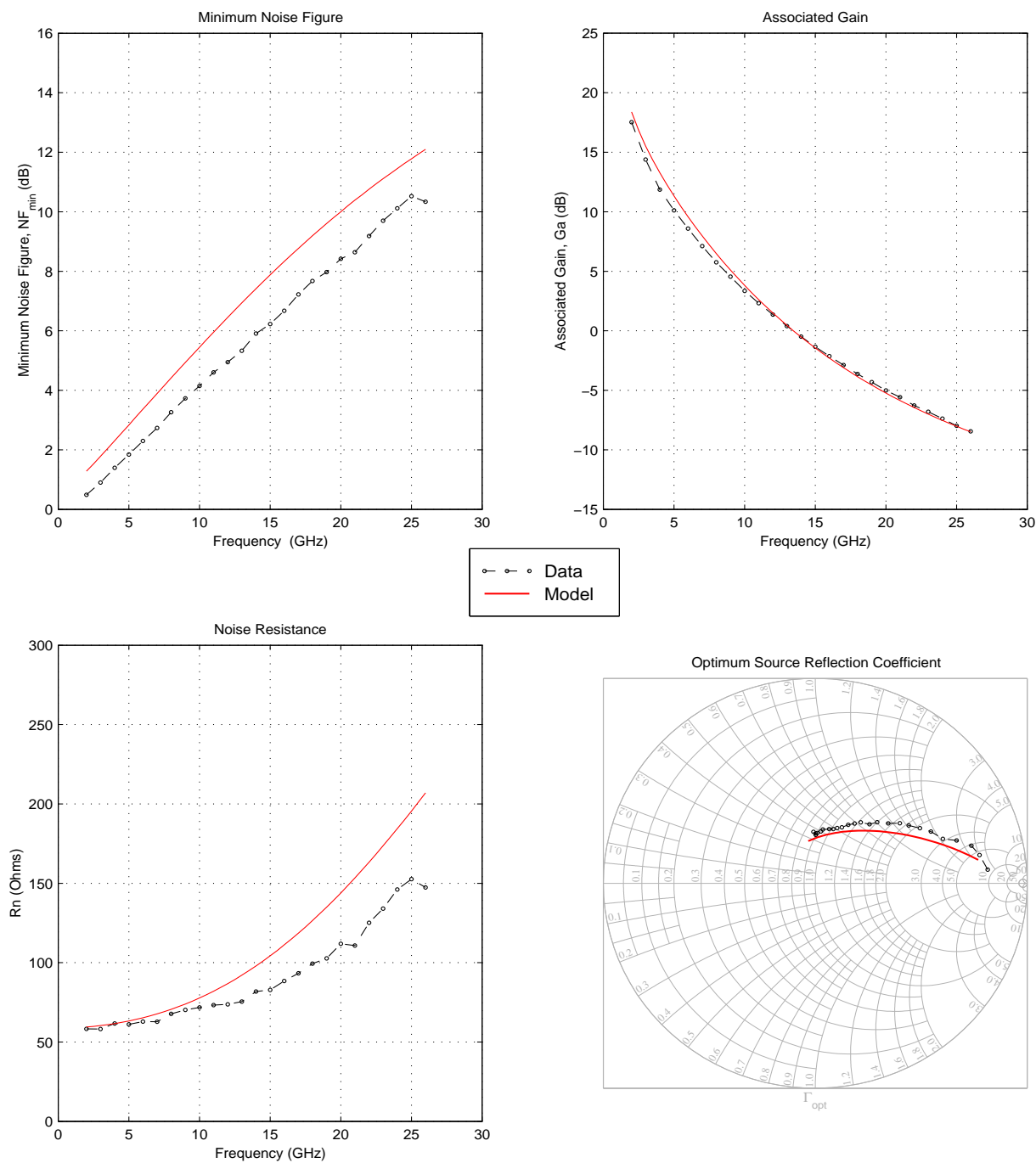
- The upper left plot shows minimum noise figure.
- The upper right plot shows the associated gain at minimum noise figure.
- The lower left plot shows the noise resistance.
- The lower right plot shows the optimum source reflection coefficient required to obtain NF_{min} .

The data was obtained using an Agilent 4142 to bias the device through an ATN NP5 Noise parameter measurement system. The raw noise figure was measured at 8 impedance points and the noise parameters were then extracted. Note that the sensitivity of the noise figure meter is quoted at about +/- 0.2 dB. As a result, there is a certain percentage of error in the extracted noise parameters as well.

At low frequencies, the reflection coefficient being close to 1, good impedance matching could not be achieved. Another source of error in the data is that the de-embedding of pads is currently incomplete, so the data shown is almost identical to that measured from the NP5 system.

All simulations were done in Spectre Direct using the S-parameter analysis procedure. For the purposes of this comparison, the Ic and Vce was set to the measurement values.

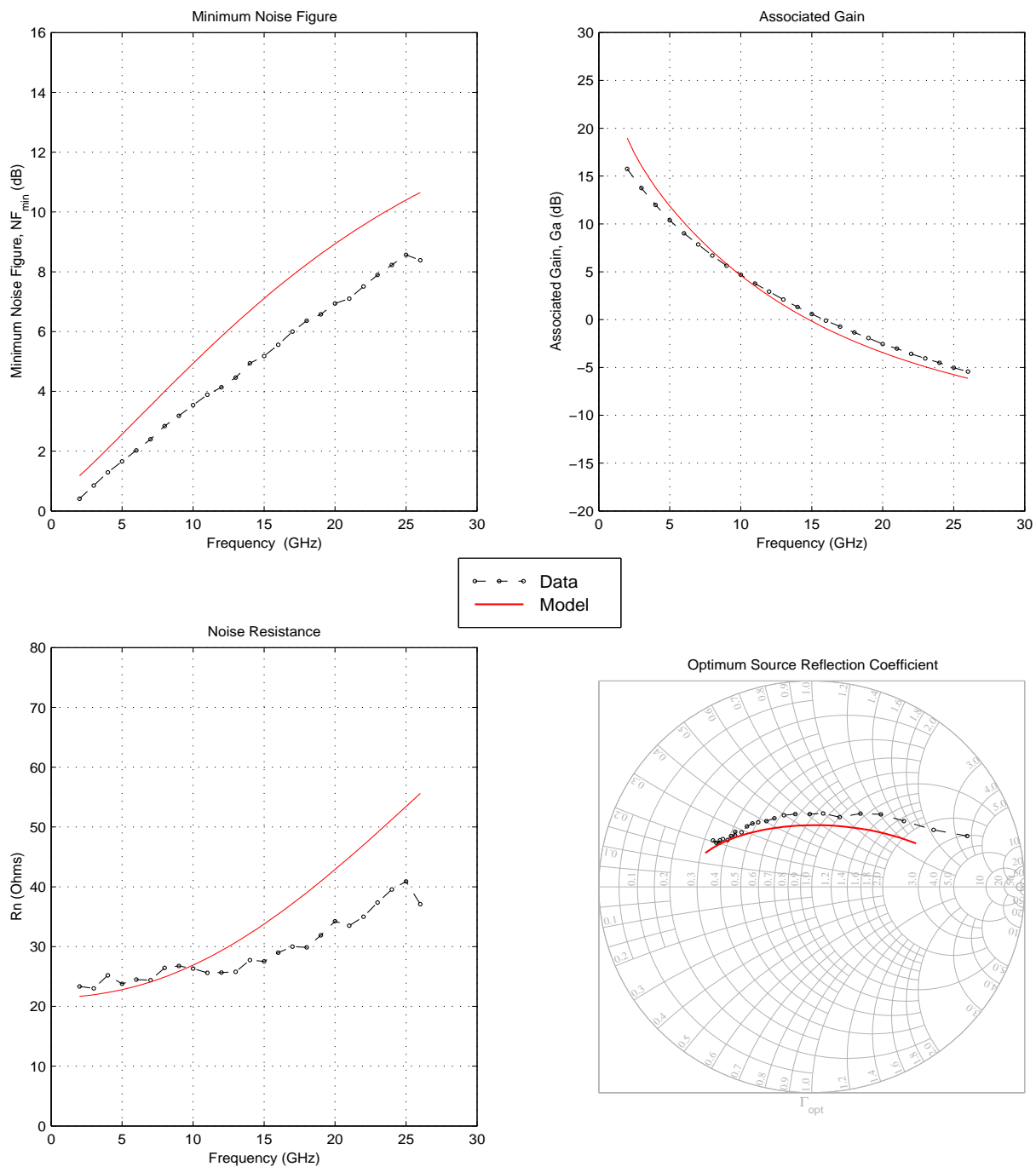
BiCMOS8HP " VPNP" – Typical Minimum Noise Figure Characteristics (25C)
Emitter Size = $0.4\ \mu\text{m} \times 20\ \mu\text{m} \times 1$, $I_c = 1.06\text{mA}$, $V_{cb} = -3.0\text{V}$



Wafer Parametrics: $vpisa = 614.8n$, $vpisp = 39.4f$, $vpibe1 = 1.9n$, $vpvef = 20.0$, $vpavc2 = 46.0$, $vpftf = 5.54p$

Figure 124. VPNP Minimum Noise Figure, $0.4\ \mu\text{m} \times 20\ \mu\text{m} \times 1$, $V_{be}=0.865V$

BiCMOS8HP "VNP" – Typical Minimum Noise Figure Characteristics (25C)
 Emitter Size = $0.4\ \mu\text{m} \times 20\ \mu\text{m} \times 2$, $I_c = 2.74\text{mA}$, $V_{cb} = -3.0\text{V}$



Wafer Parametrics: $vpisa = 614.8n$, $vpisp = 39.4f$, $vpibe = 1.9n$, $vpvfe = 20.0$, $vpavc2 = 46.0$, $vptf = 5.54p$

Figure 125. VNP Minimum Noise Figure, $0.4\ \mu\text{m} \times 20\ \mu\text{m} \times 2$, $V_{be}=0.870V$

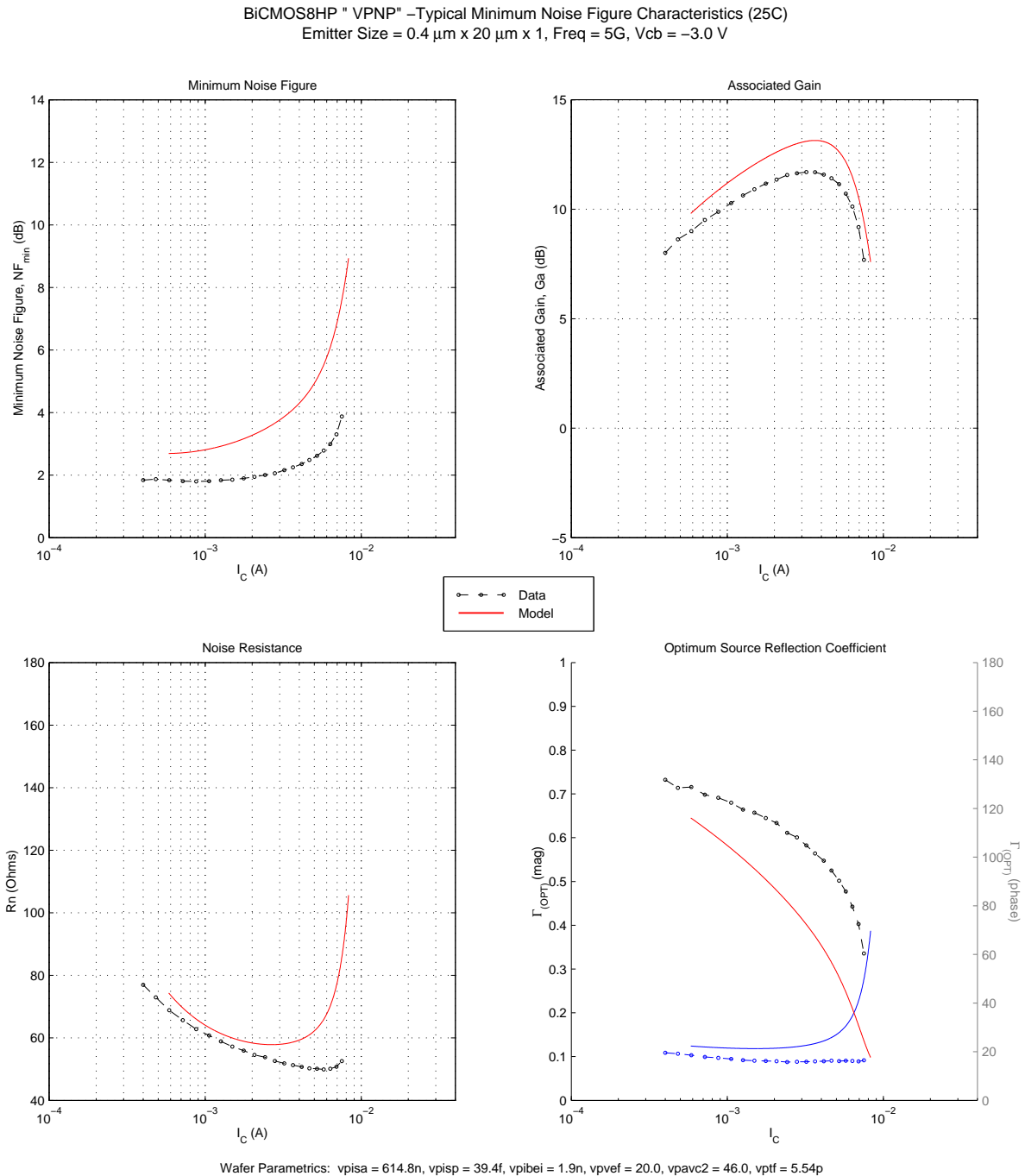


Figure 126. VPNP Minimum Noise Figure, 0.4 μm x 20 μm x 1, I_C sweep @ 5 GHz

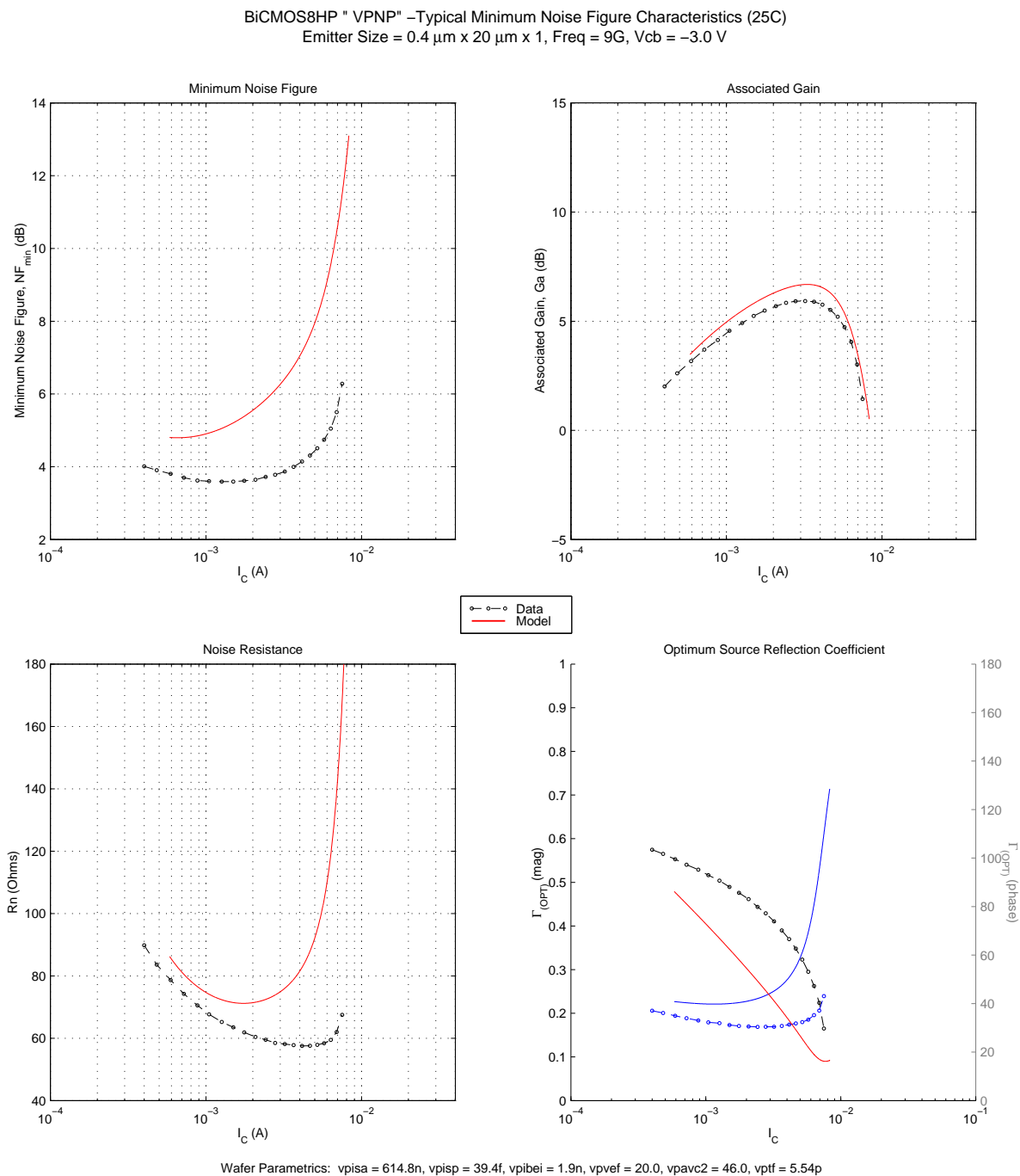
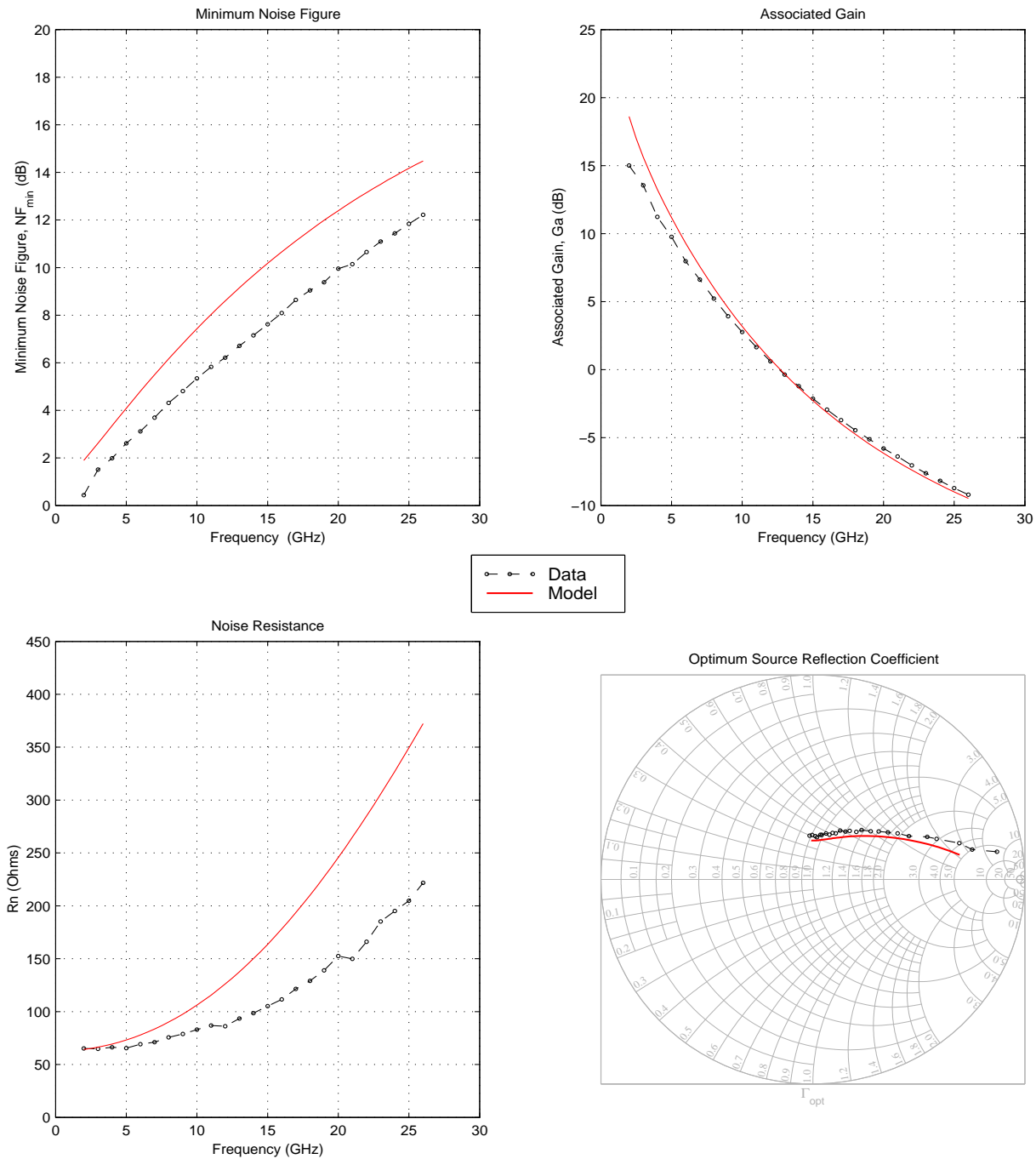


Figure 127. VPNP Minimum Noise Figure, $0.4\ \mu\text{m} \times 20\ \mu\text{m} \times 1$, I_C sweep @ 9 GHz

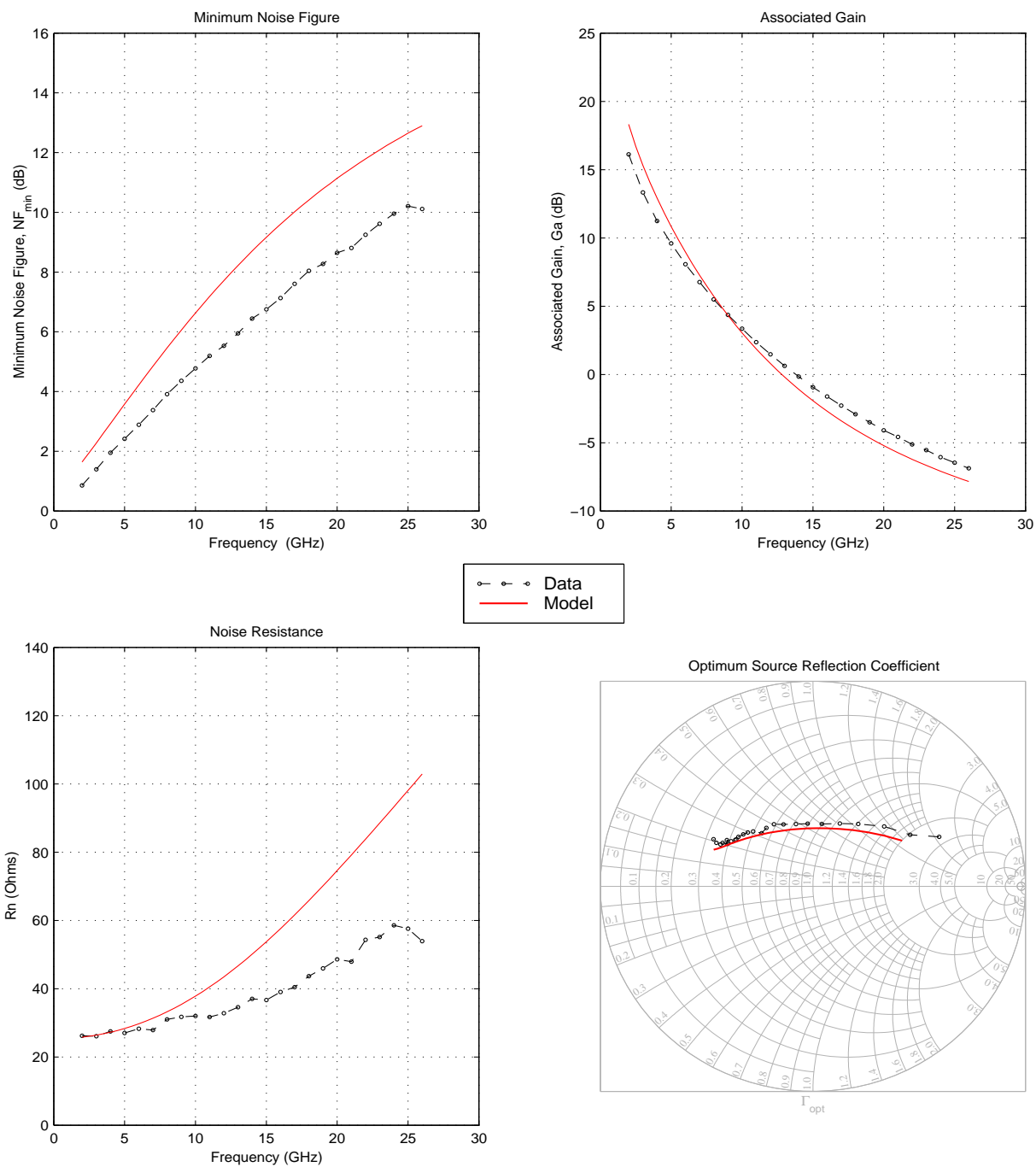
BiCMOS8HP "VPNP" – Typical Minimum Noise Figure Characteristics (25C)
Emitter Size = $0.8\ \mu\text{m} \times 20\ \mu\text{m} \times 1$, $I_c = 2.11\text{mA}$, $V_{cb} = -3.0\text{V}$



Wafer Parametrics: $vpisa = 614.8\text{n}$, $vpisp = 39.4\text{f}$, $vpibei = 1.9\text{n}$, $vpvfe = 20.0$, $vpavc2 = 46.0$, $vptf = 5.54\text{p}$

Figure 128. VPNP Minimum Noise Figure, $0.8\ \mu\text{m} \times 20\ \mu\text{m} \times 1$, $V_{be}=0.865\text{V}$

BiCMOS8HP "VPNP" – Typical Minimum Noise Figure Characteristics (25C)
 Emitter Size = $0.8\ \mu\text{m} \times 20\ \mu\text{m} \times 2$, $I_c = 3.74\text{mA}$, $V_{cb} = -3.0\text{V}$



Wafer Parametrics: $vpisa = 614.8n$, $vpisp = 39.4f$, $vpibei = 1.9n$, $vpvef = 20.0$, $vpavc2 = 46.0$, $vptf = 5.54p$

Figure 129. VPNP Minimum Noise Figure, $0.8\ \mu\text{m} \times 20\ \mu\text{m} \times 2$, $V_{be}=0.860V$

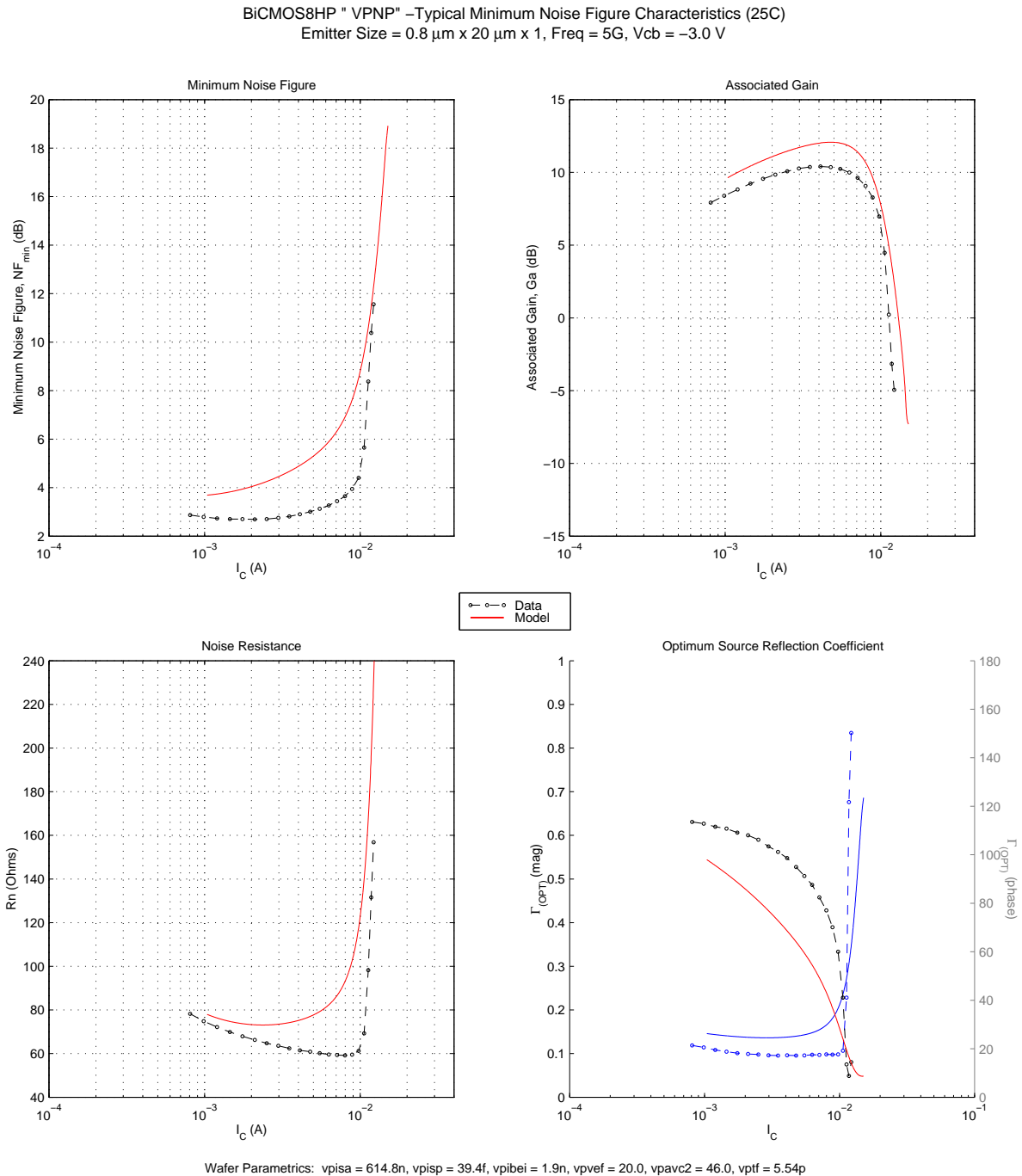


Figure 130. VPNP Minimum Noise Figure, $0.8\ \mu\text{m} \times 20\ \mu\text{m} \times 1$, I_C sweep @ 5 GHz

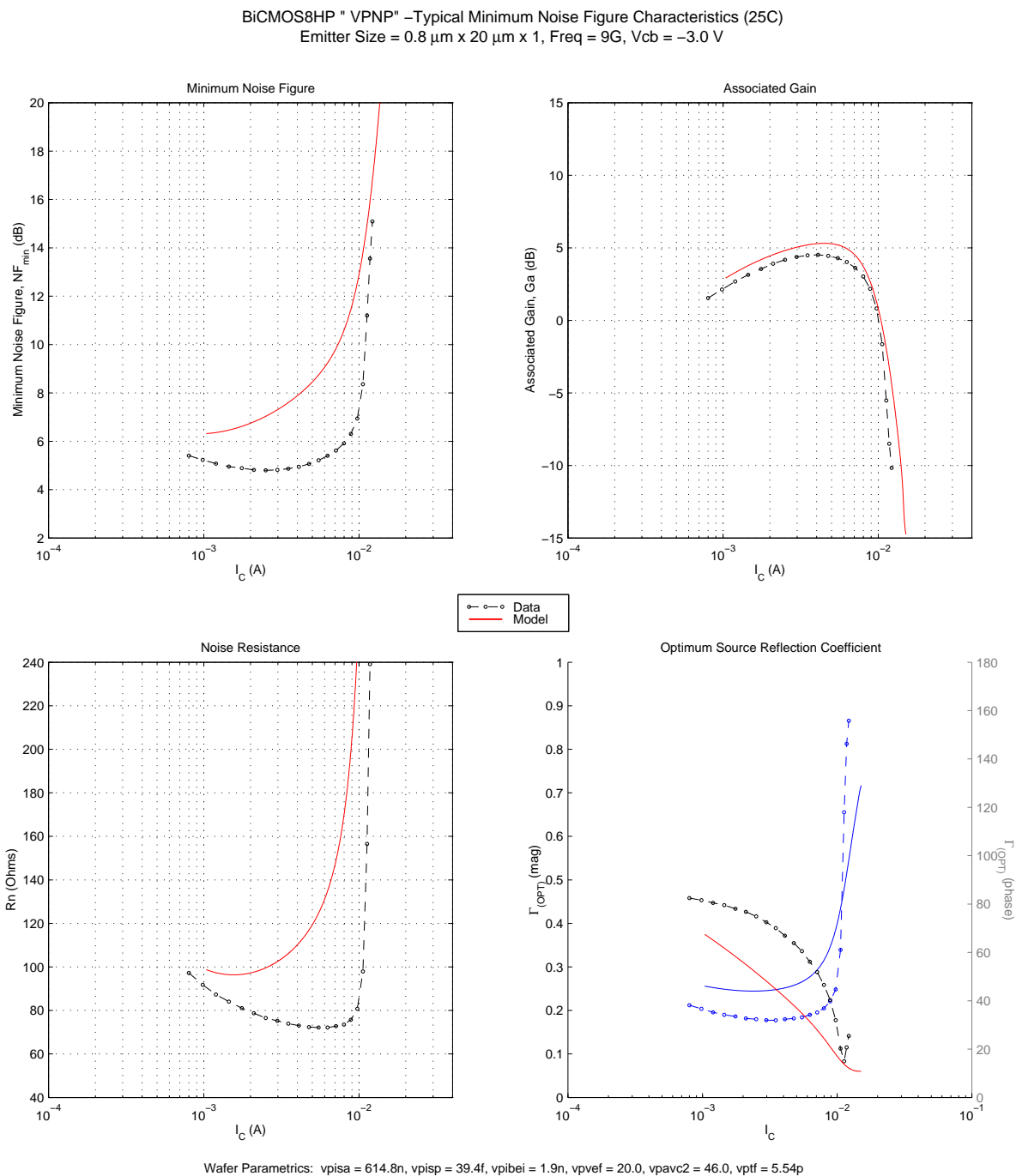


Figure 131. VPNP Minimum Noise Figure, $0.8\ \mu\text{m} \times 20\ \mu\text{m} \times 1$, I_C sweep @ 9 GHz

5.0 MOSFET Models

5.1 Model Features

The MOSFET subcircuits use the PSP intrinsic model and include the following features:

- Intrinsic gate resistance that consists of both the NQS (Non-Quasi Static) channel resistance and the distributed resistance of gates contacted from one or both ends using the instance parameter "ngcon"
- A user-defined substrate resistance multiplier (RF_RSUB = 1) based on layout (default = 50 ohms) that is used as part of the intrinsic substrate resistance network
- Use of the PSP thermal and 1/f noise equations
- Modeling of impact ionization
- Overlap and intrinsic capacitance model based on CAPMOD = 2
- Junction diode model (DIOMOD = 1)
- All devices with RF PCELLs and models use extrinsic source/drain resistance model (RDSMOD = 1) to improve the high-frequency S-Parameter and noise performance
- Device mis-match as a function of threshold voltage and mobility mis-match
- Well proximity effect based on PANW1, PANW2, ... , PANW10 instance parameters
- Shallow Trench Isolation (STI) stress effect based on SA, SB and SD instance parameters

5.1.1 Source and Drain Parasitics

All of the models have been implemented in a subcircuit format in order to incorporate device mis-match and other effects. The default values for the Source/Drain (S/D) diffusion geometry parameters AD, PD, AS, PS, NRS and NRD are zero. With these default values, S/D area and STI bounded perimeter capacitances will not be added to the circuit during simulation. The gate bounded perimeter component of capacitance is always present, regardless of the value of the geometry parameters. If the models are called from the Cadence environment, these geometry parameters will be passed as estimated or extracted values for the layout in the Cadence library.

The intrinsic models account for devices with multiple fingers using the instance parameter "NF". When NF > 1, the internal model calculations assume any specified width (W) and source drain geometry parameters (AD, PD, NRD, AS, PS, and NRS) represent the total device values, not per finger values.

Below is an example of the netlist call for a 15 finger thin oxide NFET with each finger 2μm wide and a channel length of 0.12μm:

```
xnf vout vg vsn sub nfet l=0.12u w=30u nf=15 as=6.14p ad=6.14p ps=38.14u
+pd=38.14u nrs=0.006 nrd=0.006
```

5.1.2 Well Proximity Effect

The MOSFET models include a method for adjusting the threshold voltage of the device based on the distance to a well edge. In order to utilize this effect, information about the circuit layout needs to be passed to the model. The instance parameters (panw1, panw2, ... , panw10) give the model information about how close a device is to the well edge. An example of a netlist call with these parameters is shown below:

```
T0 (d g s sub) nfet l=120.0n w=10u nf=1 m=1 par=1 ad=5.251e-12 as=5.251e-12
+pd=20.965u ps=20.965u panw1=0 panw2=0 panw3=0 panw4=0 panw5=0 panw6=2.4e-15
+panw7=2.4e-14 panw8=2.4e-14 panw9=4.8e-14 panw10=7.2e-14 dtemp=0
```

If no parameters are passed to the model, or all values are zero (the default values), then there is no adjustment to the threshold voltage.

The instance parameters are best generated from a layout extraction tool, but can be hand calculated for very small circuits. The definition of the instance parameters are as follows: PANW1 is the active area of the device within 0 - 0.30 μm of the nwell edge, PANW2 is the active area of the device within 0.30 - 0.35 μm of the nwell edge, and so on as shown in **Figure 132**. This is done for devices which are perpendicular to the nwell as shown and also parallel. If more than one nwell edge is near a device, the areas are additive.

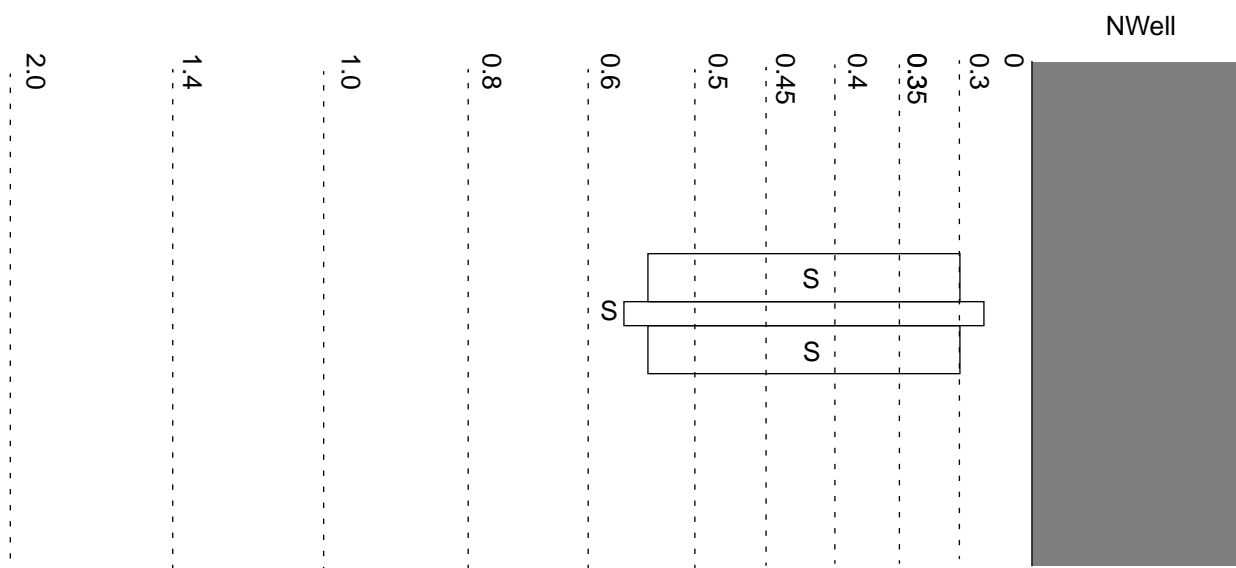


Figure 132. Extraction of active device areas near nwell edge.

Please refer to **Section 2.1** , “**Process Model User Controls**” on **page 13** for information on the global (gwells) and instance (lnws) switch parameters that are available to turn on/off this well proximity effect.

Figure 133 shows the magnitude of the NW proximity effect on the thin oxide NFET and PFET devices as a minimum width device is brought closer to an NW edge as shown in **Figure 132**. The models are set so that the effect is a 20-30 mV shift in the threshold voltage at the worst case (minimum width and as close to the nwell as allowed) for the thin oxide devices, and a 40-60 mV shift for the thick oxide devices.

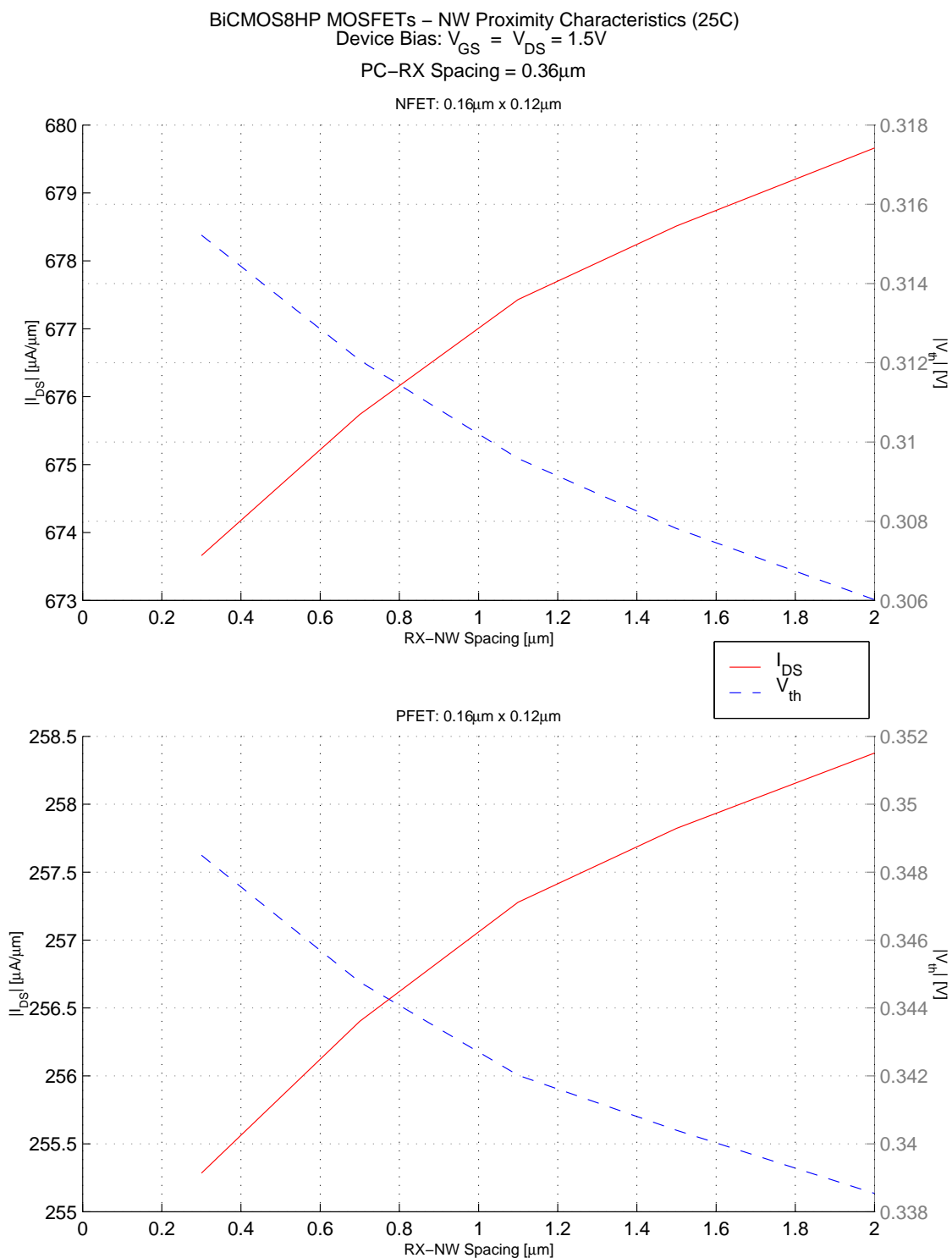


Figure 133. NW Proximity Effect for thin oxide devices

5.1.3 Isolation Proximity Effect

It is well known that mechanical stress affects the carrier mobilities in silicon. For electrons, both transverse and longitudinal compressive strain reduces the mobility. For holes, the situation is more complex as the compressive strain in one direction increases the mobility and compressive strain in the other direction decreases the mobility. There is a compressive strain field associated with the oxide isolation boundary. The effect of the STI edges is to introduce a compressive strain in the silicon nearby. The net effect on transistor characteristics is that, in absolute terms, NFET currents decrease and threshold voltages increase while PFET currents increase and threshold voltages decrease as the STI edge is brought closer to the transistor channel.

The isolation proximity effect, or STI stress effect, is now modeled by built-in equations, which consider the influence of mechanical stress on mobility, velocity saturation, threshold voltage, body effect and DIBL. Additional instance parameters SA, SB and SD need to be specified (units of meters) in the netlist in order to observe the affect of STI stress. The default values, SA = SB = SD = 0, mean there is no stress effect on the device.

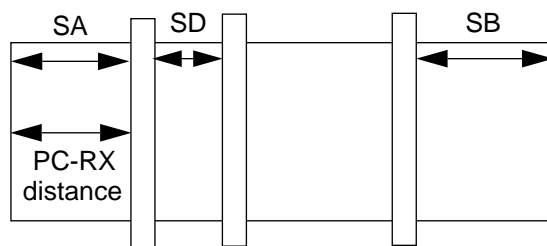


Figure 134. FET distance between RX and PC (STI and Channel) impacts mechanical stress

The following table illustrates the predicted change in drain current and threshold voltage as the PC-RX distance is varied from 3.0 μ m to 0.36 μ m for all devices where the STI stress effect has been modeled. These results are for single finger devices with symmetric layout (equal PC-RX distances to the left and right of the gate finger).

Table 49. Isolation Proximity Effect Example

Device (Geometry)	Bias	Model ΔI_{dsat}	Model ΔV_{tsat}
NFET (5 μ m x 0.12 μ m x 1)	$V_{GS} = V_{DS} = 1.2V$	- 11.5 %	+ 16 mV
PFET (5 μ m x 0.12 μ m x 1)	$V_{GS} = V_{DS} = 1.2V$	+ 12.6 %	- 11 mV
DGNFET (5 μ m x 0.24 μ m x 1)	$V_{GS} = V_{DS} = 2.5V$	- 5.8 %	+ 24 mV
DGPFET (5 μ m x 0.24 μ m x 1)	$V_{GS} = V_{DS} = 2.5V$	+ 7.8 %	- 6 mV

In addition, Figures 135-136 show the change in current and threshold voltage for each device type.

Note: The data points for the shift in V_{tsat} (mV) of the P-type devices in these figures do not follow the expected trend, i.e. opposite direction of the I_{dsat} change. The predicted model change is based on fitting of the I_{dsat} shift and maintaining the proper physical trend.

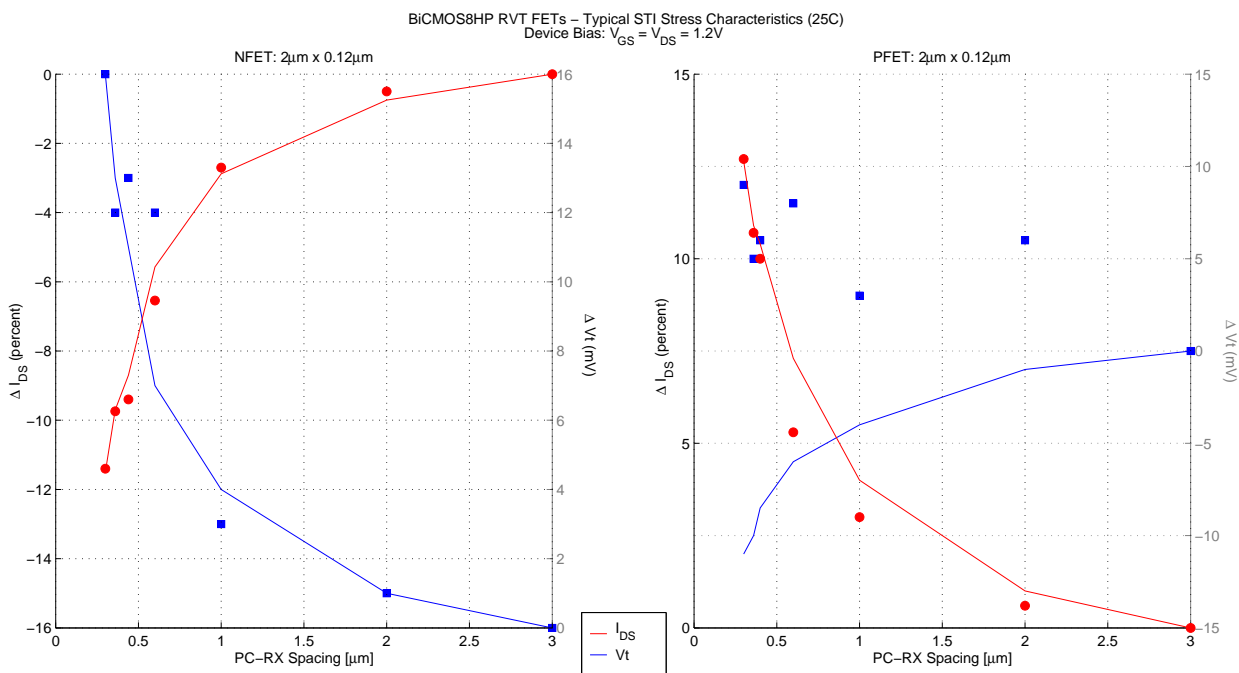


Figure 135. STI Stress Effect for thin oxide devices

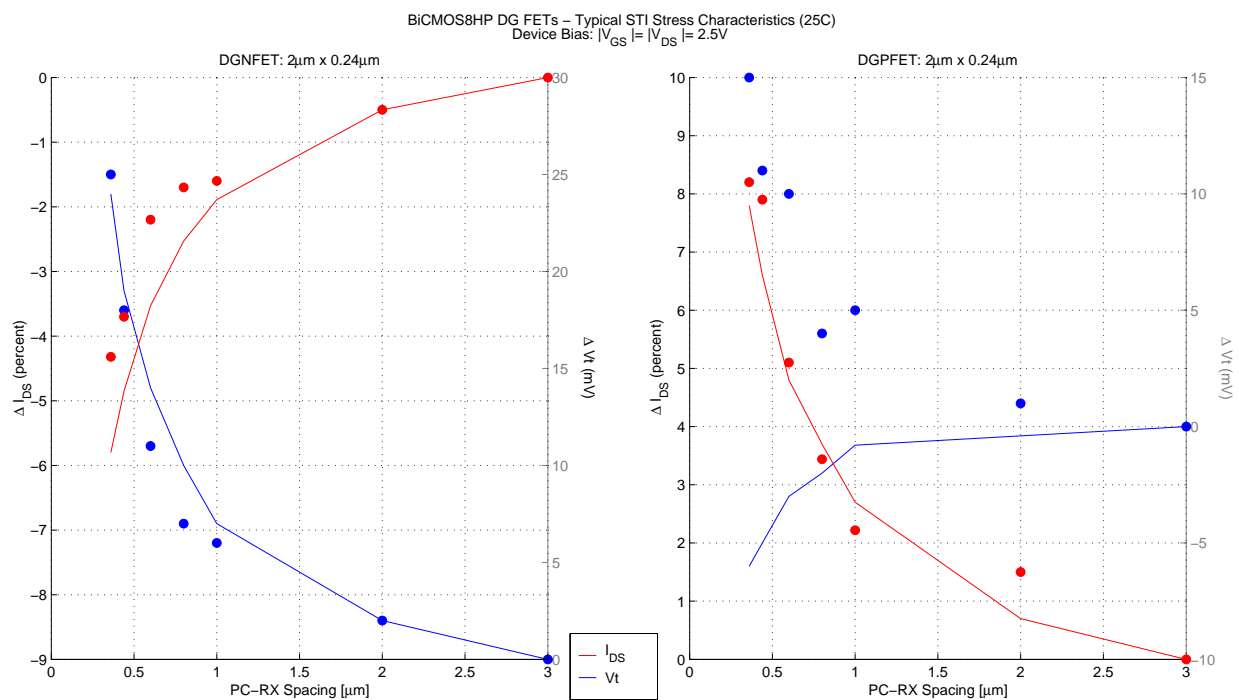


Figure 136. STI Stress Effect for thick oxide devices

5.1.4 RFFET PCELL Layout

In addition to the standard layouts, the device library contains RFFET PCELL layouts for all device types. Separate RF FET model files have been created to capture the scalable gate and substrate resistance calculations as well as parasitic wiring capacitance equations. The RF model automatically calculates values for each of these elements based on channel width, length and number of fingers. The RFFET PCELL layouts are wired to the M2 metal level, and include a substrate contact ring.

When using RFFET PCELLs, the model takes into account the parasitic effects due to wiring within the PCELL boundary. Additional wiring resistance and capacitance elements are added appropriately to each device and are only active for RF layouts. Since these wiring parasitics are included in the model for the RF layouts, the extraction program does not extract parasitic elements from within RFFET PCELLs. This is done to avoid double counting of parasitic elements. However, when the regular (non-RF) FET PCELLs are used, the extraction program will account for all wiring parasitics.

There are two additional instance parameters (rf_rsub and cwire), with default values of one, that allow designers to gauge the sensitivity of their circuits to the substrate resistance and capacitive wiring parasitics. The substrate resistance multiplier (rf_rsub) is applied to all five substrate resistance elements, while the parasitic capacitance multiplier (cwire) is applied to all three parasitic capacitance elements. The substrate resistance multiplier should be kept greater than zero.

5.1.5 Spectre Voltage Warning Checks

The SPECTRE MOSFET models also include a series of "assert" statements which have been set up to monitor the following voltage limits:

- Vgs, Vgd, Vds = 1.6V (1.2V devices) or 2.7V (2.5V devices)
- Vgb, Vbd, Vbs (rev bias) = Vgs limit + 1V (1.2V devices) or Vgs limit + 2V (2.5V devices)
- Vbd, Vbs (fwd bias) = 0V (default) to flag an inadvertent forward-bias condition for S/D to body junctions

Note: Since the 1.2V devices have an option for 1.5V use, the checking values were set to represent the higher voltage limit (including a 10% power supply tolerance assumption).

The following is an example of some of the warning messages that will be written to the log file during simulation if any of these parameter limits are exceeded:

```
Warning from spectre at dc = 0 V during DC analysis 'xxx'.
WARNING (SPECTRE-4017): X1.vgs_check: Vgs exceeds limit. Instance X1,
Parameter 'vgs' having value 2V has exceeded its upper bound '1.6'.

Warning from spectre at dc = -3.0 V during DC analysis 'xxx'.
WARNING (SPECTRE-4049): X2.vgb_check, instance X2: Vgb exceeds limit.
Expression 'vgs-vbs' exceeds its lower bound '-2.7'. Peak value was -3V at dc
0V. Total duration of overshoot was -300e-03 V.

Warning from spectre at dc = 0 V during DC analysis 'xxx'.
WARNING (SPECTRE-4052): X3.vbd_chkfwd, instance X3, Vbd drain-body diode
is being forward-biased. Expression 'vbs-vds' having value -0.5V has exceeded
its lower bound '0'.
```

The simulation results are not affected by these warnings, but designers should review the bias conditions of all devices that are identified as violating any of these voltage limits. Please refer to **Section 2.1**, “**Process Model User Controls**” on **page 13** for information on the global switch parameter (gbv) that is available to enable or disable these checks and the "fwdlim" parameter which allows the user to specify the voltage limit for the S/D forward-bias junction check (default=0V).

5.2 Model Limitations and Restrictions

- In general, the noise model has been verified across a limited device geometry, voltage bias, and temperature sample. Please see “**Thermal Noise Model Correlation**” on **page 198**. for the available correlation plots.

5.3 Model Notes

Device Model Outputs

The simulators provide some secondary outputs that may be helpful to the designer, including effective device dimensions, capacitances and threshold voltage. It is important to interpret these values carefully when trying to compare them to information that is found in the technology design manual.

One key parameter that can be ambiguous is the device threshold voltage. There are a variety of algorithms available to measure threshold voltage and each method will result in a different V_{th} value. The model output as reported by the simulator may not match the value from a given characterization algorithm.

Note that the model parameter value (v_{th0}) is adjusted to match the design manual definition and is valid only for a wide and long channel FET at nominal process. This is done to facilitate the generation of parameter overrides from wafer test data.

Known Warning Messages

The DG PFET models will generate a warning similar to the following:

```
Warning from spectre during initial setup.
WARNING: X1.dgpch: Model parameter psti=1.00e-03 should not be less than
5.00e-02.
```

The warning is related to this PSP parameter value being outside the "suggested" range and can be ignored as it will not cause any problems or inaccuracies in the simulation results.

5.4 Design Manual Specifications

The following tables are a comparison of the nominal model simulation versus the expected device specification targets as defined in the BiCMOS8HP technology design manual.

Table 50. NFET Design Manual Correlation

Parameter	Condition	Units	Geometry W_{des}/L_{des}	Model	Design Manual
Vtlin	Vd = 0.05V, Vb = 0	V	5/5	0.170	0.170
Vtsat	Vd = 1.2V, Vb = 0V	V	5/0.12	0.356	0.355
Vtsat	Vd = 1.5V, Vb = 0V	V	5/0.12	0.344	0.340
Vtsat	Vd = 1.2V, Vb = 0V	V	0.16/0.12	0.295	0.295
DIBL	Vtsat - Vtlin, Vb = 0V	V	5/0.12	0.072	0.073
Body Effect	Vd = 1.2V, Vb = 0 - 1V	V	5/0.12	0.122	0.165
Sub-Vt slope	Vd = 1.2V, Vb = 0V	mV/dec	5/0.12	87	82
Idlin	Vd = 0.05V, Vg = 1.2V, Vb = 0V	$\mu\text{A}/\mu\text{m}$	5/5	4.02	4.00
Ion	Vd = Vg = 1.2V, Vb = 0V	$\mu\text{A}/\mu\text{m}$	5/0.12	531	530
Ion	Vd = Vg = 1.5V, Vb = 0V	$\mu\text{A}/\mu\text{m}$	5/0.12	762	770
Ion	Vd = Vg = 1.2V, Vb = 0V	μA	0.16/0.12	87	86
Gm	Vd = Vg = 1.2V, Vb = 0V	$\mu\text{S}/\mu\text{m}$	5/0.12	747	750
Ioff	Vd = 1.2V, Vg = Vb = 0V	pA/ μm	5/0.12	307	300
Ioff	Vd = 1.5V, Vg = Vb = 0V	pA/ μm	5/0.12	411	450
Ioff	Vd = 1.2V, Vg = Vb = 0V	pA	0.16/0.12	225	400
Igate	Vg = 1.2V, Vd = Vb = 0V	pA/ μm^2	5/5 (x42)	20	20
Cj_area	Vj = 0V	fF/ μm^2		1.05	1.05
Cov	Vg = 0V, Vd = Vb = 0V	fF/ μm		0.350	0.350
Cgon	Vg = 1.2V, Vd = Vb = 0V	fF/ μm		1.31	1.30

Table 51. PFET Design Manual Correlation

Parameter	Condition	Units	Geometry W_{des}/L_{des}	Model	Design Manual
Vtlin	Vd = 0.05V, Vb = 0	V	5/5	-0.226	-0.225
Vtsat	Vd = 1.2V, Vb = 0V	V	5/0.12	-0.325	-0.325
Vtsat	Vd = 1.5V, Vb = 0V	V	5/0.12	-0.311	-0.310
Vtsat	Vd = 1.2V, Vb = 0V	V	0.16/0.12	-0.356	-0.355
DIBL	Vtsat - Vtlin, Vb = 0V	V	5/0.12	0.075	0.076
Body Effect	Vd = 1.2V, Vb = 0 - 1V	V	5/0.12	0.185	0.192
Sub-Vt slope	Vd = 1.2V, Vb = 0V	mV/dec	5/0.12	91	83
Idlin	Vd = 0.05V, Vg = 1.2V, Vb = 0V	$\mu A/\mu m$	5/5	0.69	0.68
Ion	Vd = Vg = 1.2V, Vb = 0V	$\mu A/\mu m$	5/0.12	190	190
Ion	Vd = Vg = 1.5V, Vb = 0V	$\mu A/\mu m$	5/0.12	312	315
Ion	Vd = Vg = 1.2V, Vb = 0V	μA	0.16/0.12	23	23
Gm	Vd = Vg = 1.2V, Vb = 0V	$\mu S/\mu m$	5/0.12	349	340
Ioff	Vd = 1.2V, Vg = Vb = 0V	pA/ μm	5/0.12	214	250
Ioff	Vd = 1.5V, Vg = Vb = 0V	pA/ μm	5/0.12	297	370
Ioff	Vd = 1.2V, Vg = Vb = 0V	pA	0.16/0.12	14	30
Igate	Vg = 1.2V, Vd = Vb = 0V	pA/ μm^2	5/5 (x42)	1	1
Cj_area	Vj = 0V	fF/ μm^2		1.05	1.05
Cov	Vg = 0V, Vd = Vb = 0V	fF/ μm		0.29	0.29
Cgon	Vg = 1.2V, Vd = Vb = 0V	fF/ μm		1.26	1.26

Table 52. DGNFET Design Manual Correlation

Parameter	Condition	Units	Geometry W_{des}/L_{des}	Model	Design Manual
Vtlin	$V_d = 0.05V, V_b = 0$	V	5/5	0.465	0.465
Vtsat	$V_d = 2.5V, V_b = 0V$	V	5/0.24	0.410	0.410
Body Effect	$V_d = 2.5V, V_b = 0 - 1V$	V	5/0.24	0.130	0.110
Sub-Vt Slope	$V_d = 2.5V, V_b = 0V$	mV/dec	5/0.24	80	80
I _{dsat}	$V_d = 2.5V, V_b = 0V$	$\mu A/\mu m$	5/0.24	660	660
I _{off}	$V_d = V_g = 2.5V, V_b = 0V$	$pA/\mu m$	5/0.24	10	10
C _{j_area}	$V_j = 0V$	$fF/\mu m^2$		1.0	1.0
Cov	$V_g = 0V, V_d = V_b = 0V$	$fF/\mu m$		0.315	0.315

Table 53. DGPFET Design Manual Correlation

Parameter	Condition	Units	Geometry W_{des}/L_{des}	Model	Design Manual
Vtlin	$V_d = 0.05V, V_b = 0$	V	5/5	-0.459	-0.445
Vtsat	$V_d = 2.5V, V_b = 0V$	V	5/0.24	-0.443	-0.440
Body Effect	$V_d = 2.5V, V_b = 0 - 1V$	V	5/0.24	0.35	0.250
Sub-Vt Slope	$V_d = 2.5V, V_b = 0V$	mV/dec	5/0.24	97	85
I _{dsat}	$V_d = 2.5V, V_b = 0V$	$\mu A/\mu m$	5/0.24	262	260
I _{off}	$V_d = V_g = 2.5V, V_b = 0V$	$pA/\mu m$	5/0.24	11	10
C _{j_area}	$V_j = 0V$	$fF/\mu m^2$		1.0	1.0
Cov	$V_g = 0V, V_d = V_b = 0V$	$fF/\mu m$		0.30	0.30

5.5 Conductance Model Extraction and Correlation

The conductance portion of the models has been optimized over the following ranges/conditions:

<i>Table 54. FET DC Extraction Range</i>				
Parameter	NFET	PFET	DGNFET	DGPFET
Channel Length	0.12 - 5 μm	0.12 - 5 μm	0.24 - 5 μm	0.24 - 5 μm
Channel Width	0.16 - 5 μm	0.16 - 5 μm	0.36 - 5 μm	0.36 - 5 μm
Drain and Gate Voltage Bias	0 to 1.6V	0 to -1.6V	0 to 2.7V	0 to -2.7V
Back Bias	0 to -1.2V	0 to 1.2V	0 to -1.8V	0 to 1.8V
Temperature	-40, 25, 125C			

The DC Model-to-Hardware plots compare simulation results against technology qualification hardware used for model parameter extraction. All simulations assume the test chip measurement values for model and/or process parameters, such as VTH0, U0, etc. as noted on each plot.

The initial group of plots represent nominal temperature (25C) DC characteristics:

<i>Table 55. FET DC Correlation Plots (25C)</i>				
Plot Type	NFET	PFET	DGNFET	DGPFET
DC Characteristics, 5 μm x L _{min}	Fig 137	Fig 142	Fig 147	Fig 152
DC Characteristics, W _{min} x L _{min}	Fig 138	Fig 143	Fig 148	Fig 153
DC Characteristics, 5 μm x 5 μm	Fig 139	Fig 144	Fig 149	Fig 154
DC Characteristics, 5 μm x 4*L _{min}	Fig 140	Fig 145	Fig 150	Fig 155
Isub/Igidl vs Vgs, step Vds, Vbs = 0V	Fig 141	Fig 146	Fig 151	Fig 151
Igate vs Vgs, step Vds, Vbs = 0V	Fig 141	Fig 146	negligible	negligible

The next group of plots represent DC characteristics at different temperatures:

<i>Table 56. FET DC Correlation Plots vs. Temperature</i>					
Plot Type	Temp	NFET	PFET	DGNFET	DGPFET
DC Characteristics, 5 μm x L _{min}	125C	Fig 156	Fig 158	n/a	n/a
DC Characteristics, 5 μm x L _{min}	-40C	Fig 157	Fig 159	n/a	n/a
DC Characteristics, 5 μm x 4*L _{min}	125C	n/a	n/a	Fig 160	Fig 162
DC Characteristics, 5 μm x 4*L _{min}	-40C	n/a	n/a	Fig 161	Fig 163

5.6 Capacitance Model Extraction and Correlation

The Gate-Drain and Gate-Source overlap capacitances are not constant. As the devices are biased heavily into accumulation, the diffused junction region below the gate depletes laterally, reducing the overlap region and, thus, the overlap capacitance decreases. This decrease in overlap capacitance has been modeled at nominal temperature (25C) for Vgd (Vgs) values from 0V to -Vdd.

The reverse bias capacitance and forward bias current of the MOSFET parasitic PN junctions have been optimized over the ranges/conditions defined in the following table.

<i>Table 57. FET Parasitic PN Junction Extraction Range</i>				
Parameter	1.5V N+ to Substrate	1.5V P+ to NWell	2.5V N+ to Substrate	2.5V P+ to NWell
Voltage bias (Capacitance)	0V to 1.5V	0V to -1.5V	0V to 2.75V	0V to -2.75V
Temperature	25C	25C	25C	25C

The capacitance Model-to-Hardware plots for Cgg, Cj, Cjswg and Cov compare simulation results against technology qualification hardware for multi-finger FETs. All simulations represent nominal temperature (25C) characteristics and assume the test chip measurement values for model and/or process parameters, such as TOX and Cj(0V), as noted on each plot.

<i>Table 58. FET C-V Correlation Plots (25C)</i>				
Plot Type	NFET	PFET	DGNFET	DGPFET
Junction, Overlap and Total Gate Cap	Fig 164	Fig 165	Fig 166	Fig 167

5.7 Mis-match Extraction and Model Correlation

Device mis-match has been implemented using a geometry dependent local variation on threshold voltage and mobility. The mis-match parameters were fit using ΔI_{ds} data from a set of common source current mirrors. The dimensions and bias conditions used for the model extraction are outlined below:

Table 59. FET Mis-match Extraction Range				
Parameter	NFET	PFET	DGNFET	DGPFET
Channel Length	0.12 - 5 μm	0.12 - 5 μm	0.24 - 5 μm	0.24 - 5 μm
Channel Width	0.16 - 5 μm	0.16 - 5 μm	0.36 - 5 μm	0.36 - 5 μm
Voltage Bias	$V_{ds} = V_{dd}$, $V_{gs} = V_t$ to V_{dd} , $V_{bs} = 0V$			

Note: Since the devices in the current mirror test structures used to obtain the mis-match measurements have the same layout, orientation and are placed in close proximity, the "fet_geo_mis" switch is set to zero during the simulation for creating these model-to-hardware correlation plots. The predicted mis-match will be higher for the default switch setting of "fet_geo_mis=1" as this represents the case where the device layout is not as ideal.

The plots of I_{ds} mis-match vs gate bias as a function of both device width and length are as follows:

Table 60. FET Mis-match Correlation				
Plot	NFET	PFET	DGNFET	DGPFET
ΔI_{ds} vs V_{gs}	Fig 168	Fig 168	Fig 169	Fig 169

5.8 Flicker Noise Model Correlation

The thermal noise and 1/f (flicker) noise have been modeled using the PSP set of noise equations. These equations incorporate the Q_{inv} term from the charge model into the thermal noise model, and a V_{ds} and V_{gs} bias dependence into the 1/f noise model. The noise parameters have been fit at 25C using a limited sample of device geometry and bias data.

Note: The nominal model predictions for noise should be regarded as typical, not worst case

The following table provides a summary of the flicker noise correlation plots.

Table 61. Nominal MOSFET Flicker Noise Correlation Plots				
Device Type	Device Sizes (W x L)	Bias Conditions (V _{bs} = 0V at 25C)		Figure
		V _{gs} range (V)	V _{ds} (V)	
NFET	80 μm x 0.12 μm	0.4 to 1.2	1.2	Fig 170
NFET	160 μm x 0.24 μm	0.4 to 0.9	1.2	Fig 171
PFET	80 μm x 0.12 μm	-0.4 to -1.2	-0.7	Fig 172
PFET	160 μm x 0.24 μm	-0.4 to -1.2	-0.7	Fig 173
DGNFET	80 μm x 0.24 μm	0.5 to 2.0	2.0	Fig 174
DGNFET	80 μm x 0.72 μm	0.5 to 2.0	2.0	Fig 175
DGPFET	80 μm x 0.24 μm	-0.5 to -2.0	-2.0	Fig 176
DGPFET	80 μm x 0.72 μm	-0.5 to -2.0	-2.0	Fig 177

Process Variation

The models also include calculations to predict the process tolerance and fluctuations in trap density for flicker noise as a function of device geometry and bias. Note that the flicker noise variations are reduced with increasing device area. The statistical limits for the models are based on hardware measurements from multiple wafers/lots. The nominal and +/- 3 sigma corner model predictions are overlayed with a large data sample to illustrate the statistical model correlation with measurements, as seen in Figures 178-179.

5.9 Thermal Noise Model Correlation

In the PSP thermal noise model equations, the mean square noise current is expressed by:

$$\overline{i_d^2} = \frac{4K_B T \Delta f}{R_{ds}(V) + \frac{L_{eff}^2}{\mu_{eff} |Q_{inv}|}} \bullet NTNOI$$

In order to improve the geometric and biased scalability of the above thermal noise model, the NTNOI parameter is derived to be an empirical equation instead of a constant value.

The following table shows the available hardware correlation plots for the thin-oxide devices:

Table 62. FET Thermal Noise Correlation Plots (25C)				
Plot Type	NFET	PFET	DGNFET	DGPFET
Output Current Noise vs Freq, vs Vgs	Fig 180	Fig 181	Fig 182	Fig 183

5.10 S-Parameter Model Correlation

The high frequency fit of the MOSFET model has been achieved by using S-Parameters to fit a subcircuit that uses a PSP model as its core along with an external resistor to account for the wiring resistance between the gate connection points of the RF PCELL and the PC gate. The RF models also contain additional scaling equations for the internal gate resistance, the body resistance network and the parasitic wiring capacitances between the gate, source and drain.

The following plots compare nominal temperature (25C) S-Parameter data with simulation results:

Table 63. FET RF PCELL S-Parameter Correlation Plots (25C)					
Device Size W x L x nf	NFET	PFET	Device Size W x L x nf	DGNFET	DGPFET
2 μm x L _{min} x 8	Fig 184	Fig 190	2 μm x L _{min} x 4	Fig 196	Fig 201
2 μm x L _{min} x 20	Fig 185	Fig 191	2 μm x L _{min} x 20	Fig 197	Fig 202
5 μm x L _{min} x 32	Fig 186	Fig 192	2 μm x L _{min} x 32	Fig 198	Fig 203
10 μm x L _{min} x 32	Fig 187	Fig 193	5 μm x 0.4 μm x 32	Fig 199	Fig 204
2 μm x 2*L _{min} x 64	Fig 188	Fig 194	2 μm x 0.72 μm x 64	Fig 200	Fig 205
2 μm x 3*L _{min} x 64	Fig 189	Fig 195			

5.10.1 f_T Correlation Plots

This next group of plots represent nominal temperature (25C) f_T results for multi-finger FETs:

Table 64. FET f _T Correlation Plots (25C)		
Plot Type	NFET, PFET	DGNFET, DGPFET
f _T vs. Vgs, Vds Dependence	Fig 206	Fig 207

5.11 Model Correlation Plots

This section contains all of the model correlation plots referenced in the tables of the previous sections. Selecting the figure number (hypertext link) in any of the tables will bring up the page with the desired plot.

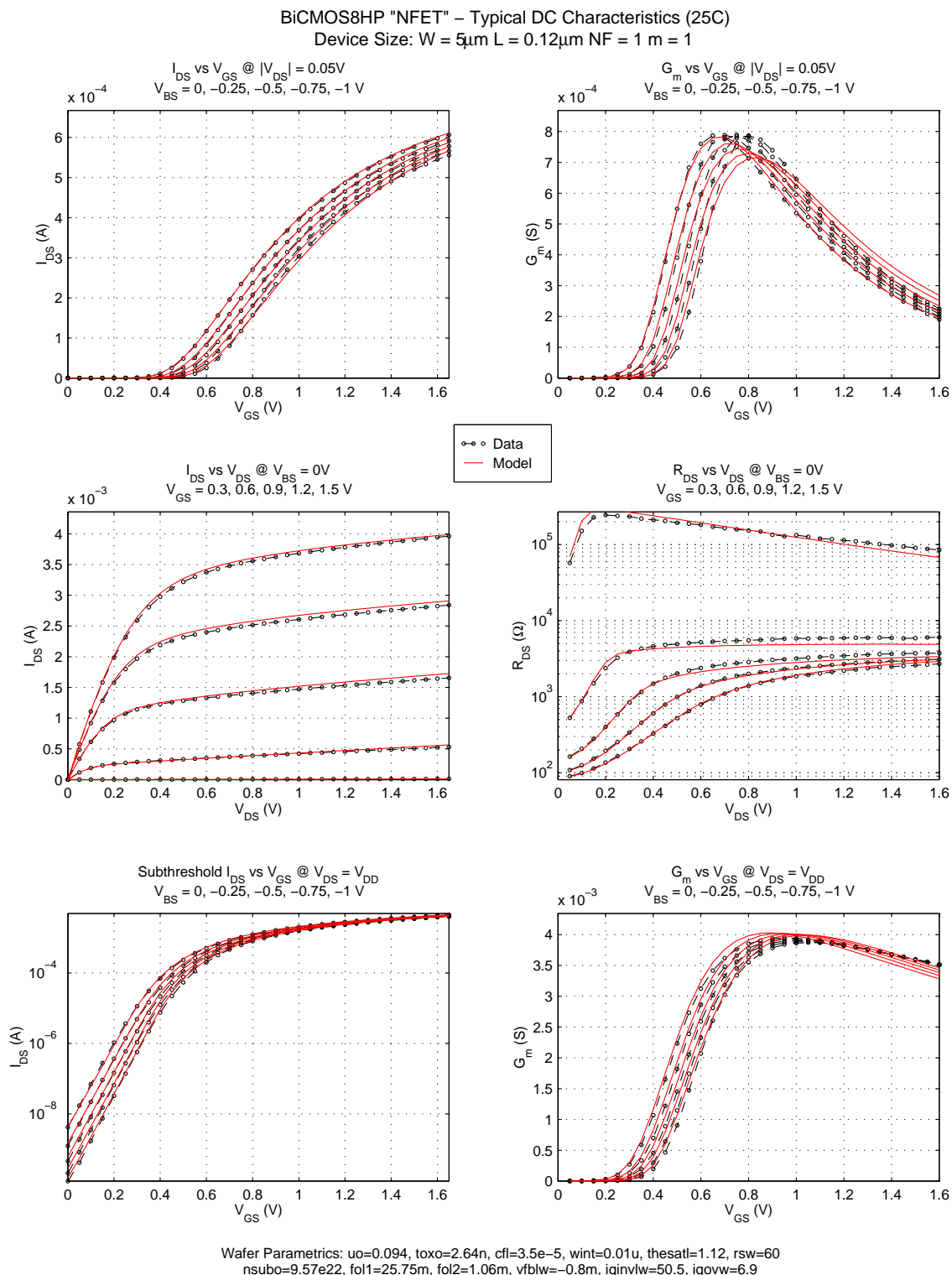


Figure 137. NFET DC Characteristics, $5\mu\text{m} \times L_{min}$

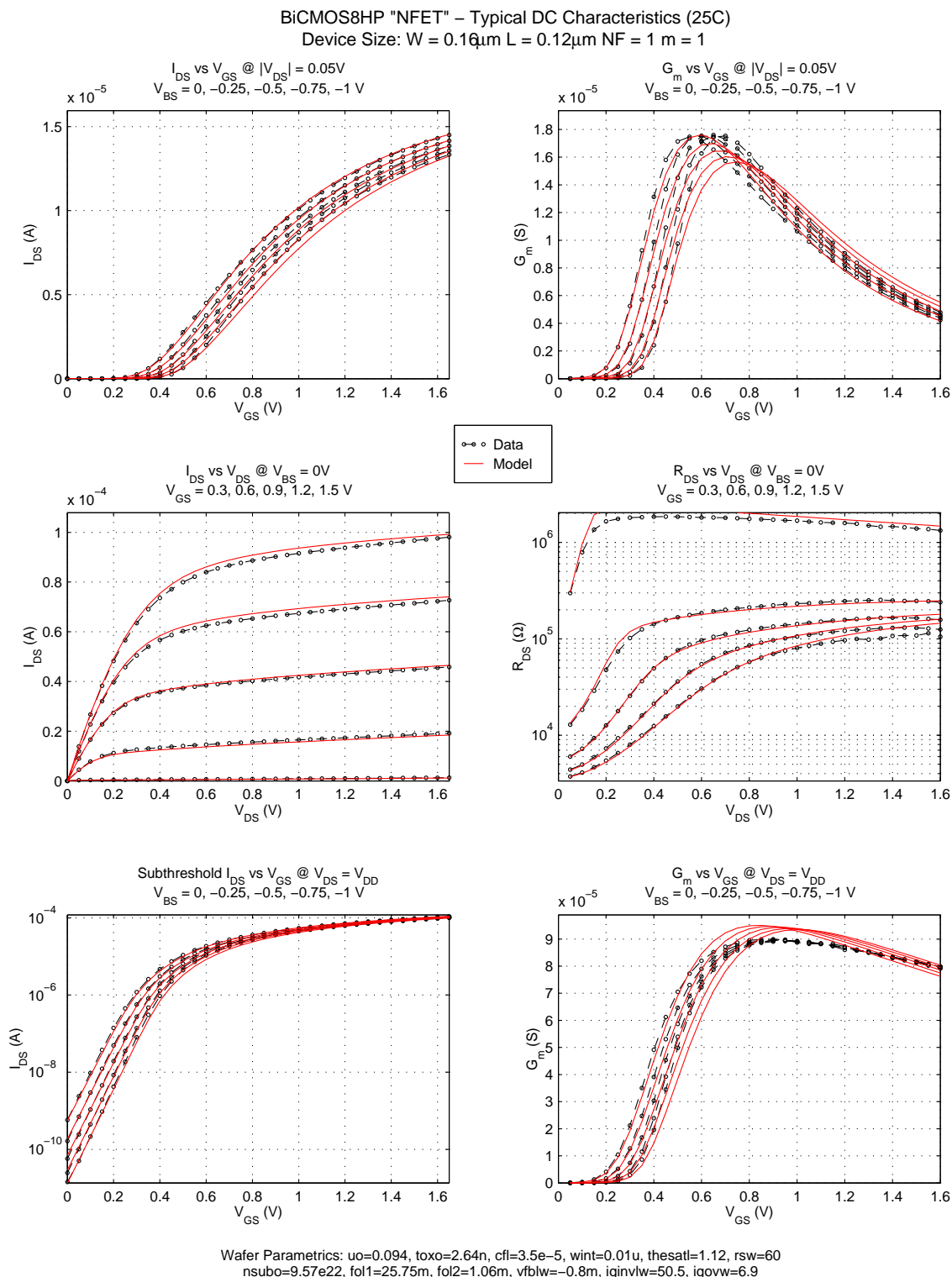


Figure 138. NFET DC Characteristics, $W_{min} \times L_{min}$

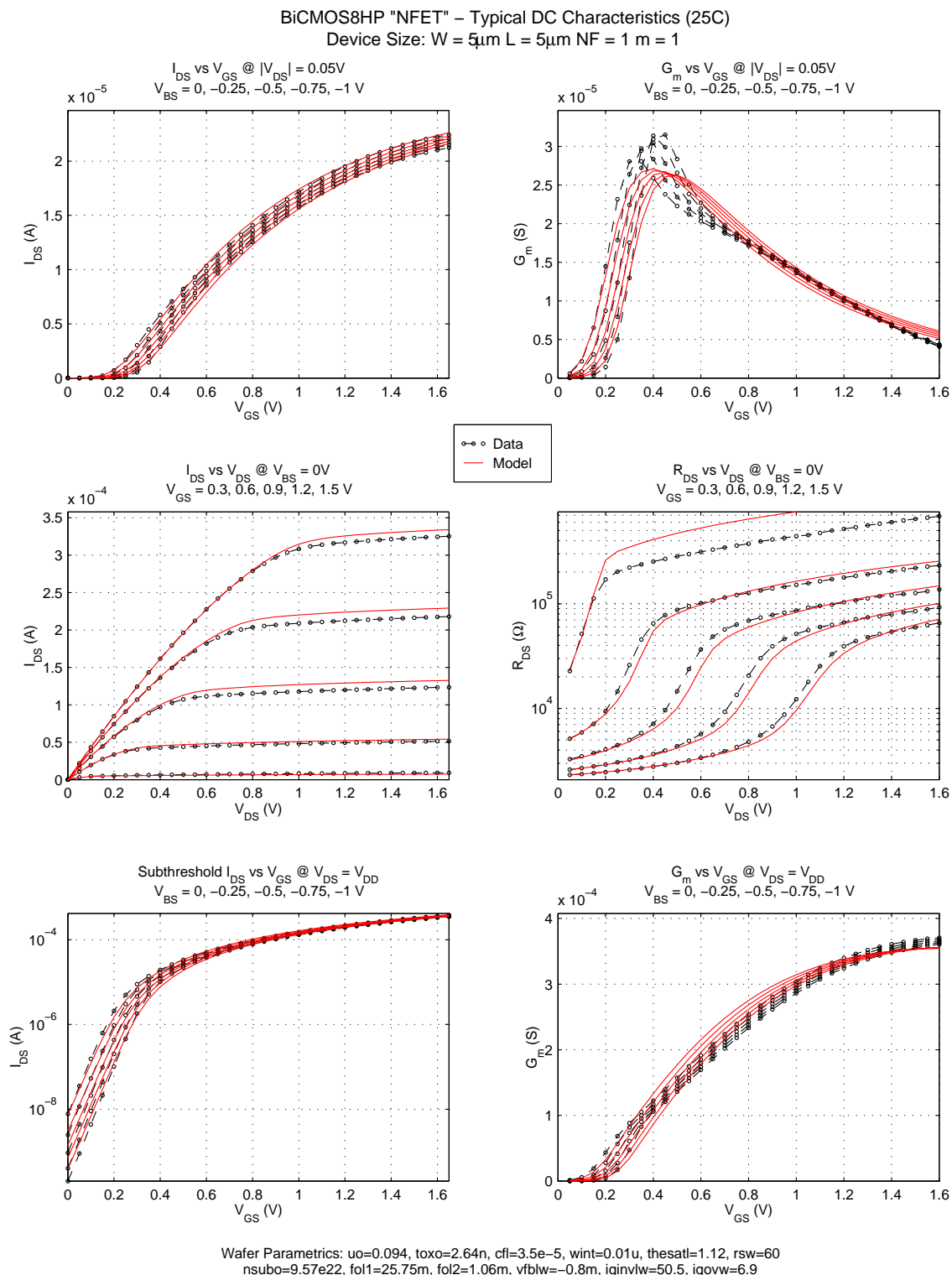


Figure 139. NFET DC Characteristics, $5\mu\text{m} \times 5\mu\text{m}$

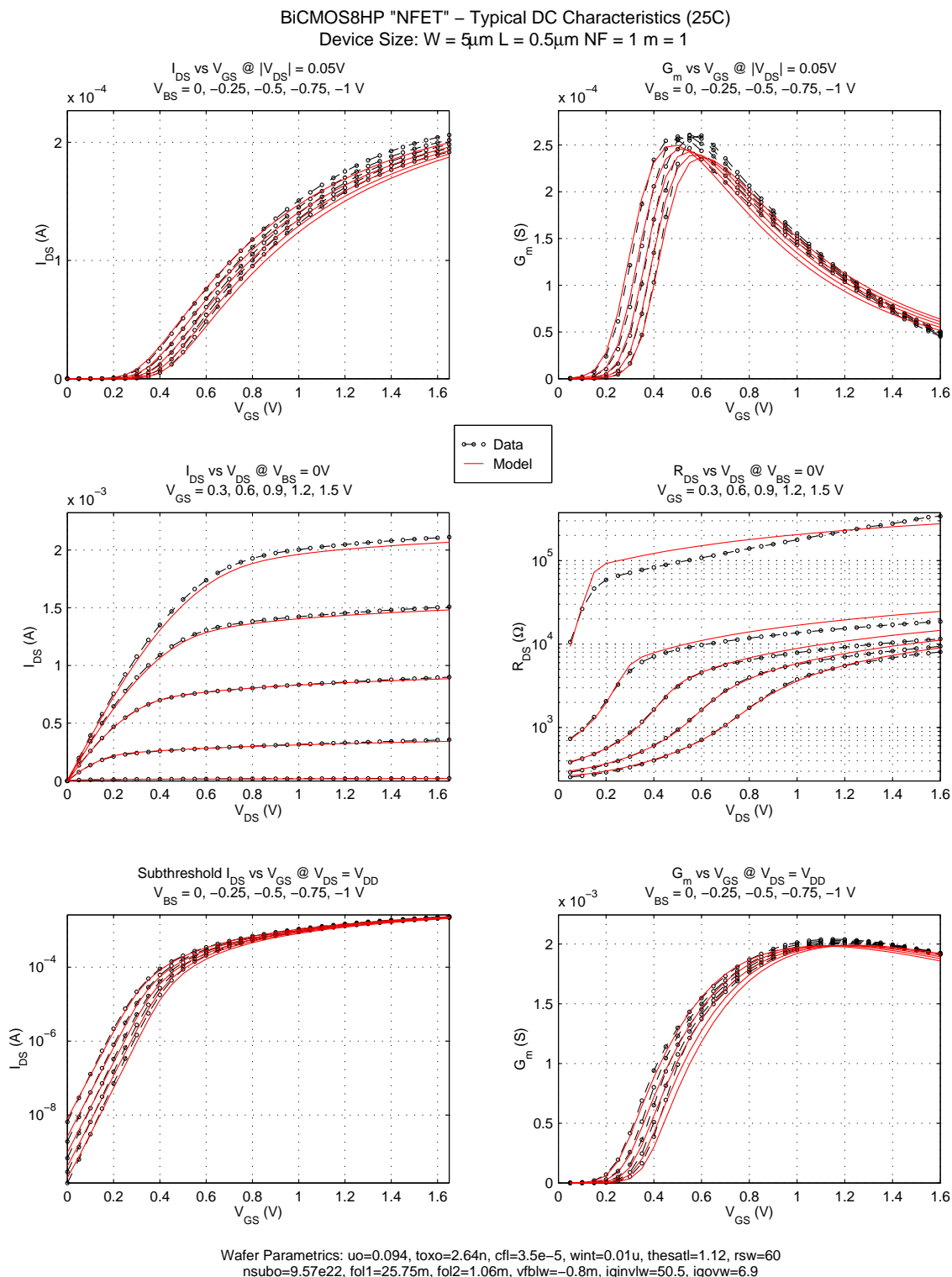


Figure 140. NFET DC Characteristics, $5\mu\text{m} \times 0.5\mu\text{m}$

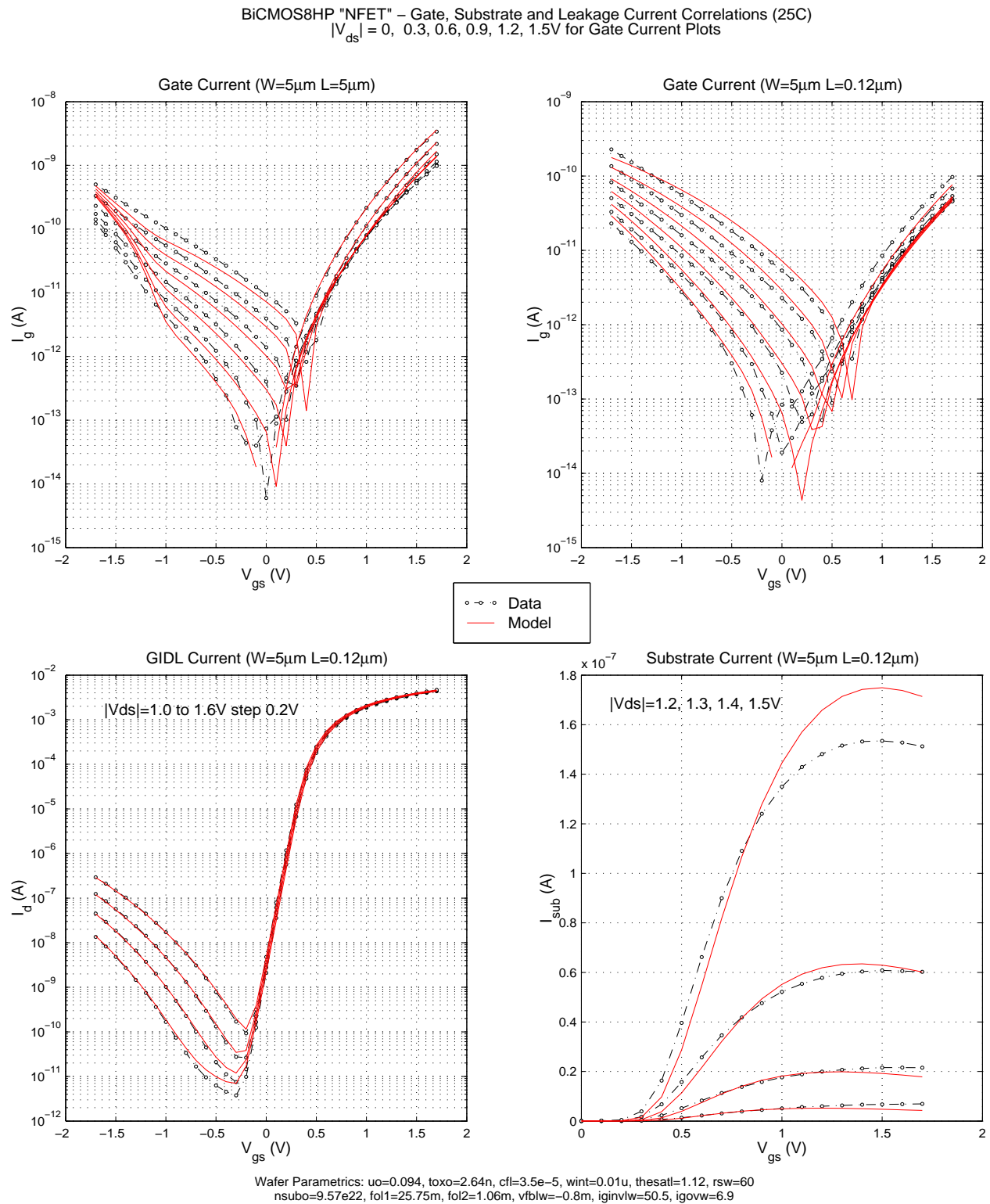


Figure 141. NFET I_{sub} / I_{gidl} / I_{gate} vs V_{gs} , step V_{ds} , $V_{bs}=0V$

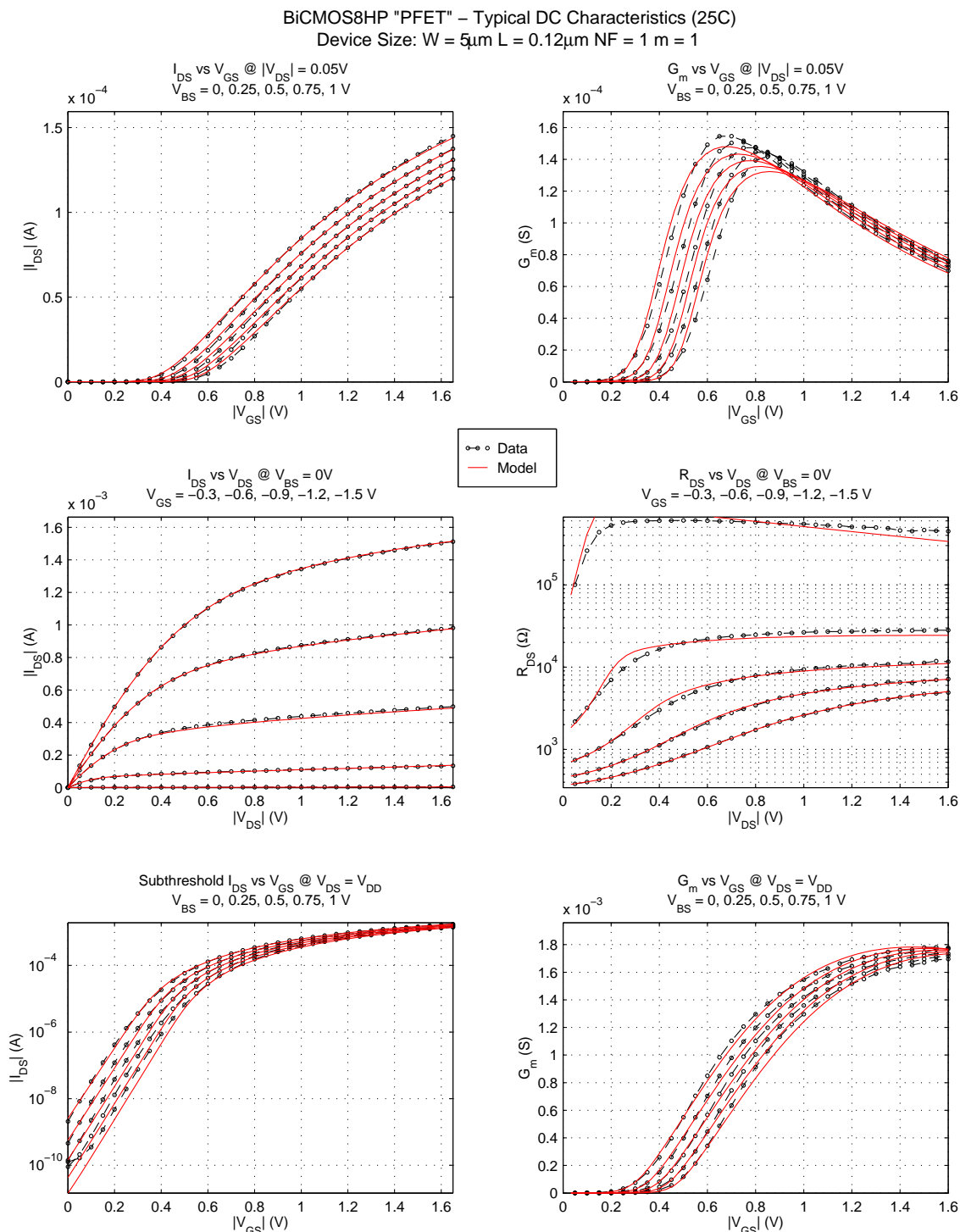


Figure 142. PFET DC Characteristics, $5\mu\text{m} \times L_{min}$

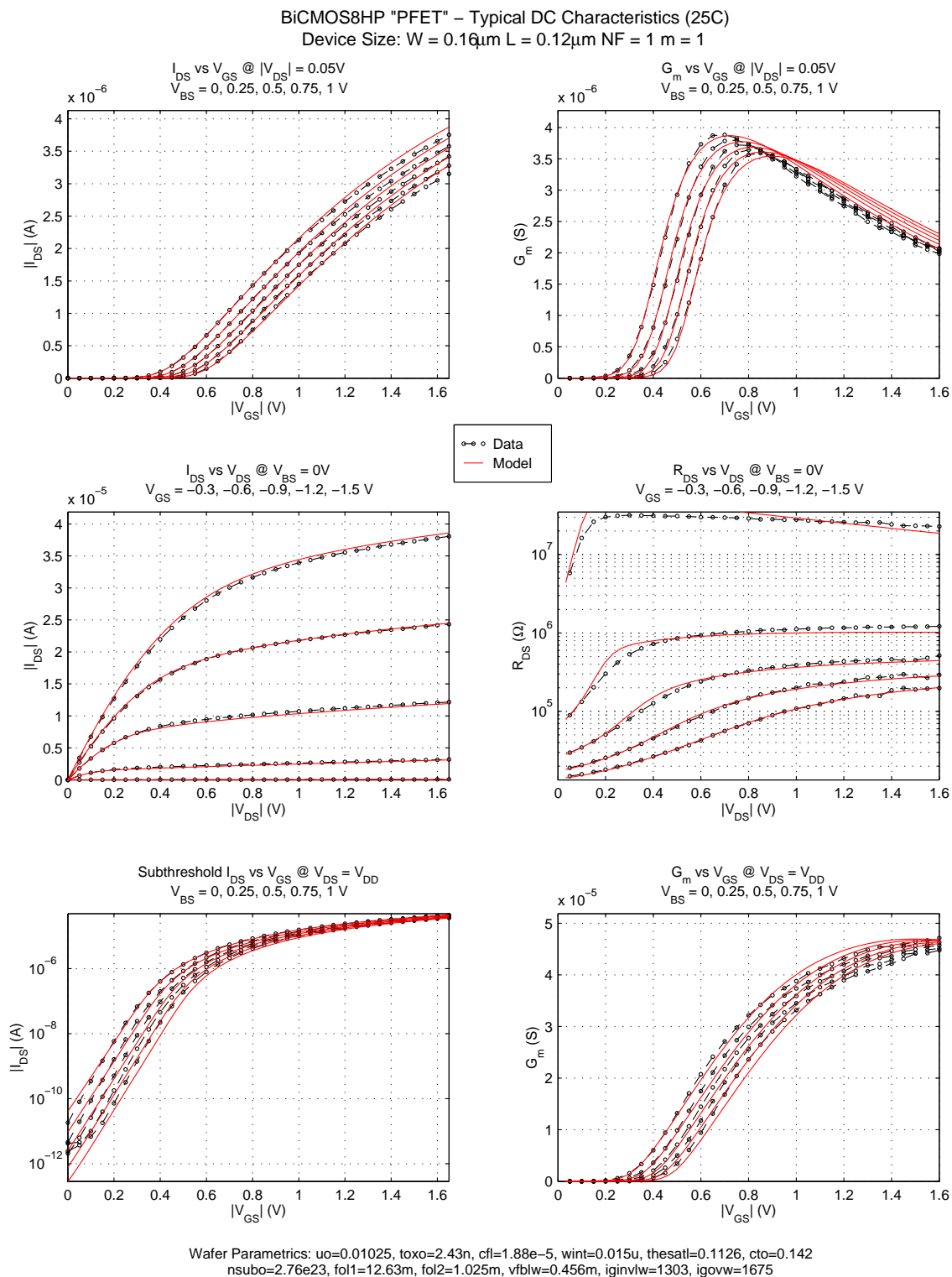


Figure 143. PFET DC Characteristics, $W_{\text{min}} \times L_{\text{min}}$

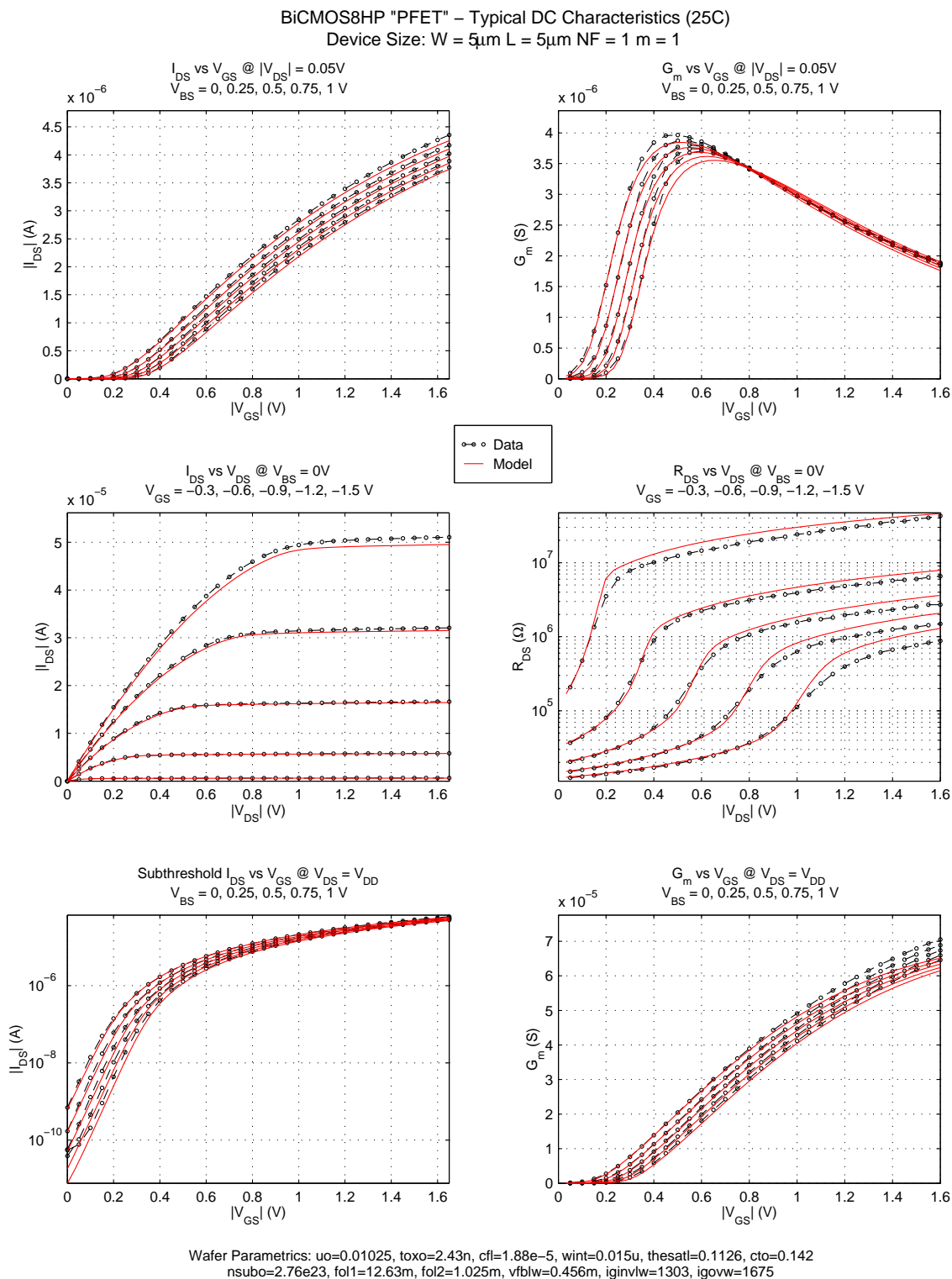


Figure 144. PFET DC Characteristics, $5\mu\text{m} \times 5\mu\text{m}$

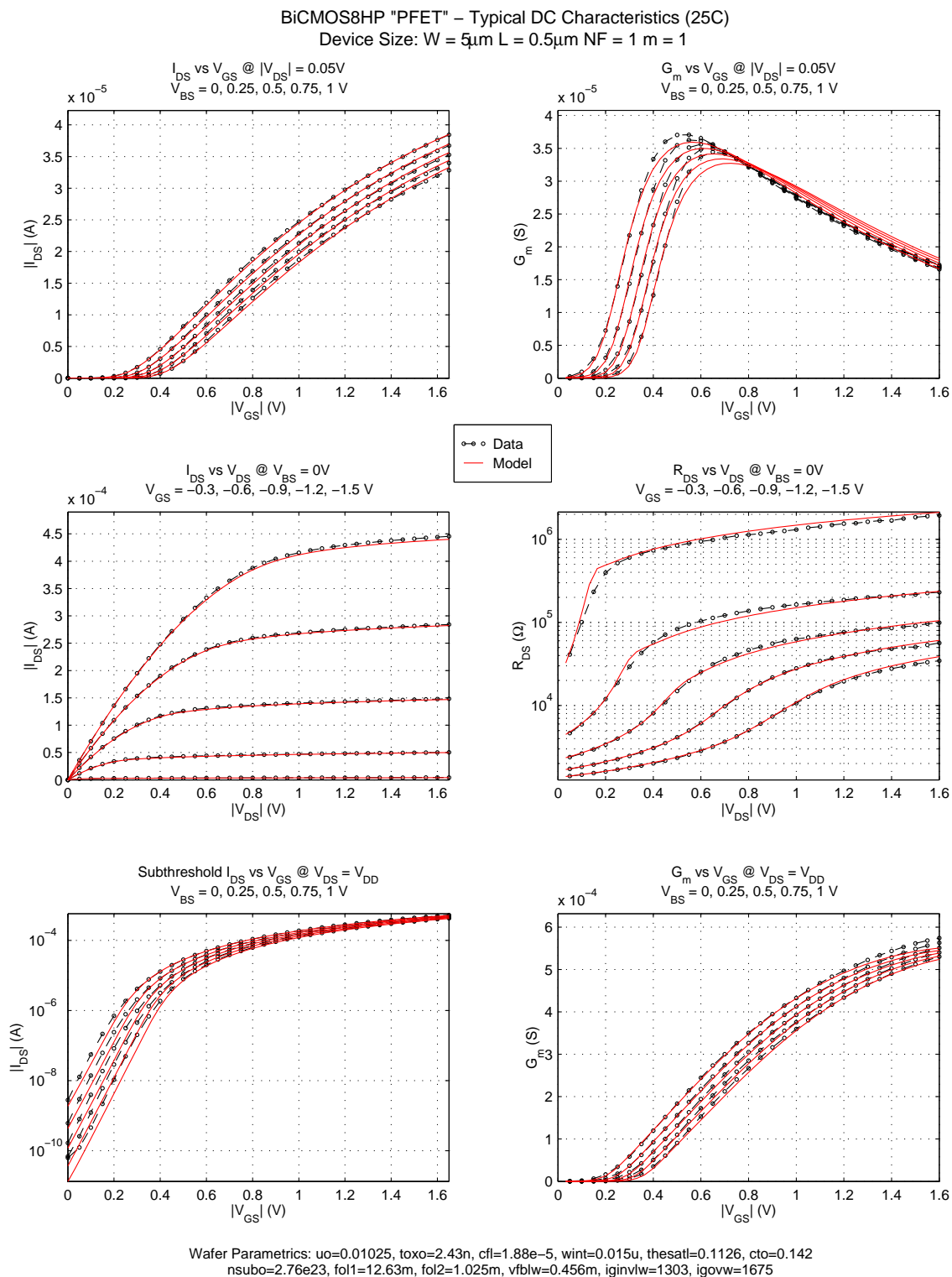


Figure 145. PFET DC Characteristics, $5\mu\text{m} \times 0.5\mu\text{m}$

BiCMOS8HP "PFET" – Gate, Substrate and Leakage Current Correlations (25C)
 $|V_{ds}| = 0, 0.3, 0.6, 0.9, 1.2, 1.5V$ for Gate Current Plots

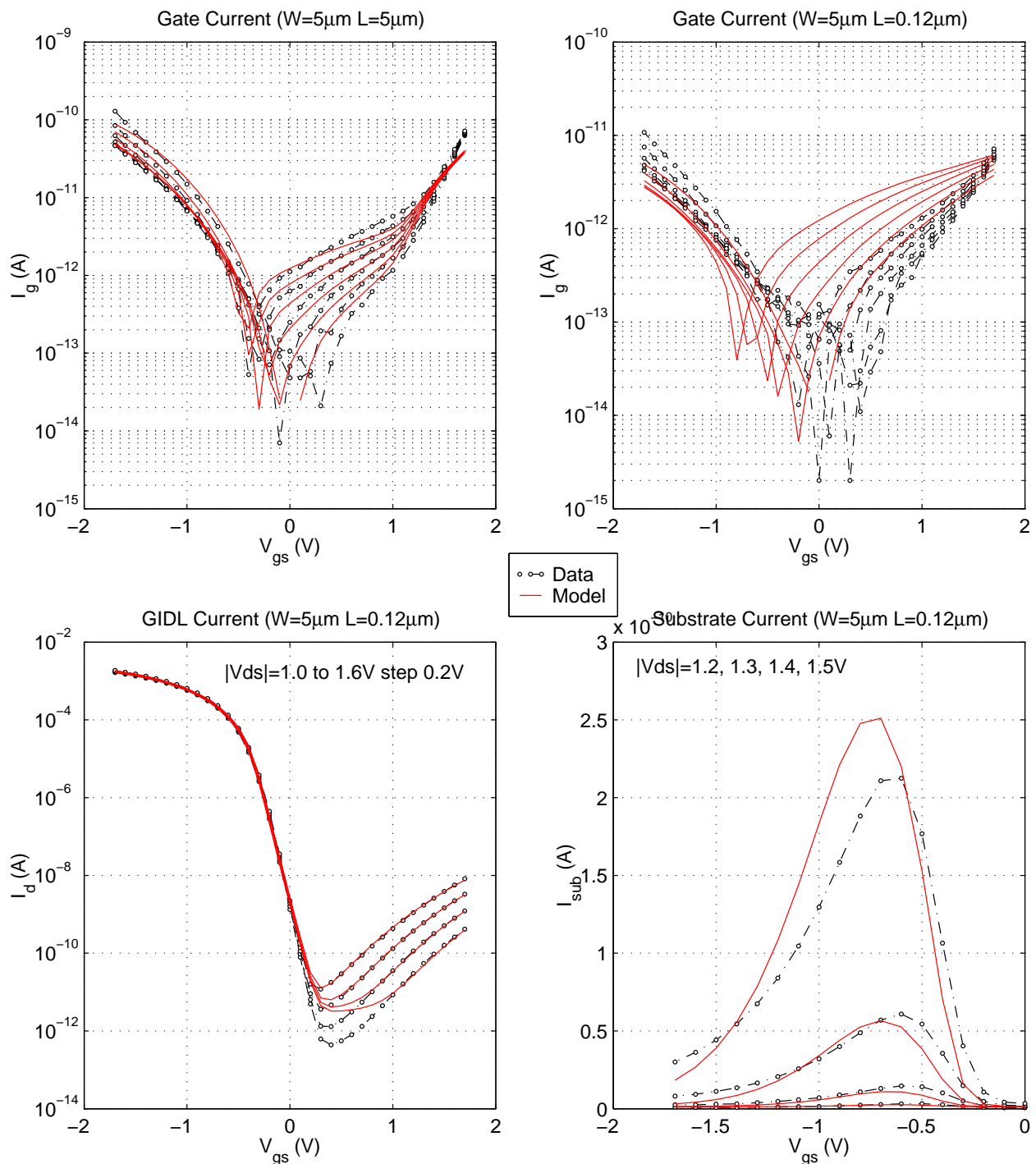
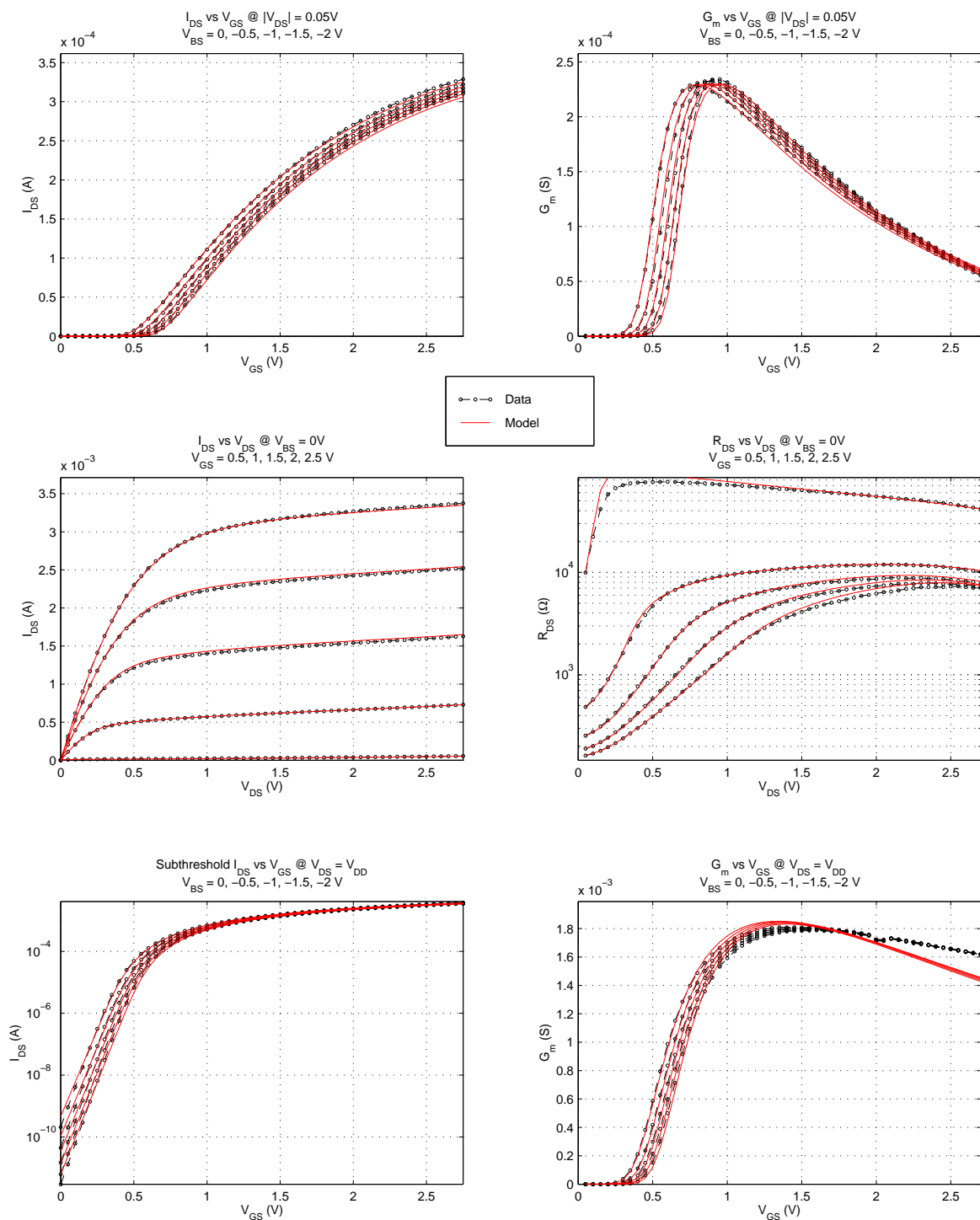


Figure 146. PFET I_{sub} / I_{gidl} / I_{gate} vs V_{gs} , step V_{ds} , $V_{bs}=0V$

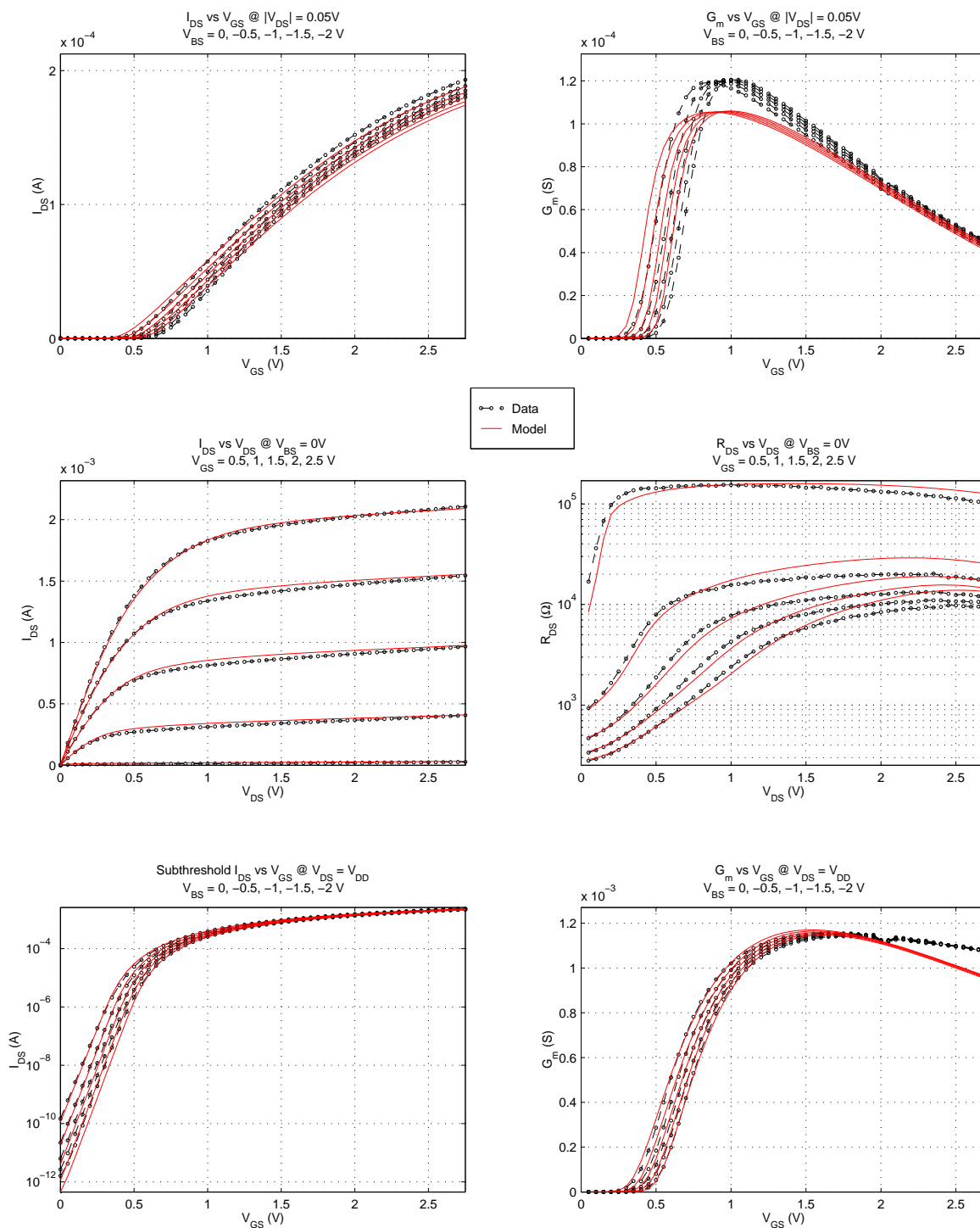
BiCMOS8HP "DGNFET" – Typical DC Characteristics (25C)
Device Size: $W = 5\mu\text{m}$ $L = 0.24\mu\text{m}$ $NF = 1$ $m = 1$



Wafer Parametrics: $\text{tox}=5.25\text{n}$, $\text{vfb}=-0.926$, $\text{vfb1}=-0.007$, $\text{thesat1}=-0.005448$, $\text{rsw}=160.6$

Figure 147. DGNFET DC Characteristics, $5\mu\text{m} \times L_{\text{min}}$

BiCMOS8HP "DGNFET" – Typical DC Characteristics (25C)
Device Size: $W = 0.36\mu\text{m}$ $L = 0.24\mu\text{m}$ $NF = 10$ $m = 1$



Wafer Parametrics: $\text{tox}=5.25\text{n}$, $\text{vfb}=-0.926$, $\text{vfb1}=-0.0007$, $\text{thesatlw}=-0.005448$, $\text{rsw}=160.6$

Figure 148. DGNFET DC Characteristics, $W_{\text{min}} \times L_{\text{min}}$, $m=10$

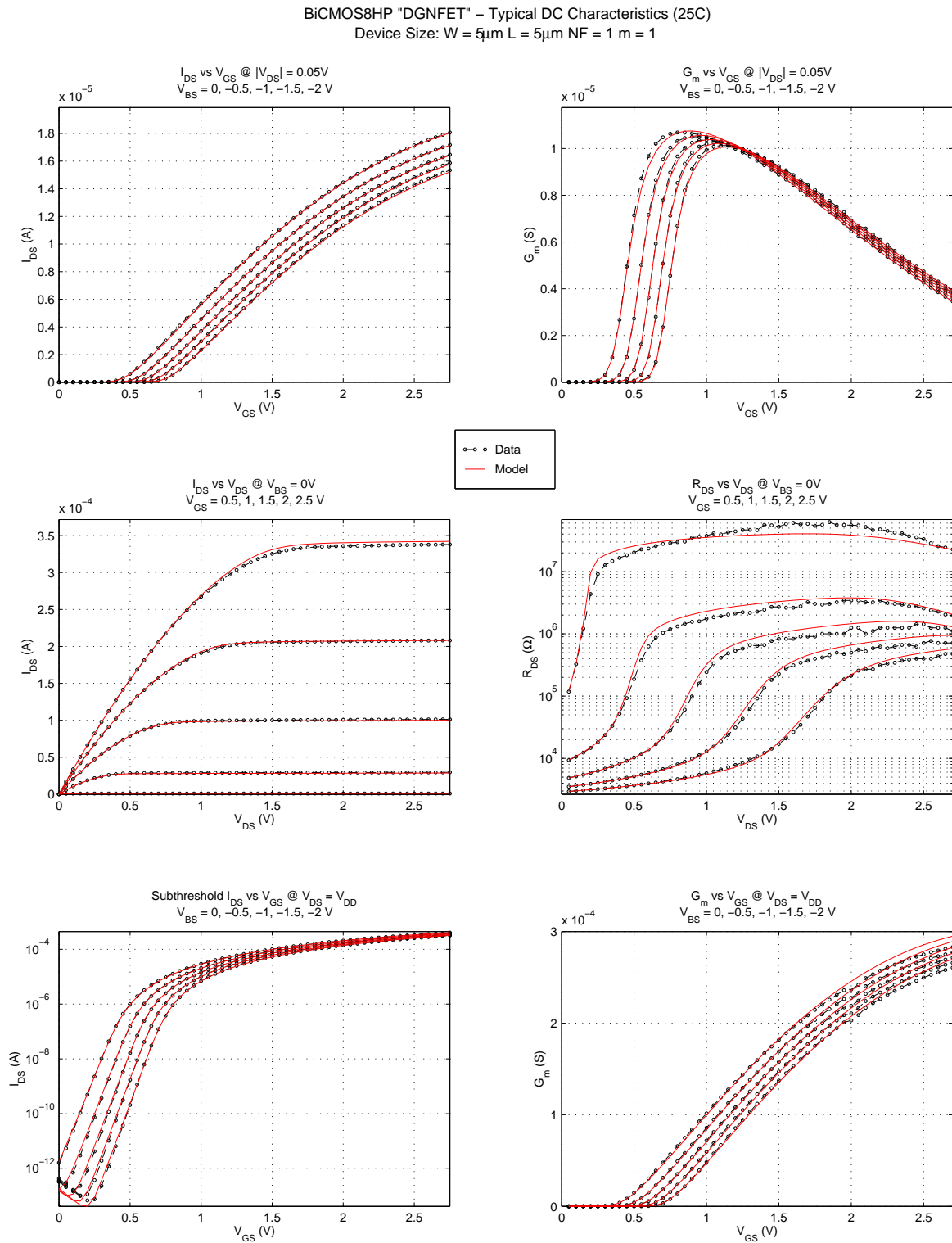
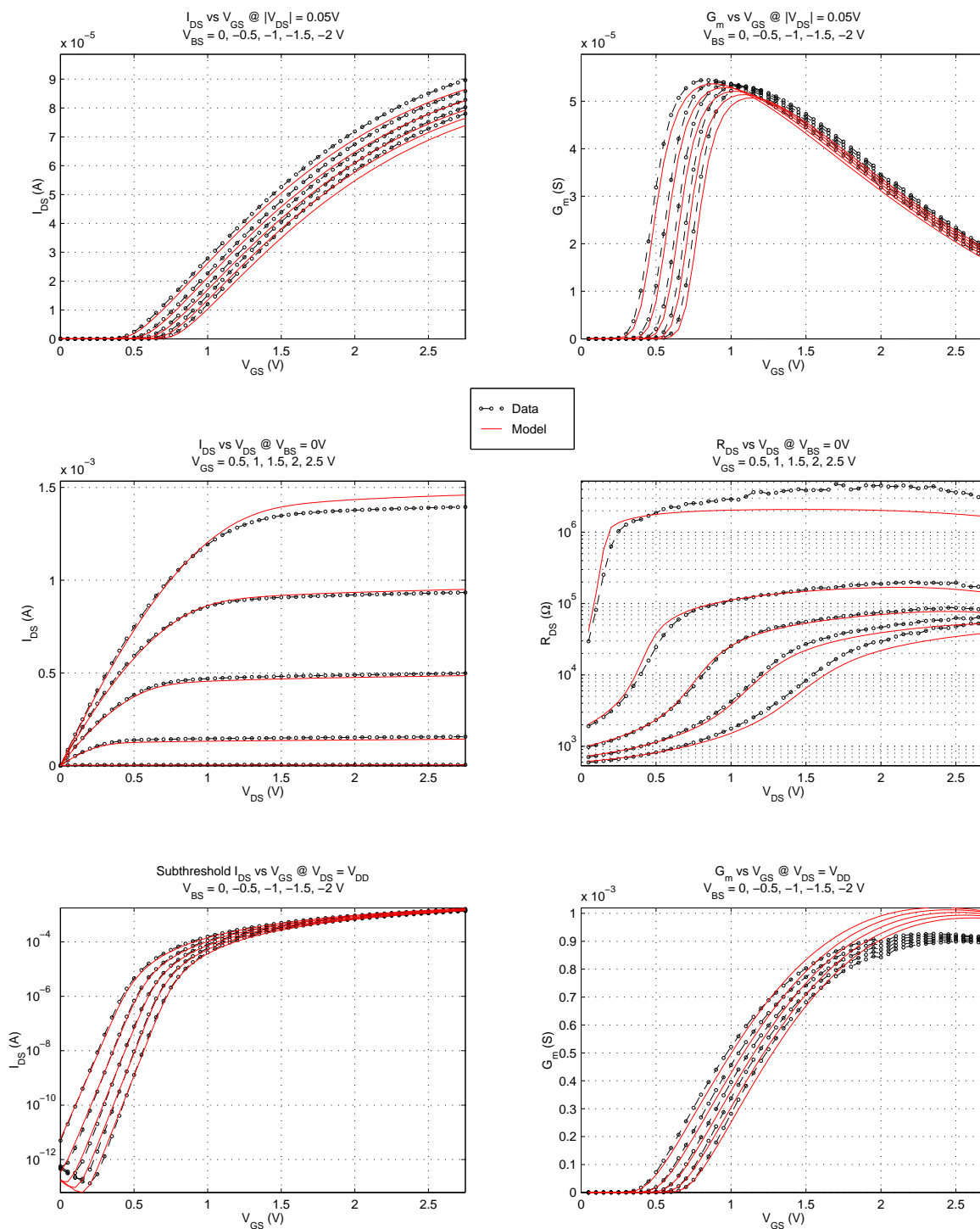


Figure 149. DGNFET DC Characteristics, $5\mu\text{m} \times 5\mu\text{m}$

BiCMOS8HP "DGNFET" – Typical DC Characteristics (25C)
Device Size: $W = 5\mu\text{m}$ $L = 1\mu\text{m}$ $NF = 1$ $m = 1$



Wafer Parameters: $\text{tox}=5.25\text{n}$, $\text{vfb}=-0.926$, $\text{vfb1}=-0.007$, $\text{thesat1}=-0.005448$, $\text{rsw}=160.6$

Figure 150. DGNFET DC Characteristics, $5\mu\text{m} \times 4^*L\text{min}$

BiCMOS8HP "DG FET" –Substrate and GIDL Current Correlations (25C)
 $|V_{ds}| = 1.9, 2.1, 2.3, 2.5V$ for Substrate Current Plots

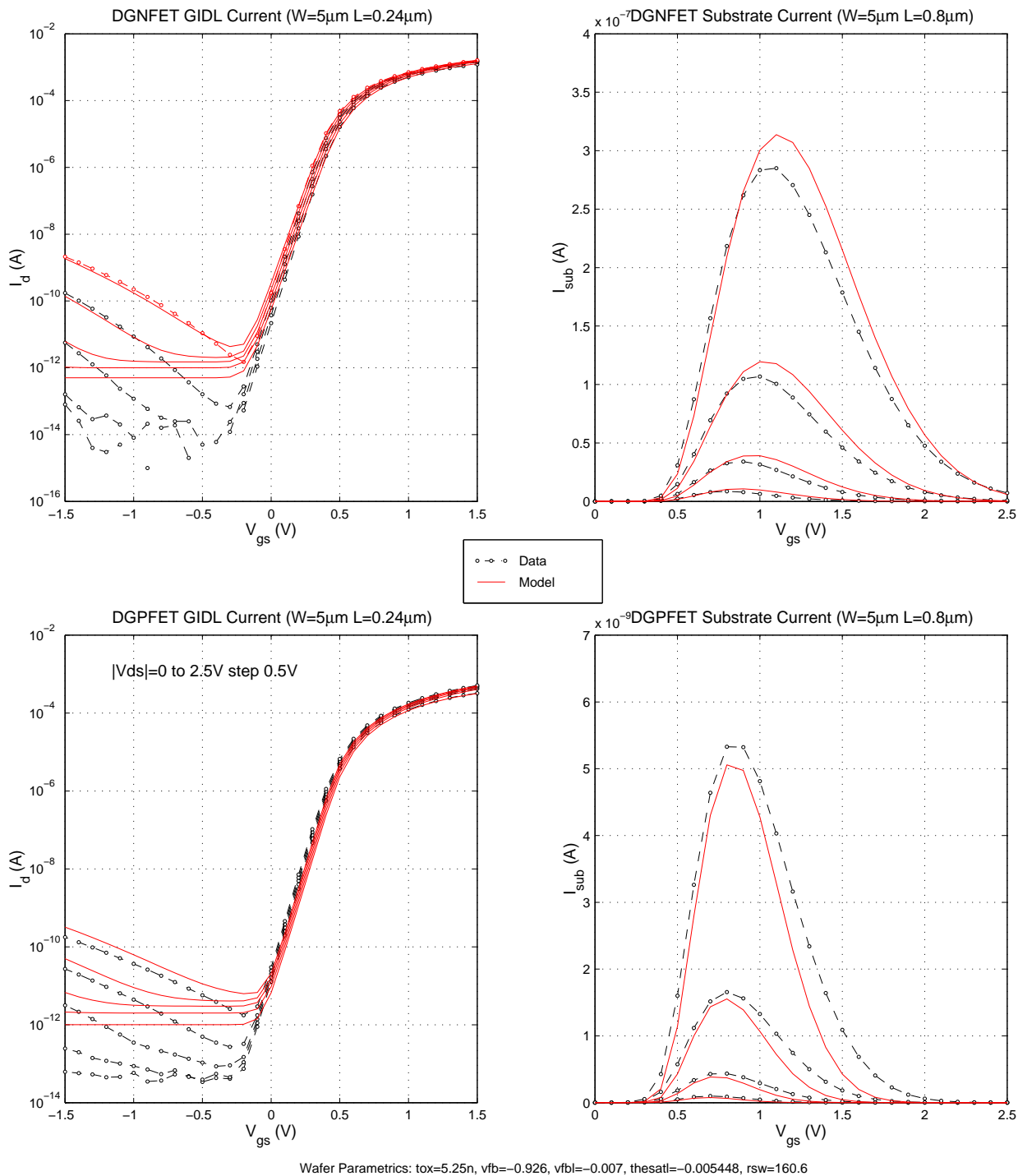
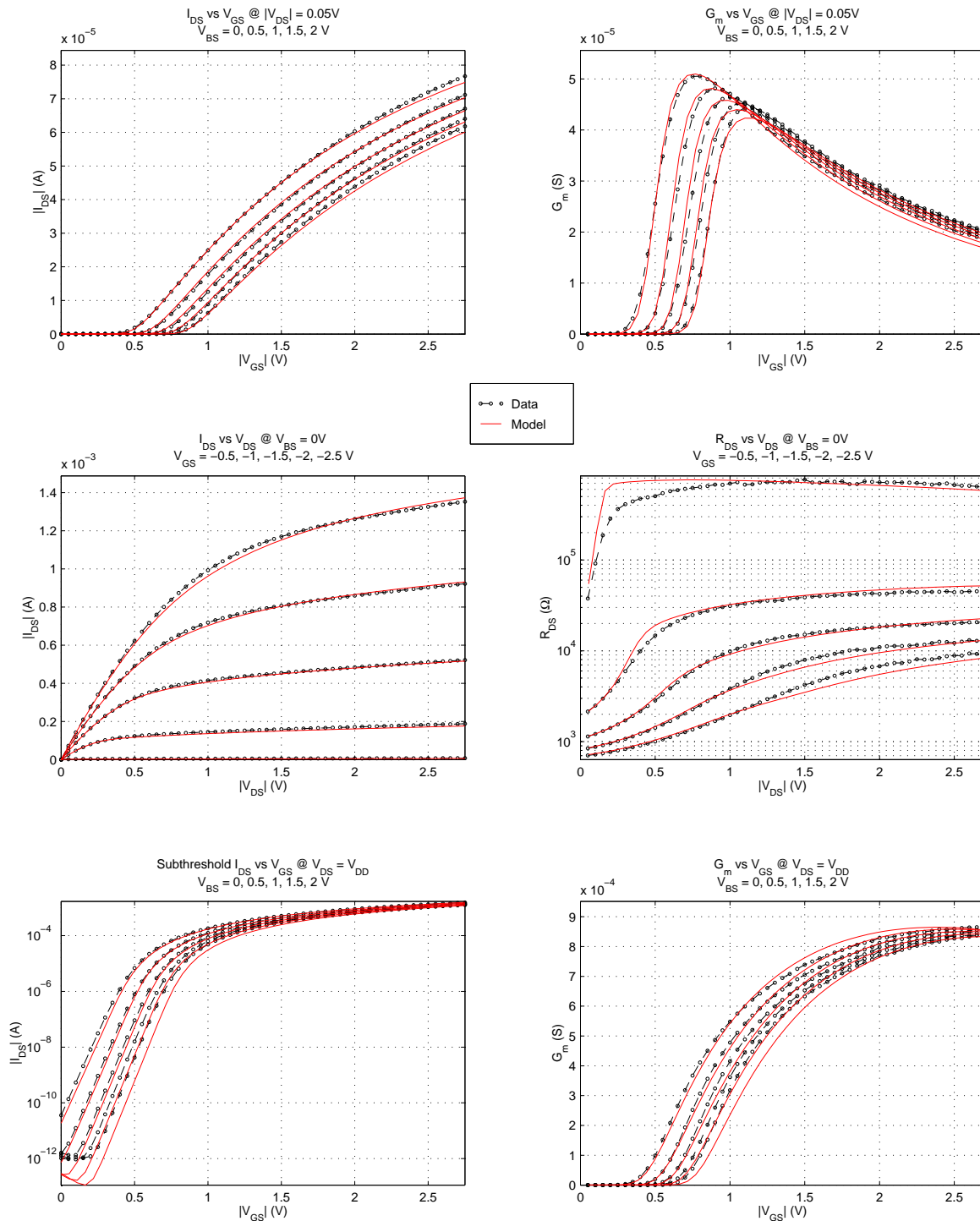


Figure 151. DGNFET, DGPJET I_{sub} / I_{gidl} vs V_{gs} , step V_{ds} , $V_{bs}=0V$

BiCMOS8HP "DGPFFET" – Typical DC Characteristics (25C)
Device Size: $W = 5\mu\text{m}$ $L = 0.24\mu\text{m}$ $NF = 1$ $m = 1$



Wafer Parametrics: $\text{tox}=5.383\text{n}$, $\text{u0}=0.01819$, $\text{vfb}=-0.9972$, $\text{vfb1}=0.01633$ $\text{dl}=3.192\text{e}-8$

Figure 152. DGPFFET DC Characteristics, $5\mu\text{m} \times L_{\text{min}}$

BiCMOS8HP "DGPFET" – Typical DC Characteristics (25C)
Device Size: $W = 0.36\mu\text{m}$ $L = 0.24\mu\text{m}$ $NF = 1$ $m = 1$

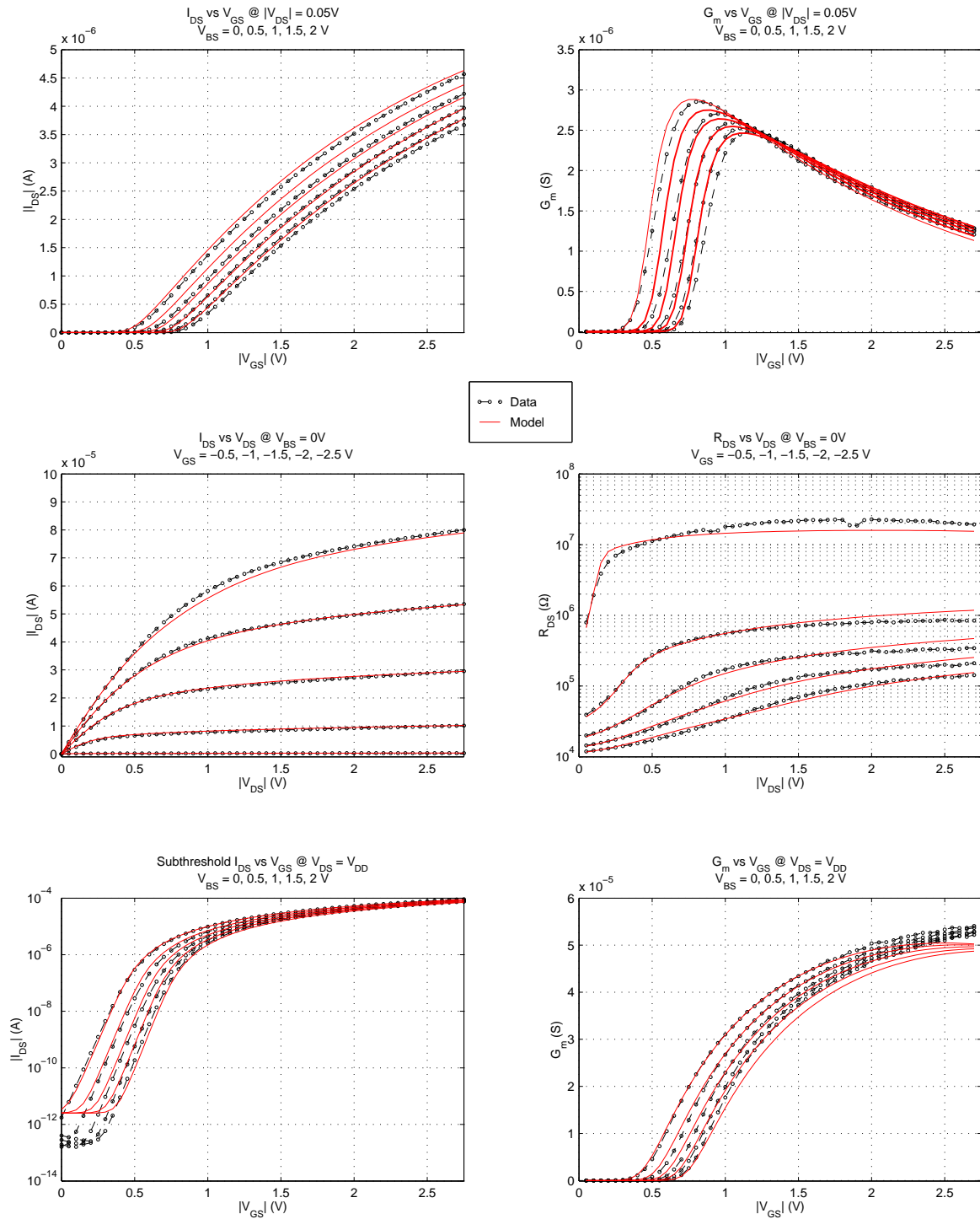


Figure 153. DGPFET DC Characteristics, $W_{\text{min}} \times L_{\text{min}}$, $m=10$

BiCMOS8HP "DGPFET" – Typical DC Characteristics (25C)
Device Size: $W = 5\mu\text{m}$ $L = 5\mu\text{m}$ $NF = 1$ $m = 1$

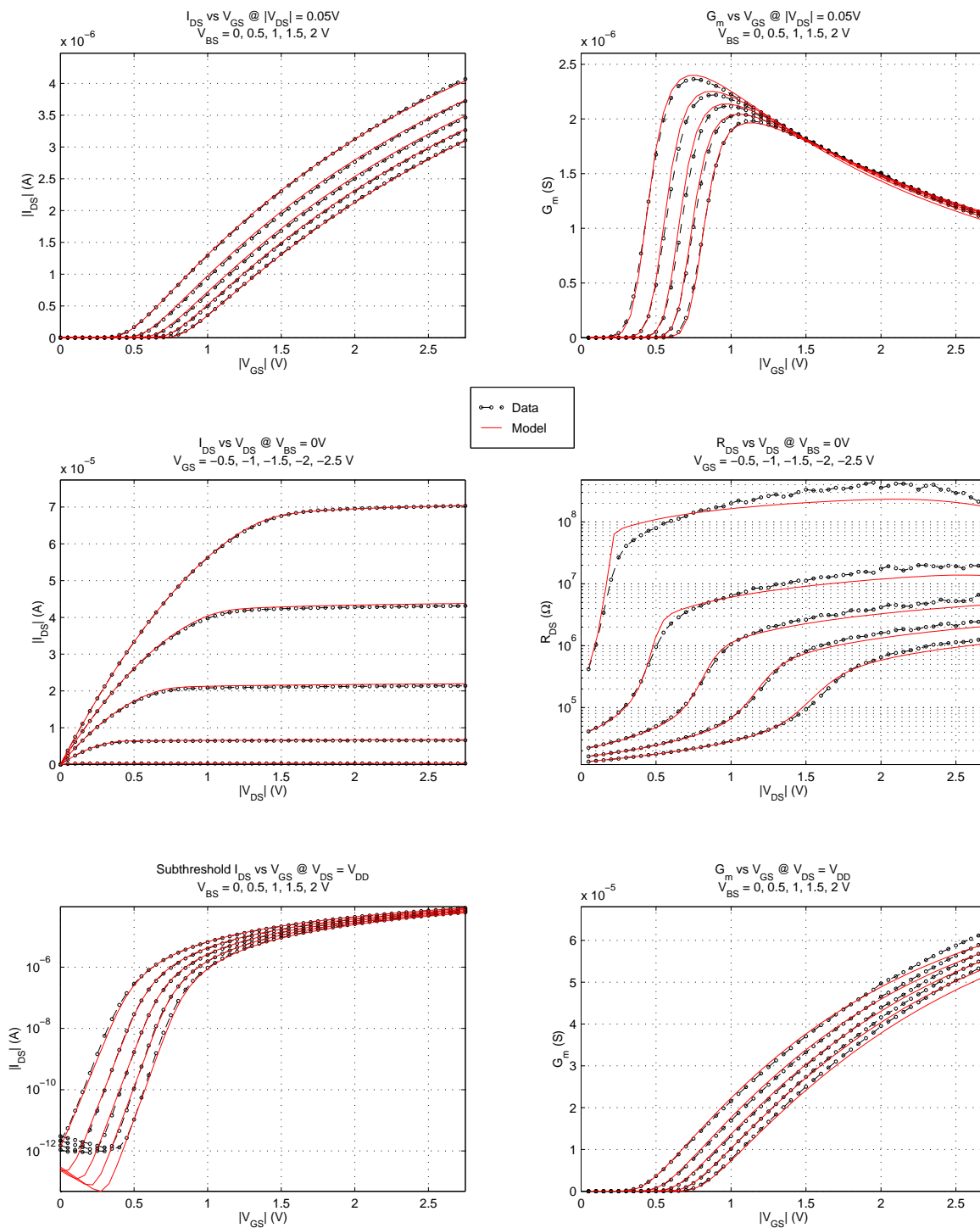
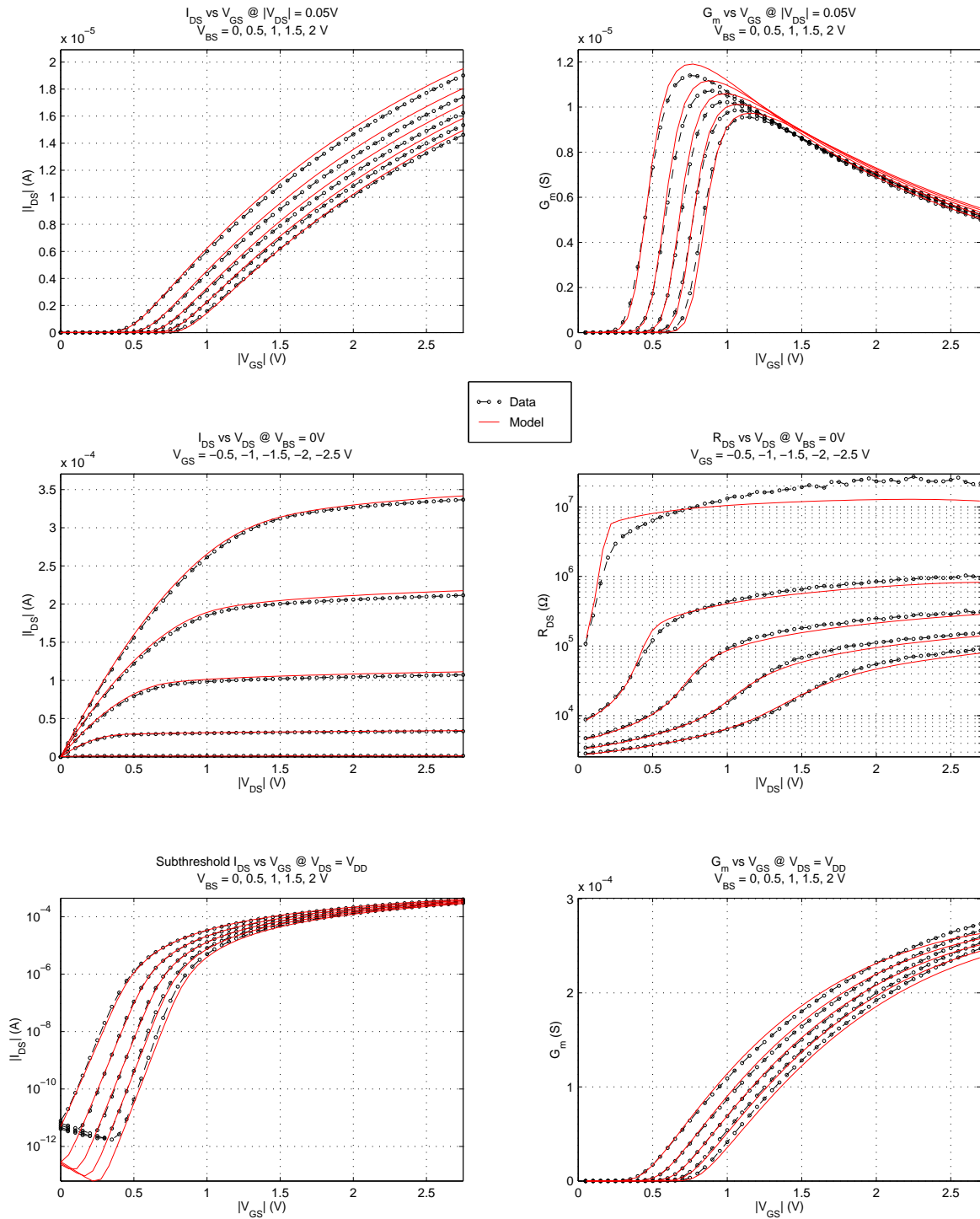


Figure 154. DGPFET DC Characteristics, $5\mu\text{m} \times 5\mu\text{m}$

BiCMOS8HP "DGPfet" – Typical DC Characteristics (25C)

Device Size: $W = 5\mu\text{m}$ $L = 1\mu\text{m}$ $NF = 1$ $m = 1$



Wafer Parametrics: $\text{tox}=5.383\text{n}$, $u_0=0.01819$, $\text{vfb}=-0.9972$, $\text{vfbI}=0.01633$ $\text{dl}=3.192\text{e}-8$

Figure 155. DGPfet DC Characteristics, $5\mu\text{m} \times 4\mu\text{m}$

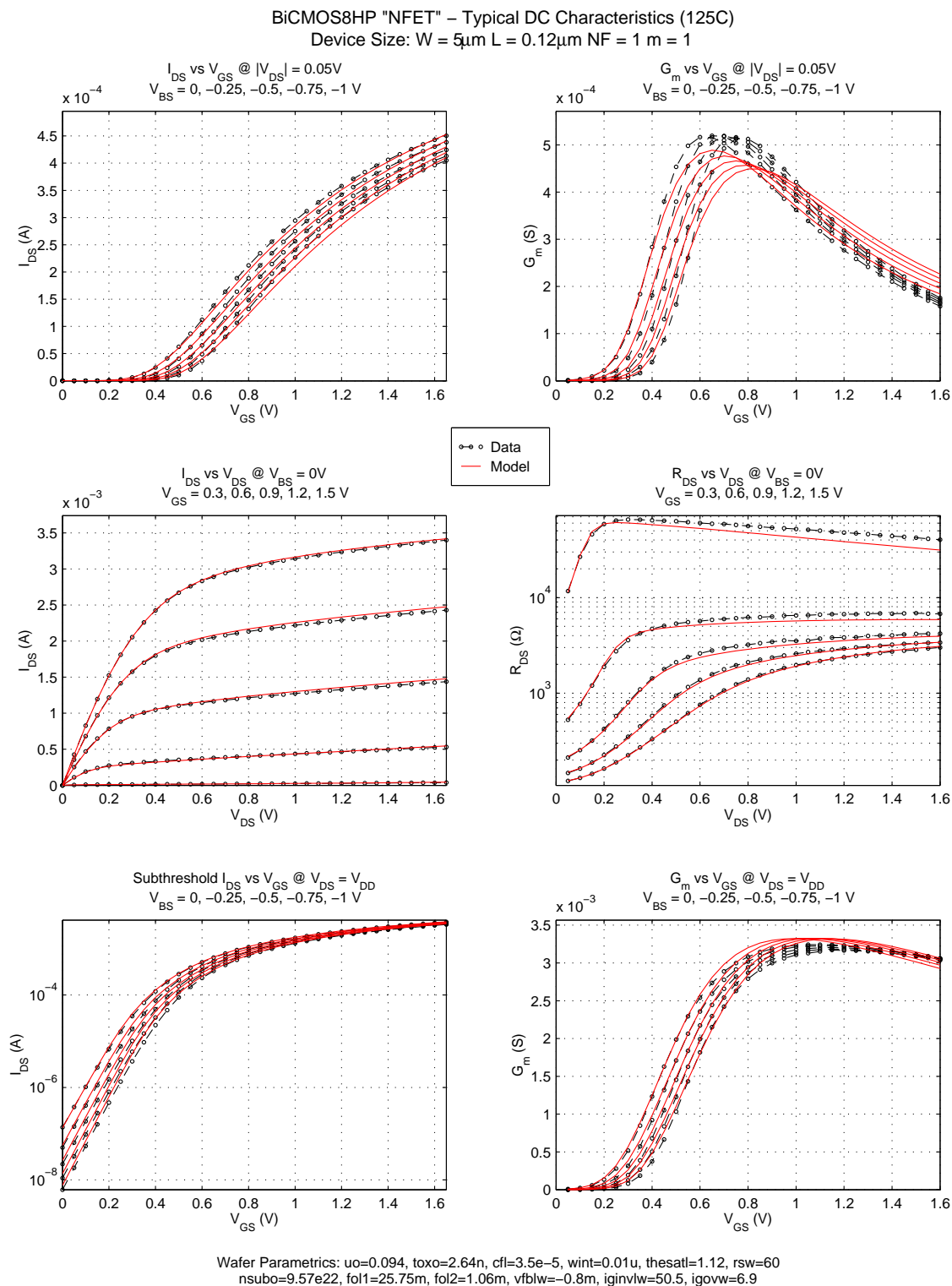


Figure 156. NFET DC Characteristics, $5\mu\text{m} \times L_{min}$ (125C)

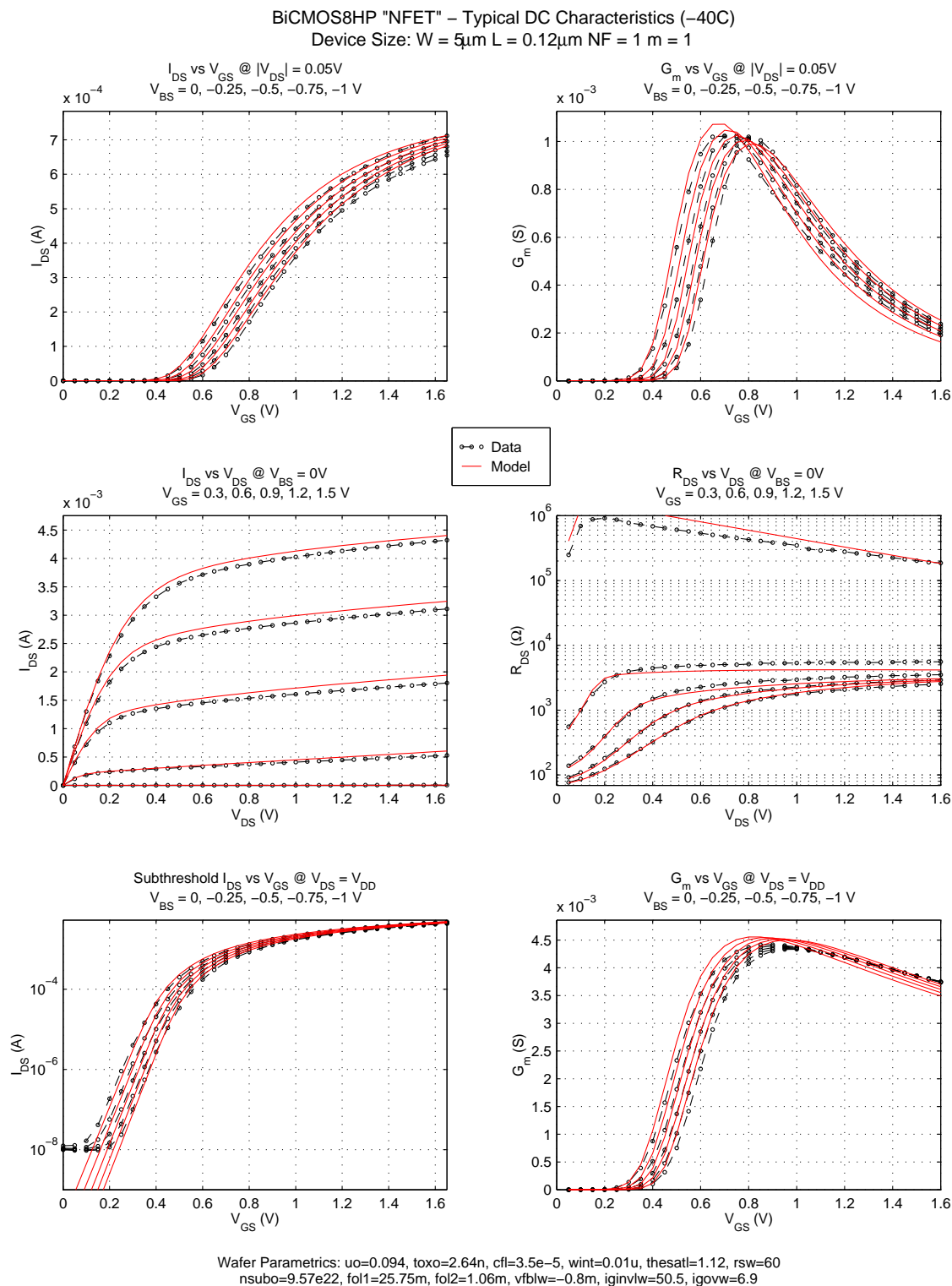


Figure 157. NFET DC Characteristics, $5\mu\text{m} \times L_{min}$ (-40C)

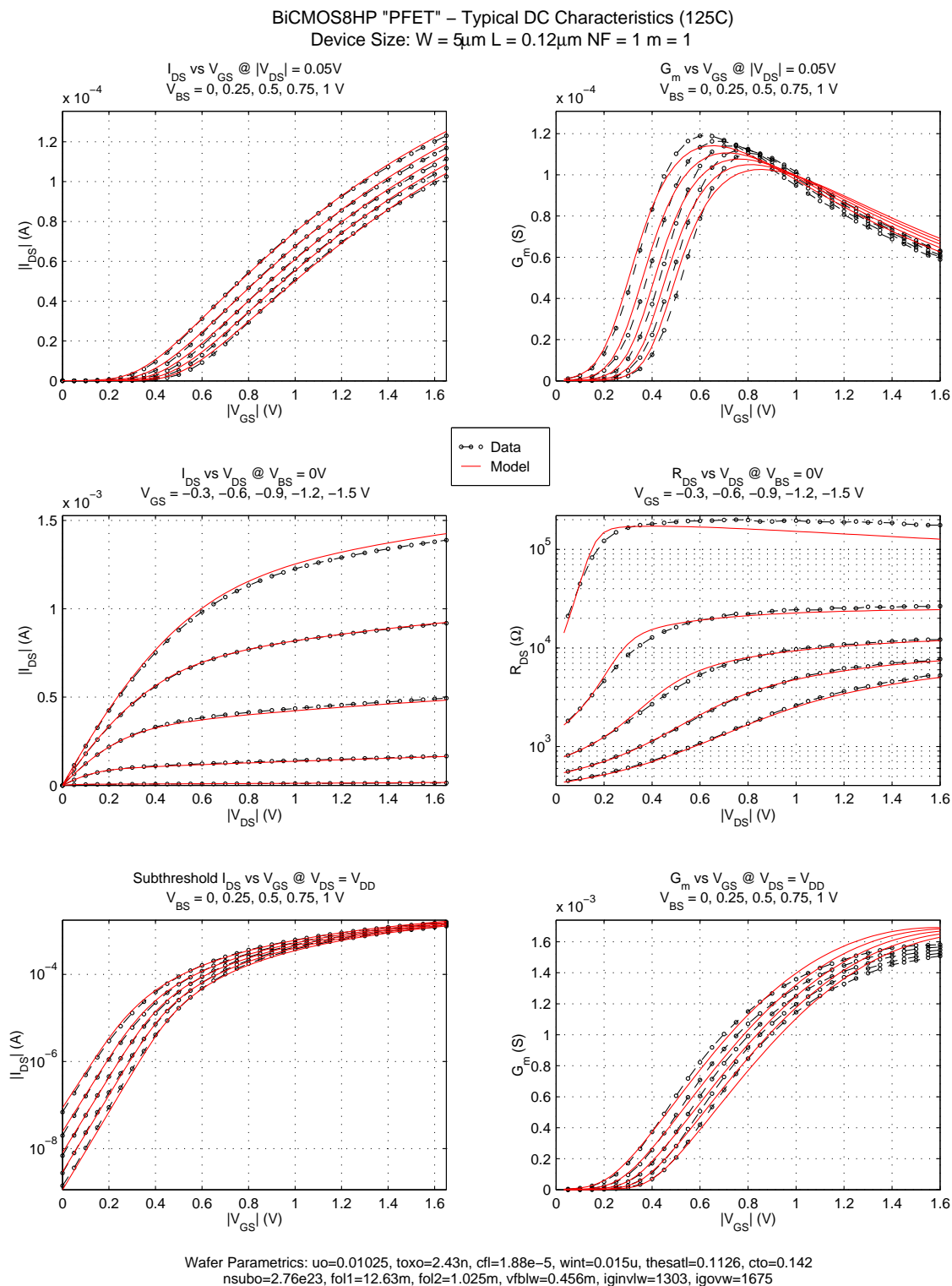


Figure 158. PFET DC Characteristics, $5\mu\text{m} \times L_{min}$ (125C)

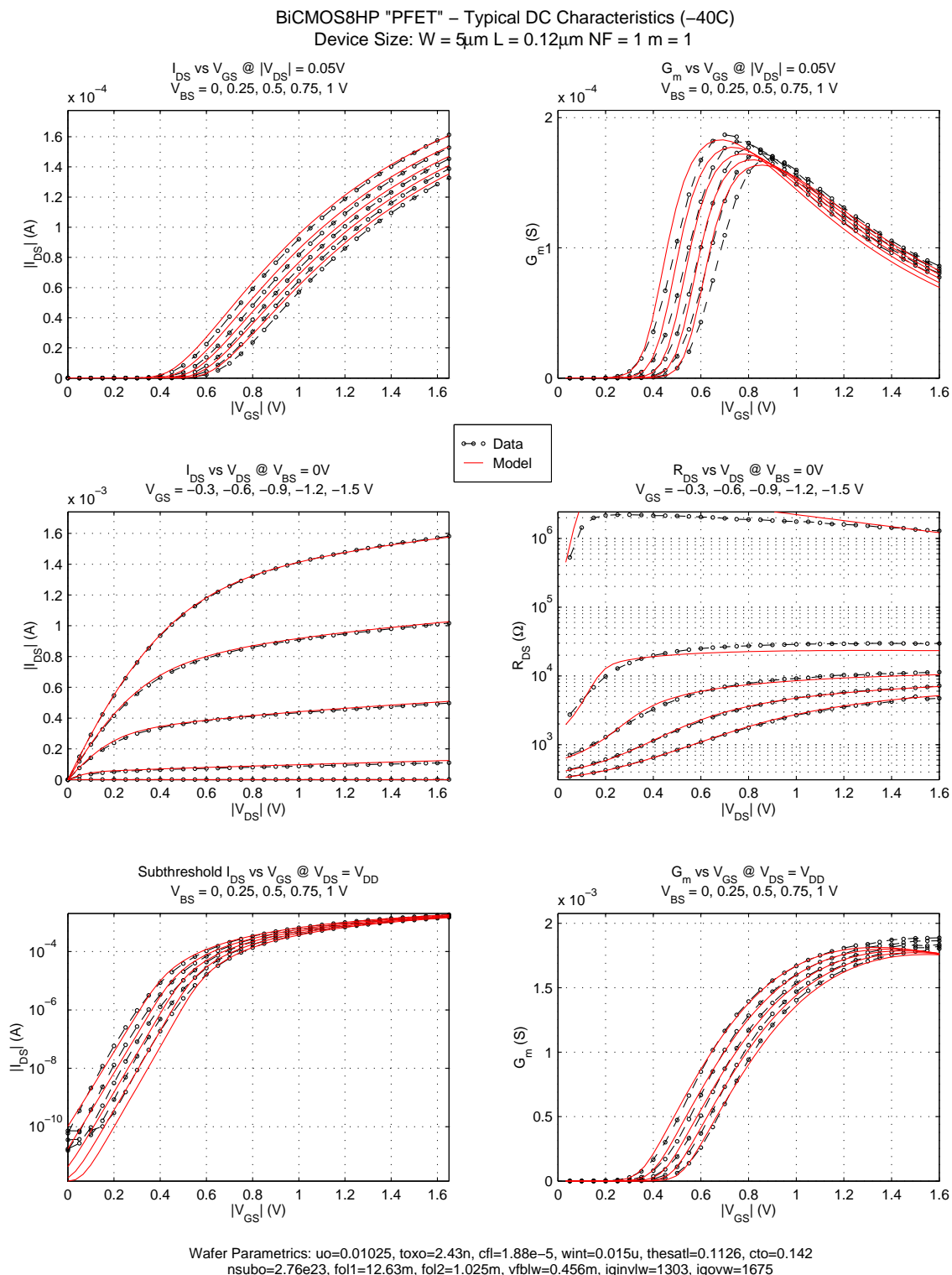
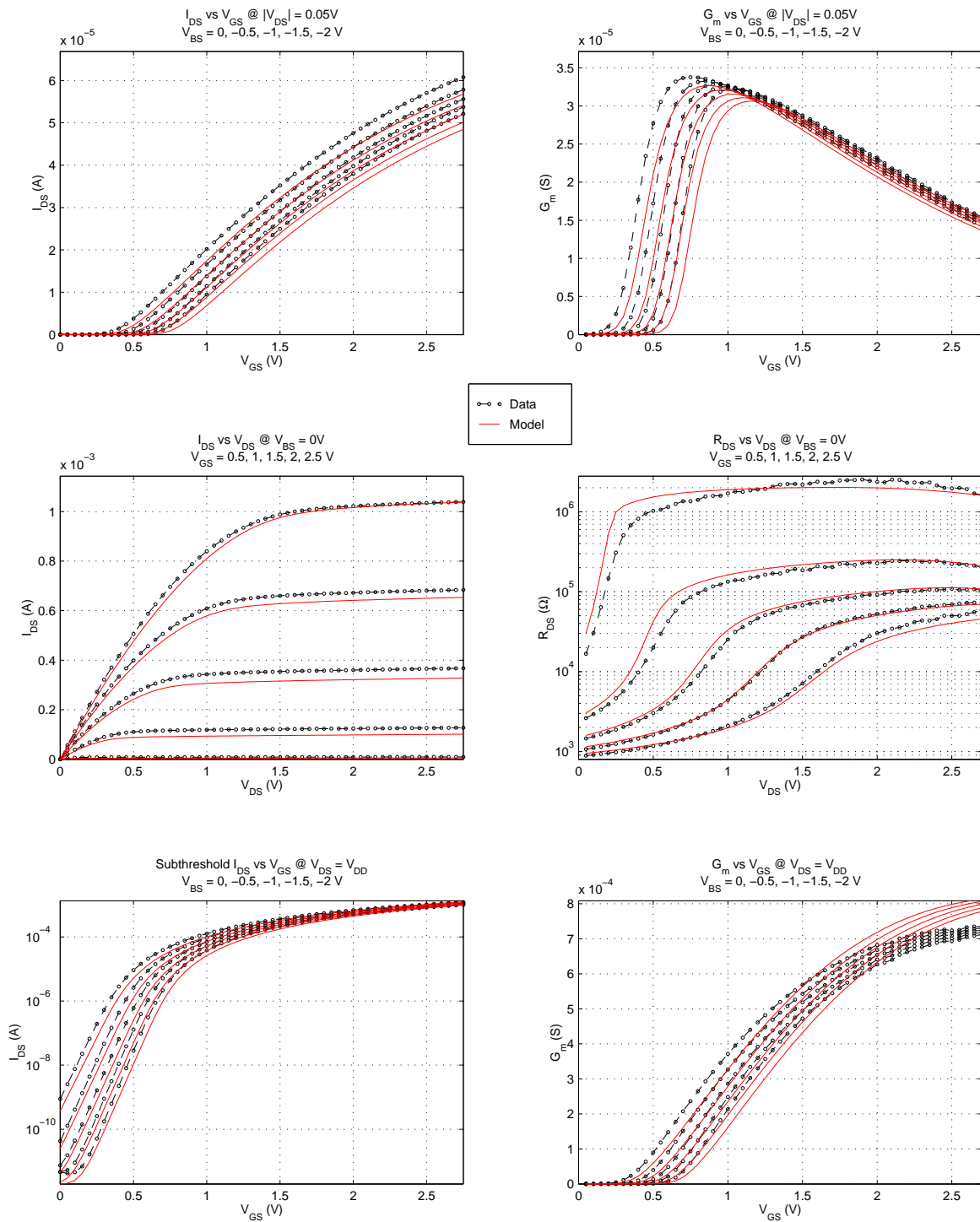


Figure 159. PFET DC Characteristics, $5\mu\text{m} \times L_{\text{min}}$ (–40C)

BiCMOS8HP "DGNFET" – Typical DC Characteristics (125C)
Device Size: $W = 5\mu\text{m}$ $L = 1\mu\text{m}$ $NF = 1$ $m = 1$



Wafer Parametrics: $\text{tox}=5.25\text{n}$, $\text{vfb}=-0.926$, $\text{vfb1}=-0.007$, $\text{thesat1}=-0.005448$, $\text{rsw}=160.6$

Figure 160. DGNFET DC Characteristics, $5\mu\text{m} \times 4^*L_{\text{min}}$ (125C)

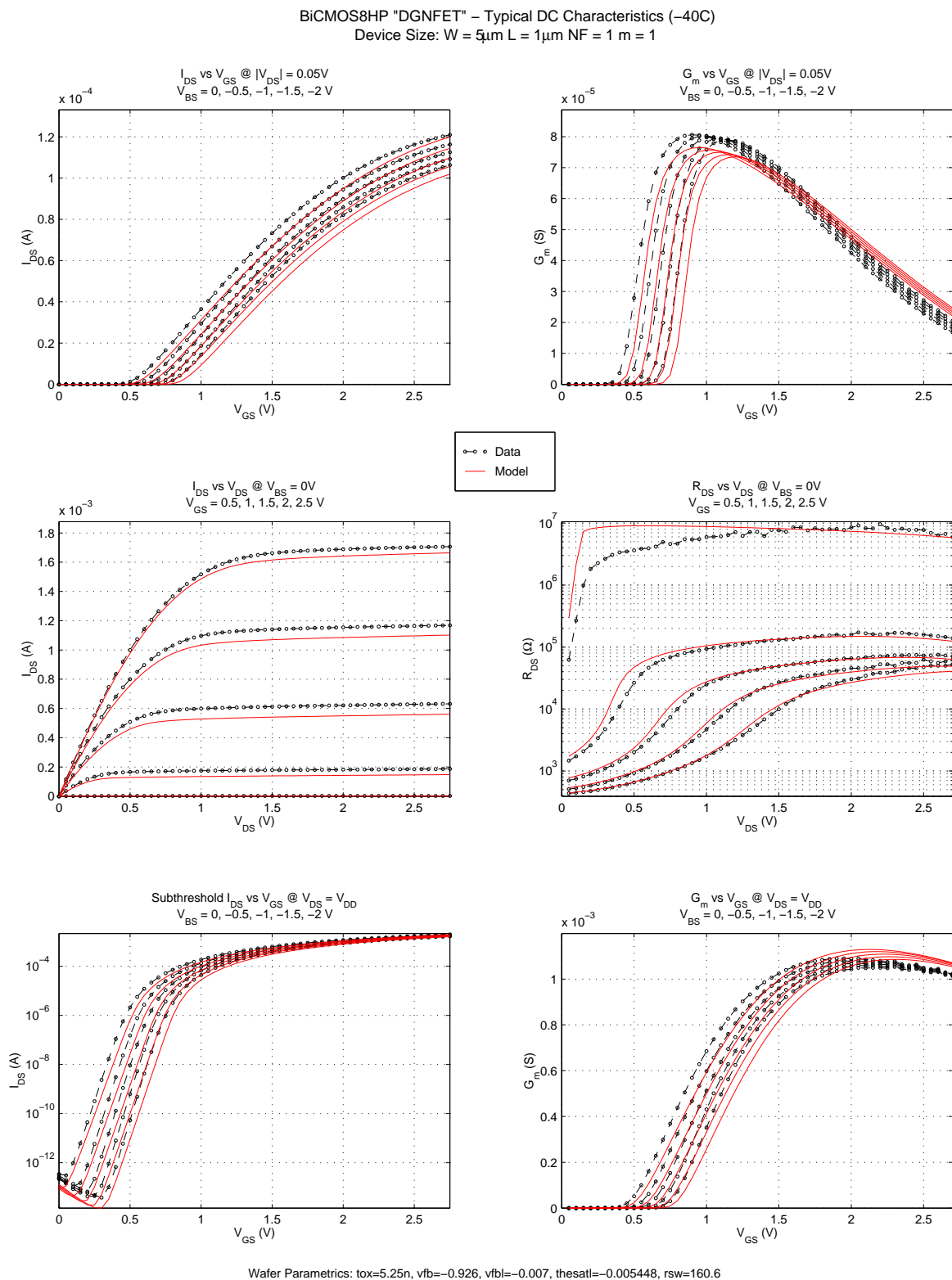


Figure 161. DGNFET DC Characteristics, $5\mu\text{m} \times 4 \times L_{\text{min}}$ (–40C)

BiCMOS8HP "DGPFFET" – Typical DC Characteristics (125C)
Device Size: $W = 5\mu\text{m}$ $L = 1\mu\text{m}$ $NF = 1$ $m = 1$

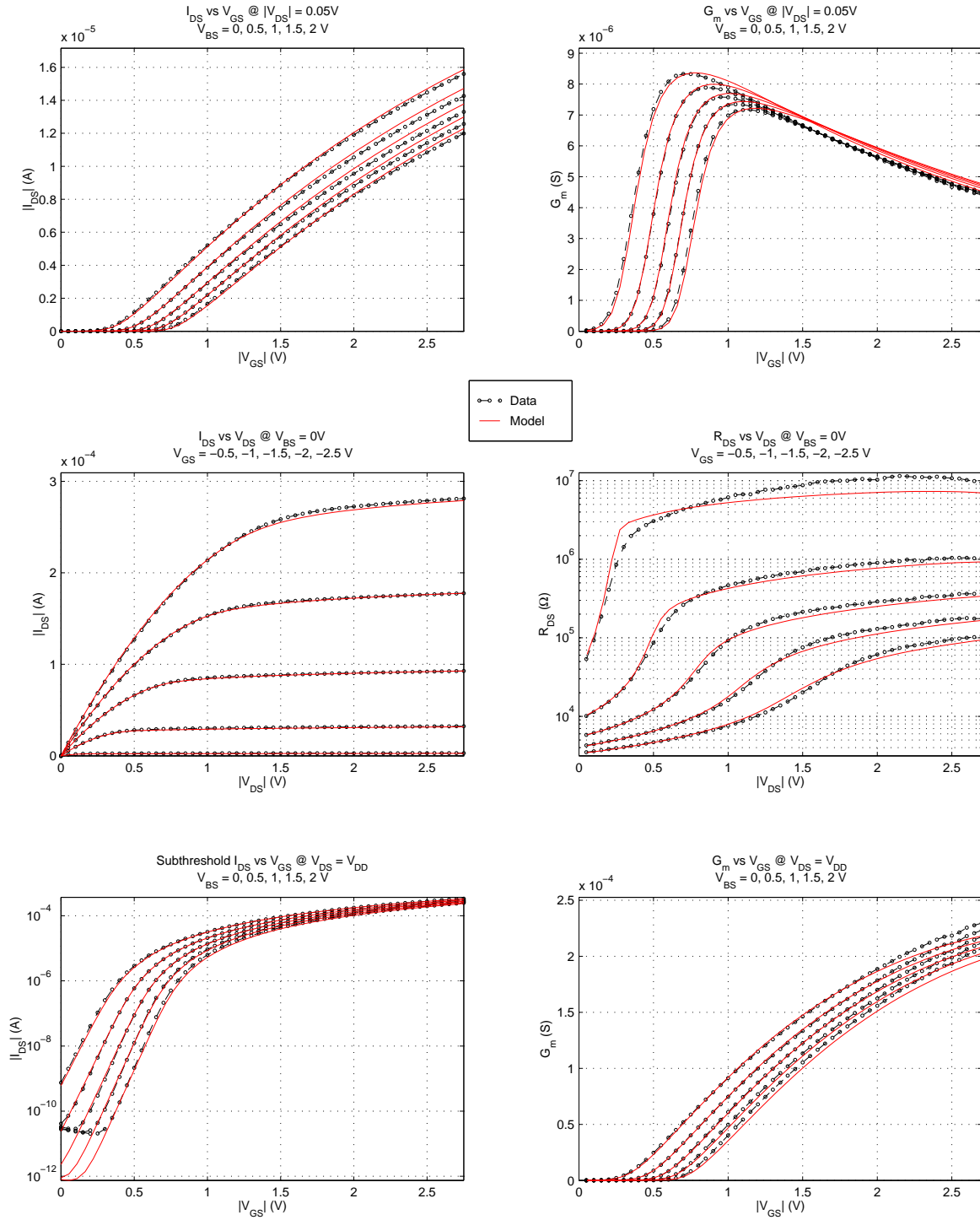


Figure 162. DGPFFET DC Characteristics, $5\mu\text{m} \times 4\text{Lmin}$ (125C)

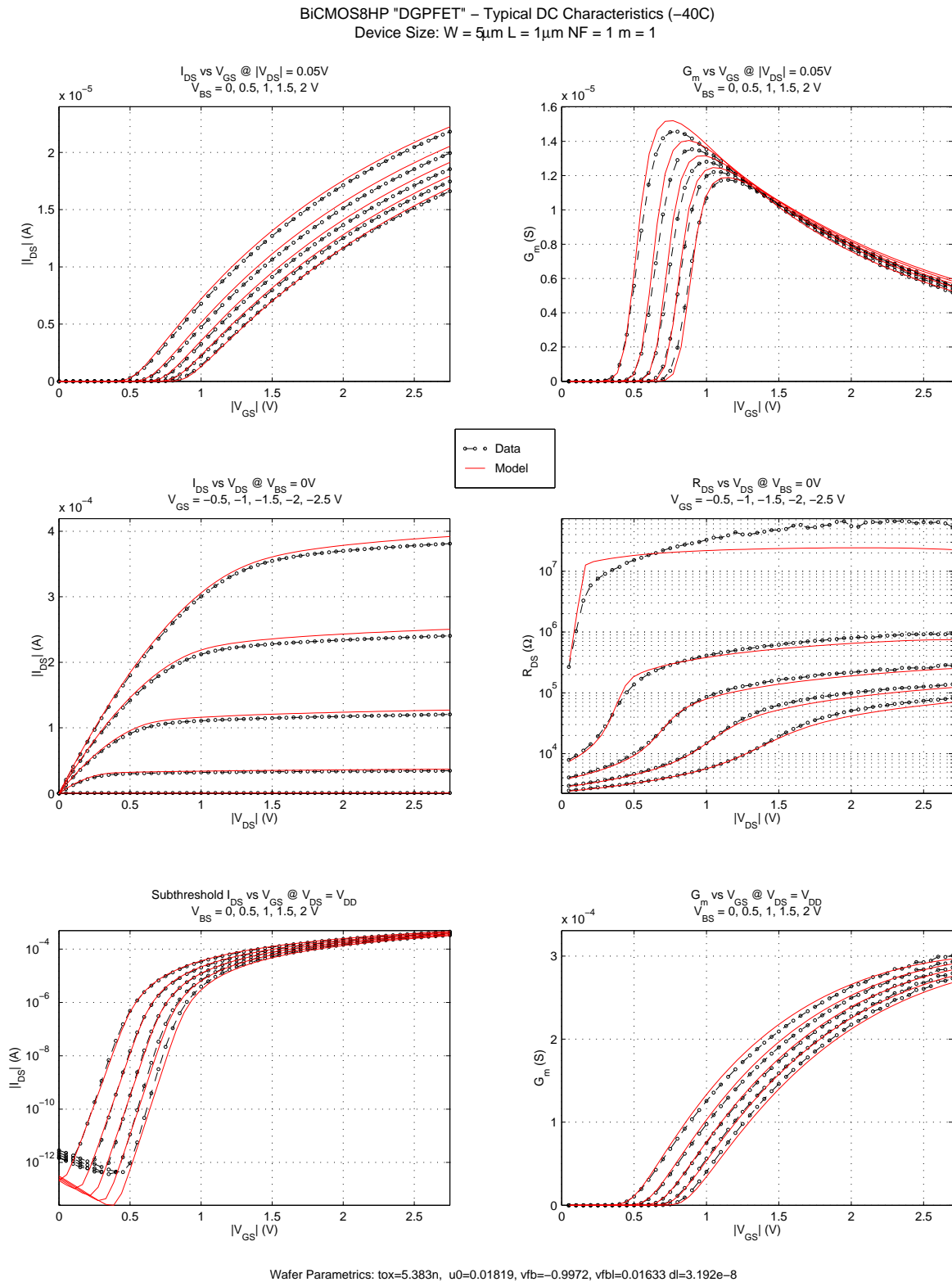


Figure 163. DGPfet DC Characteristics, $5\mu\text{m} \times 4\mu\text{m}$ (–40°C)

BiCMOS8HP "NFET" – Typical Capacitance Characteristics (25C)

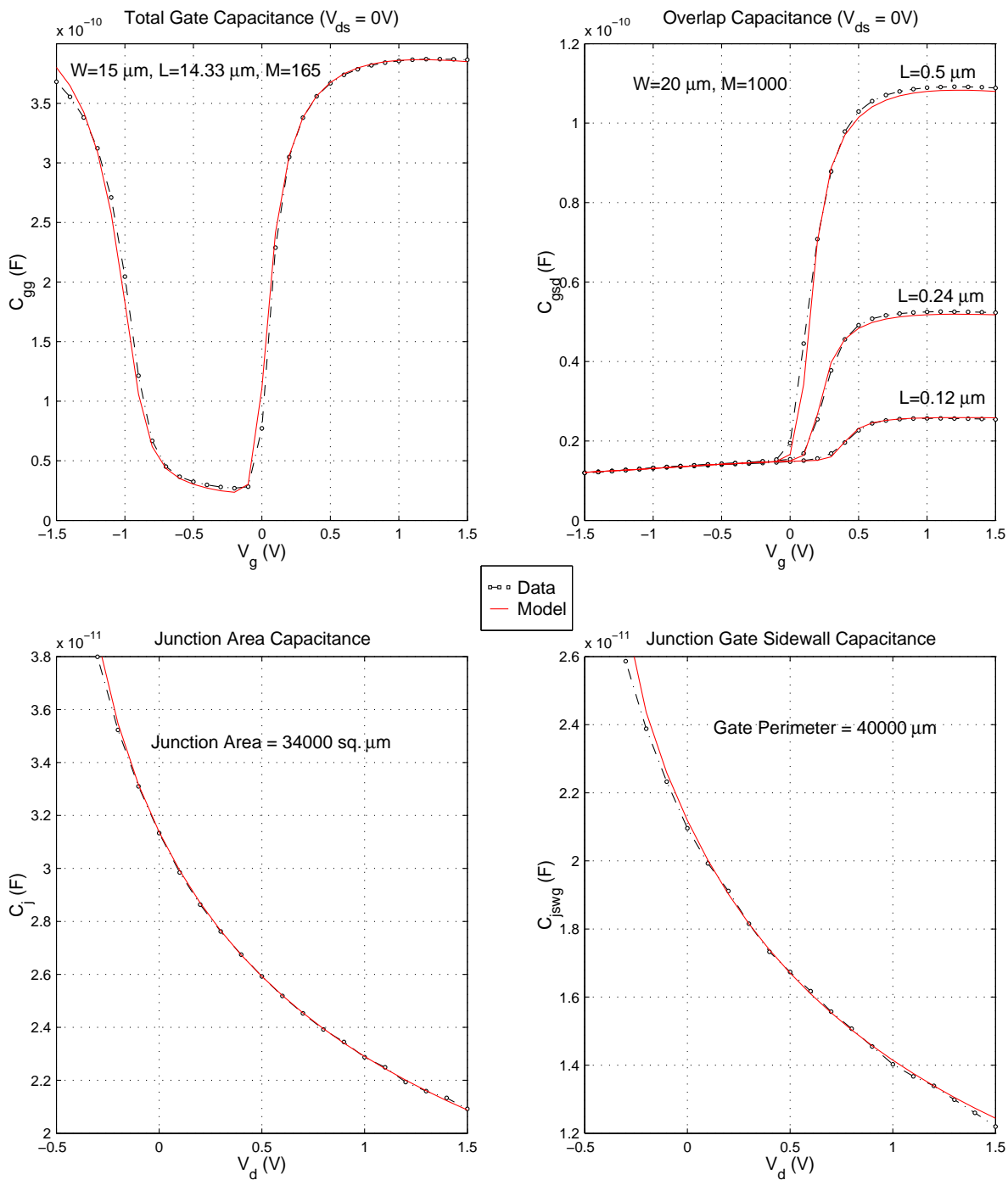


Figure 164. NFET Junction, Overlap and Total Gate Capacitances

BiCMOS8HP "PFET" – Typical Capacitance Characteristics (25C)

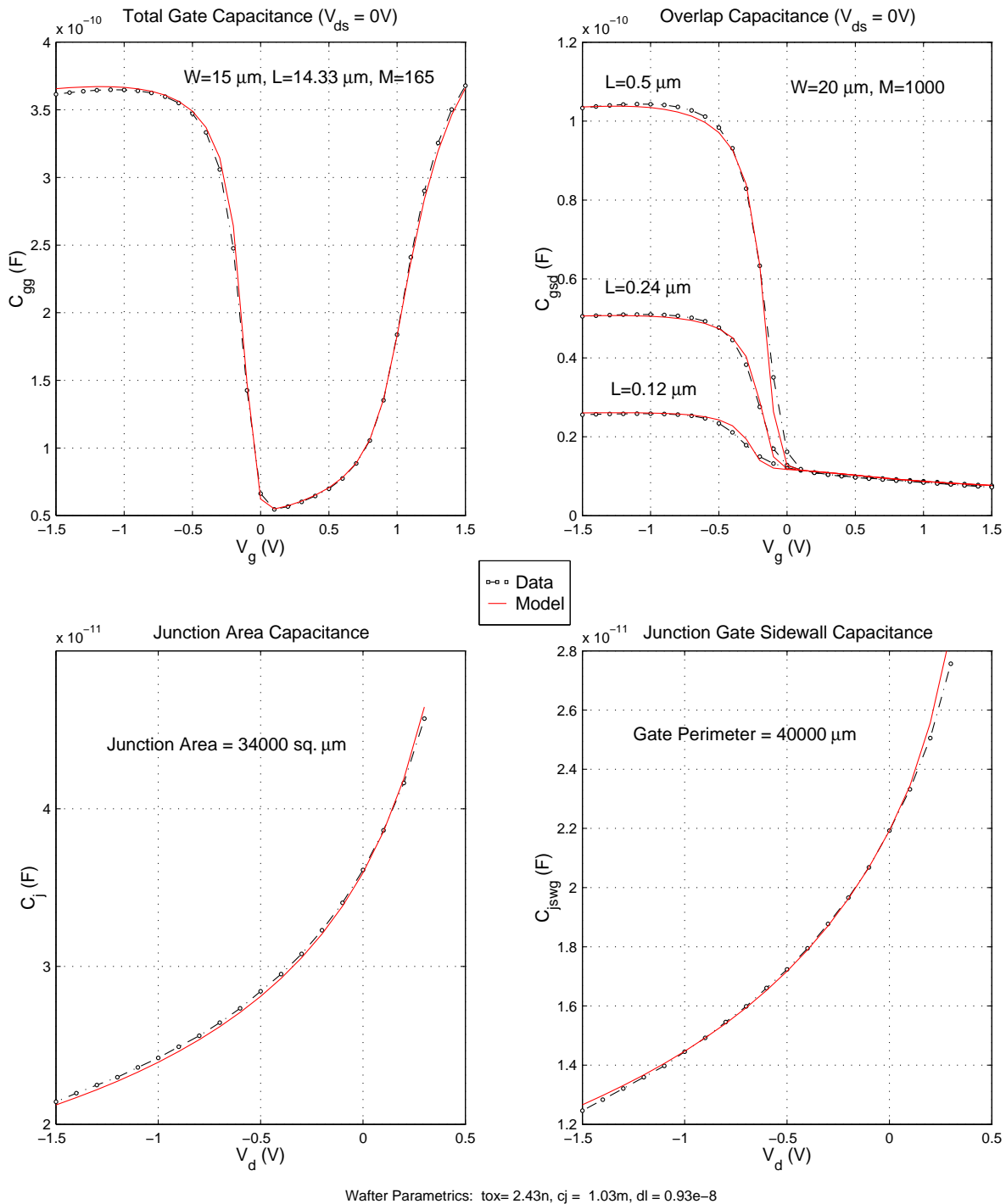
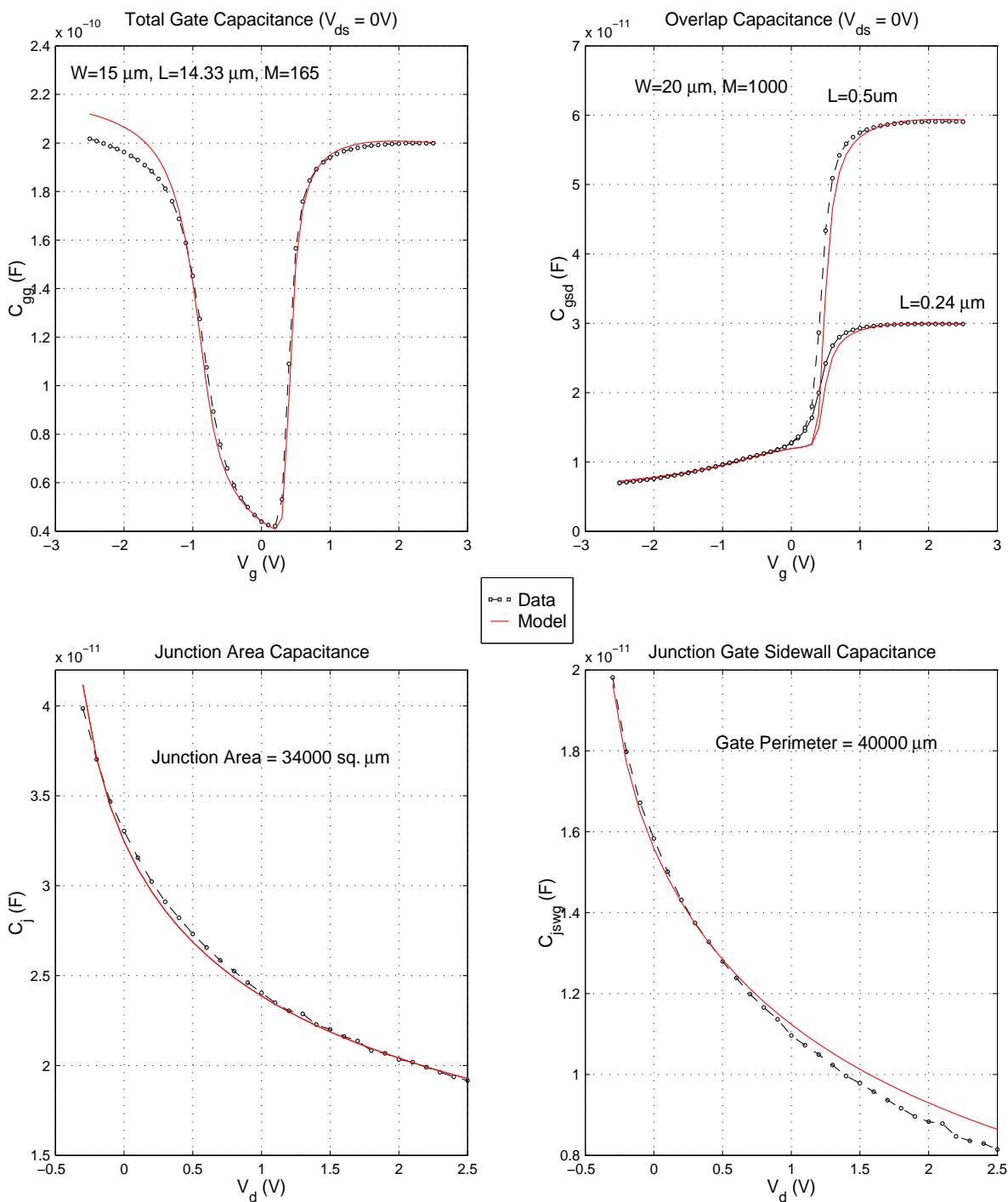


Figure 165. PFET Junction, Overlap and Total Gate Capacitances

BiCMOS8HP "DGNFET" – Typical Capacitance Characteristics (25C)



Wafer Parametrics: $tox=5.25n$, $cj=0.93m$, $cjswg=175p$

Figure 166. DGNFET Junction, Overlap and Total Gate Capacitances

BiCMOS8HP "DGPFET" – Typical Capacitance Characteristics (25C)

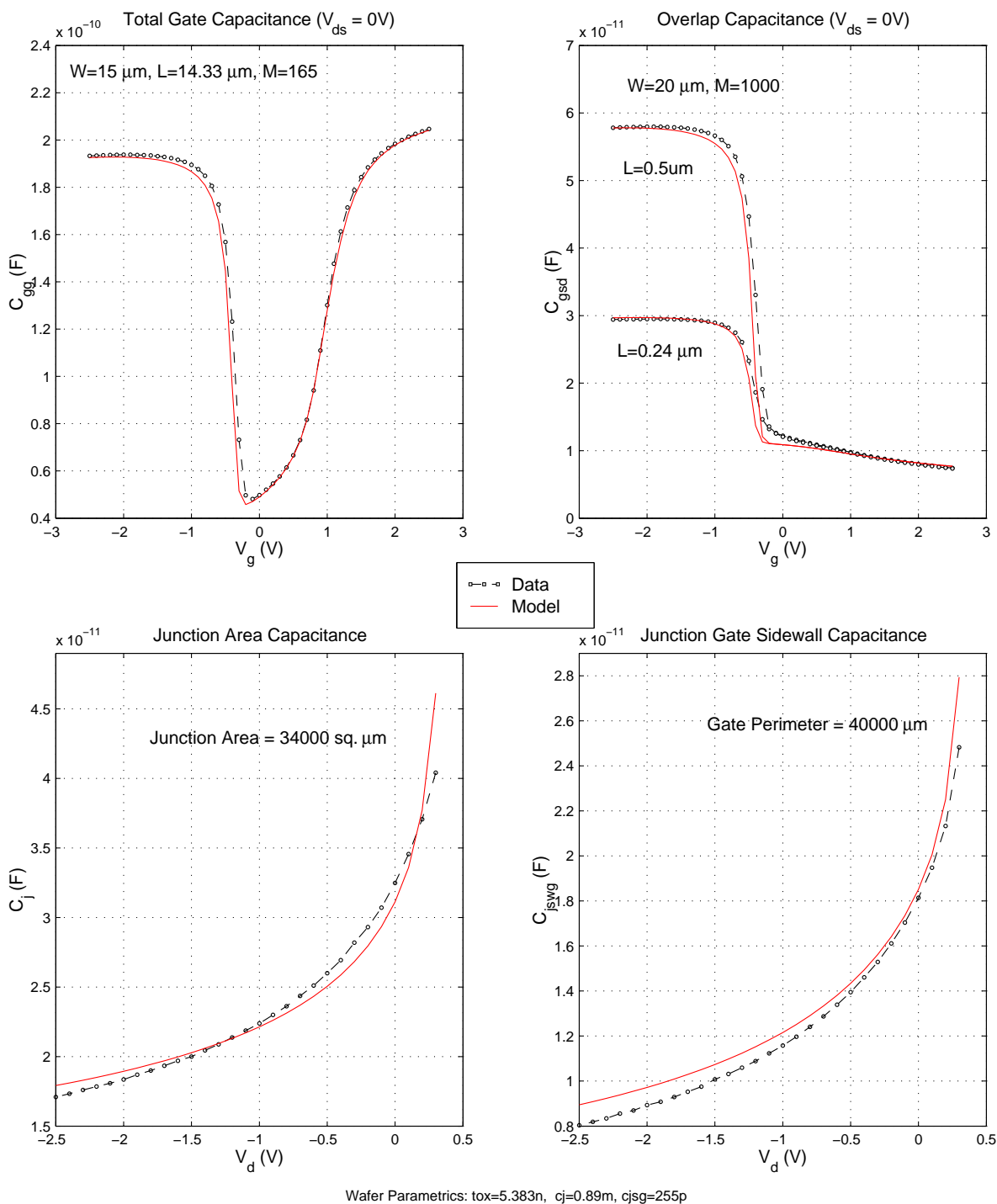


Figure 167. DGPFET Junction, Overlap and Total Gate Capacitances

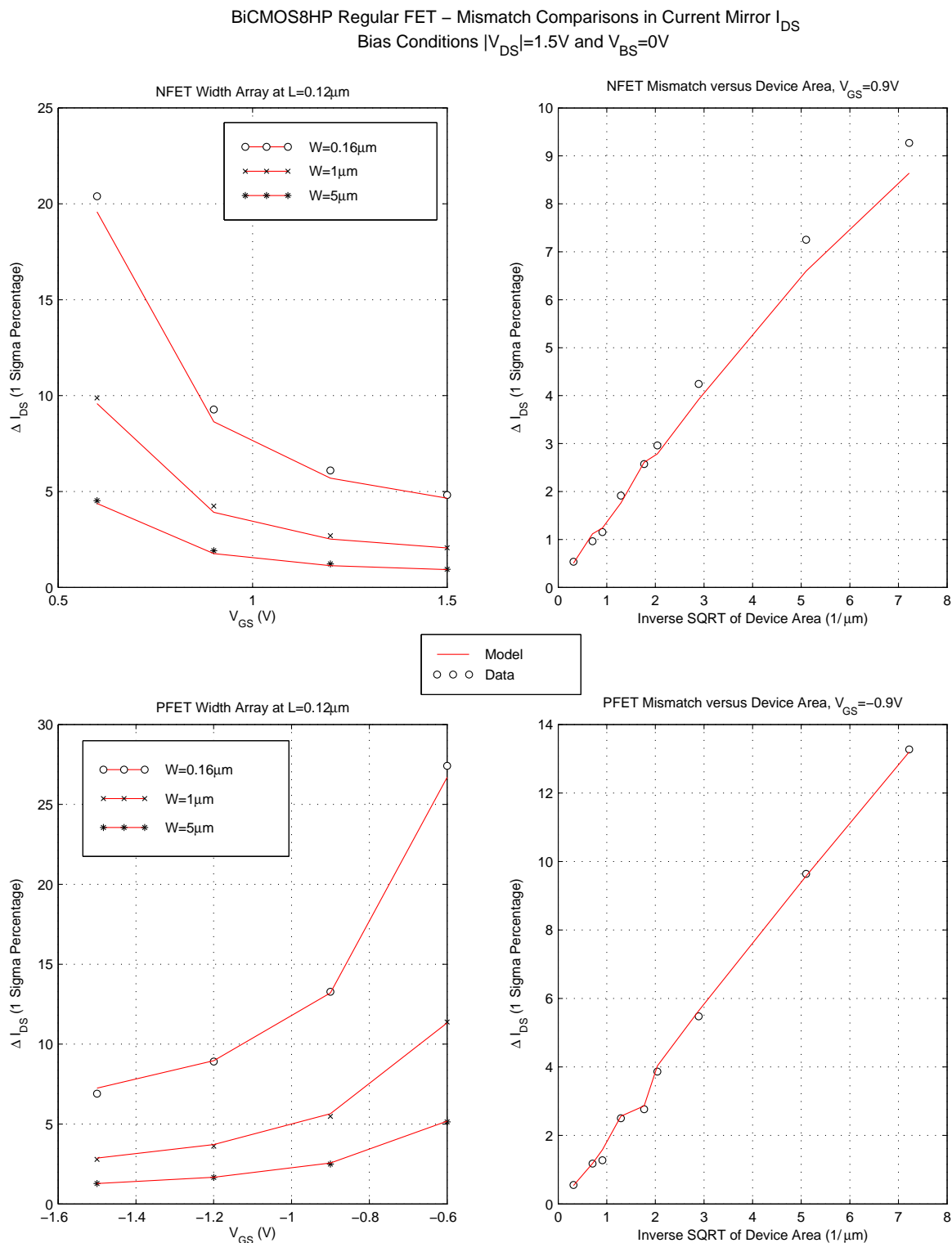


Figure 168. NFET, PFET Mis-match Characteristics

BiCMOS8HP DG FET – Mismatch Comparisons in Current Mirror I_{DS}
Bias Conditions $|V_{DS}| = 2.5V$ and $V_{BS} = 0V$

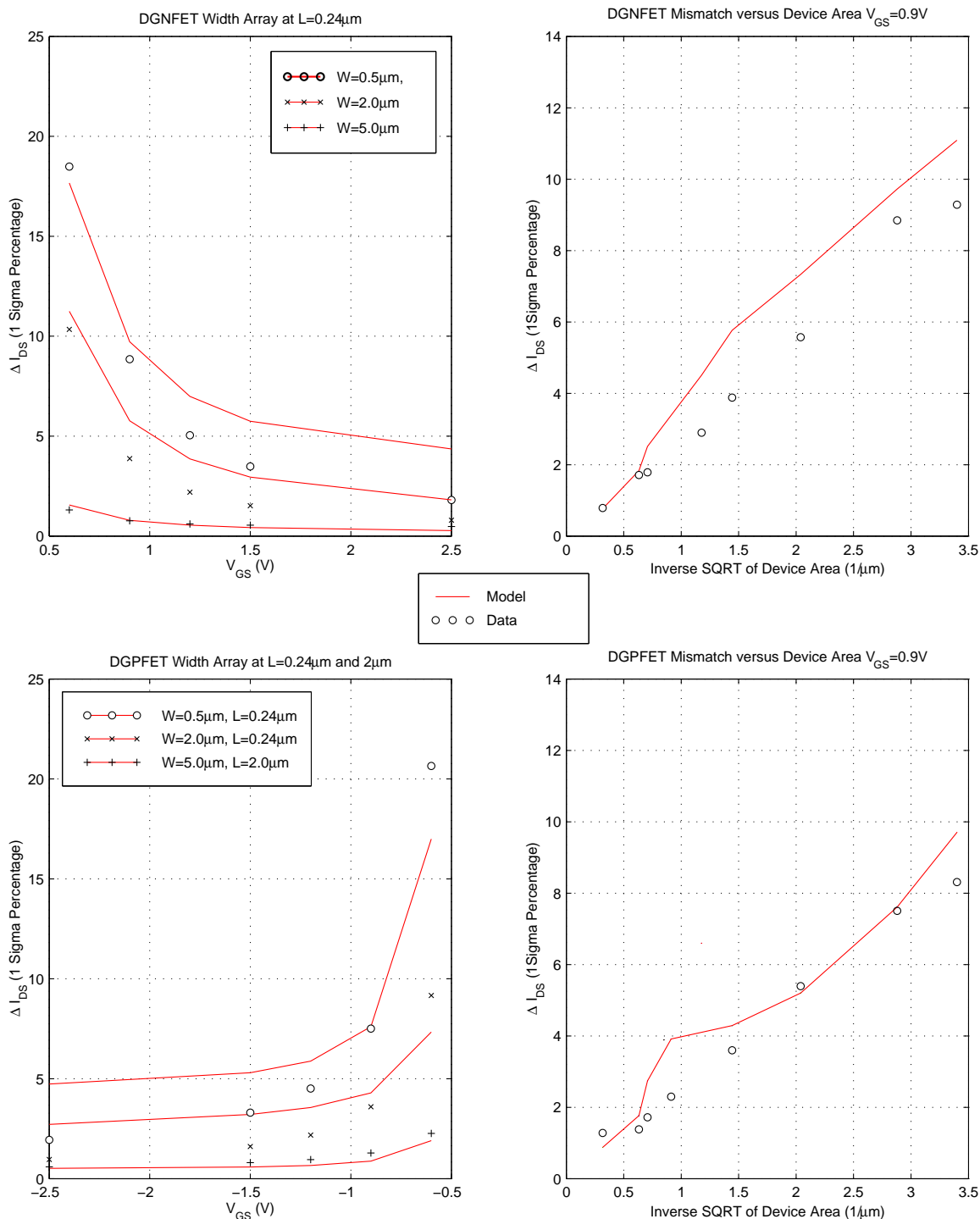


Figure 169. DGNFET, DGPFET Mis-match Characteristics

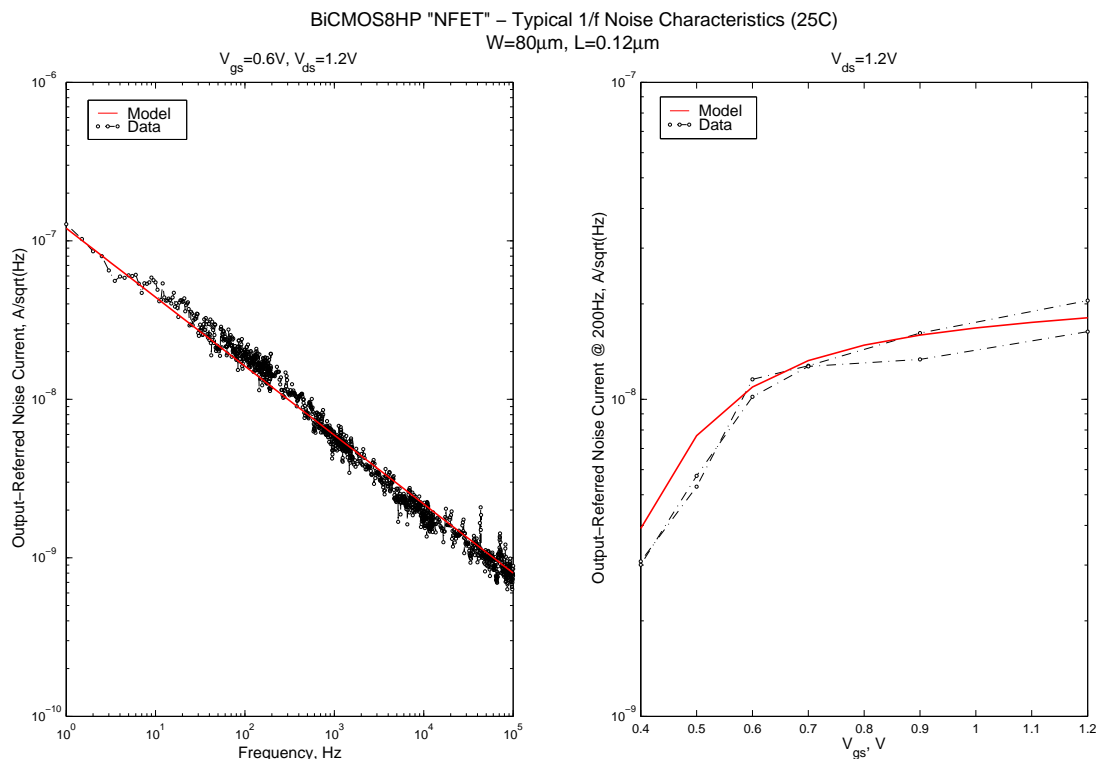


Figure 170. NFET Flicker Noise Correlation for W= 80 μ m and L=0.12 μ m

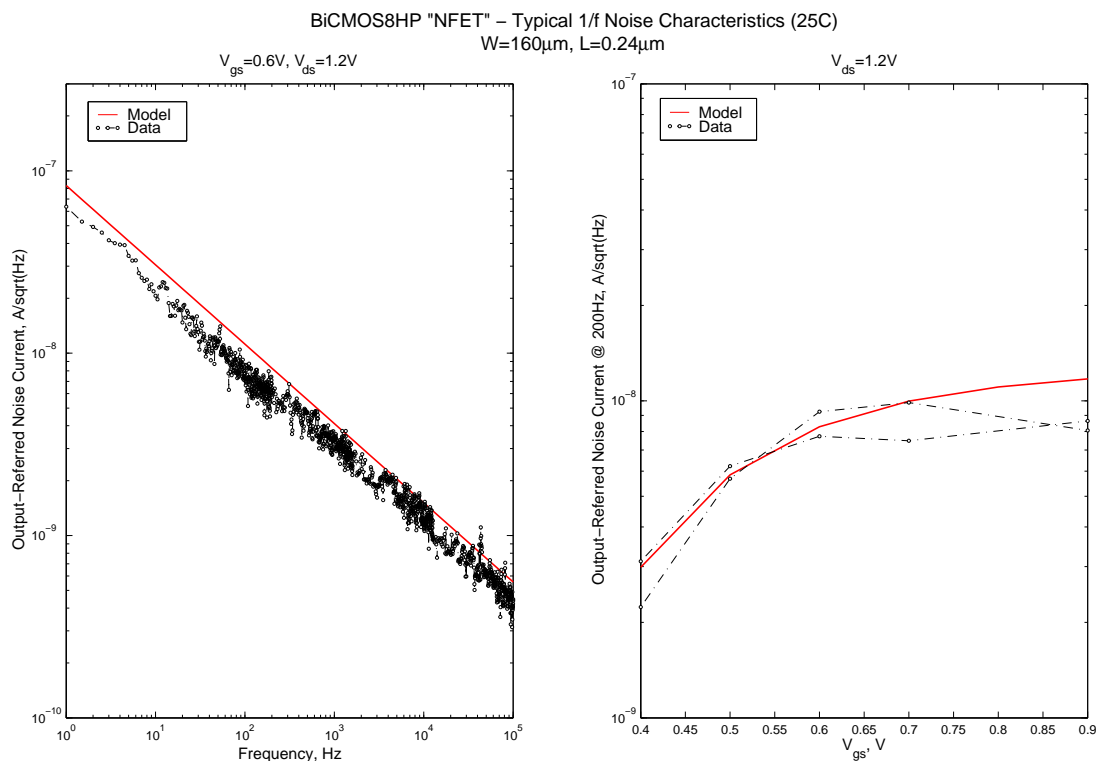


Figure 171. NFET Flicker Noise Correlation for W= 160 μ m and L=0.24 μ m

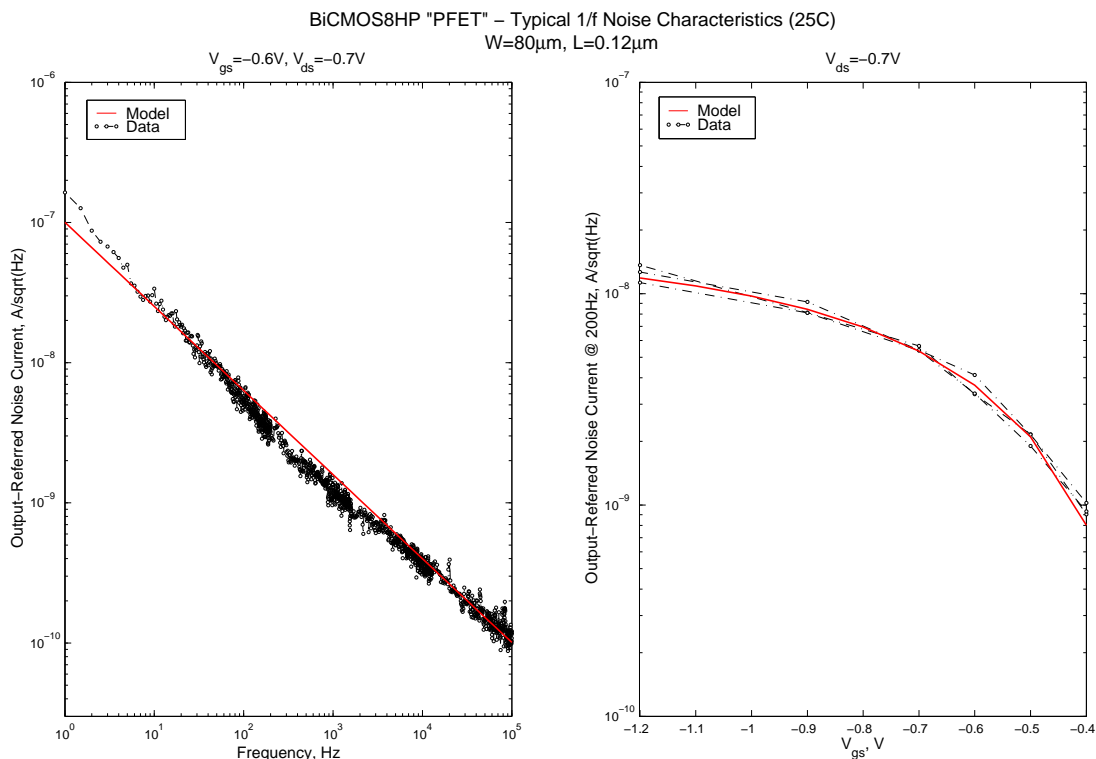


Figure 172. PFET Flicker Noise Correlation for W= 80 μ m and L=0.12 μ m

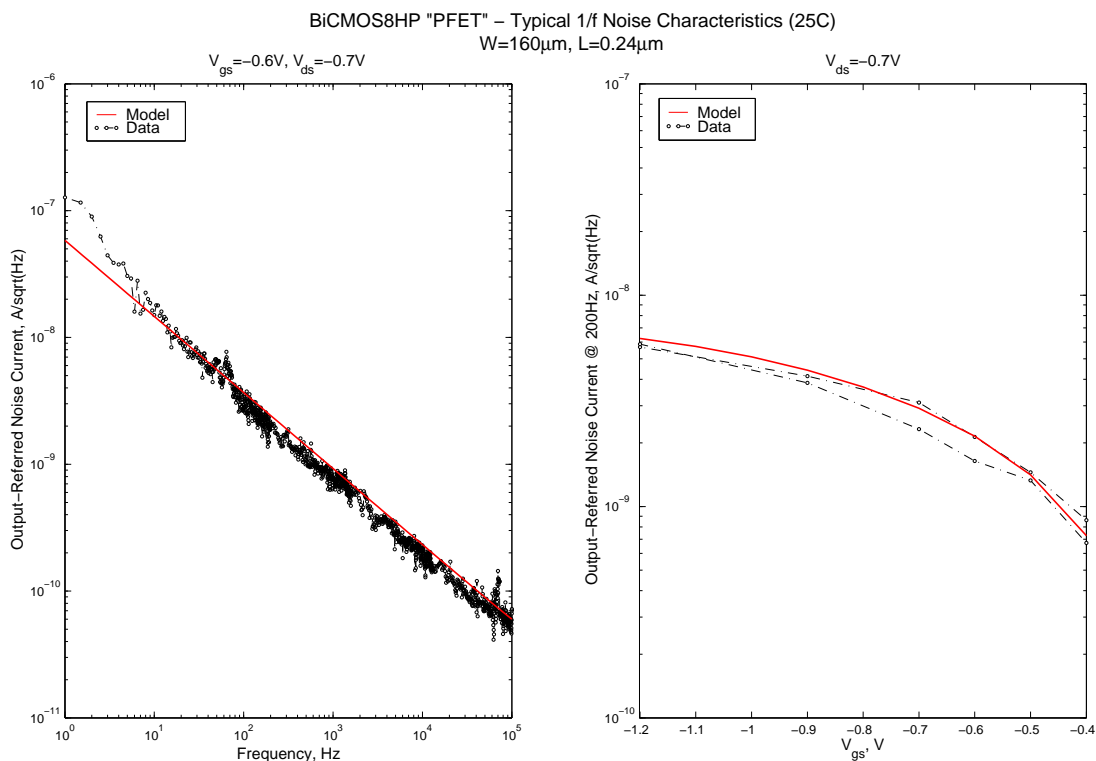


Figure 173. PFET Flicker Noise Correlation for W= 160 μ m and L=0.24 μ m

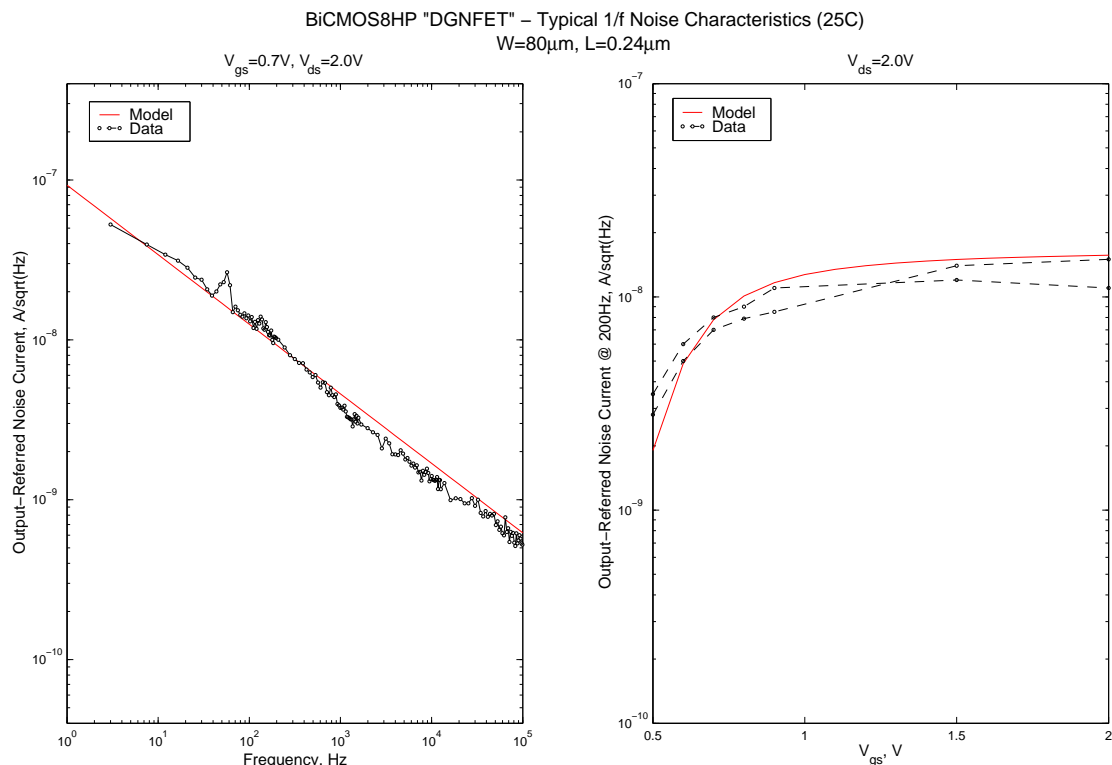


Figure 174. DGNFET Flicker Noise Correlation for W= 80μm and L=0.24μm

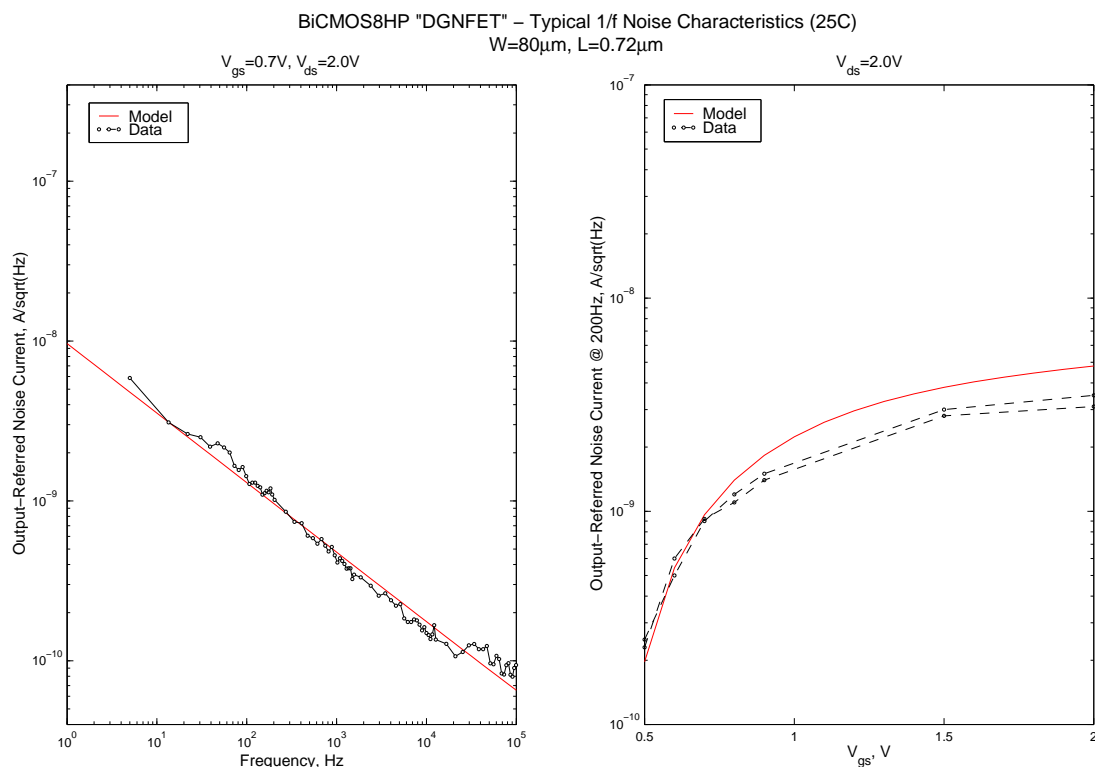


Figure 175. DGNFET Flicker Noise Correlation for W= 80μm and L=0.72μm

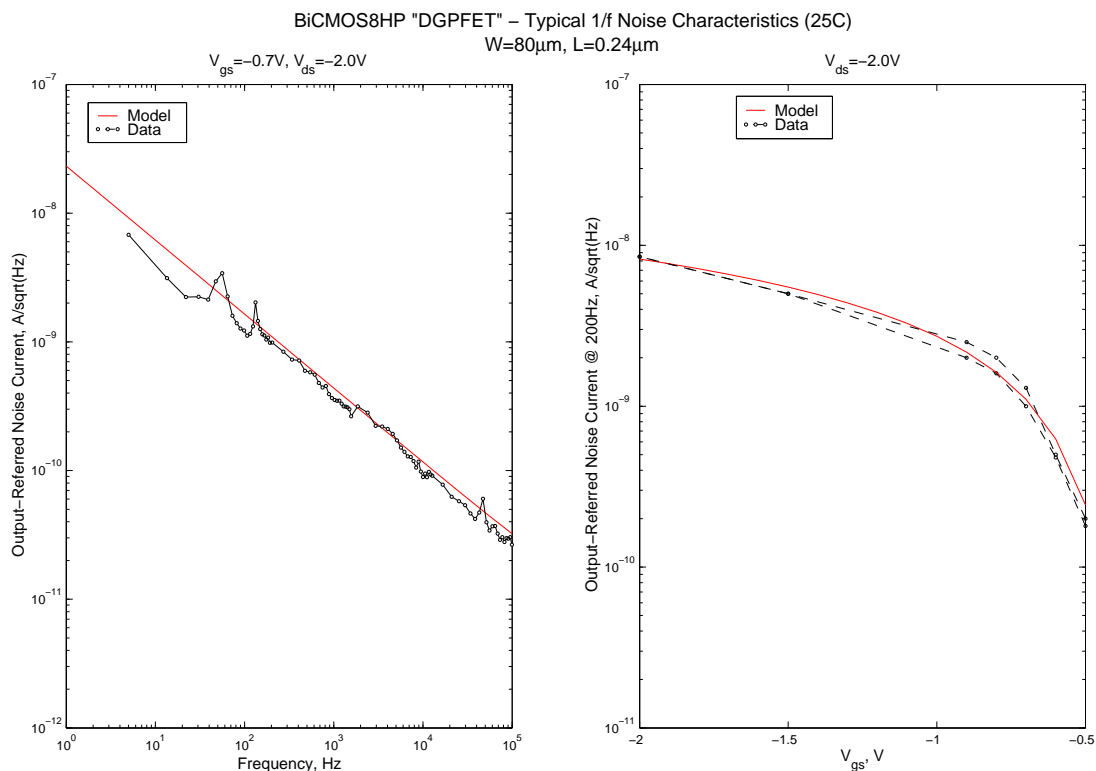


Figure 176. DGPfet Flicker Noise Correlation for W= 80 μ m and L=0.24 μ m

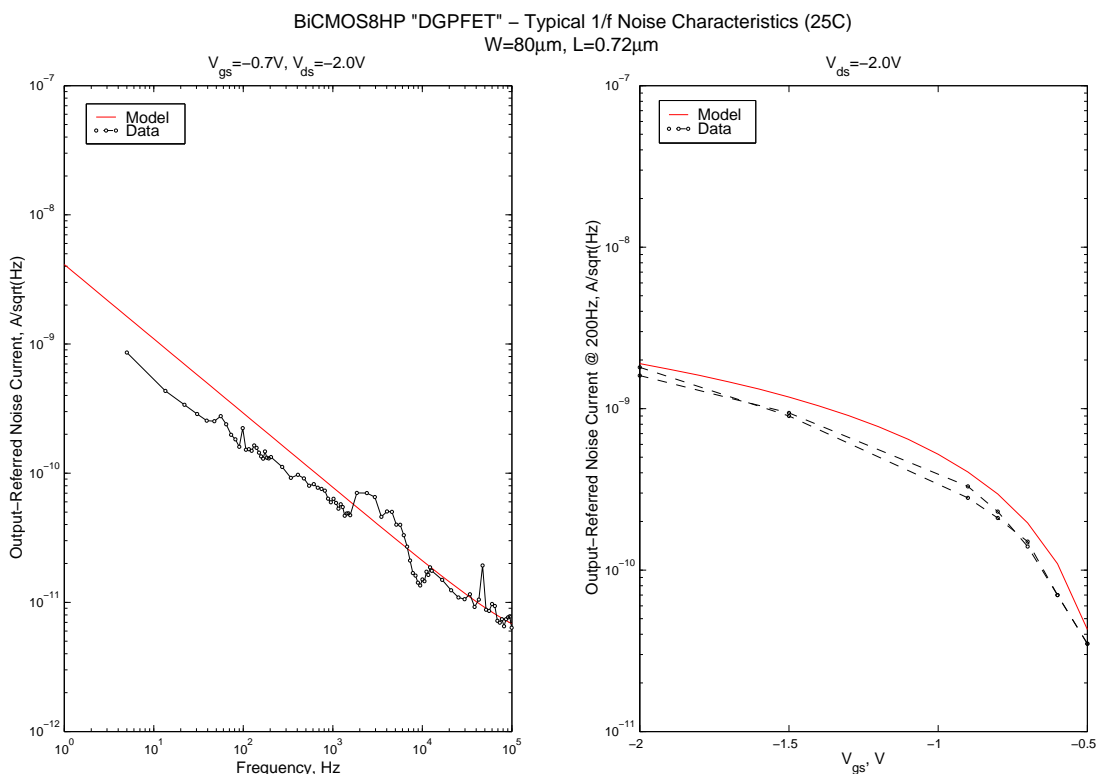


Figure 177. DGPfet Flicker Noise Correlation for W= 80 μ m and L=0.72 μ m

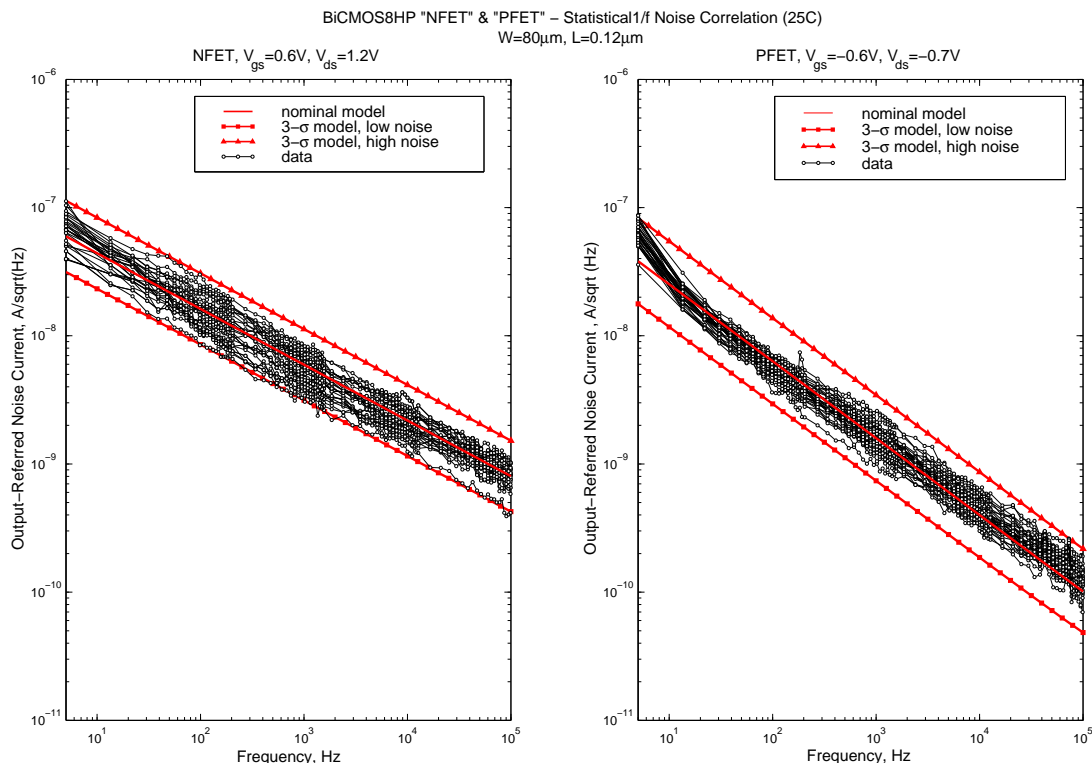


Figure 178. NFET and PFET Statistical Flicker Noise Correlation

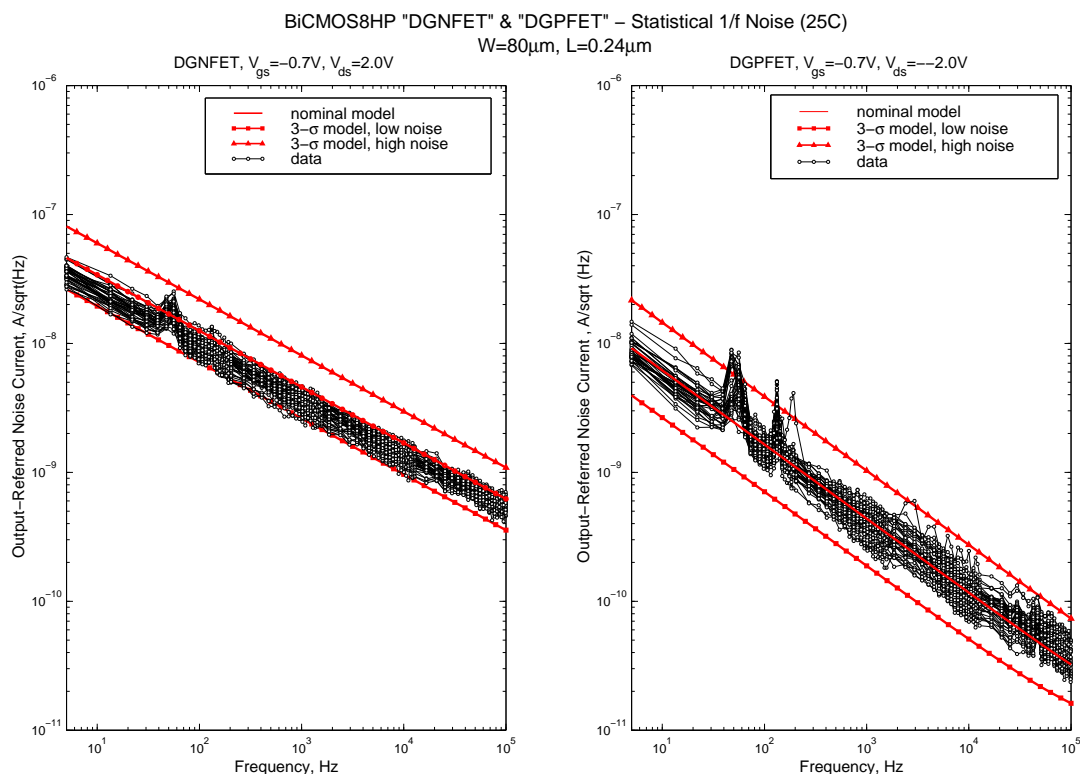


Figure 179. DGNFET and DGPFET Statistical Flicker Noise Correlation

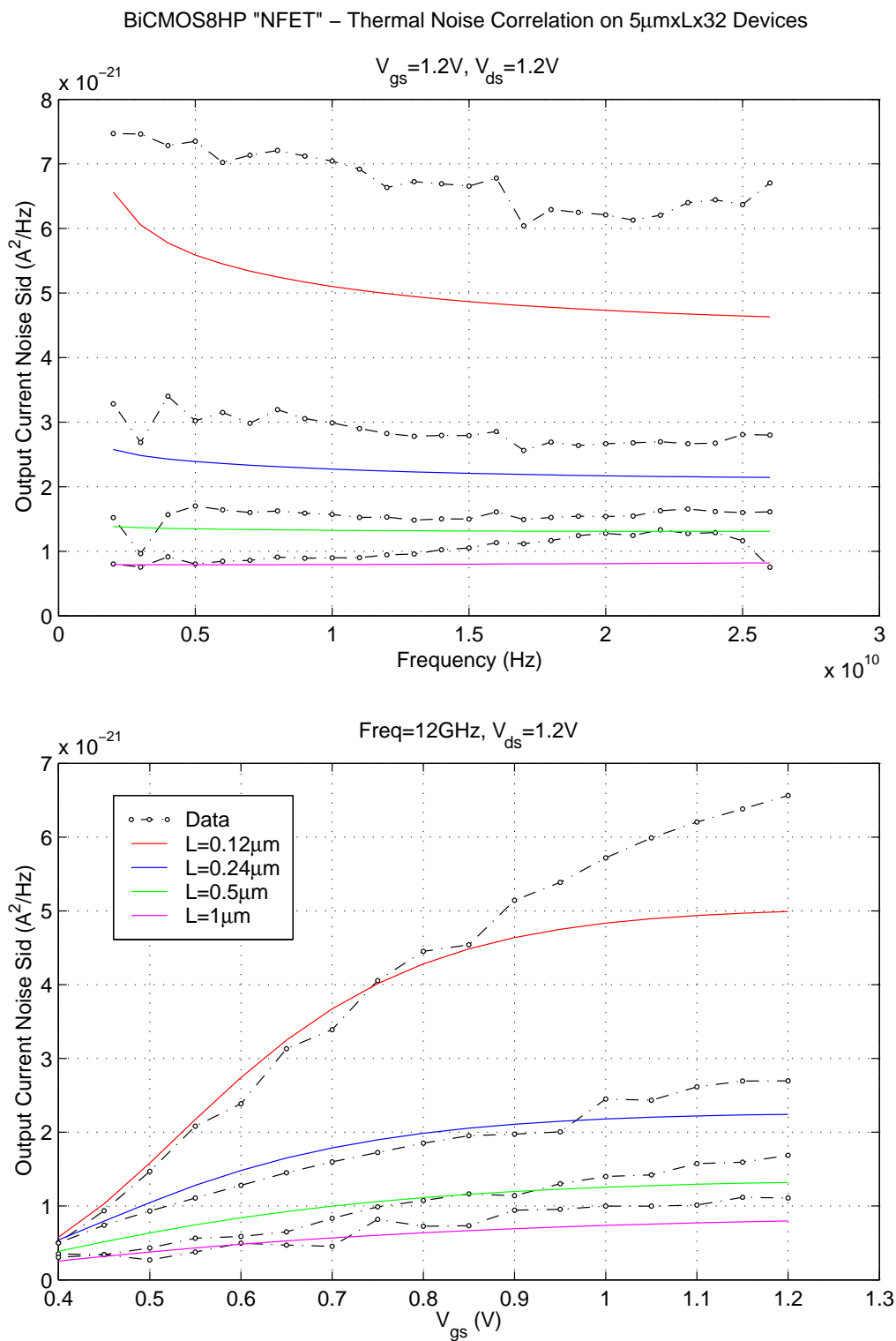


Figure 180. NFET Thermal Noise Correlation (25C)

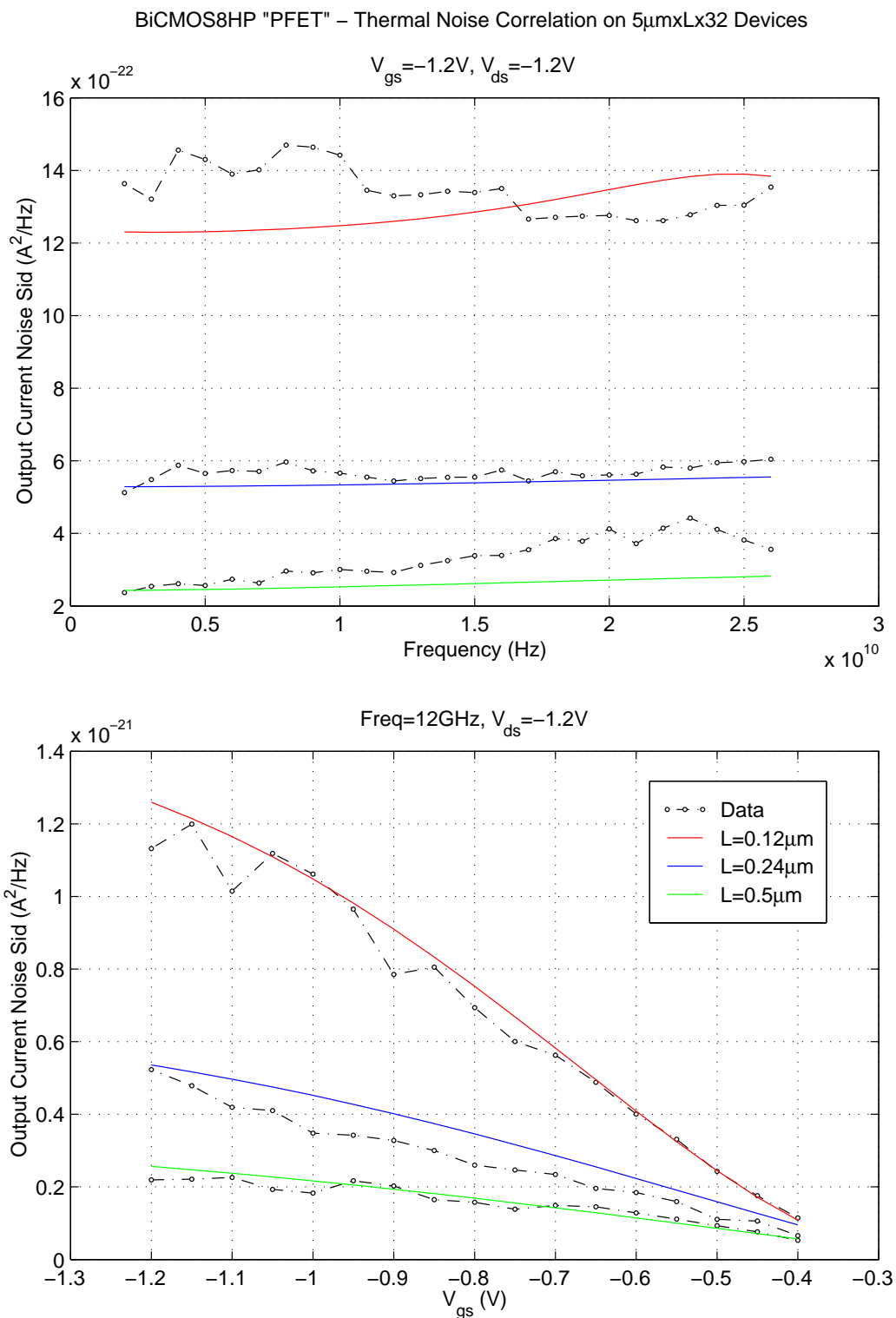


Figure 181. PFET Thermal Noise Correlation (25C)

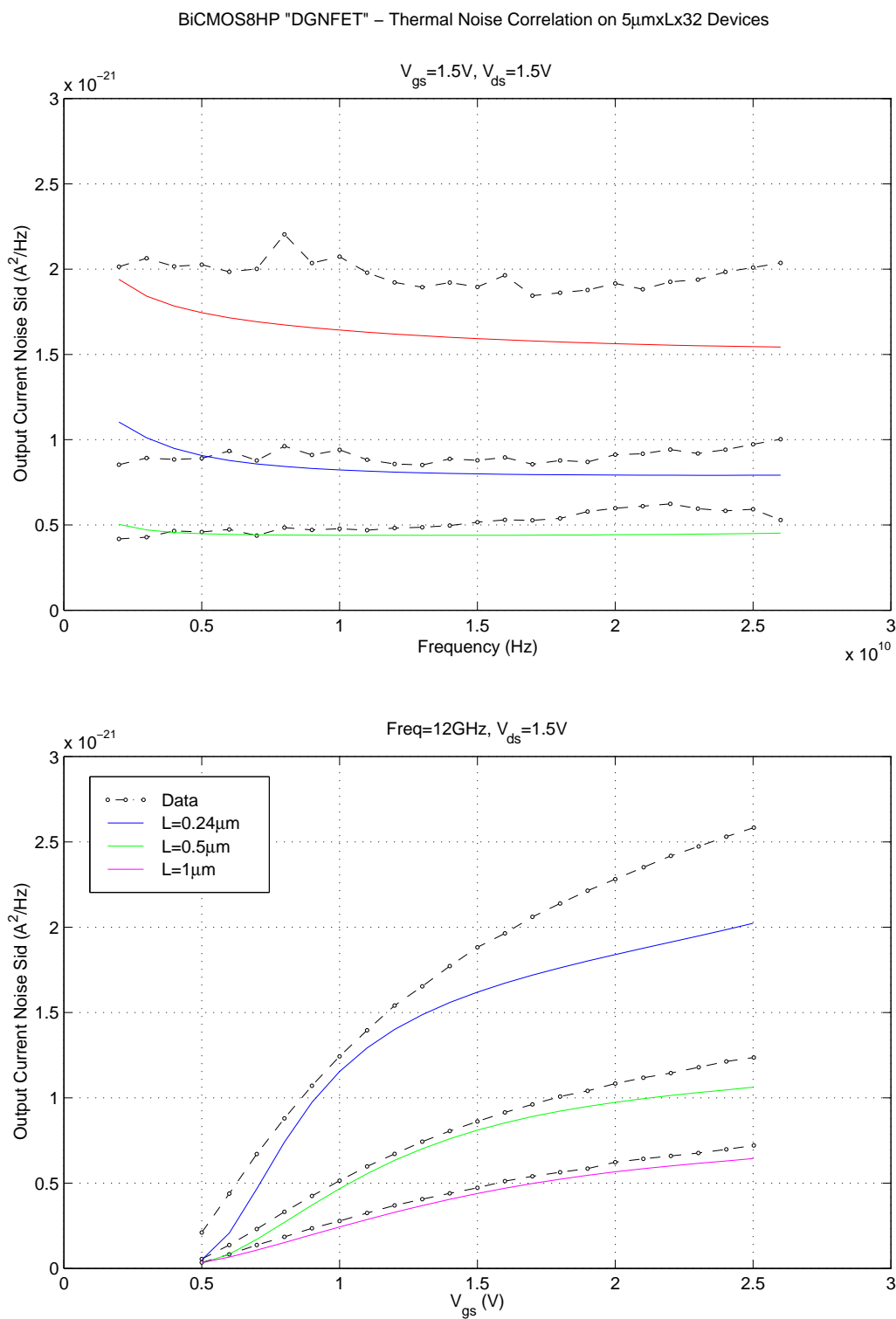


Figure 182. DGNFET Thermal Noise Correlation (25C)

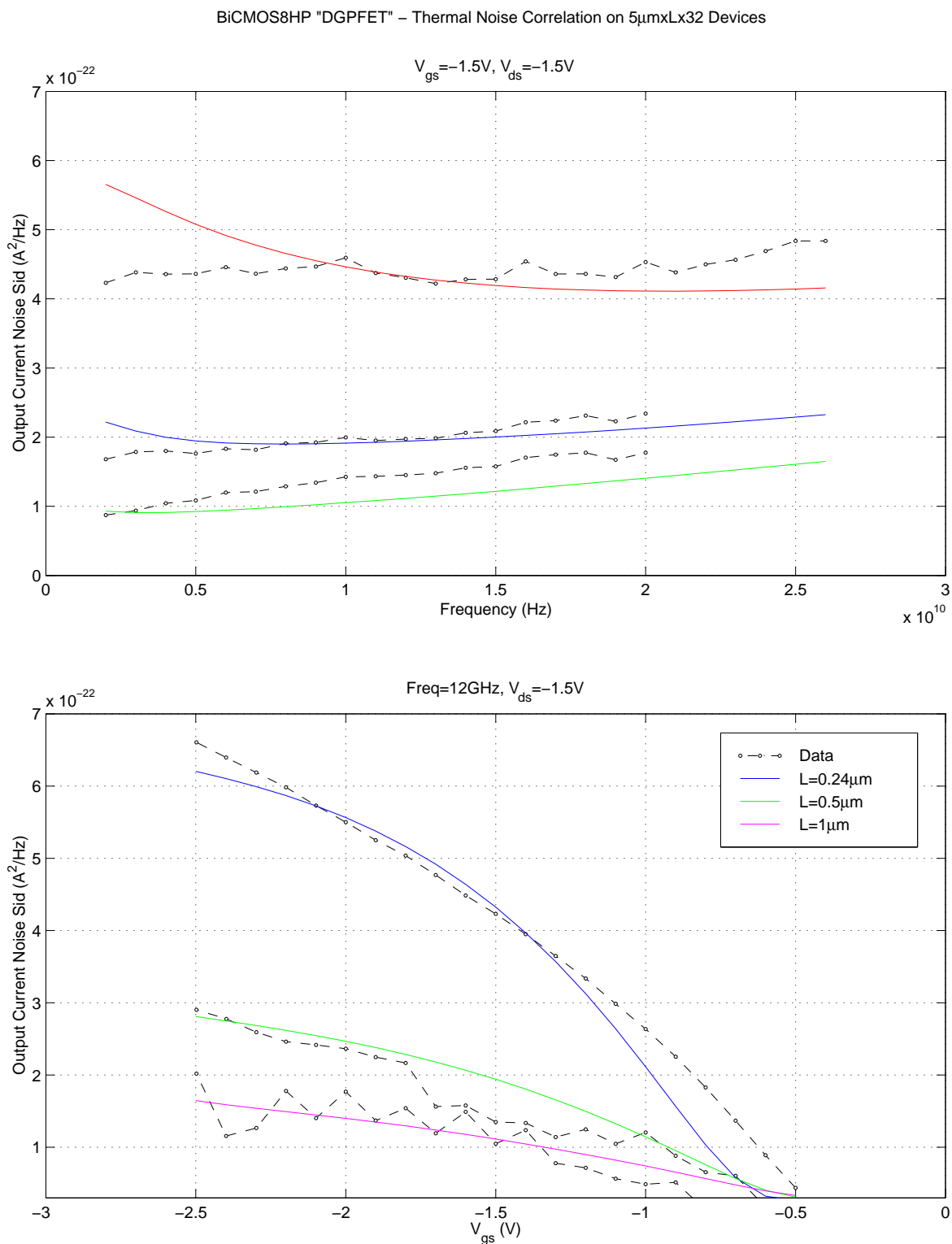


Figure 183. DGPFET Thermal Noise Correlation (25C)

BiCMOS8HP "NFET" – Typical S-Parameter Characteristics (25C)
Device Size: $W = 4\mu\text{m}$ $L = 0.12\mu\text{m}$ $NF = 8$

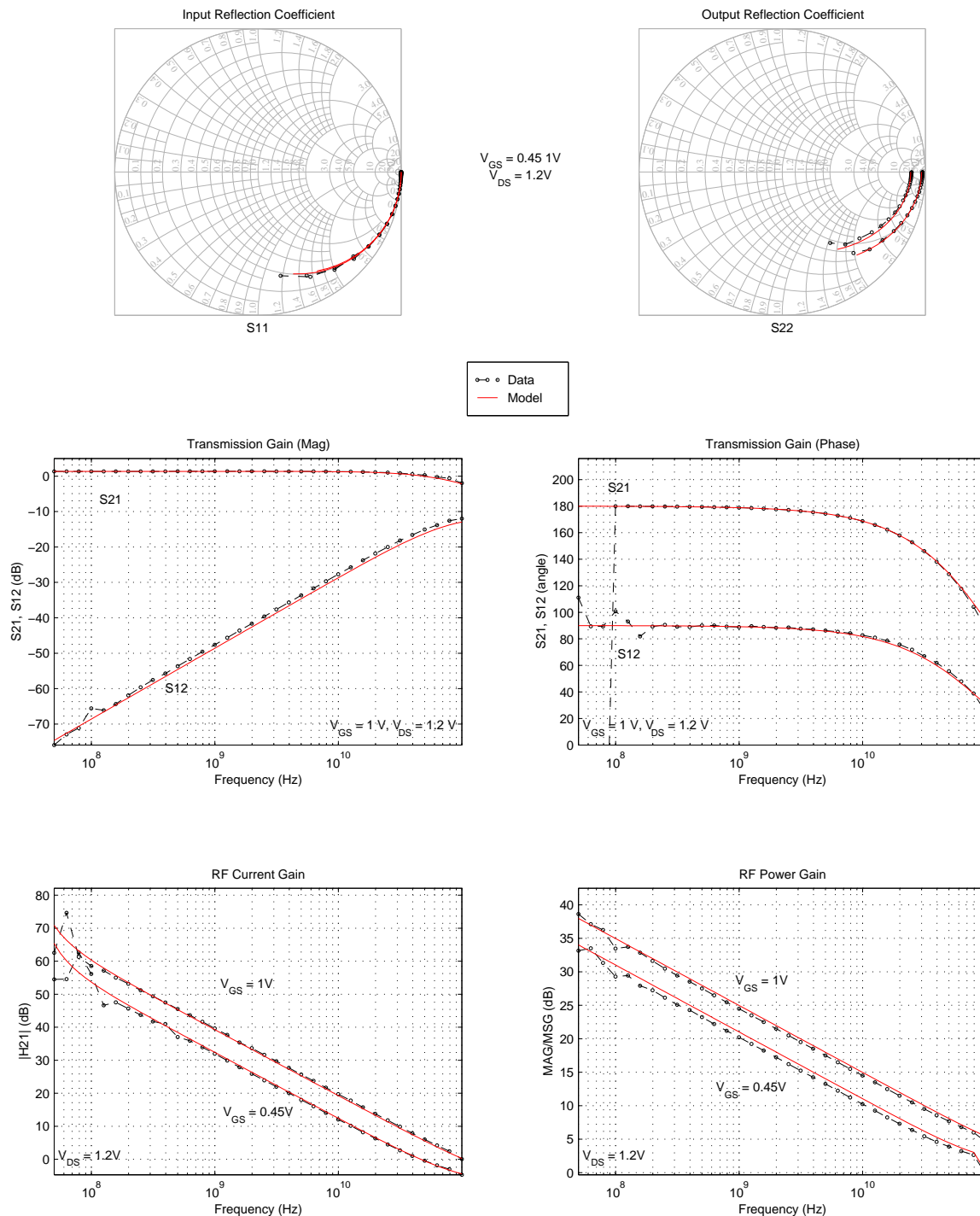
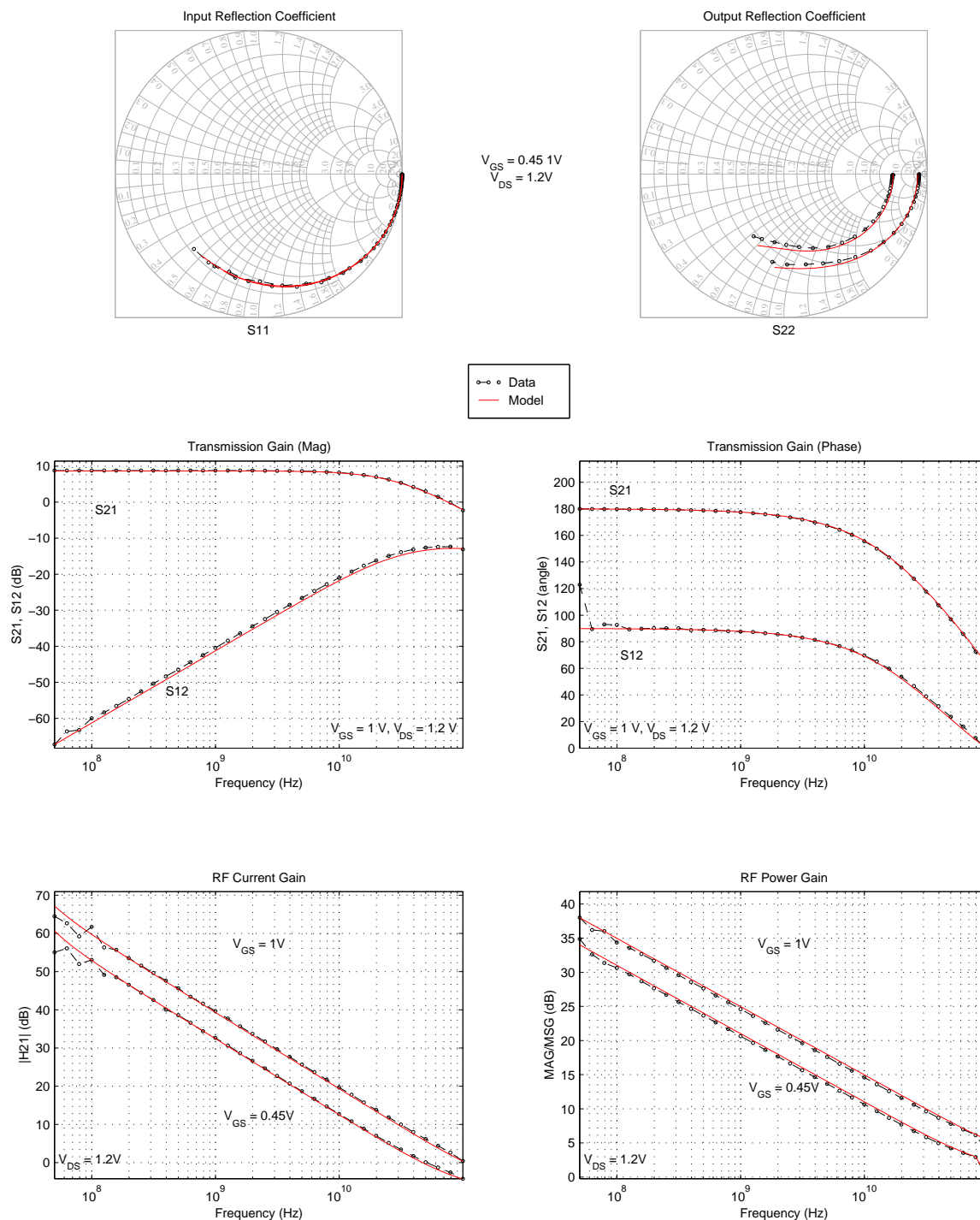


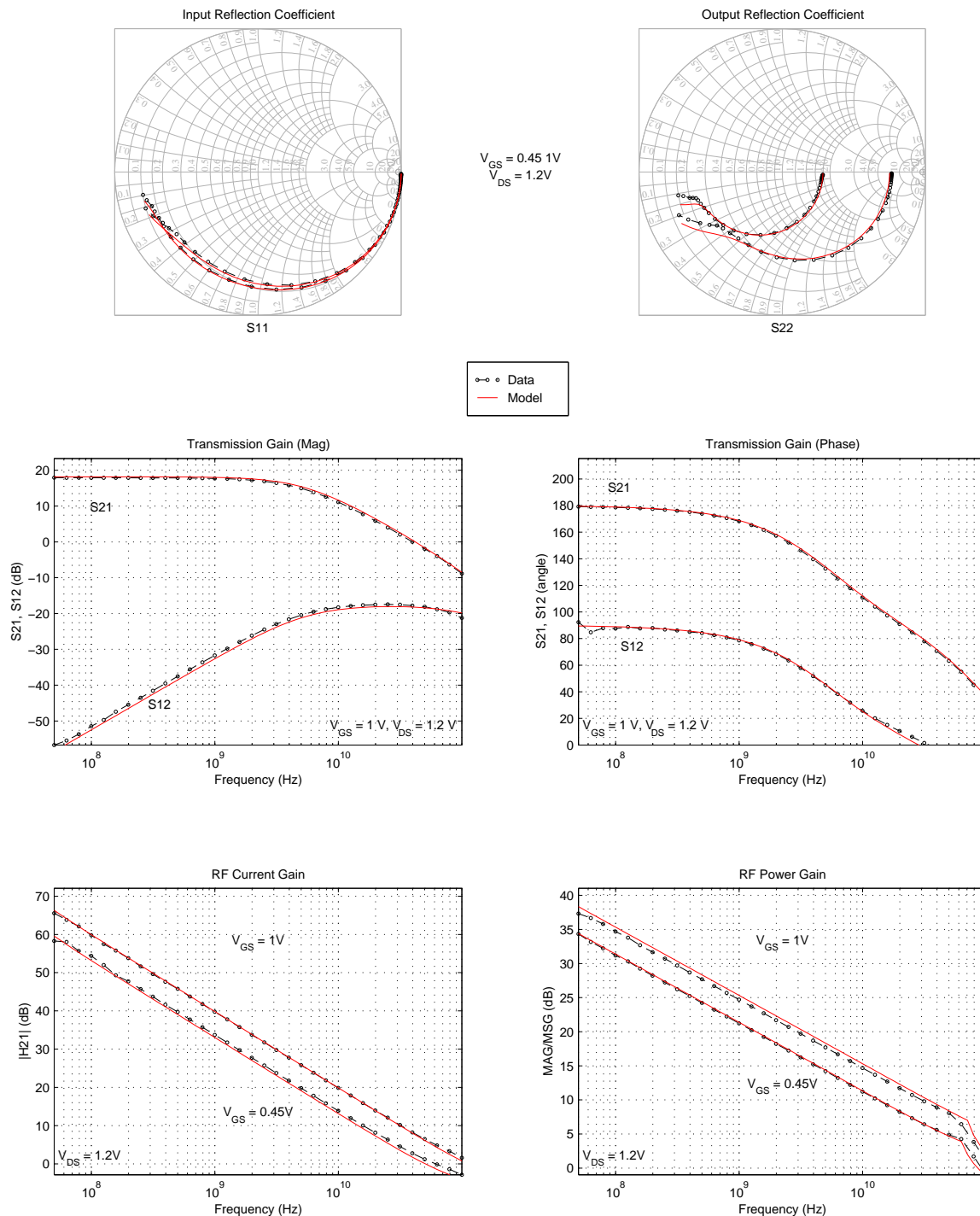
Figure 184. NFET S-Parameter Characteristics, $2\mu\text{m} \times L_{min} \times 8$

$$\begin{aligned} V_{GS} &= 0.45 \text{ V} \\ V_{DS} &= 1.2 \text{ V} \end{aligned}$$


Wafer Parametrics: uo=0.094, toxo=2.64n, cfl=3.5e-5, wint=0.01u, thesatl=1.12, rsw=60, dl=1.68e-8, cj=0.9m, dlq=-4e-8
nsubo=9.57e22, fol1=25.75m, fol2=1.06m, vfbw=-0.8m, iqinlw=50.5, iqovw=6.9

Version Date: December 9, 2011

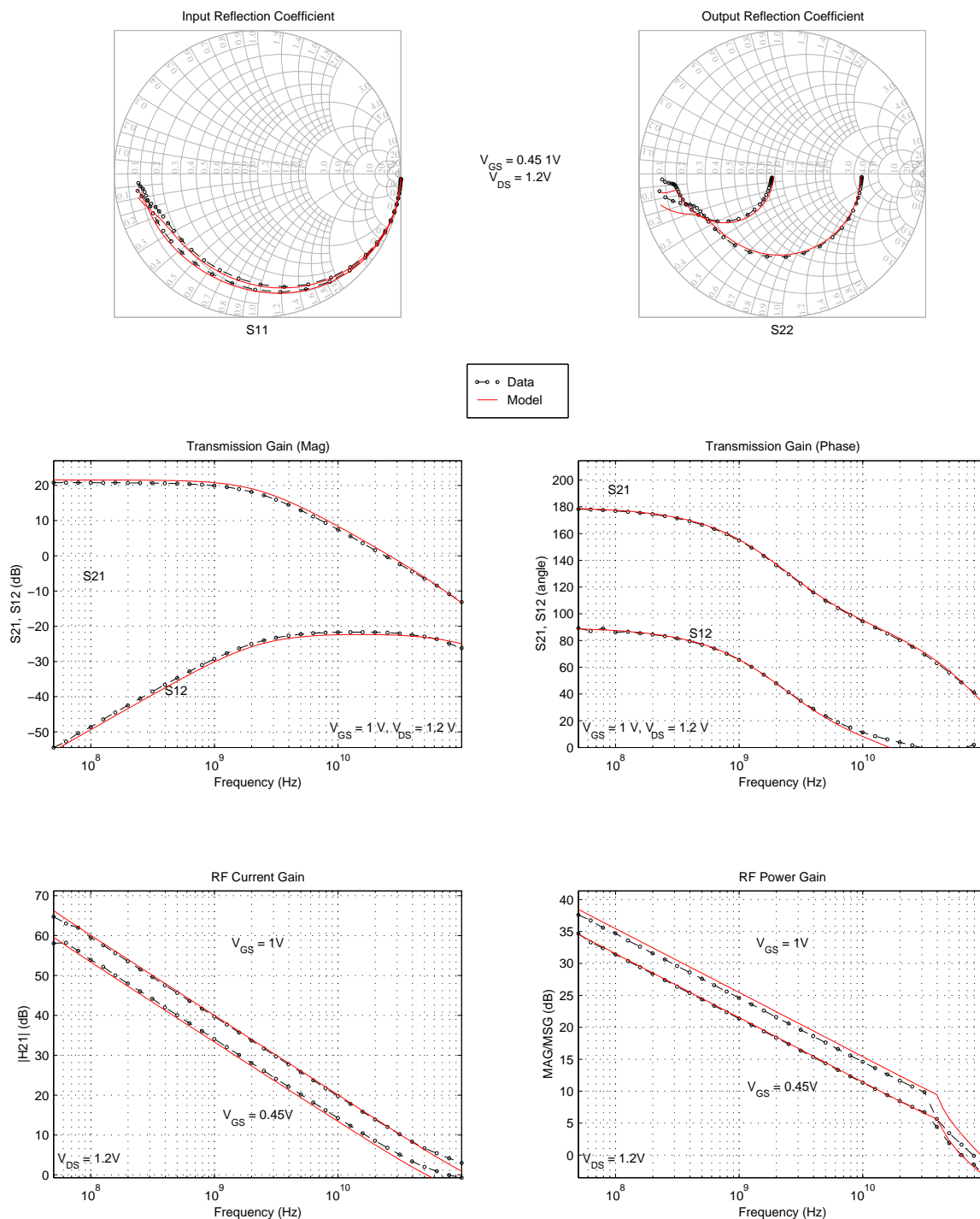
BiCMOS8HP "NFET" – Typical S-Parameter Characteristics (25C)
Device Size: $W = 5\mu\text{m}$ $L = 0.12\mu\text{m}$ $NF = 32$



Wafer Parametrics: $u_0=0.094$, $tox_0=2.64\text{n}$, $cfl=3.5e-5$, $wint=0.01u$, $thesat=1.12$, $rsw=60$, $dl=1.68e-8$, $cj=0.9\text{m}$, $dlq=-4e-8$, $nsuho=9.57e22$, $fol1=25.75\text{m}$, $fol2=1.06\text{m}$, $vfbw=-0.8\text{m}$, $iginvbw=50.5$, $igovw=6.9$

Figure 186. NFET S-Parameter Characteristics, $5\mu\text{m} \times L_{min} \times 32$

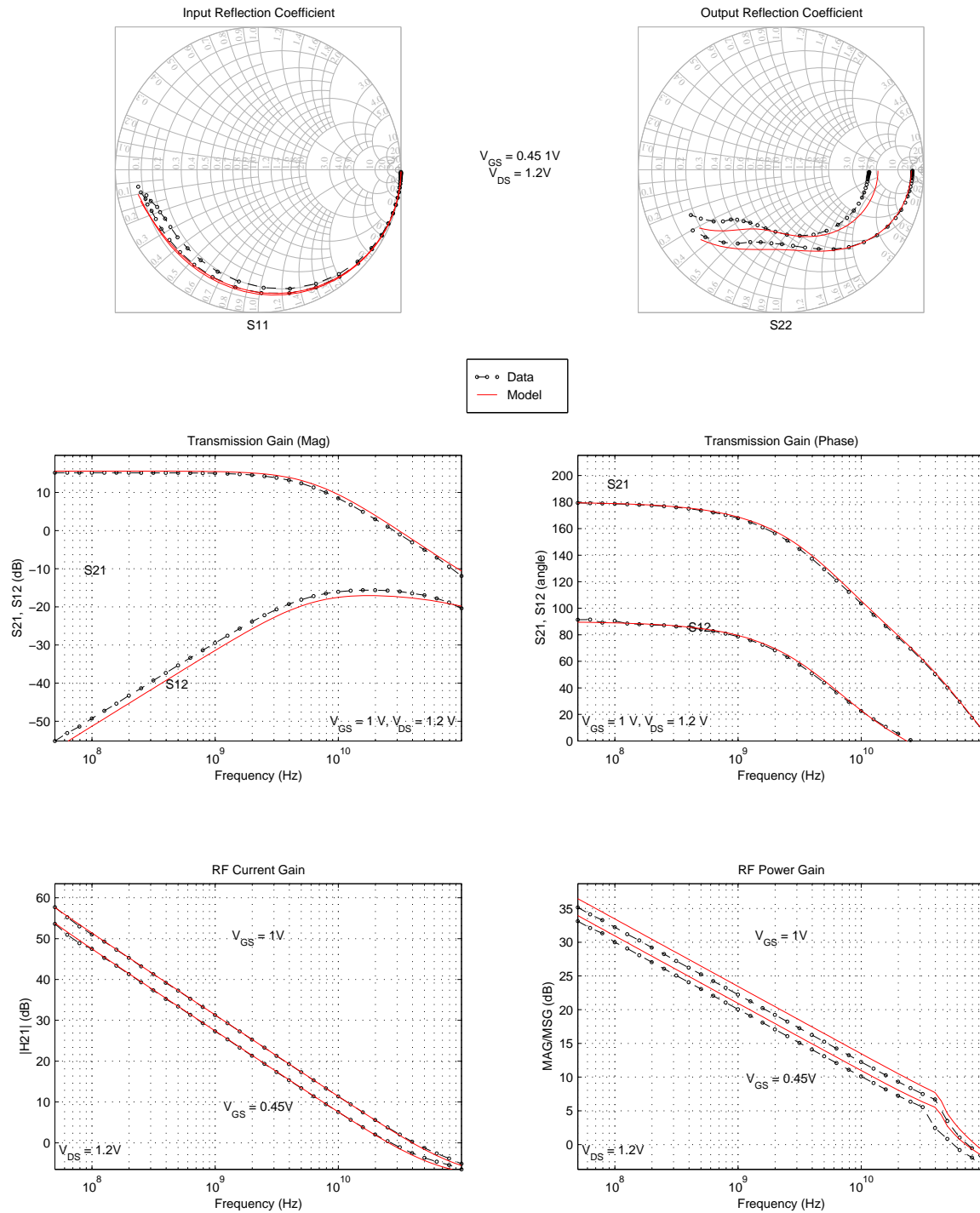
BiCMOS8HP "NFET" – Typical S-Parameter Characteristics (25C)
Device Size: W = 10 μ m L = 0.12 μ m NF = 32



Wafer Parameters: $u_0=0.094$, $toxo=2.64n$, $cl=3.5e-5$, $wint=0.01u$, $thesatl=1.12$, $rsw=60$, $dl=1.68e-8$, $cj=0.9m$, $dlq=-4e-8$, $nsuho=9.57e22$, $fol1=25.75m$, $fol2=1.06m$, $vfbw=-0.8m$, $iginvbw=50.5$, $igovbw=6.9$

Figure 187. NFET S-Parameter Characteristics, 10 μ m x Lmin x 32

BiCMOS8HP "NFET" – Typical S-Parameter Characteristics (25C)
Device Size: $W = 2\mu\text{m}$ $L = 0.24\mu\text{m}$ $NF = 64$



Wafer Parametrics: $u_0=0.094$, $tox_0=2.64\text{n}$, $cfl=3.5\text{e-}5$, $wint=0.01\text{u}$, $thesat=1.12$, $rsw=60$, $dl=1.68\text{e-}8$, $cj=0.9\text{m}$, $dlq=-4\text{e-}8$, $nsuho=9.57\text{e}22$, $fol1=25.75\text{m}$, $fol2=1.06\text{m}$, $vfbw=-0.8\text{m}$, $iginvbw=50.5$, $igovw=6.9$

Figure 188. NFET S-Parameter Characteristics, $2\mu\text{m} \times 0.24\mu\text{m} \times 64$

BiCMOS8HP "NFET" – Typical S-Parameter Characteristics (25C)
Device Size: $W = 2\mu\text{m}$ $L = 0.36\mu\text{m}$ $NF = 64$

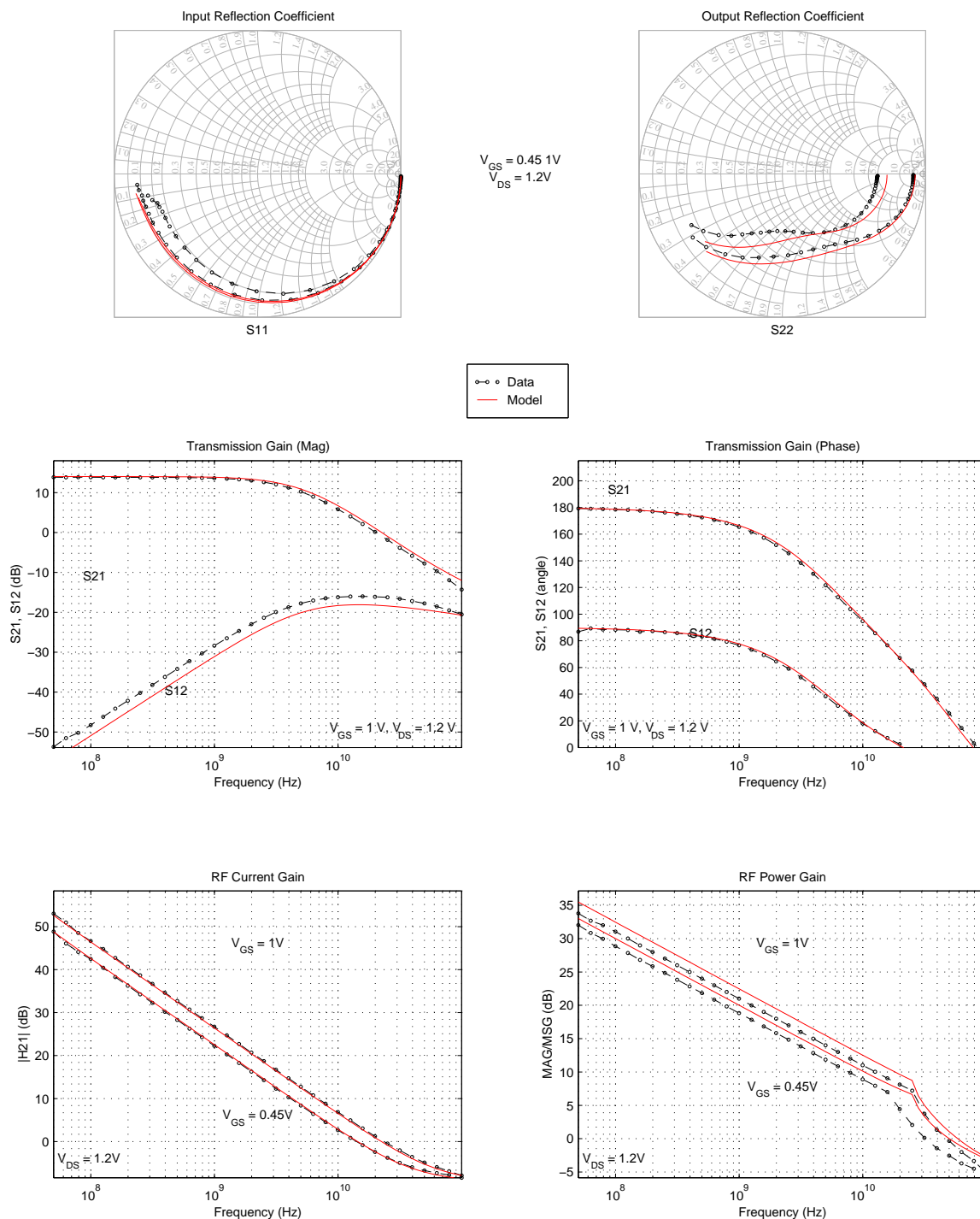
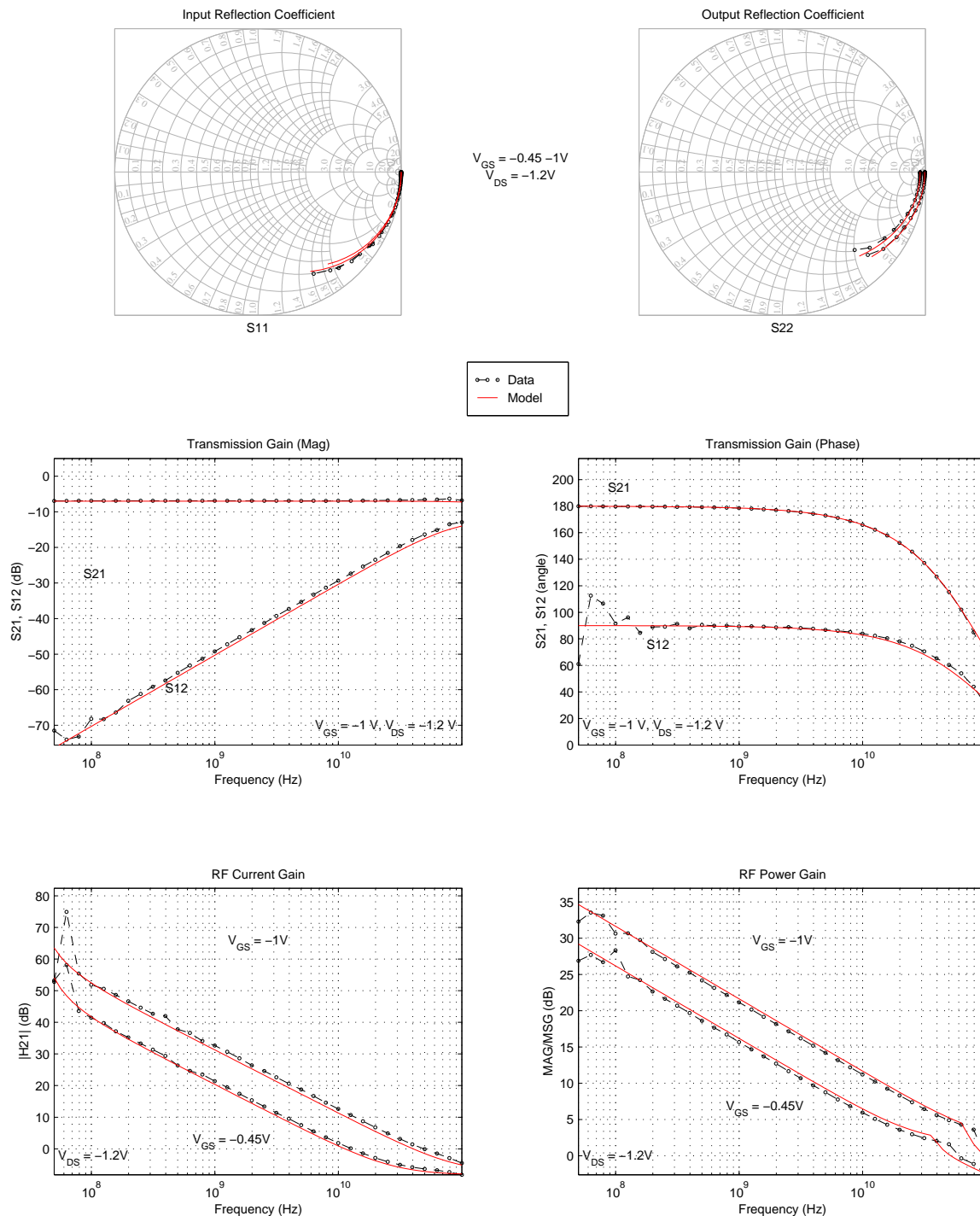


Figure 189. NFET S-Parameter Characteristics, $2\mu\text{m} \times 0.36\mu\text{m} \times 64$

BiCMOS8HP "PFET" – Typical S-Parameter Characteristics (25C)
Device Size: $W = 4\mu\text{m}$ $L = 0.12\mu\text{m}$ $NF = 8$



Wafer Parametrics: $u_0=0.01025$, $tox_0=2.43\text{n}$, $cfl=1.88\text{e-}5$, $wint=0.015\text{u}$, $thesat1=0.1126$, $cto=0.142$, $cj=1.03\text{m}$, $dlq=-2.1\text{e-}8$, $nsub_0=2.76\text{e}23$, $fol1=12.63\text{m}$, $fol2=1.025\text{m}$, $vfbw=0.456\text{m}$, $iginv1w=1303$, $igovw=1675$

Figure 190. PFET S-Parameter Characteristics, $2\mu\text{m} \times L_{min} \times 8$

BiCMOS8HP "PFET" – Typical S-Parameter Characteristics (25C)
Device Size: $W = 4\mu\text{m}$ $L = 0.12\mu\text{m}$ $NF = 20$

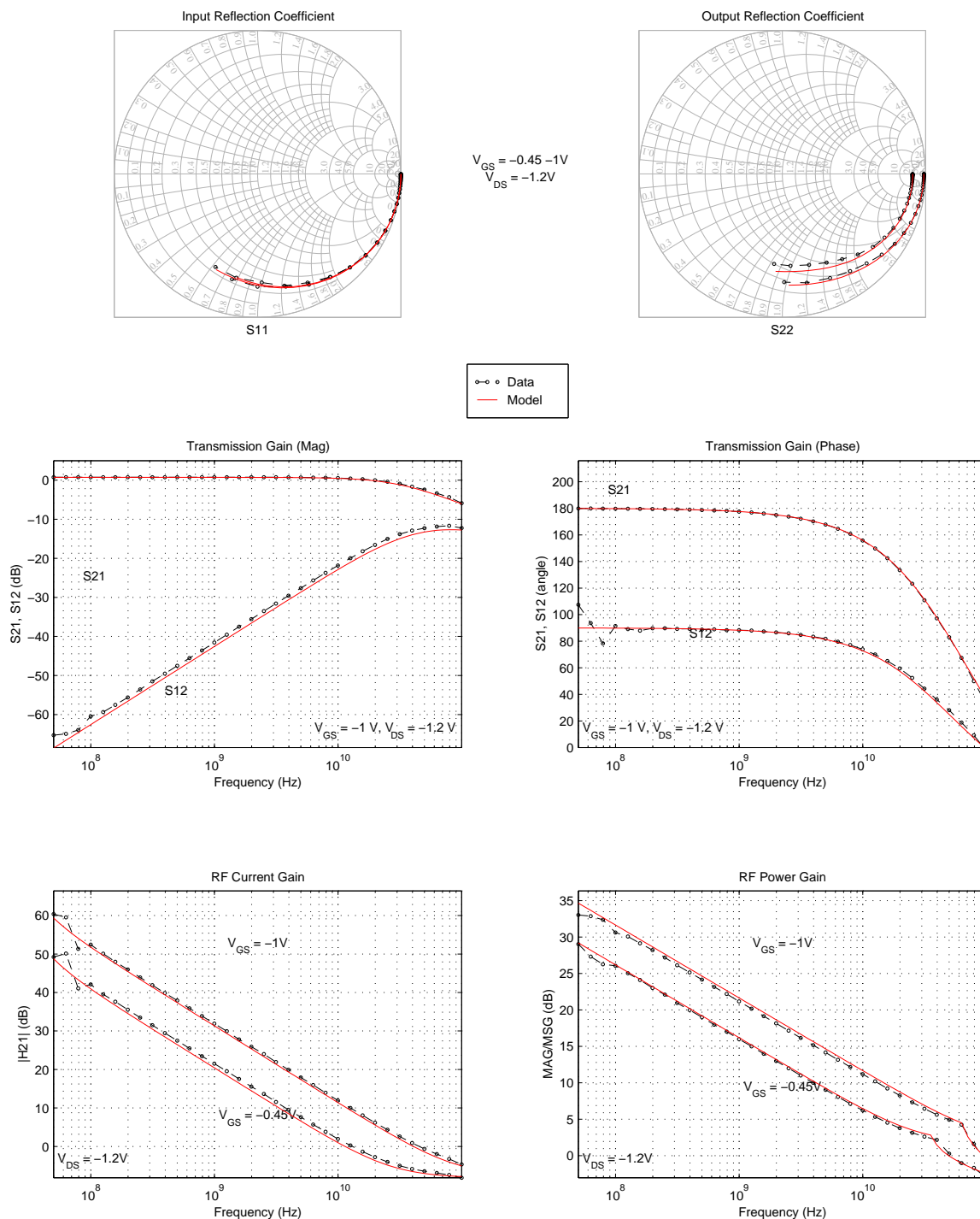


Figure 191. PFET S-Parameter Characteristics, $2\mu\text{m} \times L_{min} \times 20$

BiCMOS8HP "PFET" – Typical S-Parameter Characteristics (25C)
Device Size: $W = 5\mu\text{m}$ $L = 0.12\mu\text{m}$ $NF = 32$

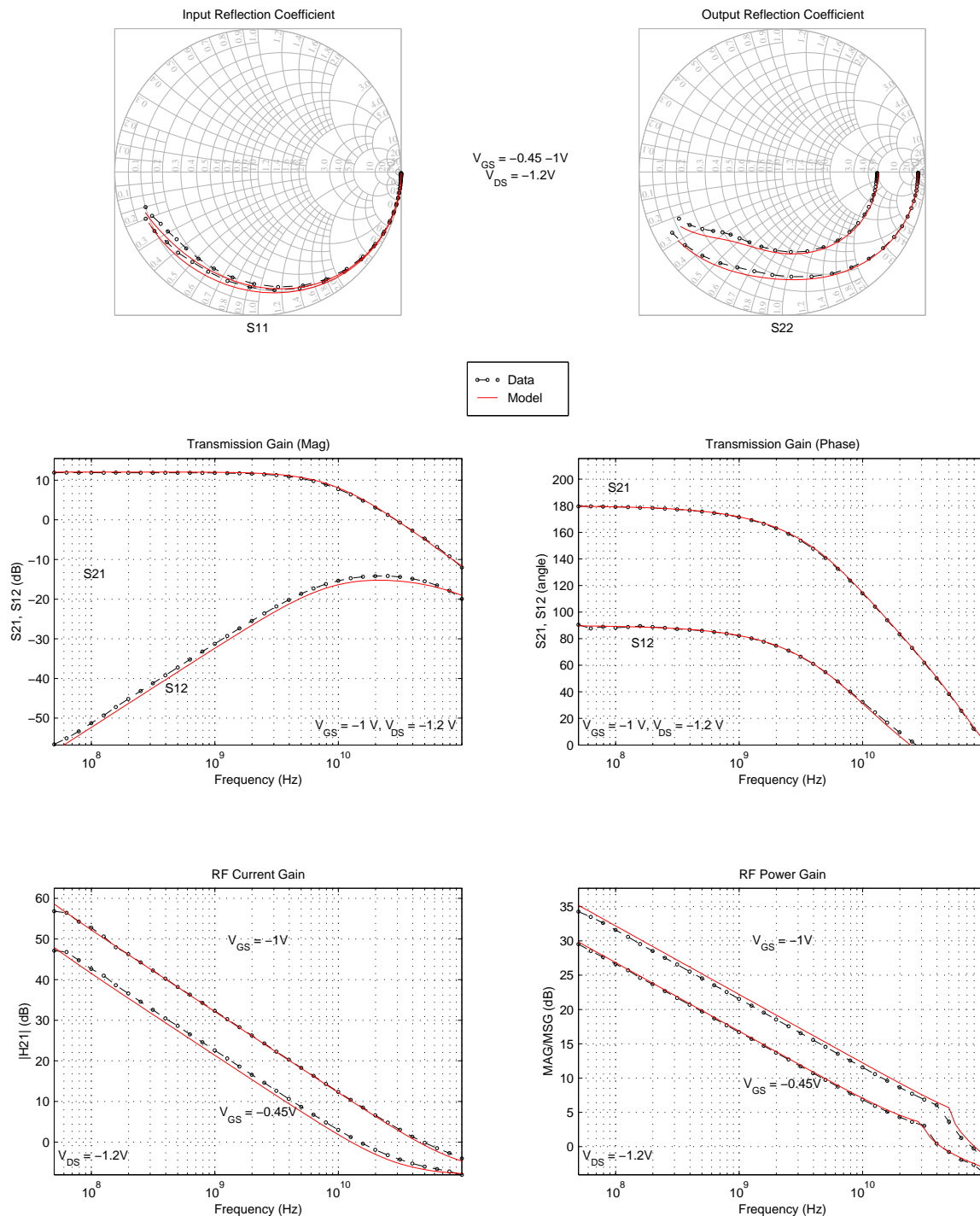


Figure 192. PFET S-Parameter Characteristics, $5\mu\text{m} \times L_{min} \times 32$

BiCMOS8HP "PFET" – Typical S-Parameter Characteristics (25C)
Device Size: $W = 10\mu\text{m}$ $L = 0.12\mu\text{m}$ $NF = 32$

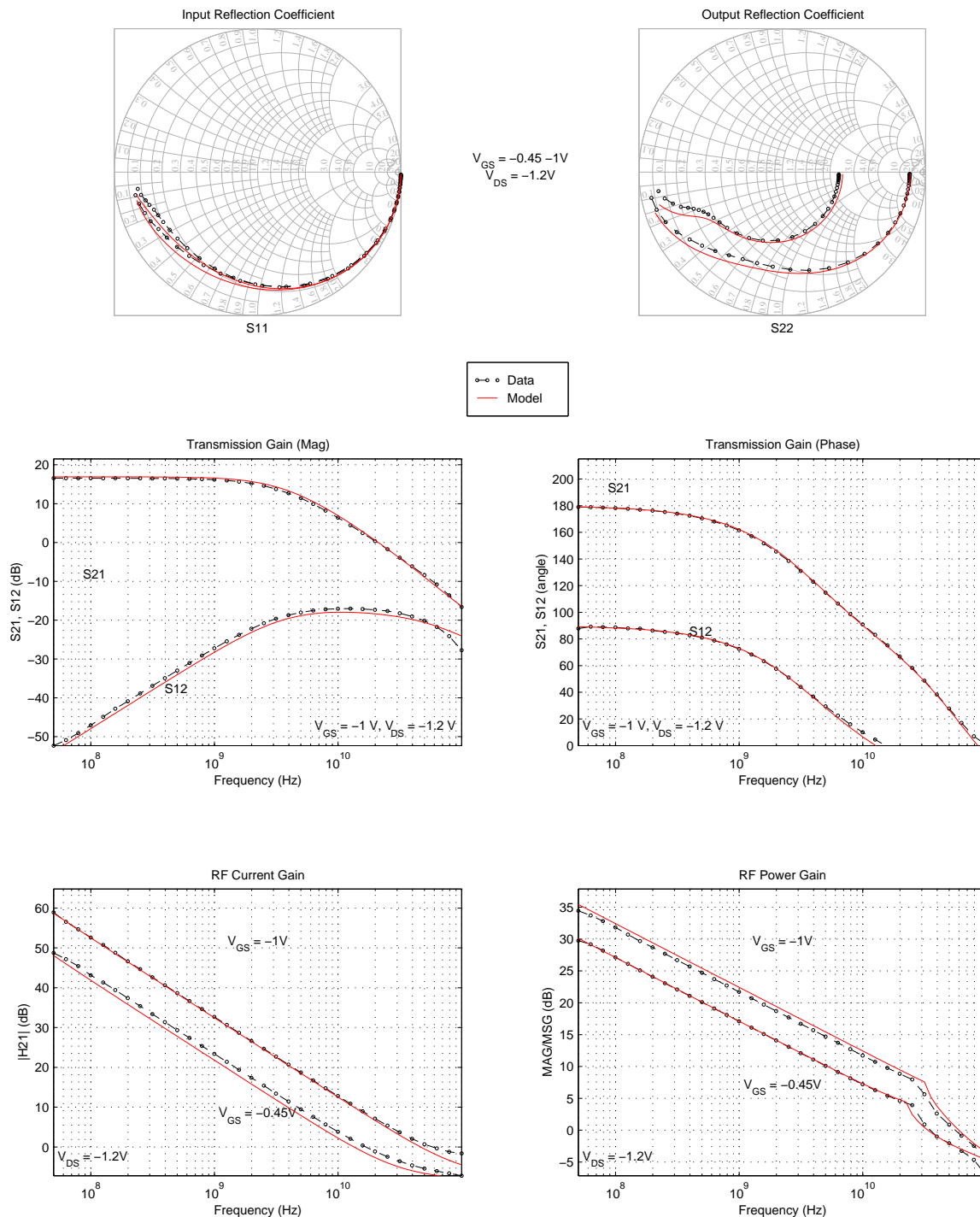


Figure 193. PFET S-Parameter Characteristics, $10\mu\text{m} \times L_{min} \times 32$

BiCMOS8HP "PFET" – Typical S-Parameter Characteristics (25C)
Device Size: $W = 2\mu\text{m}$ $L = 0.24\mu\text{m}$ $NF = 64$

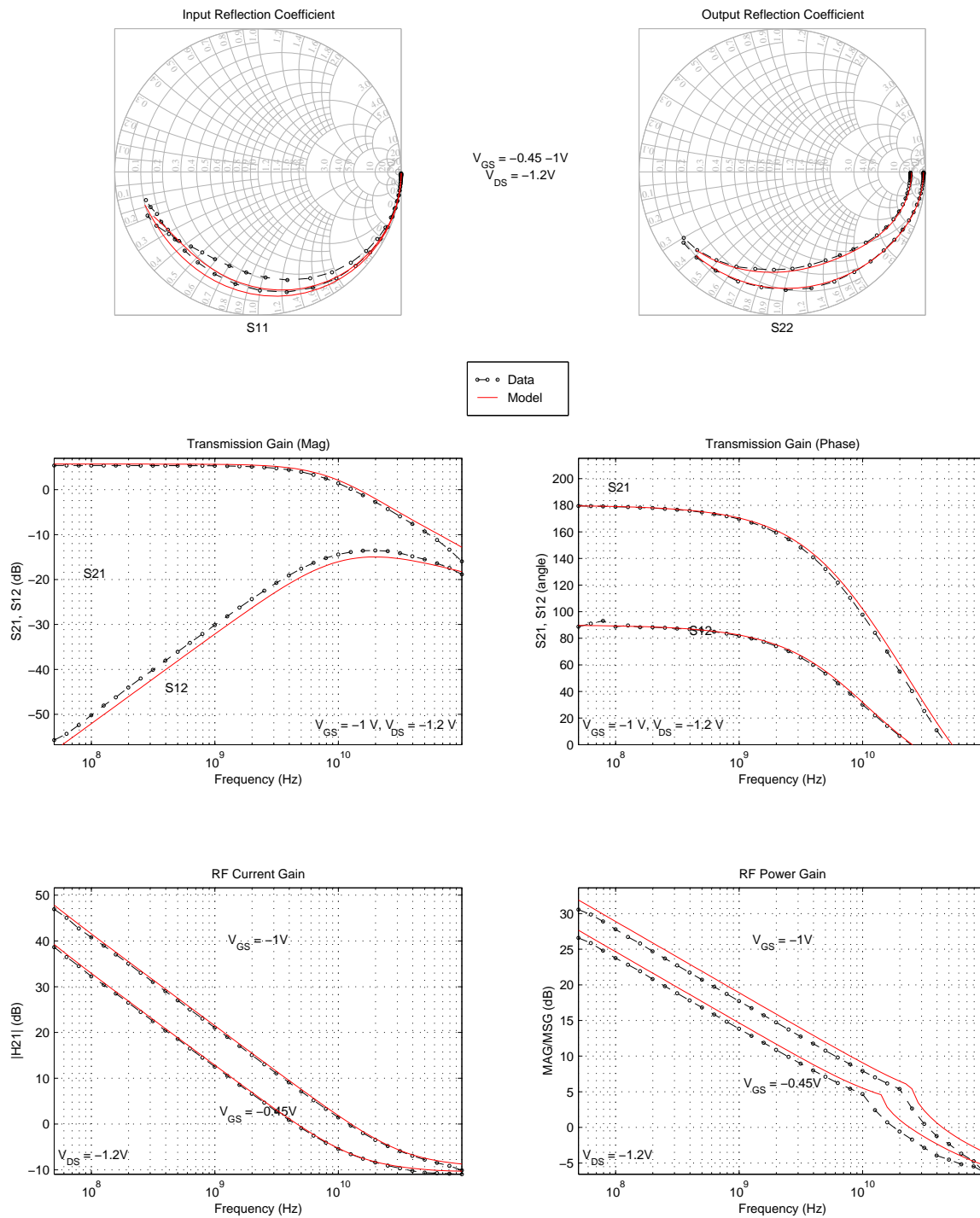


Figure 194. PFET S-Parameter Characteristics, $2\mu\text{m} \times 0.24\mu\text{m} \times 64$

BiCMOS8HP "PFET" – Typical S-Parameter Characteristics (25C)
Device Size: $W = 2\mu\text{m}$ $L = 0.36\mu\text{m}$ $NF = 64$

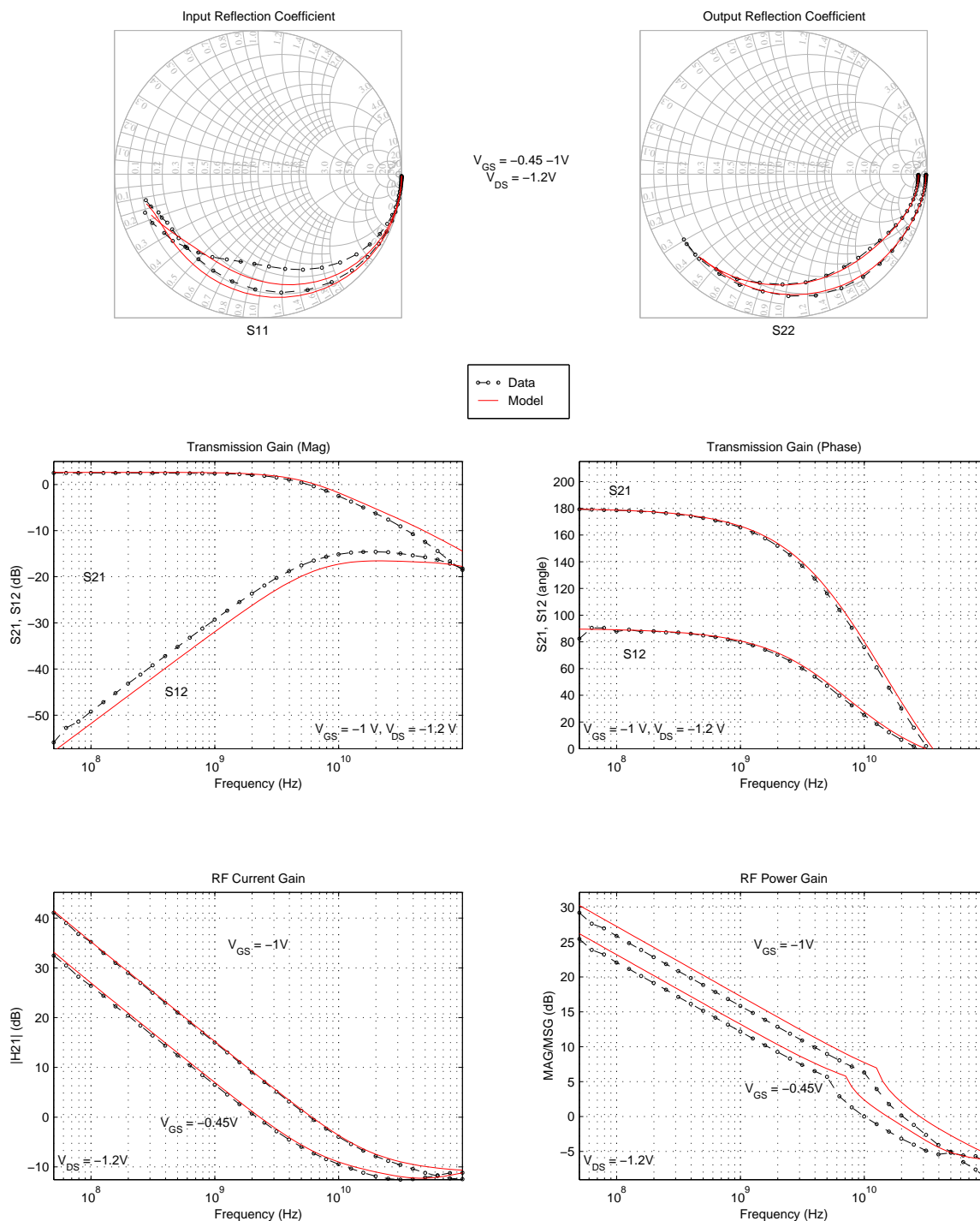


Figure 195. PFET S-Parameter Characteristics, $2\mu\text{m} \times 0.36\mu\text{m} \times 64$

BiCMOS8HP "DGNFET" – Typical S-Parameter Characteristics (25C)
Device Size: $W = 2\mu\text{m}$ $L = 0.24\mu\text{m}$ $NF = 4$

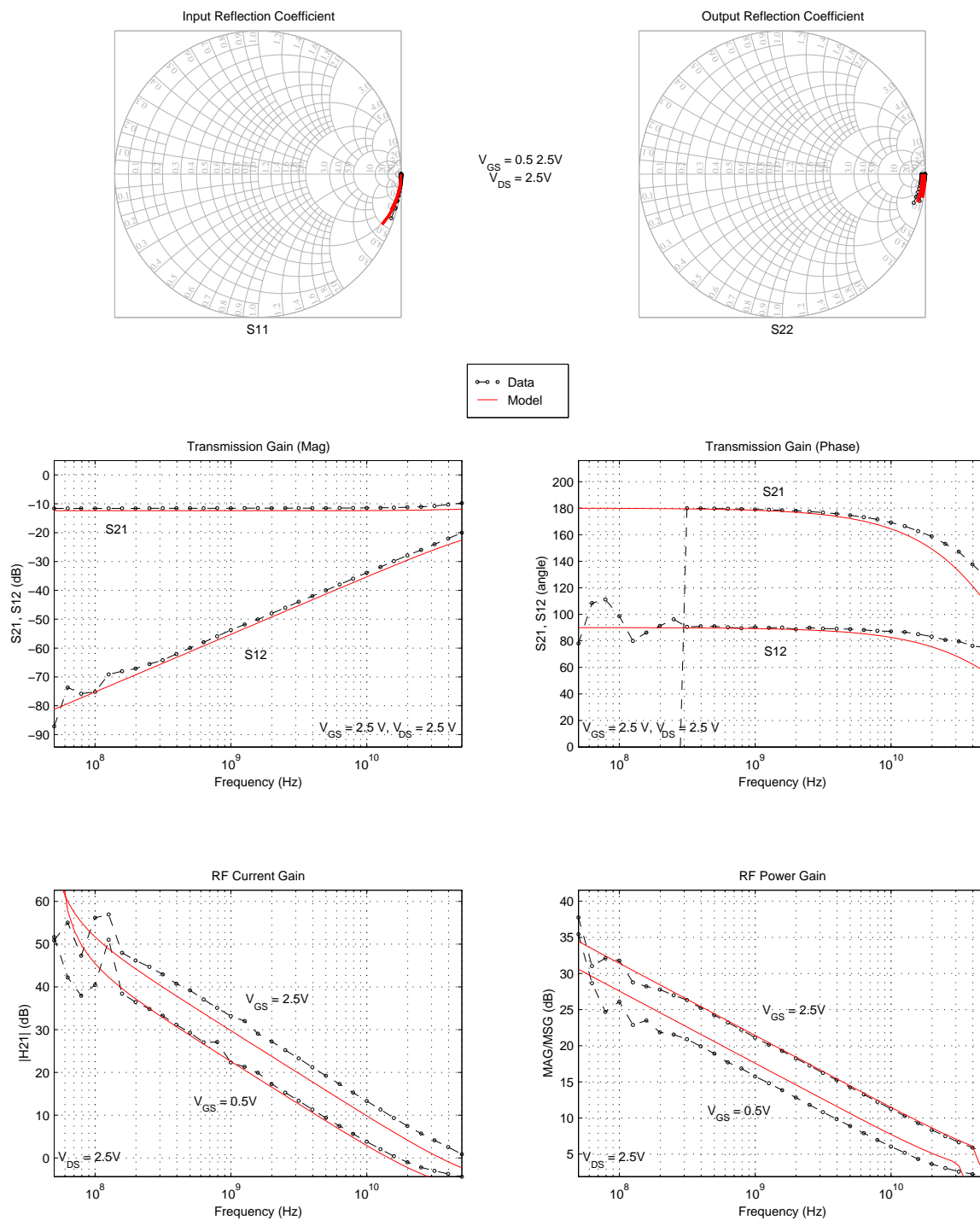


Figure 196. DGNFET S-Parameter Characteristics, $2\mu\text{m} \times L_{\text{min}} \times 4$

BiCMOS8HP "DGNFET" – Typical S-Parameter Characteristics (25C)
Device Size: $W = 2\mu\text{m}$ $L = 0.24\mu\text{m}$ $NF = 20$

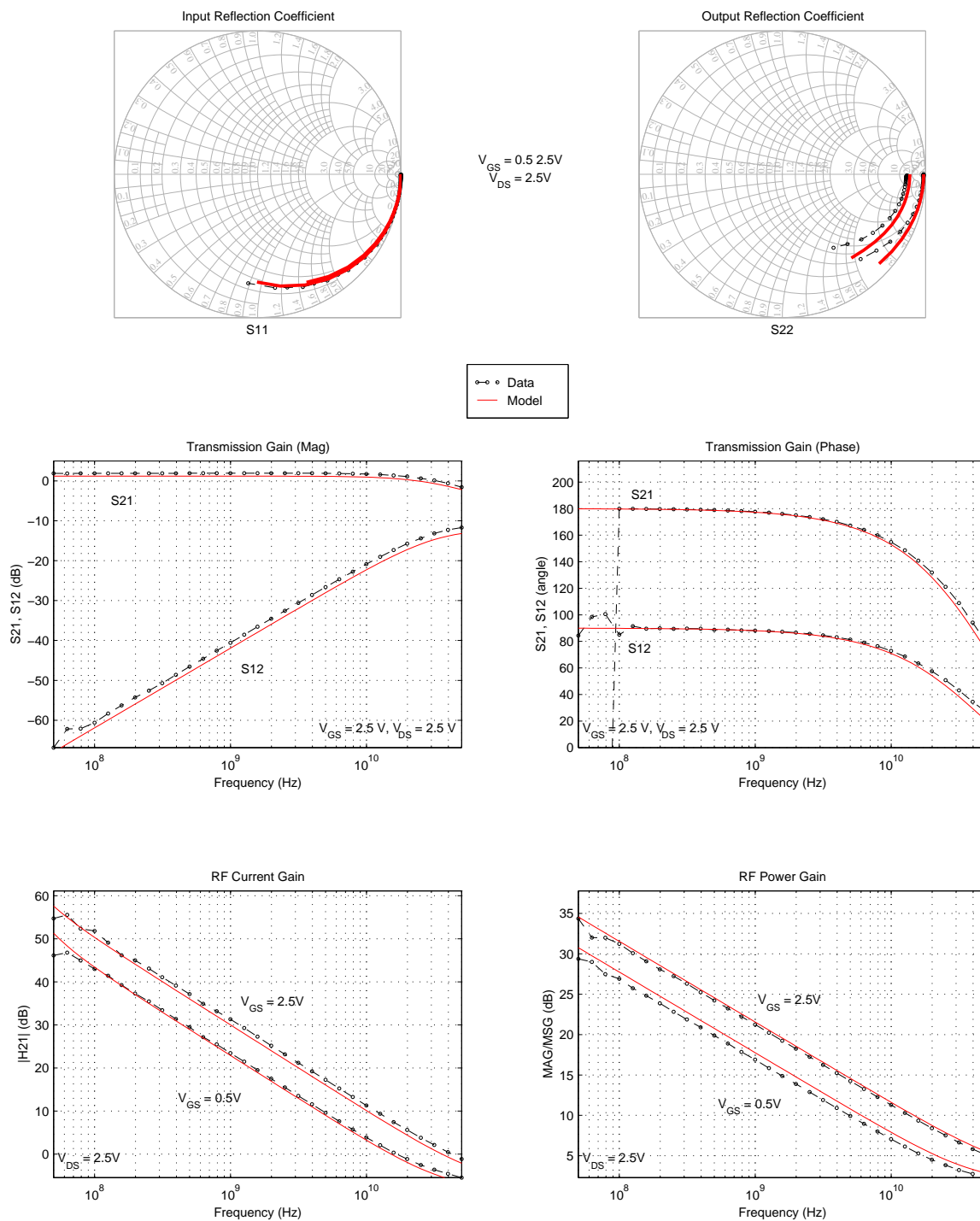


Figure 197. DGNFET S-Parameter Characteristics, $2\mu\text{m} \times L_{\text{min}} \times 20$

BiCMOS8HP "DGNFET" – Typical S-Parameter Characteristics (25C)
Device Size: $W = 2\mu\text{m}$ $L = 0.24\mu\text{m}$ $NF = 32$

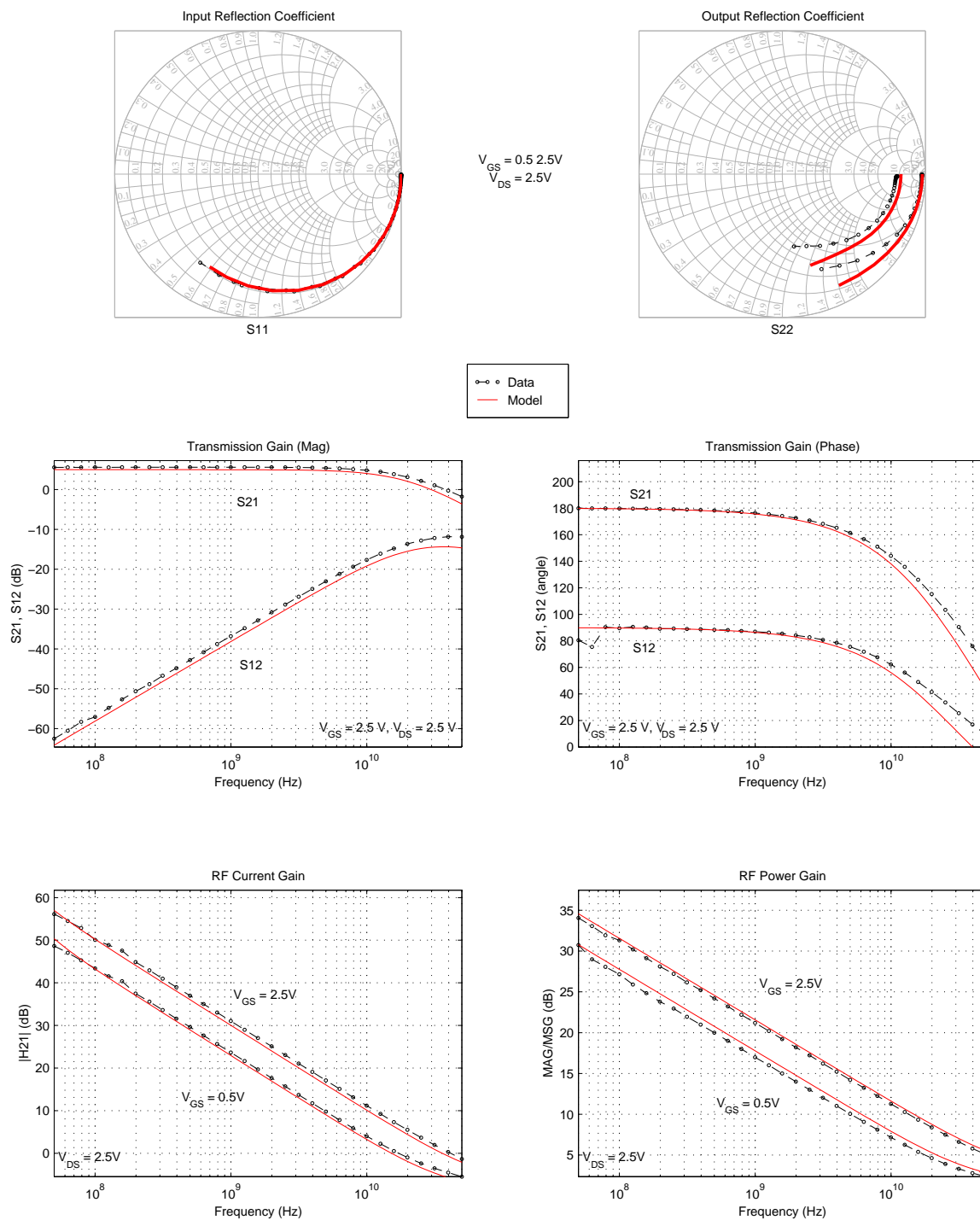


Figure 198. DGNFET S-Parameter Characteristics, $2\mu\text{m} \times L_{\text{min}} \times 32$

BiCMOS8HP "DGNFET" – Typical S-Parameter Characteristics (25C)
Device Size: $W = 5\mu\text{m}$ $L = 0.4\mu\text{m}$ $NF = 32$

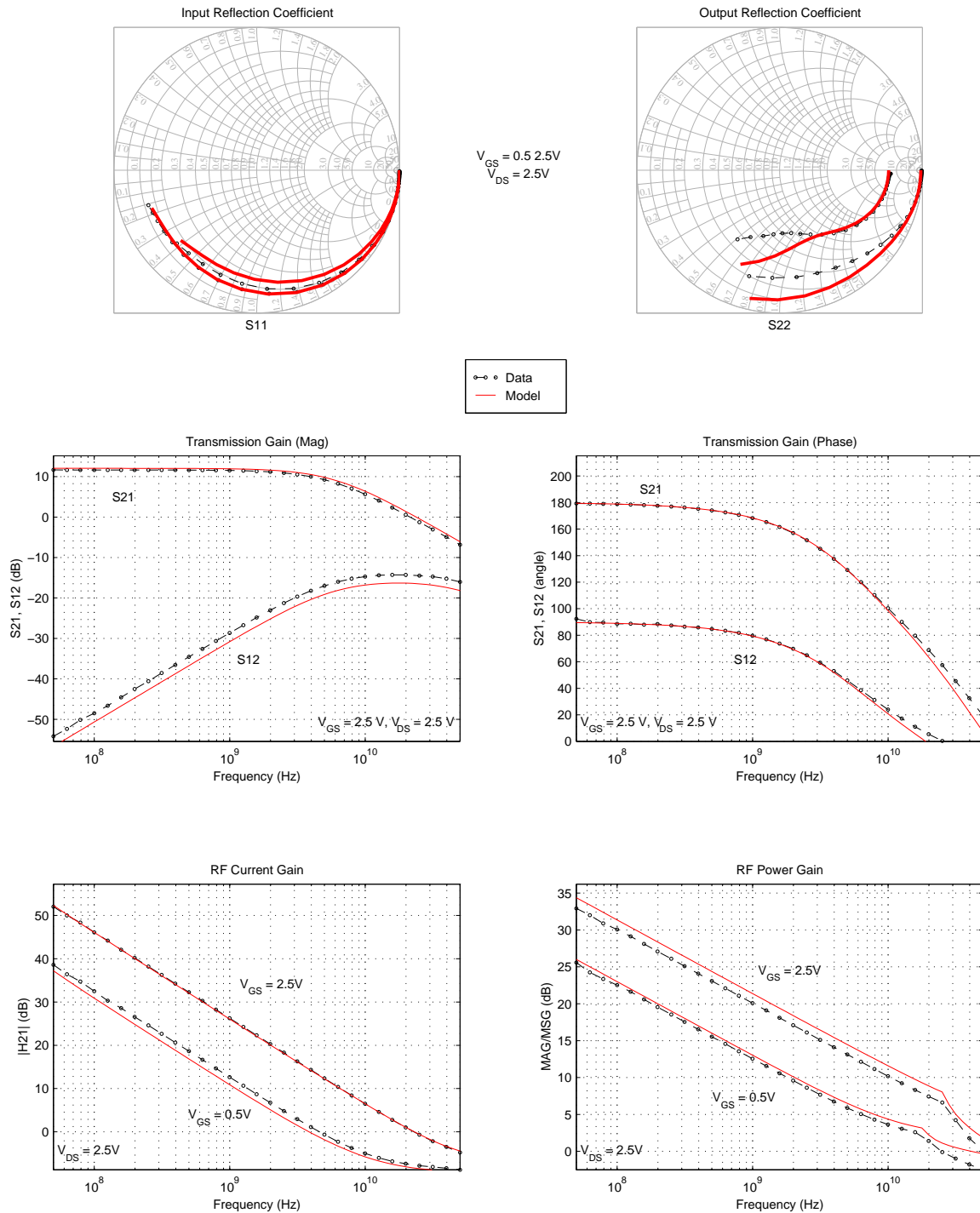


Figure 199. DGNFET S-Parameter Characteristics, $5\mu\text{m} \times 0.4\mu\text{m} \times 32$

BiCMOS8HP "DGNFET" – Typical S-Parameter Characteristics (25C)
Device Size: $W = 2\mu\text{m}$ $L = 0.72\mu\text{m}$ $NF = 64$

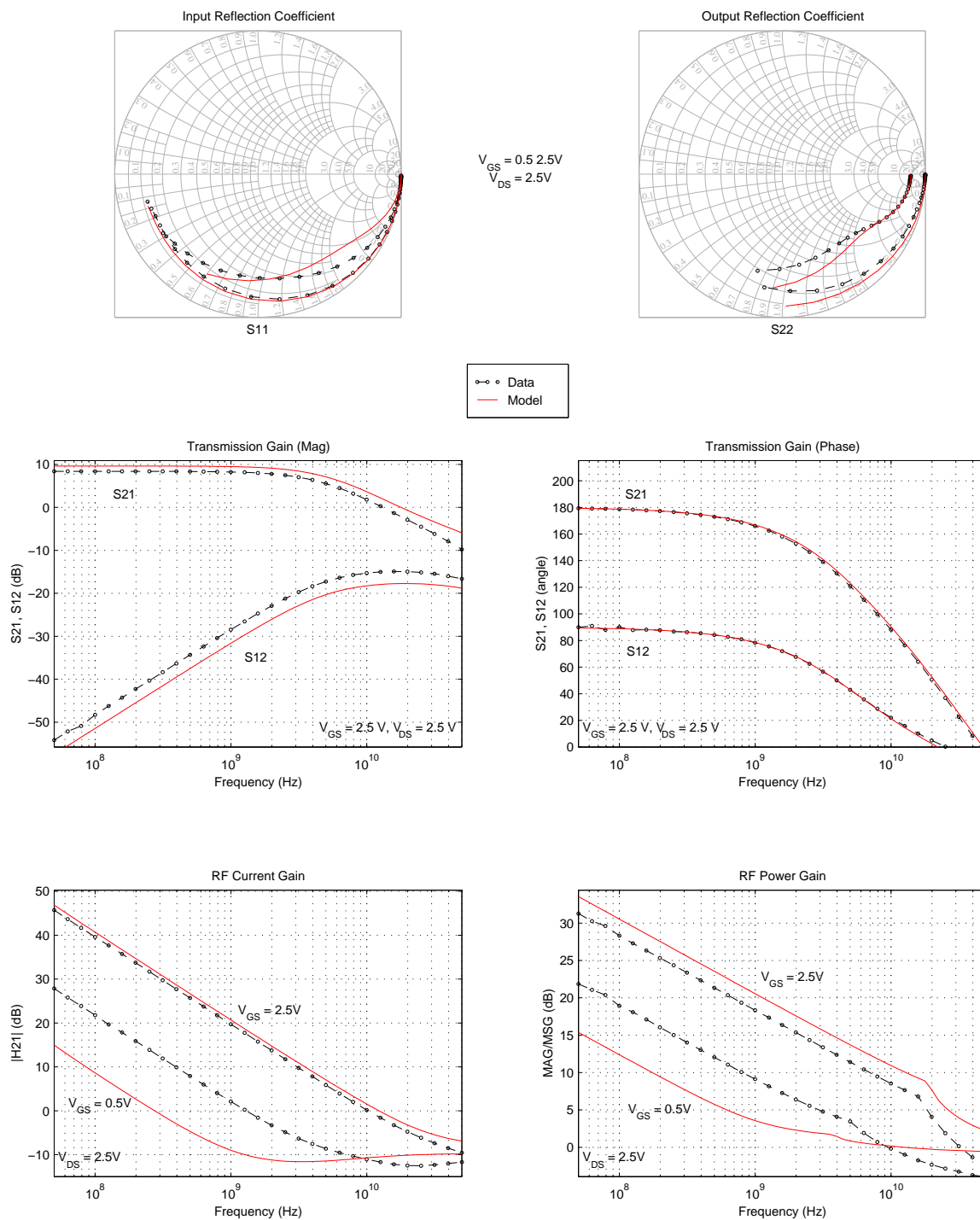
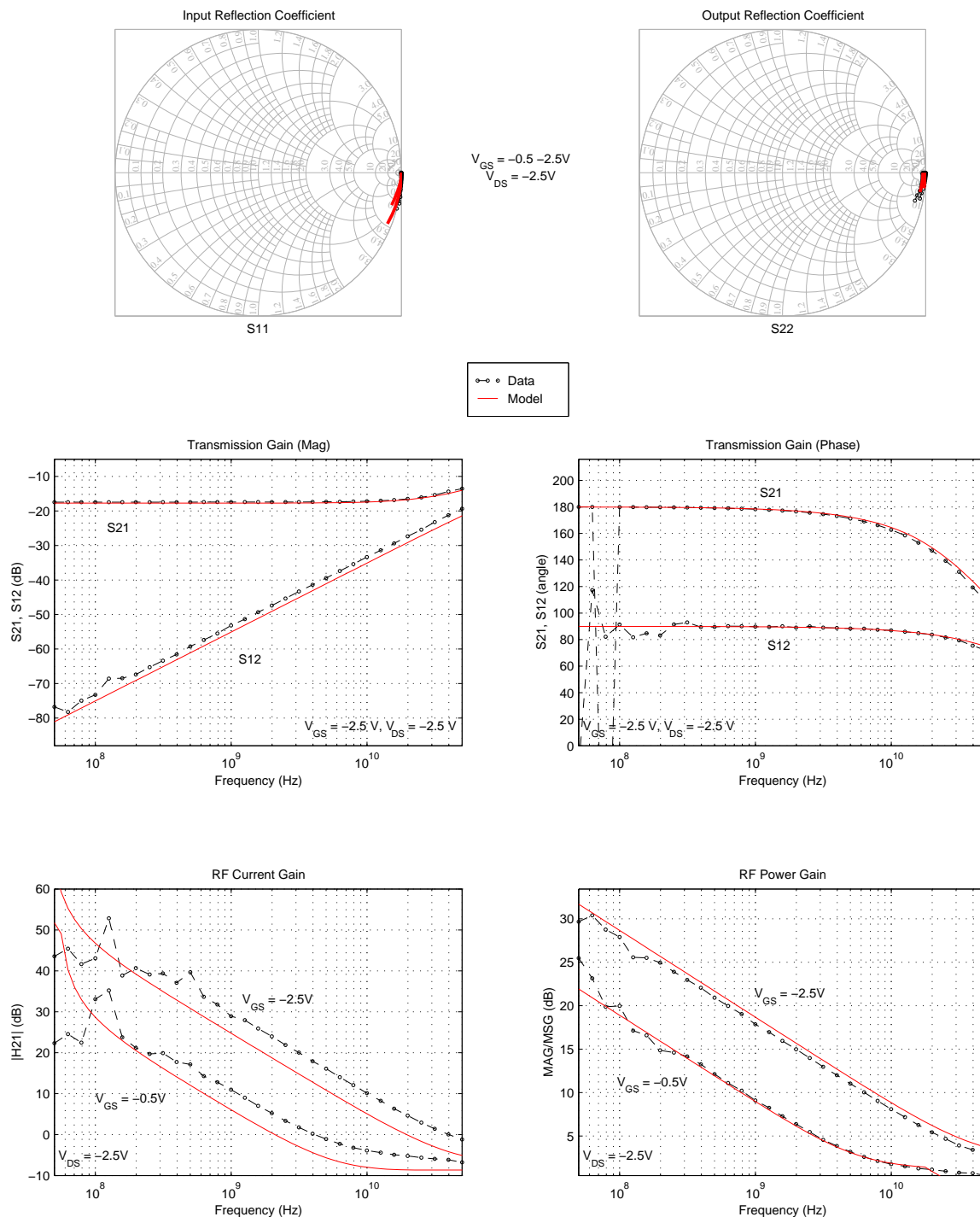


Figure 200. DGNFET S-Parameter Characteristics, $2\mu\text{m} \times 0.72\mu\text{m} \times 64$

BiCMOS8HP "DGPfet" – Typical S-Parameter Characteristics (25C)
Device Size: $W = 2\mu\text{m}$ $L = 0.24\mu\text{m}$ $NF = 4$



Wafer Parametrics: $\text{tox}=5.383\text{n}$, $\text{u0}=0.01819$, $\text{vfb}=-0.9972$, $\text{vfb1}=0.01633$ $\text{dl}=3.192\text{e}-8$

Figure 201. DGPfet S-Parameter Characteristics, $2\mu\text{m} \times L_{min} \times 4$

BiCMOS8HP "DGPfet" – Typical S-Parameter Characteristics (25C)
Device Size: $W = 2\mu\text{m}$ $L = 0.24\mu\text{m}$ $NF = 20$

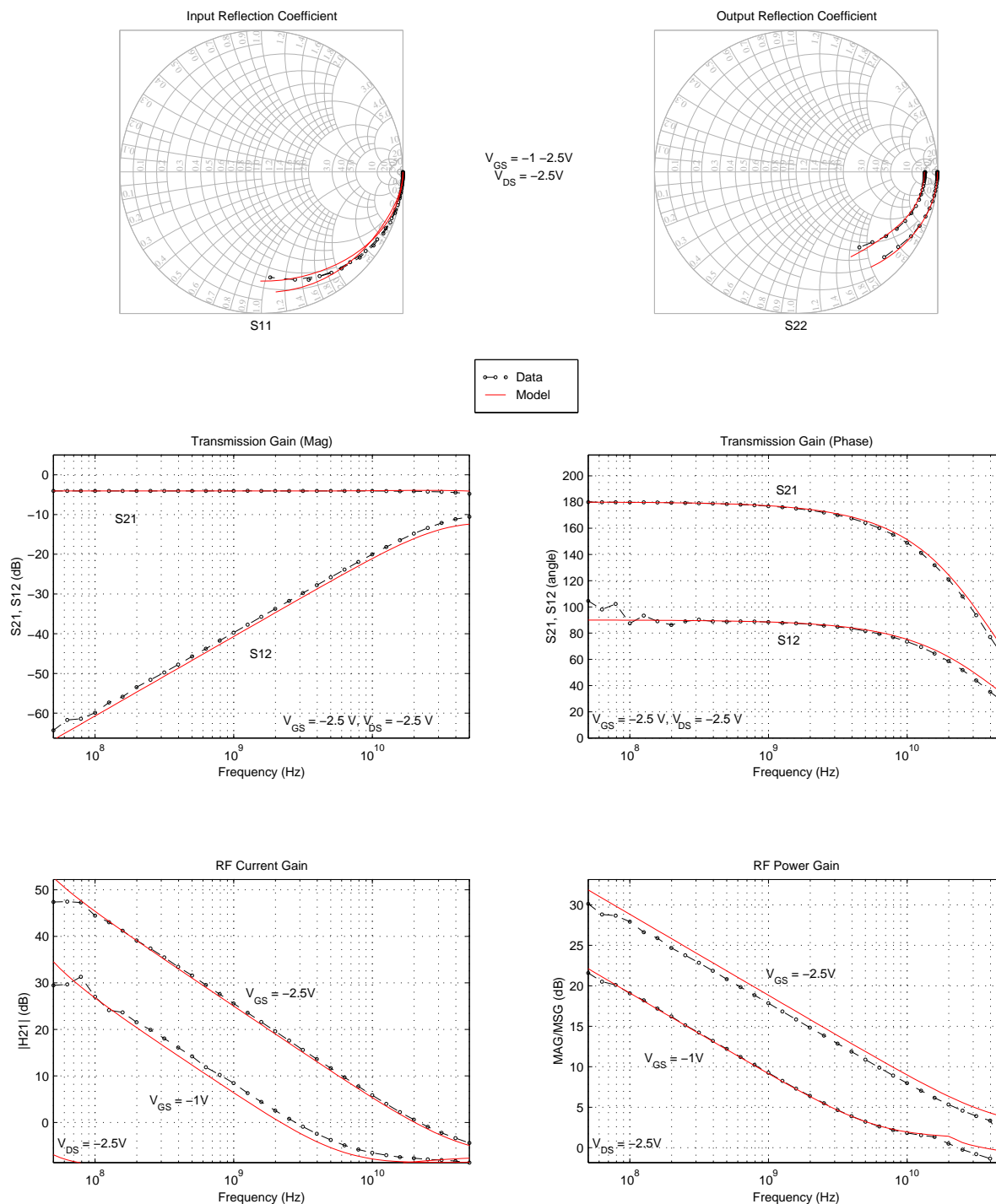


Figure 202. DGPfet S-Parameter Characteristics, $2\mu\text{m} \times L_{\text{min}} \times 20$

BiCMOS8HP "DGPFET" – Typical S-Parameter Characteristics (25C)
Device Size: $W = 2\mu\text{m}$ $L = 0.24\mu\text{m}$ $NF = 32$

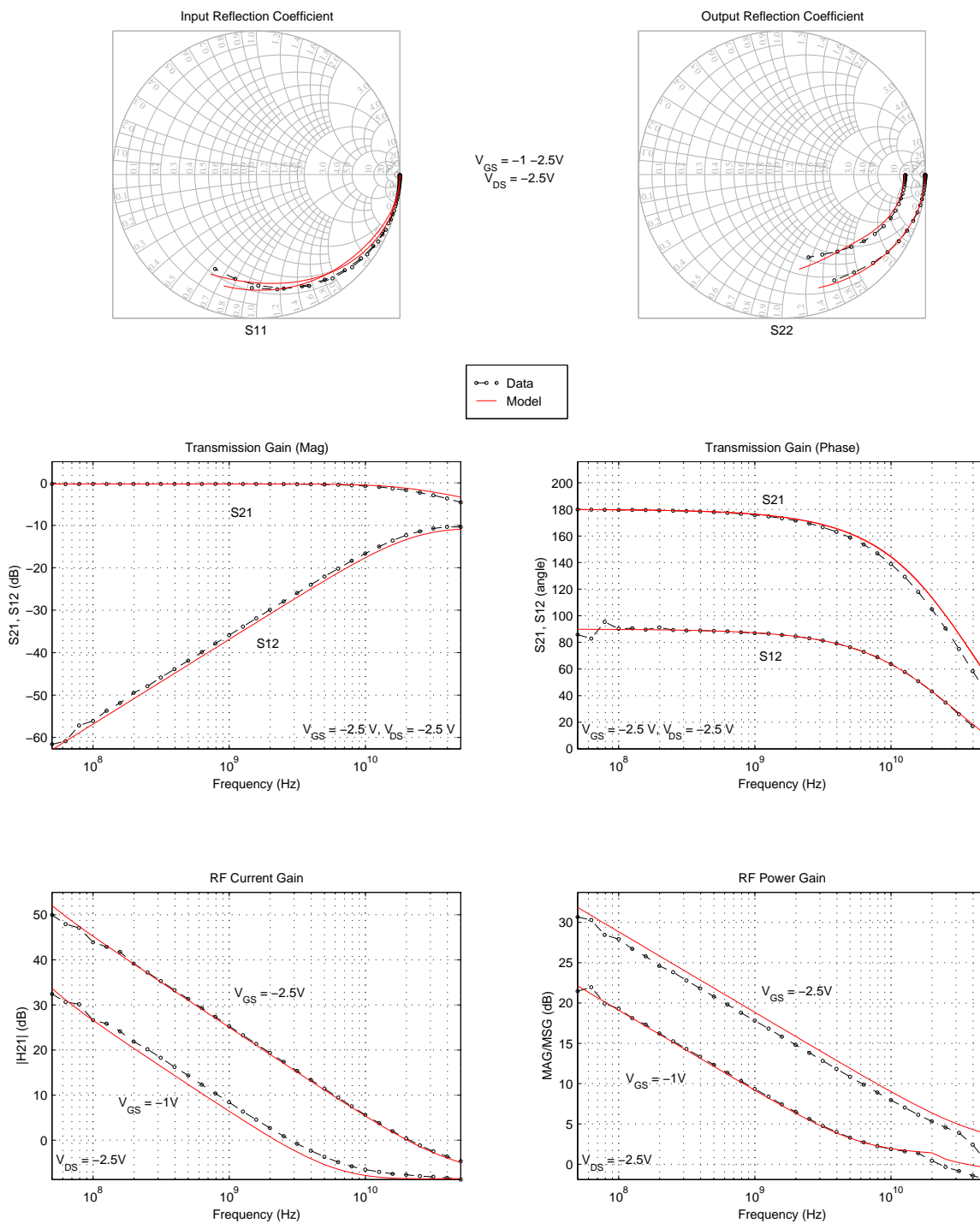


Figure 203. DGPFET S-Parameter Characteristics, $2\mu\text{m} \times L_{min} \times 32$

BiCMOS8HP "DGPFET" – Typical S-Parameter Characteristics (25C)
Device Size: $W = 5\mu\text{m}$ $L = 0.4\mu\text{m}$ $NF = 32$

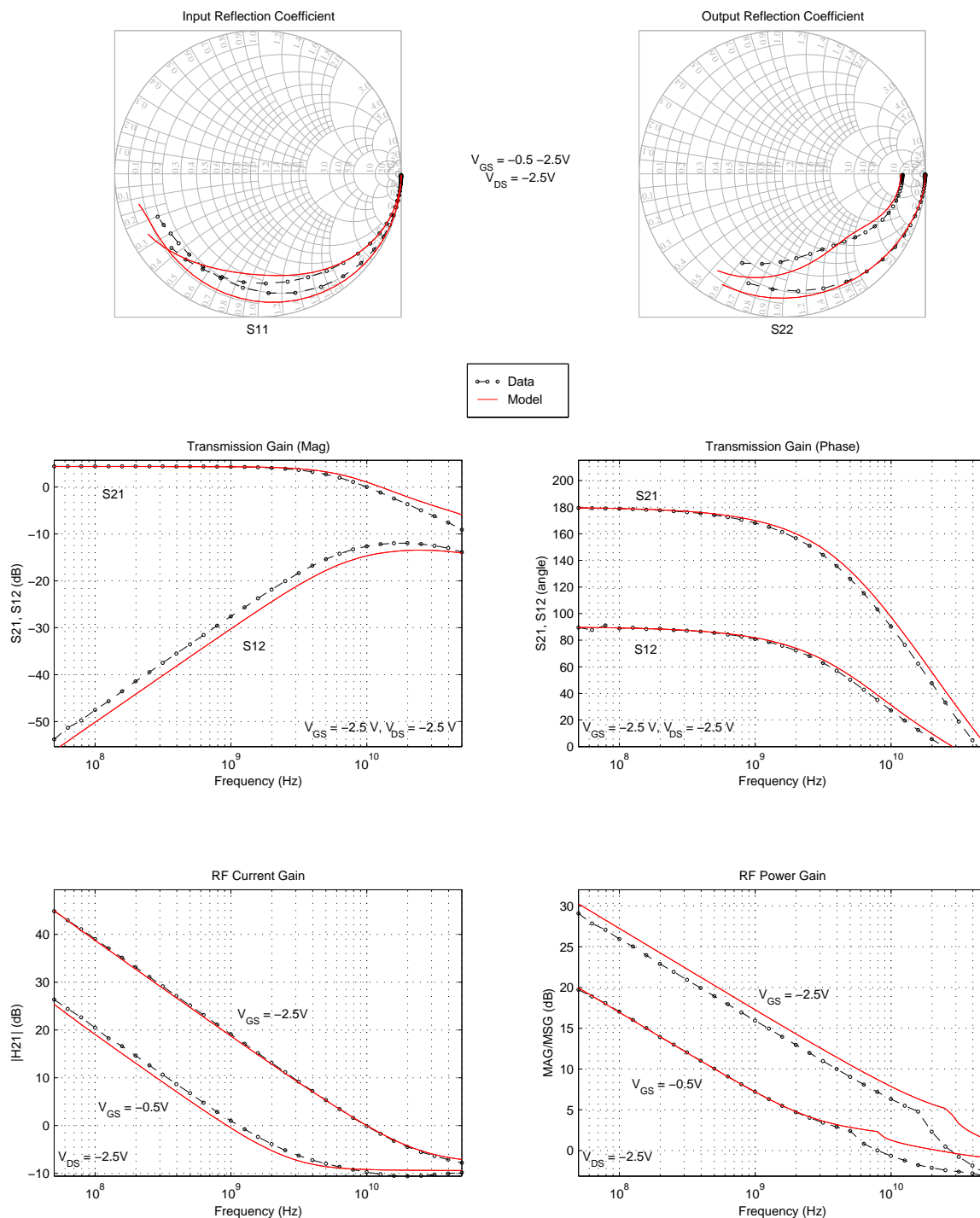


Figure 204. DGPFET S-Parameter Characteristics, $5\mu\text{m} \times 0.4\mu\text{m} \times 32$

BiCMOS8HP "DGPfet" – Typical S-Parameter Characteristics (25C)
Device Size: $W = 2\mu\text{m}$ $L = 0.72\mu\text{m}$ $NF = 64$

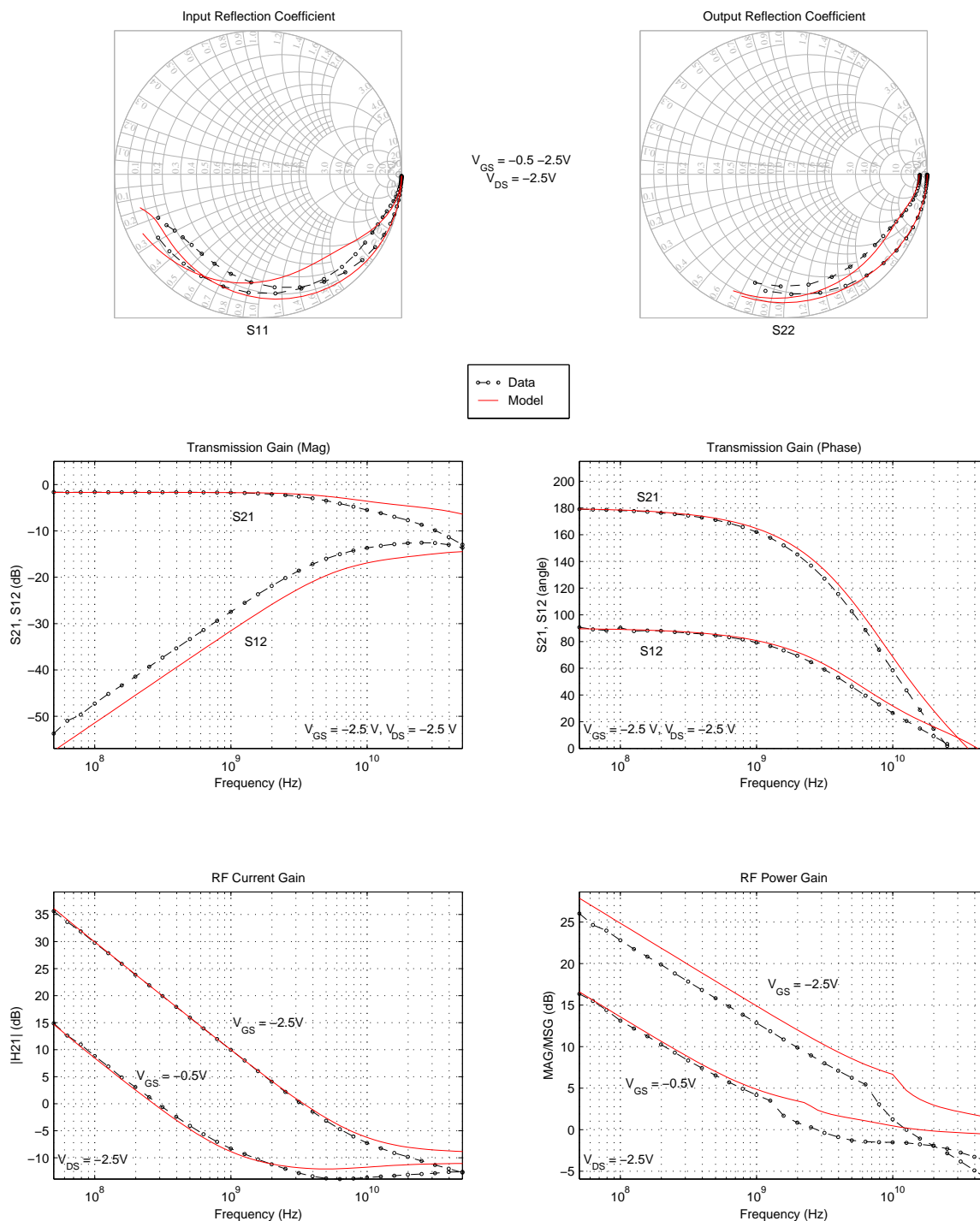


Figure 205. DGPfet S-Parameter Characteristics, $2\mu\text{m} \times 0.72\mu\text{m} \times 64$

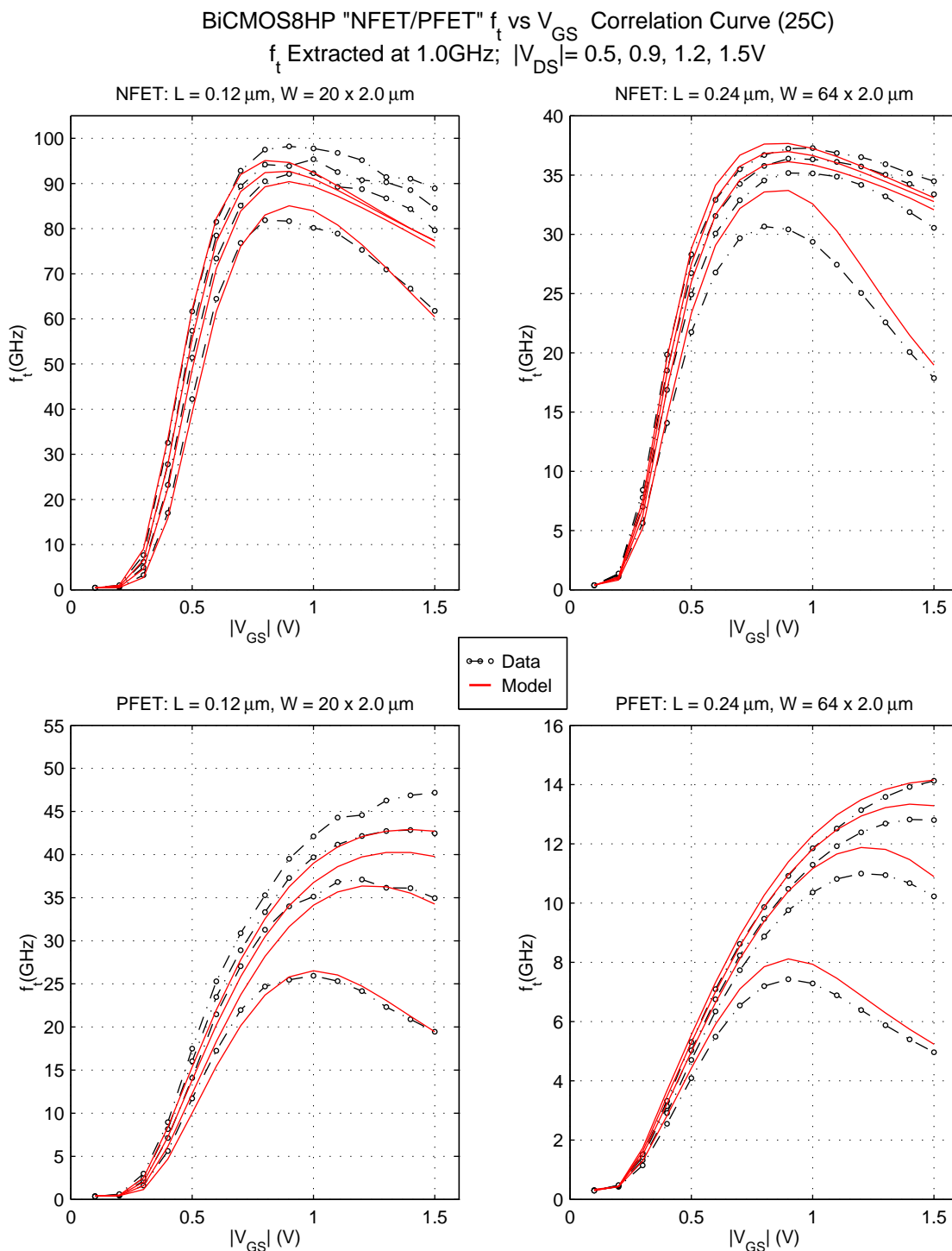
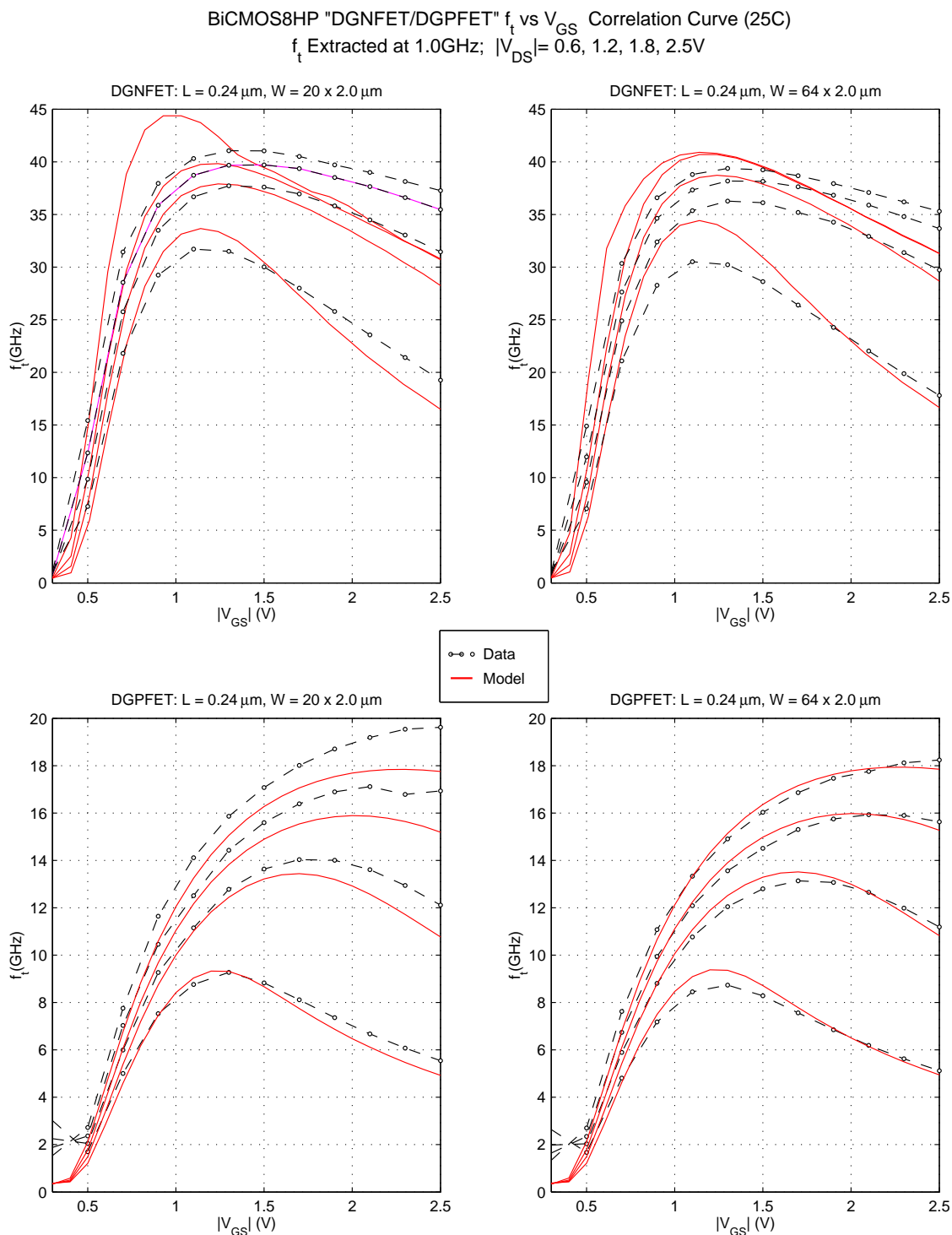


Figure 206. NFET, PFET f_T vs V_{GS} , V_{DS} Dependence



Wafer Parametrics: refer to S-param correlation plots for wafer parametrics of these devices

Figure 207. DGNFET, DGPFET f_T vs V_{GS} , V_{DS} Dependence

6.0 Resistor Models

6.1 Model Features

The resistor models include:

- Multiple lumped element R-C subcircuit for better accuracy at higher frequencies.
- Adjacent resistor mis-match as a function of resistor width and length.
- Separate body and end resistance temperature coefficients.
- User-defined substrate resistance (rsx) based on layout (default=50 ohms).
- Device temperature difference with respect to circuit temperature (dtemp).

6.2 Model Limitations and Restrictions

Known limitations of the resistor models:

- Model only supports rectangular resistors with contacts at each end of the resistor bar. “Dogbone” or multiple tap layouts are not supported.
- Model assumes minimum groundrule spacings used for placing contacts to calculate the end resistance effects based on the OP design length and the overall bar dimensions used to calculate the total parasitic capacitance.
- The models are fitted to devices with more than a single square (Length larger than Width). This ensures that the current flows through the entire device’s cross section; hence, validating the extracted sheet resistance. The model will under estimate the resistive values of devices with less than one square.

6.3 DC Correlation Tables

The following tables compare the DC characteristics of the resistor models with measurements from the technology qualification hardware. As the model supports a range of widths and lengths, the tables show model correlation for the resistor sizes available on the test structures.

Resistor simulations were done with some process parameters shifted to center the model near the mean of the measured data. Specific values used are listed with a footnote in each table. All other parameters used in the simulations (e.g. dl, dw...) remain at nominal process values.

Note the following definitions:

- “Rcalc” represents the calculated resistance from the model at nominal temperature (25C), assuming the shift in process parameters as specified.
- “Tolerance” is the total process tolerance (%) for that resistor size predicted by the model.
- “Error” reflects the difference between measured data and predicted model resistance (%) at the specified temperatures.

Table 65. <i>P+</i> Polysilicon Resistor DC Correlation				
Drawn Dimensions	Rcalc (25C)	Error(-40C)	Error (25C)	Error (125C)
W = 10μm, L = 10μm	341	-0.25	-0.11	0.32
W = 4 μm, L = 1.6μm	147	0.06	1.38	3.40
W = 4μm, L = 10μm	857	-0.72	-0.48	-0.22
W = 2 μm, L = 30 μm	5135	-1.56	-1.24	-0.99
W = 5μm, L = 30μm	2033	-1.07	-0.68	-0.09
W = 0.2μm, L = 1.6μm	3512	0.29	0.36	0.42
W = 2μm, L = 5 μm	876	-0.67	-0.54	-0.43
W = 30μm, L = 120μm	1343	-0.38	-0.08	0.37
W = 30μm, L = 20μm	225	-0.56	0.40	2.05
W = 5μm, L = 5μm	347	-0.06	-0.11	-0.01
W = 1μm, L = 1.6μm	604	1.45	0.89	0.02
Note: Rs = 335ohm/sq and Delta-W = -0.034μ m. Resistance values in ohms.				

Table 66. <i>RR</i> Polysilicon Resistor DC Correlation				
Drawn Dimensions	Rcalc (25C)	Error(-40C)	Error (25C)	Error (125C)
W = 10μm, L = 10μm	1547	-1.47	-0.68	0.36
W = 4 μm, L = 2μm	544	0.15	1.50	3.64
W = 4μm, L = 10μm	3900	-1.09	-0.35	0.57
W = 2 μm, L = 30 μm	24921	-1.28	-0.59	0.37
W = 5μm, L = 30μm	9805	-1.34	-0.62	0.32
W = 0.8μm, L = 2μm	2880	-0.54	0.42	1.79
W = 2μm, L = 5 μm	3656	-1.09	-0.27	0.72
W = 30μm, L = 120μm	6593	-1.14	-0.48	0.32
W = 10μm, L = 5μm	715	-1.45	-0.39	1.06
W = 5μm, L = 5μm	1438	-1.45	-0.39	1.06
W = 1μm, L = 2μm	2271	0.89	1.54	2.20
Note: Rs = 1655 ohm/sq and Delta-W = -0.055μ m. Resistance values in ohms.				

Table 67. **KQ BEOL Resistor** DC Correlation

Drawn Dimensions	Rcalc (25C)	Error(-40C)	Error (25C)	Error (125C)
W = 10 μ m, L = 10 μ m	63.20	0.48	4.47	-3.28
W = 5.92 μ m, L = 5 μ m	56.83	-7.78	0.17	3.49
W = 5.92 μ m, L = 10 μ m	104.66	-1.55	-1.66	-4.03
W = 7 μ m, L = 30 μ m	252.19	-3.12	-1.97	-1.48
W = 5.92 μ m, L = 30 μ m	295.98	-3.73	-2.61	-0.81
W = 7 μ m, L = 5 μ m	48.42	1.86	4.36	-4.67
W = 7 μ m, L = 7 μ m	64.72	0.07	1.66	-1.16
W = 30 μ m, L = 100 μ m	198.21	-1.08	-1.25	-1.81
W = 30 μ m, L = 20 μ m	41.12	-0.87	4.01	5.21
W = 5.92 μ m, L = 7 μ m	75.96	-5.28	-0.83	10.04
W = 10 μ m, L = 5 μ m	34.32	4.95	8.72	1.14
Note: Rs = 59.5 ohm/sq. Resistance values in ohms.				

Table 68. **NS Resistor** DC Correlation

Drawn Dimensions	Rcalc (25C)	Error(-40C)	Error (25C)	Error (125C)
W = 4 μ m, L = 10 μ m	36.64	1.92	-1.52	-2.10
W = 2 μ m, L = 30 μ m	177.4	-8.33	-8.85	-8.64
W = 5 μ m, L = 30 μ m	65.53	-5.51	-4.03	1.97
W = 2 μ m, L = 2.6 μ m	43.48	-0.56	0.77	6.15
W = 2 μ m, L = 5 μ m	55.21	0.26	-2.18	-2.31
W = 30 μ m, L = 120 μ m	37.06	-0.03	-3.49	0.69
W = 30 μ m, L = 20 μ m	7.53	5.66	20.0	58.7
W = 5 μ m, L = 5 μ m	19.69	6.31	5.91	2.28
W = 10 μ m, L = 5 μ m	9.51	14.6	8.24	12.65
Note: Rs = 8.8ohm/sq Delta-W = -0.2 μ m. Resistance values in ohms.				

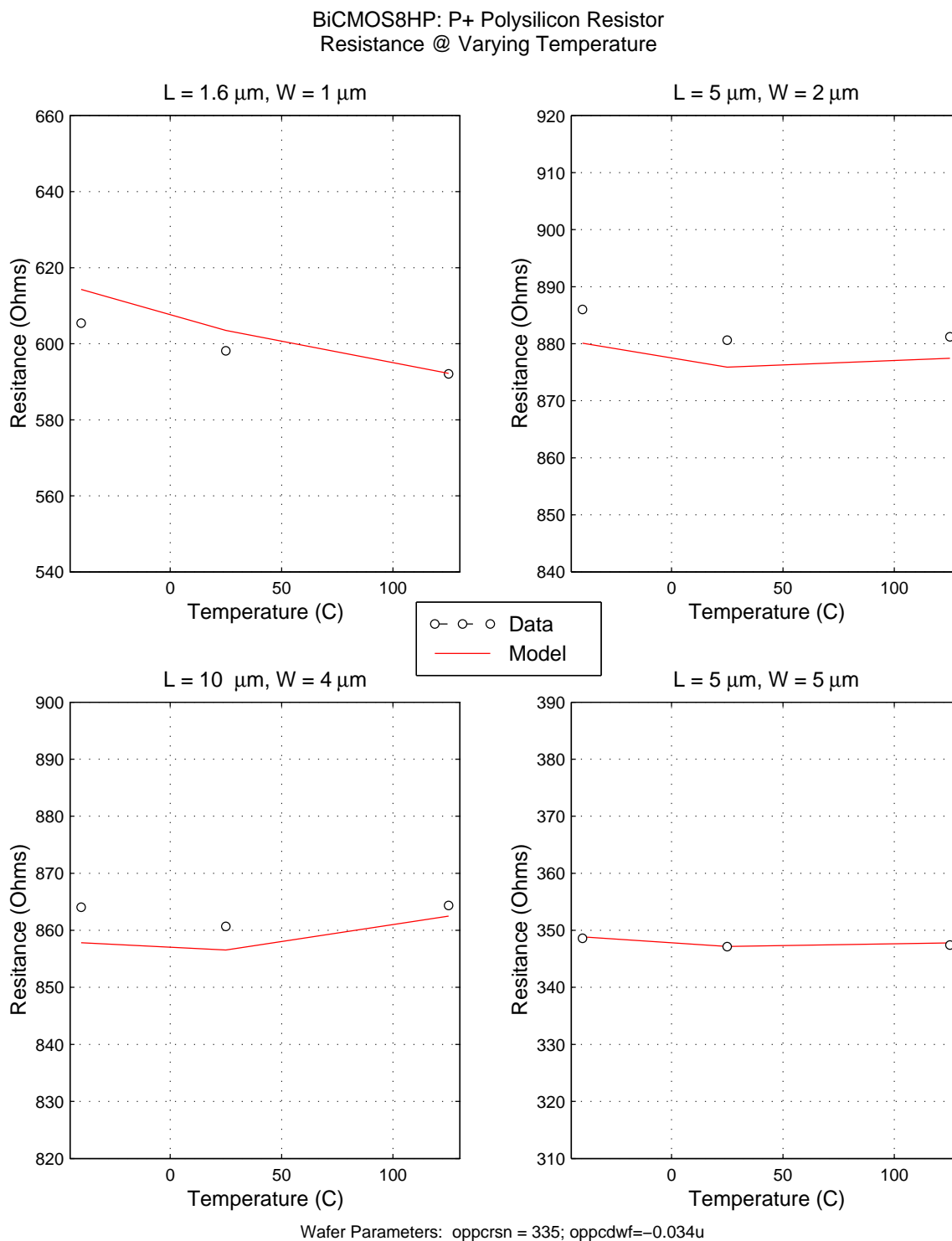


Figure 208. P+ Polysilicon Resistor Temperature Correlation

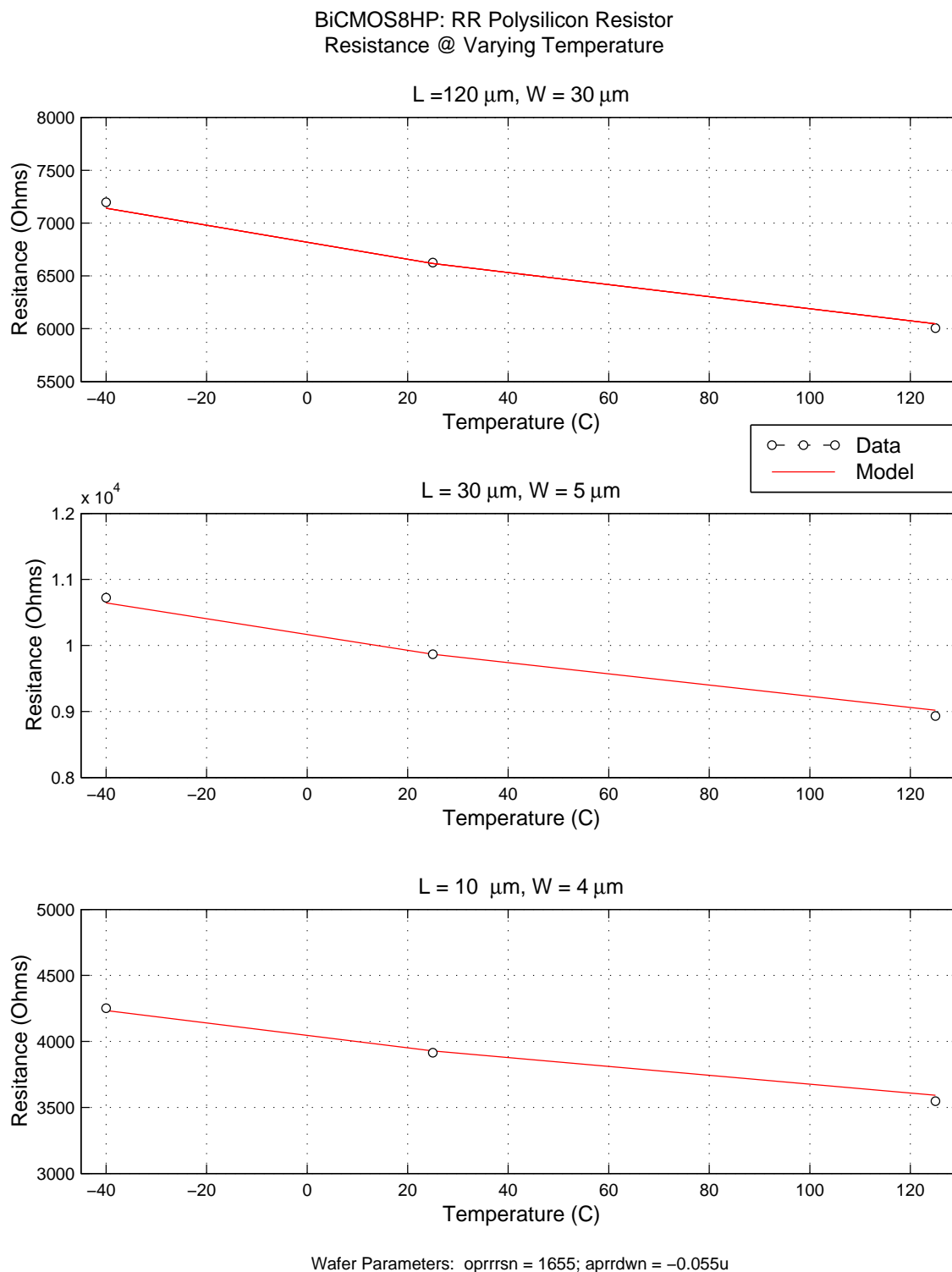


Figure 209. RR Polysilicon Resistor Temperature Correlation

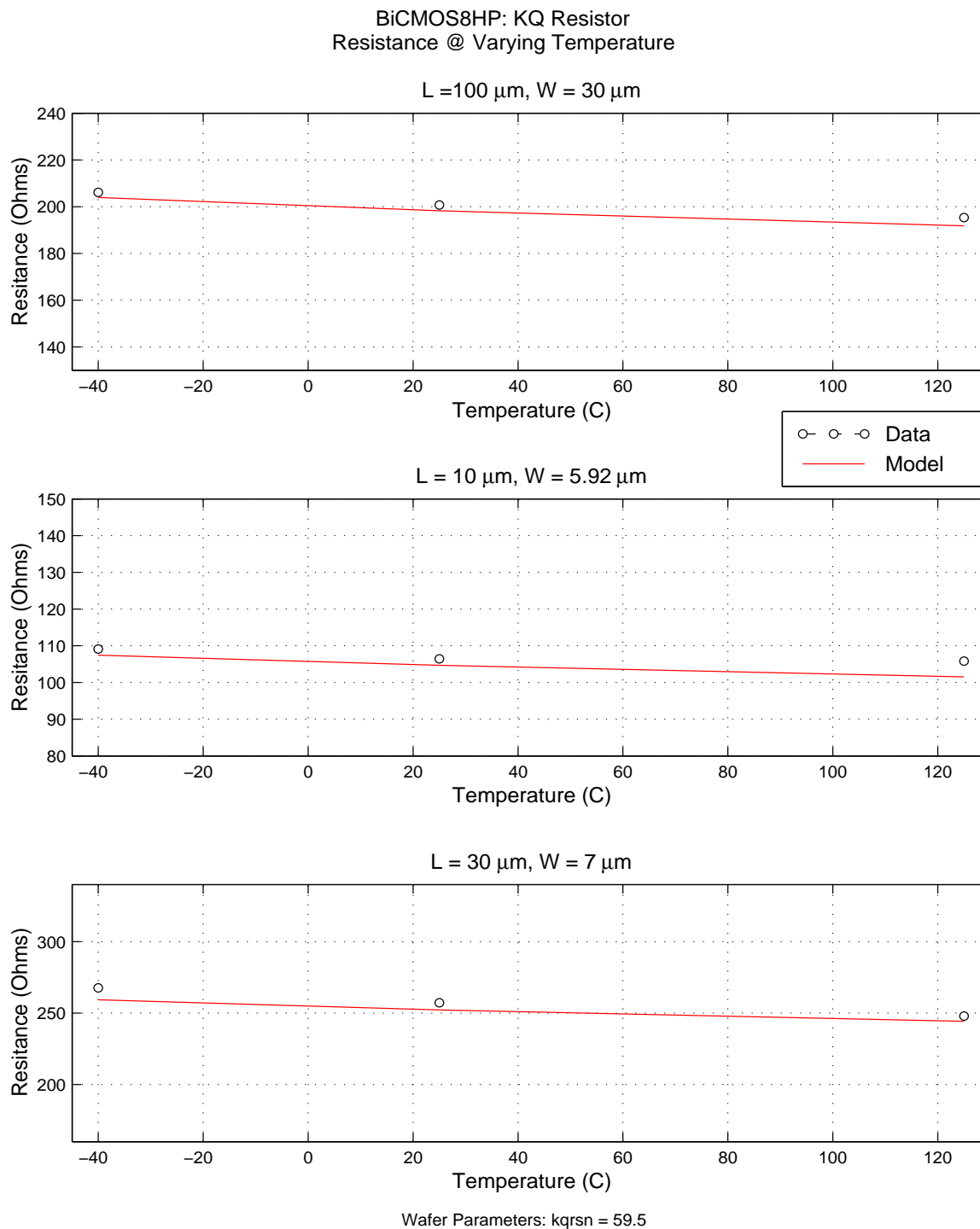


Figure 210. KQ Resistor Temperature Correlation

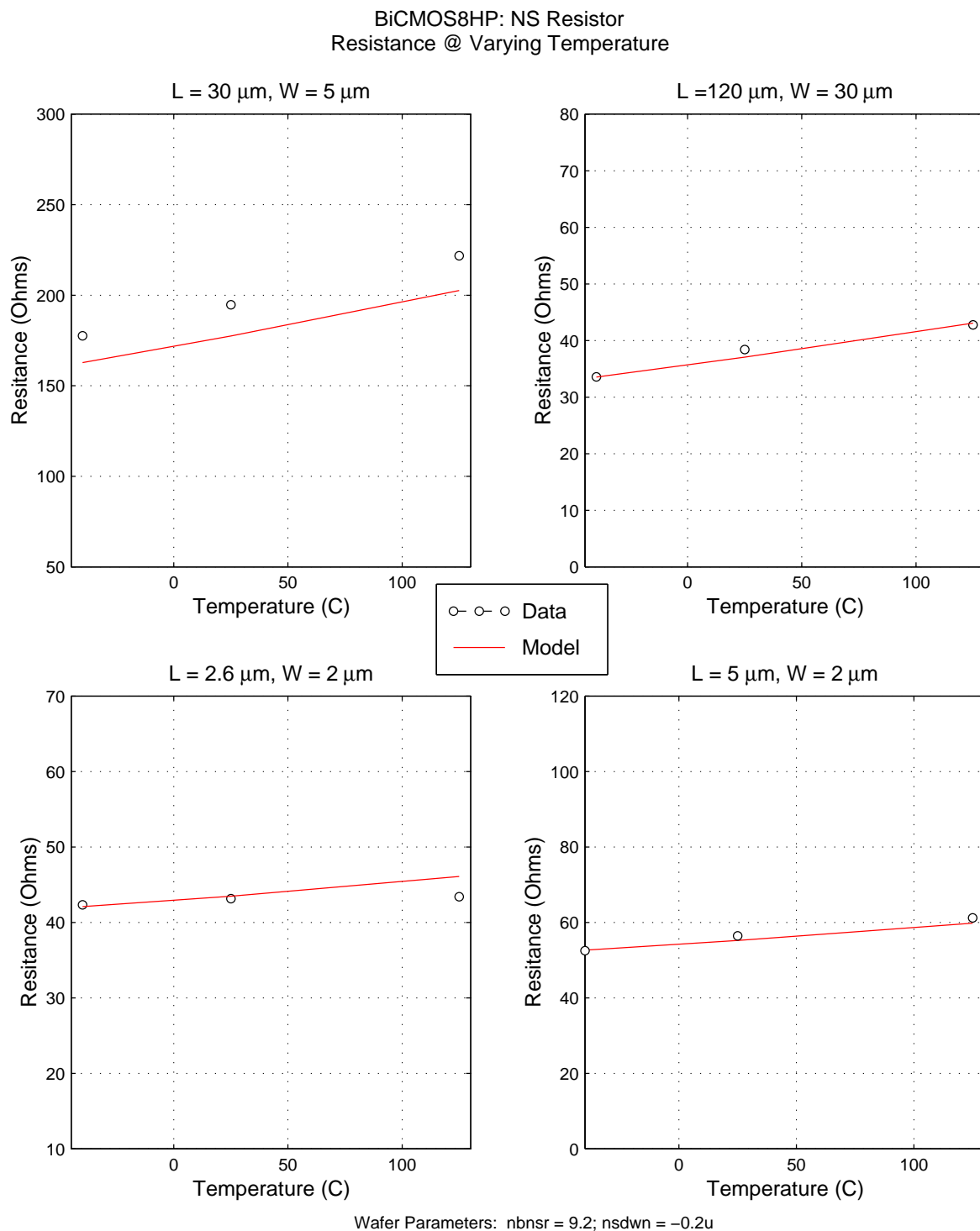


Figure 211. NS Resistor Temperature Correlation

6.4 Resistor Self-Heating Plots

The following plots in **Fig 212** and **Fig 213** compare simulation results with characterization data to demonstrate self-heating effects in the RR polysilicon and KQ BEOL resistors. Self-heating is manifested by the resistance showing a square dependence on the voltage across the resistor.

Resistor simulations were done with some parameters shifted in order to fit the resistance at low voltages. Specific values employed in the simulations are noted on each plot, including the dimensions of the device.

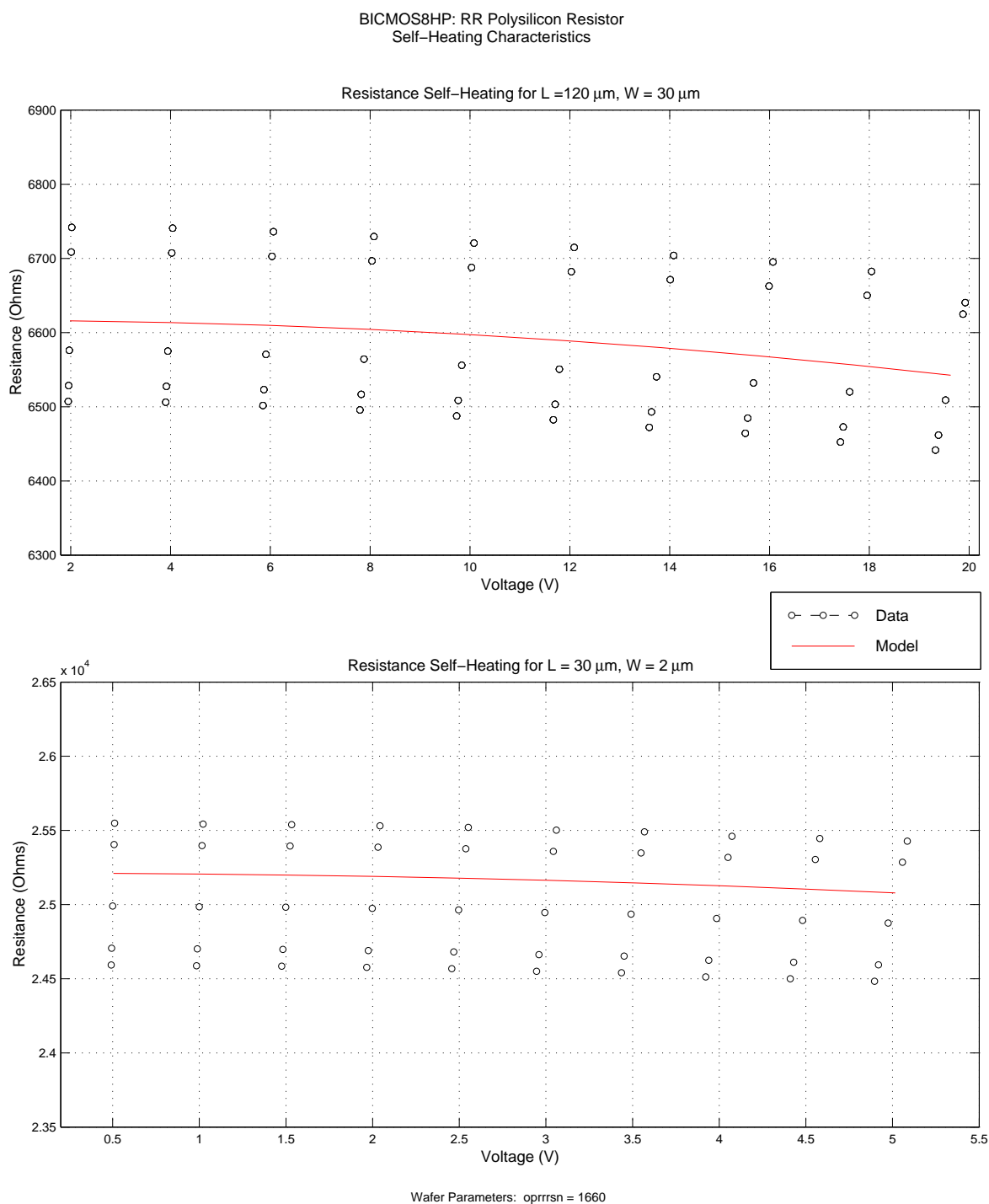


Figure 212. RR Polysilicon Resistor Self-Heating Correlation

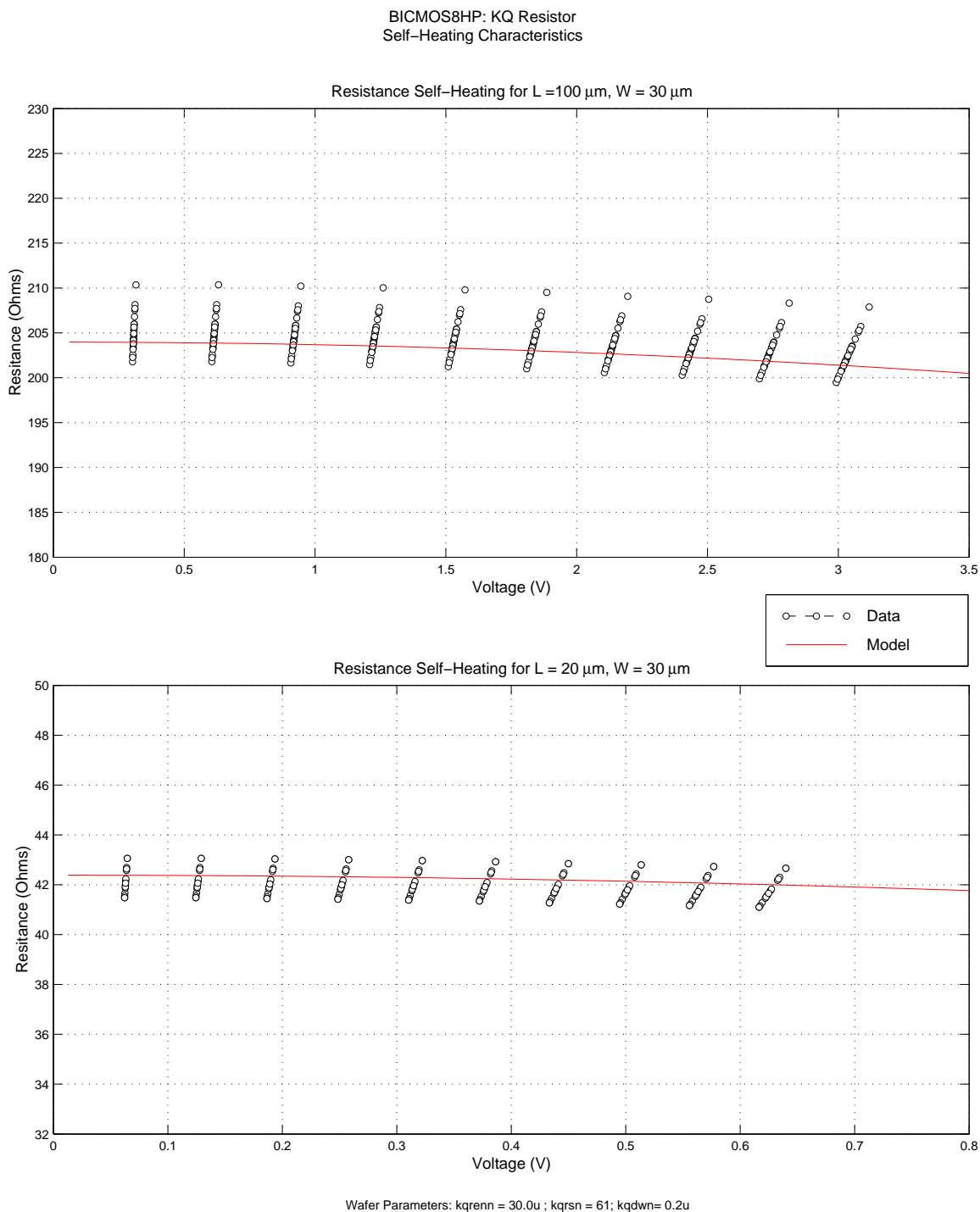


Figure 213. KQ BEOL Resistor Self-Heating Correlation

6.5 Resistor Mis-Match Reference Tables

The following tables provide a comparison of adjacent mis-match for a select set of resistor sizes. The tables also show hardware data results used to set the mis-match scaling in the models.

The data results are based on a sample of 20 sites from each of 2 wafers from 3 standard technology hardware lots. Data analysis programs calculate the mis-match based on the entire set of measured data. These results are in the 'Data Mis-Match' column. The corresponding mis-match calculated from the model is shown in the 'Model Mis-Match' column. Lastly, the low wafer / high wafer 3-sigmas of the data mis-match is given in the 'Data Limits Mis-Match' column.

Note that the general trend of the models is to predict a slightly higher mis-match than the data results. The models have been set to be conservative in this manner due to the small sample size.

Resistor simulations were done with some process parameters shifted so that the resistances are near the center of the measured data. The offsets are the same as were used for the dc correlation table above.

Table 69. P+ Polysilicon Resistor Adjacent Mis-match

Resistor Dimensions (μm) (width x length)	Model Mis-match (%)	Data Mis-Match (%)	Data Limits Mis-Match (%)
30 x 20	0.25	0.28	0.24 / 0.35
10 x 10	0.61	0.54	0.45 / 0.67
4 x 1.6	2.56	2.36	1.98 / 2.94
4 x 10	0.95	1.04	0.87 / 1.29
2 x 20	0.95	0.79	0.66 / 0.99
30 x 30	0.21	0.23	0.19 / 0.28

Table 70. RR Polysilicon Resistor Adjacent Mis-match

Resistor Dimensions (μm) (width x length)	Model Mis-match (%)	Data Mis-Match (%)	Data Limits Mis-Match (%)
30 x 20	0.34	0.40	0.33 / 0.51
10 x 10	0.79	0.74	0.61 / 0.92
4 x 2	3.04	2.71	2.26 / 3.37
4 x 10	1.21	1.13	0.94 / 1.41
2 x 20	1.30	1.22	1.02 / 1.51
0.8 x 2	6.29	5.84	4.88 / 7.25

Table 71. NS Resistor Adjacent Mis-match

Resistor Dimensions (μm) (width x length)	Model Mis-match (%)	Data Mis-Match (%)	Data Limits Mis-Match (%)
10 x 10	1.95	1.89	1.58 / 2.35
4 x 2.6	9.30	6.66	5.57 / 8.27
4 x 10	4.74	5.25	4.39 / 6.51
2 x 20	7.05	6.25	5.23 / 7.76
30 x 30	0.44	0.49	0.41 / 0.61
2 x 2.6	19.57	17.0	14.22 / 21.13

Table 72. KQ BEOL Resistor Adjacent Mis-match

Resistor Dimensions (μm) (width x length)	Model Mis-match (%)	Data Mis-Match (%)	Data Limits Mis-Match (%)
30 x 20	0.08	0.09	0.07 / 0.11
10 x 10	0.19	0.16	0.14 / 0.21
5.92 x 5	0.36	0.35	0.29 / 0.44
5.92 x 20	0.23	0.17	0.14 / 0.21
5.92 x 10	0.26	0.25	0.21 / 0.31
7 x 7	0.27	0.23	0.049 / 0.12

6.6 S-Parameter Correlation Plots

The following examples compare the S-Parameter characteristics of the resistor models with measurement data from the technology qualification hardware. Each of the figures contains plots of resistance (R_{in}) vs frequency from 100MHz to 40GHz.

Resistor simulations were done with some process parameters shifted so that the low frequency resistance and parasitic capacitance are near the center of the measured data. The offsets are the same as were used for the dc correlation table above.

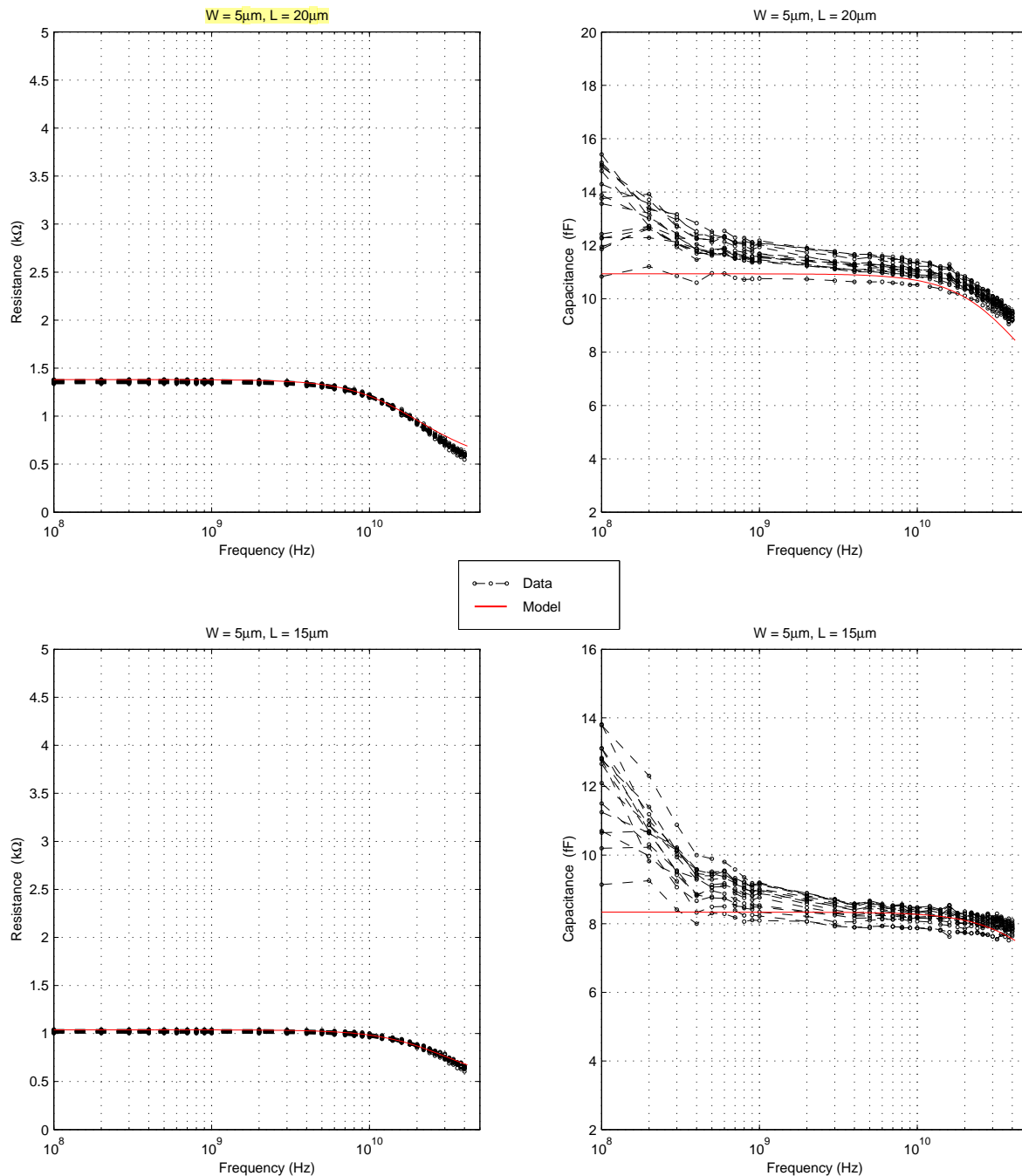
Note the following calculations:

- $R_{in} = \text{real} (1 / Y_{11})$
- $C_{in} = -1 / (\text{imag}(Z_{11}) \times \omega)$

Table 73. Resistor S-Parameter Correlation Plots

Resistor Type (over SX)	W = 5 μ m L = 15 μ m	W = 5 μ m L = 20 μ m	W = 10 μ m L = 50 μ m	W = 30 μ m L = 15 μ m	W = 10 μ m L = 43 μ m	W = 30 μ m L = 8 μ m
P+ Poly	Fig 214	Fig 214	Fig 215	Fig 215		
RR poly	Fig 216	Fig 216	Fig 217	Fig 217		
NS	Fig 218	Fig 218	Fig 219	Fig 219		
KQ BEOL					Fig 220	Fig 220

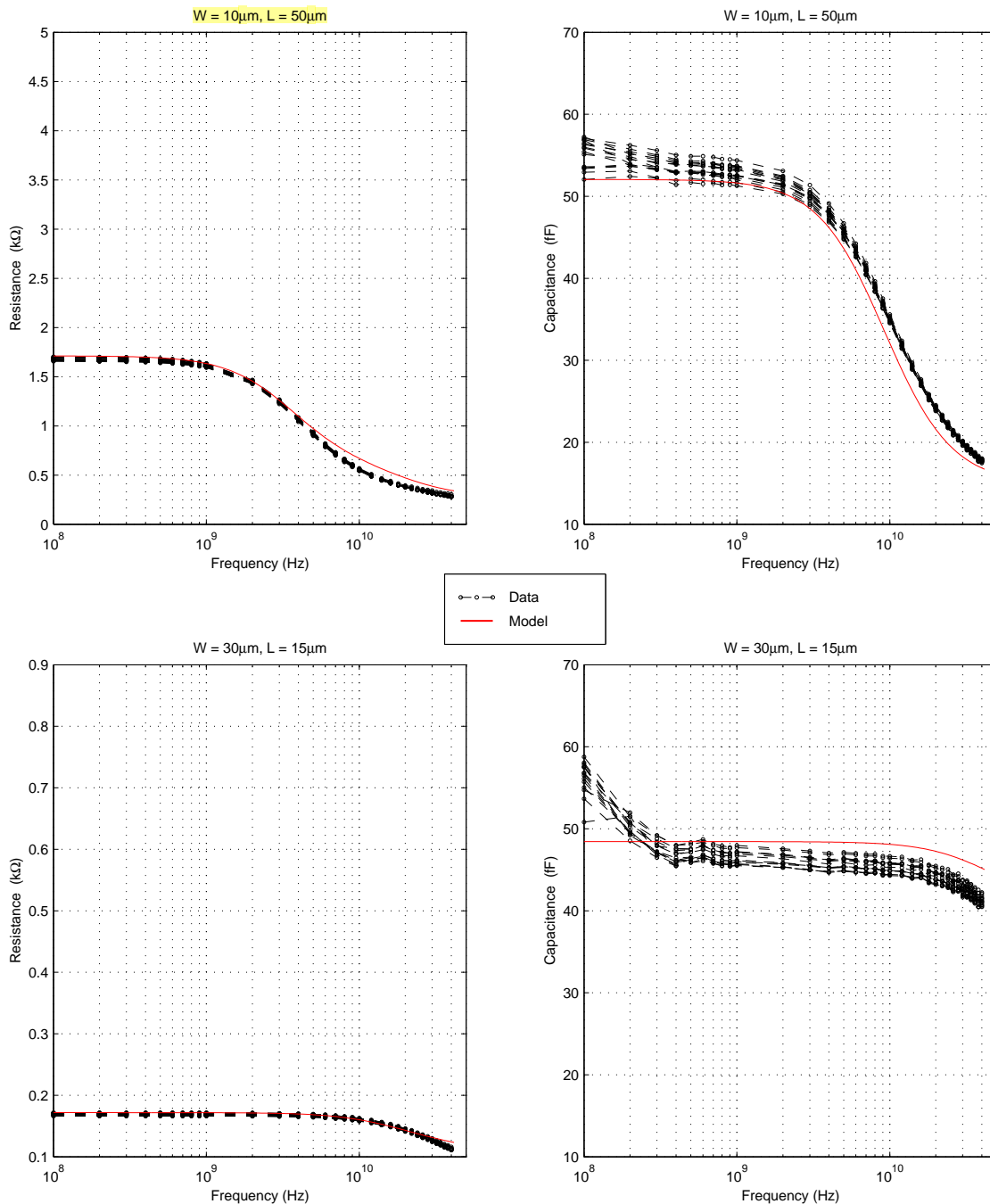
BiCMOS8HP: P+ Polysilicon Resistors
Resistors over SX (T= 25C, Vsx=0)



Wafer Parametrics: oppcdwn = 0.1m oppcfmg = 0.01n

Figure 214. P+ Polysilicon Resistor S-Parameter Correlation, $W \times L = 5\mu\text{m} \times 15\mu\text{m}$, $5\mu\text{m} \times 20\mu\text{m}$

BiCMOS8HP: P+ Polysilicon Resistors
Resistors over SX (T= 25C, V_{sx}=0)



Wafer Parametrics: oppcdwn = 0.1m oppcfrng = 0.01n

Figure 215. P+ Polysilicon Resistor S-Parameter Correlation, WxL=10μmx50μm, 30μmx15μm

BiCMOS8HP: RR Polysilicon Resistors
Resistors over SX (T= 25C, V_{sx}=0)

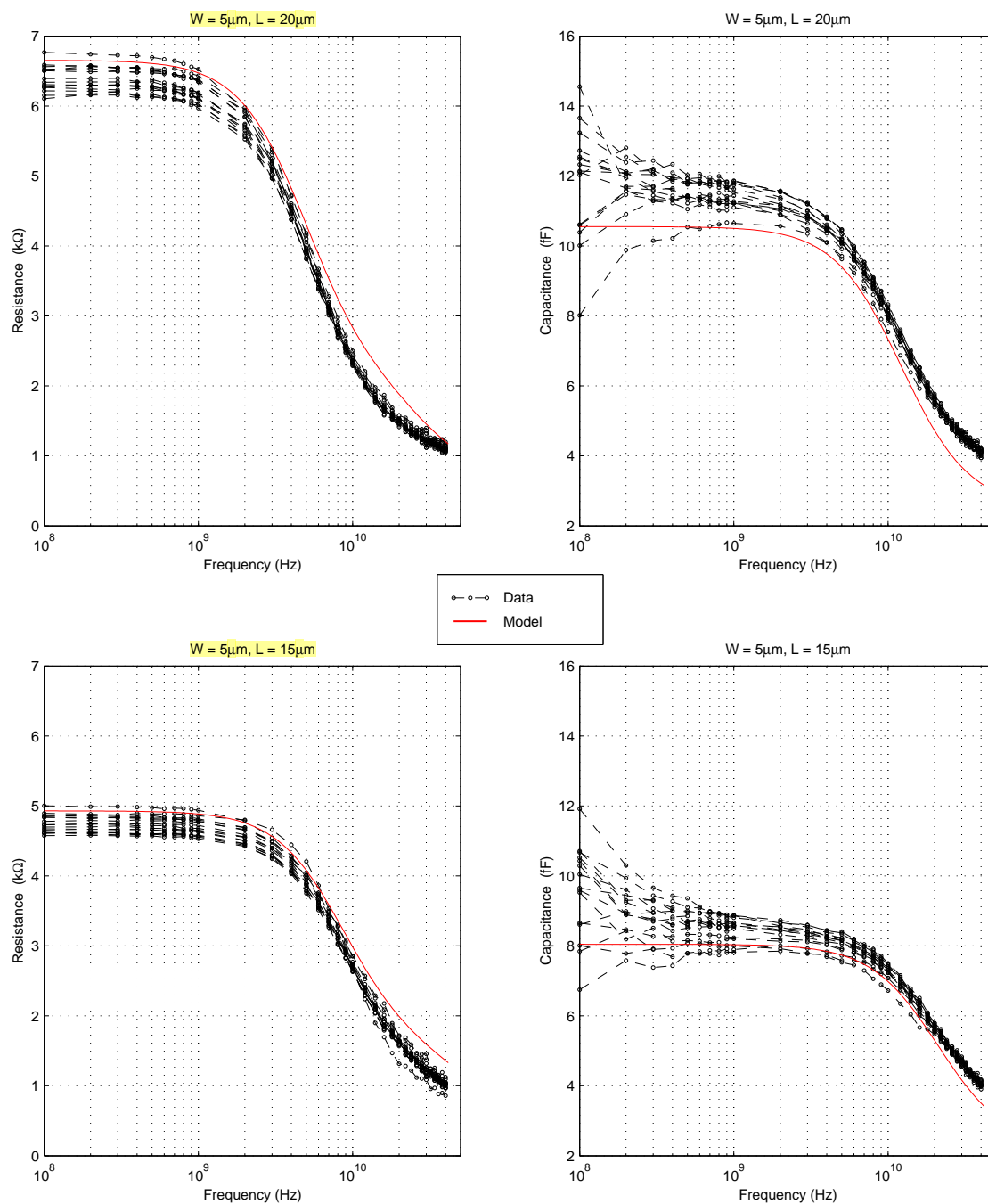


Figure 216. RR Polysilicon Resistor S-Parameter Correlation, $W \times L = 5\mu\text{m} \times 15\mu\text{m}$, $5\mu\text{m} \times 20\mu\text{m}$

BiCMOS8HP: RR Polysilicon Resistors
Resistors over SX (T= 25C, V_{sx}=0)

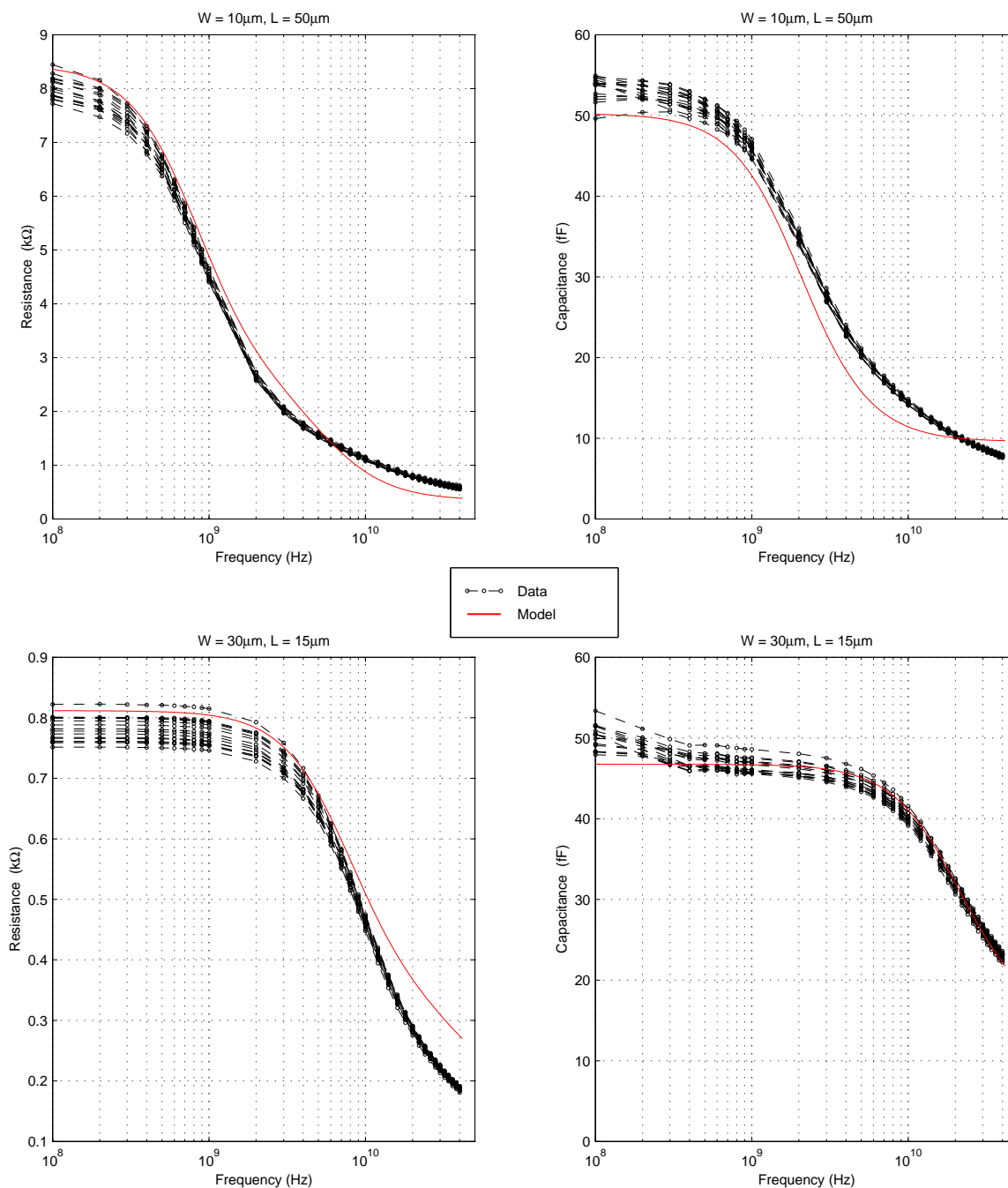


Figure 217. RR Polysilicon Resistor S-Parameter Correlation, $W \times L = 10\mu\text{m} \times 50\mu\text{m}$, $30\mu\text{m} \times 15\mu\text{m}$

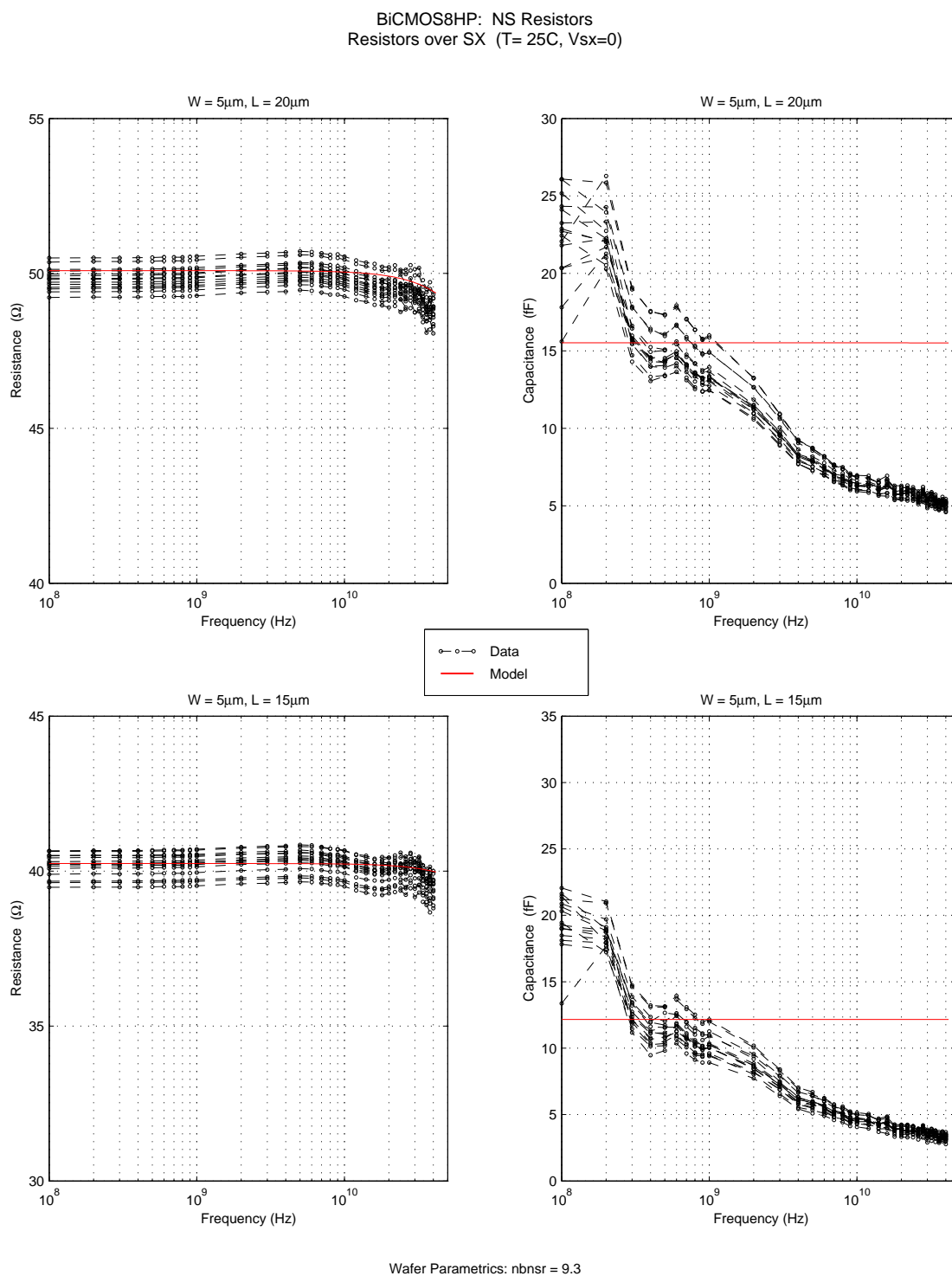


Figure 218. NS Resistor S-Parameter Correlation, WxL=5μm x 15μm, 5μm x 20μm

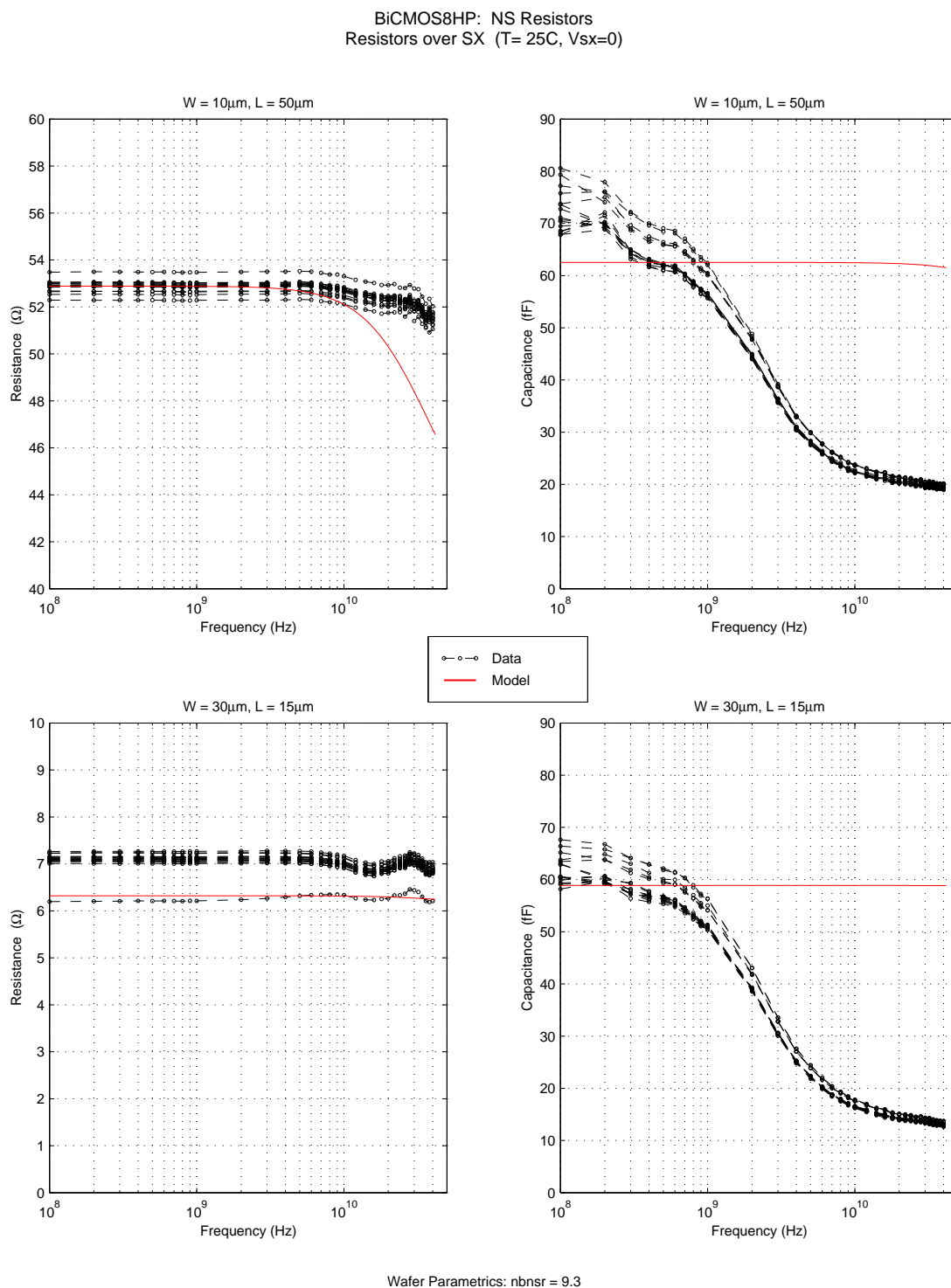


Figure 219. NS Resistor S-Parameter Correlation, WxL=10μm x 50μm, 30μm x 15μm

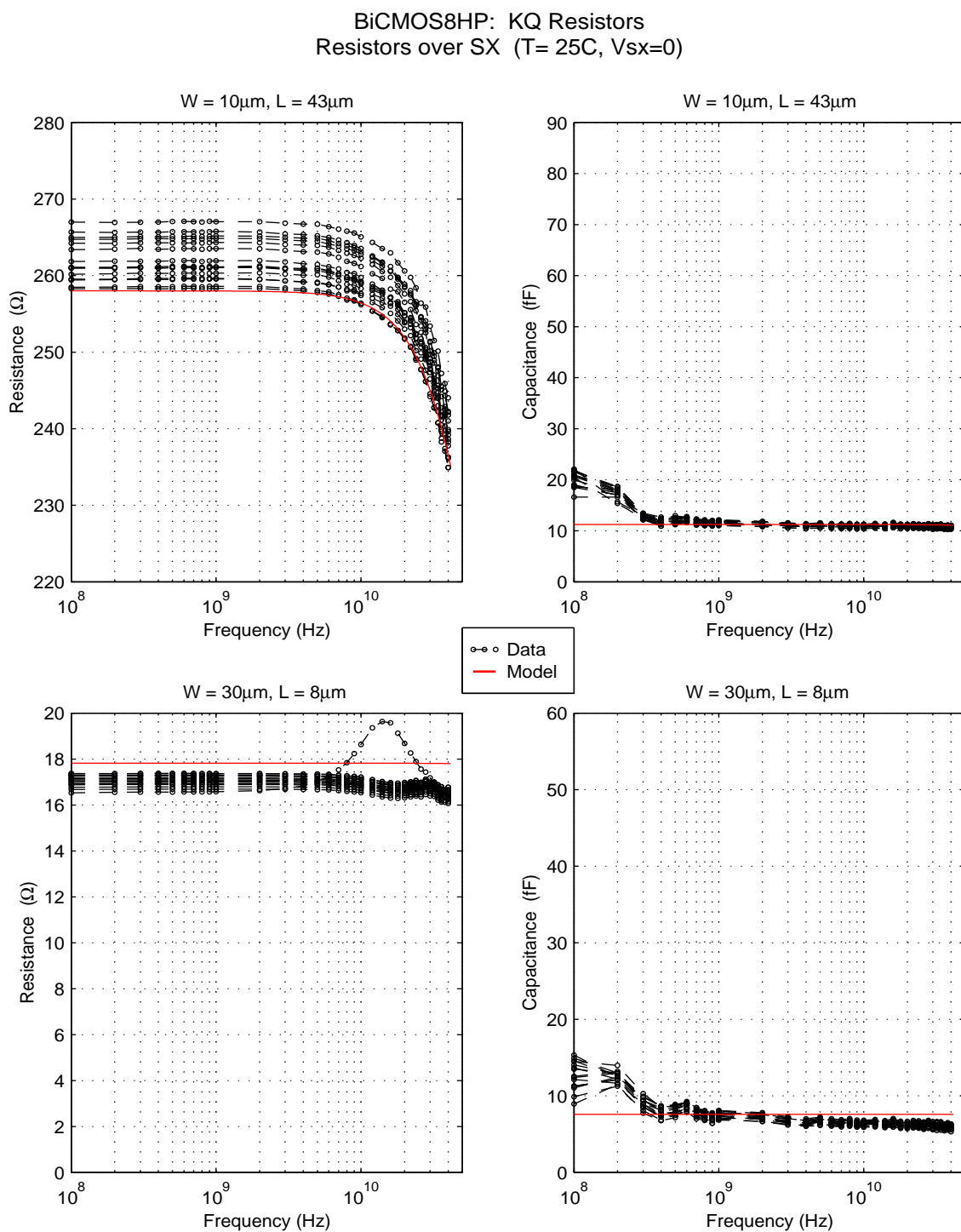


Figure 220. KQ BEOL Resistor S-Parameter Correlation

6.7 Flicker Noise Correlation Plots

The following plots compare the flicker noise characteristics of the resistor models with measurement data from the hardware. Each of the figures contains plots of flicker noise vs. frequency from 1 Hz to 100 kHz, at three biases approximately 50% of maximum current density for the device, 75% of maximum current density for the device and approximately 100% of maximum current density for the device.

BiCMOS8HP: P+ Polysilicon Resistors
Typical 1/f Noise Characteristics @25 C

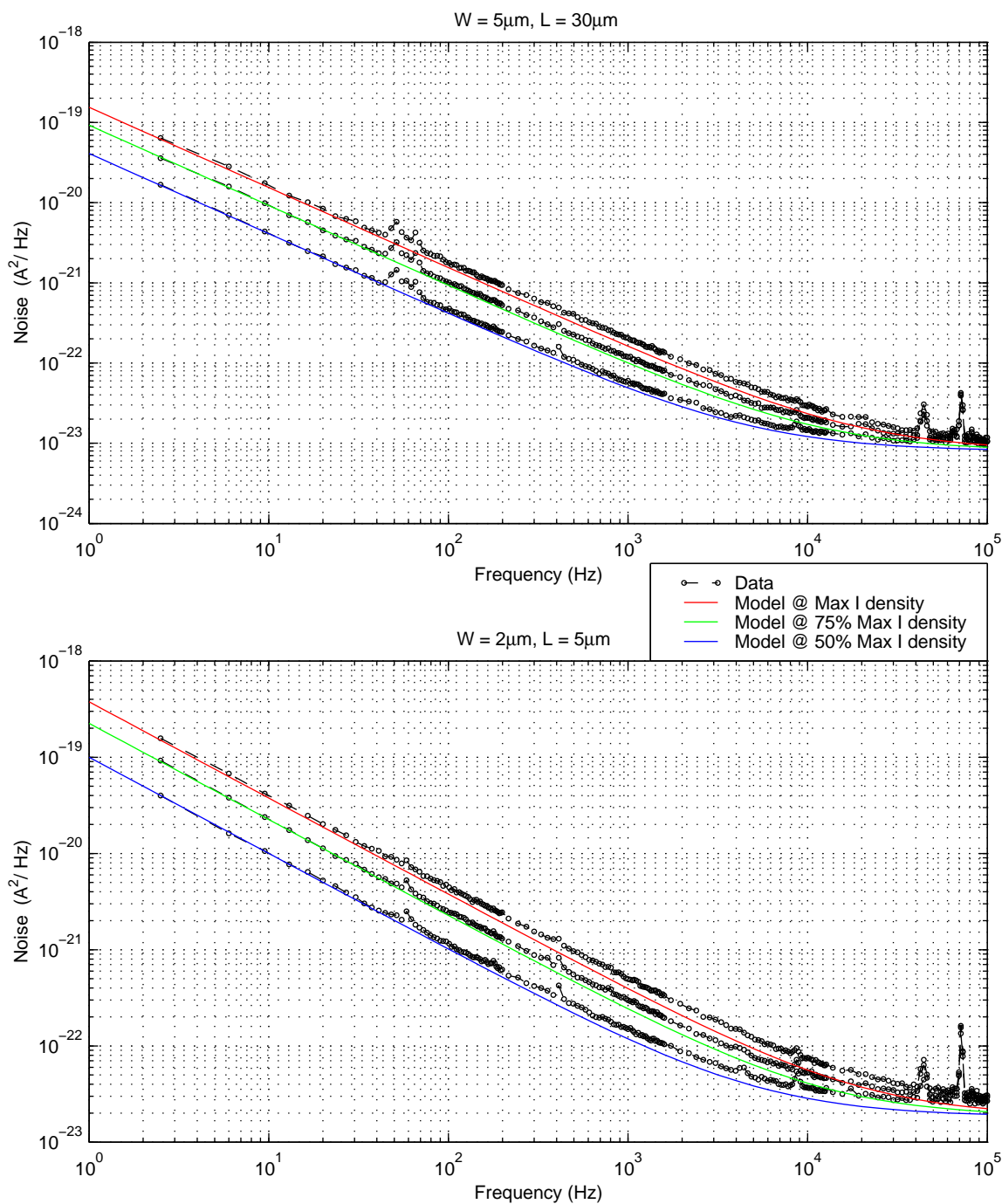


Figure 221. P+ Polysilicon Resistor Flicker (1/f) Noise Correlation

BiCMOS8HP: RR Polysilicon Resistors
Typical 1/f Noise Characteristics @25 C

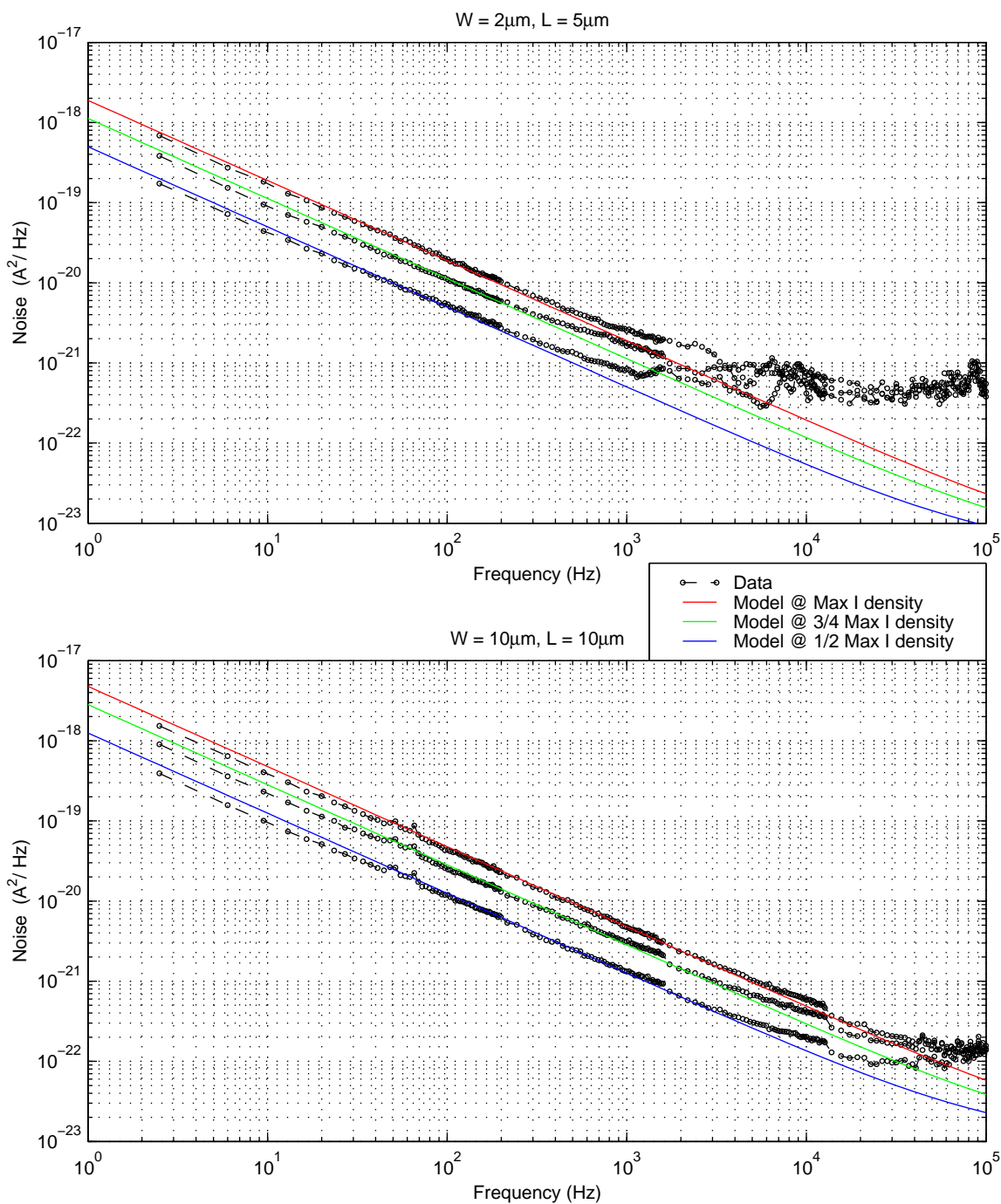


Figure 222. RR Polysilicon Resistor Flicker (1/f) Noise Correlation

BiCMOS8HP: NS Resistors
Typical 1/f Noise Characteristics @25 C

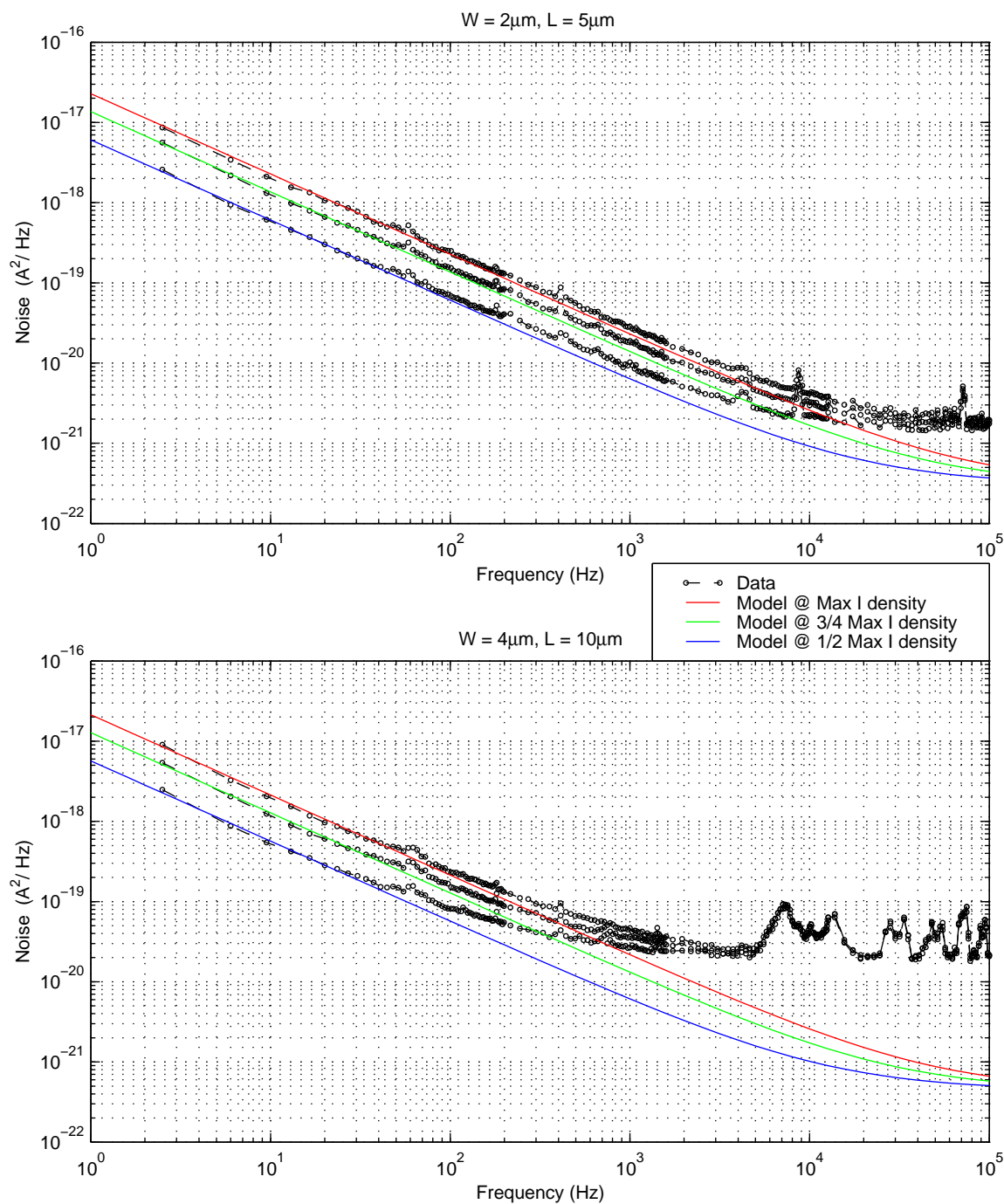


Figure 223. NS Resistor Flicker (1/f) Noise Correlation

BiCMOS8HP: KQ Resistors
Typical 1/f Noise Characteristics @25 C

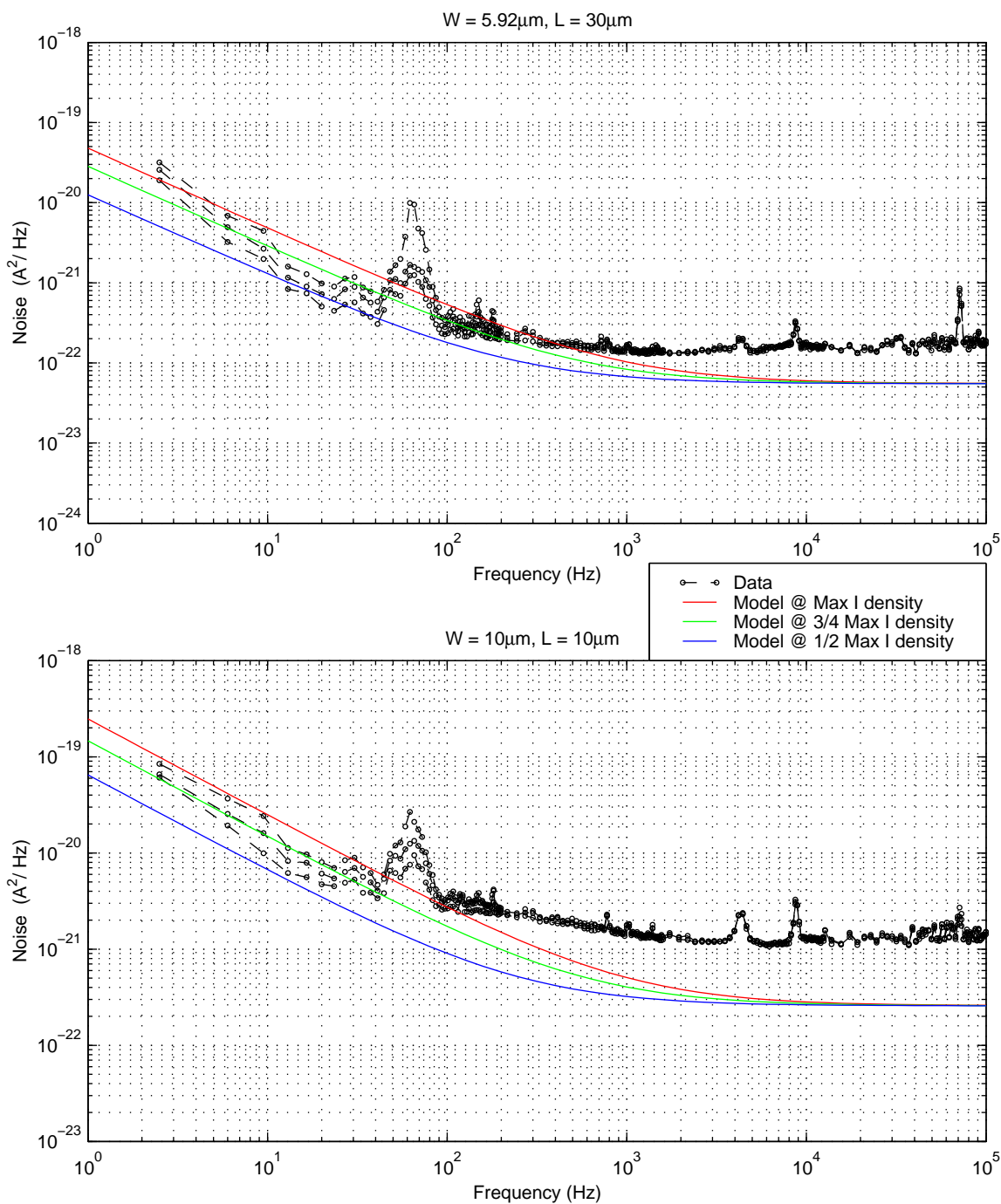


Figure 224. KQ BEOL Resistor Flicker (1/f) Noise Correlation

7.0 nMOS Varactor Model

7.1 Model Features

The thin oxide (ncap) and thick oxide (dgncap) nMOS varactor models include:

- Input parameter specification for width, length, nf (# of gates per diffusion) and nrep (# of diffusions).
- User-defined substrate resistance (rsx) based on layout (default=50 ohms).
- Device temperature difference with respect to circuit temperature (dtemp).
- The ncap model includes gate leakage current effects. The gate leakage current is found to be negligible in the dgncap. Temperature effects on gate leakage are not included.

7.2 Model Limitations and Restrictions

Known limitations of the nMOS varactor models:

- The model only supports rectangular gate areas (PC - RX intersect area). Bent gates or other irregular layouts are not supported.
- The model does not take into account any parasitic inductance introduced by the metal lines connecting to the gates or by those connecting to the source/drains. This must be supplied by the user.
- The model fit has been optimized in the bias range between $V_{g-sd} = -0.5V$ and $V_{g-sd} = +1.0V$. Outside this range, in the regions of deep inversion (due to unstable capacitance caused by hole generation) and strong accumulation (due to polysilicon depletion effect), the model is not valid.
- The models use VerilogA components to determine the primary capacitance (not fringe terms) in these devices.

7.3 Model Correlation Plots

The correlation plots for ncap on the following pages show several aspects of the thin oxide nMOS varactor model. **Fig 225** and **Fig 226** show several standard Capacitance versus Gate Voltage plots for various thin oxide device sizes. **Fig 227** and **Fig 228** are similar plots for various device sizes of the thick oxide nMOS varactor. For these measurements, the N-well is grounded and the substrate is floating. These plots include temperature variation for the model simulations.

Fig 229-231 show S-Parameter correlation plots for a variety of thin oxide device sizes with a gate voltage of -0.5 V, 0.0 V, and 1.0 V. Similar plots for some thick oxide device sizes are shown in **Fig 233-235** with a gate voltage of -0.5 V, 0.0 V, and 2.0 V. The resonance in the C_{in} versus frequency plots results from the inductance in the wiring both internal and external to the varactor.

Note the following calculation for the S-Parameter correlation plots (port 1 = gate):

- $C_{in} = (\text{imag}(Y_{11})/\omega)$
- $Q = \text{imag}(Y_{11})/\text{real}(Y_{11})$.

There is a resistance and inductance that is associated with the wiring that is used in the simulations shown in the S-parameter correlation plots. The inductance is a result of the wiring internal to the p-cell. The values used in the simulation were chosen empirically by fitting the resonance shown in the data. The resistance included in the model is that coming from the M1 strips that connect either the gates or the source/drains together. The M1 resistance that has been added for the simulations is that due to the M1 strips on the sides of the device that either connect all the gate M1 lines together or all the source/drain M1 lines together. These were not included in the model as the resistance of these lines depends upon how the device is wired to the rest of a design.

The plots in **Fig 232** shows the gate leakage current for four different ncap devices. Note that the gate leakage current is observed to be negligible for the dgncap device.

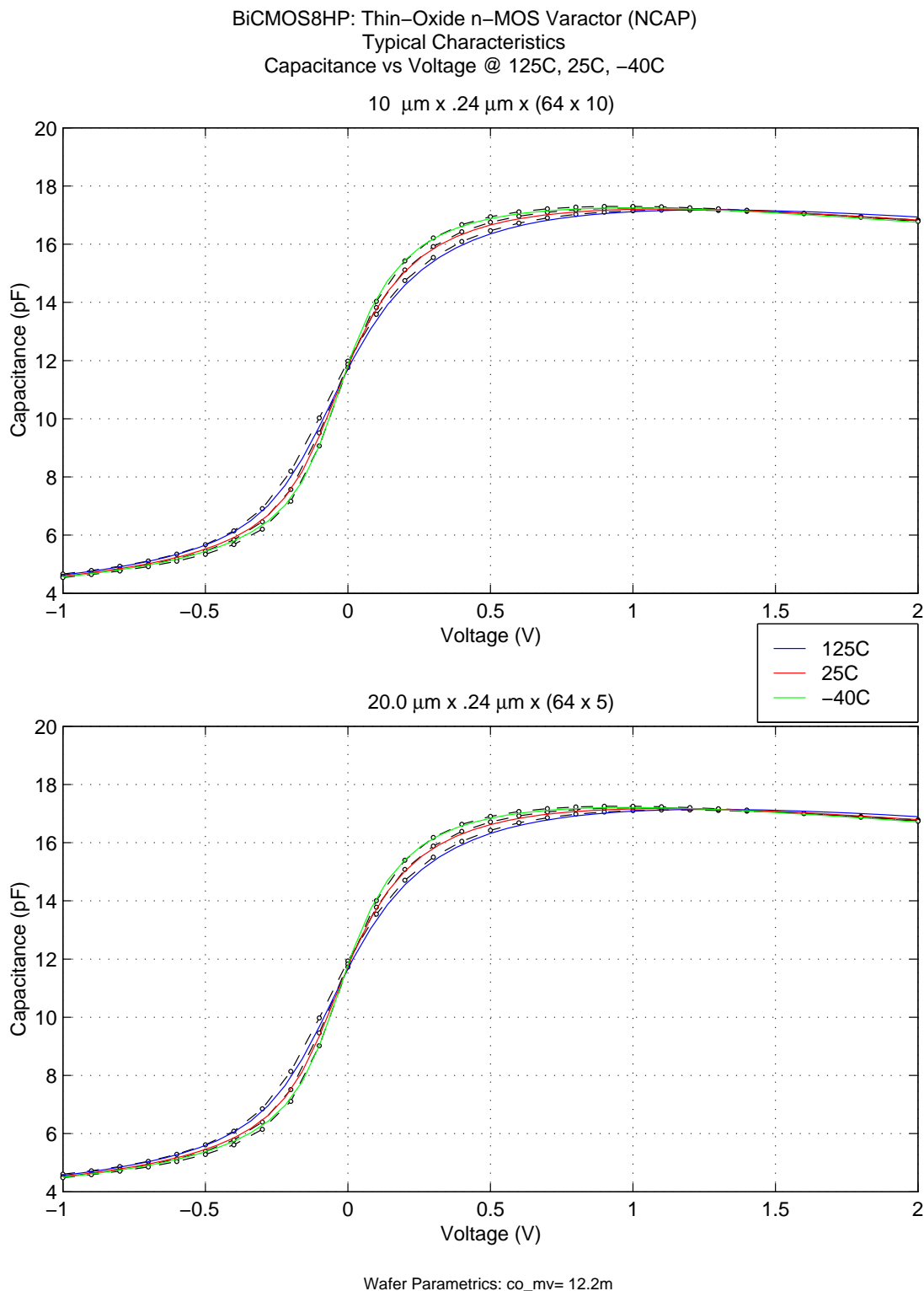


Figure 225. Thin Oxide nMOS Varactor Capacitance versus Voltage Characteristics, $L=0.24\mu\text{m}$

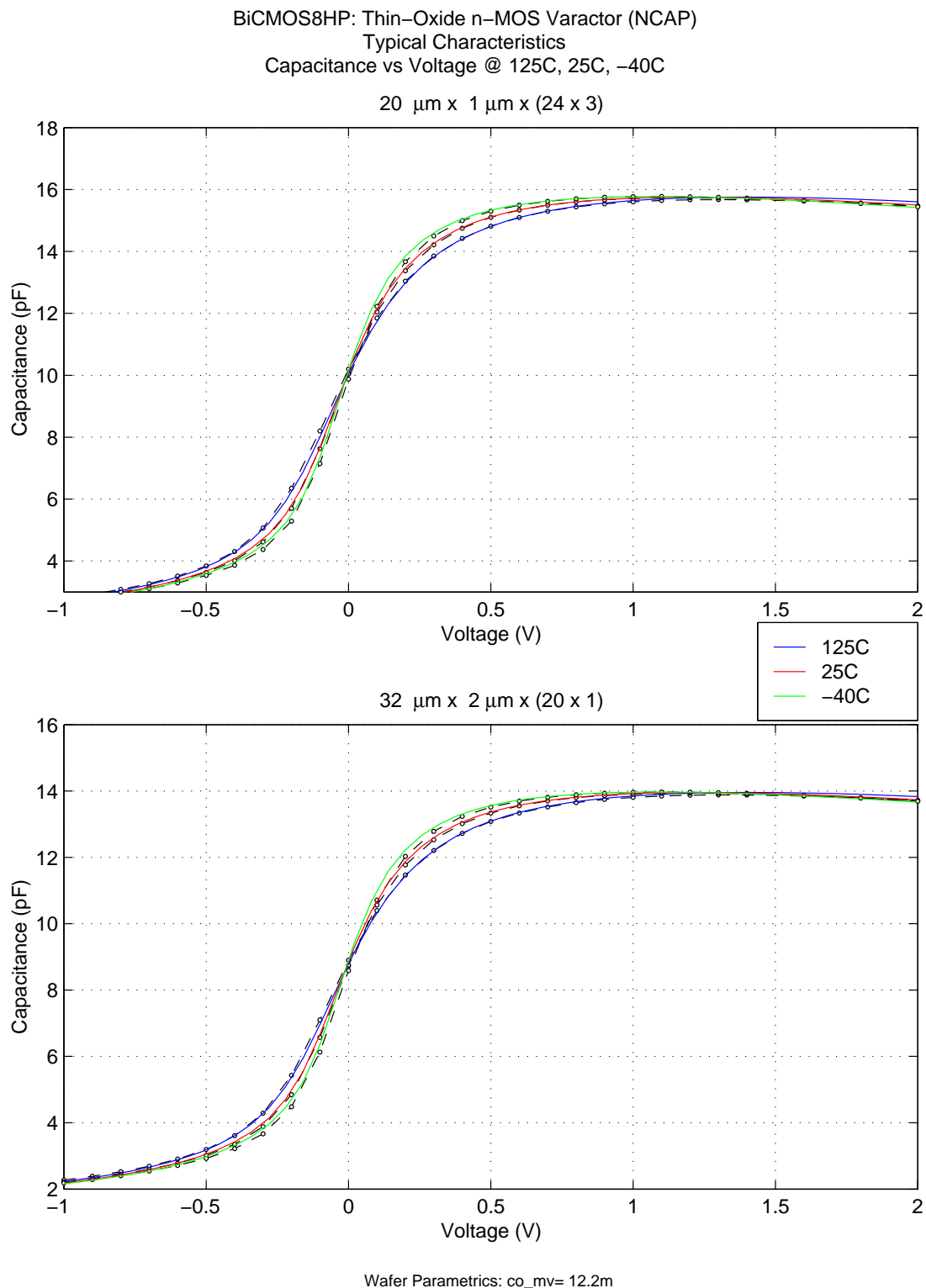


Figure 226. Thin Oxide nMOS Varactor Capacitance versus Voltage Characteristics, $L=1.0, 2.0\mu\text{m}$

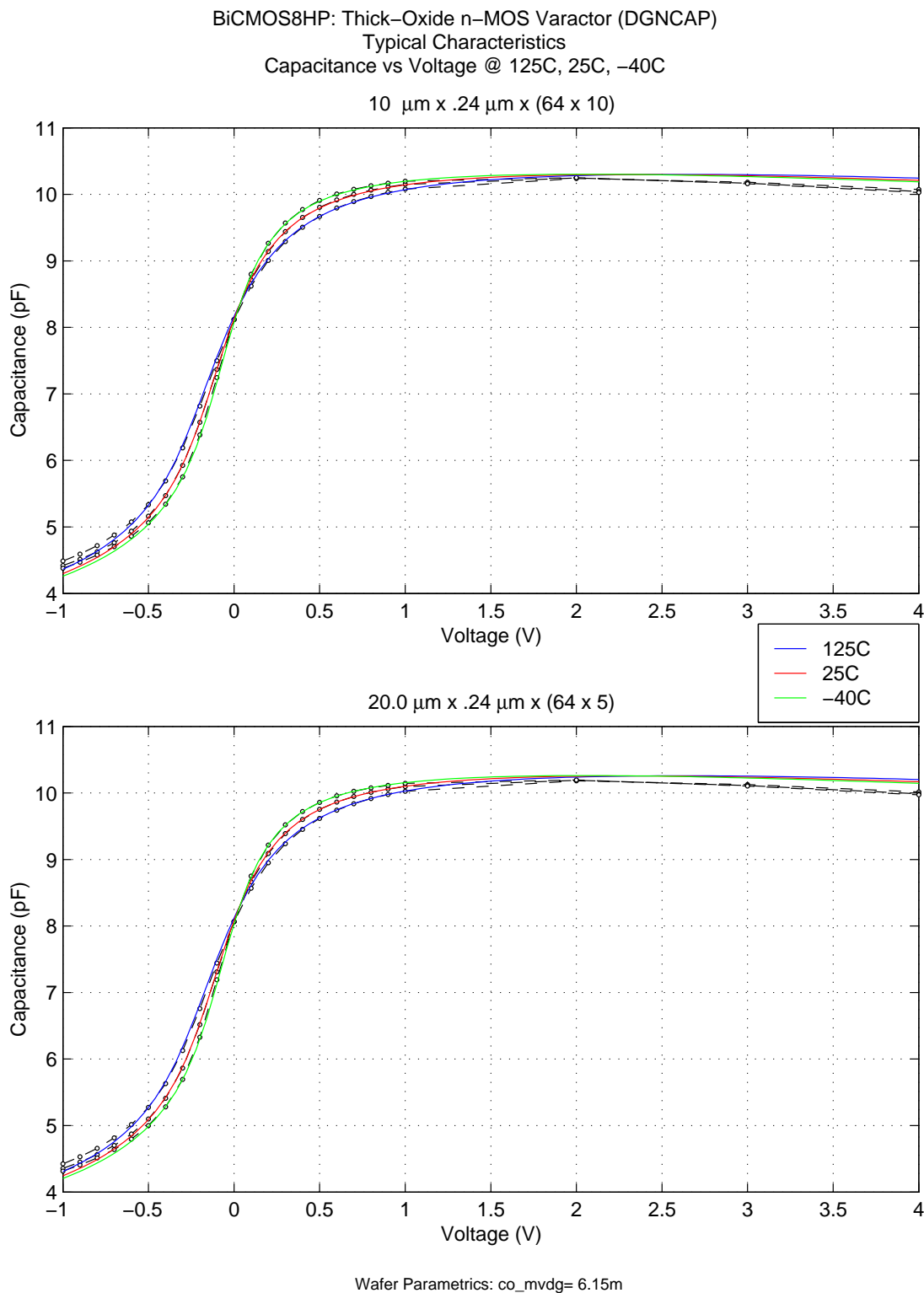


Figure 227. Thick Oxide nMOS Varactor Capacitance versus Voltage Characteristics, $L=0.24\mu\text{m}$

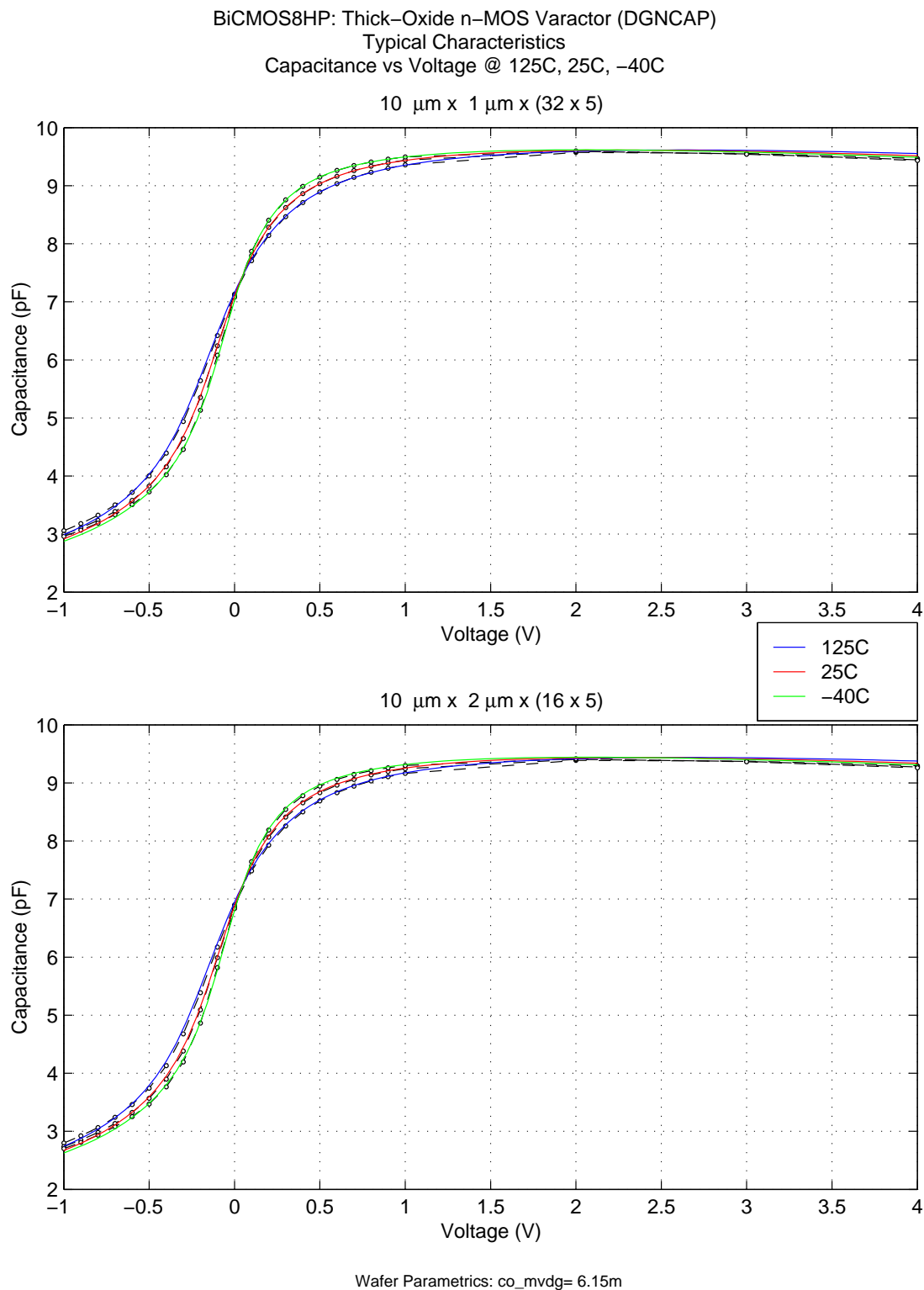


Figure 228. Thick Oxide nMOS Varactor Capacitance versus Voltage Characteristics, $L=1.0, 2.0\mu\text{m}$

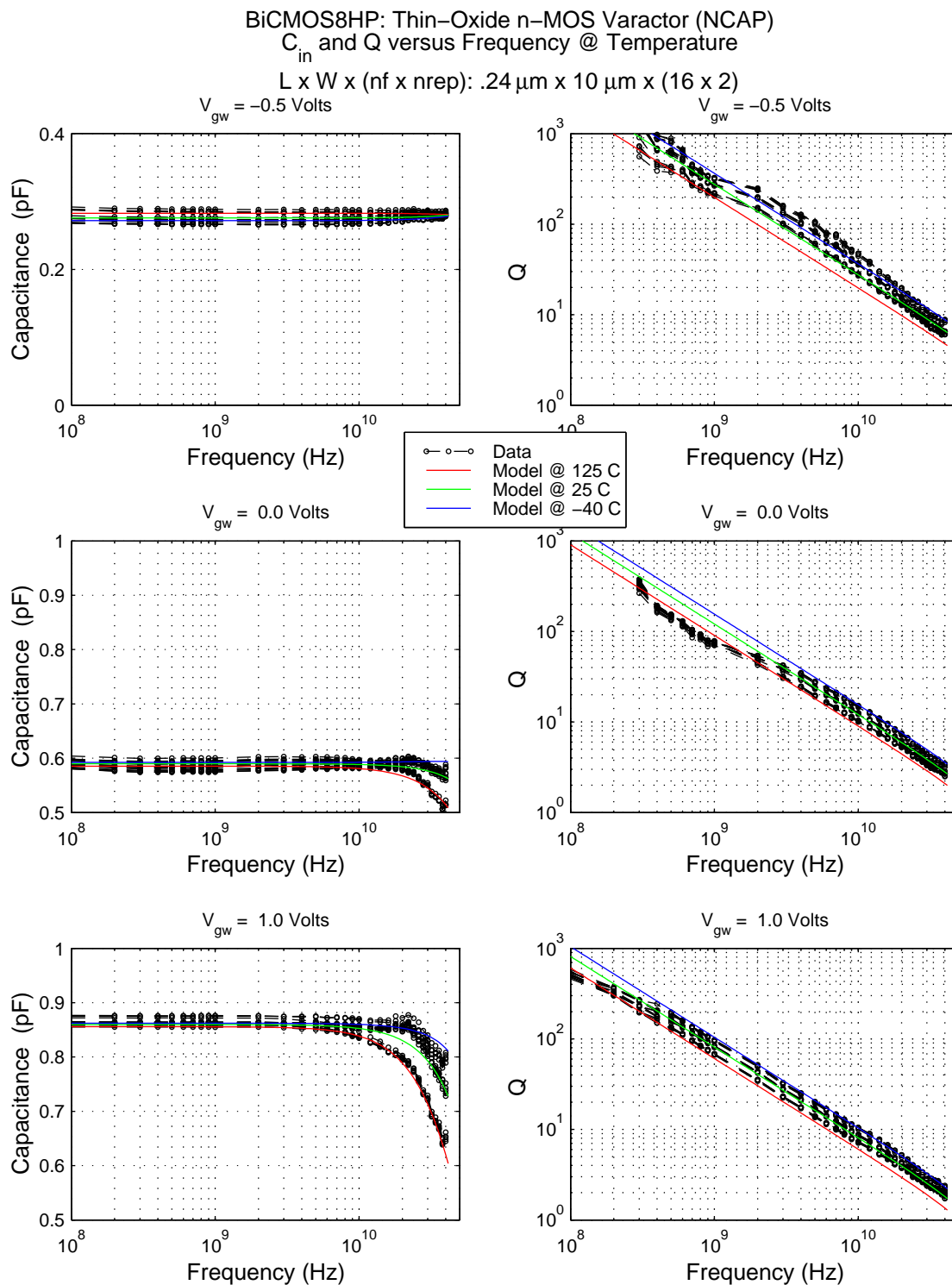


Figure 229. Thin Oxide nMOS Varactor S-Parameters C_{in} and Q versus Frequency, $L=0.24 \mu\text{m}$

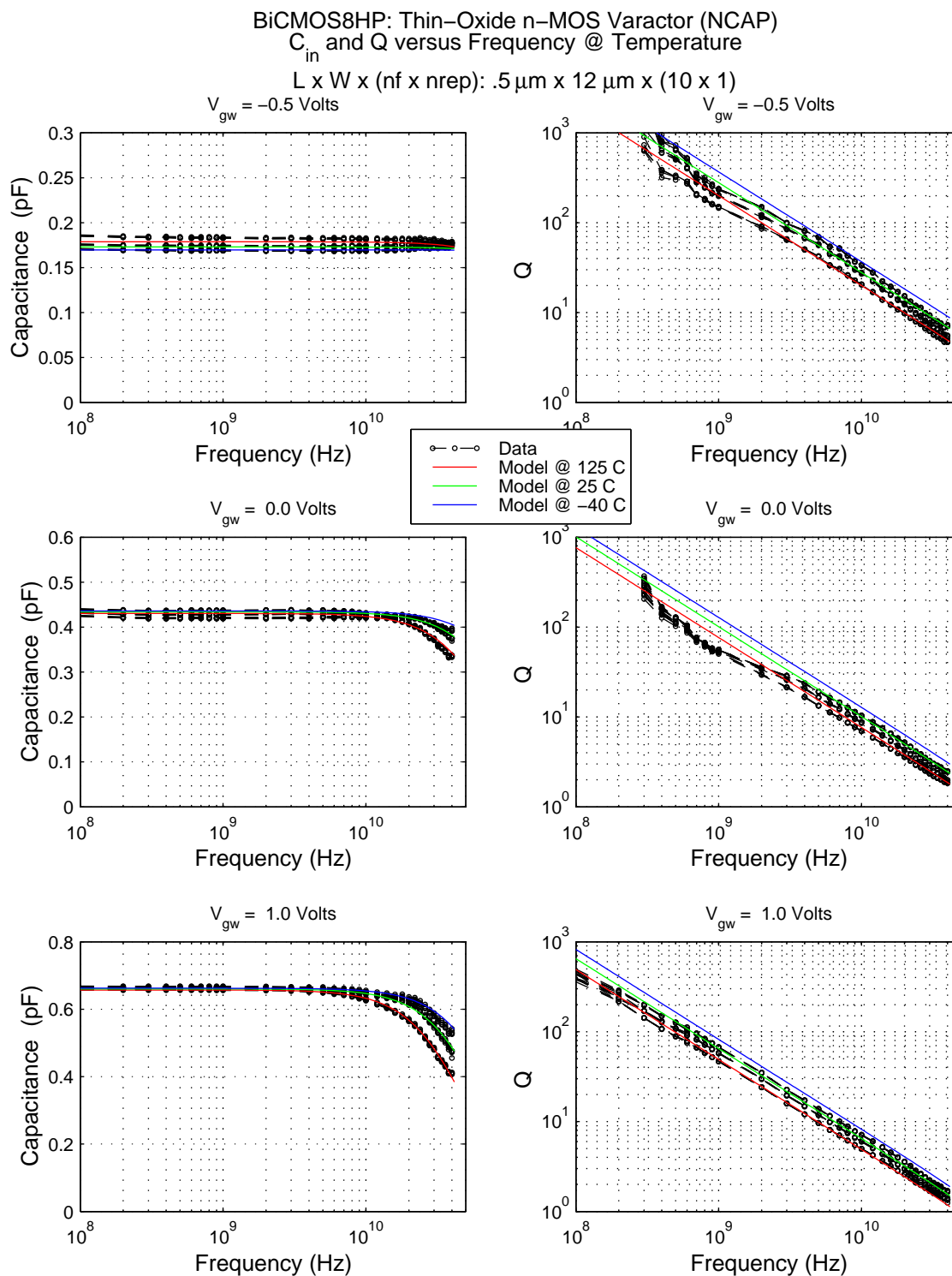


Figure 230. Thin Oxide nMOS Varactor S-Parameters C_{in} and Q versus Frequency, L=0.5 μ m

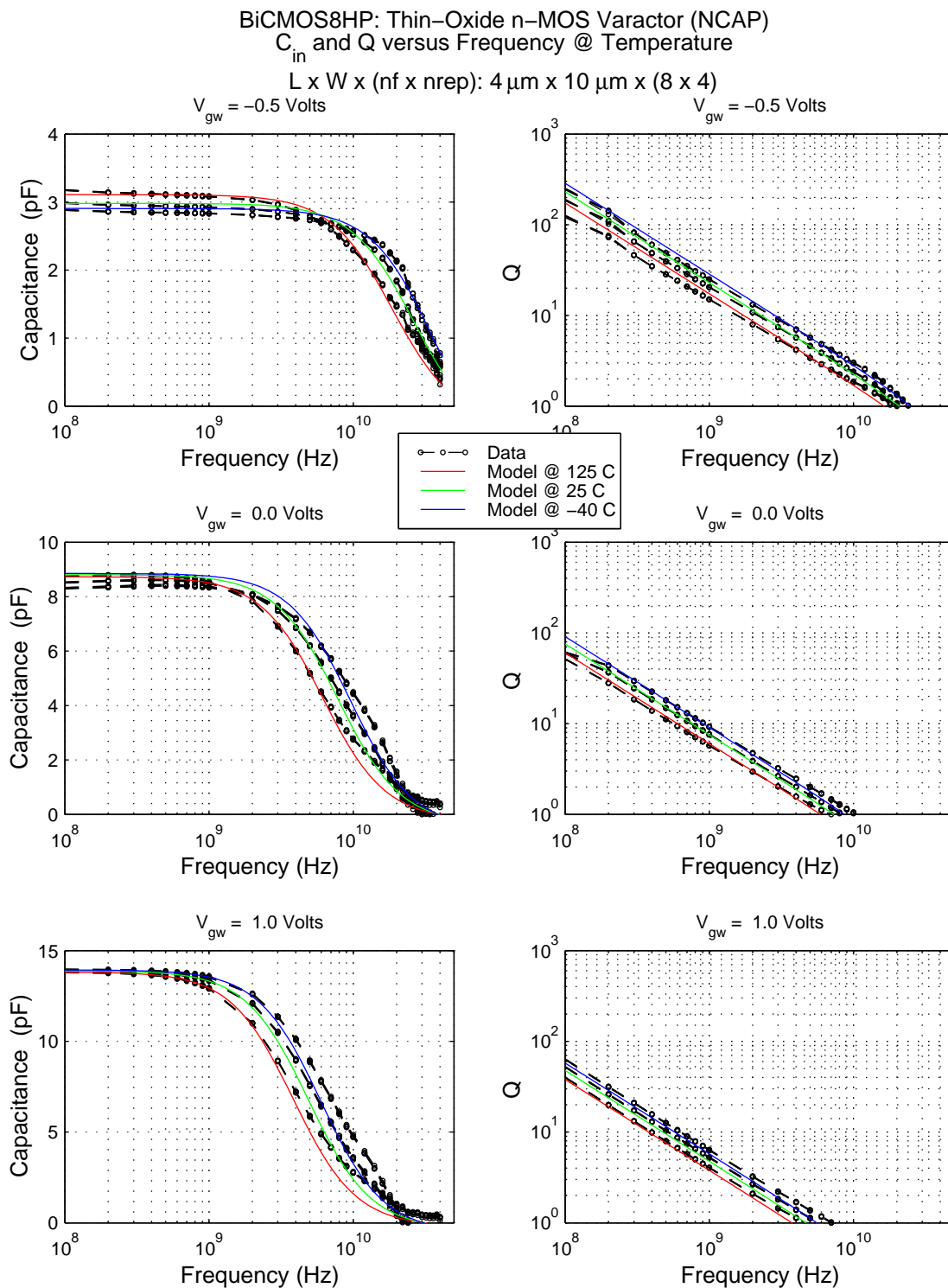


Figure 231. Thin Oxide nMOS Varactor S-Parameters C_{in} and Q versus Frequency, L=4.0 μm

BiCMOS8HP: Thin-Oxide Varactor (NCAP)
Leakage Current Characteristics @ 25 C
Device Sizes : L x W x (nf x nrep)

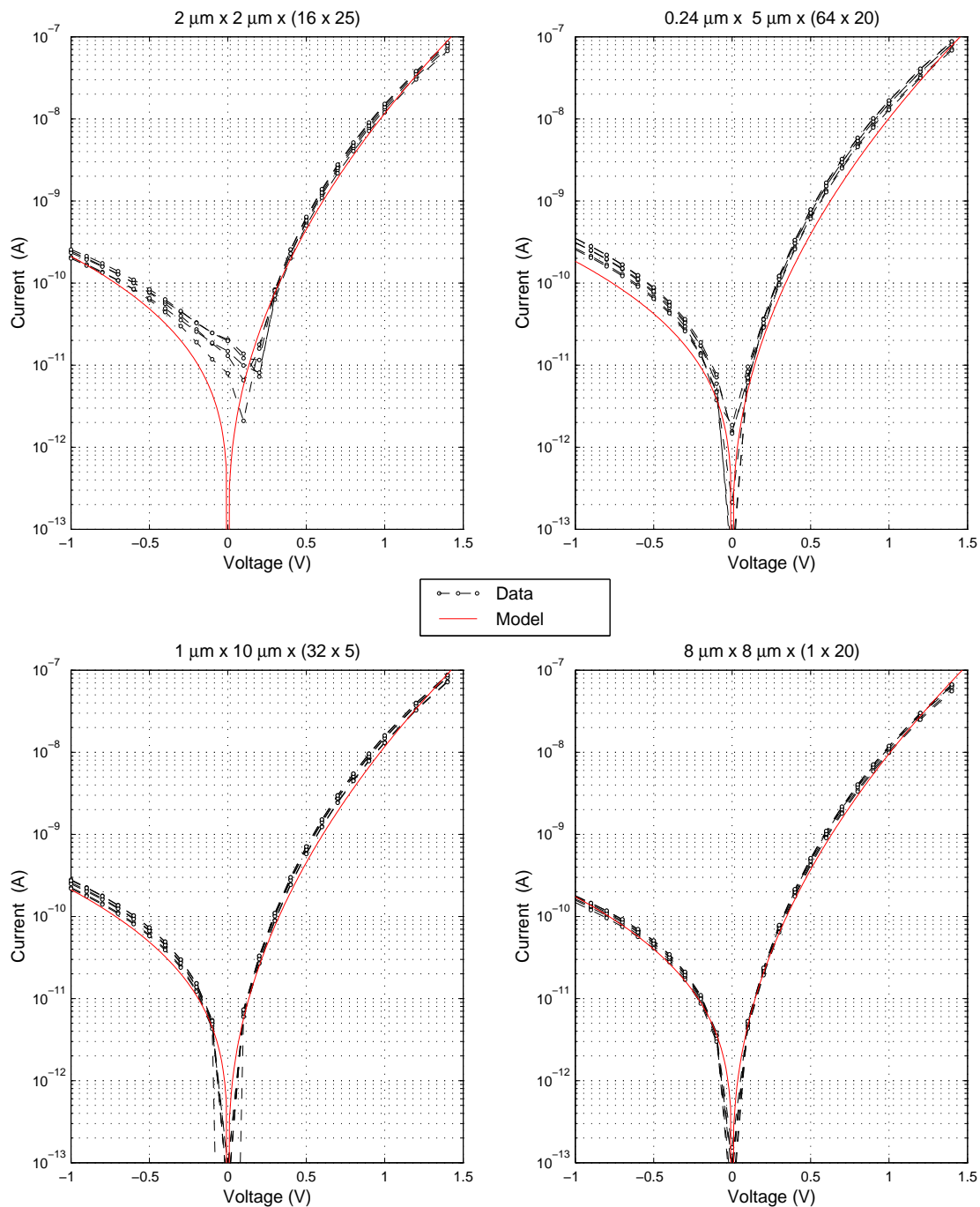


Figure 232. Thin Oxide nMOS Gate Leakage current versus Bias

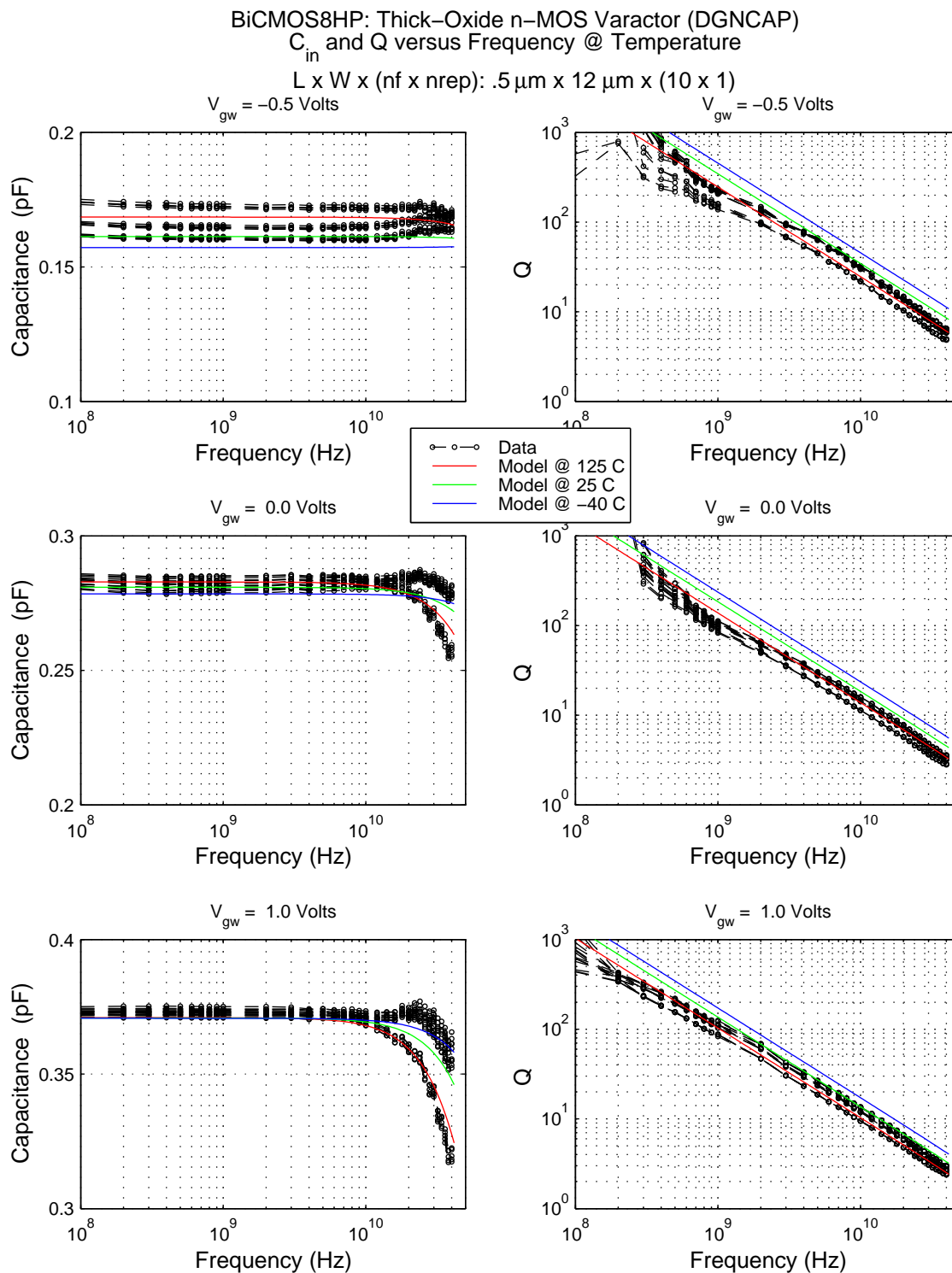


Figure 233. Thick Oxide nMOS Varactor S-Parameters C_{in} and Q versus Frequency, $L=0.5\ \mu\text{m}$

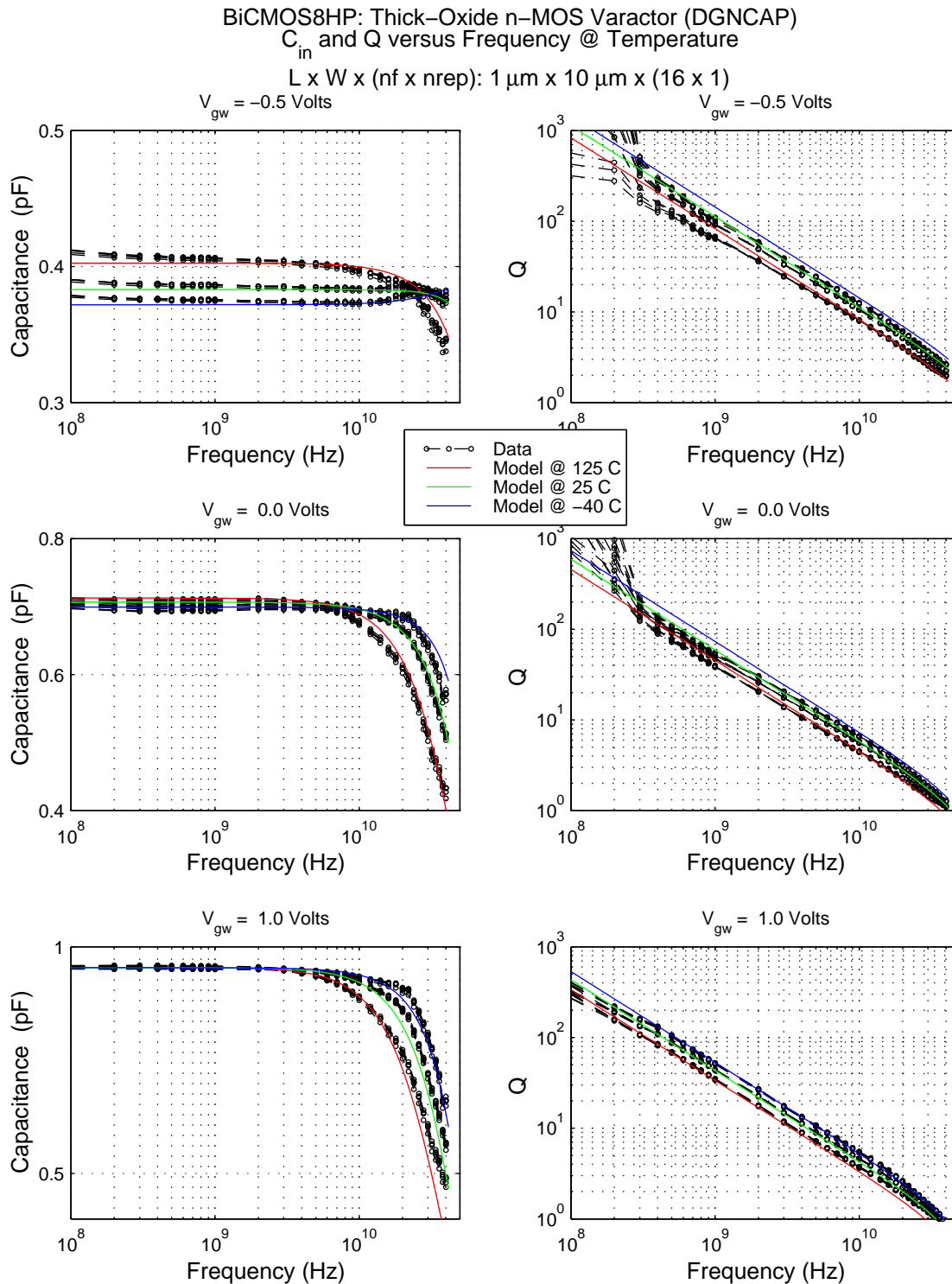


Figure 234. Thick Oxide nMOS Varactor S-Parameters C_{in} and Q versus Frequency, $L=1.0\mu\text{m}$

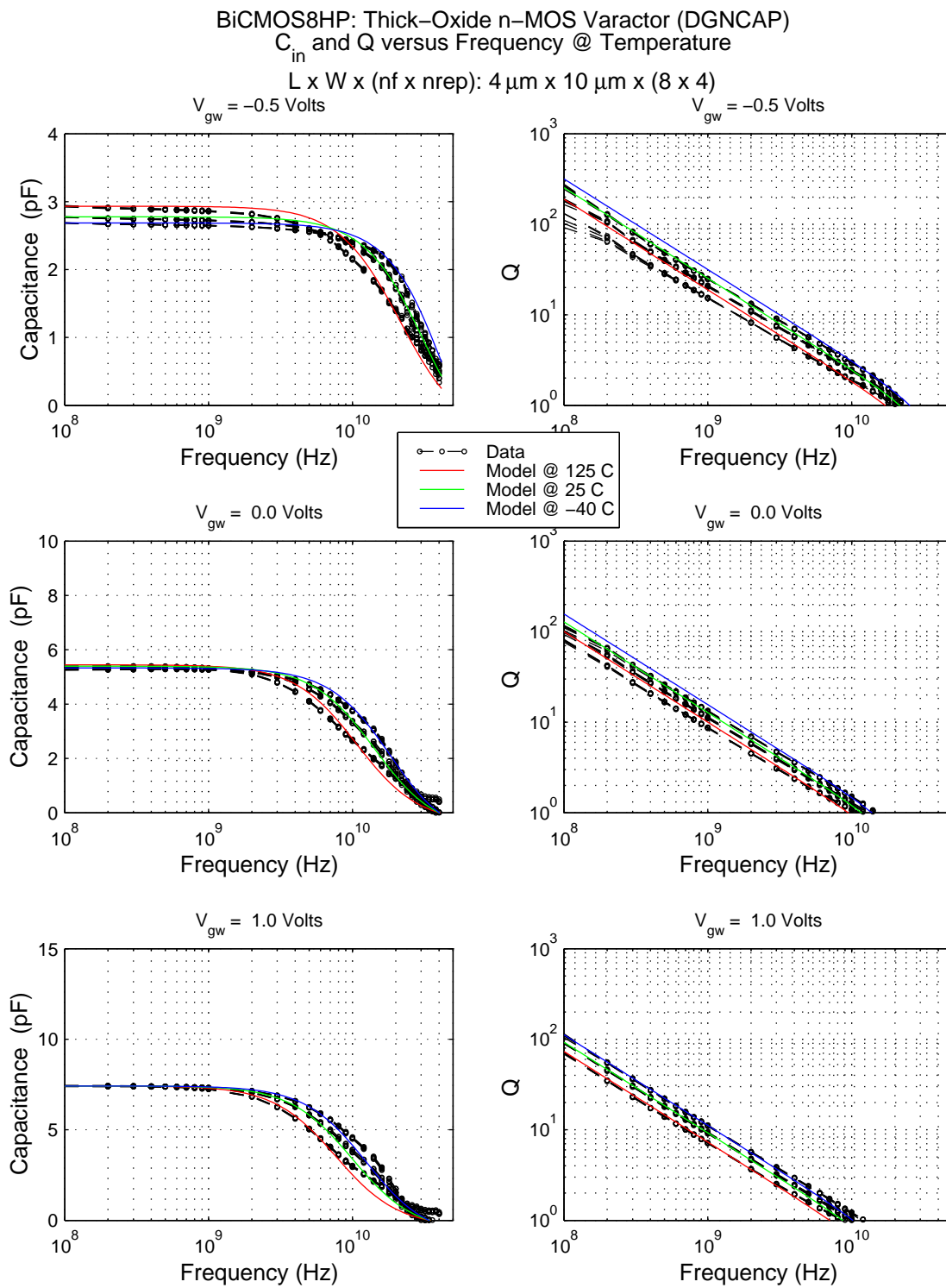


Figure 235. Thick Oxide nMOS Varactor S-Parameters C_{in} and Q versus Frequency, $L=4.0 \mu m$

8.0 Differential nMOS Varactor Model

8.1 Model Features

The differential nMOS varactor model (diffncap) includes:

- Input parameter specification for width, length, and nf (total # of interdigitated gate fingers, must be even).
- User-defined substrate resistance (rsx) based on layout (default=50 ohms).
- Device temperature difference with respect to circuit temperature (dtemp).

8.2 Model Limitations and Restrictions

Known limitations of the differential nMOS varactor model:

- The model only supports rectangular gate areas (PC - RX intersect area). Bent gates or other irregular layouts are not supported.
- The model does not take into account any parasitic inductance introduced by the metal lines connecting to the gates or by those connecting to the source/drains. This must be supplied by the user.
- The model fit has been optimized in the bias range between $V_{g-sd} = -0.5V$ and $V_{g-sd} = +1.0V$. In the deep depletion region, the model is not accurate due to unstable capacitance caused by thermal hole generation.
- The model uses VerilogA components to determine the primary capacitance (not fringe or coupling capacitance terms) in this device.
- Mis-match is not included in the current model.

8.3 Model Correlation Plots

The correlation plots for the differential nMOS varactor on the following pages show several aspects of the diffmosvar model. **Fig 236**, **Fig 237**, and **Fig 238** show the S-Parameter correlation plots for several device sizes under standard operations examining the impedance between the two sets of gates. The data in these three figures have one set of gates biased at some potential and the other set of gates biased at 0 V. The voltages applied are -0.5V, 0V, and 1.0V, respectively. The data show an increased Q factor in comparison to the standard nMOS varactor device. This can be attributed to the signal travelling into the device from one set of gates and exiting out from the other, which removes the Nwell contact resistance from the signal path and enables a closer gate spacing by removing the Nwell contacts between the gates.

Note the following calculation is used for the S-Parameter correlation plots in the figures mentioned above:

- $Z = Z_{11} + Z_{22} - Z_{21} - Z_{12}$
- $C_{in} = -1 / (\omega * \text{imag}(Z))$
- $Q = -\text{imag}(Z)/\text{real}(Z)$

The last figure, **Fig 239**, shows the single-ended operation of the differential nMOS varactor. Similar to the other plots, these plots only have the one set of gates biased, while the other is held at zero. However, the impedance between the biased set of gates and the Nwell (nw) is considered. The plots show a very low Q factor. This can also be attributed to the placement of the Nwell contacts around the outer rim of the device as opposed to in between the gates. The use of the differential nMOS varactor in this manner is not recommended. The standard nMOS varactor should be used instead.

Note the following calculation is used for the S-Parameter correlation plots in the previously mentioned figure:

- $C_{in} = -1 / (\omega * \text{imag}(Z_{11}))$
- $Q = -\text{imag}(Z_{11})/\text{real}(Z_{11})$

In the C_{in} versus frequency plots, there can be seen a slight increase in C_{in} . This is due to the inductance in the wiring both internal and external to the differential varactor. This inductance is not accounted for in any of the simulations.

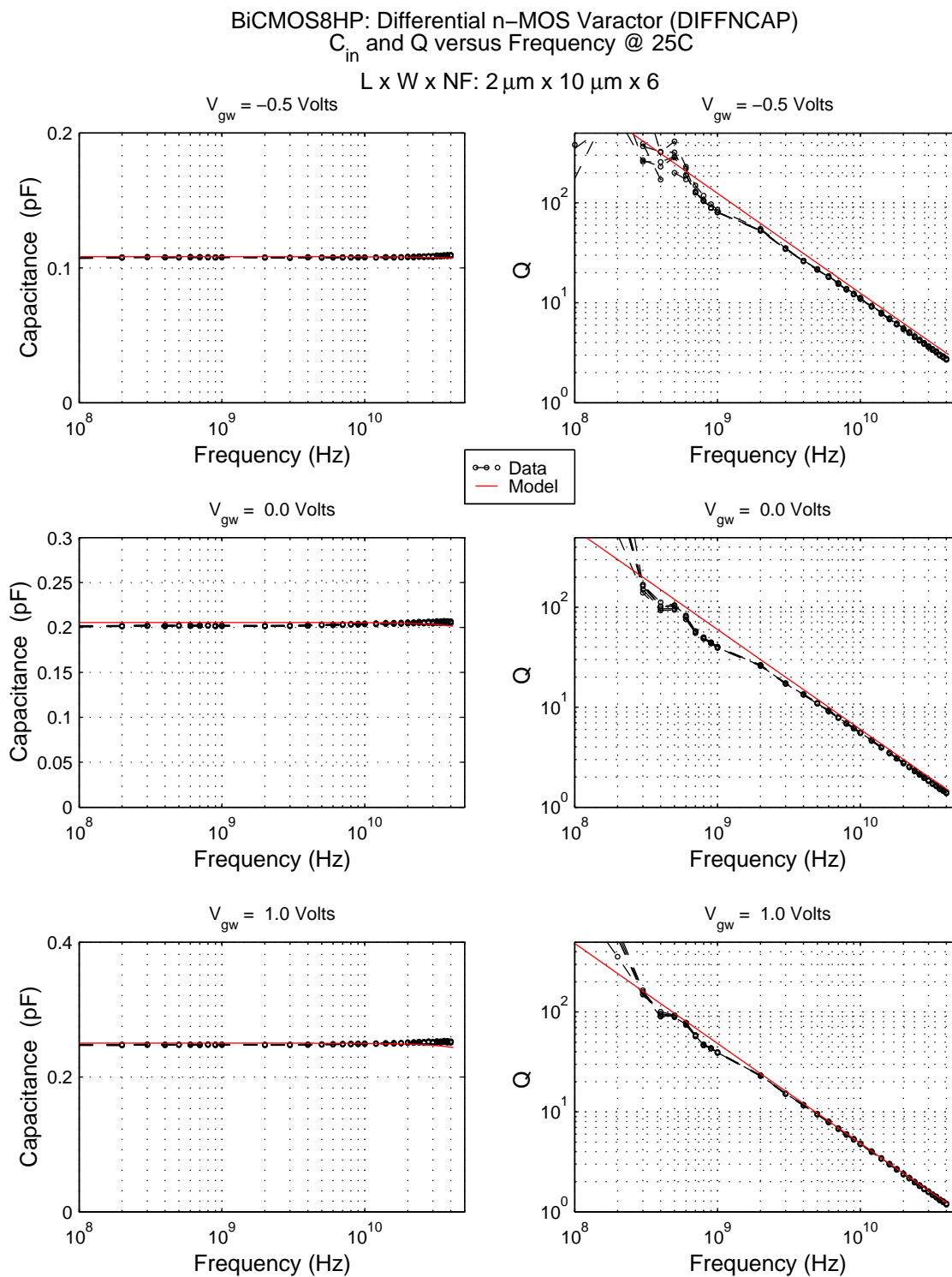


Figure 236. Differential nMOS Varactor S-Parameters C_{in} , Q vs Freq ($L \times W \times NF: 2\ \mu m \times 10\ \mu m \times 6$).

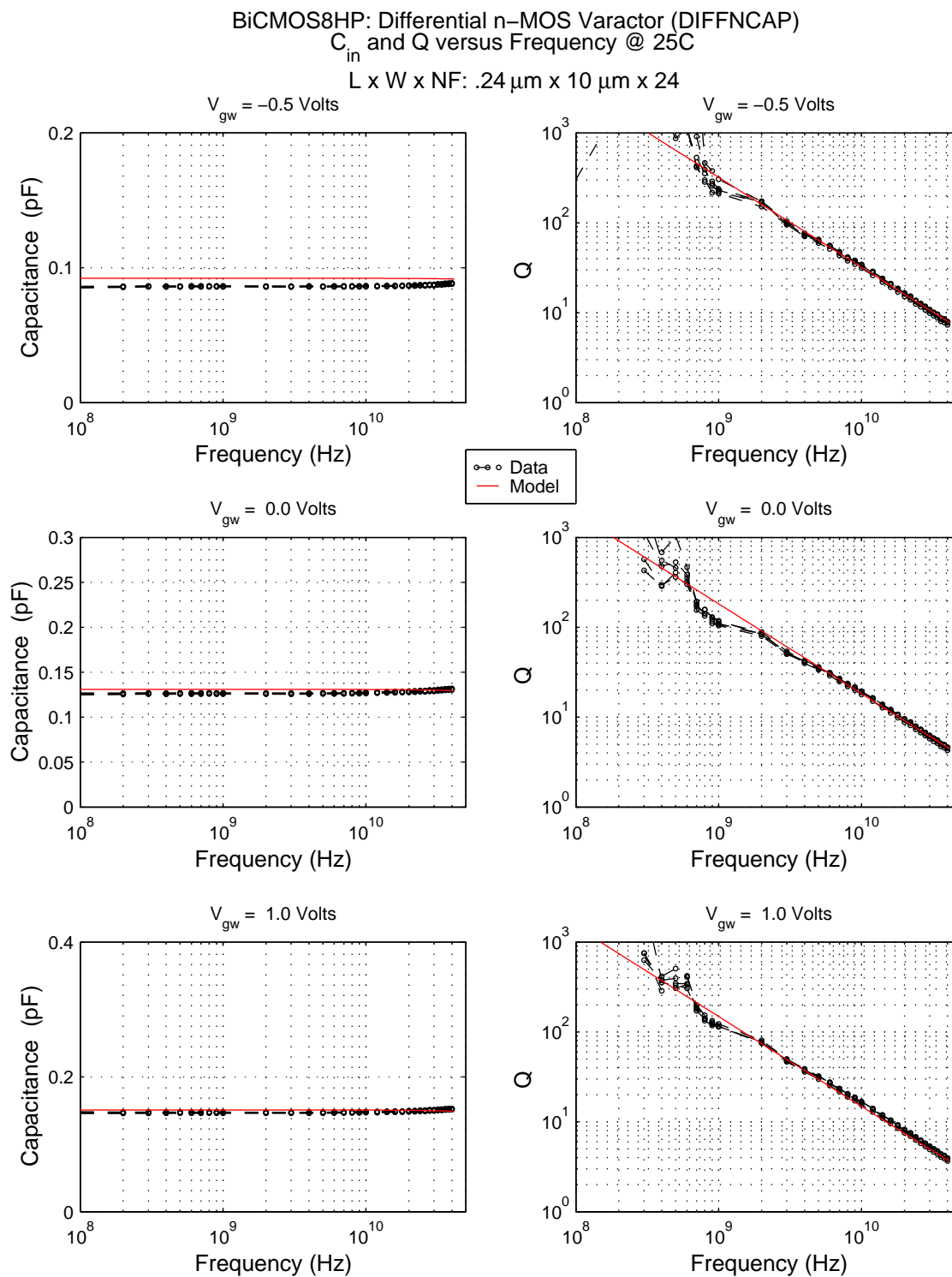
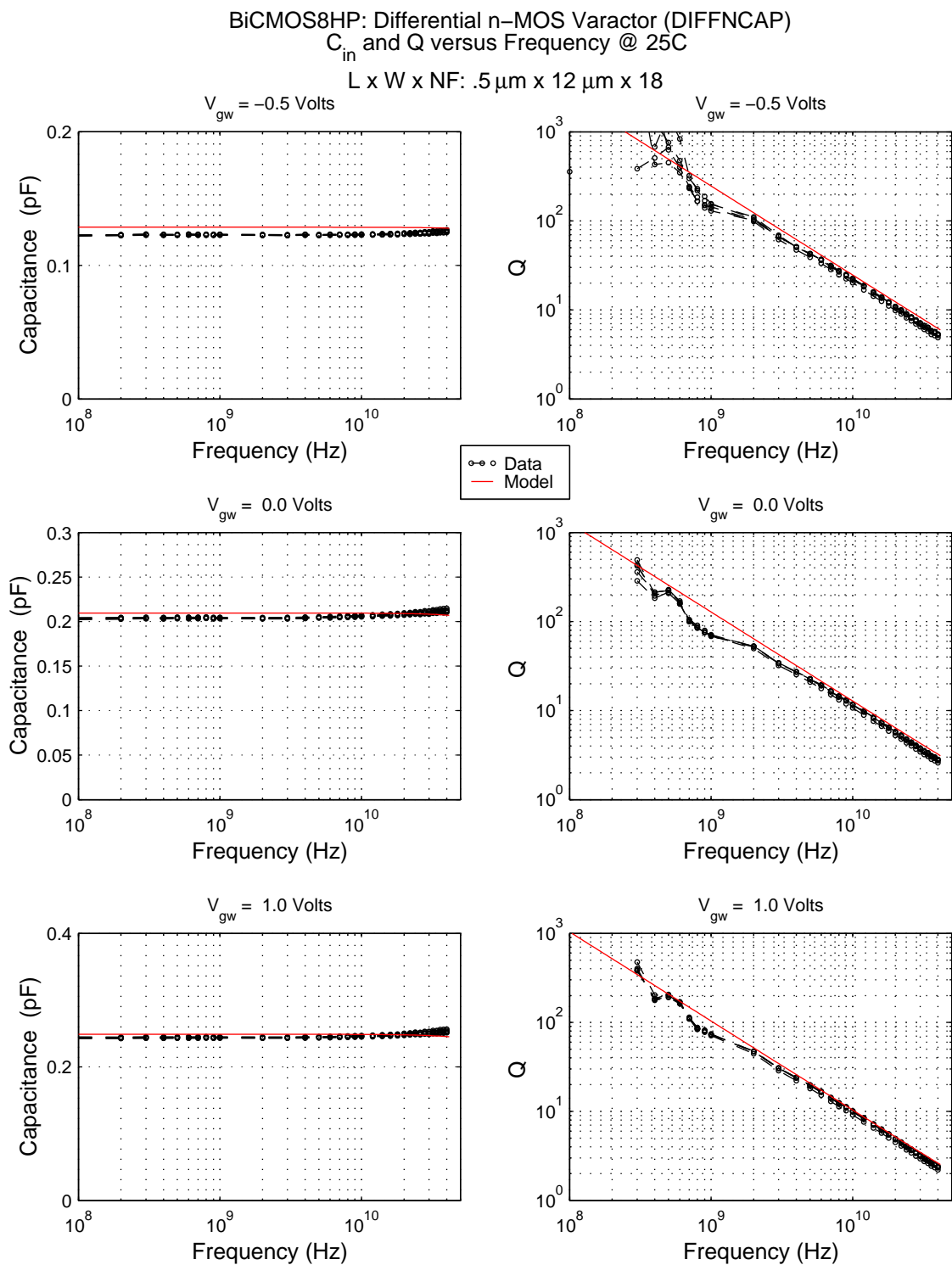


Figure 237. Differential nMOS Varactor S-Parameters C_{in} , Q vs Freq ($L \times W \times NF$: $0.24 \mu\text{m} \times 10 \mu\text{m} \times 24$).



Wafer Parametrics: co_mv= 11.75m qs_mv=460u

Figure 238. Differential nMOS Varactor S-Parameters C_{in} , Q vs Freq ($L \times W \times NF: 0.5 \mu m \times 12 \mu m \times 18$).

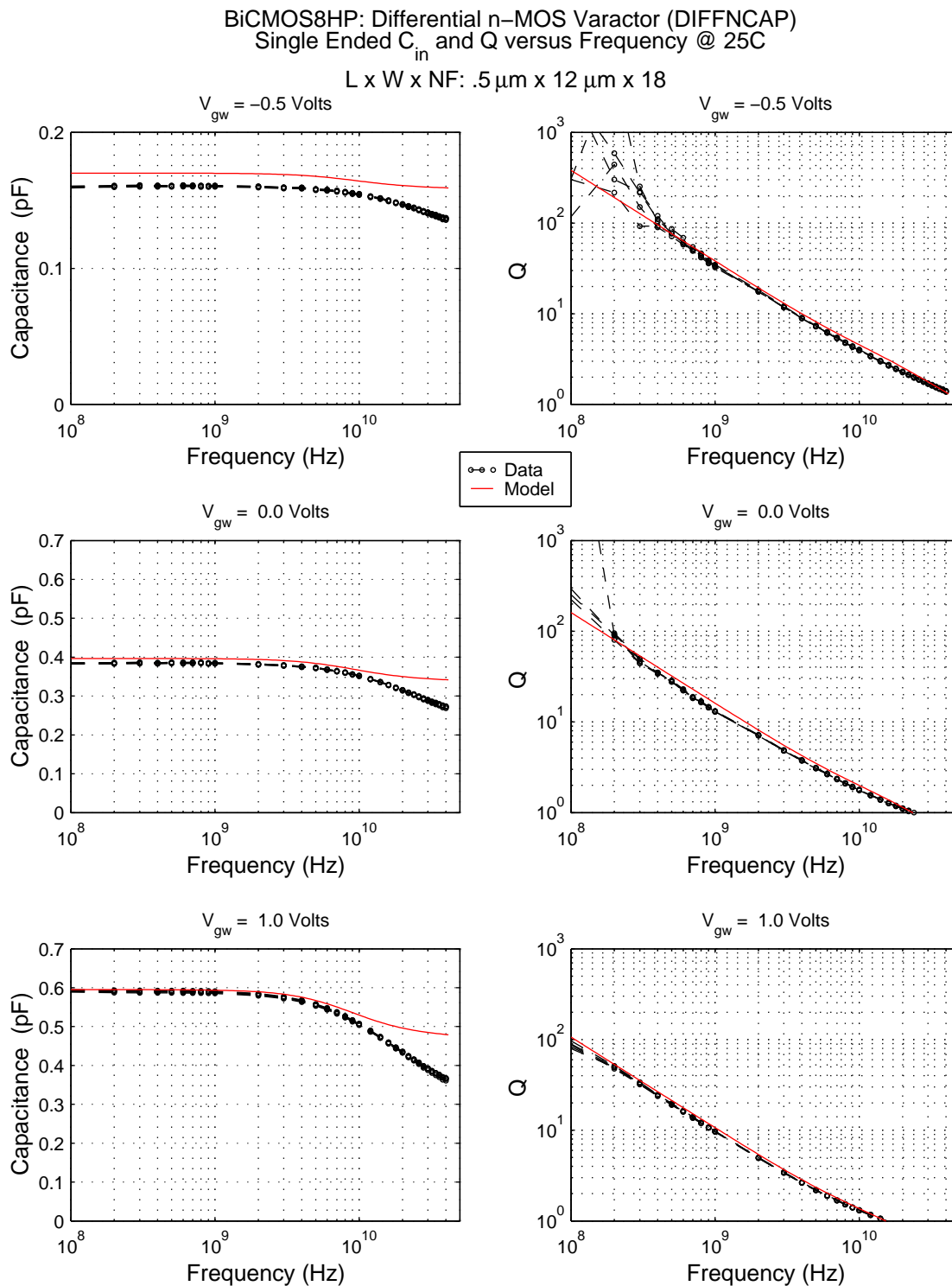


Figure 239. Differential nMOS Varactor S-Parameters, single-ended operation ($L \times W \times NF$: $0.5 \mu m \times 12 \mu m \times 18$).

9.0 Hyperabrupt (HA) Junction Varactor Model

9.1 Model Features

The HA varactor diode models include:

- Input parameter specification: anode width and length and number of anodes or anode width and capacitance at $V=0$ and number of anodes.
- Scaled cathode resistance based on device geometry and distributed effects.
- The model accounts for series resistance introduced by the M1 wiring provided by the design kit PCell. Metal wiring inductance is also calculated by the model (setind=-2), but this value can be overridden by using setind parameter.
- User-defined substrate resistance (rsx) based on layout (default=50 ohms).
- Device temperature difference with respect to circuit temperature (dtemp).

9.2 Model Limitations and Restrictions

Known limitations for the HA varactor models:

- Breakdown effects of the diode are not included in the model.
- The model does not account for charge storage effects.
- The device performance when forward biased is determined by non-linear charge storage effects which are not modelled. The S-Parameter characteristics documented in this section represent the primary application of the varactor for voltage-controlled capacitance.

9.3 Model Correlation Plots

The correlation plots for the HA varactor on the following pages are a comparison of model simulations and the technology qualification hardware as follows:

Table 74. HA Varactor Correlation Plots

Device Size (W x L x NF)	Capacitance vs Voltage (vs Temp)	Forward & Reverse Current	S-Parameters: C _{in} & Q Factor
2.0 x 10 x 20	Fig 240		
4.0 x 20 x 4	Fig 240		
4.0 x 20 x 10	Fig 241	Fig 242	
0.8 x 10 x 10		Fig 242	Fig 243
2.0 x 20 x 1			Fig 244
1.0 x 10 x 5			Fig 245
20 x 20 x 2	Fig 241		Fig 246

C-V Characteristics:

These plots show capacitance versus voltage curves for several device geometries across three temperatures (-40, 25, and 125 C).

Forward I-V and Leakage Characteristics:

- The upper plot shows a comparison of the forward currents versus voltage for a couple of device sizes.
- The lower plot shows a comparison of the reverse currents versus voltage for a couple of device sizes.

S-Parameter Characteristics:

This group of plots illustrates the capacitance (C_{in}) vs frequency and the quality factor (Q) vs frequency for 0V, -1V, and -3V reverse bias (cathode grounded) across a few device sizes. Note the following calculations for the S-Parameter correlation plots:

- $C_{in} = (\text{imag}(Y_{11}) / \omega)$
- $Q = \text{imag}(Y_{11}) / \text{real}(Y_{11})$

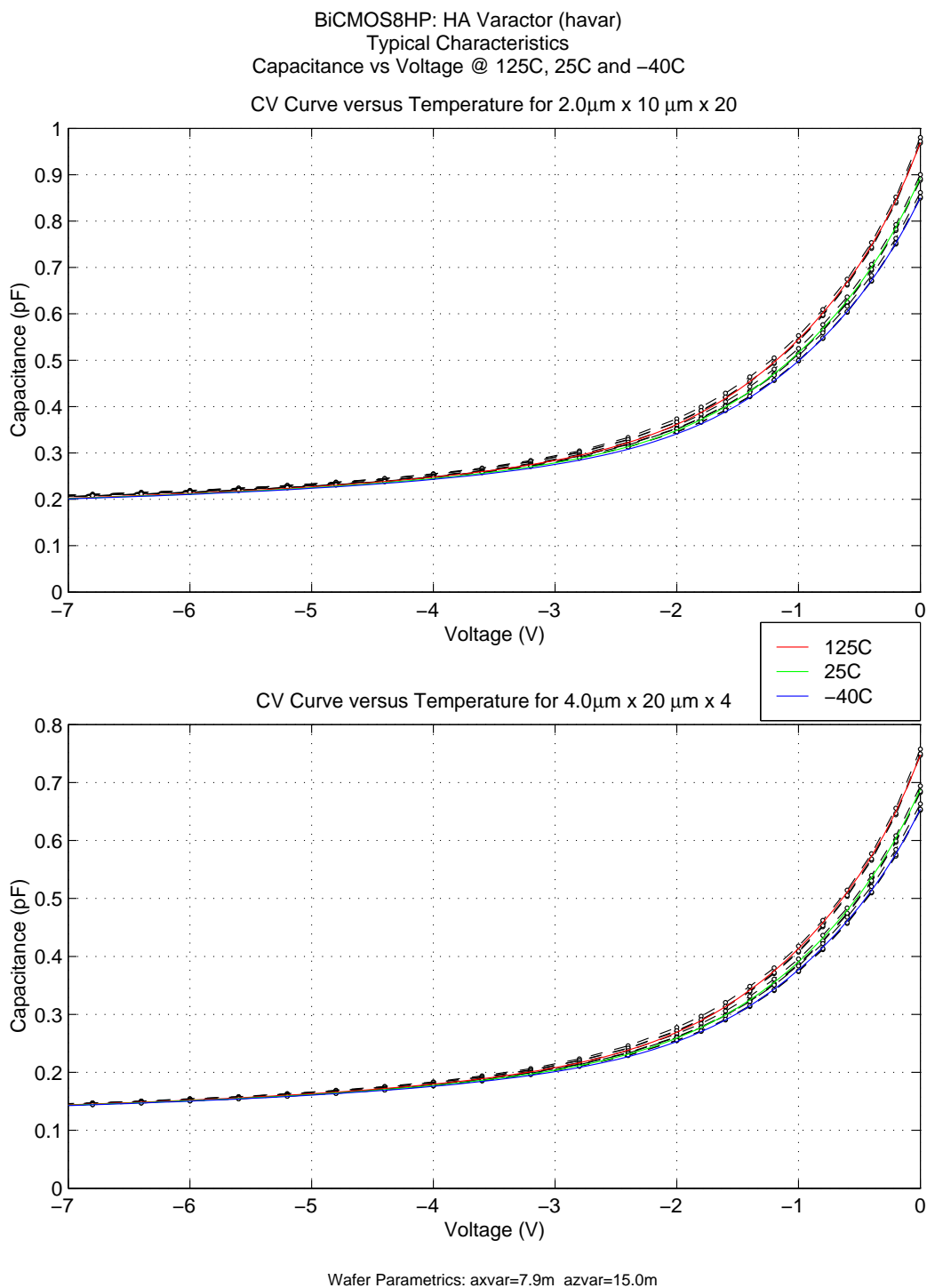


Figure 240. HA Varactor CV Characteristics at -40C, 25C, and 125C for a couple of device geometries.

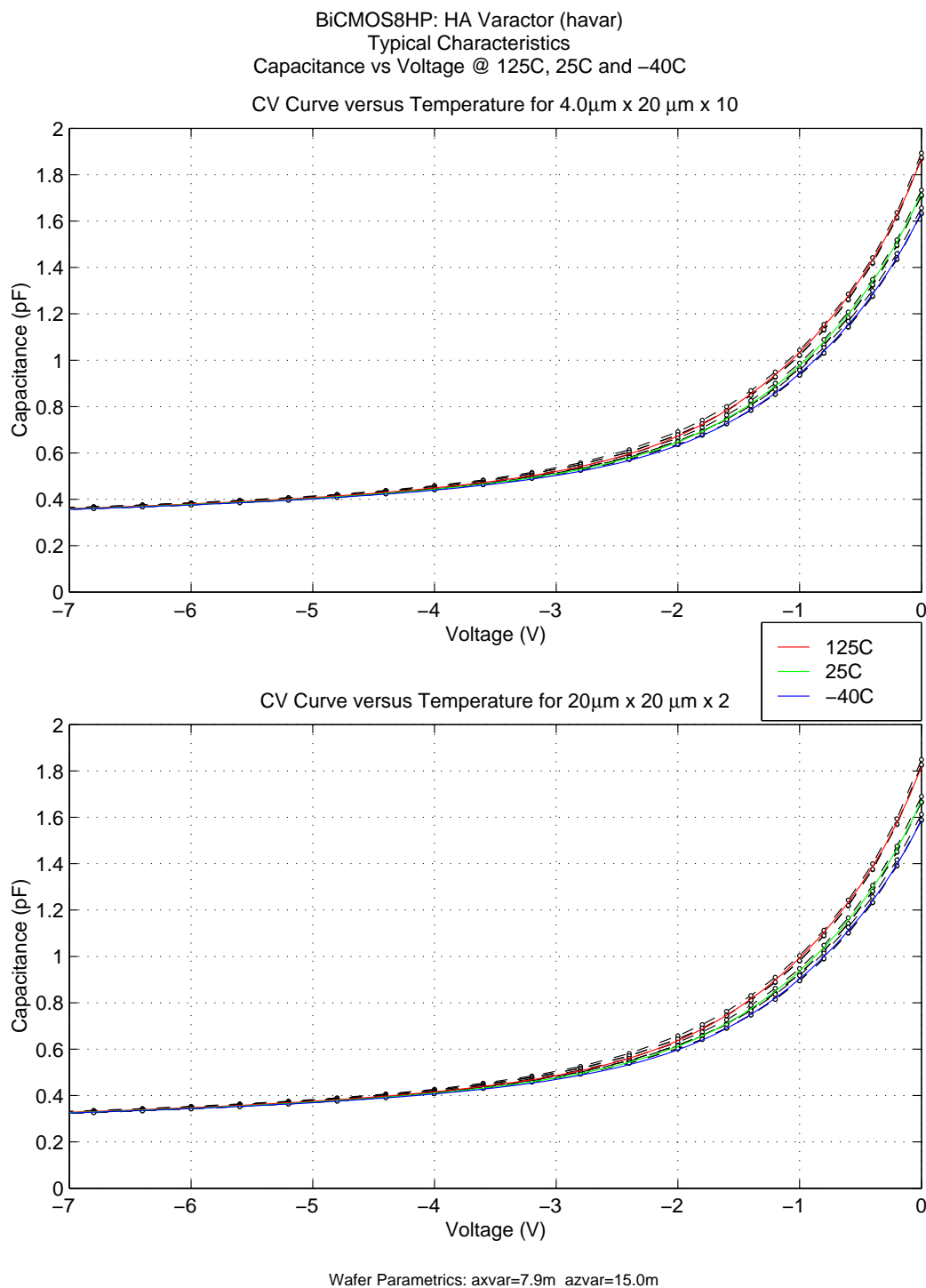


Figure 241. HA Varactor CV Characteristics at -40C, 25C, and 125C for a couple of device geometries.

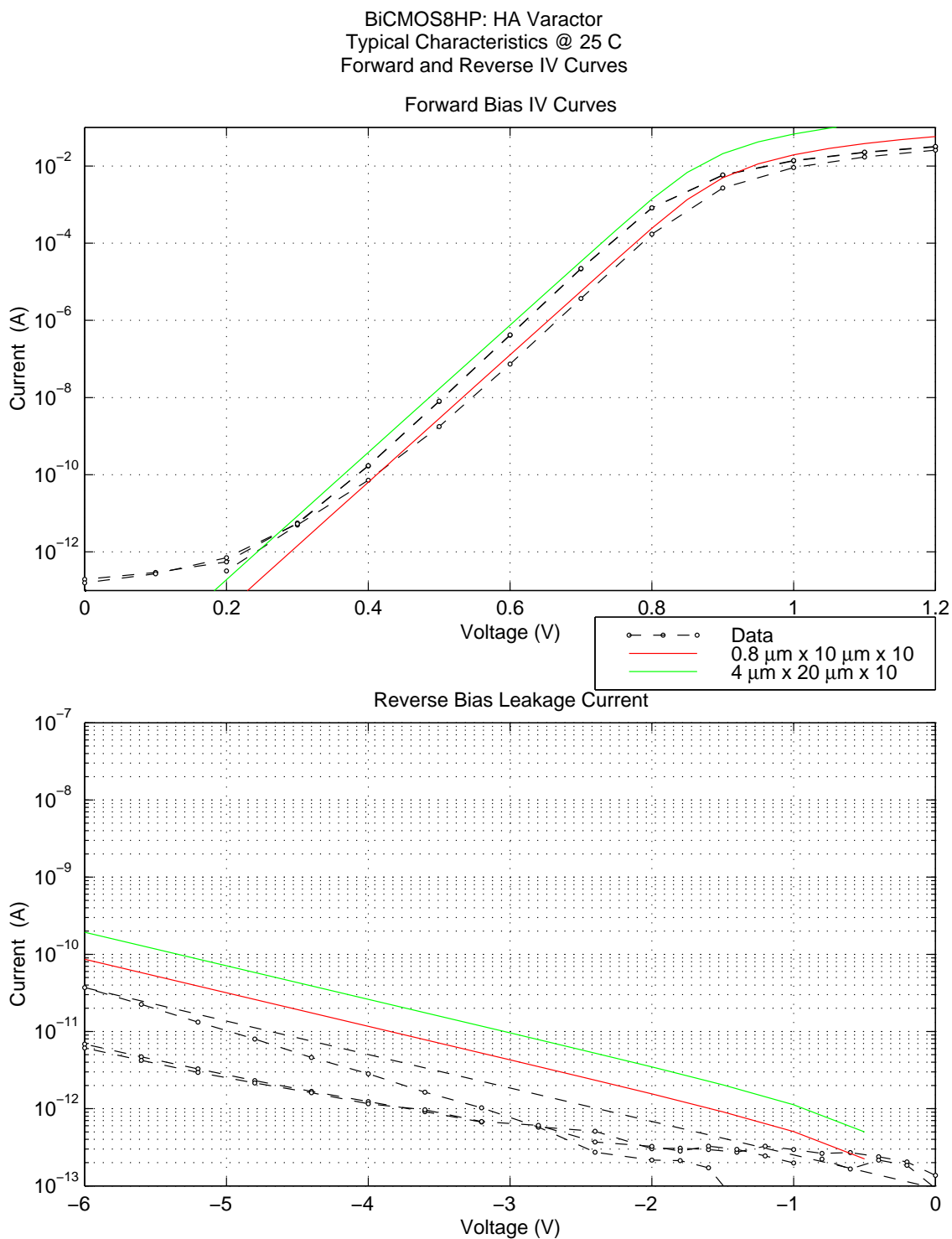


Figure 242. HA Varactor Forward-Bias and Reverse-Bias IV Curves at 25C for a couple of device geometries.

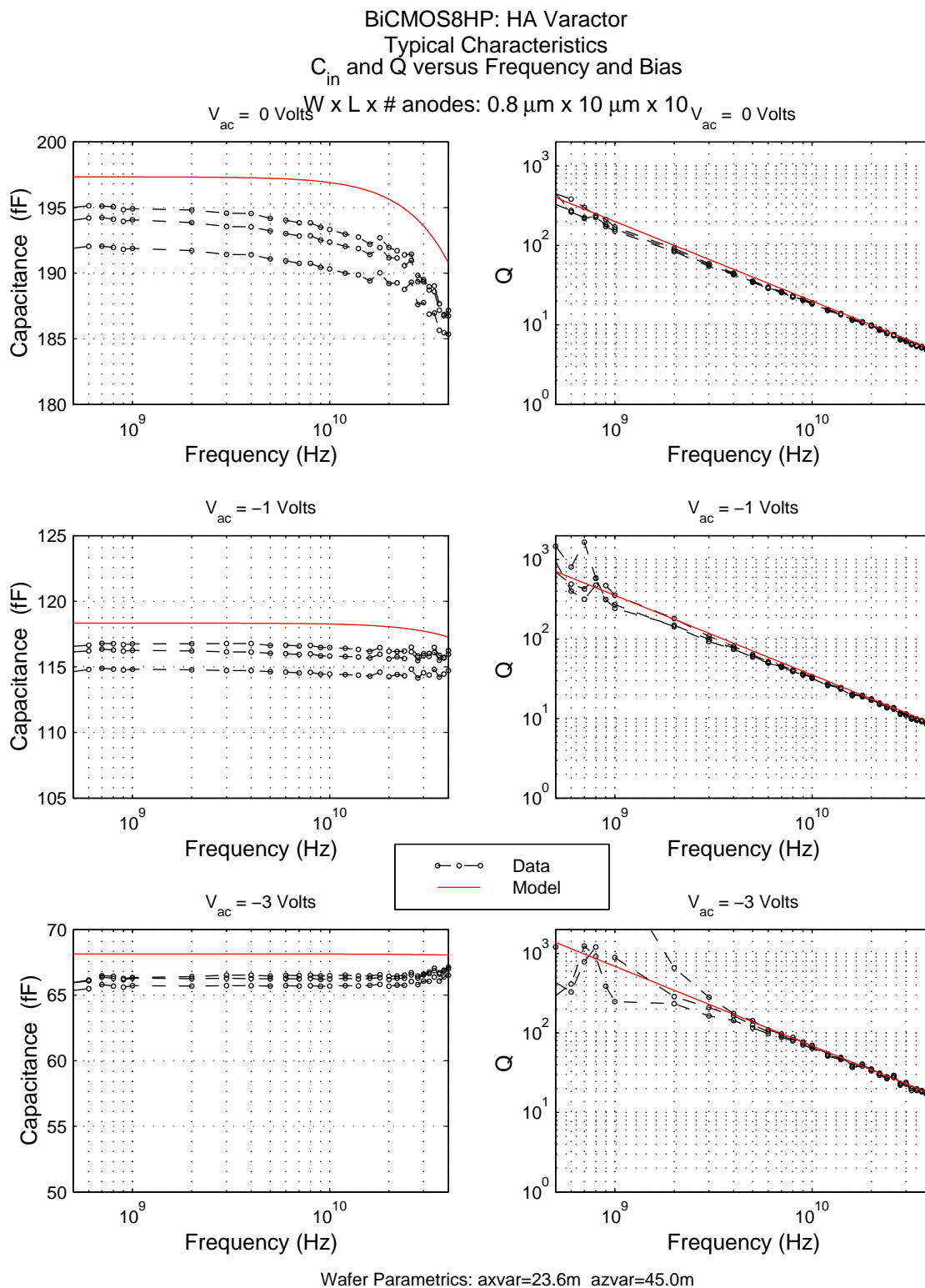


Figure 243. HA Varactor S-Parameters: C_{in} and Quality Factor versus Frequency at 25C for $0.8 \times 10 \times 10$.

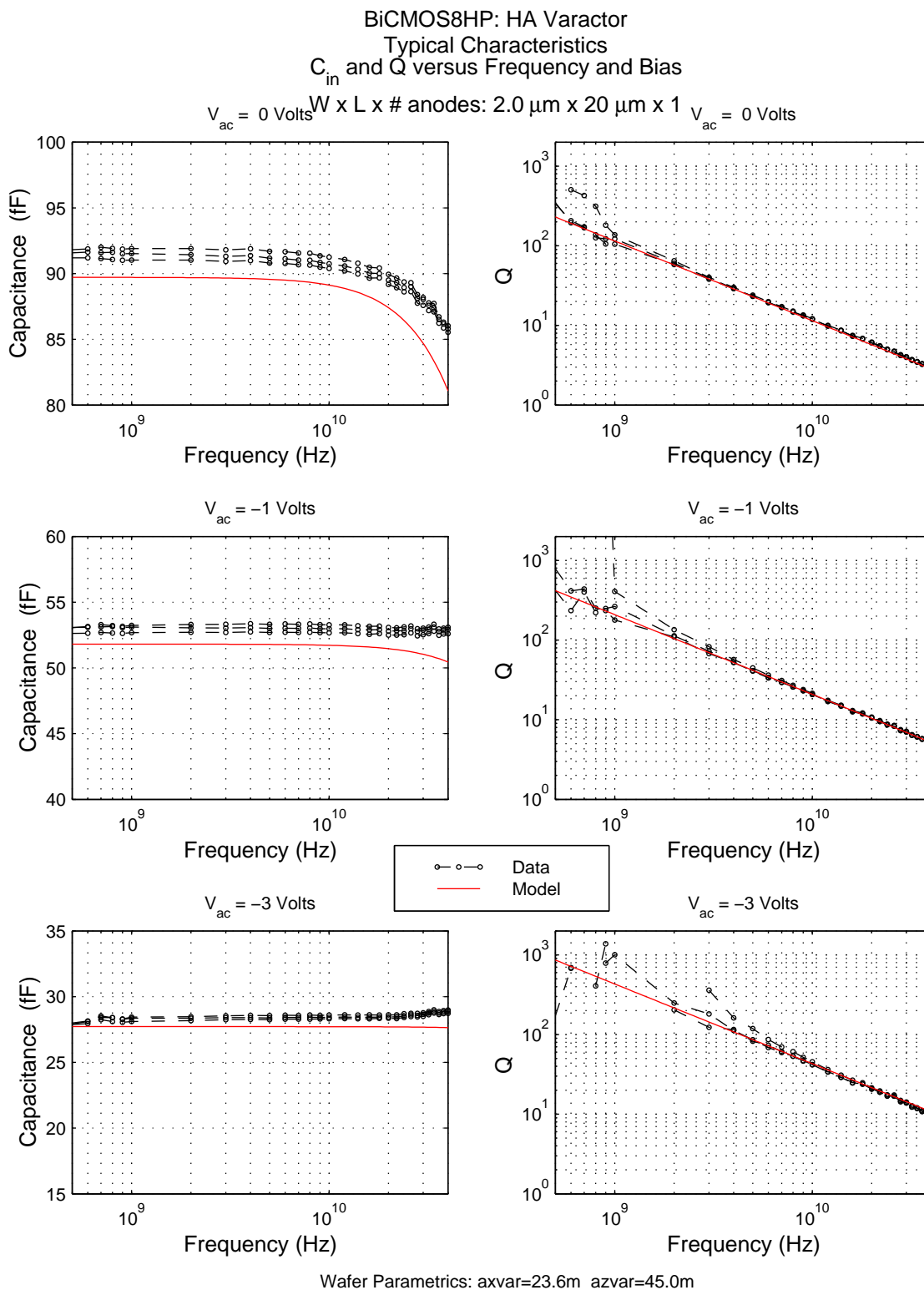


Figure 244. HA Varactor S-Parameters: C_{in} and Quality Factor versus Frequency at 25C for 2.0x20x1.

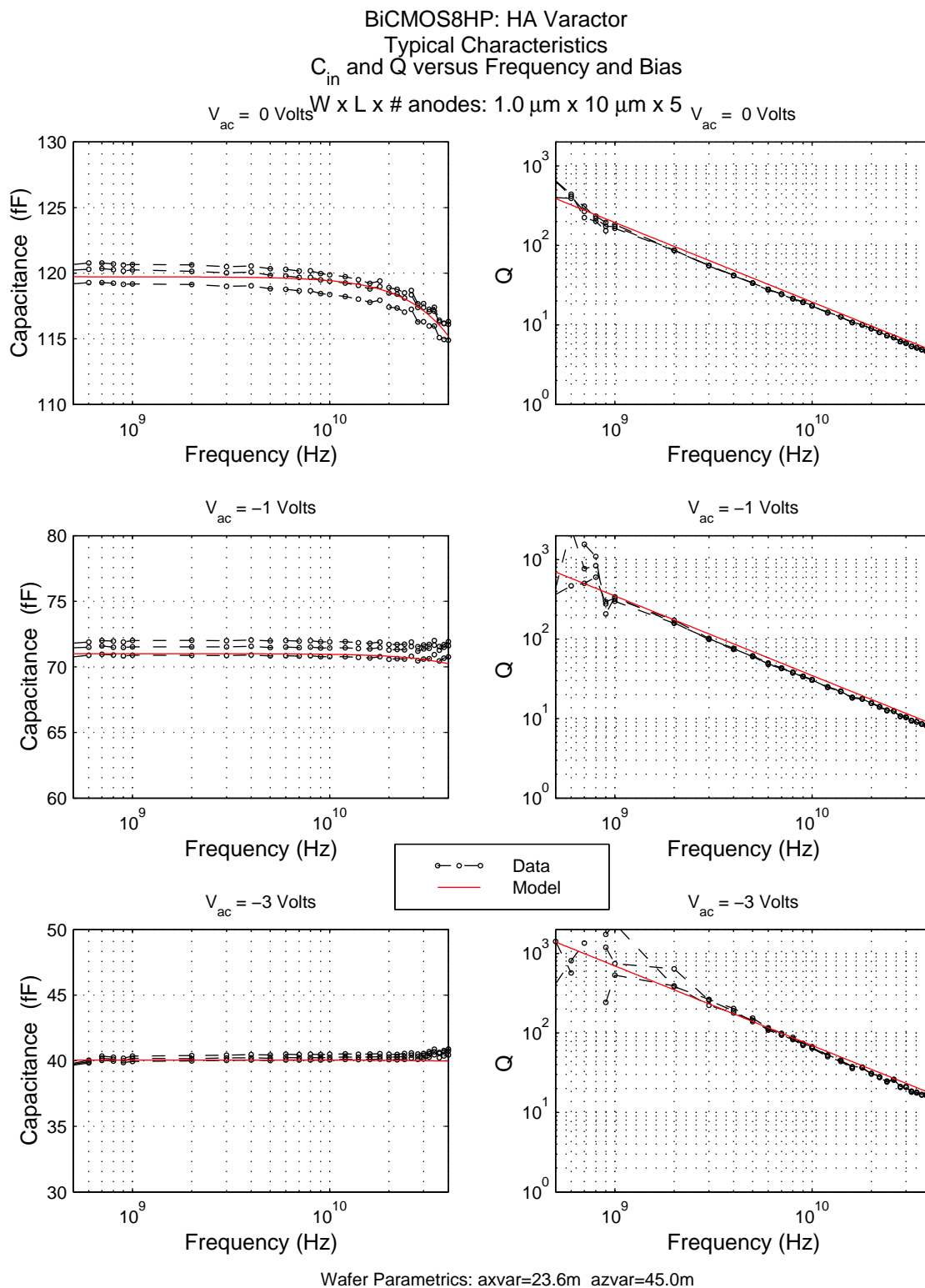


Figure 245. HA Varactor S-Parameters: C_{in} and Quality Factor versus Frequency at 25C for $1.0 \times 10 \times 5$.

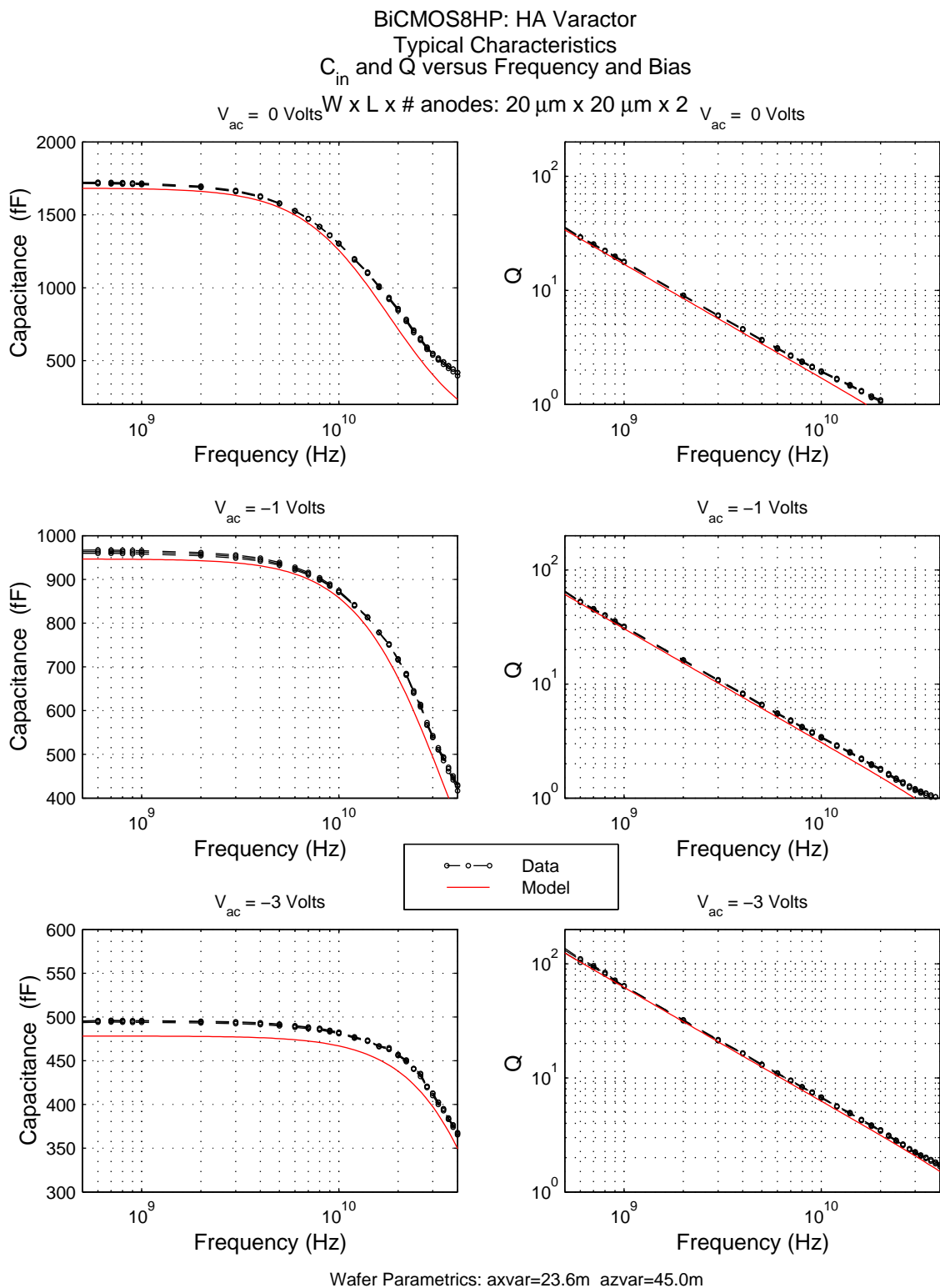


Figure 246. HA Varactor S-Parameters: C_{in} and Quality Factor versus Frequency at 25C for 20x20x2

10.0 Forward-Bias (DI) Diode Model

10.1 Model Features

The forward-bias diode model (divpnp) focuses on the forward bias I-V curves including temperature effects. This is a three node model, and employs the standard Gummel-Poon BJT transistor. The nodes are the emitter (anode), the base (NW), and the collector (SX). Features of this model include:

- Input parameter specification for width, length, and number of fingers.
- Device temperature difference with respect to circuit temperature (dtemp).
- Series resistance based on device geometry is included to describe I-V curve roll-off.
- Device mis-match for adjacent devices.

10.2 Model Limitations and Restrictions

Known limitations of the divpnp models:

- Calculations for the series resistance are based on the device geometries used in the p-cell. While other geometries are allowed, the model will not properly account for the series resistance in layouts not based on the p-cell.
- No temperature dependence is included for the capacitances.
- No transit time effects are included in the model, and no S-parameter characterisation has been done.

10.3 Mis-Match Reference Table

The following table provides a comparison of adjacent mis-match for a select set of divnp geometries. The table also show hardware data results used to set the mis-match scaling in the models.

The data results are based on a fairly small sample of 20 sites from each of 2 wafers from each of 3 standard technology hardware lots (6 wafers total). Data analysis programs calculate the mis-match based on the entire set of measured data. These results are in the 'Data Mis-Match' column. The corresponding mis-match calculated from the model is shown in the 'Model Mis-Match' column. Lastly, the low/high limits of the mis-match, based on a chi-squared analysis of the data, is given in the 'Data Limits Mis-Match' column.

Note that the general trend of the models is to predict a slightly higher mis-match than the data results. The models have been purposely set to be conservative in this manner.

Table 75. DI Diode Mis-Match

Diode Dimensions (μm) (width x length x #fingers)	Model Mis-match (%)	Data Mis-Match (%)	Data Limits Mis-Match (%)
1.0 x 10 x 1	1.75	1.60	1.34 / 2.00
1.0 x 20 x 1	1.36	1.17	0.98 / 1.47
1.0 x 40 x 1	1.11	0.88	0.73 / 1.11
1.4 x 10 x 1	1.43	1.30	1.09 / 1.63
1.4 x 20 x 1	1.09	0.91	0.75 / 1.14
2.0 x 10 x 1	1.17	1.26	1.05 / 1.57
2.0 x 20 x 1	0.87	0.78	0.65 / 0.97
1.0 x 10 x 2	1.23	1.12	0.93 / 1.39
1.0 x 10 x 4	0.87	0.92	0.77 / 1.15
1.4 x 10 x 2	1.01	1.02	0.85 / 1.28
1.4 x 10 x 4	0.72	0.79	0.66 / 0.99
1.4 x 20 x 2	0.77	0.75	0.63 / 0.95
2.0 x 10 x 2	0.83	0.78	0.65 / 0.98
2.0 x 10 x 4	0.59	0.64	0.53 / 0.80

10.4 Model Correlation Plots

10.4.1 I-V Correlation

The following plots compare the I-V characteristics of the divnpn models with a set of device measurements at various temperatures (-40C, 25C, and 125C). For these measurements, a current was forced into the anode (emitter) of the device while the cathode (base) and the substrate ring (collector) were both grounded. The voltage across the emitter-base junction was then measured.

Table 76. Forward Bias Diode Correlation Plots

Anode(Emitter) Size W x L x #fingers	divnpn
1.0 μ m x 10 μ m x 1	Fig 247
2.0 μ m x 20 μ m x 1	Fig 248
1.0 μ m x 10 μ m x 10	Fig 249
1.4 μ m x 20 μ m x 4	Fig 250

The upper plots in these figures show the standard forward-bias IV curves as a function of temperature. The lower curves show the ideality as a function of current density. The values used in to plot these curves were extracted from the values that are plotted in the upper curves.

This "forward-biased diode" shows a bipolar effect in which a portion (slightly more than half) of the current flowing in the anode (emitter) flows completely through the cathode (base) region and into the substrate (collector). **Fig 251** is a plot that shows the anode current and cathode current for a couple of devices. This figure shows that the geometry dependent expression for beta in our bipolar model does indeed correlate with our data.

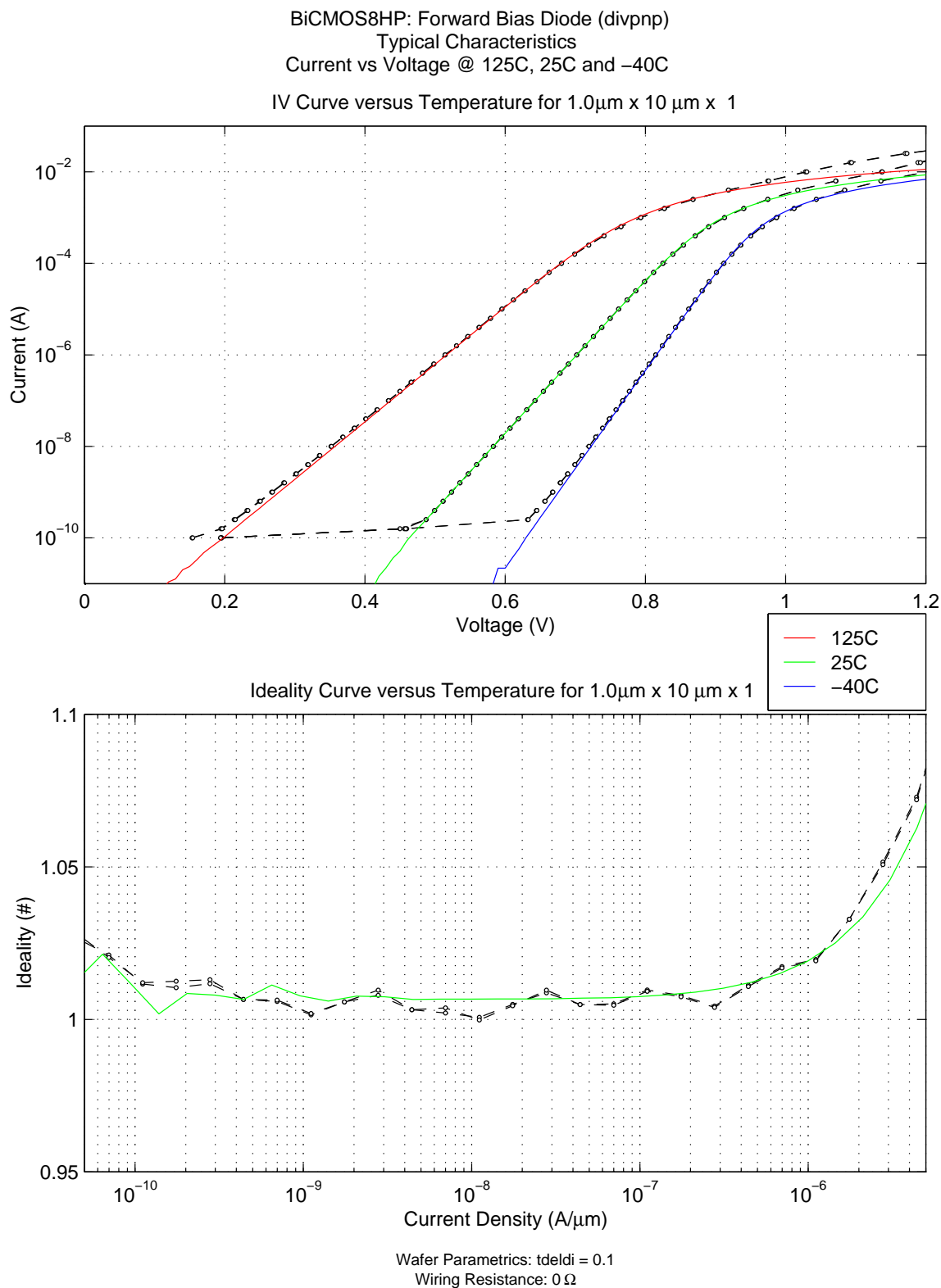


Figure 247. divnpn I-V Characteristics at -40C, 25C, and 125C for 1x10x1 device.

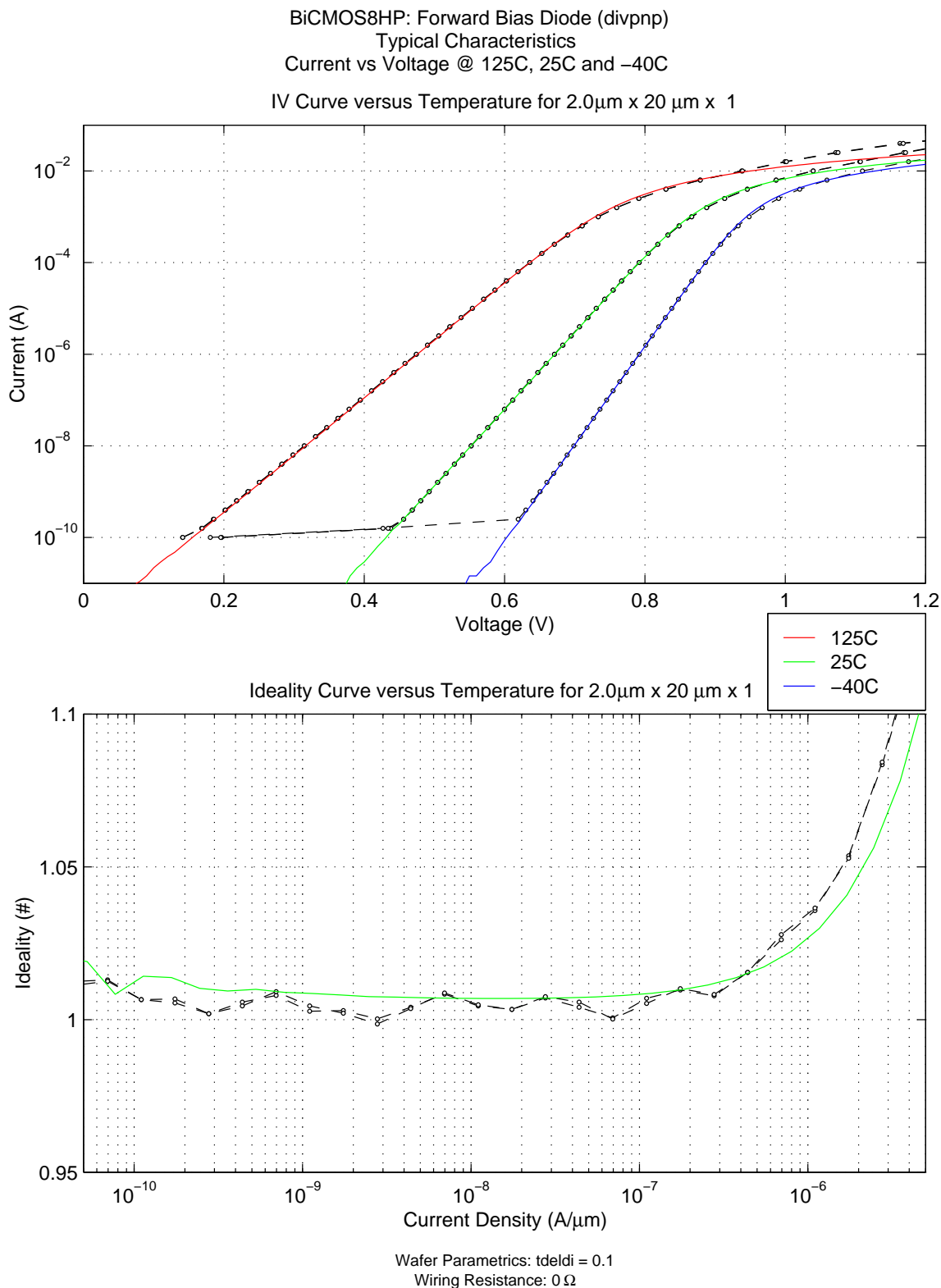


Figure 248. divnpn I-V Characteristics at -40C, 25C, and 125C for 2x20x1 device.

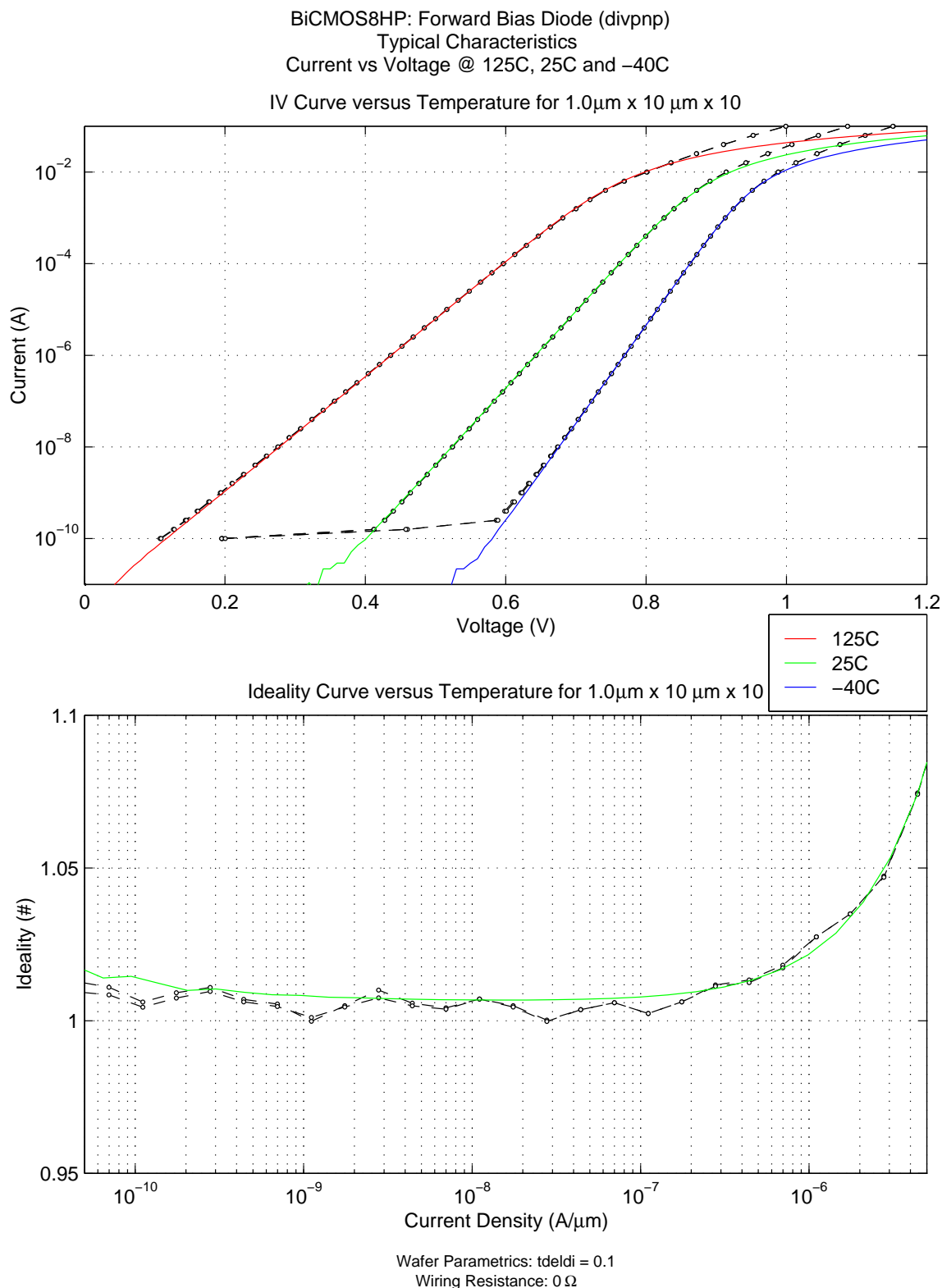


Figure 249. divnpn I-V Characteristics at -40C, 25C, and 125C for 1x10x10 device.

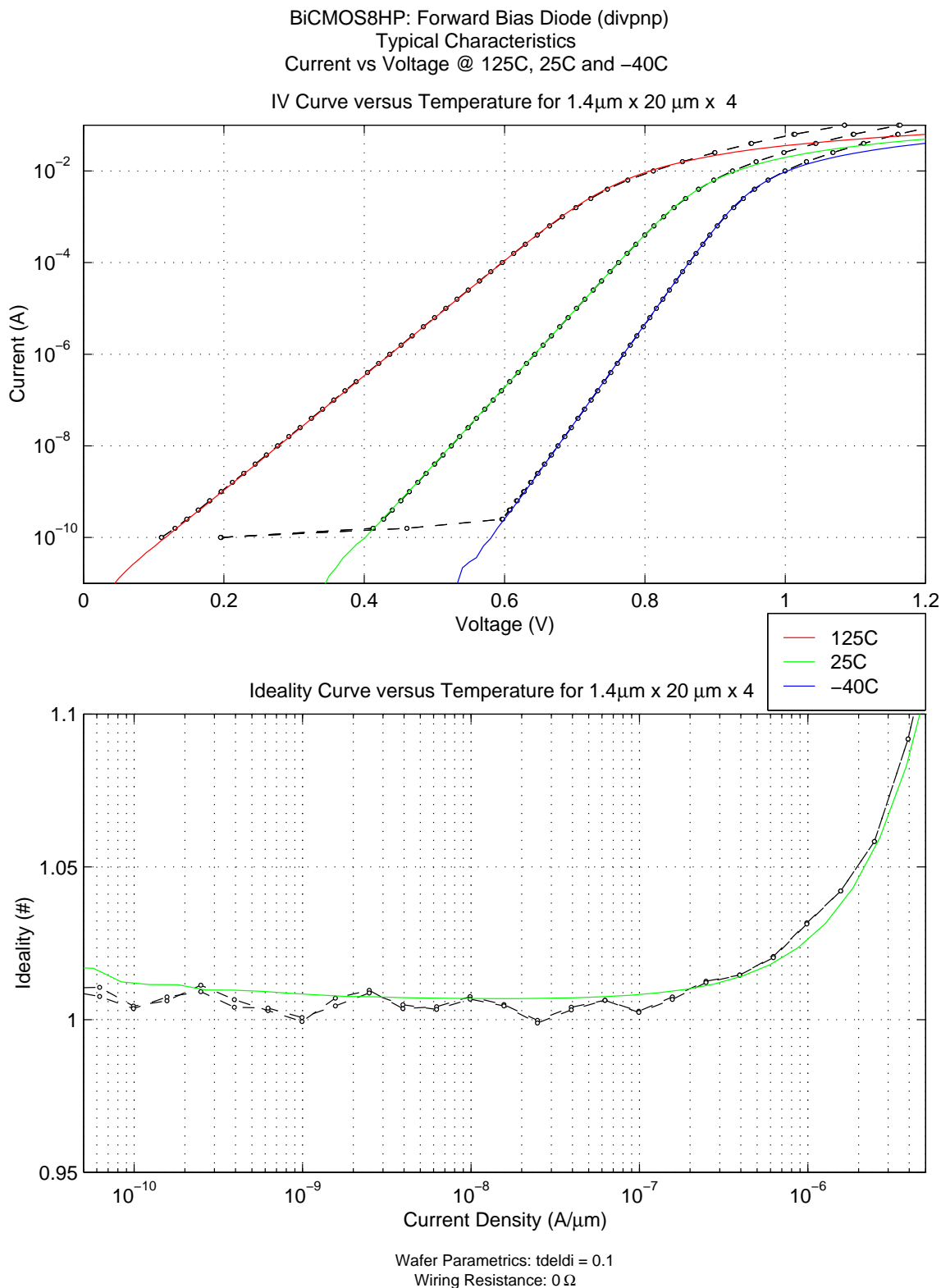


Figure 250. divnpn I-V Characteristics at -40C, 25C, and 125C for 1.4x20x4 device.

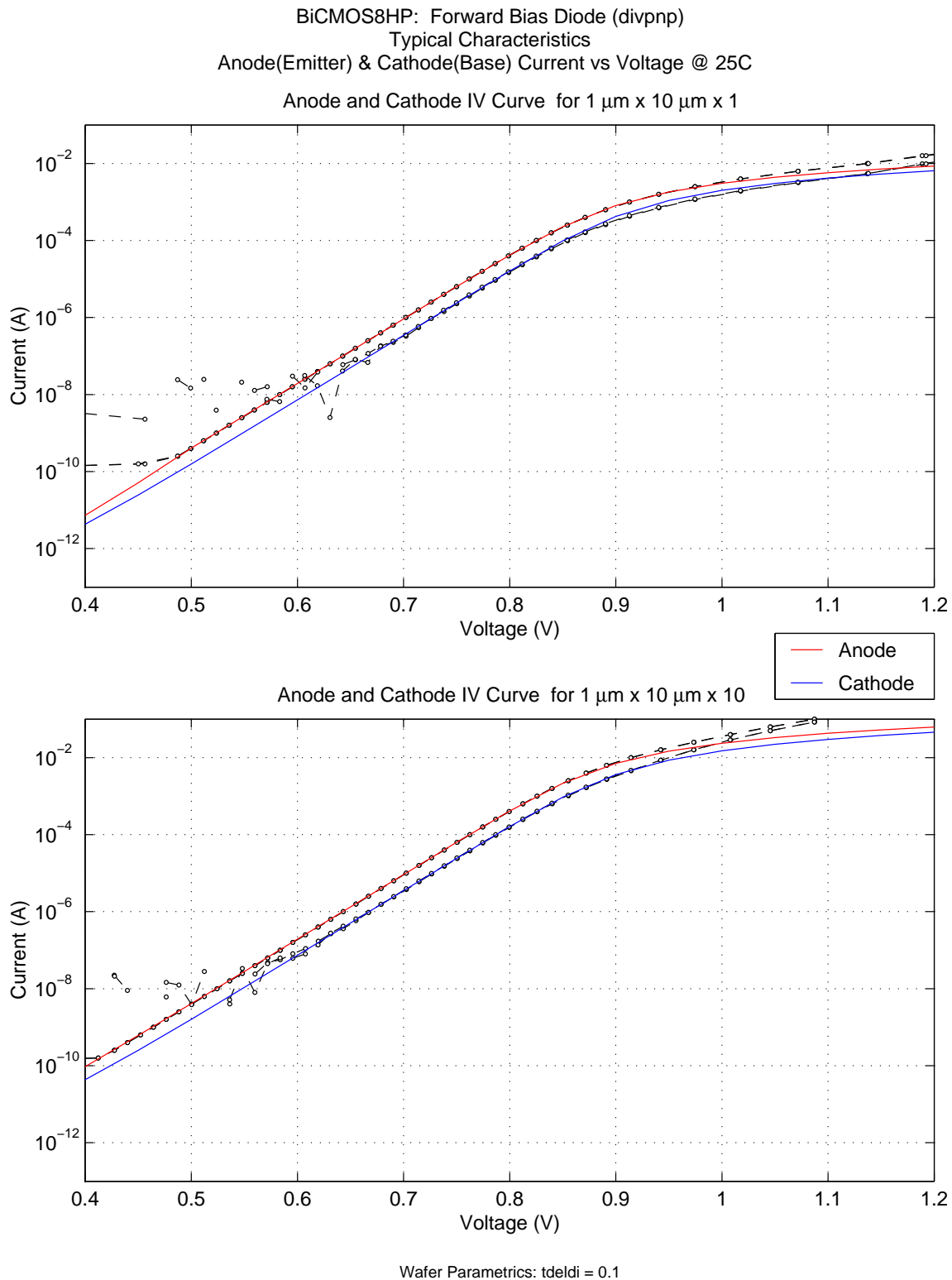


Figure 251. divnp Bipolar Beta Characteristics at 25C for a couple of device geometries.

11.0 Nitride MIM Capacitor Model

11.1 Model Features

The nitride MIM model include:

- Input parameter specification for length and width or length and capacitance.
- "nlev" parameter determines the number of metal levels present in the design. Possible values are 5-7.
- "setind" is the user determined value for the parasitic inductance. The default value of -2, which is used as a switch, forces the model calculated inductance to be used.
- "est" switch includes bottom plate parasitic capacitance (est=1, default) for the case of MIMs without any other devices placed underneath the capacitor. The capacitance is set to a negligible value of 0.01fF (est=0) to support the case of other devices being placed under the MIM where only the layout extraction tool can provide for an accurate calculation of this bottom plate parasitic capacitance.
- "rsx" determines the series resistance (rsx=50, default) from the substrate below the device to the reference node.
- Device temperature difference with respect to circuit temperature (dtemp).

11.2 Model Limitations and Restrictions

The default calculation for bottom plate parasitic capacitance (est=1) is only accurate for the case of MIMs without devices placed underneath the capacitor. For simulations using a netlist generated from the schematic only, the model will underestimate the bottom plate parasitic capacitance for the case where other devices are placed underneath a BEOL capacitor. The user has the option of using a netlist generated from layout extraction or including an additional capacitor element in the schematic to represent the increase in the parasitic capacitance. For either of these options, the model override (est=0) should be used to avoid double counting of the parasitic.

The model calculated inductance value does not include any wiring parasitics, it is only for the MIM device itself. The inductance calculation assumes the wiring is into the device on one side and out of the device on the opposing side. These two sides are assumed to be defined by the l parameter. For any other connection, the inductance of the device will be different from that calculated by the model.

11.3 MIM Mis-Match Reference Tables

The following table provides a comparison of adjacent mis-match for a select set of MIM sizes. The table also shows hardware data results used to set the mis-match scaling in the models.

The data results are based on a sample of 20 sites from each of 2 wafers from 3 standard technology hardware lots. Data analysis programs calculate the mis-match based on the entire set of measured data. These results are in the 'Data Mis-Match' column. The corresponding mis-match calculated from the model is shown in the 'Model Mis-Match' column. Lastly, the low wafer / high wafer 3-sigmas of the data mis-match is given in the 'Data Limits Mis-Match' column.

Note that the general trend of the models is to predict a slightly higher mis-match than the data results. The models have been set to be conservative in this manner due to the small sample size.

<i>Table 77. MIM Adjacent Mis-match</i>			
MIM Dimensions (μm) (width x length)	Model Mis-match (%)	Data Mis-Match (%)	Data Limits Mis-Match (%)
4 x 4	0.272	1.26	1.01 / 1.68
18 x 6	0.110	0.067	0.055 / 0.086
4 x 12	0.165	0.252	0.201 / 0.337
8 x 8	0.136	0.103	0.082 / 0.136
15 x 45	0.044	0.025	0.021 / 0.031
45 x 15	0.044	0.025	0.021 / 0.031
25 x 25	0.043	0.032	0.026 / 0.040
15 x 15	0.072	0.040	0.033 / 0.050

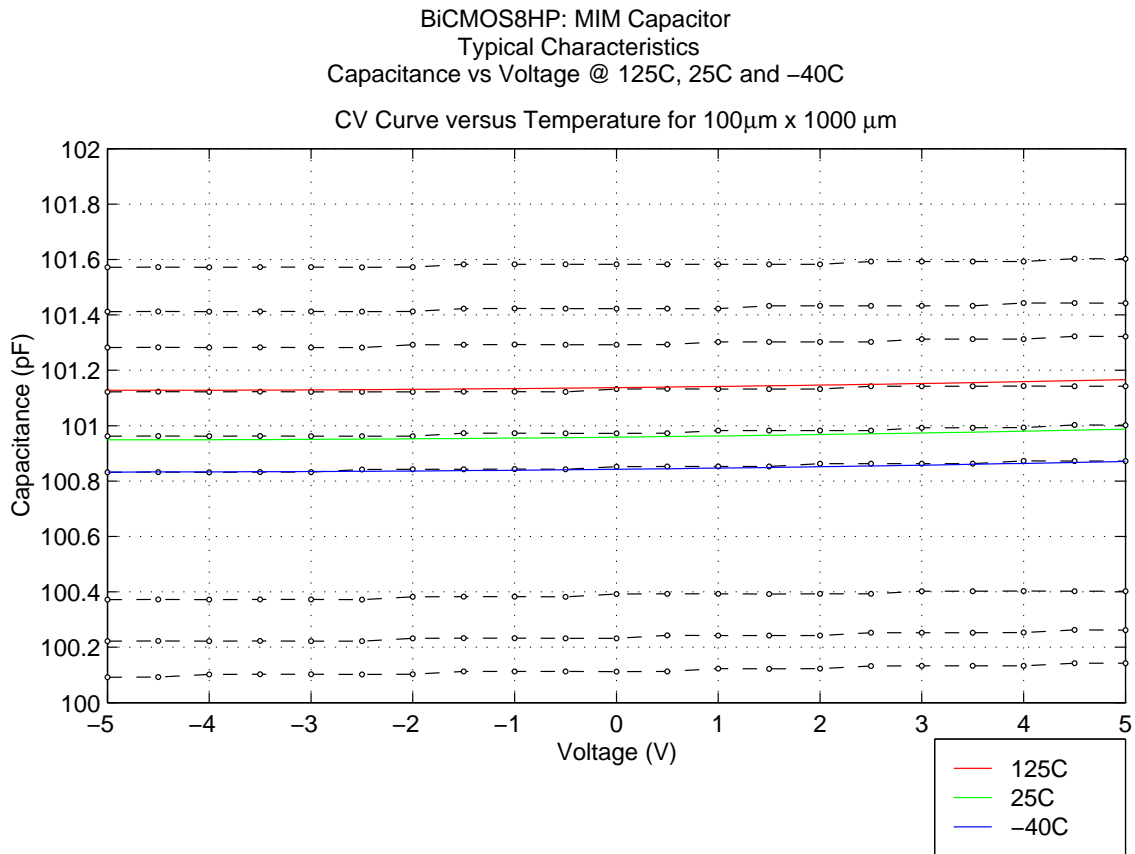
11.4 Model Correlation Plots

The MIM model includes voltage and temperature variation. These are taken from a large 100 μm x 1000 μm sized device. The data from three sites is shown in **Figure 252**. This figure shows that the site-to-site variation, even on the same wafer, far exceeds either the voltage (-5V to 5V) or temperature (-40C to 125C) variation.

We have also measured the S-parameters for the MIM. In **Figure 253** and **Figure 254** we show C_{in} and Q for four sizes of MIM capacitors: 4 μm x 4 μm , 12 μm x 4 μm , 8 μm x 8 μm , and 25 μm x 25 μm . Calibration structures were used to de-embed external capacitance (open de-embedding), resistance, and inductance (short de-embedding). We note that there is a peak in the Q for the 25 μm x 25 μm device just before the self-resonance point. This peak is not real; it is an artifact of the short de-embedding.

In these plots

- $C_{in} = Y_{11}(\text{imag}) / \omega$
- $Q = Y_{11}(\text{imag}) / Y_{11}(\text{real})$



Wafer Parametrics: ncmima=1.0082m

Figure 252. MIM Voltage and Temperature Characteristics for 100x1000 device.

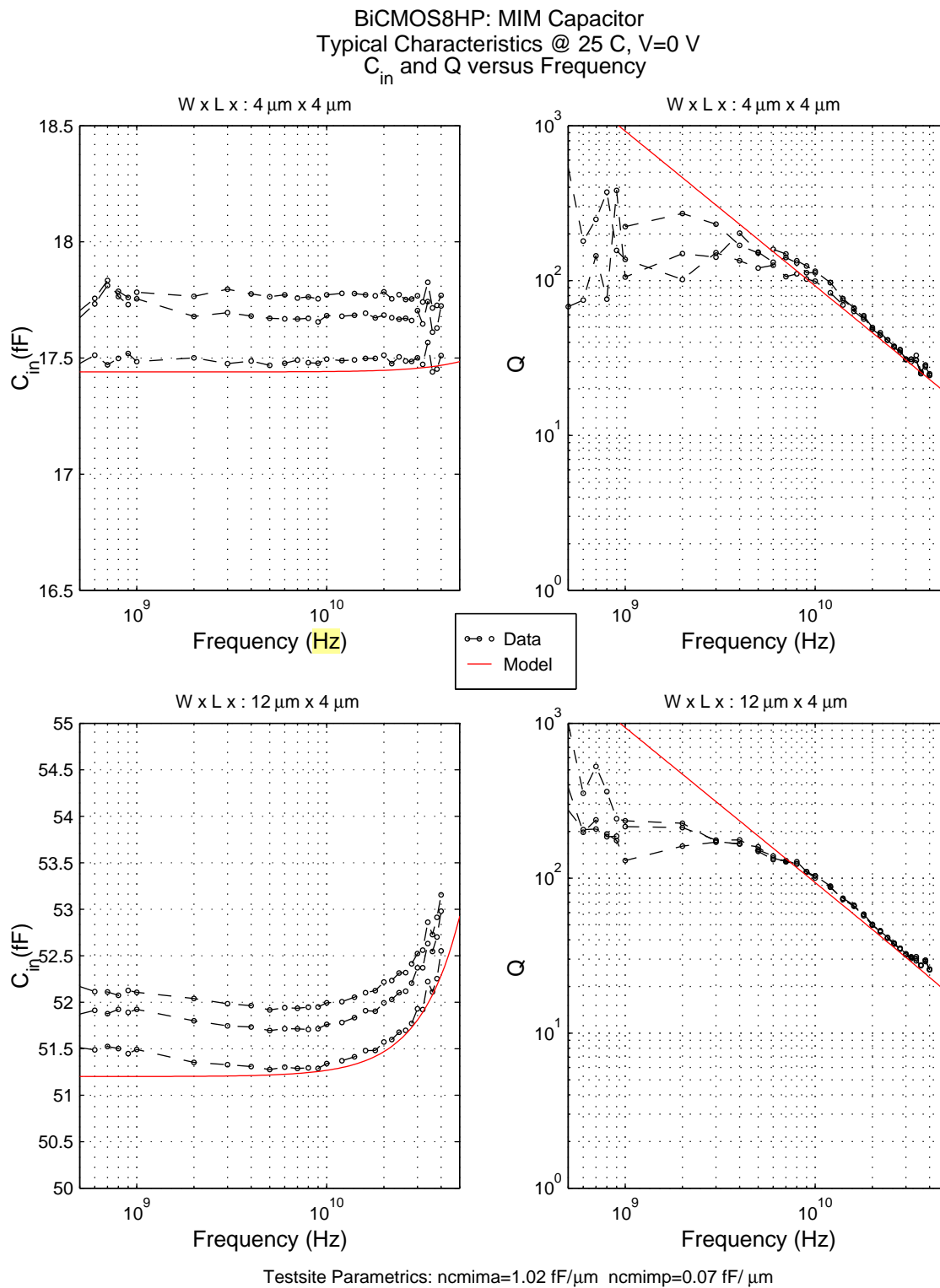


Figure 253. MIM S-Parameter Characteristics for 4x4 and 12x4 devices.

BiCMOS8HP: MIM Capacitor
Typical Characteristics @ 25 C, V=0 V
 C_{in} and Q versus Frequency

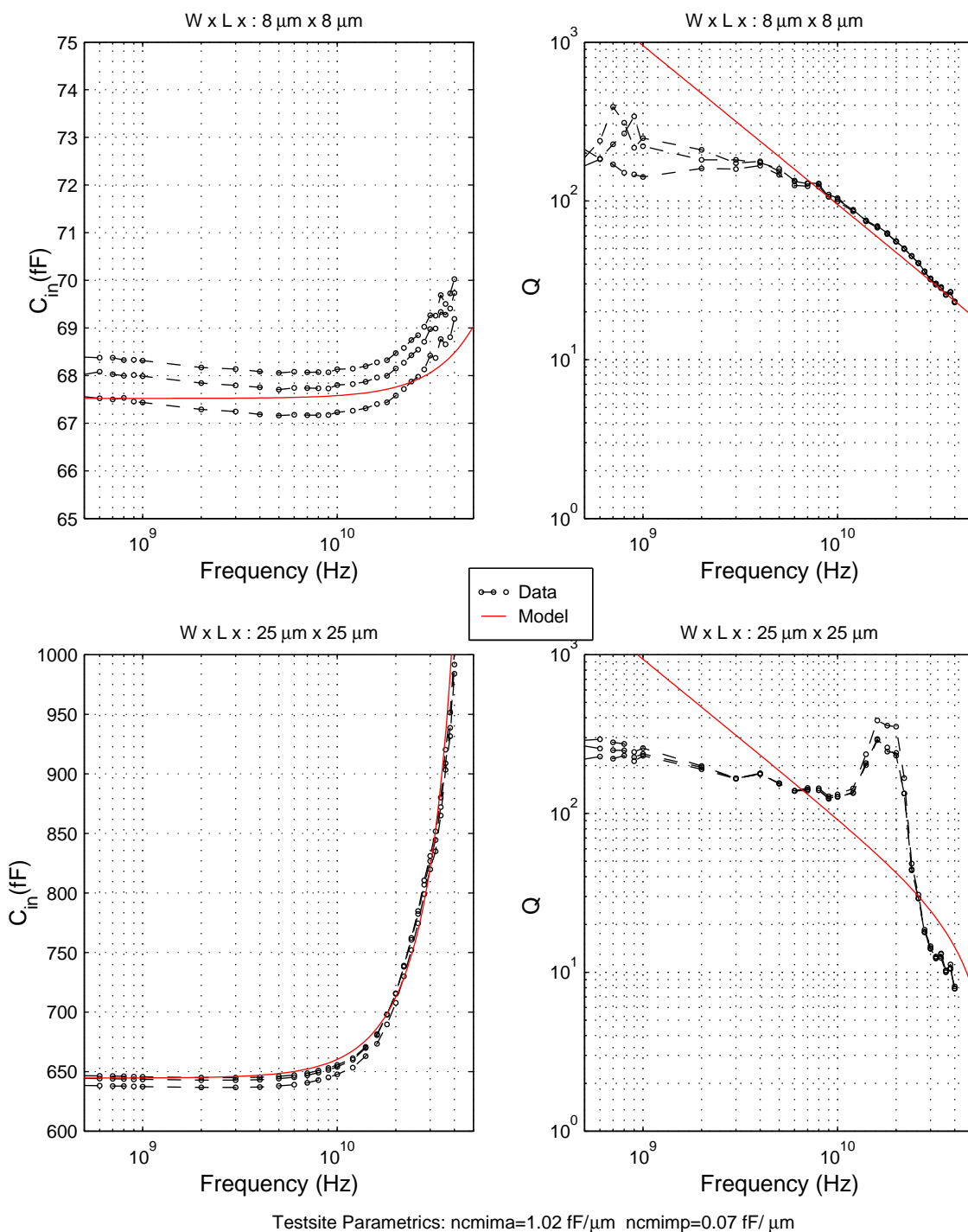


Figure 254. MIM S-Parameter Characteristics for 8x8 and 25x25 devices.

12.0 Inductor Models

BiCMOS8HP offers AM metal inductors with two different groundplane types; DT and M1. For more detailed information concerning the physical structure, model input parameters, and value ranges for the spiral inductor model, refer to the “Inductor Device Models” section of the BiCMOS8HP Design Manual.

12.1 Frequency Dependent Loss Model

The metal turns of a spiral inductor experience two significant loss mechanisms that increase with frequency; skin effect loss and magnetic field induced proximity effect loss.

Skin Effect Loss

The ac current in a metal conductor will flow increasingly on the surface as frequency increases. This causes the conductor's effective resistance and inductance to undergo change over frequency. At high frequencies, the resistance of a conductor increases as a function of the square root of frequency and the inductance decreases slightly and then levels off.

Proximity Effect Loss

In a spiral inductor the enhanced magnetic field that exist in the central portions of the spiral tends to cause nonuniform current flow in the turns. Inner turns tend to have current flow only on the innermost edge of each turn, while outer turns tend to carry current on their outermost edges. This effect is frequency dependent as the magnetic field increases with increasing frequency. The non-uniform current flow is typically called "proximity effect" and tends to cause effective spiral resistance to rise faster than can be attributed to skin effect. In addition, the net inductance will decrease due to an effective reduction in the radius of the spiral caused by the current crowding to the innermost edge of the inner turns. This "proximity effect" can be the dominant loss mechanism at frequencies of interest for multi-turn spirals.

Loss Model

One means of accounting for these frequency dependent loss mechanisms in the model is to use frequency dependent lumped elements (the resistor increasing with frequency and the inductance decreasing). This approach has a large disadvantage due to the fact that general circuit simulators (e.g. spectre, spice,...) can only calculate the frequency dependent element's value at one frequency point per simulation. This means that a frequency at which to calculate the element values is specified at simulation run-time and that value will be used for the entire simulation, even if a broadband, multi-frequency, or transient simulation is done.

An improved method of implementing this frequency dependent behavior in an inductor model is to use an R-L ladder network to replace the series loss elements in the model. An appropriate selection of element values can achieve the desired frequency dependent behavior while maintaining the ability to simulate at all frequencies under all simulation conditions (without needing to specify a frequency at which to calculate the loss). This is the technique that has been implemented in the inductor model.

12.2 Inductor Q Definition

Quality factor (Q), in general, is defined as the peak energy stored per cycle divided by the average power dissipated per cycle for a reactive element with real (resistive) losses. For a spiral inductor, which is modeled with a complex collection of reactive (inductors and capacitors) and resistive elements, the fundamental definition for Q is difficult to calculate. The reason for this is that the instantaneous energy storage must be known for each reactive element in addition to the average power dissipated. This information is simply not available from an examination of the network (S, Y, Z, etc.) parameters of the spiral. The reader is referred to the following citation for a detailed explanation of various techniques for calculating spiral inductor Q

(Kenneth O, "Estimation Methods for Quality Factors of Inductors Fabricated in Silicon Integrated Circuit Process Technologies", IEEE Journal of Solid-State Circuits, vol. 33, no. 8, August 1998).

A common method for calculating Q from network parameters (Y) is to divide the imaginary component of Y11 by the real component of Y11:

$$Q_{CONV} = -\frac{\text{Imag}\{Y_{11}\}}{\text{Real}\{Y_{11}\}}$$

This is convenient in that no knowledge of the energy storing capability of the internal reactive elements of the spiral is required. This method will be called "conventional" Q in this Model Reference Guide. This definition is accurate at low frequencies where the spiral acts like a series R-L circuit (parasitic capacitances have very high impedances). However, as the impedance of the parasitic capacitive elements approaches that of the inductive reactance (near the peak Q frequency), the simplistic assumption of a series R-L circuit yields a pessimistic estimate of the actual Q of the spiral.

Spiral inductors are often used in differential circuits. In order to reflect the unique characteristics observed when driving the spiral differentially, a new definition of Q has been proposed (and discussed in the above mentioned paper by Ken O) called "differential Q". This definition for Q is calculated by converting the standard two-port s-parameters of an inductor measured/simulated as a two-port structure into a single differential impedance. "Differential Q" is then defined as the ratio of the imaginary and real parts of the differential impedance.

$$Z_{diff} = 2 \cdot Z_0 \cdot \frac{(1 - S_{21})(1 - S_{12}) - (S_{11} \cdot S_{22})}{(1 - S_{22}) \cdot (1 - S_{11}) - (S_{12} \cdot S_{21})} \quad (\Omega)$$

$$Q_{diff} = \frac{\text{Imag}\{Z_{diff}\}}{\text{Real}\{Z_{diff}\}}$$

At the peak Q frequency (defined by the "conventional" Q) and beyond, yet another definition for Q is desired that more accurately reflects the fundamental definition of Q (the peak energy stored per cycle divided by the average power dissipated per cycle). As described in the aforementioned article, a definition of Q has been suggested that takes into account the behavior of the spiral when it is parallel resonated with an ideal capacitor. This definition has more meaning in the context of the actual characteristics of the spiral when it is included in a circuit. The resulting Q of this parallel resonant circuit can then be extracted either from an examination of the impedance bandwidth or the phase stability:

$$Q_{BW} = \frac{\omega_0}{3\text{dB bandwidth}}$$

$$Q_{PS} = \frac{SF}{2}$$

$$SF = -\omega_0 \left. \frac{d\phi}{d\omega} \right|_{\omega = \omega_0} \quad (\text{Stability Factor})$$

Either method will yield the same value for a simple parallel resonant R-L-C circuit. Although the spiral inductor is a more complex circuit, both the phase stability and bandwidth methods yield the same result.

In order to calculate a Q versus frequency characteristic for the spiral using one of these "circuit" Q definitions, the ideal capacitance added in parallel is swept in value to achieve a range of resonant frequencies.

Depending on the geometry, the "differential" and "circuit" Q definitions may yield substantially higher values at frequencies above the peak Q frequency than does the "conventional" definition. In general, the more parallel capacitance (the more turns) present in the spiral, the more the two "non-conventional" Q definitions will deviate from "conventional Q". This is due to some of the parasitic capacitance of the spiral being "absorbed" into the capacitance being used to resonate the spiral. In other words, if the parasitic parallel capacitance is well modeled (as it is in the scalable octagonal inductor model), it can be utilized in parallel with any added circuit capacitance to resonate the spiral.

For the purposes of this Model Reference Guide, all references to Q will assume the "conventional" definition unless otherwise stated.

12.3 DT Inductor Grounding Concerns During Simulation

The DT inductor model ground terminal is intended to be connected directly to an AC ground (DC bias) when included in a circuit simulation. If a series resistance is inserted between the inductor ground terminal and AC ground in order to model the proximity of substrate contacts, the simulation will be incorrect. The ground terminal of the inductor model is connected to the global node “gnd!” by default at instance creation in the BiCMOS8HP Design Kit. This is intended to be a perfect AC ground (no series impedance). The actual DC bias level on this terminal is not important (for inductor simulation), as there are no diode junctions connected internally to the inductor model ground terminal.

Under no circumstances should the ground terminal of the inductor be connected to the global substrate node “sub!”. The current return path from the “sub!” node is through the substrate contact model (subc). This inserts a series resistance between “sub!” and the DC bias connected to the substrate contact (usually gnd! node). This series resistance will tend to decouple the substrate losses of the inductor, increasing the simulated Q in a non-physical manner.

Simulating the inductor from a post layout extracted view in Cadence presents a specific difficulty in recognizing the proper connection of the ground node for the inductor. Since there is no physical third terminal related to the inductor, no connection between the ground node and the desired AC ground node (e.g. gnd!) will be extracted. This means that the third node of the inductor will be extracted as a floating node unless the appropriate layout steps are taken. The “BB Connection for Inductor and RFLINE” section of the BiCMOS8HP Process Design Kit User’s Guide document details the additional pseudo-connection (BB IND) required to be made between the inductor and the actual AC ground node in order to extract the proper ground node for the inductor. With this connection in place between the inductor and any M1 metallization that is connected to a substrate contact, the third terminal of the inductor will extract as being connected to the node associated with the M1 metallization on the substrate contact.

It is important to note that the M1 connection between the “BB IND” shape and the actual DC bias for that net, should be a wide, low resistance (low impedance) connection. If too much series resistance is extracted between the intersection of M1 of the “BB IND” and the DC bias, the substrate loss will tend to be decoupled, causing an overoptimistic simulation of the inductor. The series resistance should be kept below 10 Ω in all cases.

12.4 DT Inductor Grounding Concerns for Physical Layout

The inductors were measured and modelled with substrate contacts approximately 80 μ m away from the four corners of the spiral. It has been determined that the placement of substrate contacts in the vicinity of the inductor has essentially no effect on the characteristics, as long as the substrate contacts are kept at least 50 μ m away from the spiral. If substrate contacts are placed closer than 50 μ m, there may be a reduction in the actual Q.

12.5 Choosing DT vs M1 Groundplane

For any particular supported spiral geometry, there exist two possible substrate/groundplane layouts (M1 and DT). DT inductors have an opening in the pwell underneath the spiral to increase the resistivity of the substrate underneath the spira with a mesh of deep trench in the region devoid of pwell, while M1 inductors have a low impedance M1 comb shaped groundplane underneath them configured as a Faraday shield. The purpose of this shield is to terminate the parasitic electric field from the spiral before it reaches the substrate, thus lowering substrate losses. The proper choice between the two possibilities is dependent upon the application, but should take into account the following differences in behavior between the two types.

In all cases (for all geometries) the self resonant frequency is less for M1 groundplanes in comparison to DT inductors. This is a result of providing a low impedance groundplane in the M1 case, which accentuates the parallel spiral to substrate capacitances. Additionally, the behavior of Q with frequency differs between the two types: M1 groundplane inductors exhibit a sharper roll-off in the Q curve at frequencies above the peak Q frequency than do DT groundplane inductors.

The effective inductance, as calculated by:

$$\text{Inductance} = \frac{-Y_{21}\text{imag}}{\omega \cdot [(Y_{21}\text{real})^2 + (Y_{21}\text{imag})^2]} \text{ (H)}$$

also has a different behavior for the two types of inductors. For M1 groundplane inductors, there is a pronounced roll-off of the inductance characteristic with increasing frequency that is much less obvious in the DT inductors. In the M1 inductors, this roll-off may already be significant at or near the peak Q frequency. The explanation for this is that the M1 inductors are closer to self resonance at the peak Q frequency and, therefore, the characteristics are more influenced by the phase shift associated with self resonance. For virtually all geometries, the peak Q value will be greater for the M1 inductor. An additional advantage of the M1 groundplane is the shielding effect provided by the groundplane. The substantial crosstalk present between the spiral and substrate is effectively short circuited, minimizing noise injection and pick-up to/from the substrate. The detrimental effects of the M1 groundplane must be weighed with respect to the benefits of increased Q and isolation in making a choice between the M1 and DT inductor layouts.

12.6 Using M1 Groundplane With a Grounded Spiral

In many applications for integrated inductors, one end of the spiral will be at AC ground potential. When using the M1 groundplane inductor in an application of this type, it is suggested that the center of the spiral be placed at AC ground with the same connection that is used to ground the M1 groundplane. The reason for this is that the most benefit from the M1 groundplane is achieved when the ground potential for the spiral is exactly the same as the ground potential of the M1 groundplane. The instance properties editor in the BiCMOS8HP Design Kit Schematic/Layout Interface provides a check box labelled “External Connection for M1?” that can be used to eliminate the external M1 connection to the M1 groundplane. If this external connection is removed, the M1 groundplane’s central M1 connection should be connected directly to the innermost turn of the spiral through a low impedance via array. If the box is checked, then the M1 groundplane will be available for biasing separately from the innermost turn of the spiral (applications where one end of the spiral is not at AC ground potential).

12.7 Methodology for Choosing Geometric Parameters

The simulated peak Q, peak Q frequency and inductance for various geometries of DT and M1 inductors are shown in Tables 78 through 81 and they can be a useful tool in estimating the achievable values of peak Q and peak Q frequency given the desired inductance. An appropriate line width can be chosen that causes the inductor to peak at the correct frequency. The BiCMOS8HP Design Kit Schematic/Layout Interface can then be used to pick an appropriate number of turns and outer dimension, at the chosen line width, that achieves the desired inductance.

Alternatively, a minimum acceptable value for peak Q can be chosen and an inductance, outer dimension, line width and number of turns picked that will yield that value of peak Q at the correct frequency. The instance properties editor of the BiCMOS8HP Design Kit Schematic/Layout Interface provides a calculation of the inductance for any particular combination of geometric parameters. This calculation is provided as an estimate for user convenience. For accurate prediction of inductance and peak Q frequency, an s-parameter simulation is recommended. Given these tables and the Design Kit interface, trade-offs can be made between inductance, inductor area, peak Q frequency and peak Q value to come to an optimized choice of inductor geometry for a specific application.

12.8 AM inductor

12.8.1 AM Inductor Geometric Parameters

This table shows examples using the DT groundplane with 5μm turn-turn space:

Table 78. AM Inductor Geometry Reference Table (DT groundplane), $amrs=0.007 \text{ ohm/sq}$, $nlev=5$

Ground plane	Outer diameter (x)	Number of turns (n)	Turn width (w)	Turn-turn Space (s)	Peak Q	Peak Q Frequency	Inductance
DT	100um	1.5	5um	5um	23.7	27.9GHz	0.39nH
DT	200um	1.5	5um	5um	16.2	8.6GHz	1.09nH
DT	300um	1.5	5um	5um	14.0	5.1GHz	1.87nH
DT	100um	3.5	5um	5um	16.4	18.7GHz	0.88nH
DT	200um	3.5	5um	5um	14.3	4.1GHz	3.35nH
DT	300um	3.5	5um	5um	12.3	2.4GHz	6.36nH
DT	200um	2.5	10um	5um	17.2	4.6GHz	1.66nH
DT	200um	3.5	10um	5um	15.6	4.0GHz	2.35nH
DT	300um	3.5	10um	5um	15.2	2.1GHz	4.95nH
DT	200um	4.5	10um	5um	13.4	4.1GHz	2.88nH
DT	300um	3.5	15um	5um	15.4	2.1GHz	3.86nH
DT	300um	3.5	20um	5um	14.3	2.2GHz	3.01nH
DT	300um	3.5	25um	5um	12.8	2.4GHz	2.34nH

This table shows examples using the M1 groundplane:

Table 79. AM Inductor Geometry Reference Table (M1 groundplane), $amrs=0.007$ ohm/sq, $nlev=5$

Ground plane	Outer diameter (x)	Number of turns (n)	Turn width (w)	Turn-turn Space (s)	Peak Q	Peak Q Frequency	Inductance
M1	100um	1.5	5um	5um	28.2	29.3GHz	0.39nH
M1	200um	1.5	5um	5um	21.4	12.6GHz	1.09nH
M1	300um	1.5	5um	5um	18.4	7.8GHz	1.87nH
M1	100um	3.5	5um	5um	18.4	18.7GHz	0.88nH
M1	200um	3.5	5um	5um	19.3	5.8GHz	3.35nH
M1	300um	3.5	5um	5um	16.5	3.5GHz	6.35nH
M1	200um	2.5	10um	5um	23.3	7.5GHz	1.66nH
M1	200um	3.5	10um	5um	21.0	6.0GHz	2.35nH
M1	300um	3.5	10um	5um	20.7	3.2GHz	4.94nH
M1	200um	4.5	10um	5um	17.4	5.5GHz	2.88nH
M1	300um	3.5	15um	5um	20.6	3.2GHz	3.86nH
M1	300um	3.5	20um	5um	18.9	3.4GHz	3.00nH
M1	300um	3.5	25um	5um	16.7	3.7GHz	2.34nH

Tables **80** and **81** show the same information for the AM version of the inductor with 3um turn-turn space.

This table shows examples using the DT groundplane:

Table 80. AM Inductor Geometry Reference Table (DT groundplane), $amrs=0.007$ ohm/sq, $nlev=5$

Ground plane	Outer diameter (x)	Number of turns (n)	Turn width (w)	Turn-turn Space (s)	Peak Q	Peak Q Frequency	Inductance
DT	100um	1.5	5um	3um	24.0	26.3GHz	0.42nH
DT	200um	1.5	5um	3um	16.5	8.3GHz	1.13nH
DT	300um	1.5	5um	3um	14.3	5.1GHz	1.93nH
DT	100um	3.5	5um	3um	19.2	14.7GHz	1.09nH
DT	200um	3.5	5um	3um	15.2	3.8GHz	3.75nH
DT	300um	3.5	5um	3um	13.0	2.3GHz	6.92nH
DT	200um	2.5	10um	3um	18.0	4.3GHz	1.77nH
DT	200um	3.5	10um	3um	17.0	3.7GHz	2.60nH
DT	300um	3.5	10um	3um	16.0	2.0GHz	5.31nH
DT	200um	4.5	10um	3um	15.2	3.5GHz	3.32nH
DT	300um	3.5	15um	3um	16.4	2.0GHz	4.13nH
DT	300um	3.5	20um	3um	15.4	2.0GHz	3.22nH
DT	300um	3.5	25um	3um	13.6	2.3GHz	2.50nH

This table shows examples using the M1 groundplane:

Table 81. AM Inductor Geometry Reference Table (M1 groundplane), AMrs=0.007 ohm/sq, nlev=5

Ground plane	Outer diameter (x)	Number of turns (n)	Turn width (w)	Turn-turn Space (s)	Peak Q	Peak Q Frequency	Inductance
M1	100um	1.5	5um	3um	28.6	28.2GHz	0.42nH
M1	200um	1.5	5um	3um	21.6	12.0GHz	1.13nH
M1	300um	1.5	5um	3um	18.5	7.4GHz	1.93nH
M1	100um	3.5	5um	3um	22.7	16.1GHz	1.09nH
M1	200um	3.5	5um	3um	20.5	5.5GHz	3.75nH
M1	300um	3.5	5um	3um	17.0	3.3GHz	6.91nH
M1	200um	2.5	10um	3um	24.2	7.2GHz	1.77nH
M1	200um	3.5	10um	3um	22.8	5.7GHz	2.60nH
M1	300um	3.5	10um	3um	21.5	3.1GHz	5.30nH
M1	200um	4.5	10um	3um	20.3	5.0GHz	3.32nH
M1	300um	3.5	15um	3um	21.8	3.1GHz	4.13nH
M1	300um	3.5	20um	3um	20.2	3.2GHz	3.22nH
M1	300um	3.5	25um	3um	17.7	3.6GHz	2.50nH

12.9 Peak Q Frequency vs Inductance

Notice (in Figure 255) that there is a linear relationship between peak Q frequency and inductance which is in agreement with the fact that small inductors are generally used at higher frequencies and large inductors at lower frequencies. This plot was made using nlev=5 with DT groundplane, but the same trend can be seen for M1 groundplane and other stacking options (nlev=6 and 7).

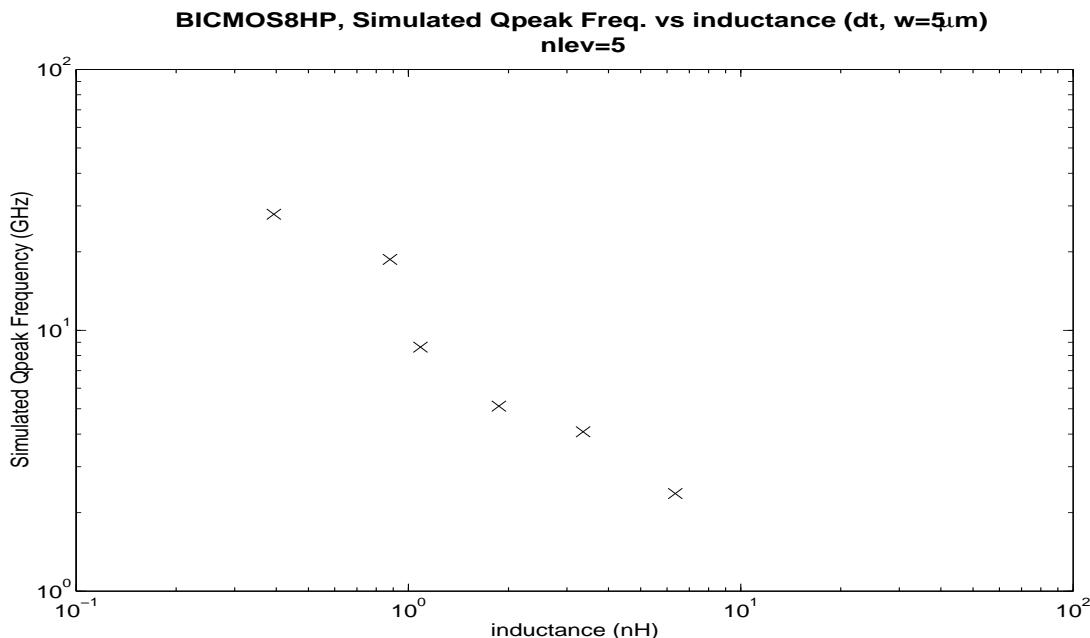


Figure 255. Simulated Peak Q Freq vs. Inductance for various geometries

12.10 Temperature Simulation Notes

Q decreases with increasing temperature over the frequency range up to and including the frequency where Q peaks. However inductance changes only a small amount over temperature. The behavior of Q with temperature can be explained by the spiral metalization and substrate resistance TCR's. Q decreases with increasing temperature below the peak Q frequency due to the positive TCR of the spiral metalization and the trend is reversed at higher frequencies due to the positive TCR of the substrate resistivity.

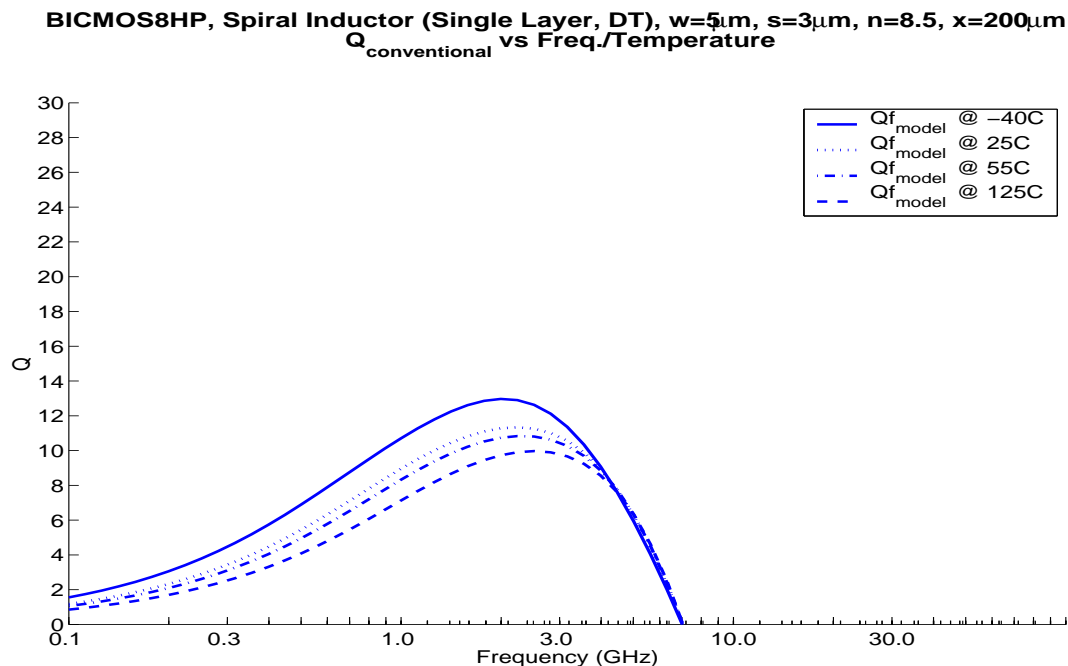


Figure 256. AM Simulated Q vs. Freq with varying temp, DT inductor: $x=200\mu\text{m}$, $n=8.5$, $w=5\mu\text{m}$, $s=3\mu\text{m}$

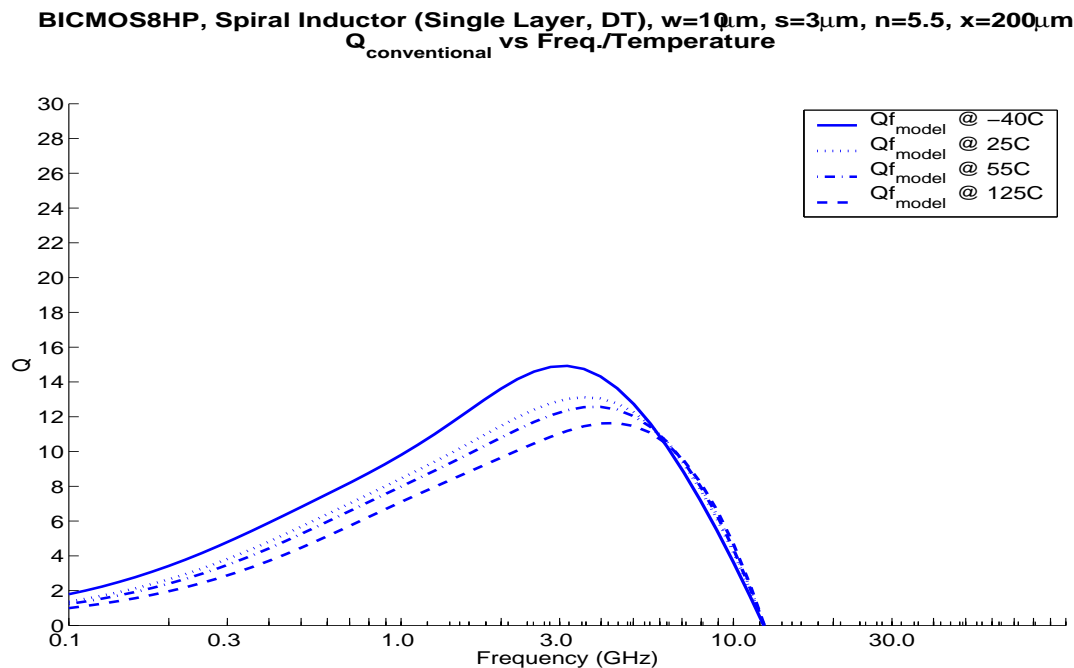


Figure 257. AM Simulated Q vs. Freq with varying temp, DT inductor: $x=200\mu\text{m}$, $n=5.5$, $w=10\mu\text{m}$, $s=3\mu\text{m}$

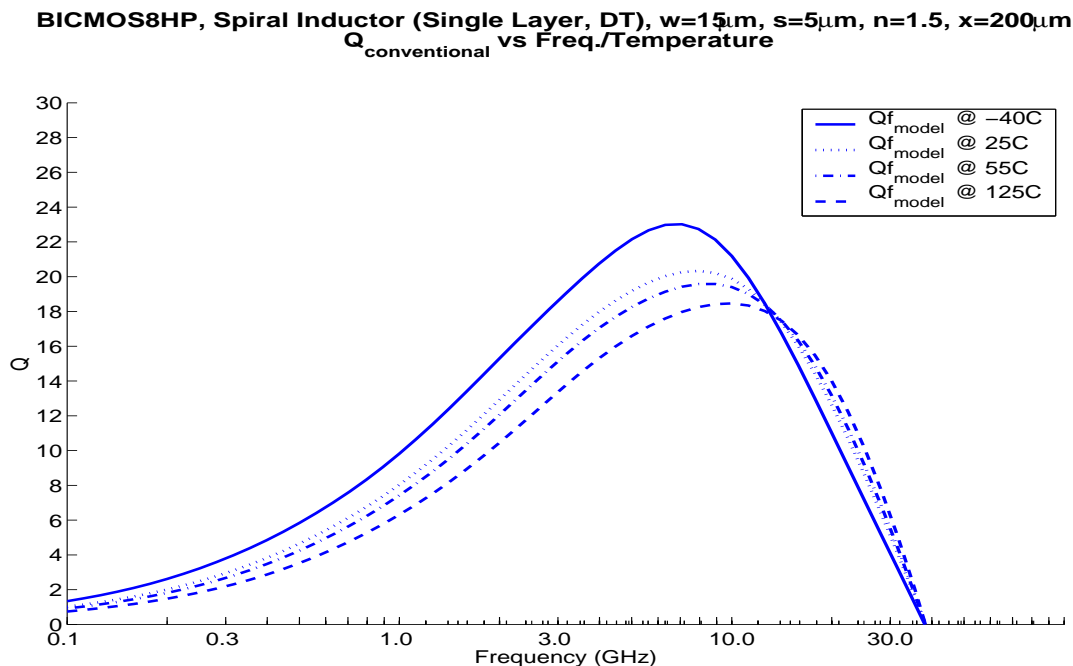


Figure 258. AM Simulated Q vs. Freq with varying temp, DT inductor: $x=200\mu\text{m}$, $n=1.5$, $w=15\mu\text{m}$, $s=5\mu\text{m}$

12.11 Variable Metal Level Simulation Notes

The variation in Q with varying numbers of metal levels is caused by the decreasing capacitance present between the spiral and the substrate as the number of metal levels (nlev) in a design grows from 5 to 7. This decreasing capacitance causes a corresponding increase in Q, as the substrate loss is less pronounced.

Figures 259, 260 and 261 show simulated variation of Q vs. frequency for three different AM spiral geometries with various metal stacking options.

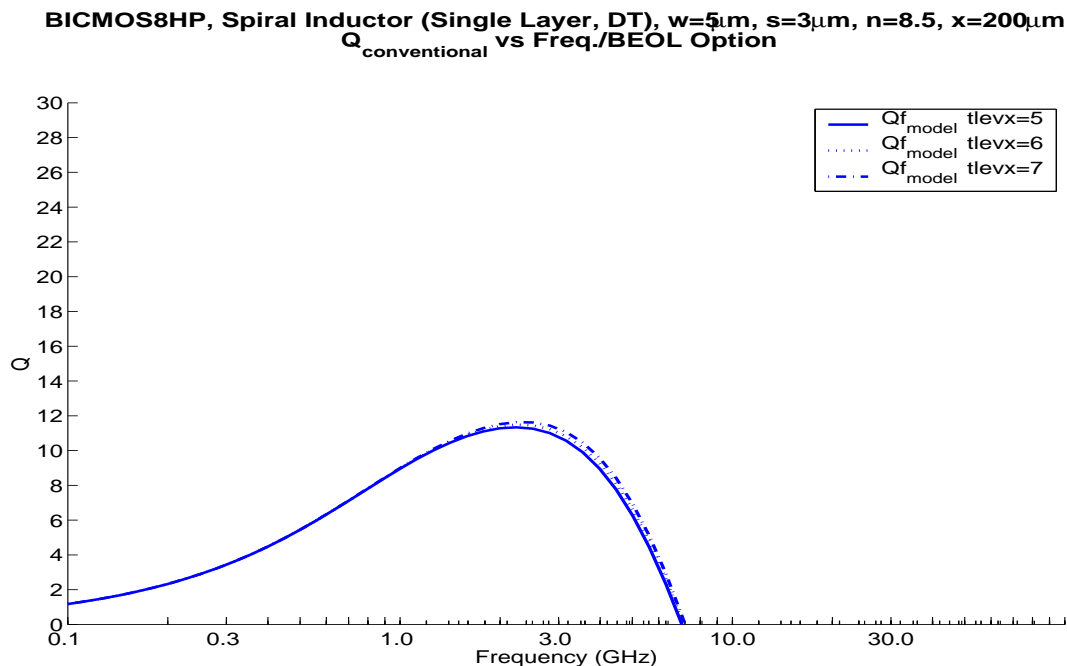


Figure 259. AM Simulated Q vs. Freq w/varying # metal levels, DT inductor: $x=200\mu\text{m}$, $n=8.5$, $w=5\mu\text{m}$, $s=3\mu\text{m}$

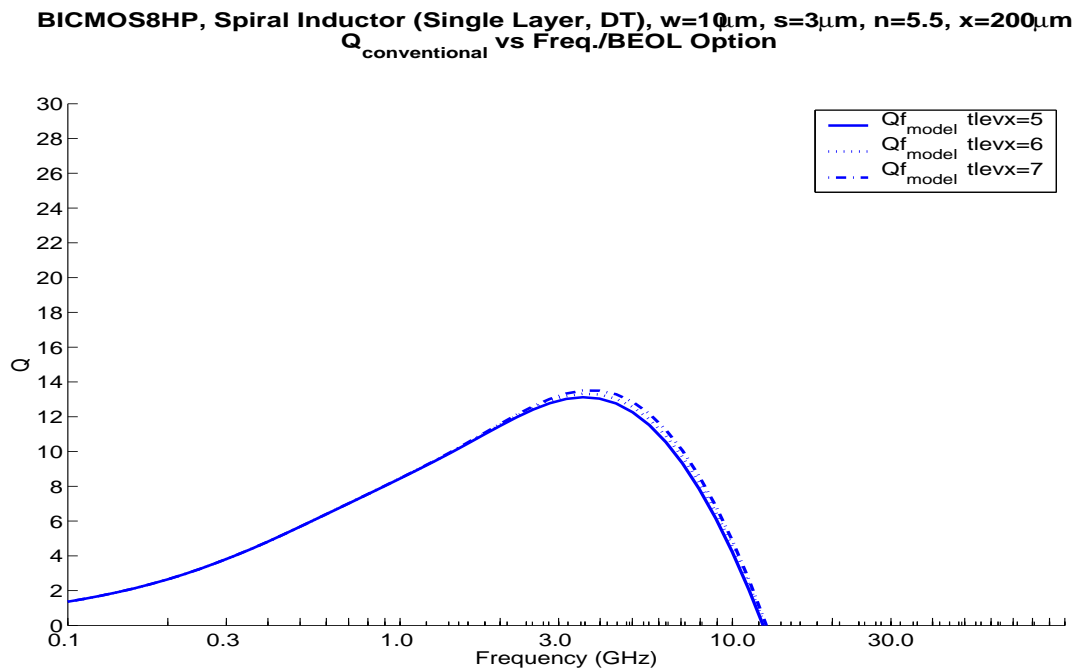


Figure 260. AM Simulated Q vs. Freq w/varying # metal levels, DT inductor: $x=200\mu\text{m}$, $n=5.5$, $w=10\mu\text{m}$, $s=3\mu\text{m}$

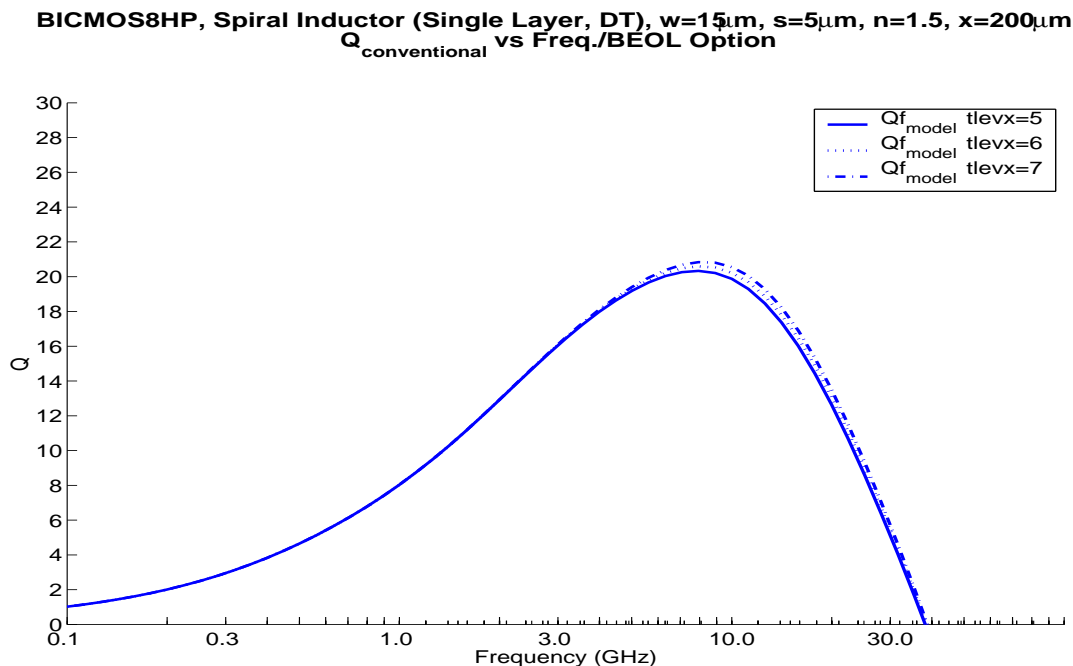


Figure 261. AM Simulated Q vs. Freq w/varying # metal levels, DT inductor: $x=200\mu\text{m}$, $n=1.5$, $w=15\mu\text{m}$, $s=5\mu\text{m}$

12.12 Model Optimization Notes

The model was optimized to provide a good fit to the Q and inductance values extracted from measurements. Q was calculated using both the “conventional” and “differential” definitions (see “Inductor Q Definition” on page 336.).

The inductance was extracted from the measured Y-Parameters using:

$$\text{Inductance} = \frac{-Y_{21}\text{imag}}{\omega \cdot [(Y_{21}\text{real})^2 + (Y_{21}\text{imag})^2]} \text{ (H)} .$$

The model was adjusted to yield the best Q fit, for both “conventional” and “differential” Q definitions, at the peak Q frequency and for as wide a range as possible around the peak Q frequency.

Figures 262 through 273 show simulation versus measured data results for inductance and Q for DT and M1 inductors.

12.13 Model vs. Hardware Relative Errors

Based on the performance of the model in BICMOS8HP the following statements can be made: Over a range of inductor geometries with diameters from 100 μm to 300 μm , simulation provides a peak Q value deviation from measured data of about +/-20% or less for both DT and M1 inductors. For smaller diameter inductors with higher Q values, measurement of Q has been challenging showing up to 50% differences to the model. The model is the more conservative value and we think it is more correct than our measurements. The relative error between the simulated inductance value (at low frequency) for the full range of geometries supported by the pcell (down to 50 μm symind and 60.7 μm ind diameters) and the measured inductance value is +/- 5% or less.

12.14 Model Correlation Plots

Correlation plots in this section show measured and simulated inductor Q and inductance with respect to frequency for a variety of inductor geometries. The plots show both the conventional Q and the differential Q as defined in **section 12.2** , “**Inductor Q Definition**” on page 336.

Examples are included for AM standard inductors(ind) for two different ground planes(DT and M1).

12.14.1 AM (“ind” model) Correlation Plots

**BICMOS8HP, Spiral Inductor (Single Layer, DT), $w=10\mu\text{m}$, $s=5\mu\text{m}$, $n=4.5$, $x=200\mu\text{m}$
 $n\text{lev}=5$**

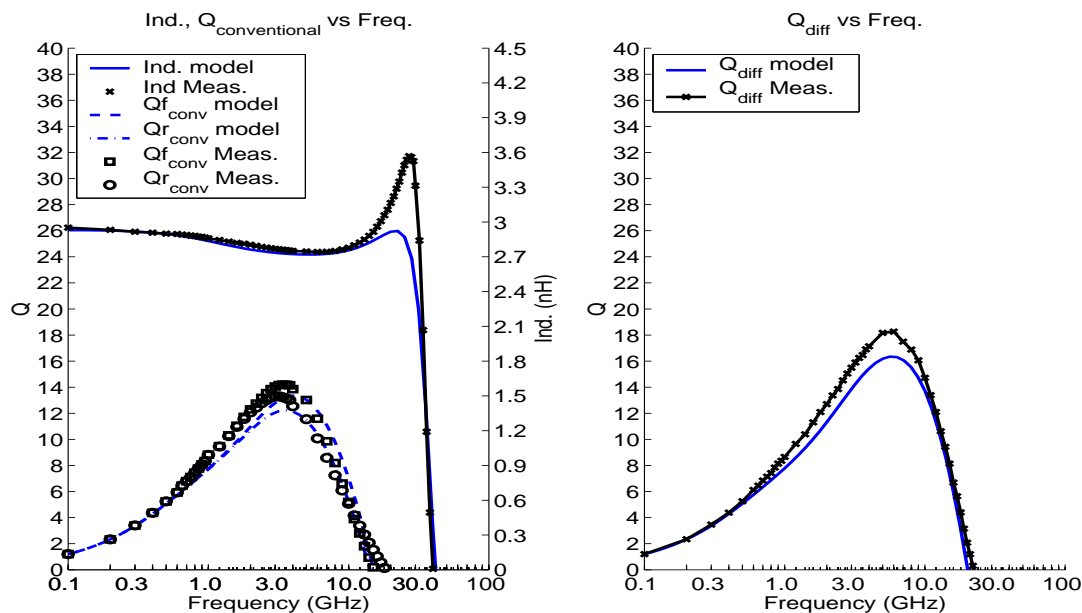


Figure 262. AM, DT, $w=10\mu\text{m}$, $s=5\mu\text{m}$, $n=4.5$, $x=200\mu\text{m}$

**BICMOS8HP, Spiral Inductor (Single Layer, M1), $w=10\mu\text{m}$, $s=5\mu\text{m}$, $n=4.5$, $x=200\mu\text{m}$
 $n\text{lev}=5$**

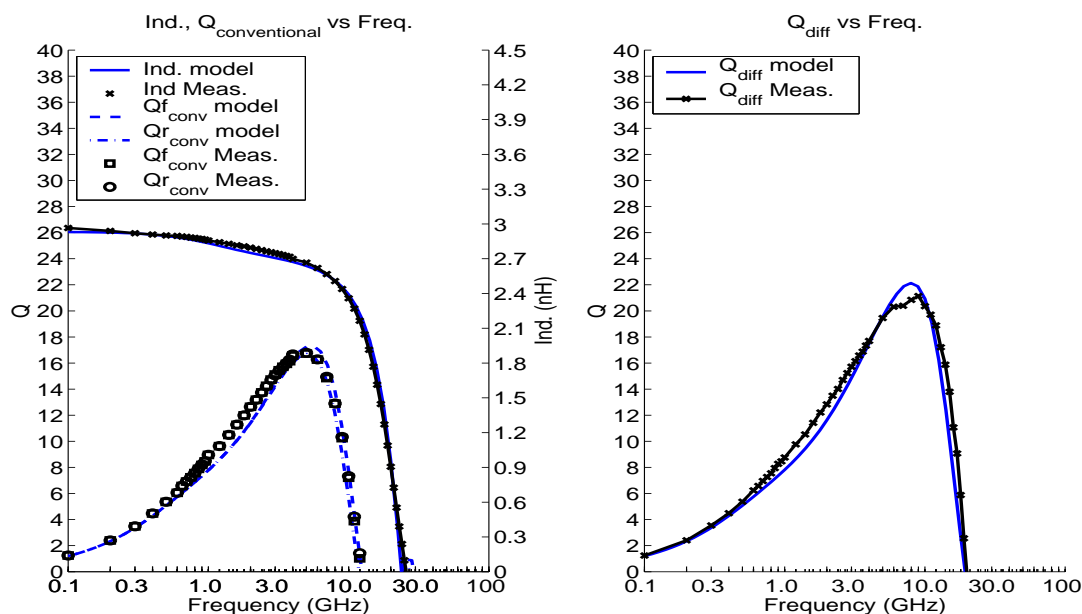


Figure 263. AM, M1, $w=10\mu\text{m}$, $s=5\mu\text{m}$, $n=4.5$, $x=200\mu\text{m}$

**BICMOS8HP, Spiral Inductor (Single Layer, DT), $w=15\mu m$, $s=5\mu m$, $n=4.5$, $x=300\mu m$
nlev=5**

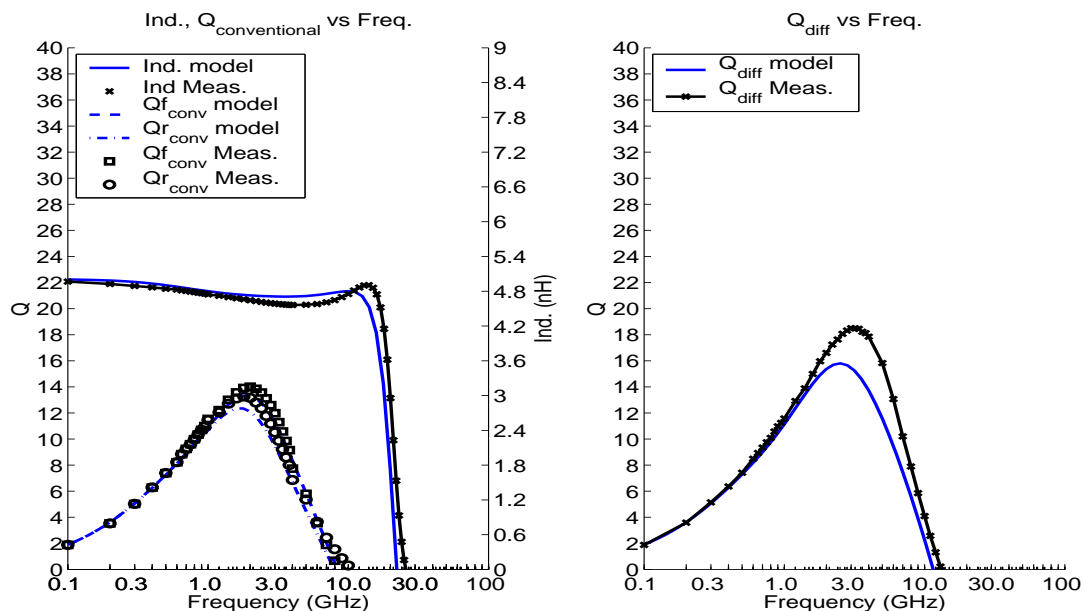


Figure 264. AM, DT, $w=15\mu m$, $s=5\mu m$, $n=4.5$, $x=300\mu m$

**BICMOS8HP, Spiral Inductor (Single Layer, M1), $w=15\mu m$, $s=5\mu m$, $n=4.5$, $x=300\mu m$
nlev=5**

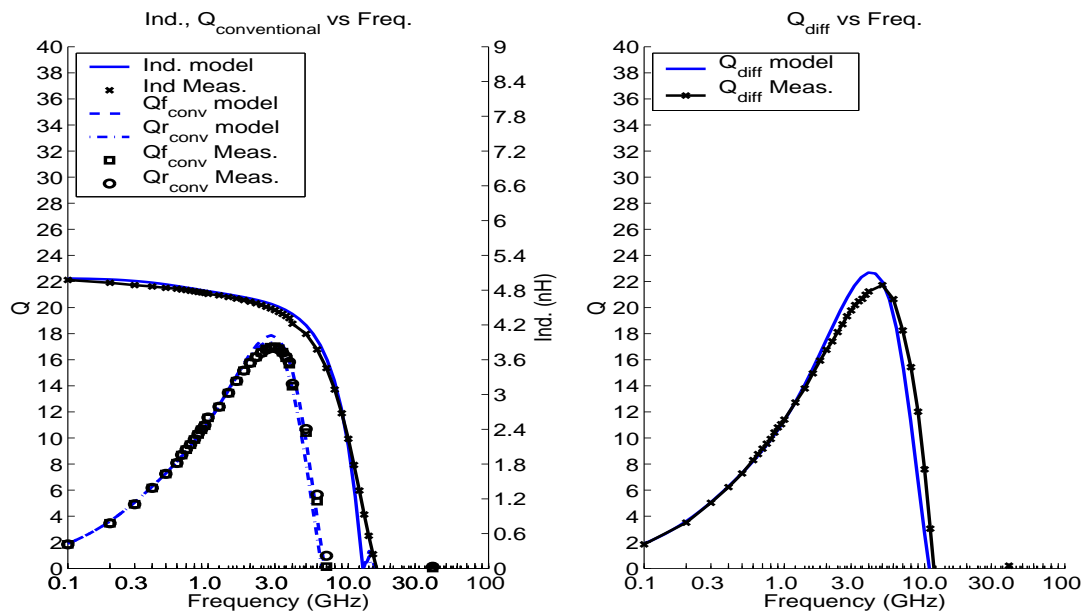


Figure 265. AM, M1, $w=15\mu m$, $s=5\mu m$, $n=4.5$, $x=300\mu m$

**BICMOS8HP, Spiral Inductor (Single Layer, DT), $w=25\mu\text{m}$, $s=5\mu\text{m}$, $n=1.5$, $x=300\mu\text{m}$
nlev=5**

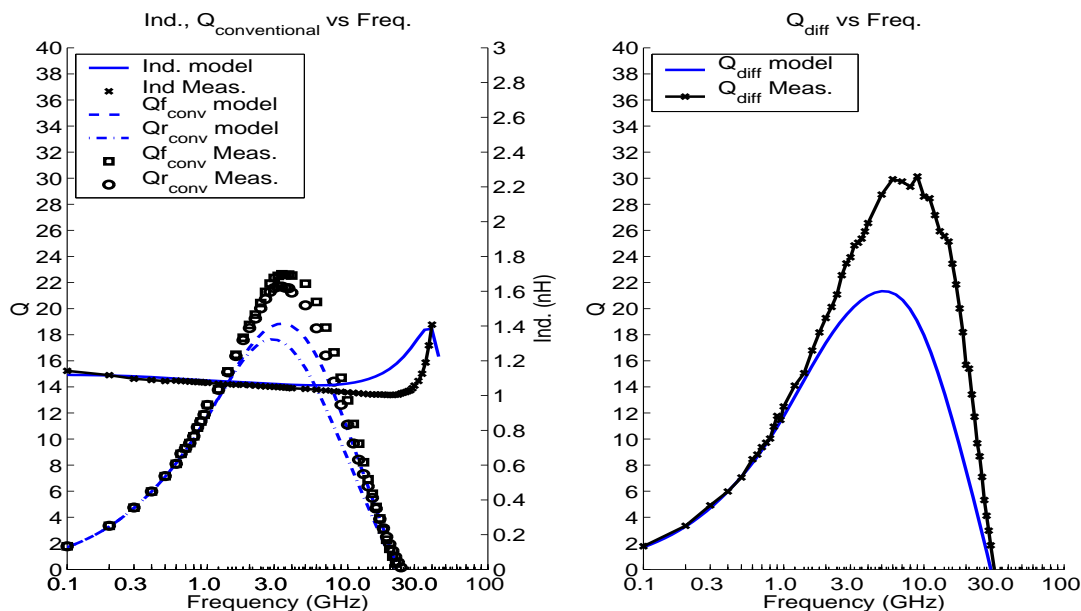


Figure 266. AM, DT, $w=25\mu\text{m}$, $s=5\mu\text{m}$, $n=1.5$, $x=300\mu\text{m}$

**BICMOS8HP, Spiral Inductor (Single Layer, M1), $w=25\mu\text{m}$, $s=5\mu\text{m}$, $n=1.5$, $x=300\mu\text{m}$
nlev=5**

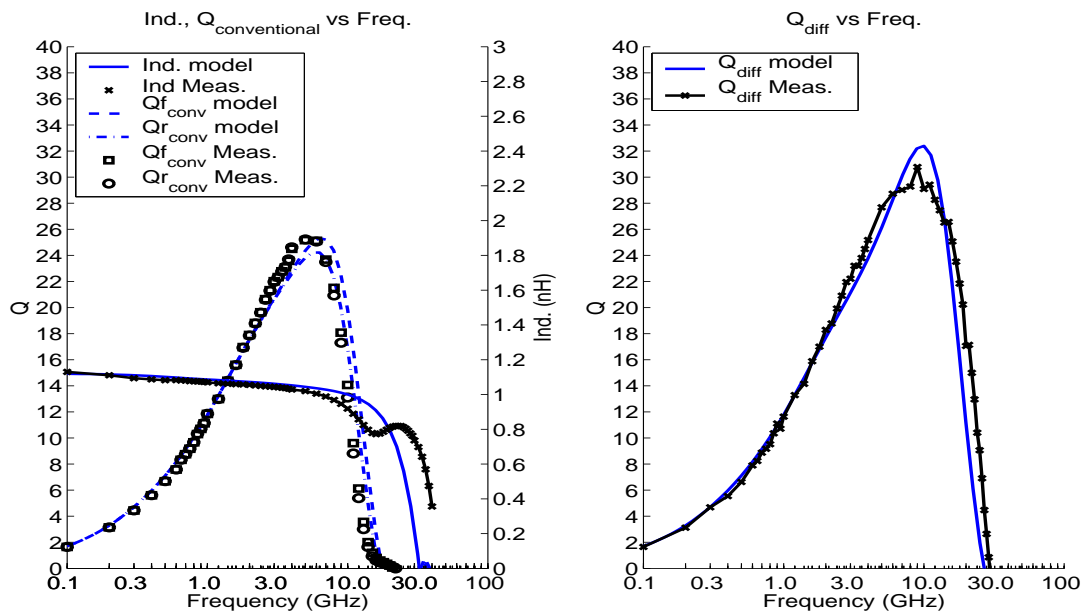


Figure 267. AM, M1, $w=25\mu\text{m}$, $s=5\mu\text{m}$, $n=1.5$, $x=300\mu\text{m}$

**BICMOS8HP, Spiral Inductor (Single Layer, DT), $w=5\mu\text{m}$, $s=3\mu\text{m}$, $n=3.5$, $x=100\mu\text{m}$
nlev=5**

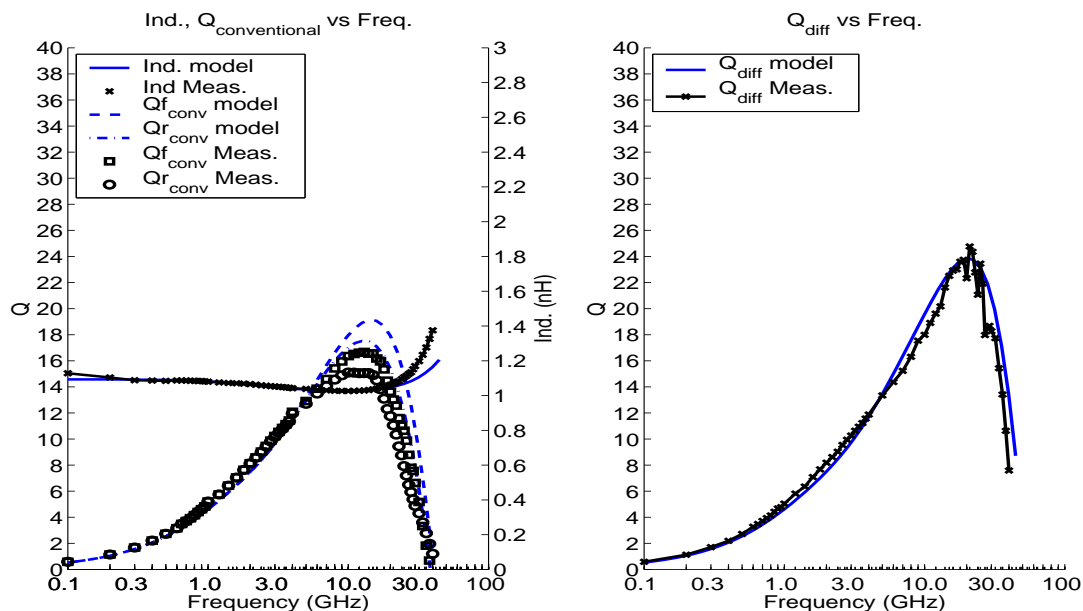


Figure 268. AM, DT, $w=5\mu\text{m}$, $s=3\mu\text{m}$, $n=3.5$, $x=100\mu\text{m}$

**BICMOS8HP, Spiral Inductor (Single Layer, M1), $w=5\mu\text{m}$, $s=3\mu\text{m}$, $n=3.5$, $x=100\mu\text{m}$
nlev=5**

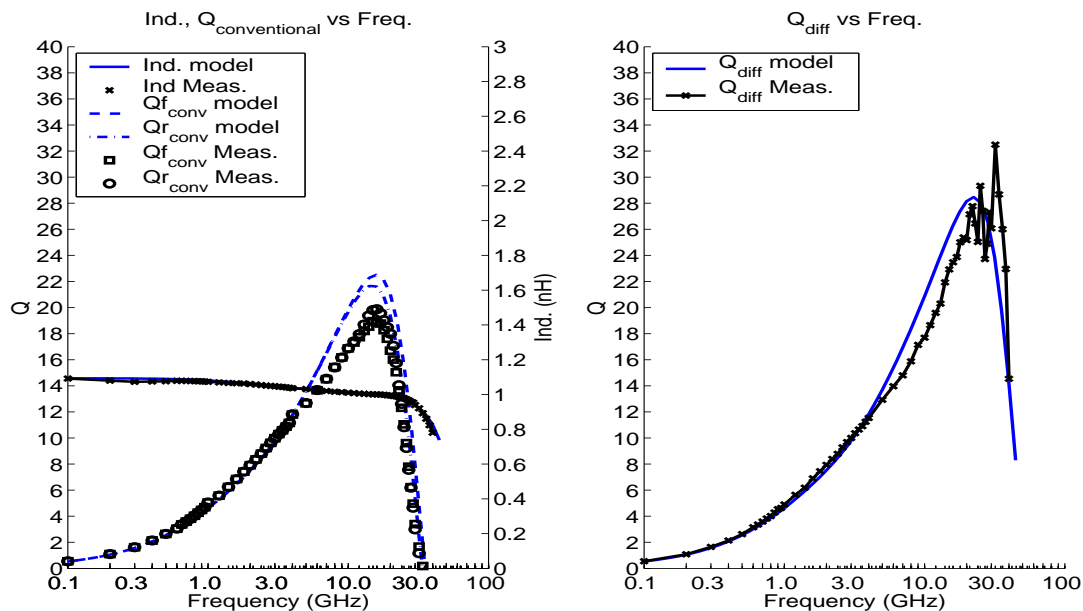


Figure 269. AM, M1, $w=5\mu\text{m}$, $s=3\mu\text{m}$, $n=3.5$, $x=100\mu\text{m}$

**BICMOS8HP, Spiral Inductor (Single Layer, DT), $w=5\mu\text{m}$, $s=5\mu\text{m}$, $n=1.5$, $x=100\mu\text{m}$
nlev=5**

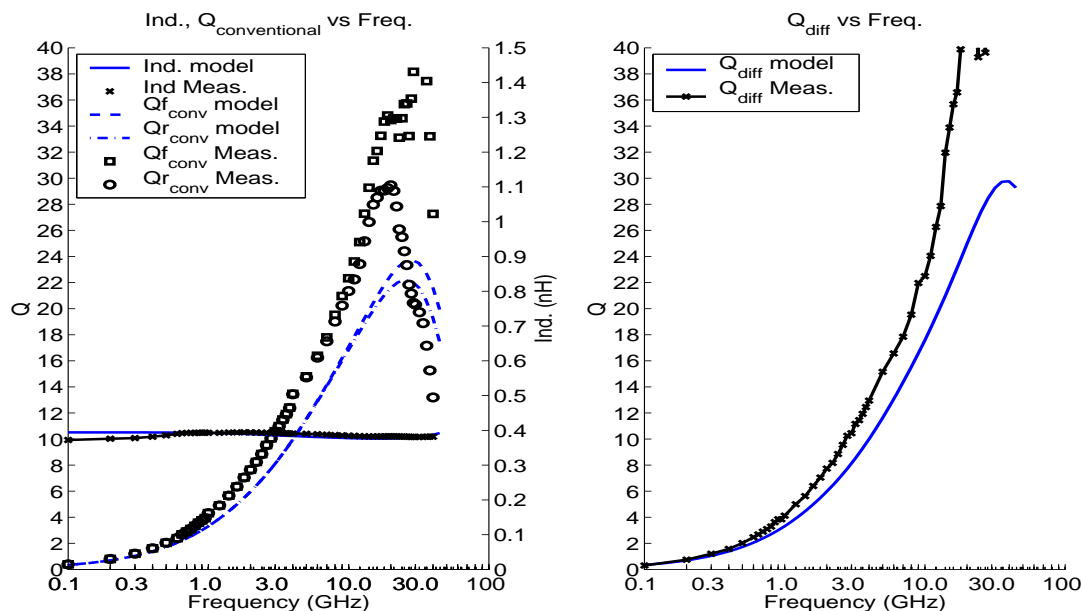


Figure 270. AM, DT, $w=5\mu\text{m}$, $s=5\mu\text{m}$, $n=1.5$, $x=100\mu\text{m}$

**BICMOS8HP, Spiral Inductor (Single Layer, M1), $w=5\mu\text{m}$, $s=5\mu\text{m}$, $n=1.5$, $x=100\mu\text{m}$
nlev=5**

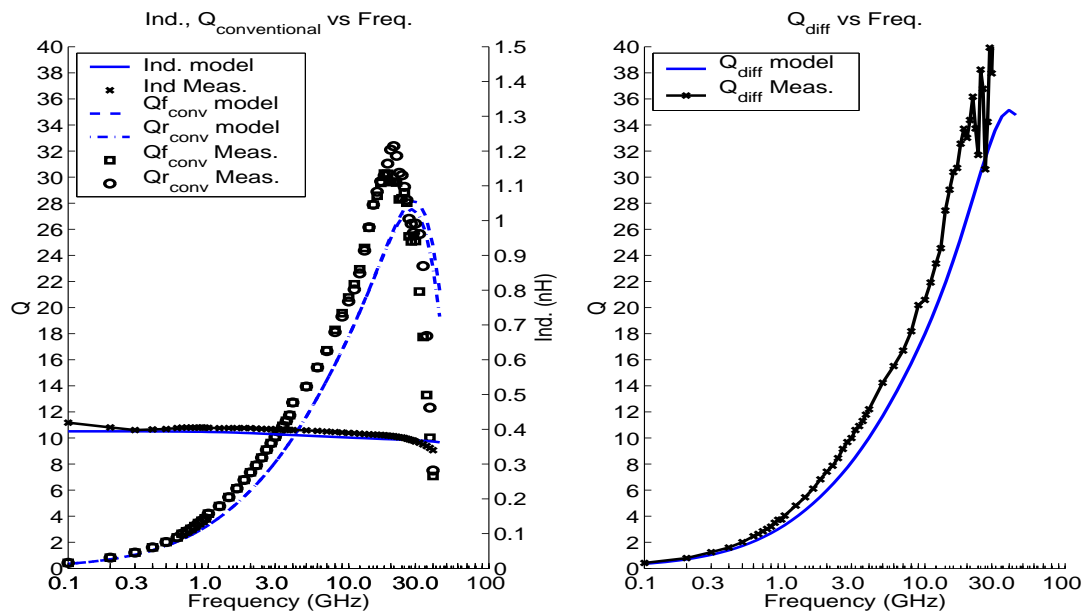


Figure 271. AM, M1, $w=5\mu\text{m}$, $s=5\mu\text{m}$, $n=1.5$, $x=100\mu\text{m}$

**BICMOS8HP, Spiral Inductor (Single Layer, DT), $w=5\mu\text{m}$, $s=5\mu\text{m}$, $n=2.5$, $x=200\mu\text{m}$
nlev=5**

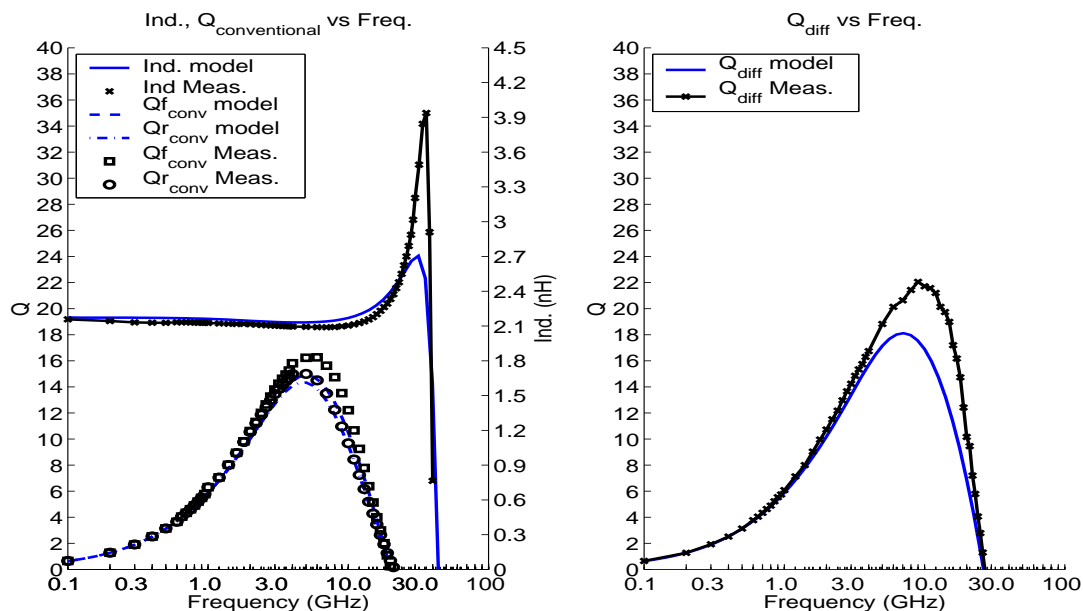


Figure 272. AM, DT, $w=5\mu\text{m}$, $s=5\mu\text{m}$, $n=2.5$, $x=200\mu\text{m}$

**BICMOS8HP, Spiral Inductor (Single Layer, M1), $w=5\mu\text{m}$, $s=5\mu\text{m}$, $n=2.5$, $x=200\mu\text{m}$
nlev=5**

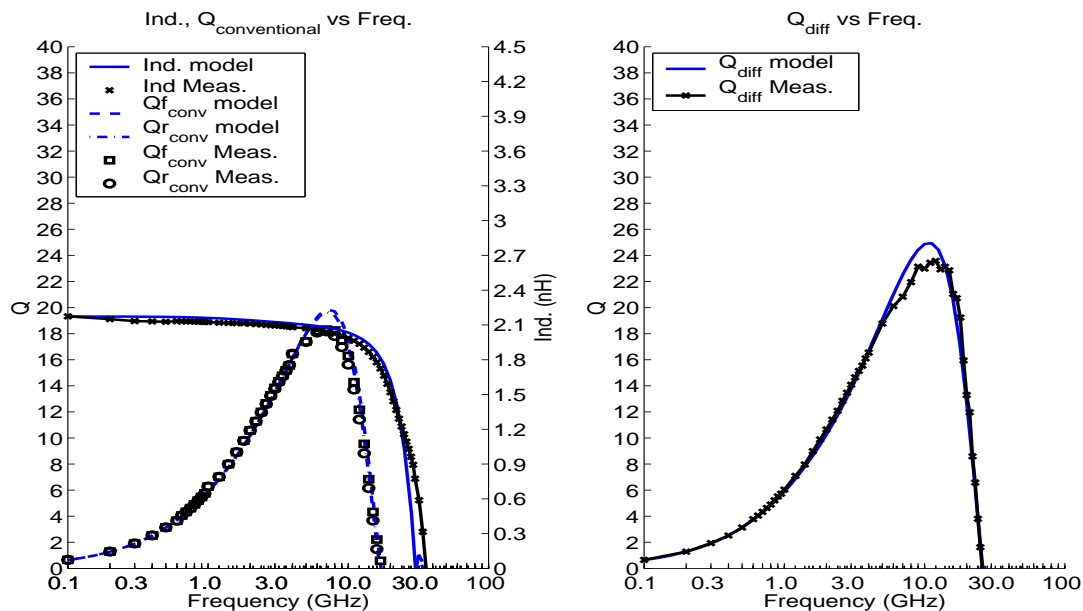


Figure 273. AM, M1, $w=5\mu\text{m}$, $s=5\mu\text{m}$, $n=2.5$, $x=200\mu\text{m}$

13.0 Symmetric Inductor Models

For information concerning the physical structure, model input parameters, and value ranges for the spiral inductor model, refer to the “Inductor Device Models” section of the BiCMOS8HP Design Manual.

13.1 Methodology for Choosing Geometric Parameters

Tables 82 and 83 show the simulated peak Q, peak Q frequency and inductance for various geometries of DT and M1 inductors and can be used in estimating the achievable values of peak Q frequency given the desired inductance. An appropriate line width can be chosen that causes the inductor to peak at the correct frequency. The BiCMOS8HP Design Kit Schematic/Layout Interface can then be used to pick an appropriate number of turns and outer dimension, at the chosen line width, that achieves the desired inductance.

Alternatively, a minimum acceptable value for peak Q can be chosen and an inductance, outer dimension, line width and number of turns picked that will yield that value of peak Q at the correct frequency. The instance properties editor of the BiCMOS8HP Design Kit Schematic/Layout Interface provides a calculation of the inductance and peak Q frequency for any particular combination of geometric parameters. This calculation is provided as an estimate for user convenience. For accurate prediction of inductance and peak Q frequency, an s-parameter simulation is recommended. Given these tables and the Design Kit interface, trade-offs can be made between inductance, inductor area, peak Q frequency and peak Q value to come to an optimized choice of inductor geometry for a specific application.

13.1.1 AM Inductor Geometric Parameters(symind)

This table shows examples using the DT groundplane:

Table 82. AM Inductor Geometry Reference Table (DT groundplane), $amrs=0.007$ ohm/sq, $nlev=5$

Ground plane	Outer diameter (x)	Number of turns (n)	Turn width (w)	Turn-turn Space (s)	Peak Q	Peak Q Frequency	Inductance
DT	100um	1.0	7um	5um	21.4	18.2GHz	0.18nH
DT	150um	3.0	7um	5um	15.1	5.6GHz	1.37nH
DT	200um	3.0	7um	5um	16.4	3.9GHz	2.25nH
DT	250um	5.0	7um	5um	12.4	2.3GHz	6.42nH
DT	200um	1.0	15um	5um	20.1	6.4GHz	0.36nH
DT	300um	1.0	15um	5um	19.3	4.3GHz	0.63nH
DT	250um	2.0	15um	5um	21.6	3.5GHz	1.31nH
DT	300um	3.0	15um	5um	18.6	2.4GHz	3.09nH
DT	300um	1.0	20um	5um	19.8	4.0GHz	0.57nH
DT	300um	2.0	20um	5um	22.4	2.8GHz	1.52nH
DT	300um	3.0	25um	5um	17.3	2.5GHz	2.07nH

This table shows examples using the M1 groundplane:

Table 83. AM Inductor Geometry Reference Table (M1 groundplane), amrs=0.007 ohm/sq, nlev=5

Ground plane	Outer diameter (x)	Number of turns (n)	Turn width (w)	Turn-turn Space (s)	Peak Q	Peak Q Frequency	Inductance
M1	100um	1.0	7um	5um	28.2	29.3GHz	0.18nH
M1	150um	3.0	7um	5um	21.2	9.1GHz	1.37nH
M1	200um	3.0	7um	5um	22.1	5.9GHz	2.25nH
M1	250um	5.0	7um	5um	15.9	3.2GHz	6.42nH
M1	200um	1.0	15um	5um	25.2	13.8GHz	0.34nH
M1	300um	1.0	15um	5um	23.0	8.1GHz	0.60nH
M1	250um	2.0	15um	5um	26.5	5.2GHz	1.31nH
M1	300um	3.0	15um	5um	23.3	3.3GHz	3.09nH
M1	300um	1.0	20um	5um	23.0	7.9GHz	0.54nH
M1	300um	2.0	20um	5um	26.8	4.1GHz	1.52nH
M1	300um	3.0	25um	5um	21.3	3.6GHz	2.07nH

13.2 Skew Parameter Adjustment

For the simulation results in the following plots, the AM metal sheet resistance(amrs) has been set to its nominal value 0.007 Ω /sq.

13.3 Temperature Simulation Notes

The variation in Q with varying temperature is caused by changes in the metal and substrate resistances. This effect is captured by the inductor models.

BICMOS8HP, Spiral Inductor (Symmetric Single, DT), $w=10\mu\text{m}$, $s=5\mu\text{m}$, $n=4$, $x=220\mu\text{m}$
 $Q_{\text{conventional}}$ vs Freq./Temperature

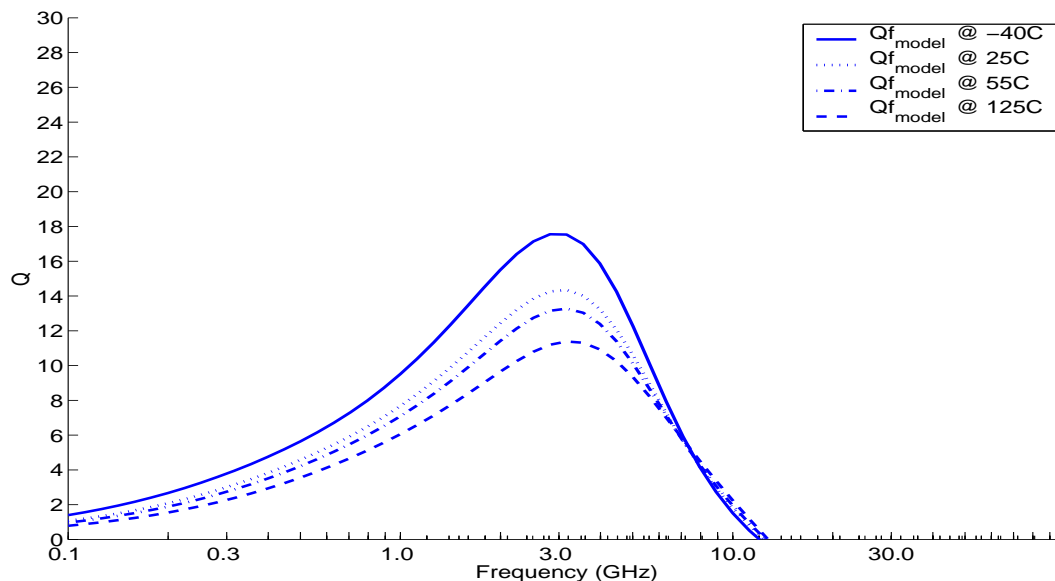


Figure 274. AM Simulated Q vs Freq with varying temp, DT inductor: $w=10\mu\text{m}$, $s=5\mu\text{m}$, $n=4$, $x=220\mu\text{m}$

BICMOS8HP, Spiral Inductor (Symmetric Single, DT), $w=15\mu\text{m}$, $s=5\mu\text{m}$, $n=2$, $x=200\mu\text{m}$
 $Q_{\text{conventional}}$ vs Freq./Temperature

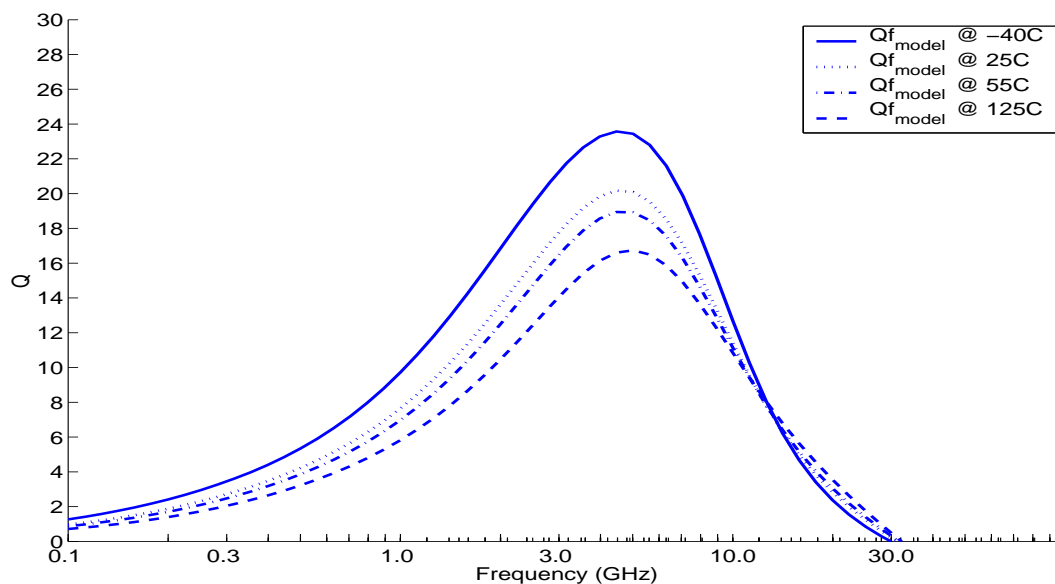


Figure 275. AM Simulated Q vs Freq with varying temp, DT inductor: $w=15\mu\text{m}$, $s=5\mu\text{m}$, $n=2$, $x=200\mu\text{m}$

BICMOS8HP, Spiral Inductor (Symmetric Single, DT), $w=15\mu\text{m}$, $s=5\mu\text{m}$, $n=3$, $x=300\mu\text{m}$
 $Q_{\text{conventional}}$ vs Freq./Temperature

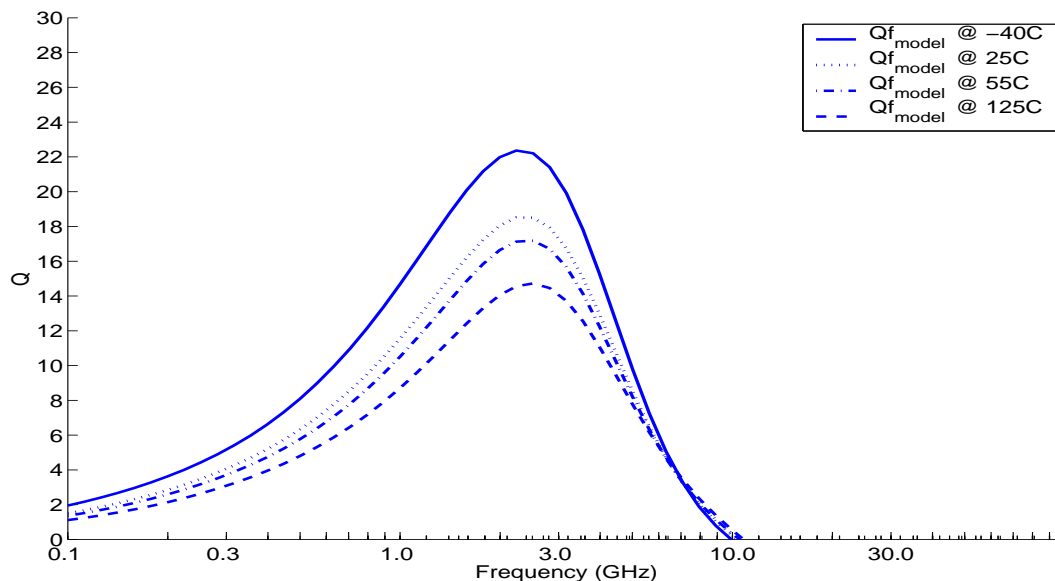


Figure 276. AM Simulated Q vs Freq with varying temp, DT inductor: $w=15\mu\text{m}$, $s=5\mu\text{m}$, $n=3$, $x=300\mu\text{m}$

13.4 Variable Metal Level Simulation Notes

The variation in Q with varying numbers of metal levels is caused by the decreasing capacitance present between the spiral and the substrate as the number of metal levels (n_{lev}) in a design grows. This decreasing capacitance causes a corresponding increase in Q , as the substrate loss is less pronounced.

Figures **277**, **278** and **279** show simulated variation of Q vs. frequency for three different AM spiral geometries.

13.4.1 AM Metal Level Variation

BICMOS8HP, Spiral Inductor (Symmetric Single, DT), $w=10\mu\text{m}$, $s=5\mu\text{m}$, $n=4$, $x=220\mu\text{m}$
 $Q_{\text{conventional}}$ vs Freq./BEOL Option

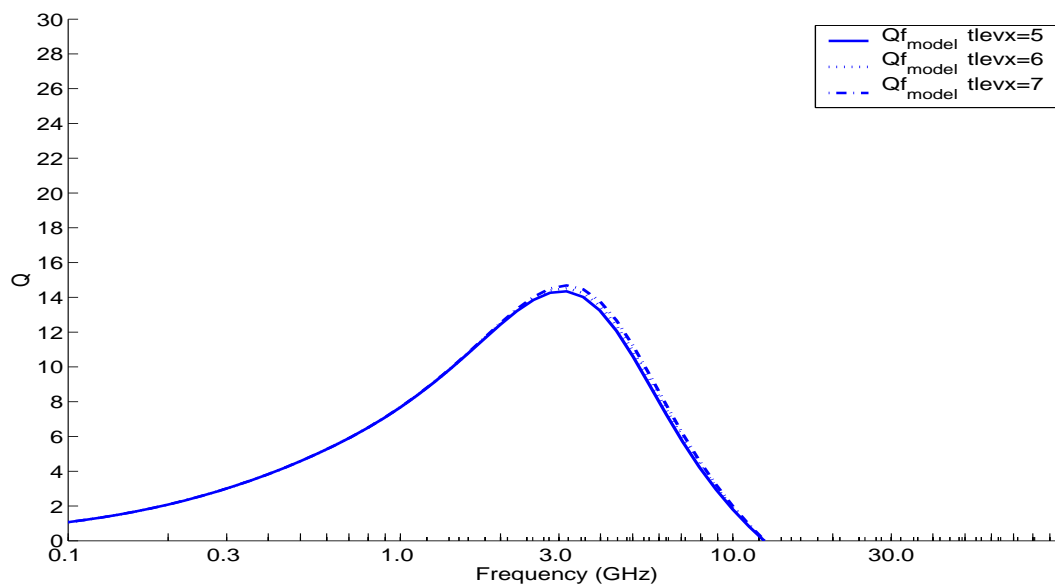


Figure 277. AM Simulated Q vs Freq w/varying # metal levels, DT inductor: $w=10\mu\text{m}$, $s=5\mu\text{m}$, $n=4$, $x=220\mu\text{m}$

BICMOS8HP, Spiral Inductor (Symmetric Single, DT), $w=15\mu\text{m}$, $s=5\mu\text{m}$, $n=2$, $x=200\mu\text{m}$
 $Q_{\text{conventional}}$ vs Freq./BEOL Option

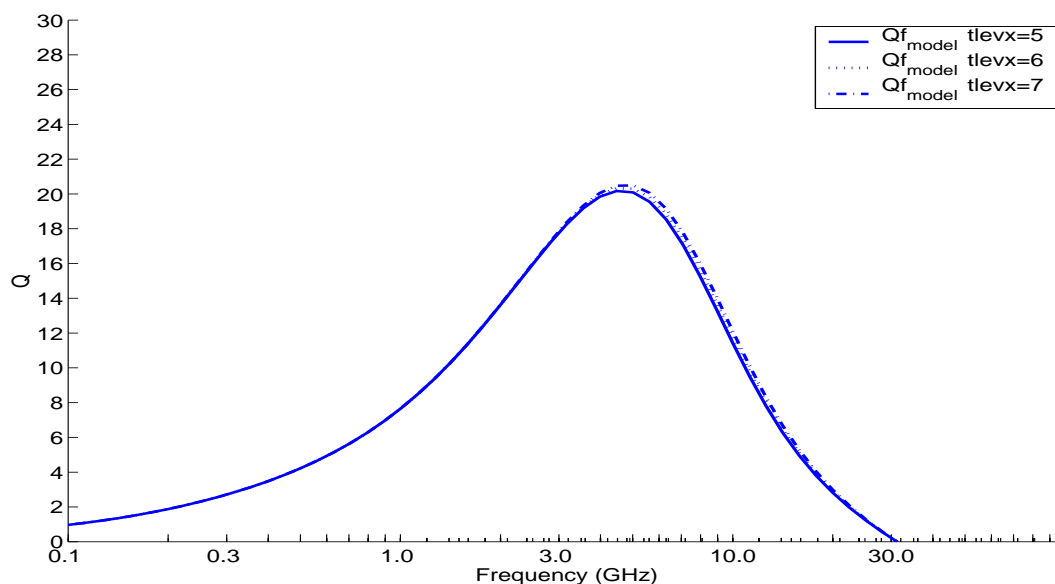


Figure 278. AM Simulated Q vs Freq w/varying # metal levels, DT inductor: $w=15\mu\text{m}$, $s=5\mu\text{m}$, $n=2$, $x=200\mu\text{m}$

BICMOS8HP, Spiral Inductor (Symmetric Single, DT), $w=15\mu\text{m}$, $s=5\mu\text{m}$, $n=3$, $x=300\mu\text{m}$
 $Q_{\text{conventional}}$ vs Freq./BEOL Option

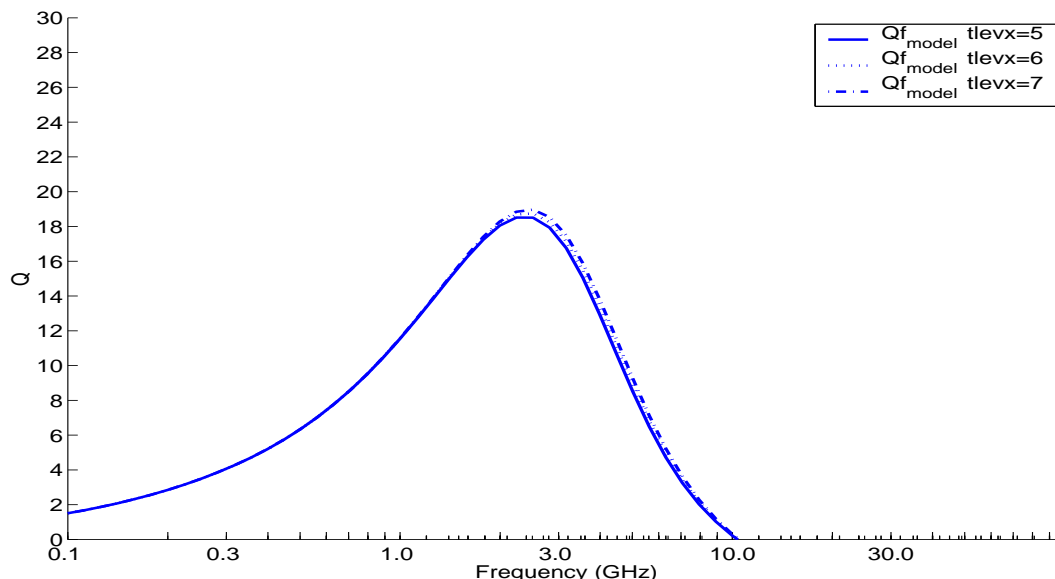


Figure 279. AM Simulated Q vs Freq w/varying # metal levels, DT inductor: $w=15\mu\text{m}$, $s=5\mu\text{m}$, $n=3$, $x=300\mu\text{m}$

13.5 DT Groundplane Model Optimization Notes

The model was optimized to provide a good fit to the Q and inductance values extracted from measurements. Q was calculated using both the “conventional” and “circuit” definitions (see “**Inductor Q Definition**” on page 336.). Both definitions assume that the underpass, connected to the inner turn of the spiral, is shorted to ground. This assumption yields the worst case value for Q, since Q varies directly with the inductor’s port 2 load impedance. Lower values of port 2 load impedance allow a higher current to flow in the inductor causing a higher power loss in the series resistance.

The inductance was extracted from the measured Y-Parameters using:

$$\text{Inductance} = \frac{Y_{21} \text{imag}}{\omega \cdot [(Y_{21} \text{real})^2 + (Y_{21} \text{imag})^2]} \quad (\text{H})$$

The model was adjusted to yield the best Q fit, for both “conventional” and “circuit” Q definitions, at the peak Q frequency and for as wide a range as possible around the peak Q frequency.

13.6 M1 Groundplane Model Optimization Notes

BiCMOS8HP hardware with M1 groundplanes under symmetric spirals was unavailable for model vs hardware correlations. As soon as hardware is available with the 8HP M1 groundplane, the model will be validated against those measurements.

13.7 M1 Groundplane Model vs. Hardware Relative Errors

Based on the performance of the model(as seen in other technologies) the following statements can be made: Over the range of available inductor geometries, simulation provides a peak Q value deviation from measured data of about +/-20% for M1 inductors.

13.8 DT Groundplane Model vs. Hardware Relative Errors

Based on the performance of the model in BiCMOS8HP the following statements can be made: Over a range of inductor geometries, simulation provides a peak Q value deviation from measured data of less than +/-15% for DT inductors.

13.9 Model Correlation Plots

Correlation plots in this section show measured and simulated inductor Q and inductance with respect to frequency for a variety of inductor geometries. The plots show both the conventional Q and the differential Q as defined in **section 12.2** , “Inductor Q Definition” on page 336.

Examples are included for AM symmetric inductors(symind) for two different ground planes (DT and M1).

13.9.1 AM (“symind” model) Correlation Plots

**BICMOS8HP, Spiral Inductor (Symmetric Single, DT), $w=10\mu\text{m}$, $s=4\mu\text{m}$, $n=1$, $x=300\mu\text{m}$
nlev=5**

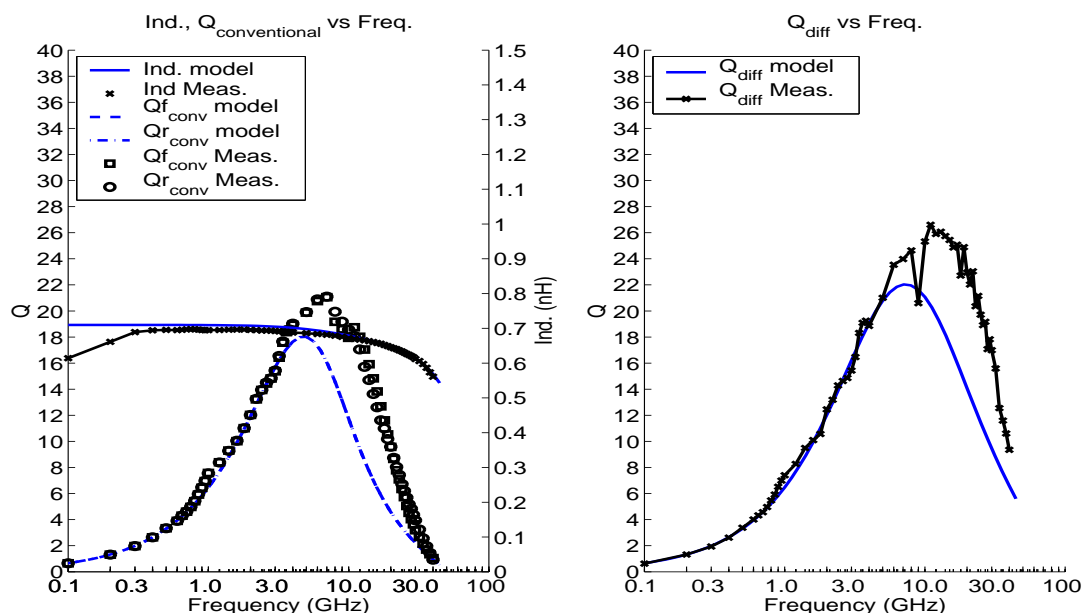


Figure 280. AM, DT, $w=10\mu\text{m}$, $s=4\mu\text{m}$, $n=1$, $x=300\mu\text{m}$

**BICMOS8HP, Spiral Inductor (Symmetric Single, DT), $w=13\mu\text{m}$, $s=4\mu\text{m}$, $n=4$, $x=200\mu\text{m}$
 $n\text{lev}=5$**

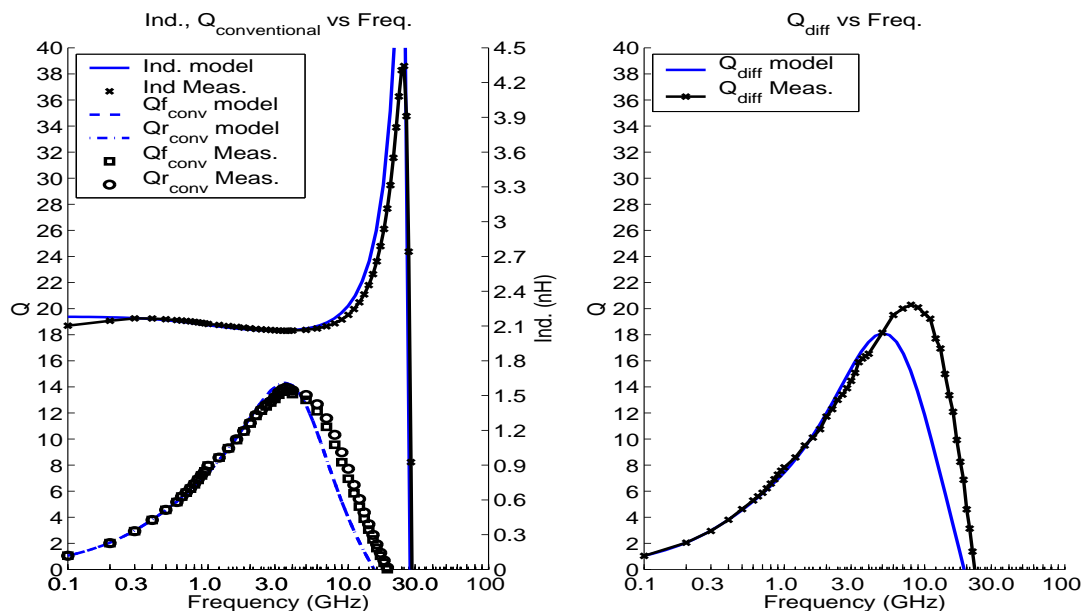


Figure 281. AM, DT, $w=13\mu\text{m}$, $s=4\mu\text{m}$, $n=4$, $x=200\mu\text{m}$

**BICMOS8HP, Spiral Inductor (Symmetric Single, DT), $w=15\mu\text{m}$, $s=3\mu\text{m}$, $n=2$, $x=150\mu\text{m}$
 $n\text{lev}=5$**

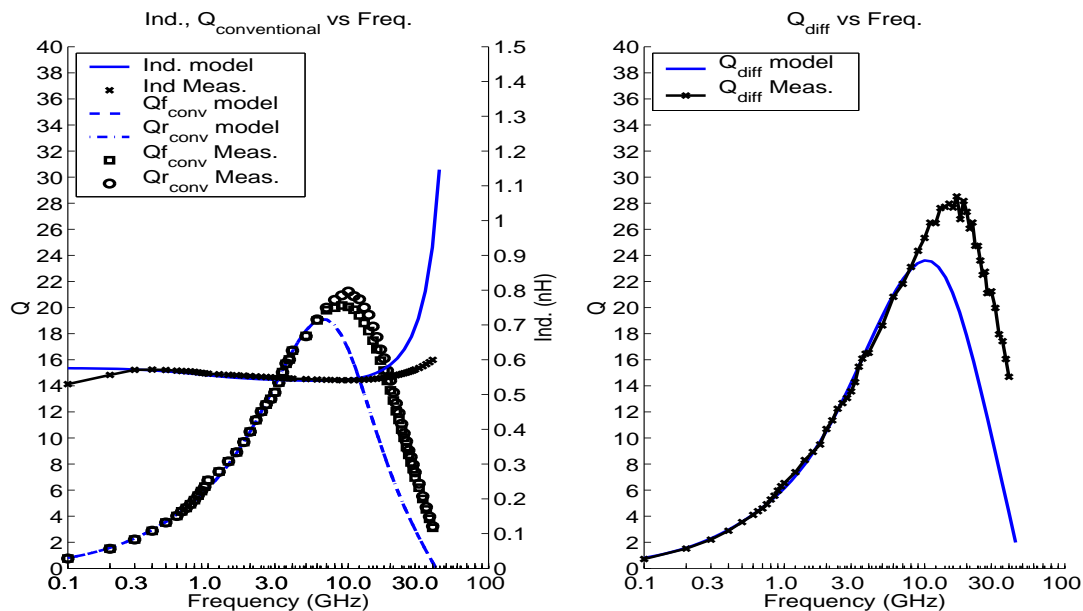


Figure 282. AM, DT, $w=15\mu\text{m}$, $s=3\mu\text{m}$, $n=2$, $x=150\mu\text{m}$

**BICMOS8HP, Spiral Inductor (Symmetric Single, DT), $w=15\mu\text{m}$, $s=4\mu\text{m}$, $n=5$, $x=300\mu\text{m}$
nlev=5**

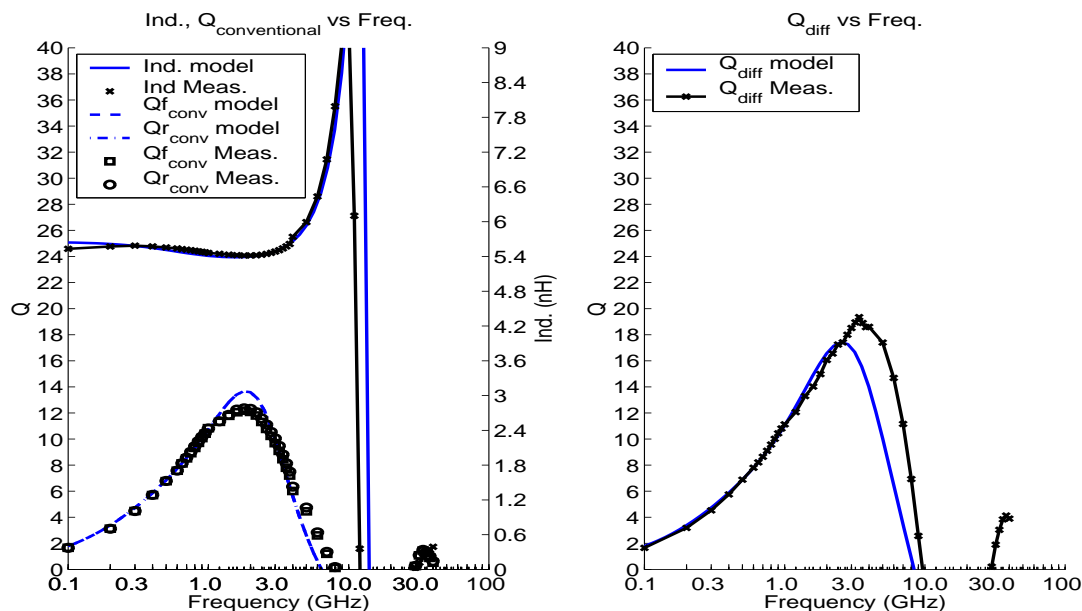


Figure 283. AM, DT, $w=15\mu\text{m}$, $s=4\mu\text{m}$, $n=5$, $x=300\mu\text{m}$

**BICMOS8HP, Spiral Inductor (Symmetric Single, DT), $w=20\mu\text{m}$, $s=4\mu\text{m}$, $n=2$, $x=200\mu\text{m}$
nlev=5**

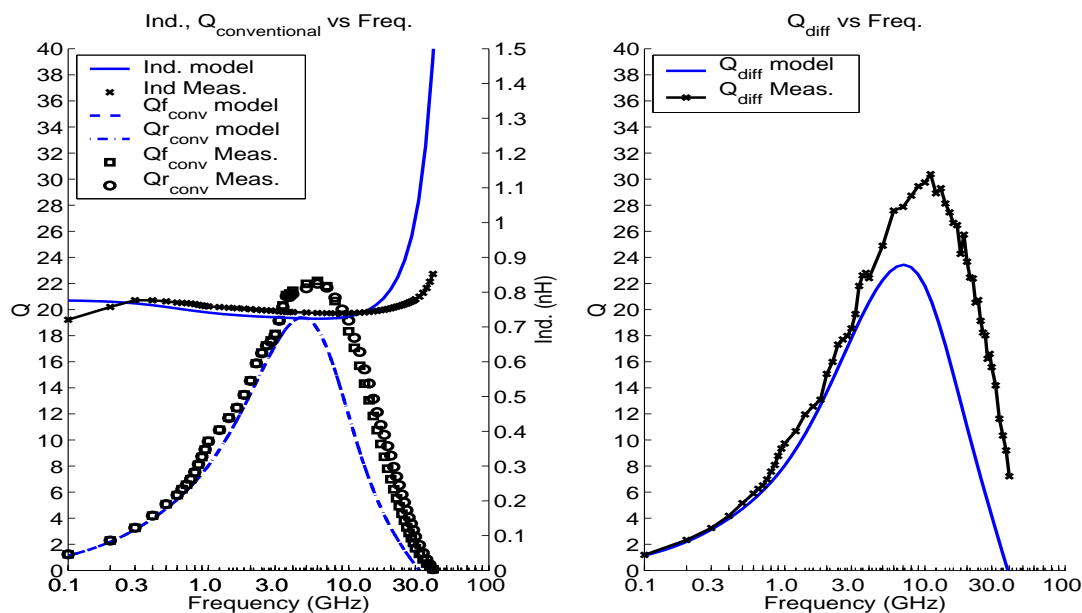


Figure 284. AM, DT, $w=20\mu\text{m}$, $s=4\mu\text{m}$, $n=2$, $x=200\mu\text{m}$

**BICMOS8HP, Spiral Inductor (Symmetric Single, DT), $w=6.48\mu\text{m}$, $s=3\mu\text{m}$, $n=1$, $x=102\mu\text{m}$
 $n\text{lev}=5$**

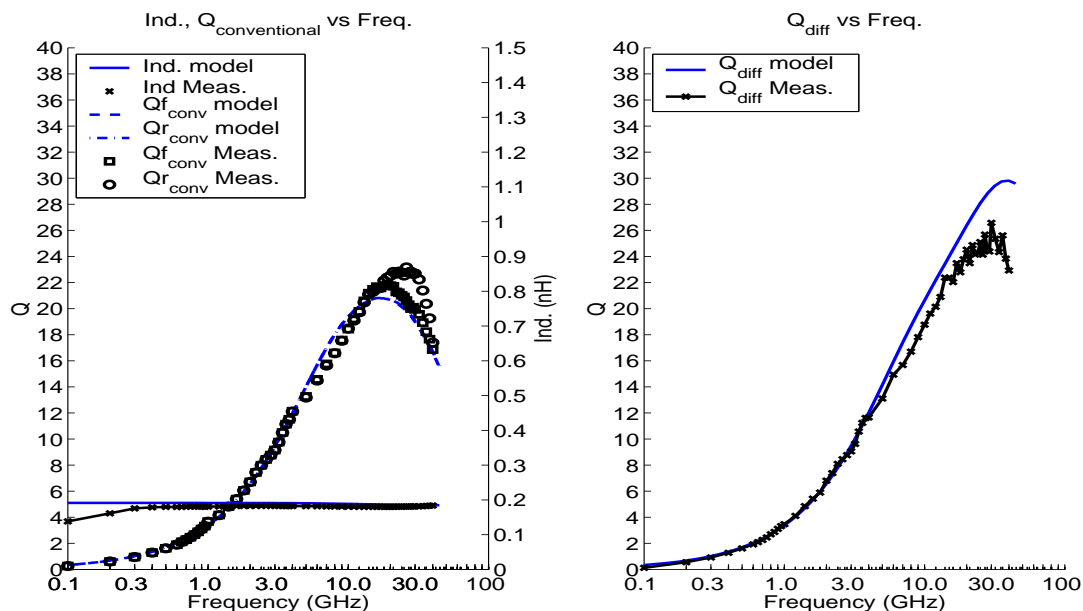


Figure 285. AM, DT, $w=6.48\mu\text{m}$, $s=3\mu\text{m}$, $n=1$, $x=102\mu\text{m}$

**BICMOS8HP, Spiral Inductor (Symmetric Single, DT), $w=6.48\mu\text{m}$, $s=4\mu\text{m}$, $n=12$, $x=300\mu\text{m}$
 $n\text{lev}=5$**

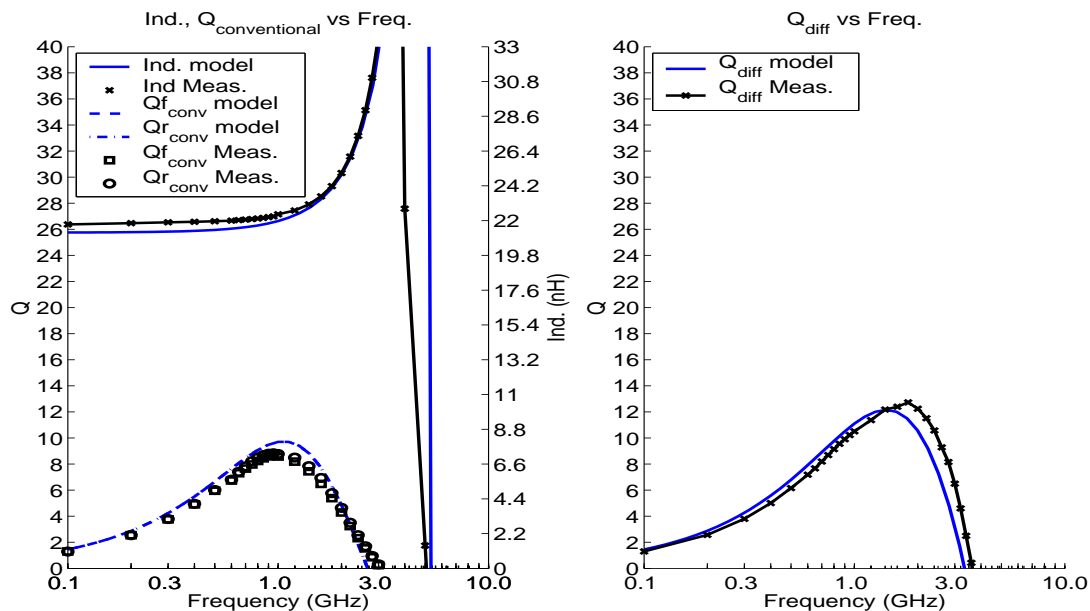


Figure 286. AM, DT, $w=6.48\mu\text{m}$, $s=4\mu\text{m}$, $n=12$, $x=300\mu\text{m}$

**BiCMOS8HP, Spiral Inductor (Symmetric Single, DT), $w=6.48\mu\text{m}$, $s=4\mu\text{m}$, $n=7$, $x=200\mu\text{m}$
nlev=5**

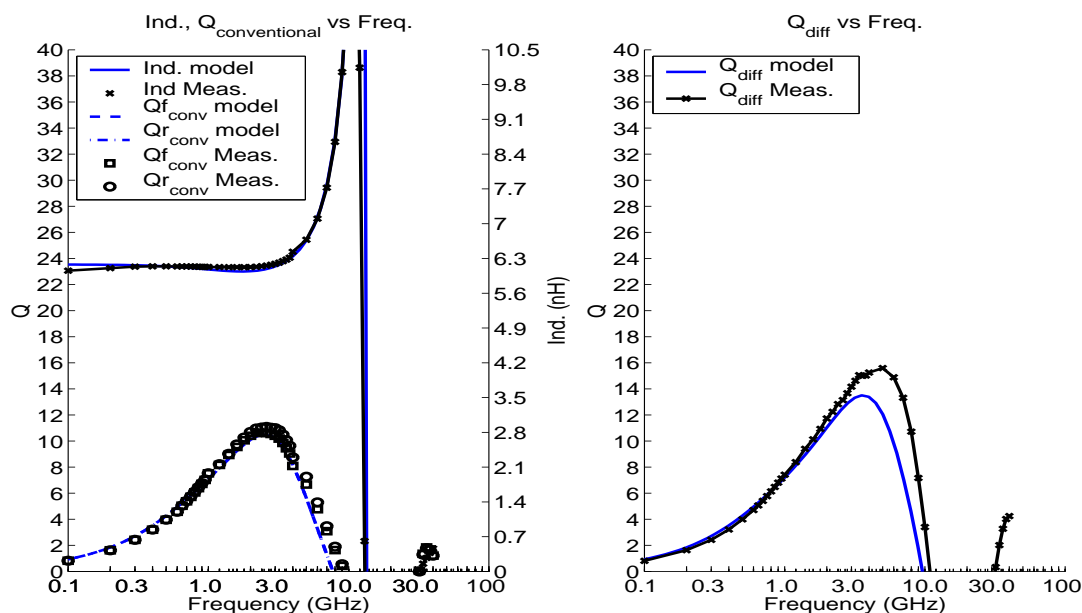


Figure 287. AM, DT, $w=6.48\mu\text{m}$, $s=4\mu\text{m}$, $n=7$, $x=200\mu\text{m}$

**BiCMOS8HP, Spiral Inductor (Symmetric Single, M1), $w=10\mu\text{m}$, $s=4\mu\text{m}$, $n=5$, $x=200\mu\text{m}$
nlev=5**

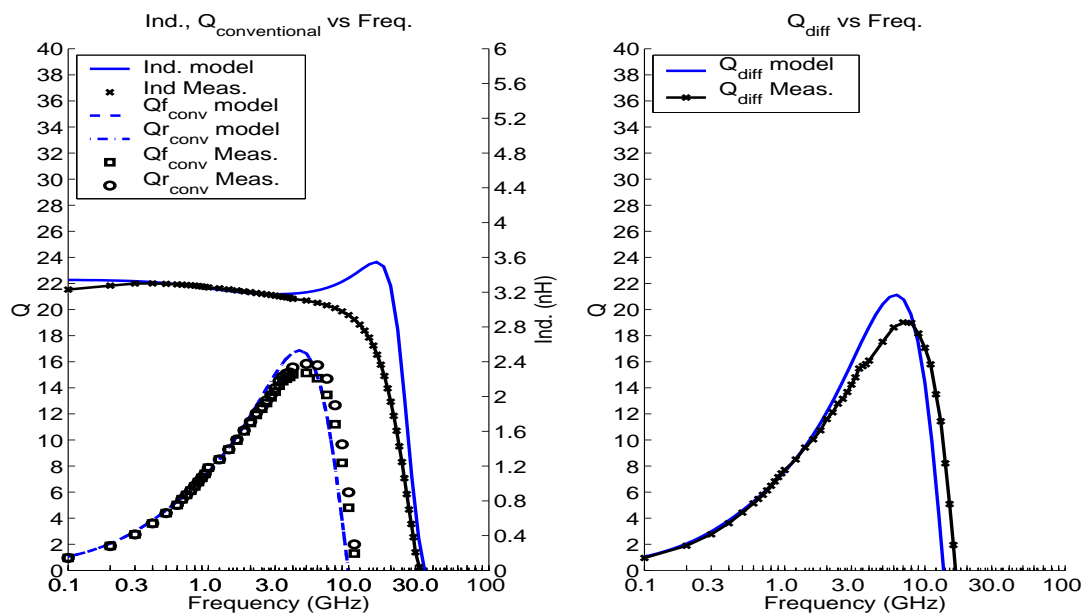


Figure 288. AM, M1, $w=10\mu\text{m}$, $s=4\mu\text{m}$, $n=5$, $x=200\mu\text{m}$

**BICMOS8HP, Spiral Inductor (Symmetric Single, M1), $w=15\mu m$, $s=4\mu m$, $n=3$, $x=200\mu m$
nlev=5**

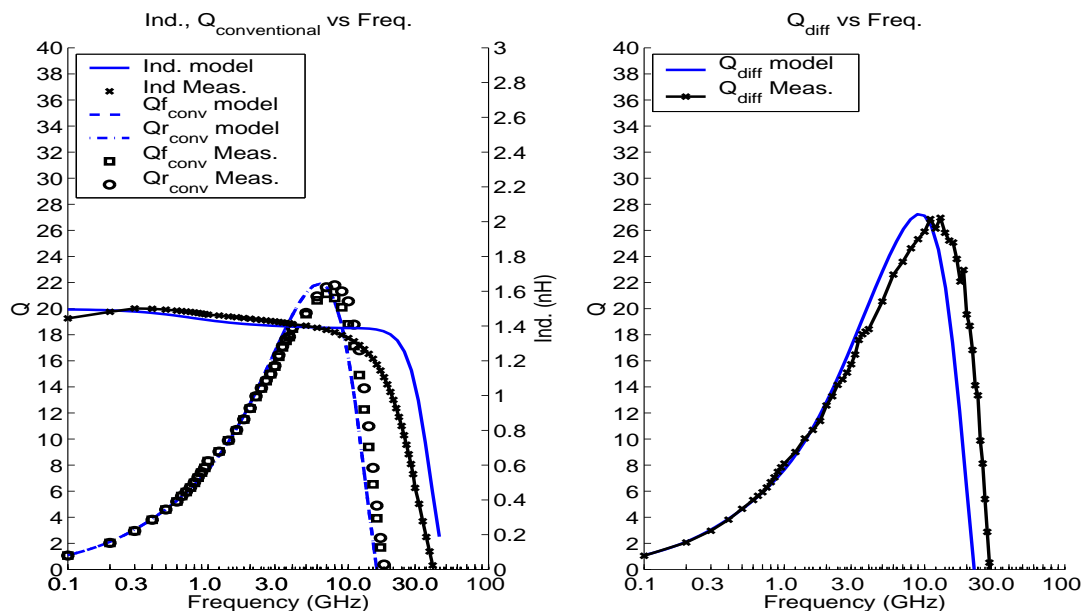


Figure 289. AM, M1, $w=15\mu m$, $s=4\mu m$, $n=3$, $x=200\mu m$

**BICMOS8HP, Spiral Inductor (Symmetric Single, M1), $w=25\mu m$, $s=4\mu m$, $n=3$, $x=300\mu m$
nlev=5**

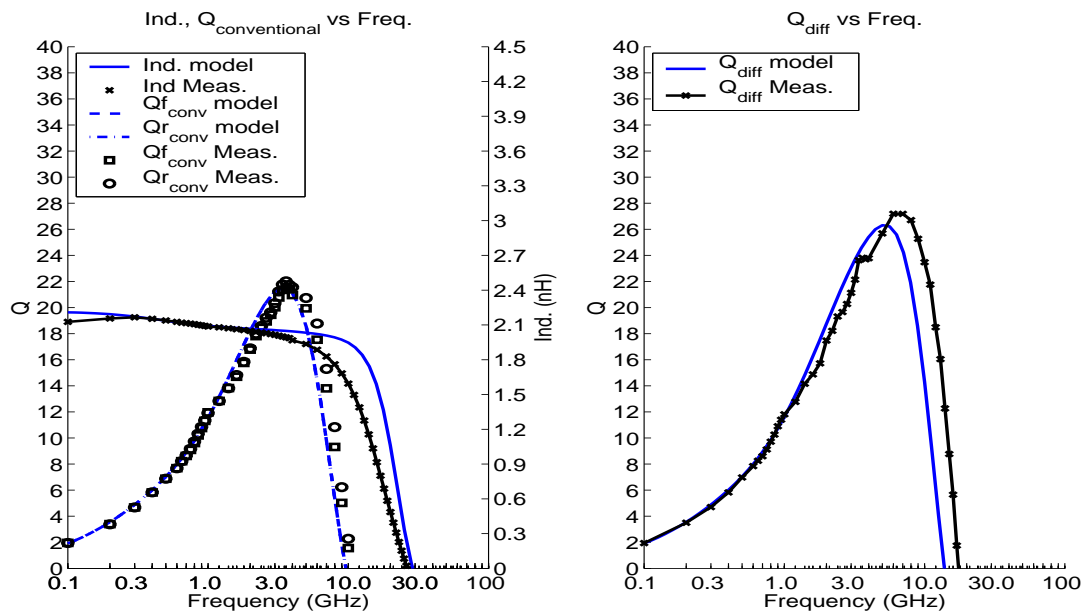


Figure 290. AM, M1, $w=25\mu m$, $s=4\mu m$, $n=3$, $x=300\mu m$

**BiCMOS8HP, Spiral Inductor (Symmetric Single, M1), $w=6.48\mu\text{m}$, $s=3\mu\text{m}$, $n=3$, $x=102\mu\text{m}$
nlev=5**

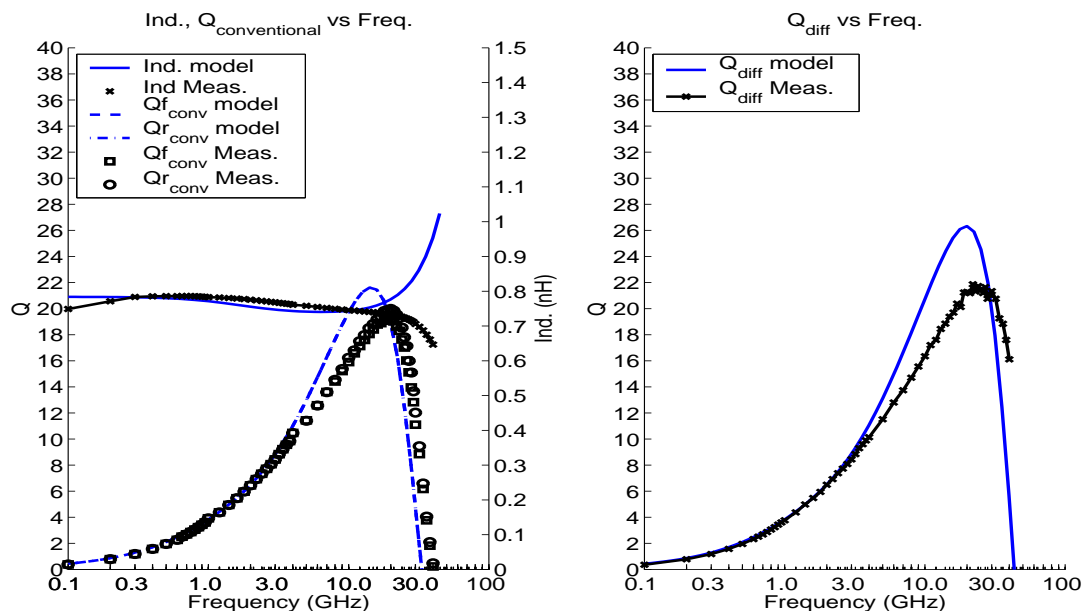


Figure 291. AM, M1, $w=6.48\mu\text{m}$, $s=3\mu\text{m}$, $n=3$, $x=102\mu\text{m}$

**BiCMOS8HP, Spiral Inductor (Symmetric Single, M1), $w=6.9\mu\text{m}$, $s=3\mu\text{m}$, $n=1$, $x=150\mu\text{m}$
nlev=5**

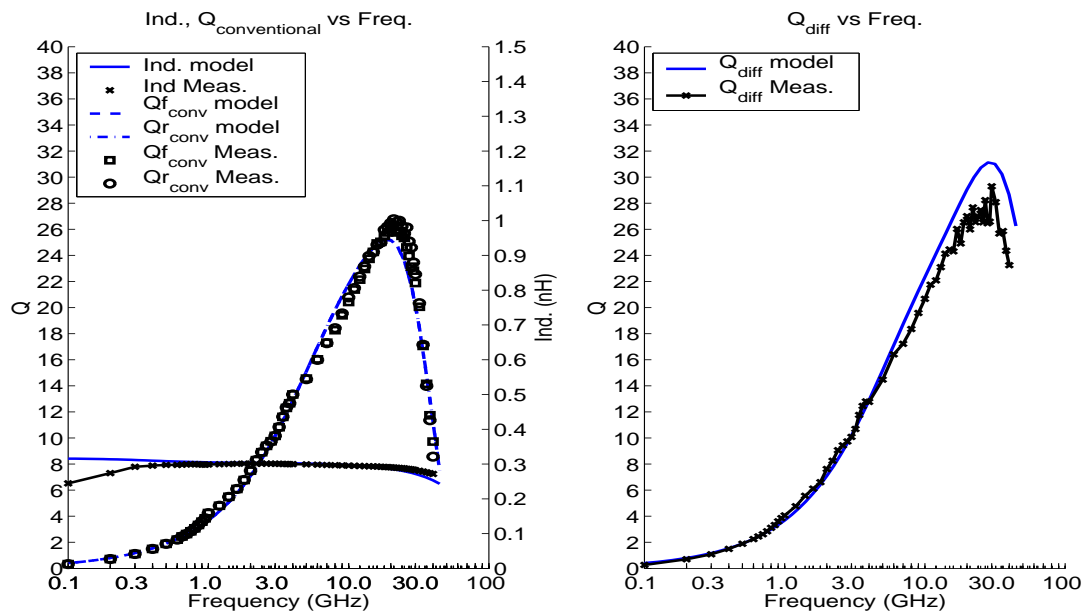


Figure 292. AM, M1, $w=6.9\mu\text{m}$, $s=3\mu\text{m}$, $n=1$, $x=150\mu\text{m}$

14.0 Rflin Models

For information concerning the physical structure, model input parameters, and value ranges for the rflin model, refer to the “Rflin Device Models” section of the BiCMOS-8HP Design Manual.

14.1 Rflin Simulation

The model takes the length and width of the line as inputs. Based on these inputs, the various model parameters (capacitance, inductance, resistance) are calculated.

14.2 Subsectioning Long Lines to Improve Accuracy

As the length of an rflin element grows beyond about 1000 μ m, simulation accuracy can be improved by placing two or more shorter rflin elements in series. The methodology for doing this is described below:

1. Calculate the overall length of the desired line and then divide that number by the desired number of subsections. This yields the length for each subsection.
2. Calculate the effective self inductance of a line of the desired overall length. This is done by creating an rflin instance using the BiCMOS-8HP Design Kit Schematic/Layout Interface using the appropriate width and length. The self inductance is calculated and appears in the field labelled “Self Inductance”. Note this value.
3. Divide the inductance value calculated in step 2 by the desired number of subsections. This will be the inductance number that is input when creating the subsection instances.
4. Create the desired number of rflin elements (subsections of the desired overall line length), entering the “Self Inductance” number calculated in step 3 along with the width and length.
5. Connect these subsections in series to yield a single long transmission line.

These steps are required because the self inductance of a straight piece of interconnect is not a linear function of its length.

14.3 Frequency Dependent Loss Model

The metal of a straight line inductor experiences skin effect losses at high frequencies. The ac current in a metal conductor will flow increasingly on the surface as frequency increases. This causes the conductor's effective resistance and inductance to undergo change over frequency. At high frequencies, the resistance of a conductor increases as a function of the square root of frequency and the inductance decreases slightly and then levels off.

One means of accounting for this frequency dependent loss mechanism in the model is to use frequency dependent lumped elements (the resistor increasing with frequency and the inductance decreasing). This approach has a large disadvantage due to the fact that general circuit simulators (e.g. spectre, spice,...) can only calculate the frequency dependent element's value at one frequency point per simulation. This means that a frequency at which to calculate the element values is specified at simulation run-time and that value will be used for the entire simulation, even if a broadband, multi-frequency, or transient simulation is done.

An improved method of implementing this frequency dependent behavior in an inductor model is to use an R-L ladder network to replace the series loss elements in the model. An appropriate selection of element values can achieve the desired frequency dependent behavior while maintaining the ability to simulate at all frequencies under all simulation conditions (without needing to specify a frequency at which to calculate the loss). This is the technique that has been implemented in the rfline model.

14.4 Q Definition

The quality factor (Q) definition for the rfline is identical to that described previously in **Section 12.2** , “**Inductor Q Definition**” on page 336.

14.5 Rfline Grounding Concerns During Simulation

The rfline model ground terminal is intended to be connected directly to an AC ground (DC bias) when included in a circuit simulation. If a series resistance is inserted between the rfline ground terminal and AC ground in order to model the proximity of substrate contacts, the simulation will be incorrect. The ground terminal of the rfline model is connected to the global node "gnd!" by default at instance creation in the BiCMOS8HP Design Kit. This is intended to be a perfect AC ground (no series impedance). The actual DC bias level on this terminal is not important (for rfline simulation), as there are no diode junctions connected internally to the rfline model ground terminal.

Under no circumstances should the ground terminal of the rfline be connected to the global substrate node "sub!". The current return path from the "sub!" node is through the substrate contact model (subc). This inserts a series resistance between "sub!" and the DC bias connected to the substrate contact (usually gnd! node). This series resistance will tend to decouple the substrate losses of the rfline, decreasing the simulated loss in a non-physical manner.

Simulating the rfline from a post layout extracted view in Cadence presents a specific difficulty in recognizing the proper connection of the ground node for the rfline. Since there is no physical third terminal related to the rfline, no connection between the ground node and the desired AC ground node (e.g. gnd!) will be extracted. This means that the third node of the rfline will be extracted as a floating node unless the appropriate layout steps are taken. The “BB Connection for Inductor and Rfline” section of the BiCMOS8HP Process Design Kit User’s Guide document details the additional pseudo-connection (BB IND) required to be made between the rfline and the actual AC ground node in order to extract the proper ground node for the rfline. With this connection in place between the rfline and any M1 metallization that is connected to a substrate contact, the third terminal of the rfline will extract as being connected to the node associated with the M1 metallization on the substrate contact (AC ground).

It is important to note that the M1 connection between the "BB IND" shape and the actual DC bias for that net, should be a wide, low resistance (low impedance) connection. If too much series resistance is extracted between the intersection of M1 and the "BB IND" and the DC bias, the substrate loss will tend to be decoupled, causing an overoptimistic simulation of the rfline. The series resistance should be kept below 5Ω in all cases.

14.6 Rfline Grounding Concerns for Physical Layout

The rflines were measured and modelled with substrate contacts approximately 80μm away from the line. It has been determined that the placement of substrate contacts in the vicinity of the rfline has essentially no effect on the characteristics, as long as the substrate contacts are kept at least 50μm away. If substrate contacts are placed closer than 50μm, there may be an increase in the actual loss.

14.7 Temperature Simulation Notes

The variation in Q with changing temperature depends upon two key factors:

1. Rflin Metal TCR (temperature coefficient of resistance)
2. Substrate Resistance TCR

The inductor metallization, which is in series with the inductance, has a positive TCR, which increases resistance and thus power loss in the inductor as the temperature increases. This serves to decrease the Q. The substrate resistance, which is in parallel with the inductor, also has a positive temperature coefficient. This decreases the power loss in the substrate as the temperature is increased (the current is shunted away from the substrate and into the inductor with increasing substrate resistance), serving to increase Q. The variation of the inductor resistance has an effect on the low frequency (below peak Q) portion of the Q vs. frequency curve, while the substrate resistance variation has an effect on the high frequency (at peak Q and beyond) portion of the curve. Figures 293, 294 and 295 show the simulated variation of Q vs. frequency for three different rflin geometries as temperature is varied.

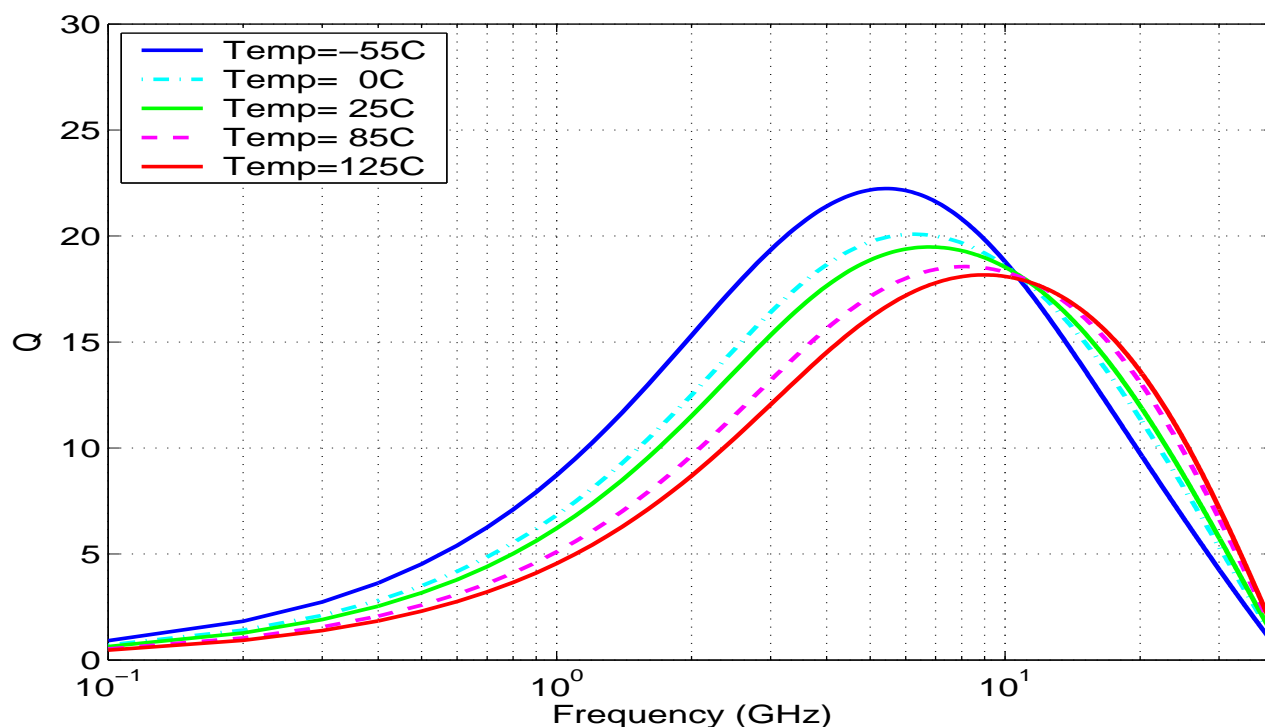


Figure 293. Simulated Q vs. Freq vs. Temp, rflin: w=5 μ m, l=750 μ m

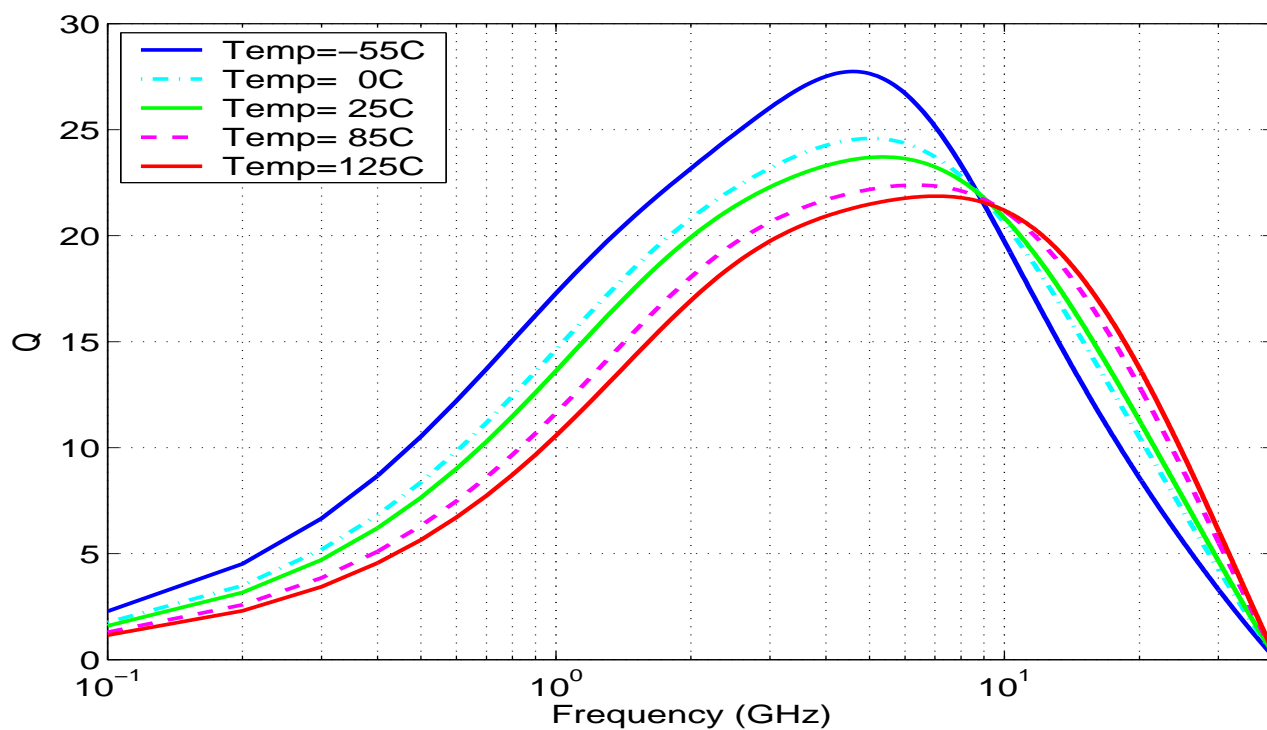


Figure 294. Simulated Q vs. Freq vs. Temp, rflin: $w=15\mu\text{m}$, $l=750\mu\text{m}$

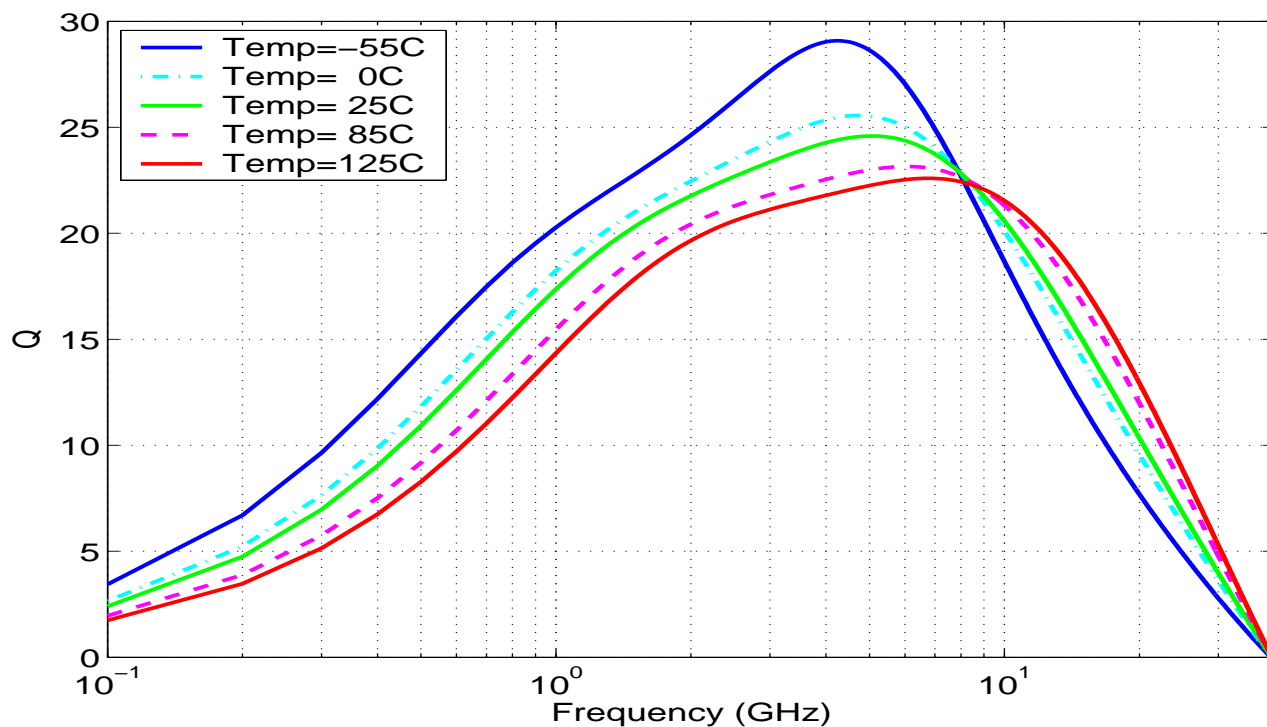


Figure 295. Simulated Q vs. Freq vs. Temp, rflin: $w=25\mu\text{m}$, $l=750\mu\text{m}$

14.8 Variable Geometry Simulation Notes

This section documents the changes of Q, S-parameters, characteristic impedance, attenuation and phase constants and inductance as a function of rflin geometry (length and width). Each plot in Figure 61- 69 shows five traces corresponding to the simulated results for rflines with the following widths: $4\mu\text{m}$, $10\mu\text{m}$, $15\mu\text{m}$, $20\mu\text{m}$, $25\mu\text{m}$. This width range spans the design space of the rflin. Figures 61, 62, and 63 show the simulated s-parameter characteristics for rflines with the five widths mentioned above for rflin lines with lengths of $200\mu\text{m}$, $400\mu\text{m}$, $600\mu\text{m}$. Figures 64, 65, and 66 show the simulated characteristic impedances and phases, and attenuation and phase constants for rflines with the same widths for rflin lines with lengths of $200\mu\text{m}$, $400\mu\text{m}$, $600\mu\text{m}$. Finally, Figures 67, 68, and 69 show the simulated Q and inductance values for the same rflin widths rflin lines with lengths of $200\mu\text{m}$, $400\mu\text{m}$, $600\mu\text{m}$. All of the rflines are in the AM metal layer of a DT lattice.

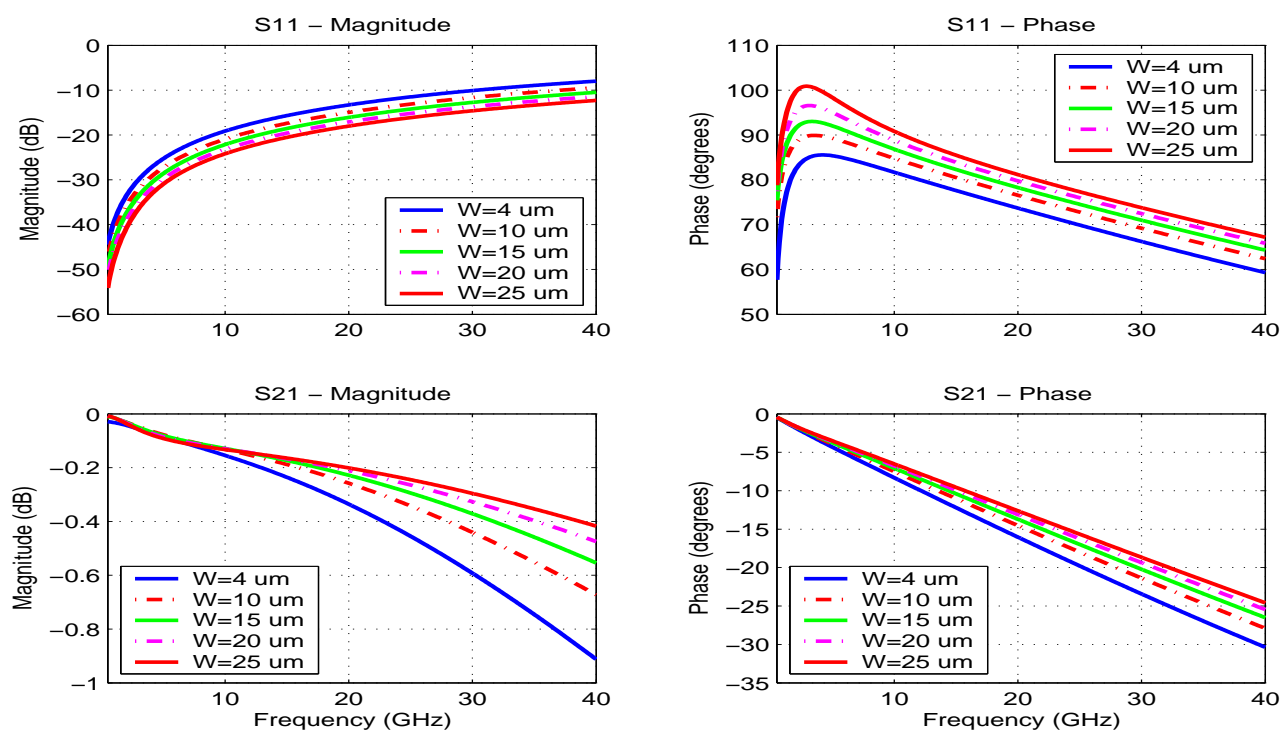


Figure 296. Simulated S-parameters vs. Freq vs. width rflin: $l=200\mu\text{m}$ (25C)

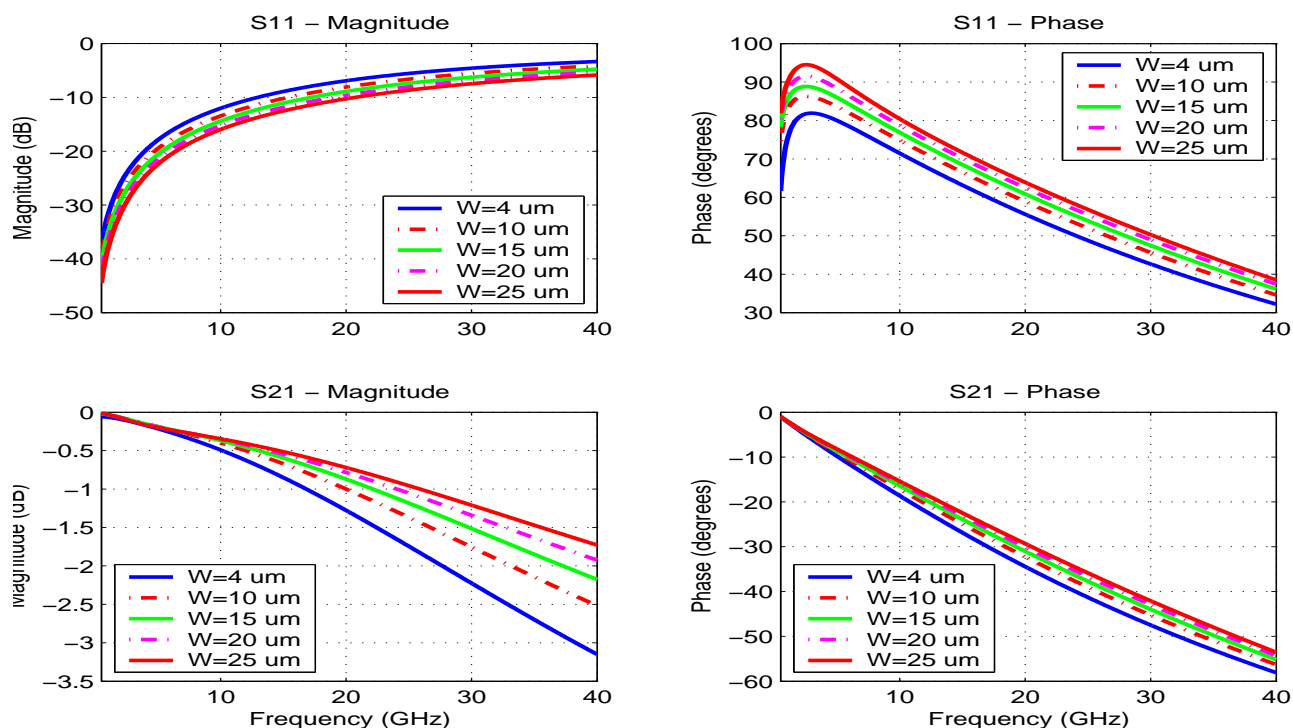


Figure 297. Simulated S-parameters vs. Freq vs. width rfline: $l=400\mu\text{m}$ (25C)

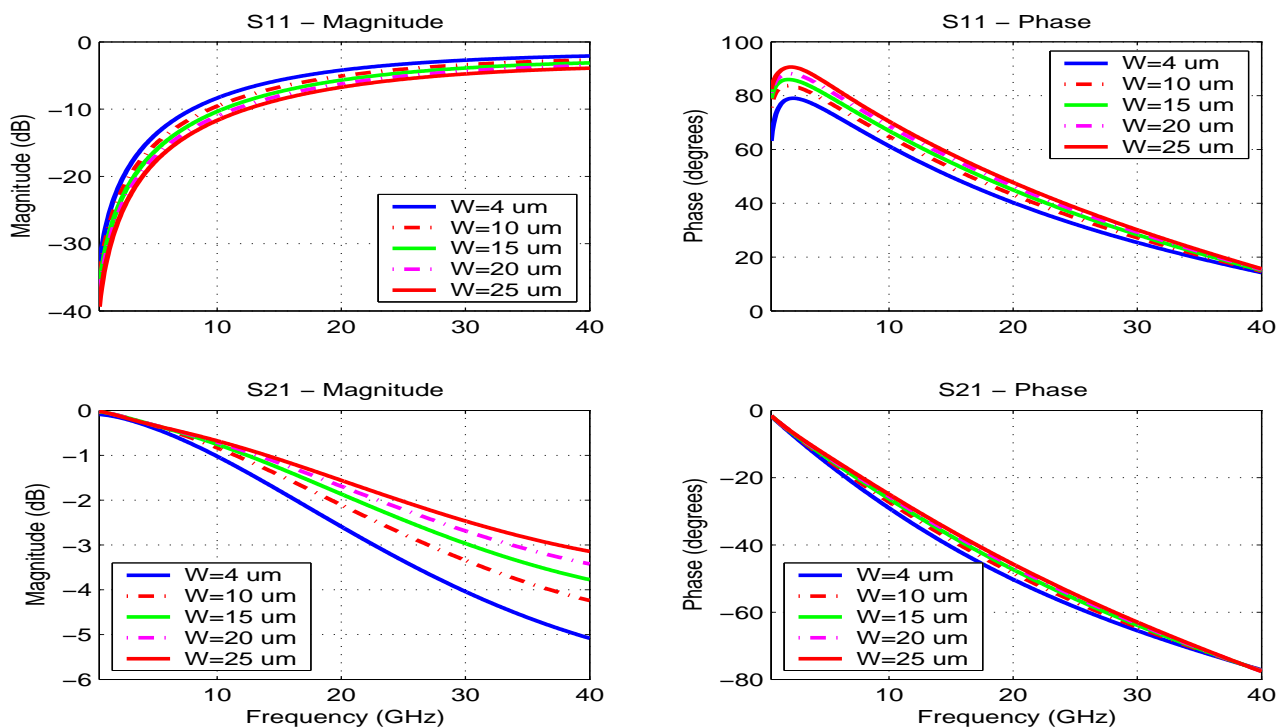


Figure 298. Simulated S-parameters vs. Freq vs. width rfline: $l=600\mu\text{m}$ (25C)

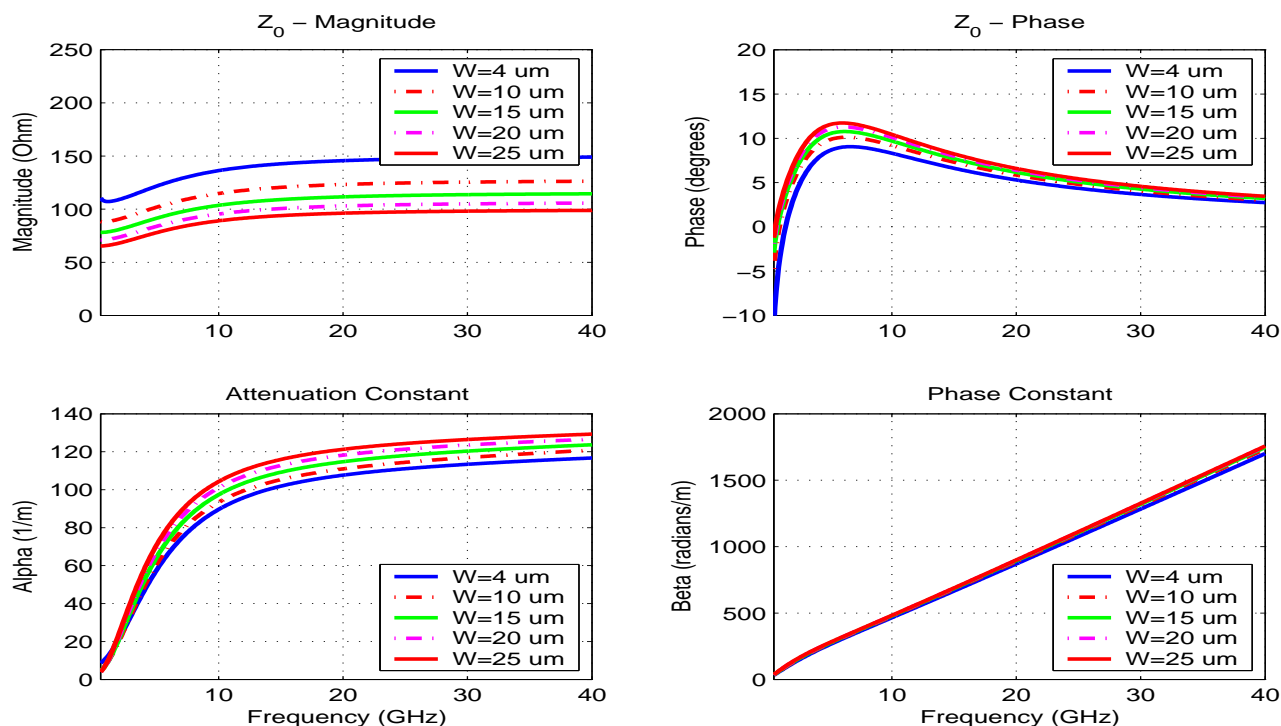


Figure 299. Simulated characteristic impedance, atten. and phase constants vs. Freq vs. width rfline: $l=200\mu\text{m}$

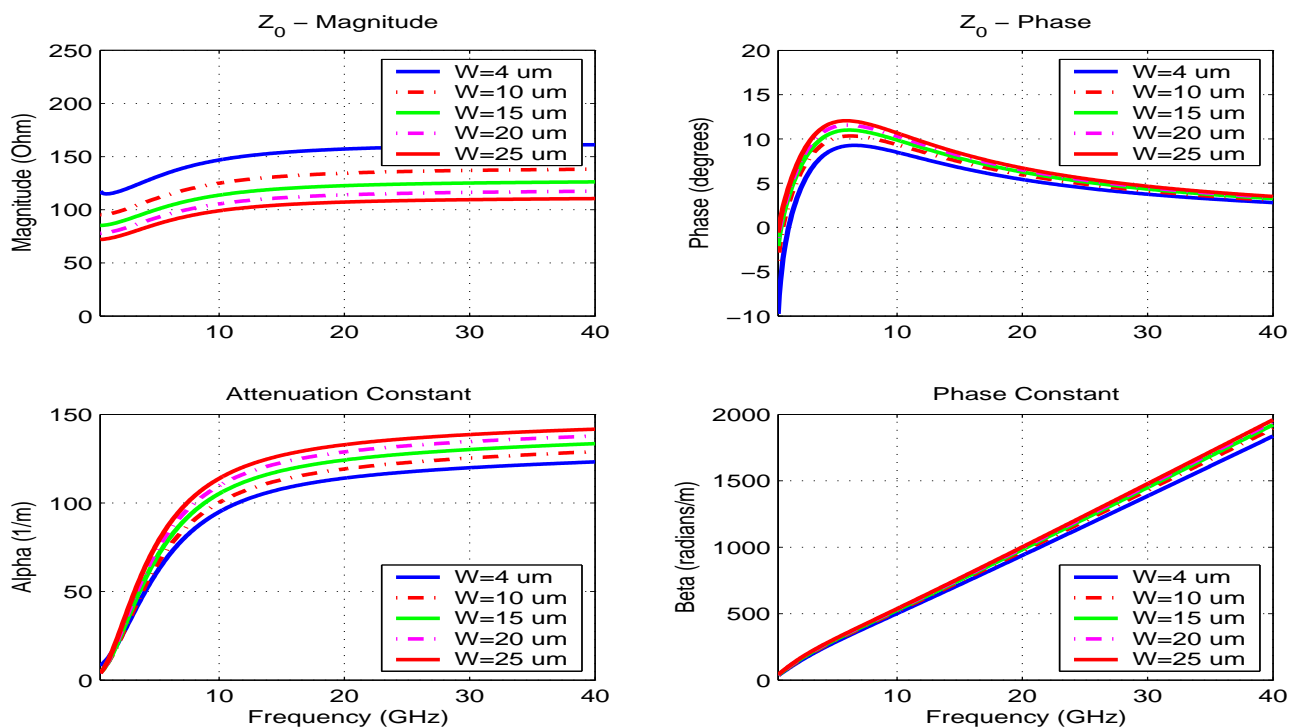


Figure 300. Simulated characteristic impedance, atten. and phase constants vs. Freq vs. width rfline: $l=400\mu\text{m}$

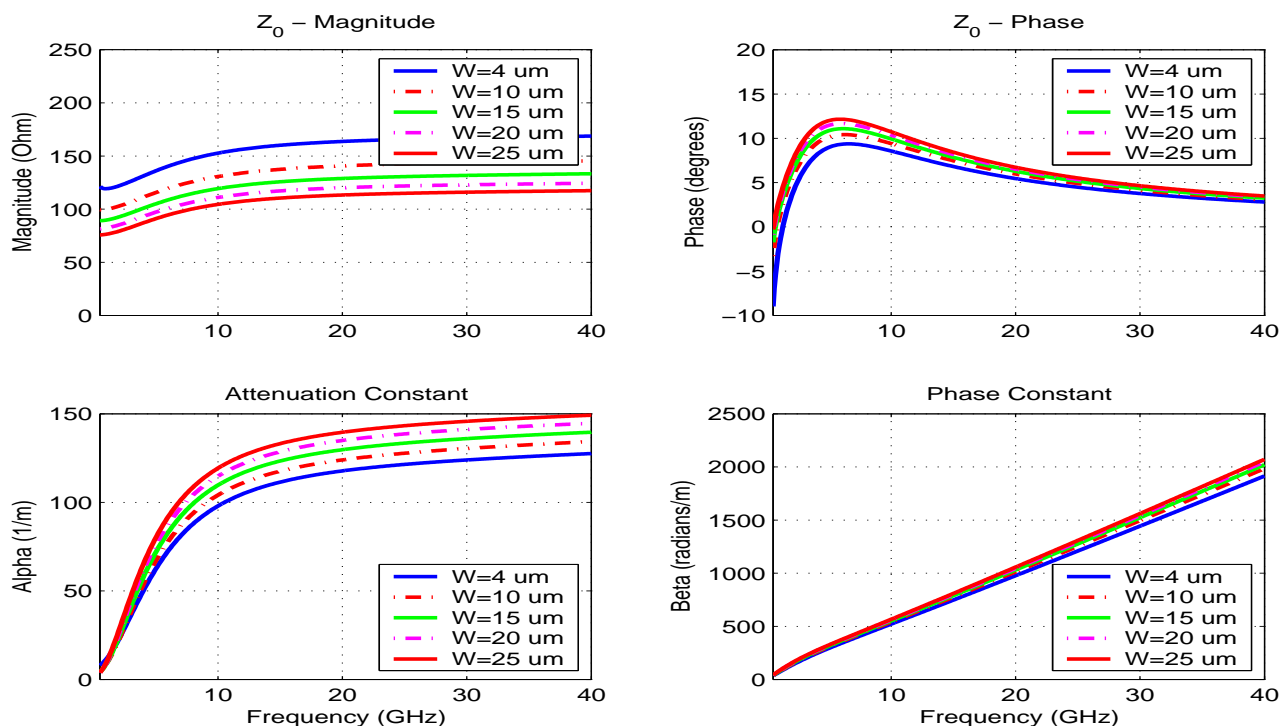


Figure 301. Simulated characteristic impedance, atten. and phase constants vs. Freq vs. width rflne: $l=600\mu m$

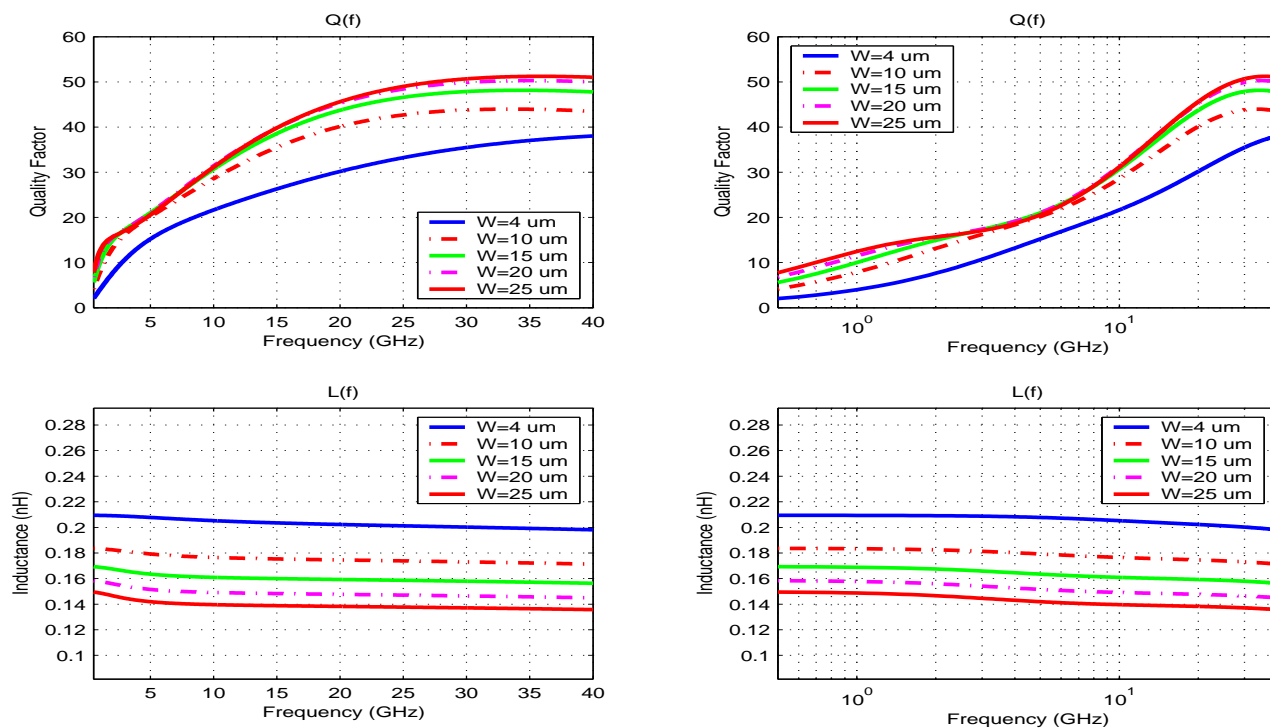


Figure 302. Simulated quality factor and inductance vs. Freq vs. width rflne: $l=200\mu m$

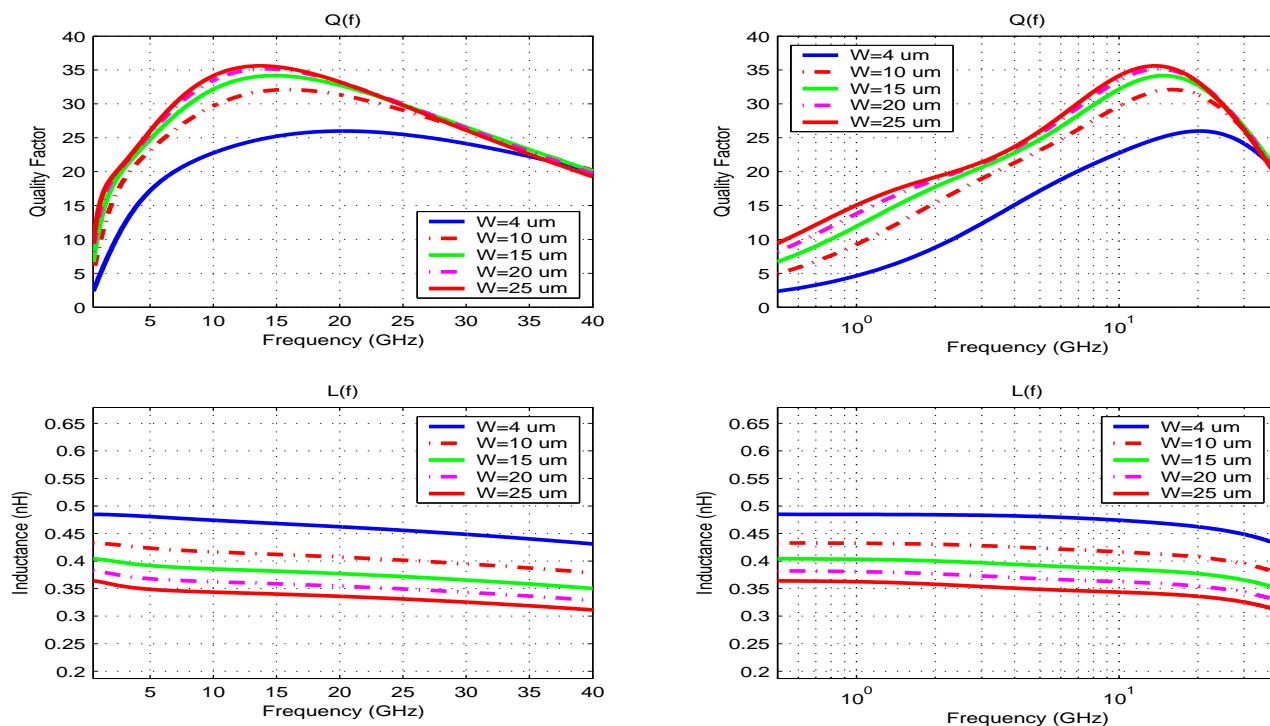


Figure 303. Simulated quality factor and inductance vs. Freq vs. width rflne: $l=400\mu\text{m}$

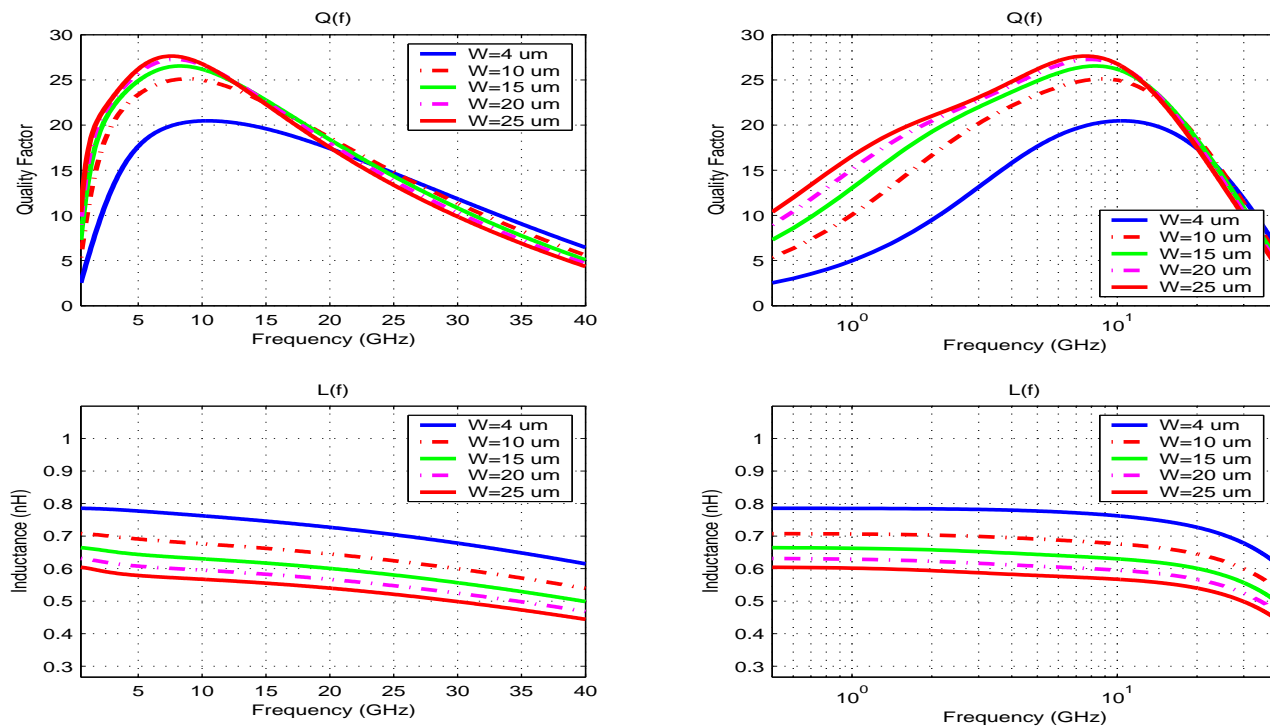


Figure 304. Simulated quality factor and inductance vs. Freq vs. width rflne: $l=600\mu\text{m}$

14.9 Model Correlation Plots

Two rflin geometries (rflin: $w=5\mu\text{m}$, $l=750\mu\text{m}$ and rflin: $w=15\mu\text{m}$, $l=750\mu\text{m}$) have been selected to illustrate representative fits of simulated inductance, Q , characteristic impedance, S -parameters, attenuation and phase constants to measured data.

All measured data was taken on hardware that had five levels of metal including the top level (M1, M2, MQ, LY, AM). This corresponds to a dielectric stack height of $12.37\mu\text{m}$ from the silicon substrate to the bottom of the AM metal layer. A DT lattice was present under each measured rflin test structure. Figures **70- 75** show simulation versus measured data results for inductance, Q , characteristic impedance, S -parameters, attenuation and phase constants.

The nature of two port on-wafer measurement structures requires a ground connection between port one and port two at the wafer level. Ground-signal-ground measurement probes are used necessitating a coplanar waveguide approach to realizing a long rflin between two measurement probes. The inductor of interest stretches from the center (signal) probe of port one to the center probe of port two. A ground connection is run on either side of this line to make the required connection between the ground probes on either side of the signal probe at each port. These ground lines are wide ($\sim 160\mu\text{m}$) to minimize their self inductance and series resistance and they are spaced about $170\mu\text{m}$ from the signal line on either side. However, the coplanar configuration of ground lines on either side of the RFLin test structures lowers the inductance value of the RFLin to be slightly lower relative to an RFLin structure with no ground return lines. This can be seen in Figures 74 and 75. Shown along with the measured and RFLin curves are the curves representing the results of ADS Momentum electromagnetic simulations of the RFLin structure.

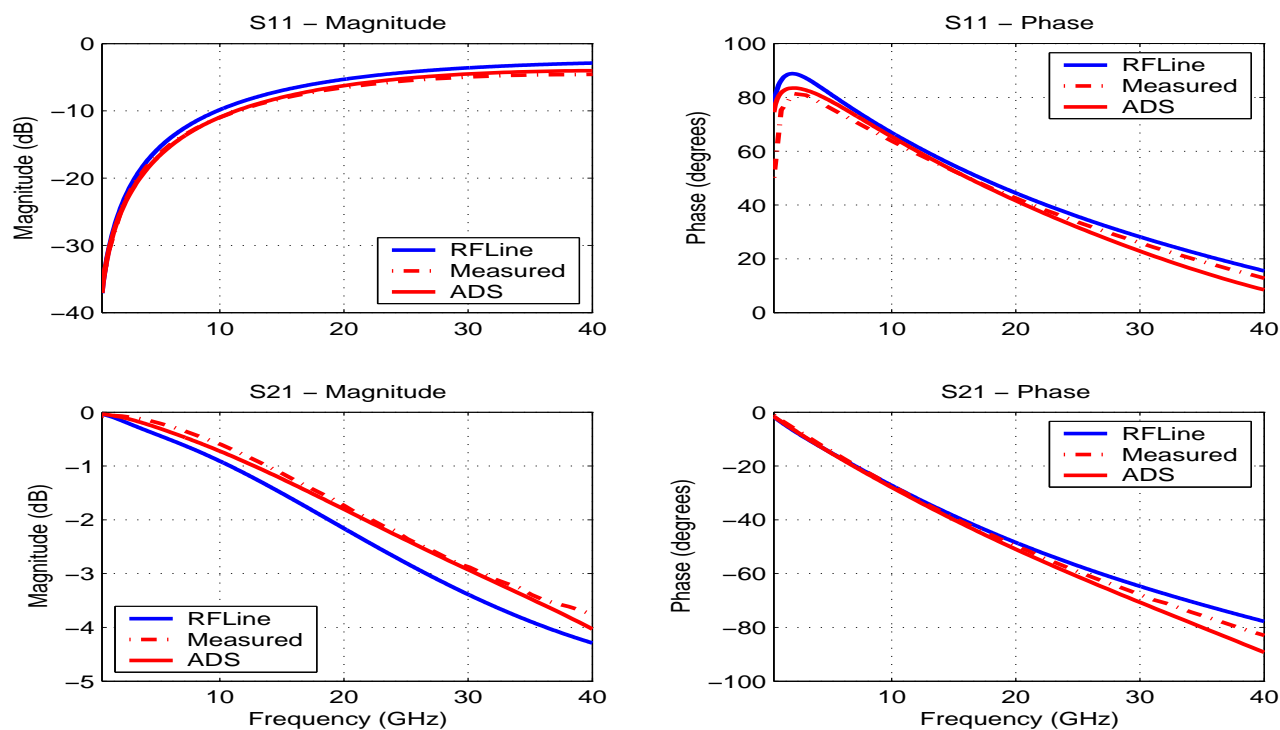


Figure 305. S-parameters vs. Freq, rfline: $w=5\mu\text{m}$, $l=750\mu\text{m}$ (25C)

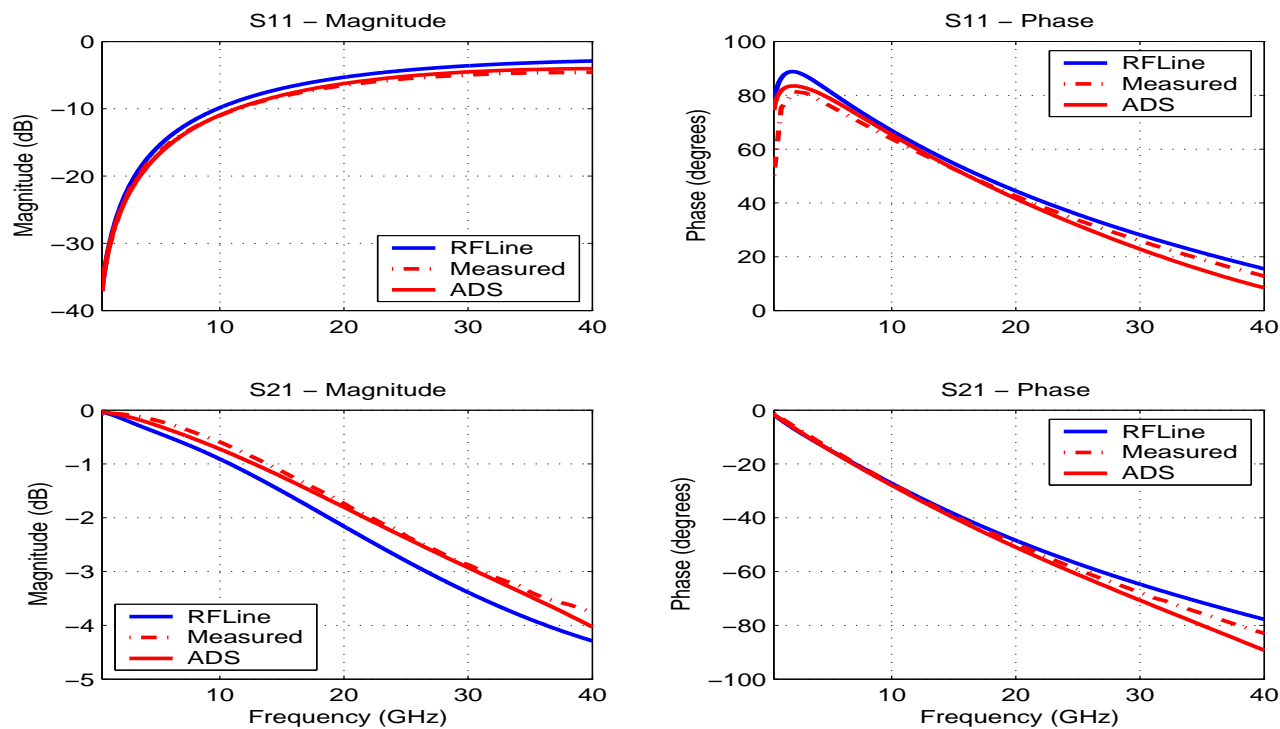


Figure 306. S-parameters vs. Freq vs. width rfline: $w=15\mu\text{m}$, $l=750\mu\text{m}$ (25C)

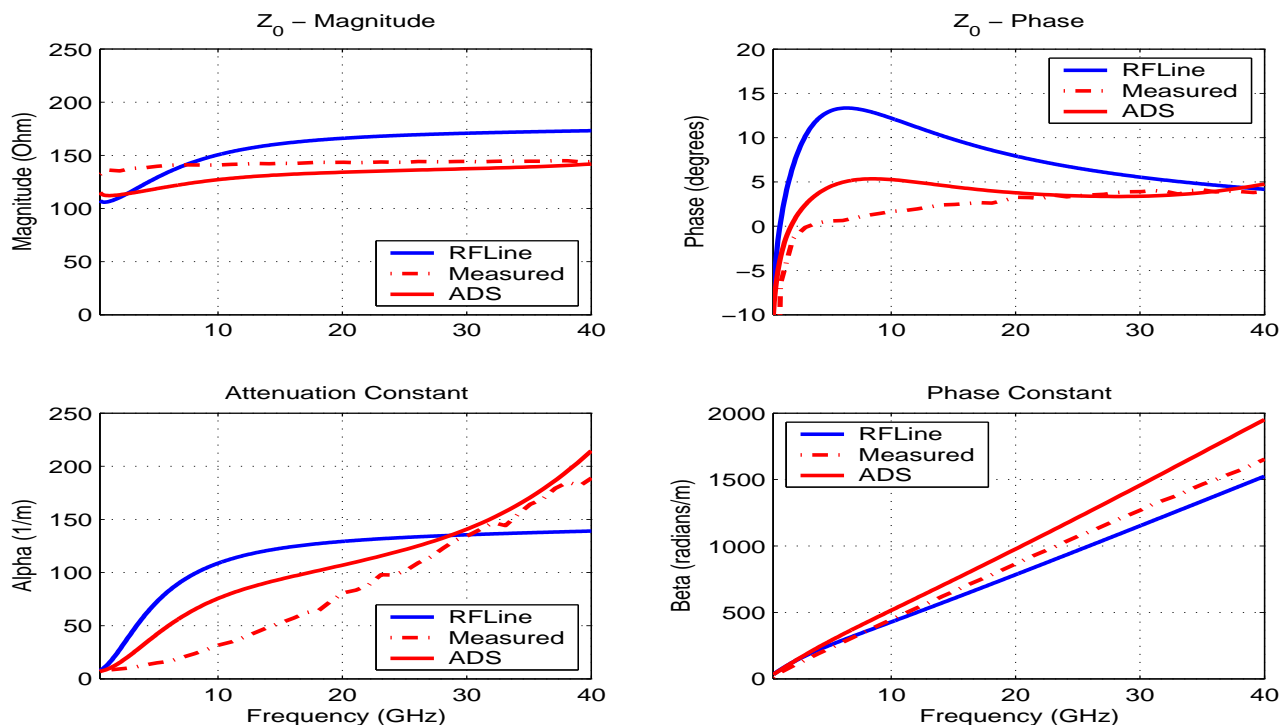


Figure 307. Characteristic impedance, atten. and phase constants vs. Freq rfline: $w=5\mu\text{m}$, $l=750\mu\text{m}$ (25C)

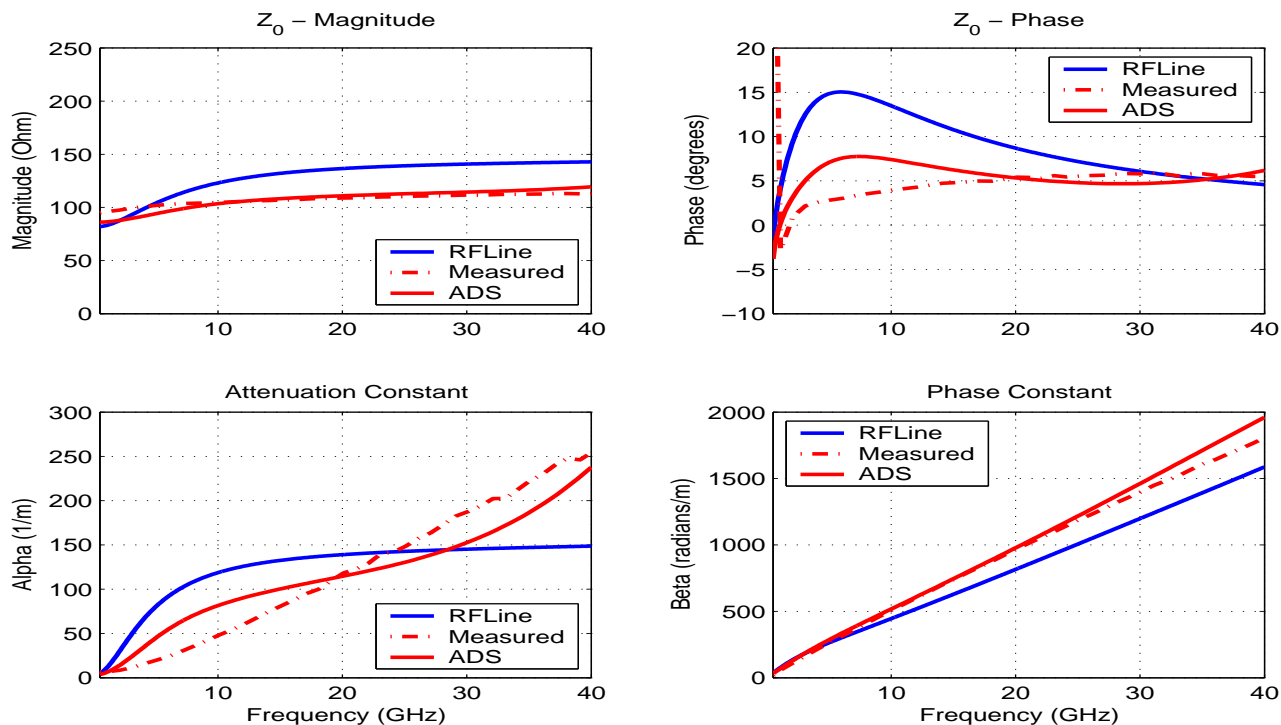


Figure 308. Characteristic impedance, atten. and phase constants vs. Freq rfline: $w=15\mu\text{m}$, $l=750\mu\text{m}$ (25C)

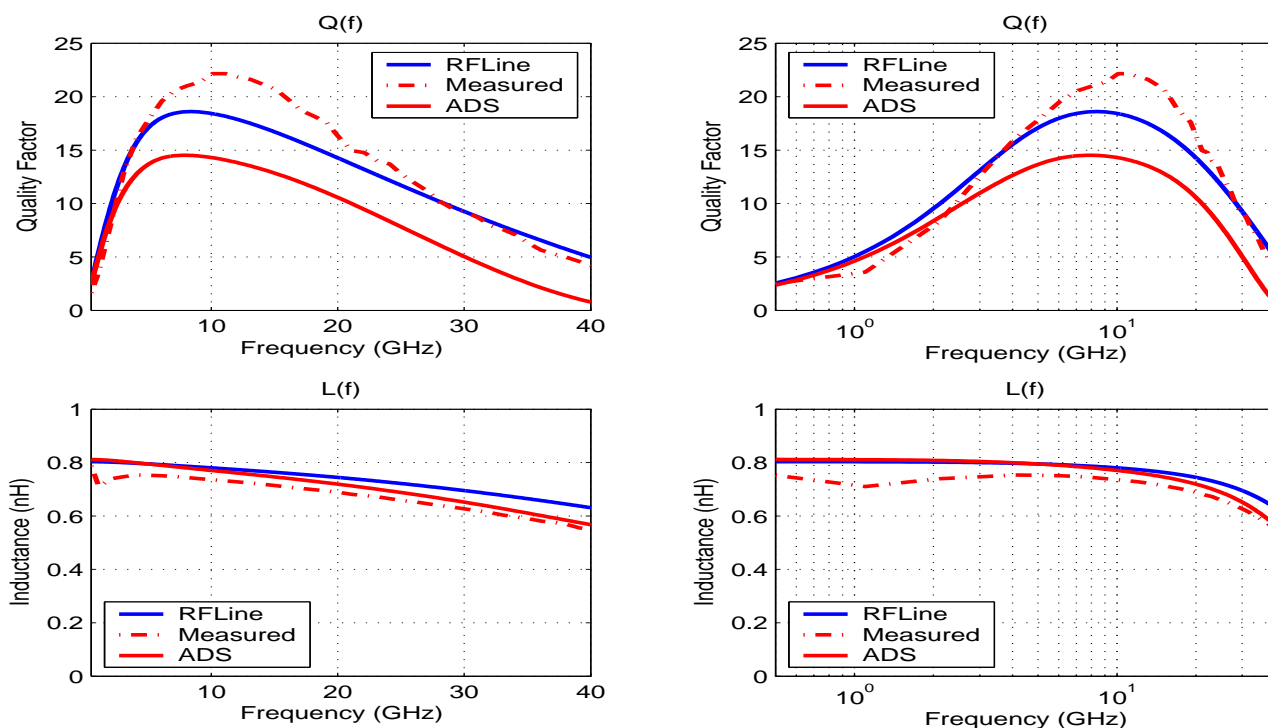


Figure 309. Quality factor and line inductance vs. Freq rfline: $w=5\mu\text{m}$, $l=750\mu\text{m}$ (25C)

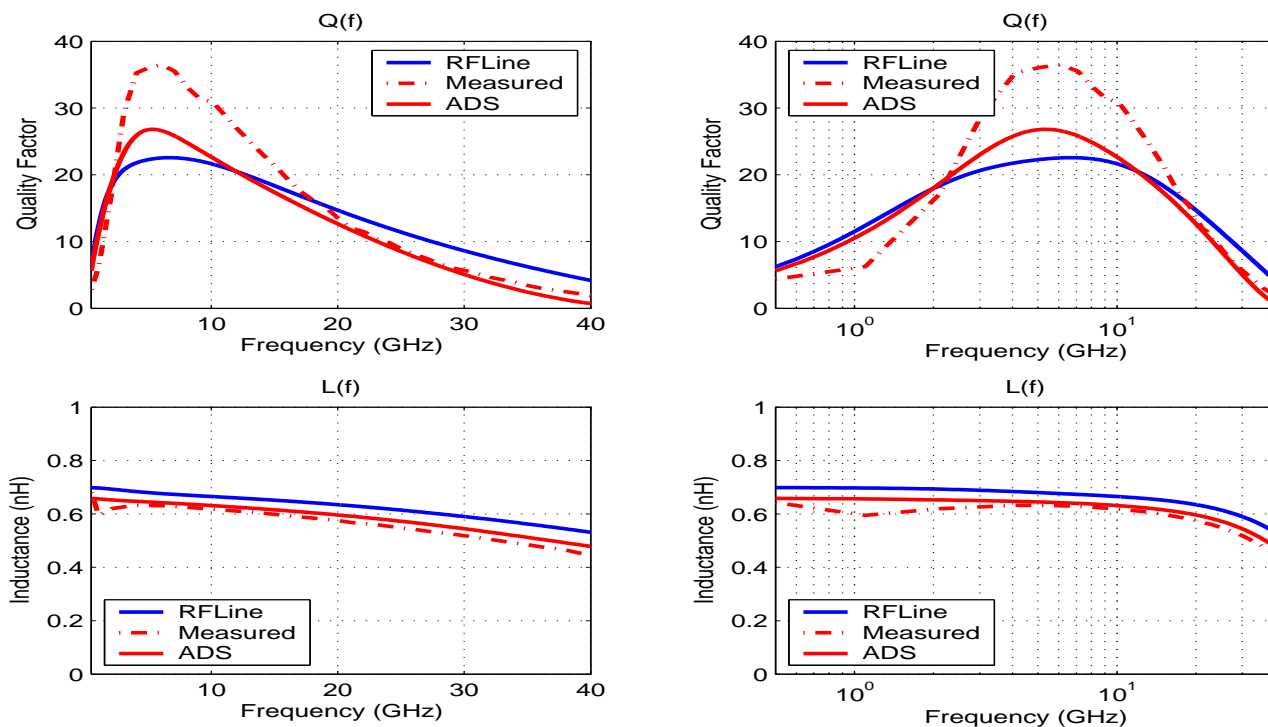


Figure 310. Quality factor and line inductance vs. Freq rfline: $w=15\mu\text{m}$, $l=750\mu\text{m}$ (25C)

15.0 Transmission Line Interconnect Models

The current design kit release includes models for the following topologies:

- Straight single wire shielded transmission line, thereafter referred to as SINGLEWIRE;
- Two straight wires shielded transmission line, thereafter referred to as COUPLEDWIRES.
- Straight single wire co-planar waveguide, thereafter referred to as SINGLECPW;
- Two straight wires coplanar waveguide, thereafter referred to as COUPLEDCPW.

Note: All interconnect models included in the current release are symmetrical.

15.1 Simulation Notes

Two-port S-parameter mode simulations were performed in the Cadence environment using the Spectre simulator. Effective R, C, L, and G (derived from simulated spectre singlewire S11- and S21-parameters) are presented. Ideal 50Ohm ports are used as loading ports in all simulations. The model file singlewire.scs contains a large number of simulated geometries with a Table form of R, L, and C data compared to z2d...not the tables in the singlewire model show the capacitance with metal pattern fill modeling enabled and without metal pattern fill modeling enabled. The resistance computed in singlewire contains the return resistance of the ground plane and side shields. For applications that need to be modeled at pure DC, please use extraction and not the singlewire model as the ground return resistance is included in the model. CPW models were run from the spectre environment and compared to z2d for frequency dependent R, C, and L.

15.2 Model versus EM Solver Plots (singlewire, coupledwires)

The singlewire model was verified against z2d which is an IBM internal 2-D field solver that solves for frequency dependent resistance, capacitance, and inductance. In the following plots: Figures 311-322, plots of frequency-dependent resistance, capacitance, inductance, and conductance (from signal line to ground...always zero) are shown. In Figures 323-326, spectre simulation of the couplewires model is shown compared to z2d. The self and mutual terms of capacitance and inductance are shown with frequency as well as resistance. The frequency-dependent resistance, capacitance, inductance, and conductance of the singlewire model are derived from the frequency-dependent S-parameter simulations of the singlewire model under various geometrical conditions. The output of z2d is already in terms of frequency-dependent R, C, L, and G...so no conversion is needed for the z2d data, so the data from z2d is directly from the output of the tool. Again, the field solver used to verify the singlewire and coupledwires models was z2d which is an IBM 2-D field solver "owned" by Alina Deutsch and her Interconnect and Packaging Analysis group (deutsch@us.ibm.com) at IBM's TJ Watson Research Center in Yorktown Heights, NY.

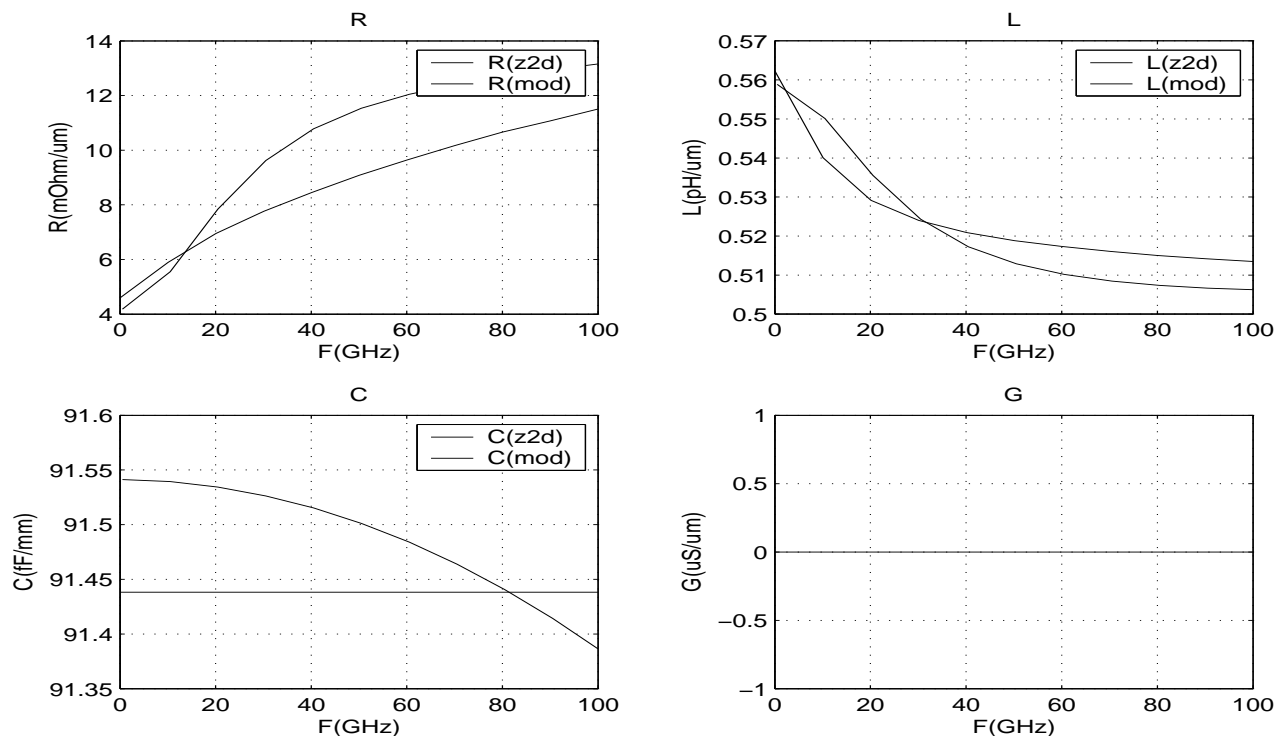


Figure 311. Simulated singlewire R, L, C, and G versus z2d for AM over M1, $w=5\mu\text{m}$, $n\text{lev}=5$.

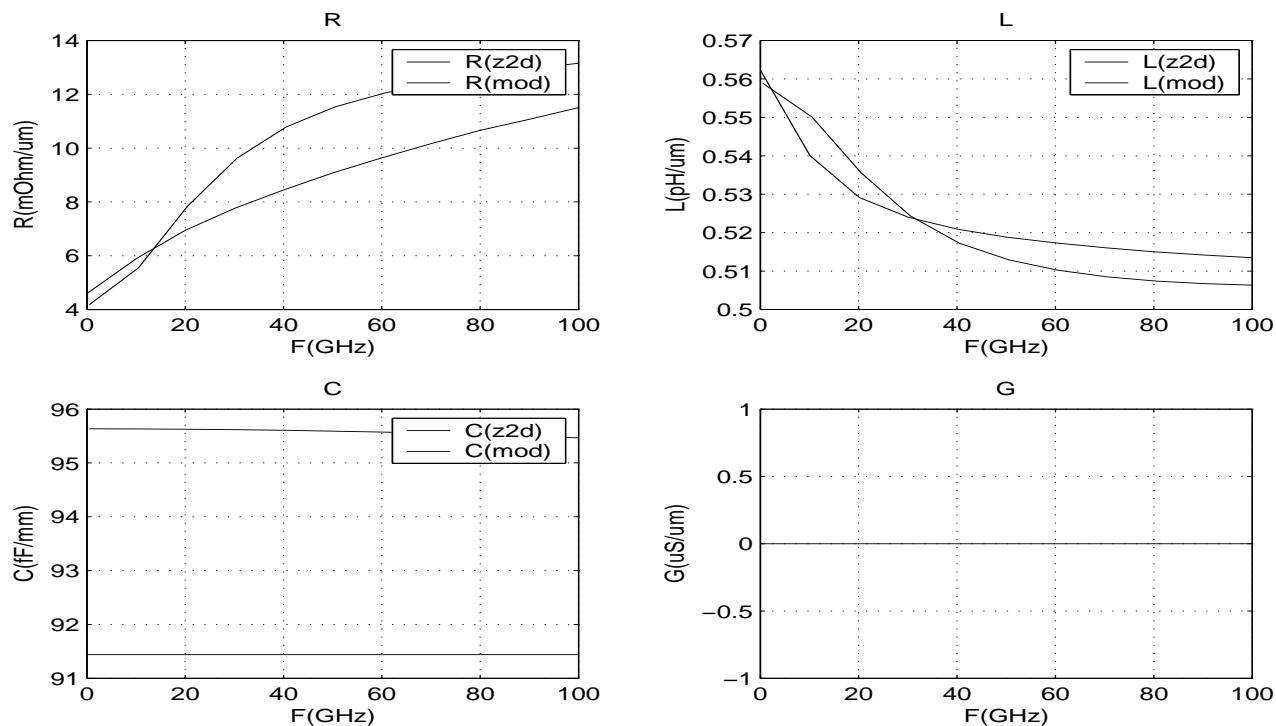


Figure 312. Simulated singlewire R, L, C, and G versus z2d for AM over M1, $w=5\mu\text{m}$, $n\text{lev}=5$ with metal fill modeled.

Note: Above simulations for singlewire, no side shielding, AM over M1, $w=5\mu\text{m}$, $n\text{lev}=5$ with and without fill.

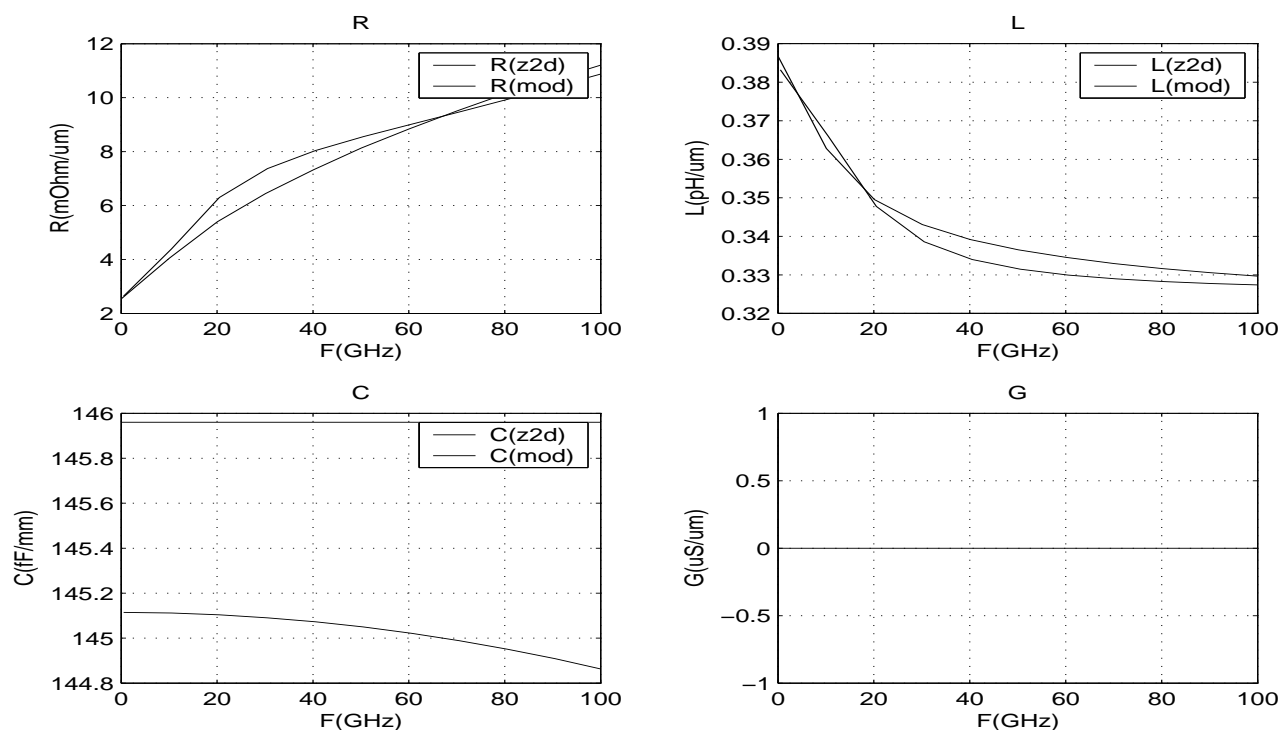


Figure 313. Simulated singlewire R, L, C, and G versus z2d for AM over M1, $w=5\mu\text{m}$, $s=6\mu\text{m}$, $nlev=5$.

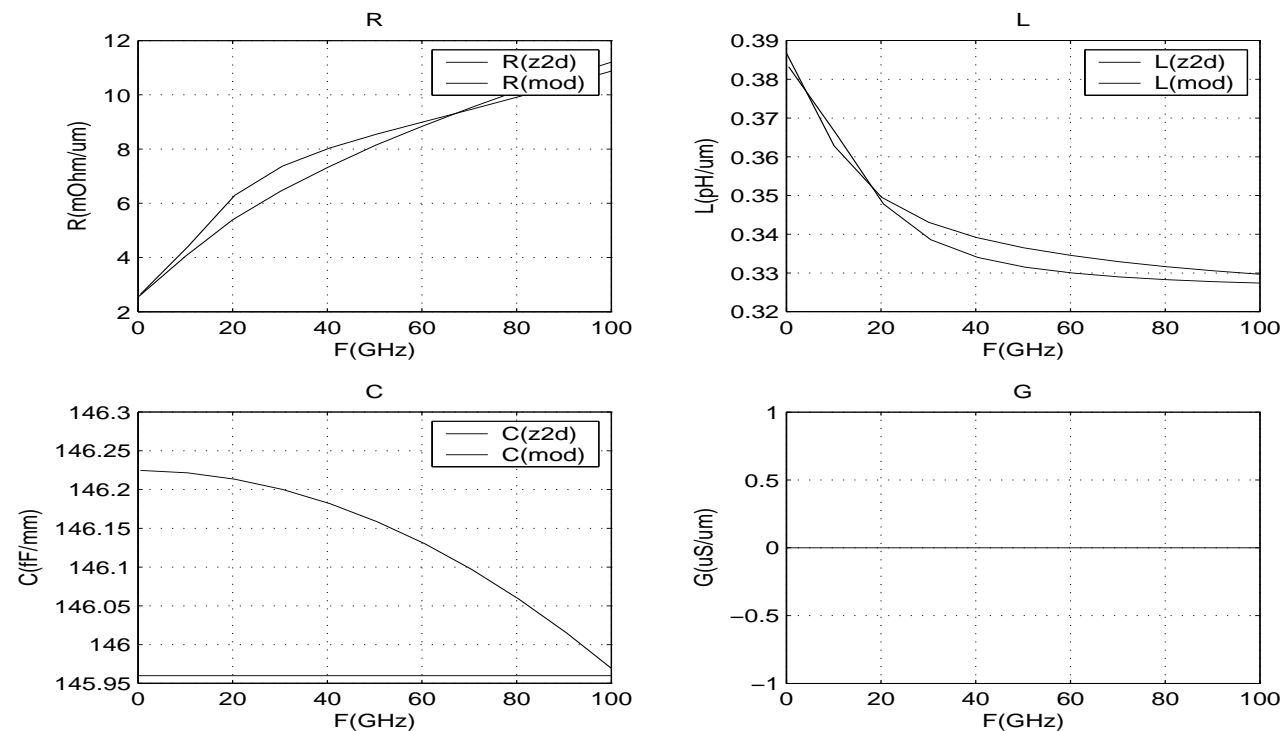


Figure 314. Simulated singlewire R, L, C, and G versus z2d for AM over M1, $w=5\mu\text{m}$, $s=6\mu\text{m}$, $nlev=5$ with metal fill.

Note: Above simulations for singlewire, AM over M1, $w=5\mu\text{m}$, $s=6\mu\text{m}$ (side-shields), $nlev=5$ with and without fill.

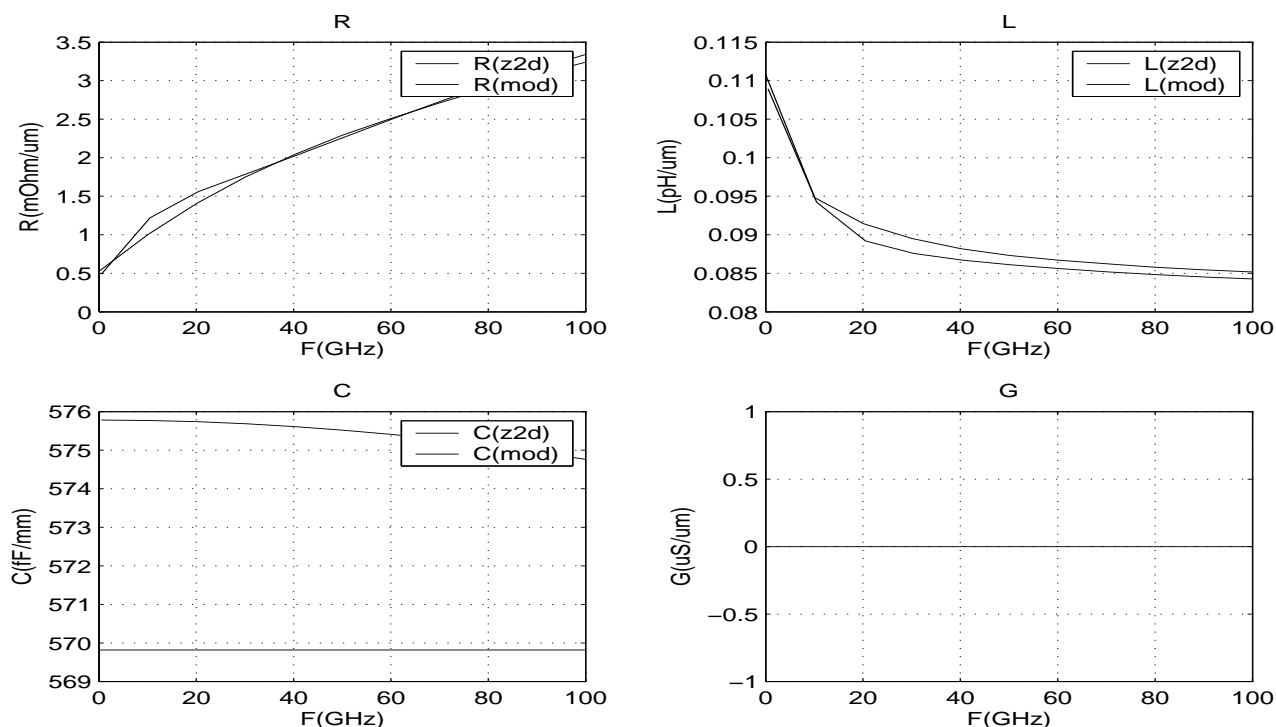


Figure 315. Simulated singlewire R, L, C, and G versus z2d for AM over LY, $w=50\mu\text{m}$, $nlev=5$.

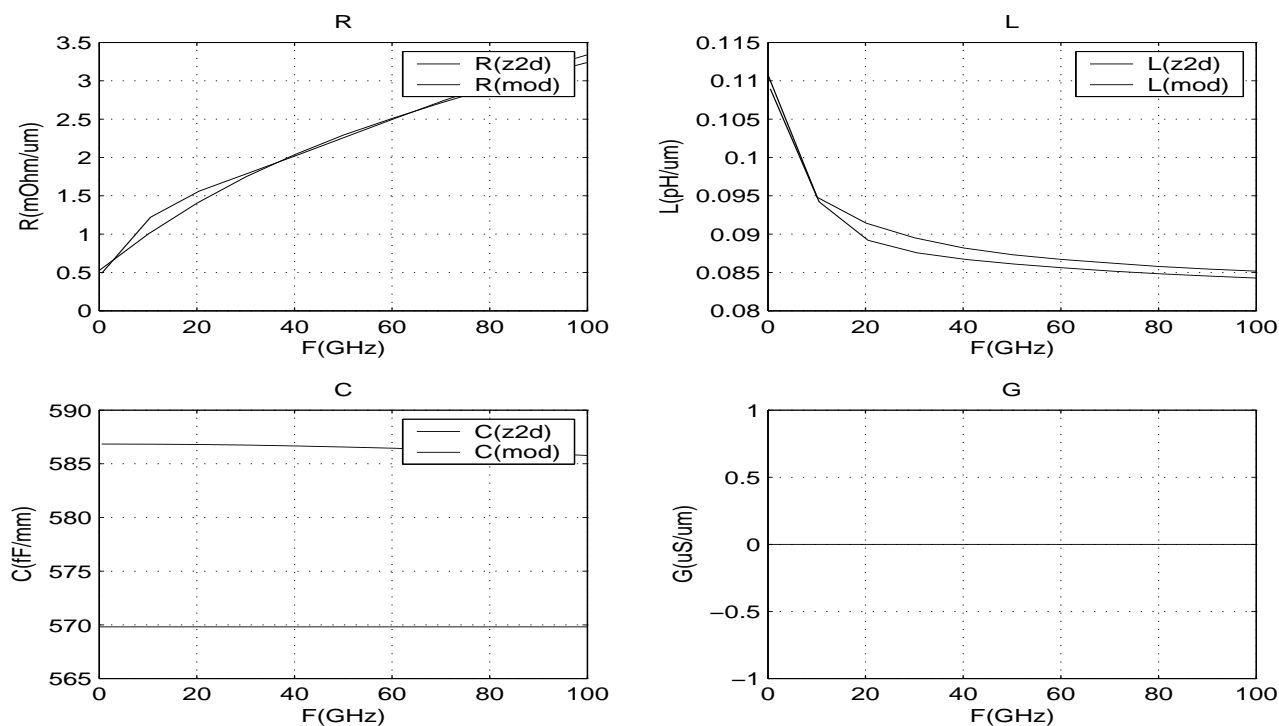


Figure 316. Simulated singlewire R, L, C, and G versus z2d for AM over LY, $w=50\mu\text{m}$, $nlev=5$, with fill.

Note: Above simulations for singlewire, AM over LY, $w=50\mu\text{m}$, $nlev=5$ with and without fill .

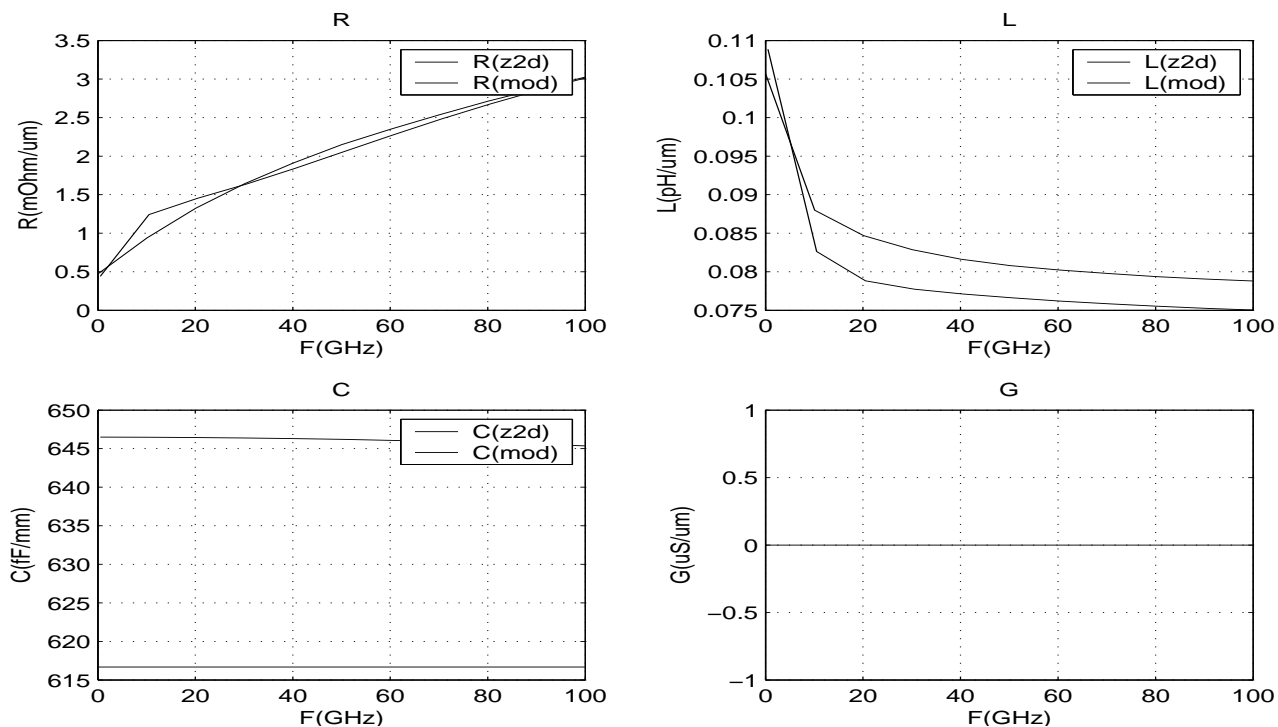


Figure 317. Simulated singlewire R, L, C, and G versus z2d for AM over LY, w=50um, s=6um, nlev=5.

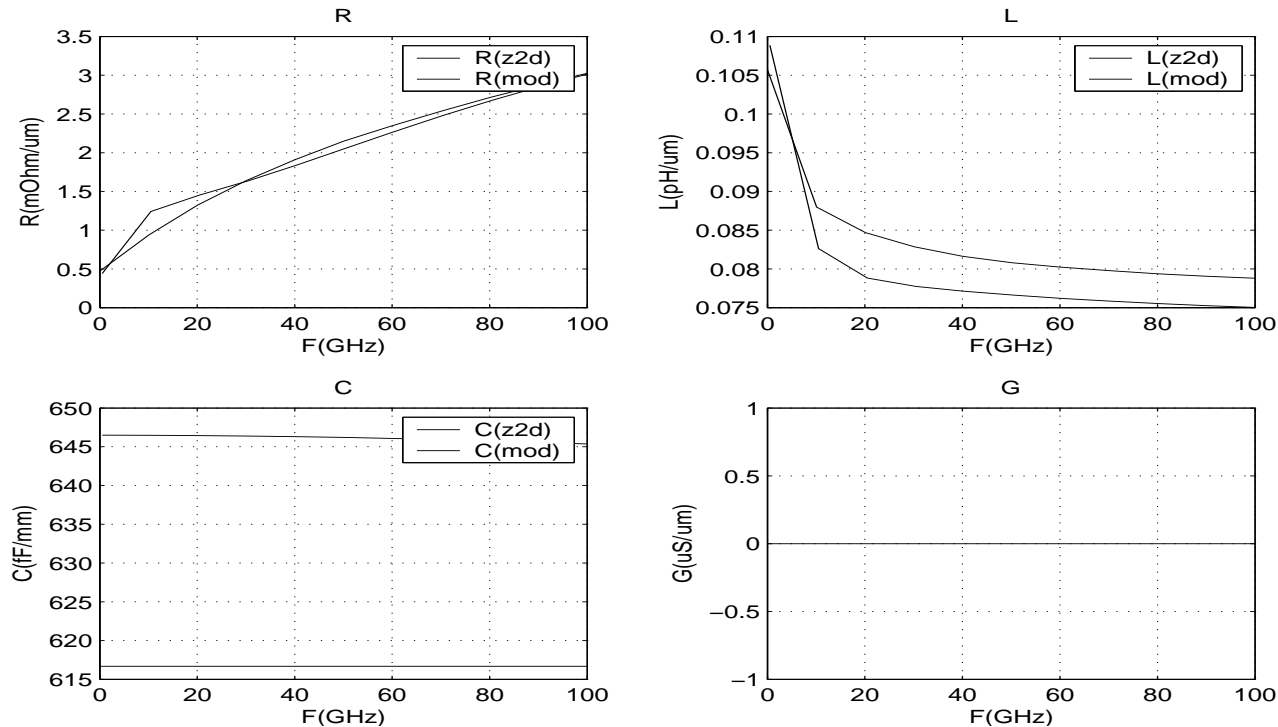


Figure 318. Simulated singlewire R, L, C, and G versus z2d for AM over LY, w=50um, s=6um, nlev=5, with fill.

Note: Above simulations for singlewire, AM over LY, w=50um, s=6um (side-shields), nlev=5 with and without fill.

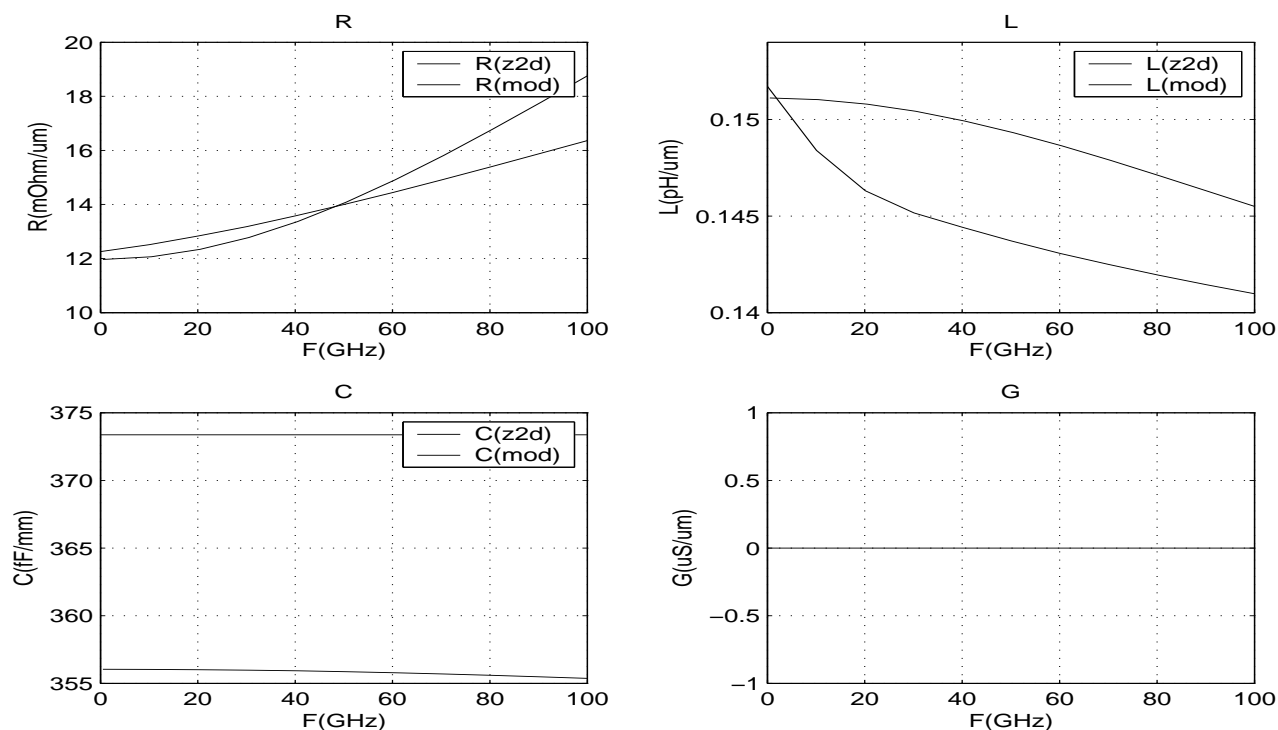


Figure 319. Simulated singlewire R, L, C, and G versus z2d for MQ over M1, $w=10\mu\text{m}$, $nlev=5$.

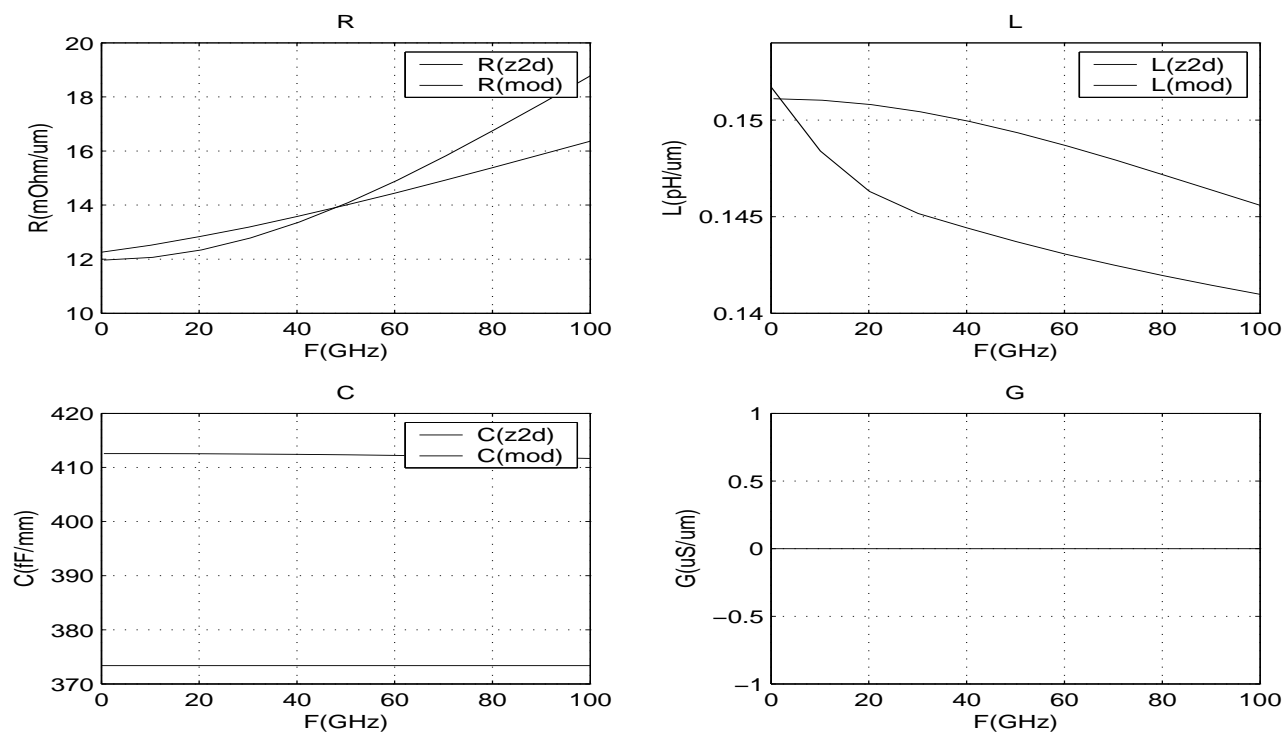


Figure 320. Simulated singlewire R, L, C, and G versus z2d for MQ over M1, $w=10\mu\text{m}$, $nlev=5$ with fill.

Note: Above simulations for singlewire, MQ over M1, $w=10\mu\text{m}$, $nlev=5$ with and without fill.

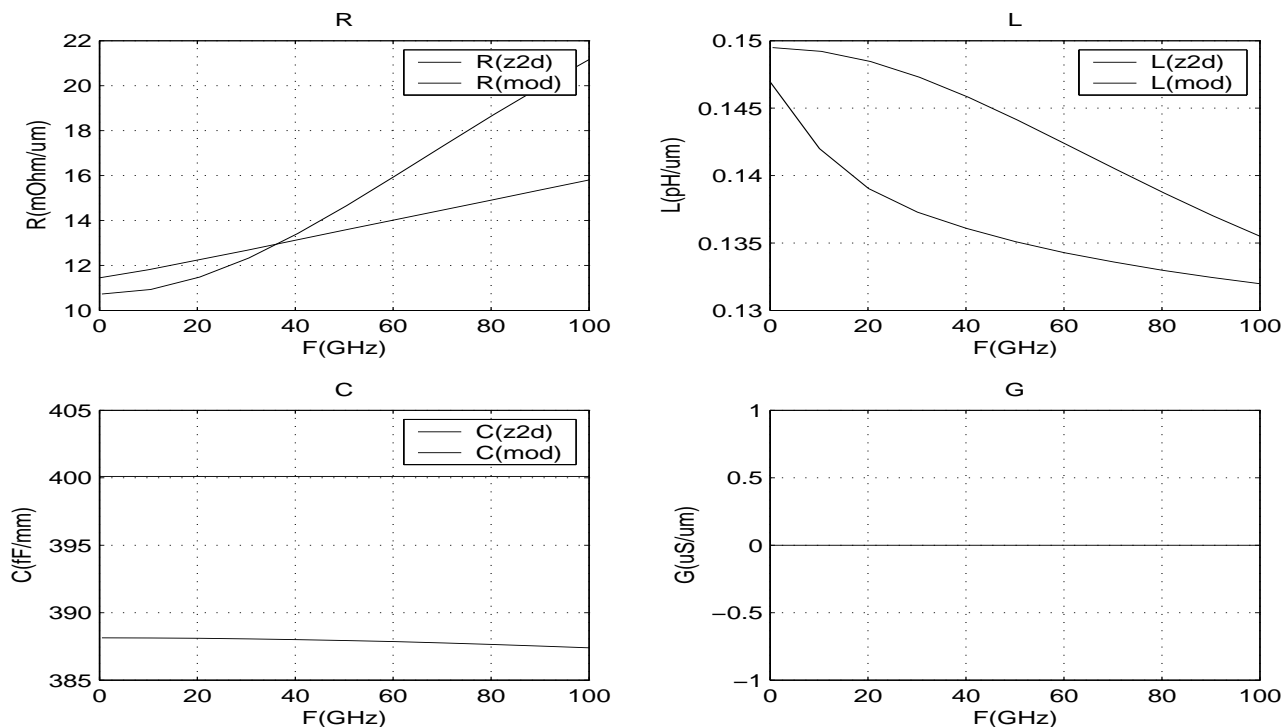


Figure 321. Simulated singlewire R, L, C, and G versus z2d for MQ over M1, $w=10\mu\text{m}$, $s=2\mu\text{m}$, $nlev=5$.

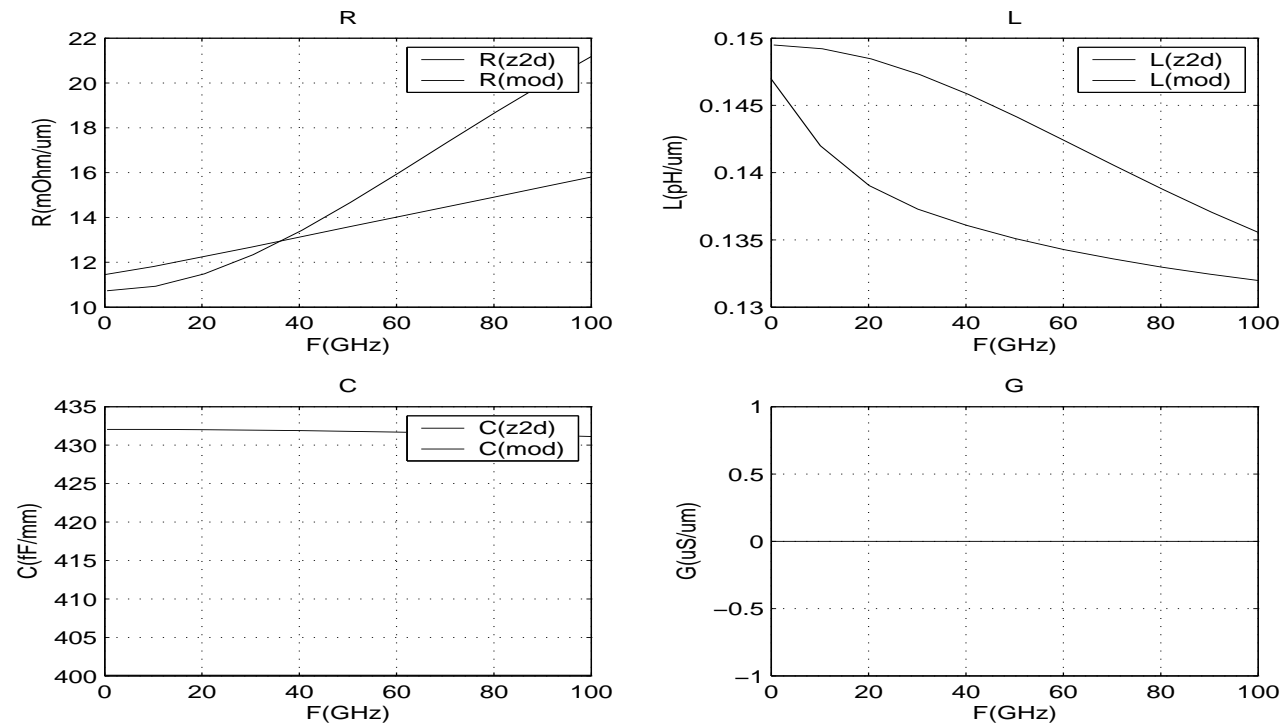


Figure 322. Simulated singlewire R, L, C, and G versus z2d for MQ over M1, $w=10\mu\text{m}$, $s=2\mu\text{m}$, $nlev=5$ with fill.

Note: Above simulations for singlewire, MQ over M1, $w=10\mu\text{m}$, $s=2\mu\text{m}$ (side-shields), $nlev=5$ with and without fill.

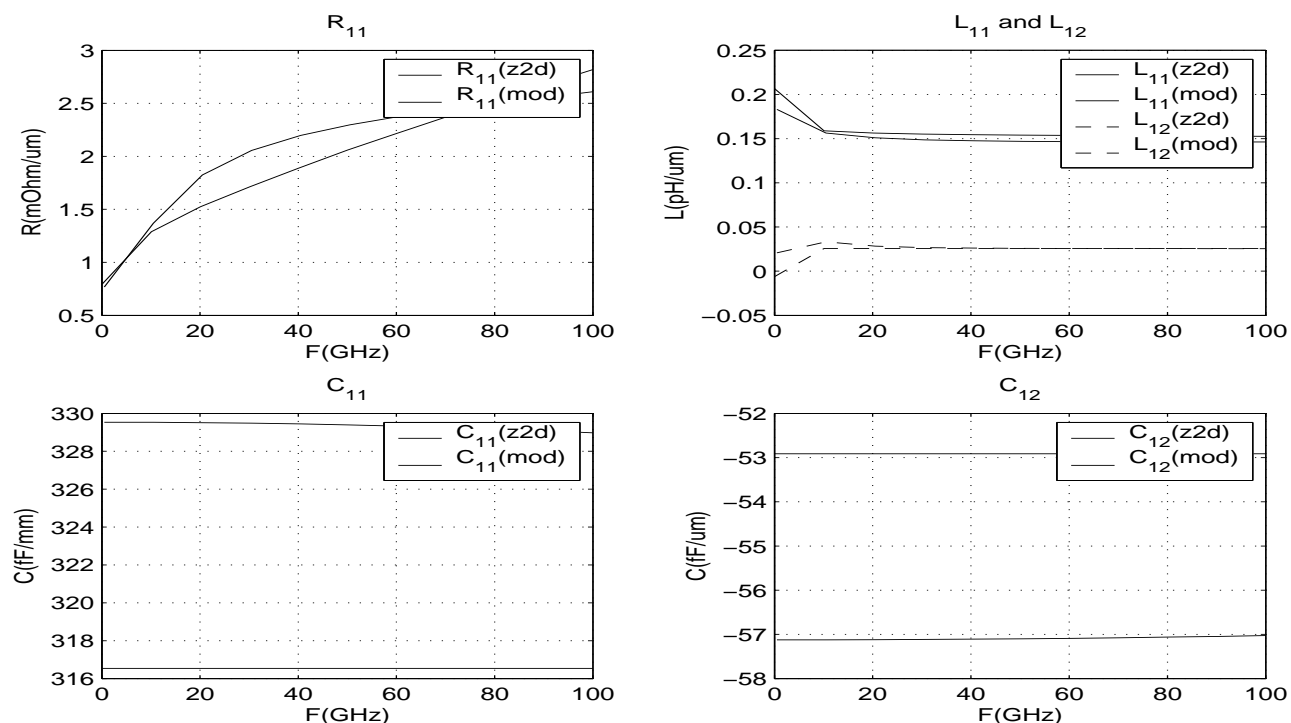


Figure 323. Simulated coupledwires R , L , C , and G versus $z2d$ for AMover MQ, $w=50\mu\text{m}$, $d=10\mu\text{m}$, $nlev=5$.

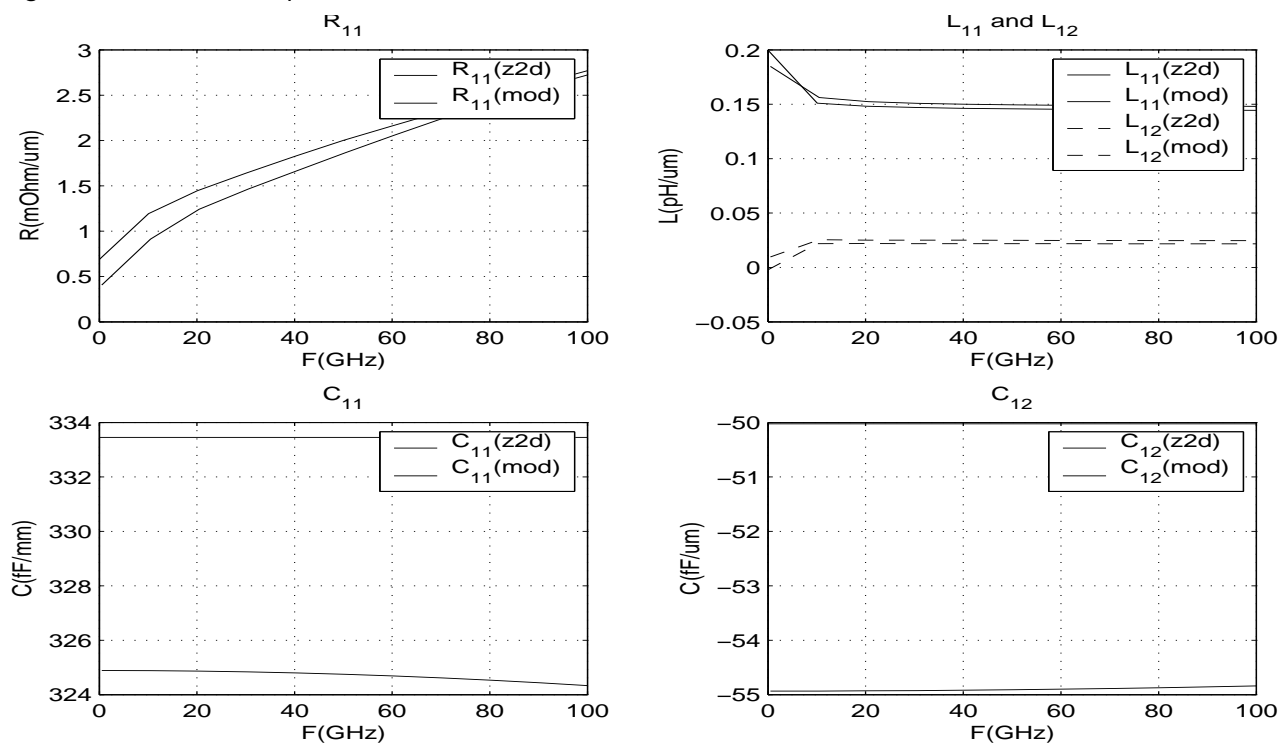


Figure 324. Simulated coupledwires R , L , C , and G versus $z2d$ for AMover MQ, $w=50\mu\text{m}$, $d=10\mu\text{m}$, $s=10\mu\text{m}$, $nlev=5$.

Note: Above simulations for coupledwires, AM over MQ, $w=50\mu\text{m}$, $d=10\mu\text{m}$, $nlev=5$ with and without side shields.

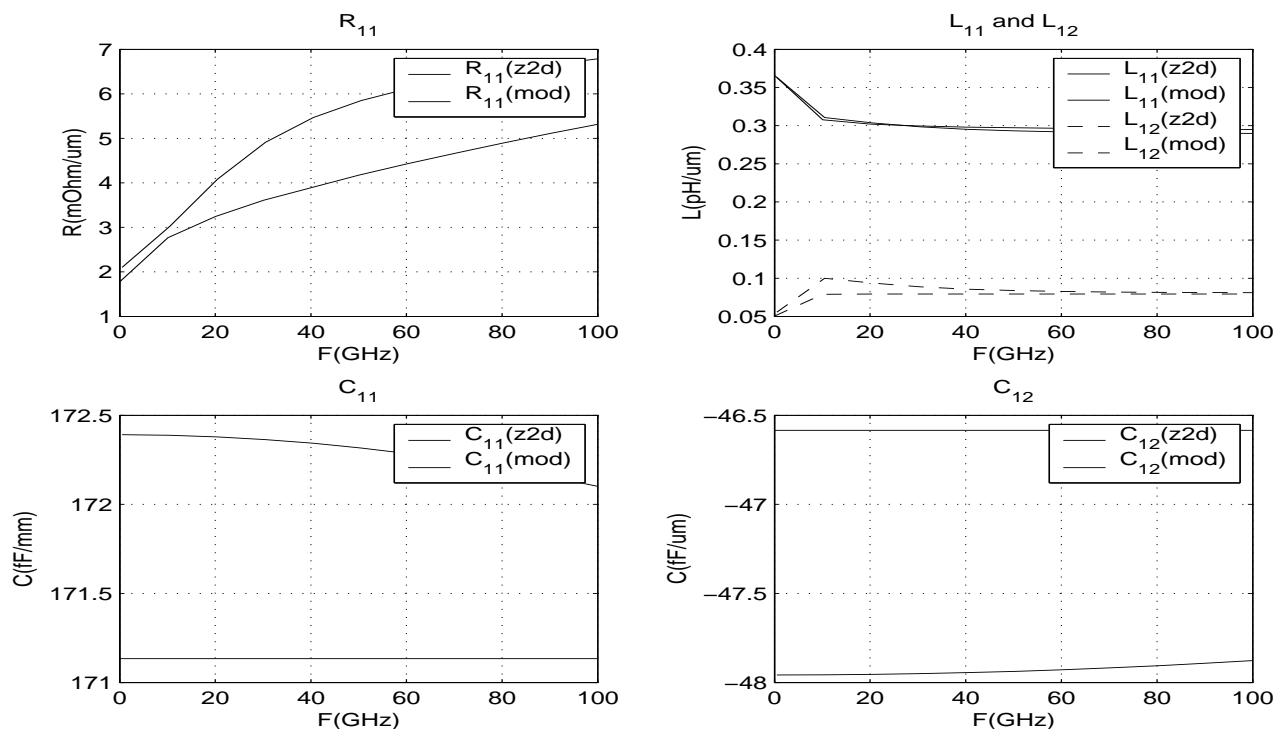


Figure 325. Simulated coupledwires, R , L , C , and G versus $z2d$ for AM over M1, $w=20\mu m$, $d=10\mu m$, $nlev=5$.

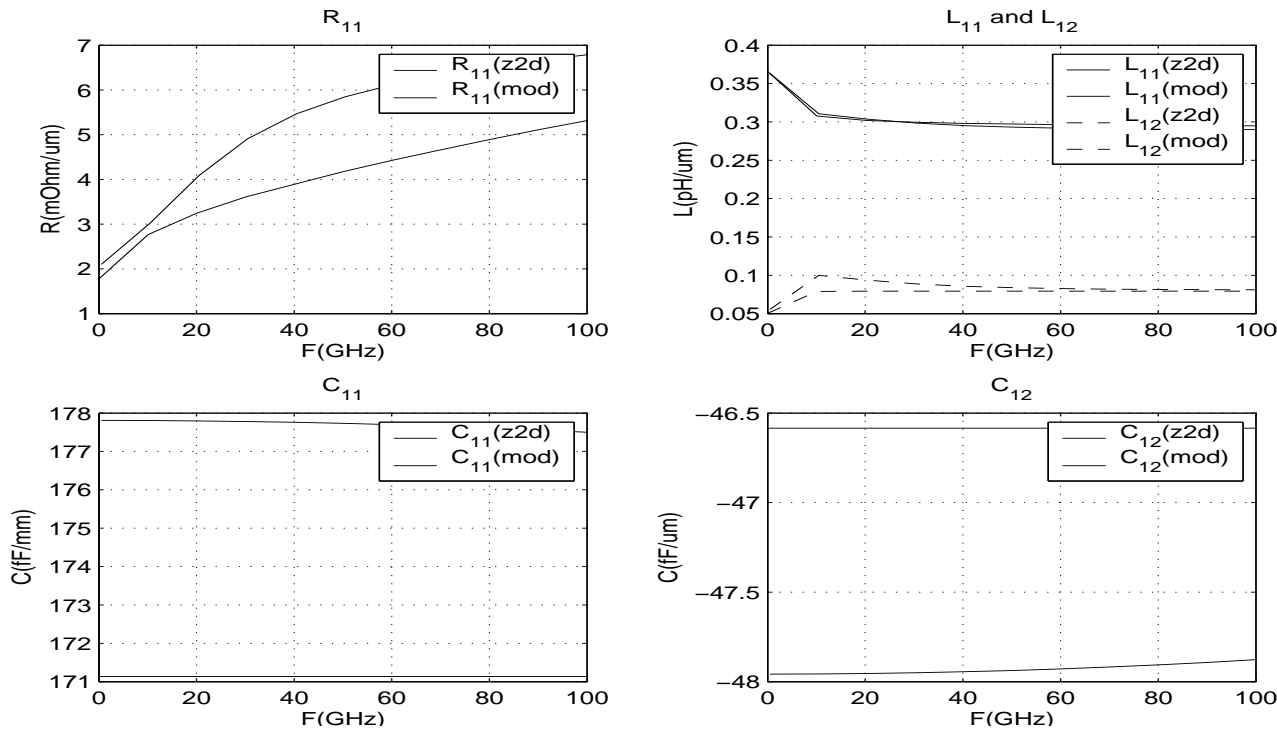


Figure 326. Simulated coupledwires, R , L , C , and G versus $z2d$ for AM over M1, $w=20\mu m$, $d=10\mu m$, $nlev=5$ with fill.

Note: Above simulations for coupledwires, AM over M1, $w=20\mu m$, $d=10\mu m$, $nlev=5$ with and without fill.

15.3 Model versus EM Solver Tables (singlewire)

Tables 85-88 represent the percentage difference between the singlewire model and field solver at various discrete frequencies for the three transmission line parameters Inductance, Resistance, and Capacitance respectively. Table 88, "Capacitance with Fill (% difference Model-Z2D)/Z2D*100" on page 414 shows the behavior of the singlewire model in the presence of dummy metal fill.

Table 84. Key to Capacitance, Inductance, and Resistance Table Testcase names

Testcase Text	Description
single	singlewire model
ss (____)	side shield or no side shield
M2_M1	(signal layer)_(ground layer)...so...signal layer = 'M2' and ground layer = 'M1'
w1 (w2)	minimum width for signal layer: w1 = [0.190 0.200 0.200 1.4900 2.000] for the layers ['M1' 'M2' 'MQ' 'LY' 'MA'], w2 = 50um
s1 (_s2_, ____)	signal to side shield space s1: s=minimum width of signal layer (see w1 above) s2: s=2um ('M1' 'M2' 'M3' 'M4' 'MQ'), s=10um ('LY' 'AM') ____: no side shield
stack5 (stack6, stack7)	nlev5, nlev6 or nlev7

Table 85. Capacitance (% difference Model-Z2D)/Z2D*100)

Testcase	10.5 GHz	20.5 GHz	30.5 GHz	40.5 GHz	50.5 GHz	60.5 GHz	70.5 GHz	80.5 GHz
single____M2_M1_w1____stack5	1.85	1.84	1.83	1.81	1.79	1.77	1.74	1.71
single_ss_M2_M1_w1_s1_stack5	-9.78	-9.78	-9.8	-9.81	-9.84	-9.87	-9.9	-9.94
single_ss_M2_M1_w1_s2_stack5	3.01	3	2.99	2.97	2.95	2.92	2.89	2.86
single____M2_M1_w2____stack5	1.15	1.14	1.13	1.11	1.09	1.06	1.03	0.99
single_ss_M2_M1_w2_s1_stack5	7.14	7.14	7.12	7.1	7.07	7.04	7	6.96
single_ss_M2_M1_w2_s2_stack5	7.43	7.42	7.4	7.38	7.35	7.31	7.27	7.22
single____MQ_M1_w1____stack5	-4.42	-4.43	-4.44	-4.45	-4.47	-4.49	-4.51	-4.54
single_ss_MQ_M1_w1_s1_stack5	-13.76	-13.77	-13.78	-13.8	-13.82	-13.84	-13.87	-13.9
single_ss_MQ_M1_w1_s2_stack5	-9.65	-9.65	-9.66	-9.67	-9.69	-9.71	-9.73	-9.75
single____MQ_M1_w2____stack5	-5.13	-5.14	-5.15	-5.16	-5.18	-5.2	-5.22	-5.25
single_ss_MQ_M1_w2_s1_stack5	-0.66	-0.67	-0.68	-0.69	-0.71	-0.73	-0.76	-0.79
single_ss_MQ_M1_w2_s2_stack5	0.26	0.25	0.24	0.23	0.21	0.19	0.16	0.13
single____LY_M1_w1____stack5	-0.51	-0.51	-0.52	-0.53	-0.55	-0.57	-0.59	-0.62
single_ss_LY_M1_w1_s1_stack5	-4.45	-4.46	-4.47	-4.48	-4.5	-4.52	-4.55	-4.57
single_ss_LY_M1_w1_s2_stack5	2.58	2.57	2.56	2.55	2.53	2.51	2.49	2.46
single____LY_M1_w2____stack5	-2.27	-2.28	-2.29	-2.3	-2.32	-2.33	-2.36	-2.38
single_ss_LY_M1_w2_s1_stack5	0.41	0.41	0.4	0.39	0.37	0.35	0.33	0.3

Table 85. Capacitance (% difference Model-Z2D)/Z2D*100)

Testcase	10.5 GHz	20.5 GHz	30.5 GHz	40.5 GHz	50.5 GHz	60.5 GHz	70.5 GHz	80.5 GHz
single_ss_LY_M1_w2_s2_stack5	1.66	1.65	1.64	1.63	1.62	1.6	1.58	1.55
single____AM_M1_w1____stack5	0.91	0.91	0.9	0.89	0.87	0.85	0.83	0.8
single_ss_AM_M1_w1_s1_stack5	-2.63	-2.64	-2.65	-2.66	-2.68	-2.7	-2.72	-2.75
single_ss_AM_M1_w1_s2_stack5	1.63	1.62	1.61	1.6	1.59	1.57	1.54	1.52
single____AM_M1_w2____stack5	-0.85	-0.85	-0.86	-0.87	-0.89	-0.91	-0.93	-0.95
single_ss_AM_M1_w2_s1_stack5	-0.79	-0.79	-0.8	-0.82	-0.83	-0.85	-0.87	-0.9
single_ss_AM_M1_w2_s2_stack5	2.11	2.11	2.1	2.09	2.07	2.05	2.03	2
single____MQ_M2_w1____stack5	-3.42	-3.43	-3.44	-3.45	-3.47	-3.49	-3.52	-3.54
single_ss_MQ_M2_w1_s1_stack5	-11.15	-11.16	-11.17	-11.18	-11.2	-11.22	-11.25	-11.28
single_ss_MQ_M2_w1_s2_stack5	-6.61	-6.62	-6.63	-6.64	-6.66	-6.68	-6.7	-6.73
single____MQ_M2_w2____stack5	-4.22	-4.23	-4.24	-4.26	-4.28	-4.3	-4.33	-4.36
single_ss_MQ_M2_w2_s1_stack5	1.19	1.18	1.17	1.15	1.13	1.1	1.07	1.04
single_ss_MQ_M2_w2_s2_stack5	1.48	1.47	1.46	1.44	1.42	1.39	1.36	1.33
single____LY_M2_w1____stack5	-0.51	-0.52	-0.53	-0.54	-0.56	-0.58	-0.6	-0.63
single_ss_LY_M2_w1_s1_stack5	-3.98	-3.99	-4	-4.01	-4.03	-4.05	-4.07	-4.1
single_ss_LY_M2_w1_s2_stack5	1.36	1.36	1.35	1.33	1.32	1.3	1.27	1.25
single____LY_M2_w2____stack5	-1.81	-1.82	-1.83	-1.84	-1.85	-1.87	-1.89	-1.92
single_ss_LY_M2_w2_s1_stack5	1.29	1.28	1.28	1.26	1.25	1.23	1.2	1.18
single_ss_LY_M2_w2_s2_stack5	1.95	1.94	1.93	1.92	1.9	1.88	1.86	1.84
single____AM_M2_w1____stack5	1.04	1.03	1.02	1.01	0.99	0.98	0.95	0.93
single_ss_AM_M2_w1_s1_stack5	-2.5	-2.51	-2.52	-2.53	-2.54	-2.56	-2.59	-2.62
single_ss_AM_M2_w1_s2_stack5	1.44	1.43	1.42	1.41	1.4	1.38	1.35	1.33
single____AM_M2_w2____stack5	-0.54	-0.54	-0.55	-0.56	-0.58	-0.6	-0.62	-0.64
single_ss_AM_M2_w2_s1_stack5	-0.32	-0.33	-0.33	-0.35	-0.36	-0.38	-0.41	-0.43
single_ss_AM_M2_w2_s2_stack5	2.39	2.38	2.37	2.36	2.34	2.32	2.3	2.28
single____LY_MQ_w1____stack5	0.74	0.73	0.72	0.71	0.69	0.67	0.65	0.62
single_ss_LY_MQ_w1_s1_stack5	-2.67	-2.68	-2.69	-2.71	-2.73	-2.75	-2.77	-2.8
single_ss_LY_MQ_w1_s2_stack5	3.92	3.91	3.9	3.89	3.87	3.85	3.83	3.8
single____LY_MQ_w2____stack5	0.22	0.22	0.21	0.2	0.18	0.16	0.14	0.11
single_ss_LY_MQ_w2_s1_stack5	3.9	3.9	3.89	3.87	3.86	3.83	3.81	3.78
single_ss_LY_MQ_w2_s2_stack5	4.37	4.36	4.35	4.34	4.32	4.3	4.28	4.25
single____AM_MQ_w1____stack5	1.7	1.7	1.69	1.68	1.66	1.64	1.62	1.59
single_ss_AM_MQ_w1_s1_stack5	-2.18	-2.19	-2.2	-2.21	-2.23	-2.25	-2.27	-2.3
single_ss_AM_MQ_w1_s2_stack5	1.12	1.11	1.11	1.09	1.08	1.06	1.03	1.01
single____AM_MQ_w2____stack5	0.53	0.52	0.52	0.5	0.49	0.47	0.45	0.42
single_ss_AM_MQ_w2_s1_stack5	0.81	0.81	0.8	0.78	0.77	0.75	0.72	0.7

Table 85. Capacitance (% difference Model-Z2D)/Z2D*100)

Testcase	10.5 GHz	20.5 GHz	30.5 GHz	40.5 GHz	50.5 GHz	60.5 GHz	70.5 GHz	80.5 GHz
single_ss_AM_MQ_w2_s2_stack5	3.27	3.26	3.26	3.24	3.23	3.21	3.18	3.16
single____AM_LY_w1____stack5	1.56	1.55	1.54	1.53	1.51	1.49	1.47	1.44
single_ss_AM_LY_w1_s1_stack5	-0.17	-0.18	-0.19	-0.2	-0.22	-0.24	-0.27	-0.29
single_ss_AM_LY_w1_s2_stack5	-2.69	-2.7	-2.71	-2.72	-2.74	-2.75	-2.78	-2.8
single____AM_LY_w2____stack5	0.78	0.78	0.77	0.76	0.74	0.72	0.7	0.67
single_ss_AM_LY_w2_s1_stack5	4.21	4.21	4.2	4.18	4.16	4.14	4.12	4.09
single_ss_AM_LY_w2_s2_stack5	3.83	3.83	3.82	3.8	3.79	3.77	3.74	3.71
single____M2_M1_w1____stack6	1.85	1.84	1.83	1.81	1.79	1.77	1.74	1.71
single_ss_M2_M1_w1_s1_stack6	-9.78	-9.78	-9.8	-9.81	-9.84	-9.87	-9.9	-9.94
single_ss_M2_M1_w1_s2_stack6	3.01	3	2.99	2.97	2.95	2.92	2.89	2.86
single____M2_M1_w2____stack6	1.15	1.14	1.13	1.11	1.09	1.06	1.03	0.99
single_ss_M2_M1_w2_s1_stack6	7.14	7.14	7.12	7.1	7.07	7.04	7	6.96
single_ss_M2_M1_w2_s2_stack6	7.43	7.42	7.4	7.38	7.35	7.31	7.27	7.22
single____M3_M1_w1____stack6	-2.29	-2.29	-2.3	-2.32	-2.33	-2.35	-2.38	-2.4
single_ss_M3_M1_w1_s1_stack6	-14	-14.01	-14.02	-14.04	-14.07	-14.1	-14.14	-14.18
single_ss_M3_M1_w1_s2_stack6	-6.05	-6.06	-6.07	-6.08	-6.09	-6.11	-6.14	-6.16
single____M3_M1_w2____stack6	-3.7	-3.71	-3.72	-3.73	-3.75	-3.77	-3.79	-3.82
single_ss_M3_M1_w2_s1_stack6	1.13	1.13	1.11	1.1	1.08	1.06	1.03	1
single_ss_M3_M1_w2_s2_stack6	2.16	2.15	2.14	2.13	2.11	2.08	2.05	2.02
single____MQ_M1_w1____stack6	-3.61	-3.62	-3.63	-3.64	-3.65	-3.67	-3.7	-3.72
single_ss_MQ_M1_w1_s1_stack6	-15	-15.01	-15.02	-15.03	-15.05	-15.08	-15.11	-15.14
single_ss_MQ_M1_w1_s2_stack6	-7.97	-7.98	-7.99	-8	-8.02	-8.03	-8.06	-8.08
single____MQ_M1_w2____stack6	-5.38	-5.38	-5.39	-5.41	-5.42	-5.44	-5.46	-5.49
single_ss_MQ_M1_w2_s1_stack6	-2.01	-2.01	-2.02	-2.04	-2.05	-2.08	-2.1	-2.13
single_ss_MQ_M1_w2_s2_stack6	-0.07	-0.08	-0.09	-0.1	-0.12	-0.14	-0.16	-0.19
single____LY_M1_w1____stack6	-0.38	-0.39	-0.4	-0.41	-0.43	-0.44	-0.47	-0.49
single_ss_LY_M1_w1_s1_stack6	-4.84	-4.85	-4.86	-4.88	-4.89	-4.91	-4.94	-4.97
single_ss_LY_M1_w1_s2_stack6	3.64	3.63	3.62	3.61	3.59	3.57	3.55	3.52
single____LY_M1_w2____stack6	-2.63	-2.64	-2.65	-2.66	-2.68	-2.69	-2.72	-2.74
single_ss_LY_M1_w2_s1_stack6	-0.37	-0.38	-0.39	-0.4	-0.41	-0.43	-0.45	-0.48
single_ss_LY_M1_w2_s2_stack6	1.45	1.45	1.44	1.43	1.41	1.39	1.37	1.34
single____AM_M1_w1____stack6	0.83	0.82	0.81	0.8	0.79	0.77	0.74	0.72
single_ss_AM_M1_w1_s1_stack6	-2.76	-2.76	-2.77	-2.79	-2.8	-2.82	-2.85	-2.87
single_ss_AM_M1_w1_s2_stack6	1.79	1.78	1.77	1.76	1.75	1.73	1.7	1.68
single____AM_M1_w2____stack6	-1.14	-1.14	-1.15	-1.16	-1.18	-1.2	-1.22	-1.24
single_ss_AM_M1_w2_s1_stack6	-1.23	-1.23	-1.24	-1.26	-1.27	-1.29	-1.31	-1.34

Table 85. Capacitance (% difference Model-Z2D)/Z2D*100)

Testcase	10.5 GHz	20.5 GHz	30.5 GHz	40.5 GHz	50.5 GHz	60.5 GHz	70.5 GHz	80.5 GHz
single_ss_AM_M1_w2_s2_stack6	1.83	1.83	1.82	1.81	1.79	1.77	1.75	1.72
single____M3_M2_w1____stack6	1.76	1.75	1.74	1.73	1.71	1.68	1.65	1.62
single_ss_M3_M2_w1_s1_stack6	-9.78	-9.79	-9.8	-9.82	-9.84	-9.87	-9.91	-9.94
single_ss_M3_M2_w1_s2_stack6	2.99	2.99	2.97	2.96	2.94	2.91	2.88	2.84
single____M3_M2_w2____stack6	1.15	1.14	1.13	1.11	1.08	1.06	1.02	0.98
single_ss_M3_M2_w2_s1_stack6	7.14	7.14	7.12	7.1	7.07	7.04	7	6.95
single_ss_M3_M2_w2_s2_stack6	7.43	7.42	7.4	7.38	7.35	7.31	7.27	7.22
single____MQ_M2_w1____stack6	-4.48	-4.49	-4.5	-4.51	-4.53	-4.55	-4.57	-4.59
single_ss_MQ_M2_w1_s1_stack6	-13.77	-13.77	-13.78	-13.8	-13.82	-13.85	-13.87	-13.91
single_ss_MQ_M2_w1_s2_stack6	-9.65	-9.66	-9.67	-9.68	-9.69	-9.71	-9.73	-9.76
single____MQ_M2_w2____stack6	-5.13	-5.14	-5.15	-5.16	-5.18	-5.2	-5.22	-5.25
single_ss_MQ_M2_w2_s1_stack6	-0.66	-0.67	-0.68	-0.7	-0.71	-0.74	-0.76	-0.79
single_ss_MQ_M2_w2_s2_stack6	0.26	0.25	0.24	0.23	0.21	0.19	0.16	0.13
single____LY_M2_w1____stack6	-0.52	-0.53	-0.54	-0.55	-0.57	-0.59	-0.61	-0.63
single_ss_LY_M2_w1_s1_stack6	-4.46	-4.46	-4.47	-4.49	-4.5	-4.53	-4.55	-4.58
single_ss_LY_M2_w1_s2_stack6	2.58	2.57	2.56	2.55	2.53	2.51	2.49	2.46
single____LY_M2_w2____stack6	-2.27	-2.28	-2.29	-2.3	-2.32	-2.33	-2.36	-2.38
single_ss_LY_M2_w2_s1_stack6	0.41	0.41	0.4	0.39	0.37	0.35	0.33	0.3
single_ss_LY_M2_w2_s2_stack6	1.66	1.65	1.64	1.63	1.62	1.6	1.58	1.55
single____AM_M2_w1____stack6	0.9	0.9	0.89	0.87	0.86	0.84	0.82	0.79
single_ss_AM_M2_w1_s1_stack6	-2.64	-2.64	-2.65	-2.66	-2.68	-2.7	-2.72	-2.75
single_ss_AM_M2_w1_s2_stack6	1.62	1.62	1.61	1.6	1.58	1.56	1.54	1.51
single____AM_M2_w2____stack6	-0.85	-0.85	-0.86	-0.87	-0.89	-0.91	-0.93	-0.95
single_ss_AM_M2_w2_s1_stack6	-0.8	-0.8	-0.81	-0.82	-0.84	-0.86	-0.88	-0.91
single_ss_AM_M2_w2_s2_stack6	2.11	2.11	2.1	2.09	2.07	2.05	2.03	2
single____MQ_M3_w1____stack6	-3.48	-3.49	-3.5	-3.51	-3.53	-3.55	-3.57	-3.6
single_ss_MQ_M3_w1_s1_stack6	-11.16	-11.17	-11.18	-11.19	-11.21	-11.24	-11.26	-11.3
single_ss_MQ_M3_w1_s2_stack6	-6.65	-6.66	-6.67	-6.68	-6.7	-6.72	-6.74	-6.77
single____MQ_M3_w2____stack6	-4.28	-4.29	-4.3	-4.32	-4.34	-4.36	-4.39	-4.42
single_ss_MQ_M3_w2_s1_stack6	1.13	1.12	1.11	1.09	1.07	1.04	1.01	0.98
single_ss_MQ_M3_w2_s2_stack6	1.42	1.41	1.4	1.38	1.36	1.33	1.3	1.27
single____LY_M3_w1____stack6	-0.52	-0.53	-0.53	-0.55	-0.56	-0.58	-0.61	-0.63
single_ss_LY_M3_w1_s1_stack6	-3.98	-3.99	-4	-4.01	-4.03	-4.05	-4.07	-4.1
single_ss_LY_M3_w1_s2_stack6	1.36	1.35	1.34	1.33	1.31	1.29	1.27	1.24
single____LY_M3_w2____stack6	-1.82	-1.82	-1.83	-1.85	-1.86	-1.88	-1.9	-1.93
single_ss_LY_M3_w2_s1_stack6	1.29	1.28	1.27	1.26	1.24	1.22	1.2	1.17

Table 85. Capacitance (% difference Model-Z2D)/Z2D*100)

Testcase	10.5 GHz	20.5 GHz	30.5 GHz	40.5 GHz	50.5 GHz	60.5 GHz	70.5 GHz	80.5 GHz
single_ss_LY_M3_w2_s2_stack6	1.94	1.93	1.92	1.91	1.9	1.88	1.86	1.83
single____AM_M3_w1____stack6	1.03	1.03	1.02	1.01	0.99	0.97	0.95	0.92
single_ss_AM_M3_w1_s1_stack6	-2.5	-2.51	-2.52	-2.53	-2.55	-2.57	-2.59	-2.62
single_ss_AM_M3_w1_s2_stack6	1.44	1.43	1.42	1.41	1.39	1.38	1.35	1.33
single____AM_M3_w2____stack6	-0.54	-0.55	-0.56	-0.57	-0.58	-0.6	-0.62	-0.65
single_ss_AM_M3_w2_s1_stack6	-0.32	-0.33	-0.34	-0.35	-0.36	-0.38	-0.41	-0.43
single_ss_AM_M3_w2_s2_stack6	2.38	2.38	2.37	2.36	2.34	2.32	2.3	2.27
single____LY_MQ_w1____stack6	0.74	0.73	0.72	0.71	0.69	0.67	0.65	0.62
single_ss_LY_MQ_w1_s1_stack6	-2.67	-2.68	-2.69	-2.71	-2.73	-2.75	-2.77	-2.8
single_ss_LY_MQ_w1_s2_stack6	3.92	3.91	3.9	3.89	3.87	3.85	3.83	3.8
single____LY_MQ_w2____stack6	0.22	0.22	0.21	0.2	0.18	0.16	0.14	0.11
single_ss_LY_MQ_w2_s1_stack6	3.9	3.9	3.89	3.87	3.86	3.83	3.81	3.78
single_ss_LY_MQ_w2_s2_stack6	4.37	4.36	4.35	4.34	4.32	4.3	4.28	4.25
single____AM_MQ_w1____stack6	1.7	1.7	1.69	1.68	1.66	1.64	1.62	1.59
single_ss_AM_MQ_w1_s1_stack6	-2.18	-2.19	-2.2	-2.21	-2.23	-2.25	-2.27	-2.3
single_ss_AM_MQ_w1_s2_stack6	1.12	1.11	1.11	1.09	1.08	1.06	1.03	1.01
single____AM_MQ_w2____stack6	0.53	0.52	0.52	0.5	0.49	0.47	0.45	0.42
single_ss_AM_MQ_w2_s1_stack6	0.81	0.81	0.8	0.78	0.77	0.75	0.72	0.7
single_ss_AM_MQ_w2_s2_stack6	3.27	3.26	3.26	3.24	3.23	3.21	3.18	3.16
single____AM_LY_w1____stack6	1.56	1.55	1.54	1.53	1.51	1.49	1.47	1.44
single_ss_AM_LY_w1_s1_stack6	-0.17	-0.18	-0.19	-0.2	-0.22	-0.24	-0.27	-0.29
single_ss_AM_LY_w1_s2_stack6	-2.69	-2.7	-2.71	-2.72	-2.74	-2.75	-2.78	-2.8
single____AM_LY_w2____stack6	0.78	0.78	0.77	0.76	0.74	0.72	0.7	0.67
single_ss_AM_LY_w2_s1_stack6	4.21	4.21	4.2	4.18	4.16	4.14	4.12	4.09
single_ss_AM_LY_w2_s2_stack6	3.83	3.83	3.82	3.8	3.79	3.77	3.74	3.71
single____M2_M1_w1____stack7	1.85	1.84	1.83	1.81	1.79	1.77	1.74	1.71
single_ss_M2_M1_w1_s1_stack7	-9.86	-9.87	-9.88	-9.9	-9.93	-9.95	-9.99	-10.02
single_ss_M2_M1_w1_s2_stack7	2.99	2.98	2.97	2.95	2.93	2.9	2.87	2.83
single____M2_M1_w2____stack7	1.15	1.14	1.13	1.11	1.09	1.06	1.03	0.99
single_ss_M2_M1_w2_s1_stack7	7.12	7.11	7.09	7.07	7.04	7.01	6.97	6.93
single_ss_M2_M1_w2_s2_stack7	7.41	7.4	7.39	7.36	7.33	7.3	7.25	7.2
single____M3_M1_w1____stack7	-2.29	-2.29	-2.3	-2.32	-2.33	-2.35	-2.38	-2.4
single_ss_M3_M1_w1_s1_stack7	-14.09	-14.1	-14.11	-14.13	-14.16	-14.19	-14.23	-14.27
single_ss_M3_M1_w1_s2_stack7	-6.08	-6.09	-6.1	-6.11	-6.13	-6.14	-6.17	-6.19
single____M3_M1_w2____stack7	-3.7	-3.71	-3.72	-3.73	-3.75	-3.77	-3.79	-3.82
single_ss_M3_M1_w2_s1_stack7	1.06	1.05	1.04	1.02	1	0.98	0.95	0.92



Table 85. Capacitance (% difference Model-Z2D)/Z2D*100)

Testcase	10.5 GHz	20.5 GHz	30.5 GHz	40.5 GHz	50.5 GHz	60.5 GHz	70.5 GHz	80.5 GHz
single_ss_M3_M1_w2_s2_stack7	2.11	2.1	2.09	2.08	2.06	2.03	2.01	1.98
single____M4_M1_w1____stack7	-0.45	-0.46	-0.47	-0.48	-0.5	-0.52	-0.54	-0.57
single_ss_M4_M1_w1_s1_stack7	-15.05	-15.06	-15.08	-15.1	-15.13	-15.17	-15.21	-15.26
single_ss_M4_M1_w1_s2_stack7	-2.56	-2.56	-2.57	-2.59	-2.6	-2.62	-2.65	-2.68
single____M4_M1_w2____stack7	-4.62	-4.62	-4.63	-4.64	-4.66	-4.68	-4.7	-4.73
single_ss_M4_M1_w2_s1_stack7	-0.9	-0.9	-0.91	-0.93	-0.95	-0.97	-1	-1.03
single_ss_M4_M1_w2_s2_stack7	1.38	1.37	1.36	1.35	1.33	1.31	1.29	1.26
single____MQ_M1_w1____stack7	-2.3	-2.31	-2.31	-2.33	-2.34	-2.36	-2.39	-2.41
single_ss_MQ_M1_w1_s1_stack7	-15.67	-15.68	-15.69	-15.71	-15.73	-15.76	-15.79	-15.82
single_ss_MQ_M1_w1_s2_stack7	-7.48	-7.49	-7.5	-7.51	-7.53	-7.55	-7.57	-7.6
single____MQ_M1_w2____stack7	-5.5	-5.51	-5.52	-5.53	-5.54	-5.56	-5.58	-5.61
single_ss_MQ_M1_w2_s1_stack7	-3.19	-3.19	-3.2	-3.22	-3.24	-3.26	-3.28	-3.31
single_ss_MQ_M1_w2_s2_stack7	-0.44	-0.45	-0.46	-0.47	-0.49	-0.51	-0.53	-0.56
single____LY_M1_w1____stack7	-0.17	-0.18	-0.18	-0.2	-0.21	-0.23	-0.26	-0.28
single_ss_LY_M1_w1_s1_stack7	-5.17	-5.18	-5.19	-5.2	-5.22	-5.24	-5.26	-5.29
single_ss_LY_M1_w1_s2_stack7	4.55	4.55	4.54	4.53	4.51	4.49	4.46	4.44
single____LY_M1_w2____stack7	-2.92	-2.93	-2.94	-2.95	-2.96	-2.98	-3	-3.03
single_ss_LY_M1_w2_s1_stack7	-1.07	-1.08	-1.09	-1.1	-1.12	-1.14	-1.16	-1.18
single_ss_LY_M1_w2_s2_stack7	1.29	1.29	1.28	1.27	1.25	1.23	1.21	1.19
single____AM_M1_w1____stack7	0.79	0.78	0.77	0.76	0.74	0.72	0.7	0.68
single_ss_AM_M1_w1_s1_stack7	-2.86	-2.87	-2.88	-2.89	-2.91	-2.93	-2.95	-2.98
single_ss_AM_M1_w1_s2_stack7	1.92	1.92	1.91	1.9	1.88	1.86	1.84	1.81
single____AM_M1_w2____stack7	-1.39	-1.4	-1.41	-1.42	-1.43	-1.45	-1.47	-1.5
single_ss_AM_M1_w2_s1_stack7	-1.63	-1.63	-1.64	-1.65	-1.67	-1.69	-1.71	-1.74
single_ss_AM_M1_w2_s2_stack7	1.57	1.56	1.55	1.54	1.52	1.51	1.48	1.46
single____M3_M2_w1____stack7	1.76	1.75	1.74	1.73	1.71	1.68	1.65	1.62
single_ss_M3_M2_w1_s1_stack7	-9.87	-9.88	-9.89	-9.91	-9.93	-9.96	-9.99	-10.03
single_ss_M3_M2_w1_s2_stack7	2.97	2.96	2.95	2.93	2.91	2.89	2.86	2.82
single____M3_M2_w2____stack7	1.15	1.14	1.13	1.11	1.08	1.06	1.02	0.98
single_ss_M3_M2_w2_s1_stack7	7.12	7.11	7.09	7.07	7.04	7.01	6.97	6.93
single_ss_M3_M2_w2_s2_stack7	7.41	7.4	7.39	7.36	7.33	7.29	7.25	7.2
single____M4_M2_w1____stack7	-2.32	-2.33	-2.34	-2.35	-2.37	-2.39	-2.41	-2.44
single_ss_M4_M2_w1_s1_stack7	-14	-14	-14.02	-14.04	-14.07	-14.1	-14.14	-14.19
single_ss_M4_M2_w1_s2_stack7	-6.04	-6.05	-6.06	-6.07	-6.08	-6.1	-6.13	-6.15
single____M4_M2_w2____stack7	-3.66	-3.67	-3.68	-3.69	-3.71	-3.73	-3.75	-3.78
single_ss_M4_M2_w2_s1_stack7	1.17	1.16	1.15	1.13	1.11	1.09	1.06	1.03

Table 85. Capacitance (% difference Model-Z2D)/Z2D*100)

Testcase	10.5 GHz	20.5 GHz	30.5 GHz	40.5 GHz	50.5 GHz	60.5 GHz	70.5 GHz	80.5 GHz
single_ss_M4_M2_w2_s2_stack7	2.19	2.19	2.18	2.16	2.14	2.12	2.09	2.06
single____MQ_M2_w1____stack7	-3.66	-3.67	-3.68	-3.69	-3.71	-3.73	-3.75	-3.77
single_ss_MQ_M2_w1_s1_stack7	-15	-15.01	-15.02	-15.04	-15.06	-15.08	-15.11	-15.15
single_ss_MQ_M2_w1_s2_stack7	-7.98	-7.98	-7.99	-8	-8.02	-8.04	-8.06	-8.09
single____MQ_M2_w2____stack7	-5.38	-5.38	-5.39	-5.4	-5.42	-5.44	-5.46	-5.49
single_ss_MQ_M2_w2_s1_stack7	-2.01	-2.02	-2.03	-2.04	-2.06	-2.08	-2.1	-2.13
single_ss_MQ_M2_w2_s2_stack7	-0.08	-0.08	-0.09	-0.11	-0.12	-0.14	-0.17	-0.19
single____LY_M2_w1____stack7	-0.4	-0.41	-0.42	-0.43	-0.44	-0.46	-0.49	-0.51
single_ss_LY_M2_w1_s1_stack7	-4.84	-4.85	-4.86	-4.88	-4.89	-4.91	-4.94	-4.96
single_ss_LY_M2_w1_s2_stack7	3.63	3.63	3.62	3.6	3.59	3.57	3.54	3.52
single____LY_M2_w2____stack7	-2.63	-2.64	-2.65	-2.66	-2.68	-2.69	-2.72	-2.74
single_ss_LY_M2_w2_s1_stack7	-0.37	-0.38	-0.39	-0.4	-0.41	-0.43	-0.45	-0.48
single_ss_LY_M2_w2_s2_stack7	1.45	1.44	1.44	1.42	1.41	1.39	1.37	1.34
single____AM_M2_w1____stack7	0.82	0.81	0.8	0.79	0.77	0.75	0.73	0.71
single_ss_AM_M2_w1_s1_stack7	-2.76	-2.76	-2.77	-2.79	-2.8	-2.82	-2.85	-2.87
single_ss_AM_M2_w1_s2_stack7	1.78	1.78	1.77	1.76	1.74	1.72	1.7	1.67
single____AM_M2_w2____stack7	-1.14	-1.14	-1.15	-1.16	-1.18	-1.2	-1.22	-1.24
single_ss_AM_M2_w2_s1_stack7	-1.23	-1.23	-1.24	-1.26	-1.27	-1.29	-1.31	-1.34
single_ss_AM_M2_w2_s2_stack7	1.83	1.82	1.82	1.8	1.79	1.77	1.75	1.72
single____M4_M3_w1____stack7	1.76	1.75	1.74	1.73	1.71	1.68	1.65	1.62
single_ss_M4_M3_w1_s1_stack7	-9.78	-9.79	-9.8	-9.82	-9.84	-9.87	-9.91	-9.94
single_ss_M4_M3_w1_s2_stack7	2.99	2.99	2.97	2.96	2.94	2.91	2.88	2.84
single____M4_M3_w2____stack7	1.15	1.14	1.13	1.11	1.08	1.06	1.02	0.98
single_ss_M4_M3_w2_s1_stack7	7.14	7.14	7.12	7.1	7.07	7.04	7	6.95
single_ss_M4_M3_w2_s2_stack7	7.43	7.42	7.4	7.38	7.35	7.31	7.27	7.22
single____MQ_M3_w1____stack7	-4.51	-4.52	-4.53	-4.54	-4.55	-4.57	-4.6	-4.62
single_ss_MQ_M3_w1_s1_stack7	-13.77	-13.78	-13.79	-13.8	-13.82	-13.85	-13.88	-13.91
single_ss_MQ_M3_w1_s2_stack7	-9.67	-9.67	-9.68	-9.69	-9.7	-9.72	-9.74	-9.77
single____MQ_M3_w2____stack7	-5.16	-5.17	-5.18	-5.19	-5.21	-5.23	-5.25	-5.28
single_ss_MQ_M3_w2_s1_stack7	-0.69	-0.7	-0.71	-0.72	-0.74	-0.76	-0.79	-0.82
single_ss_MQ_M3_w2_s2_stack7	0.23	0.22	0.21	0.2	0.18	0.16	0.13	0.1
single____LY_M3_w1____stack7	-0.53	-0.53	-0.54	-0.56	-0.57	-0.59	-0.62	-0.64
single_ss_LY_M3_w1_s1_stack7	-4.46	-4.46	-4.47	-4.49	-4.51	-4.53	-4.55	-4.58
single_ss_LY_M3_w1_s2_stack7	2.57	2.57	2.56	2.54	2.53	2.51	2.48	2.46
single____LY_M3_w2____stack7	-2.28	-2.29	-2.3	-2.31	-2.32	-2.34	-2.36	-2.39
single_ss_LY_M3_w2_s1_stack7	0.41	0.4	0.39	0.38	0.37	0.35	0.32	0.3



Table 85. Capacitance (% difference Model-Z2D)/Z2D*100)

Testcase	10.5 GHz	20.5 GHz	30.5 GHz	40.5 GHz	50.5 GHz	60.5 GHz	70.5 GHz	80.5 GHz
single_ss_LY_M3_w2_s2_stack7	1.65	1.65	1.64	1.63	1.61	1.59	1.57	1.54
single___AM_M3_w1___stack7	0.9	0.89	0.88	0.87	0.85	0.84	0.81	0.79
single_ss_AM_M3_w1_s1_stack7	-2.64	-2.64	-2.65	-2.67	-2.68	-2.7	-2.72	-2.75
single_ss_AM_M3_w1_s2_stack7	1.62	1.62	1.61	1.6	1.58	1.56	1.54	1.51
single___AM_M3_w2___stack7	-0.85	-0.86	-0.87	-0.88	-0.89	-0.91	-0.93	-0.96
single_ss_AM_M3_w2_s1_stack7	-0.8	-0.8	-0.81	-0.83	-0.84	-0.86	-0.88	-0.91
single_ss_AM_M3_w2_s2_stack7	2.11	2.1	2.1	2.08	2.07	2.05	2.03	2
single___MQ_M4_w1___stack7	-3.48	-3.49	-3.5	-3.51	-3.53	-3.55	-3.57	-3.6
single_ss_MQ_M4_w1_s1_stack7	-11.16	-11.17	-11.18	-11.19	-11.21	-11.24	-11.26	-11.3
single_ss_MQ_M4_w1_s2_stack7	-6.65	-6.66	-6.67	-6.68	-6.7	-6.72	-6.74	-6.77
single___MQ_M4_w2___stack7	-4.28	-4.29	-4.3	-4.32	-4.34	-4.36	-4.39	-4.42
single_ss_MQ_M4_w2_s1_stack7	1.13	1.12	1.11	1.09	1.07	1.04	1.01	0.98
single_ss_MQ_M4_w2_s2_stack7	1.42	1.41	1.4	1.38	1.36	1.33	1.3	1.27
single___LY_M4_w1___stack7	-0.52	-0.53	-0.53	-0.55	-0.56	-0.58	-0.61	-0.63
single_ss_LY_M4_w1_s1_stack7	-3.98	-3.99	-4	-4.01	-4.03	-4.05	-4.07	-4.1
single_ss_LY_M4_w1_s2_stack7	1.36	1.35	1.34	1.33	1.31	1.29	1.27	1.24
single___LY_M4_w2___stack7	-1.82	-1.82	-1.83	-1.85	-1.86	-1.88	-1.9	-1.93
single_ss_LY_M4_w2_s1_stack7	1.29	1.28	1.27	1.26	1.24	1.22	1.2	1.17
single_ss_LY_M4_w2_s2_stack7	1.94	1.93	1.92	1.91	1.9	1.88	1.86	1.83
single___AM_M4_w1___stack7	1.03	1.03	1.02	1.01	0.99	0.97	0.95	0.92
single_ss_AM_M4_w1_s1_stack7	-2.5	-2.51	-2.52	-2.53	-2.55	-2.57	-2.59	-2.62
single_ss_AM_M4_w1_s2_stack7	1.44	1.43	1.42	1.41	1.39	1.38	1.35	1.33
single___AM_M4_w2___stack7	-0.54	-0.55	-0.56	-0.57	-0.58	-0.6	-0.62	-0.65
single_ss_AM_M4_w2_s1_stack7	-0.32	-0.33	-0.34	-0.35	-0.36	-0.38	-0.41	-0.43
single_ss_AM_M4_w2_s2_stack7	2.38	2.38	2.37	2.36	2.34	2.32	2.3	2.27
single___LY_MQ_w1___stack7	0.74	0.73	0.72	0.71	0.69	0.67	0.65	0.62
single_ss_LY_MQ_w1_s1_stack7	-2.67	-2.68	-2.69	-2.71	-2.73	-2.75	-2.77	-2.8
single_ss_LY_MQ_w1_s2_stack7	3.92	3.91	3.9	3.89	3.87	3.85	3.83	3.8
single___LY_MQ_w2___stack7	0.22	0.22	0.21	0.2	0.18	0.16	0.14	0.11
single_ss_LY_MQ_w2_s1_stack7	3.9	3.9	3.89	3.87	3.86	3.83	3.81	3.78
single_ss_LY_MQ_w2_s2_stack7	4.37	4.36	4.35	4.34	4.32	4.3	4.28	4.25
single___AM_MQ_w1___stack7	1.7	1.7	1.69	1.68	1.66	1.64	1.62	1.59
single_ss_AM_MQ_w1_s1_stack7	-2.18	-2.19	-2.2	-2.21	-2.23	-2.25	-2.27	-2.3
single_ss_AM_MQ_w1_s2_stack7	1.12	1.11	1.11	1.09	1.08	1.06	1.03	1.01
single___AM_MQ_w2___stack7	0.53	0.52	0.52	0.5	0.49	0.47	0.45	0.42
single_ss_AM_MQ_w2_s1_stack7	0.81	0.81	0.8	0.78	0.77	0.75	0.72	0.7

Table 85. Capacitance (% difference Model-Z2D)/Z2D*100)

Testcase	10.5 GHz	20.5 GHz	30.5 GHz	40.5 GHz	50.5 GHz	60.5 GHz	70.5 GHz	80.5 GHz
single_ss_AM_MQ_w2_s2_stack7	3.27	3.26	3.26	3.24	3.23	3.21	3.18	3.16
single____AM_LY_w1____stack7	1.56	1.55	1.54	1.53	1.51	1.49	1.47	1.44
single_ss_AM_LY_w1_s1_stack7	-0.17	-0.18	-0.19	-0.2	-0.22	-0.24	-0.27	-0.29
single_ss_AM_LY_w1_s2_stack7	-2.69	-2.7	-2.71	-2.72	-2.74	-2.75	-2.78	-2.8
single____AM_LY_w2____stack7	0.78	0.78	0.77	0.76	0.74	0.72	0.7	0.67
single_ss_AM_LY_w2_s1_stack7	4.21	4.21	4.2	4.18	4.16	4.14	4.12	4.09
single_ss_AM_LY_w2_s2_stack7	3.83	3.83	3.82	3.8	3.79	3.77	3.74	3.71

Table 86. Resistance (% difference Model-Z2D)/Z2D*100)

Testcase	10.5 GHz	20.5 GHz	30.5 GHz	40.5 GHz	50.5 GHz	60.5 GHz	70.5 GHz	80.5 GHz
single____M2_M1_w1____stack5	-2.46	-2.44	-2.42	-2.38	-2.34	-2.29	-2.22	-2.14
single_ss_M2_M1_w1_s1_stack5	1.71	1.32	0.73	0.02	-0.73	-1.46	-2.13	-2.7
single_ss_M2_M1_w1_s2_stack5	-7.01	-6.96	-6.89	-6.77	-6.62	-6.44	-6.22	-5.96
single____M2_M1_w2____stack5	-0.41	-0.35	-0.21	0.01	0.3	0.66	1.08	1.55
single_ss_M2_M1_w2_s1_stack5	-0.11	0.05	0.41	0.93	1.59	2.39	3.3	4.31
single_ss_M2_M1_w2_s2_stack5	-3.58	-2.68	-1.16	0.91	3.45	6.38	9.61	13.05
single____MQ_M1_w1____stack5	-2.27	-2.26	-2.24	-2.2	-2.14	-2.05	-1.93	-1.78
single_ss_MQ_M1_w1_s1_stack5	3.38	0.44	-1.8	-2.96	-3.26	-2.96	-2.23	-1.17
single_ss_MQ_M1_w1_s2_stack5	-3.02	-3.23	-3.45	-3.64	-3.81	-3.96	-4.11	-4.23
single____MQ_M1_w2____stack5	-1.25	-1.48	-1.55	-1.48	-1.17	-0.63	0.15	1.14
single_ss_MQ_M1_w2_s1_stack5	0.63	1.08	2.24	4.11	6.58	9.49	12.7	15.98
single_ss_MQ_M1_w2_s2_stack5	-2.61	-0.6	2.84	7.32	12.44	17.81	23.12	28.16
single____LY_M1_w1____stack5	-2.06	-1.05	0.76	3.3	6.16	9.24	12.29	15.06
single_ss_LY_M1_w1_s1_stack5	0.91	2.23	5.54	9.55	13.13	15.96	18.03	19.25
single_ss_LY_M1_w1_s2_stack5	-2.96	3.6	11.84	19.83	26.21	30.81	33.83	35.39
single____LY_M1_w2____stack5	-3.21	1.28	9.81	19.93	29.62	37.88	44.39	49.16
single_ss_LY_M1_w2_s1_stack5	17.26	44.85	60.41	65.11	63.97	60.26	55.74	50.92
single_ss_LY_M1_w2_s2_stack5	21.65	61.37	77.89	81.72	80.42	77.07	72.96	68.5
single____AM_M1_w1____stack5	-2.88	9.24	20.57	27.02	29.13	29.24	27.93	25.88
single_ss_AM_M1_w1_s1_stack5	2.42	10.12	13.73	13.36	10.75	8.27	5.95	3.93
single_ss_AM_M1_w1_s2_stack5	13.15	28.16	31.39	28.36	22.94	17.95	13.25	9
single____AM_M1_w2____stack5	13.61	48.1	66.28	72.68	73.18	71.64	68.92	65.75
single_ss_AM_M1_w2_s1_stack5	69.93	43.39	26.3	16.62	10.48	7.11	5.13	4.03
single_ss_AM_M1_w2_s2_stack5	69.48	59.4	47.76	37.77	29.75	23.7	18.69	14.4
single____MQ_M2_w1____stack5	-3.78	-3.75	-3.71	-3.67	-3.59	-3.5	-3.38	-3.24
single_ss_MQ_M2_w1_s1_stack5	0.44	-0.66	-1.81	-2.72	-3.3	-3.59	-3.64	-3.5



Table 86. Resistance (% difference Model-Z2D)/Z2D*100)

Testcase	10.5 GHz	20.5 GHz	30.5 GHz	40.5 GHz	50.5 GHz	60.5 GHz	70.5 GHz	80.5 GHz
single_ss_MQ_M2_w1_s2_stack5	-6.25	-6.28	-6.26	-6.19	-6.08	-5.92	-5.71	-5.46
single____MQ_M2_w2____stack5	-0.95	-1	-0.91	-0.66	-0.22	0.42	1.26	2.3
single_ss_MQ_M2_w2_s1_stack5	-0.6	0.16	1.61	3.64	6.09	8.83	11.73	14.64
single_ss_MQ_M2_w2_s2_stack5	-3.43	-0.55	3.98	9.56	15.59	21.58	27.16	32.13
single____LY_M2_w1____stack5	-2.38	-1.8	-0.56	1.38	3.68	6.31	9.02	11.56
single_ss_LY_M2_w1_s1_stack5	0.53	2.02	5.52	9.69	13.36	16.22	18.29	19.49
single_ss_LY_M2_w1_s2_stack5	-4.52	0.75	7.6	14.5	20.24	24.63	27.71	29.53
single____LY_M2_w2____stack5	-3.17	1.28	9.79	19.77	29.13	36.9	42.83	46.99
single_ss_LY_M2_w2_s1_stack5	15.78	42.64	58.27	63.39	62.68	59.31	55.02	50.37
single_ss_LY_M2_w2_s2_stack5	23.88	63	77.33	79.53	77.21	73.19	68.6	63.82
single____AM_M2_w1____stack5	-3.11	8.77	19.79	25.91	27.75	27.66	26.23	24.08
single_ss_AM_M2_w1_s1_stack5	2.42	10.3	13.86	13.43	10.8	8.33	6.04	4.07
single_ss_AM_M2_w1_s2_stack5	10.53	24.76	28.64	26.34	21.46	16.84	12.42	8.38
single____AM_M2_w2____stack5	16.19	50.8	66.72	71.09	70.12	67.59	64.17	60.47
single_ss_AM_M2_w2_s1_stack5	68.26	42.41	25.63	16.17	10.21	7	5.15	4.16
single_ss_AM_M2_w2_s2_stack5	68.83	58.53	46.75	36.69	28.63	22.57	17.56	13.3
single____LY_MQ_w1____stack5	-2.22	-1.93	-1.07	0.43	2.2	4.21	6.22	8.02
single_ss_LY_MQ_w1_s1_stack5	-0.99	4.57	12.16	19.05	23.86	26.66	27.96	28.07
single_ss_LY_MQ_w1_s2_stack5	-3.81	3.59	12.45	20.51	26.41	30.19	32.2	32.73
single____LY_MQ_w2____stack5	-0.82	8.11	18.96	27.49	32.44	34.26	33.87	32.05
single_ss_LY_MQ_w2_s1_stack5	14.81	38.74	48.8	49.14	45.11	39.58	33.92	28.47
single_ss_LY_MQ_w2_s2_stack5	37.99	70.01	72.42	65.9	57.52	49.16	41.37	34.25
single____AM_MQ_w1____stack5	-0.46	12.48	21.34	24.21	23.09	20.78	17.75	14.52
single_ss_AM_MQ_w1_s1_stack5	7.22	17.85	19.5	16.97	12.97	9.75	7.12	5.05
single_ss_AM_MQ_w1_s2_stack5	4.49	15.45	20.04	19.19	15.56	11.84	8.11	4.62
single____AM_MQ_w2____stack5	35.05	57.56	56.73	50.08	42.22	35.3	29	23.39
single_ss_AM_MQ_w2_s1_stack5	53.47	29.14	15.81	9.77	6.86	6.16	6.24	6.6
single_ss_AM_MQ_w2_s2_stack5	65.91	51.75	37.66	26.21	17.38	11	5.94	1.84
single____AM_LY_w1____stack5	-0.8	10.24	13.65	12.25	9.06	6.23	3.74	1.7
single_ss_AM_LY_w1_s1_stack5	14.79	26.26	24.19	18.99	13.56	9.65	6.73	4.59
single_ss_AM_LY_w1_s2_stack5	-5.11	3.09	6.78	6.54	4.55	2.82	1.28	0.06
single____AM_LY_w2____stack5	30.98	14.08	3.97	0.29	-0.54	0.3	1.37	2.22
single_ss_AM_LY_w2_s1_stack5	31.31	8.9	1.07	-0.28	0.27	1.63	2.65	3.15
single_ss_AM_LY_w2_s2_stack5	32.95	8.87	0.36	-1.72	-1.52	-0.29	0.68	1.15
single____M2_M1_w1____stack6	-2.46	-2.44	-2.42	-2.38	-2.34	-2.29	-2.22	-2.14
single_ss_M2_M1_w1_s1_stack6	1.71	1.32	0.73	0.02	-0.73	-1.46	-2.13	-2.7

Table 86. Resistance (% difference Model-Z2D)/Z2D*100)

Testcase	10.5 GHz	20.5 GHz	30.5 GHz	40.5 GHz	50.5 GHz	60.5 GHz	70.5 GHz	80.5 GHz
single_ss_M2_M1_w1_s2_stack6	-7.01	-6.96	-6.89	-6.77	-6.62	-6.44	-6.22	-5.96
single____M2_M1_w2____stack6	-0.41	-0.35	-0.21	0.01	0.3	0.66	1.08	1.55
single_ss_M2_M1_w2_s1_stack6	-0.11	0.05	0.41	0.93	1.59	2.39	3.3	4.31
single_ss_M2_M1_w2_s2_stack6	-3.58	-2.68	-1.16	0.91	3.45	6.38	9.61	13.05
single____M3_M1_w1____stack6	-0.89	-0.88	-0.86	-0.83	-0.79	-0.74	-0.67	-0.59
single_ss_M3_M1_w1_s1_stack6	5.84	4.22	2.13	0.08	-1.62	-2.85	-3.61	-3.94
single_ss_M3_M1_w1_s2_stack6	-2.87	-2.98	-3.14	-3.29	-3.42	-3.51	-3.57	-3.58
single____M3_M1_w2____stack6	-0.62	-0.72	-0.72	-0.64	-0.5	-0.29	-0.04	0.29
single_ss_M3_M1_w2_s1_stack6	1.22	1.39	1.84	2.53	3.41	4.47	5.67	6.98
single_ss_M3_M1_w2_s2_stack6	-2.42	-1.79	-0.61	1.06	3.17	5.66	8.44	11.44
single____MQ_M1_w1____stack6	-1.38	-1.35	-1.28	-1.16	-0.99	-0.75	-0.46	-0.11
single_ss_MQ_M1_w1_s1_stack6	4.53	-0.1	-2.65	-3.33	-2.82	-1.53	0.29	2.5
single_ss_MQ_M1_w1_s2_stack6	-0.89	-1.72	-2.28	-2.5	-2.47	-2.25	-1.89	-1.42
single____MQ_M1_w2____stack6	-1.51	-1.77	-1.67	-1.28	-0.6	0.35	1.56	3
single_ss_MQ_M1_w2_s1_stack6	2.01	2.39	3.79	6.18	9.37	13	16.8	20.41
single_ss_MQ_M1_w2_s2_stack6	-1.39	0.41	3.78	8.4	13.8	19.53	25.22	30.58
single____LY_M1_w1____stack6	-1.52	0.15	2.82	6.24	9.84	13.46	16.84	19.75
single_ss_LY_M1_w1_s1_stack6	0.98	3.19	7.45	12.18	16.14	19.06	21.02	22.03
single_ss_LY_M1_w1_s2_stack6	-1.09	6.86	16.51	25.49	32.29	36.88	39.6	40.73
single____LY_M1_w2____stack6	-2.92	2.73	12.45	23.4	33.46	41.73	48	52.4
single_ss_LY_M1_w2_s1_stack6	18.73	46.43	60.53	63.62	61.24	56.71	51.68	46.55
single_ss_LY_M1_w2_s2_stack6	21.01	60.68	78.28	82.79	81.79	78.52	74.37	69.81
single____AM_M1_w1____stack6	-1.67	11.34	22.71	28.74	30.32	29.98	28.31	25.97
single_ss_AM_M1_w1_s1_stack6	2.9	10.87	14.32	13.72	10.94	8.33	5.91	3.81
single_ss_AM_M1_w1_s2_stack6	14.92	30.04	32.75	29.26	23.51	18.29	13.43	9.06
single____AM_M1_w2____stack6	14.63	49.32	66.99	72.89	73.04	71.25	68.38	65.11
single_ss_AM_M1_w2_s1_stack6	69.18	41.97	24.99	15.6	9.81	6.77	5.08	4.23
single_ss_AM_M1_w2_s2_stack6	71.65	61.24	49.1	38.71	30.42	24.18	19.02	14.61
single____M3_M2_w1____stack6	-2.92	-2.91	-2.9	-2.88	-2.85	-2.81	-2.77	-2.71
single_ss_M3_M2_w1_s1_stack6	1.56	1.11	0.43	-0.37	-1.21	-2.01	-2.71	-3.3
single_ss_M3_M2_w1_s2_stack6	-6.57	-6.51	-6.44	-6.33	-6.18	-6.01	-5.8	-5.56
single____M3_M2_w2____stack6	-0.38	-0.3	-0.1	0.2	0.57	1.03	1.55	2.13
single_ss_M3_M2_w2_s1_stack6	-0.05	0.17	0.61	1.24	2.03	2.97	4.03	5.19
single_ss_M3_M2_w2_s2_stack6	-3.32	-2.28	-0.56	1.77	4.61	7.84	11.35	15.03
single____MQ_M2_w1____stack6	-1.99	-2	-1.98	-1.95	-1.9	-1.82	-1.71	-1.57
single_ss_MQ_M2_w1_s1_stack6	2.87	-0.34	-2.58	-3.52	-3.49	-2.77	-1.57	0

Table 86. Resistance (% difference Model-Z2D)/Z2D*100)

Testcase	10.5 GHz	20.5 GHz	30.5 GHz	40.5 GHz	50.5 GHz	60.5 GHz	70.5 GHz	80.5 GHz
single_ss_MQ_M2_w1_s2_stack6	-2.88	-3.19	-3.47	-3.7	-3.88	-4.02	-4.13	-4.23
single____MQ_M2_w2____stack6	-1.21	-1.33	-1.23	-0.93	-0.36	0.45	1.48	2.7
single_ss_MQ_M2_w2_s1_stack6	0.75	1.38	2.81	4.99	7.77	10.92	14.28	17.57
single_ss_MQ_M2_w2_s2_stack6	-2.34	-0.03	3.81	8.74	14.23	19.85	25.24	30.18
single____LY_M2_w1____stack6	-1.82	-0.67	1.34	4.08	7.09	10.24	13.28	15.98
single_ss_LY_M2_w1_s1_stack6	0.66	3.27	7.96	13	17.13	20.08	22	22.91
single_ss_LY_M2_w1_s2_stack6	-2.54	4.05	12.29	20.22	26.49	30.99	33.88	35.33
single____LY_M2_w2____stack6	-2.85	2.83	12.58	23.36	33.05	40.79	46.44	50.19
single_ss_LY_M2_w2_s1_stack6	17.28	44.32	58.5	61.96	59.95	55.69	50.84	45.85
single_ss_LY_M2_w2_s2_stack6	22.77	62.04	77.68	80.66	78.68	74.76	70.16	65.29
single____AM_M2_w1____stack6	-1.91	10.83	21.85	27.54	28.86	28.33	26.56	24.15
single_ss_AM_M2_w1_s1_stack6	3.01	11.21	14.59	13.89	11.04	8.41	6	3.94
single_ss_AM_M2_w1_s2_stack6	12.5	26.96	30.28	27.44	22.18	17.28	12.66	8.47
single____AM_M2_w2____stack6	17.3	51.96	67.3	71.18	69.89	67.15	63.6	59.82
single_ss_AM_M2_w2_s1_stack6	67.39	40.82	24.18	15.06	9.48	6.63	5.1	4.37
single_ss_AM_M2_w2_s2_stack6	70.9	60.29	48.02	37.57	29.24	23	17.85	13.48
single____MQ_M3_w1____stack6	-3.78	-3.75	-3.71	-3.67	-3.59	-3.5	-3.38	-3.24
single_ss_MQ_M3_w1_s1_stack6	0.44	-0.66	-1.8	-2.72	-3.3	-3.58	-3.63	-3.48
single_ss_MQ_M3_w1_s2_stack6	-6.25	-6.27	-6.25	-6.18	-6.08	-5.92	-5.71	-5.45
single____MQ_M3_w2____stack6	-0.95	-1	-0.91	-0.66	-0.22	0.42	1.26	2.3
single_ss_MQ_M3_w2_s1_stack6	-0.6	0.16	1.61	3.64	6.09	8.83	11.74	14.65
single_ss_MQ_M3_w2_s2_stack6	-3.43	-0.55	3.98	9.56	15.6	21.58	27.16	32.13
single____LY_M3_w1____stack6	-2.38	-1.8	-0.56	1.38	3.68	6.31	9.02	11.56
single_ss_LY_M3_w1_s1_stack6	0.53	2.03	5.53	9.7	13.38	16.24	18.31	19.51
single_ss_LY_M3_w1_s2_stack6	-4.52	0.75	7.61	14.51	20.25	24.65	27.73	29.55
single____LY_M3_w2____stack6	-3.17	1.28	9.79	19.77	29.13	36.9	42.83	46.99
single_ss_LY_M3_w2_s1_stack6	15.79	42.65	58.28	63.4	62.68	59.31	55.02	50.37
single_ss_LY_M3_w2_s2_stack6	23.88	63	77.33	79.53	77.21	73.19	68.61	63.82
single____AM_M3_w1____stack6	-3.11	8.77	19.79	25.91	27.75	27.66	26.23	24.08
single_ss_AM_M3_w1_s1_stack6	2.43	10.3	13.87	13.44	10.8	8.33	6.04	4.07
single_ss_AM_M3_w1_s2_stack6	10.54	24.77	28.65	26.34	21.47	16.84	12.42	8.38
single____AM_M3_w2____stack6	16.19	50.8	66.72	71.09	70.12	67.59	64.17	60.47
single_ss_AM_M3_w2_s1_stack6	68.27	42.41	25.63	16.16	10.21	7	5.14	4.15
single_ss_AM_M3_w2_s2_stack6	68.83	58.53	46.75	36.69	28.63	22.57	17.56	13.3
single____LY_MQ_w1____stack6	-2.22	-1.93	-1.07	0.43	2.2	4.21	6.22	8.02
single_ss_LY_MQ_w1_s1_stack6	-0.99	4.57	12.16	19.05	23.86	26.66	27.96	28.07

Table 86. Resistance (% difference Model-Z2D)/Z2D*100)

Testcase	10.5 GHz	20.5 GHz	30.5 GHz	40.5 GHz	50.5 GHz	60.5 GHz	70.5 GHz	80.5 GHz
single_ss_LY_MQ_w1_s2_stack6	-3.81	3.59	12.45	20.51	26.41	30.19	32.2	32.73
single____LY_MQ_w2____stack6	-0.82	8.11	18.96	27.49	32.44	34.26	33.87	32.05
single_ss_LY_MQ_w2_s1_stack6	14.81	38.74	48.8	49.14	45.11	39.58	33.92	28.47
single_ss_LY_MQ_w2_s2_stack6	37.99	70.01	72.42	65.9	57.52	49.16	41.37	34.25
single____AM_MQ_w1____stack6	-0.46	12.48	21.34	24.21	23.09	20.78	17.75	14.52
single_ss_AM_MQ_w1_s1_stack6	7.22	17.85	19.5	16.97	12.97	9.75	7.12	5.05
single_ss_AM_MQ_w1_s2_stack6	4.49	15.45	20.04	19.19	15.56	11.84	8.11	4.62
single____AM_MQ_w2____stack6	35.05	57.56	56.73	50.08	42.22	35.3	29	23.39
single_ss_AM_MQ_w2_s1_stack6	53.47	29.14	15.81	9.77	6.86	6.16	6.24	6.6
single_ss_AM_MQ_w2_s2_stack6	65.91	51.75	37.66	26.21	17.38	11	5.94	1.84
single____AM_LY_w1____stack6	-0.8	10.24	13.65	12.25	9.06	6.23	3.74	1.7
single_ss_AM_LY_w1_s1_stack6	14.79	26.26	24.19	18.99	13.56	9.65	6.73	4.59
single_ss_AM_LY_w1_s2_stack6	-5.11	3.09	6.78	6.54	4.55	2.82	1.28	0.06
single____AM_LY_w2____stack6	30.98	14.08	3.97	0.29	-0.54	0.3	1.37	2.22
single_ss_AM_LY_w2_s1_stack6	31.31	8.9	1.07	-0.28	0.27	1.63	2.65	3.15
single_ss_AM_LY_w2_s2_stack6	32.95	8.87	0.36	-1.72	-1.52	-0.29	0.68	1.15
single____M2_M1_w1____stack7	-2.46	-2.44	-2.42	-2.38	-2.34	-2.29	-2.22	-2.14
single_ss_M2_M1_w1_s1_stack7	1.71	1.32	0.73	0.02	-0.73	-1.47	-2.13	-2.71
single_ss_M2_M1_w1_s2_stack7	-7.01	-6.96	-6.89	-6.77	-6.62	-6.44	-6.22	-5.96
single____M2_M1_w2____stack7	-0.41	-0.35	-0.21	0.01	0.3	0.66	1.08	1.55
single_ss_M2_M1_w2_s1_stack7	-0.11	0.05	0.41	0.92	1.59	2.38	3.29	4.3
single_ss_M2_M1_w2_s2_stack7	-3.58	-2.68	-1.16	0.9	3.44	6.37	9.6	13.04
single____M3_M1_w1____stack7	-0.89	-0.88	-0.86	-0.83	-0.79	-0.74	-0.67	-0.59
single_ss_M3_M1_w1_s1_stack7	5.83	4.21	2.13	0.08	-1.62	-2.86	-3.62	-3.96
single_ss_M3_M1_w1_s2_stack7	-2.87	-2.98	-3.14	-3.29	-3.42	-3.51	-3.57	-3.58
single____M3_M1_w2____stack7	-0.62	-0.72	-0.72	-0.64	-0.5	-0.29	-0.04	0.29
single_ss_M3_M1_w2_s1_stack7	1.21	1.38	1.82	2.49	3.36	4.4	5.58	6.88
single_ss_M3_M1_w2_s2_stack7	-2.42	-1.8	-0.63	1.03	3.14	5.61	8.38	11.36
single____M4_M1_w1____stack7	-0.45	-0.43	-0.4	-0.34	-0.25	-0.14	0.01	0.18
single_ss_M4_M1_w1_s1_stack7	7.62	4.88	1.77	-0.83	-2.61	-3.56	-3.8	-3.45
single_ss_M4_M1_w1_s2_stack7	-0.86	-1.22	-1.67	-2.09	-2.4	-2.6	-2.66	-2.61
single____M4_M1_w2____stack7	-0.88	-1.11	-1.22	-1.15	-0.97	-0.68	-0.29	0.19
single_ss_M4_M1_w2_s1_stack7	2.55	2.92	3.77	4.98	6.45	8.1	9.84	11.59
single_ss_M4_M1_w2_s2_stack7	-1.25	-0.69	0.53	2.32	4.65	7.4	10.5	13.85
single____MQ_M1_w1____stack7	-0.92	-0.83	-0.66	-0.38	-0.01	0.47	1.06	1.74
single_ss_MQ_M1_w1_s1_stack7	4.92	-0.81	-3.15	-3.17	-1.82	0.39	3.19	6.41



Table 86. Resistance (% difference Model-Z2D)/Z2D*100)

Testcase	10.5 GHz	20.5 GHz	30.5 GHz	40.5 GHz	50.5 GHz	60.5 GHz	70.5 GHz	80.5 GHz
single_ss_MQ_M1_w1_s2_stack7	0.35	-1.18	-1.94	-1.96	-1.45	-0.57	0.6	1.99
single____MQ_M1_w2____stack7	-1.77	-1.95	-1.54	-0.7	0.52	2.08	3.93	5.98
single_ss_MQ_M1_w2_s1_stack7	3.43	3.99	5.97	9.11	12.94	16.87	20.58	23.73
single_ss_MQ_M1_w2_s2_stack7	-0.17	1.58	5.33	10.64	16.92	23.48	29.86	35.73
single____LY_M1_w1____stack7	-0.98	1.44	5.09	9.45	13.81	17.93	21.57	24.51
single_ss_LY_M1_w1_s1_stack7	1.05	4.13	9.28	14.63	18.89	21.84	23.67	24.45
single_ss_LY_M1_w1_s2_stack7	0.61	10.1	21.27	31.21	38.34	42.8	45.12	45.73
single____LY_M1_w2____stack7	-2.6	4.26	15.17	26.87	37.2	45.38	51.34	55.34
single_ss_LY_M1_w2_s1_stack7	20.3	48.12	60.6	62.07	58.52	53.25	47.78	42.42
single_ss_LY_M1_w2_s2_stack7	20.76	60.3	78.71	83.72	82.91	79.66	75.44	70.78
single____AM_M1_w1____stack7	-0.41	13.52	24.88	30.43	31.46	30.66	28.64	26.04
single_ss_AM_M1_w1_s1_stack7	3.35	11.55	14.86	14.06	11.11	8.38	5.87	3.71
single_ss_AM_M1_w1_s2_stack7	16.58	31.79	33.99	30.06	24	18.56	13.55	9.07
single____AM_M1_w2____stack7	15.64	50.49	67.63	73.04	72.84	70.83	67.82	64.43
single_ss_AM_M1_w2_s1_stack7	68.37	40.6	23.78	14.71	9.25	6.53	5.12	4.5
single_ss_AM_M1_w2_s2_stack7	73.61	62.86	50.22	39.46	30.92	24.49	19.2	14.7
single____M3_M2_w1____stack7	-2.92	-2.91	-2.9	-2.88	-2.85	-2.81	-2.77	-2.71
single_ss_M3_M2_w1_s1_stack7	1.56	1.11	0.43	-0.37	-1.21	-2.01	-2.72	-3.31
single_ss_M3_M2_w1_s2_stack7	-6.57	-6.52	-6.44	-6.33	-6.18	-6.01	-5.8	-5.56
single____M3_M2_w2____stack7	-0.38	-0.3	-0.1	0.2	0.57	1.03	1.55	2.13
single_ss_M3_M2_w2_s1_stack7	-0.05	0.17	0.6	1.23	2.03	2.96	4.02	5.17
single_ss_M3_M2_w2_s2_stack7	-3.32	-2.29	-0.56	1.77	4.6	7.83	11.34	15.02
single____M4_M2_w1____stack7	-0.76	-0.76	-0.75	-0.73	-0.7	-0.66	-0.61	-0.54
single_ss_M4_M2_w1_s1_stack7	5.48	3.75	1.56	-0.54	-2.22	-3.39	-4.03	-4.21
single_ss_M4_M2_w1_s2_stack7	-2.57	-2.73	-2.93	-3.13	-3.3	-3.43	-3.52	-3.56
single____M4_M2_w2____stack7	-0.61	-0.68	-0.65	-0.51	-0.3	0	0.33	0.76
single_ss_M4_M2_w2_s1_stack7	1.21	1.47	2.06	2.91	4	5.26	6.66	8.15
single_ss_M4_M2_w2_s2_stack7	-2.24	-1.49	-0.12	1.8	4.2	6.98	10.04	13.29
single____MQ_M2_w1____stack7	-1.22	-1.2	-1.13	-1.02	-0.85	-0.6	-0.31	0.05
single_ss_MQ_M2_w1_s1_stack7	3.79	-0.99	-3.29	-3.52	-2.43	-0.5	2.03	4.99
single_ss_MQ_M2_w1_s2_stack7	-0.98	-1.96	-2.57	-2.77	-2.67	-2.34	-1.85	-1.21
single____MQ_M2_w2____stack7	-1.48	-1.63	-1.32	-0.66	0.32	1.59	3.09	4.78
single_ss_MQ_M2_w2_s1_stack7	2.09	2.74	4.51	7.3	10.81	14.59	18.36	21.78
single_ss_MQ_M2_w2_s2_stack7	-1.18	0.93	4.78	9.93	15.8	21.85	27.65	32.94
single____LY_M2_w1____stack7	-1.29	0.55	3.46	7.09	10.84	14.5	17.85	20.64
single_ss_LY_M2_w1_s1_stack7	0.79	4.5	10.3	16.09	20.54	23.5	25.21	25.82

Table 86. Resistance (% difference Model-Z2D)/Z2D*100)

Testcase	10.5 GHz	20.5 GHz	30.5 GHz	40.5 GHz	50.5 GHz	60.5 GHz	70.5 GHz	80.5 GHz
single_ss_LY_M2_w1_s2_stack7	-0.75	7.4	17.2	26.22	32.97	37.45	40.03	41
single____LY_M2_w2____stack7	-2.5	4.48	15.45	26.97	36.88	44.48	49.78	53.09
single_ss_LY_M2_w2_s1_stack7	18.92	46.16	58.7	60.43	57.15	52.1	46.77	41.52
single_ss_LY_M2_w2_s2_stack7	22.15	61.38	78.01	81.6	79.85	75.99	71.35	66.37
single____AM_M2_w1____stack7	-0.67	12.95	23.94	29.15	29.93	28.98	26.85	24.19
single_ss_AM_M2_w1_s1_stack7	3.56	12.04	15.23	14.29	11.25	8.48	5.97	3.82
single_ss_AM_M2_w1_s2_stack7	14.36	29.02	31.78	28.43	22.78	17.64	12.83	8.52
single____AM_M2_w2____stack7	18.39	53.06	67.81	71.21	69.61	66.67	62.99	59.14
single_ss_AM_M2_w2_s1_stack7	66.45	39.3	22.86	14.09	8.89	6.39	5.16	4.68
single_ss_AM_M2_w2_s2_stack7	72.76	61.82	49.07	38.26	29.68	23.27	18	13.53
single____M4_M3_w1____stack7	-2.92	-2.91	-2.9	-2.88	-2.85	-2.81	-2.77	-2.71
single_ss_M4_M3_w1_s1_stack7	1.56	1.11	0.43	-0.37	-1.21	-2.01	-2.71	-3.3
single_ss_M4_M3_w1_s2_stack7	-6.57	-6.51	-6.44	-6.33	-6.18	-6.01	-5.8	-5.56
single____M4_M3_w2____stack7	-0.38	-0.3	-0.1	0.2	0.57	1.03	1.55	2.13
single_ss_M4_M3_w2_s1_stack7	-0.05	0.17	0.61	1.24	2.03	2.97	4.03	5.19
single_ss_M4_M3_w2_s2_stack7	-3.32	-2.28	-0.56	1.77	4.61	7.84	11.35	15.03
single____MQ_M3_w1____stack7	-1.99	-2	-1.98	-1.95	-1.9	-1.82	-1.71	-1.57
single_ss_MQ_M3_w1_s1_stack7	2.87	-0.34	-2.57	-3.51	-3.48	-2.76	-1.56	0.01
single_ss_MQ_M3_w1_s2_stack7	-2.88	-3.19	-3.47	-3.7	-3.88	-4.02	-4.13	-4.23
single____MQ_M3_w2____stack7	-1.21	-1.33	-1.23	-0.93	-0.36	0.45	1.48	2.7
single_ss_MQ_M3_w2_s1_stack7	0.75	1.38	2.81	4.99	7.77	10.93	14.29	17.58
single_ss_MQ_M3_w2_s2_stack7	-2.34	-0.03	3.82	8.74	14.23	19.85	25.25	30.19
single____LY_M3_w1____stack7	-1.82	-0.67	1.34	4.08	7.09	10.24	13.28	15.98
single_ss_LY_M3_w1_s1_stack7	0.66	3.28	7.97	13.02	17.14	20.09	22.01	22.92
single_ss_LY_M3_w1_s2_stack7	-2.54	4.06	12.3	20.23	26.51	31	33.9	35.34
single____LY_M3_w2____stack7	-2.85	2.83	12.58	23.36	33.05	40.79	46.44	50.2
single_ss_LY_M3_w2_s1_stack7	17.28	44.32	58.51	61.96	59.95	55.69	50.85	45.86
single_ss_LY_M3_w2_s2_stack7	22.78	62.04	77.68	80.66	78.68	74.76	70.16	65.29
single____AM_M3_w1____stack7	-1.91	10.83	21.85	27.54	28.86	28.33	26.56	24.14
single_ss_AM_M3_w1_s1_stack7	3.02	11.21	14.59	13.89	11.04	8.41	6	3.93
single_ss_AM_M3_w1_s2_stack7	12.51	26.97	30.29	27.45	22.18	17.29	12.66	8.47
single____AM_M3_w2____stack7	17.3	51.96	67.3	71.18	69.89	67.15	63.6	59.82
single_ss_AM_M3_w2_s1_stack7	67.39	40.82	24.18	15.06	9.48	6.63	5.09	4.37
single_ss_AM_M3_w2_s2_stack7	70.9	60.29	48.02	37.57	29.24	23	17.85	13.48
single____MQ_M4_w1____stack7	-3.78	-3.75	-3.71	-3.67	-3.59	-3.5	-3.38	-3.24
single_ss_MQ_M4_w1_s1_stack7	0.44	-0.66	-1.8	-2.72	-3.3	-3.58	-3.63	-3.48



Table 86. Resistance (% difference Model-Z2D)/Z2D*100)

Testcase	10.5 GHz	20.5 GHz	30.5 GHz	40.5 GHz	50.5 GHz	60.5 GHz	70.5 GHz	80.5 GHz
single_ss_MQ_M4_w1_s2_stack7	-6.25	-6.27	-6.25	-6.18	-6.08	-5.92	-5.71	-5.45
single____MQ_M4_w2____stack7	-0.95	-1	-0.91	-0.66	-0.22	0.42	1.26	2.3
single_ss_MQ_M4_w2_s1_stack7	-0.6	0.16	1.61	3.64	6.09	8.83	11.74	14.65
single_ss_MQ_M4_w2_s2_stack7	-3.43	-0.55	3.98	9.56	15.6	21.58	27.16	32.13
single____LY_M4_w1____stack7	-2.38	-1.8	-0.56	1.38	3.68	6.31	9.02	11.56
single_ss_LY_M4_w1_s1_stack7	0.53	2.03	5.53	9.7	13.38	16.24	18.31	19.51
single_ss_LY_M4_w1_s2_stack7	-4.52	0.75	7.61	14.51	20.25	24.65	27.73	29.55
single____LY_M4_w2____stack7	-3.17	1.28	9.79	19.77	29.13	36.9	42.83	46.99
single_ss_LY_M4_w2_s1_stack7	15.79	42.65	58.28	63.4	62.68	59.31	55.02	50.37
single_ss_LY_M4_w2_s2_stack7	23.88	63	77.33	79.53	77.21	73.19	68.61	63.82
single____AM_M4_w1____stack7	-3.11	8.77	19.79	25.91	27.75	27.66	26.23	24.08
single_ss_AM_M4_w1_s1_stack7	2.43	10.3	13.87	13.44	10.8	8.33	6.04	4.07
single_ss_AM_M4_w1_s2_stack7	10.54	24.77	28.65	26.34	21.47	16.84	12.42	8.38
single____AM_M4_w2____stack7	16.19	50.8	66.72	71.09	70.12	67.59	64.17	60.47
single_ss_AM_M4_w2_s1_stack7	68.27	42.41	25.63	16.16	10.21	7	5.14	4.15
single_ss_AM_M4_w2_s2_stack7	68.83	58.53	46.75	36.69	28.63	22.57	17.56	13.3
single____LY_MQ_w1____stack7	-2.22	-1.93	-1.07	0.43	2.2	4.21	6.22	8.02
single_ss_LY_MQ_w1_s1_stack7	-0.99	4.57	12.16	19.05	23.86	26.66	27.96	28.07
single_ss_LY_MQ_w1_s2_stack7	-3.81	3.59	12.45	20.51	26.41	30.19	32.2	32.73
single____LY_MQ_w2____stack7	-0.82	8.11	18.96	27.49	32.44	34.26	33.87	32.05
single_ss_LY_MQ_w2_s1_stack7	14.81	38.74	48.8	49.14	45.11	39.58	33.92	28.47
single_ss_LY_MQ_w2_s2_stack7	37.99	70.01	72.42	65.9	57.52	49.16	41.37	34.25
single____AM_MQ_w1____stack7	-0.46	12.48	21.34	24.21	23.09	20.78	17.75	14.52
single_ss_AM_MQ_w1_s1_stack7	7.22	17.85	19.5	16.97	12.97	9.75	7.12	5.05
single_ss_AM_MQ_w1_s2_stack7	4.49	15.45	20.04	19.19	15.56	11.84	8.11	4.62
single____AM_MQ_w2____stack7	35.05	57.56	56.73	50.08	42.22	35.3	29	23.39
single_ss_AM_MQ_w2_s1_stack7	53.47	29.14	15.81	9.77	6.86	6.16	6.24	6.6
single_ss_AM_MQ_w2_s2_stack7	65.91	51.75	37.66	26.21	17.38	11	5.94	1.84
single____AM_LY_w1____stack7	-0.8	10.24	13.65	12.25	9.06	6.23	3.74	1.7
single_ss_AM_LY_w1_s1_stack7	14.79	26.26	24.19	18.99	13.56	9.65	6.73	4.59
single_ss_AM_LY_w1_s2_stack7	-5.11	3.09	6.78	6.54	4.55	2.82	1.28	0.06
single____AM_LY_w2____stack7	30.98	14.08	3.97	0.29	-0.54	0.3	1.37	2.22
single_ss_AM_LY_w2_s1_stack7	31.31	8.9	1.07	-0.28	0.27	1.63	2.65	3.15
single_ss_AM_LY_w2_s2_stack7	32.95	8.87	0.36	-1.72	-1.52	-0.29	0.68	1.15

Table 87. Inductance (% difference Model-Z2D)/Z2D*100)

Testcase	10.5 GHz	20.5 GHz	30.5 GHz	40.5 GHz	50.5 GHz	60.5 GHz	70.5 GHz	80.5 GHz
single___M2_M1_w1___stack5	-0.47	-0.45	-0.42	-0.38	-0.33	-0.26	-0.18	-0.1
single_ss_M2_M1_w1_s1_stack5	-1.45	-0.76	0.33	1.72	3.33	5.05	6.83	8.58
single_ss_M2_M1_w1_s2_stack5	6.56	6.59	6.63	6.68	6.74	6.81	6.88	6.96
single___M2_M1_w2___stack5	-2.44	-2.22	-2.12	-2.07	-2.03	-1.99	-1.97	-1.95
single_ss_M2_M1_w2_s1_stack5	-2.35	-1.99	-1.87	-1.84	-1.85	-1.9	-1.97	-2.06
single_ss_M2_M1_w2_s2_stack5	13.94	14.08	13.89	13.51	12.96	12.28	11.51	10.64
single___MQ_M1_w1___stack5	0.04	0.07	0.11	0.16	0.22	0.29	0.36	0.44
single_ss_MQ_M1_w1_s1_stack5	-2.35	3.14	8.63	12.9	15.94	18.03	19.47	20.47
single_ss_MQ_M1_w1_s2_stack5	1.15	1.4	1.64	1.84	2.01	2.16	2.29	2.42
single___MQ_M1_w2___stack5	-0.08	0.32	0.55	0.74	0.92	1.07	1.21	1.33
single_ss_MQ_M1_w2_s1_stack5	0.23	0.82	1.09	1.23	1.21	1.07	0.83	0.5
single_ss_MQ_M1_w2_s2_stack5	5	5.35	5.19	4.77	4.18	3.48	2.71	1.91
single___LY_M1_w1___stack5	0.09	0.17	0.21	0.18	0.13	0.04	-0.1	-0.22
single_ss_LY_M1_w1_s1_stack5	3.3	5.05	5.32	5.01	4.53	3.99	3.4	2.92
single_ss_LY_M1_w1_s2_stack5	0.35	-0.05	-0.75	-1.59	-2.4	-3.14	-3.78	-4.29
single___LY_M1_w2___stack5	4.3	4.8	4.72	4.28	3.72	3.12	2.58	2.14
single_ss_LY_M1_w2_s1_stack5	10.79	6.51	2.32	-0.46	-2.12	-3.09	-3.66	-3.95
single_ss_LY_M1_w2_s2_stack5	13.15	5.18	0.42	-2.05	-3.34	-4.05	-4.45	-4.64
single___AM_M1_w1___stack5	0.71	0.48	-0.33	-1.09	-1.66	-2.05	-2.26	-2.38
single_ss_AM_M1_w1_s1_stack5	2.78	2.62	1.25	0.23	-0.31	-0.49	-0.45	-0.31
single_ss_AM_M1_w1_s2_stack5	0.32	-1.57	-3.05	-3.81	-4.17	-4.3	-4.29	-4.22
single___AM_M1_w2___stack5	8.18	5.03	2.63	1.29	0.53	0.1	-0.14	-0.25
single_ss_AM_M1_w2_s1_stack5	-0.18	-3.91	-3.56	-2.88	-2.33	-1.9	-1.53	-1.24
single_ss_AM_M1_w2_s2_stack5	-0.79	-4.17	-4.58	-4.52	-4.39	-4.25	-4.09	-3.93
single___MQ_M2_w1___stack5	0.05	0.07	0.11	0.15	0.21	0.28	0.36	0.45
single_ss_MQ_M2_w1_s1_stack5	0.68	2.42	4.48	6.38	7.95	9.2	10.19	10.97
single_ss_MQ_M2_w1_s2_stack5	3.12	3.25	3.38	3.5	3.61	3.71	3.8	3.9
single___MQ_M2_w2___stack5	-0.99	-0.64	-0.41	-0.21	-0.03	0.13	0.26	0.35
single_ss_MQ_M2_w2_s1_stack5	1.4	1.95	2.05	1.98	1.76	1.42	0.99	0.47
single_ss_MQ_M2_w2_s2_stack5	12.03	12.06	11.34	10.18	8.74	7.16	5.51	3.86
single___LY_M2_w1___stack5	0.11	0.22	0.31	0.34	0.34	0.31	0.23	0.15
single_ss_LY_M2_w1_s1_stack5	3.61	5.28	5.51	5.17	4.64	4.08	3.48	2.98
single_ss_LY_M2_w1_s2_stack5	0.88	0.66	0.13	-0.53	-1.18	-1.8	-2.35	-2.79
single___LY_M2_w2___stack5	4.12	4.65	4.56	4.1	3.5	2.88	2.31	1.86
single_ss_LY_M2_w2_s1_stack5	10.2	6.08	1.99	-0.77	-2.44	-3.44	-4.03	-4.34

Table 87. Inductance (% difference Model-Z2D)/Z2D*100)

Testcase	10.5 GHz	20.5 GHz	30.5 GHz	40.5 GHz	50.5 GHz	60.5 GHz	70.5 GHz	80.5 GHz
single_ss_LY_M2_w2_s2_stack5	13.86	5.04	0.12	-2.33	-3.57	-4.25	-4.62	-4.78
single___AM_M2_w1___stack5	0.75	0.54	-0.25	-0.99	-1.55	-1.91	-2.12	-2.23
single_ss_AM_M2_w1_s1_stack5	3.06	2.85	1.45	0.44	-0.08	-0.26	-0.22	-0.08
single_ss_AM_M2_w1_s2_stack5	0.44	-1.14	-2.51	-3.25	-3.61	-3.75	-3.75	-3.68
single___AM_M2_w2___stack5	8.02	4.54	2.16	0.9	0.22	-0.17	-0.36	-0.44
single_ss_AM_M2_w2_s1_stack5	-0.25	-3.93	-3.6	-2.95	-2.42	-1.99	-1.64	-1.37
single_ss_AM_M2_w2_s2_stack5	-0.86	-4.2	-4.61	-4.53	-4.4	-4.26	-4.1	-3.94
single___LY_MQ_w1___stack5	0.17	0.32	0.44	0.49	0.52	0.5	0.45	0.4
single_ss_LY_MQ_w1_s1_stack5	8.5	9.79	9.07	7.73	6.38	5.2	4.19	3.45
single_ss_LY_MQ_w1_s2_stack5	2	1.38	0.47	-0.56	-1.51	-2.35	-3.05	-3.58
single___LY_MQ_w2___stack5	3.43	3.39	2.66	1.72	0.9	0.22	-0.26	-0.55
single_ss_LY_MQ_w2_s1_stack5	6.09	2.16	-1.32	-3.45	-4.61	-5.22	-5.52	-5.6
single_ss_LY_MQ_w2_s2_stack5	10.18	0.48	-3.62	-5.33	-6.05	-6.35	-6.44	-6.38
single___AM_MQ_w1___stack5	0.67	0.19	-0.69	-1.36	-1.79	-2.04	-2.14	-2.15
single_ss_AM_MQ_w1_s1_stack5	5.94	3.88	1.8	0.73	0.31	0.26	0.41	0.63
single_ss_AM_MQ_w1_s2_stack5	0.48	-0.27	-1.26	-1.86	-2.18	-2.31	-2.31	-2.24
single___AM_MQ_w2___stack5	5.04	1.06	-0.42	-0.94	-1.12	-1.17	-1.13	-1.05
single_ss_AM_MQ_w2_s1_stack5	-1.24	-3.46	-2.88	-2.25	-1.82	-1.54	-1.36	-1.23
single_ss_AM_MQ_w2_s2_stack5	-1.73	-4.38	-4.61	-4.47	-4.3	-4.13	-3.95	-3.77
single___AM_LY_w1___stack5	0.87	-0.11	-1.18	-1.74	-1.99	-2.04	-1.98	-1.87
single_ss_AM_LY_w1_s1_stack5	6.66	1.96	-0.68	-1.66	-1.9	-1.8	-1.54	-1.24
single_ss_AM_LY_w1_s2_stack5	3.53	3.38	2.76	2.41	2.26	2.24	2.33	2.45
single___AM_LY_w2___stack5	-1.01	-2.65	-2.16	-1.58	-1.24	-1.1	-1.01	-0.92
single_ss_AM_LY_w2_s1_stack5	-6.33	-6.64	-5.61	-4.94	-4.66	-4.62	-4.63	-4.63
single_ss_AM_LY_w2_s2_stack5	-6.05	-5.94	-5.05	-4.44	-4.16	-4.08	-4.05	-3.99
single___M2_M1_w1___stack6	-0.47	-0.45	-0.42	-0.38	-0.33	-0.26	-0.18	-0.1
single_ss_M2_M1_w1_s1_stack6	-1.45	-0.76	0.33	1.72	3.33	5.05	6.83	8.58
single_ss_M2_M1_w1_s2_stack6	6.56	6.59	6.63	6.68	6.74	6.81	6.88	6.96
single___M2_M1_w2___stack6	-2.44	-2.22	-2.12	-2.07	-2.03	-1.99	-1.97	-1.95
single_ss_M2_M1_w2_s1_stack6	-2.35	-1.99	-1.87	-1.84	-1.85	-1.9	-1.97	-2.06
single_ss_M2_M1_w2_s2_stack6	13.94	14.08	13.89	13.51	12.96	12.28	11.51	10.64
single___M3_M1_w1___stack6	-0.19	-0.16	-0.13	-0.08	-0.02	0.05	0.13	0.21
single_ss_M3_M1_w1_s1_stack6	-4.81	-1.88	2.48	7.7	13.23	18.66	23.75	28.34
single_ss_M3_M1_w1_s2_stack6	-0.35	-0.13	0.19	0.53	0.86	1.16	1.44	1.69
single___M3_M1_w2___stack6	-1.22	-0.91	-0.76	-0.66	-0.58	-0.51	-0.44	-0.38
single_ss_M3_M1_w2_s1_stack6	-2.12	-1.79	-1.67	-1.63	-1.62	-1.64	-1.69	-1.76

Table 87. Inductance (% difference Model-Z2D)/Z2D*100)

Testcase	10.5 GHz	20.5 GHz	30.5 GHz	40.5 GHz	50.5 GHz	60.5 GHz	70.5 GHz	80.5 GHz
single_ss_M3_M1_w2_s2_stack6	2.62	2.92	2.98	2.93	2.8	2.61	2.36	2.08
single____MQ_M1_w1____stack6	0.03	0.07	0.12	0.18	0.24	0.31	0.37	0.44
single_ss_MQ_M1_w1_s1_stack6	-4.26	5.85	14.74	20.87	24.8	27.24	28.72	29.58
single_ss_MQ_M1_w1_s2_stack6	1.38	2.65	3.69	4.4	4.87	5.2	5.43	5.61
single____MQ_M1_w2____stack6	0.64	1.05	1.27	1.43	1.55	1.65	1.73	1.79
single_ss_MQ_M1_w2_s1_stack6	0.23	0.87	1.2	1.37	1.32	1.1	0.75	0.31
single_ss_MQ_M1_w2_s2_stack6	2.48	2.93	2.94	2.72	2.31	1.79	1.19	0.56
single____LY_M1_w1____stack6	0.08	0.12	0.09	-0.03	-0.17	-0.35	-0.56	-0.75
single_ss_LY_M1_w1_s1_stack6	4.11	5.9	5.99	5.46	4.77	4.08	3.36	2.79
single_ss_LY_M1_w1_s2_stack6	-0.05	-0.66	-1.57	-2.59	-3.54	-4.38	-5.1	-5.64
single____LY_M1_w2____stack6	4.42	4.79	4.59	4.08	3.48	2.87	2.34	1.91
single_ss_LY_M1_w2_s1_stack6	10.35	6.02	1.93	-0.68	-2.18	-3.03	-3.5	-3.72
single_ss_LY_M1_w2_s2_stack6	11.37	4.45	0.12	-2.19	-3.42	-4.1	-4.48	-4.67
single____AM_M1_w1____stack6	0.61	0.26	-0.62	-1.39	-1.96	-2.32	-2.53	-2.63
single_ss_AM_M1_w1_s1_stack6	2.79	2.47	1.01	-0.03	-0.57	-0.74	-0.7	-0.56
single_ss_AM_M1_w1_s2_stack6	0	-2.02	-3.53	-4.28	-4.64	-4.77	-4.75	-4.67
single____AM_M1_w2____stack6	7.86	4.74	2.45	1.19	0.48	0.08	-0.13	-0.23
single_ss_AM_M1_w2_s1_stack6	-0.26	-3.77	-3.34	-2.65	-2.09	-1.66	-1.31	-1.02
single_ss_AM_M1_w2_s2_stack6	-0.76	-4.13	-4.54	-4.48	-4.35	-4.22	-4.06	-3.9
single____M3_M2_w1____stack6	-0.44	-0.42	-0.39	-0.34	-0.27	-0.2	-0.11	-0.01
single_ss_M3_M2_w1_s1_stack6	-0.93	-0.11	1.17	2.8	4.66	6.65	8.68	10.67
single_ss_M3_M2_w1_s2_stack6	6.36	6.38	6.41	6.45	6.5	6.56	6.63	6.71
single____M3_M2_w2____stack6	-2.41	-2.2	-2.13	-2.08	-2.07	-2.07	-2.07	-2.08
single_ss_M3_M2_w2_s1_stack6	-2.45	-2.14	-2.07	-2.07	-2.13	-2.22	-2.35	-2.5
single_ss_M3_M2_w2_s2_stack6	13.05	13.13	12.86	12.39	11.73	10.95	10.06	9.08
single____MQ_M2_w1____stack6	0.04	0.08	0.12	0.18	0.25	0.32	0.4	0.48
single_ss_MQ_M2_w1_s1_stack6	-1	5.41	11.67	16.41	19.69	21.88	23.32	24.26
single_ss_MQ_M2_w1_s2_stack6	1.21	1.61	1.97	2.25	2.47	2.65	2.81	2.95
single____MQ_M2_w2____stack6	-0.08	0.3	0.5	0.65	0.78	0.89	0.97	1.03
single_ss_MQ_M2_w2_s1_stack6	-0.06	0.45	0.65	0.72	0.62	0.4	0.07	-0.34
single_ss_MQ_M2_w2_s2_stack6	4.43	4.68	4.45	3.95	3.27	2.48	1.64	0.78
single____LY_M2_w1____stack6	0.1	0.18	0.2	0.15	0.07	-0.05	-0.2	-0.34
single_ss_LY_M2_w1_s1_stack6	4.63	6.33	6.32	5.69	4.91	4.15	3.39	2.79
single_ss_LY_M2_w1_s2_stack6	0.29	-0.16	-0.87	-1.71	-2.51	-3.24	-3.87	-4.37
single____LY_M2_w2____stack6	4.26	4.65	4.43	3.89	3.25	2.63	2.08	1.66
single_ss_LY_M2_w2_s1_stack6	9.66	5.51	1.53	-1.04	-2.53	-3.39	-3.87	-4.09

Table 87. Inductance (% difference Model-Z2D)/Z2D*100)

Testcase	10.5 GHz	20.5 GHz	30.5 GHz	40.5 GHz	50.5 GHz	60.5 GHz	70.5 GHz	80.5 GHz
single_ss_LY_M2_w2_s2_stack6	11.85	4.29	-0.15	-2.43	-3.61	-4.26	-4.61	-4.77
single____AM_M2_w1____stack6	0.65	0.32	-0.53	-1.28	-1.83	-2.18	-2.37	-2.46
single_ss_AM_M2_w1_s1_stack6	3.09	2.67	1.18	0.14	-0.38	-0.56	-0.51	-0.35
single_ss_AM_M2_w1_s2_stack6	0.1	-1.64	-3.06	-3.79	-4.15	-4.28	-4.28	-4.2
single____AM_M2_w2____stack6	7.67	4.27	1.99	0.82	0.19	-0.16	-0.33	-0.4
single_ss_AM_M2_w2_s1_stack6	-0.35	-3.79	-3.38	-2.7	-2.16	-1.75	-1.41	-1.14
single_ss_AM_M2_w2_s2_stack6	-0.85	-4.16	-4.57	-4.5	-4.38	-4.23	-4.07	-3.92
single____MQ_M3_w1____stack6	0.05	0.07	0.11	0.15	0.21	0.28	0.36	0.45
single_ss_MQ_M3_w1_s1_stack6	0.68	2.42	4.48	6.38	7.95	9.2	10.19	10.97
single_ss_MQ_M3_w1_s2_stack6	3.12	3.25	3.38	3.5	3.61	3.71	3.8	3.9
single____MQ_M3_w2____stack6	-0.99	-0.64	-0.41	-0.21	-0.03	0.13	0.26	0.35
single_ss_MQ_M3_w2_s1_stack6	1.4	1.95	2.05	1.98	1.76	1.42	0.99	0.47
single_ss_MQ_M3_w2_s2_stack6	12.03	12.06	11.34	10.18	8.74	7.16	5.51	3.86
single____LY_M3_w1____stack6	0.11	0.22	0.31	0.34	0.34	0.31	0.23	0.15
single_ss_LY_M3_w1_s1_stack6	3.61	5.28	5.51	5.16	4.64	4.08	3.47	2.97
single_ss_LY_M3_w1_s2_stack6	0.88	0.66	0.13	-0.53	-1.18	-1.8	-2.36	-2.8
single____LY_M3_w2____stack6	4.12	4.65	4.56	4.1	3.5	2.88	2.31	1.86
single_ss_LY_M3_w2_s1_stack6	10.2	6.08	1.98	-0.78	-2.44	-3.44	-4.03	-4.34
single_ss_LY_M3_w2_s2_stack6	13.86	5.04	0.11	-2.33	-3.57	-4.25	-4.62	-4.78
single____AM_M3_w1____stack6	0.75	0.54	-0.25	-0.99	-1.55	-1.91	-2.12	-2.23
single_ss_AM_M3_w1_s1_stack6	3.06	2.85	1.45	0.44	-0.09	-0.26	-0.23	-0.08
single_ss_AM_M3_w1_s2_stack6	0.43	-1.14	-2.52	-3.25	-3.61	-3.76	-3.75	-3.68
single____AM_M3_w2____stack6	8.02	4.54	2.16	0.9	0.22	-0.17	-0.36	-0.44
single_ss_AM_M3_w2_s1_stack6	-0.26	-3.93	-3.6	-2.95	-2.42	-2	-1.65	-1.37
single_ss_AM_M3_w2_s2_stack6	-0.87	-4.2	-4.61	-4.53	-4.4	-4.26	-4.1	-3.94
single____LY_MQ_w1____stack6	0.17	0.32	0.44	0.49	0.52	0.5	0.45	0.4
single_ss_LY_MQ_w1_s1_stack6	8.5	9.79	9.07	7.73	6.38	5.2	4.19	3.45
single_ss_LY_MQ_w1_s2_stack6	2	1.38	0.47	-0.56	-1.51	-2.35	-3.05	-3.58
single____LY_MQ_w2____stack6	3.43	3.39	2.66	1.72	0.9	0.22	-0.26	-0.55
single_ss_LY_MQ_w2_s1_stack6	6.09	2.16	-1.32	-3.45	-4.61	-5.22	-5.52	-5.6
single_ss_LY_MQ_w2_s2_stack6	10.18	0.48	-3.62	-5.33	-6.05	-6.35	-6.44	-6.38
single____AM_MQ_w1____stack6	0.67	0.19	-0.69	-1.36	-1.79	-2.04	-2.14	-2.15
single_ss_AM_MQ_w1_s1_stack6	5.94	3.88	1.8	0.73	0.31	0.26	0.41	0.63
single_ss_AM_MQ_w1_s2_stack6	0.48	-0.27	-1.26	-1.86	-2.18	-2.31	-2.31	-2.24
single____AM_MQ_w2____stack6	5.04	1.06	-0.42	-0.94	-1.12	-1.17	-1.13	-1.05
single_ss_AM_MQ_w2_s1_stack6	-1.24	-3.46	-2.88	-2.25	-1.82	-1.54	-1.36	-1.23

Table 87. Inductance (% difference Model-Z2D)/Z2D*100)

Testcase	10.5 GHz	20.5 GHz	30.5 GHz	40.5 GHz	50.5 GHz	60.5 GHz	70.5 GHz	80.5 GHz
single_ss_AM_MQ_w2_s2_stack6	-1.73	-4.38	-4.61	-4.47	-4.3	-4.13	-3.95	-3.77
single____AM_LY_w1____stack6	0.87	-0.11	-1.18	-1.74	-1.99	-2.04	-1.98	-1.87
single_ss_AM_LY_w1_s1_stack6	6.66	1.96	-0.68	-1.66	-1.9	-1.8	-1.54	-1.24
single_ss_AM_LY_w1_s2_stack6	3.53	3.38	2.76	2.41	2.26	2.24	2.33	2.45
single____AM_LY_w2____stack6	-1.01	-2.65	-2.16	-1.58	-1.24	-1.1	-1.01	-0.92
single_ss_AM_LY_w2_s1_stack6	-6.33	-6.64	-5.61	-4.94	-4.66	-4.62	-4.63	-4.63
single_ss_AM_LY_w2_s2_stack6	-6.05	-5.94	-5.05	-4.44	-4.16	-4.08	-4.05	-3.99
single____M2_M1_w1____stack7	-0.47	-0.45	-0.42	-0.38	-0.33	-0.26	-0.18	-0.1
single_ss_M2_M1_w1_s1_stack7	-1.45	-0.76	0.33	1.73	3.33	5.06	6.83	8.59
single_ss_M2_M1_w1_s2_stack7	6.56	6.59	6.63	6.68	6.74	6.81	6.88	6.96
single____M2_M1_w2____stack7	-2.44	-2.22	-2.12	-2.07	-2.03	-1.99	-1.97	-1.95
single_ss_M2_M1_w2_s1_stack7	-2.35	-1.99	-1.87	-1.84	-1.85	-1.9	-1.97	-2.06
single_ss_M2_M1_w2_s2_stack7	13.94	14.08	13.89	13.51	12.96	12.28	11.51	10.65
single____M3_M1_w1____stack7	-0.19	-0.16	-0.13	-0.08	-0.02	0.05	0.13	0.21
single_ss_M3_M1_w1_s1_stack7	-4.81	-1.88	2.48	7.7	13.23	18.67	23.75	28.34
single_ss_M3_M1_w1_s2_stack7	-0.35	-0.13	0.19	0.53	0.86	1.16	1.44	1.69
single____M3_M1_w2____stack7	-1.22	-0.91	-0.76	-0.66	-0.58	-0.51	-0.44	-0.38
single_ss_M3_M1_w2_s1_stack7	-2.12	-1.79	-1.67	-1.62	-1.61	-1.63	-1.68	-1.74
single_ss_M3_M1_w2_s2_stack7	2.62	2.92	2.98	2.93	2.81	2.62	2.37	2.09
single____M4_M1_w1____stack7	-0.13	-0.1	-0.05	0.02	0.08	0.16	0.23	0.31
single_ss_M4_M1_w1_s1_stack7	-6.91	-1.8	5.54	13.96	22.46	30.4	37.45	43.49
single_ss_M4_M1_w1_s2_stack7	0.03	0.65	1.48	2.36	3.18	3.92	4.55	5.08
single____M4_M1_w2____stack7	-0.39	0	0.18	0.3	0.4	0.48	0.55	0.62
single_ss_M4_M1_w2_s1_stack7	-1.16	-0.84	-0.76	-0.78	-0.85	-0.96	-1.11	-1.28
single_ss_M4_M1_w2_s2_stack7	0.39	0.75	0.88	0.9	0.84	0.72	0.56	0.36
single____MQ_M1_w1____stack7	0.03	0.08	0.14	0.2	0.25	0.3	0.34	0.38
single_ss_MQ_M1_w1_s1_stack7	-5.29	8.95	20.37	27.64	31.96	34.41	35.71	36.25
single_ss_MQ_M1_w1_s2_stack7	2.13	4.78	6.77	8	8.73	9.18	9.44	9.59
single____MQ_M1_w2____stack7	1.22	1.65	1.86	1.98	2.06	2.12	2.14	2.15
single_ss_MQ_M1_w2_s1_stack7	0.72	1.37	1.68	1.74	1.52	1.11	0.6	0.04
single_ss_MQ_M1_w2_s2_stack7	1.71	2.28	2.41	2.24	1.85	1.31	0.71	0.08
single____LY_M1_w1____stack7	0.07	0.05	-0.06	-0.27	-0.51	-0.78	-1.06	-1.31
single_ss_LY_M1_w1_s1_stack7	4.92	6.71	6.6	5.86	4.98	4.13	3.31	2.67
single_ss_LY_M1_w1_s2_stack7	-0.25	-1.07	-2.19	-3.41	-4.51	-5.46	-6.24	-6.82
single____LY_M1_w2____stack7	4.51	4.78	4.47	3.88	3.25	2.64	2.12	1.72
single_ss_LY_M1_w2_s1_stack7	10.13	5.65	1.6	-0.85	-2.2	-2.93	-3.31	-3.46

Table 87. Inductance (% difference Model-Z2D)/Z2D*100)

Testcase	10.5 GHz	20.5 GHz	30.5 GHz	40.5 GHz	50.5 GHz	60.5 GHz	70.5 GHz	80.5 GHz
single_ss_LY_M1_w2_s2_stack7	9.94	3.8	-0.18	-2.35	-3.51	-4.17	-4.54	-4.72
single____AM_M1_w1____stack7	0.51	0.03	-0.92	-1.7	-2.26	-2.61	-2.8	-2.89
single_ss_AM_M1_w1_s1_stack7	2.81	2.33	0.8	-0.26	-0.8	-0.97	-0.93	-0.77
single_ss_AM_M1_w1_s2_stack7	-0.26	-2.41	-3.95	-4.71	-5.06	-5.18	-5.16	-5.07
single____AM_M1_w2____stack7	7.57	4.49	2.28	1.09	0.43	0.06	-0.13	-0.21
single_ss_AM_M1_w2_s1_stack7	-0.32	-3.62	-3.13	-2.42	-1.85	-1.43	-1.08	-0.82
single_ss_AM_M1_w2_s2_stack7	-0.73	-4.08	-4.5	-4.44	-4.31	-4.18	-4.02	-3.86
single____M3_M2_w1____stack7	-0.44	-0.42	-0.39	-0.34	-0.27	-0.2	-0.11	-0.01
single_ss_M3_M2_w1_s1_stack7	-0.93	-0.11	1.17	2.8	4.66	6.65	8.68	10.67
single_ss_M3_M2_w1_s2_stack7	6.36	6.38	6.41	6.45	6.5	6.56	6.63	6.71
single____M3_M2_w2____stack7	-2.41	-2.2	-2.13	-2.08	-2.07	-2.07	-2.07	-2.08
single_ss_M3_M2_w2_s1_stack7	-2.44	-2.14	-2.07	-2.07	-2.13	-2.22	-2.34	-2.49
single_ss_M3_M2_w2_s2_stack7	13.05	13.12	12.87	12.39	11.74	10.95	10.06	9.09
single____M4_M2_w1____stack7	-0.18	-0.15	-0.11	-0.05	0.02	0.1	0.18	0.27
single_ss_M4_M2_w1_s1_stack7	-3.56	-0.34	4.43	10.1	16.09	21.93	27.35	32.21
single_ss_M4_M2_w1_s2_stack7	-0.63	-0.34	0.05	0.46	0.87	1.23	1.56	1.85
single____M4_M2_w2____stack7	-1.21	-0.91	-0.77	-0.68	-0.6	-0.54	-0.49	-0.44
single_ss_M4_M2_w2_s1_stack7	-2.09	-1.8	-1.72	-1.7	-1.74	-1.81	-1.9	-2.01
single_ss_M4_M2_w2_s2_stack7	2.4	2.66	2.68	2.59	2.41	2.17	1.86	1.53
single____MQ_M2_w1____stack7	0.04	0.08	0.14	0.21	0.27	0.34	0.4	0.47
single_ss_MQ_M2_w1_s1_stack7	-2.04	9.27	19	25.56	29.62	32.02	33.35	33.98
single_ss_MQ_M2_w1_s2_stack7	1.59	3.15	4.4	5.23	5.76	6.12	6.37	6.55
single____MQ_M2_w2____stack7	0.64	1.03	1.23	1.35	1.44	1.5	1.54	1.55
single_ss_MQ_M2_w2_s1_stack7	0.09	0.65	0.9	0.97	0.82	0.49	0.06	-0.46
single_ss_MQ_M2_w2_s2_stack7	2.16	2.55	2.51	2.21	1.72	1.11	0.44	-0.24
single____LY_M2_w1____stack7	0.09	0.12	0.07	-0.07	-0.24	-0.44	-0.67	-0.87
single_ss_LY_M2_w1_s1_stack7	5.63	7.31	7.04	6.14	5.13	4.18	3.29	2.61
single_ss_LY_M2_w1_s2_stack7	-0.04	-0.7	-1.62	-2.66	-3.62	-4.47	-5.19	-5.73
single____LY_M2_w2____stack7	4.37	4.64	4.3	3.69	3.02	2.4	1.88	1.47
single_ss_LY_M2_w2_s1_stack7	9.39	5.09	1.17	-1.23	-2.56	-3.3	-3.68	-3.84
single_ss_LY_M2_w2_s2_stack7	10.22	3.62	-0.43	-2.57	-3.68	-4.31	-4.64	-4.8
single____AM_M2_w1____stack7	0.56	0.1	-0.82	-1.58	-2.12	-2.45	-2.63	-2.71
single_ss_AM_M2_w1_s1_stack7	3.12	2.52	0.94	-0.13	-0.65	-0.82	-0.75	-0.6
single_ss_AM_M2_w1_s2_stack7	-0.18	-2.08	-3.54	-4.28	-4.63	-4.75	-4.74	-4.66
single____AM_M2_w2____stack7	7.37	4.02	1.85	0.74	0.16	-0.16	-0.32	-0.38
single_ss_AM_M2_w2_s1_stack7	-0.44	-3.64	-3.17	-2.46	-1.92	-1.51	-1.18	-0.94

Table 87. Inductance (% difference Model-Z2D)/Z2D*100)

Testcase	10.5 GHz	20.5 GHz	30.5 GHz	40.5 GHz	50.5 GHz	60.5 GHz	70.5 GHz	80.5 GHz
single_ss_AM_M2_w2_s2_stack7	-0.83	-4.12	-4.53	-4.47	-4.34	-4.2	-4.05	-3.89
single___M4_M3_w1___stack7	-0.44	-0.42	-0.39	-0.34	-0.27	-0.2	-0.11	-0.01
single_ss_M4_M3_w1_s1_stack7	-0.93	-0.11	1.17	2.8	4.66	6.65	8.68	10.67
single_ss_M4_M3_w1_s2_stack7	6.36	6.38	6.41	6.45	6.5	6.56	6.63	6.71
single___M4_M3_w2___stack7	-2.41	-2.2	-2.13	-2.08	-2.07	-2.07	-2.07	-2.08
single_ss_M4_M3_w2_s1_stack7	-2.45	-2.14	-2.07	-2.07	-2.13	-2.22	-2.35	-2.5
single_ss_M4_M3_w2_s2_stack7	13.05	13.13	12.86	12.39	11.73	10.95	10.06	9.08
single___MQ_M3_w1___stack7	0.04	0.08	0.12	0.18	0.25	0.32	0.4	0.48
single_ss_MQ_M3_w1_s1_stack7	-1	5.41	11.67	16.41	19.69	21.88	23.32	24.25
single_ss_MQ_M3_w1_s2_stack7	1.21	1.61	1.97	2.25	2.47	2.65	2.81	2.95
single___MQ_M3_w2___stack7	-0.08	0.3	0.5	0.65	0.78	0.89	0.97	1.03
single_ss_MQ_M3_w2_s1_stack7	-0.06	0.45	0.65	0.72	0.62	0.4	0.07	-0.35
single_ss_MQ_M3_w2_s2_stack7	4.43	4.68	4.45	3.95	3.27	2.48	1.64	0.78
single___LY_M3_w1___stack7	0.1	0.18	0.2	0.15	0.07	-0.05	-0.2	-0.34
single_ss_LY_M3_w1_s1_stack7	4.63	6.33	6.32	5.69	4.91	4.14	3.39	2.78
single_ss_LY_M3_w1_s2_stack7	0.29	-0.16	-0.87	-1.71	-2.51	-3.24	-3.88	-4.37
single___LY_M3_w2___stack7	4.26	4.65	4.43	3.89	3.25	2.63	2.08	1.66
single_ss_LY_M3_w2_s1_stack7	9.65	5.51	1.53	-1.04	-2.53	-3.39	-3.87	-4.1
single_ss_LY_M3_w2_s2_stack7	11.84	4.28	-0.15	-2.43	-3.61	-4.26	-4.61	-4.77
single___AM_M3_w1___stack7	0.65	0.32	-0.53	-1.28	-1.83	-2.18	-2.37	-2.46
single_ss_AM_M3_w1_s1_stack7	3.09	2.67	1.17	0.14	-0.39	-0.56	-0.51	-0.35
single_ss_AM_M3_w1_s2_stack7	0.1	-1.64	-3.06	-3.8	-4.15	-4.29	-4.28	-4.2
single___AM_M3_w2___stack7	7.67	4.27	1.99	0.82	0.19	-0.16	-0.33	-0.4
single_ss_AM_M3_w2_s1_stack7	-0.36	-3.8	-3.39	-2.7	-2.16	-1.75	-1.41	-1.14
single_ss_AM_M3_w2_s2_stack7	-0.85	-4.16	-4.57	-4.51	-4.38	-4.23	-4.08	-3.92
single___MQ_M4_w1___stack7	0.05	0.07	0.11	0.15	0.21	0.28	0.36	0.45
single_ss_MQ_M4_w1_s1_stack7	0.68	2.42	4.48	6.38	7.95	9.2	10.19	10.97
single_ss_MQ_M4_w1_s2_stack7	3.12	3.25	3.38	3.5	3.61	3.71	3.8	3.9
single___MQ_M4_w2___stack7	-0.99	-0.64	-0.41	-0.21	-0.03	0.13	0.26	0.35
single_ss_MQ_M4_w2_s1_stack7	1.4	1.95	2.05	1.98	1.76	1.42	0.99	0.47
single_ss_MQ_M4_w2_s2_stack7	12.03	12.06	11.34	10.18	8.74	7.16	5.51	3.86
single___LY_M4_w1___stack7	0.11	0.22	0.31	0.34	0.34	0.31	0.23	0.15
single_ss_LY_M4_w1_s1_stack7	3.61	5.28	5.51	5.16	4.64	4.08	3.47	2.97
single_ss_LY_M4_w1_s2_stack7	0.88	0.66	0.13	-0.53	-1.18	-1.8	-2.36	-2.8
single___LY_M4_w2___stack7	4.12	4.65	4.56	4.1	3.5	2.88	2.31	1.86
single_ss_LY_M4_w2_s1_stack7	10.2	6.08	1.98	-0.78	-2.44	-3.44	-4.03	-4.34

*Table 87. Inductance (% difference Model-Z2D)/Z2D*100)*

Testcase	10.5 GHz	20.5 GHz	30.5 GHz	40.5 GHz	50.5 GHz	60.5 GHz	70.5 GHz	80.5 GHz
single_ss_LY_M4_w2_s2_stack7	13.86	5.04	0.11	-2.33	-3.57	-4.25	-4.62	-4.78
single____AM_M4_w1____stack7	0.75	0.54	-0.25	-0.99	-1.55	-1.91	-2.12	-2.23
single_ss_AM_M4_w1_s1_stack7	3.06	2.85	1.45	0.44	-0.09	-0.26	-0.23	-0.08
single_ss_AM_M4_w1_s2_stack7	0.43	-1.14	-2.52	-3.25	-3.61	-3.76	-3.75	-3.68
single____AM_M4_w2____stack7	8.02	4.54	2.16	0.9	0.22	-0.17	-0.36	-0.44
single_ss_AM_M4_w2_s1_stack7	-0.26	-3.93	-3.6	-2.95	-2.42	-2	-1.65	-1.37
single_ss_AM_M4_w2_s2_stack7	-0.87	-4.2	-4.61	-4.53	-4.4	-4.26	-4.1	-3.94
single____LY_MQ_w1____stack7	0.17	0.32	0.44	0.49	0.52	0.5	0.45	0.4
single_ss_LY_MQ_w1_s1_stack7	8.5	9.79	9.07	7.73	6.38	5.2	4.19	3.45
single_ss_LY_MQ_w1_s2_stack7	2	1.38	0.47	-0.56	-1.51	-2.35	-3.05	-3.58
single____LY_MQ_w2____stack7	3.43	3.39	2.66	1.72	0.9	0.22	-0.26	-0.55
single_ss_LY_MQ_w2_s1_stack7	6.09	2.16	-1.32	-3.45	-4.61	-5.22	-5.52	-5.6
single_ss_LY_MQ_w2_s2_stack7	10.18	0.48	-3.62	-5.33	-6.05	-6.35	-6.44	-6.38
single____AM_MQ_w1____stack7	0.67	0.19	-0.69	-1.36	-1.79	-2.04	-2.14	-2.15
single_ss_AM_MQ_w1_s1_stack7	5.94	3.88	1.8	0.73	0.31	0.26	0.41	0.63
single_ss_AM_MQ_w1_s2_stack7	0.48	-0.27	-1.26	-1.86	-2.18	-2.31	-2.31	-2.24
single____AM_MQ_w2____stack7	5.04	1.06	-0.42	-0.94	-1.12	-1.17	-1.13	-1.05
single_ss_AM_MQ_w2_s1_stack7	-1.24	-3.46	-2.88	-2.25	-1.82	-1.54	-1.36	-1.23
single_ss_AM_MQ_w2_s2_stack7	-1.73	-4.38	-4.61	-4.47	-4.3	-4.13	-3.95	-3.77
single____AM_LY_w1____stack7	0.87	-0.11	-1.18	-1.74	-1.99	-2.04	-1.98	-1.87
single_ss_AM_LY_w1_s1_stack7	6.66	1.96	-0.68	-1.66	-1.9	-1.8	-1.54	-1.24
single_ss_AM_LY_w1_s2_stack7	3.53	3.38	2.76	2.41	2.26	2.24	2.33	2.45
single____AM_LY_w2____stack7	-1.01	-2.65	-2.16	-1.58	-1.24	-1.1	-1.01	-0.92
single_ss_AM_LY_w2_s1_stack7	-6.33	-6.64	-5.61	-4.94	-4.66	-4.62	-4.63	-4.63
single_ss_AM_LY_w2_s2_stack7	-6.05	-5.94	-5.05	-4.44	-4.16	-4.08	-4.05	-3.99

*Table 88. Capacitance with Fill (% difference Model-Z2D)/Z2D*100)*

Testcase	10.5 GHz	20.5 GHz	30.5 GHz	40.5 GHz	50.5 GHz	60.5 GHz	70.5 GHz	80.5 GHz
single____M2_M1_w1____stack5	3.36	3.35	3.34	3.33	3.31	3.28	3.25	3.22
single_ss_M2_M1_w1_s1_stack5	-9.78	-9.78	-9.8	-9.81	-9.84	-9.87	-9.9	-9.94
single_ss_M2_M1_w1_s2_stack5	6.61	6.6	6.59	6.57	6.55	6.52	6.49	6.45
single____M2_M1_w2____stack5	1.5	1.49	1.48	1.46	1.44	1.41	1.37	1.34
single_ss_M2_M1_w2_s1_stack5	7.14	7.14	7.12	7.1	7.07	7.04	7	6.96
single_ss_M2_M1_w2_s2_stack5	7.7	7.69	7.68	7.65	7.62	7.58	7.54	7.49
single____MQ_M1_w1____stack5	10.21	10.2	10.19	10.18	10.15	10.13	10.1	10.06
single_ss_MQ_M1_w1_s1_stack5	-12.49	-12.5	-12.51	-12.53	-12.55	-12.57	-12.6	-12.64

Table 88. Capacitance with Fill (% difference Model-Z2D)/Z2D*100)

Testcase	10.5 GHz	20.5 GHz	30.5 GHz	40.5 GHz	50.5 GHz	60.5 GHz	70.5 GHz	80.5 GHz
single_ss_MQ_M1_w1_s2_stack5	-4.12	-4.13	-4.14	-4.15	-4.16	-4.18	-4.21	-4.24
single____MQ_M1_w2____stack5	9.09	9.08	9.07	9.06	9.03	9.01	8.98	8.94
single_ss_MQ_M1_w2_s1_stack5	11.6	11.59	11.58	11.56	11.53	11.51	11.47	11.43
single_ss_MQ_M1_w2_s2_stack5	13.64	13.64	13.62	13.6	13.58	13.55	13.52	13.48
single____LY_M1_w1____stack5	7.63	7.63	7.61	7.6	7.58	7.56	7.53	7.5
single_ss_LY_M1_w1_s1_stack5	-3.69	-3.69	-3.7	-3.72	-3.74	-3.76	-3.78	-3.81
single_ss_LY_M1_w1_s2_stack5	6.35	6.35	6.34	6.32	6.31	6.28	6.26	6.23
single____LY_M1_w2____stack5	5.87	5.86	5.85	5.84	5.82	5.8	5.77	5.74
single_ss_LY_M1_w2_s1_stack5	5.39	5.38	5.37	5.36	5.34	5.32	5.29	5.26
single_ss_LY_M1_w2_s2_stack5	8.18	8.17	8.16	8.15	8.13	8.11	8.08	8.05
single____AM_M1_w1____stack5	5.11	5.11	5.1	5.09	5.07	5.05	5.02	5
single_ss_AM_M1_w1_s1_stack5	-2.46	-2.47	-2.48	-2.49	-2.51	-2.53	-2.55	-2.58
single_ss_AM_M1_w1_s2_stack5	2.59	2.58	2.57	2.56	2.54	2.52	2.5	2.47
single____AM_M1_w2____stack5	3.85	3.84	3.84	3.82	3.81	3.79	3.76	3.73
single_ss_AM_M1_w2_s1_stack5	0.68	0.67	0.66	0.65	0.63	0.61	0.59	0.56
single_ss_AM_M1_w2_s2_stack5	4.57	4.57	4.56	4.54	4.53	4.51	4.49	4.46
single____MQ_M2_w1____stack5	-2.04	-2.05	-2.06	-2.07	-2.09	-2.11	-2.14	-2.17
single_ss_MQ_M2_w1_s1_stack5	-11.15	-11.16	-11.17	-11.18	-11.2	-11.22	-11.25	-11.28
single_ss_MQ_M2_w1_s2_stack5	-6.61	-6.62	-6.63	-6.64	-6.66	-6.68	-6.7	-6.73
single____MQ_M2_w2____stack5	-3.76	-3.77	-3.78	-3.8	-3.82	-3.84	-3.87	-3.9
single_ss_MQ_M2_w2_s1_stack5	1.19	1.18	1.17	1.15	1.13	1.1	1.07	1.04
single_ss_MQ_M2_w2_s2_stack5	1.48	1.47	1.46	1.44	1.42	1.39	1.36	1.33
single____LY_M2_w1____stack5	5.16	5.15	5.14	5.13	5.11	5.09	5.06	5.03
single_ss_LY_M2_w1_s1_stack5	-3.39	-3.4	-3.41	-3.42	-3.44	-3.46	-3.49	-3.52
single_ss_LY_M2_w1_s2_stack5	4.11	4.1	4.09	4.08	4.06	4.04	4.01	3.99
single____LY_M2_w2____stack5	3.9	3.89	3.88	3.87	3.85	3.83	3.8	3.77
single_ss_LY_M2_w2_s1_stack5	4.86	4.85	4.84	4.83	4.81	4.79	4.77	4.74
single_ss_LY_M2_w2_s2_stack5	6.51	6.5	6.49	6.48	6.46	6.44	6.42	6.39
single____AM_M2_w1____stack5	3.93	3.92	3.91	3.9	3.88	3.86	3.84	3.81
single_ss_AM_M2_w1_s1_stack5	-2.38	-2.39	-2.4	-2.41	-2.43	-2.45	-2.47	-2.5
single_ss_AM_M2_w1_s2_stack5	2.1	2.09	2.08	2.07	2.06	2.04	2.01	1.99
single____AM_M2_w2____stack5	2.85	2.85	2.84	2.83	2.81	2.79	2.77	2.74
single_ss_AM_M2_w2_s1_stack5	0.68	0.68	0.67	0.66	0.64	0.62	0.6	0.57
single_ss_AM_M2_w2_s2_stack5	4.04	4.04	4.03	4.02	4	3.98	3.96	3.93
single____LY_MQ_w1____stack5	1.19	1.18	1.17	1.16	1.14	1.12	1.09	1.07
single_ss_LY_MQ_w1_s1_stack5	-2.67	-2.68	-2.69	-2.71	-2.73	-2.75	-2.77	-2.8



Table 88. Capacitance with Fill (% difference Model-Z2D)/Z2D*100)

Testcase	10.5 GHz	20.5 GHz	30.5 GHz	40.5 GHz	50.5 GHz	60.5 GHz	70.5 GHz	80.5 GHz
single_ss_LY_MQ_w1_s2_stack5	3.92	3.91	3.9	3.89	3.87	3.85	3.83	3.8
single____LY_MQ_w2____stack5	0.68	0.67	0.66	0.65	0.63	0.61	0.59	0.56
single_ss_LY_MQ_w2_s1_stack5	3.9	3.9	3.89	3.87	3.86	3.83	3.81	3.78
single_ss_LY_MQ_w2_s2_stack5	4.37	4.36	4.35	4.34	4.32	4.3	4.28	4.25
single____AM_MQ_w1____stack5	2.1	2.09	2.08	2.07	2.05	2.03	2.01	1.98
single_ss_AM_MQ_w1_s1_stack5	-2.18	-2.19	-2.2	-2.21	-2.23	-2.25	-2.27	-2.3
single_ss_AM_MQ_w1_s2_stack5	1.12	1.11	1.11	1.09	1.08	1.06	1.03	1.01
single____AM_MQ_w2____stack5	1.43	1.42	1.41	1.4	1.38	1.37	1.34	1.32
single_ss_AM_MQ_w2_s1_stack5	0.81	0.81	0.8	0.78	0.77	0.75	0.72	0.7
single_ss_AM_MQ_w2_s2_stack5	3.27	3.26	3.26	3.24	3.23	3.21	3.18	3.16
single____AM_LY_w1____stack5	3.09	3.08	3.07	3.06	3.04	3.02	3	2.97
single_ss_AM_LY_w1_s1_stack5	-0.17	-0.18	-0.19	-0.2	-0.22	-0.24	-0.27	-0.29
single_ss_AM_LY_w1_s2_stack5	-2.69	-2.7	-2.71	-2.72	-2.74	-2.75	-2.78	-2.8
single____AM_LY_w2____stack5	2.72	2.72	2.71	2.69	2.68	2.66	2.63	2.6
single_ss_AM_LY_w2_s1_stack5	4.21	4.21	4.2	4.18	4.16	4.14	4.12	4.09
single_ss_AM_LY_w2_s2_stack5	3.83	3.83	3.82	3.8	3.79	3.77	3.74	3.71
single____M2_M1_w1____stack6	3.36	3.35	3.34	3.33	3.31	3.28	3.25	3.22
single_ss_M2_M1_w1_s1_stack6	-9.78	-9.78	-9.8	-9.81	-9.84	-9.87	-9.9	-9.94
single_ss_M2_M1_w1_s2_stack6	6.61	6.6	6.59	6.57	6.55	6.52	6.49	6.45
single____M2_M1_w2____stack6	1.5	1.49	1.48	1.46	1.44	1.41	1.37	1.34
single_ss_M2_M1_w2_s1_stack6	7.14	7.14	7.12	7.1	7.07	7.04	7	6.96
single_ss_M2_M1_w2_s2_stack6	7.7	7.69	7.68	7.65	7.62	7.58	7.54	7.49
single____M3_M1_w1____stack6	18.44	18.43	18.42	18.4	18.38	18.35	18.31	18.27
single_ss_M3_M1_w1_s1_stack6	-12.88	-12.89	-12.91	-12.93	-12.96	-12.99	-13.03	-13.07
single_ss_M3_M1_w1_s2_stack6	11.01	11	10.99	10.97	10.95	10.92	10.89	10.86
single____M3_M1_w2____stack6	16.53	16.53	16.51	16.49	16.47	16.44	16.4	16.36
single_ss_M3_M1_w2_s1_stack6	19.26	19.25	19.24	19.22	19.19	19.16	19.12	19.07
single_ss_M3_M1_w2_s2_stack6	22.91	22.9	22.88	22.86	22.83	22.8	22.76	22.71
single____MQ_M1_w1____stack6	17.53	17.52	17.51	17.49	17.47	17.44	17.41	17.37
single_ss_MQ_M1_w1_s1_stack6	-13.74	-13.75	-13.76	-13.78	-13.8	-13.82	-13.85	-13.89
single_ss_MQ_M1_w1_s2_stack6	-1.78	-1.79	-1.8	-1.81	-1.83	-1.85	-1.88	-1.91
single____MQ_M1_w2____stack6	15.38	15.38	15.36	15.35	15.32	15.29	15.26	15.22
single_ss_MQ_M1_w2_s1_stack6	14.66	14.65	14.64	14.62	14.59	14.57	14.53	14.49
single_ss_MQ_M1_w2_s2_stack6	18.87	18.86	18.85	18.83	18.81	18.78	18.74	18.7
single____LY_M1_w1____stack6	9.91	9.9	9.89	9.88	9.86	9.83	9.8	9.77
single_ss_LY_M1_w1_s1_stack6	-3.97	-3.97	-3.98	-4	-4.02	-4.04	-4.06	-4.09

Table 88. Capacitance with Fill (% difference Model-Z2D)/Z2D*100)

Testcase	10.5 GHz	20.5 GHz	30.5 GHz	40.5 GHz	50.5 GHz	60.5 GHz	70.5 GHz	80.5 GHz
single_ss_LY_M1_w1_s2_stack6	8.17	8.16	8.15	8.14	8.12	8.1	8.07	8.04
single____LY_M1_w2____stack6	7.61	7.61	7.59	7.58	7.56	7.54	7.51	7.48
single_ss_LY_M1_w2_s1_stack6	5.67	5.66	5.65	5.64	5.62	5.6	5.57	5.54
single_ss_LY_M1_w2_s2_stack6	9.55	9.55	9.54	9.52	9.5	9.48	9.46	9.43
single____AM_M1_w1____stack6	6.26	6.25	6.24	6.23	6.21	6.19	6.16	6.13
single_ss_AM_M1_w1_s1_stack6	-2.54	-2.55	-2.56	-2.57	-2.59	-2.61	-2.63	-2.66
single_ss_AM_M1_w1_s2_stack6	2.99	2.99	2.98	2.96	2.95	2.93	2.91	2.88
single____AM_M1_w2____stack6	4.77	4.77	4.76	4.74	4.73	4.71	4.68	4.65
single_ss_AM_M1_w2_s1_stack6	0.63	0.62	0.61	0.6	0.59	0.57	0.54	0.51
single_ss_AM_M1_w2_s2_stack6	4.99	4.99	4.98	4.97	4.95	4.93	4.91	4.88
single____M3_M2_w1____stack6	3.27	3.27	3.25	3.24	3.22	3.19	3.16	3.13
single_ss_M3_M2_w1_s1_stack6	-9.78	-9.79	-9.8	-9.82	-9.84	-9.87	-9.91	-9.94
single_ss_M3_M2_w1_s2_stack6	6.6	6.59	6.58	6.56	6.54	6.51	6.47	6.44
single____M3_M2_w2____stack6	1.5	1.49	1.48	1.46	1.43	1.4	1.37	1.33
single_ss_M3_M2_w2_s1_stack6	7.14	7.14	7.12	7.1	7.07	7.04	7	6.95
single_ss_M3_M2_w2_s2_stack6	7.7	7.69	7.67	7.65	7.62	7.58	7.54	7.49
single____MQ_M2_w1____stack6	10.14	10.14	10.12	10.11	10.09	10.06	10.03	9.99
single_ss_MQ_M2_w1_s1_stack6	-12.5	-12.5	-12.52	-12.53	-12.55	-12.58	-12.61	-12.64
single_ss_MQ_M2_w1_s2_stack6	-4.12	-4.13	-4.14	-4.15	-4.17	-4.19	-4.21	-4.24
single____MQ_M2_w2____stack6	9.09	9.09	9.07	9.06	9.03	9.01	8.98	8.94
single_ss_MQ_M2_w2_s1_stack6	11.59	11.59	11.57	11.55	11.53	11.5	11.47	11.43
single_ss_MQ_M2_w2_s2_stack6	13.64	13.64	13.62	13.6	13.58	13.55	13.52	13.48
single____LY_M2_w1____stack6	7.61	7.61	7.6	7.58	7.56	7.54	7.51	7.48
single_ss_LY_M2_w1_s1_stack6	-3.69	-3.7	-3.71	-3.72	-3.74	-3.76	-3.79	-3.81
single_ss_LY_M2_w1_s2_stack6	6.35	6.35	6.34	6.32	6.31	6.28	6.26	6.23
single____LY_M2_w2____stack6	5.87	5.86	5.85	5.84	5.82	5.8	5.77	5.74
single_ss_LY_M2_w2_s1_stack6	5.39	5.38	5.37	5.36	5.34	5.32	5.29	5.26
single_ss_LY_M2_w2_s2_stack6	8.18	8.17	8.16	8.15	8.13	8.11	8.08	8.05
single____AM_M2_w1____stack6	5.1	5.1	5.09	5.07	5.06	5.04	5.01	4.98
single_ss_AM_M2_w1_s1_stack6	-2.46	-2.47	-2.48	-2.49	-2.51	-2.53	-2.55	-2.58
single_ss_AM_M2_w1_s2_stack6	2.58	2.58	2.57	2.55	2.54	2.52	2.5	2.47
single____AM_M2_w2____stack6	3.85	3.84	3.83	3.82	3.81	3.79	3.76	3.73
single_ss_AM_M2_w2_s1_stack6	0.67	0.66	0.65	0.64	0.63	0.61	0.58	0.55
single_ss_AM_M2_w2_s2_stack6	4.57	4.57	4.56	4.54	4.53	4.51	4.48	4.46
single____MQ_M3_w1____stack6	-2.1	-2.11	-2.12	-2.13	-2.15	-2.17	-2.2	-2.23
single_ss_MQ_M3_w1_s1_stack6	-11.16	-11.17	-11.18	-11.19	-11.21	-11.24	-11.26	-11.3

Table 88. Capacitance with Fill (% difference Model-Z2D)/Z2D*100)

Testcase	10.5 GHz	20.5 GHz	30.5 GHz	40.5 GHz	50.5 GHz	60.5 GHz	70.5 GHz	80.5 GHz
single_ss_MQ_M3_w1_s2_stack6	-6.65	-6.66	-6.67	-6.68	-6.7	-6.72	-6.74	-6.77
single____MQ_M3_w2____stack6	-3.82	-3.83	-3.84	-3.85	-3.87	-3.9	-3.92	-3.96
single_ss_MQ_M3_w2_s1_stack6	1.13	1.12	1.11	1.09	1.07	1.04	1.01	0.98
single_ss_MQ_M3_w2_s2_stack6	1.42	1.41	1.4	1.38	1.36	1.33	1.3	1.27
single____LY_M3_w1____stack6	5.15	5.15	5.14	5.12	5.1	5.08	5.05	5.03
single_ss_LY_M3_w1_s1_stack6	-3.39	-3.4	-3.41	-3.42	-3.44	-3.46	-3.49	-3.52
single_ss_LY_M3_w1_s2_stack6	4.1	4.1	4.09	4.07	4.05	4.03	4.01	3.98
single____LY_M3_w2____stack6	3.89	3.88	3.87	3.86	3.84	3.82	3.79	3.77
single_ss_LY_M3_w2_s1_stack6	4.85	4.85	4.84	4.82	4.8	4.78	4.76	4.73
single_ss_LY_M3_w2_s2_stack6	6.5	6.49	6.48	6.47	6.45	6.43	6.41	6.38
single____AM_M3_w1____stack6	3.92	3.92	3.91	3.89	3.88	3.86	3.83	3.8
single_ss_AM_M3_w1_s1_stack6	-2.38	-2.39	-2.4	-2.41	-2.43	-2.45	-2.47	-2.5
single_ss_AM_M3_w1_s2_stack6	2.1	2.09	2.08	2.07	2.05	2.03	2.01	1.99
single____AM_M3_w2____stack6	2.85	2.84	2.83	2.82	2.8	2.79	2.76	2.73
single_ss_AM_M3_w2_s1_stack6	0.68	0.68	0.67	0.65	0.64	0.62	0.59	0.57
single_ss_AM_M3_w2_s2_stack6	4.04	4.03	4.03	4.01	4	3.98	3.95	3.93
single____LY_MQ_w1____stack6	1.19	1.18	1.17	1.16	1.14	1.12	1.09	1.07
single_ss_LY_MQ_w1_s1_stack6	-2.67	-2.68	-2.69	-2.71	-2.73	-2.75	-2.77	-2.8
single_ss_LY_MQ_w1_s2_stack6	3.92	3.91	3.9	3.89	3.87	3.85	3.83	3.8
single____LY_MQ_w2____stack6	0.68	0.67	0.66	0.65	0.63	0.61	0.59	0.56
single_ss_LY_MQ_w2_s1_stack6	3.9	3.9	3.89	3.87	3.86	3.83	3.81	3.78
single_ss_LY_MQ_w2_s2_stack6	4.37	4.36	4.35	4.34	4.32	4.3	4.28	4.25
single____AM_MQ_w1____stack6	2.1	2.09	2.08	2.07	2.05	2.03	2.01	1.98
single_ss_AM_MQ_w1_s1_stack6	-2.18	-2.19	-2.2	-2.21	-2.23	-2.25	-2.27	-2.3
single_ss_AM_MQ_w1_s2_stack6	1.12	1.11	1.11	1.09	1.08	1.06	1.03	1.01
single____AM_MQ_w2____stack6	1.43	1.42	1.41	1.4	1.38	1.37	1.34	1.32
single_ss_AM_MQ_w2_s1_stack6	0.81	0.81	0.8	0.78	0.77	0.75	0.72	0.7
single_ss_AM_MQ_w2_s2_stack6	3.27	3.26	3.26	3.24	3.23	3.21	3.18	3.16
single____AM_LY_w1____stack6	3.09	3.08	3.07	3.06	3.04	3.02	3	2.97
single_ss_AM_LY_w1_s1_stack6	-0.17	-0.18	-0.19	-0.2	-0.22	-0.24	-0.27	-0.29
single_ss_AM_LY_w1_s2_stack6	-2.69	-2.7	-2.71	-2.72	-2.74	-2.75	-2.78	-2.8
single____AM_LY_w2____stack6	2.72	2.72	2.71	2.69	2.68	2.66	2.63	2.6
single_ss_AM_LY_w2_s1_stack6	4.21	4.21	4.2	4.18	4.16	4.14	4.12	4.09
single_ss_AM_LY_w2_s2_stack6	3.83	3.83	3.82	3.8	3.79	3.77	3.74	3.71
single____M2_M1_w1____stack7	3.36	3.35	3.34	3.33	3.31	3.28	3.25	3.22
single_ss_M2_M1_w1_s1_stack7	-9.86	-9.87	-9.88	-9.9	-9.93	-9.95	-9.99	-10.02

Table 88. Capacitance with Fill (% difference Model-Z2D)/Z2D*100)

Testcase	10.5 GHz	20.5 GHz	30.5 GHz	40.5 GHz	50.5 GHz	60.5 GHz	70.5 GHz	80.5 GHz
single_ss_M2_M1_w1_s2_stack7	6.59	6.58	6.57	6.55	6.52	6.5	6.46	6.42
single____M2_M1_w2____stack7	1.5	1.49	1.48	1.46	1.44	1.41	1.37	1.34
single_ss_M2_M1_w2_s1_stack7	7.12	7.11	7.09	7.07	7.04	7.01	6.97	6.93
single_ss_M2_M1_w2_s2_stack7	7.68	7.67	7.66	7.63	7.6	7.56	7.52	7.47
single____M3_M1_w1____stack7	18.44	18.43	18.42	18.4	18.38	18.35	18.31	18.27
single_ss_M3_M1_w1_s1_stack7	-12.98	-12.98	-13	-13.02	-13.05	-13.08	-13.12	-13.17
single_ss_M3_M1_w1_s2_stack7	10.97	10.97	10.95	10.94	10.91	10.89	10.86	10.82
single____M3_M1_w2____stack7	16.53	16.53	16.51	16.49	16.47	16.44	16.4	16.36
single_ss_M3_M1_w2_s1_stack7	19.19	19.18	19.16	19.14	19.11	19.08	19.04	19
single_ss_M3_M1_w2_s2_stack7	22.85	22.84	22.83	22.8	22.78	22.74	22.7	22.66
single____M4_M1_w1____stack7	27.19	27.18	27.17	27.15	27.12	27.09	27.05	27
single_ss_M4_M1_w1_s1_stack7	-14.16	-14.17	-14.19	-14.21	-14.24	-14.28	-14.32	-14.37
single_ss_M4_M1_w1_s2_stack7	16.87	16.86	16.85	16.83	16.8	16.77	16.73	16.69
single____M4_M1_w2____stack7	21.96	21.95	21.93	21.91	21.89	21.86	21.82	21.78
single_ss_M4_M1_w2_s1_stack7	20.89	20.88	20.87	20.84	20.82	20.78	20.74	20.7
single_ss_M4_M1_w2_s2_stack7	28.1	28.09	28.07	28.05	28.02	27.99	27.95	27.9
single____MQ_M1_w1____stack7	22.94	22.93	22.92	22.9	22.87	22.84	22.8	22.76
single_ss_MQ_M1_w1_s1_stack7	-14.55	-14.56	-14.57	-14.59	-14.61	-14.64	-14.67	-14.7
single_ss_MQ_M1_w1_s2_stack7	-1.64	-1.64	-1.65	-1.67	-1.69	-1.71	-1.74	-1.77
single____MQ_M1_w2____stack7	19.07	19.07	19.05	19.03	19.01	18.98	18.95	18.91
single_ss_MQ_M1_w2_s1_stack7	15.15	15.14	15.13	15.11	15.08	15.05	15.02	14.98
single_ss_MQ_M1_w2_s2_stack7	21.13	21.12	21.1	21.08	21.06	21.03	21	20.96
single____LY_M1_w1____stack7	12.03	12.02	12.01	11.99	11.97	11.95	11.92	11.88
single_ss_LY_M1_w1_s1_stack7	-4.22	-4.23	-4.24	-4.25	-4.27	-4.29	-4.32	-4.34
single_ss_LY_M1_w1_s2_stack7	9.63	9.62	9.61	9.6	9.58	9.56	9.53	9.5
single____LY_M1_w2____stack7	9.15	9.15	9.14	9.12	9.1	9.08	9.05	9.02
single_ss_LY_M1_w2_s1_stack7	5.77	5.77	5.76	5.74	5.73	5.7	5.68	5.65
single_ss_LY_M1_w2_s2_stack7	10.68	10.67	10.66	10.65	10.63	10.61	10.58	10.55
single____AM_M1_w1____stack7	7.36	7.35	7.34	7.33	7.31	7.29	7.27	7.24
single_ss_AM_M1_w1_s1_stack7	-2.62	-2.62	-2.63	-2.65	-2.66	-2.68	-2.7	-2.73
single_ss_AM_M1_w1_s2_stack7	3.33	3.33	3.32	3.31	3.29	3.27	3.25	3.22
single____AM_M1_w2____stack7	5.64	5.64	5.63	5.61	5.59	5.57	5.55	5.52
single_ss_AM_M1_w2_s1_stack7	0.57	0.56	0.55	0.54	0.52	0.5	0.48	0.45
single_ss_AM_M1_w2_s2_stack7	5.34	5.34	5.33	5.31	5.3	5.28	5.25	5.23
single____M3_M2_w1____stack7	3.27	3.27	3.25	3.24	3.22	3.19	3.16	3.13
single_ss_M3_M2_w1_s1_stack7	-9.87	-9.88	-9.89	-9.91	-9.93	-9.96	-9.99	-10.03



Table 88. Capacitance with Fill (% difference Model-Z2D)/Z2D*100)

Testcase	10.5 GHz	20.5 GHz	30.5 GHz	40.5 GHz	50.5 GHz	60.5 GHz	70.5 GHz	80.5 GHz
single_ss_M3_M2_w1_s2_stack7	6.57	6.56	6.55	6.53	6.51	6.48	6.45	6.41
single____M3_M2_w2____stack7	1.5	1.49	1.48	1.46	1.43	1.4	1.37	1.33
single_ss_M3_M2_w2_s1_stack7	7.12	7.11	7.09	7.07	7.04	7.01	6.97	6.93
single_ss_M3_M2_w2_s2_stack7	7.68	7.67	7.66	7.63	7.6	7.56	7.52	7.47
single____M4_M2_w1____stack7	18.4	18.39	18.38	18.36	18.33	18.3	18.27	18.23
single_ss_M4_M2_w1_s1_stack7	-12.88	-12.89	-12.91	-12.93	-12.96	-12.99	-13.03	-13.08
single_ss_M4_M2_w1_s2_stack7	11.02	11.01	11	10.98	10.96	10.94	10.9	10.87
single____M4_M2_w2____stack7	16.58	16.57	16.56	16.54	16.52	16.49	16.45	16.41
single_ss_M4_M2_w2_s1_stack7	19.3	19.29	19.28	19.26	19.23	19.2	19.16	19.11
single_ss_M4_M2_w2_s2_stack7	22.95	22.94	22.92	22.9	22.87	22.84	22.8	22.75
single____MQ_M2_w1____stack7	17.47	17.46	17.45	17.43	17.4	17.38	17.34	17.3
single_ss_MQ_M2_w1_s1_stack7	-13.74	-13.75	-13.76	-13.78	-13.8	-13.83	-13.86	-13.9
single_ss_MQ_M2_w1_s2_stack7	-1.79	-1.79	-1.8	-1.82	-1.84	-1.86	-1.88	-1.91
single____MQ_M2_w2____stack7	15.39	15.38	15.37	15.35	15.32	15.3	15.26	15.23
single_ss_MQ_M2_w2_s1_stack7	14.66	14.65	14.63	14.61	14.59	14.56	14.53	14.49
single_ss_MQ_M2_w2_s2_stack7	18.87	18.86	18.84	18.83	18.8	18.77	18.74	18.7
single____LY_M2_w1____stack7	9.89	9.88	9.87	9.85	9.83	9.81	9.78	9.75
single_ss_LY_M2_w1_s1_stack7	-3.97	-3.97	-3.98	-4	-4.02	-4.04	-4.06	-4.09
single_ss_LY_M2_w1_s2_stack7	8.16	8.16	8.15	8.13	8.11	8.09	8.07	8.04
single____LY_M2_w2____stack7	7.61	7.6	7.59	7.58	7.56	7.54	7.51	7.48
single_ss_LY_M2_w2_s1_stack7	5.67	5.66	5.65	5.64	5.62	5.6	5.57	5.54
single_ss_LY_M2_w2_s2_stack7	9.55	9.54	9.53	9.52	9.5	9.48	9.45	9.42
single____AM_M2_w1____stack7	6.24	6.24	6.23	6.21	6.2	6.17	6.15	6.12
single_ss_AM_M2_w1_s1_stack7	-2.54	-2.55	-2.56	-2.57	-2.59	-2.61	-2.63	-2.66
single_ss_AM_M2_w1_s2_stack7	2.99	2.98	2.97	2.96	2.94	2.93	2.9	2.88
single____AM_M2_w2____stack7	4.77	4.76	4.76	4.74	4.73	4.7	4.68	4.65
single_ss_AM_M2_w2_s1_stack7	0.63	0.62	0.61	0.6	0.59	0.57	0.54	0.51
single_ss_AM_M2_w2_s2_stack7	4.99	4.99	4.98	4.96	4.95	4.93	4.9	4.88
single____M4_M3_w1____stack7	3.27	3.27	3.25	3.24	3.22	3.19	3.16	3.13
single_ss_M4_M3_w1_s1_stack7	-9.78	-9.79	-9.8	-9.82	-9.84	-9.87	-9.91	-9.94
single_ss_M4_M3_w1_s2_stack7	6.6	6.59	6.58	6.56	6.54	6.51	6.47	6.44
single____M4_M3_w2____stack7	1.5	1.49	1.48	1.46	1.43	1.4	1.37	1.33
single_ss_M4_M3_w2_s1_stack7	7.14	7.14	7.12	7.1	7.07	7.04	7	6.95
single_ss_M4_M3_w2_s2_stack7	7.7	7.69	7.67	7.65	7.62	7.58	7.54	7.49
single____MQ_M3_w1____stack7	10.11	10.1	10.09	10.07	10.05	10.03	10	9.96
single_ss_MQ_M3_w1_s1_stack7	-12.5	-12.51	-12.52	-12.54	-12.56	-12.58	-12.61	-12.65

Table 88. Capacitance with Fill (% difference Model-Z2D)/Z2D*100)

Testcase	10.5 GHz	20.5 GHz	30.5 GHz	40.5 GHz	50.5 GHz	60.5 GHz	70.5 GHz	80.5 GHz
single_ss_MQ_M3_w1_s2_stack7	-4.14	-4.14	-4.15	-4.17	-4.18	-4.2	-4.23	-4.25
single____MQ_M3_w2____stack7	9.06	9.05	9.04	9.02	9	8.98	8.94	8.91
single_ss_MQ_M3_w2_s1_stack7	11.57	11.56	11.54	11.52	11.5	11.47	11.44	11.4
single_ss_MQ_M3_w2_s2_stack7	13.61	13.6	13.59	13.57	13.55	13.52	13.49	13.45
single____LY_M3_w1____stack7	7.61	7.6	7.59	7.57	7.56	7.53	7.51	7.47
single_ss_LY_M3_w1_s1_stack7	-3.69	-3.7	-3.71	-3.72	-3.74	-3.76	-3.79	-3.81
single_ss_LY_M3_w1_s2_stack7	6.35	6.34	6.33	6.32	6.3	6.28	6.25	6.23
single____LY_M3_w2____stack7	5.86	5.86	5.85	5.83	5.81	5.79	5.77	5.74
single_ss_LY_M3_w2_s1_stack7	5.38	5.37	5.36	5.35	5.33	5.31	5.29	5.26
single_ss_LY_M3_w2_s2_stack7	8.17	8.16	8.15	8.14	8.12	8.1	8.08	8.05
single____AM_M3_w1____stack7	5.1	5.09	5.08	5.07	5.05	5.03	5.01	4.98
single_ss_AM_M3_w1_s1_stack7	-2.46	-2.47	-2.48	-2.49	-2.51	-2.53	-2.55	-2.58
single_ss_AM_M3_w1_s2_stack7	2.58	2.57	2.57	2.55	2.54	2.52	2.49	2.47
single____AM_M3_w2____stack7	3.85	3.84	3.83	3.82	3.8	3.78	3.76	3.73
single_ss_AM_M3_w2_s1_stack7	0.67	0.66	0.65	0.64	0.62	0.6	0.58	0.55
single_ss_AM_M3_w2_s2_stack7	4.57	4.56	4.55	4.54	4.52	4.5	4.48	4.45
single____MQ_M4_w1____stack7	-2.1	-2.11	-2.12	-2.13	-2.15	-2.17	-2.2	-2.23
single_ss_MQ_M4_w1_s1_stack7	-11.16	-11.17	-11.18	-11.19	-11.21	-11.24	-11.26	-11.3
single_ss_MQ_M4_w1_s2_stack7	-6.65	-6.66	-6.67	-6.68	-6.7	-6.72	-6.74	-6.77
single____MQ_M4_w2____stack7	-3.82	-3.83	-3.84	-3.85	-3.87	-3.9	-3.92	-3.96
single_ss_MQ_M4_w2_s1_stack7	1.13	1.12	1.11	1.09	1.07	1.04	1.01	0.98
single_ss_MQ_M4_w2_s2_stack7	1.42	1.41	1.4	1.38	1.36	1.33	1.3	1.27
single____LY_M4_w1____stack7	5.15	5.15	5.14	5.12	5.1	5.08	5.05	5.03
single_ss_LY_M4_w1_s1_stack7	-3.39	-3.4	-3.41	-3.42	-3.44	-3.46	-3.49	-3.52
single_ss_LY_M4_w1_s2_stack7	4.1	4.1	4.09	4.07	4.05	4.03	4.01	3.98
single____LY_M4_w2____stack7	3.89	3.88	3.87	3.86	3.84	3.82	3.79	3.77
single_ss_LY_M4_w2_s1_stack7	4.85	4.85	4.84	4.82	4.8	4.78	4.76	4.73
single_ss_LY_M4_w2_s2_stack7	6.5	6.49	6.48	6.47	6.45	6.43	6.41	6.38
single____AM_M4_w1____stack7	3.92	3.92	3.91	3.89	3.88	3.86	3.83	3.8
single_ss_AM_M4_w1_s1_stack7	-2.38	-2.39	-2.4	-2.41	-2.43	-2.45	-2.47	-2.5
single_ss_AM_M4_w1_s2_stack7	2.1	2.09	2.08	2.07	2.05	2.03	2.01	1.99
single____AM_M4_w2____stack7	2.85	2.84	2.83	2.82	2.8	2.79	2.76	2.73
single_ss_AM_M4_w2_s1_stack7	0.68	0.68	0.67	0.65	0.64	0.62	0.59	0.57
single_ss_AM_M4_w2_s2_stack7	4.04	4.03	4.03	4.01	4	3.98	3.95	3.93
single____LY_MQ_w1____stack7	1.19	1.18	1.17	1.16	1.14	1.12	1.09	1.07
single_ss_LY_MQ_w1_s1_stack7	-2.67	-2.68	-2.69	-2.71	-2.73	-2.75	-2.77	-2.8

Table 88. Capacitance with Fill (% difference Model-Z2D)/Z2D*100)

Testcase	10.5 GHz	20.5 GHz	30.5 GHz	40.5 GHz	50.5 GHz	60.5 GHz	70.5 GHz	80.5 GHz
single_ss_LY_MQ_w1_s2_stack7	3.92	3.91	3.9	3.89	3.87	3.85	3.83	3.8
single____LY_MQ_w2____stack7	0.68	0.67	0.66	0.65	0.63	0.61	0.59	0.56
single_ss_LY_MQ_w2_s1_stack7	3.9	3.9	3.89	3.87	3.86	3.83	3.81	3.78
single_ss_LY_MQ_w2_s2_stack7	4.37	4.36	4.35	4.34	4.32	4.3	4.28	4.25
single____AM_MQ_w1____stack7	2.1	2.09	2.08	2.07	2.05	2.03	2.01	1.98
single_ss_AM_MQ_w1_s1_stack7	-2.18	-2.19	-2.2	-2.21	-2.23	-2.25	-2.27	-2.3
single_ss_AM_MQ_w1_s2_stack7	1.12	1.11	1.11	1.09	1.08	1.06	1.03	1.01
single____AM_MQ_w2____stack7	1.43	1.42	1.41	1.4	1.38	1.37	1.34	1.32
single_ss_AM_MQ_w2_s1_stack7	0.81	0.81	0.8	0.78	0.77	0.75	0.72	0.7
single_ss_AM_MQ_w2_s2_stack7	3.27	3.26	3.26	3.24	3.23	3.21	3.18	3.16
single____AM_LY_w1____stack7	3.09	3.08	3.07	3.06	3.04	3.02	3	2.97
single_ss_AM_LY_w1_s1_stack7	-0.17	-0.18	-0.19	-0.2	-0.22	-0.24	-0.27	-0.29
single_ss_AM_LY_w1_s2_stack7	-2.69	-2.7	-2.71	-2.72	-2.74	-2.75	-2.78	-2.8
single____AM_LY_w2____stack7	2.72	2.72	2.71	2.69	2.68	2.66	2.63	2.6
single_ss_AM_LY_w2_s1_stack7	4.21	4.21	4.2	4.18	4.16	4.14	4.12	4.09
single_ss_AM_LY_w2_s2_stack7	3.83	3.83	3.82	3.8	3.79	3.77	3.74	3.71

15.4 Model versus EM Solver Plots (singlecpw, coupledcpw)

The singlecpw and coupledcpw model were verified against z2d which is an IBM internal 2-D field solver that solves for frequency dependent resistance, capacitance, and inductance. In Figures 327-338, plots of frequency-dependent resistance, capacitance, inductance, and conductance (from signal line to grounded side shields...always zero potential) are shown. In Figures 339-342, spectre simulation of the coupledcpw model is shown compared to z2d. The self and mutual terms of capacitance and inductance are shown with frequency as well as resistance. The frequency-dependent resistance, capacitance, inductance, and conductance of the singlecpw and coupledcpw models were derived from frequency-dependent spectre S-parameter simulations of the models under the various geometries. The output of z2d is already in terms of frequency-dependent R, C, L, and G...so no conversion is needed for the z2d data. The data from z2d is the direct output of the tool. In the z2d simulations, the top of the silicon substrate is modelled as a grounded conductor. Thus, there is no frequency-dependent decrease of capacitance modelled in z2d when the signal line is exposed to the substrate (crossing="none"). Fill is not modelled in the z2d simulations. So, all capacitance in the z2d simulation is that predicted for the geometry without fill. Again, the field solver used to verify the singlecpw and coupledcpw models was z2d which is an IBM 2-D field solver "owned" by Alina Deutsch and her Interconnect and Packaging Analysis group (deutsch@us.ibm.com) at IBM's TJ Watson Research Center in Yorktown Heights, NY.

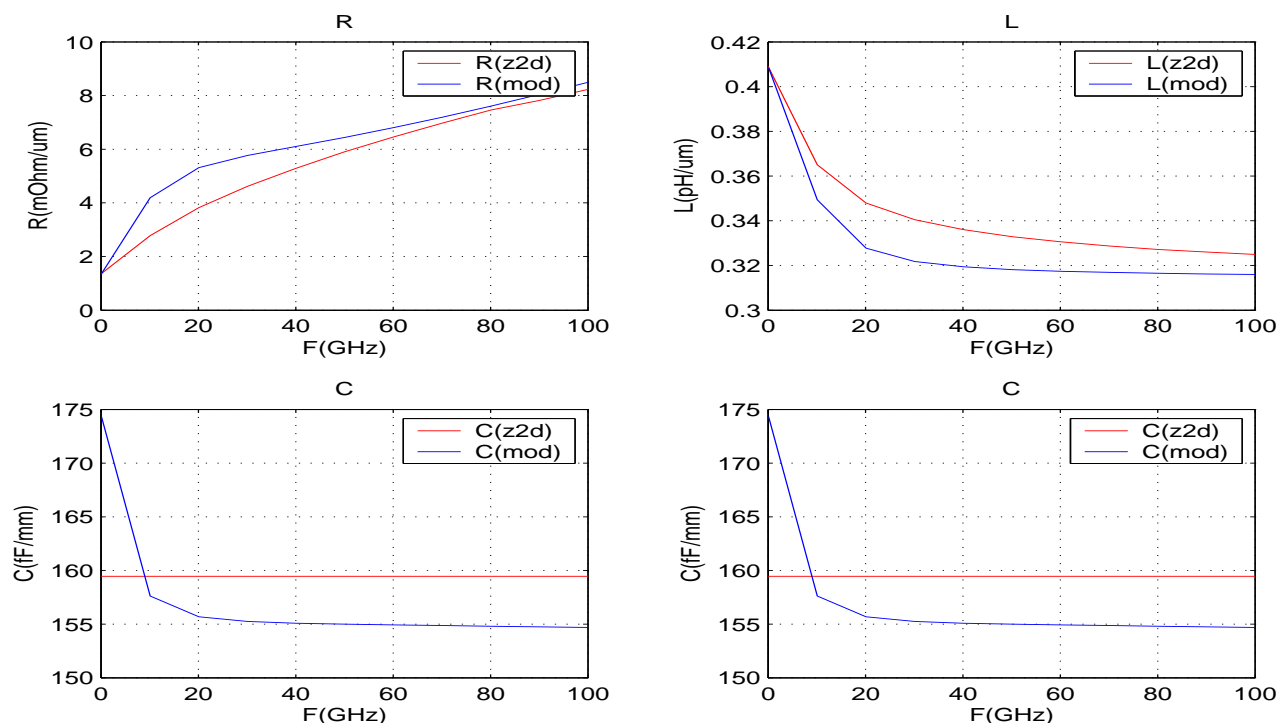


Figure 327. Simulated singlecpw: AM over Si (crossing="none"), $w=5\mu\text{m}$, $s=5\mu\text{m}$, $n\text{lev}=5$.

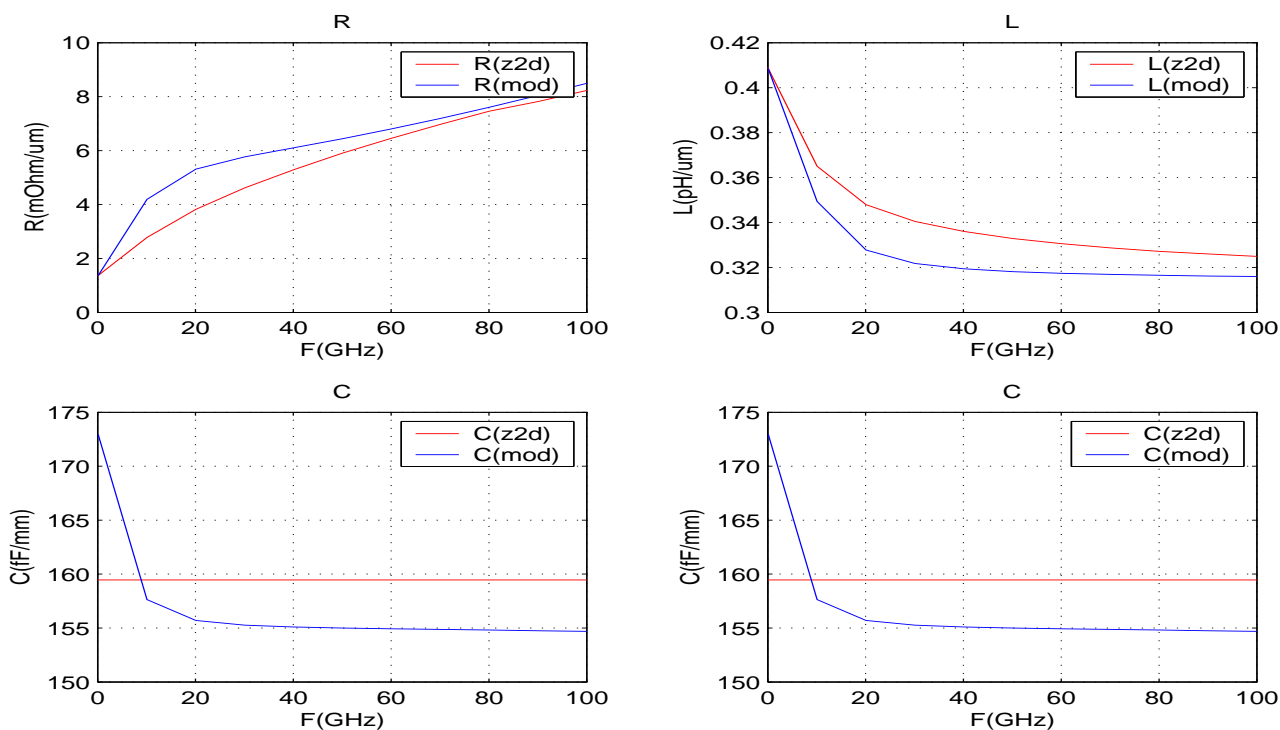


Figure 328. Simulated singlecpw: AM over Si (crossing="none"), $w=5\mu\text{m}$, $s=5\mu\text{m}$, $n\text{lev}=5$ without metal fill.

Note: Above simulations for singlecpw AM over Silicon, $w=5\mu\text{m}$, $s=5\mu\text{m}$, $n\text{lev}=5$ with and without fill.

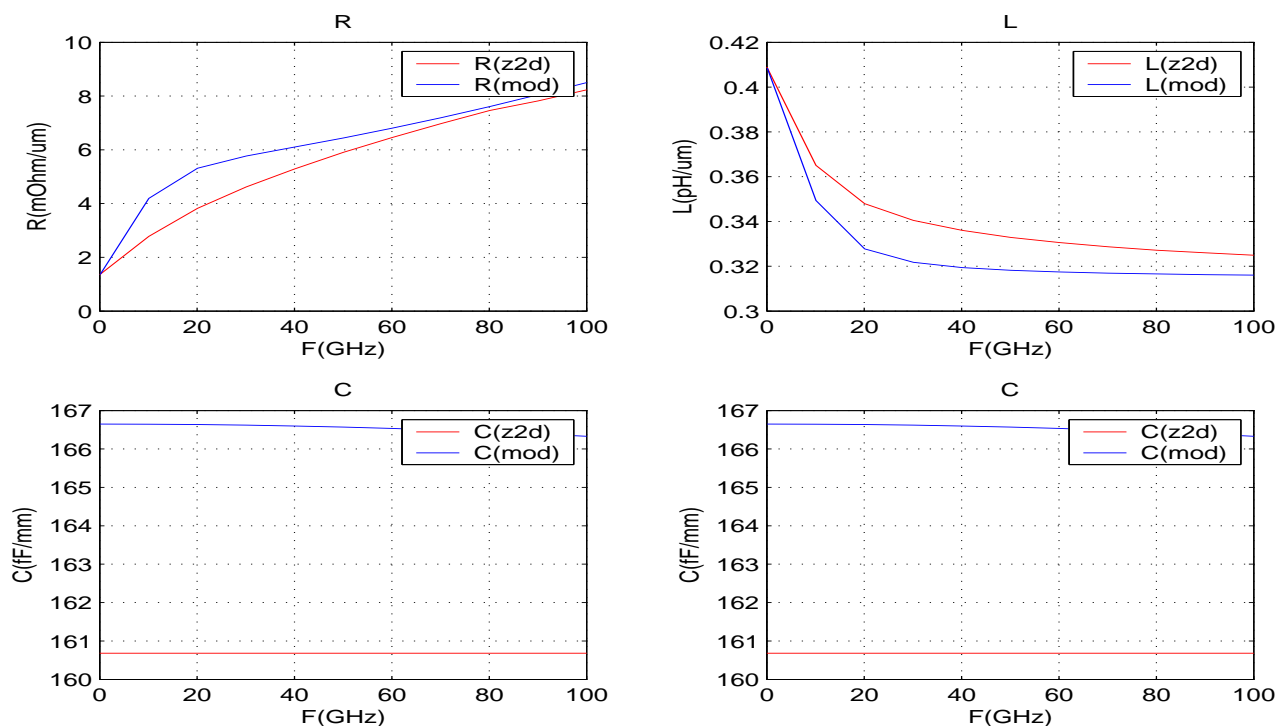


Figure 329. Simulated singlecpw: AM over M1 (crossing="below"), $w=5\mu\text{m}$, $s=5\mu\text{m}$, $nlev=5$.

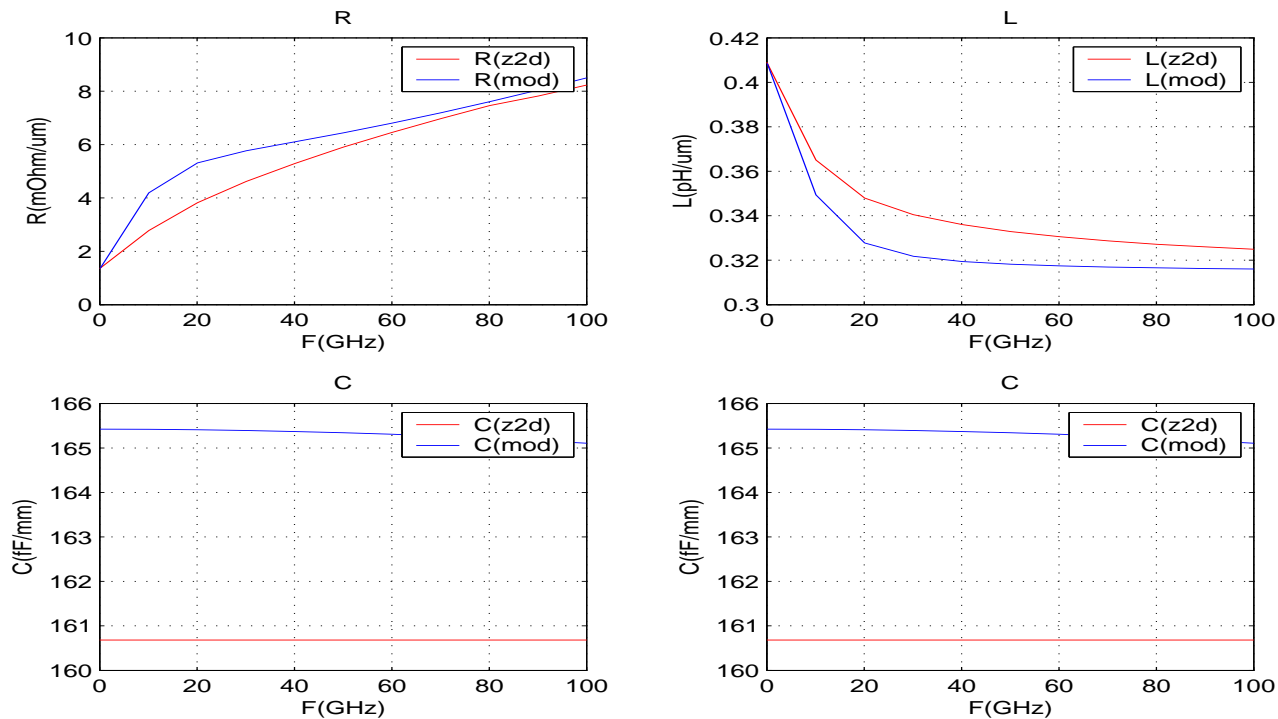


Figure 330. Simulated singlecpw: AM over M1 (crossing="below"), $w=5\mu\text{m}$, $s=5\mu\text{m}$, $nlev=5$ without metal fill.

Note: Above simulations for singlecpw, AM over M1, $w=5\mu\text{m}$, $s=5\mu\text{m}$, $nlev=5$ with and without fill.

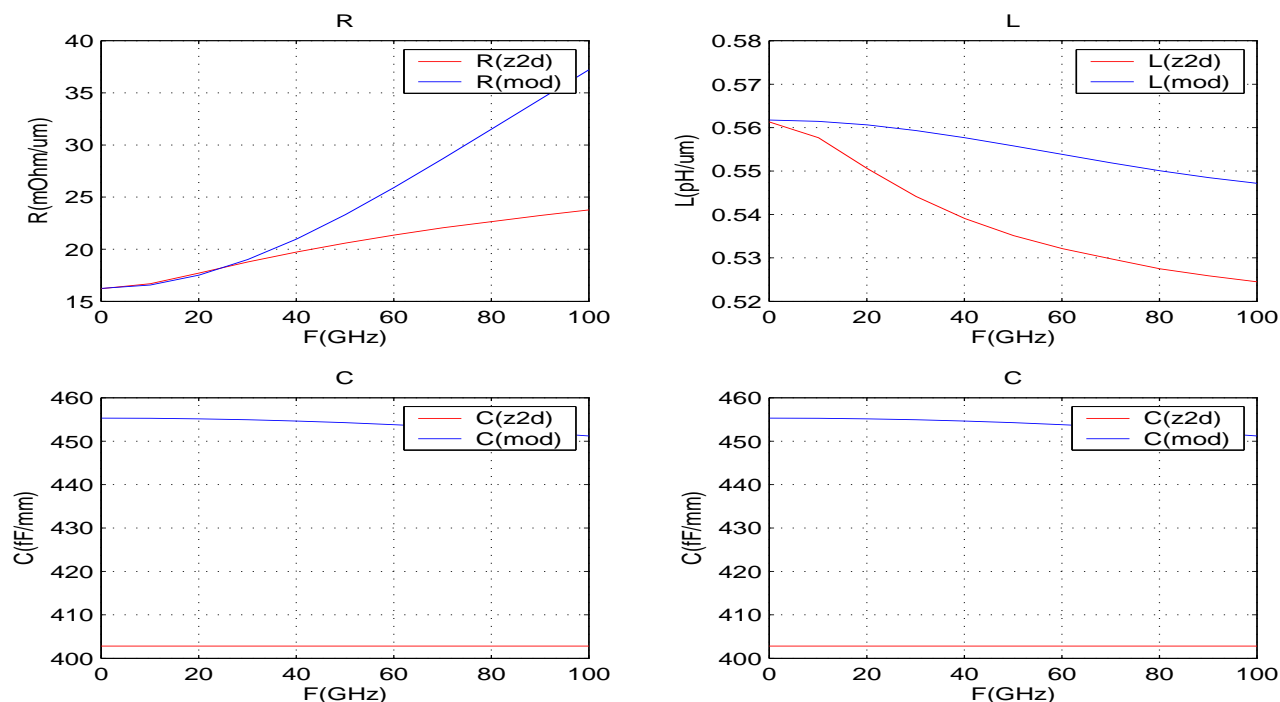


Figure 331. Simulated singlecpw: M3 over M1 under MQ, (crossing="both"), $w=5\mu\text{m}$, $s=5\mu\text{m}$, $nlev=7$

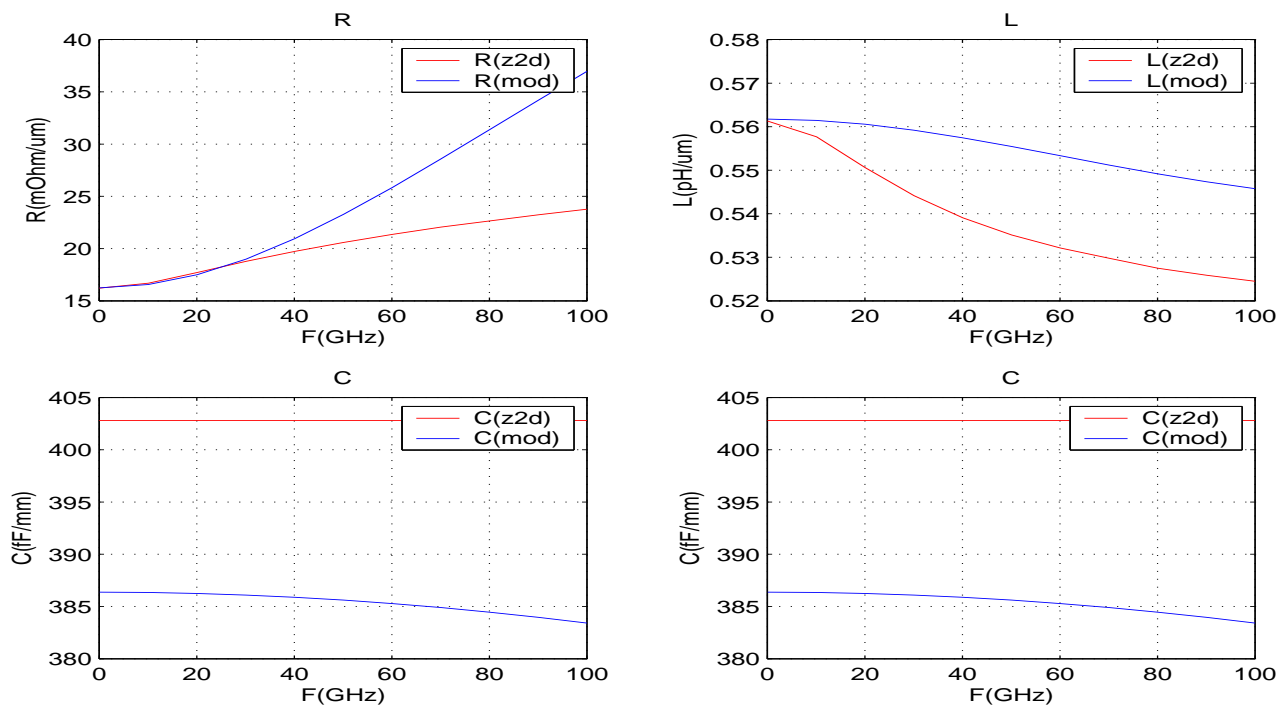


Figure 332. Simulated singlecpw: M3 over M1 under MQ (crossing="both"), $w=5\mu\text{m}$, $s=5\mu\text{m}$, $nlev=7$, without metal fill

Note: Above simulations for singlecpw, M3 over M1 under MQ, $w=5\mu\text{m}$, $s=5\mu\text{m}$, $nlev=7$ with and without fill .

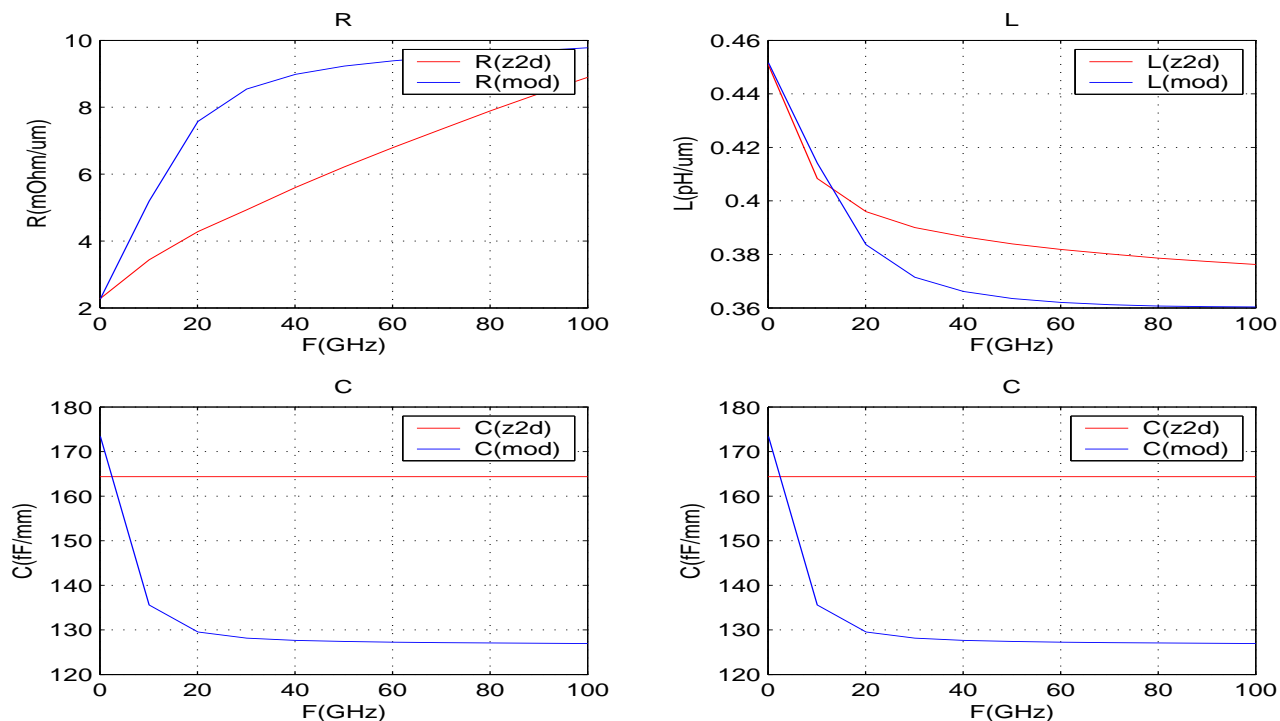


Figure 333. Simulated singlecpw: LY over Si(crossing="none"), $w=10\mu\text{m}$, $s=5\mu\text{m}$, $nlev=5$.

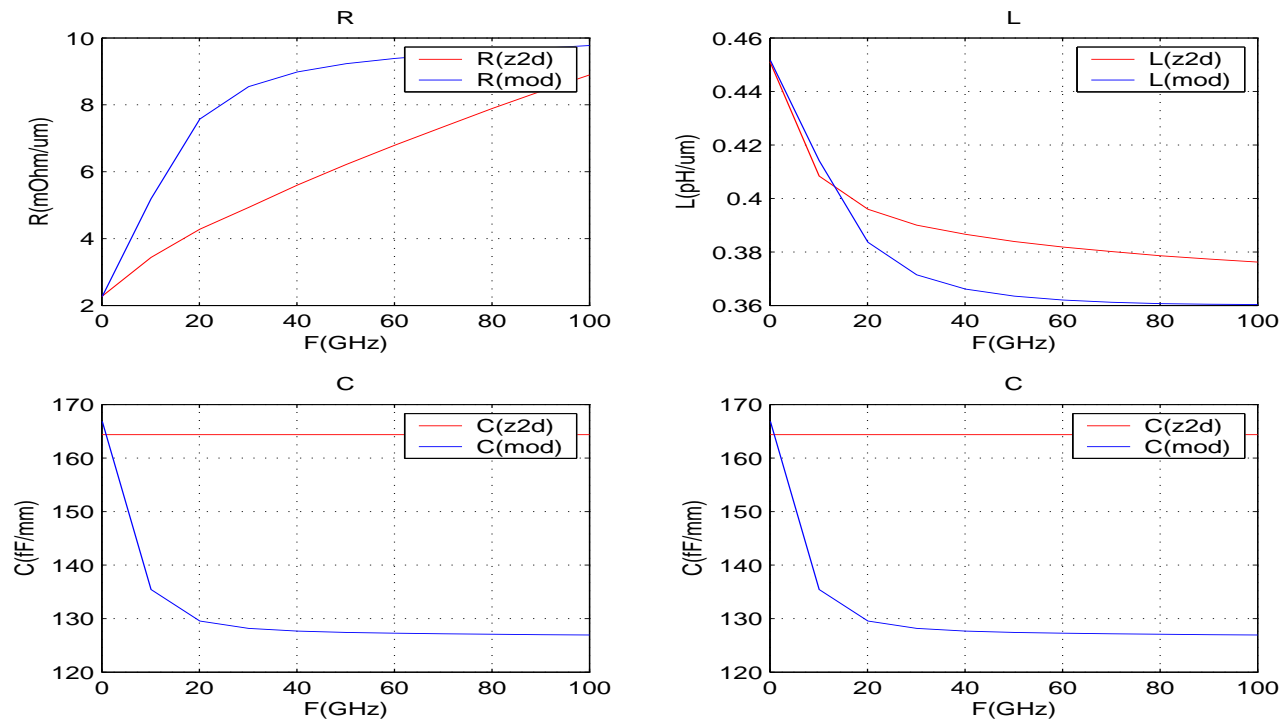


Figure 334. Simulated singlecpw: LY over Si(crossing="none"), $w=10\mu\text{m}$, $s=5\mu\text{m}$, $nlev=5$, without metal fill

Note: Above simulations for singlecpw LY over Si (crossing="none"), $w=10\mu\text{m}$, $s=5\mu\text{m}$, $nlev=5$ with and without fill.

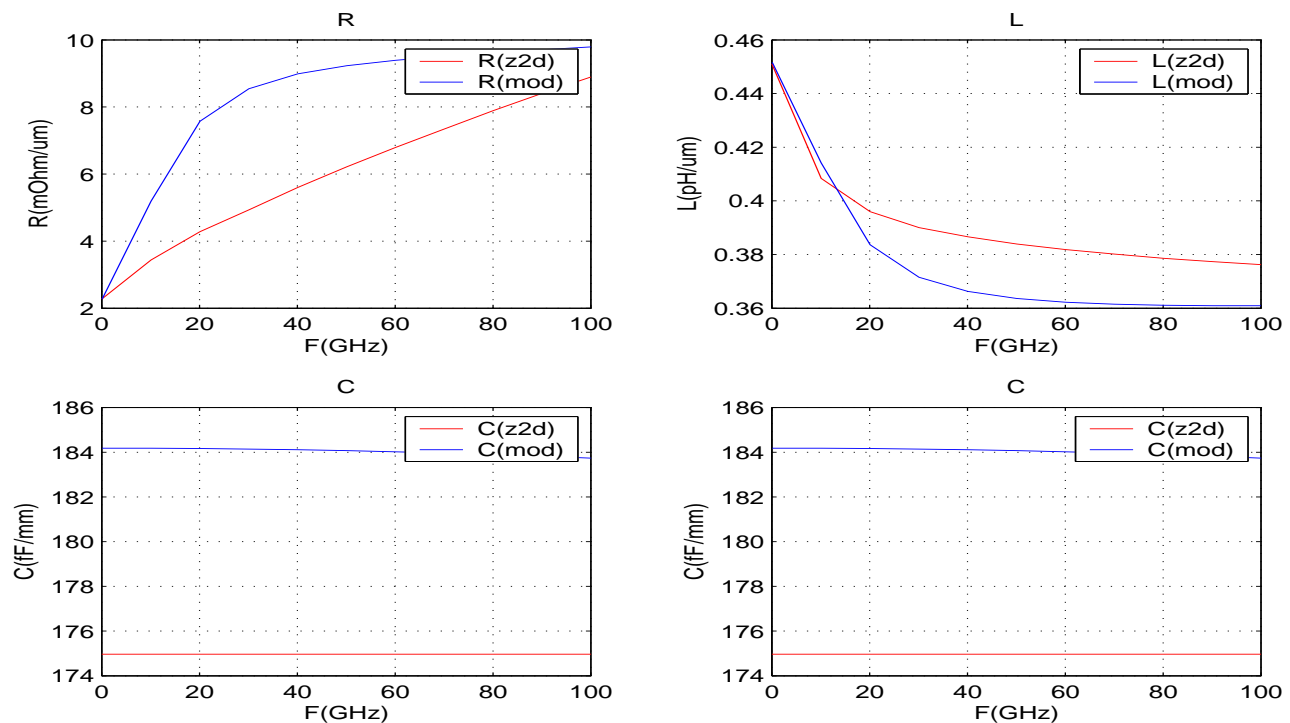


Figure 335. Simulated singlecpw: LY over M1 (crossing="below"), w=10um, s=5um, nlev=5.

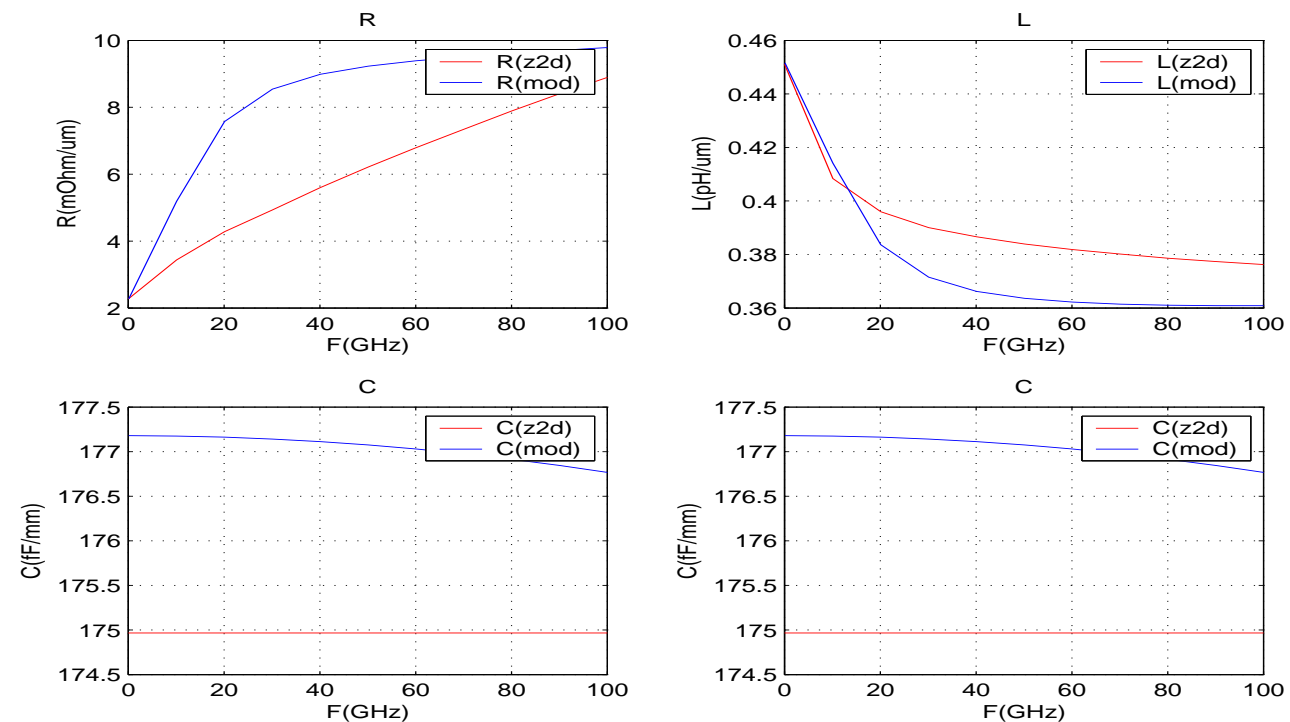


Figure 336. Simulated singlecpw: LY over M1 (crossing="below"), w=10um, s=5um, nlev=5 without metal fill

Note: Above simulations for singlecpw, LY over M1(crossing="below"), w=10um, nlev=5 with and without fill.

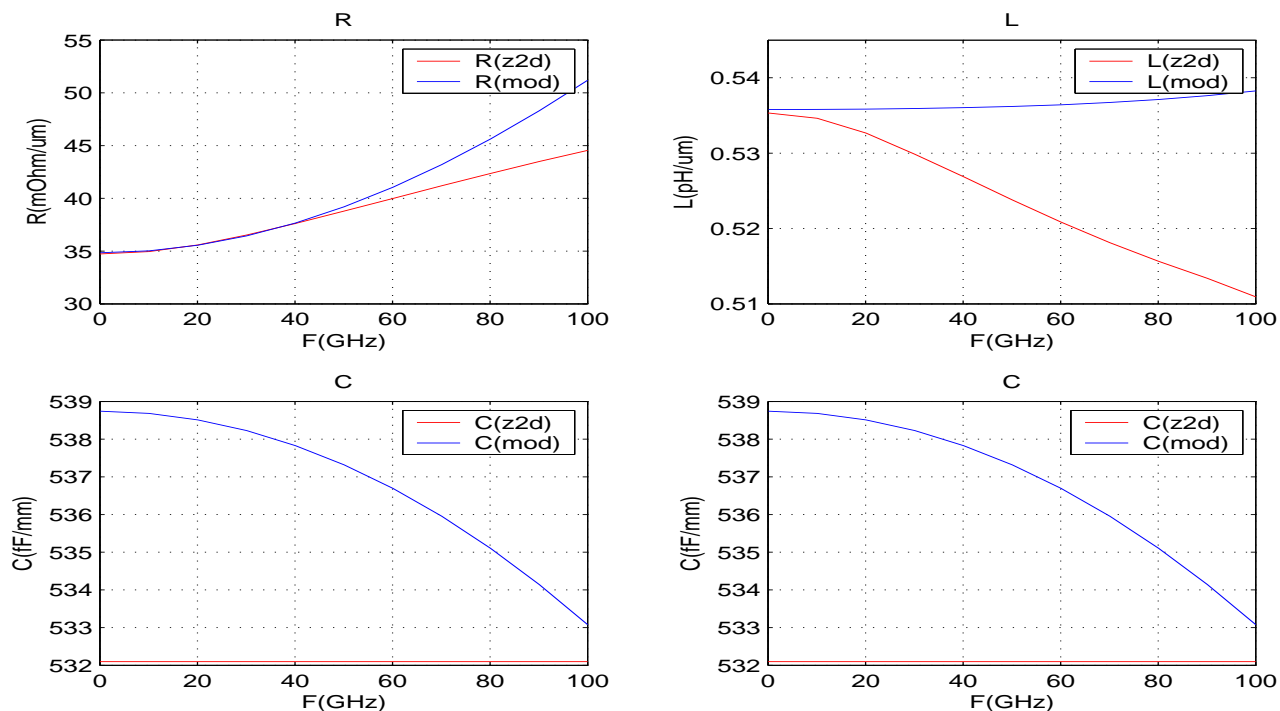


Figure 337. Simulated singlecpw: M2 over M1 under M3 (crossing="both"), $w=2\mu\text{m}$, $s=2\mu\text{m}$, $n\text{lev}=7$.

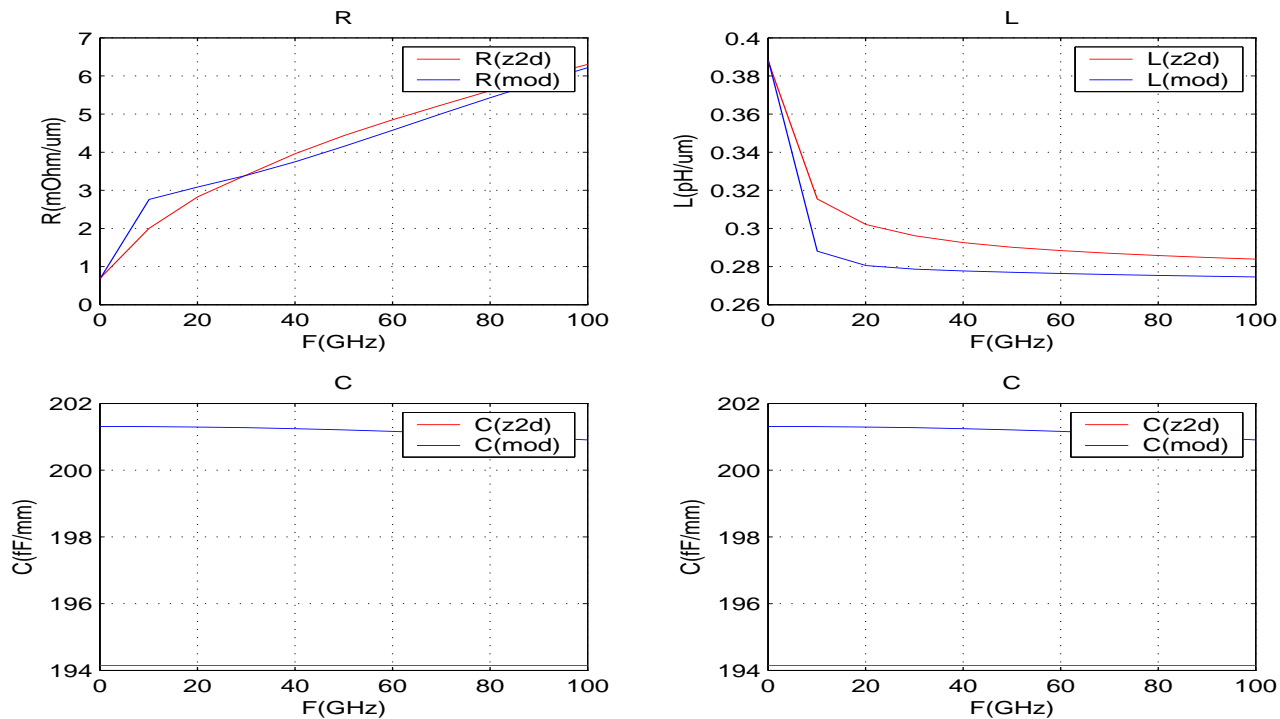


Figure 338. Simulated singlecpw: AM over MQ (crossing="below"), $w=10\mu\text{m}$, $s=5\mu\text{m}$, $n\text{lev}=5$.

Note: Above simulations for singlecpw, M2 over M1 under M3 and AM over M2 with metal fill.

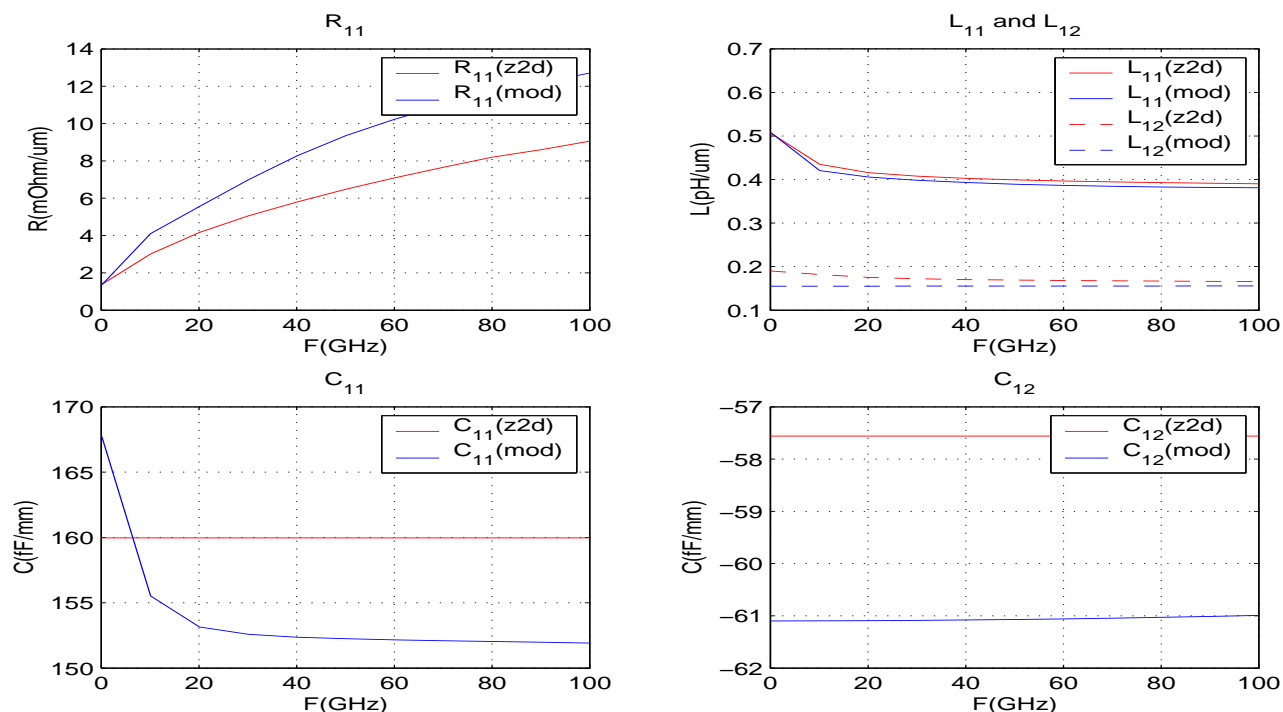


Figure 339. Simulated coupledcpw: AMover Si (crossing="none"), w=5um, s=5um, d=5um, nlev=5.

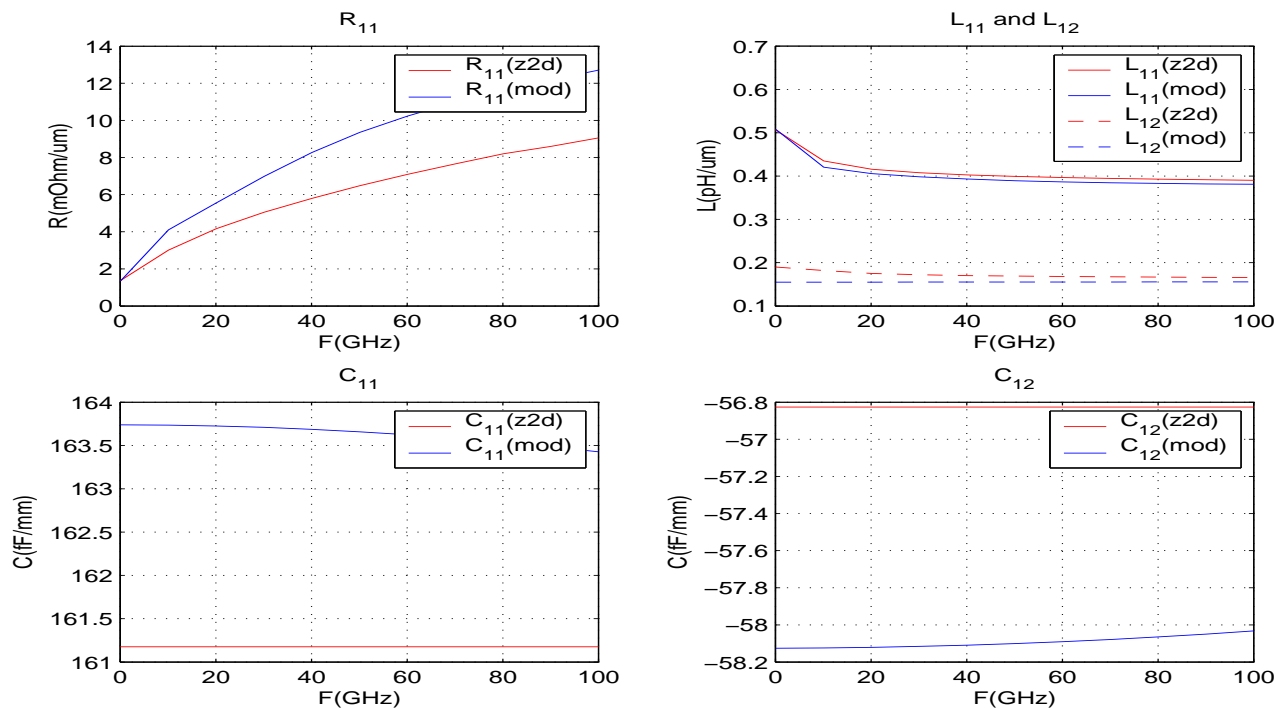


Figure 340. Simulated coupledcpw: AMover M1 (crossing="below"), w=5um, d=5um, s=5um, nlev=5.

Note: Above simulations for coupledcpw, AM over Si and AM over M1, s=w=d=5um, nlev=5 with metal fill

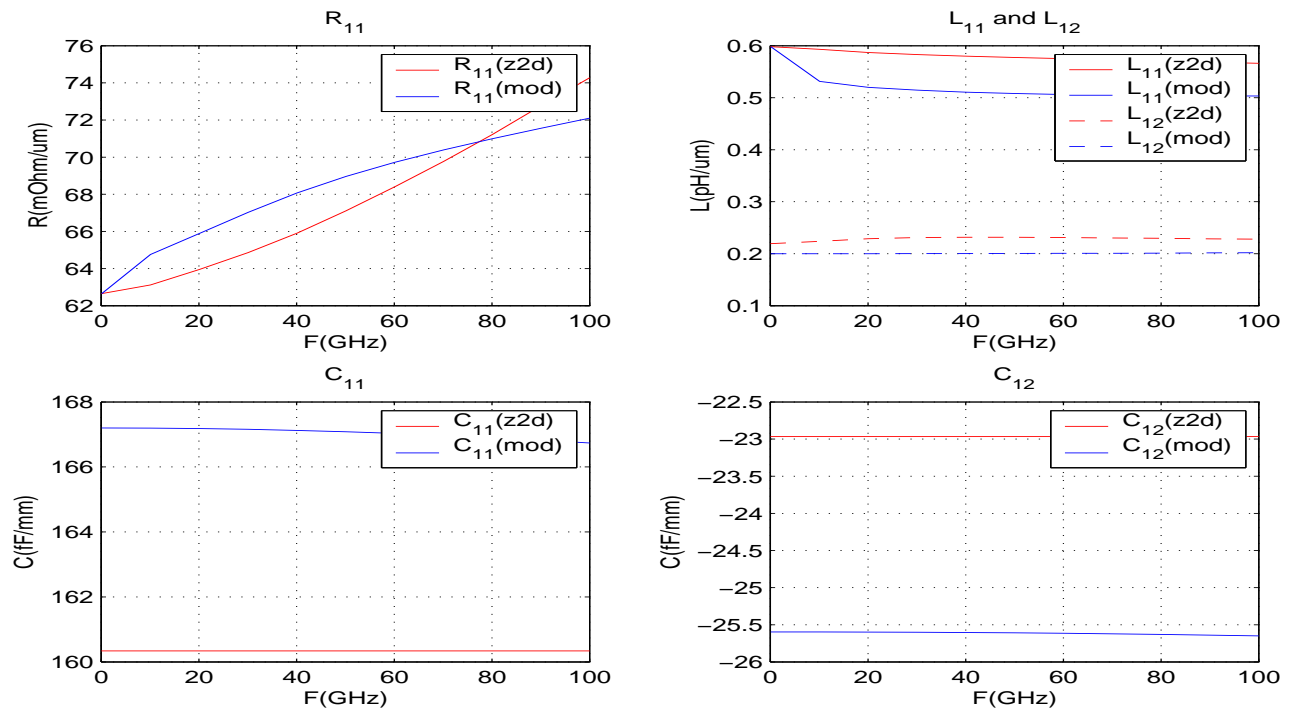


Figure 341. Simulated coupledcpw: M3 over M1 under MQ, $s=w=d=1\mu\text{m}$, $n\text{lev}=7$.

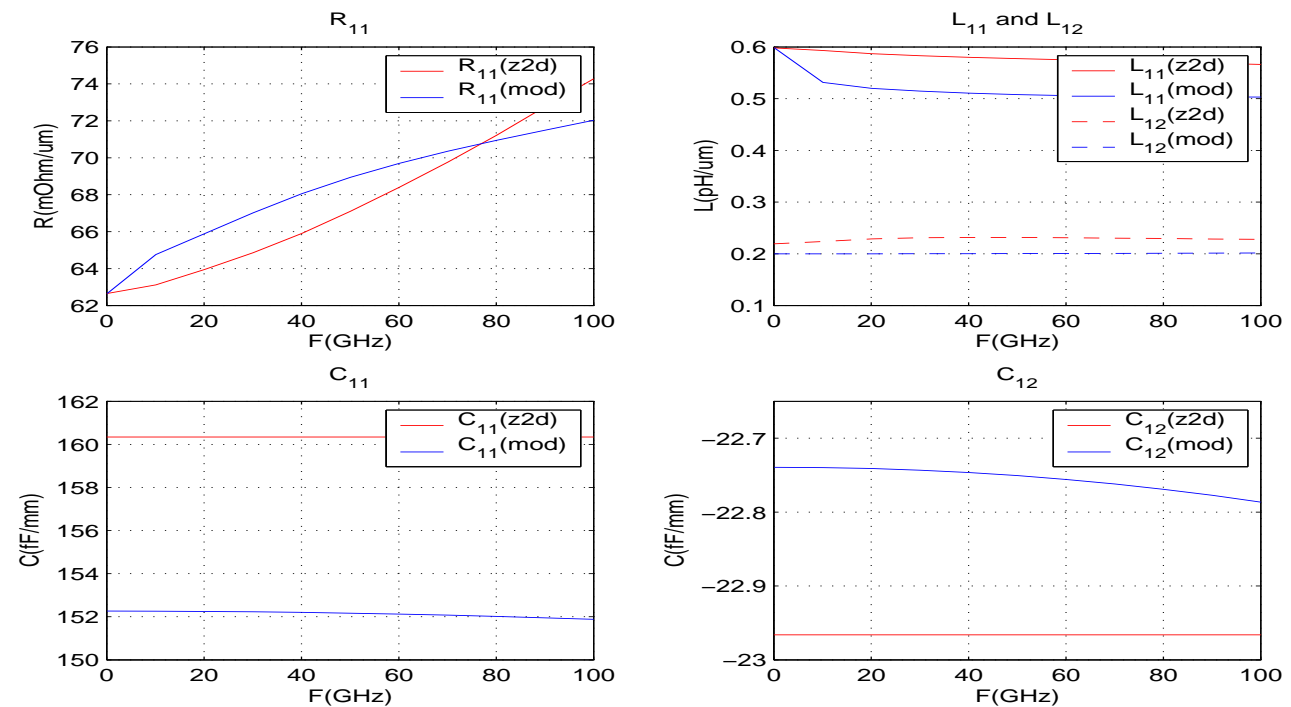


Figure 342. Simulated coupledcpw: M3 over M1 under MQ, $s=w=d=1\mu\text{m}$, $n\text{lev}=7$ without fill.

Note: Above simulations for coupledcpw, M3 over M1 under MQ, $s=w=d=1\mu\text{m}$, $n\text{lev}=7$ with and without metal fill.

15.5 Model vs. Hardware and EM (singlecpw, coupledcpw)

The singlecpw and coupledcpw model were verified against 2-port G-S-G probe pad measurements and against z2d which is an IBM internal 2-D field solver that solves for frequency dependent resistance, capacitance, and inductance. In Figures 343-345, plots of frequency-dependent resistance, capacitance, inductance, and conductance (from signal line to grounded side shields...always zero potential) are shown. In the frequency-dependent resistance, capacitance, inductance, and conductance of the singlecpw and coupledcpw models were derived from frequency-dependent spectre S-parameter simulations of the models under the various geometries. The output of z2d is already in terms of frequency-dependent R, C, L, and G...so no conversion is needed for the z2d data. The data from z2d is the direct output of the tool. In the z2d simulations, the top of the silicon substrate is modelled as a grounded conductor. Thus, there is no frequency-dependent decrease of capacitance modelled in z2d when the signal line is exposed to the substrate (crossing="none") as in Figures 222-224 and the capacitance predicted by Z2D corresponds to the DC capacitance. Fill is not modelled in the z2d simulations. So, all capacitance in the z2d simulation is that predicted for the geometry without fill. In the previous sections showing z2d versus model, the dielectric assumed was 4.1 (oxide) "everywhere" above the surface of the silicon in the 2-D interconnect cross-sections. In this Model vs. Hardware section, the detailed passivation dielectric layers are modelled, and instead of assuming oxide "everywhere" above the silicon substrate, as in the previous sections, the oxide layer modelled extends from the silicon substrate to 1.35 μm above the top of the AM metal layer...followed by two dielectric layers in the final passivation region. Again, the field solver used to verify the singlecpw and coupledcpw models was z2d which is an IBM 2-D field solver "owned" by Alina Deutsch and her Interconnect and Packaging Analysis group (deutsch@us.ibm.com) at IBM's TJ Watson Research Center in Yorktown Heights, NY.

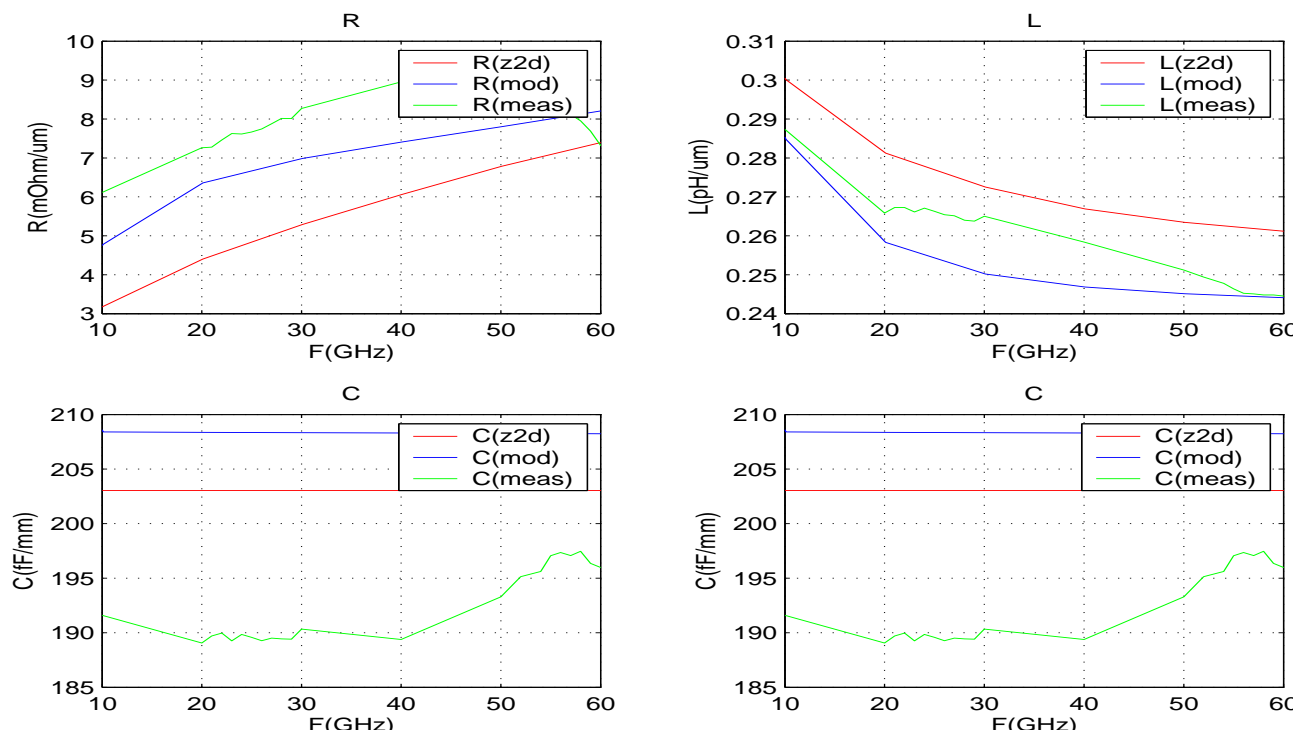


Figure 343. Model-to-Hardware Correlation for singlecpw: AM over Si (crossing="none"), $w=4\mu\text{m}$, $s=3\mu\text{m}$, $n\text{lev}=5$.

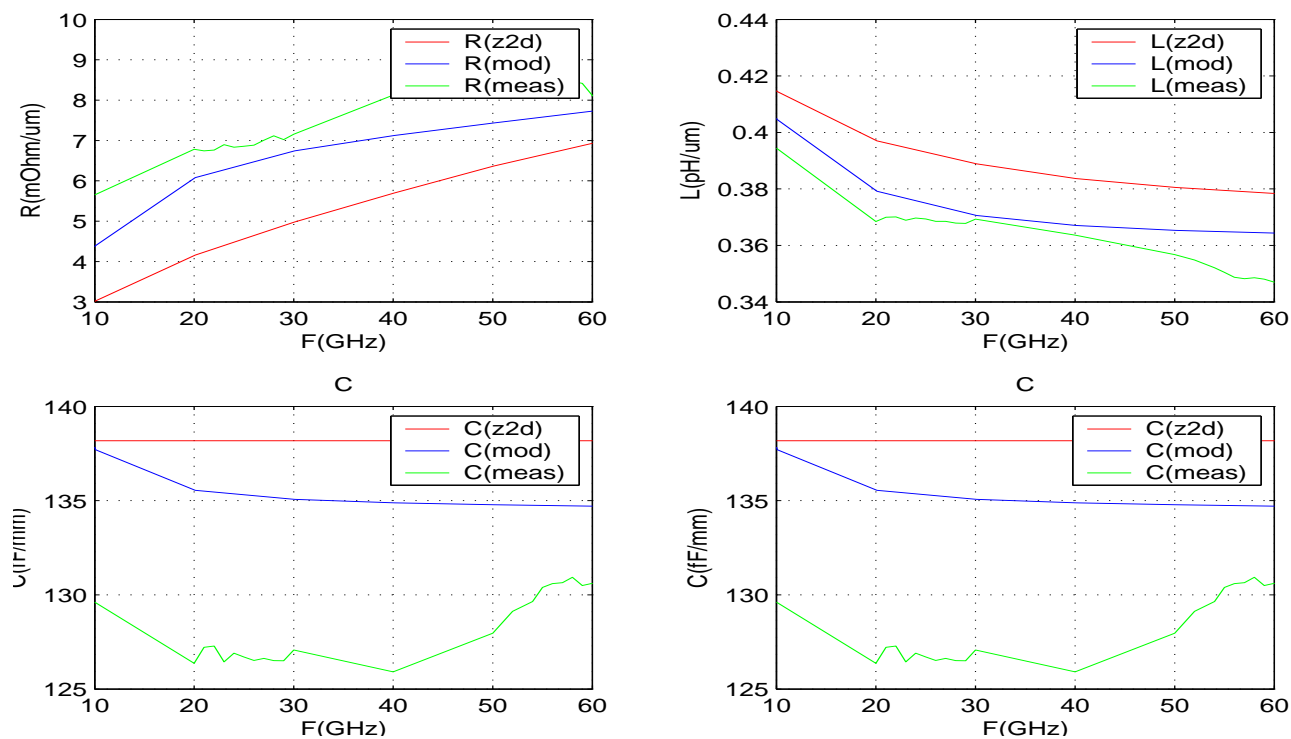


Figure 344. Model-to-Hardware Correlation for singlecpw: AM over Si (crossing="none"), $w=4\mu\text{m}$, $s=6\mu\text{m}$, $n\text{lev}=5$

Note: Z2d capacitance shown is DC capacitance (Si substrate considered grounded conductor)

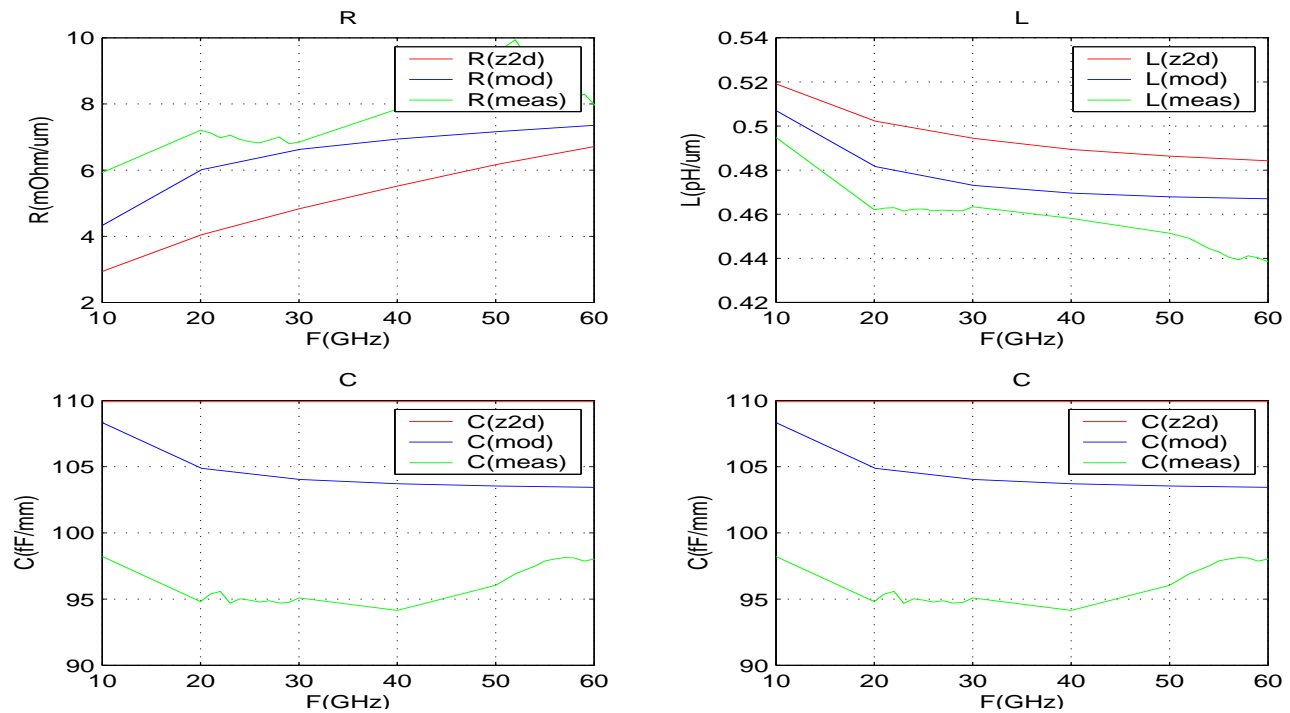


Figure 345. Model-to-Hardware Correlation for singlecpw: AM over M1 (crossing="below"), $w=4\mu\text{m}$, $s=10\mu\text{m}$, $nlev=5$.

16.0 Bondpad Models

The BiCMOS8HP technology supports wirebond and C4 pads made in the AM (final thick aluminum layer).

16.1 Bondpad Model vs Package Parasitics

The bondpad model simulates the effect of parallel plate and fringing capacitance between the bondpad and the groundplane. In the case of a C4 pad the model does not model the effects of parasitic coupling from the C4 ball or the Pad Limiting Metal (PLM) to either the package or the wafer substrate/groundplane. The effects of these parasitics should be included in a package model if accurate simulation of the interface between the chip and the package is desired.

16.2 Model Topology

The model is comprised of a capacitance (Cox), a groundplane resistance (Rgp), a groundplane capacitance (Cgp), and a diode (Dsx). Each of these elements is distributed into two individual pieces to model high frequency effects more accurately.

- Cox represents the oxide capacitance between the AM bondpad and the groundplane.
- Rgp represents the series resistance of the groundplane.
- Cgp represents the parallel capacitance of the groundplane.
- Dsx represents the diode present between the groundplane and the wafer substrate (if present).

16.3 Model Groundplane Options

The bondpad offers two groundplane options to provide flexibility in controlling noise coupling to/from the substrate

16.3.1 M1 Groundplane

The M1 groundplane provides a lattice of M1 underneath the bondpad. The main difference between the M1 and NS groundplanes is that the M1 groundplane is electrically isolated from the substrate by a dielectric. This means that the coupling between the groundplane and the substrate should be at a minimum. A second difference is that the groundplane resistance is significantly lower in the M1 groundplane.

16.3.2 NS Groundplane

The NS groundplane provides a region of N+ subcollector underneath the bondpad that provides a relatively low impedance ground node. This region is electrically isolated from the substrate by the subcollector to substrate diode. This may be appropriate for applications where it is desirable to have a well controlled impedance loading the bondpad, but where a relatively large groundplane to substrate capacitance is tolerable.

16.4 Model Correlation Plots

The following plots show model vs hardware correlations for the rectangular and octagonal AM bondpads for various BEOL stacking options and simulations for several other options.

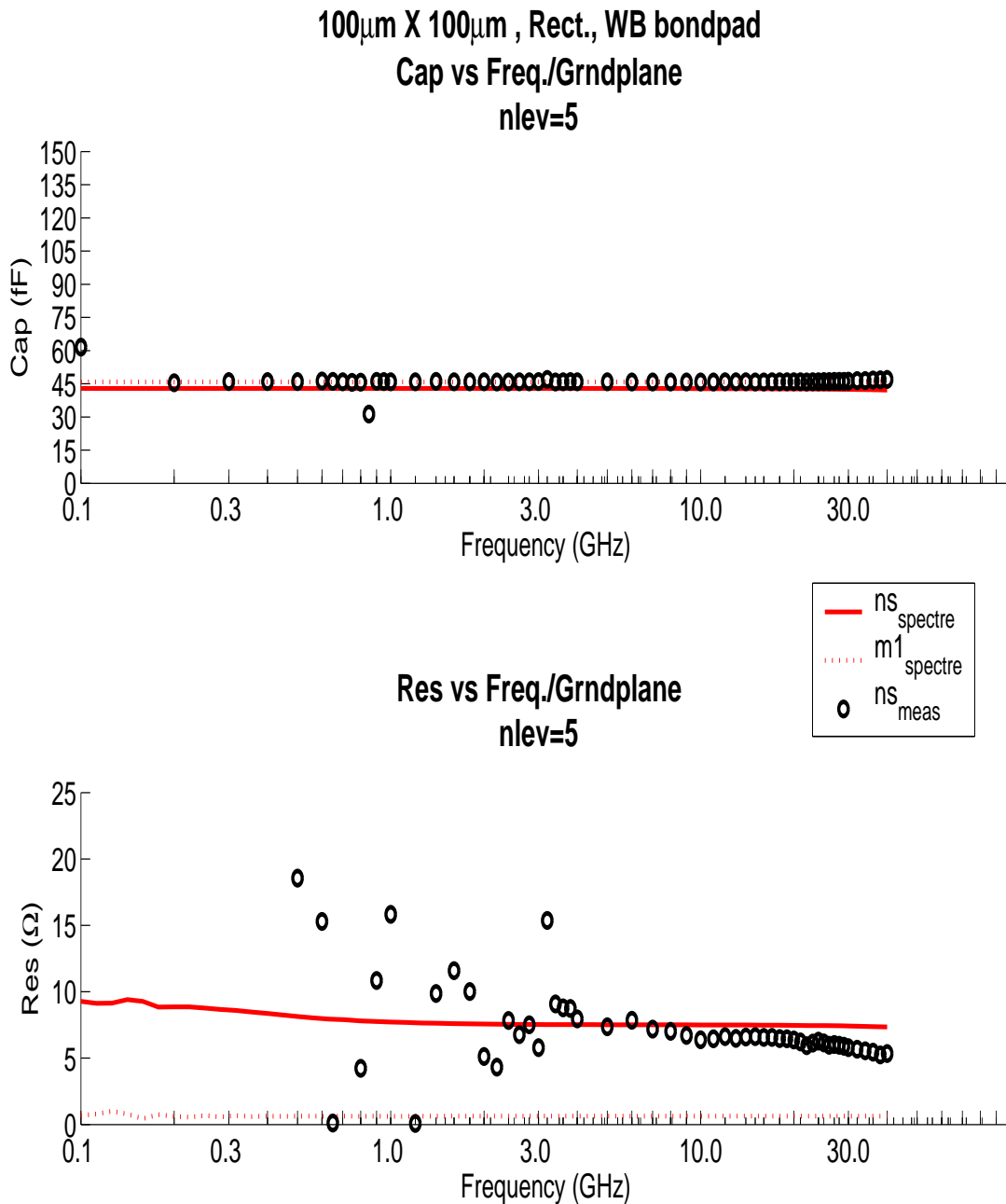


Figure 346. Capacitance/Resistance vs Freq., Rect. wirebond, $l=100\mu\text{m}$, $w=100\mu\text{m}$ (NS, M1 groundplanes)

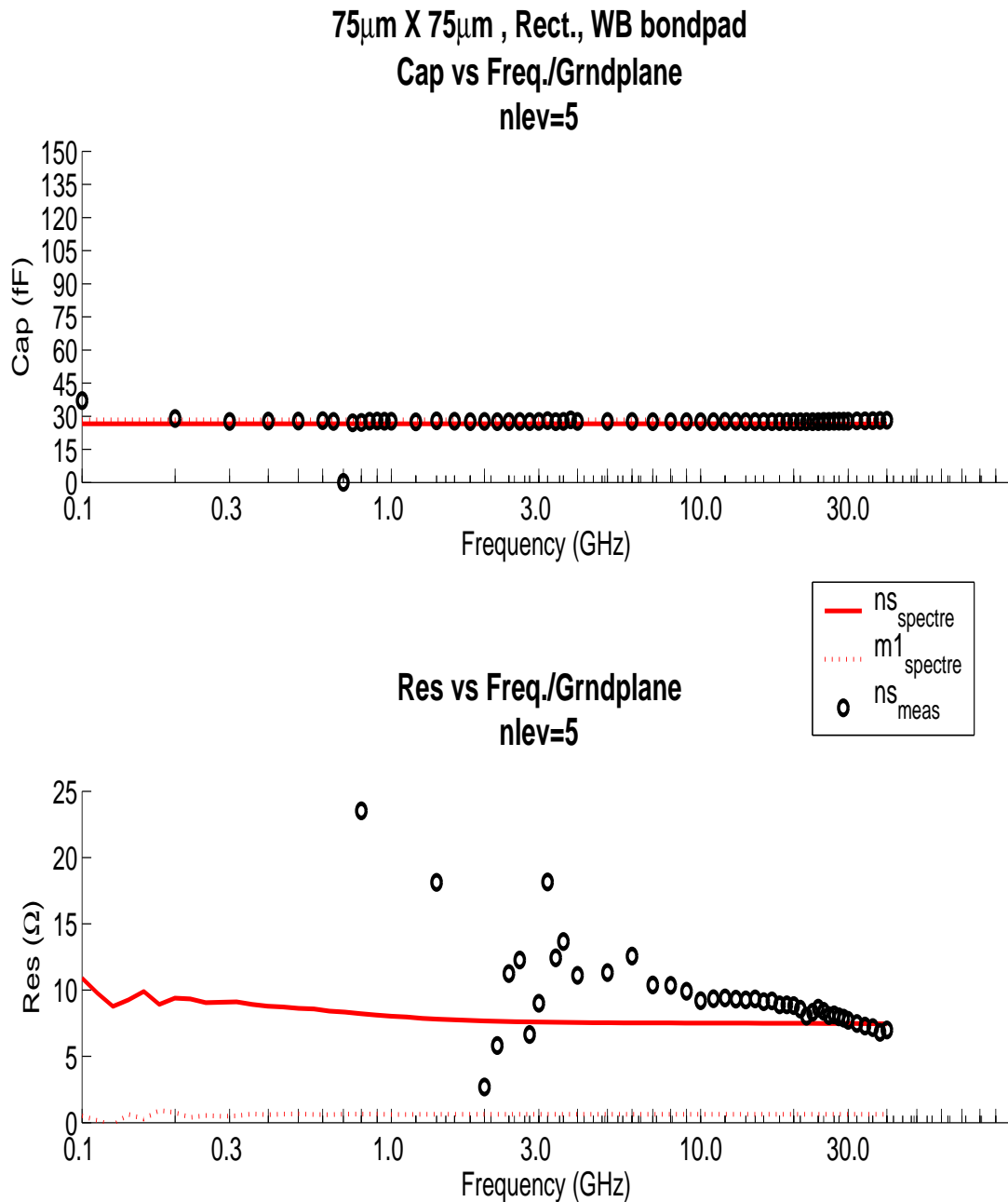


Figure 347. Capacitance/Resistance vs Freq., Rect. wirebond, $l=75\mu\text{m}$, $w=75\mu\text{m}$ (NS, M1 groundplanes)

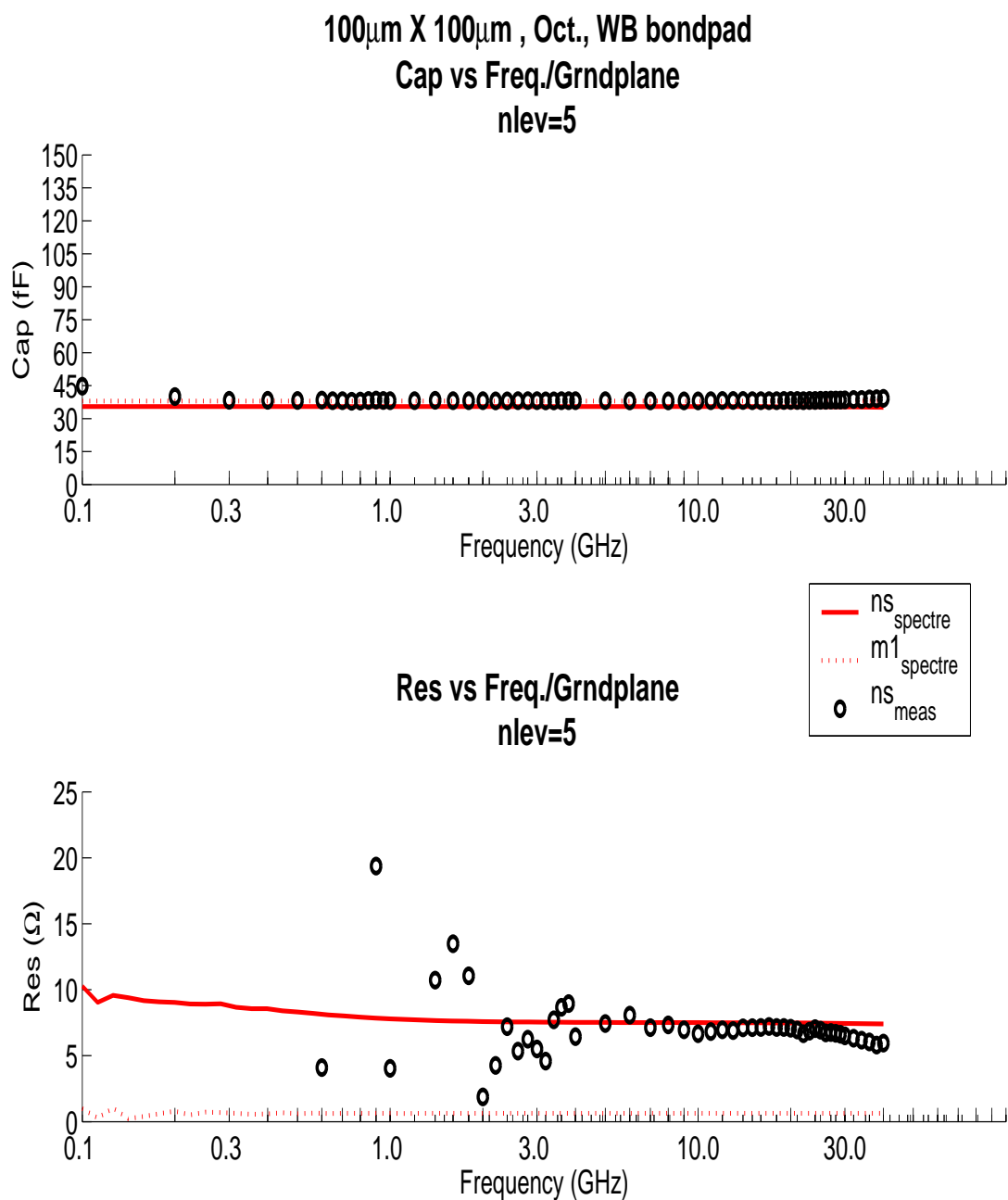


Figure 348. Capacitance/Resistance vs Freq., Oct. wirebond, $l=100\mu\text{m}$, $w=100\mu\text{m}$ (NS, M1 groundplanes)

17.0 Distributed Passive Device Models

The main purpose of this section is to provide information for the BEOL distributed passive (DP) models that are available in the current design kit.

17.1 Model Overview

This section gives a brief overview of IBM DP modeling methodology. The DP models (except langecoupler) are a combination of the physics-based models and models that use curve-fitted polynomials. In both cases the models use elementary resistors (R), inductors (L), and capacitors (C) to determine the netlist. The frequency dependency of R and L is represented using multiple-paralleled LR circuitries serial to the base L and R. The curve-fitted model of a device is obtained via RLC extraction over a wide range of geometrical parameters. Full 3D electromagnetic extractors (Ansoft's Q3D extractor) are used to extract the RLC components. The models are then fitted and the fitting algorithm is optimized for each device, depending on the allowed geometry variation of each distributed passive component. The allowable geometry variation ranges are described in the electrical section of the Design Manual and forced by the device CDF.

The current model release includes:

- bend
- tee
- step
- yjunction
- open
- short
- radialstub
- gap
- taper
- meanderlinex (x=1 or 2)
- branchcouplerx (x=0, 1 or 2)
- powerdividerx (x=0, 1 or 2)
- langecoupler
- ratracehybrid

17.2 Model Topologies and Correlation Plots

17.2.1 bend

Model Topology

The bend junction is modeled using two serial connected RLC branches, each branch modeling one side of the device. The values of resistance (R), inductance (L) and capacitance (C) were extracted using a 3D extraction tool (Ansoft's Q3D). Three section parallel LR circuitries are used to account for the skin effect on both ac resistance and inductance. The bend layout Pcell is fully compatible with the singelwire Pcell. The mitered-bend, also known as compensated bend which reduces the parasitic effect by allowing a smooth or guided flow of current with a reduced area, is supported as "miter" option. The current supported miter is a 45-degree or 50% cut of the overlapped area of the two bend arms.

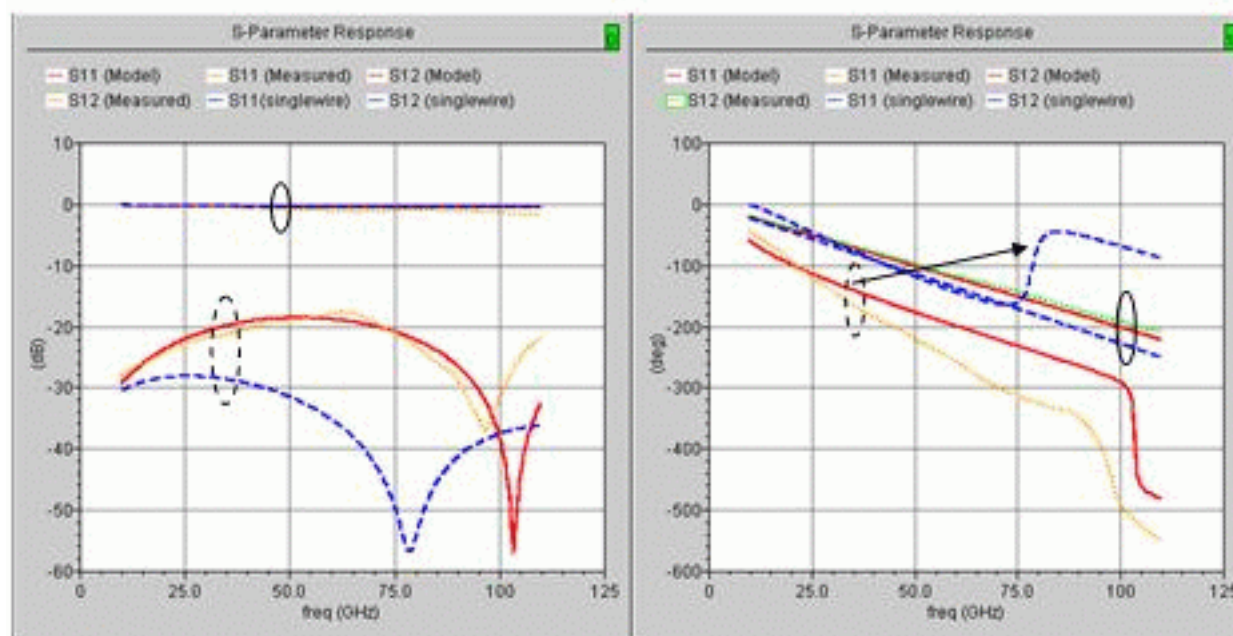


Figure 349. Comparison between Spectre model and hardware for a structure with bends/straight lines and a reference of straight line data. Solid (red) lines: Model, Dot (yellow or green) lines: Measured, Dash (blue) lines: Straight line without bend. Solid circle group: S21, Dash circle group: S11. Left: Amplitude in dB, Right: Phase in degree

Model Verification (Model vs. Hardware)

The bend models have been verified for a number of different configurations. Figure 349 shows a comparison between the Spectre model and hardware on a structure with bends. The structure is a meander line (meanderline2) which has a total length of 930um and is constructed from 15 pieces of singelwire and 8 pieces of bend in the 5-metal stack. The signal is on metal AM with width of 15.48um (resulting in about 50ohm characteristic impedance) and the bottom ground shield is on M2 without side shields. The solid (red) lines in the figure are for model simulations of the meander line, the dot (yellow or green) lines are for measured data for the meander line. The model simulation results of a stright line (singelwire) with same width and total length are also showed in Figure 1 as dash (blue) lines, which have significant difference from the measured data for both S11 amplitude and phase.

17.2.2 tee

Model Topology

The tee junction is modeled using three RLC branches (T-type connection), each branch modeling one side of the device of possibly different widths. The values of resistance (R), inductance (L) and capacitance (C) were extracted using a 3D extraction tool (Ansoft's Q3D). Three section parallel LR circuitries are used to account for the skin effect on both ac resistance and inductance. The tee junction layout pcell is compatible with the singlewire Pcell.

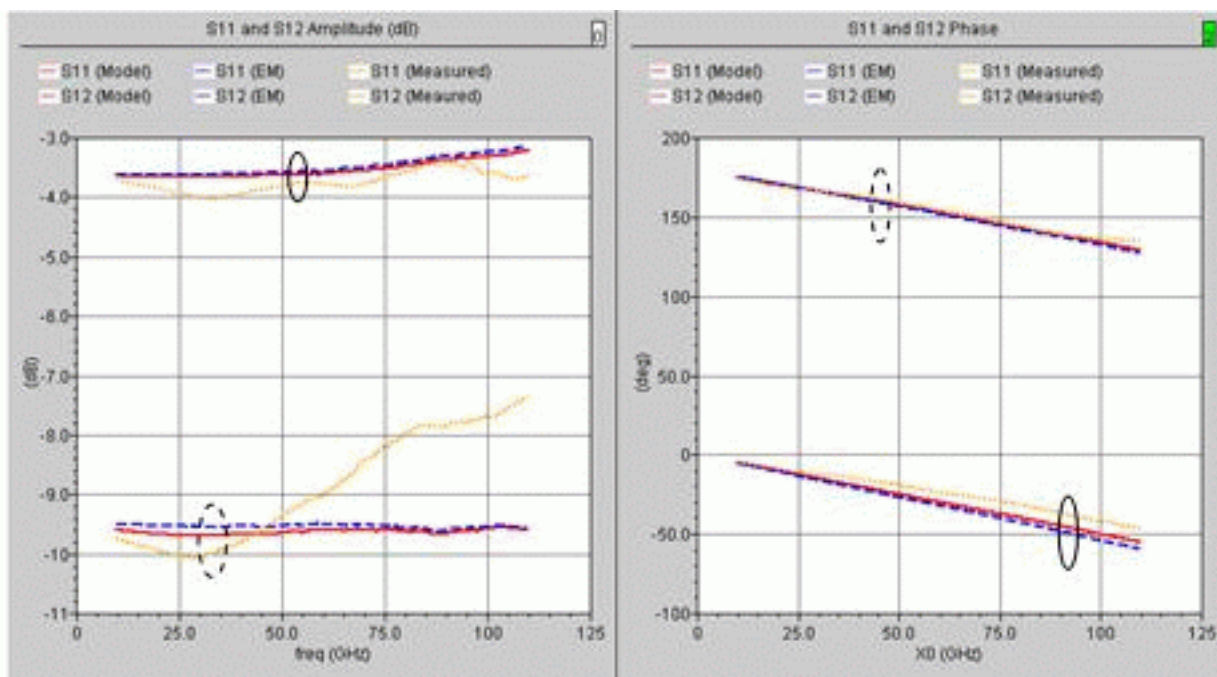


Figure 350. Comparison of Spectre model vs. EM vs. hardware for a structure with a tee and straight lines. Solid (red) lines: Model, Dot (yellow) lines: Measured, Dash (blue) lines: EM. Solid circle group: S21, Dash circle group: S11. Left: Amplitude in dB, Right: Phase in degree

Model Verification (Model vs. EM vs. Hardware)

The tee junction models have been verified for a number of different configurations. Figure 350 shows a comparison of model vs. EM (Ansoft HFSS) vs. hardware for a structure with a tee junction. The structure is constructed of three singlewires, one on-chip 50ohm termination and a tee without side shields in the 5-metal stack. The signal metal (AM) widths of three tee arms are $W1=13.36\text{ }\mu\text{m}$ ($Z0\sim 50\text{ ohms}$), $W2=26.44\text{ }\mu\text{m}$ ($Z0\sim 35\text{ ohms}$) and $W3=13.36\text{ }\mu\text{m}$ ($Z0\sim 50\text{ ohms}$), the bottom ground shield is on MQ. Each tee arm connects one singlewire, which has the same width as the arm to be connected, to extend the arm length for measurement probing. The singlewires have lengths of $95.09\text{ }\mu\text{m}$, $95.09\text{ }\mu\text{m}$ and $88.53\text{ }\mu\text{m}$ corresponding to $W1$, $W2$ and $W3$ connections. The distance between two terminals (widths of $W1$ and $W2$) for the measurement is $230\text{ }\mu\text{m}$. The on-chip 50ohm termination connects to the arm $W3$. The measured S-parameter of the on-chip 50ohm termination is also used in model/EM simulations. In the figure, the solid (red) lines are model simulated data, the dash (blue) lines are EM simulated data and the dot (yellow) lines are measured data.

17.2.3 step

Model Topology

The step junction is modeled using two serial connected RLC branches, each branch modeling one side of the device of possibly different widths. The values of resistance (R), inductance (L) and capacitance (C) were extracted using a 3D extraction tool (Ansoft Q3D). Three section parallel LR circuitries are used to account for the skin effect on both ac resistance and inductance. The step junction layout pcell is compatible with the singlewire pcell.

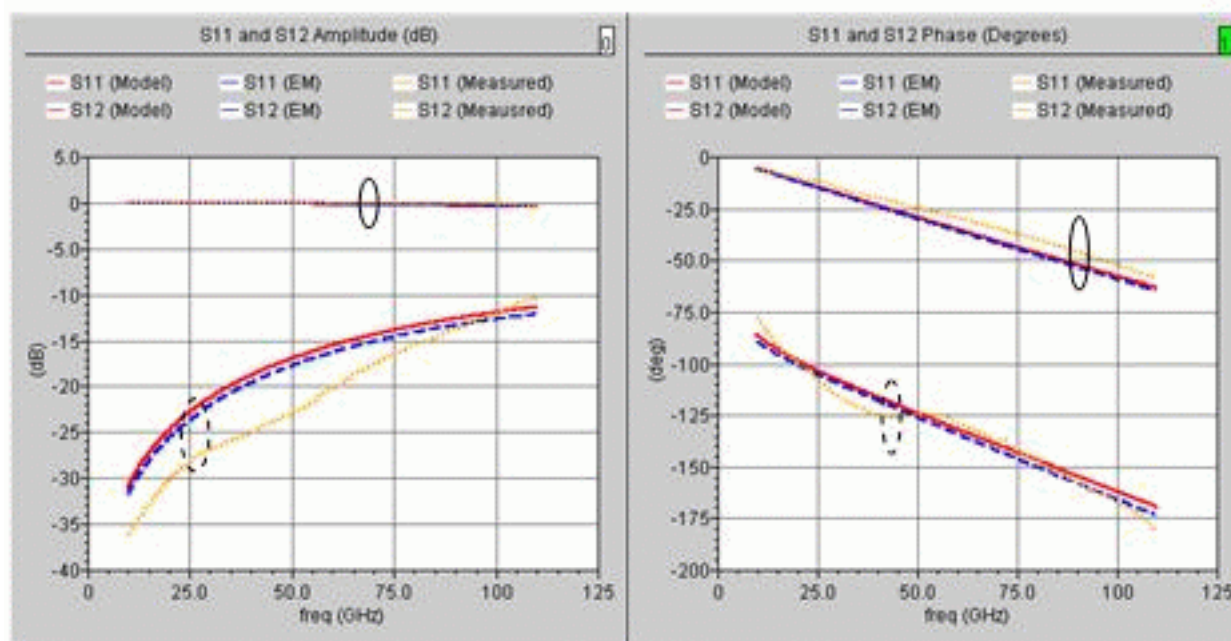


Figure 351. Comparison of Spectre model vs. EM vs. hardware for a structure with a step. Solid (red) lines: Model, Dot (yellow) lines: Measured, Dash (blue) lines: EM. Solid circle group: S21, Dash circle group: S11. Left: Amplitude in dB, Right: Phase in degree

Model Verification (Model vs. EM vs. Hardware)

The step junction models have been verified for a number of different configurations. Figure 351 shows a comparison of Spectre model vs. EM (HFSS) vs. hardware for a structure with a step junction. The structure consists of two singulwires and a step in the 5-metal stack. The widths of the step are $W_1=13.36\text{ }\mu\text{m}$, $W_2=26.44\text{ }\mu\text{m}$ with side shield spaced $15\text{ }\mu\text{m}$ away from the signal line on AM, the bottom ground shield is on MQ. Each side of the step connects one singulwire, which has the same width and side shields as the side of the step to be connected, to extend the structure length. Both singulwires have a length of $105\text{ }\mu\text{m}$ to make the distance of $230\text{ }\mu\text{m}$ from one end to another end of the structure for measurements. In the figure, the solid (red) lines are model simulated data, the dash (blue) lines are EM simulated data and the dot (yellow) lines are measured data.

17.2.4 yjunction

Model Topology

The yjunction is modeled using three RLC branches and two transmission-line segments at the split sides. The values of resistance (R), inductance (L) and capacitance (C) were extracted using a 3D extraction tool (Q3D). Three section parallel LR circuitries are used to account for the skin effect on both ac resistance and inductance. The y-junction layout pcell is compatible with the singlewire pcell. The model allows the user to set the separation distance between the two branches which are of the same characteristic impedance.

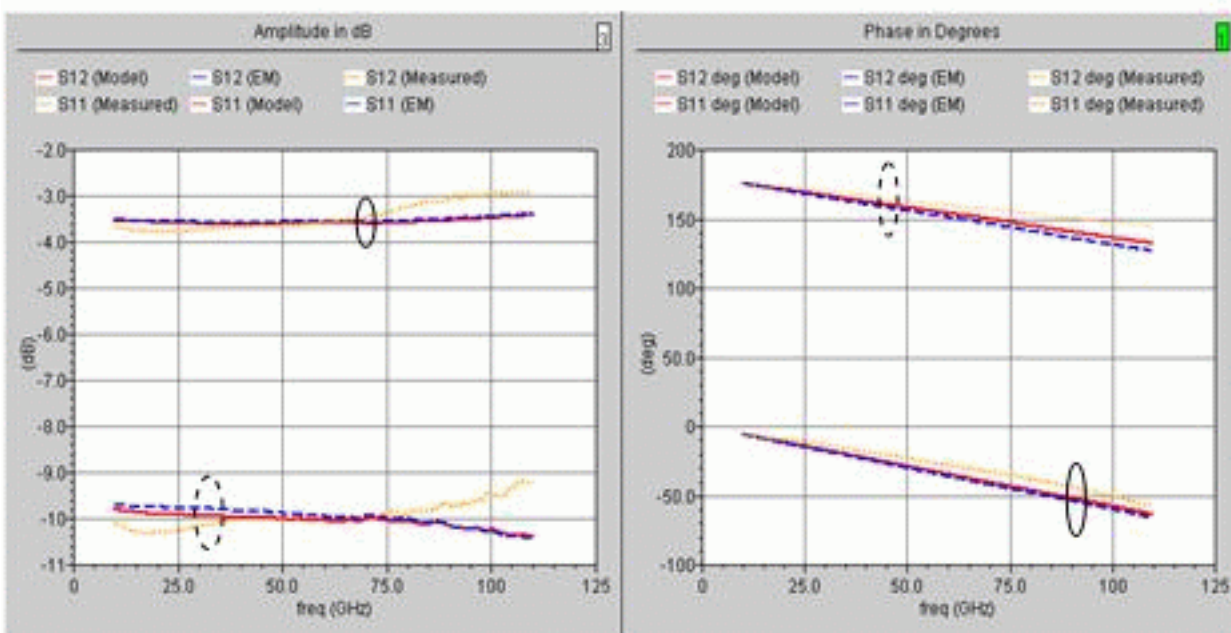


Figure 352. Comparison of Spectre model vs. EM vs. hardware for a structure with a yjunction. Solid (red) lines: Model, Dot (yellow) lines: Measured, Dash (blue) lines: EM. Solid circle group: S21, Dash circle group: S11. Left: Amplitude in dB, Right: Phase in degree

Model Verification (Model vs. EM vs. Hardware)

The yjunction models have been verified for a number of different configurations. Figure 352 shows a comparison of Spectre model vs. EM (Ansoft HFSS) vs. hardware for a structure with a yjunction. The structure consists of three singlewires and a yjunction in the 5-metal stack. The three terminal widths of the yjunction are same, AM signal width is 13.36 μ m without side shields and the bottom ground shield is on MQ. The separation between two split arms is 100 μ m (signal line edge to edge). Each terminal connects one singlewire to extend the length for measurements. The 83.9 μ m long singlewire connects the input terminal and two 63.89 μ m long singlewires connect to the two split terminals. All singlewires have the signal metal width of 13.36 μ m. One of the split terminals is then (after the singlewire) terminated with an on-chip 50ohm resistor. This on-chip 50ohm resistor is also measured and used as the termination for the Spectre model and EM model simulations. In the figure, the solid (red) lines are the model simulated data, the dash (blue) lines are the EM simulated data, and the dot (yellow) lines are the measured data.

17.2.5 open

Model Topology

The open stub is modeled using a transmission line terminated with a capacitor, which models the electric field fringing from the open end to the shields. The capacitance (Cend) is determined using the physical size of the stub. The model accounts for the metal losses, inductance and capacitance of the line to both the bottom and side-shields. The model excludes any radiation effects. The open stub layout PCell is compatible with the singlewire PCell. The model allows the user to set the width and length of the line with and without side-shields, different signal and bottom ground shield metals.

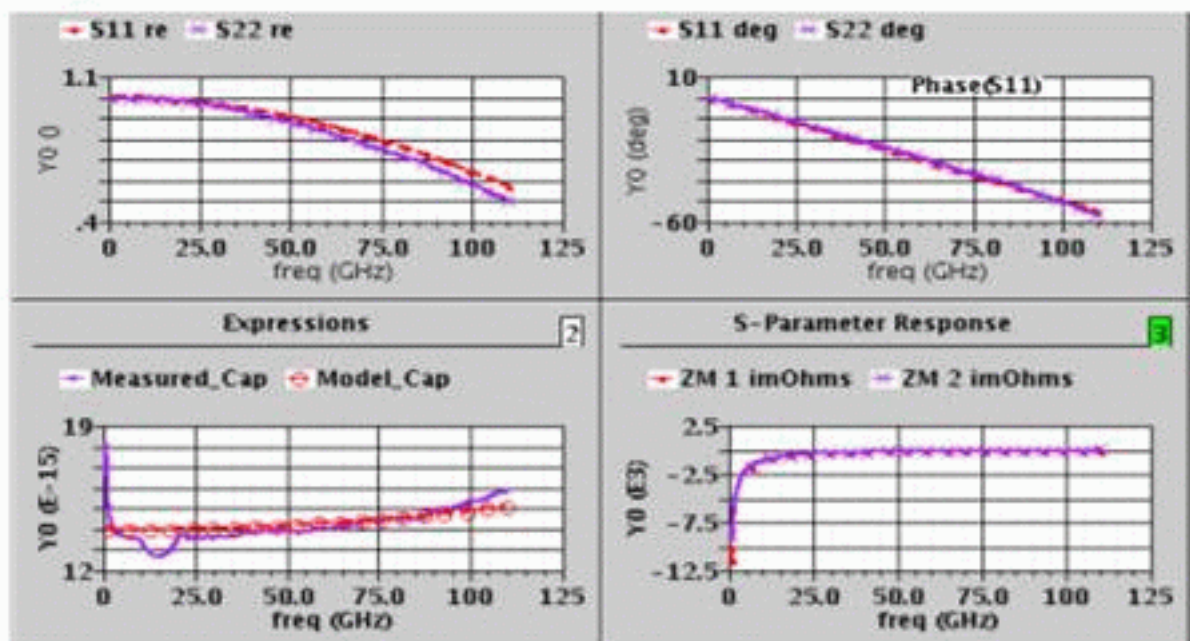


Figure 353. Comparison of Spectre model vs. hardware for an open stub. Dash (red) lines: Model, Solid (purple) lines: Measured. Top Left: Reflection Amplitude, Top Right: Reflection Phase in degree, Bottom Left: Equivalent Capacitance, Bottom Right: Imaginary Part of Input Impedance

Model Verification (Model vs. Hardware)

The open stub models have been verified for a number of different configurations. Figure 353 shows a comparison of Spectre model vs. hardware of a 50 ohm open-circuited stub with a length of 100 μm in the 5-metal stack. The signal metal is 15.48 μm wide on AM and the bottom ground shield is on M2. In the figure, the dash (red) lines are the model simulated data and the solid (purple) lines are the measured data. The S11 (port reflection) real part and phase, port input reactance and extracted capacitance value comparisons are all shown in Figure 353.

17.2.6 short

Model Topology

The short stub is modeled using a transmission line terminated with a network of resistors and inductors that model the ohmic loss and inductive effect through the vias at both DC and mmwave frequencies. The model accounts for the metal losses, inductance and capacitance of the signal line to the bottom shield and also to the side-shields, if present. The short stub layout PCell is compatible with the singlewire PCell. The model allows the user to set the width and length of the line with and without side-shields, different signal and bottom ground shield metals. Multi-section parallel R-L network is used to accurately model the increasing via-resistance and decreasing via-inductance because of the skin effect. The values for resistance were obtained from the geometries of the vias and the values for inductance were obtained as a result of polynomial curve fitting.

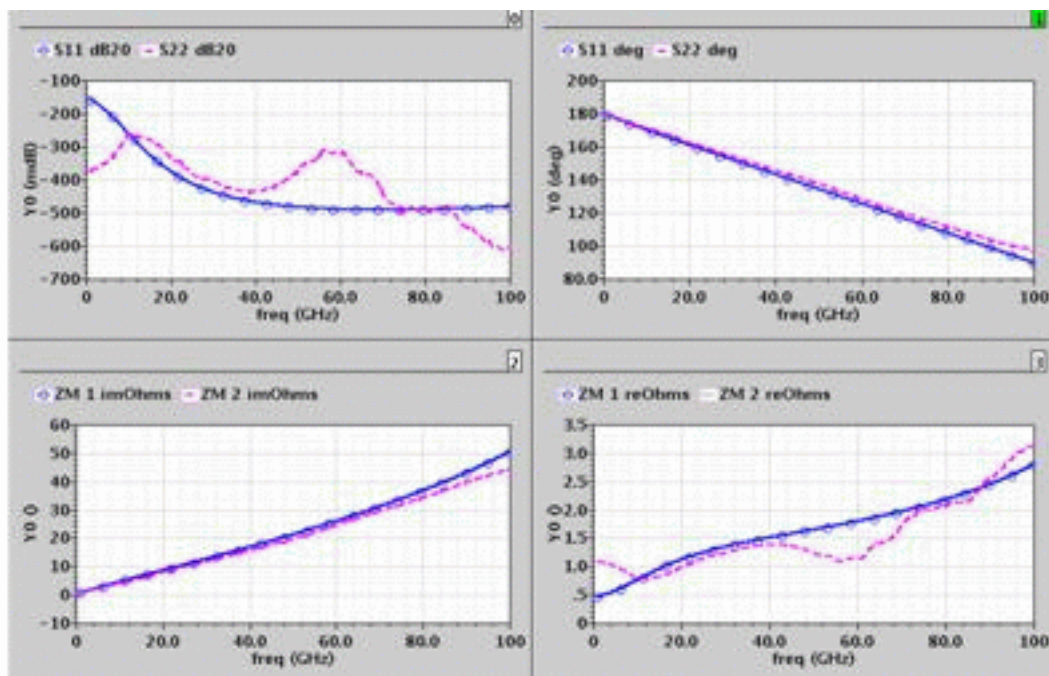


Figure 354. Comparison of Spectre model vs. hardware for a short stub. Solid (blue) lines: Model, Dash (purple) lines: Measured. Top Left: Reflection Amplitude in ndB , Top Right: Reflection Phase in degree, Bottom Left: Real Part of Input Impedance, Bottom Right: Imaginary Part of Input Impedance

Model Verification (Model vs. Hardware)

The short stub models have been verified for a number of different configurations. Figure 354 shows a comparison of Spectre model vs. hardware of a 180 μm -long short-circuited stub in the 5-metal stack. The signal metal width is 15.48 μm on AM and the bottom ground shield is on M2. In the figure, the solid (blue) lines are the model simulated data and the dash (purple) lines are the measured data. Both the S11 (reflection) amplitude and phase, as well as the real and imagine parts of the port input impedance are shoed in Figure 354.

17.2.7 radialstub

Model Topology

The radial stub is constructed by sequentially connected transmission lines of increasing widths and fixed length. For modeling purposes three different regions of the stubs are identified; (1) input launch: a short straight transmission line used to avoid DRC errors for connecting to other devices; (2) part of the stub from input to maximum width (linear region), and (3) angular region of the stub, which includes the fringing of E-field from the open face of the stub.

- a. The linear region can be modeled by sequentially connected transmission lines. The increments in the widths of the lines are determined using angle, number of sections, and the signal width. Since the stub is constructed using incremental widths of lines, there exists minimal but finite E-field fringing due to difference in the widths of adjacent two pieces. The E-field fringing because of this difference from at each increment was also determined. Initial results show that these fringing capacitors make minimal contribution in the performance of the radial stub.
- b. The angular region is modeled by sequentially connected transmission lines and terminated using a capacitor, which models the E-field fringing of the open end of the stub (including the effects of finite height of the signal lines from the bottom shield). A closed-form expression was used for the capacitance. The bottom-shield extends out on all sides thereby completely shielding the signal line from silicon. Resultantly, the fringing capacitances are frequency independent.

Model Verification (Model vs. EM vs. Hardware)

The radial stub models have been verified for a number of different configurations. Figure 355 shows a comparison of Spectre model vs. hardware vs. 3D EM (HFSS) of a structure with a radial stub. The structure consists of a singlewire and a radialstub in the 5-metal stack. The radialstub has $w=13.36\text{ }\mu\text{m}$, $r=300\text{ }\mu\text{m}$, and $\text{angle}=90\text{ degrees}$. The singlewire has $w=13.36\text{ }\mu\text{m}$ and length of $40\text{ }\mu\text{m}$ to provide the enough separation between the radial stub and the probing pads. The stub was designed using AM as signal and MQ metal layer as bottom ground shield. In the figure, the dash (red) lines are model simulated data, the solid (green) lines are the EM simulated data, and the solid (purple) lines are the measured data. The S11 (port reflection) amplitude and phase, port input reactance in ohms, and input port capacitance are compared.

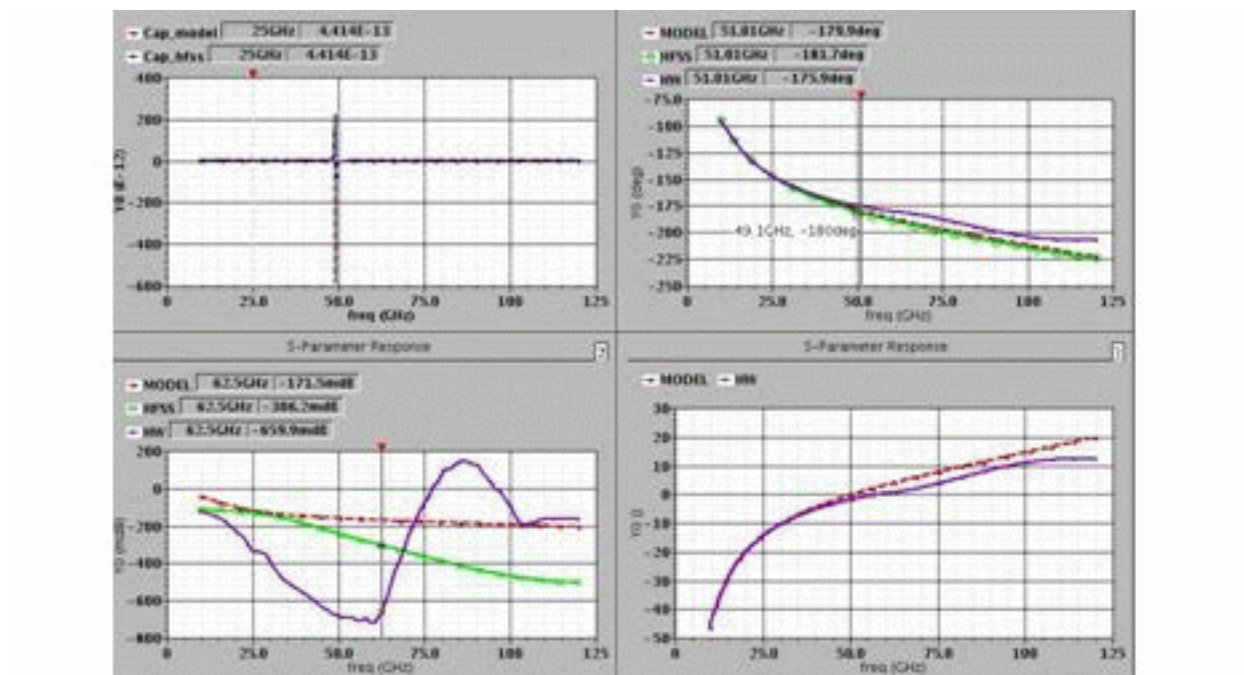


Figure 355. Comparison of Spectre model vs. EM vs. hardware for a radialstub. Dash (red) lines: Model, Solid (purple) lines: Measured, Solide (green) lines: EM. Top Left: Equivalent Capacitance (Model vs. EM), Bottom Left: Reflection Amplitude in mdB, Top Right: Reflection Phase in degree, Bottom Right: Imaginary Part of Input Impedance

17.2.8 gap

Model Topology

The gap is modeled using two RLC branches connected in series with a coupling using capacitor. Each RLC branch models one side of the device, and the serial capacitor accounts for the capacitive coupling between the two sides of the gap. The values of resistance (R), inductance (L) and capacitance (C) were extracted using a 3D extraction tool (Ansoft's Q3D). Three section parallel LR circuitries are used to account for the skin effect on both ac resistance and inductance. The gap layout Pcell is compatible with the singlewire Pcell.

Model Verification (Model vs. EM vs. Hardware)

The gap models have been verified for a number of different configurations. Figure 356 shows a comparison of Spectre model vs. 3D EM (HFSS) vs. hardware for a structure with a gap device. The structure consists of two singlewires and a gap device in the 5-metal stack. The two terminals of gap device has same signal width of 15.48 μm on AM, the bottom ground shield is on M2, the gap is 7 μm . Each terminal of the gap device connects a singlewire (55 μm long) to extend the length for measurements. The signal width of the singlewires is 15.48 μm . The total length of the structure is 130 μm . In the figure, the solid lines without markers are measured data, the dash lines with circle markers are model simulated data, and the dash lines with arrow markers are EM simulated data.

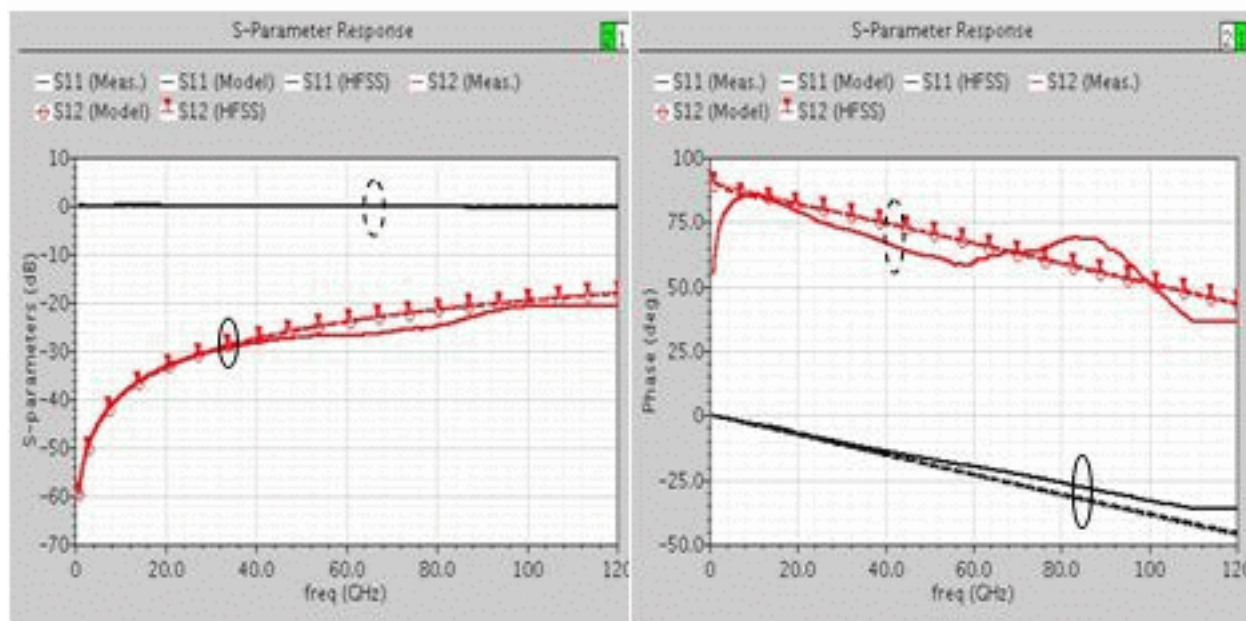


Figure 356. Comparison of Spectre model vs. EM vs. hardware for a structure with a gap. Dash (black or red) lines with circle markers: Model, Solid (black or red) lines: Measured, Dash (black or red) lines with arrow markers: EM. Solid circle group: S12, Dash circle group: S11. Left: Magnitude in dB, Right: Phase in degree

17.2.9 taper

Model Topology

The taper model is constructed by sequentially connected transmission lines and capacitors to model fringing. The model is based on multiple segments of transmission lines of increasing/decreasing widths. Since the entire device is connection of piecewise increase/decrease in widths, the additional capacitance at the outside edges of the device is modeled via shunt connection of capacitor between each segment. The lengths of the singlewire segments are dependent on the total length of the taper for highest model accuracy.

Model Verification

The taper model sub-circuits have been verified for a number of different configurations. Figure 357 shows a comparison of Spectre model vs. EM model vs. hardware for a structure with tapers in the 5-metal stack. The structure consists of the first singlewire, first taper (narrow-to-wide), second singlewire, second taper (wide-to-narrow, mirror of the first taper) and the third singlewire (same as the first singlewire). The taper has AM signal widths of 12um and 45um with length of 40um, the bottom ground shield is on M1. The first and third singlewires has signal width of 12um with length of 37.5um. The second singlewire has signal width of 45um with length of 75um. The total length of the structure is 230um. In the figure, the solid (red) lines are the model simulated data, the dash (blue) lines are the EM simulated data, and the dot (light green) lines are the measured data.

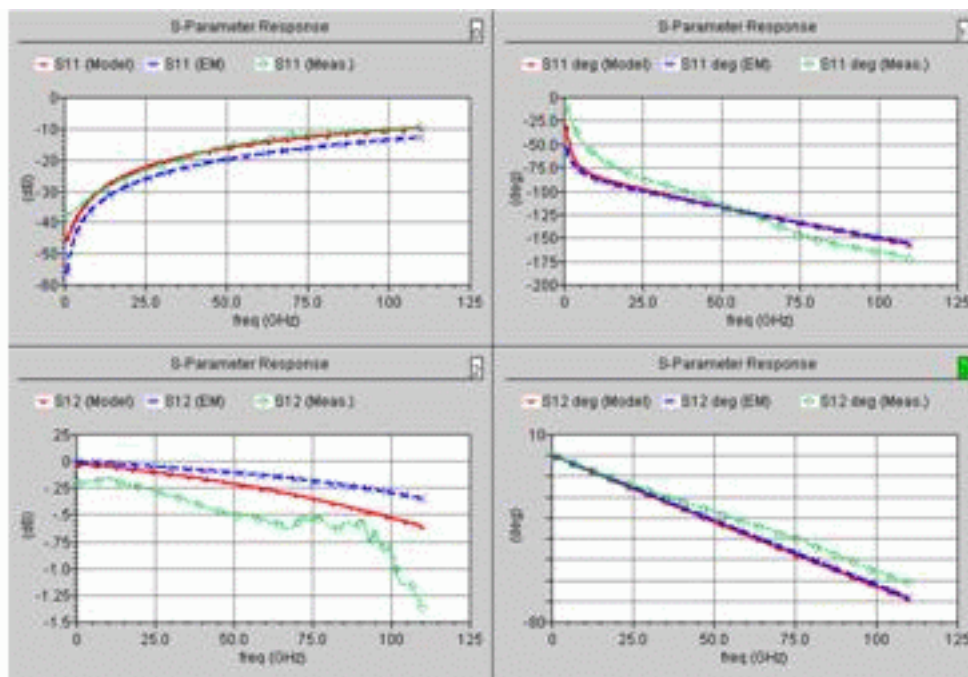


Figure 357. Comparison of Spectre model vs. EM vs. hardware for a structure with tapers. Solid (red) lines: Model, Dot (light green) lines: Measured, Dash (blue) lines: EM. Top Left: S11 Magnitude in dB, Top Right: S11 Phase in degree, Bottom Left: S12 Magnitude in dB, Bottom Right: S12 Phase in degree

17.2.10 meanderlinex (x=1 or 2)

Model Topology

The meander-line model is a hierarchical sub-circuit which calls singlewire and bend models, therefore there is no Spectre or Hspice model file associate to the meander lines. Figure 358 shows the layout PCell and model sub-circuit for meanderline2 (two meanders). The physical total length of a meander line is defined as the center-line length of the meander line from end to end.

Model Verification

The meander-line model sub-circuits have been verified for a number of different configurations. The results have been used for the bend model correlations. Reference Figure 349 for an example, in which a comparison of Spectre model vs. hardware for a meanderline2 with length of 930um is displayed.

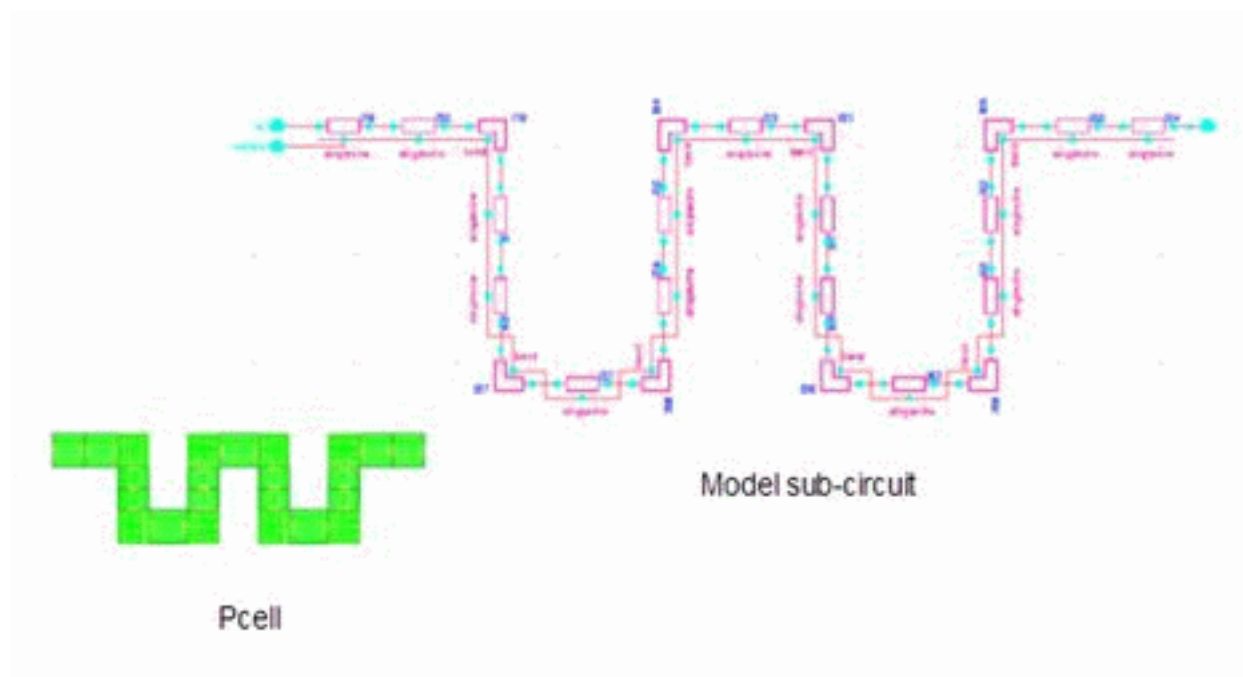


Figure 358. Pcell and Model Sub-Circuit for meanderline2

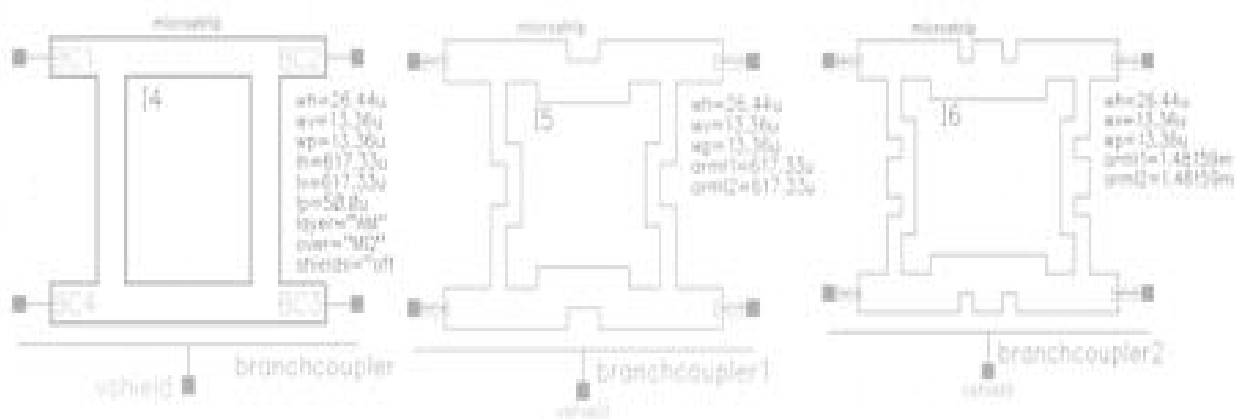
17.2.11 branchcouplerx (x=0, 1 or 2)

Model Topology

The branch coupler “model” is a two or three level hierarchical sub-circuit, which calls models of tee, bend, and singlewire or/and meanderline1 or meanderline2. Figure 359 shows symbols for three variants of Branch-line couplers. For the device branchcoupler0, no meander line model is called. For the device branchcoupler1, the meanderline1 models are called, and for the device branchcoupler2, the meanderline2 models are called. Figure 360 shows the model sub-circuit, layout Pcell and symbol for branchcoupler1. The meander shaped line is a useful feature to reduce the overall area of the coupler without much degradation in performance.

Model Verification

The branch coupler models have been verified for a number of different configurations. Figure 361 shows a comparison of the model simulation vs. hardware for a 60 GHz Branch coupler. This Branch coupler uses branchcoupler1 device with “Horizontal Line Width” of 26.44um, “Vertical Line Width” of 13.36um, “Port width” of 13.36um, “Miter type” of No, “Frequency [Hz]” of 60G, “Override Length Calculations?” selected, “Horizontal Line Length” and “Vertical Line Length” of 680um, “Port Length” of 134.64um, “Side Shielding” unselected, “Metal Levels” of 5, “Signal Layer” of AM, “Bottom Shield Layer” of MQ, and “Temperature Delta” of 0. The solid lines are the model simulated results and the dash lines are the measured data.



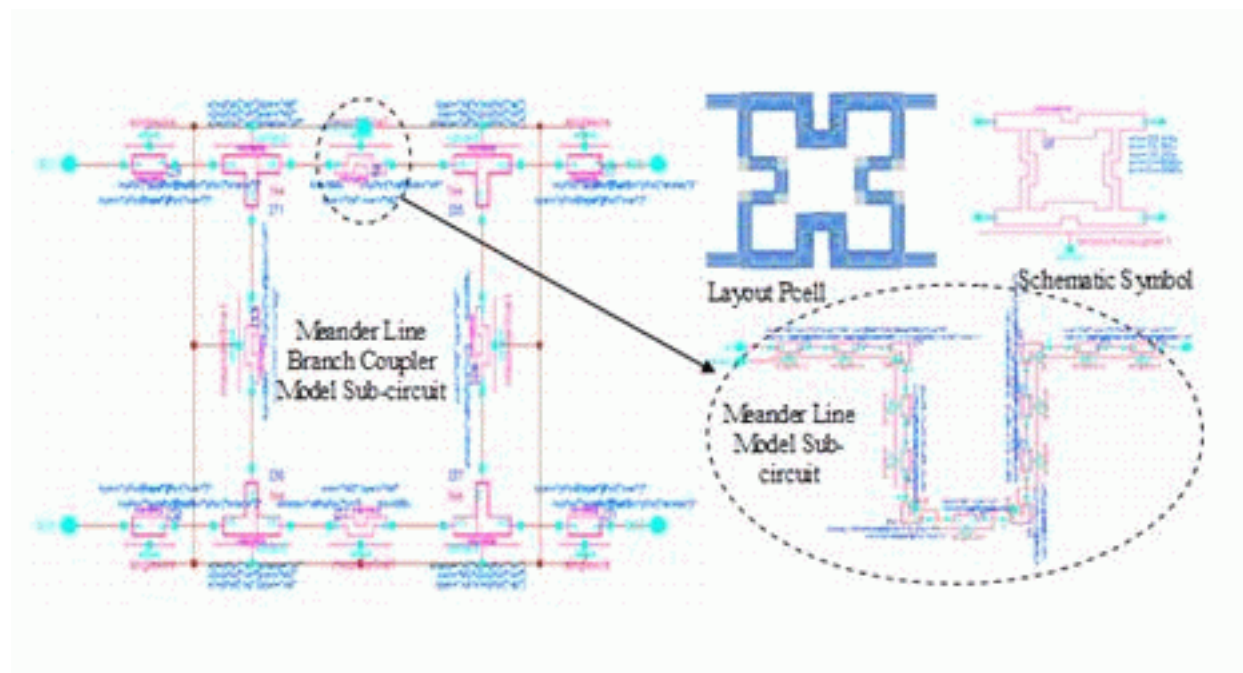


Figure 360. Model sub-circuit, Pcell and Symbol for branchcoupler1

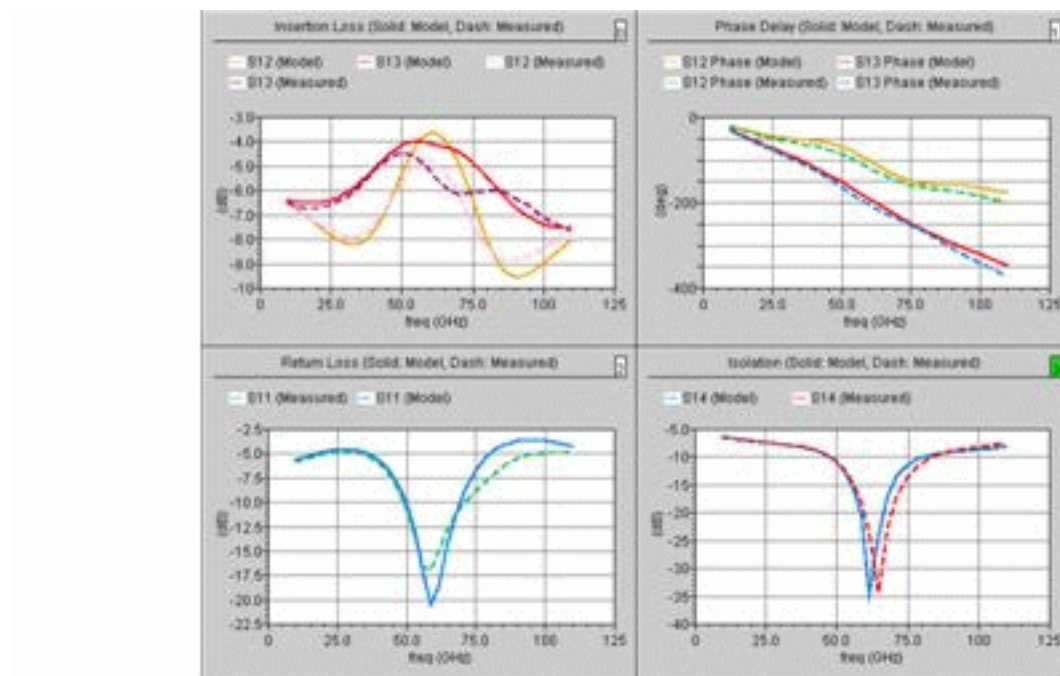


Figure 361. Comparison of Spectre model vs. measurement for a 60GHz branchcoupler1. Top-left: S12 (through) and S13 (coupling) magnitude in dB; Top-right: S12 (through) and S13 (coupling) phase in degree; Bottom-left: S11 magnitude in dB; Bottom-right: S14 (isolation) magnitude in dB.

17.2.12 powerdividerx (x=0, 1, or 2)

Model Topology

The Wilkinson power divider “model” is a two or three level hierarchical sub-circuit, which calls models of tee, KQ-metal resistor (kqres), bend, singlewire and/or meanderline1 or meanderline2. The meander shaped line is used to reduce the overall area of the divider without much degradation in performance. Figure 362 shows the symbols for three variants of the Wilkinson power divider. No meander line is called by powerdivider0, while meanderline1 is called by powerdivider1 and meanderline2 is called by powerdivider2. Figure 363 shows the hierarchical model sub-circuit and the layout PCell for powerdivider1.

Model Verification

The power divider models have been verified for a number of different configurations. Figure 364 shows a comparison of model simulation vs. hardware for a 94 GHz power divider design. This design uses powerdivider0 device with “Width” of 5.74um, “Port Width” of 15.54um, “Miter Type” of 45_degree, “Frequency [Hz]” of 94G, “Override Length Calculations?” selected, “Port Length” of 90um, “Total Length” of 415um, “Separation” of 102um, “Side Shielding” unselected, “Metal Levels” of 5, “Signal Layer” of AM, “Bottom Shield Layer” of M2, “Temperature Delta” of 0, “Span” of 225um, “Resistor Width” of 5.92um, and “Resistor Length” of 9.16um. In the figure, the solid (red/blue/green) lines are the model simulated data, the dash (black/pink/brown) lines are measured data.

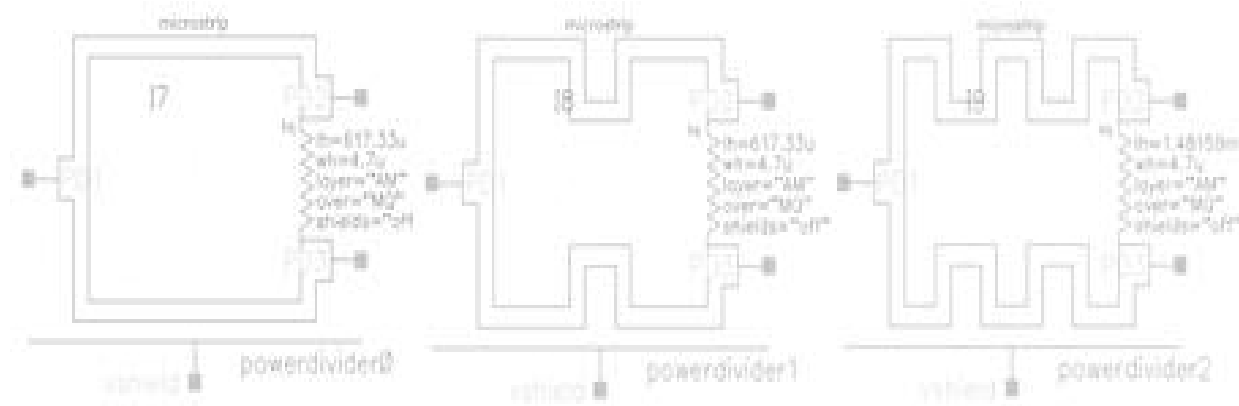


Figure 362. Schematic symbols of powerdivider0 (left), powerdivider1 (middle) and powerdivider2 (right)

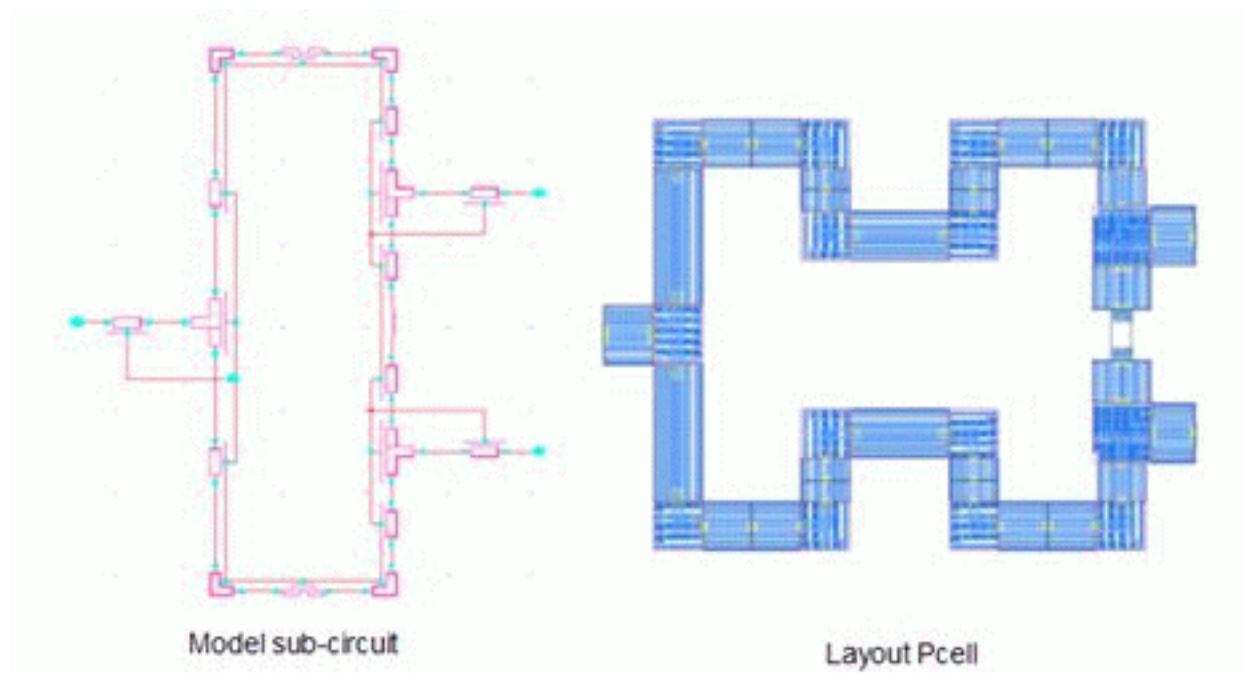


Figure 363. Model sub-circuit and Pcell for powerdivider1

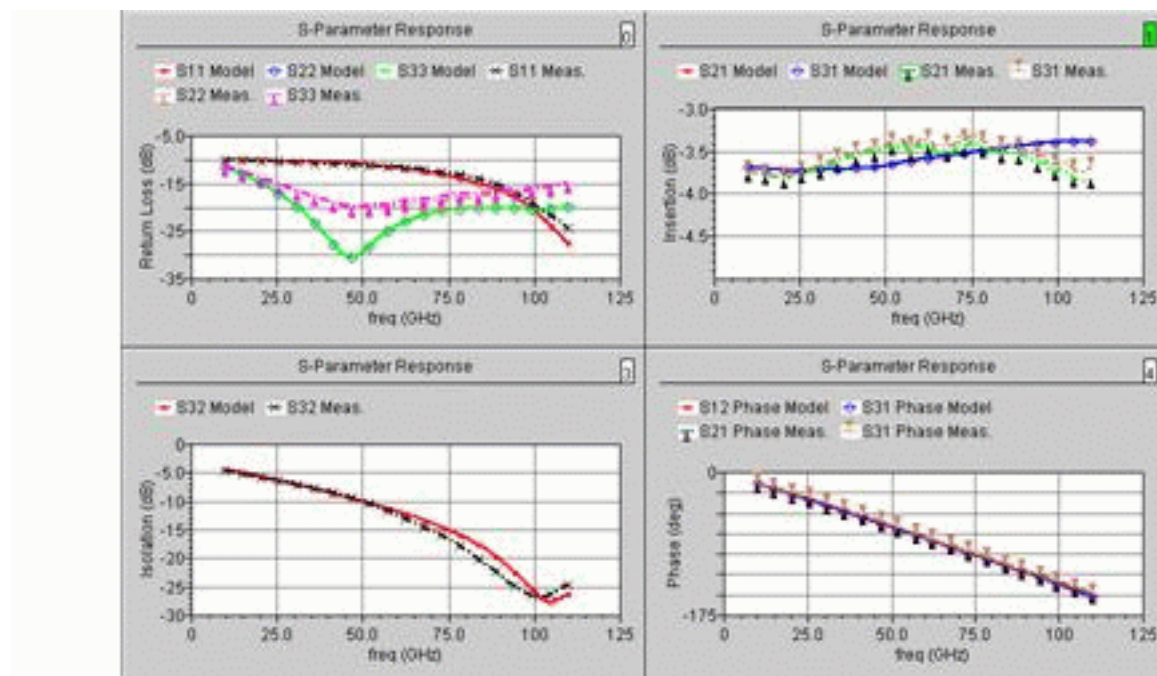


Figure 364. Comparison of Spectre model vs. measurement for a 94GHz powerdivider0. Top-left: Port reflection magnitude in dB; Top-right: S21 and S31 magnitude in dB; Bottom-left: S32 (isolation) magnitude in dB; Bottom-right: S21 and S31 phase in degree.

17.2.13 langecoupler

Model Topology

The Lange coupler “model” is a behavior-based model that uses multiple controlled sources and passive devices to provide a causal and stable model. The model was created from the s-parameters of the device obtained via a full-wave 3D EM solver. The model accounts for the losses, coupling, and Si-substrate effects. Figure 365 shows the symbol for the langecoupler device.

Model Limitation

Since the langecoupler was constructed as a behavioral model, it does not predict correct noise behavior of the device at this time.

Model Verification

The langercoupler models have been verified for a number of different configurations. Figure 366 shows a comparison of model simulation vs. EM simulation vs. hardware for a 60 GHz Lange coupler structure. This Lange coupler structure consists of a langecoupler and 4 singlewires. The singlewires are used to extend the ports to certain length for the measurements. The langecoupler has “Total Length” of 580um, “Metal Levels” of 5, and “Temperature Delta” of 0. The singlewires connected to Port1 (LC1) and Port4 (LC4) have signal width of 10um on LY, bottom ground shield on M1, “Metal Levels” of 5 and “Length” of 56.61um. The singlewires connected to Port2 (LC2) and Port3 (LC3) have signal width of 10um on LY, bottom ground shield on M1, “Metal Levels” of 5 and “Length” of 145.47um. In the figure, the solid square-marked (red/pink) lines are the model simulated data, the dash x-marked (blue) and up-arrow marked (light blue) liens are the EM simulated data, and the dot x-marked (black) and down-arrow (grey) marked lines are the measured data.

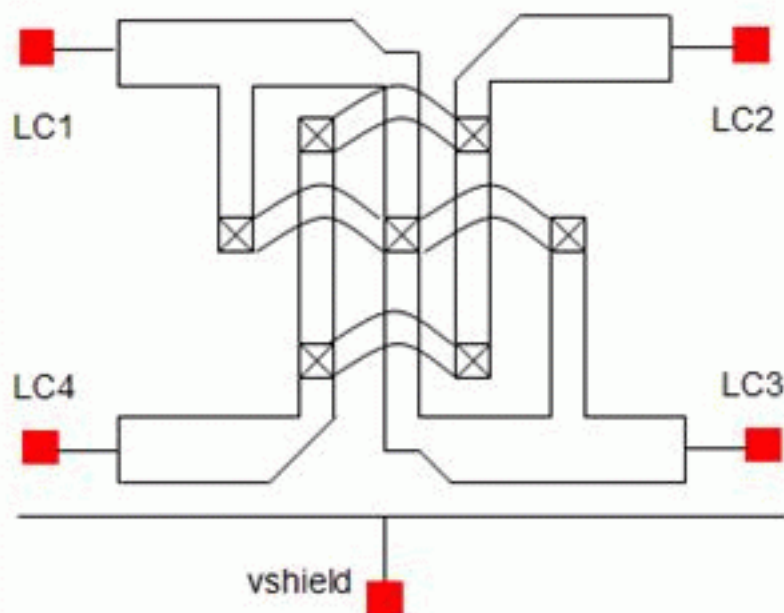


Figure 365. Schematic symbols of langecoupler

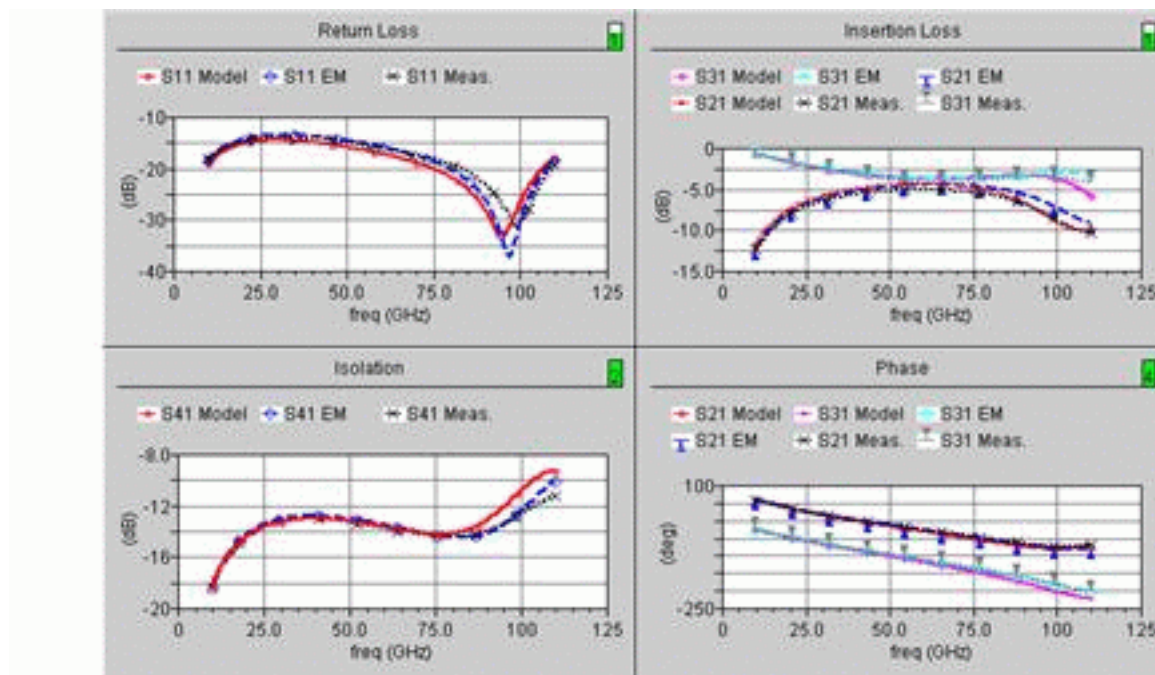


Figure 366. Comparison of Spectre model vs. EM vs. measurement for a 60GHz Lange coupler. Solid lines: model data; Dash lines: EM data; Dot lines: measured data; Top-left: S11 magnitude in dB; Top-right: S21 (coupling) and S31 (through) magnitude in dB; Bottom-left: S41 (isolation) magnitude in dB; Bottom-right: S21 (coupling) and S31 (through) phase in degree.

17.2.14 ratracehybrid

Model Topology

The Rat Race Hybrid “model” is a three level hierarchical sub-circuit, which calls models of tee, bend, singlewire and meanderline1. The meander shaped line is used to reduce the overall area of the coupler. Figure 367 shows the layout and sub-circuit model for the Rat Race coupler.

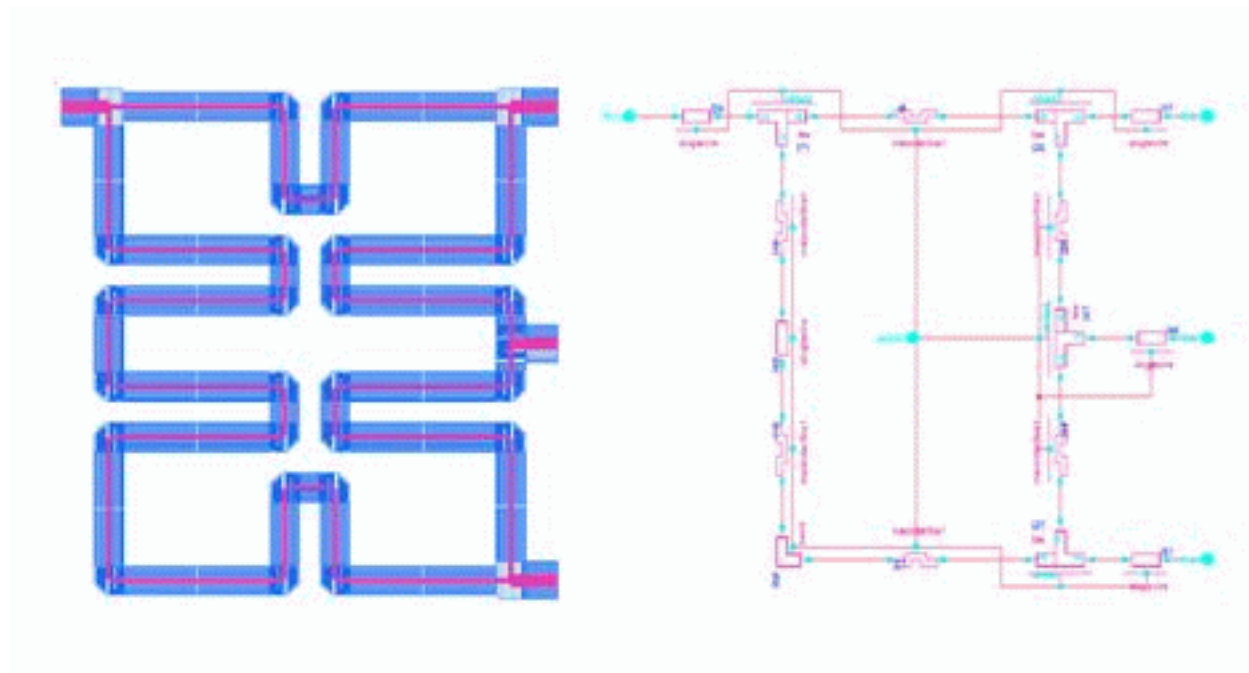


Figure 367. Pcell and sub-circuit model for ratracehybrid

Model Verification

The ratracehybrid model has been verified for a number of different configurations using EM simulations (Ansoft HFSS). Figure 368 shows a comparison of model simulation vs. EM simulation for a 60 GHz Rat Race Hybrid design. This design uses AM as signal metal without side shields and MQ as bottom ground shield. The signal line width is 4.4um with port line width of 13um. The branch length is 620um (effective quarter wavelength). In the figure, the solid (red/pink) lines are the model simulated data and the dash (blue/green) lines are the EM simulated data.

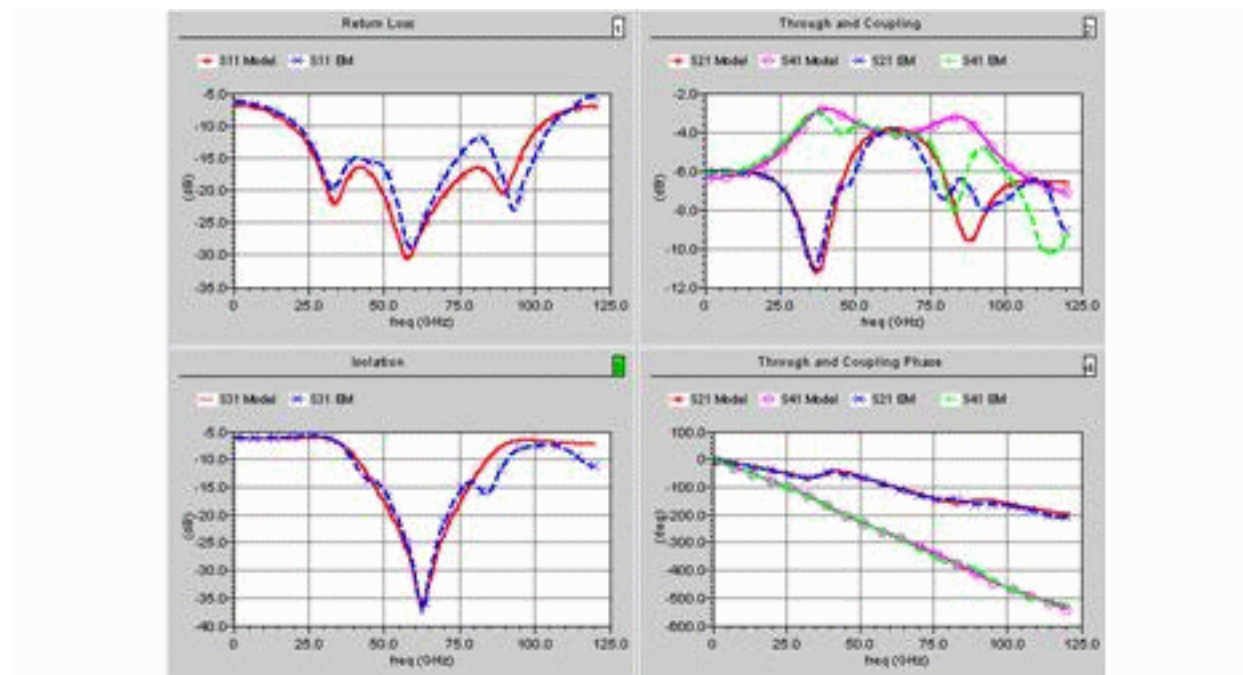


Figure 368. Comparison of Spectre model vs. EM for a 60GHz ratracehybrid. Solid lines: model data; Dash lines: EM data; Top-left: S11 magnitude in dB; Top-right: S21 (through) and S41 (coupling) magnitude in dB; Bottom-left: S31 (isolation) magnitude in dB; Bottom-right: S21 (through) and S41 (coupling) phase in degree.

17.3 Common Features added to the Device CDF

- Characteristic impedance callback function is added to all DP device CDF. This function will estimate a high frequency characteristic impedance value once a line width is given for given signal and return metal layers.
- For functional DP devices (Branch coupler, Wilkinson power divider, Lange coupler and Rat Race hybrid), a one-click S-parameter plotting function is added to the CDF (button at the bottom of the CDF window). Once the button is clicked, a background S-parameter simulation will be run based on the predefined setup and the full S-parameters for the device will be plot automatically. This function allows user to check the device performance before to place it into either schematic or layout.

Figure 369 shows the CDF for branchcoupler1 with Z0 callback and one-click plotting functions.

17.4 T-Line Path Creation Tool

A T-Line path creation tool (Create T-Line Path) is added under Misc of IBM_PDK tab in Virtuoso Layout Editing window. This tool allow users to draw a transmission-line path between any two points using TL1s (singlewire) and bends just like drawing a normal path connection. The tool also allows user to generate a symbol for the T-Line path created so that they can be used in schematic simulations. Figure 370 shows the T-Line Creation Tool window and an example T-Line created using the tool.

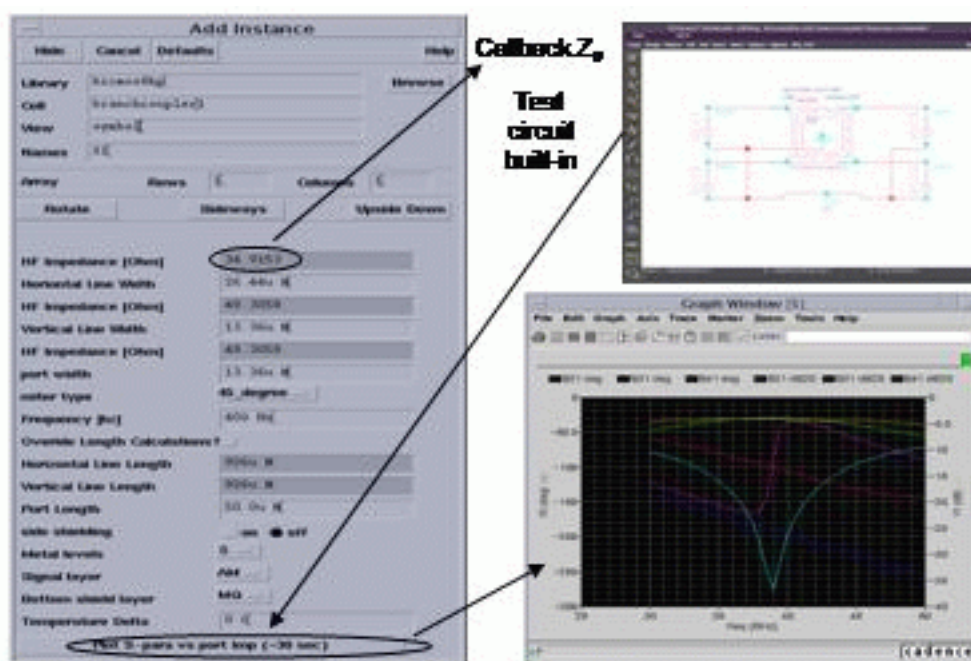


Figure 369. Callback and one-click functions in the CDF window.

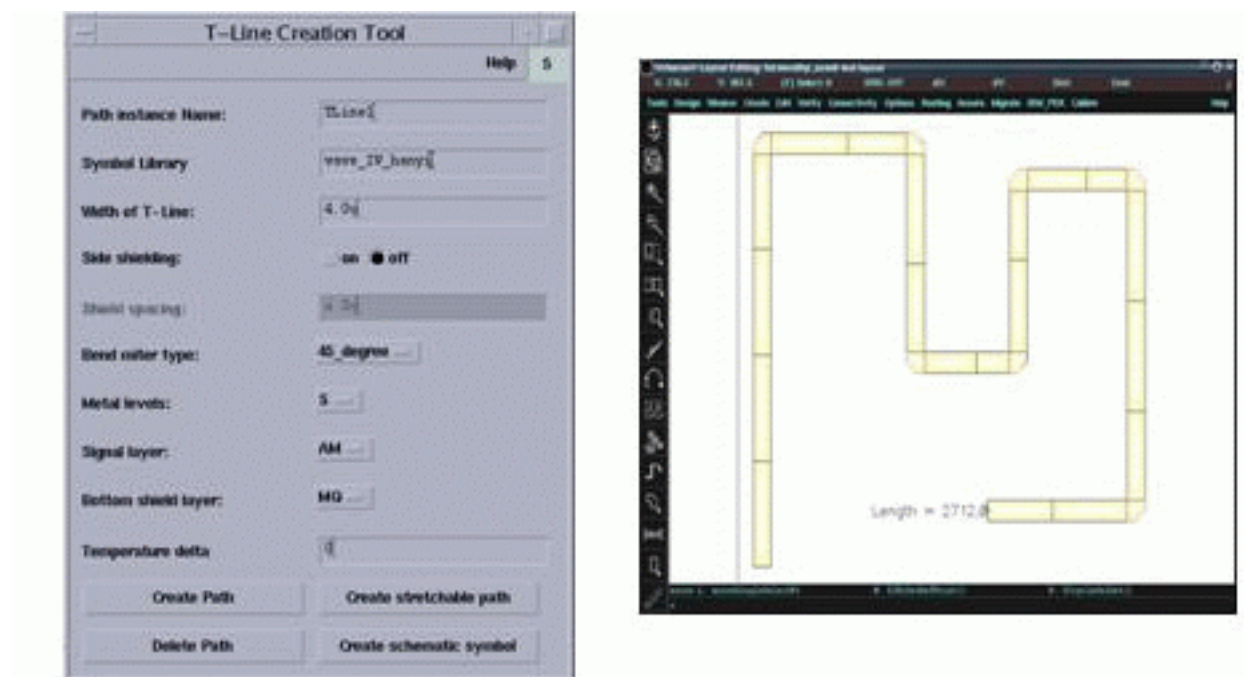


Figure 370. T-Line Creation Tool window and an example T-Line created using the tool



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