
BiCMOS8HP

Design Manual

Owner: Department 9G8A
Analog & Mixed Signal Technology Development
IBM Microelectronics Division

ES Number: ES#70P3264

Version Date: December 14, 2011
Document Review Date: 02/01/2012

Engineering Specification Changes

EC# H96318	July 14, 2004
EC# J93676	Oct. 7, 2005
EC# J87934	Jan. 19, 2007
EC# J97129	July 18, 2007
EC# L87575	May 12, 2011
EC# L88035	June 29, 2011
EC# L88560	December 14, 2011

Manufacturing TPRS Name: SIGE8HP

This document is maintained by Mixed Signal Technology Development Solutions. Users should not make unauthorized copies or alterations. It is the user's responsibility to verify that the hard copy version date is the most current version by contacting the document author. Instructions for verification may be found in section "Document Distribution and Ownership" on page 15.

THIS HARD COPY MUST BE PROMPTLY REMOVED FROM USE WHEN OBSOLETE.

Notices:

WITH RESPECT TO MATERIALS AND INFORMATION PROVIDED BY IBM, NO WARRANTIES EXPRESS OR IMPLIED, INCLUDING ANY IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, ARE OFFERED HEREIN. In no event shall IBM be liable for any actual, incidental, consequential, or other damages, including lost profits or lost savings, even if it is given prior notice of the same, which result from any use of the materials or information.

Copyright:

© Copyright International Business Machines Corporation 2003, 2004, 2005, 2006, 2007, and 2011. All rights reserved. Redistribution is not authorized without the express written permission of IBM Mixed Signal Technology Development Solutions.

Note to U.S. Government Users – Documentation related to restricted rights – Use, duplication or disclosure is subject to restrictions set forth in GSA ADP Schedule Contract with IBM Corporation.

Trademarks:

GDSII and Spectre are trademarks of Cadence Design Systems, Inc.
HSpice is a trademark of Synopsys, Inc.

V1.2.3.0: (Version Date: December 14, 2011)

This version of the BiCMOS8HP Design Manual applies to the V1.2.3.0 version of the BiCMOS8HP models and design kit. It will also apply to all subsequent releases, versions, and modifications until otherwise indicated in new editions or addenda. The TPRS manufacturing technology name to which this manual applies is SIGE8HP, the FEOL process specification ES is 70P9534 and the ILETs specification ES is 70P8879.

For access to this manual, please contact your IBM Product Engineer. Any comments, questions, suggestions, or additions regarding its contents can also be addressed to:

E-mail: fdrytech@us.ibm.com

Analog and Mixed Signal Technology Development
IBM Microelectronics Division
B/972-1
1000 River St.
Essex Junction, VT 05452-4299

Contents

1.0 Technology Introduction	9
1.1 Technology Features	9
1.2 Ordering Information	11
1.3 Document Distribution and Ownership	15
1.4 Document Change Approval	16
1.5 Summary of Changes	17
1.6 Chip Design Check List	18
1.7 Change list	18
1.8 BiCMOS8HP Cross Section	21
2.0 Physical Layout Information	25
2.1 Design Grid	25
2.2 Mask Level Definitions	25
2.3 Dummy Design Levels and Utility Levels	36
2.4 Masks for Non-Design Levels	43
2.5 Level Generation and Design Preparation	44
2.6 Mask Metallization Options	49
2.7 Design Truth Tables	49
2.8 Design Geometry Restrictions	56
2.9 Important Design Guidelines	59
2.10 Pattern Density Rules	62
3.0 Layout Rules	69
3.1 Polysilicon and Isolation Layout Rules	69
3.2 Contact (CA, CABAR) Layout Rules	80
3.3 N-well, Contact, Junction Layout Rules	83
3.4 Threshold Voltage Rules	89
3.5 BP Layout Rules	90
3.6 Butted Junction Layout Rules	94
3.7 CA, Metals and Via Layout Rules	96
3.8 Analog Layout Rules	119
3.9 Vertical PNP (VPNP) Rules	134
3.10 Mask Process Control Images	139
3.11 ESD Rules	140
3.12 ESDIODE Layout Rules	153
3.13 Forward-Biased Diode Layout Rules	154
3.14 OP Resistor Layout Rules	157
3.15 NS Subcollector Diffused Resistor	163
3.16 PD Layout Rules	163
3.17 OP RR Resistor (RR) Layout Rules	164
3.18 KQ Resistor Layout Rules	166
3.19 BFMOAT Design Rules	169
3.20 DG Layout Rules	169
3.21 nFET-in-Nwell (VAR) Device Layout Rules	173
3.22 Triple Well (Isolated) NFET Layout Rules	175
3.23 Electrical Fuse	180
3.24 HA Varactor (JD) Layout Rules	185

3.25 Metal-to-Metal Capacitor (MIM) Layout Rules	186
3.26 Inductor Layout Rules	189
3.27 Transmission Line and RF Interconnect Layout Rules	191
3.28 Terminals, IO Pads, C4 and Wirebond	193
3.29 Slots in Wide Metal	202
3.30 Chip Guard Ring and Chamfer	203
3.31 Protect Layer	208
3.32 Crackstop	213
3.33 Product Labels	213
3.34 No Polyimide Final Passivation option	217
3.35 Allowable Chip (CHIPEDGE) Sizes	218
3.36 Latchup Guidelines, Layout Constraints, and Rules	221
4.0 Electrical Parameters and Models	243
4.1 Available Devices and Models	243
4.2 Si/SiGe Heterojunction Bipolar Transistor	244
4.3 Vertical PNP Bipolar Transistor	246
4.4 General FET Design Discussion	247
4.5 Electrical Parameters of FETs	255
4.6 Junction Diodes	260
4.7 Resistor Models	265
4.8 NCAP and DGNCAP Models	273
4.9 Differential Varactor	275
4.10 Hyperabrupt (HA) Junction Varactor Diode	275
4.11 MIMCAP	277
4.12 Capacitor Application Notes	279
4.13 Forward-Biased Diode Device Models	279
4.14 Wiring Resistance and Capacitance Models	282
4.15 Electrical Moat Parameters	294
4.16 Inductor Models	297
4.17 Rfline Device Models	299
4.18 Capacitive Loading/Transmission Line Effects for Arbitrarily Shaped Interconnects	300
4.19 Bondpad Models	302
4.20 Shielded Transmission Line (T-line) Interconnect Models	303
4.21 Distributed Passive (DP) Devices	313
4.22 Mixed Voltage Interfaces	325
5.0 Reliability Design Rules and Models	331
5.1 Guidelines for Optimal Reliability	331
5.2 Reliability Screening	332
5.3 Front End Of Line (FEOL) Reliability Design Rules	334
5.4 Back End Of Line (BEOL) Reliability Design Rules	358
6.0 Electro-static Discharge (ESD) Protection	369
6.1 General	369
6.2 Usage Rules	370
6.3 Placement and Wiring	371
6.4 ESD Protection Circuits	372
6.5 Device Considerations	381
6.6 SiGe NPN Transistors	382
6.7 CMOS Receiver Circuits	383

6.8 ESD CMOS FET OCD Design Rules	383
6.9 Miscellaneous I/O Elements	386
6.10 Electro-static Discharge (ESD) Wiring Rules	386
6.11 Salicide-blocked FETs for ESD	388
6.12 ESD Background and Experimental Data	389
6.13 ESD Schematic level checks	389
7.0 Design for Manufactureability	395
7.1 Yield Enhancement Design Techniques	395
7.2 Design for Manufactureability Initiatives	399
Appendix A. Guidelines for Optimal Model-Hardware Correlation	407
Appendix B. Total Standby Current (I_{dd})	408
Appendix C. Design Hierarchy Guidelines	410
Appendix D. Rule Syntax (Definitions)	411
Appendix E. Definitions of Process-Related Terms	414
Appendix F. Migration into Future Technologies	415
Appendix G. Design Preparation	416
G.1 Complex Optical Manipulations	416
G.2 Dense SRAM Design (Not Offered)	416
G.3 PC	416
G.4 Far BEOL Manipulation	416
Appendix H. Pattern Fill Rules	417
H.1 xxFILL and xxHOLE Generation	417
H.2 Recommended Design Practices Related to Generated FILL and HOLES Shapes	432
Appendix I. MxPLANE Information	434
I.1 Introduction	434
I.2 Definitions	434
I.3 Design Considerations	434
I.4 Design Guidelines	435

This Page Intentionally Left Blank

1.0 Technology Introduction

This manual describes the BiCMOS8HP technology.

Note: Items that are defined with Gray shading within this Design Manual are preliminary and may become a feature of the BiCMOS8HP technology. However, these items are not supported or qualified at this time and are not guaranteed to be offered.

1.1 Technology Features

General CMOS Process

- $V_{dd} = 1.2V$ with option for 1.5 V use.
- Starting substrate resistivity of 11-16 ohm-cm
- Twin well CMOS technology on non-epi P^- substrate.
- Shallow trench isolation (STI).
- Dual gate oxide with physical thicknesses 2.2 nm and 5.2 nm.
- Minimum lithographic image = 0.12 μm (gate only).
- Low resistance Co salicided N^+ and P^+ polysilicon and diffusion areas.
- 5, 6 or 7 levels of global metal (two-to-four levels of 1x Copper; M1, M2, M3, M4, 1 level of 2x Copper; MQ, 2 levels of Analog Metal; LY, AM; see Section 2.6 , “Mask Metallization Options” on page 49)
- Tungsten stud contact connecting polysilicon or diffusion to the first metal level.
- Common wiring level vias V1, V2, VL with additional via options related to various metal options (see Section 2.6 , “Mask Metallization Options” on page 49).
- Planarized passivation and interlevel dielectrics with low-K (FSG) value.
- Wire-bond pads or controlled collapse chip connections (C4s)
- Optional Electronic Fuse

List of supported base feature devices:

- Thin oxide surface channel¹ NFET and PFET with $L_p \geq 0.092 \pm 0.011 \mu m$
- NPN High Performance
- ESD Devices
 - Vertical ESD PNP (P^+/NW diode) (esdvpnp)

1. The L_p tolerance is the 3σ chip mean variation (chip-to-chip) and does not include across-chip linewidth variation (=ACLV).

- N+/SX diode
- NW/SX diode
- Modelled device structures:
 - Inductors (2 variants)
 - Bondpads (C4 and Wirebond; (2 variants each)
 - RF Interconnect Lines
 - Transmission Lines
 - Distributed Passives
 -

List of supported devices not requiring additional masks, and are feature options:

- PCDCAP/MOS Varactor (for 1.5V operation) (optional)
- Resistors:
 - p+ polysilicon (2 placement variants)
 - NS resistor
- Electronic Fuse
- Forward-Biased (DI) Diode
- PCDCAP (diffncap) Thin Oxide (similar to Thin Oxide MOS Varactor)

List of Features and optional devices requiring additional masks:

- NPN High Breakdown (optional, requires 1 design mask)
- Thick oxide devices for native 2.5V operations, I/O and analog applications (minimum $L_{drawn}=0.24\mu m$)(optional, requires 1 design mask, and 2 or 3 additional derived mask levels)
- Thin Oxide Triple Well (optional, requires 1 design mask)
- Thick Oxide Triple Well (optional, requires 2 design masks, 2 additional derived mask levels)
- HA Varactor (optional, requires 2 masks; 1 additional design mask; JD, 1 additional generated mask; VI)
- PCDCAP/MOS Varactor (for 2.5V operation) (optional, requires 1 additional design mask)
- Metal-Insulator-Metal (MIM) Capacitor (optional, requires 1 additional design mask -- QY, 2 placement variants)
- Resistors:
 - RR resistor (optional, requires 1 additional mask, 2 placement variants offered)

- KQ resistor (Back-End-Of-Line resistor) (optional, requires 1 additional mask)
- Spacer Reintegration Feature (PF, PQ, no PX)
- Vertical PNP (4 additional masks) (vpnp_{sx})
- ESD Devices:
 - Salicide Blocked ESD Regular (Thin Oxide) NFET (requires 1 additional mask, OP). See Table 1-1 on page 12 and select Miscellaneous FEOL feature option.
 - Salicide Blocked ESD (2.5V) Thick Oxide NFET (requires 2 additional masks; DG, OP, and 2 additional derived masks; DW, DE. See Table 1-1 on page 12 and select Thin oxide + thick oxide feature option and Miscellaneous FEOL feature option. Note: a fifth mask; DF, is also used during processing with these feature selections.

The technology is intended to be operated over the following temperature and voltage ranges:

- Maximum power supply voltage of 1.6V ($1.5V \pm 0.1V$ power supply) for 2.2nm oxide field-effect transistors (FETs), 2.7V ($2.5V \pm 0.2V$ power supply) for the 5.2nm oxide FETs.
- Maximum HA Varactor use voltage = 3.6V
- Maximum MIM use voltage: See section 4.22.9 , “VMAX for MIM Capacitor” on page 329.
- For P+ Polysilicon, RR or KQ Resistor limits, see Table 4-17, “Resistor Design Specifications” on page 265 and Section 5.3.7 , “Resistor Reliability” on page 353.
- Operating temperature range of -55 to 125°C (junction Temp.)

List of devices or features that are not supported in the BiCMOS8HP technology:

- Dense SRAM
- Last Metal Fuse
- FETs: Low V_t, Zero-V_t, High V_t, Low Power (super-high) V_t, 3.3V I/O Devices
- PC groundplane modelled bondpad
- Resistors: N+ Diffused, N-well

1.2 Ordering Information

Designers can use Table 1-1 to compile a list of features and part numbers required by IBM manufacturing. For more information, contact your IBM technical representative, or the Foundry Technical Support team by sending an E-mail to fdrytech@us.ibm.com, or through the web at <http://www.ibm.com/technologyconnect>. Feature availability and use restrictions are for reference only and may change. Requested features will be evaluated based on current information as part of the ordering process.

Note: All Shaded Gray Features are not offered in the BiCMOS8HP technology at this time and are RESTRICTED

Table 1-1. Optional Features with Feature Part Numbers

Feature Group and Restrictions	Description	Additional Masks ¹	Feature Part Number ²	
			With PX	Without PX
Always included	Base features for BiCMOS8HP (SIG8HP) ^{3,4}	-	70P8901	Same
Oxide Choice (select one)	Thin Oxide Only	-	75H3168	Same
	Thin Oxide + Thick Oxide	DE, DF, DG, DW	70P0331	Same
Thin Oxide Optional Devices (select any)	Thin Triple Well NFET	PI	70P7900	Same
	PCDCAP (thin ox decoupling capacitor)	-	75H3027	Same
	Varactor (thin ox)	-	75H3089	Same
Thick Ox Optional Devices (select any)	Thick Triple Well NFET	DE, DG, DW, PI	70P7901	Same
	PCDCAP25 (thick ox decoupling capacitor)	DG	75H3219	Same
	Varactor (thick ox)	DG	70P7902	Same
Thin Ox Vt NFET Choice	Regular Vt NFET	-	75H2982	Same
Thin Ox Vt PFET Choice	Regular Vt PFET	-	75H3093	Same
Transistors (select any)	Higher Breakdown	DS	27R4768	Same
Miscellaneous FEOL Must Select One	Standard Spacer Integration No longer supported ⁵	-	70P8901	-
	Spacer Reintegration Selection REQUIRED ⁶	PF, PQ, no PX	-	84Y8169
Vertical PNP Must Select Spacer Reintegration	Vertical PNP	OZ, DE, EV, (EH ⁷), T3	-	84Y6775
Diode (select any)	HA Varactor Diode	JD, VI	70P7907	Same
	DI Diode ⁸	-	70P0106	Same
Resistors (select any)	OP PPOLY	-	46L0744	Same
	PC OP RR polysilicon resistor	RR	57P4863	Same
	NS resistor	-	45L8354	Same

Table 1-1. Optional Features with Feature Part Numbers

Feature Group and Restrictions	Description	Additional Masks ¹	Feature Part Number ²	
			With PX	Without PX
Metallization Options (Levels of Metal) (must select one)	Five metal levels (5LM) (M1, V1, M2)	See Table 2-7, “Back End Of Line (BEOL) Metalliza- tion Options,” on page 49	01L6952	Same
	Six metal levels (6LM) (M1, V1, M2, V2, M3)		01L6953	Same
	Seven metal levels (7LM) (M1, V1, M2, V2, M3, V3, M4)		29L6986	Same
Analog Metal, (Last Metal) REQUIRED	Analog Metal	AM	06K3730	Same
Wiring Metal (Second to Last Metal) REQUIRED	Low resistivity metal wiring level directly below the AM level	LY, PY	70P8026	Same
Wiring Metal (3rd to Last Metal) REQUIRED	One Thick copper level	MQ, VL	27R4770	Same
Via (Via to 2nd last metal) REQUIRED	VY Via	VY	20F8337	Same
Via (Via to last metal) REQUIRED	AV Via	AV	06K3731	Same
Metal-to-Metal (MIM) Capacitor option	AM-1 MIMCAP (QY) capaci- tor, 1.0 +/- 15% fF/μm ²	QY	20F8334	Same
Resistors BEOL	TaN BEOL Resistor	KQ	27R4771	Same
Fuse Selection	Electronic Fuse (eFuse)	-	57P6150	Same
Final Via (select one)	DV (must also select Wirebond Bonding Type)	DV	29L5231	Same
	LV (must also select C4 Plated Bonding Type)	LV	01L6998	Same
	DV - without Polyimide ⁹ Must also include ID shape NOPLYMD in layout. Must also pick Not Bumped or Bonded by IBM (21L2039)	DV	39N3035	Same
	LV - without Polyimide ⁹ Must also include ID shape NOPLYMD in layout. Must also pick Not Bumped or Bonded by IBM (21L2039)	LV	48J7330	Same

Table 1-1. Optional Features with Feature Part Numbers

Feature Group and Restrictions	Description	Additional Masks ¹	Feature Part Number ²	
			With PX	Without PX
Bonding Type (select one)	C4 Plated (must select LV Final Via)	-	01L6993	Same
	Wirebond (must select DV Final Via)	-	01L6995	Same
	Not Bumped or Bonded by IBM (must also pick either DV - No Polyimide Final Via option or LV - No Polyimide Final Via option)	-	21L2039	Same
Reliability Grade (select one)	Grade 3	Grade 3	29L5234	Same
	Consumer Grade 4	Consumer Grade 4	66P7361	Same
	Industry Standard (Std) Foundry Screen	Industry Std. Foundry Screen	29L5235	Same

1. Additional masks beyond the base feature-required front-end-of-line mask levels (that is, ZL, NS, DT, RX, DY, RN, BT, NW, BF, PX, PC, BH, PH, BX, CX, LE, EX, NP, PB, BP, BN, OP, and CA).
2. Features marked "limited" have some restrictions on use. The base features part number represents standard processing for that technology. In order to ensure correct manufacture of each part a list of features must be supplied to manufacturing. This table is intended to assist designers in providing the necessary information to their IBM Technical Representative. Feature availability and limitations are shown here for reference only and may change. Features must be evaluated based on current information as part of the ordering process.
3. The base feature part number represents the standard process for this technology. All designs also require the use of Back-End-Of-Line (BEOL) mask levels M1, V1, M2, VL, MQ as well as one of the Final Via and Bonding Type feature options. However, the M1, V1, M2, VL, MQ as well Final Via mask levels are not part of the base feature part number for this technology.
4. Designs based on the 0.13µm BiCMOS8HP (SIGE8HP) technology must include at least one thin-oxide NFET and one thin-oxide PFET.
5. Included in base Features, Standard Spacer Integration Feature no longer supported after 06/30/2011, contact your IBM technical representative for use restrictions.
6. Feature use optional prior to 06/30/2011, REQUIRED for all designs submitted to IBM after 06/30/2011.
7. Propagated from OZ.
8. Qualification pending.
9. IBM's technology level qualifications have included polyimide final passivation, but IBM sees no intrinsic impact to the wafer reliability failure rate for foundry customers who require wafers without polyimide. The customer is responsible however to evaluate product and packaging reliability failure rates for wafers without polyimide.

1.2.1 Non Qualified Devices or Features

Table 1-2. Non Qualified Features

Feature Description	Checked by Rule(s)
Forward-Biased (DI) Diode	-
PCDCAP (diffncap) Thin Oxide	-

1.3 Document Distribution and Ownership

The owner of this document is the manager of Mixed Signal Technology Development.

The author, who is responsible for the organization and approval of this document, is Lowell Nelson.

The complete and current version of this document can be obtained from the author. Please contact your IBM Product Engineer for assistance.

If you are on the document's distribution list and have been sent a manual directly, you will automatically be sent updates and/or reissuances as they become available. However, to be sure that you have the latest version or for information regarding future updates, please contact the author or your IBM Product Engineer.

Superseded versions of this document will be retained by the document owner for the life of the program. The final version of the document will be retained according to IBM corporate guidelines.

1.4 Document Change Approval

The following people review and approve any changes to this document.

Table 1-3.Document Approvers

Function	Name/Title	Date
AMS Technology Development	Lowell Nelson / Eng	12/14/2011
Design Services	Jeanne Sucharitaves / Eng	12/14/2011
Data Preparation	Michael Hulvey / Eng	12/13/2011
Technology Reliability	Ping-Chuan Wang / Eng	12/12/2011
Product Reliability Engineering	Ernest A. Viau / Eng	12/09/2011
BTV wafer fab ME	Brett Phillips / Eng	12/06/2011
Logic Bond, Assembly and Test	Tim Daubenspeck / Eng	12/09/2011
Wafer Finishing (Burlington)	Gary W. Lines / Eng	12/16/2011
Wafer Finishing (Bromont)	Stephane Mainville / Eng	12/06/2011
C4 Plated Terminal Metals ME	Sarah Knickerbocker / Eng	12/08/2011
Wafer Probing ME	Akiko Balchiunas / Eng	12/07/2011
Wirebond Packaging ME	John Malinowski / Eng	12/12/2011
Mask Product Engineering	Adam Smith / Eng	11/17/2011
AMS Modeling	Nick Schmidt / Eng	11/28/2011
Foundry Technology Enablement	Supatta Niramamkarn / Eng	12/07/2011
Foundry Products	Paul Pfeiffer / Eng	12/08/2011
ESD and Latchup	Mujahid Muhammad / Eng	12/09/2011
Kerf & Reticle Design	Mark Poulio t/ Eng	12/08/2011

Approval records for the revisions listed in Document Change Approval, are available from the author. Approvals for current versions will be retained indefinitely. Approvals for earlier versions will be retained for no less than one year after they are superseded.

1.5 Summary of Changes

The following is a history of this document and summarizes the changes made in each version and/or revision. A more complete list of changes, for the current version, can be found in the section Section 1.7 “Change list” on page 18.

Table 1-4. Summary of Changes

Version Date	Brief Change Description
Nov 6, 2003	V.0.0.0.0 Alpha Design Kit Version
Jan 20, 2004	V.0.0.1.0 Design Kit Version, Add DT local pattern density rule and delete DT option from passive devices.
July 14, 2004	V1.0.0.0 Design Kit Version - BiCMOS8HP Technology Qualification and Device Additions
Oct 7, 2005	V1030 Design Kit Updates, Revise KQ resistor and Thick Oxide PFET Vtlin specifications, Revise Design Services Appendix Rule Table descriptions, Update List of Document Approvers, Remove 4.5 on 9 C4 pitch and Moly Bump (Evaporated) Feature Part Number.
Jan 19, 2007	V 1.0.6.0 Design Kit: PC and M1 pattern density relaxations; change BT mask level; add DY mask level, remove PC bondpad, add M1 bondpad; enable square corner chipedge, update efuse specifications, document resistor current limit versus temperature, revise 2.2nm n-channel hot carrier parameters, and other reliability section information revision.
July 18, 2007	V 1.1.0.0 Design Kit: Change DY minimum values, add non-design mask levels PF, PQ, clarify other layout rules, change PC, LY, DT local pattern density rules to recommended rules, add predictive minimum PC global pattern density, remove QY minimum global density rule, add additional modelled devices, clarify table signs, update information in Reliability Section 5.0, including gate dielectric example text, update ESD Section 6.0 information and clarify post IBM design services validation rules in appendix section.
May 12, 2011	V1.2.0.0 Add VPNP Device. Updated MIM Rules. Add Estimated Pattern Density Rules / algorithms. Improved RX and M1 estimated pattern density checking. Relaxed M1, M2, M3, M4, & MQ; ground rules under Bondpads. Revised ESD Section Rules and add ESD Schematic Guidelines.
June 29, 2011	V1.2.1.0 Add Spacer Reintegration Feature, update VPNP Models, add VPNP reliability section.
December 15, 2011	V1.2.3.0 Updated VPNP models / specifications

1.6 Chip Design Check List

The following checklist is required to be completed prior to design data submission:

1. The design passes DRC (design rule checking). **Refer to the AMS User's Guide documentation for information on the required checks.**
2. Floating I/O pads are not allowed especially pads which are wired only to MIM Capacitors. C4s and Wire-Bond pads must have a DC connection to a RX shape (see GRs 908 and 953).
3. The design passes layout versus schematic (LVS) checking.
4. Simulations of all circuits produce acceptable behavior over the entire operating range and range of process variation, and produce acceptable behavior through wearout mechanisms modeled including Burn-In and total use conditions through the product lifetime.
 - No hot carrier shifts result in loss of circuit function, timing skew, performance shift or increases in standby current.
 - No contacts or metal lines carry more than their rated currents.
 - All circuits operate at the reliability screen conditions and/or at burn-in conditions (Section 5.1 , "Guidelines for Optimal Reliability" on page 331)
5. To ensure chip testability is not compromised by oscillations or other undesired behavior, module testing of RF products at IBM require chip level simulations using socket models. Socket models may be obtained from your IBM Product Engineer.
6. Electro-static Discharge (ESD) and latchup layout and design requirements have been met (see Section 6.0 "Electro-static Discharge (ESD) Protection" on page 369 and section 3.36 , "Latchup Guidelines, Layout Constraints, and Rules" on page 221).
7. No floating wells are present.
8. Internal power bus networks minimize local power supply drops and deviations.
9. Power supply networks test probe and package lead impedances match those expected to ensure functionality and testability.
10. Recommendations listed in section Appendix A., "Guidelines for Optimal Model-Hardware Correlation" on page 407 have been considered.
11. Recommendations listed in section Appendix C., "Design Hierarchy Guidelines" on page 410 have been considered.

1.7 Change list

Changes since the June 29, 2011 V.1.2.1.0 Design Manual version are;

- Cover: Updated Document Date and add EC # L88560
- Inside Cover: Change text from: V.1.2.1.0 (Version Date: June 29, 2011) to: V.1.2.3.0 (Version Date: December 14, 2011). Change Department: from "9GA8" to "9G8A".

The following changes were made to Section 1.0 , "Technology Introduction" on page 9;

- Section 1.2 , "Ordering Information" on page 11

- Table 1-1, “Optional Features with Feature Part Numbers” on page 12
- 1. Feature Vertical PNP removed “not qualified” text.
- Table 1-2, “Non Qualified Features” on page 15
- 2. Delete Row: “VPNP” (Feature now qualified).
- Table 1-3, “Document Approvers” on page 16
- 3. Row: Foundry Technology Enablement, change approver from “Bhagwat Mangla” to “Supatta Niramamkarn”.

The following changes were made to Section 3.0 , “Layout Rules” on page 69;

- Section 3.1 , “Polysilicon and Isolation Layout Rules” on page 69
 - Table 3-1, “Polysilicon and Isolation Layout Rules” on page 69
 - 4. Rule EPDL_RX_min modified text: “(rx_estimated) minimum density (%) over local 126mm x 126mm areas stepped in 63mm increments across the chip, except those checking boxes that touch LOGOBND or corner chamfers (PROTECT)...” to “(rx_estimated) minimum density (%) over local 126mm x 126mm areas stepped in 63mm increments across the chip, except those checking boxes that touch corner chamfers (PROTECT)....” Removed LOGOBND exclusion (to match PC&F deck)
 - Table 3-2, “Additional Isolation Layout Rules” on page 77
 - 5. Rule RX23a modified text: “RX(over BB, not over NW, over VPNP) must be covered by BPHOLE” to “RX(over BB, over NW, over VPNP) must be covered by BPHOLE”. Correct typo (no DRC updates).
- Section 3.7 , “CA, Metals and Via Layout Rules” on page 96;
 - 6. Figure 3-7. “CA, Metal, Via Interconnect Rules” on page 100, change “V2” adjacent to GR502 to “V1”.
- Section 3.25 , “Metal-to-Metal Capacitor (MIM) Layout Rules” on page 186;
 - 7. Rule QCAP1, removed text “(MIMCAPs \leq 8.00 μ m are not qualified)” and Footnote ¹: “QY MIMCAPs < 8.0um are not permitted”.
- Section 3.28.2 , “Wirebond” on page 198;
 - 8. Added text: “The customer is responsible for the qualification of non-IBM wirebond builds (non-IBM wirebond builds may have different requirements for: pads, metals, and devices under pads).”

The following changes were made to Section 4.0 , “Electrical Parameters and Models” on page 243;

- Section 4.3 , “Vertical PNP Bipolar Transistor” on page 246: **removed text “Not Qualified)”**;
 - Table 4-4, “Electrical Parameters for the Vertical PNP (0.4 mm x 2.5 mm, single emitter)” on page 246
 - 9. Beta and BVCEO specifications updated.
- Section 4.14 , “Wiring Resistance and Capacitance Models” on page 282
 - 10. Add Section 4.14.3 , “Wiring Capacitance Models” on page 287.
 - 11. Add Section 4.14.4 , “Interlevel Area Capacitance” on page 287.
 - 12. Add Section 4.14.5 , “Parameters for Capacitance Calculation” on page 287.
 - 13. Add Section 4.14.6 , “Wiring Capacitance Tracking” on page 289.
 - 14. Add Section 4.14.7 , “Quick Lookup Wiring Capacitances” on page 289.

15. Add Section 4.14.8 , “PC to CA Capacitance” on page 290.

- Section 4.14.11 , “Resistance and Capacitance Extraction Parameters” on page 291;

- Table 4-40, “Extraction Parameters for Metal Wiring” on page 292

16. Row AM resistance / Pattern Factor S 12.5, Column Physical Line Bias: value changed from -0.080 to +0.080.

17. Footnote ³ changed equation: from “Bias per edge = $[-((0.028 \times S) - 0.19)]/2$ Bias per edge = -0.08” to “Bias per edge = $[((0.028 \times S) - 0.19)]/2$ Bias per edge = 0.08”.

The following changes were made Section 5.0 , “Reliability Design Rules and Models” on page 331;

The following changes were made Section Appendix H., “Pattern Fill Rules” on page 417;

- Section H.1.1 , “Estimated Pattern Density Generation” on page 425;

- Table H-3. “Pattern Density Rules” on page 425,

18. Rule PD1a: Delete previous Footnote ¹ “RXFILL is not placed in LOGOBND in the KERF” and update Footnote ¹ to: “For this local density requirement, the checking box is 126mm x 126mm stepped in 63mm increments. Rule PD1a is not in force for any checking box that touches corner chamfers and PROTECT regions which are outside of CHIPEDGE. IBM includes RXFILL within LOGOBND regions. If a designer places an RXEXCLUDE within LOGOBND, it is expected that the checking box touching the (RXEXCLUDE over LOGOBND) still comply with the minimum density value specified. The only exception for RX local density is within the IBM KERF LOGOBND area, since RXFILL is not automatically included in this region. The interpretation of (RX, RXFILL) in this description is the equivalent of Union (RX, RXFILL), which is the sum of the Design Level RX and the Reserved Level RXFILL, for checking purposes of this rule. The Current Practice value specified is the value that is to be coded into the IBM Release Team Design Rule checking decks used by IBM, and represents the minimum density acceptable after Design Services is applied to a chip during the IBM release process.”

- Table H-4. “Estimated Pattern Density Rules” on page 427,

19. Rules: EPDLi_M1_min, EPDLi_M2_min, EPDLi_M3_min, EPDLi_M4_min, and EPDLi_MQ_min; changed units from “mm” to “μm”.

20. Equation RXEX_FRAME modified text: from: “Union(CHIPEDGE, CRACKSTOP) sized by -50” to “CHIPEDGE sized by -50”.

----- END OF CHANGE LIST -----

1.8 BiCMOS8HP Cross Section

The following figure is a schematic cross sections. The figure is not drawn to scale and many of the detailed process steps have been omitted. The figure is intended to give the reader a basic picture of the process flow and mask levels used.

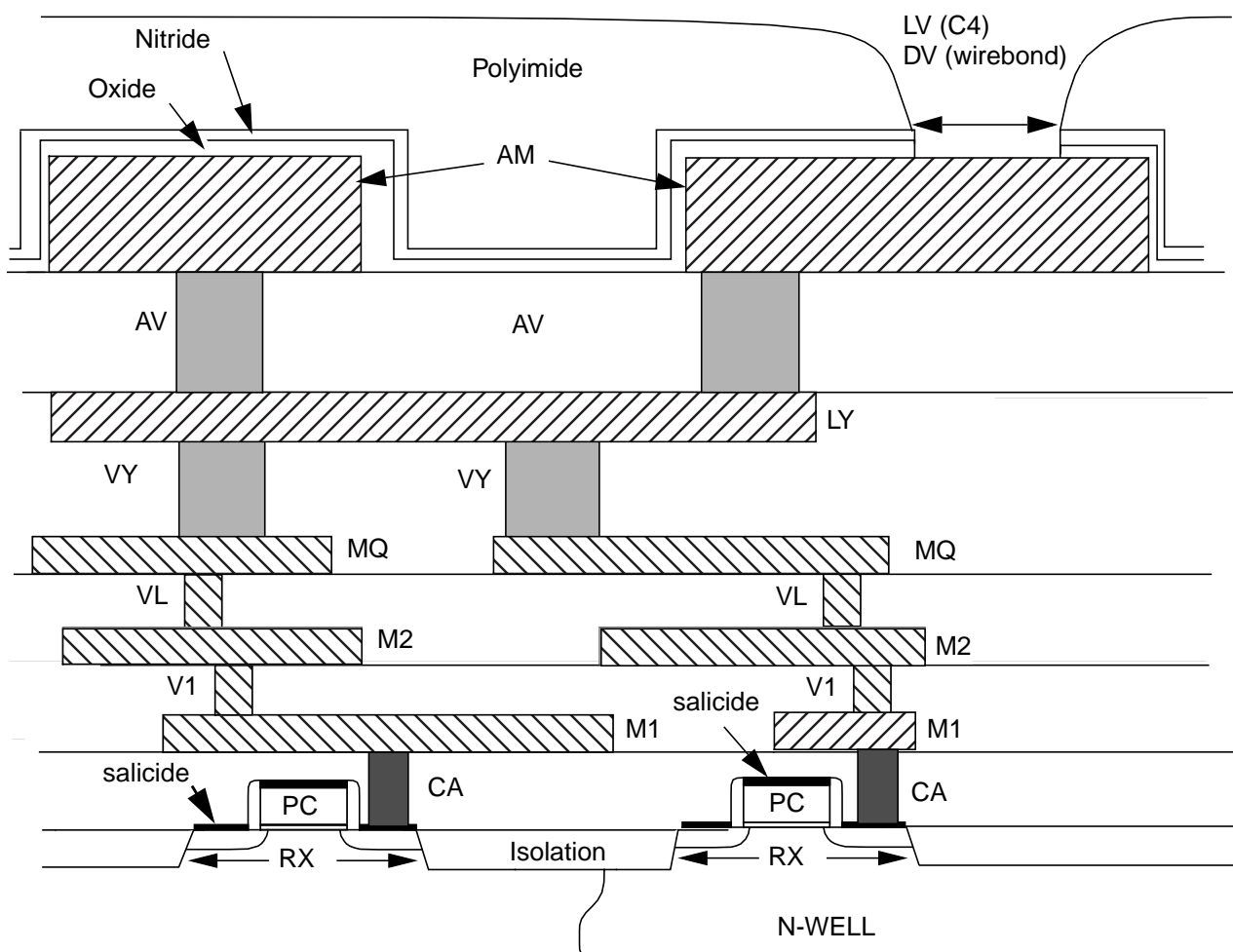


Figure 1-1. Cross Section of the 5 Level of Metal BEOL Option (2 Thin Mx; x=1,2 and 1 Thick = MQ and Analog Metal = LY, AM) with either DV or LV Final Passivation (not drawn to scale)



This Page Intentionally Left Blank

2.0 Physical Layout Information

2.1 Design Grid

BiCMOS8HP (SIGE8HP) designs are required to be laid out on a 0.01 - μm grid (see Table 2-13, “Geometry Restrictions,” on page 57 and section 3.35 , “Allowable Chip (CHIPEDGE) Sizes” on page 218 for more information).

2.2 Mask Level Definitions

Shapes drawn by a customer on any level other than those listed in Table 2-1 as Design Levels will not be included in the associated Mask Level. In order to prevent level name conflicts during Design Services, Data Preparation and Kerf Merge, the reserved design levels in Table 2-2, “Design Services and Data Preparation Mask Levels (Restricted),” on page 30 and Table 2-3, “KERF Dummy Design Levels (Restricted),” on page 35 can not be used by the designer. See Rules RL01 through RL07b in Table 2-14, “Reserved Level Layout Rules,” on page 58.

Appropriate metal and via levels must be submitted with BiCMOS8HP (SIGE8HP) designs as presented in Section 2.6 , “Mask Metallization Options” on page 49.

Table 2-1.Mask and Design Level Definitions

Mask Level	Design Level	CDS name	CDS purpose	Description
		GDSII number	GDSII type	
ZL	ZL	--	--	Alignment Level (for IBM KERF only; enablement is not required in Technology Design Kit; only GDSII definitions provided)
		12	92	
NS	NS	NS	dg ¹	Shape = N+ Subcollector (used for High Performance NPN, NS resistor and passive devices)
		0	0	
DS	DS	DS	dg ¹	Shape = N+ Subcollector (only used for High Breakdown NPN device) Use is OPTIONAL .
		0	5	
DT	DT	DT	dg	Shape = Deep Trench
		1	0	
RX	RX	RX	dg	Shape = active area (gate oxide and N ⁺ /P ⁺ diffused regions).
		2	0	
RN	RN	RN	dg	Shape = N+ Reach Through diffusion used to contact NS or DS in the NPN.
		23	0	

Table 2-1.Mask and Design Level Definitions

Mask Level	Design Level	CDS name	CDS purpose	Description
		GDSII number	GDSII type	
PI	PI	PI	dg ¹	Shape = Triple Well NFET N type isolation implant and Pwell. Use is OPTIONAL .
		6	33	
JD	JD	JD	dg	Shape = ion implant area for varactor HA device(s). Use is OPTIONAL .
		12	101	
T3	VPNP	VPNP	dg	Shape = Used over VPNP.
		212	148	
		T3	dg	Reserved Level for IBM use only. Shape = Isolation Well implant area.
		3	0	
NW	NW	NW	dg ¹	Shape = N-well region.
		4	0	
-	BB	BB	dg	Shape = Block Bipolar - this level is used to generate BT, BF and BP, BH.
		91	100	
PX	PX	PX	dg	Shape = NPN base protect area.
		58	0	
DG	DG	DG	dg	Shape = areas which have a thicker gate (5.2nm) oxide. Use is OPTIONAL .
		12	4	
PC	PC	PC	dg ¹	Shape = polysilicon line. (PC over RX within BP) over DG will receive the p-channel Dual Gate device mask compensation. (PC over RX outside of BP) over DG will receive the n-channel Dual Gate device mask comp. (PC not over RX) not over DG will receive the polysilicon wiring mask comp.
		7	0	
	PCING	PCING	dg	
		7	4	
	PCFUSE	PC	fuse	
		7	44	
OZ	OZ	OZ	dg	Shape = Window for VPNP collector implant.
		12	234	
EV	EV	EV	dg	Shape = Window for VPNP emitter opening.
		12	233	

Table 2-1.Mask and Design Level Definitions

Mask Level	Design Level	CDS name	CDS purpose	Description
		GDSII number	GDSII type	
BX	BX	BX	dg	Shape = Window for base-collector junction to form.
		29	6	
CX	CX	CX	dg	Shape = Collector pedestal mask.
		29	3	
LE	LE	LE	dg	Shape = NPN emitter landing pad
		29	5	
EX	EX	EX	dg	Shape = NPN emitter
		29	4	
NP	NP	NP	dg	Shape = NPN Polysilicon
		29	7	
PB	PB	PB	dg ¹	Shape = NPN base Polysilicon.
		29	8	
BP	BP	BP	dg	Shape = areas which are blocked from the n+ source/drain implant (identifies PFETs, P ⁺ junctions and substrate contacts).
		10	0	
BN	PD ²	BN	dev	Shape = P ⁺ implant area for contacts of high Resistance polysilicon resistor.
		11	1	
RR	RR	RR	dg	Shape = High value poly resistor. Use is OPTIONAL .
		12	107	
OP	OP	OP	dg	Shape = areas which are blocked from silicide formation over PC and RX, creating a resistor.
		37	0	

Table 2-1.Mask and Design Level Definitions

Mask Level	Design Level	CDS name	CDS purpose	Description
		GDSII number	GDSII type	
CA	CA	CA	dg ¹	Shape = square stud contact. CA connects either RX or PC to M1.
		14	0	
	CABAR	CABAR	dg ¹	Shape = rectangular stud contact. CABAR is allowed only in the bipolar transistor collector, the NS resistor and, Chip Guard Ring and Part Number / Labels. See Layout Rule 228 in Table 3-3, "CA, CABAR Layout Rules," on page 80.
		14	1	
	CEBAR	CE	BAR ¹	Shape = rectangular bar contact. CEBAR is allowed only in the NPN emitter contact.
		14	101	
M1	M1	M1	dg/vdd/ gnd ¹	Shape = first-level thin metal lines.
		15	0/0/0	
V1	V1	V1	dg ¹	Shape = square vias for connecting M1 to M2.
		16	0	
	V1BAR	V1BAR	dg ¹	Shape = rectangular vias for connecting M1 to M2. V1BAR is allowed only in the Chip Guard Ring.
		16	1	
M2	M2	M2	dg/vdd/ gnd ¹	Shape = second-level thin metal lines.
		17	0/0/0	
V2	V2	V2	dg ¹	Shape = square vias for connecting M2 to M3. Use is OPTIONAL .
		18	0	
	V2BAR	V2BAR	dg ¹	Shape = rectangular vias for connecting M2 to M3. V2BAR is allowed only in the Chip Guard Ring.
		18	1	
M3	M3	M3	dg/vdd/ gnd ¹	Shape = third-level thin metal lines. Use is OPTIONAL
		19	0/0/0	

Table 2-1.Mask and Design Level Definitions

Mask Level	Design Level	CDS name	CDS purpose	Description
		GDSII number	GDSII type	
V3	V3	V3	dg ¹	Shape = square vias for connecting M3 to M4. Use is OPTIONAL .
		20	0	
	V3BAR	V3BAR	dg ¹	Shape = rectangular vias for connecting M3 to M4. V3BAR is allowed only in the Chip Guard Ring.
		20	1	
M4	M4	M4	dg/vdd/ gnd ¹	Shape = fourth-level thin metal lines. Use is OPTIONAL .
		21	0/0/0	
VL	VL	VL	dg ¹	Shape = square vias for connecting M2, M3, M4 to MQ
		35	0	
	VLBAR	VLBAR	dg ¹	Shape = bar vias for connecting M2, M3, M4 to MQ
		35	1	
MQ	MQ	MQ	dg/vdd/ gnd ¹	Shape = first level of thick wiring.
		34	0/0/0	
KQ	KQ	KQ	dg	Shape = Metal Level (KQ) Resistor. Use is OPTIONAL .
		6	9	
VY	VY	VY	dg ¹	Shape = square vias for connecting MQ to LY
		129	0	
	VYBAR	VYBAR	dg ¹	Shape = bar vias for connecting MQ to LY or KQ to LY. VYBAR must be used in the Chip Guard Ring and to connect KQ to LY, and may also be used elsewhere in designs to connect MQ to LY.
		129	1	
LY	LY	LY	dg/vdd/ gnd ¹	Shape = Low resistivity metal wiring level directly below the AM level.
		42	1/1/1	
QY	QY	QY	dg	Shape = Aluminum MIM Capacitor Top plate for the single Aluminum MIM or Mid Plate for the dual Aluminum MIM Use of QY is OPTIONAL .
		30	5	

Table 2-1.Mask and Design Level Definitions

Mask Level	Design Level	CDS name	CDS purpose	Description
		GDSII number	GDSII type	
AV	AV	AV	dg ¹	Shape = square analog vias for connecting LY to AM or QY MIM plates to AM.
		52	0	
		AVBAR	dg ¹	Shape = bar analog vias for connecting LY to AM. AVBAR must be used in the Chip Guard Ring, and may also be used elsewhere in designs to connect LY to AM.
		52	1	
AM	AM	AM	dg/vdd/ gnd ¹	Shape = Analog metal for thick AlCu inductors, indlines, transmission lines, wiring channels, transfer pads. This level must be used with the LY level.
		53	0/0/0	
DV	DV	DV	dg ¹	Shape = opening in the final oxide/nitride passivation. Required for wire bond pad connections, probe pads, etc. Not used for C4 terminals.
		27	1	
LV	LV	LV	dg ¹	Shape = opening in the final oxide/nitride passivation to the AM level of metal. Required for C4 terminals only. Not used for wirebond pads or probe pads.
		28	0	

1. DRC will check to insure that the net purpose is not outside or straddling the dg (drawing) purpose on these design levels.

2. PD is not a mask level, it is a design level used for Data Preparation. See Mask Level BN in Table 2-6 on page 44. For PD rules, see Table 3-40 on page 163.

The mask levels, identified in Table 2-2, “Design Services and Data Preparation Mask Levels (Restricted),” on page 30, are for IBM use only. Designers shall not specify new mask levels, nor use design levels, similar to those identified in Table 2-4.

Table 2-2.Design Services and Data Preparation Mask Levels (Restricted)

Restricted Use Level	CDS name	CDS purpose	Description	Associated With
	GDSII number	GDSII type		
AMFILL ¹	AM	fill	Reserved Level Name. Used to fill empty space at the AM mask level to meet pattern density requirements of the manufacturing process.	Design Services, Pattern Density
	53	35		
DNIRxx ²	-	-	Reserved Level Names	Mask Merge

Table 2-2.Design Services and Data Preparation Mask Levels (Restricted)

Restricted Use Level	CDS name	CDS purpose	Description	Associated With
	GDSII number	GDSII type		
DPWAIVxx ³	-	-	Reserved Level for IBM use only, used for Dataprep layout checking (xx=any combination of alphanumeric characters)	Dataprep
FUSE ¹	OUT-LINE	fuse	Reserved Level Name. See Last Metal Fuse in section , “List of devices or features that are not supported in the BiCMOS8HP technology:” on page 11.	Design Services.
	60	26		
KERFEXCL ⁴	KER-FEXCL	dg	Reserved Level name for IBM use only, associated with optical and alignment structures in the manufacturing KERF. Used to inhibit xxFILL generation inside certain optical and alignment marks. KER-FEXCL is verified during DRC per Rule RL07a in Table 2-14, “Reserved Level Layout Rules,” on page 58 since it should not be present in a chip production design, except in the IBM developed KERF (outside CHIPEDGE).	Kerf Design
	101	250		
Kx (x=2,3,4) ⁵	-	-	Reserved Level Name	DRC
LMDUMHOL ⁵			Reserved Level Name	DRC
LYFILL ¹	LY	fill	Reserved Level Name. Used to fill empty space at the LY mask level to meet pattern density requirements of the manufacturing process.	Design Services, Pattern Density
	42	35		
Mx (x=5,6,G,T,E) ⁵			Reserved Level Name	Dataprep
MTDUMHOL ⁵			Reserved Level Name	DRC
MxCHEXCL ¹	Mx	chexcl	Reserved Level for IBM use only. Placed over specific areas of the chip that can not receive Mx (x=1,2,3,4,Q) Hole shapes.	Mx Hole Exclusion
(x=1)	15	47		
(x=2)	17	47		
(x=3)	19	47		
(x=4)	21	47		
(x=Q)	34	47		

Table 2-2. Design Services and Data Preparation Mask Levels (Restricted)

Restricted Use Level	CDS name	CDS purpose	Description	Associated With
	GDSII number	GDSII type		
MxEXCLUD ¹	Mx	exclude	Reserved Level for IBM use only. Placed over specific areas of the chip that can not receive Mx (x=1,2,3,4,Q) Fill shapes.	MxFILL Exclusion
(x=1)	15	2		
(x=2)	17	2		
(x=3)	19	2		
(x=4)	21	2		
(x=Q)	34	2		
MxFILL ¹	Mx	fill	Reserved Level Name. Used to fill empty space at the Mx mask level to meet pattern density requirements of the manufacturing process.	Design Services, Pattern Density
(x=1)	15	35		
(x=2)	17	35		
(x=3)	19	35		
(x=4)	21	35		
(x=Q)	34	35		
MxHOLE ¹	Mx	HOLE	Reserved Level for IBM use only. Used to check the interior of wide Mx (x=1,2,3,4,Q) wires to meet the pattern density layout requirements of the Copper manufacturing process.	Mx Density
(x=1)	15	1		
(x=2)	17	1		
(x=3)	19	1		
(x=4)	21	1		
(x=Q)	34	1		
NIX _{xx} ²	-	-	Reserved Level Names	Data Preparation
NOKERF	-	-	Reserved Level Name	Data Preparation
NONIAG _{xx}	-	-	Reserved Level Names	Data Preparation
NR ⁵			Reserved Level Name	DRC
NV ⁵			Reserved Level Name	DRC
NW_RES	-	-	Reserved Level Name	Design Kit
OUTLINE_RF	-	-	Reserved Level Name	Design Kit

Table 2-2.Design Services and Data Preparation Mask Levels (Restricted)

Restricted Use Level	CDS name	CDS purpose	Description	Associated With
	GDSII number	GDSII type		
OV	OV	dg	Reserved Level for IBM use only Shape = Photoresist opening to aid in the etching of the SV trench.	DRC/Dataprep
	190	0		
PAD_GBIT	PAD	GBIT	Reserved Level Name	Design Services
	41	26		
PCFILL ¹	PC	fill	Reserved Level Name. Used to fill empty space at the PC mask level to meet pattern density requirements of the manufacturing process.	Design Services, Pattern Density
	7	35		
PR ⁵			Reserved Level Name	DRC
PROBE ⁵	-	-	Reserved Level Name	DRC
PV ⁵			Reserved Level Name	DRC
PYFILL ¹	PY	fill	Reserved Level Name. Used to fill empty space at the PY mask level to meet pattern density requirements of the manufacturing process.	Design Services, Pattern Density
	153	35		
RP ⁵	-	-	Reserved Level Name	DRC
RXFILL ¹	RX	fill	Reserved Level Name. Used to fill empty space at the RX mask level to meet pattern density requirements of the manufacturing process.	Design Services, Pattern Density
	2	35		
SRAMCA SRAMM1 SRAMPC SRAMRX	-	-	Reserved Level Name	Design Kit
SV	SV	dg	Reserved Level for IBM use only. Shape = Through Silicon Via.	DRC/Dataprep
	184	0		
TSV	TSV	dg	Reserved Level for IBM use only. Shape = Photoresist opening to aid in the etching of the SV trench.	DRC/Dataprep
	212	160		

Table 2-2.Design Services and Data Preparation Mask Levels (Restricted)

Restricted Use Level	CDS name	CDS purpose	Description	Associated With
	GDSII number	GDSII type		
VPPCAP VPPCAPM _x (x=1,2,3,4,5,6) ⁵	-	-	Reserved Level Name	Design Kit
V _x HOLE	V _x	HOLE	Reserved Level for IBM use only. Used to tailor V _x in the presence of metal HOLE shapes.	Design Services
(x=1)	16	51		
(x=2)	18	51		
(x=3)	20	51		
(x=L)	35	51		
V _x HOLE (x=4,5,Q,G) ⁵	-	-	Reserved Level Name used to tailor V _x in the presence of metal HOLE shapes.	Dataprep
V _x (where x=4,5,G, A, M) ⁵			Reserved Level Name	Dataprep
V _x BAR (where x=4,5,G, A, M) ⁵			Reserved Level Name	Dataprep
WVR	-	-	Used with Waiver Shapes for DRC	DRC
XE ⁵	XE	dg	Reserved Level Name Shape = LDD for the 3.3V I/O nFET	DRC/Dataprep
	12	41		
XF ⁵	XF	dg	Reserved Level Name Shape = LDD for the 3.3V I/O pFET	DRC/Dataprep
	12	67		
x _B (x = 1,2,3,4,5,6,7,8) ⁵			Reserved Level Name	Mask House Process Control
xxANCHOR ²	-	-	Reserved Level Names	Data Preparation
xxCUS ²	-	-	Reserved Level Names	Data Preparation
xxNOTCH ²	-	-	Reserved Level Names	Data Preparation
xxOPC ²	-	-	Reserved Level Names	Data Preparation
xxOPCHOLE ²	-	-	Reserved Level Names	Data Preparation

1. Level is included in the Design Kit Technology File. For additional information, see Table 2-14, “Reserved Level Layout Rules,” on page 58.
2. “xx” = any combination of alphanumeric characters representing Design or Mask Level names.
3. “xx” = any combination of one or two alphabetic characters representing the Design or Mask Level names identified in Table 2-1, “Mask and Design Level Definitions,” on page 25.
4. KERFEXCL is included in the Design Kit Technology File. For additional information on KERFEXCL, see Table 2-3, “KERF Dummy Design Levels (Restricted),” on page 35 and Rule RL07a in Table 2-14, “Reserved Level Layout Rules,” on page 58.
5. Level is not used in the BiCMOS8HP technology, but is reserved.

The levels, identified in Table 2-3, “KERF Dummy Design Levels (Restricted),” on page 35, are for IBM use only. The levels in Table 2-3 can not be used by designers. Designers shall not specify new mask levels similar to those identified in Table 2-3.

<i>Table 2-3. KERF Dummy Design Levels (Restricted)</i>		
Restricted Use Level	Description	Associated With
KERFxxx ¹	Reserved Level for IBM use only, used in the kerf design and merged during mask assembly.	Kerf Design
KERFEXCL ²	Reserved Level for IBM use only, associated with optical and alignment structures in the manufacturing kerf. Used to inhibit xxFILL generation inside certain optical and alignment marks.	Kerf Design
KERFNUL	Reserved Level for IBM use only, used in the kerf design and merged during mask assembly	Kerf Design
NEGMKS	Reserved Level for IBM use only, used during the auto kerf merge process during mask assembly of CN masks, associated with data extremes.	Kerf Design and Mask Merge
POSMKS	Reserved Level for IBM use only, used during the auto kerf merge process during mask assembly of CP masks, associated with data extremes.	Kerf Design and Mask Merge
FRAME	Reserved Level for IBM use only, Reserved Level, used during the auto kerf merge process during mask assembly of CP masks, associated with shutter blade positioning.	Kerf Design and Mask Merge

1. “xxx” = any combination of one, two or three alpha-numerics.
2. For additional information on KERFEXCL, see Table 2-2, “Design Services and Data Preparation Mask Levels (Restricted),” on page 30 and Rule RL07a in Table 2-14, “Reserved Level Layout Rules,” on page 58.

2.3 Dummy Design Levels and Utility Levels

The following levels are drawn by the designer. CHIPEDGE is required for all chip designs.

Table 2-4. Dummy Design Levels and Utility Levels

Design Level	CDS name	CDS purpose	Description	Associ- ated With
	GDSII number	GDSII type		
AMESD ¹	AM	esd	Shape = Label that is used to identify pads used for ESD and Latchup Rule checking	DRC
	53	60		
AMEXCLUD	AM	TRANS	Reserved Level of IBM use only. Shape Identifies Transmission Lines Fill Exclusion	DRC/Data prep
	53	18		
AMPIN ²	AM	pin	Shape = Used to define ports of a device or cell. Also, used for transmission line verification.	LVS/ DRC
	53	32		
AVESD_FINGER	AV	esdf	Placed over AV or AVBAR to enable AV area summing.	ESD Rules/ DRC
	130	62		
BFMOAT	BFMOAT	dg	Used to block P-well and N-well implants from BFMOAT regions to create regions of high resistive path.	BFMOAT device
	5	5		
BFMOATIND	BFMOAT	ind	Used to identify the M1 ground plane inductor.	DRC
	5	4		
BONDPAD	PAD	DEV	Shape identifies Wirebond and C-4 pads which are treated as devices and modeled.	DRC/ Modeling
	41	25		
BPHOLE	BP	HOLE	Shape = Areas which abates generation of BP from BB.	Data prep / DRC
	10	100		
BPERI	OUTLINE	BPERI	Shape identifies NPN Bipolar transistors and Collector-Pwell Varactors.	DRC/ Modeling
	60	1		
C4LV	C4	dg	Shape identifies LV shapes which are C-4s and not octagonal wirebond pads. Any LV not under C4LV defaults to being checked to wirebond rules.	DRC/ Data prep
	41	0		

Table 2-4. Dummy Design Levels and Utility Levels

Design Level	CDS name	CDS purpose	Description	Associ- ated With
	GDSII number	GDSII type		
CAESD_FINGER	CA	esdf	Placed over CA to enable CA area summing.	ESD Rules/ DRC
	14	62		
CHIPEDGE	CHIP- EDGE	dg	<p>A shape on the dummy design level, CHIPEDGE, must encompass all active chip design shapes including the chip substrate ring. see section 3.30 , “Chip Guard Ring and Chamfer” on page 203</p> <p>It is used for merging kerf data. It also defines a buffer zone on the outside edge the chip guardring for the edge seal. See rules 658c and 658d in Table 3-11, rules 906 and 906b in Table 3-56, rules 944b and 945b in Table 3-57 on page 199, rules 999, 999a and 999b” in Table 3-59 on page 205.</p> <p>These rules assume dicing being done by IBM. If this is done elsewhere, these rules must be defined by the appropriate dicing organization.</p> <p>For information on square or rectangular (non-beveled) CHIPEDGE use restrictions, per Rule PT999s3 listed in Table 3-60, see Note in Section 3.31 , “Protect Layer” on page 208.</p>	chip sub- strate ring chamfer kerf
	62	1		
DCAP	PC	CAP	Shape identifies certain decoupling capacitor structures.	LVS
	7	15		
DEGEN	DEGEN	dg	Shape = Areas which are copied to the DE mask. For use only in the VPNP device. If the VPNP device is used the DE mask is required to be built.	Data prep / DRC
	212	24		
DI	DI	dg	Placed over p-type junctions used under forward-bias in bandgap reference circuits. Used for verification -- both design rule checking and layout vs schematic.	Forward biased- diodes
	29	0		
DIODE	DIODE	DG	Shape to identify the diodes that should be recognized as devices rather than parasitics.	DRC/ Modeling
	62	4		
DTMESH	DT	FILTRGR1	Shape identifies DT_LATTICES with up to 10 μ m pitch.	DRC
	1	18		

Table 2-4. Dummy Design Levels and Utility Levels

Design Level	CDS name	CDS purpose	Description	Associated With
	GDSII number	GDSII type		
EDGE LAYER	edgeLayer	dg	Shape assists in the identification of device dimensions.	LVS
	2	19		
EFUSE	OUTLINE	efuse	Electrical fuse marking layer used for BH generation.	Dataprep
	12	98		
ESD_CDM	ESD	cdm	Special level that is placed over ESD HBM structures	ESD rules
	12	88		
ESDIODE	ESDIODE	dg	Special level that is placed over CMOS compatible ESD diodes.	ESD rules
	62	71		
ESDUMMY	ESDUMMY	dg	Special level that is placed over the ESD pad structure.	ESD rules
	63	36		
ESDUMMY_DEV	ESDUMMY	DEV	Shape identifies NW ESD Diode devices and are modeling and DRC checked to additional rules.	DRC/ Modeling
	63	35		
GRLOGIC	GR- LOGIC	dg	Shape identifies structures that are exempt from recommended or more stringent layout rule verification. Intended for use in IBM Digital Library offerings. See Rule 110a, 110aR, 269a, 385a, 715a, 717a, 717a1, 735b, 737aR, OP30, OP31, PBR29, PBR33, DG110a.	DRC
	6	34		
GUARDRNG	OUTLINE	guardrng	Marking layer for the chip guard ring.	DRC
	12	71		
INJECTOR_CDE	INJECTOR	cde	Special level placed over I/O structures connected to a pad and used for checking	External Latchup rules to meet CDE/HM M requirements
	12	84		

Table 2-4. Dummy Design Levels and Utility Levels

Design Level	CDS name	CDS purpose	Description	Associ- ated With
	GDSII number	GDSII type		
INJECTOR_ JEDEC	INJECTOR	jedec	Special level placed over I/O structures con- nected to a pad and used for checking	External Latchup rules to meet JEDEC require- ments
	12	85		
IODUMMY	IODUMMY	dg	IBM Reserved level (do not use). Obsolete level name formerly used over signal pads which require ESD and latchup Rule check- ing.	ESD and Latchup rules
	63	37		
IND_FILT	OUTLINE	IND	Shape identifies INDUCTOR AM shapes and are modeled and DRC checked to additional rules.	DRC/ Modeling
	60	4		
LOGOBND	LOGOBND	dg	Placed over Product Labels to assist in DRC verification. See section 3.33 , “Product Labels” on page 213	Labels
	62	5		
LOWCRNT	OUTLINE	LOWCRNT	Shape identifies AV or AVBAR vias which only use 20% or less of the rated current. See section 5.4 , “Back End Of Line (BEOL) Reliability Design Rules” on page 358 for current ratings and Rule AM1a.	Labels
	60	28		
LVDUMMY	LVDUMMY	dg	Shape used to specify area for C4 ball place- ment but not open to LV etch. When C4 ter- minal connections are used (not wirebond), dummy terminals provide additional mechan- ical support. See section 3.28.1.2 , “Dummy C4 Terminals” on page 198.	C4
	28	1		
LVSPAD	PAD	pad	Shape identifies difference between wireb- ond and C4 pad.	LVS
	41	27		
LYESD ¹	LY	esd	Shape = Label that is used to identify pads used for ESD and Latchup Rule checking	DRC
	42	60		
LYESD_ FINGER	LY	esdf	Placed over fingered metal to enable width summing.	ESD Rules/ DRC
	123	62		
LYEXCLUD	LY	TRANS	Reserved Level of IBM use only. Shape Iden- tifies Transmission Lines Fill Exclusion	DRC/Data prep
	42	18		

Table 2-4. Dummy Design Levels and Utility Levels

Design Level	CDS name	CDS purpose	Description	Associ- ated With
	GDSII number	GDSII type		
LYPIN ²	LY	pin	Shape = Used to define ports of a device or cell. Also, used for transmission line verification.	LVS/ DRC
	42	32		
MULTI_CAP	MULTI	CAP	Shape identifies multiplicity for MIMs and devices under MIMs.	LVS
	60	27		
MULTI_RES	MULTI	RES	Shape identifies multiplicity for BEOL (KQ) resistors.	LVS
	212	19		
MULTI	MULTI	DEV	Shape identifies multiple devices which represent a single schematic symbol with a value greater than one	LVS
	60	25		
MxESD	Mx	esd	Shape = Label that is used to identify pads used for ESD and Latchup Rule checking.	DRC
(x=1)	15	60		
(x=2)	17	60		
(x=3)	19	60		
(x=4)	21	60		
(x=Q)	34	60		
MxESD_FINGER	Mx	esdf	Shape = Label that is used to identify pads used for ESD and Latchup Rule checking.	ESD Rules/ DRC
(x=1)	15	62		
(x=2)	17	62		
(x=3)	19	62		
(x=4)	21	62		
(x=Q)	34	62		
MxTRANS	Mx	TRANS	Reserved Level of IBM use only. Shape Identifies Transmission Lines. These levels are presently included in the technology, but are NOT used during the IBM Release process. These shapes do not affect normal IBM auto-generated MxFILL in the transmission line device structures.	DRC/Data prep
(x=1)	15	18		
(x=2)	17	18		
(x=3)	19	18		
(x=4)	21	18		
(x=Q)	34	18		

Table 2-4. Dummy Design Levels and Utility Levels

Design Level	CDS name	CDS purpose	Description	Associ- ated With
	GDSII number	GDSII type		
MxPLANE, (x=1)	Mx	PLANE	Shape identifies Mx wires that are wider than Rule 500b (for M1) or 600b (for M2,M3,M4) or 690b (for MQ)	DRC/Data prep
(x=2)	15	19		
(x=3)	17	19		
(x=4)	19	19		
(x=Q)	21	19		
	34	19		
NOPLYMD	NOPLYMD	dg	Shape identifies designs which use the no final polyimide chip passivation, see section 3.34 , “No Polyimide Final Passivation option” on page 217.	DRC / Technol- ogy Fea- tures
	212	136		
NSR	NS	RES1	Shape identifies NS Resistors	DRC/ Modeling
	0	10		
NWASP	NWASP	dg	Placed over NW shapes to denote Nwells at the same potential. Used to denote relaxed NW to NW space rules for groundrule checking for this situation.	Nwells at same potential
	4	3		
OUTLINE ³	OUTLINE	dg	Defines edge of IBM cells.	-
	62	21		
PCEXCLUD ⁴	PC	exclude	Placed over specific areas of the chip that can not receive PCFILL shapes, such as ESD/IO circuits.	PCFILL exclusion.
	7	2		
PROTECT	PROTECT	dg	Used during the CP mask assembly auto- matic KERF merge process associated with preventing mask background overwrite. Tri- angular shape added to the four corners of the chip data on this level.	KERF design and mask merge
	102	18		
RXEXCLUD ⁴	RX	exclude	Placed over specific areas of the chip that can not receive RXFILL shapes, such as ESD/IO circuits, or N-Well resistors.	RXFILL exclusion.
	2	2		
SBLK ⁵	SBLK	dg	Shape identifies ballasted FETs. SBLK is to be drawn over RX shapes.	DRC/Mod eling
	12	48		
TLINE	AM	IND	Shape identifies AM shapes which are to be modeled as indlines.	DRC/ Modeling
	53	4		

Table 2-4. Dummy Design Levels and Utility Levels

Design Level	CDS name	CDS purpose	Description	Associ- ated With
	GDSII number	GDSII type		
TRANSMIS	OUTLINE	TRANS	Shape identifies structures which are to be modeled as transmission lines.	DRC/ Modeling
	60	18		
VAR ⁶	VAR	dg	Placed over PCDCAP ("Nfet-in-nwell") structures to avoid extension or halo implants.	Decou- pling capacitors / varactors
	12	24		
VTSENS	VTSENS	dg	Placed over (PC intersect RX). (PC intersect RX) must be completely within VTSENS	Vt sensi- tivity checking.
	12	52		
VxESD_FINGER	Vx	esdf	Placed over Vx ⁷ to enable Vx area summing.	ESD Rules/ DRC
(x=1)	16	62		
(x=2)	18	62		
(x=3)	20	62		
(x=L)	35	62		
(x=Y)	129	62	Placed over VY or VYBAR to enable VY and VYBAR area summing.	

1. The levels are for labels only. For additional information, see section 3.11.5 , "Net Definitions for ESD Checking and Latchup Verification" on page 151
2. For additional information, see Table , " , " on page 191.
3. OUTLINE [OUTLIN dg] is also used for IBM testsite macro outline definition.
4. For information on usage of REXCLUDE and PCXCLUDE shapes, see section 2.9 , "Important Design Guidelines" on page 59, and see section 2.10 , "Pattern Density Rules" on page 62
5. Use of SBLK shapes are for ESD purposes only. See Rules 736a, 736a1, 736a2, 736a3 and PBR19 Table 3-38, "OP Resistor Layout Rules," on page 158.
6. For additional information, see See section 3.21 , "nFET-in-Nwell (VAR) Device Layout Rules" on page 173. .
7. VxBAR (x = 1,2,3,L) are not included since VxBAR as not supported except in the Chip Guard Ring.

2.4 Masks for Non-Design Levels

The following mask levels are generated during mask build and can not be drawn by the designer.

Table 2-5. Masks for Non-Design Levels¹

Mask Level	CDS name	CDS purpose	Description
	GDSII number	GDSII type	
BT	BT	dg	Shape = blocks deep implant in both Nwell and Pwell regions of a chip design. Regions of the chip design blocked from deep implant are identified by Design or Dummy Design Levels {BFMOAT, BB, (ESDIODE sized by +0.1 μ m per edge) or Mask Levels {(PI sized by +1.1 μ m per edge), JD}
	12	55	
DW	DW	dg	Shape = thick oxide gate device well implant area. Use is OPTIONAL ²
	48	0	
BF	BF	dg	Shape = complement of the P-well implant.
	5	0	
BH	BH	dg	Shape = complement of the nFET halo implant. Determines the nFET halo/extension implant area.
	12	5	
DY	DY	dg	Shape = derived level from the DT design level. Used to aid in planarization.
	212	81	
DF	DF	dg	Shape = 5.2nm oxide pFET halo/LDD implant. Use is OPTIONAL ²
	12	12	
DE	DE	dg	Shape = 5.2nm oxide nFET halo/LDD implant. Use is OPTIONAL ²
	12	7	
PH	PH	dg	Shape = pFET extension/halo implant area.
	9	0	
PF	PF	dg	Shape = opens window in resist over NPN for device formation.
	212	82	
PQ	PQ	dg	Shape = resist island over NPN to inhibit processing.
	212	62	
BN ³	BN	dg	Shape = P ⁺ source/drain implant area.
	11	0	

Table 2-5. Masks for Non-Design Levels¹

Mask Level	CDS name	CDS purpose	Description
	GDSII number	GDSII type	
VI	VI	dg	Shape = P ⁺ implant area for HA Varactor. Use is OPTIONAL ²
	12	120	
PY	PY	dg	Shape = copy of LY wiring level used for planarization.
	153	0	
TM	TM	dg	Shape = area for plated terminal metal (C4 Plating)
	49	0	

1. Some Design Levels also receive manipulation during mask data preparation (DPREP). See section 2.5 , “Level Generation and Design Preparation” on page 44.

2. For more information on optional Masks for Non-Design Levels, see Table 1-1, “Optional Features with Feature Part Numbers,” on page 12 and Table 2-6, “Shape Manipulation Prior to Mask Write,” on page 44.

3. BN generations use BP shapes as designed and not the BP as generated in mask data preparation (DPREP).

2.5 Level Generation and Design Preparation

Table 2-6. Shape Manipulation Prior to Mask Write

Mask Level	Description of Design Preparation From Design Levels
BT	BT = Union [BFMOAT, BB, (PI sized by +1.1um per edge), JD, IBLK, (ESDIODE sized by +0.1um per edge)] Remove gaps ≤ 0.98 Remove slivers ≤ 0.98

Table 2-6. Shape Manipulation Prior to Mask Write

Mask Level	Description of Design Preparation From Design Levels
DY	DY = Union [DDY15, DDY25] where: DDY11 = DT sized by 1.0μm DDY12 = DDY11 sized by -1.52μm DDY13 = DDY12 sized by 0.52μm DDY15 = DDY13 not touching RX DDY16 = DT sized by 0.18μm DDY17 = RX sized by 0.12μm DDY20 = Difference [DDY16, DDY17] DDY21 = DDY20 sized by 0.52μm DDY25 = DDY21 sized by -0.52μm
DW	DW = Difference [DG, NW]
BF	BF = Union [DERIVEDBF, BFMOAT, DBF1] where: DERIVEDBF= NW DBF1= Union [PI, JD, BB] Remove gaps ≤ 0.62 Remove slivers ≤ 0.28
BP	BP = Union [BP, (BB - BPHOLE)]
BH	BH = DBH50, where: DBH10 = { difference [intersection (OP, PC), (RX sized by +0.20)] sized by +0.12 } DBH25 = { [PC(touching OP, over RR)] sized by +0.12 } DBH40 = union { DG, NW, VAR, JD, DBH10, DBH25, BB, EFUSE } DBH50 = Remove slivers ≤ 0.38 for DBH40
DE	DE = Union(Difference [DG, Union(NW, XE)], DEGEN, (ZEROVT ¹ SIZED BY +0.52))
DF	DF = Difference { intersection [DG, NW], Union(VAR, XF) }
EH	EH=OZ ²

Table 2-6. Shape Manipulation Prior to Mask Write

Mask Level	Description of Design Preparation From Design Levels
BN	<p>BN = Union ((DERIVEDBN not touching (PD or JD)), DBN1, DBN2³)</p> <p>where</p> <p>DERIVEDBN = BP</p> <p>DBN1 = PD</p> <p>DBN2 = BI³</p> <p>BN gaps are filled where the spacing is ≤ 0.34, the run length is ≥ 5.00, the net union of the BN space to be filled is not touching RX or PC, and the space to be filled is ≥ 0.12 from any RX or PC shape.</p>
PH	<p>PH = DPH2 where:</p> <p>DPH1 = { difference [intersection (OP, PC), (RX sized by +0.20)] sized by +0.12 }</p> <p>Slivers ≤ 0.38 are removed after DPH1 derivation</p> <p>DPH2 = difference {NW, union (DG, VAR, JD, RP⁴, DPH1)}</p>
PF	<p>PF = DPF22 where:</p> <p>DPF10 = union [JD, SB⁵]</p> <p>DPF11 = difference [RN, DPF10]</p> <p>DPF12 = union [DPF11, PB]</p> <p>DPF13 = (DPF12 sized by +0.20)</p> <p>DPF15 = (DPF13 with gap fill for spaces ≤ 1.0)</p> <p>DPF16 = union [PB, RN]</p> <p>DPF17 = difference [RX, DPF16]</p> <p>DPF18 = (DPF17 sized by +0.15)</p> <p>DPF20 = difference [DPF15, DPF18]</p> <p>DPF21 = OZ sized by +0.80</p> <p>DPF22 = union(DPF20, DPF21)</p>

Table 2-6. Shape Manipulation Prior to Mask Write

Mask Level	Description of Design Preparation From Design Levels
PQ	<p>PQ = DPQ22 where:</p> <p>DPQ10 = union [JD, SB ⁵]</p> <p>DPQ11 = difference [RN, DPQ10]</p> <p>DPQ12 = union [DPQ11, PB]</p> <p>DPQ13 = (DPQ12 sized by +0.02)</p> <p>DPQ15 = (DPQ13 with gap fill for spaces ≤ 1.52)</p> <p>DPQ16 = union [PB, RN]</p> <p>DPQ17 = difference [RX, DPQ16]</p> <p>DPQ18 = (DPQ17 sized by +0.33)</p> <p>DPQ20 = difference [DPQ15, DPQ18]</p> <p>DPQ21 = OZ sized by +0.50</p> <p>DPQ22= union(DPQ20, DPQ21)</p>
OV	OV = SV sized by 1.5
VI	VI= intersection [BP,JD]
PY	PY = LY (PYFILL= LYFILL)
M1 ⁶	Data preparation for OPC, anchors, etc. Consult your IBM Technical Representative for more detail.
M2 ⁶	
M3 ⁶	
M4 ⁶	
MQ ⁶	Data preparation for anchors, etc. Consult your IBM Technical Representative for more detail.
V1 ⁶	Data preparation for VxHOLE. Consult your IBM Technical Representative for more detail.
V2 ⁶	
V3 ⁶	
VL ⁶	
LY ⁶	For IBM KERF LYFILL Generation
AM ⁶	For IBM KERF AMFILL Generation
PC	Consult your IBM Technical Representative for more details.
RX	Consult your IBM Technical Representative for more detail.

Table 2-6. Shape Manipulation Prior to Mask Write

Mask Level	Description of Design Preparation From Design Levels
LV	Terminal octagons of correct dimensions are converted to circles, all other LV shapes are passed through to the generated layer and not modified. (LV over C4LV) octagons converted to circles. Size LV circle by +0.00 μm . See section 3.28.1 , “C4 Terminals” on page 194.
T3	$T3^7 = \text{VPNP}$
TM ⁸	Generated from ((LV over C4LV), LVDUMMY) (C4 Plating)

1. ZEROVT is not coded in this Boolean. ZEROVT is listed for reference only, for shared internal IBM dataprep keyword usage. ZEROVT design level is not included in the techfile or map files within the design kit.
2. Propagated from OZ.
3. DBN2 in the description of Design Preparation boolean equation is restricted design level BI. Design Level BI is not supported in this technology per Rule RL08 in Table 2-14, “Reserved Level Layout Rules” on page 58. BI is documented in the dataprep description for IBM data preparation common keyword use.
4. RP is a restricted design level per Table 2-2, “Design Services and Data Preparation Mask Levels (Restricted)” on page 30. RP is documented in the dataprep description for IBM data preparation common keyword use. RP is not verified during Design Rule verification.
5. DPF10 in the description of PF Design Preparation boolean equation, and DPQ10 in the description of PQ Design Preparation boolean equation include restricted design level SB. Design Level SB is not supported in this technology per Rule RL08 in Table 2-14, “Reserved Level Layout Rules” on page 58. SB is documented in these two dataprep boolean equation descriptions for IBM data preparation common keyword use.
6. These keywords are listed to ensure inclusion of MxFILL (where x = 1,2,3,4,Q), LYFILL and AMFILL in the KERF electrical macros. These levels are not required in DRC.
7. Via Mask Comp Spec.
8. Riston Cu plating mask process.

2.6 Mask Metallization Options

The BiCMOS8HP metallization options are listed in Table 2-7.

<i>Table 2-7.Back End Of Line (BEOL) Metallization Options</i>							
Levels Of Metal	Type Of Metallization			Optional BEOL Resistor	Required Mask Levels (except KQ is optional)	Final ^{1, 2} Passivation	
	Thin Copper	Thick Copper	Thick Alum			Wire-bond	C4
7LM	4	1	2	KQ	M1, V1, M2, V2, M3, V3, M4, VL, MQ, (KQ), VY, LY ³ , PY, AV, AM	DV	LV
6LM	3	1	2	KQ	M1, V1, M2, V2, M3, VL, MQ, (KQ), VY, LY ³ , PY, AV, AM		
5LM	2	1	2	KQ	M1, V1, M2, VL, MQ, (KQ), VY, LY ³ , PY, AV, AM		

1. For Wirebond Final Passivation, see section 3.28.2 , “Wirebond” on page 198

2. For C4 Final Passivation, see section 3.28.1 , “C4 Terminals” on page 194

3. If optional MIM is present, mask level QY is located above LY.

2.7 Design Truth Tables

The Design Truth Table is provided as an aid to the layout of various structures. In this table a “0” indicates that design level must not touch the structure. A “1” indicates that design level must cover or match the structure. “X” means “don’t care;” there is no electrical effect of this mask on this feature. “P” means the structure must be partial covered by the shape. “G” indicates that the shape is generated. “B” is Boolean switch where the feature can be turned on and off depending on desired electrical characteristics.

The structures in this table are the only structures permitted in this technology. Use of any other structure requires prior approval in writing from the IBM Technical Representative.

In addition to the levels in the Truth Table the Identification level PD is required on the PC RR poly resistor. IND_FILT is required on AM Inductors.

Table 2-8. Design Truth Table																									
STRUCTURE	Design Levels																								
	N S	D S	D T	R X	R N	P I	J D	N W	B B	P X	D G	P C	B X	C X	L E	E X	N P	P B	B P	R R	P D	O P	C A	C E	
NPN-E (HP)	1	0	P	1	0	0	0	0	1	1	0	0	1	1	1	1	1	1	G	0	0	0	0	1	

STRUCTURE	Design Levels																								
	N S	D S	D T	R X	R N	P I	J D	N W	B B	P X	D G	P C	B X	C X	L E	E X	N P	P B	B P	R R	P D	O P	C A	C E	
NPN-E (HB)	0	1	P	1	0	0	0	0	1	1	0	0	1	0	1	1	1	1	G	0	0	0	0	1	
NPN-B (HP)	1	0	P	0	0	0	0	0	1	1	0	0	0	0	0	0	0	1	G	0	0	0	1	0	
NPN-B (HB)	0	1	P	0	0	0	0	0	1	1	0	0	0	0	0	0	0	1	G	0	0	0	1	0	
NPN-C (HP)	1	0	P	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	G	0	0	0	1	0	
NPN-C (HB)	0	1	P	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	G	0	0	0	1	0	
Regular NFET	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0	
Regular PFET	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	0	0	0	1	0	0	0	1	0	
Thick NFET25	0	0	0	1	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	1	0	
Thick PFET25	0	0	0	1	0	0	0	1	0	0	1	1	0	0	0	0	0	0	1	0	0	0	1	0	
Triple Well Thin NFET (active device)	0	0	0	1	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0	
Triple Well Thick NFET (active device)	0	0	0	1	0	1	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	1	0	
Triple Well Iso-lation	0	0	0	x	0	1	0	1	0	0	x	x	0	0	0	0	0	0	x	x	x	x	1	0	
Triple Well Con-tact	0	0	0	1	0	1	0	0	0	0	x	0	0	0	0	0	0	0	1	0	0	0	1	0	
N-well Contact	0	0	0	1	0	0	0	1	0	0	x	0	0	0	0	0	0	0	0	0	0	0	1	0	
N ⁺ Junction	0	0	0	1	0	0	0	0	0	0	x	0	0	0	0	0	0	0	0	0	0	0	0	0	
Substrate Con-tact	0	0	0	1	0	0	0	0	0	0	x	0	0	0	0	0	0	0	1	0	0	0	1	0	
P ⁺ Junction ¹	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	
OP P+ poly resistor ²	x	0	x	0	0	x	0	x	x	0	0	1	0	0	0	0	0	0	x	0	x	1	1	0	
OP RR PC poly resistor ³	x	0	x	0	0	0	0	x	x	0	0	1	0	0	0	0	0	0	x	1	1	1	1	0	
NS resistor	1	0	P	P	P	0	0	0	1	0	x	x	0	0	0	0	0	0	G	0	0	x	1	0	
KQ BEOL resis-tor	x	x	x	x	x	x	x	x	x	x	x	x	0	0	0	0	0	0	x	0	x	x	0	0	
HA Varactor	0	0	P	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	
PCDCAP Thin Oxide/ Varactor Thin Oxide	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0	
PCDCAP Thick Oxide/Varactor Thick Oxide	0	0	0	1	0	0	0	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	1	0	

STRUCTURE	Design Levels																								
	N S	D S	D T	R X	R N	P I	J D	N W	B B	P X	D G	P C	B X	C X	L E	E X	N P	P B	B P	R R	P D	O P	C A	C E	
MIM ⁴	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Inductor	0	0	x	x ⁵	0	0	0	0	1	0	0	x ⁶	0	0	0	0	0	0	G	0	0	0	0	0	0
Bondpad	x	0	x	x ⁵	0	0	0	0	1	x	0	0	0	0	0	0	0	0	G	0	0	0	0	0	0
rfline (AM, BB, DT)	0	0	1	0	0	0	0	0	1	x	0	0	0	0	0	0	0	0	G	0	0	0	0	0	0
Transmission Line and Distributed Passives	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Diode P+/NW (no NS, no DT)	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0
Diode P+/NW (NS)	1	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0
Diode P+/NW (DT)	0	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0
Diode P+/NW (NS, DT)	1	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0
Diode N+/SX	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0
Diode NW/SX (no NS, no DT)	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0
Diode NW/SX (NS, no DT)	1	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0
Diode NW/SX (no NS, DT)	0	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0
Diode NW/SX (NS, DT)	1	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0
Electronic Fuse ⁷	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	1	0	0

1. Forward-biased junctions employed in bandgap reference circuits require an additional design level (DI) for model extraction and design rule checking. See Table 3-37, "DI Layout Rules," on page 155.
2. There are multiple layouts of this device. When BB is not present, BP is used. When BB is present, then PD is used and BP is generated during Data Preparation, and drawn BP is not present (see Rule BB35), Resistor NS backplates must be within BB. For NW backplates, BB use is restricted per Rule BB34a (use BP instead).
3. There are multiple layouts of this device. PD is always present. When BB is not present, BP is used. When BB is present, then BP is generated during Data Preparation, and drawn BP is not present (see Rule BB35), Resistor NS backplates must be within BB. For NW backplates, BB use is restricted per Rule BB34a (use BP instead).
4. There are multiple layout options for this device. When BB is not present, BP is used. When BB is present, then BP is generated during Data Preparation, and drawn BP is not present (see Rule BB35), The NS backplates must be within BB.
5. x is used as RX Fill and PC Fill will be automatically generated during Design Preparation.
6. x is used as PC not touching (CA, CABAR) is allowed per Rule IND11 and PC Fill will be automatically generated during Design Preparation.

7. Requires Design Level PCFUSE.

Table 2-9. Design Truth Table for Non-Design Mask Levels and Dummy Design Levels

STRUCTURE Derived Levels (Generated)														
	D Y	B T	D W	B F	B H	D F	D E	P H	P F	P Q	B N	B P	V I	P Y
NPN-C	x	1	0	1	1	0	0	0	1	1	0	1	0	x
NPN-B	x	1	0	1	1	0	0	0	1	1	0	1	0	x
NPN-E (HP)	x	1	0	1	1	0	0	0	1	1	0	1	0	x
NPN-E (HB)	x	1	0	1	1	0	0	0	1	1	0	1	0	x
Regular NFET	x	0	0	0	0	0	0	0	1	1	0	0	0	x
Regular PFET	x	0	0	1	1	0	0	1	0	0	1	1	0	x
Thick NFET25	x	0	1	0	1	0	1	0	0	0	0	0	0	x
Thick PFET25	x	0	0	1	1	1	0 ¹	0 ¹	0	0	1	1	0	x
Triple Well NFET	x	1	0	1	0	0	0	0	0	0	0	0	0	x
Triple Well Thick NFET	x	1	1	1	1	0	1	0	0	0	0	0	0	x
Triple Well Isolation	x	1	x	1	P ²	0	x	P	0	0	x	0	0	x
Triple Well Contact	x	1	0	1	0	0	0	0	0	0	1	1	0	x
N-well Contact	x	0	0	1	1	x	0	x	0	0	0	0	0	x
Silicided N ⁺ Junction	x	0	0	0	x	0	x	0	0	0	0	0	0	x
Substrate Contact	x	0	0	0	x	0	x	0	0	0	1	1	0	x
Silicided P ⁺ Junction ³	x	0	0	1	1	x	0	x	0	0	1	1	0	x
OP P+ poly resistor (without BB)	x	0	0	x	1	0	0	0	0	0	1	1	0	x
PC P+ poly resistor (with BB)	x	1	0	1	1	0	0	0	0	0	1	1	0	x

Table 2-9. Design Truth Table for Non-Design Mask Levels and Dummy Design Levels

STRUCTURE Derived Levels (Generated)														
	D Y	B T	D W	B F	B H	D F	D E	P H	P F	P Q	B N	B P	V I	P Y
OP RR PC poly resistor (without BB)	x	0	0	x	1	0	0	0	0	0	1	1	0	x
OP RR PC poly resistor (with BB)	x	1	0	1	1	0	0	0	0	0	1	1	0	x
NS resistor	x	1	x	1	1	x	x	0	1	1	0	1	0	x
KQ BEOL resistor	x	x	x	x	x	x	x	x	x	x	x	x	x	x
HA Varactor	x	1	0	1	1	0	0	0	0	0	0	1	1	x
PCDCAP Thin Oxide/ Varactor Thin Oxide	x	0	0	1	1	0	0	0	0	0	0	0	0	x
PCDCAP Thick Oxide/Varac- tor Thick Oxide	x	0	0	1	1	0	0	0	0	0	0	0	0	x
MIM	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Inductor	x	1	0	1	1	0	0	0	0	0	0	1	0	x
Bondpad	x	1	0	1	1	0	0	0	0	0	0	1	0	x
rfline (AM, BB, DT)	x	1	x	1	1	0	0	0	0	0	0	1	0	x
Transmis- sion Line and Distributed Passives	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Diode P+/NW (all 4 vari- ants)	x	0	0	1	1	0	0	1	0	0	1	1	0	x
Diode N+/SX	x	0	0	0	0	0	0	0	0	0	1	1	0	x
Diode NW/SX (all 4 vari- ants)	x	0	0	1	1	0	0	1	0	0	1	1	0	x
Electronic Fuse	x	0	0	0	1	0	0	0	0	0	1	1	0	x

1. DE may be formed by dataprep outside the active device, where DE shapes = ((DG overlap past NW) not over BP). PH may be formed by dataprep outside the active device, where PH shapes = NW(not over DG)

2. BH is generated for the NW isolation ring, but not under the active device.
3. Forward-biased junctions employed in bandgap reference circuits require an additional design level (DI) for model extraction and design rule checking. See Table 3-37, "DI Layout Rules," on page 155.

Table 2-10. Design Truth Table for Dummy Design and Utility Levels

STRUCTURE	Dummy Design and Utility Levels											
	V A R	B P R E I	N S R	D I O D E	I N D - F I L T	B O N D P A D	T L I N E	T R A N S M I S	x T R A N S	E S D U M M Y	P C F U S E	E F U S E
NPN-C	0	1	0	0	0	0	0	x	x	0	0	0
NPN-B	0	1	0	0	0	0	0	x	x	0	0	0
NPN-E (HP)	0	1	0	0	0	0	0	x	x	0	0	0
NPN-E (HB)	0	1	0	0	0	0	0	x	x	0	0	0
Regular NFET	0	0	0	0	0	0	0	x	x	0	0	0
Regular PFET	0	0	0	0	0	0	0	x	x	0	0	0
Thick NFET25	0	0	0	0	0	0	0	x	x	0	0	0
Thick PFET25	0	0	0	0	0	0	0	x	x	0	0	0
Triple Well NFET	0	0	0	0	0	0	0	x	x	0	0	0
Triple Well Thick NFET	0	0	0	0	0	0	0	x	x	0	0	0
Triple Well Isolation	0	0	0	0	0	x	0	x	x	0	0	0
Triple Well Contact	0	0	0	0	0	0	0	x	x	0	0	0
N-well Contact	0	0	0	0	0	0	0	x	x	x	0	0
Silicided N ⁺ Junction	0	0	0	0	0	0	0	x	x	x	0	0
Substrate Contact	0	0	0	0	0	0	0	x	x	x	0	0
Silicided P ⁺ Junction ¹	0	0	0	0	0	0	0	x	x	x	0	0
OP P+ poly resistor	0	0	0	0	0	0	0	x	x	x	0	0
OP RR PC poly resistor	0	0	0	0	0	0	0	x	x	x	0	0
NS resistor	0	0	1	0	0	0	0	x	x	0	0	0
KQ BEOL resistor	x	x	x	x	0	0	0	0	x ²	x	x	x
HA Varactor	0	0	0	0	0	0	0	x	x	0	0	0

Table 2-10. Design Truth Table for Dummy Design and Utility Levels

STRUCTURE	Dummy Design and Utility Levels											
	V A R	B P R E I	N S R	D I O D E	I N D F I L T	B O N D P A D	T L I N E	T R A N S M I S	x x T R A N S	E S D U M M Y	P C F U S E	E F U S E
PCDCAP Thin Oxide/ Varactor Thin Oxide	1	0	0	0	0	0	0	x	x	0	0	0
PCDCAP Thick Oxide/Varactor Thick Oxide	1	0	0	0	0	0	0	x	x	0	0	0
MIM	x	x	x	x	0	0	0	x	x ³	x	x	x
Inductor	0	0	0	0	1	0	x	0	0	0	0	0
Bondpad	0	0	0	0	0	1	0	0	0	0	0	0
rfline (AM, BB, DT)	0	0	0	0	0	0	1	0	0	0	0	0
Transmission Line and Distributed Passives	x	x	x	x	0	0	0	1	x	x	x	x
Diode P+/NW (all 4 variants)	0	0	0	0	0	0	0	x	x	1	0	0
Diode N+/SX	0	0	0	0	0	0	0	x	x	1	0	0
Diode NW/SX (all 4 variants)	0	0	0	0	0	0	0	x	x	1	0	0
Electronic Fuse	0	0	0	0	0	0	0	x	x	x	1	1

- Forward-biased junctions employed in bandgap reference circuits require an additional design level (DI) for model extraction and design rule checking. See Table 3-37, "DI Layout Rules," on page 155.
- MQTRANS touching KQ is not recommended.
- LYTRANS touching QY is not recommended.

STRUCTURE	Design Levels																											
	N S	D S	D T	R X	R N	P I	J D	N W	B B	P X	D G	P C	B X	O Z	E V	C X	L E	E X	N P	P B	B P	R R	P D	O P	C A	C E	C A B A R	
PNP-Emitter	0	0	0	1	0	0	0	0	1	0	0	0	0	1	1	0	0	0	0	1	G	0	0	0	0	0	0	P
PNP-Base	0	0	0	1	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	P	0	0
PNP-Collector	0	0	0	1	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0	0	G	0	1	0	0	0	0	P
PNP-Isolation Contact	0	0	0	1	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	P	0	0

1. Structures: MIM, Transmission Line, and Distributed Passives; have truth table value = “x” (don’t care) for Design Levels OZ + EV. All other structures have table value = “0” (must not touch), associated with Design Levels OZ + EV.

Table 2-12. VPNP Design Truth Table for Non-Design Mask Levels and Dummy Design Levels															
STRUCTURE Derived Levels (Generated)															
	D Y	T 3	B T	D W	B F	B H	D F	D E	P H	P F	P Q	B N	B P	V I	P Y
PNP-Emitter	x	1	1	0	1	1	0	0	0	1	1	0	1	0	x
PNP-Base	x	1	1	0	1	1	0	1	0	1	1	0	0	0	x
PNP-Collector	x	1	1	0	1	1	0	0	0	1	1	1	1	0	x
PNP-Isolation Contact	x	1	1	0	1	1	0	0	1	1	0	0	0	0	x

2.8 Design Geometry Restrictions

Column named: “Class”, adjacent to “Rule column”, specifies Manufacturability Rule Classification with respect to DRC violations;

- a. = Automatic Reject (severity1),
 - Possible impact to either: production tools or processes
 - Possible impact to either: IBM Kerf and/or WAC
 - Possible impact to mask build
 - Possible impact to other rider (multi-client MPW)
- b. = Significant Yield / Reliability Impact (severity2),
- c. = Moderate Yield / Reliability Impact (severity3),
- d. = Yield Enhancement (recommend compliance) (severity4).

The following layout ground rules are present in the design rule checking deck.

<i>Table 2-13. Geometry Restrictions</i>			
Rule	Class	Notes	Description
S1	a	-	The design grid must be an integer multiple of 0.01 μm .
S2	a	1	Shapes with acute angles are not allowed.
S3	a	-	Shapes that intersect and overlap themselves are not allowed (shapes that abut themselves are acceptable).
S4	a	-	Shapes that cross over themselves are not allowed (also known as bow ties and re-entrant shapes).
S5	a	-	Shapes with zero area are not allowed.
S6	a	-	Only shapes that are orthogonal or on a 45° angle are allowed except in alphanumeric labels.
S7	a	-	Shapes that are formed with two lines that never intersect are not allowed (also known as inside-outside shapes).
S8	a	-	Shapes that are formed with the line op code or path codes are not allowed to have 45 bends.
S9	a	-	Line end segments formed with line op codes or path op codes must have a length to width ratio > 0.50.
S10	a	-	Text data (Alpha op code) is not allow on any mask build level.

1. Acute notches verification is accomplished by the spacing rule for each design level (verification of the compliment of an obtuse angle that is formed within a design level shape is accomplished by the spacing rule for each design level).

2.8.1 IBM Reserved Level Layout Rules

The following rules correspond to the Reserved Levels described in Table 2-2, “Design Services and Data Preparation Mask Levels (Restricted),” on page 30 and Table 2-3, “KERF Dummy Design Levels (Restricted),” on page 35.

Table 2-14. Reserved Level Layout Rules					
Rule	Class	Notes	Description		Design Min
RL01	a	-	xxFILL touching CHIPEDGE not allowed (xx = RX, PC, M1, M2, M3, M4, MQ, LY, AM)	=	-
RL03R	d	1	xxEXCLUD touching CHIPEDGE not allowed (xx = M1, M2, M3, M4, MQ)	=	-
RL03a	a	2	(LYEXCLUD not covered by TRANSMIS) touching CHIPEDGE not allowed (AMEXCLUD not covered by TRANSMIS) touching CHIPEDGE not allowed	=	-
RL04	a	-	xxCHEXCL touching CHIPEDGE not allowed (xx = M1, M2, M3, M4, MQ)	=	-
RL05	a	-	xxHOLE touching CHIPEDGE not allowed (xx = M1, M2, M3, M4, MQ)	=	-
RL06	a	-	xxHOLE touching CHIPEDGE not allowed (xx = V1, V2, V3, VL)	=	-
RL07	a	3	{FRAME, NEGMKS, POSMKS} touching CHIPEDGE not allowed	=	-
RL07a	a	-	{PAD_GBIF, FUSE, KERFEXCL} touching CHIPEDGE not allowed.	=	-
RL08	a	-	{BI, C_OUTLIN, FS, LA, PIN_DIO, RD, SB, TC, VI, VICUS} touching CHIPEDGE not allowed.	=	-
RLIOFET	a	-	{XE, XF} touching CHIPEDGE is prohibited.	=	-
RLT3	b	-	T3 touching CHIPEDGE is prohibited.	=	-
RLTSV	a	-	{TSV, SV} touching CHIPEDGE is prohibited.	=	-

1. Use of MxEXCLUD is allowed, but should be used only sparingly. Excessive use of MxEXCLUD shapes will result in low pattern density regions, that could negatively affect manufacturability. Over use of MxEXCLUD shapes will also drive DRC errors in the EPD_Mx_min series of ground rules. MxEXCLUD regions should be << 126 μm checking box.

2. See also related Rule TLR1 in Table 3-52, “Transmission Line Layout Rules,” on page 191.

3. This rule is not checked in DRC since these levels are not included in the technology file.

2.9 Important Design Guidelines

The following design guidelines are not design rule checked which means a careful reading is particularly important.

All wells must be contacted

Regular Array Layouts

Dummy cells or half cells are often used to terminate arrays. These are images that are not electrically active, but serve to create a consistent physical environment across all of the active cells. Both RX and PC photo effects have been observed that make the last cells on the edges of the array behave differently than the rest. The addition of these dummy images will mitigate these effects.

Dynamic Circuits

Dynamic circuits are sensitive to leakage currents which could come from many sources. The designers must ensure the circuits will function at all worst-case leakage conditions. Please refer to Section 4.0 , “Electrical Parameters and Models” on page 243 for detailed information.

- Keep dynamic nodes away from any junction that gets forward-biased (at least 3X minimum spacing rules). If the junction is forward biased by an input-output (I/O) signal, an N-well guardring is recommended.

Metal-to-Metal Capacitors

See Section 3.25 , “Metal-to-Metal Capacitor (MIM) Layout Rules” on page 186

Forward-Biased Diodes

The use of forward biased diodes is restricted as described Section 4.6.3 , “Forward-Biased Diodes” on page 263.

Polysilicon and Diffusion Wiring

Narrow polysilicon ($PC < 0.19 \mu\text{m}$ wide) and diffusion lines ($RX < 0.24 \mu\text{m}$ wide) are highly susceptible to defects which result in localized increases in the sheet resistance. The following design practices are strongly recommended:

- Narrow lines of polysilicon or diffusion must not be used in applications where DC voltage drops are important.
- Avoid chaining of gates.
- Place contacts close to the end of the gate, preferably on both ends of the gate.
- The length of narrow polysilicon or diffusion lines used for wiring should be kept to a minimum.

Leakage Sensitive Circuits

- For circuits that are more sensitive to leakage than static logic designs, please see Section 4.0 , “Electrical Parameters and Models” on page 243 for leakage-dictated design constraints.

No Polyimide Final Passivation Option - Modeling Implications

- If a No Polyimide Final Passivation Feature is used (see section Table 1-1., “Optional Features with Feature Part Numbers” on page 12), the Polyimide elimination is not accounted for in the device models. See section 3.34 , “No Polyimide Final Passivation option” on page 217. , and see “Note” on page 297.

Mixed Voltage Interfaces

Special consideration must be given when the design will interface to a voltage above 1.6V. See Section 4.22 , “Mixed Voltage Interfaces” on page 325.

Relaxed Designs and Recommended Rules

- Process and reliability yields will generally improve when designs are relaxed from the ground rule minimums. Minimum design dimensions should only be used to decrease the chip size or to improve the device performance.
- Design rules requiring exact dimensions (denoted by “≡” in the rule tables) are not to be relaxed.
- By using recommended rules ‘R’, higher product yields may be expected

Contacts and Vias

- Using redundant contacts and vias is strongly recommended to prevent contact open circuits in the design. See the recommendations in Section 5.4.2.3 , “General Rules at 100C/100K POH” on page 360 for using contacts and vias in wide lines.
- The electromigration (EM) reliability in terms of minimum intersection area of M1/CA, M2/V1, etc. must be verified as described in Section 5.4 , “Back End Of Line (BEOL) Reliability Design Rules” on page 358. Verification is particularly important for designs that will be miniaturized in future technologies.

Jogs and Non-orthogonal Lines

- Minimize the use of jogs below 0.25 μm in order to increase repairability of masks. Defects in the vicinity of jogs < 0.25 μm are generally not repairable.
- Avoid the use of 45° lines. Their use increases data volumes and the possibility of checking errors. Note that 45° lines are not allowed on several design levels as detailed in the Layout Rules tables.
- The compact device models do not reflect bent-gate structures due to the inherent three dimensional nature of these devices and the variable gate length at the bents.

Reduction of White Space on PC Level

- To assist with chip line width variation (ACLV) and chip mean variation of the device channel length, it is recommended that designers meet a local PC pattern density recommended rule, see Section 2.10.2.2 , “Local PC Pattern Density Guidelines” on page 65. High local PC density is caused by large areas of dense polysilicon (e.g. decoupling capacitors) that can degrade the ACLV. See Section 4.7 , “Resistor Models” on page 265 for more information on spacing from these type of structures.

Reduction of White Space on RX Level

- In order to adequately control the STI etch and polish processes, a global RX-density constraint (see Section 2.10, “Pattern Density Rules” on page 62) and a local RX-density constraint (see Rule 40 in Table 3-1, “Polysilicon and Isolation Layout Rules” on page 69). are required. IBM recommends using the RXFILL shapes that are automatically generated during data preparation by IBM during the release process.

Chip Origin

- The chip origin ($x=0$, $y=0$) must be placed at the lower left corner of the chip. CHIPEDGE must be bounded at $X=0$ on the left side of the chip (not in the chamfer area), and bounded at $Y=0$ at the bottom of the chip. See rule 999 in Table 3-59 on page 205.

Layout Rule Table Notes

The following notes apply to the tables in the Layout Rules section (starting with Table 3-1 on page 69 through Table 3-61 on page 214).

1. All layout rules are given in μm or in μm^2 .
2. Rules ending with the letter “R”, such as 104R, indicate that they are strong recommendations for a designer to follow. Recommended rules are not present in the checking deck.
3. Rules ending with the letter “M”, such as 51M, indicate that they are required for the design to be migrated (shrunk) into future technologies. These rules are not requirements for designs only to be built in the technology described in this document.
4. While most wafer nominal dimensions refer to the bottoms of features, the following conventions are followed:
 - 4a) Widths of features are the width at the bottom.
 - 4b) Spaces between like features are the minimum distance. For example, for poly lines the distance is bottom-bottom, while stud contacts and stud vias the distance is top-top.
 - 4c) Spaces between features on different levels are the horizontal component of the distance between the bottom of the upper feature to the top of the lower feature.
 - 4d) RX features are measured from the bottom of the silicide, which is the top of the isolation trench.
 - 4e) Deviations from these conventions are noted in the tables.
5. Use of “length” indicates that the shape is required to be a rectangle.
6. RX Rules: RX denotes the active silicon region (source, drain, FET channel, capacitor, etc.) which is also known as diffusion and as thin oxide. Where distinction is useful, junctions and contacts are distinguished.

OP resistors

- The use of the n^+ -type poly and p^+ -type diffusion resistors are not offered due to higher overall process tolerances.
- The poly width should be greater than $1.5 \mu\text{m}$ in order to obtain reasonably small absolute variation.

2.10 Pattern Density Rules

2.10.1 Global Pattern Density

Table 2-15. Pattern Density Rules ¹						
Rule	Class	Notes	Description		Design Min.	Design Max.
PDRX_max	a	-	(Summed RX area across full chip) / (CHIPEDGE area).	≥	-	≤ 75% ²
EPDG_RX_min	a	-	(Summed RX estimated area across full chip) / (CHIPEDGE area).	≥	25% ³	≤ -
PDPC_max	a	-	(Summed PC area across full chip) / (CHIPEDGE area).	≥	-	≤ 30% ⁴
EPDG_PC_min	a	⁵	(Summed PC estimated area across full chip) / (CHIPEDGE area).	≥	15%	≤ -
PDDT	a	-	(Summed DT area across full chip) / (CHIPEDGE area).	≥	1%	≤ 20%
PDDTR	d	-	(Summed DT area across full chip) / (CHIPEDGE area).	≥	4%	≤ 20%
PDEV	a	-	(Summed EV area across full chip) / (CHIPEDGE area).	≥	0.0%	≤ 5%
PDEX	a	-	(Summed EX area across full chip) / (CHIPEDGE area).	≥	0.0%	≤ 5%
PDQY	a	⁶	(Summed QY area across full chip) / (CHIPEDGE area).	≥	0.0%	≤ 40%
PDLY	a	-	(Summed LY area across full chip) / (CHIPEDGE area).	≥	23%	≤ 70%
PDAM	a	-	(Summed AM area across full chip) / (CHIPEDGE area).	≥	23%	≤ 70%
PDLV	a	-	(Summed LV area across full chip) / (CHIPEDGE area).	≥	0%	≤ 20%
PDDV	a	-	(Summed DV area across full chip) / (CHIPEDGE area).	≥	0%	≤ 20%

1. These rules will be checked as part of the IBM release process.

2. The interpretation of the RX density value for the Design Maximum in the Global Pattern Density rule is for the drawn RX shapes in the chip design. When feasible, it is recommended that designers avoid submitting designs to IBM close to the maximum RX global pattern density limit.

3. The RX Design Min (minimum) Global Pattern Density rule is not checked in the Technology Design Kit. IBM prefers that RX minimum Global Pattern Density is not checked by the customer, or attempted to be met by the customer, prior to submission of the chip design to IBM. The RX minimum Global Pattern Density for the chip design will be verified by the IBM release team, to this rule requirement, after IBM-generated RXFILL is applied to the chip design, which is part of the IBM release process. After IBM auto-generated RXFILL is applied, the RX minimum Global Pattern Density must be met as a requirement. Any chip design aspects that prohibit the RX Global Pattern Density minimum from being met will require modification prior to final design submission. The RX maximum Global Density Rule is checked in the Technology Design Kit and should not be exceeded upon chip design submission to IBM.

4. The interpretation of the PC density value for the Design Maximum in this Global Pattern Density rule is for the drawn PC shapes in the chip design, prior to the inclusion of IBM generated PCFILL. The PC maximum Global Density Rule is not verified using a predictive algorithm. After the IBM release process is completed, (PC + IBM generated PCFILL) may exceed this value. This effect is anticipated and is accounted for the Manufacturing Process assumptions.

5. The PC Design Min (minimum) Global Pattern Density rule is verified using a predictive algorithm (for more details, see Rule PDPC in Table H-4, “Estimated Pattern Density Rules,” on page 427), because IBM prefers customers use auto-generated PCFILL added by IBM Product Engineering as a part of the standard Tape-out and Release process and because the recommended PC local density (see Rule 42aR in section Table 3-1., “Polysilicon and Isolation Layout Rules” on page 69) is not required to be met prior to submission of the chip design to IBM. The actual PC minimum Global Pattern Density for the chip design will be verified by the IBM release team, to this rule requirement, after IBM-generated PCFILL is applied to the chip design during the release process. The PC minimum Global Pattern Density must be met as a requirement prior to mask build. Any chip design aspects that prohibits the PC Global Pattern Density minimum from being met, as discussed in section 2.10.1.3, “Global PC Pattern Density Requirements” on page 64 or section 2.10.2.2, “Local PC Pattern Density Guidelines” on page 65 or section H.1.1, “Estimated Pattern Density Generation” on page 425, will require modification prior to final design submission. If customer drawn PC, or the PCEXCLUD design levels are used, these levels are accounted for in the predictive PC Global Density algorithm.

6. QY global pattern density minimum limit is not required.

2.10.1.1 RX and PC General Pattern Density Requirements

Minimum-density requirements for RX and PC are normally satisfied by the use of IBM-generated FILL shapes on those levels, and need not be satisfied before the design is released to IBM. If a particular design does not use IBM-generated FILL shapes on any of these levels, the minimum-density requirement for that level must be met as-designed.

2.10.1.2 Global RX Pattern Density Requirements

See Rules EPDG_RX_min and PDRX_max in Table 2-15 on page 62. The BiCMOS8HP Shallow Trench Isolation manufacturing process requires that the chip-average RX density be between 25% and 75%.

The BiCMOS8HP Shallow Trench Isolation manufacturing process requires that local RX density be at least 20% over a distance of 126 μm (Primary Layout Rule EPDL_RX_min). This STI-specific process requirement can be satisfied by inactive “dummy” shapes placed by the designer on the level RX. Although non-functional from a circuit perspective, these added shapes must satisfy all of the design rules applicable to RX. Alternatively, dummy shapes generated on the reserved level RXFILL (available from IBM Product Engineering as a part of the standard Tape-out and Release process) will also satisfy the STI manufacturing process requirements, and with potentially much less design effort.

If RXFILL programs are to be used, shapes **must** be added to mark all of the following structures for exclusion from RXFILL:

- product label area: BM will place RXFILL shapes within product label areas defined by the design level LOGOBN. If designers seek to exclude RXFILL shapes from the product label area, draw RXEXCLUD over the entire product label. The local RX density within such RXEXCLUD shapes must satisfy the minimum local-RX-density (see Rule EPDL_RX_min in Table 3-1 on page 69). For addi-

tional information on LOGOBND, see section 3.33 , “Product Labels” on page 213

- N-well resistors. Draw RXEXCLUD over the body of all n-well resistors greater than or equal to 1.4 μ m in the minor dimension. **Note:** N-well resistors are not supported in the BiCMOS8HP technology.
- other regions: in certain rare circumstances it may be beneficial to exclude RXFILL shapes from other circuit regions; draw RXEXCLUD to cover such regions. The local RX density within such RXEXCLUD shapes must satisfy the minimum local-RX-density (See Layout Rule EPDL_RX_min in Table 3-1 on page 69). Contact IBM Product Engineering for detailed guidelines.

See additional information in section 2.10.2.1 , “Local RX Pattern Density Requirements” on page 64

2.10.1.3 Global PC Pattern Density Requirements

See Rules EPDPC_PC_min and PDPC_max, in Table 2-15 on page 62. The BiCMOS8HP PC manufacturing process requires that the chip-average PC density be between 15% and 30%. This process requirement can be satisfied by inactive dummy shapes placed by the designer on the level PC. Although non-functional from a circuit perspective, these added shapes must satisfy all of the design rules applicable to PC. Alternatively, dummy shapes generated on the reserved level PCFILL (available from IBM Product Engineering as a part of the standard Tape-out and Release process) will also satisfy the manufacturing process requirements.

If PCFILL programs are to be used, shapes **must** be added to mark all of the following structures for exclusion from PCFILL:

- product label area: draw LOGOBND over the entire product label. See section 3.33 , “Product Labels” on page 213.
- other regions: in certain rare circumstances it may be beneficial to exclude PCFILL shapes from other circuit regions; draw PCEXCLUD to cover such regions. The local PC density within such PCEXCLUD shapes should still satisfy the recommended minimum local-PC-density (Primary Layout Rule EPDL_PC_minR). Contact IBM Product Engineering for detailed guidelines.

2.10.2 Local Pattern Density

2.10.2.1 Local RX Pattern Density Requirements

The BiCMOS8HP Shallow Trench Isolation manufacturing process requires that local RX density be at least 20% over a distance of 126 μ m (see Layout Rule EPDL_RX_min in Table 3-1 on page 69).

All portions of the chip, except those specifically stated in Section 2.10.1.2 “Global RX Pattern Density Requirements” on page 63 will receive RXFILL shapes as part of the standard Tape-out and Release process. If RXFILL generation is not performed by Product Engineering, the minimum local-RX-density (See Layout Rule EPDL_RX_min) must be met for the entire design, as specified in Table 3-1, “Polysilicon and Isolation Layout Rules,” on page 69. If RXFILL generation is performed by Product Engineering, Rule EPDL_RX_min must be met within every region. Note that certain discouraged design practices, such as long dense runs of PC wiring, are not compatible with RXFILL. Contact your IBM technical representative for more guidelines.

2.10.2.2 Local PC Pattern Density Guidelines

The BiCMOS8HP PC manufacturing process recommends that the local PC density be between 5% and 80%. To assist with meeting this recommended rule, all portions of the chip, except those specifically stated in Section 2.10.1.3 “Global PC Pattern Density Requirements” on page 64 will receive PCFILL shapes as part of the standard Tape-out and Release process.

If PCFILL generation is not performed by Product Engineering, the minimum local-PC-density (see Layout Rule EPDL_PC_minR) is recommended to be achieved, as specified in Table 3-1, “Polysilicon and Isolation Layout Rules,” on page 69. When PCFILL generation is performed by Product Engineering, the goal is to achieve the recommended design minimum of Rule EPDL_PC_minR within every region. Contact your IBM technical representative for more guidelines.

2.10.2.3 Local Metal Pattern Density Requirements

Copper Pattern Density Layout Requirements

The BiCMOS8HP Copper manufacturing process requires several design constraints on the wiring levels that are not necessary for Aluminum and Tungsten/Oxide based technologies. Specifically, local regions of very-high or very-low metal pattern density are difficult to manufacture, as are very wide wires or very wide regions of white space. Because of these constraints, IBM-generated Metal FILL and Metal HOLE shapes are required for all BiCMOS8HP designs. All portions of the chip except those specifically enumerated below will receive Metal FILL and Metal HOLE shapes from IBM Product Engineering as a part of the standard Tape-out and Release process.

Wide Copper Mx (x=1,2,3,4,Q) wires (structures) that violate the spirit of the wide line restrictions (see Rules 500b, 600b or 690b) should use MxPLANE levels for 70% pattern density See Section Appendix I., “MxPLANE Information” on page 434. Contact your IBM technical representative for more guidelines.

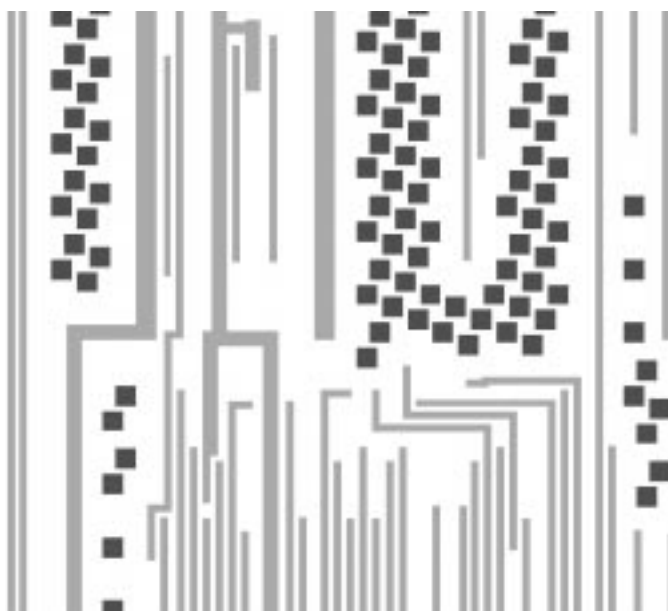


Figure 2-1. IBM-generated Metal Fill Shapes

IBM-generated MxFILL shapes are small, electrically-isolated metal shapes on a staggered grid. They are squares, three times as large as the minimum linewidth for that metal level. The closest approach to of an MxFILL shape to Mx is twice the minimum space for that metal level. (see Table H-1, “xxFILL Rules,” on page 417).

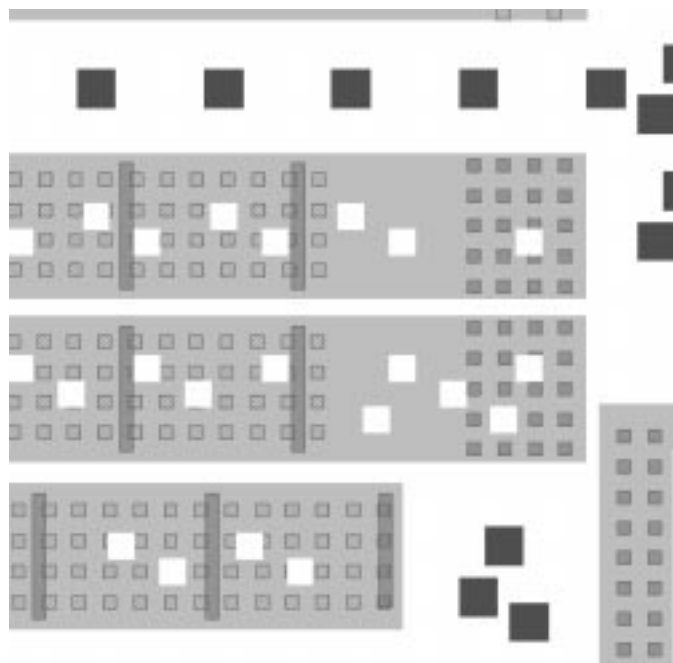


Figure 2-2. IBM-generated Metal HOLE shapes

IBM-generated MxHOLE shapes lie on the same staggered grid as MxFILL shapes, and are resolved at Mask-write as small openings in the associated metal level. HOLE shapes are squares, two times as large as the minimum linewidth for that metal level, and are only placed within wide metal. The closest approach of an MxHOLE shape to the inside edge of an Mx line is twice the Mx minimum linewidth. HOLE shapes do not obstruct single vias, single rows of vias or double rows of vias, and M1HOLE shapes do not obstruct CA or CABAR shapes. MxHOLE shapes are allowed to touch or intersect a fraction of the vias directly above or below Mx if those vias are redundant, as for example those in a dense array of vias contacting the same wide metal above and below. (See Figure 2-2) Typically 80% of the metal/via/metal intersect-area in such an array is unobstructed by MxHOLE shapes. The via resistances specifications in Table 4-32, “Effective Linewidth for Wires with HOLE Shapes,” on page 286 are met for any collection of vias, even in the presence of IBM-generated HOLE shapes.

VxHOLE shapes are used to remove from the design those few redundant vias that are covered or nearly-covered by a metal hole on the level immediately above.

The specified metal sheet resistance (Table 4-31, “Conducting Film Thicknesses and Sheet Resistances at 25°C,” on page 284 and Table 4-32, “Effective Linewidth for Wires with HOLE Shapes,” on page 286) anticipate the placement of generated Fill and Hole shapes, and accurately reflect their effects on the measurable wiring resistance and capacitance. Contact IBM Product Engineering for further details.

As MxFILL and MxHOLE shapes are generated for every design in BiCMOS8HP, shapes **must** be added to mark all of the following specific structures for exclusion:

- Modelled Wirebond or C4 pads: draw BONDPAD to cover AM. See section 3.28 , “Terminals, IO Pads, C4 and Wirebond” on page 193. Drawing BONDPAD is not required for typical non-modelled wirebond or C4 pads. No explicit MxEXCLUDE shapes are required or recommended for wirebond pads; all necessary exclude shapes are automatically generated in Design Services.
- Chip guardring: draw GUARDRNG to cover the guardring structure. No explicit MxEXCLUDE or MxCHEXCL shapes are required or recommended for the Chip Guard Ring; all necessary exclude shapes are automatically generated in Design Services. See section 3.30 , “Chip Guard Ring and Chamfer” on page 203.
- Product Label area: draw LOGOBN over the entire product label. See section 3.33 , “Product Labels” on page 213.
- Inductors: draw IND_FILT to cover the body of the inductor. See section 3.26 , “Inductor Layout Rules” on page 189.
- RF Interconnect Line: draw TLINE to cover the structure. See section 3.27 , “Transmission Line and RF Interconnect Layout Rules” on page 191.
- Transmission Lines and Distributed Passives: IBM uses TRANSMIS to cover the body of the transmission line and distributed passives. See TRANSMIS in Table 2-4, “Dummy Design Levels and Utility Levels,” on page 36. The TRANSMIS shape enables the use of xxEXCLUDE (xx = LY, AM) per Rules RL03a (see Table 2-14, “Reserved Level Layout Rules,” on page 58). Note that MxEXCLUDE (x=1,2,3,4,Q) use is prohibited. Transmission line and distributed passive structures receive IBM auto-generated MxFILL on the Mx (x=1,2,3,4,Q) mask levels during the IBM release process.
- KQ BEOL Resistor: IBM uses the KQ design level to prohibit MQFILL physically under this device, for the MQ design level only. When KQ BEOL resistors are placed in a chip design, Rule KQ10 (see Table 3-42, “KQ Resistor Layout Rules,” on page 167) must be met prior to design submission to IBM, and Rule PD4a (see Table H-3, “Pattern Density Rules,” on page 425) must be met after IBM-generated Metal FILL is applied as a part of the standard IBM Product Engineering Tape-out and Release process.

Note: MxEXCLUDE or MxCHEXCL shapes are prohibited without prior approval of IBM Product Engineering, where Mx = 1,2,3,4, or Q.

Additional Aluminum Pattern Density Layout Requirements

The following rules describe additional layout rules to be met if the designer includes inactive metal shapes prior to design submission to IBM. The fill shapes drawn by the customer must be on the existing metal drawing levels and can not be on the reserved levels xxFILL.

For further details on the IBM FILL-aware checking decks, or to have IBM fill the design in lieu of the designer including inactive metal shapes, contact your IBM Product Engineering Representative.

Table 2-16. Additional LY or AM Rules ¹					
Rule	Class	Notes	Description		Design Min
F27a	b	2	Inactive LY area (μm^2) maximum per shape.	\leq	144.0
F27c	b	3, 4	Inactive AM area (μm^2) maximum per shape.	\leq	100.0

1. Inactive xx (where xx = metal level name) identified in this table refers to "electrically inactive shapes drawn by the designer on the respective LY, or AM design levels. xx does not refer to xxFILL shapes designed on these levels that are reserved for IBM use only.
2. Inactive LY is checked as: LY not touching {VY, VYBAR AV, AVBAR, TRANSMIS, LOGOBND, TLINE}
3. Inactive AM is checked as: AM not touching {AV or AVBAR or (LV or LVDUMMY or DV) or TRANSMIS or LOGOBND or TLINE}.
4. Inactive AM is only required to meet Global Pattern Density Requirements. There is not a local pattern density requirement for AM.

2.10.3 RX, PC, M1, M2, M3, M4, and MQ; Estimated Pattern Density Rules

Estimated pattern density algorithms are defined in Section H.1.1, "Estimated Pattern Density Generation" on page 425. Estimated pattern density rules provide an early warning to designers on both low and high density areas.

3.0 Layout Rules

3.1 Polysilicon and Isolation Layout Rules

All layer names referred to in this design manual are design level names unless otherwise stated. For layer names, see section 2.0 , “Physical Layout Information” on page 25.

Column named: “Class”, adjacent to “Rule column”, specifies Manufacturability Rule Classification with respect to DRC violations;

- a = Automatic Reject (severity1),
 - Possible impact to either: production tools or processes
 - Possible impact to either: IBM Kerf and/or WAC
 - Possible impact to mask build
 - Possible impact to other rider (multi-client MPW)
- b = Significant Yield / Reliability Impact (severity2),
- c = Moderate Yield / Reliability Impact (severity3),
- d = Yield Enhancement (recommend compliance) (severity4).

Table 3-1. Polysilicon and Isolation Layout Rules

Rule	Class	Notes	Description		Des Min.	Waf. Dim.	Tol.
1	a	-	PC width over RX for NFET device Lp.	≥	0.12	0.180 ¹	0.022 ¹
2	a	-	PC width over RX for PFET device Lp.	≥	0.12	0.092 ¹	0.022 ¹
3	c	-	PC width over RX for 45° NFET device Lp.	≥	0.127	0.0990 ¹	0.029 ¹
3R	d	-	PC width over RX for 45° NFET device Lp.	≥	0.140	0.1120 ¹	0.029 ¹
4	c	-	PC width over RX for 45° PFET device Lp.	≥	0.127	0.0990 ¹	0.029 ¹
4R	d	-	PC width over RX for 45° PFET device Lp.	≥	0.140	0.1240 ¹	0.029 ¹
10	a	-	RX width under PC for NFET device W.	≥	0.16	0.1150	0.040
11	a	-	RX width under PC for PFET device W.	≥	0.16	0.1150	0.040

Table 3-1. Polysilicon and Isolation Layout Rules

Rule	Class	Notes	Description		Des Min.	Waf. Dim.	Tol.
40	-	-	This rule has been deleted, and replaced by EPDL_RX_min.				
EPDL_RX_min	a	2,3,4	(rx_estimated) minimum density (%) over local 126 μ m x 126 μ m areas stepped in 63 μ m increments across the chip, except those checking boxes that touch LOGOBND or corner chamfers (PROTECT) (where rx_estimated is defined as EPDL_rx_min).	\geq	20	-	-
41	a	2,5	RX maximum density (%) over local 126mm x 126mm areas stepped in 63mm increments across the chip.	\leq	75	-	-
42aR	-	-	This rule has been deleted, and replaced by EPDL_PC_minR.				
EPDL_PC_minR	d	6,7,8	(pc_estimated) minimum density (%) over local 126 μ m x 126 μ m areas stepped in 63 μ m increments across the chip, except those checking boxes that touch LOGOBND or corner chamfers (PROTECT) (where pc_estimated is defined as EPDL_pc_min).	\geq	5	-	-
42b	a	6,9	PC maximum density (%) over local 126 μ m x 126 μ m areas stepped in 63 μ m increments across the chip, applies to all regions of the chip except regions within VAR.	\leq	80	-	-
50	a	-	RX width (silicide).	\geq	0.16	0.1150	0.04
50b	b	-	RX width (silicide), in at least one direction, minor dimension.	\leq	100.00	-	-
50R	d	-	RX width (silicide).	\geq	0.24	0.1950	0.040
51	a	-	RX area (μ m ²).	\geq	0.100	-	-
51R	d	-	RX area (μ m ²).	\geq	0.140	-	-
52	b	-	RX to RX space (trench).	\geq	0.18	0.2100	0.044
52R	d	-	RX to RX space (trench).	\geq	0.26	0.2900	0.044
100	a	-	PC width not over RX (w/o spacer).	\geq	0.12	0.092	0.022

Table 3-1. Polysilicon and Isolation Layout Rules

Rule	Class	Notes	Description		Des Min.	Waf. Dim.	Tol.
100R	d	-	PC width not over RX (w/o spacer).	\geq	0.19	0.1620	0.022
101a	a	-	PC area (μm^2).	\geq	0.105	-	-
101b	a	-	PC enclosed area (μm^2).	\geq	0.151	-	-
102	b	-	(PC to PC space) not over RX.	\geq	0.20	0.1630	0.022
102R	d	-	(PC to PC space) not over RX.	\geq	0.26	0.2230	0.022
104a	b	-	(PC to PC) over RX (NFET spacing).	\geq	0.20	0.0847	0.026
104b	b	-	(PC to PC) over RX (PFET spacing).	\geq	0.20	0.0847	0.026
104R	d	-	(PC to PC) over RX.	\geq	0.26	-	-
110	b	-	RX overlap past PC (silicide width). This Rule is checked as <i>outside edge</i> of PC to <i>inside edge</i> of RX except for floating gate tie-down shapes. See <i>two</i> usage examples in Figure 3-1, "Isolation and Polysilicon Rules" on page 78.	\geq	0.20	0.1199	0.065
110R	d	-	RX overlap past PC (silicide width). This Rule is checked as <i>outside edge</i> of PC to <i>inside edge</i> of RX except for floating gate tie-downs.	\geq	0.33	0.2499	0.065
110a	b	-	((RX overlap past PC) not over GRLOGIC) (silicide width). This Rule is checked as <i>outside edge</i> of PC to <i>inside edge</i> of RX except for floating gate tie-downs. See <i>one</i> example in Figure 3-1, "Isolation and Polysilicon Rules" on page 78. Note: Rule 110a only applies to RX (diffusion) overlap past PC (gate edge) on the same FET.	\geq	0.55	0.4699	0.065
110aR	d	-	((RX overlap past PC) not over GRLOGIC) (silicide width). This Rule is checked as <i>outside edge</i> of PC to <i>inside edge</i> of RX except for floating gate tie-downs. Note: Rule 110aR only applies to RX (diffusion) overlap past PC (gate edge) on the same FET.	\geq	0.680	0.5999	0.065

Table 3-1. Polysilicon and Isolation Layout Rules

Rule	Class	Notes	Description		Des Min.	Waf. Dim.	Tol.
111	b	-	PC overlap past RX, when [(PC intersect RX) to RX corner $\geq 0.08 \mu\text{m}$] and [PC(END) area not over RX $< 0.046 \mu\text{m}^2$].	\geq	0.23	0.0845	0.068
111b	b	-	(PC overlap past RX), when [PC(END) area not over RX $\geq 0.046 \mu\text{m}^2$].	\geq	0.200	-	-
111R	d	-	PC overlap past RX, when [(PC intersect RX) to RX corner $\geq 0.08 \mu\text{m}$] and [PC(END) area not over RX $< 0.046 \mu\text{m}^2$].	\geq	0.25	-	-
112	b	-	PC overlap past RX, when (PC intersect RX) to RX corner $< 0.08 \mu\text{m}$.	\geq	0.28	0.0345	0.077
112R	d	-	PC overlap past RX, when (PC intersect RX) to RX corner $< 0.08 \mu\text{m}$.	\geq	0.30	-	-
113b	c	-	PC to RX, for common run lengths $> 2.00 \mu\text{m}$ (See rule 130b).	\geq	0.08	-	-
113R	d	-	PC to RX for low PC wiring capacitance (except where PC is tied to RX).	\geq	0.08	0.1130	0.064
114	c	-	PC to RX corner, when RX corner and gate are on same FET.	\geq	0.06	-0.007	0.074
114b	c	10	PC to RX corner, when RX notch width < 0.28 and RX corner and gate are on same FET.	\geq	0.10	-0.007	0.074
114c	c	10	PC to RX corner, when RX notch width < 0.24 and RX corner and gate are on same FET.	\geq	0.15	-0.007	0.074
114R	d	-	PC to RX corner, for constant W_{eff} .	\geq	0.24	0.1730	0.074
115	c	-	PC corner to RX, when gate corner and RX are on same FET; does NOT maintain constant L_{eff} .	\geq	0.08	0.0255	0.067
115R	d	-	PC corner to RX, when gate corner and RX are on same FET; for constant L_{eff} .	\geq	0.24	0.1855	0.067
119	c	-	PC vertex within RX.	\geq	0.20	-	-

Table 3-1. Polysilicon and Isolation Layout Rules

Rule	Class	Notes	Description		Des Min.	Waf. Dim.	Tol.
120a	c	-	Only 45° PC gate vertices are allowed over RX.	≡	-	-	-
120b	c	-	Distance between two inside corners of bent gate which bends twice in the same direction (length of 45° gate segment).	≥	0.08	-	-
120c	c	-	Minimum PC notch over RX.	≥	0.33	-	-
121	c	-	PC may only straddle RX at 90 degrees.	≡	-	-	-
123a	c	11	Only inside 45 degree RX vertices are allowed under (PC not over GRLOGIC).	≡	-	-	-
123b	c	11	Distance between 2 inside corners of ((RX under PC) not over GRLOGIC).	≥	0.08	-	-
125	c	12	PC over RX must divide the RX into two or more diffusions.	≡	-	-	-
130a	b	-	For PC intersecting RX, maximum ratio of (the total PC area) / (the total PC area over RX).	≤	100	-	-
130b	b	-	PC(not intersecting any RX) to RX.	≥	0.08	-	-
130c	b	-	For PC intersecting RX, maximum ratio of [perimeter (PC not over RX)] / [area (PC over RX)] ; where ([perimeter] / [area] rule units in terms of 1/μm).	≤	210	-	-
131	b	13,14	<p>Gates connected to Mx must meet the following ratio: { (Mx area) / [(PC over RX) area + (5 * (diode diffusion area))] } ≤ 150. Where Mx = M1, M2, M3, M4.</p> <p>Gates connected to Mz must meet the following ratio: { (Mz area) / [(PC over RX) area + (2 * (diode diffusion area))] } ≤ 150. Where Mz = MQ, LY, AM.</p> <p>(Note: See also Rule 131f)</p>				

Table 3-1. Polysilicon and Isolation Layout Rules

Rule	Class	Notes	Description		Des Min.	Waf. Dim.	Tol.
131a	b	15	<p>Gates (Thick Oxide) connected to Vx must meet the following ratio: $\{ (Vx \text{ area}) / [((PC \text{ over RX}) \text{ over DG}) \text{ area} + (7.5 * (\text{diode diffusion area}))] \} \leq 0.50$, where Vx = [union (V1, V1BAR) or union (V2, V2BAR) or union (V3, V3BAR)].</p> <p>Gates (Thick Oxide) connected to ViaZ must meet the following ratio: $\{ (ViaZ \text{ area}) / [((PC \text{ over RX}) \text{ over DG}) \text{ area} + (3.0 * (\text{diode diffusion area}))] \} \leq 0.50$ where ViaZ = [union (VL, VLBAR) or union (VY, VYBAR) or union (AV, AVBAR)].</p>				
131b	b	15	<p>Gates (Thin Oxide) connected to Vx must meet the following ratio: $\{ (Vx \text{ area}) / [((PC \text{ over RX}) \text{ NOT over DG}) \text{ area} + (7.5 * (\text{diode diffusion area}))] \} \leq 10.00$, where Vx = [union (V1, V1BAR) or union (V2, V2BAR) or union (V3, V3BAR)].</p> <p>Gates (Thin Oxide) connected to ViaZ must meet the following ratio: $\{ (ViaZ \text{ area}) / [((PC \text{ over RX}) \text{ not over DG}) \text{ area} + (3.0 * (\text{diode diffusion area}))] \} \leq 10.00$, where ViaZ = [union (VL, VLBAR) or union (VY, VYBAR) or union (AV, AVBAR)].</p>				
131c	b	-	Ratio of union (CA, CABAR) contact area to (PC over RX) oxide area	\leq	2.00	-	-
131f	b	13	Gates connected to (VL or VLBAR) must have an RX diode diffusion tie down (see section 3.1.1, "Antenna Rules" on page 78 for valid tiedown definition) at Mx or lower. Where Mx = M1, M2, M3, M4 (Note: See also Rule 131)				
132	c	-	(PC intersect RX) must have an area (μm^2)	\leq	230.00	-	-
132R	d	-	(PC intersect RX) must have an area (μm^2)	\leq	45.00	-	-

Table 3-1. Polysilicon and Isolation Layout Rules

Rule	Class	Notes	Description		Des Min.	Waf. Dim.	Tol.
134	b	-	<p>Every Nwell containing a gate¹⁶ (PC intersect RX) must satisfy either</p> <ul style="list-style-type: none"> — there is a p+ diffusion in the Nwell that is connected to a n+ diode diffusion outside of (Nwell or PI or JD or BFMOAT or BB or RN or BX). — there is a n+ Nwell contact connected to an n+ diode diffusion outside of (Nwell or PI or JD or BFMOAT or BB or RN or BX) (this may be satisfied by an RX image straddling the Nwell). — there is a n+ Nwell contact (in the Nwell) or p+ diffusion (in the Nwell) connected to a valid substrate contact [(RX over BP) not over (Nwell or PC or IND_FILT or BFMOAT or PI or JD or BB or RN or BX)] <p>by the time M1 level is complete.</p>	≡	-	-	-

1. This measurement is a physical on-wafer dimension.

2. In checking this local area requirement the checking box must be stepped in half box sized increments. When tiling steps over the chip or cell boundary, move the tile back *in bounds* to satisfy this requirement. For tiles containing corner chamfers, corner density is calculated based on the least enclosing rectangular shape. If chip will be filled by IBM Product Engineering as part of the release process, designers are expected to meet this rule, including areas that will be prevented from receiving IBM generated RXFILL (i.e., within RXEXCLUD or PCEXCLUD if RXFILL and PCFILL run together using Design Services) prior to design submission. For regions of RXEXCLUD that are smaller than the checking box in at least one direction, the RX density must satisfy the minimum specification for the checking box, taking into account that the region of RXEXCLUD will not get any additional RXFILL to increase the RX density. For more information, see Section 2.10.2 , “Local Pattern Density” on page 64. IBM will place RXFILL within (LOGOBND intersect CHIPEDGE). For RXFILL aspects within LOGOBND that is part of the IBM KERF (LOGOBND not touching CHIPEDGE), refer to the applicable RXFILL rule in Section Table H-1. , “xxFILL Rules” on page 417.

3. In the design kit, the actual Design Minimum value is coded at 25% in lieu of the specified 20% value in this table to account for any potential tool-to-tool variation between the predicted density value and the actual density that results after the IBM design services process is completed as part of the IBM release process. IBM strongly recommends designers adhere to the design kit checking of this rule, even though it is slightly more restrictive than the actual rule, to avoid evidencing local density violations during the final design release process, which could result in design submission delay. If Rule 40 errors are evidenced during layout, IBM recommends spacing RXFILL inhibiting devices or design levels further apart, such as polysilicon resistors (P+, OP RR), or long dense PC wires, PCFUSE devices or RXEXCLUD shapes. Else, IBM suggests limiting usage of design levels that intentionally reduce auto-generated RXFILL density or also spacing these levels further apart, such as BONDPAD, BFMOAT, IND_FILT. Additional note to designers: The design may expect CHIPEDGE to be present for these checks to function accurately. Therefore, designers are encouraged to place the CHIPEDGE shape around their layout if checking is not occurring at the actual chip level for the most accurate predictive checking for this layout rule.
4. This rule is intended to be equivalent to the checking that is performed per Rule PD1a, after IBM design services is completed during the typical IBM release process (see Table H-3, "Pattern Density Rules," on page 425). Graphical representation of the individual RXFILL shapes is not provided, rather a summary of the predicted local density results. This rule is included to "predictively estimate" the resulting RX local pattern density, inclusive of IBM added RXFILL, that will occur in the final chip design, after IBM design services is applied, to assist designers with layout so that the RX local density requirements that is necessary for Front-End-Of-Line manufactureability can be achieved.
5. The design kit uses the same design minimum value that is specified in this table for checking to this requirement. This check is not required to include predictive RXFILL added during the IBM release process.
6. In checking this local area requirement the checking box must be stepped in half box sized increments. When tiling steps over the chip or cell boundary, move the tile back *in bounds* to satisfy this requirement. For tiles containing corner chamfers, corner density is calculated based on the least enclosing rectangular shape. If chip will be filled by IBM Product Engineering as part of the release process, as a guideline it is preferred that designers meet this recommended rule in areas that will be prevented from receiving IBM generated PCFILL (i.e., within PCEXCLUD or RXEXCLUD if RXFILL and PCFILL run together using Design Services) prior to design submission. For regions of PCEXCLUD that are smaller than the checking box in at least one direction, the PC density is recommended to meet the minimum specification for the checking box, taking into account that the region of PCEXCLUD will not get any additional PCFILL to increase the PC density. For more information, see "" on page 65. As stated in the rule description, this recommended rule is not applicable for checking boxes that touch LOGOBNB as the LOGOBNB shape does not receive IBM auto-generated PCFILL.
7. If designers are having difficulty meeting recommended Rule 42aR during layout, IBM recommends spacing PCFILL inhibiting devices or design levels further apart, such as HA Varactors, ESD diodes, N+ diffusion or NW resistors or wide RX shapes without PC or (PC over RX) structures in the local vicinity, or PCEXCLUD shapes. Else, IBM suggests limiting usage of design levels that intentionally reduce auto-generated PCFILL density or also spacing these levels further apart, such as BONDPAD, BFMOAT, IND_FILT, TLINE.
8. For details on the algorithm used for predictive checking of this recommended rule, see Rule 42aR in Table H-4, "Estimated Pattern Density Rules," on page 427. This recommended rule is intended to be equivalent to the description of recommended Rule PD2aR (see section Table H-3, "Pattern Density Rules" on page 425), after IBM design services is completed during the typical IBM release process. This rule, if enabled "predictively estimates" the resulting PC local pattern density that occur in the final chip design, after IBM design services is applied, to assist designers with layout so that the PC local density recommended rule can be achieved.
9. The design kit uses the same design minimum value that is specified in this table for checking to this requirement. This check is not required to include predictive PCFILL added during the IBM release process.
10. Rule 114b and 114c are intended to protect against RX (space/notch) end shorting that travels perpendicular to the PC line direction. A PC line traveling across a narrow RX notch (run perpendicular to the notch run - all or part way) should be subject to this rule. However, (PC end that is coming into the RX notch) or (PC overlap past RX into the notch) are covered by other rules.
11. Rule 123b value is determined by Rule 120b.
12. Rule 125 is waived for decoupling capacitors or varactors where (PC over RX) is covered by VAR. For additional information, see Rule VAR29 in see section Table 3-45., "Varactor Layout Rules" on page 173.
13. For more information concerning these rules, including pass through resistors, see section 3.1.1.1, "Definitions" on page 78. Rules 130a and 131 and 131f are intended to avoid gate oxide integrity degradation by polysilicon charging during manufacturing. If PC is within 0.08 μm (Rule 130b for PC of RX, PC may overlap RX and form a very large antenna. Therefore It is highly recommended that ALL PC touching RX (PC < Rule 130b from RX) be connected to N+ or P+ junction prior to the MQ wiring level. Circuits whose operation is critically dependent on threshold voltage control or matching should not have antennae without this diode clamp. Note All gates are assumed to be analog gates and must be tied down to a diffusion before the MQ wiring level. Even if gates are covered by GRLOGIC, or are logic gates, they are only assumed to be able to withstand the threshold voltage shift of the metal antenna mentioned in the first line of Rule 131 if they are not in the same net as (Mx touching VL). However, gates tied to substrate contacts do not need to meet the tiedown diffusion area requirements.
14. Presently GR131 may not be checked as specified above by some tools provided. GR131 may be checked, in an alternative and conservative manner as 2 separate ratio checks. Consult your IBM Technical Representative for additional information.
15. Rule does not apply to gates tied to substrate contacts.

16. GR 134 includes PCDCAP/MOS varactors NW's and NW's bounded by DT. All NW's containing ((PC intersect RX) must satisfy the requirements specified.

Table 3-2. Additional Isolation Layout Rules

Rule	Class	Notes	Description		Des Min.	Waf. Dim.	Tol.
RX3	a	¹	RX to DT (RX touching DT not allowed).	≥	0.240	0.265	0.070
CPRX4	c	-	RX is within (DS or (NS not touching (NW intersect ESDUMMY)).	≥	0.000	1.4975	0.281
RX5	a	-	((RX within RN) not touching JD) must be covered by (NS or DS).				
RX8b	a	²	BF(not touching NW) to adj NW to insure BF-BF space.	≥	0.92	-	-
RX8c	a	²	BF(touching NW) to adj {NW(not over NWASP)} to insure BF-BF space.	≥	0.92	-	-
RX8d	a	²	BF(touching NW(touching NWASP)) to adjacent NW; to insure BF-BF space.	≥	0.70		
RX13	c	³	RX(touching NSR, touching RN, touching NS(not touching PB)) to RX(touching NSR, touching RN, touching NS(not touching PB)) (NS res min length touching the same NSR).	≥	2.600	2.645	0.040
RX17a	b	⁴	RX(touching RN, not touching JD) must be covered by BB.				
RX19	b	⁵	Distinct {NW, NSR, NS, DS} within a common {BB,BF} must be isolated from each other with a DT fence(within {BB, BF}) around each RX shape=> for trench.				
RX22	b	-	RX(over BB, over NW, not over {PC, PB, VPNP}) must be covered by {PD,RN}) } to make sure the silicon gets doped.				
RX23	b	⁶	RX(over BB, not over NW, not over VPNP, not over IND_FILT, not over {PC,PB}) must be covered by RN.				
RX23a	b	-	RX(over BB, not over NW, over VPNP) must be covered by BPHOLE.				
RX27	b	-	RX(over PB, touching CEBAR) must be covered by (BX over PX).				
RX27a	b		RX(over PB, touching CABAR) must be covered by OZ.				
RX29	b	-	(RX not over OZ) straddling PB not allowed.				
RX29a	b	-	(RX over OZ) must be covered by {PD, (DEGEN union PB)}.				

1. See rule BB8, RX3 for how to design the BB and DT shapes with respect to enclosing the RX with a DTfence and covering it with BB. BB8, RX3 applies if DT isolation is being used.
2. These rules are to check shapes internally generated in the DRC deck as defined in Table 2-6.
3. NSR is a dummy design level touching NS resistors to aid in DRC checking and to distinguish NS resistors from NS isolation beds. See Dummy Design Level NS in Table 2-4 on page 36.
4. See also Rule JD12a for the complement of this check.
5. See rule NS15a, NS15b.
6. RX used as FILL within the DTLATTICE is exempt from this rule.

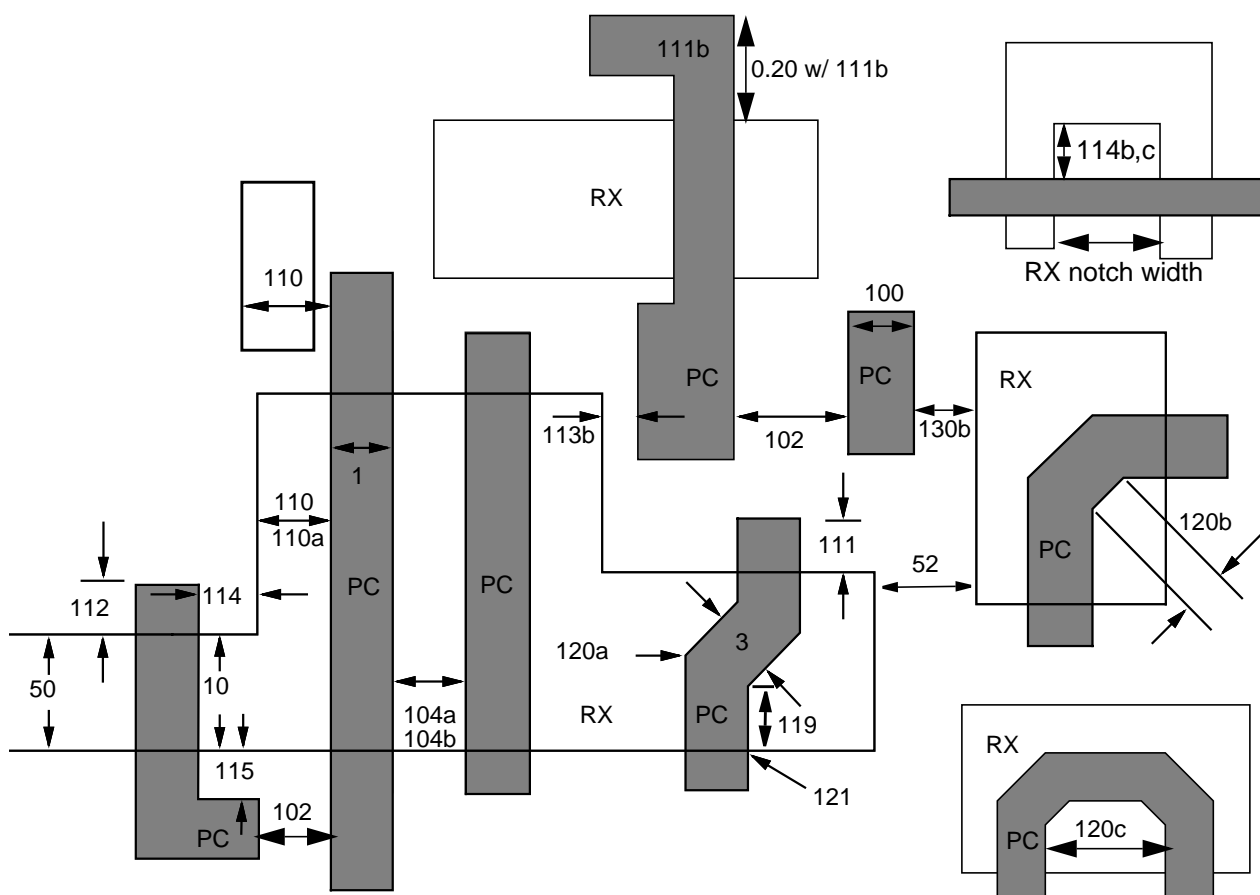


Figure 3-1. Isolation and Polysilicon Rules

3.1.1 Antenna Rules

3.1.1.1 Definitions

- A floating gate device is any device where the PC (poly) shape
 - touches RX (diffusion) and

- is NOT electrically connected to RX
- The PC over RX area is defined as the gate oxide area.
- For each PC shape intersecting RX, the poly antenna ratio is defined as the ratio of the total PC area to the gate oxide area.
- The metal antenna ratio is defined as the ratio of the metal area to the gate oxide area to which it is connected at any level at which the gate has not yet been electrically connected to RX. Example: For gate not electrically connected to RX at M2 (nor at M1), the M1 and M2 antenna ratios would be the M1 and M2 area, respectively, divided by the gate oxide area of the gate to which the M1 and M2 are connected.
- The antenna ratio defined is for individual level, not cumulative.
- A valid tiedown RX diffusion is defined as (RX not touching ((BFMOAT or BB or RN or BX or JD or ((NW not touching PI) which is not tied down (see rule 134 or rule DT267)) or (PI which is not tied down (see rule TW134)) or IND_FILT). The following is a list of the valid tiedown devices: NFET source/drain (including thick oxide version), N+ Diffused resistor, N+ junction in the substrate, Thin or Thick Triple Well NFET source/drain in a tied down well (see rule TW134), PFET source/drain (including thick oxide versions), P+ junction in a tied down NWell and substrate contact. Note: PFET pass-through not allowed for tie-down net connectivity ((PC intersect RX) forming a gate breaks the net connectivity) not allowed).
- For diffused resistors with an aspect ratio (OP intersect RX) greater than or equal to 100:1, only the contact area (RX not over OP) which is part of the net is a valid tiedown.
- The connectivity net definition allows pass through for resistors which have an (OP intersect (RX or PC)) aspect ratio of less than 100:1. This limits the resistance of pass through resistors.

3.1.1.2 Rules

- These rules are intended to avoid gate oxide integrity degradation by polysilicon charging. See Rules 130a, 130c, 131, 131a, 131b and 131f.

3.1.1.3 Recommendations

- It is recommended that all PC touching RX be connected to RX (N⁺ or P⁺ diffusion) by M1.
- Circuits whose operation is critically dependent on threshold voltage control or matching should not have antennae without a diode clamp. The diode area need to follow R131-R134.

3.2 Contact (CA, CABAR) Layout Rules

Table 3-3. CA, CABAR Layout Rules

Rule	Class	Notes	Description		Des Min.	Waf. Dim.	Tol.
200	a	-	CA width; CA length.	≡	0.16	0.1750	0.025
201	b	-	CA must be rectangular and not at 45°.	≡	-	-	-
203	a	1	CA to CA space.	≥	0.24	0.1840	0.047
203b	a	-	CA to CA space, for common run lengths ≤ 0μm, corner to corner spacing.	≥	0.20	0.1440	0.047
204	b	-	CA within RX.	≥	0.06	0.0300	0.088
204R	d	2	CA within RX.	≥	0.14	0.1175	0.088
204a	b	-	CABAR within RX.	≥	0.20	0.1775	0.094
207	b	3	CA (over RX) to adjacent PC; for PC width < 0.13μm.	≥	0.10	0.0825	0.065
207a	b	-	CA(over RX) to adj PB.	≥	0.36	0.3030	0.159
207b	b	-	CA (over RX) to adjacent PC, when (0.13 ≤ PC width < 0.18μm).	≥	0.12	-	-
207c	b	-	CA (over RX) to adjacent PC, when PC width is ≥ 0.18μm.	≥	0.14	-	-
207R	d	-	CA (over RX) to adjacent PC - Recommended.	≥	0.14	-	-
208	c	-	(CA over {PC, PB}) to adjacent RX.	≥	0.11	0.1325	0.089
208a	c	-	(CABAR over {PC, PB}) to adj RX.	≥	0.20	0.2225	0.094
209	b	3	CA within PC.	≥	0.02	0.0020	0.062
209R	d	-	CA within PC - Recommended for no CA etch into PC spacer. (CA landed on PC).	≥	0.09	0.0720	0.062
209a	b	-	CABAR within PC.	≥	0.16	0.1495	0.070
209b	b	-	CA within PB.	≥	0.24	0.2325	0.158
209c	b	-	CABAR within PB.	≥	0.30	0.3000	0.161

Table 3-3. CA, CABAR Layout Rules

Rule	Notes	Description		Des Min.	Waf. Dim.	Tol.
	c l a s s					
211	c	-	{CA, CABAR} (not over {BX, (PD over OZ), EV}) over ({PC, PB} intersect RX) not allowed. (No {CA, CABAR} over thin gate oxide).	≡	-	-
212	c	-	{CA, CABAR} must be within RX or PC or PB (must satisfy rule 204 or 204a or 209 or 209a or 209b or 209c).	≡	-	-
214	a	-	Maximum percent (%) union (CA, CABAR, CEBAR) permitted over a 25μm x 25μm localized area stepped in 12.5μm increments.	≤	16	-
214R	d	-	Maximum percent (%) union (CA, CABAR, CEBAR) permitted over a 25μm x 25μm localized area stepped in 12.5μm increments.	≤	10	-
220	a	⁴	CABAR width (exact).	≡	0.200	0.200
221	b	-	CABAR length (rectangles only).	≥	0.600	0.600
222	c	-	Maximum CABAR length (except Guard Ring).	≤	5.00	-
223a	a	-	CABAR to CABAR (touching not allowed).	≥	0.360	0.319
223b	a	-	CABAR to CABAR (touching not allowed) -- common run > 2.50μm.	≥	0.520	0.479
223c	a	-	CABAR to CA space (CA must not touch CABAR)(Neither full nor partial overlap is allowed).	≥	0.280	0.232
225	b	-	CABAR(over RX) to adjacent PC(where the CABAR does not intersect the PC).	≥	0.240	0.201
225a	b	-	CABAR(over RX) to adjacent PB(where the CABAR does not intersect the PB).	≥	0.400	0.351
225R	d	-	CABAR to adj {PC,PB} for common run > 2.5μm(where the CABAR does not intersect the {PC,PB}).	≥	0.520	-
228	c	-	CABAR not over (bipolar transistor collector {RX(over RN, over ((NS or DS) touching EX)}), or the NS resistor ((RX over RN) over NSR), or chip guard ring (RX over GUARDRNG), or (Vertical PNP collector (PD over OZ)), or Vertical PNP emitter (EV over PB)) is prohibited.			

Table 3-3. CA, CABAR Layout Rules

Rule	Class	Notes	Description		Des Min.	Waf. Dim.	Tol.
232	a	-	((Union [CABAR,CEBAR]) not touching LOGOBND) density % (maximum) over local 25um x 25um areas, stepped in 12.5um increments, across the chip.	≤	12	-	-
CA6	b	-	CA to NP space (CA cannot touch NP)	≥	0.410	0.382	0.224
CA7	b	-	CABAR to NP space (CABAR cannot touch NP, use CEBAR instead).	≥	0.530	0.510	0.230
CA7R	d	-	CABAR to NP space for common run > 2.5μm.	≥	0.930	0.910	0.230

1. The wafer value for this rule is measured at the top of CA.
2. IBM recommends following Rule 204R to prevent border leakage.
3. CA resistance tolerance depends on PC to CA distance and CA within PC, see Table 4-29, "Contact Resistance," on page 283 and Table 4-30, "Via Resistance," on page 283.
4. CABAR can be used for wiring. See Rule 228 for CABAR use and Rule 990d for CABAR within the Chip Guard Ring.

3.3 N-well, Contact, Junction Layout Rules

Table 3-4. N-well, Contact, Junction Layout Rules

Rule	Class	Notes	Description		Des Min.	Waf. Dim.	Tol.
250	a	-	NW ¹ width.	≥	0.68	0.68	0.208
250a	c	-	NW shapes must be orthogonal.	≡	-	-	-
252a	b	2	NW to NW space.	≥	0.92	0.92	0.208
252b	a	-	NW to NW space - for same potential wells ³ ; this usage is restricted to <i>unbended</i> common run lengths ≥ 0.68μm (Rule 250).	≥	0.70	0.000	0.208
252c	b	-	RX shapes are not allowed between NW shapes that are spaced less than 0.92 μm apart.	≡	-	-	-
252dR	d	-	NW-NW space for area >300 μm ² and NW width >6.0μm	≥	1.48	-	-
260	b	4	RX P ⁺ Junction ^{4,5} within NW	≥	0.30	0.3825	0.099
260aR	d	-	RX P ⁺ Junction ⁵ within NW for [NW width ≥ 18.0μm and ((not NW) width ≥ 18.0μm)]	≥	0.52	-	-
CP260	c	-	RX P ⁺ jct ⁵ (not touching NW) must be bordered by a DT fence within the BB (for DT isolation) or be within BB on the unbordered side (for junction isolation) by.	≥	1.280	1.2425	0.112
CP260b	b	-	((RX touching RN) not over JD) must be bordered by a DT fence within the BB (for DT isolation) or be within BB on the unbordered side (for junction isolation) by.	≥	1.280	1.2425	0.112
CP260c	c	-	(RX not touching RN) N contact must be bordered by a DT fence within the BB (for DT isolation) or be within BB on the unbordered side (for junction isolation).	≥	1.280	1.2425	0.112
261	b	-	RX N-well Contact overlap of NW, when overlap area is <0.13μm ² .	≥	0.33	0.5275	0.130
261f	b	-	RX N-well Contact overlap of NW, when overlap area is ≥ 0.13μm ² .	≥	0.20	0.3975	0.130

Table 3-4. N-well, Contact, Junction Layout Rules

Rule	Class	Notes	Description		Des Min.	Waf. Dim.	Tol.
262	b	-	RX N-well Contact overlap area with NW (μm^2)	\geq	0.076	-	-
265	b	-	RX N ⁺ Junction ⁵ to adjacent NW (where the RX does not intersect the NW).	\geq	0.30	0.2625	0.099
265aR	d	-	RX N+ Junction ⁵ to adjacent NW for (NW width $\geq 18.0\mu\text{m}$).	\geq	0.52	-	-
266	b	-	RX Substrate Contact to NW - High resistance contact.	\geq	0.06	0.0225	0.099
266R	d	-	RX Substrate Contact to NW - Recommended for low resistance contact.	\geq	0.20	0.1625	0.099
267R	d	⁶	All PMOS transistor N-wells(enclosed by DT) and thin gateox backplates (enclosed by DT) must be tied to an N+ S/D diffusion in the pwell substrate by the time M1 processing is complete. (See Rule 134).				
DT267R	d	⁶	<p>Every ((NW not DT) touching (PC over RX)) (including Nfet-in-Nwell MOS varactors) which are fully bordered by DT must satisfy either:</p> <ul style="list-style-type: none"> — there is a p+ diffusion in the Nwell that is connected to a valid S/D (n+ diode) diffusion or Nwell contact as defined by RX not touching {NW, PI, JD, BFMOAT, BB, RN, BX or ((NW not DT) shapes which are covered by a DTHole)}. — there is a n+ Nwell contact connected to a valid S/D (n+ diode) diffusion or NW contact, as defined by RX not touching {NW, PI, JD, BFMOAT, BB, RN, BX or ((NW not DT) shapes which are covered by a DTHole)} (Note: RX straddling DT(touching NW) is not allowed to satisfy this rule per Rule RX3). <p>by the time M1 level is complete (See Rule 134).</p>				
268	b	⁷	(RX P ⁺ Junction in (NW not DT) well to RX N-well Contact in the same (NW not DT) for no latchup. (Each (NW not over DT) with a P ⁺ Junction must have an N-well contact in that (NW not over DT)).	\leq	38.12	-	-
268b	b	^{8,9,10}	RX N+ Junction to substrate contact(not touching {DT,BB, BFMOAT,JD})	\leq	38.12	-	-
268g	b	-	{ (NW not touching VPNP), BB, BF} donut or DT (which encloses a P+ junction AND a N+ junction) must enclose a substrate contact (latchup concerns).				

Table 3-4. N-well, Contact, Junction Layout Rules

Rule	Class	Notes	Description		Des Min.	Waf. Dim.	Tol.
269	c	-	(PC over RX where RX straddles NW) to NW	\geq	0.50	-	-
269a	c	-	RX N+ junction overlap past (NW not over GRLOGIC) (for valid NW tiedown N+ junction).	\geq	0.50	-	-
NW2	c	-	NW intersect DT.	\geq	0.280	0.2600	0.117
NW2aR	d	-	NW overlap of DT.	\equiv	0.520	0.5000	0.117
NW3	a	-	NW to adjacent DT (keep NW from adj. device)	\geq	0.840	0.6400	0.117
NW3a	c	-	DT touching NW must completely cover NW(not covered by PI) edges.				
NW4	a	-	NW to adjacent (BB not over OZ) (for BF(from NW)- BB space and BH-BH generation purposes).	\geq	1.760	1.760	0.075
NW4a	a	-	NW to adjacent (BB touching OZ).	\geq	1.76	1.76	0.075

1. It is *strongly recommended* that shapes on levels involving pre-mask data preparation (DPREP) *difference* functions be placed at the same cell nesting hierarchy in the design data. Examples of these levels are NW and DG; see Data preparation section.
2. The 2 NWells will be merged for NW space $\leq 0.9\mu\text{m}$.
3. The dummy level NWASP must be placed over (and fully covering) adjacent NW shapes at the same potential; place these shapes at the lowest level of nesting possible for design rule checking. N-well regions using this rule may be electrically shorted together; hence, RX shapes are not allowed between NW shapes spaced less than the value of Rule 252a apart.
4. P+ Junction refers to the RX diffusion over BP and over NW.
5. N+ and P+ Junctions in these rules must include the gate area (RX) under the PC for these rules.
6. This rule has been replaced by Rule 134.
7. See Section 3.36 , "Latchup Guidelines, Layout Constraints, and Rules" on page 221. NW to be expanded in this rule by +0.46 per edge to achieve what the recommended figure intends
8. In case of large N+ diffusions, one requires to measure from the farthest N+ RX edge to the RX substrate contact.
9. See Rule TW268b for Triple Well NFET device and Rule TW268c for Thick Ox Triple Well NFET device.
10. RX N+ junction for Rule 268b is defined as RX not over {NW, BP, BB, JD, BFMOAT, PB}. {NW, BFMOAT, BB, DT, JD} are blocking shapes.

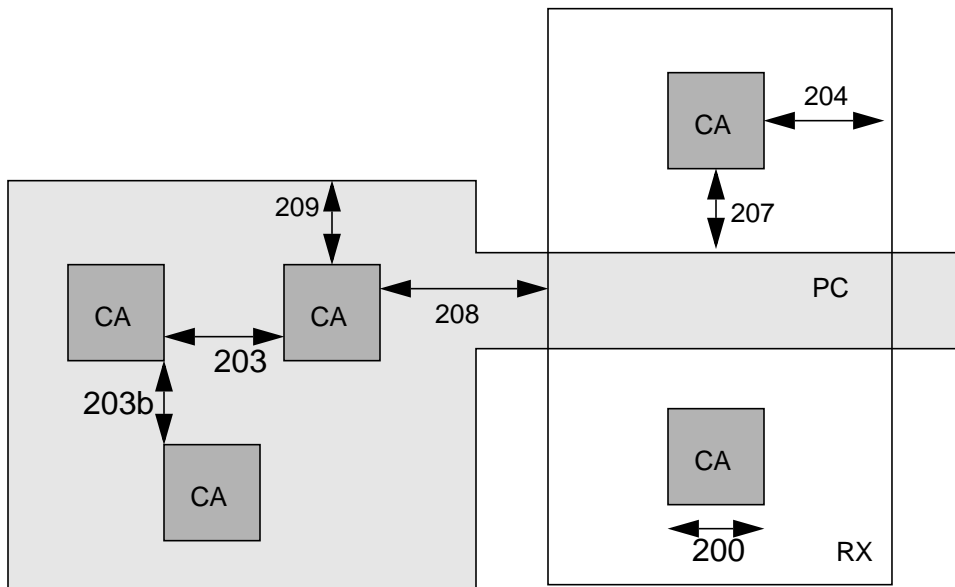


Figure 3-2. CA Rules



Figure 3-3. Rule to Avoid Latchup

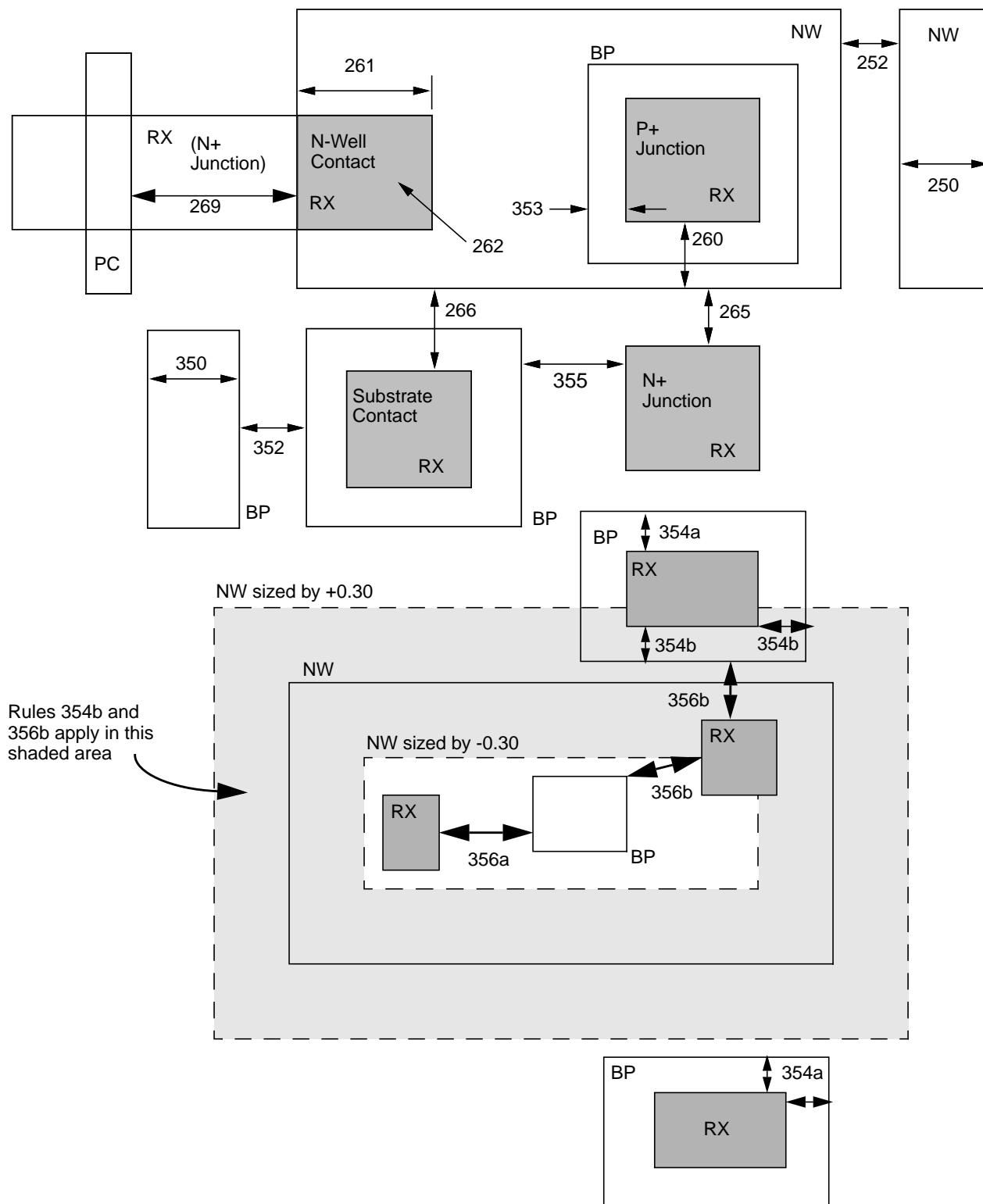


Figure 3-4. N-well, Contact, Junction Rules

Table 3-5. Additional N-well and Junction Layout Rules

Rule	Class	Notes	Description		Des. Min.	Wafer	Tol.
NWASP1	b	¹	NW shapes within NWASP (Adjacent NW(at the same potential) must be within the same NWASP net to use Rule 252b).	\geq	0.000	-	-
265b	b	-	RX N+ Junction ² to adjacent NS(where the RX does not touch the NS)(different net).	\geq	2.320	0.8500	0.281
DS265b	b	-	RX N+ Junction ² to adjacent DS(where the RX does not touch the DS)(different net).	\geq	3.000	1.5300	0.281
JD265bR	d	-	RX N+ Junction ² to adjacent JD(where the RX does not touch the JD)(different net) (see Rule JD6).	\geq	3.000	2.9550	0.251
CP265b	b	-	RX N+ jct ² to adj BB (Where the RX does not intersect the BB)(different net).	\geq	0.420	-	-
266b	b	-	RX(touching BP) Sub Contact to NS (touching not allowed).	\geq	2.080	-	-
DS266b	b	-	RX(touching BP) Sub Contact to DS (touching not allowed).	\geq	3.000	-	-
CP266c	b	-	RX(touching BP) P contact to BB	\geq	0.400	-	-
BB268	b	-	Maximum ((RX over PD) not touching IND_FILT) P+ jct in (BB(not touching NW) not over DT) well to RX(touching RN,touching BB) contact in the same (BB(not touching NW) not over DT) for no latchup. (Each (BB(not touching NW) not over DT) well with a P+ jct must have a RX(touching RN) contact in that (BB(not touching NW) not over DT)).	\leq	38.00	-	-
268dR	d	-	Maximum BB(not touching NW) well to P well Substrate Contact.	\leq	38.00	-	-
268eR	d	³	Maximum NW well to P well Substrate Contact.	\leq	38.00	-	-
JD268eR	d	⁴	Maximum JD well to P well Substrate Contact.	\leq	38.00	-	-

Table 3-5. Additional N-well and Junction Layout Rules

Rule	Class	Notes	Description		Des. Min.	Wafer	Tol.
268gR	d	-	JD donut or DT(which encloses a P+ junction AND a N+ junction) must enclose a substrate contact (latchup concerns) (covered by Rule JD15)				
NW8	b	5	Distinct NW shapes(within a common BB) must be isolated from each other with DTfences around each NW shape to keep them from shorting together through the N-epi well created by the BB.				

1. See also Rule 252b in Table 3-4 and the note requirement specified.
2. N+ and P+ Junctions in these rules must include the gate area (RX) under the PC for these rules.
3. Recommended rule to avoid the N+ jct(the Nwell) in the Pwell becoming forward biased.
4. Recommended rule to avoid the N+ jct(the Nwell) in the JD well becoming forward biased.
5. The Designer must either make 1 (one) NW(within common BB) shape, or put DT isolation around each NW(within common BB).

3.4 Threshold Voltage Rules

Table 3-6. VTSENS (Threshold Voltage) Layout Rules

Rule	Class	Notes	Description		Des Min.	Waf. Dim.	Tol.
VTSENS00	c	-	(RX intersect PC) within VTSENS.	≥	0.00	-	-
VTSENS01	c	-	((PC intersect RX) over VTSENS) to {NW, BB, BFMOAT, JD}.	≥	3.00	-	-
VTSENS01a	c	-	((PC intersect RX) over VTSENS) to ESDIODE.	≥	3.10	-	-
VTSENS02	c	-	((((PC intersect RX) over BP) over VTSENS) within {NW, BB, BFMOAT, JD, PI}.	≥	2.30	-	-
VTSENS03	c	-	((PC intersect RX) over VTSENS) to PI.	≥	4.10	-	-

3.5 BP Layout Rules

Table 3-7. BP Layout Rules

Rule	Class	Notes	Description		Des Min.	Waf. Dim.	Tol.
350	a	-	BP Width.	≥	0.24	0.2400	0.075
351a	a	-	BP area (μm^2).	≥	0.197	-	-
351b	a	-	BP enclosed area (μm^2).	≥	0.197	-	-
352	a	-	BP to BP space.	≥	0.24	0.240	0.075
353R	d	-	RX P ⁺ Junction ¹ within {BP, BB}.	≥	0.14	0.1625	0.095
353	b	-	RX P ⁺ Junction ¹ within {BP, BB}.	≥	0.12	0.1425	0.095
354a	b	2	[RX Substrate Contact not over (NW sized by +0.30)] within BP.	≥	0.00	0.0225	0.095
354bR	d	-	[RX Substrate Contact over (NW sized by +0.30)] within BP.	≥	0.14	0.1625	0.095
354b	b	-	[RX Substrate Contact over (NW sized by +0.30)] within BP.	≥	0.12	-	-
355R	d	-	RX N ⁺ Junction to adjacent BP.	≥	0.14	0.1625	0.095
355	b	-	RX N ⁺ Junction to adjacent BP.	≥	0.12	-	-
356a	b	3	[RX N-well Contact over (NW sized by -0.30)] to BP.	≥	0.00	0.0225	0.095
356bR	d	-	[RX N-well Contact not over (NW sized by -0.30)] to BP.	≥	0.14	0.1625	0.095
356b	b	-	[RX N-well Contact not over (NW sized by -0.30)] to BP.	≥	0.12	-	-
357	b	4	BH to {NW, BB}.	≥	0.40	0.40	0.075
357a	a	4	BH width(for the BH mask).	≥	0.40	0.40	0.075
357b	a	4	BH to BH space(for BH mask).	≥	0.40	0.40	0.075
357b2	a	4	BH to VAR, DG, JD, EFUSE.	≥	0.40	0.40	0.075
357b3	a	4	BH to PC(touching OP, over RR).	≥	0.52	0.52	0.075

Table 3-7. BP Layout Rules

Rule	Class	Notes	Description		Des Min.	Waf. Dim.	Tol.
358b	a	4	PH width(for the PH mask).	≥	0.40	0.40	0.075
358c	a	4	PH space(for the PH mask).	≥	0.40	0.40	0.075
358d	a	4	BN width(for the BN mask).	≥	0.24	0.24	0.075
358e	a	4	BN to BN space(for the BN mask).	≥	0.24	0.24	0.075
358f	a	-	{BN ⁴ ,PD} to {BN ⁴ ,PD} (for generation of BN mask).	≥	0.24	0.24	0.075
358g	a	-	BP to PD (for generation of BN mask).	≥	0.24	0.24	0.075
358h	a	4	BF width (for the BF mask).	≥	0.68	0.68	0.122
358h1	a	4	((BF to BF space) not over NWASP).	≥	0.92	0.92	0.122
358h2	a	4	(BF to BF) over NWASP, including notch.	≥	0.70	-	-
358h3	a	4	BF notch.	≥	0.70	-	-
358j	a	4	DE width.	≥	0.40	0.40	0.075
358k	a	4	DE space.	≥	0.40	0.40	0.075
358m	a	4	DF width.	≥	0.40	0.40	0.075
358n	a	4	DF space.	≥	0.40	0.40	0.075
358p	a	4	BT width.	≥	1.00	1.00	0.122
358q	a	4	BT space.	≥	1.00	1.00	0.122
358r	a	4	DW width.	≥	0.40	0.40	0.075
358s	a	4	DW space.	≥	0.40	0.40	0.075
358t	a	4	VI width.	≥	0.80	0.8000	0.080
358u	a	4	VI space.	≥	0.80	0.8000	0.080
358v	a	5	PY width.	≥	1.520	1.2700	0.339
358w	a	5	PY space.	≥	1.520	1.7700	0.339
358x	a	4	DY minimum width.	≥	1.04	1.04	0.120
358y	a	4	DY minimum space.	≥	1.04	1.04	0.120
358z	a	4	DY minimum area (μm ²).	≥	2.04	2.04	-

Table 3-7. BP Layout Rules

Rule	Class	Notes	Description		Des Min.	Waf. Dim.	Tol.
359a	a	4	PF minimum width.	\geq	0.98	0.98	0.075
359b	a	4	PF minimum space.	\geq	1.00	1.00	0.075
359c	a	4	PQ minimum width.	\geq	0.68	0.68	0.100
359d	a	4	PQ minimum space.	\geq	1.52	1.52	0.100
359e	a	6	(PQ not over PF) touching {PC, RX} is prohibited.	=	-	-	-
370	b	7	(PC over RX) to BP for no P ⁺ in NFET gate (for NFET fully open to N ⁺ implant).	\geq	0.25	0.2550	0.095
370a	b	-	(PC over RX) to BB (for NFET fully open to N ⁺ implant).	\geq	0.50	-	-
370b	b	-	(PC over RX) to PD (for NFET fully blocked from P ⁺ implant). (PC over RX) touching PD not allowed.	\geq	0.50	-	-
371	b	8	(PC over RX) within BP for no N ⁺ in PFET gate.	\geq	0.25	0.2550	0.095
BP3	-	-	Rule Deleted				

1. If a violation occurs where the RX is not fully within BP, then the Butted Junction rules apply. See Table 3-9, "CA, M1 Metal and Via Layout Rules," on page 96.
2. This rule does not need to be checked. When "RX within BP" < 0, butted junction rules apply. This rule clarifies that the coincidence of BP and RX are allowed when Rule 354b does not apply.
3. This rule does not need to be checked. When "RX to BP" < 0, butted junction rules apply. This rule clarifies that the coincidence of BP and RX are allowed when Rule 356b does not apply.
4. These rules are to check shapes internally generated in the DRC deck as defined in Table 2-6.
5. Not required to be checked in DRC.
6. The PF, PQ shapes in this rule are the shapes internally generated in the DRC deck, as defined in Table 2-6, being verified to the drawn PC or RX shapes in the actual design layout. The intent of this rule is to prevent certain RN to RN, RN to PB, or PB to PB spacings in the indeterminate range of 1.01um through 1.51um spacings during PF, PQ algorithm gap fill, where PQ mask level may be not over PF mask level, from touching any drawn RX or PC structures during manufacturing processing. However, IBM auto-generated PCFILL or RXFILL shapes are exempt from this requirement.
7. Exempt for BP edge of Butted Substrate Contact; see rule 378.
8. Exempt for BP edge of Butted N-well Contact; see rule 379. Space from butting BP inner edge of N-well contact to gate is given by rule 379.

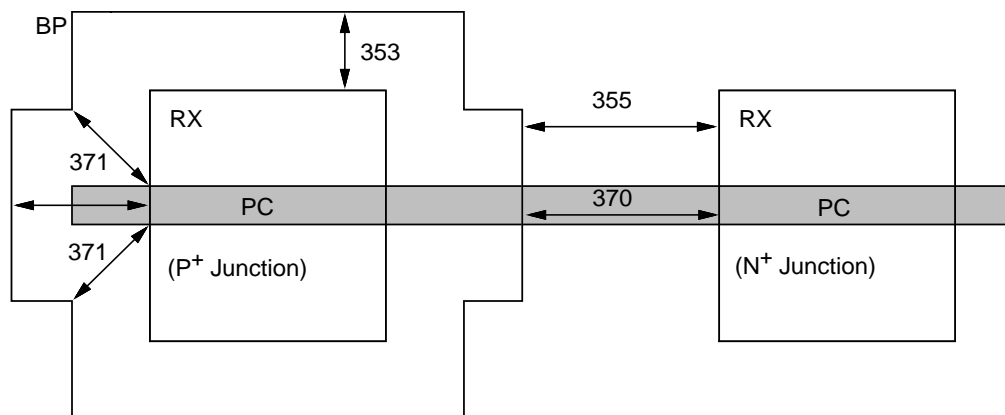


Figure 3-5. BP Rules

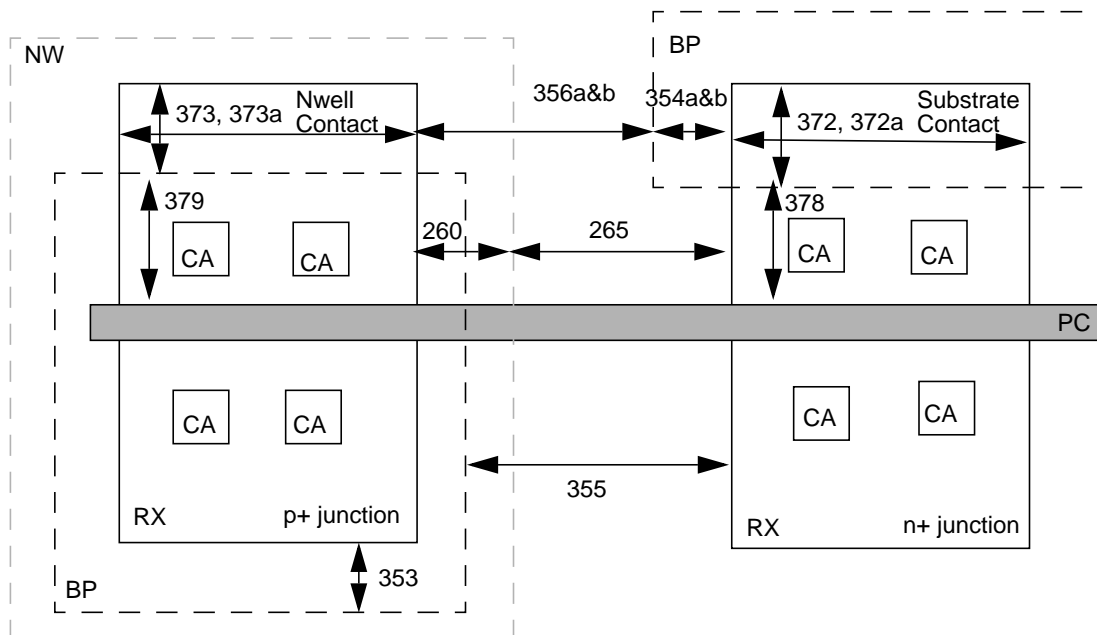
3.6 Butted Junction Layout Rules

Butted junctions are formed when BP intersects RX. This region will be either a N+ junction and a P+ substrate contact (if not over NW), or a P+ junction and a N-well contact (if over RX) within the same RX shape. In Figure 3-6, on page 94, Rules 260, 265, 353, 355 still apply outside the butted junction region. **A butted junction in close proximity to a FET can degrade the device. Therefore, the use of butted junction is not recommended in analog, matching, or performance-critical circuits.**

Figure 3-6. Butted Junction Rules

Table 3-8. Butted Junction Layout Rules

Rule	Class	Notes	Description		Des Min.	Waf. Dim.	Tol.
372	b	-	{BP(not touching BB)} overlap of RX (butted substrate contact).	\geq	0.18	0.1575	0.095
372a	b	-	BP overlap RX - area (μm^2); (butted substrate contact).	\geq	0.076	-	-
373	b	-	RX overlap past BP (butted n-well contact).	\geq	0.18	0.1575	0.095
373a	b	-	RX overlap past BP - area (μm^2); (butted n-well contact).	\geq	0.076	-	-
374	b	-	(RX not over BP) over (NW sized by $-0.08\mu\text{m}$) area (μm^2) (butted Nwell contact).	\geq	0.076	-	-
378	b	-	(BP intersect RX) to adjacent [(PC intersect RX) not within BP]. NFET gate to substrate contact space.	\geq	0.24	0.1824	0.111
379	b	-	(BP intersect RX) overlap past [(PC intersect RX) within BP]. PFET gate to n-well contact space.	\geq	0.24	0.1824	0.111



3.7 CA, Metals and Via Layout Rules

3.7.1 CA, M1 (Thin) Metal and Vx Via Rules

Table 3-9. CA, M1 Metal and Via Layout Rules							
Rule	Class	Notes	Description		Des Min.	Waf. Dim.	Tol.
500	a	-	M1 width (minimum).	\geq	0.16	0.160	0.045
500b	a	-	(M1 not over M1PLANE) width (maximum).	\leq	50.00	-	-
500c	a	-	(M1 width $> 50\mu\text{m}$) must be covered by M1PLANE.	\equiv	-	-	-
500dR	d		(M1 over M1PLANE) width (maximum) (μm).	\leq	2000.0	-	-
500e	b	-	(M1 width $\leq 50\mu\text{m}$) over M1PLANE not allowed.	\equiv	-	-	-
501a	b	-	M1 area (μm^2).	\geq	0.089	-	-
501b	a	-	M1 enclosed area (μm^2).	\geq	0.366	-	-
501cR	d	-	<p>(M1 not over M1PLANE) pass-through (feed-through) within or enclosed by (M1 over M1PLANE) (maximum)(μm^2)</p> <p>Note: M1 pass-through (feed-through) is defined as:</p> <ol style="list-style-type: none"> 1. (M1 not over M1PLANE) must have an area less than the Design Min specified, and 2. The V1 vias above are each enlarged by $0.10\mu\text{m}/\text{side}$, then unioned together, and the (M1 not over M1PLANE) shape initially contacted by the vias must be completely covered by the enlarged and unioned via set, and 3. (M1 not over M1PLANE) pass-through meets GR 504e spacing rule within (enclosed) by (M1 over M1PLANE). 	\leq	100.0	-	-
502	a	-	M1 to M1 space.	\geq	0.16	0.1448	0.045

Table 3-9. CA, M1 Metal and Via Layout Rules

Rule	Class	Notes	Description		Des Min.	Waf. Dim.	Tol.
504	b	-	M1 to M1 space ; (if at least one metal line is >1.76 μm wide).	\geq	0.26	-	-
504R	d	-	M1 to M1 space ; (if at least one metal line is >1.04 μm wide).	\geq	0.36	-	-
504b	b	-	M1 to M1 space ; (if at least one metal line is >8.0 μm wide) .	\geq	1.12	-	-
504c	b	-	M1 to M1 space ; (if at least one metal line is >25.0 μm wide).	\geq	1.92	-	-
504d	b	-	M1 to M1 space ; (if both metal lines are >4.0 μm wide).	\geq	0.36	-	-
504e	c	-	(M1 not over M1PLANE) to (M1 over M1PLANE) space.	\geq	10.000	-	-
504f	c	-	(M1 over M1PLANE) to (M1 over M1PLANE) space.	\geq	2.000	-	-
EPDL_M1_min	a	-	(m1_estimated) minimum density (%) for boxes which do not touch { IND_FILT, BONDPAD } over local 126 μm x 126 μm areas stepped in 63 μm increments across the chip, where m1_estimated is defined in Table H-4, “Estimated Pattern Density Rules” on page 427.	\geq	10	-	-
EPDLi_M1_min	a	-	(m1_estimated) minimum density (%) for boxes which touch {IND_FILT, BONDPAD} over local 126 μm x 126 μm areas stepped in 63 μm increments across the chip.	\geq	8	-	-
505a	b	-	CA must be within M1.	\geq	0.00	-0.0205	0.069
505a2	b	-	CABAR must be within M1.	\geq	0.04	0.020	0.074
505b1	b	-	CEBAR must be within M1.	\geq	0.130	0.1057	0.111
505c	b	-	{CA, CABAR, CEBAR} touching M1PLANE not allowed (use wires less than or equal to 50 μm to connect to devices).	\equiv	-	-	-
505dR	d	-	M1PLANE (over M1) in the chip guard ring not allowed (see Rule 505c).	\equiv	-	-	-
506a	b	-	M1 overlap past CA for at least 2 sides ¹ .	\geq	0.06	-0.0205	0.069

Table 3-9. CA, M1 Metal and Via Layout Rules

Rule	Class	Notes	Description		Des Min.	Waf. Dim.	Tol.
506aR	d	-	M1 overlap past CA for two opposite sides.	\geq	0.06	-0.0205	0.069
506ab	b	-	CA must be within M1 ¹ .	\geq	0.04	-0.0405	0.069
550	a	-	V1, V2, V3 width and length.	\equiv	0.20	0.230	0.050
551	b	-	A Via array is defined as any group of two or more Vx (x = 1,2,3) vias spaced $\leq 0.38\mu\text{m}$ apart.	\equiv	-	-	-
551a	b	2	If (Vx expanded by $+0.19\mu\text{m}$ then shrunk $-0.69\mu\text{m}$) ≥ 0.40 , space and notch to (Vx expanded by $+0.19\mu\text{m}$ then shrunk $-0.69\mu\text{m}$) where x=1,2,3. Four by n min pitch via arrays must be $\geq 0.60\mu\text{m}$ from any other via array.	\geq	1.60	-	-
551b	b	2	If (Vx expanded by $+0.19\mu\text{m}$ then shrunk $-0.69\mu\text{m}$) ≥ 0.80 , space and notch to (Vx expanded by $+0.19\mu\text{m}$ then shrunk $-0.69\mu\text{m}$) where x=1,2,3. Five by n min pitch via arrays must be $\geq 1.0\mu\text{m}$ from any other via array.	\geq	2.00	-	-
551c	b	2	If (Vx expanded by $+0.19\mu\text{m}$ then shrunk $-0.69\mu\text{m}$) = 1.20, space and notch to (Vx expanded by $+0.19\mu\text{m}$ then shrunk $-0.69\mu\text{m}$) where x=1,2,3. Six by n min pitch via arrays must be $\geq 1.4\mu\text{m}$ from any other via array.	\geq	2.40	-	-
551d	b	2	(Vx expanded by $+0.19\mu\text{m}$ then shrunk $-0.69\mu\text{m}$) maximum width, where x=1,2,3. Via arrays larger than six by n are not allowed.	\leq	1.20	-	-
553	a	-	Vx to Vx space where x=1,2,3.	\geq	0.20	0.17	0.050
553b	a	-	Vx minimum space for run length $> 0\mu\text{m}$, where x = 1,2,3 on different nets.	\geq	0.28	0.25	0.050
553c	-	-	Rule Deleted	\equiv	-	-	-
557	c	-	All Via shapes must be square or rectangular and not at 45° , except in chamfer required chip guard rings. Includes Vx, VxBAR, VL, VLBAR (x=1,2,3).	\equiv	-	-	-

Table 3-9. CA, M1 Metal and Via Layout Rules

Rule	Class	Notes	Description		Des Min.	Waf. Dim.	Tol.
557a	c	-	All VY and AV Via shapes must be square or rectangular and not at 45°, except in chamfer required chip guard rings. Includes VY, VYBAR, AV and AVBAR.	≡	-	-	-
558	c	-	V1BAR, V2BAR, V3BAR, VLBAR are ONLY permitted in the Chip Guard Ring. See Table 3-59, “Chip Guard Ring Layout Rules,” on page 205 for via bar dimensions.	≡	-	-	-
570	b	-	V1 must be within M1 ³ .	≥	-0.02	-0.0274	0.067
571	b	-	M1 overlap past V1 for at least 2 sides ³ .	≥	0.06	-0.0074	0.067
571aR	d	-	M1 overlap past V1 for two opposite sides.	≥	0.06	-0.0074	0.067
571b	b	-	V1 must be within M1 ³ .	≥	0.02	-0.0474	0.067
571c	b	-	V1 within (M1 over M1PLANE).	≥	0.16	0.0926	0.067
575	b	-	V1 must be within M2.	≥	0.00	-0.0639	0.099
575a	b	-	V1 within (M2 over M2PLANE).	≥	0.16	0.0961	0.099
594	a	4,5,6,7	For nets connected to NW contact, where the NW contact is not connected to a substrate contact defined as ((RX over BP) not over (NW or JD or PI or BB ⁸)), the ratio of [(20 * Mx area) + (p+ junction area (((RX over BP) not over PC) over NW))] / (union [NW,PI] area), where x = 1,2,3,4.	≥	0.20	-	-
595	a	4, 6, 7,9	For nets connected to ((RX over BP) over PI) (triple well pwell contact), the ratio of [(20 * Mx area) + (n+ junction area ((RX not over (BP or NW or JD or PC or BB)) over PI) area] / ((PI not over NW) area), where x = 1,2,3,4.	≥	0.20	-	-

1. Either rule 506ab OR (rule 505a + 506a) must be used.
2. All expand rules, which determine the boundaries of the via arrays, are in $\mu\text{m}/\text{edge}$ and are derived from: $(V_x \text{ expanded by } (V_x - 0.01\mu\text{m}))$, the generated shapes are unioned, then shrunk $((-3.5 \times V_x) + 0.01 \mu\text{m})$. The space and notch to any other V_x union (same expand and shrink as above) must be \geq groundrule defined width.
3. Either rule 571b OR (rule 570 + 571) must be used.
4. Only the current metal level is included in the metal area measurement.

5. Only (RX p+ junction not over PC) connected to (NW contact of the NW level in which the p+ junction resides) is included in the area measurement; any p+ junction not connected to the NW level in which it resides is ignored in the area measurement.
6. (NW not PI) and PI are conductors, so two different NW contacts in the same NW level or two different PI contacts in the same PI level are assumed to be shorted.
7. The connectivity net definition for these rules allows pass through for resistors which have an (OP intersect {RX or PC}) aspect ratio of less than 100 to 1. This limits the resistance of pass through resistors.
8. See also Rule BB35. In Rule 594, BB is included in the rule for completeness since verification of Rule BB35 is in a different tool than Rule 594 is verified in.
9. Only n+ junctions ((RX not over NW) not over PC) connected to (triple well contact of the isolated pwell in which the n+ junction resides) is included in the area measurement; any n+ junction not connected to the isolated pwell in which it resides is ignored in the area measurement.

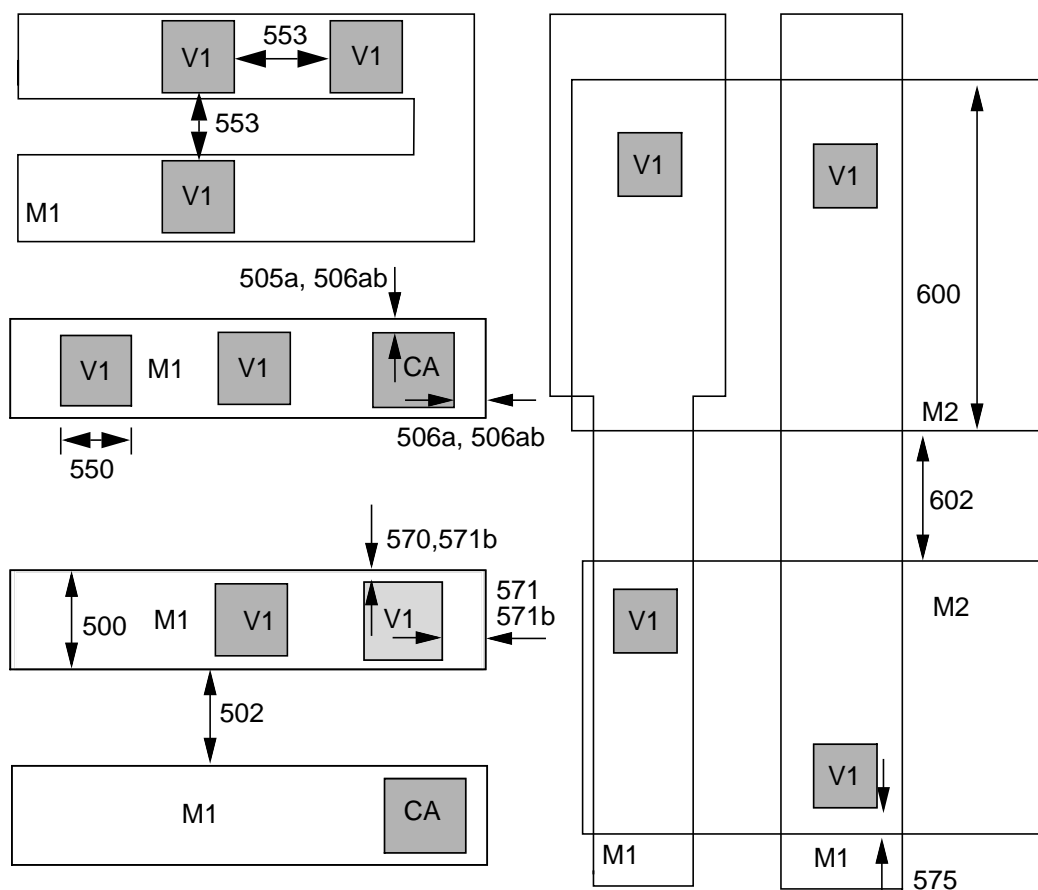


Figure 3-7. CA, Metal, Via Interconnect Rules

Clusters of min pitch Via arrays ≤ 0.38 apart will be unioned after expansion and treated as a larger array (generated light gray shaded shape) which is measured against the size in the first line of Rule 551a, Rule 551b, Rule 551c description (≥ 0.40 , ≥ 0.80 , $= 1.20$) OR the Design Min column in GR 551d.

Example: Three 2X8 arrays spaced exactly equal to 0.38 apart are treated as a 6X8 array wider than allowed by GR551d.

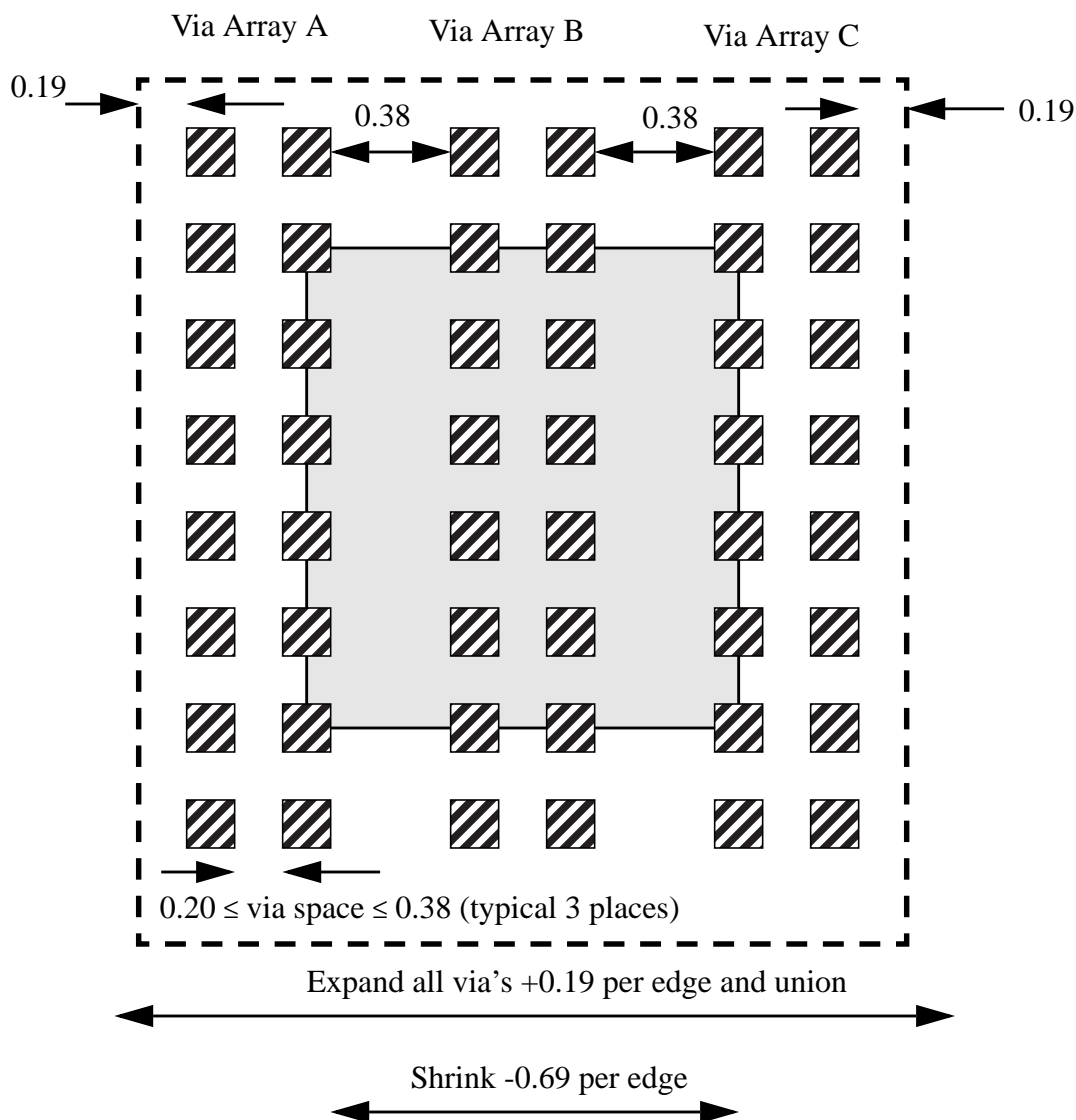


Figure 3-8. Example of 551d for 6x8 array Via Expansion, Union and Shrink

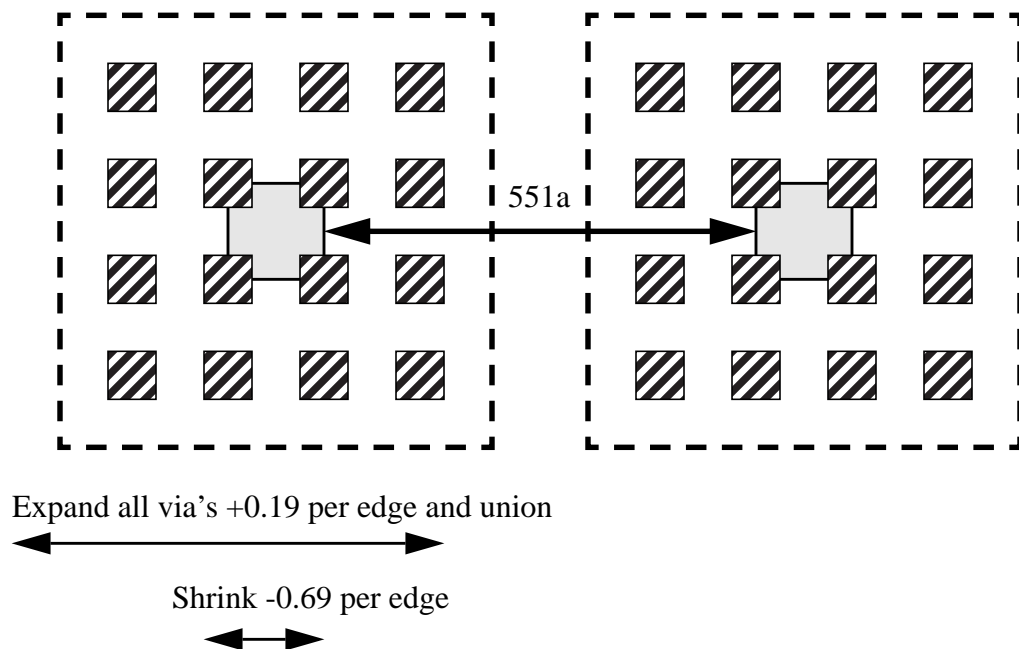


Figure 3-9. Example of 4xN Via Spacing array Rule

3.7.2 Mx (Thin) Metal, Interconnect and VL Via Rules

Table 3-10. Mx (x=2,3,4) Metal and Via Layout Rules

Rule	Class	Notes	Description		Des Min.	Waf. Dim.	Tol.
600	a	-	M2, M3, M4 width (minimum).	\geq	0.20	0.2000	0.060
600b	c	-	((M2, M3, M4) not over MxPLANE) width (maximum) (x=2,3,4).	\leq	50.00	-	-
600c	c	-	((Mx) width > 50 μ m) must be covered by MxPLANE (x=2,3,4).	\equiv	-	-	-
600dR	d	-	(Mx over MxPLANE) width (maximum) (μ m) (x=2,3,4).	\leq	2000.0	-	-
600e	c	-	(Mx width \leq 50 μ m) over MxPLANE not allowed (x=2,3,4).	\equiv	-	-	-
601a	a	-	M2, M3, M4 area (μ m ²).	\geq	0.120	-	-
601b	a	-	M2, M3, M4 enclosed area (μ m ²).	\geq	0.366	-	-
601cR	d	-	<p>(Mx not over MxPLANE) pass-through (feed-through) within or enclosed by (Mx over MxPLANE) (x=2,3,4) (maximum)(μm²)</p> <p>Note: Mx pass-through (feed-through) is defined as:</p> <ol style="list-style-type: none"> 1. (Mx not over MxPLANE) must have an area less than the Design Min specified, and 2. The ((Vx vias above are each enlarged by 0.10μm/side) or the (VL vias above are each enlarged by 0.20μm/side)) and the (Vx-1) vias below are each enlarged by 0.10μm/side, then unioned together, and the (Mx not over MxPLANE) shape initially contacted by the vias must be completely covered by the enlarged and unioned via sets, and 3. (Mx not over MxPLANE) pass-through meets GR 604e spacing rule within (enclosed by) (Mx over MxPLANE). 	\leq	100.0	-	-
602	a	-	M2 to M2, M3 to M3, M4 to M4 space (top to top).	\geq	0.20	0.1632	0.060

Table 3-10. Mx (x=2,3,4) Metal and Via Layout Rules

Rule	Class	Notes	Description		Des Min.	Waf. Dim.	Tol.
604	c	-	M2 to M2, M3 to M3, M4 to M4 space ; (if at least one metal line is >2.0μm wide).	≥	0.28	-	-
604R	d	-	M2 to M2, M3 to M3, M4 to M4 space ; (if at least one metal line is >1.0μm wide).	≥	0.36	-	-
604b	c	-	M2 to M2, M3 to M3, M4 to M4 space ; (if at least one metal line is > 8.0μm wide).	≥	1.12	-	-
604c	c	-	M2 to M2, M3 to M3, M4 to M4 space ; (if at least one metal line is > 25.0μm wide).	≥	1.92	-	-
604d	c	-	M2 to M2, M3 to M3, M4 to M4 space ; (if both metal lines are > 4.0μm wide).	≥	0.36	-	-
604e	c	-	(Mx not over MxPLANE) to (Mx over MxPLANE) space (x=2,3,4).	≥	10.000	-	-
604f	c	-	(Mx over MxPLANE) to (Mx over MxPLANE) space (x=2,3,4).	≥	2.000	-	-
605d	c	-	MxPLANE (over Mx) in the chip guard ring not allowed (x=2,3,4).	≡	-	-	-
EPDL_M2_min	a	-	(m2_estimated) minimum density (%) for boxes which do not touch { IND_FILT, BONDPAD } over local 126μm x 126μm areas stepped in 63μm increments across the chip, where m2_estimated is defined in Table H-4, “Estimated Pattern Density Rules” on page 427.	≥	10	-	-
EPDLi_M2_min	a	-	(m2_estimated) minimum density (%) for boxes which touch {IND_FILT, BONDPAD} over local 126μm x 126μm areas stepped in 63μm increments across the chip.	≥	8	-	-
EPDL_M3_min	a	-	(m3_estimated) minimum density (%) for boxes which do not touch { IND_FILT, BONDPAD } over local 126μm x 126μm areas stepped in 63μm increments across the chip, where m2_estimated is defined in Table H-4, “Estimated Pattern Density Rules” on page 427.	≥	10	-	-

Table 3-10. Mx (x=2,3,4) Metal and Via Layout Rules

Rule	Class	Notes	Description		Des Min.	Waf. Dim.	Tol.
EPDLi_M3_min	a	-	(m3_estimated) minimum density (%) for boxes which touch {IND_FILT, BONDPAD} over local 126μm x 126μm areas stepped in 63μm increments across the chip.	≥	8	-	-
EPDL_M4_min	a	-	(m4_estimated) minimum density (%) for boxes which do not touch { IND_FILT, BONDPAD } over local 126μm x 126μm areas stepped in 63μm increments across the chip, where m2_estimated is defined in Table H-4, “Estimated Pattern Density Rules” on page 427.	≥	10	-	-
EPDLi_M4_min	a	-	(m4_estimated) minimum density (%) for boxes which touch {IND_FILT, BONDPAD} over local 126μm x 126μm areas stepped in 63μm increments across the chip.	≥	8	-	-
609	b	1, 2	[(Mx width > 2.8μm) intersect M(x+1)] density must be ≤ 56% over local 200 x 200um areas, stepped in 100 μm increments (for Mx = M1, M2, M3, M4 and (for M(x+1) = M2, M3, M4, MQ).	≡	-	-	-
609R	d	1, 2	[(Mx width > 2.8μm) intersect M(x+1)] density must be ≤ 50% over local 200 x 200um areas, stepped in 100 μm increments (for Mx = M1, M2, M3, M4 and (for M(x+1) = M2, M3, M4, MQ).	≡	-	-	-
610	b	-	Vx must be within Mx, where x = 2,3.	≥	0.00	0.0034	0.078
610R	d	-	Vx must be within Mx, for two opposite sides, where x = 2,3.	≥	0.09	0.0934	0.078
610aR	-	-	Rule Deleted	≡	-	-	-
610a2	b	-	Vx within (Mx over MxPLANE), where x = 2,3.	≥	0.16	0.1634	0.078
611	b	-	V2 must be within M3, V3 must be within M4.	≥	0.00	-0.0839	0.105
611a	b	-	Vx within (M(x+1) over M(x+1)PLANE) (x=2,3)	≥	0.16	0.0761	0.105

Table 3-10. Mx (x=2,3,4) Metal and Via Layout Rules

Rule	Class	Notes	Description		Des Min.	Waf. Dim.	Tol.
612	c	3	At least 2 vias must connect metal below to metal above when metal width is $\geq 1.04\mu\text{m}$. For example, Mx to M(x+1) ⁴ when either Mx or M(x+1) $\geq 1.04\mu\text{m}$ wide. See Figure 3-10, “Redundant Via on Wide Line Rules (Mx=M1,M2,M3; M(x+1) = M2,M3,M4)” on page 107 for drawings of this rule’s use.	\equiv	-	-	-
612b	c	3	At least 3 vias must connect metal below to metal above when metal width is $\geq 1.4\mu\text{m}$.	\equiv	-	-	-
612c	c	3	At least 4 vias must connect metal below to metal above when metal width is $\geq 3.0\mu\text{m}$.	\equiv	-	-	-
620a	a	-	VL width.	\equiv	0.40	0.40	0.050
620b	a	-	VL length.	\equiv	0.40	0.40	0.050
622	a	-	VL to VL space.	\geq	0.40	0.40	0.050
622b	a	-	VL to VL space for common run length greater than $0\mu\text{m}$; vias on the same net are exempt.	\geq	0.56	0.3100	0.050
622c	-	-	Rule Deleted	\equiv	-	-	-
623a	b	-	VL must be within the Mx metal below ⁵ .	\geq	0.00	0.0284	0.083
623b	b	-	VL within the ((Mx metal below ⁵) over MxPLANE).	\geq	0.16	0.1884	0.083
624a	b	-	VL must be within MQ.	\geq	0.00	-0.0450	0.123
624b	b	-	VL within (MQ over MQPLANE).	\geq	0.16	0.1150	0.123

1. This local density requirement is calculated using the intersection of consecutive metal shapes over which the checking box is stepped. When the box steps over the chip boundary, the box is moved back in bounds. The metal density is calculated using design layout data prior to IBM design services MxHOLE or MxFILL.
2. This local density requirement limits the stacked metal pattern (directly above and below) using an intersection methodology for compatibility with available checking tools
3. As further clarification for Rule 612, 612b, 612c: Redundant Vx vias can exist in any (Mx over M(x+1)) intersection under evaluation as long as the redundant vias under consideration touch the wide metal intersection under consideration. To satisfy Rule 612, 612b, 612c, only one via has to touch the wide metal intersection under consideration, while the remaining redundant vias, spaced according to the note above and Figure 3-10, can be in any (Mx over M(x+1)) intersection, whether it is comprised of wide wires or thin wires, or any combination thereof, that touch (or abut) the initial wide metal intersection, to satisfy this rule. It is preferred that all vias are placed in the intersection where the wide metal is located, but it is not mandatory. See Figure 3-11 for one example layout.

4. M_x is metal below via and M_{x+1} is metal above the via.
5. See various BEOL metallization options under Table 2-7, “Back End Of Line (BEOL) Metallization Options,” on page 49.

Note on Redundant Via Rule 612

In order to avoid a reliability failure mechanism for opens, redundant vias are required on any V1, V2, V3 level that is used to electrically connect two metal levels (M_1, M_2, M_3, M_4) where either metal shape is greater than the wide metal criteria of Rule 612, 612b, 612c.

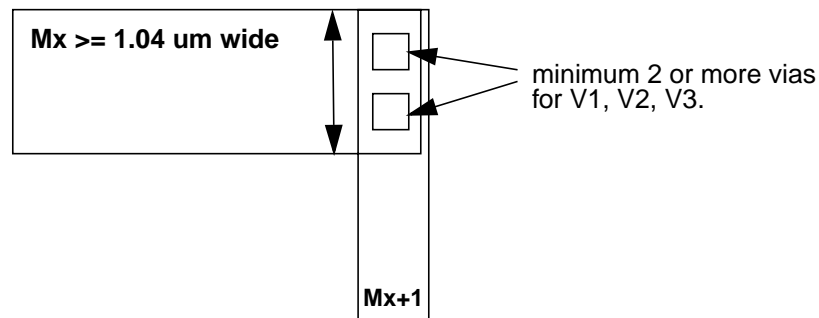


Figure 3-10. Redundant Via on Wide Line Rules ($M_x=M_1,M_2,M_3$; $M_{(x+1)} = M_2,M_3,M_4$)

One Example of Redundant Via Rule 612c:

The example layout shown in Figure 3-11 satisfies Rule 612c. This is just one example for reference.

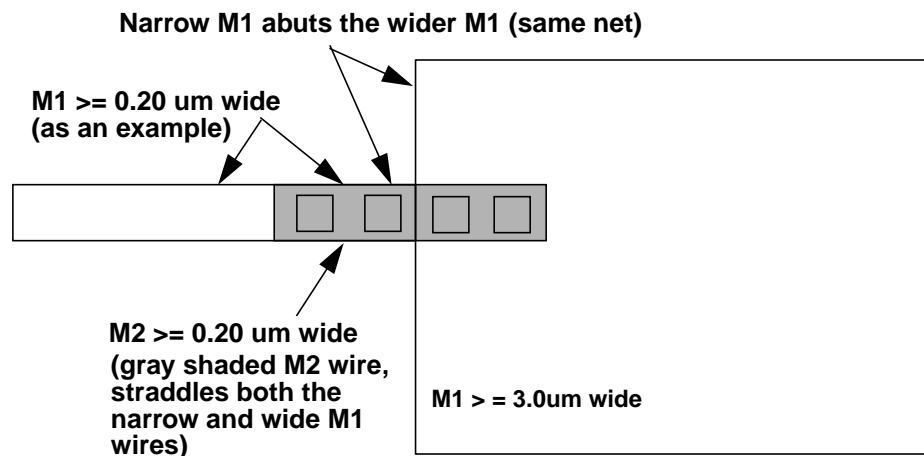


Figure 3-11. Redundant Via on Wide Line Rules ($x=1,2,3,4$)

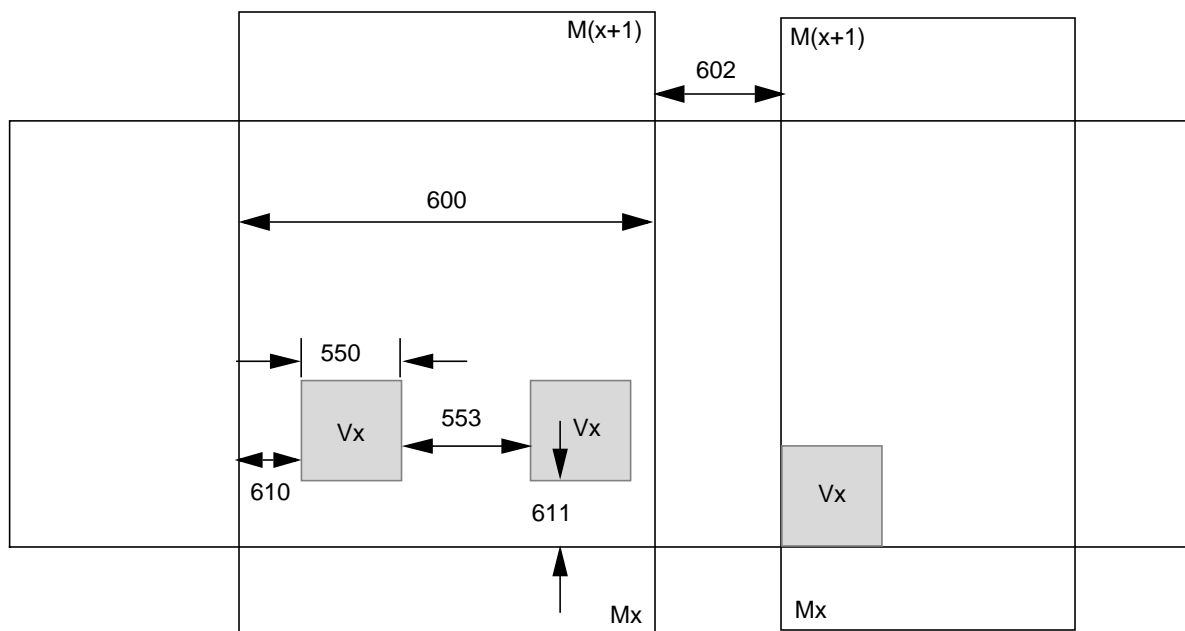


Figure 3-12. Thin Metal Interconnect Rules ($x=1,2,3$)

3.7.3 LV and DV Layout Rules

Table 3-11. DV and LV Layout Rules							
Rule	Class	Notes	Description		Des Min.	Waf. Dim.	Tol.
650a	b	-	LV width (wafer bias shown is for small LV).	≥	14.000	14.000	4.000
650b	a	-	DV width.	≥	14.000	14.000	5.500
651a	c	-	LV area (min. μm^2).	≥	550.00	-	-
651b	c	-	DV area (min. μm^2).	≥	480.00	-	-
653b	a	-	DV to DV space (wafer bias shown is for small DV).	≥	11.00	11.00	4.000
653c	a	-	LV to LV space (wafer bias shown is for small LV or LV.) (If C4s are used).	≥	29.000	29.000	5.500
BEOL1	b	-	Use LV for C4 builds Use DV for Wire Bond				
658c	a	-	DV within CHIPEDGE.	≥	20.000	-	-
658d	a	-	LV within CHIPEDGE (If C4s are used).	≥	29.000	-	-

3.7.4 MQ (Thick Metal) Layout Rules

Table 3-12. MQ (Thick Metal) Layout Rules							
Rule	Class	Notes	Description		Des Min.	Waf. Dim.	Tol.
690	a	-	MQ width (minimum)	≥	0.40	0.4000	0.09
690b	c	-	(MQ not over MQPLANE) width (maximum)	≤	50.0	50.0	0.09
690c	c	-	(MQ width > 50 μm) must be covered by MQPLANE	≡	-	-	-

Table 3-12. MQ (Thick Metal) Layout Rules

Rule	Class	Notes	Description		Des Min.	Waf. Dim.	Tol.
690dR	d	-	(MQ over MQPLANE) width (maximum) (μm).	\leq	2000.0	-	-
690e	c	-	(MQ width $\leq 50\mu\text{m}$) over MQPLANE not allowed.	\equiv	-	-	-
691a	a	-	MQ area (μm^2).	\geq	0.48	-	-
691b	a	-	MQ enclosed area (μm^2).	\geq	0.87	-	-
691cR	d	-	<p>(MQ not over MQPLANE) pass-through (feed-through) within or enclosed by (MQ over MQPLANE)(maximum)(μm^2)</p> <p>Note: MQ pass-through (feed-through) is defined as:</p> <ol style="list-style-type: none"> 1. (MQ not over MQPLANE) must have an area less than the Design Min specified, and 2. The (VY or VYBAR) vias above are each enlarged by $0.62\mu\text{m}/\text{side}$ and the VL vias below are each enlarged by $0.20\mu\text{m}/\text{side}$, then unioned together, and the (MQ not over MQPLANE) shape initially contacted by the vias must be completely covered by the enlarged and unioned via sets, and 3. (MQ not over MQPLANE) pass-through meets GR 694e spacing rule within (enclosed by) (MQ over MQPLANE) 	\leq	100.0	-	-
692	a	-	MQ to MQ space.	\geq	0.40	0.3424	0.09

Table 3-12. MQ (Thick Metal) Layout Rules

Rule	Class	Notes	Description		Des Min.	Waf. Dim.	Tol.
EPDL_MQ_min	a	-	(mq_estimated) minimum density (%) for boxes which do not touch { IND_FILT, BONDPAD } over local 126μm x 126μm areas stepped in 63μm increments across the chip, where mq_estimated is defined in Table H-4, “Estimated Pattern Density Rules” on page 427.	≥	10	-	-
EPDLi_MQ_min	a	-	(mq_estimated) minimum density (%) for boxes which touch { IND_FILT, BONDPAD } over local 126μm x 126μm areas stepped in 63μm increments across the chip.	≥	8	-	-
694	b	-	MQ to MQ space when at least one metal line is > 2.0μm wide.	≥	0.60	-	-
694b	b	-	MQ to MQ space when at least one metal line is > 8.0um wide.	≥	1.12	-	-
694c	b	-	MQ to MQ space when at least one metal line is > 25.0μm wide.	≥	1.92	-	-
694e	b	-	(MQ not over MQPLANE) to (MQ over MQPLANE) space.	≥	10.000	-	-
694f	b	-	(MQ over MQPLANE) to (MQ over MQPLANE) space.	≥	2.000	-	-
695d	c	-	MQPLANE (over MQ) in the chip guard ring not allowed.	≡	-	-	-

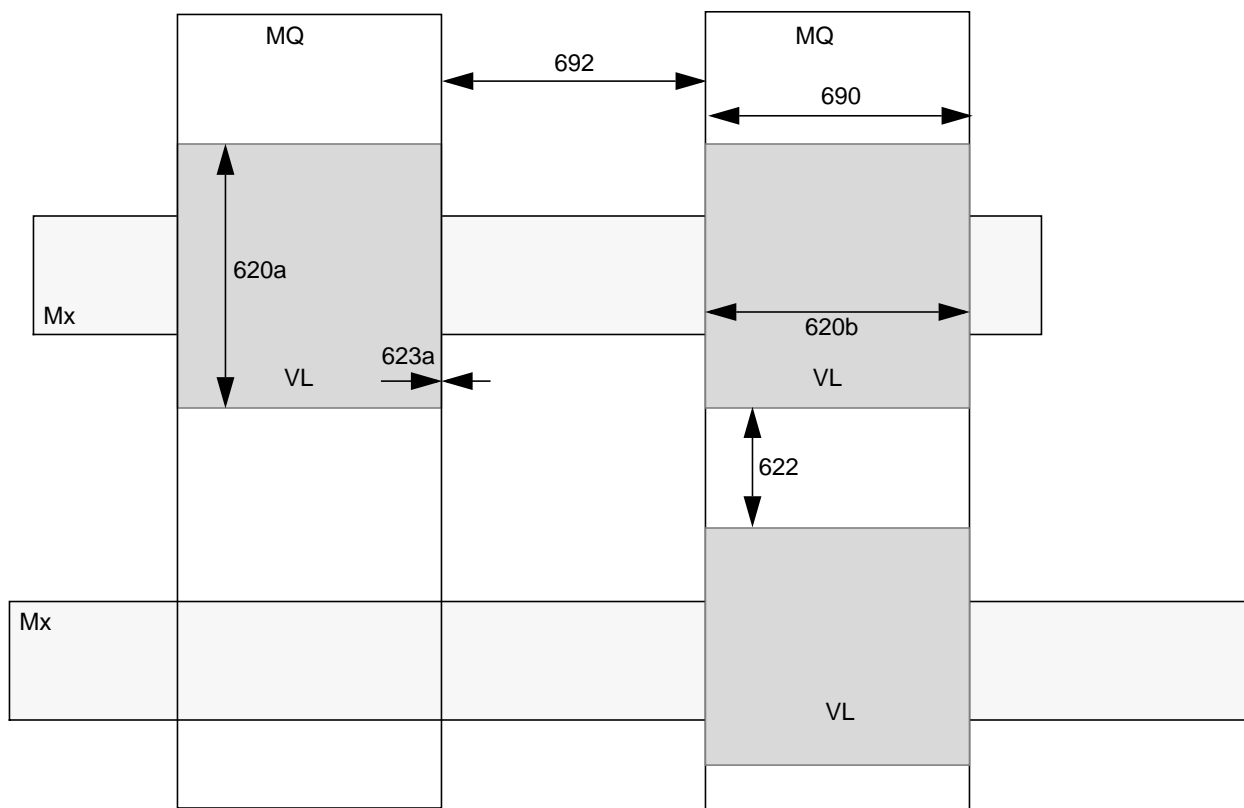


Figure 3-13. VL and MQ Interconnect Rules ($x=2,3,4$)

3.7.5 VY and VYBAR Layout Rules

Table 3-13. VY and VYBAR Layout Rules ¹							
Rule	Class	Notes	Description		Des Min.	Waf. Dim.	Tol.
VY1	a	-	{VY, VYBAR} (tungsten via) width (exact).	\equiv	1.240	1.2400	0.240
VY2	a	-	VY (tungsten via) length.	\equiv	1.240	-	-
VY2a	b	-	VYBAR (tungsten via bar) length (maximum).	\leq	20.000	-	-
VY2b	b	-	VYBAR (tungsten via bar) length (minimum).	\geq	3.72	-	-

Table 3-13. VY and VYBAR Layout Rules¹

Rule	Class	Notes	Description		Des Min.	Waf. Dim.	Tol.
VY3	b	-	{VY, VYBAR} must be square or rectangular and not at 45 degrees. (no polygon shapes allowed, except in chip guard ring).				
VY4	a	-	{VY, VYBAR} space.	≥	2.000	0.8757	0.240
VY4a	a	-	VY to VYBAR space (VY touching VYBAR not allowed).	≥	2.000	-	-
VY5	b	-	VYBAR space for common run > 5.00 μm.	≥	4.000	2.8757	0.240
VY6	b	-	VY must be within MQ.	≥	0.800	0.800	0.516
VY6a	b	-	{VY, VYBAR} within (MQ over MQPLANE).	≥	0.880	0.880	0.516
VY6b	b	2	(VYBAR not over KQ) must be within MQ.	≥	0.800	0.800	0.516
VY7	b	-	A minimum of 2 (VY or VYBAR) vias, spaced ≥ 2.0 μm and ≤ 4.0 μm, must connect MQ to LY.				

1. All Rules, except VY2, VY2a, VY2b, VY6 and VY6b apply to either VY or VYBAR. For rule VY2 equivalent VYBAR rule, see VY2a.
For VY6 equivalent VYBAR rule, see VY6b

2. VYBAR is used to contact KQ, see Rule KQ3 in Table 3-42, "KQ Resistor Layout Rules," on page 167.

3.7.6 LY Layout Rules

Table 3-14. LY Layout Rules

Rule	Class	Notes	Description		Des Min.	Waf. Dim.	Tol.
LY1	a	-	LY width.	≥	1.520	1.7700	0.340
LY2	a	-	LY space.	≥	1.520	1.2700	0.340
LY2a	a	-	LY to LY space; (if one metal lines is > 100.0μm wide).	≥	10.00	-	-
LY3	b	-	{VY, VYBAR} ¹ must be within LY.	≥	1.320	0.8828	0.542
LY4	b	-	LY Area (μm ²).	≥	2.000	-	-

Table 3-14. LY Layout Rules

Rule	Class	Notes	Description		Des Min.	Waf. Dim.	Tol.
LY5	a	-	LY Enclosed Area (μm^2).	\geq	6.000	-	-
LY6R	d	2	LY pattern density % over local $400\mu\text{m} \times 400\mu\text{m}$ areas stepped in $400\mu\text{m}$ increments across the chip.	\geq	10	-	-
LY6a	-	-	Rule Deleted	=	-	-	-

1. Rule applies to VY or VYBAR
2. Rule does not apply if the checking box is touching 8 neighbors (sides and corners) with $\geq 10\%$ LY density.

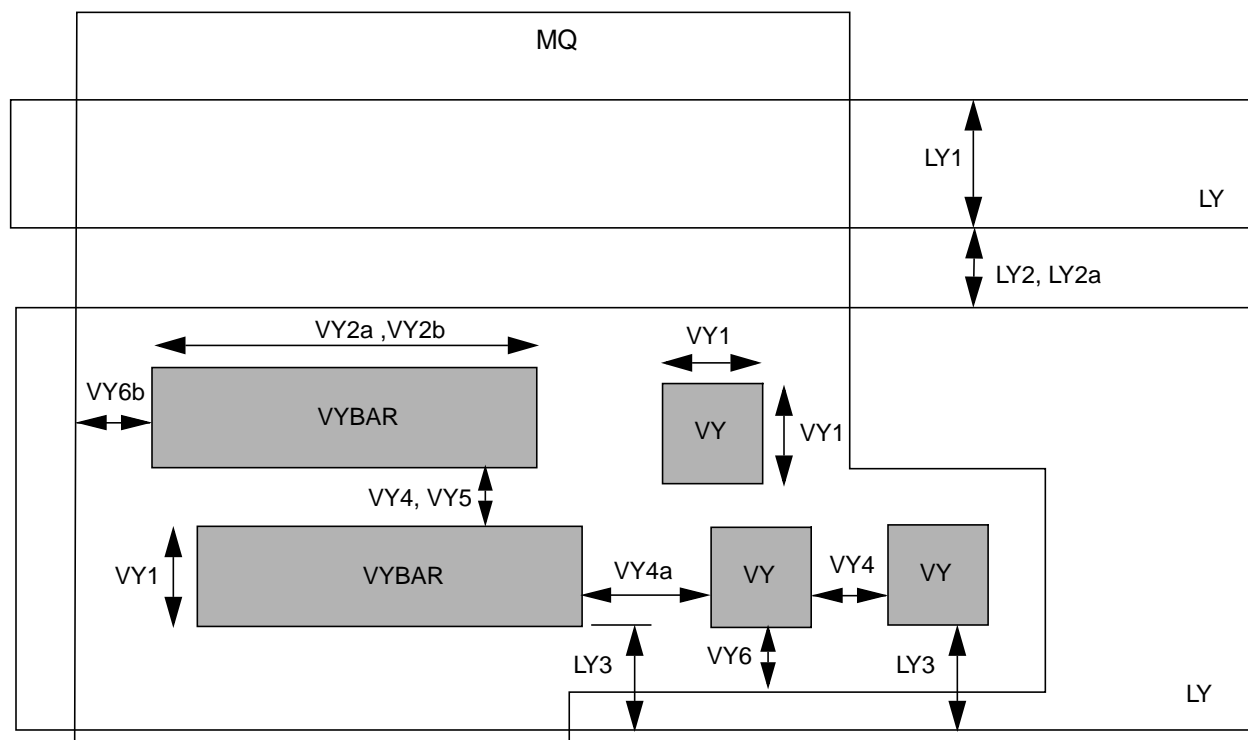


Figure 3-14. VY and LY Rules

3.7.7 AV and AVBAR Layout Rules

Table 3-15. AV and AVBAR Layout Rules ¹							
Rule	Class	Notes	Description		Des Min.	Waf. Dim.	Tol.
AV1	a	-	{AV, AVBAR} Width (only value allowed) (Wafer value at bottom).	≡	1.24	1.24	0.240
AV2	b	-	AV Maximum length.	≡	1.24	-	-
AV2a	b	-	AVBAR (tungsten via bar) length (maximum).	≤	20.00	-	-
AV2b	a	-	AVBAR (tungsten via bar) length (minimum).	≥	3.72	-	-
AV3	b	-	{AV, AVBAR} must be square or rectangular (no polygon shapes allowed except in chip guard ring).				
AV4	a	-	{AV, AVBAR} space.	≥	2.00	1.480	0.240
AV4a	a	-	AV to AVBAR space (AV touching AVBAR not allowed).	≥	2.000	-	-
AV5	b	-	AVBAR space for common run lengths greater than 5.0 μm.	≥	4.00	3.480	0.240
AV6	b	-	{AV, AVBAR} must be within LY.	≥	1.00	1.125	0.542
AV7	b	²	A minimum of 2 (AV or AVBAR) vias, spaced ≥ 2.0 μm and ≤ 4.0 μm, must connect LY to AM.				

1. All Rules, except AV2 and AV2a apply to AV or AVBAR

2. Rule is not applicable to AV vias for minimum size MIM (vias to connect QY to AM)

3.7.8 AM Layout Rules

Table 3-16. AM Layout Rules

Rule	Class	Notes	Description		Des Min.	Waf. Dim.	Tol.
AM1	a	-	AM Width.	\geq	2.000	2.160 ¹	0.600
AM1a	a	-	AM minimum area (μm^2).	\geq	10.00	-	-
AM2	a	-	AM space.	\geq	2.800	2.640 ¹	0.600
AM2a	c	2,3	AM space for AM edges over the same ({AV, AVBAR} not over {LOWCRNT ⁴ , IND_FILT}) sized by 8 μm).	\geq	5.000	-	-
AM2aa	c	2, 3	AM space for AM edges over the same ((({AV, AVBAR} over IND_FILT) not over LOWCRNT) sized by 6 μm).	\geq	5.000	-	-
AM2b	c	5, 3, 6	(AM not over IND_FILT) space (if at least one metal line is greater than 10 μm wide).	\geq	4.000	-	-
AM2b1	-	-	Rule Deleted	\equiv	-	-	-
AM2ba	c	5, 3, 6	(AM over (IND_FILT sized by 25 μm per edge)) space (if at least one metal line is > 10 μm and \leq 25 μm wide).	\geq	3.000	-	-
AM2b2	c	5, 3	(AM over (IND_FILT sized by 50 μm per edge)) space (if at least one metal line is > 25 μm and \leq 50.0 μm wide).	\geq	4.000	-	-
AM2c	c	5, 3	AM space (if at least one metal line is greater than 50 μm wide).	\geq	5.000	-	-
AM3	b	-	{AV, AVBAR} must be within AM.	\geq	1.000	0.820	0.682
AM4	c	-	{LV,DV} (within CHIPEDGE) must be covered by AM.				

1. The physical wafer values are at half-height measurements of a isolated feature. For the complete listing of wafer values see Table 4-40, "Extraction Parameters for Metal Wiring," on page 292.

2. Notch checks **not** required for these rules. AM2 will cover the minimum AM notch check.

3. Due to grid snapping ± 0.014 tolerance, or the grid times the square root of 2 tolerances applies to this Design Minimum dimension.

4. For additional information on LOWCRNT, see Table 2-4, "Dummy Design Levels and Utility Levels," on page 36.

5. Notch checks are required for these Rules.

6. Rule AM2b supersedes Rule AM2ba for (AM not over IND_FILT).

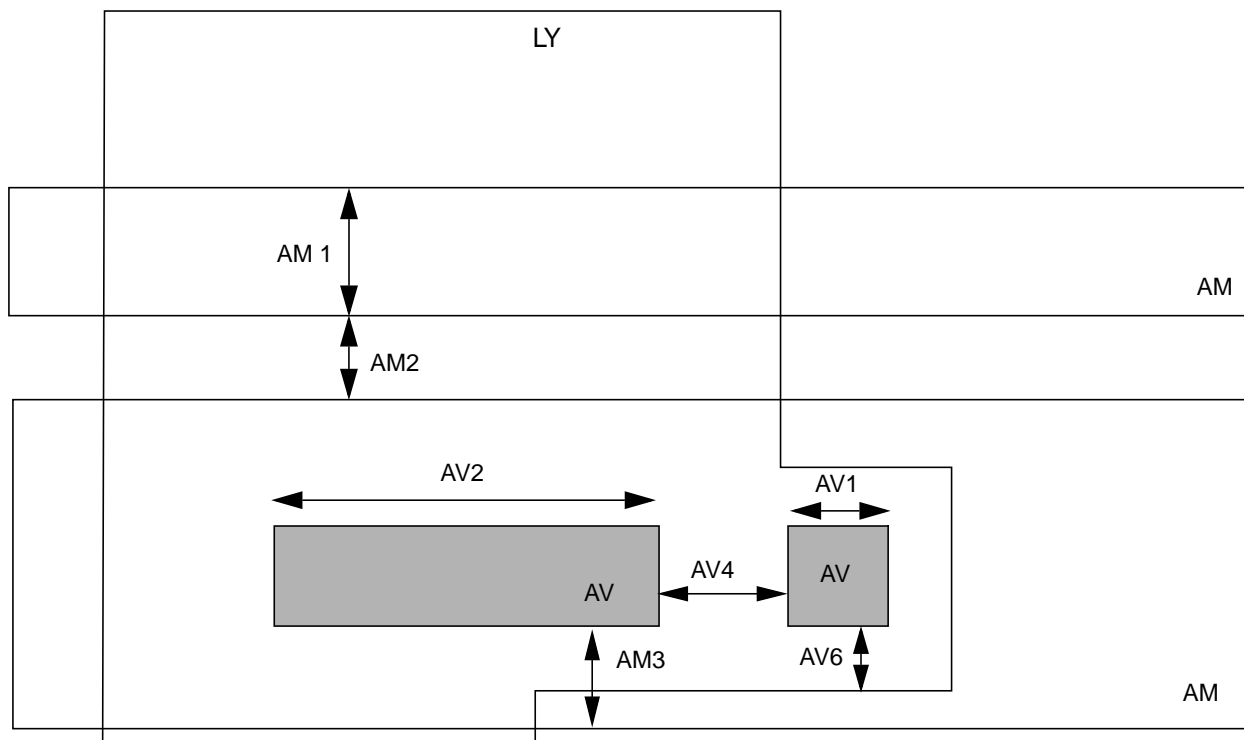


Figure 3-15. AV and AM Layout Rules

3.7.9 MxPLANE Layout Rules

Table 3-17. MXPLANE Layout Rules						
Rule	Class	Notes	Description	Des Min.	Waf. Dim.	Tol.
MXPL1	b	-	MxPLANE not touching Mx not allowed (x=1,2,3,4,Q).			
MXPL2	b	-	MxPLANE touching (IND_FILT or DV) not allowed (x=1,2,3,4,Q).			

Table 3-17. MXPLANE Layout Rules

Rule	Class	Notes	Description		Des Min.	Waf. Dim.	Tol.
MXPL3	b	1	<p>M1PLANE touching M2PLANE not allowed (for designs with 5LM, 6LM, or 7LM)</p> <p>M2PLANE touching M3PLANE not allowed (for designs with 6LM or 7LM)</p> <p>M3PLANE touching M4PLANE not allowed (for designs with 7LM)</p> <p>M2PLANE touching MQPLANE not allowed (for designs with 5LM)</p> <p>M3PLANE touching MQPLANE not allowed (for designs with 6LM)</p> <p>M4PLANE touching MQPLANE not allowed (for designs with 7LM)</p>				
MXPL4R	d	-	<p>M1PLANE to M2PLANE space (for designs with 5LM, 6LM, or 7LM)</p> <p>M2PLANE to M3PLANE space (for designs with 6LM or 7LM)</p> <p>M3PLANE to M4PLANE space (for designs with 7LM)</p> <p>M2PLANE to MQPLANE space (for designs with 5LM)</p> <p>M3PLANE to MQPLANE space (for designs with 6LM)</p> <p>M4PLANE to MQPLANE space (for designs with 7LM)</p>	≥	10.00	-	-

1. For levels of metal details, see Table 2-7, "Back End Of Line (BEOL) Metallization Options," on page 49.

3.8 Analog Layout Rules

3.8.1 LE, EX, CEBAR, NP, PB, and BX Rules

Table 3-18. LE (Emitter Landing Pad) Layout Rules

Rule	Class	Notes	Description		Des. Min.	Wafer	Tol.
LE1	a	-	LE width.	\geq	0.300	0.320	0.030
LE2	a	-	LE space.	\geq	0.300	0.280	0.030
LE3	b	-	EX must be within LE.	\geq	0.090	0.100	0.055
LE4	b	-	LE must be within (RX touching EX).	\geq	0.160	0.145	0.065
LE5	b	-	Number of distinct LE shapes within (RX touching (EX touching CEBAR)).	\equiv	1	-	-
LE6	b	-	LE must be rectangular (orthogonal, not at 45°).				
LE7	b	-	(LE touching CEBAR) must be covered by BB.				
LE8	b	-	LE must be covered by NP.				

Table 3-19. EX (Emitter) Layout Rules

Rule	Class	Notes	Description		Des. Min.	Wafer	Tol.
EX1	a	-	EX width (electrical on-wafer dimension).	\geq	0.12	0.135	0.0353
EX1a	b	-	(EX touching CEBAR) width (exact value).	\equiv	0.12	0.120	0.0353
EX1d	b	-	(EX not touching CEBAR) width maximum.	\leq	10.00	-	-
EX2	a	-	EX length (electrical on-wafer dimension).	\geq	0.52	-	0.0353
EX2a	-	-	Rule Deleted	\equiv	-	-	-

Table 3-19. EX (Emitter) Layout Rules

Rule	Class	Notes	Description		Des. Min.	Wafer	Tol.
EX3	a	-	EX space (electrical on-wafer dimension).	\geq	0.320	0.320	0.0353
EX4	a	-	EX must be within RX (elect on-wafer dim).	\geq	0.240	0.235	0.0825
EX5	a	-	EX must be rectangular.				
EX6	b	-	(EX touching CEBAR) must be within (NS or DS).				
EX7	b	-	Number of distinct EX shapes touching NP(maximum of 1 emitter stripes allowed).	\equiv	1	-	-
EX8	a	-	EX length (maximum).	\leq	18.00	-	-
EX9	a	-	EX area (μm^2).	\geq	0.0576		
EX9a	a	-	EX enclosed area (μm^2).	\geq	0.291		
EX10	b	-	(EX not touching CEBAR) to (EX touching CEBAR) space.	\geq	3.00	-	-

Table 3-20. CEBAR (Contact Emitter BAR poly) Contact Layout Rules

Rule	Class	Notes	Description		Des. Min.	Wafer	Tol.
CE7	a	1	CEBAR width(exact).	\equiv	0.200	0.2200	0.056
CE7a	b	-	45 deg CEBAR not allowed.				
CE7b	a	-	CEBAR space.	\geq	0.300	0.2514	0.060
CE8R	d	-	CEBAR must satisfy both CE9 and CE10.				
CE9	a	-	CEBAR length for rectangle.	\geq	0.600	0.620	0.056
CE10	b	-	CEBAR must be rectangular.				
CE13a	c	-	CEBAR overlap of EX.	\geq	0.160	0.170	0.120
CE13c	c	-	CEBAR overlap past EX.	\leq	0.040	0.050	0.120

Table 3-20. CEBAR (Contact Emitter BAR poly) Contact Layout Rules

Rule	Class	Notes	Description		Des. Min.	Wafer	Tol.
CE13e	c	-	The ratio of (CEBAR(intersect EX)area)/(EX area) must be.	\geq	0.40	-	-
CE14	b	-	CEBAR must be within NP.	\geq	0.180	0.170	0.103
CE14aR	d	-	CEBAR not allowed in Chip Guard Ring.				
CE19	a	-	CA to CEBAR.	\geq	0.420	0.368	0.093
CE28a	a	-	CEBAR *must not touch* {CA,CABAR.}				
CE29	c	-	{CA,CABAR} touching NP not allowed. Use CEBAR instead (see CA6 and CA7).				
CE31a	a	-	CEBAR to CABAR; common run $\leq 2.50\mu\text{m}$.	\geq	0.370	0.3252	0.097
CE31b	a	-	CEBAR to CABAR; common run $> 2.50\mu\text{m}$.	\geq	0.530	0.4852	0.097
CE32	b	-	Maximum CEBAR length.	\leq	5.00	-	-
CE33a	b	-	CEBAR to (M1 touching (CA or CABAR)).	\geq	0.37	0.3457	0.111
CE34	b	-	CE not allowed. Use CEBAR instead.				

1. CEBAR can not be used for wiring. CEBAR is to be used for interconnect purposes only.

Table 3-21. NP (NPN Emitter Poly) Layout Rules

Rule	Class	Notes	Description		Des. Min.	Wafer	Tol.
NP1	a	-	NP width.	\geq	0.56	0.5600	0.075
NP1a	a	-	NP area (maximum per shape) (μm^2).	\leq	250.00	-	-
NP1b	b	-	NP length (maximum per shape when NP width ≤ 13.56).	\leq	18.44	-	-
NP2	a	-	NP space.	\geq	0.68	0.6800	0.075
NP3	a	-	EX must be within NP (elect on-wafer dim).	\geq	0.22	0.2200	0.0908

Table 3-21. NP (NPN Emitter Poly) Layout Rules

Rule		Notes	Description		Des. Min.	Wafer	Tol.
	Class						
NP4	c	-	NP must not touch OP (NP strap res not allowed).				
NP5R	d	-	NP must be covered by PB (see Rule PBN8).				
NP5a	a	-	NP must not touch PC.				
PB101a	-	-	Rule Deleted				
PB101b	b	-	PB enclosed area (μm ²).	≥	4.52	-	-
PBN1	a	-	PB not over OZ width.	≥	1.30	1.3000	0.150
PBN1a	a	-	PB over OZ width (0.40μm wide emitter).	≥	1.08	0.92	0.15
PBN1b	a	-	PB over OZ length.	≥	1.88	0.92	0.15
PBN1c	b	-	PB over OZ must be rectangular.				
PBN2	c	-	All PB shapes must be orthogonal (not at 45°).				
PBN3	a	-	PB space (also minimum PB notch).	≥	1.00	1.0000	0.150
PBN3a	b	-	PB to PC (PB cannot touch PC) (PB touching PC) not allowed.	≥	1.00	1.0105	0.146
PBN4	b	-	PB to adj RX (shapes can not abut).	≥	0.24	0.2450	0.159
PBN4R	d	-	PB to RX (for no PF generation over RX).	≥	0.35	-	-
PBN5	b	-	(RX not over OZ) within PB.	≥	0.24	0.245	0.159
PBN5a	b		(PB over OZ) within RX.	≥	0.34	-	-
PBN6	b	-	BX must be within PB.	≥	0.26	0.1900	0.201
PBN8	b	-	NP must be within PB.	≥	0.46	0.4600	0.166
PBN9	b	-	PB within {BB,BP} (straddling not allowed).	≥	0.32	0.3200	0.183
PBN9c	b	-	PB(touching {CA,CEBAR}) must be covered by BB.	=	-	-	-
PBN10	b	-	PC(touching PD,RR,RN) must be within BB or BP.	≥	0.40	0.4105	0.111
PBN11	b	-	((PC intersection BB) not over IND_FILT) must be within {PD, RR} (to dope the polysilicon)				

Table 3-21. NP (NPN Emitter Poly) Layout Rules

Rule	Class	Notes	Description		Des. Min.	Wafer	Tol.
PBN12	a	-	PB to {BB,BP} (abutting or straddling not allowed)	≥	0.32	0.3200	0.183
PBN12aR	-	-	Rule Deleted	=	-	-	-
PBN12b	b	-	PC to BB (abutting or straddling not allowed).	≥	0.32	0.3305	0.111

Table 3-22. BX Rules

Rule	Class	Notes	Description		Des. Min.	Wafer	Tol
BX1	a	-	BX width.	≥	0.82	0.9600	0.150
BX1a	a	-	BX min area (μm^2)(for min etched area).	≥	0.78	-	-
BX1b	a	-	BX enclosed area (μm^2)(min photoresist land).	≥	0.76	-	-
BX2	a	-	BX space.	≥	0.820	0.680	0.150
BX4	b	-	BX to adjacent RX (abutting not allowed).	≥	0.24	0.1750	0.127
BX6	b	-	(RX touching (EX touching CEBAR)) must within BX (exact).	=	0.100	0.1750	0.127
BX7b	a	-	BX must be within PX.	≥	0.35	0.2600	0.170
BX8a	b	-	BX to adj PC(intersect RX).	≥	0.40	0.3405	0.139
BX8b	b	-	BX to adj PB(intersect RX).	≥	0.41	0.3400	0.201
BX12	a	-	(RX over BX) must be within PB.	≥	0.37	0.3000	0.201
BX14	b	-	PC touching BX not allowed. Use PB instead.				
BX15	b	-	BX only allowed on NPN (BX must be touching (NS or DS), and RX, and not touching NW, and touching BB, and touching PB.				
BX18	b	1	EX within BX (electrical on-wafer dimension).	≥	0.24	0.3100	0.149

Table 3-22. BX Rules

Rule	Class	Notes	Description		Des. Min.	Wafer	Tol
BX18a	b	-	(EX touching CEBAR)) must within BX (exact).	\equiv	0.350	0.4200	0.149
BX20	b	¹	{BX,CX} must be within BB.				

1. This rule is needed in case BX is used to mask the NU ion implant.

Table 3-23. CX Layout Rules

Rule	Class	Notes	Description		Des. Min.	Wafer	Tol.
CX2	b	¹	EX within CX (exact).	\equiv	0.080	0.280	0.115
CX4	b	-	RX within CX(not touching EX).	\geq	0.360	0.365	0.082
CX6	b	-	CX to adjacent RX.	\geq	0.240	0.245	0.082
CX7	a	-	CX width.	\geq	0.280	0.280	0.075
CX8	a	-	CX space.	\geq	0.480	0.480	0.075
CX9	b	-	CX can not touch DS.				

1. This rule is needed in case BX is used to mask the NU ion implant and the NU design level is eliminated.

3.8.2 RN, PX, NS, DS, DT and BB Rules

Table 3-24. RN (Reach through N+)

Rule	Class	Notes	Description		Des. Min.	Wafer	Tol.
RN1	a	-	RN width.	\geq	0.800	0.800	0.105
RN2	a	-	RN space (diffusion-to-diffusion).	\geq	1.920	1.320	0.109
RN2a	a	-	RN notch (same potential).	\geq	1.520	0.920	0.109
RN3	a	-	RN to adjacent RX.	\geq	0.360	0.365	0.118
RN3a	b	-	RN(not DT) touching more than one RX shape not allowed.				
RN4	b	-	RX within RN (RX sides where RN intersects DT, the rule can be ≥ 0.200 (only where the RN is over DT)).	\equiv	0.200	0.205	0.118
RN4a	b	-	(RN not DT) must touch RX.				
RN5a	b	-	(RX within RN) must not touch BP unless BP is touching BB.				
RN6	b	¹	RN must not touch P+ Junction.				
RN7	b	-	RN must not touch Substrate Contact (P Contact.				
RN9	a	-	RN enclosed area, μm^2 (for min resist island).	\geq	0.537	-	-
RN10	b	-	(RN over RX) must not touch PD.				
RN12a	a	-	RN not touching {RX,BB,NS,DS,JD} not allowed.				
RN16	a	-	RN to PC (RN touching PC not allowed).	\geq	0.500	0.5105	0.131
RN18	a	-	RN to NW (RN touching NW not allowed).	\geq	3.680	3.3800	0.174

1. P+ Junction = (RN must not touch (RX over (NW over BP))).

Table 3-25.PX Rules

Rule	Classes	Notes	Description		Des. Min.	Wafer	Tol.
PX1	a	-	PX width.	≥	0.72	0.6800	0.100
PX2	a	-	PX min area (μm^2)	≥	0.64	-	-
PX2a	a	-	PX enclosed area (μm^2).	≥	0.64	-	-
PX3	a	-	PX-PX space.	≥	0.68	0.7200	0.100
PX4	c	-	PX to adjacent RX.	≥	0.24	0.2650	0.117
PX5	b	-	RX within PX.	≥	0.20	0.1850	0.117
PX8a	b	-	PX to adj PB(intersect RX.)	≥	0.29	0.3100	0.195
PX8b	b	-	PX to adj PC (PC touching PX not allowed).	≥	0.29	0.3205	0.131
PX9	b	-	RX overlap past PX (min silicide).	≥	0.34	0.3375	0.117
PX10	b	-	PX to adj CA(over RX, not over {PC,PB}). (PX touching CA(over RX, not over {PC,PB}) not allowed).	≥	0.20	0.2125	0.144
PX11	b	-	PX to adj CABAR(over RX, not over {PC,PB}). (PX touching CABAR(over RX, not over {PC,PB}) not allowed).	≥	0.24	0.2600	0.146
PX12	b	-	PB(touching PX) can not touch RX(not covered by PX).				
PX13	c	-	CA(over PB) within PX (straddle not allowed).	≥	0.24	0.2125	0.144
PX14	b	-	CABAR(over PB) within PX (straddle not allowed).	≥	0.28	0.2600	0.146
PX15	b	-	PX must be covered by BB (straddle not allowed).				
PX25R	d	-	PX touching {PD, RR, OP} not allowed.				

Table 3-26.DT Rules

Rule	Class	Notes	Description		Des. Min.	Wafer	Tol
DT1	a	-	DT width (exact).	\equiv	1.040	1.000	0.060
DT2	a	-	DT length.	\geq	1.960	1.920	0.060
DT4	a	-	DT space.	\geq	1.440	1.480	0.060
DT5	a	-	No DT tabs allowed in DT_HOLE regions.				
DT5a	b	-	DT outside corner to RX.	\geq	1.760	1.785	0.070
DT7	b	-	DT overlap of (NS or DS).	\geq	0.340	0.300	0.231
DT7R	b	-	DT overlap of (NS or DS).	\equiv	0.520	0.480	0.231
DT8	b	¹	(DT not over ((NS sized by +0.72) or (NW sized by +0.76))) to NS (keep NS from adjacent device).	\geq	4.000	1.2900	0.276
DT8a	b	²	(DT not over ((DS sized by +0.72) or (NW sized by +0.76))) to DS (keep DS from adjacent device).	\geq	4.000	1.2900	0.276
DT8b	b	¹	(DT over ((NS sized by +0.72) or (NW sized by +0.76)) to (NS edge over DT))(keep NS from adjacent device).	\geq	1.800	-	0.276
DT8ba	b	¹	(DT over ((DS sized by +0.72) or (NW sized by +0.76)) to (DS edge over DT))(keep DS from adjacent device).	\geq	1.800	-	0.276
DT9	b	-	DT overlap past RN.	\geq	0.200	0.180	0.134
DT12R	d	-	DT must not touch RX (checked by RX3).				
DT13	b	³	((NS over NSR) over DT_HOLE) width (NS resistor minimum width touching the same NSR.	\geq	2.000	2.0400	0.060
DT14	b	⁴	A rectangle on the dummy level called NSR must be placed coincident with the inner edge of the "DTHOLE" formed by the inner edges of the DT fence around the NS resistor (for DRC checking). (exact).	\equiv	0.000	-	-
DT15	b	-	DT shapes must be orthogonal except ortho 45 DT shapes are allowed on: {chamfer on Chip Guard Ring, DT(touching IND_FILT))}				

Table 3-26.DT Rules

Rule	Class	Notes	Description		Des. Min.	Wafer	Tol
DT16	b	-	DT(enclosing NPN) within BB.	≥	0.240	0.260	0.118
DT17	b	-	DT(over DTMESH) or DT(with 1.44X1.44 spaces ⁵) over NW not allowed.				
DT20R	d	⁶	DT density % (maximum) over local 20μm X 20μm areas, stepped in 10μm increments, across the chip.	≤	20	-	-
DT21	b	-	DTMESH not touching {TLINE, IND_FILT} not allowed.				
DT22	b	-	DTMESH not touching DT not allowed.				
DT24	b	-	{DT Lattices, DTMESH} must be within BB (to keep PWell implants out of the DT Lattice or DTMESH).	≥	0.520	-	-
DT25	a	-	DT to PI (DT touching PI not allowed).	≥	1.350	1.3700	0.194

1. The NS expansion is based on the difference between Rules DT1 and DT7. The NW expansion is based on the difference between Rules DT1 and NW2 (see Table 3-5, "Additional N-well and Junction Layout Rules" on page 88).

2. The NS expansion is based on the difference between Rules DT1 and DT7. The NW expansion is based on the difference between Rules DT1 and NW2 (see Table 3-5, "Additional N-well and Junction Layout Rules" on page 88).

3. NSR is a dummy design level touching NS resistors to aid in DRC checking and to distinguish NS resistors from NS isolation beds.

4. "DTHOLE" is within NSR \equiv Rule DT 14.

5. DT(with 1.44x 1.44 spaces) = DTHOLE is coded using areas < 3.0 μ m².

6. DT in this rule applies to all DT in the technology (for example, any drawn DT, as well as all DT that is checked as part of DTMESH or DT Lattice in DRC).

Table 3-27.BB (Block Bipolar) Rules

Rule	Class	Notes	Description		Des. Min.	Wafer	Tol
BB1	a	1	BB width	≥	2.760	-	0.100
BB2	a	1	BB to BB space	≥	2.00	-	0.100

Table 3-27.BB (Block Bipolar) Rules

Rule	Class	Notes	Description		Des. Min.	Wafer	Tol
CP751a	b	-	BB containing ((NS or DS), QY, AM(over IND_FILT), RX, PB, PC) must have ((NS or DS), QY, AM(over IND_FILT), RX, PB, PC) bordered by a DT fence within the BB(for DT isolation) or be spaced away from any adjacent BB by	\geq	3.84	-	-
BB6	a	-	BB area for minimal resist island μm^2	\geq	9.600	-	-
BB7	a	-	BB enclosed area, μm^2	\geq	4.000	-	-
BB8	c	1	BB overlap of DT.	\geq	0.520	0.500	0.129
BB34a	b	-	(NW not touching VPNP) touching BB is prohibited.				
BB34b	b	-	(NW touching VPNP) must be covered by BB.				
BB35	b	-	(BB not over VPNP) to BP ((BB not over VPNP) touching BP not allowed.	\geq	0.400	-	-
BB35aR	d	-	BB straddling BP not allowed (No partial overlap between BB and BP allowed. One must be fully inside the other or not touch at all).				
BB35b	b		(BB over VPNP) to BP.	\geq	1.480	-	-
BB35bR	b	-	BP covered by BB is redundant. There is no P+ JCT formed since no BN is generated from BP touching BB; Use PD instead.				
BB36	b	-	NP within BB	\geq	0.400	-	-
BB37	c	-	PD must be within { ({BB, BP(expanded by 0.04)} intersect((PC touching OP) expanded by 0.44)) , RR(expanded by 0.02), (OZ not over DEGEN)}	\geq	0.000	0.0000	0.131
BB38	c	-	(((RX touching BB) not over VPNP) not over IND_FILT) not touching {NS, DS} is prohibited.				
BB40	c	-	((NP touching EX) touching CEBAR) must be covered by BB				
BB41	c	-	PC within BB (PC straddling BB not allowed).	\geq	0.500	-	-

1. These Design Rules must be made compatible with BF since BB derives/generates (is copied to) BP, BH and BF masks. BF is the level with the thickest resist and the lowest line/space resolution capability.

3.8.3 NS Design Rules, Ground Planes and Beds

Polysilicon resistors, MIMCAPS and bondpads may be layed out over a NS ground plane which acts as a shield for noise coupling to the substrate. The NS region is n+ in the p- silicon substrate, and is normally tied to the highest potential on the chip. Designers may tie the NS region to other potentials, such as the quietest supply voltage on chip, as long as the NS to p- substrate does not become forward biased.

Table 3-28.NS (N+ Subcollector) Rule

Rule	Class	Notes	Description		Des. Min.	Wafer	Tol
NS1	a	-	NS width.	\geq	1.360	1.3200	0.300
NS2	a	-	(NS edge not over DT) to NS space.	\geq	5.520	1.7870	0.424
NS2R	d	-	NS space (merge NS shapes if necessary).	\geq	6.000	3.0150	0.424
NS2b	a	-	(NS edge over DT) to (NS edge over DT).	\geq	2.480	-	0.424
NS4a	b	-	The edge of (NS over (DT intersect ESDUMMY)) within the edge of (NW over (DT intersect ESDUMMY)) (with respect to the NW outer edges that overlap of DT per Rule NW2 or NW2aR and the outer edges of NS that overlap of DT per Rule DT7 or DT7R) (NS and NW edges are coincident when NS and NW overlap of the inner edge of a DT ring).	\geq	0.000	-	0.256
CPNS4	a	-	NS within NW (exact with respect to the NW edges not intersecting DT for junction isolation).	\equiv	1.100	1.1200	0.256
NS5	b	-	NS to adjacent NW.	\geq	3.680	0.730	0.297
NS5R	d	-	NS to adjacent NW.	\geq	4.600	1.650	0.297
NS5a	c	-	NS can not touch NW (not over ESDUMMY).				
NS5b	c	1	NS can not touch BP (not over ESDUMMY).				
CPNS7	b	-	NS edge(not intersecting DT) within BB (exact) (for junction isolation.)	\equiv	2.100	-0.8150	0.310
NS8	b	-	(NS not intersecting NW) must be within BB (see also Rule NS19 and CPNS4).	\geq	0.000	-	-
NS10	b	-	NS to adj BB.	\geq	5.200	2.5300	0.305

Table 3-28.NS (N+ Subcollector) Rule

Rule	Class	Notes	Description		Des. Min.	Wafer	Tol
NS15	b	²	NS shapes in the design must ultimately be bounded by a DT fence. (This rule is to stop NS to P-wafer substrate junction leakage caused by dicing damage at the edge of the chip. See also Rule # 266b.				
NS15a	b	³	Distinct NS shapes(within a common BB) must be isolated from each other with DTfences around each NS shape to keep them from shorting together through the N- epi well created by the BB.				
NS15b	b	⁴	Distinct NS shapes(within a common NW) must be isolated from each other with DTfences around each NS shape to keep them from shorting together through the NW well.				
NS16	a	-	Every NS "AC ground plane bed" must be electrically contacted (no floating NS allowed)(use {[RX(touching RN,touching BB)] or [RX(not touching RN, over NW, over ESDUMMY)] contacts to NS beds). Each NS(not over DT, not coveredby ESDUMMY) must have one RX(over RN) contact to it.				
NS17R	d	-	NS beds for isolation(such as under resistors or MIMs) are normally electrically tied to highest DC potential. (Rule is not checked by DRC, see text below heading section 3.8.3 , "NS Design Rules, Ground Planes and Beds" on page 130)				
NS18	b	⁵	NS to {DTLattice, DTMESH} (NS touching {DT Lattice,DTMESH} not allowed).	≥	4.000	1.2900	0.276
NS19	b	-	NS must be covered by (BB or NW(over ESDUMMY)) (See also Rule NS8).				
NS21b	b	-	NS to (RX touching {PD, BP(not over ESDUMMY)}) ((NS cannot touch (RX touching {PD, BP(not over ESDUMMY)}) except for ESD Diodes).	≥	2.76	0.8985	0.281
NS25	b	-	NS(touching DT) must have all edges covered by DT.				
NS26	b	-	NS touching DG not allowed.				
NS27	b	-	(NS touching ESDUMMY) ⁶ touching {(PC intersect RX), NSR} not allowed.				

1. This rule does not apply to generated BP from the design level BB. Drawn design level BP touching NS is only allowed in ESD devices. Generated BP from design level BB is used in several devices where BB (generated BP) intersects NS.
2. This ground rule is only checked by the DRC deck when CHIPEDGE is present in the cell being checked. Use of design kit pcell with DT in the chip guard ring is suggested to satisfy this ground rule.
3. The Designer must either make 1 NS(within common BB) shape, or put DT isolation around each NS(within common BB).
4. The Designer must either make 1 NS(within common NW) shape, or put DT isolation around each NS(within common NW).
5. DT Lattice in Rule NS18 is not a dummy design level. The term DT Lattice is a pseudo-generated level in DRC that refers to any lattice of DT with an area of the hole formed by the DT being less than 3.00µm² and is not covered by DTMESH. For DTMESH, see Table 2-4, "Dummy Design Levels and Utility Levels," on page 36.

6. Design Level NS used in P+/NW and NW/SX ESD diodes should not touch active FET device gate or NS resistors.

3.8.4 DS Design Rules, Ground Planes and Beds

The DS region is n+ in the p- silicon substrate, and is normally tied to the highest potential on the chip. Designers may tie the DS region to other potentials, such as the quietest supply voltage on chip, as long as the DS to p- substrate does not become forward biased.

Table 3-29.DS (N+ Subcollector) Rules

Rule	Class	Notes	Description		Des. Min.	Wafer	Tol
DS1	a	-	DS width.	\geq	1.360	1.3200	0.300
DS2	a	-	(DS edge not over DT) to DS space.	\geq	5.520	1.7870	0.424
DS2R	d	-	DS space (merge DS shapes if necessary).	\geq	6.000	3.0150	0.424
DS2b	a	-	(DS edge over DT) to (DS edge over DT).	\geq	2.480	-	0.424
DS3	a	-	DS to NS space (DS can not touch NS) (see Rule DS4a).	\geq	5.520	1.7870	0.424
DS3R	d	-	DS to NS space (DS can not touch NS) (see Rule DS4a).	\geq	6.000	3.0150	0.424
DS4R	d	-	DS can only be used in the NPN High Break-down device (see rules DS4a, DS4b, DS4c, DS4d, CX9).	=	-	-	-
DS4a	b	-	DS touching (NS or NSR) not allowed.	=	-	-	-
DS4b	b	-	DS not touching {BB, DT, RX, RN, BX, LE, EX, NP, PB, PX} not allowed.	=	-	-	-
DS4c	b	-	DS touching OP not allowed.	=	-	-	-
DS4d	b	-	DS touching {PI, JD, PD, VAR, DG, (PC intersect RX)} not allowed.	=	-	-	-
DS5	a	-	DS to adjacent NW (DS can not touch NW).	\geq	3.680	0.730	0.297
DS5R	d	-	DS to adjacent NW.	\geq	4.600	1.650	0.297
DS6	c	-	{QY, BONDPAD, IND_FILT, TLINE} covered by DS not allowed.	=	-	-	-

Table 3-29.DS (N+ Subcollector) Rules

Rule	Class	Notes	Description		Des. Min.	Wafer	Tol
CPDS7	b	-	DS edge(not intersecting DT) within BB(exact) (for junction isolation).	\equiv	2.100	-0.8150	0.310
DS8	b	-	DS must be within BB (see also Rule DS19).	\geq	0.000	-	-
DS10	b	-	DS to adj BB.	\geq	5.200	2.5300	0.305
DS15	b	¹	DS shapes in the design must ultimately be bounded by a DT fence. (This rule is to stop DS to P-wafer substrate junction leakage caused by dicing damage at the edge of the chip. See also Rule DS266b.				
DS15a	b	²	Distinct DS shapes(within a common BB) must be isolated from each other with DTfences around each DS shape to keep them from shorting together through the N- epi well created by the BB.				
DS15b	b	³	Distinct ((union {DS,NS} shapes) within a common BB) must be isolated from each other with DTfences around each (DS or NS) shape to keep them from shorting together through the N- epi well created by the BB.				
DS16	a	-	Every DS "AC ground plane bed" must be electrically contacted (no floating DS allowed)(use RX(touching RN,touching BB) contacts to DS beds). Each (DS not over DT) must have one RX(over RN) contact to it.				
DS18	b	⁴	DS to {DT Lattice, DTMESH} (DS touching {DT Lattice, DTMESH} not allowed).	\geq	4.000	1.2900	0.276
DS19	b	-	DS must be covered by BB (See also Rule DS8)				
DS21b	b	-	DS to (RX touching {PD, BP}) (DS cannot touch (RX touching {PD, BP}))	\geq	2.760	0.8985	0.281
DS25	b	-	DS(touching DT) must have all edges covered by DT				

1. This ground rule is only checked by the DRC deck when CHIPEDGE is present in the cell being checked. Use of design kit pcell with DT in the chip guard ring is suggested to satisfy this ground rule.

2. The Designer must either make 1 DS(within common BB) shape, or put DT isolation around each DS(within common BB).

3. The Designer must either make 1 DS(within common BB) shape, or put DT isolation around each DS(within common BB).

4. DT Lattice in Rule DS18 is not a dummy design level. The term DT Lattice is a pseudo-generated level in DRC that refers to any lattice of DT with an area of the hole formed by the DT being less than $3.00\mu\text{m}^2$ and is not covered by DTMESH. For DTMESH, see Table 2-4, "Dummy Design Levels and Utility Levels," on page 36.

3.9 Vertical PNP (VPNP) Rules

The Vertical PNP (VPNP) is formed using the PB poly silicon for the emitter pedestal, an emitter window etch (EV) and an implanted intrinsic base and sub collector (OZ). BPHOLE (BP mask) and DEGEN (DE mask) are used in IBM Data Prep to add the N+ extrinsic base implants. The T3 implant is used to isolate the VPNP collector from the substrate.

Table 3-30. Vertical PNP Design Rules

Rule	Class	Notes	Description		Des. Min.	Wafer	Tol
VPNP01	a	-	VPNP width.	\geq	8.94	-	-
VPNP02	a	-	VPNP length.	\geq	9.64	-	-
VPNP03	b	-	VPNP to VPNP space.	\geq	5.00	-	-
VPNP05	c	-	VPNP must be an orthogonal rectangle.				
VPNP06	c	-	RX within VPNP.	\geq	0.380	-	-
VPNP10	a	-	VPNP must be covered by BB.				
VPNP15	b	-	VPNP overlap of NW.	\geq	2.00	-	-
VPNP16	b	-	NW overlap past VPNP.	\geq	1.10	-	-
VPNP20	b	-	VPNP must touch (NW, RX, BPHOLE, PD, DEGEN, PB, CA, CABAR).				
VPNP50	b	-	VPNP touching {NS, DS, DT, RN, JD, T3, PI, PX, DG, PC, BX, CX, LE, EX, NP, RR, OP, BFMOAT, EFUSE, ESDIODE, KQ, QY, IND_FILT, TLINE, BONDPAD, LOGOBND} is prohibited.				
VPNPPT01h	a	-	VPNP over PROTECT is prohibited.				

Table 3-30. Vertical PNP Design Rules

Rule	Class	Notes	Description		Des. Min.	Wafer	Tol
VPNPPN100	c	-	VPNP touching LOGOBND is prohibited.				
VPNP999a	a	-	VPNP must be within CHIPEDGE.	≥	0.00	-	-
VPNP594c	a	-	<p>For nets connected to NW contact touching VPNP electrical net where the NW net is not connected to a substrate contact defined by ((RX over BP) not over (NW or JD or PI or VPNP)), the ratio of [(20*Mx area) + (Non-isolated p+ junction area (((RX over BP) over NW) not over PC))] / (union[NW, PI, JD, VPNP] area) where x=1, 2, 3, 4, 5.</p> <p>(This check is for the isolation well perimeter Nwells not connected to a substrate contact, and p+ junctions in the non-isolated substrate regions are used to meet the ratio.</p> <p>This check assumes the T3 isolation well NW contact (i.e. the contact to the T3 isolation) does not contact the T3 isolated Pwell).</p>	≥	0.20	-	-

Table 3-31. EV Vertical PNP (VPNP) Rules

Rule	Class	Notes	Description		Des. Min.	Wafer	Tol
EV0	c	-	EV width other than {0.40, 0.80} μm is prohibited.				
EV1a	b	1	EV width (minimum).	≥	0.400	-	-
EV1b	c	1	EV width (maximum).	≤	0.800	-	-
EV1c	c	-	EV must be an orthogonal rectangular.				
EV2a	c	-	EV length (minimum for 0.40 μm width emitter).	≥	1.200	-	-
EV2b	c	-	EV length (minimum for 0.80 μm width emitter).	≥	2.400	-	-
EV2c	b	-	EV length (maximum).	≤	20.000	-	-
EV3	a	-	EV to EV space.	≥	0.320	-	-

Table 3-31. EV Vertical PNP (VPNP) Rules

Rule	Class	Notes	Description		Des. Min.	Wafer	Tol
EV4	a	-	EV must be within PB.	≥	0.340	-	-
EV6	a	-	(EV touching CABAR) must be within OZ.				
EV7	b	-	More than 1 EV shape touching a PB shape not allowed				
EV7a	b	-	Number of distinct EV shapes touching OZ (maximum of 2 emitter stripes allowed, minimum of 1 emitter stripe required) {C BEB C BEB C}				
EV11	a	-	EV to PD, EV cannot touch PD.	≥	1.120	-	-
EV11a	b	-	EV to NW, EV cannot touch NW.	≥	2.220	-	-
EV12	b	-	EV must touch CABAR.				
EV12a	b	-	EV touching CA is prohibited.				
EV13	b	-	EV to DEGEN (EV cannot touch DEGEN).	≥	0.260	-	-
EV14	b	-	(RX touching EV) edges must be covered by BPHOLE (for lower base resistance).				
EV15	b	-	(RX touching EV) edges must be covered by DEGEN (for lower base resistance).				
EV16	b	-	EV to BPHOLE (EV cannot touch BPHOLE).	≥	0.560	-	-
EV17	a	-	EV must be within RX.	≥	0.760	-	-
EV18	b	-	(BB touching EV) touching {NS, DS, DT, RN, JD, PI, PX, DG, PC, BX, CX, LE, EX, NP, RR, OP, BFMOAT, EFUSE, IND_FILT, TLINE, BONDPAD, LOGOBND} is prohibited.				

1. Design Kit Device Models only support 0.40 and 0.80 μm width VPNP Devices.

Table 3-32. OZ Vertical PNP (VPNP) Rules

Rule	Class	Notes	Description		Des. Min.	Wafer	Tol
OZ1	a	-	OZ width.	≥	4.620	-	-
OZ1a	b	-	OZ must be an orthogonal rectangle.				
OZ2	b	-	OZ min area (μm^2).	≥	20.80	-	-
OZ3	a	-	OZ space.	≥	3.500	-	-
OZ3a	a	-	OZ enclosed area (μm^2).	≥	20.80	-	-
OZ4	b	-	RX within OZ.	≥	0.140	-	-

Table 3-32. OZ Vertical PNP (VPNP) Rules

Rule	Class	Notes	Description		Des. Min.	Wafer	Tol
OZ7	b	-	OZ to NW, OZ cannot touch NW (collector to isolation space).	\equiv	0.160	-	-
OZ8	b	-	(NW within (BB over (OZ sized by 3.0 μ m))).	\geq	1.000	-	-
OZ9	b	-	(OZ sized by 0.17) edges must touch NW (gap width).				
OZ10	b	-	OZ must be within BB.	\geq	3.260	-	-
OZ11	b	-	OZ must be within VPNP.	\geq	2.160	-	-
OZ12	b	-	OZ must touch EV.				
OZ13	b	-	EV must be within OZ.	\geq	2.060	-	-
OZ14	b	-	DEGEN must be within OZ.	\geq	1.280	-	-
OZ15	b	-	(BPHOLE within OZ).	\geq	1.160	-	-
OZ15a	b	-	More than one OZ within a common BB shape is prohibited.				
OZ16R	d	-	(PB over OZ) within RX (lower base resistance).	\geq	0.420	-	-
OZ17	b	-	(BB touching OZ) cannot touch {NS, JD, PX, DG, PC, BX, EX, NP, BP, RR, OP, LOGOBND, IND_FILT, BOND PAD, TLINE}.				
OZ19HP	b	-	PD overlap past OZ.	\geq	0.060	-	-
OZ20	b	-	(PB touching EV) must be within OZ.	\geq	1.720	-	-
OZ21	b	-	(CA over OZ) within DEGEN.	\geq	0.160	-	-
OZ22	b	-	(CA over OZ) within BPHOLE.	\geq	0.160	-	-
OZ23	b	-	(CABAR over OZ) within EV.	\geq	0.020	-	-
OZ260c	b	-	(RX over OZ) must be within BB.	\geq	3.400	-	-

Table 3-33.BPHOLE and DEGEN Vertical PNP (VPNP) Rules							
Rule	Class	Notes	Description		Des. Min.	Wafer	Tol
BPH1	a	-	BPHOLE width.	≥	0.340	-	-
BPH2	a	-	BPHOLE space.	≥	0.340	-	-
BPH3	a	-	BPHOLE enclosed area (μm^2).	≥	0.790	-	-
BPH5	b	-	BPHOLE must be within (BB touching OZ).	≥	1.300	-	-
BPH7	b	-	BPHOLE to PB (BPHOLE cannot touch PB).	≥	0.220	-	-
BPH9	b	-	BPHOLE overlap past RX.	≥	0.140	-	-
BPH10	b	-	BPHOLE to RX.	≥	0.420	-	-
BPH11	b	-	(BPHOLE over OZ) to NW. (BPHOLE over OZ) cannot touch NW.	≥	1.320	-	-
BPH12	b	-	BPHOLE cannot touch PD.	≡	-	-	-
BPH13R	d	-	BPHOLE not within BB, covered by Rules OZ10 and OZ15.	≥	4.420	-	-
BPH20	b	-	(CA over NW) within BPHOLE.	≥	0.280	-	-
DE1	a	-	DEGEN width.	≥	0.440 ¹	-	-
DE2	a	-	DEGEN space.	≥	0.440 ¹	-	-
DE3	b	-	DEGEN must be within (BB touching OZ).	≥	4.540	-	-
DE4	b	-	DEGEN overlap of BPHOLE.	≥	0.220	-	-
DE5	b	-	DEGEN to RX.	≥	0.540	-	-
DE6	b	-	DEGEN overlap of PB.	≥	0.080	-	-
DE7	b	-	DEGEN cannot touch PD.	≡	-	-	-

1. Technology limit =0.40.

3.10 Mask Process Control Images

To achieve tight image size and registration control for PC mask, special reticle measurement features, called Process Control Images (PCIs) are **required** to be placed in the data.

The PCI requirement is waived on any chip with a width or length shorter than 6mm on any side. Sufficient PCIs are placed in the kerf for chips with a length or width dimension smaller than 6mm.

Requirements:

1. The design level PCING must be used to draw each PCI
2. The PCI shape must exist in its own, separate data cell (model). The cell must have a 6-8 character uppercase alphanumeric name containing the string "IPCI". The character string "IPCI" must be in the upper case. There is no limit to the number of cell names.
3. The character string "IPCI" must not be used in any other cell names.
4. Ideally, if the chip was divided into a 12 x 12 matrix, each of the 144 "tiles" would contain one PCI. However, it is sufficient to have some PCI's near each of the corners of the chip and some PCI's in the interior of the chip near the center.
5. The centerpoint of the PCI shape must be identical to the origin of the cell (model). The centerpoint is at the center of the intersect of horizontal and vertical arms.

Table 3-34. PCING Layout Rules

Rule	Class	Notes	Description		Des Min.
780	a	-	PCING width.	≡	0.12
781b	a	-	The character sequence "IPCI" (all uppercase) is prohibited in all data cells in the design except those defined by Rules 780, 782, and 783.	≡	-
782	a	-	PCING to any PC, PCING, RX, NP, CA, CABAR, CEBAR shapes (PCING can not touch any of these levels).	≥	0.42
782b	a	-	PCING to any PB shapes (PCING touching PB not allowed).	≥	1.02
783	a	-	Length of PCING arm from corner to end.	≥	2.00
784	a	-	At least 40 PCI cells should be uniformly distributed over the active chip area.	≡	-

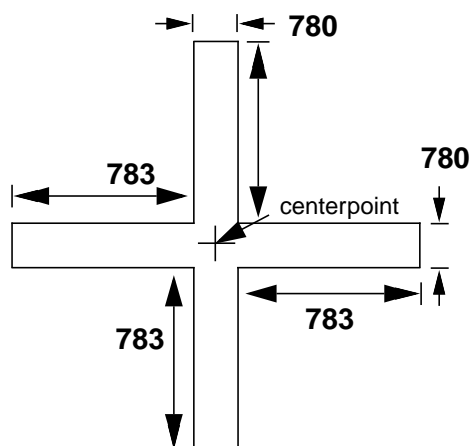


Figure 3-16. Figure 3-17. PCING Structure

3.11 ESD Rules

3.11.1 Rule Definitions

I/O pad: DV wire-bond or LV C4 pad (for AM BEOL) including signal and power pads.

I/O signal pad: All I/O pads either labeled "FULL_ESD" on the xxESD level or not otherwise identified as LC power or HC power supply pads, where xx = the appropriate alphabetic or numeric or alphanumeric identifiers supported for pad definition (see Table 2-4, "Dummy Design Levels and Utility Levels," on page 36).

Low Capacitance (LC) power supply pad:

An I/O pad either labeled "LC_POWER_ESD" on the xxESD level or electrically connected to a metal and labeled LC_POWER_ESD on the xxESD level, where xx = the appropriate alphabetic or numeric or alphanumeric identifiers supported for pad definition (see Table 2-4, "Dummy Design Levels and Utility Levels," on page 36).

High Capacitance (HC) power supply pad:

An I/O pad either labeled “HC_POWER_ESD” on the xxESD level or electrically connected to a metal and labeled HC_POWER_ESD on the xxESD level, where xx = the appropriate alphabetic or numeric or alphanumeric identifiers supported for pad definition (see Table 2-4, “Dummy Design Levels and Utility Levels,” on page 36).

Design rule ESD30, presented in Table 3-35, “ESD Layout Rules” on page 142, uses the following syntax:

HBM diode string:	A diode-based ESD HBM protection device comprised of two or three p+ n-well diodes connected in series between an I/O pad and a power supply and an N+ substrate diode connected between an I/O pad and a ground.
HBM NFET:	An NFET-based ESD HBM protection device comprised of a grounded gate NFET with a drain connected to an I/O pad.
HBM double diode:	A diode-based ESD HBM protection device comprised of one P+ n-well diode connected between an I/O pad and a power supply and one N+ substrate diode connected between an I/O pad and a ground.
CDM resistor:	A P+ polysilicon OP resistor placed in the path between an I/O signal pad and receiver FET gates.

3.11.2 Layout Rules

Table 3-35. ESD Layout Rules

Rule	Class	Notes	Description		Des Min.
ESD0e	c	-	<p>LC power supply pads must be connected to:</p> <ul style="list-style-type: none"> — One or more (RX n+ diffusions satisfying Rule ESD01a) and one or more (RX p+ diffusions satisfying Rule ESD01b) or — One or more (RX n+ diffusions touching NFET gates, satisfying Rule ESD01c) <p>--> Diode based, NFET based or RC-triggered power clamp based ESD device required.</p>	≡	-
ESD01	c	1	<p>All I/O (not including power supply pads) pads must be connected to one or more RX (not covered by BP) or RX (covered by BP inside NW) shapes within ESDUMMY satisfying (ESD01a and ESD01b) or ESD01c</p> <p>--> Diode based or NFET based ESD device required</p>	≡	-
ESD01a	c	-	<p>If none of the diffusion shapes within ESDUMMY identified in ESD01 contain an NFET, the pad must be connected to one or more RX (not covered by {BP, BB}) shapes within ESDUMMY having a total perimeter [μm]</p> <p>--> N+/SX or NW/SX diode perimeter</p>	≥	110
ESD01aR	c	-	<p>If none of the diffusion shapes within ESDUMMY identified in ESD01 contain an NFET, the pad must be connected to one or more RX (not covered by {BP, BB}) shapes within ESDUMMY having a total perimeter [μm] (On pads where minimum capacitance is not required, it is strongly recommended to use this groundrule to meet ESD robustness requirement)</p> <p>--> N+/SX or NW/SX diode perimeter</p>	≥	125
ESD01b	c	-	<p>If none of the diffusion shapes within ESDUMMY identified in ESD01 contain an NFET, the pad must be connected to one or more RX (covered by BP inside NW) shapes within ESDUMMY having a total perimeter</p> <p>--> P+/NW diode perimeter</p>	≥	220

Table 3-35. ESD Layout Rules

Rule	Class	Notes	Description		Des Min.
ESD01bR	c	-	If none of the diffusion shapes within ESDUMMY identified in ESD01 contain an NFET, the pad must be connected to one or more RX (covered by BP inside NW) shapes within ESDUMMY having a total perimeter [μm] (On pads where minimum capacitance is not required, it is strongly recommended to use this groundrule to meet ESD robustness requirement) --> P+/NW diode perimeter	\geq	350
ESD01c	c	2	If one or more of the diffusion shapes within ESDUMMY identified in ESD01 contain an NFET, the pad must be connected to one or more RX (not covered by BP or NW) shapes within ESDUMMY where the gate (PC intersect RX) perimeter [μm]. --> NFET width/perimeter	\geq	400
ESD01cR	c	2	If one or more of the diffusion shapes within ESDUMMY identified in ESD01 contain an NFET, the pad must be connected to one or more RX (not covered by BP or NW) shapes within ESDUMMY where the gate (PC intersect RX) perimeter [μm]. --> NFET width/perimeter	\geq	800
ESD02a	-	-	Rule deleted.	-	-
ESD03a	-	-	Rule deleted.	-	-
ESD04	-	-	Rule deleted.	-	-
ESD04a	-	-	Rule deleted.	-	-
ESD05	-	-	Rule deleted.	-	-
ESD06	-	-	Rule deleted.	-	-
ESD06b	-	-	Rule deleted.	-	-
ESD07a	-	-	Rule deleted.	-	-

Table 3-35. ESD Layout Rules

Rule	Class	Notes	Description		Des Min.
ESD08	c	3,4	{[NW connected to I/O signal pads], [(NW within ESDUMMY) connected to LC power supply pads]} minimum space to NW, different net [μm]. --> Minimizing current through parasitic NPN (NW/SX/NW) during negative mode HBM event	\geq	4.40
ESD09	c	3, 4	{[RX n+ diffusions connected to I/O signal pads], [(RX n+ diffusions within ESDUMMY) connected to LC power supply pads]} minimum space to RX n+ diffusions, different net [μm]. --> Minimizing current through parasitic NPN (N+/SX/N+) during negative mode HBM event.	\geq	3.50
ESD10	c	3, 4	{[RX n+ diffusions connected to I/O signal pads], [(RX n+ diffusions within ESDUMMY) connected to LC power supply pads]} or {[NW connected to I/O signal pads], [(NW within ESDUMMY) connected to LC power supply pads]} minimum space to {NW, different net} or {RX n+ diffusions, different net}; respectively [μm]. --> Minimizing current through parasitic NPN (N+/SX/NW) or (NW/SX/N+) during negative mode HBM event.	\geq	3.50
ESD11a	-	-	Rule deleted.	-	-
ESD11bR	-	-	Rule deleted.	-	-
ESD11dR	-	-	Rule deleted.	-	-
ESD11eR	-	-	Rule deleted.	-	-
ESD12f	-	-	Rule deleted.	-	-
ESD12g	-	-	Rule deleted.	-	-
ESD13A	c	4	NWell Guardring Rule, Refer to Rule LUP13.		
ESD13B	c	4	Substrate Guardring Rule, Refer to Rule LUP13.		

Table 3-35. ESD Layout Rules

Rule	Class	Notes	Description		Des Min.
ESD14f	c	-	CA within RX within ESDUMMY [μm], Refer to Rule 204R --> CA within RX covered by ESDUMMY must follow recommended Rule 204R	\geq	0.14
ESD15a	-	-	Rule deleted.	—	-
ESD15b	-	-	Rule deleted.	—	-
ESD16	c	-	If any resistor connected to an IO pad is < 20 ohms, it is considered a conductor/short from a checking standpoint for rules ESD01 to ESD14f. If it is ≥ 20 ohms and it is outside ESDUMMY, it is considered an open for ESD01 to ESD14f. Resistance values are calculated using the equations in Section 4.7 , “Resistor Models” on page 265, ignoring temperature and voltage dependencies; end resistance is included.	—	-
ESD17	c	-	Rules 710, 710R, 711, 711R, 712, 712R, 713, 713R, 735a, 735b1, 737, 737a, 738 do not apply if covered by (ESDUMMY or ESD_CDM)	—	-
ESD20	c	2	(OP under (ESDUMMY or ESD_CDM)) to PC.	\equiv	0.24
ESD21	c	-	(OP under (ESDUMMY or ESD_CDM)) cannot touch BP, NW.	—	-
ESD22	c	-	(OP under (ESDUMMY or ESD_CDM)) must cut RX into two diffusions.	—	-
ESD23	c	-	(OP under (ESDUMMY or ESD_CDM)) width on the source.	\equiv	0.44
ESD24	c	-	(OP under (ESDUMMY or ESD_CDM)) width on the drain not within DG.	\geq	2.00
ESD24a	c	-	(OP under (ESDUMMY or ESD_CDM)) width on the drain within DG.	\geq	3.00
ESD25	c	-	((PC over (RX touching OP) under (ESDUMMY or ESD_CDM)) expanded by $0.24 \mu\text{m}$) must touch exactly one (OP= $0.44 \mu\text{m}$ under (ESDUMMY or ESD_CDM)) source and exactly one (OP $\geq 2.0 \mu\text{m}$ under (ESDUMMY or ESD_CDM)) drain.	—	-
ESD26	c	-	((OP under ESDUMMY) expanded by $0.24 \mu\text{m}$) touches exactly one (PC intersect RX).	—	-

Table 3-35. ESD Layout Rules

Rule	Class	Notes	Description		Des Min.
ESD30	c	5, 6	All gates connected to an I/O signal pad and an HBM device must be connected through a CDM resistor to one or more (RX diffusions within ESD_CDM) CDM Resistor = A P+ polysilicon OP resistor placed in the path between an IO signal pad and receiver FET gate.	≡	-
ESD31a	-	-	Rule deleted.	-	-
ESD31b	-	-	Rule deleted.	-	-
ESD31c	-	-	Rule deleted.	-	-
ESD32a	-	-	Rule deleted.	-	-
ESD32b	-	-	Rule deleted.	-	-
ESD32bR	-	-	Rule deleted.	-	-
ESD32c	-	-	Rule deleted.	-	-
ESD33	-	-	Rule deleted.	-	-
ESD34a	-	-	Rule deleted.	-	-
ESD34b	-	-	Rule deleted.	-	-
ESD34c	-	-	Rule deleted.	-	-
ESD35a	-	-	Rule deleted.	-	-
ESD35b	-	-	Rule deleted.	-	-
ESD35c	-	-	Rule deleted.	-	-
ESD39	-	-	Rule deleted.	-	-
ESD40	-	-	Rule deleted.	-	-

1. ESDUMMY is a dummy shape that is placed over the ESD structure
2. Designers MUST pass rules ESD20 to ESD26 only on NFETs if they are used as HBM or CDM protection devices.
3. RX diffusion and NW shapes covered by the same ESDUMMY marker shape are exempt from this rule. NW shapes that are terminals of the same string diode or anti-parallel diodes are also exempt
4. This rule does not apply for (RX diffusions not touching PC) with an area < 1.0μm²
5. "HBM Device" is a term inclusive of the following devices: HBM diode string, HBM double diode, and HBM NFET. These devices are defined in detail in Section , "" on page 140
6. "RX diffusions within ESD_CDM" are the RX portion of the CDM Diodes

3.11.2.1 Notes:

- The ESDUMMY shapes should be drawn to cover all RX shapes (expanded by $\geq 0.5 \mu\text{m}$) associated with the ESD design that are connected to the IO pad.
- It is recommended to tie both the Source and the Substrate of a transistor to the same ground and not different grounds to stop the formation of a parasitic diode between any two grounds
- Rule ESD14f conflicts with Rule 739aR for certain programs when diffused OP resistors are used. In this case Rule ESD14f takes precedence.
- Note that all required guardrings are not included in the figures that follow.
- A CDM resistor length of $2.5\mu\text{m}$ will allow a maximum of 40V across the resistor.
- See section 3.11.2.2 , “Pad Identification for ESD Verification Purposes:” on page 147.
- ESD HBM diodes with diode finger length $< 35\mu\text{m}$ result in a higher on-resistance of the diode and could lead to lower ESD results

3.11.2.2 Pad Identification for ESD Verification Purposes:

IBM strongly supports using Pad Labeling as defined in Section 3.11.5 , “Net Definitions for ESD Checking and Latchup Verification” on page 151. The IODUMMY methodology is not supported.

All pads identified using the net definitions defined in Section 3.11.5 , “Net Definitions for ESD Checking and Latchup Verification” on page 151 will be checked for ESD and Latchup rule compliance.

3.11.3 ESD Groundrule Figures (Diode Based Protection)

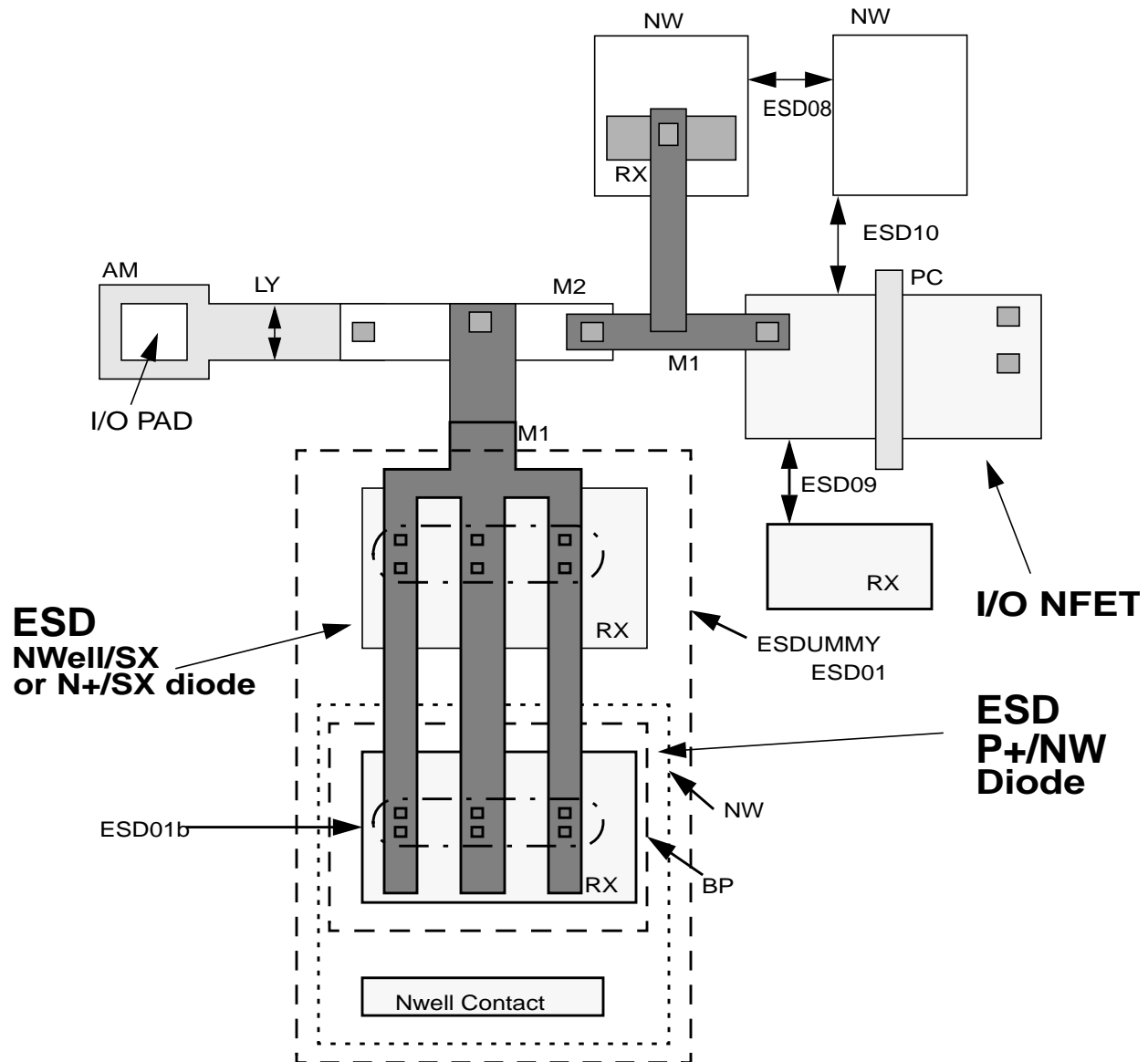


Figure 3-18. ESD Diode Based Protection

3.11.4 ESD Groundrule Figures (MOSFET Based Protection)

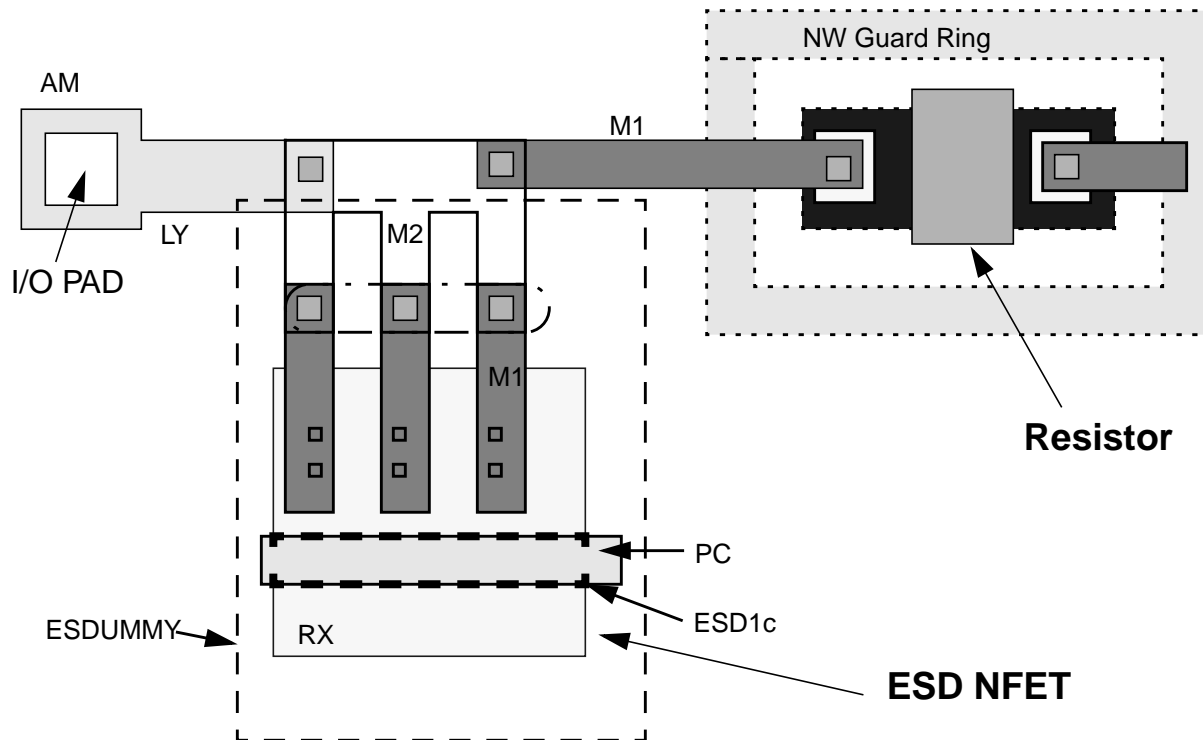


Figure 3-19. ESD MOSFET Based Protection Figure 1

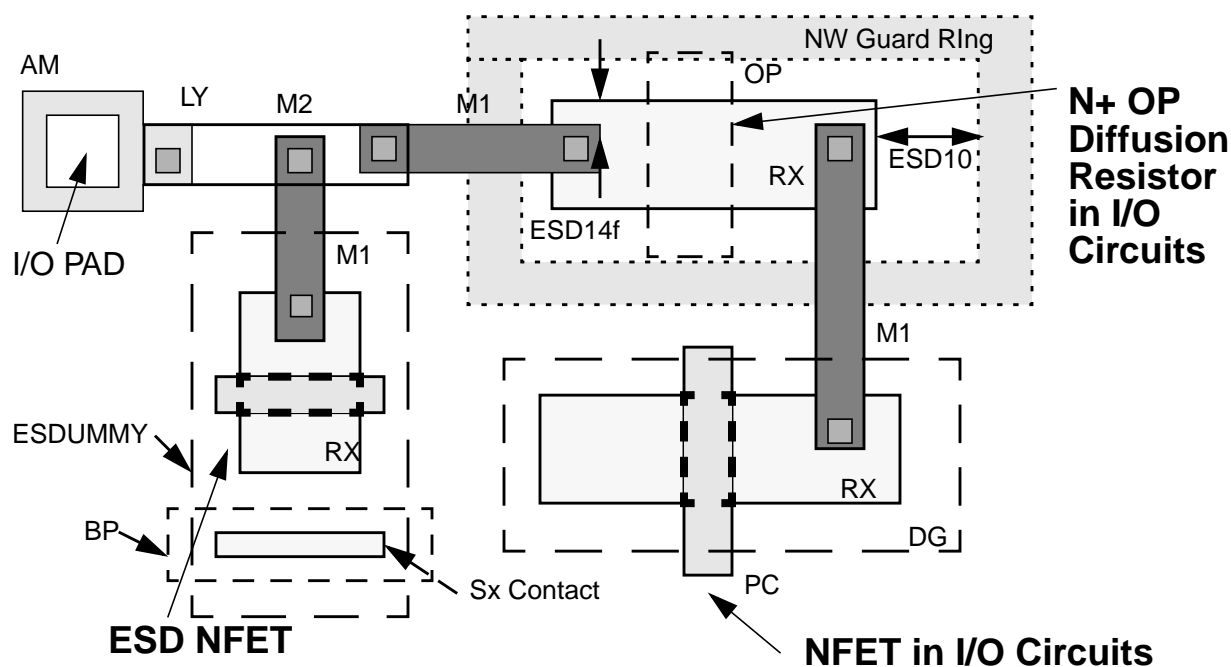


Figure 3-20. ESD MOSFET Based Protection

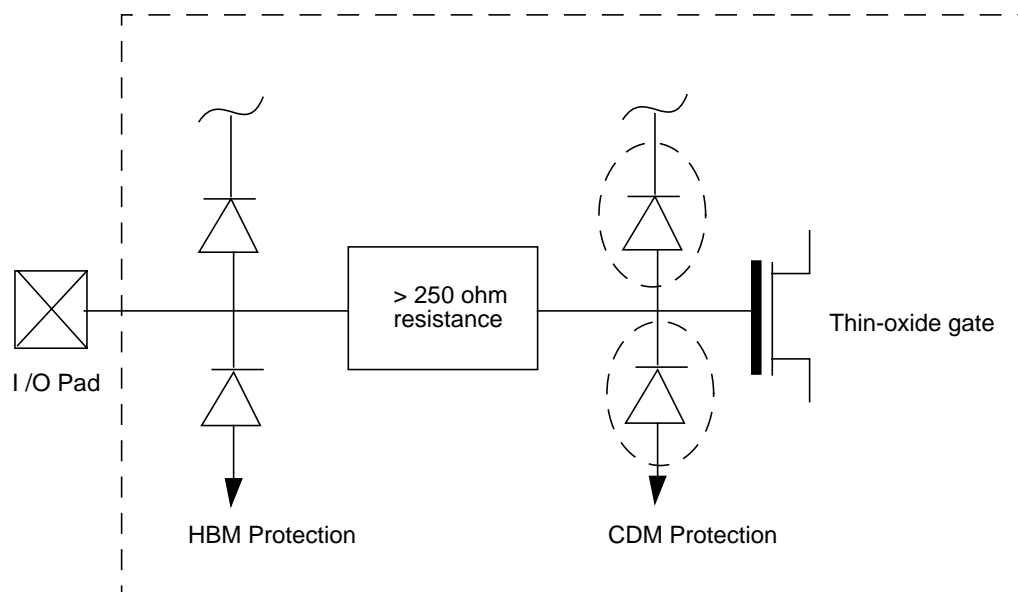


Figure 3-21. ESD30 when > 250 ohm is used and diode / bipolar based CDM is used

3.11.5 Net Definitions for ESD Checking and Latchup Verification

For cell-level testing, all nets that ultimately will be connected to chip pads should be labelled with one of the labels defined below. These text labels must be placed on an xxESD level, where xx = M1, M2, and so forth.

For chip level testing, only the FULL_ESD, LC_POWER_ESD or HC_POWER_ESD labels are valid on chip pads. All pads not identified with any label will be assumed to have the FULL_ESD label and checked as a signal I/O pad. These chip pad text labels should use LMESD or MAESD or LDESSED level and the text should be placed within the chip pad region (e.g. DV, LV, etc. passivation opening layer). Use of LMESD or MAESD or LDESSED is determined by which Back-End-Of-Line metallization option is being used for the chip design, as described in Table 2-7, "Back End Of Line (BEOL) Metallization Options," on page 49.

LC_POWER_ESD and HC_POWER_ESD labels on xxESD used in cell level checking can also be used to identify pads as if those pads were labelled with LMESD or MAESD text as described above (i.e. chip pads connected to metal levels containing these xxESD labels are to be treated as power supply pads).

"FULL_ESD" - Full checking of all ESD and Latchup layout rules, signal pads with ESD protection.

"WIRE_ESD" - Used to check metal width, contact and via areas for fat wire like books w/o ESD protection, pad transfer books. ESD02a-ESD06e values (wires, vias, contacts only checked) are applicable here even if the metal does not extend to RX.

"WIRE_ESD_ENDPT" - Used to define a termination point for wide metal checking of cell I/O pads labeled WIRE_ESD and LC_POWER_WIRE_ESD within a cell.

"NO_PROTECT_HBM" - Used for internal books without HBM protection but will eventually go to a pad. All rules except ESD01 - ESD06e apply.

HBM rules		To be applied under ESDUMMY only
ESD01	ESD01a	ESD08 to ESD10
		ESD13A to ESD13B/LUP13
		ESD14f to ESD15a
	ESD01b	LUP14a
		ESD14f
		ESD15b
		LUP14b to LUP15b
	ESD01c	ESD09 to ESD10
		ESD13A to ESD13B/LUP13

HBM rules		To be applied under ESDUMMY only
CDM rules		
ESD30	CDM rules	Exclude gates under ESDUMMY and ESD_CDM when NFET clamps are used in either HBM or CDM protection

“**HC_POWER_ESD**” - Used for power supply pins that DO achieve 100nF of chip capacitance between the supply and GND. Metal rules ESD02a-ESD06c should be followed, similar to WIRE_ESD.

“**LC_POWER_WIRE_ESD**” - Used for a power supply net that DOESN'T achieve 100nF of chip capacitance between the supply and GND, and whose HBM protection is provided in another cell that connects to the chip pad. Metal rules ESD02a-ESD06c and CDM rule ESD30 are applicable.

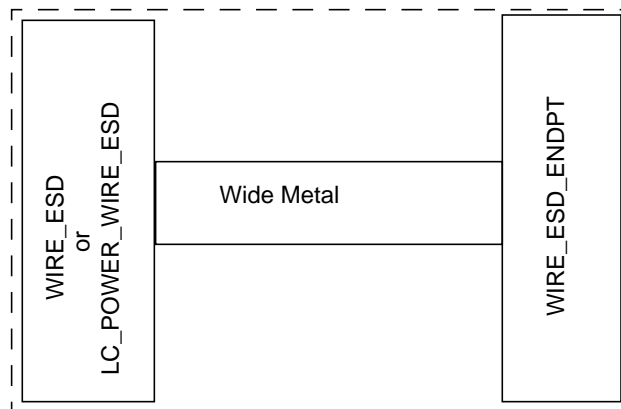


Figure 3-22. WIRE_ESD_ENDPT Text Label (Example)

3.12 ESDIODE Layout Rules

3.12.1 General

To keep the NW sheet resistance low enough, as well as the parasitic vertical pnp current gain, the blanket PW implant needs to be blocked from beneath the CMOS compatible P+/NW diodes and the NW/PW diodes but not from the N+/PW diodes. For this purpose, the layer ESDIODE is introduced.

Table 3-36. ESDIODE Layout Rules

Rule	Class	Notes	Description		Des Min.
BT00	a	-	ESDIODE width.	≥	1.00
BT02	a	-	ESDIODE space.	≥	1.00
BT02R	d	-	ESDIODE space.	≥	1.12
BT03a	a	-	ESDIODE to (PI expanded by 1.1μm) (for BT generation).	≥	1.00
BT03aR	d	-	ESDIODE to (PI expanded by 1.1μm) (for BT generation).	≥	1.12
BT04	b	-	ESDIODE to {BFMOAT, BB}.	≥	1.00
BT04R	d	-	ESDIODE to {BFMOAT, BB}.	≥	1.12
BT04a	b	-	ESDIODE touching BB not allowed.	≡	-
BT20	b	-	RX n+ junction to ESDIODE (RX n+ junction touching ESDIODE not allowed)	≥	1.0
BT21	b	-	RX p+ junction within ESDIODE	≥	0.5
BT22	a	-	NW within ESDIODE	≡	0.0
BT23	a	-	ESDIODE to JD (JD touching ESDIODE not allowed) (for BT generation)	≥	3.10
BT24	b	-	ESDIODE to (NS or DS ¹) (NS touching ESDIODE not allowed)	≥	6.00
BT25	b	-	ESDIODE to DT (DT touching ESDIODE not allowed)	≥	6.00
BT41	b	-	ESDIODE to (PC over RX)	≥	2.0
BT42	c	-	ESDIODE touching {PC, PCFUSE, VAR, DG, DI, (RX touching OP) } not allowed	≡	-
BT42b	c	-	ESDIODE touching RR not allowed	≡	-

1. (DS touching ESDIODE) not allowed is checked by Rule BT04a and DS5 and DS8.

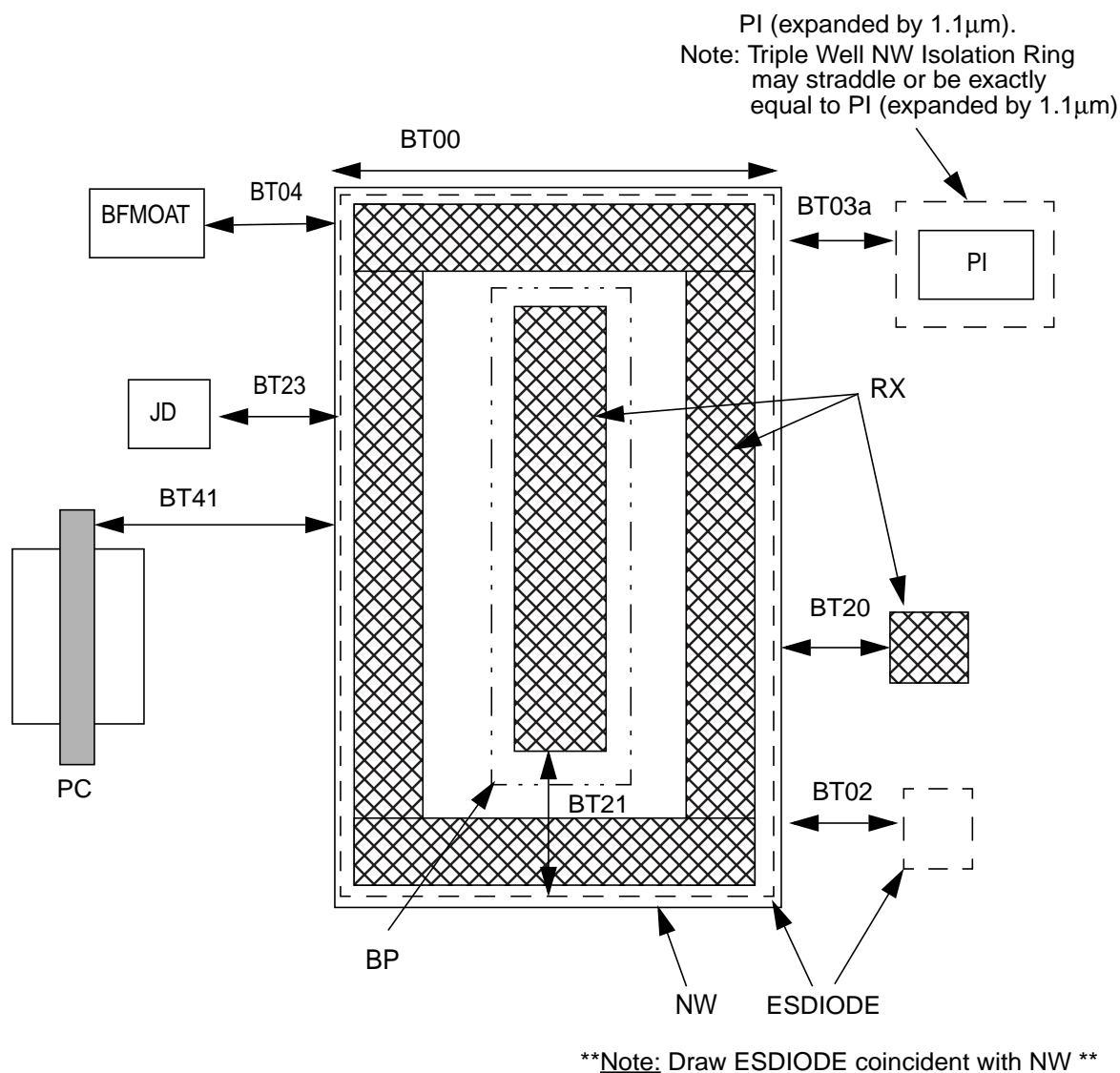


Figure 3-23. ESDIODE Layout Rules for p+/NW diode (ESDIODE drawn coincident with NW)

3.13 Forward-Biased Diode Layout Rules

The general use of forward-biased diodes as circuit elements is not supported. For compatibility with IBM technology offerings, layout rules for bandgap reference circuits employing forward-biased p-diffusions in a grounded n-well, using design level DI, are provided in the layout rules below. However, this device is not offered in the BiCMOS8HP technology (see section , "List of devices or features that are not supported in the

BiCMOS8HP technology.” on page 11. or section 4.6.3 , “Forward-Biased Diodes” on page 263). For additional information, contact your IBM Technical Representative.

The following rules apply to forward-biased diodes:

- Design a single diode as a “unit-cell” and duplicate the unit cell in a regular array at one chip location as necessary to achieve scaling of circuit components. This will assure closest matching.
- It is highly recommended to use the following unit cell: a 1.4 μm x 6 μm rectangle
- Surround each diode with a stripe of diffusion that will be the n-well contact. This n-well contact mesh should be connected to ground, as should a ring of p-diffusion substrate contact that surrounds the entire group of diodes as a guard ring. These two ground contacts assure low series resistance and isolation from other devices.
- connect the array of unit cells with a total area to provide the desired operating current. If exponential I-V dependence is critical to the application, the required current densities are provided in Section 4.6.3 , “Forward-Biased Diodes” on page 263. Note that the current density limits do not scale with technology layout rules; designing at a limit will hamper migration.

The level “DI” is required as a dummy level for forward-biased diodes. ESD diodes must be marked with the ESDUMMY level. These dummy levels are used for both DRC and LVS verification. Rules for implementing DI are tabulated below. See Section , “” on page 140 for other ESD diode design rules.

Table 3-37. DI Layout Rules

Rule	Class	Notes	Description		Des Min.
380	b	-	DI must be within BP.	\equiv	0.04
380a	b	-	(NW touching DI) to JD. (((NW touching DI) touching JD) not allowed).	\geq	5.00
380b	b	-	DI to {BB, DT, NS, DS, PI} (DI can not touch {BB, DT, NS, DS})	\geq	6.00
380c	b	-	(NW touching DI) touching PI not allowed	\equiv	-
380d	b	-	(NW touching DI) to RR ((NW touching DI) touching RR not allowed)	\geq	2.50
380g	b	-	(BP touching DI) touching PD not allowed	\equiv	-
381	b	-	RX within DI (minimum)	\geq	0.10
381b	b	-	RX within DI (maximum)	\leq	0.34
382b	b	-	RX nWell contact to DI	\leq	0.30

Table 3-37. DI Layout Rules

Rule	Class	Notes	Description		Des Min.
383	b	-	DI must enclose RX	≡	-
384	b	-	DI touching {DG, PC, OP} not allowed	≡	-
384a	b	-	(NW touching DI) touching {DG, PC, OP} not allowed	≡	-
385	b	-	RX width - (when RX is within DI)	≥	1.00
385a	b	1	(RX not over GRLOGIC) width (maximum) - (when RX is within DI)	≤	2.00
386	b	2	RX minimum length - (when RX is within DI)	≥	2.00
387	b	-	(RX within DI) must be within NW		-
387b	b	3	(NW touching DI) to RX substrate contact space - Maximum	≤	1.00
388	b	-	[RX nWell contact over (NW touching DI)] to BP	≥	0.12
389	b	-	[RX substrate contact over ((NW touching DI) sized by +1.00)] within BP	≥	0.12

1. The maximum width is limited to minimize current crowding in the structure that affects series resistance. Larger diode width can be used if the RX p+ anode is covered by a GRLOGIC shape, but these geometries are not represented by the IBM device model.

2. RX minimum length requirement applies to (RX within DI), for the allowable range of (RX within DI) widths that are specified in Rule 385 as well as Rule 385a. When (RX within DI) over GRLOGIC width exceeds 2.00μm, it is expected that (RX within DI) length complies with Rule 386.

3. Rule requires a substrate contact ring (((RX touching CA) not touching PC) over BP) not over {NW,BB}) to enclose the perimeter of this diode device defined by (NW touching DI) at a spacing that does not exceed the value specified.

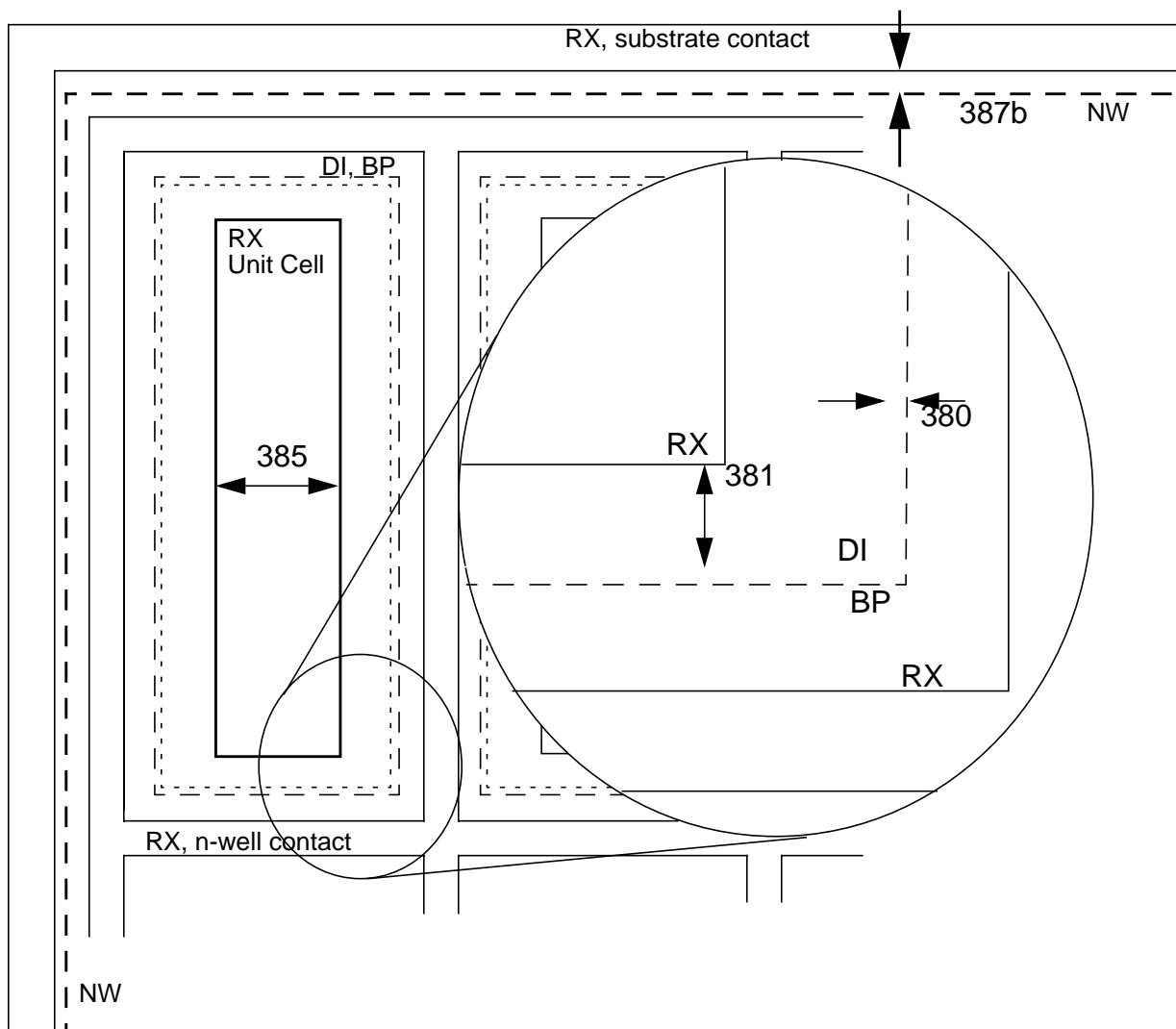


Figure 3-24. Forward-Biased Diode Layout Rules (The figure illustrates the layout for p-diffusion in grounded n-well diodes)

3.14 OP Resistor Layout Rules

The OP mask is used to block the formation of silicide, creating N+ diffusion and P+ poly resistors. Below are the rules used to form the OP diffusion and poly resistor.

Table 3-38. OP Resistor Layout Rules

Rule	Class	Notes	Description		Des. Min.	Wafer	Tol.
710	b	1	Diffusion resistor length (OP intersect RX).	\geq	0.44	0.4400	0.100
710R	d	1, 2	Diffusion resistor length (OP intersect RX)	\geq	1.60	1.6000	0.100
711	b	1	Diffusion resistor width (OP intersect RX)	\geq	0.20	0.1900	0.040
711R	d	1, 2	Diffusion resistor width (OP intersect RX)	\geq	1.50	1.4900	0.040
712	b	1	Poly resistor length (OP intersect PC)	\geq	0.80	0.8000	0.100
712R	d	1, 2	Poly resistor length (OP intersect PC)	\geq	1.60	1.6000	0.100
713	b	1	Poly resistor width (OP intersect PC)	\geq	0.20	0.1790	0.020
713R	d	1, 2	Poly resistor width (OP intersect PC)	\geq	1.50	1.4790	0.020
715a	b	-	((RX touching OP) not covered by GRLOGIC) N+ diffusion resistor to NW(N+ diffusion resistor must be outside NW)	\geq	0.35	0.1525	0.099
716a	b	-	(RX touching OP) must not touch NW	\equiv	-	-	-
716b	b	-	(RX touching OP) must not touch BB (straddling not allowed)	\equiv	-	-	-
716d	b	-	(OP intersect RX) must not touch BP	\equiv	-	-	-
716e	b	-	(OP intersect PC) must touch (BP or BB)	\equiv	-	-	-
717a	c	-	((PC intersect OP) covered by GRLOGIC) to (NW covered by GRLOGIC) space (for BH generation)	\geq	0.52	0.5200	0.15
717a1	c	-	((PC intersect OP) not over GRLOGIC) to (NW not over GRLOGIC) space (for BH generation)	\geq	0.63	0.4400	0.075
717b	c	-	(PC intersect OP) within NW (for PH generation)	\geq	0.52	0.5200	0.15
717c	c	-	(PC intersect OP) to (PC intersect OP) space (for PH, BH generation).	\geq	0.64	0.6400	0.10
725	a	-	OP width.	\geq	0.40	0.4000	0.100
726	a	-	OP to OP space.	\geq	0.40	0.4000	0.100

Table 3-38. OP Resistor Layout Rules

Rule	Class	Notes	Description		Des. Min.	Wafer	Tol.
727	b	-	OP overlap past RX	≥	0.18	0.2025	0.114
728	b	-	OP to RX	≥	0.16	0.1825	0.114
729a	a	-	OP area	≥	0.37	-	-
729b	a	-	OP enclosed area	≥	0.37	-	-
730	b	-	OP overlap past PC	≥	0.20	0.2105	0.127
730a1	b	-	OP to PB (OP over PB not allowed)	≥	0.29	0.2900	0.193
731	b	-	OP to PC (shapes can not abut)	≥	0.24	0.2505	0.127
732	b	-	{CA, CABAR} over OP is not allowed	≡	-	-	-
733	b	-	(CA over (RX or PC)) to adjacent (OP intersect (RX or PC))	≥	0.20	0.200	0.140
733R	d	-	(CA over (RX or PC)) to adjacent (OP intersect (RX or PC))	≡	0.20	0.200	0.140
733a	b	-	CABAR to OP	≥	0.360	0.360	0.144
734b	b	1	(RX touching OP) to BP	≥	0.20	0.2050	0.095
734c	b	-	(RX touching OP) to BB (see also Rule CP265b)	≥	0.420	-	-
735a	b	1	((PC touching OP) not touching BB) must be within BP	≥	0.25	0.2605	0.11
735a2	b	-	((PC touching OP) not touching BP ³) must be within BB	≥	0.30	0.3105	0.123
735a3R	d	-	((PC touching OP) not touching {BB, BP} not allowed	≡	-	-	-
735b	b	1	((PC touching OP) not over GRLOGIC) to adjacent BP	≥	0.30	0.3105	0.111
736	c	-	OP over (PC intersect RX) not allowed	≡	-	-	-
736a	c	4	RX(touching OP) touching PC not allowed	≡	-	-	-
736a1	c	-	RX(touching OP, not touching PC) touching SBLK not allowed	≡	-	-	-
736a2	c	-	PC(touching OP) touching SBLK not allowed	≡	-	-	-
736a3	b	-	SBLK must touch OP	≡	-	-	-

Table 3-38.OP Resistor Layout Rules

Rule	Class	Notes	Description		Des. Min.	Wafer	Tol.
736b	b	4	RX(touching OP) touching PB not allowed	≡	-	-	-
737	c	1	OP shapes touching DG - not allowed	≡	-	-	-
737aR	d	1	((RX not touching {SBLK, PC, GRLOGIC}) touching OP) touching DG - not allowed	≡	-	-	-
738	c	1	(OP intersect (RX or PC)) must be rectangular	≡	-	-	-
738b	c	-	OP over RX must divide the RX into two separate diffusions; OP over PC must divide the PC into two separate poly regions.	≡	-	-	-
739a	c	-	RX overlap past OP	≥	0.45	0.4450	0.11
739aR	d	-	RX overlap past OP	≡	0.46	0.4550	0.11
739b	c	-	PC overlap past OP	≥	0.42	0.4095	0.13
739bR	d	-	PC overlap past OP	≡	0.46	0.4495	0.13
OP5	b	-	OP to adjacent NP	≥	0.68	0.6800	0.2378
OP9	c	-	OP to adjacent PD (resistors)	≥	0.44	0.2800	0.147
OP9a	b	-	OP(over RR) overlap of PD (resistors)	≡	0.380	0.5160	0.147
OP20	c	-	OP to adjacent RN (resistors)	≥	0.600	0.300	0.162
OP24	c	-	OP touching RX (over RN) not allowed				
OP25	c	-	OP touching EX not allowed				
OP29	c	-	PC(touching OP) not allowed to touch RX				
OP30	c	-	((((PC over OP) over NW) not over GRLOGIC) to RX	≥	0.320	-	-
OP31	c	-	((((PC over RX) over NW) not over GRLOGIC) to {diff- erence [intersection (OP, PC), (RX sized by +0.20)] sized by +0.12}	≥	0.320	-	-
OP35	c	-	(RX intersect OP) touching PX not allowed				

Table 3-38. OP Resistor Layout Rules

Rule	Class	Notes	Description		Des. Min.	Wafer	Tol.
PBR14R	d	-	PC(touching OP) within the perimeter of the DT_LATTICE ⁵ . (Note that the perimeter of the DT maze must overlap past the PC).	≥	0.280	0.2705	0.091
PBR19	c	⁴	No more than 1 set of contacts allowed on any resistor (no center-tapping allowed!) (only1 OP allowed per resistor => no center tapping of resistor body!)				
PBR29	c	-	PC(touching OP, not over GRLOGIC) within NW(not over DT) (to keep the NW fully viewable under the resistor body)	≥	2.000	2.0705	0.114
PBR31	c	-	PC(touching OP, touching BB) within BB(not over DT ⁶) (to keep the BB fully viewable under the resistor body)	≥	2.000	1.9505	0.126
PBR33	c	-	PC(touching OP, not touching NW, not over GRLOGIC) to adj NW (to keep the pwell fully viewable under the resistor body) (abutting not allowed)	≥	2.000	1.9505	0.114
PBR35	c	-	PC(touching OP, not touching BB) to adj BB (to keep the pwell fully viewable under the resistor body)	≥	2.000	2.0705	0.126
PCR20	c	^{7,8}	PC(touching OP, touching NS) to adjacent DT	≥	0.400	0.4305	0.091
PCR20a	c	^{1, 2}	PC(touching OP) within NS	≥	0.720	2.2230	0.287
PCR20b	c	-	PC can not touch DS				
PCR21R	-	-	Rule Deleted				
PCR21a	-	-	Rule Deleted				
PCR22	-	-	Rule Deleted				
PCR23	c	-	((OP over PC) touching PD) must divide the PC into 2 separate shapes (in order to dope the two ends of the OP RR PH resistor).				

1. Approved IBM ESD structures covered by (ESDUMMY or ESD_CDM) are exempt from this rule. See also ESD specific rules Section , "" on page 140.
2. For details on the OP recommended rules, see Section 4.7 , "Resistor Models" on page 265
3. BP in this rule is BP dg (drawn BP). It is not intended to be checked to BP generated from the BB design level per Table 2-6, "Shape Manipulation Prior to Mask Write" on page 44.
4. Approved IBM ESD structures ((OP intersect RX) touching SBLK) are exempt from this rule. See also ESD specific rules Section , "" on page 140.

5. DT Lattice in Rule PCR21a is not a dummy design level. The term DT Lattice is a pseudo-generated level in DRC that refers to any lattice of DT with an area of the hole formed by the DT being less than $3.00\mu\text{m}^2$. DT below the poly resistor is not a supported feature in the BiCMOS8HP technology.
6. The BB(not over DT) part of the rule does not include DT_LATTICE structures.
7. These rules also refer to PC resistors which use the NS bed (always tied to highest DC potential) under them.
8. To keep the NS or NW fully viewable as an AC ground plane under the PC resistor. The NS or NW is normally tied to the highest DC potential. See Section 3.8.3 , “NS Design Rules, Ground Planes and Beds” on page 130.

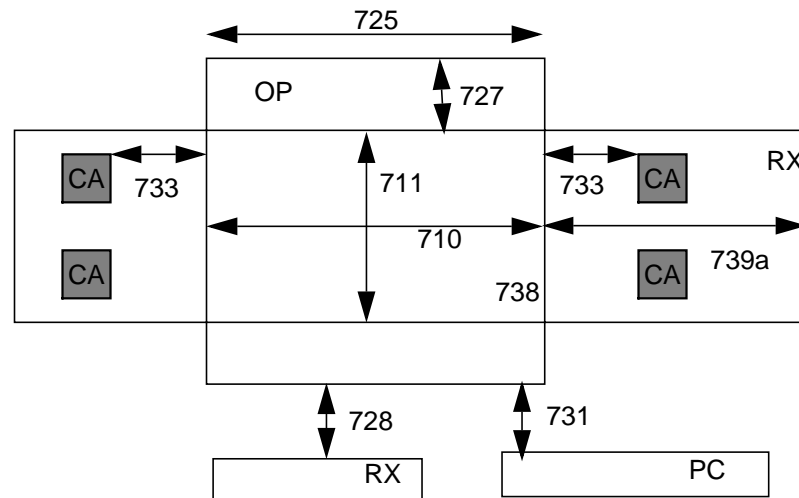


Figure 3-25. Layout for OP N+ Diffusion Resistor

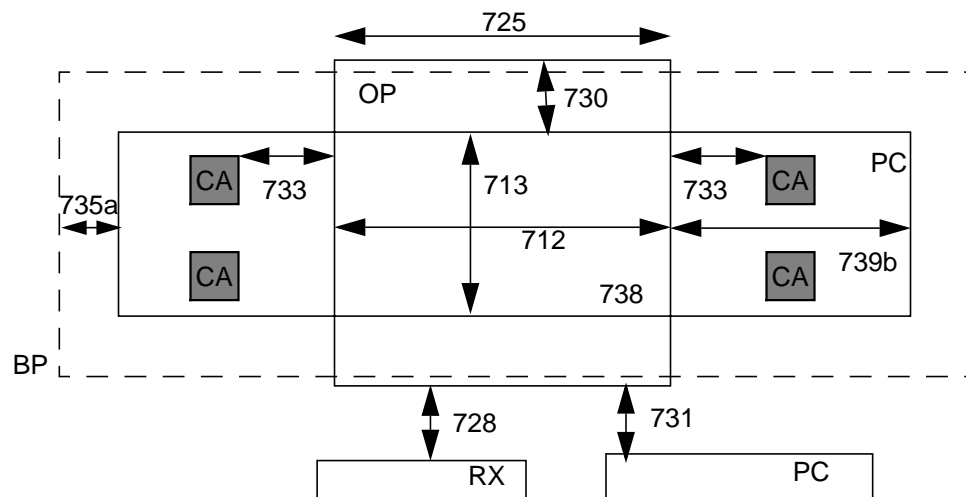


Figure 3-26. Layout for OP P+ Polysilicon Resistor

3.15 NS Subcollector Diffused Resistor

Below are the rules used to form the NS subcollector diffused resistor. For electrical characteristics see Section 4.14.1, “Conducting Film Thickness” on page 282, for the model see Section 4.7, “Resistor Models” on page 265

Table 3-39. NS Resistor Layout Rules							
Rule	Class	Notes	Description		Des Min	Wafer	Tol.
PCR19a	c	-	No more than 2 RX(touching RN) contacts allowed on { NS (touching NSR, not touching PC, not touching PD) not over DT} (the NS res.) (no center tapping allowed!).				
PCR24	c	-	{ NS(touching NSR, not touching PC, not touching PD) not over DT} touching NW not allowed (the NS resistor can not touch NW).				
PCR25	c	-	NSR must be covered by NS.				

3.16 PD Layout Rules

Table 3-40. PD Layout Rules							
Rule	Class	Notes	Description		Des Min.	Waf. Dim.	Tol.
PD1	a	-	PD width ¹	≥	0.340	0.3400	0.075
PD2s	a	-	PD space ¹	≥	0.340	0.0680	0.085
PD4	b	-	PD to adjacent (RX not over OZ) (shapes cannot abut).	≥	0.360	0.365	0.095
PD4aa	b	-	PD to adjacent RX (shapes cannot abut).	≥	0.140	0.148	0.115

Table 3-40. PD Layout Rules

Rule	Class	Notes	Description		Des Min.	Waf. Dim.	Tol.
PD6	b	-	(RX not over OZ) within PD.	≥	0.200	0.205	0.110
PD6a	b	-	(RX over OZ) within PD.	≥	0.140	0.148	0.115
PD7	b	-	PD overlap past PC.	≥	0.280	0.2905	0.111
PD8a	b	-	PD to adj NP((NP touching PD) not allowed).	≥	0.430	0.430	0.230
PD9	b	-	PD must be orthogonal.				
PD10a		-	PD to adj PC (abutting not allowed).	≥	0.280	0.2905	0.111
PD10b	b	-	PD to adj PB (abutting not allowed) ((PB touching PD) not allowed).	≥	0.380	0.380	0.183
PD11	a	-	PD enclosed area (μm^2)(min resist island).	≥	0.320	-	-
PD12	b	-	PD touching DS not allowed.				

1. PD is not a mask level, it is a design level used for Data Preparation. PD is merged onto the BN mask. See Mask Level BN, Design Level PD in Table 2-1, "Mask and Design Level Definitions" on page 25 and Mask Level BN in Table 2-6, "Shape Manipulation Prior to Mask Write" on page 44. PD min width and space specified in this table is larger than BN minimum width and space for the technology by design. However, the technology minimum BN limits are specified in GR 358d and 358e in Table 3-7, "BP Layout Rules" on page 90.

3.17 OP RR Resistor (RR) Layout Rules

Table 3-41. RR Layout Rules

Rule	Class	Notes	Description		Des Min.	Waf. Dim.	Tol.
RR1	a	-	RR width.	≥	0.800	0.800	0.105
RR2	a	-	RR space.	≥	0.800	0.800	0.105
RR3	c	-	RR must be orthogonal.				
RR4a	b	-	(PC touching OP) within RR.	≥	0.260	0.2705	0.157

Table 3-41. RR Layout Rules

Rule	Class	Notes	Description		Des Min.	Waf. Dim.	Tol.
RR5	b	-	RR to adj PC.	\geq	0.280	0.2905	0.157
RR5a	b	-	RR to (PC over RX).	\geq	0.400	0.3424	0.157
RR6	b	-	RR to adj PB (RR touching PB not allowed).	\geq	0.400	0.4000	0.214
RR7	b	-	RR to adj RX (RX touching RR not allowed).	\geq	0.280	0.2850	0.146
RR8	b	-	BP within RR.	\geq	0.000	0.0000	0.172
RR9	b	-	(BP touching RR) can not touch {(PC not touching RR), PB, BB}.				
RR9aR	d	¹	(OP touching RR) overlap of PD.	\equiv	0.380	0.5160	0.147
RR10a	c	-	(PC not touching OP) can not touch RR.				
RR11	b	-	(CA over RR) must be covered by PD.				
RR14a	c	-	RR touching ESDIODE not allowed.				
RR14b	c	-	RR touching DG not allowed.				
RR15	b	-	((PC touching OP) touching RR) width (minimum.)	\geq	0.740	0.719	0.022
RR24	c	-	RR to adj NS.	\geq	4.000	1.2700	0.316
RR26	c	-	RR to adj DS (DS touching RR not allowed).	\geq	4.000	1.2700	0.316
RR27	c	-	RR touching PX not allowed.				
RR40R	d	²	((PC touching OP) over RR) must be within {BP, BB}.	\geq	0.400	0.4105	0.111

1. See Rule OP9a (see Table 3-38, "OP Resistor Layout Rules," on page 158) for the OP RR Resistor.

2. See Rule PBN10. Rule PBN10 supersedes Design Min in Rule 735a or 735a2 (see Table 3-38, "OP Resistor Layout Rules," on page 158) for the OP RR Resistor.

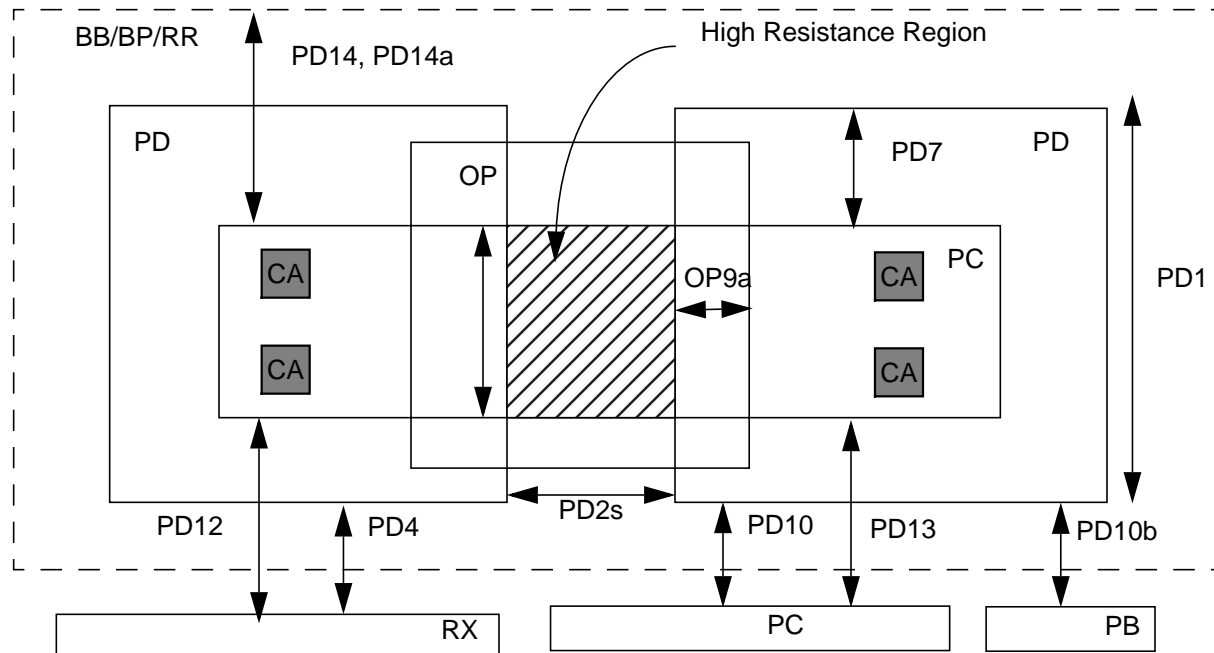


Figure 3-27. OP RR Resistor Layout Rules

3.18 KQ Resistor Layout Rules

Below are the rules used to form the KQ resistor between the MQ and LY design levels. For the model see Section 4.7 , “Resistor Models” on page 265.

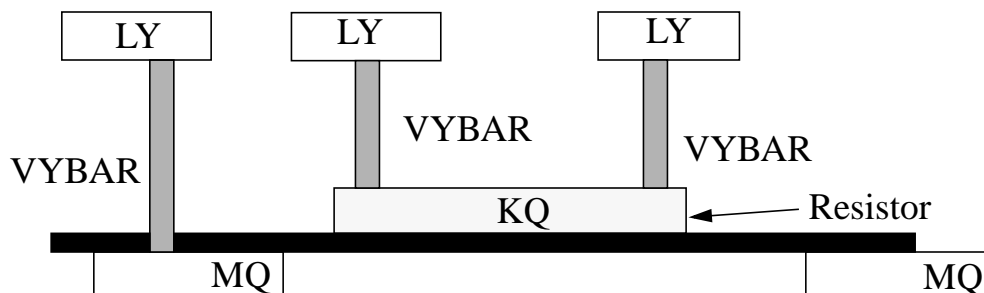


Figure 3-28. Cross Section of the BEOL Resistor (KQ) structure.

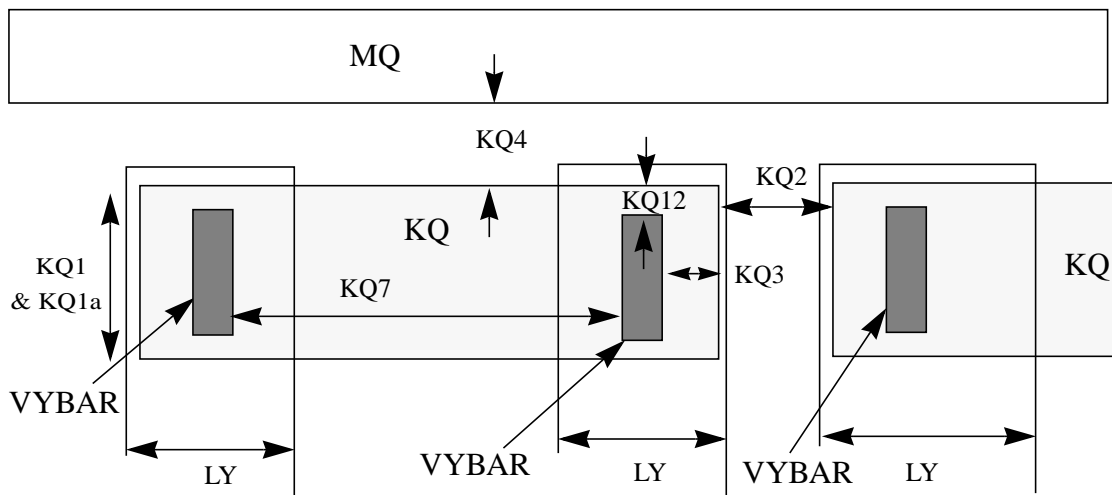


Figure 3-29. Layout for BEOL (KQ) Layout

Table 3-42. KQ Resistor Layout Rules							
Rule	Class	Notes	Description		Des Min	Wafer	Tol.
KQ1	a	-	KQ width (minimum).	\geq	5.00	5.00	0.14
KQ1a	c	-	KQ width (maximum).	\leq	30.00	-	-
KQ2	a	-	KQ space.	\geq	5.50	5.50	0.14
KQ2a	a	-	VY (1.24 x 1.24 point vias) must not touch KQ (VYBAR to be used to connect KQ to LY).				
KQ3	b	-	VYBAR within KQ (The via used to connect KQ to LY must be VYBAR vias, 1.24 x L).	\geq	1.100	1.1013	0.638
KQ4	b	-	KQ to MQ space. (KQ touching MQ not allowed).	\geq	1.250	1.250	0.311
KQ4a	b	-	KQ to (MQ over MQPLANE) space. (KQ touching (MQ over MQPLANE) not allowed).	\geq	10.00	-	-
KQ5	c	-	No more than 1 set of VYBAR bar vias allowed on KQ resistor (no center-tapping allowed).				
KQ7	b	-	KQ minimum length (measured as (VYBAR over KQ) to (VYBAR over KQ) space).	\geq	5.00	5.00	0.240
KQ8	c	-	KQ shapes must be rectangular. 45° KQ shapes not allowed.				

Table 3-42.KQ Resistor Layout Rules

Rule	Notes	Description		Des Min	Wafer	Tol.
KQ9	c -	KQ to QY space. (KQ touching QY not allowed).	≥	5.00	5.00	0.688
KQ9a	c -	KQ to IND_FILT space (KQ touching IND_FILT not allowed).	≥	10.00	-	-
KQ10	- 1,2,3	Rule Deleted. This rule has been superseded by EPDL_MQ_min.	≥	10.00	-	-
KQ11R	d -	(VYBAR touching KQ) to (VYBAR touching KQ) space on the same connection end of the resistor (see Rule KQ7 for via spacing to other end of the resistor); (see also Rule VY4).	≡	2.00	2.00	0.050
KQ14R	d 4	KQ touching TRANSMIS is prohibited.	≡	-	-	-

1. This rule is equivalent to the checking that is performed per Rule PD4a, for the MQ design level when a KQ BEOL resistor is present or in the event that an IBM reserved MQEXCLUDE dummy design were present within CHIPEDGE, after IBM design services is completed during the typical IBM release process (see Table H-3, "Pattern Density Rules," on page 425). This rule is included and verified in the design kit, to "predictively estimate" the resulting MQ local pattern density that will occur in the final chip design, after IBM design services is applied, to assist designers with KQ BEOL Resistor placement so that the MQ local density requirements that are necessary for Back-End-Of-Line manufactureability can be achieved. Graphical representation of the individual MQFILL shapes is not provided, rather a summary of the predicted density results is reported. Rule KQ10 predictively checks the resulting MQ local density since KQ resistors, when implemented in a physical chip design, result in local 0% MQ density regions where KQ resistors are placed. The KQ design level, like the IBM reserved MQEXCLUDE design level, intentionally prohibit MQFILL placement. Since MQFILL, as well as user designed MQ level, are both prohibited from touching KQ resistors, placement of KQ resistors create lower than normal MQ local density regions in a chip design compared to regions (local areas) where KQ resistors are not present. However, Rule PD4a local MQ pattern density criteria must still be met inclusive of the KQ BEOL resistors placed in a chip design. For example, if a KQ resistor is used, IBM auto-generated MQFILL is not located below the KQ resistor body, which depending on placement and spacing to other KQ BEOL resistors, or other features of the technology that affect normally applied IBM auto-generated MQFILL, low MQ density errors may result when checking for Rule PD4a occurs during the IBM release process, which is not acceptable for manufactureability. If the predictively checked Rule KQ10 or PD4a local density errors result, and by inspection of the chip layout (by the designer) it is determined to be a result of KQ resistor inclusion or placement, IBM recommends that KQ resistor widths be reduced, or KQ resistors be spaced further from other design levels that also intentionally generate low MQ pattern densities, such as the dummy design & utility levels such as BOND PAD, IND_FILT or TLINE or LOGOBND, or if multiple KQ resistors are placed in close proximity to each other, then KQ resistors should be spaced far enough apart to satisfy the design kit Rule KQ10 (MQ) local pattern density checking results without errors. Requests for waivers to Rule KQ10 or PD4a may not be accepted by IBM, if determined to be attributed solely to KQ resistor placement.

2. If MQ shapes are added by designers, MQ shapes are not allowed under KQ shapes and the MQ shapes added shall be spaced from KQ shapes per rule KQ4. This practice is not recommended. IBM generated MxFILL shapes added near the KQ resistor design level, will be in accordance with Copper Pattern Density and Layout Requirements, defined in Rule DS525e in Table H-3, "Pattern Density Rules," on page 425.

3. In the design kit, the actual Design Minimum value is verified to the design minimum value of 15% in lieu of the specified 10% value in the table for Rule KQ10, to account for any potential tool-to-tool variation between the “predicted” density value and the actual density that results after the IBM design services process is completed as part of the IBM release process. IBM strongly recommends designers adhere to the design kit verification result of this rule, even though it is slightly more restrictive than the actual rule limit, to avoid evidencing local density violations during the final design release process, which could result in design submission delay. Additional note to designers: The design may expect CHIPEDGE to be present for these checks to function accurately. Therefore, designers should verify that a CHIPEDGE design level is present in their layout during the local density verification process, to achieve the most accurate predictive MQ local pattern density checking for this layout rule.
4. KQ BEOL resistors should not straddle through transmission line devices.

3.19 BFMOAT Design Rules

The BFMOAT level may be used to layout a ring of resistive substrate area that is useful in reducing the coupling of substrate noise between regions on the same chip. Section 4.15 , “Electrical Moat Parameters” on page 294 provides the amount of resistance given for various moat lengths (BFMOAT width). Section H.1 , “xxFILL and xxHOLE Generation” on page 417 provides BFMOAT pattern file rules.

Table 3-43. BFMOAT Layout Rules¹

Rule	Class	Notes	Description		Des Min.	Waf. Dim.	Tol.
790	c	-	BFMOAT width	≥	10.00	-	-
792	c	-	BFMOAT space	≥	10.00	-	-
793	c	-	BFMOAT to adjacent NW space	≥	2.00	-	-
795	c	-	BFMOAT to adjacent RX space	≥	1.00	-	-
797	c	-	BFMOAT to (PC over RX)	≥	3.00	-	-
797c	c	-	BFMOAT to BB (BFMOAT touching BB not allowed)	≥	2.00	-	-
799	b	-	{RX, PC, NW, NS, DS, RN, BB, BX, PB, PX, PI, JD, CEBAR, CABAR, CA, M1} touching BFMOAT - NOT ALLOWED M1 shapes that do not touch (CA or CABAR or CEBAR) or V1) (floating M1) are allowed to touch BFMOAT. Consult your IBM technical representative.				

1. All these rules, may be modified for the beta design kit.

3.20 DG Layout Rules

For IO circuits and peripheral circuits, see Section 3.36 , “Latchup Guidelines, Layout Constraints, and Rules” on page 221.

Table 3-44. DG Layout Rules¹

Rule	Class	Notes	Description		Des Min.	Waf. Dim.	Tol.
DG1	c	-	DG must be orthogonal.	≡	-	-	-
DG1b	c	-	NW touching DG must be orthogonal.	≡	-	-	-
DG1c	c	-	Intersection(DG,NW) touching VAR must be orthogonal.	≡	-	-	-
DG2R	d	-	(PC over RX) touching DG must be orthogonal.	≡	-	-	-
DG2bR	d	-	RX touching DG must be orthogonal.	≡	-	-	-
DG3	b	-	(PC vertices touching DG) to RX space.	≥	0.08	0.0955	0.064
DG4	b	-	(PC over RX) within DG	≥	0.50	0.4424	0.132
DG5	b	-	(PC over RX) to DG	≥	0.50	0.4424	0.132
DG6	a	-	DG ² width	≥	0.40	0.4000	0.122
DG7	a	-	DG space and notch	≥	0.40	0.4000	0.122
DG8a	b	-	[(PC over RX) over DG] width for NFET device Leff	≥	0.24	0.300 ³	0.060
DG8a45	b	-	[(PC over RX) over DG] width for 45° NFET device Leff	≥	0.26	0.2400	0.034
DG8b	b	-	[(PC over RX) over DG] width for PFET device Leff	≥	0.24	0.2140 ³	0.034
DG8b45	b	-	[(PC over RX) over DG] width for 45° PFET device Leff	≥	0.26	0.2340	0.034
DG8c	b	-	(((PC to PC) over RX) over DG) - spacer to spacer	≥	0.30	0.1847	0.026
DG8cR	d	-	(PC touching DG) minimum space to adjacent PC	≥	0.30	-	-
DG9	a	-	DG overlap past NW (for DE level derivation)	≥	0.40	-	-
DG13	a	-	DG to NW space (for BH derivation)	≥	0.40	-	-
DG13a	a	-	DG to {BB,BH} space (for BH derivation)	≥	0.40	-	-
DG14	a	-	DG overlap NW (for DF derivation)	≥	0.40	-	-
DG15	a	-	DG to (OP intersect PC) (for BH derivation)	≥	0.52	-	-

Table 3-44. DG Layout Rules¹

Rule	Class	Notes	Description		Des Min.	Waf. Dim.	Tol.
DG16	a	-	NW overlap past DG (for PH derivation)	≥	0.40	-	-
DG21	b	-	(DG touching (RX not touching RN)) can not touch BB				
DGBB1	b	-	DG to BB (DG can not touch BB)	≥	2.00	-	-
DGBX1	b	-	DG to BX (DG can not touch BX)	≥	1.00	-	-
DGJD1	b	-	DG to JD (DG can not touch JD) (for PH generation)	≥	3.00	-	-
DGNS1	b	-	DG to NS (DG can not touch NS)	≥	1.00	-	-
DGDS1	b	-	DG to DS (DG can not touch DS)	≥	1.00	-	-
DGPBN1	b	-	DG to PB (DG can not touch PB)	≥	1.00	-	-
DGPX1	b	-	DG to PX (DG can not touch PX)	≥	1.00	-	-
DG50	c	-	[(RX over PC) over DG] width for device Weff	≥	0.36	-	-
DG52	b	-	(RX touching DG) to RX	≥	0.22	0.2170	0.040
DG110	c	-	((RX over DG) overlap past PC) (Checked as <i>outside edge</i> of PC to <i>inside edge</i> of RX)	≥	0.25	0.2170	0.040
DG110a	c	-	(((RX straddling DG) overlap past PC) not over GRLOGIC) Note: Rule DG110a only applies to RX (diffusion) overlap past PC (gate edge) on the same Thick Oxide FET whether DG covers the entire RX diffusion, or RX diffusion straddles DG.	≥	0.60	0.5670	0.040
DG252R	d	4	NW to NW space - if either NW shape touches DG	≥	1.30	-	-
DG260	b	-	((RX P+ junction ⁵) touching DG) within NW	≥	0.50	0.5825	0.099
DG265a	b	-	((RX N+ junction ⁵) touching DG) to adjacent NW	≥	0.50	0.805	0.200
DG265a1	b	-	((RX N+ junction ⁵) touching DG) to adjacent BB	≥	0.50	0.805	-
DG265b	b	-	(RX N+ junction ⁵) to adjacent (NW touching DG)	≥	0.50	0.805	0.200
DG268a	b	-	(RX P+ Junction touching DG) to RX N-well Contact for no latchup	≤	15.00	-	-

Table 3-44. DG Layout Rules¹

Rule	Class	Notes	Description		Des Min.	Waf. Dim.	Tol.
DG268b	b	-	(RX N ⁺ Junction touching DG) to RX Substrate Contact outside of {NW,BB,BFMOAT,JD} for no latchup. Note that DT is a blocking shape since a DT fence between an N+ Junction and its Pwell Substrate Contact can cause the path length between them to exceed the maximum given in Rule. {NW, BFMOAT, BB, JD} are also blocking shapes between an N+ Junction and its Pwell Substrate Contact and can cause the path length between them to exceed the maximum given in Rule.	≤	14.00	-	-

1. All these rules, may be modified for the beta design kit.
2. It is *strongly recommended* that shapes on levels involving pre-mask data preparation (DPREP) *difference* functions be placed at the same cell nesting hierarchy in the design data. Examples of these levels are NW and DG; see Data Preparation Section
3. This is an effective electrical value, not a physical on-wafer dimension.
4. This is strongly recommended for a Nwell to Nwell potential difference $\geq 2.5V$
5. The N+ and P+ junctions in these rules must include the gate area (RX) under the PC for these rules.

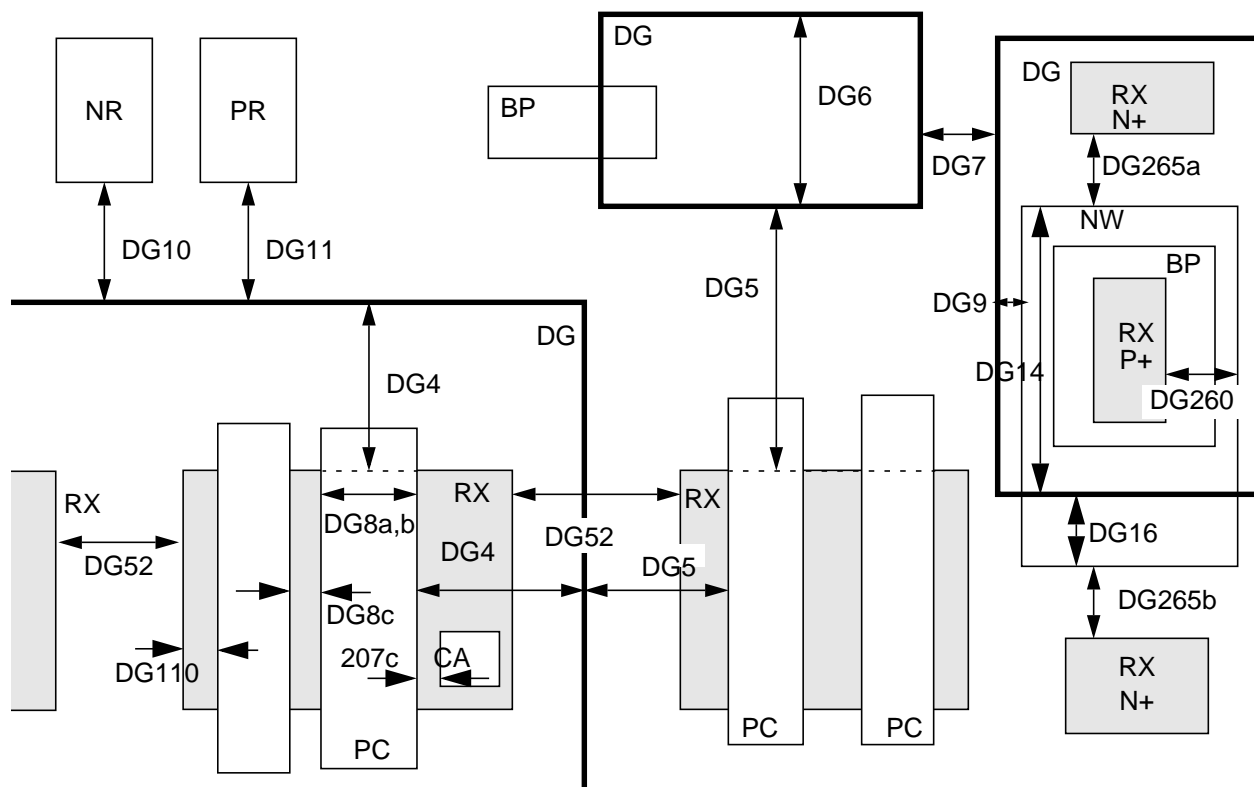


Figure 3-30. Dual Gate (DG) Oxide Rules

3.21 nFET-in-Nwell (VAR) Device Layout Rules

The decoupling capacitor and varactor are a capacitor that consists of an N+ poly gate electrode and an N-well contacted through N+ diffusions.

In rules 'VAR1a', gatlength refers to PC length while in rules 'VAR10a' it refers to RX width.

Table 3-45. Varactor Layout Rules

Rule	Notes	Description		Des Min.
VAR0	a	-	VAR width	≥ 0.68
VAR1a	a	-	((PC over RX) over VAR) min width gatlength	≥ 0.24
VAR1aR	d	-	((PC over RX) over VAR) exact width gate length	≡ 1.0
VAR1b	c	-	((PC over RX) over VAR) max width gate length	≤ 10.0

Table 3-45. Varactor Layout Rules

Rule	Class	Notes	Description		Des Min.
VAR10a	a	-	((RX width under PC) over VAR) min width gate width.	\geq	1.0
VAR10aR	d	-	((RX width under PC) over VAR) exact width gate width.	\equiv	10.0
VAR10b	c	-	((RX width under PC) over VAR) max width gate width.	\leq	32.0
VAR2	a	-	VAR to VAR space.	\geq	0.92
VAR2b	c	-	VAR shapes must be orthogonal.	\equiv	-
VAR5	c	-	VAR overlap past RX.	\geq	0.30
VAR6	c	-	VAR must enclose NW.	\geq	0.00
VAR6b	b	-	NW cannot straddle VAR.	\equiv	-
VAR7	b	-	BP touching VAR not allowed.	\equiv	-
VAR8	b	-	(RX over VAR) must be within NW.	\equiv	-
VAR11	a	-	DG to VAR space (for BH and DE generations).	\geq	0.40
VAR11c	a	-	DG overlap past VAR (for dataprep).	\geq	0.40
VAR12	a	-	NW to VAR space (for BH generations).	\geq	0.40
VAR14	a	-	(PC over OP) to VAR space (for BH generations).	\geq	0.56
VAR29	c	-	(PC over RX) within VAR.	\geq	0.4
VAR30	c	-	(PC over RX) to VAR.	\geq	0.5

3.22 Triple Well (Isolated) NFET Layout Rules

The PI level along with an NW ring forms the N type isolation for the isolated pwell of a triple well NFET device. All FET rules also apply to the Triple Well. PFETs are not supported in the isolated Pwell or allowed within the NW over the PI isolation design level per Rule TW260.

Table 3-46. Triple Well nFET Rules

Rule	Class	Notes	Description		Des Min	Wafer	Tol.
TW00	a	-	PI touching greater than one (PI not NW) is prohibited.	=	-	-	-
TW01	a	-	PI width.	≥	2.100	2.1000	0.208
TW02	a	-	PI space (including notch).	≥	1.000	1.0000	0.208
TW03	c	-	PI shapes must be orthogonal.				
TW04	b	-	PI edges must be covered by NW (all edges).				
TW05	b	-	PI overlap of NW.	≥	0.400	0.400	0.189
TW06	b	-	NW overlap past PI.	≥	1.100	1.100	0.189
TW07	c	-	RX can not straddle PI.				
TW07a	c	-	{(PC intersect RX), (PC touching OP) } touching (NW intersect (PI expanded by +1.1um)) not allowed. {((PC intersect RX), (PC touching OP) } straddling (NW intersect (PI expanded by +1.1um)) not allowed).				
TW08	c	-	PI touching {DI,VAR} not allowed.				
TW10	c	-	NW ring must have at least one RX(not over PI) NW contact (NW ring around the PI triple well tub must have at least one RX NW contact that is not over the PI which contains Pwell. RX NW contact abutting PI not allowed).				
TW12	a	-	(NW over PI) minimum spacing and notch.	≥	1.300	1.300	0.208
TW13	a	-	PI to BFMOAT (PI touching BFMOAT not allowed) (for BF and BT generation).	≥	3.100	3.1000	0.205
TW13a	c	-	PI to BB (PI touching BB not allowed).	≥	3.100	3.1000	0.205
TW13d	c	-	PCFUSE touching PI not allowed.				
TW13f	c	-	{ESDIODE, ESDUMMY, ESD_CDM} touching PI not allowed.				
TW13g	c	-	{ NS, PB, PD, PX, RN } touching PI not allowed.				

Table 3-46. Triple Well nFET Rules

Rule	Class	Notes	Description		Des Min	Wafer	Tol.
TW14	c	-	PI to JD space (PI touching JD not allowed).	\geq	4.600	4.5500	0.310
TW15	c	-	PI to adj NW (for NW that is not straddling PI edges).	\geq	2.020	-	0.223
TW16	c	-	PI to adj (PC intersect OP).	\geq	1.750	1.7605	0.192
TW19	c	-	(PI not over NW) must touch (RX over BP) to insure triple well contact.				
TW110a	b	-	((RX overlap past PC) over PI) (silicide width). (Checked as <i>outside edge</i> of PC to <i>inside edge</i> of RX except for floating gate tie-down shapes. See <i>one</i> example in Figure 3-1, "Isolation and Polysilicon Rules" on page 78. Note: Rule TW110a only applies to RX (diffusion) overlap past PC (gate edge) on the same Triple Well FET.	\geq	0.55	0.4699	0.065
TWDG110a	c	-	((RX straddling DG) overlap past PC) over PI Note: Rule TWDG110a only applies to RX (diffusion) overlap past PC (gate edge) on the same Triple Well Thick Oxide FET whether DG covers the entire RX diffusion, or RX diffusion straddles DG.	\geq	0.60	0.5670	0.040
TW134	b	-	All triple wells (PI not NW) must touch RX, which is electrically connected to M1 to a (RX not over (PI or NW or JD or BFMOAT or BB or BX or PX)) OR (RX over (NW which is tied down (see Rule DT267 or 134))).				
TW260	b	-	RX P ⁺ Junction ¹ to adjacent PI ((RX over BP) over NW) touching PI not allowed (for BT spacing to P+ junction).	\geq	2.320	2.3425	0.184
TW260a	b	-	((RX P ⁺ Junction ¹) over DG) to adjacent PI ((RX over BP) over NW) touching PI not allowed (for BT spacing to P+ junction).	\geq	2.580	2.6025	0.184
TW261	b	-	RX NW contact to PI (RX NW contact can not touch PI, RX NW contact abutting PI not allowed).	\geq	0.290	-.0542	0.541
TW265	b	-	(RX N+ junction ¹ over PI) min space to NW.	\geq	0.460	0.4225	0.099
TW265a	b	-	((RX N+ junction ¹) touching DG) over PI) min space to NW.	\geq	0.600	0.5625	0.099

Table 3-46. Triple Well nFET Rules

Rule	Class	Notes	Description		Des Min	Wafer	Tol.
TW265b	b	-	(RX N ⁺ Junction ¹ not over PI) to adjacent (NW touching PI) (where the RX does not intersect the (NW touching PI))	≥	0.560	0.5225	0.099
TW265c	b	-	((RX N ⁺ Junction ¹) touching DG) not over PI) to adjacent (NW touching PI) (where the (RX touching DG) does not intersect the (NW touching PI))	≥	0.940	0.9025	0.099
TW266	b	-	(RX triple-well contact over PI) min space to NW	≥	0.290	0.3125	0.099
TW266a	b	-	((RX Substrate Contact) not over PI) to (NW touching PI)	≥	0.120	0.0825	0.099
TW268b	b	-	(RX N+ junction over PI) maximum distance to RX triple-well contact [for no latchup]	≤	15.00	-	-
TW268c	b	-	((RX N+ junction over PI) over DG) maximum distance to RX triple-well contact [for no latchup]	≤	10.00	-	-

1. The N+ and P+ junctions in these rules must include the gate area (RX) under the PC for these rules.

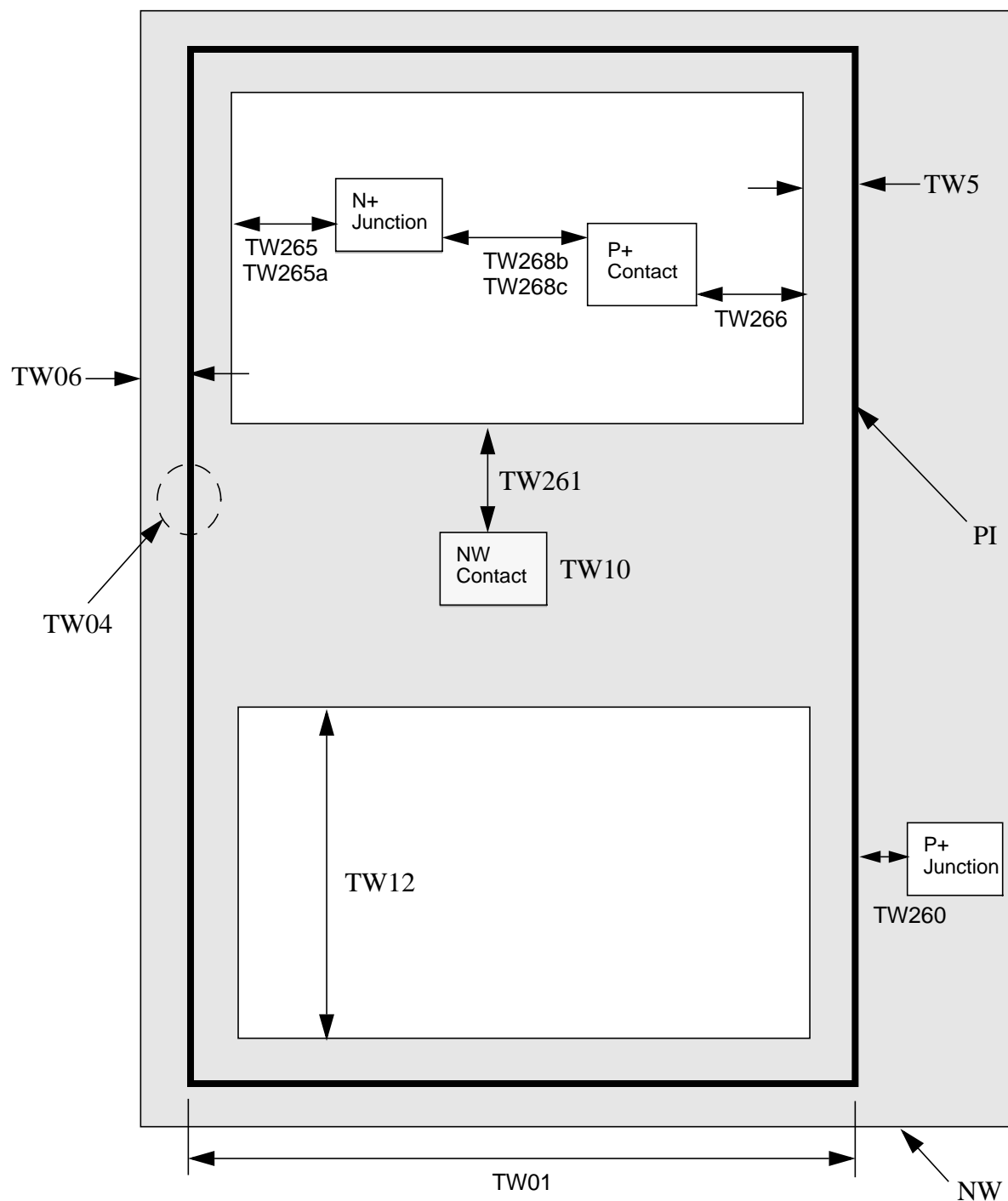


Figure 3-31. Triple Well NFET (Single PI shapes)

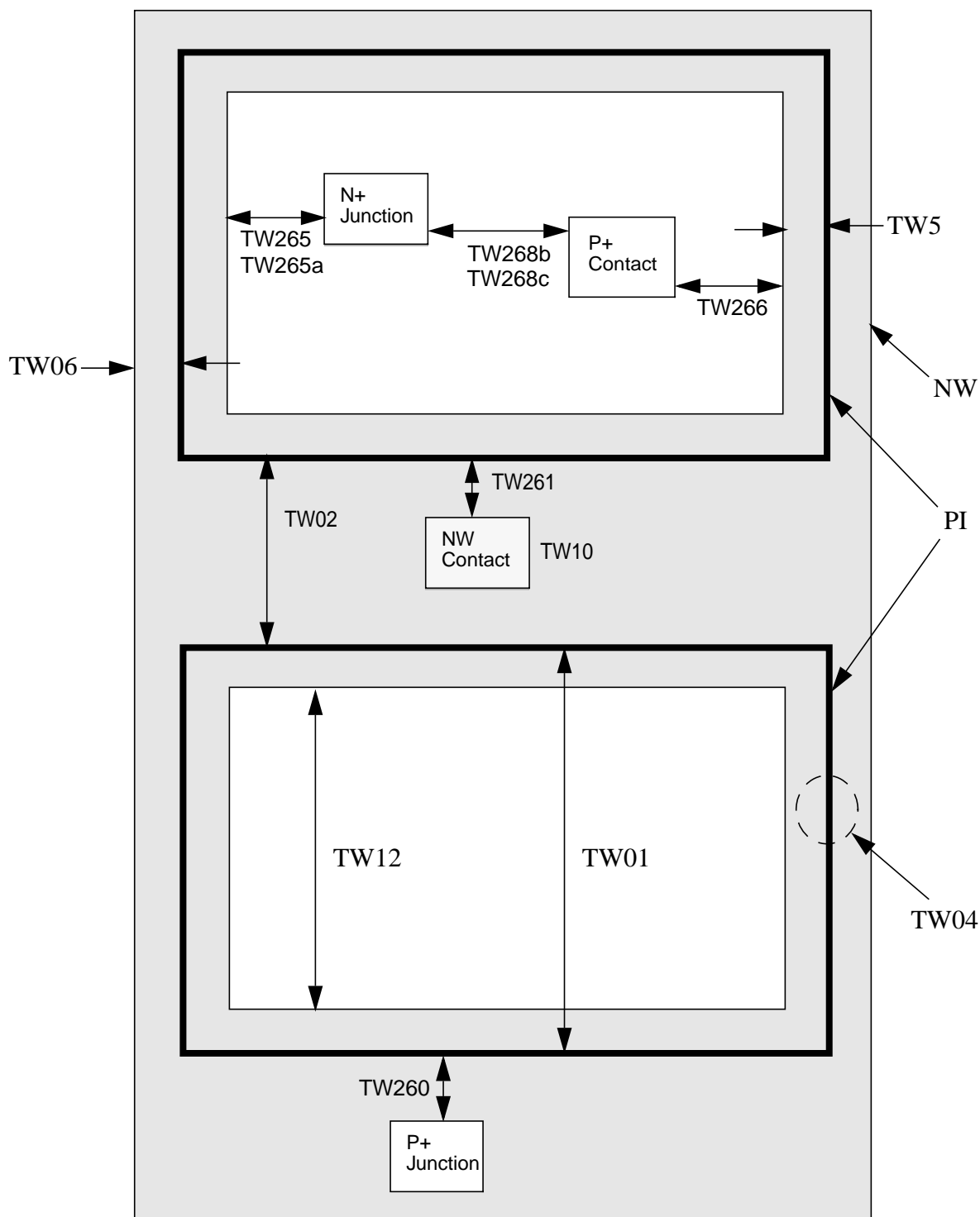


Figure 3-32. Triple Well NFET (Multiple PI shapes)

3.23 Electrical Fuse

This section describes the rules for the electrically programmed fuse (efuse).

3.23.1 Specifications

The electrically programmable fuse (e-fuse) is constructed on the poly-silicide level, which also is the level at which the transistor gates are formed. The shape of the e-fuse is as shown in Figure 3-33, “Electrically Programmable Fuse (e-fuse) Layout” on page 180. For layout purposes, the e-fuse-link will be drawn in the PCFUSE level which will be later integrated into PC level during data preparation. The EFUSE level is used in dataprep to block the N+ S/D implant from being in the fuse device area.

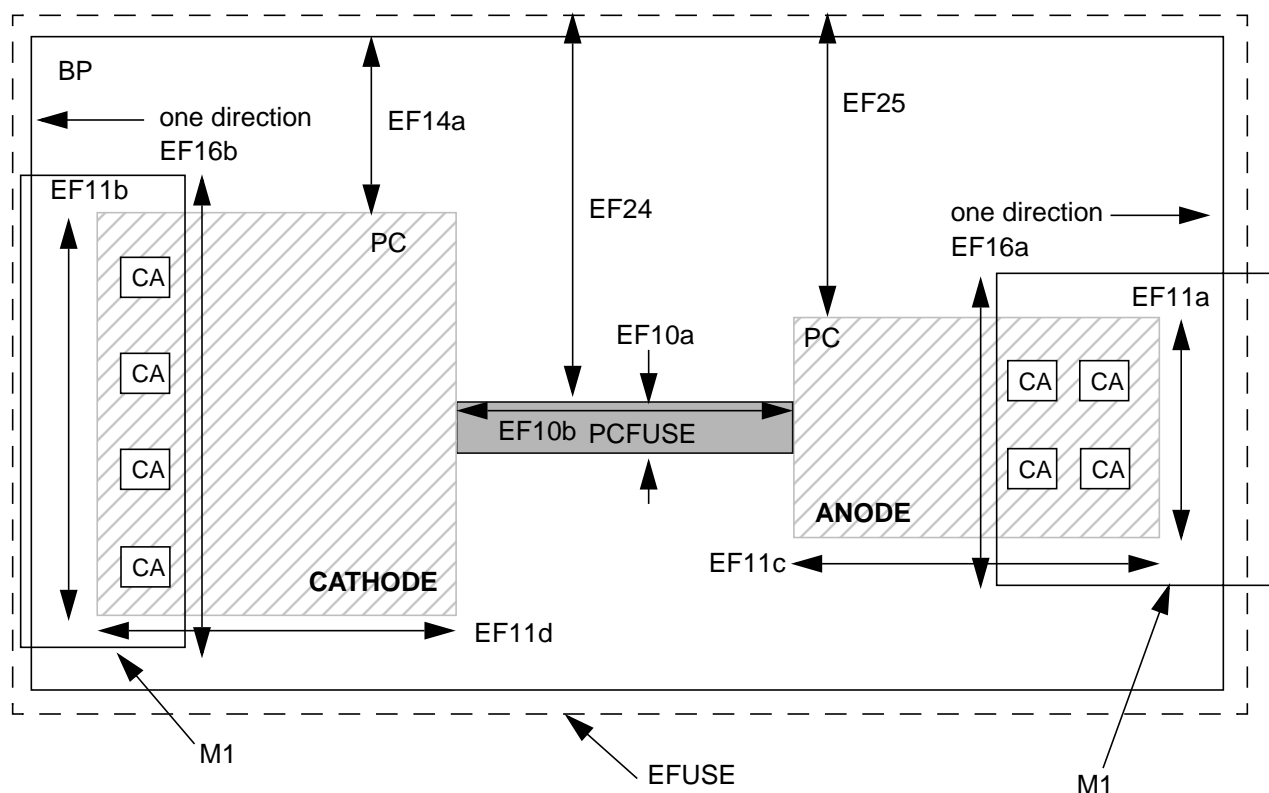


Figure 3-33. Electrically Programmable Fuse (e-fuse) Layout

3.23.1.1 Fuse Design Guidelines

- The e-fuse anode and cathode have a positive and negative electrical bias with respect to each other during fuse programming.

- The e-fuse structure is positioned above the shallow trench isolation (STI) region. The poly-silicon on the e-fuse link is p-doped. Hence, the e-fuse layout is enclosed by a BP mask.
- Programming voltage must be applied with a positive bias on the anode.
- The FET channel length must be the minimum allowed by the Layout Rules.
- Each e-fuse is to be programmed by a programming transistor attached to it (shown schematically for one e-fuse in Figure 3-34). The electrical parameter requirements for the e-fuse are given in Table 3-47, “e-fuse programming specifications” on page 181.

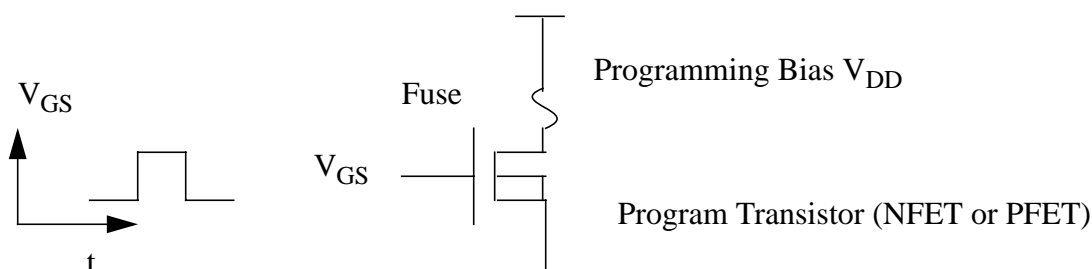


Figure 3-34. The e-fuse appears as the load of a programming transistor.

The transistor and e-fuse programming specifications are shown in the following Table 3-47:

Table 3-47.e-fuse programming specifications

eFuse Property	Specification	Tolerance
Programming voltage V_{DD}	$3.3V \leq V_{DD} < 3.7V$, $V_{DD} = 3.3V$ recommended.	$\pm 100mV$
Programming transistor current I_{on}	$10\text{ mA} < I_{on} < 13.5mA$	-
Programming time, t	$0.18\text{ ms} \leq t < 1.0\text{ ms}$	-
Programming Pulse Rise time	$< 200ns$	-
Intact e-fuse resistance	$50\ \Omega < R < 130\ \Omega$	-
Programmed e-fuse resistance	$> 5\text{ k}\Omega$	-
Fuse sense voltage	-	$\pm 100mV$
Blown fuse sense voltage ¹	1.6V Maximum	-
Fuse sense current	$< 0.5mA$	-
Fuse sense time	$< 100ns$	-

Table 3-47. e-fuse programming specifications

eFuse Property	Specification	Tolerance
Fuse sense operations	$< 1 \times 10^9$	-
Sensed Programmed e-fuse	Positive Bias on Anode	-

1. Maximum sensing voltage across the blown (post programmed) fuse.

For further details, please contact your IBM Representative.

3.23.2 ECID Fuse Requirements

Electronic chip identification (ECID) designs must use at least 72 fuses to accommodate the 12-character (six fuses per character) wafer ID. The wafer ID is comprised of the following characters:

- Two-character IBM part number
- Six-character wafer number unique to the manufacturer
- Two-character manufacturer code
- Two-character checksum on the previous ten characters

3.23.3 Layout Rules

Table 3-48. Electrically Programmable Fuse Layout Rules

Rule	Class	Notes	Description		Des Min.
EF10a	a	-	PCFUSE width	≡	0.12
EF10b	c	-	PCFUSE length	≡	1.20
EF10c	c	-	PCFUSE to PCFUSE space	≥	2.00
EF10d	c	-	PCFUSE shapes must be orthogonal rectangles	≡	-
EF10e	c	-	PC touching (PCFUSE sized by +2.00) must be orthogonal rectangles	≡	-
EF10f	c	-	PC touching (PCFUSE sized by +2.00) must abut PCFUSE	≡	-
EF11a	c	-	(PC touching PCFUSE) butting edge length on one side of PCFUSE (anode)	≡	0.68

Table 3-48. Electrically Programmable Fuse Layout Rules

Rule	Class	Notes	Description		Des Min.
EF11b	c	-	(PC touching PCFUSE) butting edge length on other side of PCFUSE (cathode)	≡	1.70
EF11c	c	-	(PC touching PCFUSE) butting edge width on one side of PCFUSE (anode)	≡	1.73
EF11d	c	-	(PC touching PCFUSE) butting edge width on other side of PCFUSE (cathode)	≡	1.38
EF12b	c	-	PCFUSE to M1	≥	1.00
EF12c1	c	-	PCFUSE to {RX, NW, OP, DG, V1, M2, V2}	≥	2.00
EF12d1	c	-	PCFUSE not allowed over {RX, NW, OP, DG, CA, M1, V1, M2, V2}	≡	-
EF12e	c	-	(PCFUSE edges not abutting PC) ¹ to PC	≥	2.01
EF12f	c	-	PCFUSE to BFMOAT (PCFUSE not allowed over BFMOAT)	≥	3.00
EF12f1	c	-	PCFUSE to BB (PCFUSE not allowed over BB)	≥	3.00
EF12g	c	-	(BP touching PCFUSE) to JD (((BP touching PCFUSE) touching JD) not allowed)	≥	3.00
EF12h	c	-	PCFUSE not allowed over PI	≡	-
EF12j	c	-	PCFUSE to {PD, RR}	≥	2.00
EF12k	c	-	PCFUSE not allowed over {PD, RR}	≡	-
EF12m	c	-	{(PC touching PCFUSE), PCFUSE} to DT ({(PC touching PCFUSE), PCFUSE} touching DT not allowed)	≥	0.25
EF13b	c	-	PCFUSE must abut PC on both ends ²	≡	-
EF13c	c	-	PCFUSE may only abut one anode and one cathode	≡	-
EF13e	c	-	PCFUSE must be centered at PC anode and cathode ends	≡	-
EF14a	c	-	(PC touching PCFUSE) must be within BP	≥	0.25
EF14b	c	-	PCFUSE must be within BP	≥	0.25
EF15	c	-	(PC touching PCFUSE) must touch exactly 4 CA shapes (4 CA's on the anode and 4 CA's on the cathode)	≡	-
EF16a	c	-	{(M1 touching (PC touching PCFUSE)) /Anode width} in one direction	≤	0.8

Table 3-48. Electrically Programmable Fuse Layout Rules

Rule	Class	Notes	Description		Des Min.
EF16b	c	-	{(M1 touching (PC touching PCFUSE)) /Cathode width} in one direction	≤	1.8
EF20	c	-	EFUSE shapes must be orthogonal	≡	-
EF21	c	-	EFUSE width (minimum)	≥	0.40
EF22	c	-	EFUSE spacing and notch (minimum)	≥	0.40
EF23	c	-	EFUSE must touch PCFUSE	≡	-
EF24	c	-	PCFUSE must be within EFUSE	≥	0.40
EF25	c	-	(PC touching PCFUSE) must be within EFUSE	≥	0.40
EF27	c	-	EFUSE over {RX, OP} not allowed	≡	-
EF27a	c	-	EFUSE over {PI, BFMOAT} not allowed	≡	-
EF27a1	c	-	EFUSE to BB (EFUSE touching BB not allowed) (for BH generation)	≥	0.40
EF28	c	-	EFUSE to adj {NW, DG,VAR} (EFUSE touching {NW, DG,VAR} not allowed) (for BH generation)	≥	0.40
EF28a	c	-	EFUSE to {difference [intersection (OP, PC), (RX sized by +0.20)]} (for BH generation)	≥	0.52
EF28c	c	-	EFUSE to JD (EFUSE touching JD not allowed) (for BH generation)	≥	3.00
EF28dR	d	-	EFUSE to [PC(touching OP, over RR)] (for BH generation, see Rule EF29)	≥	2.00
EF29	c	-	EFUSE to {PD, RR} (EFUSE touching {PD, RR} not allowed)	≥	1.60
EF30	c	-	EFUSE to (PC over RX) ((EFUSE touching (PC over RX) not allowed)	≥	0.50
EF31	c	-	EFUSE to RX	≥	0.30

- Both larger edges of PCFUSE must be spaced away from (and not abut) separate {PC, PCEND} shapes.
- The PCFUSE must abut two separate PC shapes on each small edge end of PCFUSE.

3.24 HA Varactor (JD) Layout Rules

Table 3-49. JD Rules

Rule	Class	Notes	Description		Des Min.	Waf. Dim.	Tol.
JD1	a	-	JD width	≥	3.000	3.4500	0.300
JD2	a	-	JD space	≥	5.000	4.5500	0.300
JD3	b	-	(RX over JD) over BP) min width (anode)	≥	0.800	-	-
JD3aR	d	-	(BP over JD) min width (for VI generation)	≥	1.080	-	-
JD3b	b	1	(RX over JD) width (maximum)	≤	65.000	-	-
JD3c	b	-	RX (over RN, touching JD, not touching BP) width (minimum) (cathode)	≥	0.400	-	-
JD3d	b	-	RX(over RN, over JD) contact area (cathode) (μm ²)	≥	3.712	-	-
JD4a	b	-	((RX intersect BP) to (RX over RN)) over JD) space	≡	0.560	-	-
JD6	b	-	JD to adj RX	≥	3.000	2.9550	0.251
JD7	b	-	JD to adj BP	≥	3.000	2.9500	0.273
JD7b	a	-	BP straddling JD not allowed ((BP over JD) can not be shared with any other (BP not over JD)) (for VI generation)	≡	-	-	-
JD8	b	-	JD to adj NW (NW touching JD not allowed)	≥	3.680	3.4100	0.268
JD9	b	2	JD to adj {BFMOAT, VAR, ESDIODE} (JD can not touch {BFMOAT, VAR, ESDIODE})	≥	3.000		
JD9a	c	-	JD to adj PC (JD can not touch PC)	≥	3.000		
JD9c	b	-	JD to adj {RR, OP,PD} (JD can not touch {RR, OP, PD, ESDIODE})	≥	3.000		
JD9d	b	-	JD to adj IND_FILT (JD can not touch IND_FILT)	≥	3.000		
JD9g	b	-	JD to adj PB (JD can not touch PB)	≥	3.000	2.9500	0.296
JD9h	b	-	JD to adj BB (JD can not touch BB)	≥	3.000		
JD10	b	-	JD to adj PX (JD can not touch PX)	≥	3.000	2.9500	0.276
JD11	a	-	JD to adj NS (JD can not touch NS)	≥	5.520	3.9775	0.376

Table 3-49. JD Rules

Rule	Class	Notes	Description		Des Min.	Waf. Dim.	Tol.
JD11a	a	-	JD to adj DS (JD can not touch DS)	\geq	5.520	3.9775	0.376
JD12	b	-	RX(over RN) cathode contract ring within JD	\geq	0.760	0.8150	0.251
JD12a	b	-	RX(touching RN, not touching BB) must be covered by JD				
JD13	b	-	((RX not over BP) over JD) must be covered by RN				
JD14	b	-	JD overlap of DT	\geq	0.520	0.4500	0.259
JD15	b	-	JD edges must be covered by DT (all edges)				
JD17	b	-	JD to adj DT	\geq	2.520	2.9700	0.258
JD18	a	-	RN straddling JD not allowed				
JD20	c	-	JD must be orthogonal				

1. For more information, see Rule 41 in Table 3-1, "Polysilicon and Isolation Layout Rules" on page 69.
2. JD to VAR for BH generation. For design level DG, see Rule DGJD1 in Table 3-44, "DG Layout Rules" on page 170

3.25 Metal-to-Metal Capacitor (MIM) Layout Rules

A single LY to AM metal-to-metal capacitor is formed by adding a thin layer of metal, QY, between AM metal and the underlying layer of metal, LY. The top plate of the single capacitor, QY, is connected to AM with the via level AV.

The MIM capacitor can be formed over a NW Ground Plane or other devices and wiring.

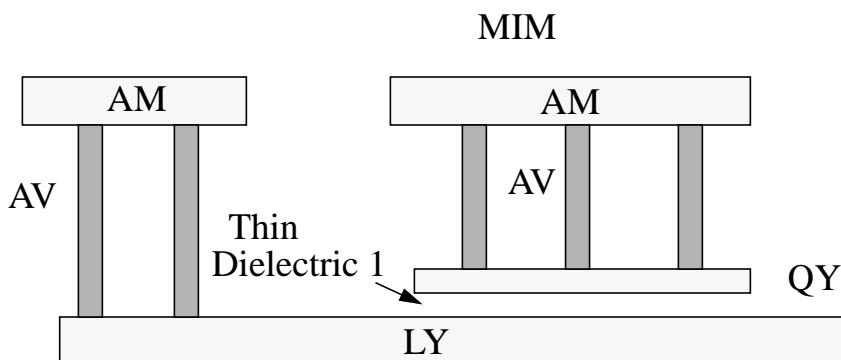


Figure 3-35. Cross Section of a MIM capacitor structures.

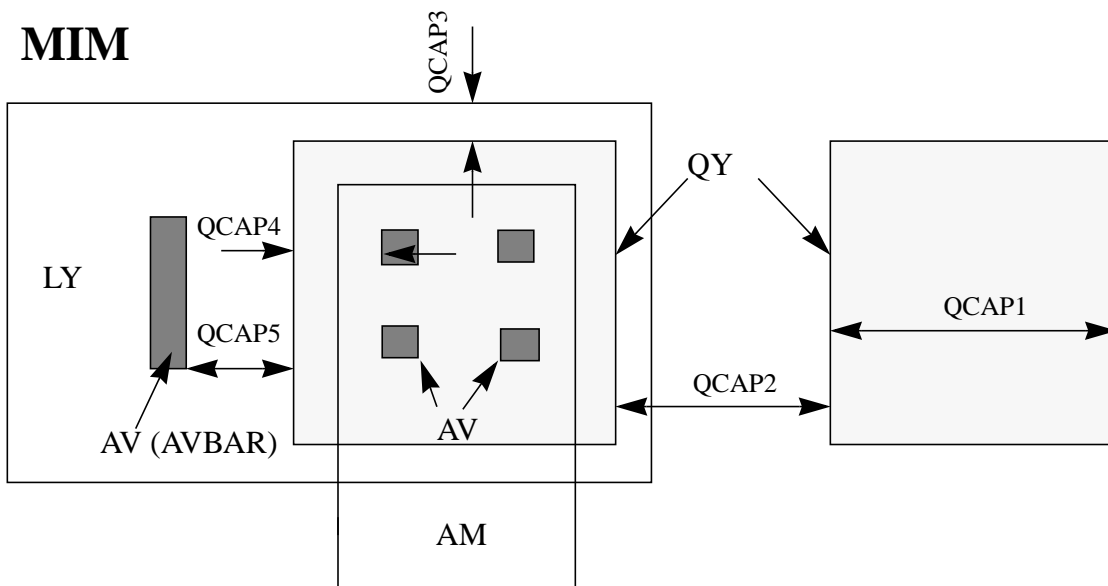


Figure 3-36. Layout for Single and Dual MIMCAP

Table 3-50.MIM (QY) Capacitor Rules

Rule	Class	Notes	Description		Design Min.
QCAP1	a	-	QY minimum width (MIMCAPs $\leq 8.00\mu\text{m}$ are not qualified).	\geq	4.000
QCAP1b	c	-	QY area (μm^2) (maximum per shape).	\leq	100,000
QCAP1c	c	-	QY area (maximum per chip ^{1,2}) (μm^2).	\leq	2,000,000
QCAP1dR	d	-	QY maximum width (covered by Rule QCAP2b and QCAP1b)	\leq	1,000
QCAP2	a	-	QY to QY space.	\geq	5.0
QCAP2a	c	-	QY must be rectangular (45° QY not allowed).		
QCAP2b	c	-	QY aspect ratio (length/width ratio) (Needed for Rule QCAP1dR).	\leq	3
QCAP3	a	-	QY must be within LY.	\geq	2.0
QCAP4	a	-	(AV touching QY) must be within QY (QY must touch AV).	\geq	1.2
QCAP4R	d	-	(AV touching QY) must be within QY (QY must touch AV).	\geq	2.00
QCAP4a	b	³	(LY touching QY) touching {VY, VYBAR} not allowed.		
QCAP5	b	-	(AV or AVBAR) to adjacent QY (applies to QY and (AV or AVBAR) on the same level).	\geq	2.0

Table 3-50.MIM (QY) Capacitor Rules

Rule	Class	Notes	Description		Design Min.
QCAP7a	c	-	QY touching DTMESH not allowed.	≡	-
QCAP12	c	-	QY (covered by ((NS not touching (PC over OP)) not over BPERI)) to DT (to keep the NS fully viewable as an AC ground plane under the QY MIMbody).	≥	1.960
QCAP12a	c	-	QY (covered by ((NS not touching (PC over OP)) not over BPERI)) within NS (to keep the NS fully viewable as an AC ground plane under the QY MIM body).	≥	3.960
QCAP13	c	-	QY (covered by ((NS not touching (PC over OP)) not over BPERI)) touching {DT lattice, DTMESH} not allowed.		
QCAP16	c	-	NS to adjacent (QY not touching {NS, PC, RX}).	≥	4.600
QCAP16a	c	-	DS to adjacent (QY not touching {NS, DS, PC, RX}).	≥	6.000
QCAP17R	d	-	(QY(expanded by GR QCAP3) not touching {RX, PC}) to RX.	≥	3.500
QCAP18	b	-	QY must touch AV.	≡	-
QCAP18a	c	-	QY touching AVBAR not allowed.	≡	-
QCAP20	c	-	QY to IND_FILT space.	≥	5.000
QCAP21	-	-	Rule Deleted.	≥	2.000
QCAP22	c	-	(QY width ≥ 8 μm) must touch at least two AV vias.		
QCAP24	b	3, 4	QY MIM top capacitor plate must be tied down, after being connected to AM metal, to (RX not over {PC,OP}).		
QCAP24b	b	3, 4	(LY touching QY) MIM capacitor bottom plate must be tied down, after being connected to AM metal, to (RX not over {PC,OP}).		

1. The maximum MIM Capacitor area rule is based on 3.3V, 85C, 100K POH and 10 FIT use conditions. See Section 4.22.9 , "VMAX for MIM Capacitor" on page 329 for complete Reliability Model.
2. The maximum area limit only applies to all QY shapes. This includes QY shapes added to meet pattern density (see section 2.10 , "Pattern Density Rules" on page 62).
3. This rule requires MIM capacitor top and bottom plates to be wired up to the AM metal, before being connected to other circuit nodes using the AM metal and then also requires both MIM capacitor plates to be connected to any RX(not over (PC or OP)) shape (can be connected through NP/PB polysilicon on the NPN) starting at the top plate of the MIMCAPs. This insures that all MIMs electrically float until AFTER all RIE processing above QY is completed and then are tied to a RX shape. Rule QCAP24 checks the tiedown criteria.
4. The connectivity net definition for this rule allows pass through for resistors which have an (OP intersect {RX or PC} aspect ratio of less than 100 to 1. This limits the resistance of pass through resistors.

3.26 Inductor Layout Rules

Table 3-51. Inductor Layout Rules

Rule	Class	Notes	Description		Des. Min.	Wafer	Tol.
IND7	c	-	Place a symmetric lattice of DT(covered by BB, covered by DTMESH) groundplane under ({(AM over IND_FILT) not touching M1}, (AM over TLINE)}) structures to minimize capacitance to substrate for the inductor or RF line devices. Place a (M1 touching BB) groundplane under ((AM over IND_FILT) not touching DT) to minimize capacitance to substrate for the inductor. See Rules BB8, IND8, DT24, TL7 for the required layout details.				
IND8	c	-	(AM over IND_FILT) within DT ¹	≥	1.520	1.500	0.610
IND9	c	-	Rule Deleted	=	-	-	-
IND10	c	-	AM for inductor must INTERSECT the marker level IND_FILT	≥	0.000		
IND11	c	-	The following levels can not touch IND_FILT: {NS, DS, (RX touching CA), RN, PI, JD, NW, PX, DG, (PC touching {CA, CABAR}), CX, EX, LE, PB, BP, PD, RR, OP, CABAR, CEBAR, KQ, QY, DV, LV, LVDUMMY, C4LV, ((Mx not touching V(x-1) (x=2,3,4)),(MQ not touching {VY, VYBAR}), (LY not touching {AV, AVBAR}), AMEXCLUD (AM TRANS), BFMOAT, BONDPAD, LYEXCLUD (LY TRANS), MxTRANS (x=1,2,3,4,Q), TRANSMIS. (Note: See Rule IND21 for straddling restrictions)				
IND11a	c	-	IND_FILT over TRANSMIS not allowed	=	-	-	-
IND12	c	-	NS to IND_FILT	≥	4.600	1.870	0.614
IND12a	c	-	DS to IND_FILT	≥	6.000	3.270	0.614
IND12b	c	-	NW to IND_FILT	≥	4.600	1.870	0.614
IND14	c	²	Lattices of DT at 10 μm pitch (8.96μm space) touching {IND_FILT (for inductors), TLINE (for rline)} must be covered by DTMESH				
IND14a	c	-	DT space under DTMESH	=	8.960	-	-
IND15	c	-	(IND_FILT touching DT) must be within DTMESH	≥	0.00	-	-
IND16	c	-	(BB touching IND_FILT) cannot touch (BP or ((PC or RX or PB) not touching IND_FILT))				
IND17	c	-	(AM over IND_FILT) touching {DT Lattices ³ , (DT not covered by DTMESH)} not allowed				

Table 3-51. Inductor Layout Rules

Rule	Class	Notes	Description		Des. Min.	Wafer	Tol.
IND20	c	-	(IND_FILT touching AM) to adjacent Mx (x=1,2,3,4,Q) outside of IND_FILT (for required MxFILL exclusion region for low MxFILL density regions of a chip design)	≥	10.0	-	-
IND21	c	4	{RX, M4, M3} straddling IND_FILT is not allowed				
IND24	c	-	M2 straddling IND_FILT must touch (V1 over IND_FILT)	=	-		
IND25	c	-	M1 groundplane, when used in a completed chip design, can not be electrically floating	=	-		

1. DT in Rule IND8 applies only to the outer perimeter edges of the DT. DT used in the inductor device structure touches Dummy Design and Utility Level IND_FILT. DT used in the Inductor is covered by Dummy Design and Utility Level DTMESH. For IND_FILT or DTMESH, see Table 2-4, "Dummy Design Levels and Utility Levels," on page 36.
2. DTMESH is a Dummy Design and Utility Level (rectangular shape) to recognize DT that are not at 2.48μm space for the Inductor or RF Interconnect Line. For DTMESH, see Table 2-4, "Dummy Design Levels and Utility Levels," on page 36.
3. DT Lattices in Rule IND17 is not a dummy design level. The term DT Lattices is a pseudo-generated level in DRC that refers to any lattice of DT with an area of the hole formed by the DT being less than 3.00μm and is not covered by DTMESH. For DTMESH, see Table 2-4, "Dummy Design Levels and Utility Levels," on page 36.
4. Metal design levels AM, LY, M2, M1 are allowed to straddle (IND_FILT touching AM).

3.27 Transmission Line and RF Interconnect Layout Rules

3.27.1 Transmission Line Layout Rules

Table 3-52. Transmission Line Layout Rules							
Rule	C l a s s	Notes	Description		Des. Min.	Wafer	Tol.
TLR1	a	¹	xxEXCLUD ² must touch UNION {LYPIN, AMPIN} (where xx = LY, AM)	=	-	-	-

1. The XX pin levels in this rule correspond to the CDS names (XX = LY, AM). These XX pin levels are not identified in Table 2-4, "Dummy Design Levels and Utility Levels," on page 36.

2. The xxEXCLUD levels in this rule correspond to the xx TRANS CDS names (xx = LY, AM) identified in Table 2-4, "Dummy Design Levels and Utility Levels," on page 36. The GL1 level name xxEXCLUD (where xx = LY, AM) are also listed in Rule RL03a in Table 2-14, "Reserved Level Layout Rules," on page 58.

3.27.2 RF Interconnect (rfline) Layout Rules

Table 3-53.AM rfline Rules

Rule	Class	Notes	Description		Des. Min.	Wafer	Tol.
TL1aR	d	-	(AM over (TLINE not over IND_FILT)) minimum width	\geq	4.000	-	-
TL1b	c	-	(AM over (TLINE not over IND_FILT)) shape maximum width	\leq	25.000	-	-
TL2a	c	-	(TLINE not over IND_FILT) overlap past AM	\geq	20.000	-	-
TL2b	c	-	AM overlap past (TLINE not over IND_FILT)	\geq	1.000	-	-
TL3a	c	-	(AM over (TLINE not over IND_FILT)) shape minimum area(μm^2)	\geq	400.0	-	-
TL3b	c	-	(AM over (TLINE not over IND_FILT)) shape minimum length	\geq	100.0	-	-
TL4a	c	-	(AM over (TLINE not over IND_FILT)) shape maximum area(μm^2)	\leq	37500.	-	-
TL4b	c	-	(AM over (TLINE not over IND_FILT)) shape maximum length	\leq	1500.0	-	-
TL5	c	-	(AM over (TLINE not over IND_FILT)) must be within BB	\geq	4.000	-	-
TL6a	c	¹	(TLINE not over IND_FILT) touching BP, BX, DG, DS, DV, EX, JD, KQ, LE, LV, LVDUMMY, LY, Mx (x = 1,2,3,4,Q), NS, NW, OP, PC, PB, PD, PI, RN, RR, RX not allowed				
TL6b	c	-	(AM over (TLINE not over IND_FILT)) space	\geq	40.000		
TL7	c	-	(AM over (TLINE not over IND_FILT)) within DT ²	\geq	4.000	-	-
TL8	c	-	(AM over (TLINE not over IND_FILT)) touching {DT Lattice ³ , (DT not covered by DTMESH)} not allowed				
TL9	c	-	(AM over (TLINE not over IND_FILT)) must be rectangular				
TL10	c	⁴	AM for RF Line must touch the marker level (TLINE not over IND_FILT)				

1. For the RF interconnect line device, the dummy design and utility levels listed in the columns within Table 2-9, "Design Truth Table for Non-Design Mask Levels and Dummy Design Levels," on page 52, on the rfline (AM, BB, DT) row, are not verified in DRC. However, the truth table criteria may be used in other non DRC verification tools.

2. DT in Rule TL7 applies only to the outer perimeter edges of the DT. DT used in the “rflne” device structure touches Dummy Design and Utility Level TLINE. For TLINE, see Table 2-4, “Dummy Design Levels and Utility Levels,” on page 36.

3. DT Lattices in Rule TL8 is not a dummy design level. The term DT Lattices is a pseudo-generated level in DRC that refers to any lattice of DT with an area of the hole formed by the DT being less than $3.00\mu\text{m}^2$ and is not covered by DTMESH. For DTMESH, see Table 2-4, “Dummy Design Levels and Utility Levels,” on page 36.

4. Rule is not coded in DRC. Rule is stated for informational purposes only.

3.28 Terminals, IO Pads, C4 and Wirebond

Either C4 terminals or wirebond terminals may be used.

Note: See Section 5.3.6 , “Soft Error Rate” on page 351 and Table 5-4, “Adjustment Factors for I(dc) only, for Temperature and Time, based on 100C and for 100,000 POH lifetime,” on page 364 for additional information.

Table 3-54. Pad Model (BONDPAD) Rules for C4 and Wirebond Pads

Rule	Class	Notes	Description		Design Min.
BONDPAD1	c	-	BONDPAD overlap past AM.	≥	0.100
BONDPAD2	c	-	(AM over BONDPAD) to {DT, DTMESH, DT_LATTICE ¹ } ({DT, DTMESH, DT_LATTICE ¹ } touching (AM over BONDPAD) not allowed).	≥	4.900
BONDPAD3	c	-	[(AM over BONDPAD) must be covered by NS] or [(AM over BONDPAD) must touch (M1 touching BB)].	≡	-
BONDPAD3a	c	-	Rule Deleted	≡	-
BONDPAD4	c	-	(AM over BONDPAD) to (NW, BP, CA, CABAR, CEBAR, M2, M3, M4, MQ, LY). ((AM over BONDPAD) cannot touch (NW, CA, CABAR, CEBAR, M2, M3, M4, MQ, LY)).	≥	4.900
BONDPAD5	c	-	BONDPAD to {PC, RX} (BONDPAD touching {PC, RX} not allowed).	≥	3.400
BONDPAD5a	c	-	BONDPAD touching PB not allowed.	≡	-
BONDPAD7	c	-	Rule Deleted	≡	-

1. DT_LATTICE is a pseudo-generated level in DRC for checking DT with greater than 11 vertices.

3.28.1 C4 Terminals

3.28.1.1 Active C4 Terminals

The C4 structure is a solder ball over a transition metallurgy (BLM/UBM) pad. This section describes the *required* design rules for connecting a C4 terminal to the chip circuitry (an active C4). Section 3.28.1.2 , “Dummy C4 Terminals” on page 198 describes how dummy C4 terminals can be used.

The active C4 terminal makes contact with the final level of metal through the LV via in the final passivation (polyimide, nitride, oxide). The structure is shown in Figure 3-38, “Active and Dummy C4 Terminal Structures” on page 198.

The guidelines below must be followed when designing a C4 pattern.

- The outer row of pads must be *asymmetrical* on all four sides of the chip.
- The asymmetrical pad design is required within 2.34 mm of the true chip center for all chips larger than 10 mm on a side in one or both dimensions. The preferred pattern of asymmetry is three adjacent depopulated C4 sites surrounded by an area of fully populated sites. The three depopulated sites should not be in the same row or the same column.
- For standard C4 “flip chip” packages, LV terminal to CHIPEDGE must be $\leq 250 \mu\text{m}$ on at least three sides of the chip for some C4s. Dummy C4 pads can be used to achieve this requirement.
- This outer row of pads must be approximately the same distance from the edge of the chip on all sides.
- Circular patterns of C4 pads are prohibited.
- C4s are prohibited outside of CHIPEDGE.
- C4 terminals connected to the last wiring metal (AM) pads must not float. The metal must be connected to RX and must satisfy the ESD rules given in Section , “” on page 140 and Section 6.0 , “Electro-static Discharge (ESD) Protection” on page 369. See also Rule 908. Floating C4 terminals that use the LVDUMMY level are permitted.
- All designs with > 5000 tested pins must have prior approval from Test Probe Engineering

In addition, the following guidelines are recommended:

- For designers who plan to characterize their designs prior to C4 processing by probing last metal pads, the following recommendation should be observed to prevent probe damage to adjacent wiring: AM pad to AM wiring should be at least $30 \mu\text{m}$.
- Using a “5 on 10” C4 size/pitch or fewer than the maximum number of C4 terminals per chip, typically improves manufacturing yields. The “5 on 10” syntax refers to a 5mil solder bump on a 10mil pitch (1 mil = 0.001 inch = $25.4 \mu\text{m}$). C4 solder ball sizes (wafer dimensions) are typically about 1 mil larger.
- There should be no area on the chip larger than 3 mm in any direction that does not contain C4s. Dummy C4s should be inserted where ever possible to fill empty areas. This helps ensure C4 height uniformity.

Note: The C4 terminal design must be reviewed with packaging and test groups. C4 terminal designs with on-chip pitches of less than 230 μm must be reviewed with probe engineering. Deviations from the above guidelines or from the design rules in Section Table 3-56., “C4 Layout Rules (Active and Dummy)” on page 196 must be approved by IBM Terminal Metals engineering.

Layout Rules 901 in Table 3-56, “C4 Layout Rules (Active and Dummy),” on page 196, define the periodicity for 4 and 5 mil pads that are necessary for a product to function at PAS (Pad Analysis System). Please note this periodicity is not the minimum “diagonal” spacing when staggered pads are used. This is a larger number which is also listed. The pad periodicity is required in the perpendicular, or X/Y direction. If the minimum pad spacings (diagonal) cannot be met the part may not be PAS (Pad Analysis System) checkable. The pad periodicity can vary in the X and Y dimensions as long as the diagonal minimum value is met (**NOTE:** Diagonal values cannot be checked by the DRC decks).

LV is the Design Level for C4 Terminals and LV will be the generated Mask Level used to manufacture C4 terminals. See Mask Level LV and Design Level LV in Table 2-1 on page 25.

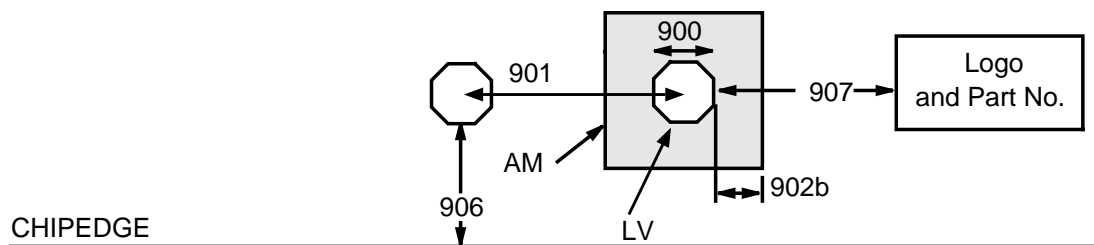


Figure 3-37. Rules for C4 Terminals

Table 3-55. C4 Diameter / Pitch Rules¹

Rule	Class	Notes	Dimensions		Design	Design	Design
C4DP	C	-	C4 BLM/UBM diameter and pitch	=	4 on 8	4 on 9	5 on 10
C4MX	C	-	Number of C4's per chip - max	≤	9000	9000	7000
C4MN	C	-	Number of C4's per chip - min	≥	3	3	3

1. For Mask ordering purposes when using Plated Bumps, both High Temp and Low Temp, a Mask Size 1mil smaller than the required Plated bump diameter should be ordered. For example, for a 5mil Plated bump, a 4mil mask should be ordered. C4 Plated bump sizes (wafer dimensions) are typically about 1 mil larger than the stated BLM/UBM design size.

Table 3-56. C4 Layout Rules (Active and Dummy)

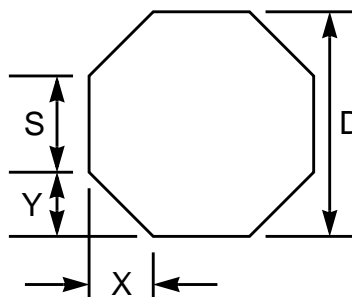
Rule	Class	Notes	Dimensions		Design	Design	Design
900	C	¹	LV ² octagon dimension "D" ³	≡	47.00	47.00	47.00
900a	C	⁴	LV octagon must be within C4LV	≥	0.000	0.000	0.000
900b	C	⁴	C4LV must touch LV	=	-	-	-
900c	A	⁵	LV/C4LV used for C4 pads must be octagonal.				
901	C	⁶	LV center to center	≥	200.00	225.00	250.00
902b	C	⁴	LV within AM	≥	14.50	14.50	14.50
906	C	⁷	LV within CHIPEDGE	≥	86.00	86.00	104.00
906R	C	-	LV within CHIPEDGE	≥	101.00	101.00	113.00
907	C	-	LV to Chip Logo and PN ⁸ (LV can not touch LOGOBND)	≥	64.00	64.00	80.00
908	C	^{9, 10}	AM containing a LV shape must be connected to an RX shape (DC path) (No electrically floating active C4's allowed). AM containing LVDUMMY shapes are allowed.	=	-	-	-
911a	C	-	LVDUMMY must not touch {LV, C4LV}	=	-	-	-

Table 3-56.C4 Layout Rules (Active and Dummy)

Rule	C l a s s	Notes	Dimensions		Design	Design	Design
927	c	11	CHIPEDGE must be within {[UNION (LV, LVDUMMY)] sized by +1,500.0µm}	≥	0.0	0.0	0.0

- For details on the generated LV, see section Table 2-6., “Shape Manipulation Prior to Mask Write” on page 44.
- All LV shapes in this table should be understood to be LV terminal vias for active C4’s unless noted otherwise.
- Octagon dimensions are given below for C4 LV and LVDUMMY shapes. Dimensions have a tolerance of $\pm 0.10 \mu\text{m}$ associated with them. As a part of design preparation during mask build, octagons will be converted to circles.
- These rules do not apply to LVDUMMY.
- Non-octagonal C4’s will be removed from the dataset during design services and design preparation.
- Exact pitch design must be determined by matching to the package application.
- These rules are to keep the C4s from shorting to the KERF crackstop. Also, the minimum distance between the C4 edge (Rule 906) and the diced chip edge is a critical parameter for certain package types, especially flip chip plastic ball grid array packages. For specific applications, this minimum distance must be reviewed for compliance with reliability restrictions.
- The purpose of rule 907 is to prevent the chip identification from being obscured by the terminals.
- AM pads must be tied down to a valid RX diffusion not touching (BB or RN or BX or ((NW touching DT) that does not satisfy Rule 134 or DT267R) and must satisfy the ESD rules given in “Electro-static Discharge (ESD) Protection” on page 369. The connection to RX must be a DC path (not through a capacitor).
- The connectivity net definition for this rule allows pass through for resistors which have an (OP intersect {RX or PC} aspect ratio of less than 100 to 1. This limits the resistance of pass through resistors.
- Dummy C4’s should be used to meet this density rule, if the requirement can not be met with active C4’s.

Octagon Dimension	LV
D	47.00
S	19.48
X, Y	13.76



3.28.1.2 Dummy C4 Terminals

Dummy C4 terminals are electrically inactive. They may be designed to provide additional mechanical support or to enable the same C4 masks to be used for multiple part numbers. C4 dummy terminals are designed by using the dummy level LVDUMMY instead of LV so that there is no LV opening in the nitride passivation. Locate LVDUMMY anywhere that is consistent with the LV rules for designs in Table 3-56, “C4 Layout Rules (Active and Dummy)” on page 196 with the exception that rules 900a, 900b, 902b, and 908 do not apply. LV shapes may not be located under LVDUMMY.

NOTE: LV will be the generated Mask Level used to manufacture Dummy C4 terminals. See Mask Level LV and Design Level LV in Table 2-1 on page 25 and Rule GLV in Table 2-6 on page 44.

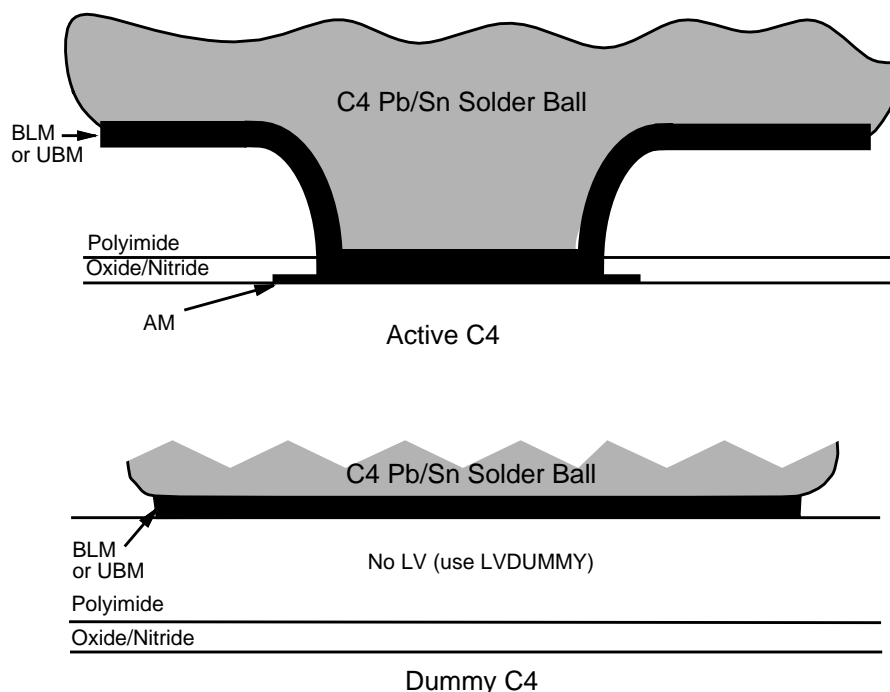


Figure 3-38. Active and Dummy C4 Terminal Structures

NOTE: For definition of BLM or UBM, see section Appendix E., “Definitions of Process-Related Terms” on page 414.

3.28.2 Wirebond

The following rules are based on IBM performing the packaging and wafer level testing. If these functions are performed elsewhere then the requirements may differ. **The customer is responsible for the qualification of non-IBM wirebond builds (non-IBM wirebond builds may have different requirements for: pads, metals, and devices under pads).** Also see section 3.28.3 , “Wire-bond Part Testing and Packaging Restrictions” on page 200.

The size of the wire bond pads that are standard for this technology are for gold ball bonds. If you or your customer plan to use a wedge bond you will need to increase the size of the bond pad to accommodate the bonding wedge.

Table 3-57. Wirebond Layout Rules

Rule	Class	Notes	Description		Des. Min.
941b	c	-	DV terminal pad ¹ center to center (single row of pads)	≥	73.00
942b	c	-	DV terminal pad to {{EX, LE} touching CEBAR}, {{NP,PB} touching {CA, CABAR, CEBAR}}, DI, EFUSE, KQ, VY, VYBAR, QY, AV, AVBAR, IND_FILT, JD, LOGOBND, MxPLANE (x=1,2,3,4), NSR, OP, PCFUSE, {PC, PB} over RX(expanded by 0.14 μm per edge), RX over (PC,PB), TLINE, TRANSMIS}.	≥	3.00
942R	c	-	DV terminal pad to {BX, IND_FILT, LOGOBND, PX}.	≥	3.00
944b	c	-	DV must be within CHIPEDGE (minimum)	≥	16.000
945b	c	-	DV must be within CHIPEDGE (maximum)	≤	190.00
946b	c	-	DV terminal pad width (parallel to closest CHIPEDGE) (must be rectangular)	≥	62.00
946g	c	-	DV terminal pad length (perpendicular to closest CHIPEDGE) (increasing the dimension perpendicular to chipedge does not impact the pitch)	≥	95.000
948b1	c	-	DV terminal pad must be within AM	≥	3.00
951	c	-	(DV expanded by Rule 948b1) terminal pad over {{EX, LE} touching CEBAR}, {{NP,PB} touching {CA, CABAR, CEBAR}}, DI, EFUSE, KQ, VY, VYBAR, LY, QY, AV, AVBAR, JD, MxPLANE (x=1,2,3,4), NSR, OP, PCFUSE, {PC, PB} over RX(expanded by 0.14 μm per edge), RX over (PC, PB), TLINE, TRANSMIS} not allowed.	≡	-
951R	d	-	(DV expanded by Rule 948b1) terminal pad can not touch {BX, IND_FILT, LOGOBND, PX}.	≡	-
953	c	2, 3	AM containing a DV wirebond pad must be connected to an { RX, PB(over BX, over RX) (base Diode), EX (NPN emitter) } shape. (Floating wirebond pads are not allowed).	≡	-
954	-	-	Rule deleted.		
956	-	-	Rule deleted.		
957	-	-	Rule deleted.		

1. All references to DV refer only to openings in the passivation above a wirebond pad unless otherwise noted.

2. AM pads must be tied down to a valid RX diffusion not touching (BB or RN or BX or ((NW touching DT) that does not satisfy Rule DT267) and must satisfy the ESD rules given in "Electro-static Discharge (ESD) Protection" on page 369. The connection to RX must be a DC path (not through a capacitor).

3. The connectivity net definition for this rule allows pass through for resistors which have an (OP intersect {RX or PC}) aspect ratio of less than 100 to 1. This limits the resistance of pass through resistors.

Note: If the pitch used is less than 90 μm , the designer must take into account that there may be unique packaging and test requirements. Designs that use a tight pitch should be reviewed with the IBM Technical Representative

There may be special concerns when minimum pitch is used near chip corners. It is required that designs with tight pitches in the corners be reviewed with the IBM Technical Representative prior to completion of the design.

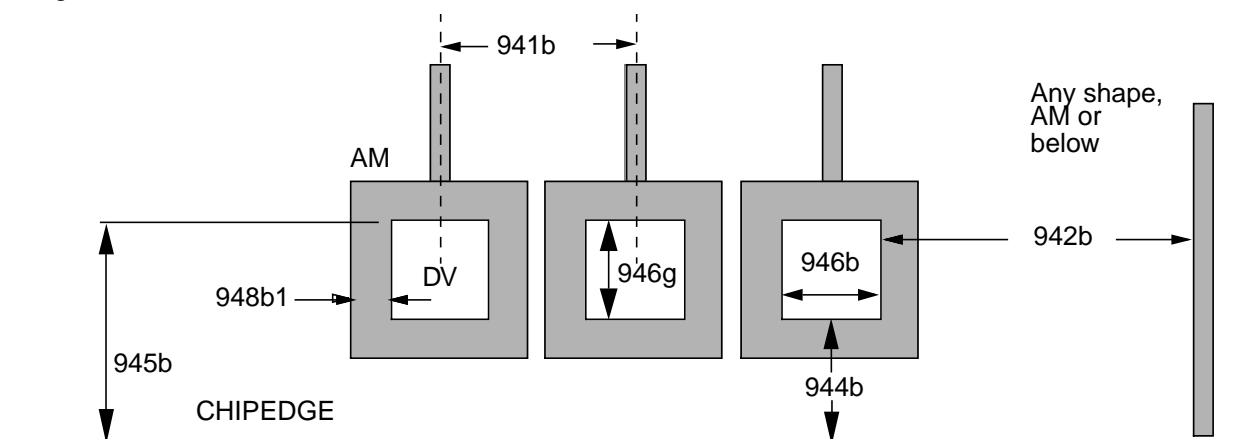
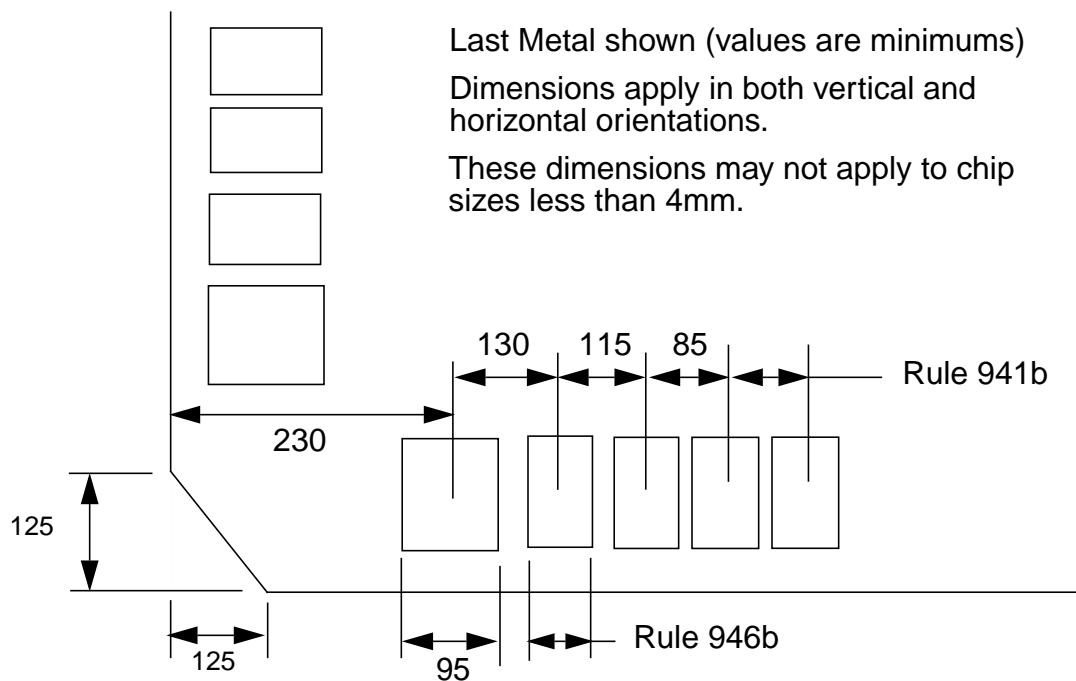


Figure 3-39. Illustration for Wirebond Terminal Layout Rules

3.28.3 Wire-bond Part Testing and Packaging Restrictions

For IBM-tested wire-bond parts, note the following testing and packaging restrictions:

- **The largest possible pad size and opening** should be used for manufacturing robustness.
- Pad designs and the associated test approach must be approved by your IBM technical representative.
- Testing is done at 30 - 85 degrees C unless prior arrangements are made with the applicable test group.
- Corner Rules:
 - *Inline pads:*
 - (1) At the four corner areas, the first bond pad must be placed away from the mechanical and thermal stress concentrated die edges. Unique patterns must be placed there for eye points recognition. Starting from the corners, the first four pitches must be wider than the pitch in regularly-repeating bond pad center area. See Figure 3-40, on page 201 for design dimensions. All pads must be located geometrically or symmetrically toward the direction of internal leads. This may not apply to chip sizes less than or equal to 4mm - Contact your IBM Packaging Representative.
 - (2) For Multi-DUT, an additional bondpad centerline spacing criteria must be satisfied at the four corners. See Figure 3-41, "In Line Wirebond Corner Pad Design Rules for Multi-DUT Probing (Device Under Test)" on page 202.



(Note: Figure is not drawn to scale)

Figure 3-40. Corner Rules, In Line Wirebond Corner Pad for Single DUT (Device Under Test).

3.28.4 Multiple DUT Pad Design Rules

The following device pad design restriction enables multiple device-under-test (DUT) probing productivity enhancements:

For wire-bond pads probed in chip corners, the probe region vertical and horizontal center lines in the corner pads must be spaced at least 200µm apart.

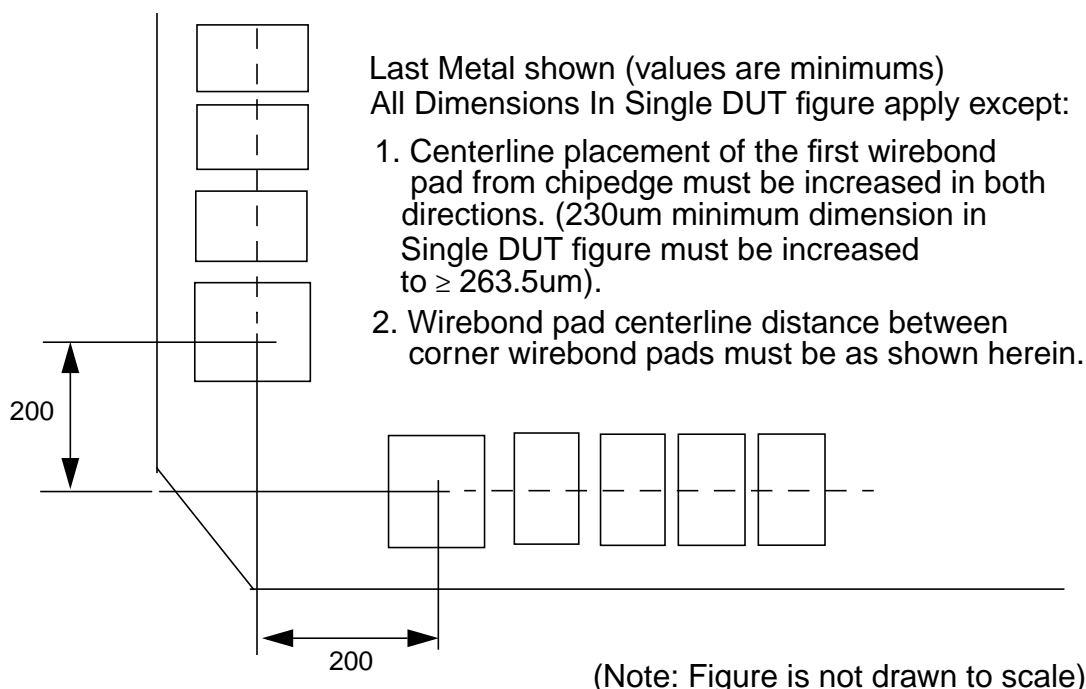


Figure 3-41. In Line Wirebond Corner Pad Design Rules for Multi-DUT Probing (Device Under Test)

3.29 Slots in Wide Metal

The guidelines in this section are only applicable to Wirebond chips that are greater than 10mm x 10mm in size and are packaged in a plastic package.

Chips packaged in plastic flat packs are subject to chip/plastic thermal mismatch stress which can result in dielectric cracking and metal movement around the chip periphery. Susceptibility is a function of many factors including the module build process, chip size, chip film thicknesses and composition, topology, and metal layout. It is strongly recommended that chips to be packaged in wirebond plastic flat packs follow the slot and corner chamfer guidelines below.

1. The portion of the chip where slots in the metal will provide stress relief can be approximated by placing a dummy box that is 10mm x 10mm in the center of the chip. Wide metal lines outside of the box should have slots placed in them.
2. The data suggests that the order of importance for placing slots in metal is from top to bottom. That is, it is most important to place slots in AM, LY, MQ and least important to place them in M1.
3. A wide metal line is defined as being $\geq 40\mu\text{m}$ wide. Only wirebond pad areas are excepted.
4. Slots in AM and LY are recommended to be approximately $5\mu\text{m}$ wide and $30\mu\text{m}$ long. Slots in MQ and lower Mx levels ($x=1,2,3,4$) are recommended to be approximately $3\mu\text{m}$ wide and $30\mu\text{m}$ long.
5. Slots should be placed such that the maximum last metal width (outside of the 10x10 box) should be $< 40\mu\text{m}$ wide.
6. If the lines are very wide, space the slots 10 to $40\mu\text{m}$ apart along their sides. End to end spacing between slots should be $\geq 3\mu\text{m}$ for MQ or Mx ($x=1, 2, 3, 4$) and $\geq 5\mu\text{m}$ for LY and AM, See Table 3-58, "Wide Metal Slot Widths" on page 203. It is desirable to stagger the starting position of the slots for long,

wide metal.

7. To avoid EM problems resulting from current funneling due to slots, the length of the slots should be parallel to the current flow. Care should be taken to avoid geometries that will funnel currents and lead to EM problems.
8. Areas of the chip that should have slots in the metal should also have chamfered corners on right angled bends of wide AM, LY, MQ, Mx (x=1, 2, 3, 4) lines. The length of the inside edge of the chamfered corner should be $\geq 15 \mu\text{m}$ long.
9. The use of AM, LY, MQ in the corners of the chip should be avoided other than for wirebond pads and the chip guard ring. The corners of the chip are defined as the four triangular regions in the corners whose sides along the edge of the chip are $125 \mu\text{m}$ long.

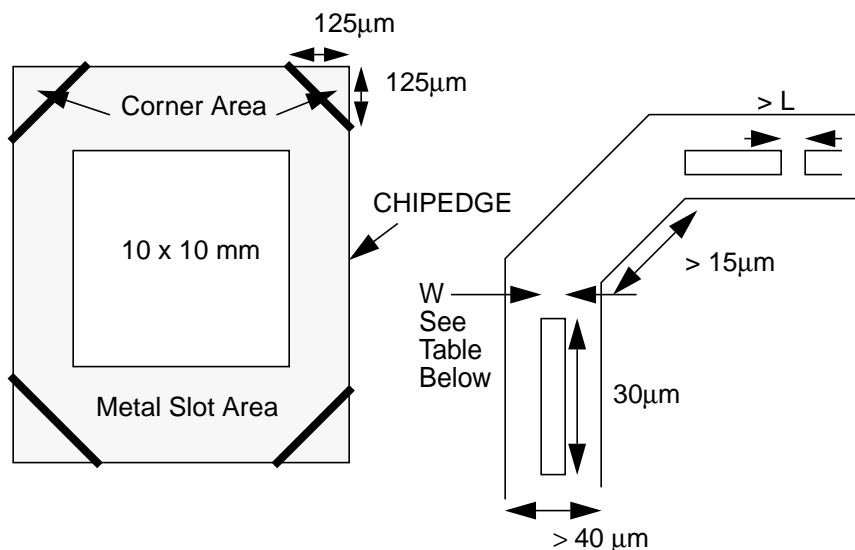


Figure 3-42. Guidelines for Slots in Last Metal - See "Wide Metal Slot Widths" on page 203

Table 3-58. Wide Metal Slot Widths		
Levels	W (μm)	L (μm)
AM	5	5
LY	5	5
MQ	3	3
Mx (x=1,2,3,4)	3	3

3.30 Chip Guard Ring and Chamfer

The chip guard ring provides both a low resistance path to ground for surge currents and a metal seal against ionic contaminants.

The guidelines below *must* be followed when designing a chip guard ring:

- The chip guard ring must be a complete, unbroken ring around the entire active chip area. This applies to all shapes used to define the guard ring. The chip guard ring must be connected to the ground bus.
- The chip guard ring must be comprised of the following levels: RX, BP, DT, CABAR, M1, V1BAR, M2, VLBAR, MQ, VYBAR, LY, AVBAR, AM. Continuous xxBAR vias and contacts must be used in the guard ring structure. The following levels must be present in the chip guard ring if they are present in the design data: V2BAR, M3, V3BAR, M4.
- The chip guard ring must not have any vertices except for the 45° angles that occur at the corner bevels for a non-rectangular chipedge or 90° angles that occur at the corners for a square or rectangular chipedge.
- The measured width of the 45° CABAR, V1BAR, V2BAR, V3BAR, VLBAR, VYBAR, and AVBAR shapes on the corner bevels may not exactly match the specified dimensions due to grid snapping (± 0.014 tolerance, or the grid x the square root of 2 tolerance). This tolerance also applies to the chip guard ring “within” rules.
- The length restriction on CABAR, V1BAR, V2BAR, V3BAR, VLBAR, VYBAR, AVBAR does not apply to the chip guard ring.
- Chamfer regions are required for *all* IBM products or chip designs to be packaged by IBM. An exact 125 μm chamfer or corner bevel must be cut from each corner of the chip. For process robustness, *designs are that are not IBM products, nor packaged by IBM, are recommended to follow the chamfer rules.* The chamfer area is triangular, and has an area of exactly half of a 125 μm^2 square. The chip guard ring does not enclose the chamfer area. The non-orthogonal chipedge chip guard ring has 45° edges at the corners of the active chip area.

Note: *Foundry wafers or chips that will not become IBM products, nor packaged by IBM, are exempt from the requirement to have chamfer regions.*

- Four PROTECT shapes must be added to all chip designs (see section 3.31 , “Protect Layer” on page 208.).
 - For non-orthogonal chipedges and chip guard rings, the PROTECT shapes must not touch the chipedge or chip guard ring.
 - For square or rectangular chipedges or chip guard rings, the PROTECT shapes must be located within the chip guard ring.

Note: Data preparation is not performed on the 125 μm chamfer regions outside of a non-rectangular chipedge. Design services is performed on the 125 μm chamfer region, out to the least enclosing rectangle of chipedge, when the KERF is merged.

Note: During KERF merge, the crackstop will always be square or rectangular, even when a non-rectangular (beveled) chipedge is present.

In addition, the following guideline is recommended:

- The chip guard ring should be comprised of four cells (top, bottom, left and right) placed on the primary cell. This eases hierarchical data manipulation for design rule checking and design preparation.
- The chip guard ring is available in the Design Kit.

Table 3-59. Chip Guard Ring Layout Rules

Rule	Class	Notes	Description		Des. Min.
990a	c	-	RX width	≥	1.50
990b	c	-	BP width	≥	1.82
990d	a	-	CABAR width in chip guard ring (see Rule 228 for where CABAR is allowed)	≡	0.20
990d1	a	-	A minimum of one continuous (CABAR over GUARDRNG) must be in the chip guard ring layout between RX and M1.	≡	-
990d1a	a	-	CABAR to CABAR space	≥	0.52
990d1b	a	-	CA to CA space (see Rule 203)		
990d1c	a	-	CABAR to CA space (see Rule 223c)		
990e	a	-	V1BAR, V2BAR, V3BAR width (VxBAR is ONLY allowed in the Chip Guard Ring; where x=1,2,3)	≡	0.20
990e1	a	-	A minimum of one continuous (VxBAR over GUARDRNG) must be in the chip guard ring layout between each pair of consecutive metal levels ¹ , where x = 1,2,3.	≡	-
990e1a	a	-	VxBAR to VxBAR space, where x=1,2,3.	≥	0.80
990e1b	a	-	Vx to Vx space, where x = 1,2,3	≥	0.28
990e1c	a	-	Vx to VxBAR space (Vx touching VxBAR is prohibited) (x=1,2,3).	≥	0.60
990f	a	-	M1 width, M2 width, M3 width, M4 width	≥	1.50
990g	a	-	VLBAR width (VLBAR is ONLY allowed in the Chip Guard Ring)	≡	0.40
990g1		-	A minimum of one continuous (VLBAR over GUARDRNG) must be in the chip guard ring layout between each pair of consecutive metal levels [(Mx; where x = 2,3,4), MQ].	≡	-
990g1a	a	-	VLBAR to VLBAR space	≥	1.20
990g1b	a	-	VL to VL space	≥	0.56
990g1c	a	-	VL to VLBAR space (VL touching VLBAR is prohibited)	≥	1.20
990h	c	-	MQ width	≥	1.50
990j	a	-	VYBAR width (see VY1)		

Table 3-59. Chip Guard Ring Layout Rules

Rule	Class	Notes	Description		Des. Min.
990j1	a	-	A minimum of one continuous (VYBAR over GUARDRNG) must be in the chip guard ring layout between consecutive metal levels MQ and LY.	≡	-
990j1a	a	-	VYBAR to VYBAR space	≥	4.00
990j1b	a	-	VY to VY space	≥	2.00
990j1c	a	-	VY to VYBAR space (VY touching VYBAR is prohibited)	≥	4.00
990k	a	²	Mx inside GUARDRNG, Mx=M1,M2,M3,M4,MQ or LY or AM that are part of the guardring (Mx or LY for the chip guard ring only, must be within GUARDRNG. AM is allowed to straddle the GUARDRNG shape to satisfy Rule 1000)	≥	0.00
990LY1	a	-	LY width	≥	3.88
990m	c	-	AM width	≥	4.00
990n	a	-	AVBAR width (See AV1)		
990n1	a	-	A minimum of one continuous (AYBAR over GUARDRNG) must be in the chip guard ring layout between consecutive metal levels LY and AM.	≡	-
990n1a	a	-	AVBAR to AVBAR space	≥	4.00
990n1b	a	-	AV to AV space	≥	2.00
990n1c	a	-	AV to AVBAR space (AV touching AVBAR is prohibited)	≥	4.00
991	c	-	RX must be within BP	≥	0.16
991a	c	-	RX in the chip guard ring must be encircled by a DT guard ring		
991b	a	-	DT guard ring width (See DT1)		
991c	a	-	RX to DT guard ring (See RX3)		
992c	c	-	CABAR must be within RX	≥	0.67
993	c	-	CABAR must be within M1	≥	0.67
994a	c	-	V1BAR must be within M1	≥	0.65
994b	c	-	V2BAR must be within M2	≥	0.65
994c	c	-	V3BAR must be within M3	≥	0.65

Table 3-59. Chip Guard Ring Layout Rules

Rule	Class	Notes	Description		Des. Min.
994h	C	-	VLBAR must be within M3 (for 7LM) VLBAR must be within M4 (for 6LM)	≥	0.55
994h1	C	-	VLBAR must be within M2 (for 5LM)	≥	0.55
994AV	C	-	AVBAR must be within LY	≥	1.00
994VY	C	-	VYBAR must be within MQ	≥	0.800
995a	C	-	V1BAR must be within M2	≥	0.65
996a	C	-	V2BAR must be within M3	≥	0.65
996c	C	-	V3BAR must be within M4	≥	0.65
997a	C	-	VLBAR must be within MQ	≥	0.55
998a	C	-	VYBAR must be within LY	≥	1.320
998b	C	-	AVBAR must be within AM	≥	1.300
999	a	-	RX, M1, M2, M3, M4, MQ must be within CHIPEDGE	≡	1.46
999a	a	-	All Active chip design (except BP) must be within CHIPEDGE The dummy design level CHIPEDGE must encompass all active chip design shapes. CHIPEDGE is bounded at X=0 on the left and Y=0 on the bottom.	≥	0.00
999b	a	-	BP within CHIPEDGE	≥	1.30
999c	a	-	(LY and AM) must be within CHIPEDGE	≡	0.00
999d	a	-	DT must be within CHIPEDGE	≡	0.00
1000	C	-	The guard ring must be connected, using AM metal, to a wirebond or C4 pad	≡	-

1. See Table 2-7, "Back End Of Line (BEOL) Metallization Options," on page 49.
2. GUARDRNG must be drawn so as to completely cover the metal of the chip guard ring, but not cover any metal shapes unrelated to the chip guard ring except for AM when used to satisfy Rule 1000.

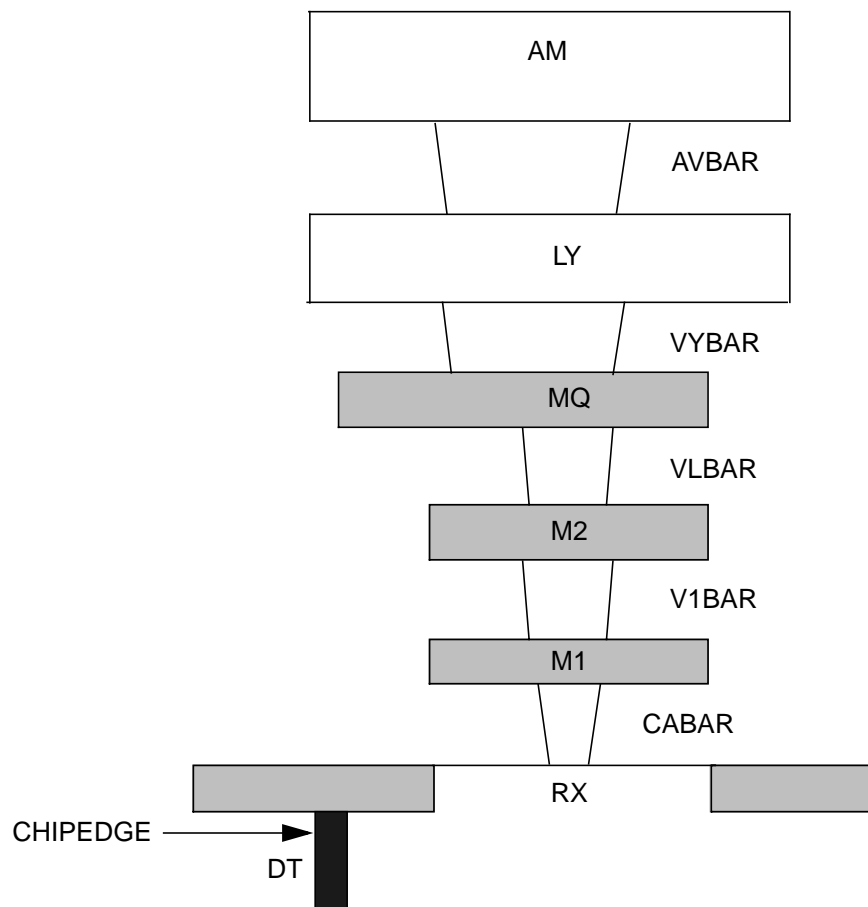


Figure 3-43. Rules for Chip Guard Ring (5 Level metal). Not drawn to scale.

3.31 Protect Layer

Four PROTECT shapes must be added to all chip designs. The function of the PROTECT level is to enable the chip design data and IBM KERF to be job decked at the mask house. The four PROTECT shapes define the maximum extents of a square, rectangular or non-rectangular (beveled) chipedge.

Note: Non-rectangular (beveled) CHIPEDGE must be used for IBM packaged chip designs. Square or rectangular CHIPEDGE only allowed for chip designs not packaged by IBM.

Note: CHIPEDGE widths or lengths less than or equal to 320µm are not recommended and must be reviewed by the IBM KERF team prior to design submission. Contact your IBM technical representative for additional information.

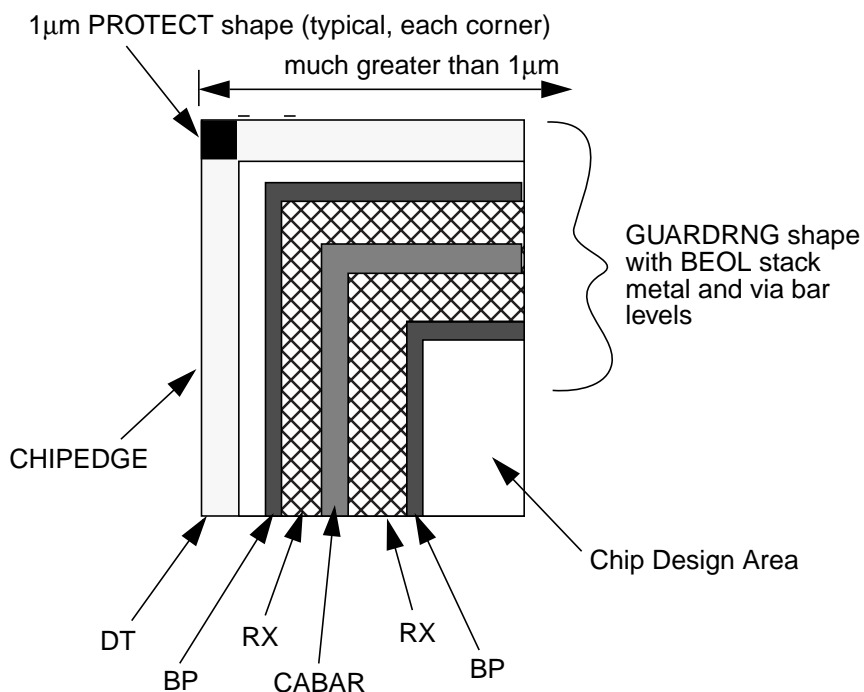
Table 3-60. Protect Layer Rules

Rule	Class	Notes	Description		Design Min.
PT01as	a	-	PROTECT must be an orthogonal rectangle.	≡	-
PT01bs	a	-	The exact number of PROTECT shapes for every (least enclosing rectangle of CHIPEDGE) shape.	≡	4
PT01cs	a	-	Union ((least enclosing rectangle of CHIPEDGE), PROTECT) must be a single orthogonal rectangle.	≡	-
PT01ds	a	-	Each PROTECT shape must have two edges coincident with (least enclosing rectangle of CHIPEDGE).	≡	-
PT01es1	a	-	PROTECT exact width (μm).	=	1.0
PT01es2	a	1	PROTECT exact area (μm^2).	=	1.0
PT01es3	a	-	Rule Deleted	≡	-
PT01gs	a	-	PROTECT must be within (least enclosing rectangle of CHIPEDGE).	\geq	0.0

Table 3-60. Protect Layer Rules

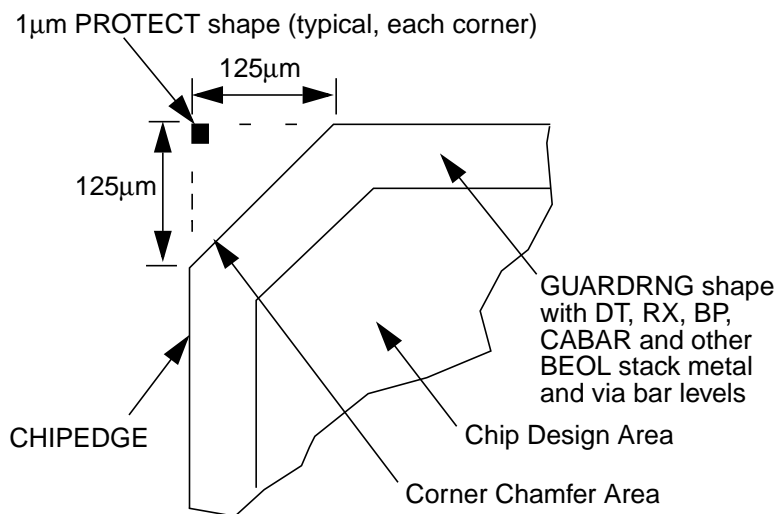
Rule	Class	Notes	Description		Design Min.
PT01hs1	a	-	<p>All Design levels affecting mask build, except {DT, RX, BP, CABAR, M1, V1BAR, M2, V2BAR, M3, V3BAR, M4, VLBAR, MQ, VYBAR, LY, AVBAR, AM, CHIPEDGE, GUARDRNG}, are prohibited touching PROTECT.</p> <p>This rule is verified as:</p> <p>The following Design Levels² are prohibited touching PROTECT:</p> <p>NS, DS, RN, PI, JD, NW, BB, PX, DG, PC, BX, CX, LE, EX, NP, PB, PD, RR, OP, CA, CEBAR, V1, V2, V3, VL, KQ, VY, QY, AV, DV, LV, BFMOAT, BOND PAD, BPERI, C4LV, DI, LYEXCLUD, AMEX-CLUD, ESDIODE, EFUSE, IND_FILT, LOGOBND, AMTRANS, MyTRANS where y = 1,2,3,4,Q, MzPLANE where z=1,2,3,4,Q, NSR, OUTLINE, PCEXCLUD, RXEXCLUD, SBLK, TLINE, TRANSMIS, VAR.</p> <p>The following Restricted³ Design Levels are prohibited touching PROTECT, except if generated by IBM during the release process: ({MxCHEXCL, MxFILL, MxEXCLUD} where (x=1,2,3,4,Q), VxHOLE where (x=1,2,3,L), LYFILL, PYFILL, AMFILL, PCFILL, RXFILL, KERFEXCL, PAD_GBIF, FUSE.</p> <p>The following Masks⁴ for Non-Design Levels are prohibited within PROTECT, except if generated by IBM: BT, DW, BF, BH, DE, DF, PH, VI, BN, PY, DY.</p>	-	-
PT01hs2	a	-	(PROTECT not touching CHIPEDGE) touching {DT, RX, BP, CABAR, M1, V1BAR, M2, V2BAR, M3, V3BAR, M4, VLBAR, MQ, VYBAR, LY, AVBAR, AM, GUARDRNG} is prohibited.	-	-
PT999s1	a	-	(CHIPEDGE not touching PROTECT) must have chamfered corners. The orthogonal x and y dimensions of the chamfer must be exactly 125µm.	-	-
PT999s2	a	5	PROTECT minimum space (µm) to non-rectangular CHIPEDGE (PROTECT touching non-rectangular CHIPEDGE is prohibited).	≥	86.0
PT999s3	c	6	(CHIPEDGE touching PROTECT) must be an orthogonal rectangle.	-	-

-
1. Area requirement is for each PROTECT shape, not the sum of the PROTECT shapes. Each PROTECT shape is intended to be 1 μ m width x 1 μ m length.
 2. For Rule PT01hs1 pin levels are to be checked.
 3. The Restricted design levels may be omitted from checking to this rule, if they are checked by other rules in DRC used to identify them as "Restricted". This Rule check for the PROTECT shape differs from the Rules checking these levels for the CHIPEDGE (see related Rules in Table 2-14, "Reserved Level Layout Rules," on page 58).
 4. These Masks for Non-Design Levels may be omitted from checking to this rule, if they are checked by other rules in DRC used to identify them as "Restricted" for design use or not allowed to be drawn within PROTECT. See Table 2-5, "Masks for Non-Design Levels," on page 43.
 5. Due to grid snapping ± 0.014 tolerance, or the grid times the square root of 2 tolerances applies to this Design Minimum dimension.
 6. DRC to issue the following warning message only when a rectangular CHIPEDGE is found. "Warning: Rectangular CHIPEDGE found. See Design Manual". See limitation note about rectangular CHIPEDGE use above Table 3-60, "Protect Layer Rules," on page 209.



Square or Rectangular CHIPEDGE

(BEOL metals and via bar levels are shown as removed)
(small top view of the corner is shown, not drawn to scale)



Non-Rectangular (beveled) CHIPEDGE

(all design levels except CHIPEDGE and GUARDRNG are not shown)
(top view of the corner is shown, not drawn to scale)

Figure 3-44. Guidelines for PROTECT shape placement

3.32 Crackstop

Crackstop is a specially designed metal ring structure placed around the chip, outside the guardring, which inhibits propagation of mechanical cracks into the chip active area. Wafer dicing may cause cracks to form on the exterior part of the chip due to mechanical stress. Without a crackstop, these cracks can propagate through out the chip, causing damage to active areas of the chip.

Crackstop is recommended for all diced chips. Crackstop is required for all chips diced by IBM.

The crackstop is not part of the client designed gds. Rather, IBM places crackstop outside CHIPEDGE after submission of data to IBM.

Currently, only one crackstop design (15.0 μm wide) is available in BiCMOS8HP.

The crackstop is identified in the IBM stepplan for the chip. Contact your IBM representative if deviations from normal crackstop placement by IBM are desired.

3.33 Product Labels

Product labels are placed in the chip, not in the kerf, and consist of:

- Chip Legal Protection Notices
 - copyright symbol and year
 - company logo
 - maskwork notice
- Chip Identification
 - part number
 - release version or EC number
- Mask Level Identification
 - mask level names /versions

3.33.1 General Requirements

1. Product labels must be placed in one or more corners of the chip (placement in the lower left corner of chip is preferred).
 - a. For products requiring packaging, at least one product label must be included. This label is used to orient the chip during packaging.
 - b. When using two corners for the product labels, it is recommended to use corners on the same side of the chip rather than diagonally across. This reduces the risk of the chip being oriented incorrectly during packaging operations.
2. IBM strongly recommends a substrate contact ring (See “Chip Guard Ring and Chamfer” on page 203) surround the entire group of product label areas. No functional chip structures are to be placed within this region.

3. The entire product label area must be covered by the LOGOBND dummy level. LOGOBND is used to suppress spurious DRC errors. Only labels and noncircuit shapes are permitted under LOGOBND.
4. The proper xxEXCLUD levels are also required to protect the area from pattern filling routines (xx level identifier). The design must still pass all local and global pattern density rules. **NOTE:** IBM places auto-generated RXFILL in LOGOBND regions.
5. Layouts within the LOGOBND area must abide by all line, space and global pattern density rules for the level on which they are designed.
6. No extraneous symbols are allowed as they can cause mask processing difficulties.
7. Alphanumeric Polygon Definitions:
 - a. A character set is available in a design kit provided by your IBM technical representative.
 - b. If the IBM provided character set is not used, characters must be composed of polygons that follow the design rules for line widths, spacing, orthogonal and 45° shapes, enclosed shapes, shape areas, and so forth, and that meet the expanded spacing rules in Table 3-61, “Special LOGOBND Rules,” on page 214.
8. See Figure 3-46, “Example Placement of Product Labels” on page 217 for an example of the placement of product labels and surrounding substrate contact ring.
9. Characters or symbols are prohibited on LV or DV levels (see Rule PN907)
10. Characters are required only on PC and M1 levels. If a designer chooses to place characters on other levels, satisfying the design rules may be difficult.
11. See Table 3-61 for additional LOGOBND Rules

Table 3-61. Special LOGOBND Rules					
Rule	Class	Notes	Description		Des. Min.
PN100	b	1	No active chip design shape or Dummy Design and Utility Levels manipulated during Dataprep may straddle LOGOBND.		
PN101	b	-	The leading edge of LOGOBND must be within CHIPEDGE (maximum)	<	50.0
PN101a	b	-	LOGOBND must not touch (CHIPEDGE sized by -150μm) (LOGOBND straddling (CHIPEDGE sized by -150μm) is prohibited)	=	-
PN101b	b	-	LOGOBND width (orthogonal edges parallel to x or y axis, maximum)	≤	150.0
PN101c	b	-	LOGOBND area (μm ² , each shape, maximum)	≤	14050.0
PN101d	b	-	LOGOBND area (μm ² , maximum per chip)	≤	28100.0
PN203	a	2	CA to CA space over LOGOBND	≥	0.28

Table 3-61. Special LOGOBND Rules

Rule	Class	Notes	Description		Des. Min.
PN502	a	-	M1 to M1 space and notch over LOGOBND	≥	0.28
PN553	a	3	Vx to Vx space (x=1,2,3) over LOGOBND	≥	0.28
PN602	a	-	Mx to Mx space (x=2,3,4) over LOGOBND	≥	0.28
PN620	a	-	VL to VL space	≥	0.40
PN692	a	-	MQ to MQ space	≥	0.40
PN907	c	4	{LV, LVDUMMY, DV} not allowed over LOGOBND		

1. For levels verified in DRC, see Section 2.2 , “Mask Level Definitions” on page 25, Table 2-1 and Table 2-2 (for only the levels supported in the design kit techfile in Table 2-2), Section 2.3 , “Dummy Design Levels and Utility Levels” on page 36, Table 2-4, and Section 2.4 , “Masks for Non-Design Levels” on page 43, Table 2-5 and Section G.4 , “Far BEOL Manipulation” on page 416 (unless already verified from Table 2-1 or Table 2-5).

2. PN203 includes CA and CABAR.

3. PN553 includes Vx and VxBAR (x=1,2,3,4).

4. See also Rule 907 in Table 3-56, “C4 Layout Rules (Active and Dummy),” on page 196 for LV and LVDUMMY.

3.33.2 Chip Protection Notices

The copyright notice, the company logos, and the maskwork notice (*M*), are legal notices that provide legal protection of proprietary design layouts and certain chip features. It is recommended that all product designs contain both the company logos and the maskwork notice. Product designs that contain significant designs or have a substantial risk of being copied may also be protected with the copyright notice.

These chip protection notices must be placed on first metal (M1) only.

An example of a combined maskwork and copyright notice is shown below. Note that the font shown has enclosed shapes which might be subminimum. A design character generator will produce shapes without enclosed areas.

© 2011 IBM *M*

Figure 3-45. Combined Maskwork and Copyright Notice

3.33.3 Chip Identification (Part Number and Release Version or EC Number)

1. Part Numbers

- The IBM-assigned chip part number is required on the PC and M1 levels of each chip. The IBM part number is required whether the design is a test site, prototype, or production part. If a “RIT A/B”

approach is being used, where the front-end-of-line (silicon) and back-end-of-line (wiring levels) designs have different part numbers, the RIT A part number appears on PC and the RIT B part number appears on M1. IBM part numbers may be obtained from your IBM product engineer prior to design submission.

Exceptions

- (1) Products for which the deliverable is untested wafers
 - (2) If the customer supplies a merged dataset that contains several chips or tiles, as in a multi-project wafer (MPW) or an array of chip variants for design optimization, the IBM-assigned part number must only appear once in the dataset. Place the part number in one of the corners of the dataset as described in section 3.33.1 , “General Requirements” on page 213. In addition, the following two statements apply:
 - If IBM is required to dice the sandbox into chip dies or test the chips, the Customer should place a unique identifier for each instance of the chip. The customer should also provide a drawing / GIF of the location and label of each chip with data submission.
 - If IBM does not dice the sandbox, some level of identification is required, minimally a Customer name.
 - b. If the product part number is later changed for any reason, a waiver is not required. The IBM product engineer must submit an EC and maintain a change log for traceability purposes.
 - c. Customer part numbers and identifiers can be placed in addition to the IBM assigned part number.
2. Release Version or EC Number
- A single letter release version label (A, B, etc.) may appear on each level (subject to the constraints listed in section 3.33.1 , “General Requirements” on page 213.) Alternatively the actual EC number may be used.

3.33.4 Mask Level Identification

Mask level identification is not allowed on any Front-End-Of-Line design levels except PC or RX due to shape propagation to derived levels.

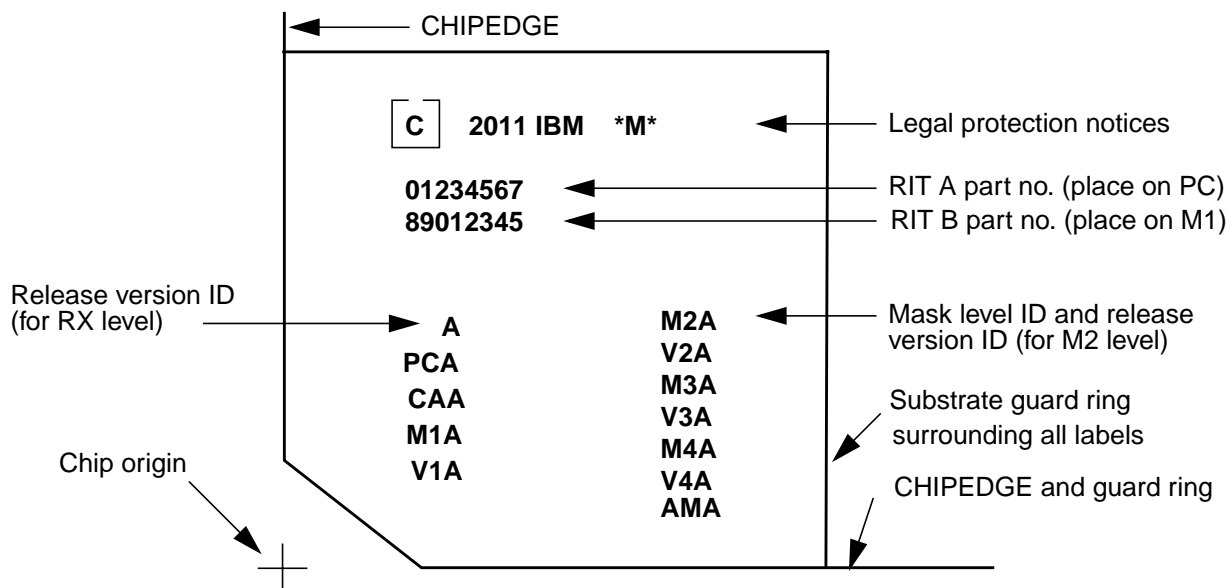


Figure 3-46. Example Placement of Product Labels

The surrounding line is the substrate contact ring at the lower left side of the chip.

3.34 No Polyimide Final Passivation option

IBM's technology level qualifications have included polyimide final passivation, but IBM sees no intrinsic impact to the wafer reliability failure rate for foundry customers who require wafers without polyimide. The customer is responsible, however, to evaluate product and packaging reliability failure rates for wafers without polyimide. If the no polyimide option is selected in the Features Table (see Table 1-1, "Optional Features with Feature Part Numbers," on page 12), the ID shape: NOPLYMD; must be added to the layout covering the CHIPEDGE shape. Also see section 2.9 , "Important Design Guidelines" on page 59.

Table 3-62.No Polyimide Rules					
Rule	Class	Notes	Description		Des. Min.
NOPLYMD01	b	1	NOPLYMD level requires feature selection review with IBM Product Engineering. Contact your IBM technical representative for more details.		
NOPLYMD02	b	2,3	If NOPLYMD exists, NOPLYMD must be drawn exactly coincident with CHIPEDGE.	≡	-

1. NOPLYMD (no polyimide) level found warning message is to be reported during a DRC run if the NOPLYMD level is found in the design data. No polyimide feature selection is prohibited for IBM tested and packaged products.
2. For NOPLYMD or CHIPEDGE containing 45 degree angle bevels, the measured coincidence of these levels may not exactly match due to grid snapping. A +/- square root of 2 x grid tolerance can apply during coincident checking
3. For multi project wafer (MPW) designs submissions that may require both polyimide and no polyimide processing, contact your IBM technical representative

3.35 Allowable Chip (CHIPEDGE) Sizes

Allowable chip (CHIPEDGE) size are limited to the following:

1. Maximum chip size is 20 mm in the x and y directions.
2. The X and Y dimensions of CHIPEDGE must be a multiple of 0.01 μm and must be on grid. See Table 3-63, "CHIPEDGE Design Rules," on page 218.
3. Large chip sizes, **exceeding 14.6 mm** on a side, may result in nonlinear cost increases compared to smaller chips.

The maximum die size might be restricted depending on the selected package technology, contact your IBM technical representative to obtain the correct die size for the specific package and the associated reliability grade.

Note: When square or rectangular corner (non-beveled) CHIPEDGE is used, see Section 3.31 , "Protect Layer" on page 208 for usage restriction.

Table 3-63.CHIPEDGE Design Rules

Rule	C l a s s	Notes	Description		Des. Min.
CE001	a	-	CHIPEDGE x and y dimensions must be an even number of grid points (2 x 0.01).	\equiv	-
CE003a	b	-	CHIPEDGE maximum x dimension (mm).	\leq	20.0
CE003b	b	-	CHIPEDGE maximum y dimension (mm).	\leq	20.0





3.36 Latchup Guidelines, Layout Constraints, and Rules

The BiCMOS8HP process was designed so that products built with good design practices would have sufficient latchup immunity. The following layout restrictions and recommendations provide guidelines for maintaining sufficient latchup immunity. When verifying that a design meets these rules the designer must consider all operating conditions of the circuit (normal operation, power up, power down, test, disconnect, etc.

3.36.1 Introduction

Latchup occurs when diffusions are placed in close proximity to each other and they form a PNP or NPN, often referred to as a silicon controlled rectifier (SCR) or thyristor. Latchup is destructive if the holding voltage is less than the V_{dd} supply. Destruction will occur in this case if V_{dd} > V_{holding} after the triggering of the SCR. The parasitic SCR can be triggered by three mechanisms; overshoot, undershoot and hot electron/hole generation. There are two categories of latchup; internal latchup and external latchup. Internal latchup occurs to circuits which are not connected to I/O or signal pads (C4 or wirebond pads) and external latchup occurs to circuits which are connected to I/O or signal pads.

3.36.2 Electrical Measurements

Electrical measurements to evaluate the latchup sensitivity of the technology is shown in Table 3-64. The parameters of interest are the bipolar current gain of the parasitic npn transistor (β_{npn}) and pnp transistors (β_{pnp}) (note:at a current of 1 mA), the voltage overshoot (V_{over}), the current overshoot (I_{over}), the voltage undershoot (V_{under}), the current undershoot (I_{under}), and the holding voltage (V_{hold}) . These measurements represent the case where a dc supply voltage is present on the structure with a transient pulse superimposed on the dc voltage and ground state conditions. The structure represented is the minimum p+/n+ space supported in the technology. The latchup results are shown for different substrate contact-to-diffusion spacings below the substrate contact spacing requirement (See Table 3-4, “N-well, Contact, Junction Layout Rules,” on page 83). Measurements were taken at a temperature of 140 C.

Table 3-64.Latchup Electrical Measurements (Minimum Design Space @ 140 C).						
Latchup Parameter	Substrate Contact to Diffusion Spacing (μm)					
	0.44	1.0	5.0	10	20	50
β_{npn}	3.4	3.5	4.1	4.2	4.2	4.8
β_{pnp}	1.9	1.92	1.92	1.92	1.92	1.78
V _{over} (V)	1.06	1.06	0.98	0.90	0.85	0.82
V _{under} (V)	-0.96	-0.96	-1.02	-1.08	-1.04	-1.2
I _{over} (mA)	8.0	7.0	4.5	3.5	2.5	2.0
I _{under} (mA)	-10.0	-10.0	-10.0	-10.0	-10.0	-10.0
V _{hold} (V)	2.05	1.95	1.8	1.8	1.75	1.65

3.36.3 Latchup Considerations

3.36.3.1 Latchup Prevention Recommendations

Internal

To ensure internal latchup triggering does not occur the following guidelines should be used. Overshoot and undershoot should be limited to less than 0.4V. Hot electron/hole generation should be limited such that the Substrate and Nwell voltage excursions should be less than 0.4V ($V_{sub_local} = I_{sx} * R_{sx}$, where I_{sx} = Substrate/Nwell current generated by impact ionization from NFETs or PFETs respectively and where R_{sx} = Substrate/Nwell resistance).

An Array N-well MUST have an N-well guard ring biased at Vdd and a substrate guard ring in the following cases:

- The array N-well is biased by an on-chip bias generator.
- Overshoot or undershoot is a concern.

This structure must exist on any edge where there is a concern for internal undershoot voltage or overshoot voltage being generated. It is recommended that for large arrays a guard ring be used because of edge bit leakage mechanisms.

External

External latchup considerations should address NWell and Substrate Guard Rings (Rule LUP13R), power sequencing, and satisfy the JEDEC Latchup specification.

Power-up Sequencing

To avoid latchup, it is recommended that power-up sequences be clearly defined for the application and that the overshoot and undershoot criteria are met during power-up. Power up sequencing is a function of the ESD design and the I/O circuitry. Given a sequence independent ESD design, this is not a concern for the $V_{dd}(1)$ and $V_{dd}(2)$ power supplies. In designs with multiple grounds, it is critical that the sequencing of ALL grounds be taken into account in power up strategy. This is critical when using supply-supply ESD protection circuits and ESD designs with multiple V_{ss} and V_{dd} rails tied to external pins.

Single Ground

The ground should be well established prior to the power supply voltage application. Signal pins should not be sequenced prior to ground establishment.

Multiple Grounds

All ground potentials should be well established prior to any power supply voltage application. Where a sequencing process is defined, the differential voltage between any two grounds should be minimized to avoid voltage excursions in excess of the holding voltage condition. Mixed-voltage ground guard ring rules should be applied in environments where structures on one ground rail is adjacent to the structures to a second ground rail. ESD power clamp elements should be placed between the ground rails in order to minimize the voltage excursion triggering of latchup. ESD power clamp elements should be placed between the ground rail and its corresponding power supply to minimize the triggering of latchup.

Single Power Supply

The ground should be established prior to the power supply. The single power supply voltage should be settled and established prior voltage application of the signal pins.

Multiple Power Supplies

Where a sequencing process is defined, the differential voltage between any two power supplies should be minimized to avoid voltage excursions in excess of the holding voltage condition. Mixed-voltage ground guard ring rules should be applied in environments where structures on one ground rail is adjacent to the structures to a second ground rail. ESD power clamp elements should be placed between the two power supplies or between power supply and its corresponding ground rail in order to minimize the voltage excursion triggering of latchup.

3.36.3.2 Latchup Resistance Components

Internal latchup can occur via overshoots, undershoots or hot electron/hole generation. The variables are:

1. Beta of the parasitic devices determined by n+ to p+ spacing.
2. Substrate resistance, this is determined by (5) components shown in Figure 3-47, "Substrate Resistance Components" on page 224. The (5) components consist of the following resistances:
 - R1 - Vertical resistance of substrate guardring around chip
 - R2 - Horizontal resistance from substrate guardring around chip to the device
 - R3 - Vertical resistance of the local substrate contact
 - R4 - Horizontal resistance of the local substrate contact to the device
 - R5 - Vertical resistance beneath the device channel

R3 is determined by the area of the local substrate contact and is provided in Table 4-29, "Contact Resistance," on page 283. R4 is provided as a sheet resistance and the sheet rho in Table 4-31, "Conducting Film Thicknesses and Sheet Resistances at 25°C," on page 284. Controlling the upper limit of R3 is addressed in latchup rules LUP05R, and LUP06R and controlling the upper limit of R4 is addressed in rule LUP02R. See section 3.36.5, "Latchup Rules" on page 232.

3. NWell resistance, this is determined by (3) components shown in Figure 3-48, "NWell Resistance Components" on page 224. The (3) components consist of the following resistances:
 - R1 - Vertical resistance of the local NWell contact
 - R2 - Horizontal resistance of the local NWell contact to the device
 - R3 - Vertical NWell resistance beneath the device channel

R1 is determined by the area of the local NWell contact and is given in Table 4-29, "Contact Resistance," on page 283. R2 is provided as a sheet resistance and the sheet rho in Table 4-31, "Conducting Film Thicknesses and Sheet Resistances at 25°C," on page 284. The upper limit of R1 is controlled by rules LUP05R and LUP06R and the upper limit of R2 is controlled by rule LUP02R. See section 3.36.5, "Latchup Rules" on page 232.

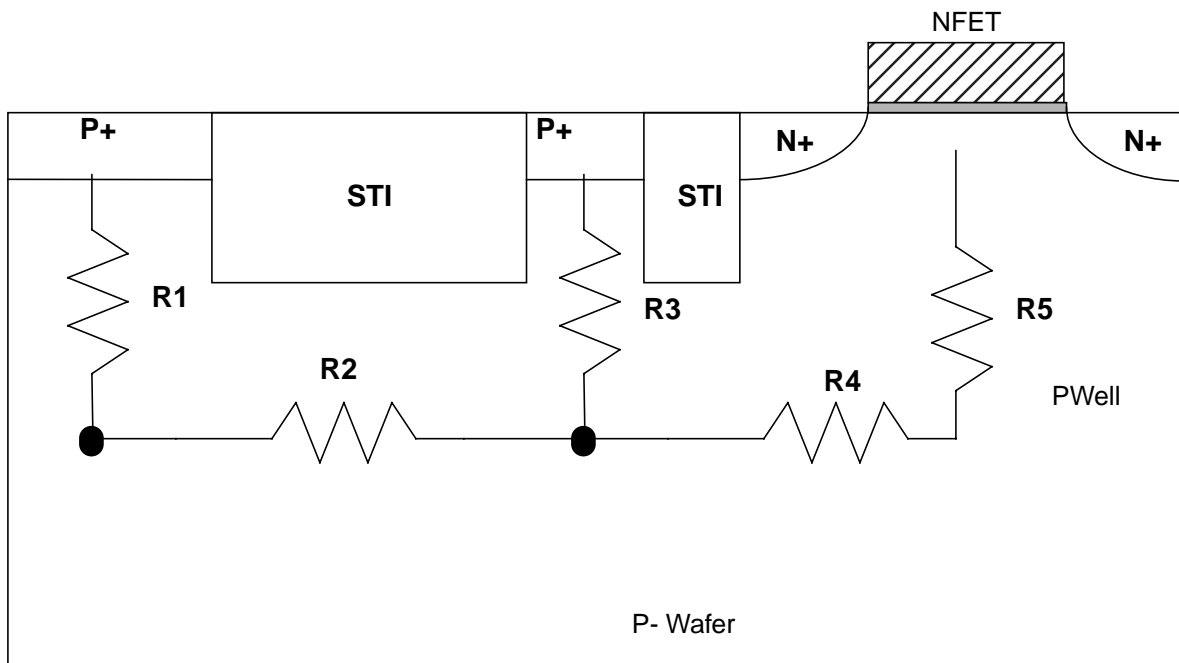


Figure 3-47. Substrate Resistance Components

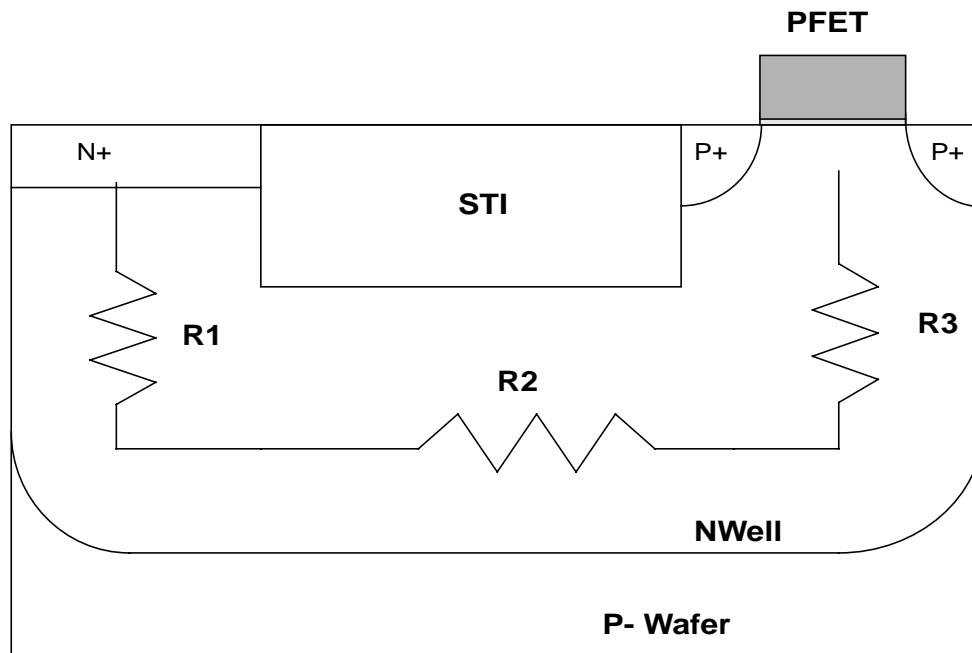


Figure 3-48. NWell Resistance Components

3.36.4 Guard Ring Layout

Figure 3-49, “Guard Ring Layout for CMOS I/O and Array N-Well Circuits.” on page 229 shows examples of designing a NWell and/or substrate guardring around structures connected to I/O pads (see Rule LUP13R) and examples of NWell guardrings around large arrays. The guardrings are designed to collective potential carriers flowing in the substrate between the NFET and PFET. The guardrings collect these carriers and there effectiveness is based on what is typically referred to as guardring efficiency (ratio of {carriers collected by guardring/carriers injected}).

3.36.4.1 Guard Rings

Native Voltage Circuits

- External Circuits for the native power supply should use a p+ substrate ring guard ring, a n-well guard ring and any allowed deep trench (DT) guard ring structures.

Non-Native Voltage Circuits

- Circuits for mixed voltage interface networks or voltage supplies above the native voltage should use a p+ substrate ring guard ring, a n-well guard ring, and any allowed deep trench (DT) guard ring structures. Additionally, usage of a n+ implant (inside an n-well) around the perimeter of any n-well improves latchup tolerance.

Some hints for improving guardring efficiency:

1. NWell guardrings, width of nwell guardring will improve its collection efficiency
2. NWell guardrings, the contacts and metal strapping improve its collection efficiency
3. Substrate guardrings, width of nwell guardring will improve its collection efficiency
4. Substrate guardrings, the contacts and metal strapping improve its collection efficiency as well as its effective resistance down to the actual substrate.
5. Deep Trench (DT) guardrings are to be placed around any injecting structure or sensitive circuits.
6. Deep Trench (DT) guardrings placed around a P+ substrate guardring and a NWell guardring will provide the maximum latchup tolerance.
7. Deep Trench (DT) guardrings that bound Nwells containing one or more PFETs improve latchup robustness.
8. Maximum latchup tolerance will be achieved with a Subcollector (NS) and Deep Trench (DT) bound Nwell structures.

Guard Ring Efficiency

Table 3-65. Guardring Efficiency Measurements at 25 Degrees Celsius	
Guardrings	Guardring Efficiency (I collected/I injected)
PP	0.342
P+ / NW	0.089
P+ / DT	0.058

Passive Elements

Resistors - Resistor elements which are connected to an external pad or power and a ROX opening (e.g. silicon resistor) should have a guard ring.

Capacitors - Capacitor elements which are connected to an external pad or power and a ROX opening (e.g. MOSCAP) should have a guard ring.

Active Elements

Triple Well (Isolated FET) - Triple Well (Isolated FETs) can initiate latchup when proper sequencing of the epitaxial region, substrate and the buried layer (e.g. subcollector) is not followed. The sequencing of the isolated epitaxial region and the buried layer should be such to avoid forward biasing.

Logic or Analog Sensitive Circuits

Gate Array - Gate array circuits adjacent to the peripheral circuit region (e.g. ESD, driver network) can have logic disturbs or latchup. To avoid this condition, gate array circuits should not be placed adjacent to peripheral circuits. Gate array elements should be placed at the External Latchup design rule spacing table to avoid logic disturbs and latchup. Guard rings should be placed between the gate array elements and the peripheral circuit region. Unused gate array segments should not be connected to the VDD and VSS power supplies. Deep Trench (DT) guardring can be placed around gate array regions to isolate from other injecting circuitry.

SRAM - SRAM circuits adjacent to the peripheral circuit region (e.g. ESD, driver network) can have logic disturbs or latchup. To avoid this condition, SRAM arrays should not be placed adjacent to peripheral circuits. SRAM array elements should be placed at the worst case External Latchup design rule spacing table to avoid SRAM disturbs. Deep Trench (DT) guardring can be placed around SRAM array regions to isolate from other injecting circuitry.

DRAM - DRAM cells and sense amplifiers adjacent to the peripheral circuit region (e.g. ESD, driver network) can have logic disturbs. To avoid this condition, DRAM arrays should not be placed adjacent to peripheral circuits. DRAM array elements and sense amplifier circuits should be placed at the worst case External Latchup design rule spacing table to avoid DRAM and sense amplifier timing disruption. Deep Trench (DT) guardring can be placed around DRAM array regions to isolate from other injecting circuitry.

I/O Rules

Receivers

- Half Pass Transistors - Half pass transistors connected to an external pad should place a guard ring to avoid electron injection into the chip substrate.
- Full Pass Transistors - Full pass transistor networks can latchup. Avoid usage of full pass transistor elements connecting to any external pad. Usage of a full pass transistor to an external pad requires a guard ring between the p-channel MOSFET and the n-channel MOSFET. A guard ring can be placed around the full pass transistor connected to the pad to avoid interaction with adjacent circuit nodes whose nodes support a node which can establish a parasitic pnpn condition.
- PFET Keeper Networks - PFET keeper feedback networks should utilize floating well bias control networks to minimize forward bias of the PFET source in mis-sequencing.

Drivers

- Single Transistor Pull down NFET- NFET transistors should be isolated from PFETs to prevent latchup using the guard rings.

- **Cascoded Transistor Pull down NFET**- For mixed voltage driver applications, where the power supply voltage is above the native voltage, guard rings associated with mixed voltage application should be used. The NFET transistors do not have to be separated from each other.
- **PFET Pull-up** - P-channel MOSFET latchup robustness increases by placement of a n+ diffusion implant inside the n-well edge along its perimeter. Deep Trench (DT) guardring can bound Nwells containing one or more PFETs improve latchup robustness.
- **Floating well PFET driver network** - For mixed voltage driver applications, using a floating well driver, the resistance in the well should be minimized to improve latchup tolerance. Deep Trench (DT) guardring can bound Nwells containing one or more PFETs improve latchup robustness.

ESD Networks

ESD Input Devices

- **N-well Diodes** - N-well diodes can lead to injection of electrons into the substrate to induce external latchup. N-well diodes must have a guard ring placed within close proximity of the diode structure to avoid substrate electron injection. An n-well guard ring placed 3 to 6 μm from the n-well diode edge connected to VDD reduces electron injection into the substrate. Placement of a p+ diffusion between the n-well diode and n-well guard ring reduces also reduces substrate injection. Placement of a trench guard ring about the n-well guard ring will further reduce the substrate injection and electron migration. This element can be avoided by utilization of a p+/n-well diode for negative injection. Deep Trench (DT) guardring can bound Nwell diodes to improve latchup robustness.
- **N+ Diodes** - N+ diodes can lead to injection of electrons into the substrate to induce external latchup. N+ diodes must have a guard ring placed within close proximity of the diode structure to avoid substrate electron injection. An n-well guard ring placed 3 to 6 μm from the n-well diode edge connected to VDD reduces electron injection into the substrate. Placement of a p+ diffusion between the n-well diode and n-well guard ring reduces also reduces substrate injection. Placement of a trench guard ring about the n-well guard ring will further reduce the substrate injection and electron migration. This element can be avoided by utilization of a p+/n-well diode for negative injection. Deep Trench (DT) guardring can bound N+ diodes to improve latchup robustness.
- **P+ Diode** -P+ diodes can lead to hole injection into the chip substrate. Lateral injection can be reduced with the usage of a n+ implant about the well perimeter contained within the n-well region. Placement of trench guard ring eliminates lateral injection. Addition of a subcollector implant reduces injection into the substrate. For positive pulses, the cathode is connected to VDD. For negative pulses, the anode is connected to VSS. Deep Trench (DT) guardring can bound P+/Nwell diodes to improve latchup robustness.
- **SiGe Varactor** - SiGe varactor structure can inject holes into the substrate. Subcollector reduces the injection into the substrate. For positive pulses, the cathode is connected to VDD. For negative pulses, the anode is connected to VSS.
- **NFET ESD Element** - NFET based ESD elements can lead to electron injection into the substrate. Sufficient guard rings (e.g. p+ substrate ring and n-well guard ring) should be placed on the NFET ESD to avoid electron injection into the substrate.

ESD Power Clamps

- **CMOS Power Clamps**
 - **RC Triggered MOSFET Power Clamps**
 - Resistor and Capacitor discriminator elements should have guard rings if the elements are

FEOL devices. Guard rings are not required for resistors and capacitors when utilizing BEOL elements (e.g. metal resistors, polysilicon resistors, MIM capacitors). These elements should be isolated from the complimentary elements of the drive circuit or clamp element.

- Inverter drive circuit require mixed voltage guard rings between the PFET and NFET elements. PFETs can be placed in the same well. NFETs can be placed in the same epitaxial region.
- NFET Clamp transistor must have a guard ring placed about the element to isolate from adjacent structures.
- Deep Trench (DT) guardring can bound the entire ESD power clamp to improve latchup robustness.
- Mixed Voltage RC Triggered MOSFET Power Clamps
 - Mixed voltage RC Triggered MOSFET power clamp must have a guard ring around the entire ESD power clamp and apply the same rules as shown above.
 - Deep Trench (DT) guardring can bound the entire ESD power clamp to improve latchup robustness.
- SiGe Bipolar Power Clamps
 - The SiGe bipolar ESD power clamp NPN output transistor must be separated from adjacent circuitry by 5 microns.
 - Deep Trench (DT) guardring can bound the entire ESD power clamp to improve latchup robustness
- Mixed Voltage SiGe Bipolar Clamps
 - Mixed voltage SiGe ESD power clamp diode string trigger network should be separated from adjacent circuitry by 8 microns. The mixed voltage SiGe ESD power clamp trigger network must not be within 5 microns of the SiGe NPN output clamp.
 - Deep Trench (DT) guardring can bound the entire ESD power clamp to improve latchup robustness
- ESD Rail-to-Rail Clamps
 - ESD Rail-to-Rail clamps require a P+ substrate ring and NW guard ring around the structure.
 - Deep Trench (DT) guardring can bound the entire ESD power clamp to improve latchup robustness

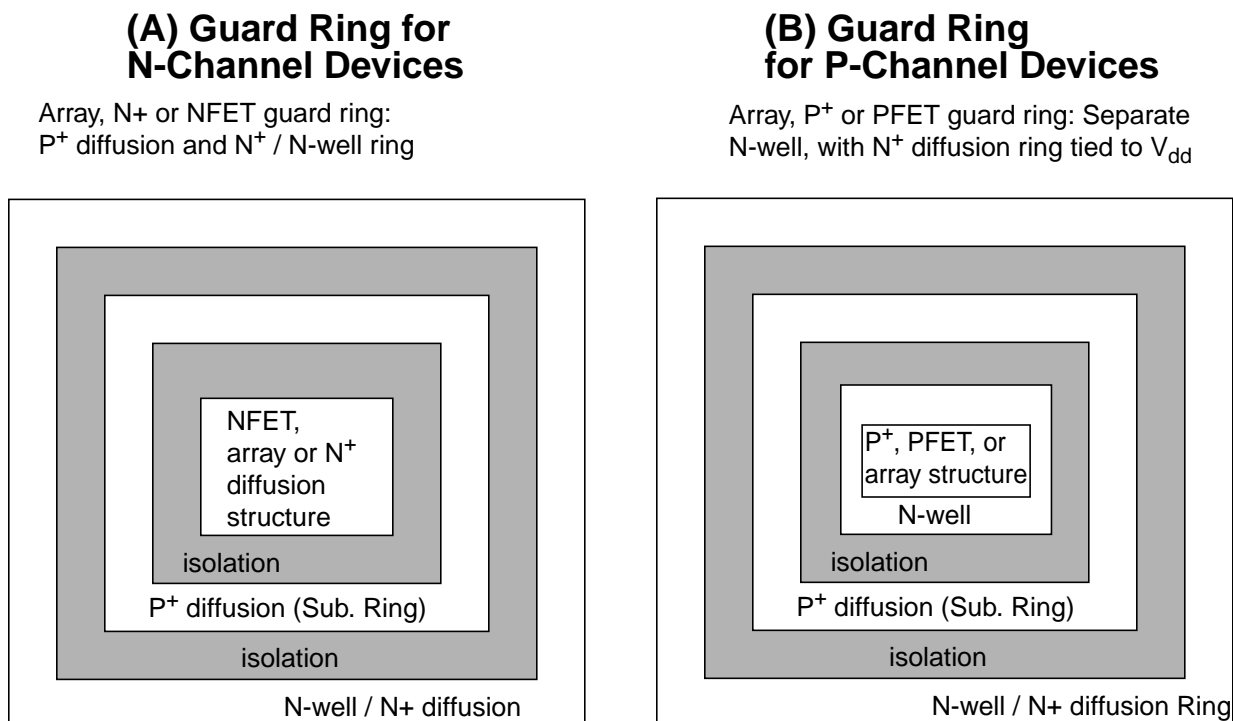


Figure 3-49. Guard Ring Layout for CMOS I/O and Array N-Well Circuits.

The guard rings for NFETs and PFETs are shown in Figure (A) and (B) respectively.
The N⁺/N-well Guard Ring for both NFETs and PFETs is connected to V_{dd}.

The I/O guard rings protect circuits connected to I/O pads against latchup.

Rules for I/O Guard Rings:

- Any N⁺ diffusion connected to an I/O pad MUST lie within a substrate (P⁺) and a NWell guardring (Rule LUP13R). These circuits include:
 - OCD (off-chip driver NFETs), protect diodes, ESD protect circuit, pass transistors, diodes, bleed transistors, diffusion resistors, etc.

Note: The NWell guardrings around a specific I/O book are allowed to merge with adjacent I/O's guardrings. Also, internal to a specific I/O the NFET's NWell guardring can merge with the ESD device's NWell guardring and/or the PFETs NWell guardring.

- The NWell guardring specified in item #1 above must obey the following groundrule:
 - ESD10 (N-well-to-RX distance rule)
- All p-channel transistors, or P⁺ diodes attached to I/O circuitry MUST be in a separate N-well which is separate from other chip circuitry by a substrate guard ring.

- For isolation, an N⁺/N-well guard ring surrounds the substrate guard ring and N-well tub of the P⁺ diffusion or PFET structure.
 - The N-well guard ring is to be tied to V_{dd} or $V_{dd(I/O)}$.
 - Minimum well-well space can be used.
 - When using separate N-well guard ring structures outside of the p-channel's well structure, this structure can be abutted to other separate N-well ring structures.
 - Deep Trench (DT) guarding can bound the entire circuit to improve latchup robustness.
- 4. Those portions of the substrate bias charge pump or well bias generator circuits where the voltage is biased below ground potential or above the supply voltage must fulfill the rules above (see I/O circuits). The same applies for voltage regulator or bootstrap circuits.
- 5. Guardrings (Nwell or substrate) should be contacted as frequently as possible and strapped with metal wherever possible. Latchup rule LUP13R ensures N⁺ diffusions connected to I/O pads are enclosed in both substrate and Nwell guardrings. Guardring design layouts are available.
- 6. Rules LUP02R specify substrate contact spacing between Nwells. Paths to substrate contacts to satisfy LUP02R between minimum spaced Nwells should be avoided. See Figure 3-50, “Substrate Contact Occurring Between Adjacent NWells” on page 230.

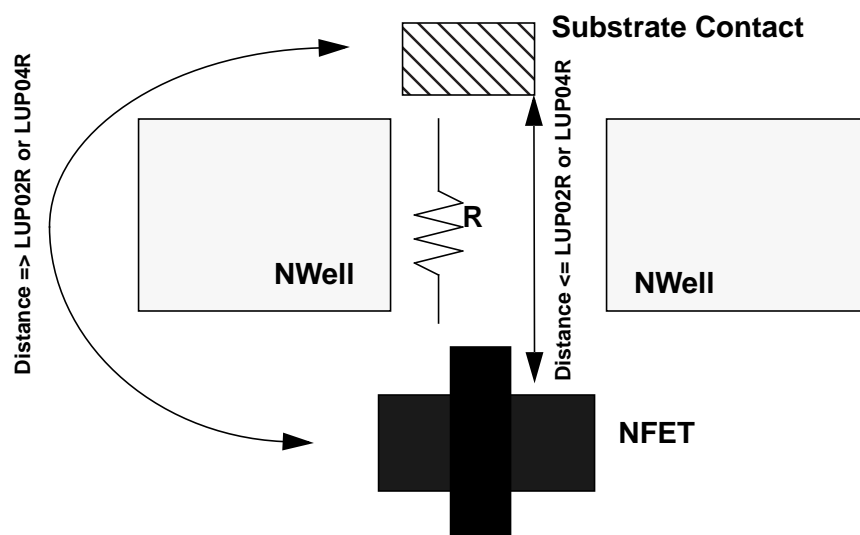


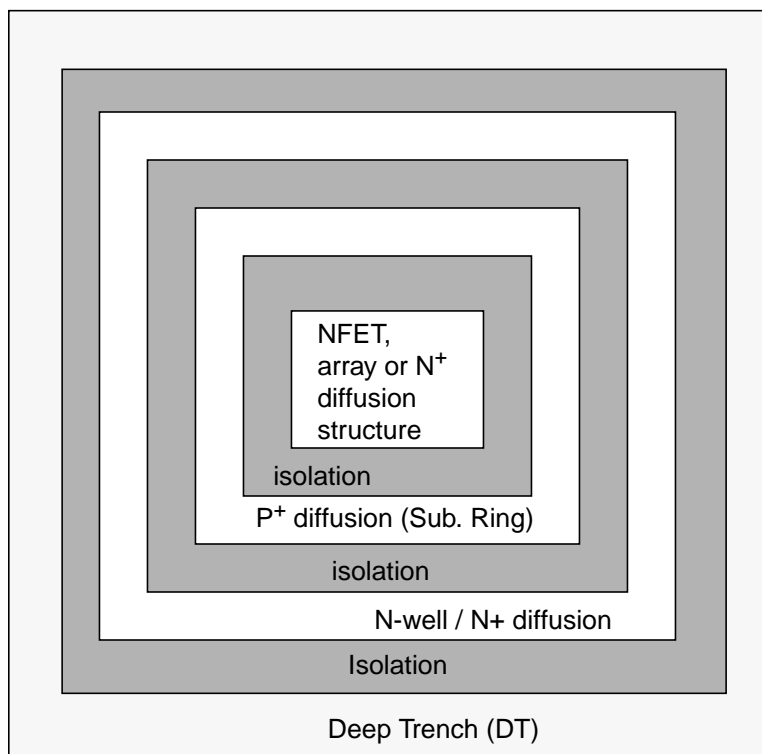
Figure 3-50. Substrate Contact Occurring Between Adjacent NWells

Rules for Deep Trench Guard Rings

- For N⁺ areas to be protected, DT must surround both the N⁺ area and also a P⁺ substrate contact, as shown in Figure 3-51, on page 231. The P⁺ substrate contact must contain design levels RX and BP and must be electrically tied (with metal) to ground. Isolation separates the NWell and DT guardrings.
- For P⁺ areas to be protected, DT must surround both the P⁺ area and also a N⁺ NWell contact, as shown in Figure 3-51, on page 231. The DT covers the NWell edge. The N⁺ contact must contain the design level RX and preferably RN. The N⁺ contact must be electrically tied (with metal) to V_{high}.

(A) DT Guard Ring for N-Channel Devices

Array, N+ or NFET guard ring:
P⁺ diffusion and N⁺ / N-well ring
and Deep Trench



(B) DT Guard Ring for P-Channel Devices

Array, P⁺ or PFET guard ring: Separate
N-well, with N⁺ diffusion ring tied to V_{dd}

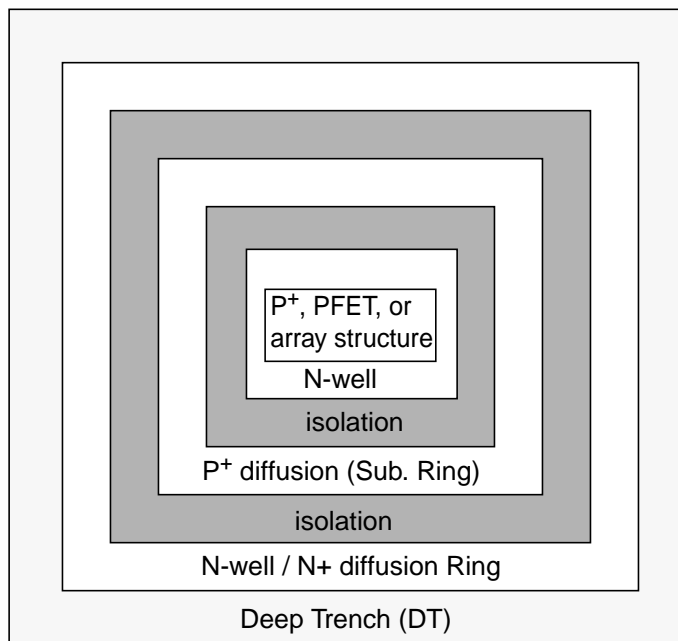


Figure 3-51. Deep Trench Guard Ring Layout

3.36.5 Latchup Rules

The latchup rules provided in Table 3-66, on page 232 are identified as recommended rules. However, rules LUP01R, LUP02R, LUP03R, LUP04R, LUP05R LUP06R, LUP07R and LUP08R reference other layout rules within this document whose criteria are Design Rule Checked (DRC) to their Design Minimum values and the reference rule is not considered recommended.

Table 3-66. Latchup Rules					
Rule	Class	Notes	Description		Design Min.
LUP01R	d	-	Nwell contact distance to thin-oxide PFET and p+ junctions, refer to Rule 268 (see Table 3-4, “N-well, Contact, Junction Layout Rules,” on page 83) --> Limit resistance from PFET source/drain and p+ junctions to NW contact inside Nwell (thin-oxide PFET and p+ junctions)	=	-
LUP02R	d	-	Substrate contact distance to thin-oxide NFET and n+ junctions, refer to Rule 268b (see Table 3-4, “N-well, Contact, Junction Layout Rules,” on page 83). --> Limit resistance from NFET source/drain and n+ junctions to SX contact (thin-oxide NFET and n+ junctions)	=	-
LUP03R	d	-	Nwell contact distance to thick-oxide PFET and p+ junctions, refer to Rule DG268a (see Table 3-44, “DG Layout Rules,” on page 170). --> Limit resistance from PFET source/drain and p+ junctions to NW contact inside Nwell (thick-oxide PFET and p+ junctions)	=	-
LUP04R	d	-	Substrate contact distance to thick-oxide NFET and n+ junctions, refer to Rule DG268b (see Table 3-44, “DG Layout Rules,” on page 170). --> Limit resistance from NFET source/drain and n+ junctions to SX contact (thick-oxide NFET and n+ junctions)	=	-
LUP05R	d	-	RX P+ junction within NW, refer to Rule 260 (see Table 3-4, “N-well, Contact, Junction Layout Rules,” on page 83). --> P+ inside NW, defines minimum lateral PNP (P+/NW/SX) base width (thin-oxide diffusions)	=	-

Table 3-66. Latchup Rules

Rule	Class	Notes	Description		Design Min.
LUP06R	d	-	RX N+ junction to adjacent NW, refer to Rule 265 (see Table 3-4, “N-well, Contact, Junction Layout Rules,” on page 83). --> N+ to adjacent NW, defines minimum lateral NPN (N+/SX/NW) base width (thin-oxide diffusions)	=	-
LUP07R	d	-	(RX P+ junction touching DG) within NW, refer to Rule DG260 (see Table 3-44, “DG Layout Rules,” on page 170). --> P+ inside NW, defines minimum lateral PNP (P+/NW/SX) base width (thick-oxide diffusions)	=	-
LUP08R	d	-	(RX N+ junction touching DG) to adjacent NW, refer to Rule DG265a (see Table 3-44, “DG Layout Rules,” on page 170). --> N+ to adjacent NW, defines minimum lateral NPN (N+/SX/NW) base width (thick-oxide diffusions)	=	-
LUP09A	b	-	(Total area of RX intersect BP outside {BB,NW}) / (Total {PC intersect RX} outside {BB,NW}) over local $(2.1XLUP02)^2$ area stepped in $((2.1XLUP02)/2)$ increments (Applicable if burn-in or in general elevated voltage stressing will NOT occur) --> Limit amount of vertical SX resistance seen by thin-oxide NFETs in a given tile	≥	0.01
LUP09B	b	-	(Total area of RX intersect BP outside {BB,NW}) / (Total {PC intersect RX} outside {BB,NW}) over local $(2.1XLUP02)^2$ area stepped in $((2.1XLUP02)/2)$ increments (Applicable if burn-in [1.5X Vdd] WILL occur) --> Limit amount of vertical SX resistance seen by thin-oxide NFETs in a given tile	≥	0.2

Table 3-66. Latchup Rules

Rule	C l a s s	Notes	Description		Design Min.
LUP10A	b	-	(Total area of RX intersect NW outside BP) / (Total {PC intersect RX and BP} inside NW) over local $(2.1XLUP01)^2$ area stepped in $((2.1XLUP01)/2)$ increments (Applicable if burn-in or in general elevated voltage stressing will NOT occur) (For each Nwell within the tile, the ratio should be checked separately) --> Limit amount of vertical NWell resistance seen by thin-oxide PFETs in a given tile	≥	0.01
LUP10B	b	-	(Total area of RX intersect NW outside BP)/(Total {PC intersect RX and BP} inside NW) over local $(2.1XLUP01)^2$ area stepped in $((2.1XLUP01)/2)$ increments (Applicable if burn-in, [1.5X Vdd] WILL occur) (For each Nwell within the tile, the ratio should be checked separately) --> Limit amount of vertical NWell resistance seen by thin-oxide PFETs in a given tile	≥	0.2
LUP11A	b	-	(Total area of RX intersect BP outside {BB,NW}) / (Total {(PC intersect RX) over DG} outside {BB,NW}) over local $(2.1XLUP02)^2$ area stepped in $((2.1XLUP02)/2)$ increments (Applicable if burn-in or in general elevated voltage stressing will NOT occur) --> Limit amount of vertical SX resistance seen by thick-oxide NFETs in a given tile	≥	0.06
LUP11B	b	-	(Total area of RX intersect BP outside {BB,NW}) / (Total {(PC intersect RX) over DG} outside {BB,NW}) over local $(2.1XLUP02)^2$ area stepped in $((2.1XLUP02)/2)$ increments (Applicable if burn-in [1.5X Vdd] WILL occur) --> Limit amount of vertical SX resistance seen by thick-oxide NFETs in a given tile	≥	1.0

Table 3-66. Latchup Rules

Rule	Class	Notes	Description		Design Min.
LUP12A	b	-	(Total area of RX intersect NW outside BP) / (Total {(PC intersect RX and BP} over DG inside NW) over local (2.1XLUP01) ² area stepped in ((2.1XLUP01)/2) (Applicable if burn-in or in general elevated voltage stressing will NOT occur) (For each Nwell within the tile, the ratio should be checked separately) --> Limit amount of vertical NWell resistance seen by thick-oxide PFETs in a given tile	≥	0.06
LUP12B	b	-	(Total area of RX intersect NW outside BP) / (Total {(PC intersect RX and BP} over DG inside NW) over local (2.1XLUP01) ² area stepped in ((2.1XLUP01)/2) (Applicable if burn-in, [1.5X Vdd] WILL occur) (For each Nwell within the tile, the ratio should be checked separately) --> Limit amount of vertical NWell resistance seen by thick-oxide PFETs in a given tile	≥	1.0
LUP13	b	1	RX N+ (RX not over BP) shapes connected to an IO signal pad must be contained within a Substrate guard ring (RX over BP) and a Nwell guard ring (N+ inside NW). The guard rings must be within ≤ 15 μm from at least one edge of the RX shape. No P+ shapes within NW are allowed within this guardring. --> NW guardring is used to collect minority electrons injected into the substrate.	=	-
LUP13aR	d	-	{[NW touching (RX n-well contact guard ring, satisfying Rule LUP13)] over ESDUMMY} minimum width.	≥	2.0
LUP13bR	d	-	[CA over (RX n-well contact guard ring, satisfying Rule LUP13a)] maximum space.	≤	10.0
LUP14A	b	-	NW of ESD01b must be enclosed within a P+ diffusion ring (substrate ring)	=	-
LUP14B	b	-	Inside edge of P+ diffusion ring of LUP14A must be placed near the outer edge of the NW of ESD01b	≤	5.0
LUP15A	b	-	LUP14A P+ diffusion rings must have a width [μm].	≥	1.0
LUP15B	b	-	LUP14A P+ diffusion rings must have CA/CA spacing [μm]	≤	10.0

1. P+ shapes within NW are allowed within this guardring.

3.36.5.1 Notes:

- GR = groundrule in above table
- SX = substrate in above table
- NW = NWell in above table
- Substrate contacts are defined as (BP intersect RX) outside of (NW or BB)
- NWell contacts are defined as (RX intersect NW) outside BP
- Substrate is defined as the compliment of (NW or BB)
- Window shapes are squares of size $(2.1 * GR / 268)$ and the windows are stepped across the data in increments of $((2.1 * GR / 268) / 2)$
- N-Type gate is defined as (RX intersect PC) outside (BP or BP) and outside NW
- P-Type gate is defined as (RX intersect PC) inside BP and inside NW
- N-Type DG gates are defined as N-Type gates inside DG
- P-Type DG gates are defined as P-Type gates inside DG
- All thin oxide NFET with channel lengths $> 1.5 \times$ (Rule 1) should NOT be included for checking
- All thin oxide PFET with channel lengths $> 1.5 \times$ (Rule 2) should NOT be included for checking
- All thick oxide NFET with channel lengths $> 1.5 \times$ (Rule DG8a) should NOT be included for checking
- All thick oxide PFET with channel lengths $> 1.5 \times$ (Rule DG8b) should NOT be included for checking
- For latchup ratio rules, a gate only fails if it is hit by a failing window
- In a given tile, the thick oxide gate areas should be weighed by the ratio of LUP11A/LUP09A (i.e. DG gate area \times LUP11A/LUP09A) and the tile used should be the same as that used in LUP9A
- In a given tile, the thick oxide gate areas should be weighed by the ratio of LUP11B/LUP09B (i.e. DG gate area \times LUP11B/LUP09B) and the tile used should be the same as that used in LUP9B
- In a given tile, the thick oxide gate areas should be weighed by the ratio of LUP12A/LUP10A (i.e. DG gate area \times LUP12A/LUP10A) and the tile used should be the same as that used in LUP10A
- In a given tile, the thick oxide gate areas should be weighed by the ratio of LUP12B/LUP10B (i.e. DG gate area \times LUP12B/LUP10B) and the tile used should be the same as that used in LUP10B
- For checking time improvement, Nwells with a ratio $> 10 \times$ (LUP10A or LUP10B or LUP112A or LUP12B) maybe screened out as passed.



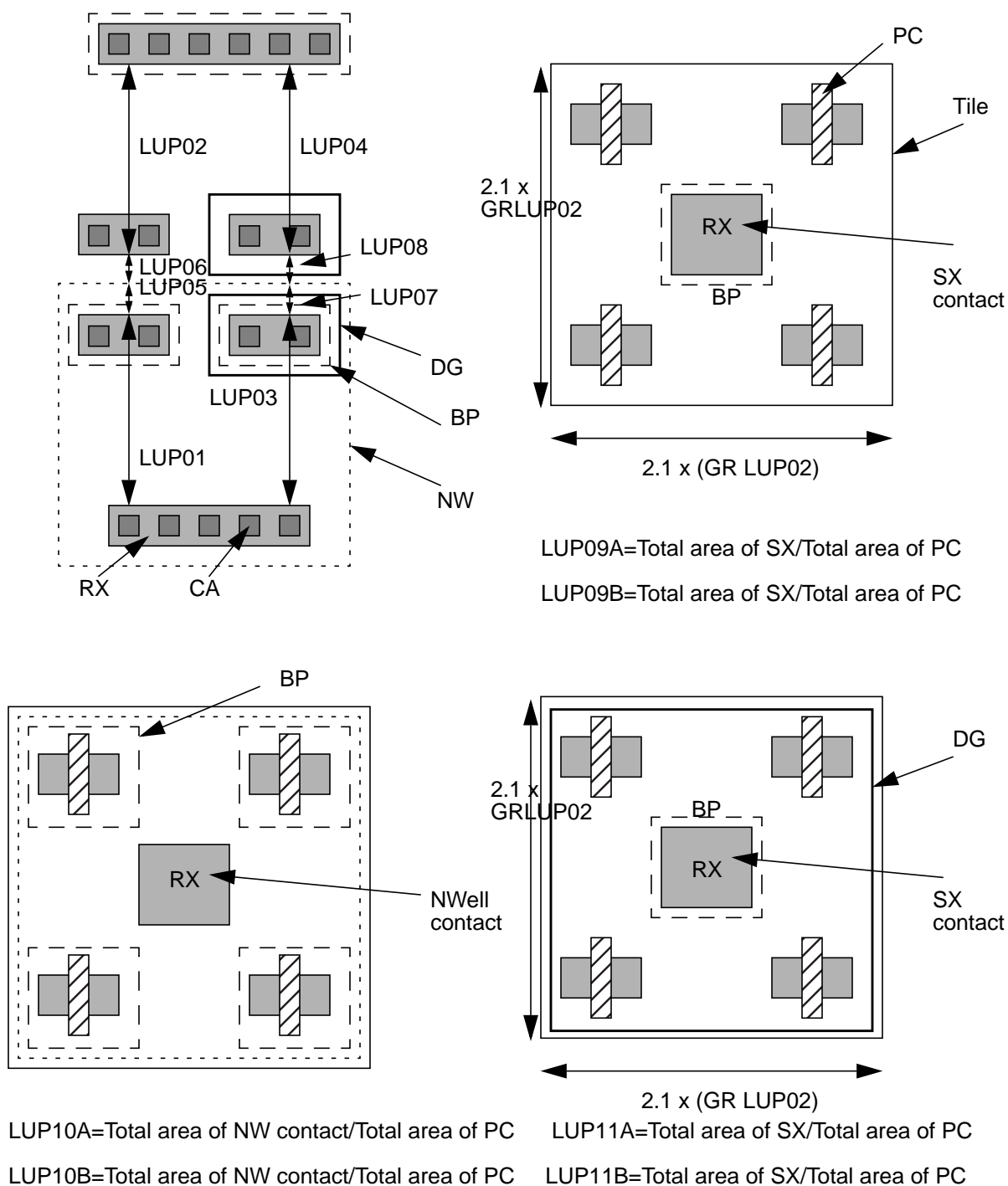


Figure 3-52. Latchup Rule Figure

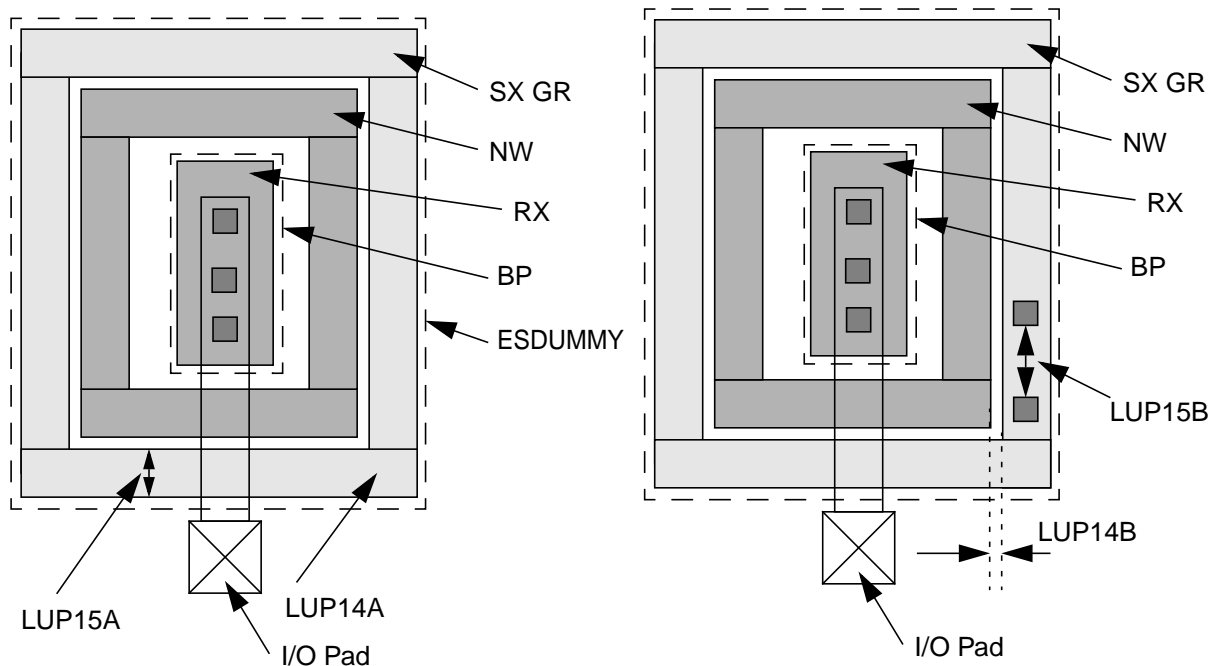
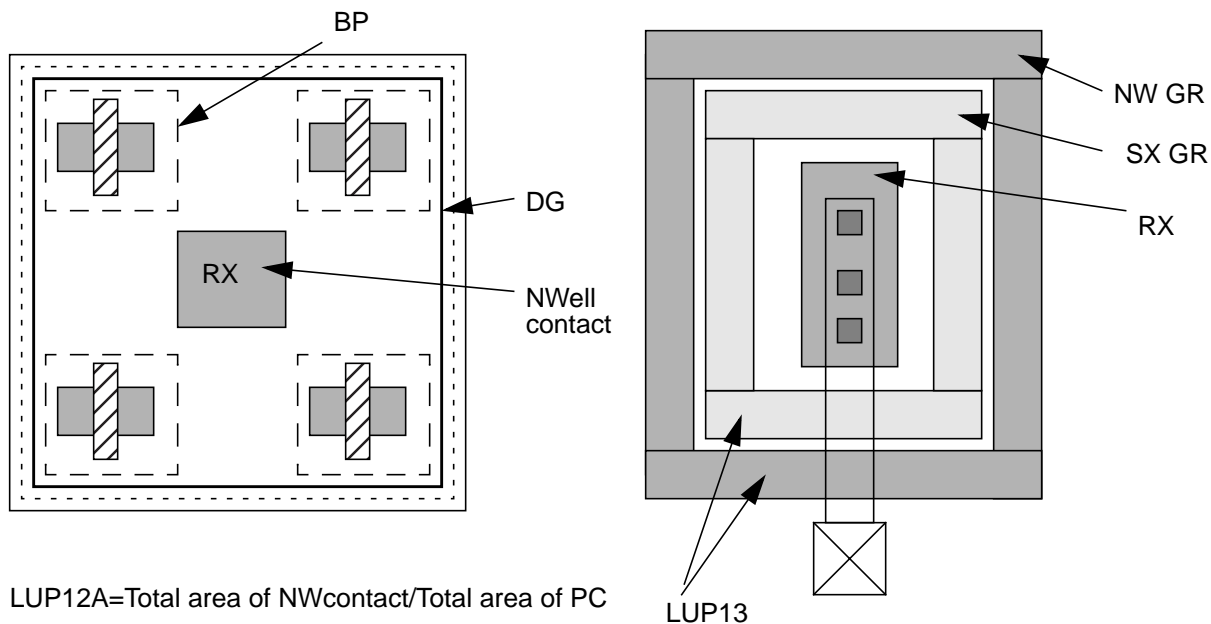


Figure 3-53. Latchup Rule Figure

3.36.6 External Latchup Design Rules

Array I/O

Array I/O can induce latchup as a result of influencing adjacent circuitry. See the table below. Array I/O should keep sensitive circuits away from the negative injecting elements to avoid latchup or noise disruptions. Deep Trench (DT) guarding can bound the entire Array I/O to improve external latchup robustness

Peripheral I/O

Peripheral circuit perimeter I/O are placed on the perimeter of a chip. Peripheral circuits should place the ESD element and noise injecting elements toward the outside of the chip design to minimize external latchup. See the table below on placement of the sensitive circuits relative to the injection source. Deep Trench (DT) guarding can bound the entire Peripheral I/O to improve external latchup robustness.

Circuit Design under external latchup conditions

Circuit elements adjacent to ESD networks or I/O element that serves as an injection source can lead to latchup. These sensitive circuits may include CMOS gate array elements, SRAMs, sense amplifiers, Full pass transistors, and other CMOS circuits. To obtain a latchup margin to a 200 mA negative injection source, the injection source to circuit space can be reduced by placement of substrate and well contacts below the design manual minimum and provide latchup hardening of the CMOS circuit. Further hardening can be achieved by reducing the n-well contact to PFET spacing equivalent to the Substrate Contact spacing to provide additional margin to the 200 mA latchup objective. For additional information, For additional information, see Table 3-67.

<i>Table 3-67. External Latchup Design Guidelines</i>		
Injection Source-to-Circuit Space (μm)	Substrate Contact-to-FET Space¹ (μm)	Latchup Margin (mA)
200	15	-200
150	10	-200
100	5	-200
50	2.5	-200

1. Values shown in Table 3-67 are below values stated in LUP02R or LUP04R (see Table 3-66, on page 232 or its corresponding layout rule in the referenced Tables).



This Page Intentionally Left Blank

4.0 Electrical Parameters and Models

4.1 Available Devices and Models

All the dimensions in this section are wafer dimensions, unless specified otherwise.

The electrical parameters are given for T=25C, unless specified otherwise.

The following tables list the available devices in this technology. For information on design levels, see Table 2-8, "Design Truth Table," on page 49.

<i>Table 4-1. Device models offered</i>		
Device Name	Model Name	Comment
Si/SiGe HBT	vbic	High Performance and High Breakdown NPN
Regular NFET	nfet nfet_rf	Thin oxide n-type FET device
Regular PFET	pfet pfet_rf	Thin oxide p-type FET device
Thick NFET25 (Regular IO NFET)	dgnfet dgnfet_rf	Thick oxide n-type FET device
Thick PFET25 (Regular IO PFET)	dgpfet dgpfet_rf	Thick oxide p-type FET device
NFETTW Thin Triple Well NFET	nfettw nfettw_rf	Thin oxide n-type device in triple well
NFET25TW Thick Triple Well NFET	dgnfettw dgnfettw_rf	Thick oxide n-type device in triple well
OP P+Poly Resistor	opppres	P type doped OP polysilicon resistor
RR Poly Resistor	oprrpres	P type lightly doped OP polysilicon resistor
NS N+ Diffusion Resistor	nsres	N+ subcollector resistor
KQ BEOL Resistor	kqres	Back-End-Of-Line resistor
nMOS varactor Thin Ox	ncap	NFET-in-Nwell MOS capacitor with tox=2.2nm
nMOS varactor Thick Ox	dgncap	NFET-in-Nwell MOS capacitor with tox=5.2nm
HA Varactor	havar	Tunable diode varactor
MIM	mim	Metal-Insulator-Metal capacitor

Table 4-1. Device models offered

Device Name	Model Name	Comment
E-fuse	efuse	Electronic fuse
Inductor	ind	Single layer inductor
	symind	Symmetric, single layer inductor
Transmission Line	singlewire	Single wire microstrip transmission line
Coupled Trans. Line	coupledwires	Two coupled wires microstrip transmission line
RF Interconnect	rfline	AM line over DT lattice
Coplanar Waveguide	singlecpw	Single wire coplanar waveguide
	coupledcpw	Two wires coplanar waveguide
Bondpad	bondpad	C4 and wirebond bondpad
Substrate Contact	subc	Substrate contact
NW/SX diode	diodenwx	Parasitic diode. Reverse bias use only.
N+/SX diode	diodenx	Parasitic diode. Reverse bias use only.
P+/Nwell diode	diodepnw	Parasitic diode. Reverse bias use only.
Niso(PI)/SX diode	diodepisx	Parasitic diode. Reverse bias use only.
PW/Niso(PI) diode	diodewpwi	Parasitic diode. Reverse bias use only.
ESD N+/SX diode	esdndsx	N+/SX junction diode. For ESD use only.
ESD NW/SX diode	esdnwsx	NW/SX junction diode. For ESD use only.
ESD P+/NW diode	esdvnpn	P+/NW junction diode. For ESD use only.
Distributed Passives	See section 4.21 , “Distributed Passive (DP) Devices” on page 313.	

4.2 Si/SiGe Heterojunction Bipolar Transistor

The BiCMOS-8HP technology offers a high performance and high breakdown vertical NPN bipolar transistor. The high performance NPN provides the fastest performance with the specifications given in Table 4-2. The high breakdown NPN has the highest breakdown characteristics with specifications given in Table 4-3.

Supported layouts consist of single emitter stripe devices with a fixed emitter (EX) width of 0.12 μm . The emitter length can be scaled to obtain the desired current rating with a minimum length equal to 0.52 μm and a maximum length of 18 μm . The high frequency device is offered in both CBEBC and CBE configurations while the high breakdown device is offered in CBEBC only. To handle higher current densities the p-cell permits an increase in the number of collector contact rows as well as the base metal width.

All NPNs have polysilicon emitters with a non-self-aligned extrinsic base. Note that the device model library is based entirely on the standard devices provided in the device set layout. Use of other device layout/geometries is not supported. Should you require modeling support for other geometries, please contact your IBM Product Engineer.

The following table contains standard device specs which represent 3-sigma process capability targets.

<i>Table 4-2. Electrical Parameters for High Performance NPN (0.12 μm x 2.5 μm)</i>					
Parameter	Units	Minimum	Nominal	Maximum	Conditions
V_{BE}	Volts	0.696	0.726	0.756	$I_C = 10 \mu\text{A}$, $V_{CB} = 0$
Beta		100	600		$V_{BE} = 0.72 \text{ V}$, $V_{CB} = 0$
$f_T(\text{peak})$	GHz	180	200		$V_{CB} = 0.5 \text{ V}$, $I_C = 12 \text{ mA}/\mu\text{m}^2$
BVEBO	Volts	1.2	2.1		$I = 10 \mu\text{A}$
BVCBO	Volts	5.5	5.9		$I = 10 \mu\text{A}$
BVCEO	Volts	1.5	1.77		$I = 10 \mu\text{A}$
BVCSO	Volts	20	50		$I = 10 \mu\text{A}$

<i>Table 4-3. Electrical Parameters for High Breakdown NPN (0.12 μm x 2.5 μm)</i>					
Parameter	Units	Minimum	Nominal	Maximum	Conditions
V_{BE}	Volts	0.698	0.728	0.758	$I_C = 10 \mu\text{A}$, $V_{CB} = 0$
Beta		94	470		$V_{BE} = 0.72 \text{ V}$, $V_{CB} = 0$
$f_T(\text{peak})$	GHz	44	57		$V_{CB} = 1.0 \text{ V}$, $I_C = 1.4 \text{ mA}/\mu\text{m}^2$
BVEBO	Volts	1.2	2.1		$I = 10 \mu\text{A}$
BVCBO	Volts	9	12		$I = 10 \mu\text{A}$
BVCEO	Volts	3.1	3.55		$I = 10 \mu\text{A}$
BVCSO	Volts	20	50		$I = 10 \mu\text{A}$

Note: In the above tables, BV_{ceo} is not a voltage limit for biasing unless the NPN is operated under a forced I_b condition. V_{ce} greater than BV_{ceo} is allowed for other bias configurations, lower base impedance leading to higher voltage limits.

4.3 Vertical PNP Bipolar Transistor

The BiCMOS8HP technology offers a vertical PNP (VPNP) bipolar transistor. Supported layouts include single and dual emitter stripe devices with fixed emitter (EV) widths of 0.4 μm and 0.8 μm . The emitter length can be scaled to obtain the desired current rating, up to a maximum of 20 μm . The minimum emitter length is 1.2 μm for the 0.4 μm wide device, and 2.4 μm for the 0.8 μm wide device.

The vertical PNP has a polysilicon emitter with a non-self-aligned extrinsic base and an implanted subcollector. Note that the device model library is based entirely on the standard devices provided in the device set layout. Use of other device layout/geometries is not supported. Should you require modeling support for other geometries, please contact your IBM Product Engineer.

The following table contains standard device specs which represent 3-sigma process capability targets.

Table 4-4. Electrical Parameters for the Vertical PNP (0.4 μm x 2.5 μm , single emitter)

Parameter	Units	Minimum	Nominal	Maximum	Conditions
V_{BE}	Volts	-0.775	-0.790	-0.805	$I_C = -10 \mu\text{A}$, $V_{CB} = 0$
Beta		80	230	450	$V_{BE} = -0.78 \text{ V}$, $V_{CB} = 0$
$f_T(\text{peak})$	GHz	15	17	19	$V_{CB} = -3\text{V}$, $I_C = -1.0 \text{ mA}/\mu\text{m}^2$
V_{Early}	Volts	12	30	60	$V_{BE} = -0.8\text{V}$, $V_{CE} = -2\text{V} \rightarrow -3.75\text{V}$
BVEBO	Volts	2.4	2.8		$I = -10 \mu\text{A}$
BVCBO	Volts	15	18		$I = -10 \mu\text{A}$
BVCEO	Volts	6.5	8.2	12	$I = -10 \mu\text{A}$
Maximum Allowed V_{CE} ¹	Volts			-3.6V	
V_{BE} Matching ²	mV	-0.94	0	+0.94	$V_{CB} = 0\text{V}$, $I_E = -10\mu\text{A}$, adjacent vpmps
Beta Matching ²	%	-8.1	0	+8.1	$V_{CB} = 0\text{V}$, $I_E = -10\mu\text{A}$, adjacent vpmps

1. The maximum allowed Vce to ensure device reliability is set as per Section 5.3.9 , “VPNP Bipolar Reliability” on page 357. BVCEO is not the limiting factor for reliable device operation.
2. Optimal matching is obtained by having symmetrical layout using the following layout techniques:
 - Locating devices as close to each other as possible
 - Same device size and orientation
 - Similar wiring, particularly for VPNP emitters
 - Similar nearest neighbor topology including wiring

4.4 General FET Design Discussion

The following table lists the available FETs in this technology.

<i>Table 4-5.FETs</i>				
Device Name (FET)	Model Name	Max ¹ V _{dd} [V]	Min L _{Des} [um]	T _{ox} [nm]
Regular NFET	nfet	1.6	0.12	2.2
Regular PFET	pfet	1.6	0.12	2.2
Thick NFET25 (Regular IO NFET)	dgnfet	2.7	0.24	5.2
Thick PFET25 (Regular IO PFET)	dgpfet	2.7	0.24	5.2
Thin Triple Well NFET	nfettw	1.6	0.12	2.2
Thick Triple well NFET	dgnfettw	2.7	0.24	5.2

1. For maximum voltage use, see Section 5.0 , “Reliability Design Rules and Models” on page 331 as well as Section 4.22 , “Mixed Voltage Interfaces” on page 325.

The following discussion applies to all FETs unless specified otherwise.

4.4.1 Isolation Oxide (STI) Design Specifications

The following specifications restrict the isolation oxide (STI) width, and the applied voltage under normal operating conditions, which may be used to ensure the acceptable leakage level of 1.0 pA/μm.

- Voltages greater than 6.0 V may not be used on PC lines which gate n(+) diffusions separated by thick oxide (isolation oxide) design widths of < 0.60 μm.
- Voltages up to 6.0 V may be used on metal lines with isolation widths down to 0.60 μm on n-channel structures.

P-channel PC gated structures may carry negative voltages (boot strapped below ground) with V_{ws} biases > 0.7 V and V_{gs} > -3.0 V.

4.4.2 Applied Voltage Limitations for FETs

4.4.2.1 Maximum Operating Voltage Due to Hot Electrons

A degradation in FET device characteristics occurs as a result of exposure to high drain to source bias over time. Hot electron effects will limit the practical burn-in voltages that may be used with 8HP, and are most severe at shorter channel length. Circuit designers should simulate the worst case circuits to ensure stability

during worst case power supply and minimum channel length applications. In order to avoid device degradation during product use conditions, the maximum potential difference allowed across source-drain during normal device operation is listed in Table 4-6.

<i>Table 4-6. Maximum Operating Voltage Due to Hot Electrons</i>	
Devices	maximum potential
Regular NFET and PFET	1.6 V
NFET25 and PFET25 (Regular IO N/P FET)	2.7 V

4.4.2.2 Trigger and Sustaining Voltage

Snap-back occurs at high drain-to-source bias with small L_{eff} . In snap-back, the device suddenly transfers from a stable operating point at a high drain-to-source bias with a low drain-to-source current to a lower drain-to-source bias at a high current. The higher bias is called the trigger voltage and the lower bias is called the sustaining voltage. A negative resistance region is encountered during the transition between these stable operating points. Operation in the snap-back region does not necessarily imply catastrophic failure. However, due to localized hot spots induced by silicided source and drain diffusions, even a small current flow could cause thermal failure of the NFET device. At very short channel lengths, the trigger voltage is approaching the sustaining voltage. Therefore, it is a good practice to limit the maximum voltage across a device to less than the sustaining voltage.

Table 4-7 lists the trigger voltage and sustaining voltage for FETs.

<i>Table 4-7. Trigger and Sustaining Voltage</i>		
Devices	Trigger Voltage	Sustaining Voltage
Regular NFET and PFET	< 6.0 V	> 3.5 V
NFET25 and PFET25	< 8.0 V	> 5.0 V

4.4.3 Gate Dielectric Thickness (T_{ox_qm} , T_{ox_inv})

The effective gate oxide thickness, T_{ox_inv} , is greater than the physical T_{ox_qm} of the FETs due to gate depletion effects. As a result the T_{ox_inv} is used in the electrical models:

For thin oxide devices,

$$T_{ox_inv} = 3.15 \pm 0.2 \text{ nm for NFETs, and } T_{ox_inv} = 3.30 \pm 0.2 \text{ nm for PFETs}$$

$$\text{where } T_{ox_qm} = 2.2 \pm 0.15 \text{ nm}$$

For the thick oxide devices,

$T_{ox_inv} = 5.9 \pm 0.4$ nm for NFETs, and $T_{ox_inv} = 6.15 \pm 0.4$ nm for PFETs

where $T_{ox_qm} = 5.2 \pm 0.4$ nm

The T_{ox_inv} is defined as $T_{ox_inv} = \kappa_{ox} * \epsilon_0 / C_{inv}$

where

- ϵ_0 is the vacuum permeability: $\epsilon_0 = 8.854 \times 10^{-14}$ F/cm.
- C_{inv} is the gate capacitance measured under the strong inversion condition.

4.4.4 Device Channel Length and Width

The device design length (L_{des}) is referred to PC design level. The device design width (W_{des}) is referred to RX design level. The effective channel length (defined as the poly gate length L_p) and channel width (W_{eff}) after processing are used in device design, performance projection and device modeling. They differ from L_{des} and W_{des} by ΔL and ΔW :

- $L_p = L_{des} - \Delta L$
- $W_{eff} = W_{des} - \Delta W$

The values of ΔL and ΔW for each device are given in Table 4-8. As an example, the effective channel length and width for minimum design length are width are listed in the table.

Table 4-8. Device ΔL and ΔW and Effective Channel Length and Width for minimum design

FET Name	ΔL [μ m] NOM	ΔW [μ m] NOM	Min L_{Des} [μ m]	Effective Min Channel length L_p [μ m]	Min W_{Des} [μ m]	Effective Min Channel Width W_{eff} [μ m]
Regular NFET	0.028	0.010	0.12	0.092	0.16	0.150
Regular PFET	0.028	0.040	0.12	0.092	0.16	0.120
NFET25 (Regular IO NFET)	0.020	0.000	0.24	0.220	0.36	0.360
PFET25 (Regular IO PFET)	0.020	-0.020	0.24	0.220	0.36	0.340

4.4.5 Channel Length Variation

4.4.5.1 Total Channel Length Variation (L_{tol})

The process variation in gate lithography, etch bias, lateral source/drain diffusion as well as mask compensation results in the channel length variation. The total channel length variation (L_{tol}) includes the chip mean variation (L_{chip}^{tol}).

4.4.5.2 Chip Mean Variation (L_{chip}^{tol})

The 3σ chip mean length variation (L_{chip}^{tol}) refers to the length variation between two identical devices (width, length, and orientation) on different chips. It includes chip to chip, wafer to wafer, and lot to lot variation. For example, for regular FET, L_{chip}^{tol} is $\pm 0.011 \mu m$.

4.4.6 Threshold Voltage

4.4.6.1 Threshold Voltage Definition

The threshold voltage V_G is defined as the gate to source bias, V_{gs} , at which

$$|I_{ds}| = 300 \text{ nA } W_{eff}/L_p \text{ for all NFETs}$$

$$|I_{ds}| = 70 \text{ nA } W_{eff}/L_p \text{ for all PFETs}$$

where $L_p = L_{design} - \Delta L(nom)$, and $W_{eff} = W_{design} - \Delta W(nom)$

4.4.6.2 Threshold Voltage Tolerance

The threshold voltage tolerance may be calculated for any given device by combining the base case tolerance with the tolerance expected from the short and narrow channel effects. The threshold tolerance, D_{vt} , is:

$$D_{vt} = \left\{ \left(\frac{9}{2} \right) \sigma^2 (\Delta V_t) + (D_{vtb})^2 + [V_t(L_{pnom}) - V_t(L_{pmin})]^2 + [V_t(W_{effnom}) - V_t(W_{effmin})]^2 \right\}^{1/2}$$

where

- D_{vtb} is the 3σ base case tolerance: $\pm 0.040 \text{ V}$ (additional end of life mismatch due to ionic V_t shift must be taken into account when calculating the total tracking).
- $\sigma(DV_t)$ is the 1-sigma threshold voltage tracking as defined in Section 4.4.7.3, "Device Current Matching for Separations Less than $200 \mu m$ " on page 252.
- The subscripts "nom" and "min" indicate the nominal and minimum device lengths and widths as defined in Section 4.4.4, "Device Channel Length and Width" on page 249.

4.4.6.3 Threshold Voltage Effect Near NW Edge

Devices located in close proximity to the NW edge (which defines the edge of Nwell and Pwell) will have an increased threshold voltage relative to devices remote from the edge (for a PFET, the threshold voltage becomes more negative). Minimum width NFET devices have a threshold voltage increase as much as 20±20 mV (per NW edge) large than nominal, and this effect is 3 to 5 times larger for thick oxide devices. Impact to certain digital circuit performance and functionality may occur (sense amplifiers, current mirrors,...). This effect has been included in the compact model. Please note the special rules regarding matching-critical analog considerations.

4.4.7 Tracking and Matching

4.4.7.1 Channel Length Tracking

Channel length tracking is the difference in channel length between two devices, $\delta L = L_1 - L_2$. If L_1 and L_2 each have standard deviation σ_L , then the standard deviation of the tracking is

$$\sigma_{\delta L} = \sqrt{\sigma_L^2 + \sigma_L^2} = \sqrt{2}\sigma_L.$$

For example, the 3-sigma localized variation of the channel length *offset* between two identical devices (same width, length, and orientation) is $\sqrt{2}(0.0085) \mu\text{m}$.

Table 4-9. Gate Length Variation for thin oxide FET (3 σ)		
Component	Linewidth Variation within 200 μm	Cross-Chip Variation (μm) ¹
(1) Site-to-Site Variation ²	± 0.005	± 0.0085
(2) Horizontal-Vertical variation ³	± 0.0045	
(3) Nested-to-isolated variation ⁴	± 0.0053	
(4) total across-chip variation (ACLV)	± 0.011	

1. Use these numbers for linewidths placed randomly over the entire chip area.
2. This is the variation of an identical line placed randomly across the chip. Identical means same line width, same line space along with the same local environment (both PC and RX).
3. This is the variation in line width between two otherwise identical lines except for the orientation. Identical means same line width, same line space along with the same local environment (both PC and RX).
4. This is the variation in line width between lines with the same orientation, same line width but different local environment (e.g. line space, pitch or density).

Table 4-10. Gate Length Variation for thick oxide FETs (3σ)

Component	Cross-Chip Variation (μm)
(1) Site-to-Site Variation ¹	± 0.0120
(2) Horizontal-Vertical variation ²	± 0.0065
(3) Nested-to-isolated variation ³	± 0.0077

1. This is the variation of an identical line placed randomly across the chip. Identical means same line width, same line space along with the same local environment (both PC and RX).
2. This is the variation in line width between two otherwise identical lines except for the orientation. Identical means same line width, same line space along with the same local environment (both PC and RX).
3. This is the variation in line width between lines with the same orientation, same line width but different local environment (e.g. line space, pitch or density).

Note that the gate length variation numbers specified above assume that the PC density requirements as described in Section 2.9 , “Important Design Guidelines” on page 59 are satisfied.

4.4.7.2 Circuit-Path Mean Variation

The 3σ cross-chip variation of one circuit-path mean L_p to another circuit-path mean L_p is $\pm 0.0085 \mu\text{m}$ (this is useful for evaluating circuit-path matching within a chip, and is only true for circuits with similar width/space/orientation topography).

4.4.7.3 Device Current Matching for Separations Less than 200 μm

For identical devices, with the same orientation, separated by less than 200 μm , the mismatch in device current at final wafer test has been characterized using the following model:

$$I = 0.5 * K * (V_{GS} - V_T)^2,$$

Adjacent FET device mismatch is modeled as a combination of threshold voltage mismatch and beta (mobility) mismatch terms that vary in proportion to $1/(\sqrt{WL})$

$$\sigma\left(\frac{\Delta I_{ds}}{I_{ds}}\right) = \sqrt{\sigma^2\left(\frac{\Delta\beta}{\beta}\right) + \sigma^2\left(\frac{2\Delta V_T}{(V_{GS} - V_T)}\right)}$$

where

$$\Delta\text{mobility} = \Delta\beta = \frac{K_\beta}{\sqrt{(W - K_{\beta W})NF(L - K_{\beta L})}}$$

and

$$\Delta V_T = \frac{K_V}{\sqrt{(W - K_{VTW})NF(L - K_{VTL})}}$$

Table 4-11. Threshold Voltage and Mobility Mismatch equation coefficients

Device type	K_β	$K_{\beta W}$	$K_{\beta L}$	K_{VT}	K_{VTW}	K_{VTL}
NFET/NFETTW	2.1E-9	-6.0E-8	-1.7E-7	1.21E-8	0.4E-8	-5.0E-8
PFET	2.7E-10	4.0E-8	-1.5E-7	9.9E-9	-8.1E-8	5.0E-8
NFET25/NFET25T W	1.0E-9	0	-5.0E-7	1.05E-8	1.4E-7	1.3E-7
PFET25	7.5E-10	-1.0E-6	-8.5E-7	1.0E-8	-3.6E-7	0.8E-7

Note: The V_t mismatch relationship described above predicts that the mismatch observed on short channel devices can be improved by using wide multi-finger devices. This has not been verified in hardware.

Note: Units for L and W are meters in Δ mobility and ΔV_T function calculations above.

4.4.7.4 Isolation Proximity Effect on FETs

The FETs current depends on the distance from the active gate region to the isolation edge. The effect of the isolation edge (RX) perpendicular to the gate polysilicon(PC) is accounted for as a portion of the narrow width effect. However, the proximity effect of the isolation edge parallel to the gate polysilicon must be separately considered and can be empirically modeled by the modification of the mobility.

The isolation proximity effect on FETs diminishes as the distance of the PC-RX increases. When the PC-RX distance on either side of a polysilicon gate is less than 1 μ m, the NFET current is degraded and the PFET current is enhanced.

The net current enhancement or degradation for a device with non-symmetric source and drain (where the PC-RX distance is different for the source and drain) is always less than a symmetric ground rule minimum device.

4.4.8 Guidelines for Device Matching

Metal Antenna

Keep the metal antenna ratio to a minimum, preferably tying the gates to diodes at M1. If metal antennae do occur at M1, make the ratio small, equal for the devices to be matched, and tie the gates to diffusions at M2,

Wiring Over Gates

Metal wiring over gates for each metal level should cover the same percentage of the device active area (PC over RX) on matching devices.

Well Proximity

The NW mask edge should be at least 3 μm from the active area (PC over RX) of devices to be matched if the V_t matching is required to be within limits. At closer spacings, the V_t associated with that active device is raised by an amount that increases with reduction in the space.

If a 3 μm spacing is impossible to achieve, identical layouts must be used. The layout must be identical with respect to placement of the Nwell relative to the source and drain nodes of the device, and the absolute value of the threshold will be modified by the presence of mask edge. Mirror image layouts are subject to V_t mismatch induced by well misalignment which can be 20mV or larger depending on well misalignment and device type. Such asymmetric layouts must be reviewed by your IBM technical representative prior to use.

RX Width Consideration

For precise current ratioing always use different numbers of identically designed fingers and do not expect that the ratio of the current in a wide or long device to that of a short or narrow device is precisely represented by the model. When using multiple fingers designed in a common active area rectangle, the carrier mobility in the outermost fingers, adjacent to a parallel RX (active area) edge, will not match the inner fingers due to stress propagated from the RX edge to the adjacent device region. It is advisable to use dummy fingers on the outside of the RX edge to ensure that the inner fingers all match.

4.4.9 RF Performance¹

4.4.9.1 Maximum Oscillation Frequency (f_{max})

The maximum oscillation frequency is defined as the frequency where the maximum available gain (MAG) equals 1. The MAG itself is defined as the maximum power amplification of a FET which is achieved by impedance matching of the input port and the output port under stable transistor operating condition (stability factor $k \geq 1$). The MAG is calculated from the S-parameters as

$$MAG = \left| \frac{S_{21}}{S_{12}} (k - \sqrt{k^2 - 1}) \right|$$

where the stability factor k is defined as

$$k = \frac{1 + |S_{11}S_{22} - S_{12}S_{21}|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{12}S_{21}|}$$

1. The information in this section is pending on data.

If the impedance matched device is not stable ($k < 1$) the gain is calculated under nonideal impedance matching but stable operating conditions (MSG, maximum stable gain). The value of f_{max} is extracted by extrapolating the MAG value (which slope is typically about -20dB/dec) to the frequency where MAG becomes 1.

4.4.9.2 Minimum Noise Figure (NF_{min})

The noise figure NF of a two port is defined as the ratio of the signal (S) to noise (N) power ratio at the input, to the signal to noise power ratio at the output.

$$NF = 10 \log \frac{S_i / N_i}{S_o / N_o}$$

The noise figure depends on the source admittance at the input (Y_s), on the noise resistance (R_n) of the two port and on the optimum source admittance (Y_{opt})

$$NF = NF_{min} + \frac{R_n}{\Re(Y_s)} |Y_s - Y_{opt}|^2$$

For $Y_s = Y_{opt}$ the noise figure of the two port reaches its minimum value NF_{min} :

$$NF = NF_{min} \Big|_{Y_s = Y_{opt}}$$

4.4.9.3 Electrical Parameters F_t , F_{max} , and NF_{min}

The electrical parameters for the FETs are under evaluation and will be updated once the information become available.

4.5 Electrical Parameters of FETs

4.5.1 Explanation of the electrical parameters

Isx - substrate current

Avalanche multiplication increases the channel current at high drain to source bias in the saturation region of operation. Holes and electrons, generated by impact ionization, flow to the substrate or well and drain. This current can be substantial and may predominate the well and substrate current at room temperatures. The substrate current Isx listed in the tables are measured under an estimated worst case bias condition.

Ij - drain/source reversed biased junction leakage

The junction leakage of the FETs is a concern for low power applications. The drain/source reversed biased junction leakage is a function of both voltage and temperature. The circuit models do not predict the leakage accurately. The numbers listed in the tables are based on the measurement data and may be used for estimation of power consumption.

GIDL - gate induced drain leakage

Additional diffusion-to-well current is caused by gate induced drain leakage (GIDL). GIDL occurs as the result of high electric fields at the diffusion edge under thin oxide when the device is in an off-state. The Ioff current listed in the device parameter tables do not include the GIDL. For this technology, GIDL is the range of pA/um and is only a concern for the low power applications where the Ioff is low and the contribution of GIDL leakage becomes significant. The low power FETs' GIDL information will be updated once the data is available.

Gate Oxide Leakage

For this technology, the gate oxide leakage for thin oxide is in the range of pA/um and is a concern for low power applications where the Ioff is low and the contribution of the gate oxide leakage becomes significant.

4.5.2 Regular NFET and PFET

Table 4-12.Regular FET Electrical Parameter Specifications ¹					
Parameter	Definition	Unit	W _{Des} /L _{Des}	NFET	PFET
ΔL		μm		0.028 $\pm 0.011^2$ $\pm 0.022^3$	0.028 $\pm 0.011^2$ $\pm 0.022^3$
ΔW		μm		0.01 $\pm 0.044^2$ $\pm 0.084^3$	0.04 $\pm 0.044^2$ $\pm 0.084^3$
Effective T _{ox}		nm		3.03 ± 0.2	3.23 ± 0.2
Physical T _{ox}		nm		2.2 ± 0.15	2.2 ± 0.15
Gate Oxide leakage (I _g)		pA/um ²	5x5 (x 42)	20 (WC 80) ⁴	1 (WC 4) ⁴
Gate Oxide Breakdown Voltage	I _G <10 uA/um ²	V		> 4.5	> 4.5
V _{thlin}	V _D =0.05, V _B =0	V	5/5	0.17 \pm 0.045	-0.225 \pm 0.045
V _{tsat}	V _D =1.2V, V _B =0V	V	5/0.12	0.355 \pm 0.050	-0.325 \pm 0.050

Table 4-12.Regular FET Electrical Parameter Specifications ¹

Parameter	Definition	Unit	W _{Des} /L _{Des}	NFET	PFET
V _{tsat}	V _D =1.5V, V _B =0V	V	5/0.12	0.340 ± 0.055	-0.310 ± 0.055
V _{tsat}	V _D =1.2V, V _B =0V	V	0.16/0.12	0.295 ± 0.080	-0.355± 0.080
DIBL	V _B =0V, V _{tsat} -V _{tlin}	mV	5/0.12	73 +50/-30	76 ± 40
Body Effect	V _D =1.2V, V _t -shift V _B =0 ...-1V	V	5/0.12	0.165 ± 0.040	0.192 ± 0.040
Sub V _t Slope	V _D =1.2V, V _B =0V	mV/dec	5/0.12	82 +8 / -8	83 +8 / -8
I _{dlin}	V _D =0.05 V, V _G =1.2 V, V _B =0V	μA/μm	5/5	4.00 +/-0.60	0.68 +/-0.10
I _{on}	V _D =V _G =1.2V, V _B =0V	μA/μm	5/0.12	530 ± 85	190 ± 45
I _{on}	V _D =V _G =1.5V, V _B =0V	μA/μm	5/0.12	770 +/- 120	315 +/- 70
I _{on}	V _D =V _G =1.2V, V _B =0V	μA	0.16/0.12	86 +/- 35	23 +15/-12
G _m	V _D =V _G =1.2V, V _B =0V	μS/um	5/0.12	750 +/- 70	340 +/- 50
I _{off}	V _D =1.2V, V _G =V _B =0V	nA/μm	5/L _{min}	<2	<2.5
I _{off}	V _D =1.2V, V _G =V _B =0V	pA/μm	5/0.12	300(<1140)	250(<900)
I _{off}	V _D =1.5V, V _G =V _B =0V	pA/μm	5/0.12	450(<1820)	370(<1470)
I _{off}	V _D =1.2V, V _G =V _B =0 V	pA	0.16/0.12	400(<1200)	30(<100)
I _{off}	V _D =1.2V, V _G =V _B =0V, T=85C	nA/μm	5/L _{min}	<24	<14
I _{off}	V _D =1.2V, V _G =V _B =0V, T=85C	nA/μm	5/0.12	5(<21)	4.5(<20.5)

Table 4-12.Regular FET Electrical Parameter Specifications ¹

Parameter	Definition	Unit	W_{Des}/L_{Des}	NFET	PFET
$V_{leakage}$	$V_G=V_B=0V$, $I_D=1\text{ nA}/\mu\text{m}$	V	5/0.12	2.4	-2.5
$V_{breakdown}$	$V_G=V_B=0V$, $I_D=1\mu\text{A}/\mu\text{m}$	V	5/0.12	4.3	-4.7
I_{sx}	$V_G=0.7V$ $V_D=1.6V$	nA/ μm	5/0.12	30 + 30 / -20	0.4 +0.6 / -0.3
$C_{j\text{ area}}$	$V_j=0V$	fF/ μm^2		1.05 ± 0.2	1.05 ± 0.2
C_{overl}	$V_G=0.0V$	fF/ μm	-/0.12	0.35 ± 0.045	0.29 ± 0.045
C_{gon}	$V_G=1.2V$	fF/ μm	-/0.12	1.30 ± 0.25	1.26 ± 0.25
I_j	$V_j=1.2\text{ V}$, T=25 C	fA/ μm^2		< 600 (typical 125)	<1 (typical 0.5)
I_j	$V_j=1.6\text{ V}$, T=25 C	fA/ μm^2		< 2000 (typical 750)	<5 (typical 1)
I_j	$V_j=1.2\text{ V}$, T=85 C	fA/ μm^2		<800	<5
$V_{j\text{ breakdown}}$ (avalanche)		V		> 10	> 10
RO Delay Time ⁵	$V_{DD}=1.2V$	psec	4/0.12	18.5 ± 4.5	

1. All tolerance are 3σ
2. ACLV or ACWV
3. Total tolerance
4. WC means 3 sigma Worst Case (thinnest oxide). Leakage per gate length can be calculated by $I_g \times L_p$
5. This number depends on the exact details of the layout. This example is for $W_n=4\mu\text{m}$, $W_p=7\mu\text{m}$ and minimum CA/M1 to PC capacitances.

4.5.3 Thin Triple Well NFET

See NFET information in Section 4.5.2 , “Regular NFET and PFET” on page 256

4.5.4 NFET25 and PFET 25 (Regular IO NFET and PFET)

Table 4-13.NFET25 and PFET 25 (Regular IO FET) Electrical Parameter Specifications

Parameter	Definition	Unit	W_{Des}/L_{Des}	NFET	PFET
ΔL		μm		0.028 $\pm 0.016^1$ $\pm 0.032^2$	0.028 $\pm 0.016^1$ $\pm 0.032^2$
ΔW		μm		0.000 $\pm 0.030^1$ $\pm 0.065^2$	-0.020 $\pm 0.030^1$ $\pm 0.065^2$
Effective T_{ox}		nm		5.9 ± 0.4	6.15 ± 0.4
Physical T_{ox}		nm		5.2 ± 0.4	5.2 ± 0.4
Gate Oxide Breakdown Voltage	$I_G < 10 \mu A/\mu m^2$	V		> 8.5	> 8.5
V_{tlin}^3	$V_D=0.5V, V_B=0V$	V	5/5	0.465 ± 0.060	-0.445 ± 0.055
V_{tsat}^3	$V_D=2.5V, V_B=0V$	V	5/0.24	0.410 $+0.075/-0.095$	-0.440 $-0.075/+0.095$
Body Effect 3	$V_D=0.05V,$ V_t -shift $V_B=0 \dots 1V$	V	5/0.24	0.110 ± 0.040	0.250 ± 0.040
Sub V_t Slope	$V_D=2.5V, V_B=0V$	mV/dec	5/0.24	80 ± 8	85 ± 8
I_{on}	$V_D=V_G=2.5V,$ $V_B=0V$	$\mu A/\mu m$	5/0.24	660 ± 100	$260 +75/-50$
I_{off}	$V_D=2.5V,$ $V_G=V_B=0V$	$pA/\mu m$	5/ L_{min}	150	20
I_{off}	$V_D=2.5V,$ $V_G=V_B=0V$	$pA/\mu m$	5/0.24	10 (<260)	10 (< 60)
I_{off}	$V_D=2.5V,$ $V_G=V_B=0V,$ $T=85C$	$nA/\mu m$	5/ L_{min}	< 3	< 0.2
I_{off}	$V_D=2.5V,$ $V_G=V_B=0V, T=85C$	$nA/\mu m$	5/0.24	<1	<0.1
Early Voltage	$V_{ds}=1.25, (V_{gs}-V_t)$ $=0.3V$	V	5/0.24	18	23

Table 4-13.NFET25 and PFET 25 (Regular IO FET) Electrical Parameter Specifications

Parameter	Definition	Unit	W_{Des}/L_{Des}	NFET	PFET
Gmsat	$V_{GS}=V_{DS}=2.5V$	$\mu S/\mu m$	5/0.24	330 ± 50	170 ± 20
$V_{leakage}$	$V_G=V_B=0V$, $I_D=0.1 \text{ nA}/\mu m$	V	5/0.24	>4.0	>4
$V_{breakdown}$	$V_G=V_B=0V$, $I_D=1 \mu A/\mu m$	V	5/0.24	>6.0	$> - 6.0$
R_{ext}		$\Omega \mu m$		225 ± 30	450 ± 30
$I_{sx} \text{ (Max)}$	$V_G=1.35$ $V_D=2.70$	$\mu A/\mu m$	5/0.24	1.1 $+0.4/-0.2$	0.02 $+0.02/-0.015$
$C_{j \text{ area}}^4$	$V_j=0V$	$fF/\mu m^2$		1.0 ± 0.2	1.0 ± 0.2
C_{overl}		$fF/\mu m$		0.315 ± 0.045	0.300 ± 0.045
I_j^5	$V_j=2.5V$	$fA/\mu m^2$		< 200	< 1
I_j^5	$V_j=2.5V, T=85C$	$fA/\mu m^2$		< 400	< 5
$V_j \text{ breakdown}$ (Avalanche)		V		> 10	>10

1. ACLV or ACWV
2. Total tolerance
3. The Threshold Voltage is defined as the gate to source bias at which
 $|I_D| = 300nA W_{eff}/L_{eff}$ for NFET
 $|I_D| = 70nA W_{eff}/L_{eff}$ for PFET
4. Junction capacitance
5. Junction leakage

4.5.5 Thick Triple Well NFET

See NFET information in Section 4.5.4 , “NFET25 and PFET 25 (Regular IO NFET and PFET)” on page 258

4.6 Junction Diodes

4.6.1 STI-Bounded Breakdown

<i>Table 4-14.Reverse-Bias Breakdown Voltage (V), $I_L = 1\mu A$, Area = $100 \times 100\mu m^2$</i>			
Device	P+ / N-Well	N+ / P-Well	N-Well / Substrate
Regular V_t	> 5.5	> 7	> 10
Thick Oxide	> 7	> 7	> 10

<i>Table 4-15.intra-well punch through voltage (V), $I_L = 1nA/\mu m$</i>		
Diffusion Space	n+ / n+	p+ / p+
0.18 μm	> 4	> 7
0.36 μm	> 4	> 7

4.6.2 Junction Capacitance

The junction area capacitances at zero bias have been listed in the electrical parameter tables for each type of FETs. The following table includes the STI bounded and PC bounded perimeter components.

<i>Table 4-16.Junction Capacitances</i>					
Structure	Regular V_t device		Thick Oxide device		N-Well
	N+ diffusion	P+ diffusion	N+ diffusion	P+ diffusion	
CjA - Area component (fF/ μm^2)	1.05	1.05	1.00	1.00	0.25 ¹ 1.00 ²
Cjsw - Perimeter component, STI bordered (fF/ μm)	0.001	0.004	0.03	0.05	0.75
Cjswg - Perimeter component, [poly bordered (fF/ μm)	0.488	0.438	0.17	0.28	-

1. for regions under ESDIODE and PI
2. for all other regions

Capacitances of N⁺, P⁺, and N-well diffusions are a function of bias and temperature. The junction area and perimeter components of capacitance are given by:

Area component: Vbx is the source or drain diffusion to substrate/well bias (Vbx <0 for reverse bias).

$$C_{jA}(V) = C_{jA}(T) \times \left(1 - \frac{V_{bx}}{PB - TPB \times (T - T_{ref})} \right)^{-MJ}$$

STI bordered perimeter component: ($V_{bx} < 0$)

$$C_{jsw}(V) = C_{jsw}(T) \times \left(1 - \frac{V_{bx}}{P_{BSW} - TP_{BSW} \times (T - T_{ref})} \right)^{-M_{JSW}}$$

Poly bordered perimeter component: ($V_{bx} < 0$)

$$C_{jswg}(V) = C_{jswg}(T) \times \left(1 - \frac{V_{bx}}{P_{BSWG} - TP_{BSWG} \times (T - T_{ref})} \right)^{-M_{JSWG}}$$

where T= Temperature in °C , Tref=25°C and

$$C_{jA}(T) = C_{jA}(1 + T_{cj} \times (T - T_{ref}))$$

$$C_{jsw}(T) = C_{jsw}(1 + T_{cjsw} \times (T - T_{ref}))$$

$$C_{jswg}(T) = C_{jswg}(1 + T_{cjswg} \times (T - T_{ref}))$$

When modeling junction capacitance, the substrate/N-well resistance from the bottom of the junction to the substrate/N-well contact should be included. The junction capacitance is given by:

$$C_j(V) = C_{jAt}(V) + C_{jswt}(V) + C_{jswgt}(V)$$

The following two *examples* illustrate how to calculate the area and perimeter terms:

1. Rectangular diffusion bounded on all four sides by STI (shallow trench isolation)

$$C_{jAt}(V) = C_{jA}(V) \times ((Length + 2b) \times (Width + 2b))$$

$$C_{jswt}(V) = 2C_{jsw}(V) \{ (Length + 2b) + (Width + 2b) \}$$

2. Rectangular diffusion bounded by an FET gate at the long end and STI on the other three sides

$$C_{jswgt}(V) = C_{jswg}(V) \times (Width + 2b)$$

$$C_{jAt}(V) = C_{jA}(V) \times ((Length + b + a) \times (Width + 2b))$$

$$C_{jswt}(V) = C_{jsw}(V)(Width + 2b) + 2C_{jsw}(T)(Length + b + a)$$

where

Length = design length (STI to PC dimension if a FET), μm

Width = design width (STI to STI dimension), μm

a = the bias per edge (E8) listed in Table 4-39, "Extraction Parameters for Diffusion," on page 291.

b = the bias per edge (E8) listed in Table 4-39, "Extraction Parameters for Diffusion," on page 291.

4.6.3 Forward-Biased Diodes

The general use of forward-biased diodes as circuit elements is not supported. Additionally, the application referred to as a bandgap reference circuit using a p-diffusion in a grounded (tied to substrate) n-well as a diode, is not offered in the BiCMOS8HP technology (see "List of devices or features that are not supported in the BiCMOS8HP technology:" on page 11.). For additional details, contact your IBM Technical Representative.

4.7 Resistor Models

The BiCMOS-8HP technology currently provides four types of resistors: OP P+ polysilicon resistors, RR polysilicon resistors, NS diffusion resistors, and a KQ BEOL resistor. The OP resistor is made by blocking salicidation of P+ polysilicon (without HALO/extension) using the OP masking level. The length of the OP mask determines the length of the OP P+ and RR resistors (regions not covered by OP are silicided) and the VY to VY spacing determines the length of the KQ resistor. The NS resistor is made of the NS subcollector, with silicided Reach-thru diffusions at each end for contacting the resistor. The reach-thrus determine the length of the NS resistor. Supported resistor geometries include squares and rectangles. Other irregular shapes, such as dog bones or L-shapes, are not supported. The polysilicon resistors can be placed entirely over SX or NS. The polysilicon resistors, as modeled, cannot be placed over thin oxide (RX). The polysilicon resistor model does not support resistors placed over deep trench and does not incorporate the substrate capacitance reduction when the resistor is placed over a deep trench lattice. See also the effect of deep trench lattice structures on resistance in section 4.7.6, “Resistor Tolerance” on page 271.

4.7.1 Resistor Specifications

The following specifications may be used as a guide in applications for the resistors.

<i>Table 4-17. Resistor Design Specifications</i>				
Specification	NS Diffusion	P+Poly	RR poly	KQ BEOL
Rs¹ (Ω/sq) (0V, 25 °C)	8.8 ± 1.32	340 ± 51	1700 ± 340	60.5 ± 4.8
Rend² ($\Omega\text{-}\mu\text{m}$)	24.0 ± 20	23.5 ± 16	23.5 ± 16	28 ± 10
L (μm)	RX - RX	OP length	OP length	VY - VY
W (μm)	DT width	Poly width	Poly width	KQ width
ΔL_R (μm)	0 ± 0.048	0 ± 0.1	0 ± 0.1	0 ± 0.05
ΔW_R (μm)	-0.277 ± 0.3	-0.04 ± 0.1	-0.071 ± 0.1	0.3 ± 0.14
Rs TCR (ppm per °C)	tc1 = 1586 tc2 = 1	tc1 = 66 tc2 = 0.57	tc1 = -1079 tc2 = 2.15	tc1 = -399 tc2 = 0.72
Rend TCR (ppm per °C)	tc1 = 99 tc2 = 0.48	tc1 = -3728	tc1 = -3728	n/a
VCR (% per Volt)	154	0	0	0
Current Limit³ (mA/μm)	< 1.0	See section 5.3.7.1, “Front-End of Line Resistors” on page 353	< 0.1	See section 5.3.7.2, “Back-End-Of-Line KQ Resistors” on page 355
Parasitic capacitance C_{A0} (fF/μm^2) C_{P0} (fF/μm)	0.1 0.1	0.0965 0.0097	0.0965 0.0097	0.01 0.037

1. Sheet resistance: $R_s \pm 3\sigma$ tolerance
2. R_{end} is the end-resistance. In OP resistor model: $R_{end} \pm TR_{end}$, where CA to OP edge spacing is given by ground rule 733, and the CA to CA space is given by ground rule 203. If another layout is used, adjustment to the end resistance will be required based on the dimensions adopted and the CA and silicide specific resistances.
3. OP resistor current level is limited by heating.

4.7.2 Resistor Design

There are three design equations for the different resistors. The resistor models assume minimum groundrule spacings for the placement of the contacts consistent with the layout rules contained in the resistor pcells. Example layout diagrams are shown, along with the nominal resistance calculations.

For the P^+ (opppcres) polysilicon resistor, the nominal value resistance equation at 25 °C and 0 volts is:

$$R_{nom} = \left(R_s \cdot \frac{L}{W} \right) + \left(2 \cdot \frac{R_{end}}{W} \right) \quad \Omega$$

where:

R_s = Sheet Resistance in Ω/\square

R_{end} = End Resistance in $\Omega\text{-}\mu\text{m}$

$L = L_{OP}$ μm

$W = W_D + dw$ μm

L_{OP} = Design Length (OP length) in μm

W_D = Design Width (RX or PC width) in μm

Values for the parameters in the above equations are given in Table 4-18.

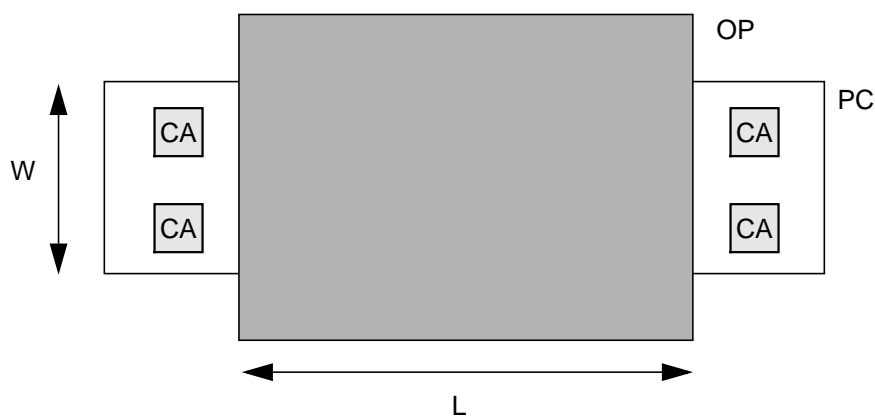


Figure 4-1. Example layout for the P^+ Polysilicon and RP Polysilicon resistor types: opppcres and oprppres

For the RR polysilicon resistor (oprppres) the nominal value resistance equation at 25 °C and 0 volts is:

$$R_{nom} = \left(R_s \cdot \frac{L - (2 \cdot Lbn)}{W} \right) + \left(2 \cdot \frac{Rbn \cdot Lbn}{W} \right) + \left(2 \cdot \frac{R_{end}}{W} \right) \quad \Omega$$

where:

R_s = Sheet Resistance in Ω/\square
 R_{end} = End Resistance in $\Omega\text{-}\mu\text{m}$
 $L = L_{OP}$ μm
 $W = W_D + dw$ μm

R_{bn} = P+ Poly Sheet Resistance in Ω/\square
 L_{bn} = BN overlap OP Length in μm
 L_{OP} = Design Length (OP length) in μm
 W_D = Design Width (PC width) in μm

Values for the parameters in the above equations are given in Table 4-18.

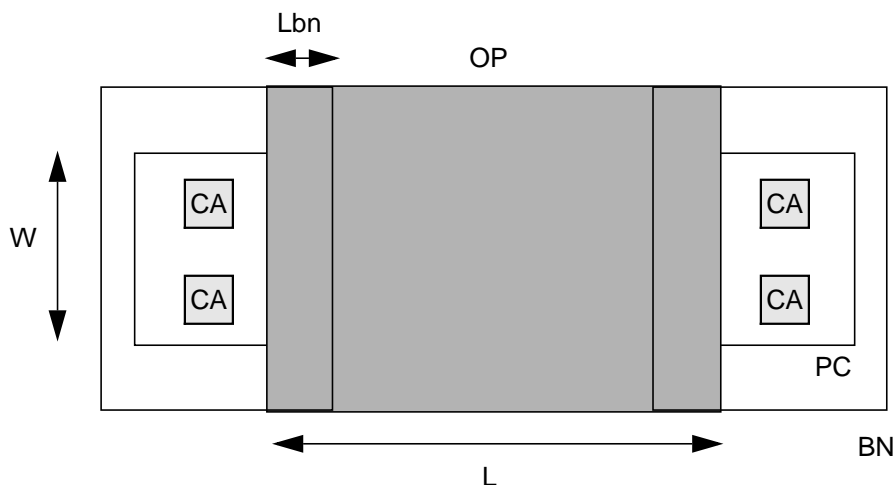


Figure 4-2. Example layout for RR Polysilicon resistor type: oprpres

For the KQ (kqres) resistor, the nominal value resistance equation at 25 °C and 0 volts is:

$$R_{nom} = \left(R_s \cdot \frac{L}{W} \right) + \left(2 \cdot \frac{R_{end}}{W} \right) \quad \Omega$$

where:

R_s = Sheet Resistance in Ω/\square
 R_{end} = End Resistance in $\Omega\text{-}\mu\text{m}$
 $L = L_{RAV}$ μm
 $W = W_D + dw$ μm

L_{RAV} = Design Length (VYbar to VYbar length) in μm
 W_D = Design Width (KQ width) in μm

Values for the parameters in the above equations are given in Table 4-18.



Figure 4-3. Example layout for BEOL KQ resistor type: kqres

For the NS (nsres) resistor, the nominal value resistance equation at 25 °C and 0 volts is:

$$R_{nom} = \left(R_s \cdot \frac{L}{W} \right) + \left(2 \cdot \frac{R_{end}}{W - 0.24} \right) \quad \Omega$$

where:

R_s = Sheet Resistance in Ω/\square

R_{end} = End Resistance in $\Omega\text{-}\mu\text{m}$

$L = L_{RX-RX} \mu\text{m}$

$W = W_{DT} + dw \mu\text{m}$

L_{OP} = Design Length (RX-RX spacinglength) in μm

W_{DT} = Design Width (inner DT width) in μm

Values for the parameters in the above equations are given in Table 4-18.

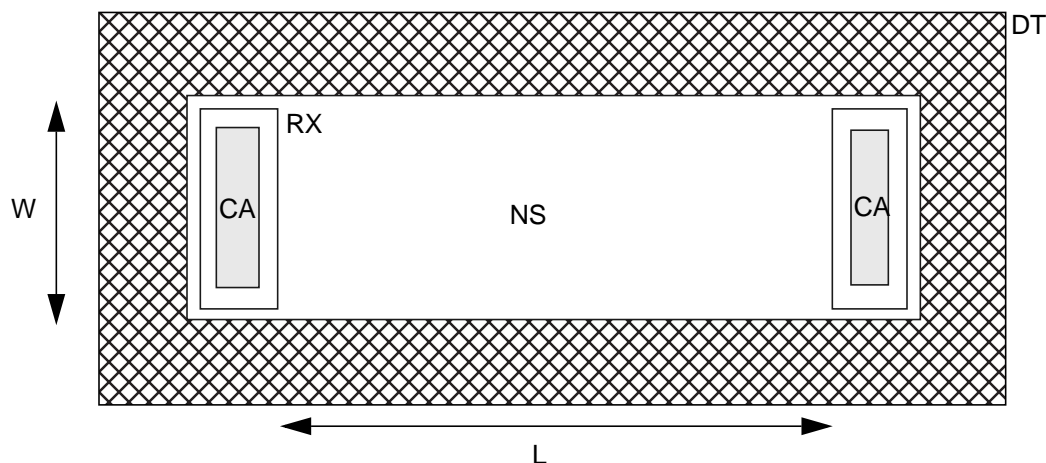


Figure 4-4. Example layout for the NS Resistor: nsres. ⁴

Table 4-18. Resistor Model Parameters				
Resistivity Parameters	opppcres Resistor	oprrpres Resistor	kqres Resistor	nsres Resistor
R_s (Ω/\square)	340	1700	60.5	8.8
R_{end} ($\Omega\text{-}\mu\text{m}$)	23.51	23.51	28	24
R_{bn} (Ω/\square)	n/a ¹	340	n/a ¹	n/a ¹
Shape Bias				
dw (μm)	-0.04	-0.071	0.3	-0.277
Lbn (μm)	n/a ¹	0.46	n/a ¹	n/a ¹
Note: 1. An unsilicided P+ (BN) region has an affect only in the RR polysilicon resistor				

4.7.3 Resistor Geometry

The minimum allowable drawn dimensions are shown in Table 4-19. It is highly recommended that resistors be made larger than minimum lengths and widths to improve both tolerance and matching (see the OP layout rules for the recommended minimum dimensions). Note that the minimum width values are not determined from the layout rules for OP over RX (or PC), which would result in smaller values for the minimum resistor widths. Rather, the minimum width values in Table 4-19 are obtained from the layout rules regarding the dimensions of CA and the minimum CA to RX (or PC) edge distance. Since dog-bone shapes are not supported, the larger values are used to specify the minimum widths allowed for the resistors.

Table 4-19. Minimum Groundrule Resistor Layout Dimensions				
Layout Dimension	NS Diffusion	P+Poly	RR poly	KQ BEOL
Width (μm)	2.00	0.20	0.74	5.92
Length (μm)	2.60	1.60	1.10	5.0

Design Layout Reminder

Strict adherence to the groundrules and layout details provided in the device set is recommended to ensure full and consistent device model and design tool compatibility and accuracy. Should you require modeling support for geometries other than those described here, please contact your IBM Product Engineers.

4.7.4 Temperature and Self-Heating Effects

The resistivity (R_s) and end resistance (R_{end}) of each of the various types of resistors varies with temperature. This temperature variation is handled through the standard HSpice or spectre resistor model equations. The temperature coefficients for R_s and R_{end} are given in Table 4-18 on page 269.

In addition, the RR polysilicon (oprrpres) resistor is observed to have a self-heating effect at high current levels, those approaching the limits specified in Table 4-18. The self-heating is expressed in terms of the resistivity possessing a voltage dependence that varies as the square of the voltage across the resistor. Including the geometrical scaling, the resistance variation due to self-heating is given by the equation

$$R = R_{nom} \times \left(1 + \left(\frac{-136}{A \cdot R_{nom}} \cdot A^{0.2} \cdot V^2 \right) \right)$$

where:

$A = L_{OP} \cdot W_D$, L_{OP} (μm) and W_D (μm) being the drawn OP length and PC width, respectively.

There is also a self-heating effect for the KQ BEOL resistor (kqres) at high current levels. The self-heating is also expressed in terms of the resistivity possessing a voltage dependence that varies as the square of the voltage across the resistor. Including geometrical scaling, the resistance variation due to self-heating is given by the equation:

$$R = R_{nom} \times \left(1 + \left(\frac{-126}{A \cdot R_{nom}} \cdot A^{0.241} \cdot V^2 \right) \right)$$

where $A = L_{RAV} \cdot W_D$, W_D and L_{RAV} being the design width and length in μm , and V is applied voltage.

4.7.5 Voltage Coefficient of Resistance

As the voltage across the junction isolating a diffusion resistor from either N-well or substrate changes, the resistance of the resistor changes by a small amount. The voltage dependence for the resistors is calculated as a linear function of the resistor to N-well or substrate reverse bias. The voltage (V_{avg}) is an average of the voltage difference between the resistor and the N-well or substrate. Note that the N^+ (P^+) S/D must always be positive-biased (negative-biased) relative to the substrate (N-well), in order not to forward bias the junction between the N^+ (P^+) resistor and the substrate (N-well). The equations calculate the percentage change factor used by the model to adjust the 0V resistance value according to the applied voltage bias. The voltage coefficients for the various resistors are listed in the following table.

Specification	nsres Resistor	oppccres Resistor	oprrpres Resistor	kqres Resistor
AVCR (% per V)	154	0	0	0

The effect of bias voltage on resistance for the NS diffusion and the polysilicon resistors is given by the equation:

$$VCR_X = (1.0 + (AVCR \cdot 10^{-2} \times |V_{avg}|))$$

4.7.6 Resistor Tolerance

The resistor tolerance is defined based on measured variation of both geometric process parameters and sheet resistivities. In most cases, the dominant variation of resistance is due to only a few of the process parameters defining a resistor's value.

The models define statistical distributions for each resistance equation parameter in Table 4-20.

Table 4-20. Resistor Tolerance Parameters				
Tolerance Parameter	nsres Resistor	opp cres Resistor	oprrpres Resistor	kqres Resistor
$T_{rs} (\Omega/\square)$	20.0	51.0	340	4.8
$T_{rend} (\Omega\cdot\mu m)$	16.0	16.0	16.0	10.0
$T_{lop} (\mu m)$	0.10	0.10	0.105	0.5
$T_w (\mu m)$	0.06	0.02	0.02	0.14
$T_{lbn} (\mu m)$	n/a ¹	n/a ¹	0.17 ¹	0.11
Note: Tolerance values represent 3-sigma process capability. 1. An unsilicided P+ (BN) region has an affect only in the RR polysilicon resistor. 2. The length tolerance for KQ resistor is based on VY tolerance and is independent of OP tolerances				

The 3-sigma tolerance for the NS diffusion, P⁺ polysilicon and KQ BEOL resistors can be estimated by:

$$T = \sqrt{\frac{(Trs \cdot L)^2}{W^2} + \frac{(Tlop \cdot Rs)^2}{W^2} + \frac{(2 \cdot Trend)^2}{W^2} + \frac{(Tw \cdot R_{nom})^2}{W^2}}$$

The 3-sigma tolerance for the RR polysilicon resistor can be estimated by:

$$T = \sqrt{\frac{(Trs \cdot (L - 2Lbn))^2}{W^2} + \frac{(Tlop \cdot Rs)^2}{W^2} + \frac{(Tw \cdot (Rs \cdot (L - 2Lbn) + 2 \cdot Rbn \cdot Lbn + 2Rend))^2}{W^4} + \frac{(2Tlbn \cdot (Rs - Rbn))^2}{W^2}}$$

The tolerance parameter values for these equations can be found in the preceding table. Nominal sheet resistivities and definitions of all of the effective width and length dimensions can be found in "Resistor Design Specifications" on page 265. Each of these terms can be significant in determining the overall tolerance, depending on the actual width and length of the resistor layout. For large resistor dimensions, sheet resistivity tolerances will be the most dominant effect.

Polysilicon resistors placed over deep trench are not supported by the model. The presence of deep trench lattices under 400 square microns have not been observed to modulate resistance values. Polysilicon resistors placed over large deep trench lattices, though they remained within tolerance, were observed to have a systematic change in value. For optimal resistance tolerance, it is recommended that polysilicon resistors are not placed over large area deep trench lattice structures.

4.7.7 Resistor Matching

The percentage matching for identical, adjacent resistors with the same orientation, at the same temperature, is given by the equation below. It should be noted that any interconnect parasitic resistance and the voltage coefficient of resistance may have an effect at these matching levels. When matching ratioed resistors, the resistor must be built by combining identical unit resistors either in parallel or in series. Care should be taken to adhere to symmetrical layout of matched resistors. Considerations should not only include length and width, but metal coverage, deep trench isolation underlying polysilicon resistors and symmetry of generated levels, i.e. special care should be given to assure that any block mask levels being generated are present on both matched resistors.

The resistance matching is given by the equation:

$$M = \sqrt{\frac{M_a^2}{W \cdot L} + \frac{M_w^2}{W^2} + \frac{M_l^2}{L^2}} \quad \%$$

where L and W are as defined previously in the Resistor Design section. Values for the matching parameters for each resistor are defined as follows:

<i>Table 4-21. Resistor Matching Equation Parameters</i>				
Matching Parameters	nsres Resistor	opp cres Resistor	oprrpres Resistor	kgres Resistor
M_a	9.0	5.9	7.1	0.0
M_w	53.7 ¹	1.2 ¹	1.2	1.4
M_l	0.0	1.7	3.4	1.4
Note: Matching values represent 3-sigma limits.				

1. For this devices the length term is $Mw^2 / (L * W^2)$

4.7.8 OP Resistor Application Notes

Use of the OP poly resistor is allowed to be connected to an I/O pad. However, the OP poly resistor must be wide enough to handle the current flowing into or out of the I/O during normal operation. In the input receiver path, OP poly resistors are preferred over diffusion resistors. Diffusion resistors in the input path have a parasitic diode associated with them that can cause low CDM ESD failures. In the output driver path, OP poly resistors or OP diffusion resistors can be used however the maximum current densities of the OP poly resistor listed in the reliability section and the OP diffusion resistor listed in the reliability section must not be exceeded. OP poly resistors are not recommended in the HBM ESD current path.

The resistor models are designed as a subcircuit, or network of elements. The user must specify either the resistance and width of the resistor, or the length and width of the resistor; the proper parasitic elements are calculated based on these parameters. Please refer to the Modeling Reference Guide for syntax specifics.

The OP resistor current levels are limited by heating, and should not exceed the maximum current.

4.8 NCAP and DGNCAP Models

The CMOS8RF (CMRF8SF) nMOS varactor (ncap) is a tunable capacitor using a thin oxide NFET in an N-well with N+ source and drains shorted together. The variable capacitance is achieved by controlling the gate to diffusion/N-well potential within the range of -0.5V to 1.0V, which takes the silicon surface under the gate from depletion to accumulation. The capacitance per unit area can be varied from C_{max} to a minimum of approximately 20% of C_{max} over this range. There are also fringe components that depend on channel width and length and number of devices wired in parallel. At V_{g-d} below -0.5V, there is danger of instability because of the need for hole generation as the device passes into inversion. The construction of the equilibrium inversion layer takes some time (time scale on order of minutes) to accomplish. While this is occurring, the depletion width is being reduced. Hence, the capacitance of the device is unstable during this time. The maximum allowed voltage including power supply tolerances (V_{g-d}) for the ncap is +1.6 volts.

There is also a thick oxide NFET in an N-well device (dgncap). The capacitance per unit area can be varied from C_{max} to a minimum of approximately 37% of C_{max} over the range -0.5V to 1.0V. The same instabilities found for the ncap are also found for the dgncap. The maximum allowed voltage including power supply tolerances (V_{g-d}) for the dgncap is +3.6 volts.

Both the ncap and dgncap models support variable channel lengths and widths. Further, arrays of single devices can be formed. Any other irregular capacitor designs are **not** supported. The model does not calculate any inductance introduced by the metal wiring included in the ncap or dgncap. This must be supplied by the user and is layout dependent.

NCAP and DGNCAP or PCDCAPs are supported within the T3 isolation well.

4.8.1 MOS varactor Design

The nominal value equation for the capacitance of a MOS varactor at 25°C is:

$$C_{Nom}(V) = (C_A(V) \cdot L \cdot W \cdot F) + (C_L \cdot 2 \cdot L \cdot F) + (C_W \cdot 2 \cdot W \cdot F) + (C_F \cdot F)$$

where C_A(V) is the capacitance per area. The expression for C_A(V) is determined from first principles. The C_L, C_W, and C_F terms are fringe capacitance terms that are functions of the channel length (L), RX width (W), and number of individual devices wired in parallel (F).

The parameters in this equation for the ncap are given by:

$L = L_{Design} + dL \text{ } \mu\text{m}$	$dL = -0.028 \pm 0.022 \mu\text{m}$
$W = W_{Design} + dW \text{ } \mu\text{m}$	$dW = -0.045 \pm 0.04 \text{ } \mu\text{m}$
$F = \# \text{ of individual devices}$	
$C_A @ 1 \text{ V} = 10.8 \text{ fF}/\mu\text{m}^2$	$C_A @ -0.5 \text{ V} = 2.2 \text{ fF}/\mu\text{m}^2$
$C_L = 0.192 \text{ fF}/\mu\text{m}$	$C_W = 0.186 \text{ fF}/\mu\text{m}$
$C_F = 0.153 \text{ fF}/\#$	

The parameters in this equation for the dgncap are given by:

$L = L_{Design} + dL \text{ } \mu\text{m}$	$dL = -0.02 \pm 0.034 \mu\text{m}$
$W = W_{Design} + dW \text{ } \mu\text{m}$	$dW = -0.045 \pm 0.04 \text{ } \mu\text{m}$
$F = \# \text{ of individual devices}$	
$C_A @ 2 \text{ V} = 5.70 \text{ fF}/\mu\text{m}^2$	$C_A @ -0.5 \text{ V} = 2.0 \text{ fF}/\mu\text{m}^2$
$C_L = 0.11 \text{ fF}/\mu\text{m}$	$C_W = 0.161 \text{ fF}/\mu\text{m}$
$C_F = 0.152 \text{ fF}/\#$	

4.8.2 NCAP and DGNCAP Temperature Effects

Temperature variation has been included in the ncap and dgncap models. The models also include the effects of the depletion of the polysilicon gate in accumulation mode. The change in the gate and N-well depletion with temperature is the dominate mechanism for the change in shape of the CV curves with temperature.

4.8.3 NCAP and DGNCAP Parasitic Capacitance

The parasitic backplate capacitance of either the ncap or the dgncap is composed of both an area and perimeter component. The overall length and width of the NW shape is used to determine both the area and perimeter of the NW-to-substrate diode.

The voltage dependence of the NW-to-substrate junction capacitances is given by the equations:

$$C_A = \frac{C_{A0}}{\left(1 - \frac{V}{pb}\right)^{ma}} \quad \text{fF}/\mu\text{m}^2$$

$$C_P = \frac{C_{P0}}{\left(1 - \frac{V}{php}\right)^{mp}} \quad \text{fF}/\mu\text{m}$$

where C_A is the area component of capacitance, C_P is the perimeter component of capacitance and V is the bias voltage across the junction isolation. Values for the parameters in these equations are found in Table 4-22. Temperature variation of the NW-to-substrate parasitic diode has been characterized and is included in the model. The voltage polarity defined in the model causes a decrease in parasitic capacitance for the mosvar with increasing reverse-bias (negative voltage) across the N-well to substrate junction.

Table 4-22.ncap and dgncap Parasitic Capacitance Parameters

Capacitance Parameters	C_{A0} (fF/ μm^2)	pb (Volts)	ma	C_{P0} (fF/ μm)	php (Volts)	mp
(dg) ncap NW-SX	0.93	0.78	0.34	0.50	0.63	0.34

4.8.4 NCAP and DGNCAP Layout Notes

The ncap or dgncap may be defined as either squares or rectangles.

Design Layout Reminder

The ncap and dgncap models reflect the default capacitor device layout. Strict adherence to the groundrules and layout details provided in the device layout is recommended to achieve consistent device model and design tool compatibility and accuracy. Of course, use of the ncap and dgncap pcells in laying out any of these devices yield the most accurate model to hardware correlation. If designers choose to lay out these devices themselves, it is very important to remember that the ncap and dgncap devices *must* have a VAR layer surrounding them. This layer ensures proper device processing and recognition during LVS extraction.

The minimum length dimension for both the ncap and the dgncap is $L = 0.24 \mu\text{m}$. The minimum width dimension for both the ncap or dgncap is $W = 1.0 \mu\text{m}$.

The following caution applies when using either a ncap or a dgncap with a large perimeter in a design. Large perimeter designs have large fringe capacitances associated with them. These large fringe terms reduce the tunability of the device. Further, due to overhead in making electrical connections to all the fingers, the physical dimensions of large perimeter devices are larger, for a given total gate area, than for smaller perimeter devices. On the other hand, large individual gate area devices have lower Q values than smaller individual gate area devices, for the same total gate area.

4.9 Differential Varactor

A thin oxide nMOS varactor device (diffncap) is specifically designed as differential devices for use in VCO circuits. The diffncap device consists of two identical sets of polysilicon gates that are interdigitated and share the same N-well. Since the signal travels into the device through one set of gates/anodes and exits the device through the other set, there is no need for well contacts between the gates/anodes. This allows for an increased Q-factor compared to the standard device. For single-ended operation however, the standard device should be used as the Q will be better due to the close proximity of the well contacts to the gates/anodes in the standard device.

While the capacitance per area for the differential devices is exactly that of the corresponding standard devices, being calculated by the same Verilog-A modules, there are a few notable differences between the standard models and the differential models. First and foremost, the diffncap model has four nodes: one for each set of gates/anodes, one for biasing the common subcollector, and one for the usual substrate node. Second, the fringe capacitance changes slightly and a parasitic capacitance coupling between the two sets of gates/anodes is introduced. Lastly, the manner in which the various resistances within the model are distributed and combined are tailored to the specific layout of the diffncap; so use of the diffncap pcell in laying out any differential nMOS varactors yields the most accurate model to hardware correlation.

As always, please see to the Model Reference Guide for model-to-hardware correlation plots.

4.10 Hyperabrupt (HA) Junction Varactor Diode

The BiCMOS8HP technology provides a scalable hyperabrupt P+/N junction diode used as a tunable capacitor. The P+ region is similar to the PFET S/D while the N region is comprised of a N+ subcollector and a N-type implant. The N+ subcollector under the entire structure reduces the parasitic resistance, i.e., it improves the varactor Q factor, while the tailored N-type implant enhances tunability. A reachthrough is used at the cathode contact to provide a low-impedance path to the N+ deep implant. Scalability is obtained by selecting both the size and number of anodes. Supported layouts consist of a single or multiple anodes, all with wrap-around cathodes.

The model includes an approximate calculation for the inductance introduced by the metal wiring included in the havar p-cell. This inductance calculation is derived based on the layout of the supplied p-cell, assuming contact is made to the device at the centers of the anode and cathode metal bus lines connecting the fingers of the anode and cathode together. Use of the havar p-cell in this configuration yields the most accurate model to hardware correlation. If the internal inductance calculation is not desired, it can be overridden with a user-defined inductance value by the use of a switch.

As input, the model requires the anode width, length and number of anodes, or the anode width, zero volt device capacitance and number of anodes. Please review the HA varactor diode model file for syntax specifics.

4.10.1 HA Varactor Design

The nominal value equation for the capacitance of a HA varactor at 25°C is:

$$C_{Nom}(V) = (C_A(V) \cdot L \cdot W \cdot N) + (C_P(V) \cdot 2N \cdot (W + L))$$

where $C_A(V)$ is the capacitance per area and $C_P(V)$ the capacitance per length.

The parameters in these nominal capacitance equations are given by:

$$\begin{aligned} L &= L_{Design} + dL \text{ } \mu\text{m} & dL &= -0.045 \pm 0.04 \text{ } \mu\text{m} \\ W &= W_{Design} + dW \text{ } \mu\text{m} & dW &= -0.045 \pm 0.04 \text{ } \mu\text{m} \\ N &= \# \text{ of anodes} \\ C_A @ 0 \text{ V} &= 2.05 \text{ fF}/\mu\text{m}^2 & C_P @ 0 \text{ V} &= 0.176 \text{ fF}/\mu\text{m} \end{aligned}$$

The model employs a physics-based calculation to determine the capacitance as a function of applied voltage using VerilogA. The temperature dependence of the capacitance is also included in the model and comes through the temperature variation in the built-in potential across the p-n junction.

4.10.2 HA Varactor Parasitic Capacitance

The parasitic backplate capacitance of the HA varactor is composed of both an area and perimeter component. The overall length and width of the subcollector shape is used to determine both the area and perimeter of the cathode-to-substrate diode. The voltage dependences of the cathode-to-substrate junction capacitances are given by the standard junction equations, see section 4.8.3, “NCAP and DGNCAP Parasitic Capacitance” on page 274. Values for the parameters in these equations are found in the Table 4-23.

<i>Table 4-23. HA Varactor Parasitic Junction Capacitance Parameters</i>	
Capacitance Parameters	Cathode-SX Parasitic Diode
C_{AO} (fF/ μm^2)	0.1
pb (Volts)	0.7
ma	0.344
C_{PO} (fF/ μm)	0.1
php (Volts)	1.0
mp	0.01

4.10.3 HA Varactor Leakage Current

The leakage current in the HA varactor model is found to only involve a perimeter (I_{Plk}) component so $I_{leak} = I_{Plk}(V) \cdot 2N \cdot (W + L)$, where W, L, and N are as previously defined for the junction capacitance. The $I_{Plk}(V)$ are function of V given by

$$I_{Plk} = 2.0 \sinh(1.0 V) \frac{fA}{\mu m}$$

4.10.4 HA Varactor Design Layout Reminder

The HAVAR varactor model reflects the default capacitor device layout. Strict adherence to the groundrules and layout details provided in the device layout is recommended to achieve consistent device model and design tool compatibility and accuracy. Use of the HAVAR varactor p-cell in laying out any HA varactor yields the most accurate model to hardware correlation. Use of other device layout/geometries is not supported. Should you require modeling support for other diode geometries, please contact your IBM Product Engineer.

4.11 MIMCAP

The MIM capacitor is built between the thin layer of the metal, QY, and LY. QY is the top plate of the capacitor.

The models support variable dimensions for both width and length. Allowable capacitor shapes include both squares and rectangles. Note that any other irregular capacitor designs are **not** supported.

4.11.0.1 Capacitor Design Specifications

The specifications in Table 4-24 may be used as a guide in applications.

Table 4-24.MIM Capacitor Specifications	
Specification	Single MIM
Area Capacitance (0V, 25°C) = CA	1.00 fF/μm ²
Perimeter Capacitance = CP	0.063 fF/μm
Temperature dependence	17.7 ppm / °C

Where:

The nominal value equation for the capacitance of a MIM capacitor at 25°C and 0 volts is:

$$C_N = (C_A \cdot L \cdot W) + (C_P \cdot 2 \cdot (L + W)) \quad fF$$

L = Design Length (QY) in μm

W = Design Width (QY) in μm

4.11.0.2 Voltage Coefficient of Capacitance

The voltage coefficient ratio of the MIM capacitor is governed by the equation:

$$VCR = 1.0 + (38 \times 10^{-6} \cdot V) + (3.7 \times 10^{-6} \cdot V^2)$$

where V is the voltage across the capacitor (bottom plate positive).

4.11.0.3 Capacitor Tolerance

The capacitor tolerances are defined based on measured variation of both geometric layout parameters and process (sheet resistivities, unit capacitances) parameters. In most cases, the dominant variation of the capacitance is due to only a few of the process parameters defining a capacitor's value.

- The tolerance on the area capacitance is 0.15 fF/μm²
- The tolerance on the perimeter capacitance is 0.08 fF/μm

4.11.1 Capacitor Matching

The 3-sigma percentage matching for identical, adjacent MIM capacitors with the same orientation and at the same voltage is given by the equation:

$$M = \sqrt{\frac{(1.0)^2}{A^2} + \frac{0.3^2}{W^2} + \frac{0.3^2}{L^2}} \quad \%$$

where width and length are the QY drawn dimensions in μm. It should be noted that interconnect parasitic capacitance may have an effect at these matching levels. When matching ratioed capacitors, the capacitors must be built by paralleling identical unit capacitors.

4.11.2 Capacitor Parasitics

The model includes a calculation for the parasitic capacitance from the bottom plate of the MIM capacitor to substrate assuming the MIM is placed over a buried subcollector (NS) plate. This capacitance depends on the BEOL metallization option (nlev = 5,6 or 7). The general form of the parasitic capacitance is given by:

$$C_{parasitic} = (C_A \cdot L \cdot W) + (C_P \cdot 2 \cdot (L + W)) \quad fF$$

with the width and length dimensions for the QY shape in μm. Since the top plate is designed to be smaller than the QY shape, there are no parasitic fringing effects between the top plate and substrate.

The unit area and perimeter capacitance values for the bottom plate are shown in the following table:

Table 4-25.MIM Capacitor Bottom Plate Parasitics		
Area Parasitic Capacitance C_A (fF/ μm^2)		
nlev = 5	nlev = 6	nlev = 7
0.0054	0.0050	0.0045
Perimeter Parasitic Capacitance C_P (fF/ μm)		
nlev = 5	nlev = 6	nlev = 7
0.0376	0.0366	0.0357

Note: This internal parasitic capacitance is set to a negligible value (0.01fF) whenever a netlist is generated using the layout extraction tool or can be manually “turned off” by setting the model parameter est=0 in the netlist. This allows for a more accurate calculation of the bottom plate parasitic capacitance to support the option of placing other devices underneath the MIM. Simulations using a netlist generated from the schematic with the default parameter settings (est=1) will underestimate this bottom plate parasitic capacitance for the case where other devices will be placed underneath a MIM.

The MIM capacitor models have an internal parasitic inductance in series with the capacitance. Inductance of any wires leading to the MIM capacitor must be accounted for in the netlist with some additional parasitic elements external to the device model.

4.12 Capacitor Application Notes

Design Layout Reminder

All capacitor models reflect their default device set layout. Strict adherence to the ground rules and layout details provided in the device set layout is recommended to ensure full and consistent device model and design tool compatibility and accuracy.

The MIM is very susceptible to ESD. If the MIM is connected to a terminal pad ESD protection should be used. If this is not possible then handling procedures must be followed to prevent electro-static discharge damage to the MIM. The floating metal check requires at least a minimum diode for minimal protection during test and assembly.

4.13 Forward-Biased Diode Device Models

The general use of forward-biased diodes as circuit elements is not supported. Forward bias of diffusions will produce current at adjacent diffusions that can affect circuit performance, degrade device characteristics, and cause latchup. It is to be avoided wherever possible by careful circuit design.

Customers are required to request a waiver from the IBM Technical Representative for each specific design application where a forward-biased diode is used as a active circuit element. However, one application, band-gap reference circuits using the P-diffusion in a (**recommended tied to substrate**) N-well as a diode, is being allowed within specific restrictions. Supported geometries include squares and rectangles; other shapes, such as L-shapes, are **not** supported. The designer is allowed to select lengths and (limited) widths and number of fingers to optimize the physical size of the diode while remaining within the current density limits.

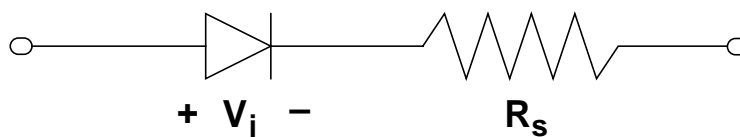
Ideally, the P+/N-well diode pcell (divnpn) should be used in order to ensure a fully consistent device model. Both of these models simulate the same P+/NW junction. The divnpn model is a three terminal model (bjt model) that has separate N-well and substrate ring nodes. It is *strongly* recommended that these nodes be shorted together to prevent accidental forward biasing of the NW/SX junction. Should you require modelling support for geometries other than those described here, please contact your IBM Technical Representative.

The allowable width and length dimensions are given in Table 4-26.

Table 4-26. Groundrule Layout Dimensions for P+ Nwell Diodes

Layout Dimensions	Width (Min)	Width (Max)	Length (Min)
P+ Nwell Diode	1.0	2.0	2.0

The DC model described here becomes a poor predictor of the actual current-voltage relationship for current densities above $100 \mu\text{A}/\mu\text{m}^2$. The P-diffusion in a grounded N-well diode-current can be modeled as an ideal diode with a series resistor, as shown below.



The current flowing through the device is given by the expression

$$I = I_o \times \left[\exp\left(\frac{qV_j}{N_f kT}\right) - 1 \right]$$

where V_j is the voltage drop across the junction, I_o the saturation current and N_f the ideality factor. For small current values, the voltage drop across the resistor can be neglected resulting in a purely exponential I-V dependence. In this case, V_j can be replaced with V_A , the voltage applied to the anode. When the exponential I-V relation is critical to the application, current densities should be maintained above $500 \text{ pA}/\mu\text{m}^2$ and below $1 \mu\text{A}/\mu\text{m}^2$.

The saturation current I_o is expressed as a function of the area and perimeter of the anode

$$I_o = J \cdot \text{Area} + K \cdot \text{Perimeter}$$

At higher current levels, the series resistance R_s cannot be ignored. The dominate terms for this resistance are the resistance through the N-well from the anode to the cathode contact, and particularly the resistance up through the cathode contact itself.

Extracted values at 25°C for the various parameters used in these expressions for the forward-bias DC operation of the P+ Nwell diode are given in Table 4-27.

Table 4-27. Forward-Bias Parameters for dipdnw diode

DC Parameter Values (@ 25°C)	N_f	J ($10^{-21} \text{ A}/\mu\text{m}^2$)	K ($10^{-21} \text{ A}/\mu\text{m}$)
P+ Nwell Diode	1.006	90. $\pm 50\%$	27. $\pm 50\%$

The preceding model parameters are valid at $T_{nom} = 25\text{ }^{\circ}\text{C}$. The most dominant temperature effect is an increase in the saturation current I_o . The theoretical temperature dependence of I_o is given by the expression

$$\ln[I_o(T)] - \ln[I_o(T_{nom})] = \frac{E_{gap}(T_{nom})}{V_{thrm}(T_{nom})} - \frac{E_{gap}(T)}{V_{thrm}(T)} + 3 \ln\left(\frac{T + 273}{T_{nom} + 273}\right)$$

where E_{gap} is the band gap energy and V_{thrm} is the usual kT

$$V_{thrm} = 8.617 \times 10^{-5} (T + 273) \text{ eV.}$$

The band gap energy has its own temperature dependence given by the expression

$$E_{gap}(T) = E_{gap}(0K) - \frac{\alpha_{eg}(T + 273)^2}{\beta_{eg} + (T + 273)} \text{ eV}$$

where α_{eg} and β_{eg} are parameters taken from the literature. The $E_{gap}(0K)$ is the value of the band gap energy at absolute zero, and has been adjusted in order to obtain a good fit to the measured data for the temperature dependence of I_o . Values for the parameters in the expression for the temperature dependence of the band gap energy are given in Table 4-28.

Table 4-28. Parameters for the temperature of the band gap energy

Temperature Dependence Parameters	$E_{gap}(0K)$ (eV)	α_{eg} (10^{-4} eV/K)	β_{eg} (K)
	1.13	4.73	636

The percentage matching for identical, adjacent diodes with the same orientation, at the same temperature, is given by the equation below. Care should be taken to adhere to symmetrical layout of matched diodes. Considerations should not only include length and width, but metal coverage and symmetry of generated levels, i.e. special care should be given to assure that any block mask levels being generated are present on both matched diodes.

The diode matching is handled through the saturation current and the matching coefficient is given by the equation:

$$M = \sqrt{\frac{4.9^2}{W \cdot L \cdot F} + \frac{0.8^2}{L \cdot L \cdot F} + \frac{0.8^2}{W \cdot W \cdot F}} \quad \%$$

where L and W are the drawn length and width of the device in μm , respectively, and F is the number of fingers.

4.14 Wiring Resistance and Capacitance Models

4.14.1 Conducting Film Thickness

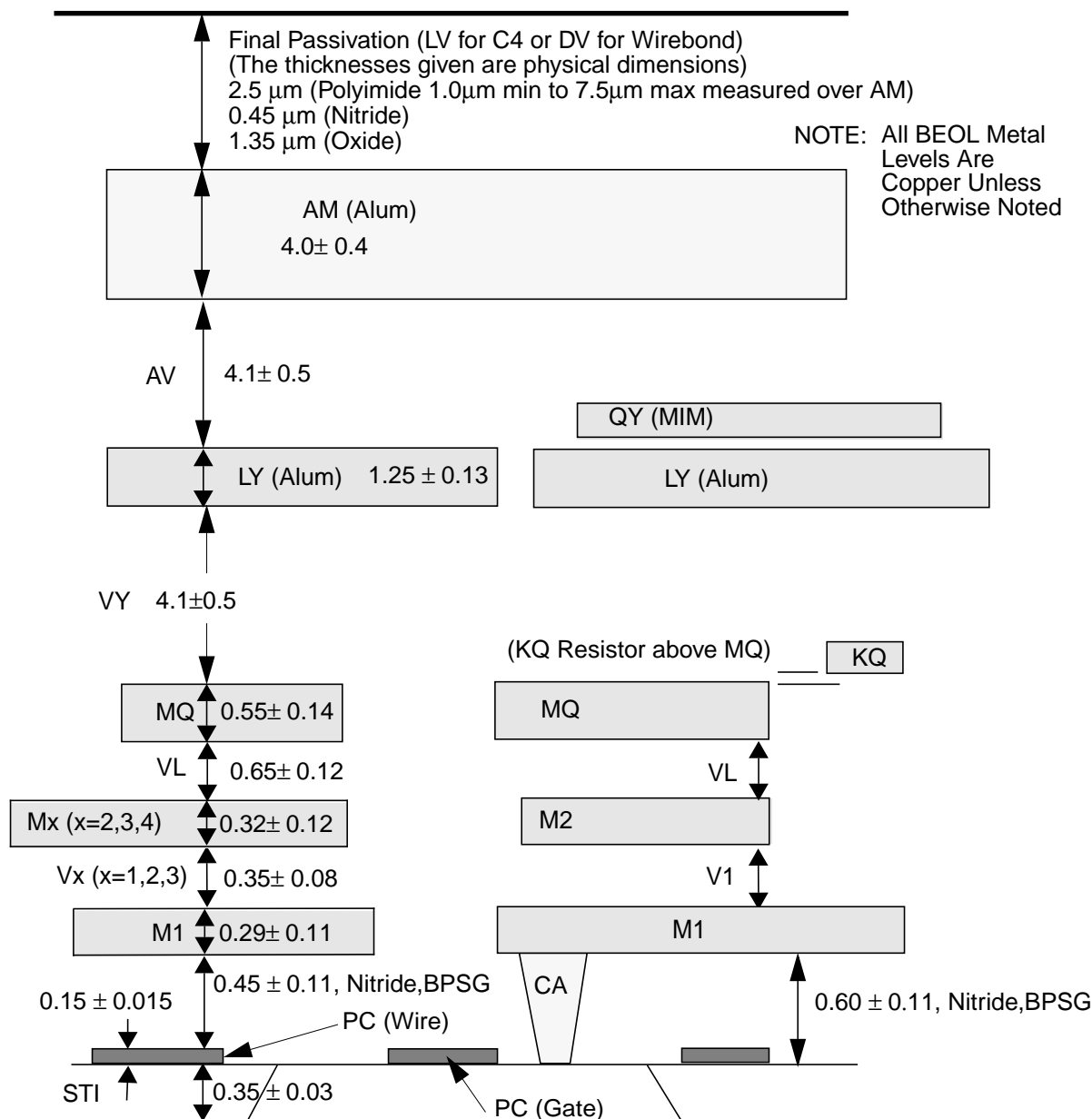


Figure 4-5. BEOL Conducting and Interlevel Film Thicknesses - not drawn to scale

4.14.2 Wire Resistance Models

4.14.2.1 Contact and Via Resistance

The following table lists contact resistance values. Contacts are made through M1/CA to RX or PC. If M1 through RX or M1 through PC contacts are stacked vertically, add the two relevant contact resistances to get the total.

Do NOT RSS the contact resistance values for multiple contacts. For worst case analysis use the parallel combination of several contacts all at their worst case resistance value. The resistances include the metal pad immediately above and any resistance due to the 90 degree bend in the current flow.

The resistances of the allowed via sizes described in section 3.1, “Polysilicon and Isolation Layout Rules” on page 69 are listed in Table 4-29, “Contact Resistance” on page 283. For worst case analysis use the parallel combination of several vias all at their worst case resistance value.

Table 4-29. Contact Resistance				
Contact	Levels	Nominal [Ω /contact]	Minimum / Maximum [Ω /contact]	TCR ¹ [% / ° C]
CA ²	M1-CA-PC M1-CA-RX	9	5 / 20	<0.5
CA ³	M1-CA-PC M1-CA-RX	9	5 / 25	<0.5

1. TCR is nominal room temperature (25° C)
2. The nominal CA resistances are extracted from a single contact, fully landed
3. for (PC-CA space < 0.12) OR (CA within PC < 0.04 μ m), see R207 and R209, Table 3-4, “N-well, Contact, Junction Layout Rules” on page 83

Table 4-30. Via Resistance				
Via	Levels	Nominal Resistance [Ω /via]	Minimum / Maximum Resistance [Ω /via]	TCR [% / ° C]
V _x ² (x=1,2,3)	M2-V1-M1	0.9	0.2 / 6.0	0.33
VL	MQ-VL-M4 MQ-VL-M3 MQ-VL-M2	0.25	0.1 / 3.0	0.33
VY	MQ-VY-LY	0.51	0.2 / 3.0	<0.5
AV	LY-AV-AM	0.38	0.2 / 3.0	< 0.5
C4 VIA	AM	0.02	0.004 / 0.1	< 0.33

1. Including TCR
2. All nominal via resistances are extracted for fully landed Via

4.14.2.2 Resistance of Conducting Film

The 25° C sheet resistances and film thicknesses are listed in the following tables.

Note: Starting substrate resistivity is 11-16 ohm-cm.

Table 4-31. Conducting Film Thicknesses and Sheet Resistances at 25°C					
Film	Rules	Design Width [μm]	Thickness [μm]	R _s [Ω/square]	TCR [% / ° C]
P-well (under STI)	-	-	-	140 ¹ ± 110 260 ² ± 110	-
Vertical P-well resistance	-	-	1.0	1.0 ± 0.35 [kΩ-μm ²]	-
N-well (under STI)	250	0.7	-	540 ± 110	0.2
N-well ³ (under STI outside (PI expanded by +1.1μm))	TW06	1.10	-	420 ± 110	0.2
Vertical N-well resistance	-	-	1.0	1.5 ± 0.40 [kΩ-μm ²]	-
P+ unsalicided poly	-	> 2	0.15 ± 0.015	340 ± 40	-0.08 ± 0.06
N+ unsalicided diffusion	-	> 0.20	-	73 ± 8	0.143 ± 0.1
N+ diffusion bounded by PC and isolation	110	≥ 0.28	-	7 ± 3	0.32
P+ diffusion bounded by PC and isolation	110	≥ 0.28	-	7 ± 3	0.34
N+ diffusion bounded by PC	104	< 0.22	-	12 -7 / +60	0.31
N+ diffusion bounded by PC	104	≥ 0.22 < 0.26	-	10 -5 / +15	0.31
N+ diffusion bounded by PC	104	≥ 0.26	-	7 ± 3	0.31
P+ diffusion bounded by PC	104	< 0.22	-	12 -7 / +100	0.34
P+ diffusion bounded by PC	104	≥ 0.22 < 0.26	-	10 -5 / +15	0.34

Table 4-31. Conducting Film Thicknesses and Sheet Resistances at 25°C

Film	Rules	Design Width [μm]	Thickness [μm]	R _s [Ω/square]	TCR [% / ° C]
P+ diffusion bounded by PC	104	≥ 0.26	-	7 ± 3	0.31
N+ diffusion bounded by isolation ⁴	50	≥ 0.22	0.17 ± 0.017	7 ± 3	0.32
P+ diffusion bounded by isolation	50	≥ 0.22	0.15 ± 0.015	7 ± 3	0.29
PC (N+ or P+)	100	≥ 0.12	0.15 ± 0.015	7 ± 3	0.32
M1	500	< 1.0	0.29 ± 0.11	0.0709 ± 0.0297	0.30
M1	500	≥ 1.0	0.32 ± 0.11	0.0643 ± 0.0242	0.30
M2, M3, M4	600	< 1.0	0.32 ± 0.12	0.0639 ± 0.0262	0.30
M2, M3, M4	600	≥ 1.0	0.35 ± 0.12	0.0584 ± 0.0217	0.30
MQ	635	< 1.0	0.55 ± 0.140	0.0373 ± 0.0082	0.30
MQ	635	≥ 1.0	0.60 ± 0.140	0.0339 ± 0.0068	0.30
MQ over MQPLANE	635d	> 50.0	0.55 ± 0.140	0.0373 ± 0.0082	0.30
LY	LY1	≥ 1.52	1.25 ± 0.13	0.023 ± 0.005	0.33
AM	AM1	≥ 2.0	4.0 ± 0.4	0.007 ± 0.0014	0.38

1. Measured over long distance (> 10 μm). The lower resistance results from the fact that the current path is able to extend deep into the bulk (with blanket implant).
2. Measured over short distances (< 10 μm).
3. N-well R_s and TCR for NW outside PI is preliminary information, and is subject to change. See BT generation in Table 2-6, "Shape Manipulation Prior to Mask Write" on page 44
4. Measured from bottom of CoSi₂ to junction edge.

4.14.2.3 Calculating Metal Line Resistance

The metal line resistance R per unit length is calculated as [Ω/μm]

$$R = \frac{R_s}{W_{eff}}$$

with R_s taken from Table 4-31, "Conducting Film Thicknesses and Sheet Resistances at 25°C" and W_{eff} defined as W_{eff} = [W_c - (2 x PLB) - (2 x ELB)] from Table 4-32, "Effective Linewidth for Wires with HOLE Shapes", and for 'W_d' in Table 4-40, "Extraction Parameters for Metal Wiring".

Table 4-32. Effective Linewidth for Wires with HOLE Shapes ¹		
Contact	Designed Linewidth, Wd	Corrected Linewidth, Wc
M1	$0.16 \leq Wd \leq 1.8$	Wd
M1	$1.8 < Wd \leq 50$	$1.4 + 0.7 * (Wd - 1.4)$
(M1 over M1PLANE)	$Wd > 50$	$1.4 + 0.52 * (Wd - 1.4)$
M2, M3, M4	$0.2 \leq Wd \leq 1.8$	Wd
M2, M3, M4	$1.8 < Wd \leq 50$	$1.4 + 0.7 * (Wd - 1.4)$
(Mx over MxPLANE) (x=2,3,4)	$Wd > 50$	$1.4 + 0.52 * (Wd - 1.4)$
MQ	$0.4 \leq Wd \leq 2.4$	Wd
MQ	$2.4 < Wd \leq 50$	$2.4 + 0.7 * (Wd - 2.4)$
(MQ over MQPLANE)	$Wd > 50$	$2.4 + 0.53 * (Wd - 2.4)$

1. Because wide Copper wires will contain Metal HOLE shapes, the Effective Linewidth Weff must be used for all Electron migration calculations (see Table 5-1, “Current Limits at (100/125) degrees C (for PC, M1, M2, M3, M4, MQ, LY, AM),” on page 362).

The wiring resistance tolerance as a percent may be calculated as follows. The tolerances for ‘T’ can be found in Table 4-31, “Conducting Film Thicknesses and Sheet Resistances at 25°C”, and ‘Weff’ from Wd in Table 4-32, “Effective Linewidth for Wires with HOLE Shapes” with Table 4-40, “Extraction Parameters for Metal Wiring”. By applying this procedure to an array of minimum width and minimum space wires, the results in 4-33 are obtained. Note that all these cases give metal density pattern factors below 50%.

$$\frac{\Delta R}{R} = \left(\frac{\Delta A}{A} \right) \sqrt{1 + \frac{8}{9} \left(\frac{\Delta A}{A} \right)^2}$$

$$\frac{\Delta A}{A} = \sqrt{\left(\frac{\Delta T}{T} \right)^2 + \left(\frac{\Delta Weff}{Weff} \right)^2}$$

Table 4-33. Wire Resistance in an Array of Minimum Width and minimum Space Wires at 25°C			
Metal Layer	Wire Resistance per Unit Length	Wire Resistance Tolerance	
	[Ω/μm]	[Ω/μm]	[%]
M1 (Wd = 0.16μm)	0.518 ¹	0.287	55.5
M2, M3, M4 (Wd = 0.20μm)	0.32 ¹	0.162	50.6

Table 4-33. Wire Resistance in an Array of Minimum Width and minimum Space Wires at 25°C

Metal Layer	Wire Resistance per Unit Length	Wire Resistance Tolerance	
	[$\Omega/\mu\text{m}$]	[$\Omega/\mu\text{m}$]	[%]
MQ (Wd = 0.4 μm)	0.105 ¹	0.039	36.8
MQ (Wd = 1.0 μm)	0.035	0.010	27.9

1. The wire resistance per unit length entry is from the Wafer Acceptance Criteria.

4.14.3 Wiring Capacitance Models

4.14.4 Interlevel Area Capacitance

The area component of wiring capacitance may be calculated using the dielectric thicknesses given in the following tables.

4.14.5 Parameters for Capacitance Calculation

The film parameters for the calculation of the wiring capacitances are found in Table 4-34, “Wiring Capacitance Model Parameters,” on page 288. These numbers assume that the calculation will be done with wiring at pitch (a minimum line with neighboring lines at minimum space) and 100% metal coverage above and below by metal. The interlevel thicknesses (h_a , h_b) are the physical dielectric thicknesses.

The actual wiring capacitance is the sum of four capacitance components: C_{up} , C_{down} , C_{right} , and C_{left} . Each component can be calculated as follows. Calculate an initial value for each component by assuming that the surrounding dielectric medium is uniform and has a relative dielectric constant equal to one. This calculation can be done using an analytical formula or a two-dimensional simulation tool. The final value for each component is then obtained by multiplying the initial value by the corresponding effective dielectric constant, as given in Table 4-35, “Effective Dielectric Constant,” on page 288.

These tables are not substitute for EM field solvers and accurate calculations of capacitance will require appropriate 2-dimensional or 3-dimensional electromagnetic simulations. Such simulations should be performed for all structures in which accurate prediction of capacitance and capacitive effects are deemed critical to the overall circuit performance.

Table 4-34. Wiring Capacitance Model Parameters

Wiring Levels	Design Size (L/S) [μm]	h_B (lower ILD) [μm]	h_A (upper ILD) [μm]	W^1 (wire width) [μm]	D^1 (wire spacing) [μm]	T_{film} (wire height) [μm]
PC over isolation under M1	0.12 / 0.20	0.35	0.45	0.092	0.228	0.15
M1 over PC under M2	0.16 / 0.16	0.45	0.35	0.16	0.16	0.29
M1 over isolation under M2	0.16 / 0.16	0.95	0.35	0.16	0.16	0.29
M2 over M1 under M3 M3 over M2 under M4	0.2 / 0.2	0.35	0.35	0.22	0.18	0.32
M2 over M1 under MQ M3 over M2 under MQ M4 over M3 under MQ	0.2 / 0.2	0.35	0.65	0.22	0.18	0.32
MQ over M2 under LY MQ over M3 under LY MQ over M4 under LY	0.4 / 0.4	0.65	4.10	0.42	0.38	0.55
LY over MQ under AM	1.52 / 1.52	4.10	4.10	1.645	1.395	1.25
AM over LY	2.0 / 2.8	4.10	4.30	2.16	2.64	4.00

1. **Note:** The 'W' and 'D' are wafer values at 'half height'.

Table 4-35. Effective Dielectric Constant

Wiring Levels	ϵ_{up}	ϵ_{down}	$\epsilon_{right} \epsilon_{left}$ nested	$\epsilon_{right} \epsilon_{left}$ isolated
PC over isolation under M1	4.36	4.10	6.00	6.00
M1 over PC under M2	4.18	4.36	4.28	4.00
M1 over isolation under M2	4.18	4.21	4.34	4.34
M2 over M1 under M3 M3 over M2 under M4	4.18	4.18	4.00	3.60
M2 over M1 under MQ M3 over M2 under MQ M4 over M3 under MQ	3.96	4.18	4.14	3.60
MQ over M2 under LY MQ over M3 under LY MQ over M4 under LY	4.13	3.96	3.95	3.60
LY over MQ under AM	4.14	4.13	4.56	4.24

Table 4-35. Effective Dielectric Constant

Wiring Levels	ϵ_{up}	ϵ_{down}	$\epsilon_{right} \epsilon_{left}$ nested	$\epsilon_{right} \epsilon_{left}$ isolated
AM over LY	3.81 ¹	4.14	4.24	3.84 ¹

1. **NOTE:** Values are derived by using information provided in Figure 4-5. “BEOL Conducting and Interlevel Film Thicknesses - not drawn to scale” on page 282 and Table 4-37 on page 290 with assumption that all dielectrics are treated as planar.

4.14.6 Wiring Capacitance Tracking

The tracking percentages listed below are for identical metal lines (M1, Mx and AM, MQ) on the same wiring level that are less than 1500 μm long and less than 500 μm apart. In addition, the lines must be symmetrical with respect to conductors crossing above and below and with respect to adjacent lines on the same level. The lines are assumed to be design minimum width.

- M1 $\pm 5\%$
- Mx $\pm 5\%$
- AM, MQ $\pm 5\%$

4.14.7 Quick Lookup Wiring Capacitances

Interlevel Capacitance

Table 4-36, “Wiring Capacitances”, presents the wiring capacitance for the various levels. (These numbers assume a metal plate above and below, and minimum pitch wiring at the same level.) See the pitches in Table 4-34, “Wiring Capacitance Model Parameters,” on page 288.

Table 4-36. Wiring Capacitances¹

Wiring Levels					Isolated Line		
	C_{up}	C_{down}	$C_{left/Right}$	C_{total}	C_{up}	C_{down}	C_{total}
PC over isolation under M1	0.027	0.032	0.051	0.161	0.055	0.066	0.121
M1 over PC under M2	0.034	0.028	0.094	0.250	0.077	0.065	0.142
M1 over isolation under M2	0.035	0.014	0.099	0.247	0.090	0.039	0.129
M2 over M1 under M3	0.041	0.041	0.085	0.252	0.080	0.080	0.160
M2 over M1 under MQ	0.022	0.041	0.090	0.243	0.051	0.088	0.139
M3 over M2 under MQ							
M4 over M3 under MQ							
MQ over M2 under LY	0.009	0.046	0.077	0.210	0.022	0.103	0.125
MQ over M3 under LY							
MQ over M4 under LY							
LY over MQ under AM	0.029	0.028	0.067	0.191	0.062	0.060	0.122
AM over LY	n/a	0.046	0.079	0.204	n/a	0.109	0.109

1. Capacitance per unit length [fF/ μ m]

4.14.8 PC to CA Capacitance

This capacitance becomes important at minimum CA to PC spaces and is sensitive to alignment. Contact your IBM technical representative for additional details.

4.14.9 Final Passivation

Final Passivation over AM is 1.35 μ m oxide, 0.45 μ m nitride, plus 1.0 to 7.5 μ m (2.5 μ m nominal) polyimide and is shown in Figure 4-5, on page 282. For the final passivation dielectric constants, see Table 4-37, on page 290. All parameters are assumed to be nominal. All values in the table are for wafer dimensions.

4.14.10 Dielectric Constants

Table 4-37. Dielectric Constants	
Material	Value
Oxide	4.1 or 3.6 (dependent on metal/via interlevel level dielectric)
Nitride	7.0
Polyimide	3.4

4.14.11 Resistance and Capacitance Extraction Parameters

Table 4-38.Extraction Parameters for Polysilicon¹

Parameter	Label	Description	Design [μm]	Wafer Physical [μm]	Bias per edge (design – physical)/2 [μm]	3σ Tolerance per edge [μm]
Polysilicon resistance and parasitic capacitance. (Wiring)	E1	PC width at half-height	0.12	0.092	0.014	0.011
Polysilicon resistance and parasitic capacitance. (Wiring)	E1UT	PC width at half-height	0.12	0.070	0.025	0.0095
Polysilicon resistance and parasitic capacitance to metal layers.	E2	NGATE and PGATE width at half-height	0.12	0.092	0.014	0.011
Polysilicon resistance and parasitic capacitance to metal layers.	E2UT	NGATE and PGATE width at half-height	0.12	0.070	0.025	0.0095
Polysilicon to polysilicon wiring capacitance	E3	PC to PC space at half-height	0.20	0.228	– 0.014	0.011
Polysilicon to polysilicon wiring capacitance	E3UT	PC to PC space at half-height	0.20	0.250	– 0.025	0.0095
Polysilicon wiring to diffusion capacitance	E4	PC to RX space at half-height	0.08	0.094	– 0.014 (per shape)	0.042
Polysilicon wiring to diffusion capacitance	E4UT	PC to RX space at half-height	0.08	0.105	– 0.025 (per shape)	0.042
Spacer width	E5	-	-	0.07	-	0.007

1. NGATE is defined as PC over RX not over BP; PGATE is defined as PC over both RX and BP; PC is defined as PC not over RX. Note that “width” as used here is in the direction of Leff.

Table 4-39.Extraction Parameters for Diffusion¹

Parameter	Label	Description	Design [μm]	Wafer Physical [μm]	Bias per edge (design – physical)/2 [μm]	3σ Tolerance per edge [μm]
Butted Junction	E10	Butted Junction	0.16	0.115	0.023	0.040

Table 4-39. Extraction Parameters for Diffusion¹

Parameter	Label	Description	Design [μm]	Wafer Physical [μm]	Bias per edge (design – physical)/2 [μm]	3σ Tolerance per edge [μm]
Diffusion resistance, poly-bounded	E7	RX bounded by NGATE/PGATE poly and spacers.	0.20	0.088	0.056	0.017
Diffusion capaci- tance, poly-bounded, a	E8	RX bounded by NGATE/PGATE poly (width at half-height)	0.20	0.228	– 0.014	0.011
Diffusion resistance, poly-bounded	E7UT	RX bounded by NGATE/PGATE spacers	0.20	0.110	0.045	0.017
Diffusion capaci- tance, poly-bounded, a	E8UT	RX bounded by NGATE/PGATE poly (width at half-height)	0.20	0.250	– 0.025	0.0095
Diffusion resistance and capacitance, N and P, isola- tion-bounded, b	E9	RX width at top bounded by shallow trench isolation	0.16	0.115	0.0225	0.020
N-well resistance & capacitance		Effective electrical width	0.7	0.556	0.072	0.05

1. See section 4.6, “Junction Diodes” on page 260, for use of a and b in capacitance calculations.

Table 4-40. Extraction Parameters for Metal Wiring

Parameter	Design width	Pattern Factor	Physical Line Bias ¹ per edge = (design – physical)/2 = PLB [μm]	Electrical Line Bias ² per edge = (physical – electrical)/2 = ELB [μm]	3σ Tolerance per edge [μm]
M1 resistance	all	all	0.00	0.0115	± 0.0225
M2, M3, M4 resis- tance	all	all	-0.01	0.0000	± 0.030
MQ resistance	all	all	-0.01	0.0220	± 0.045
LY resistance	all	all	-0.0625	0.0	± 0.170
AM resistance	all	S≥12.5 ³	+0.080	0.0	± 0.300

Table 4-40. Extraction Parameters for Metal Wiring

Parameter	Design width	Pattern Factor	Physical Line Bias ¹ per edge = (design – physical)/2 = PLB [μm]	Electrical Line Bias ² per edge = (physical – electrical)/2 = ELB [μm]	3σ Tolerance per edge [μm]
AM resistance	all	$S < 12.5^3$	0.0558^4	0.0	± 0.300

1. Per edge, a positive number means that the on wafer is smaller than the design dimension. The physical (on wafer) dimension here is measured at the half height.

2. Per edge, a positive number means that the electrical linewidth is smaller than the physical dimension.

3. Resistive bias of AM lines as a function of the space to the next line (S) is given by the following: If $S < 12.5$ If $S \geq 12.5$
Bias per edge = $[-((0.028 \times S) - 0.19)]/2$ Bias per edge = -0.08 .

4. Assumes minimum AM-AM space of 2.8μm.

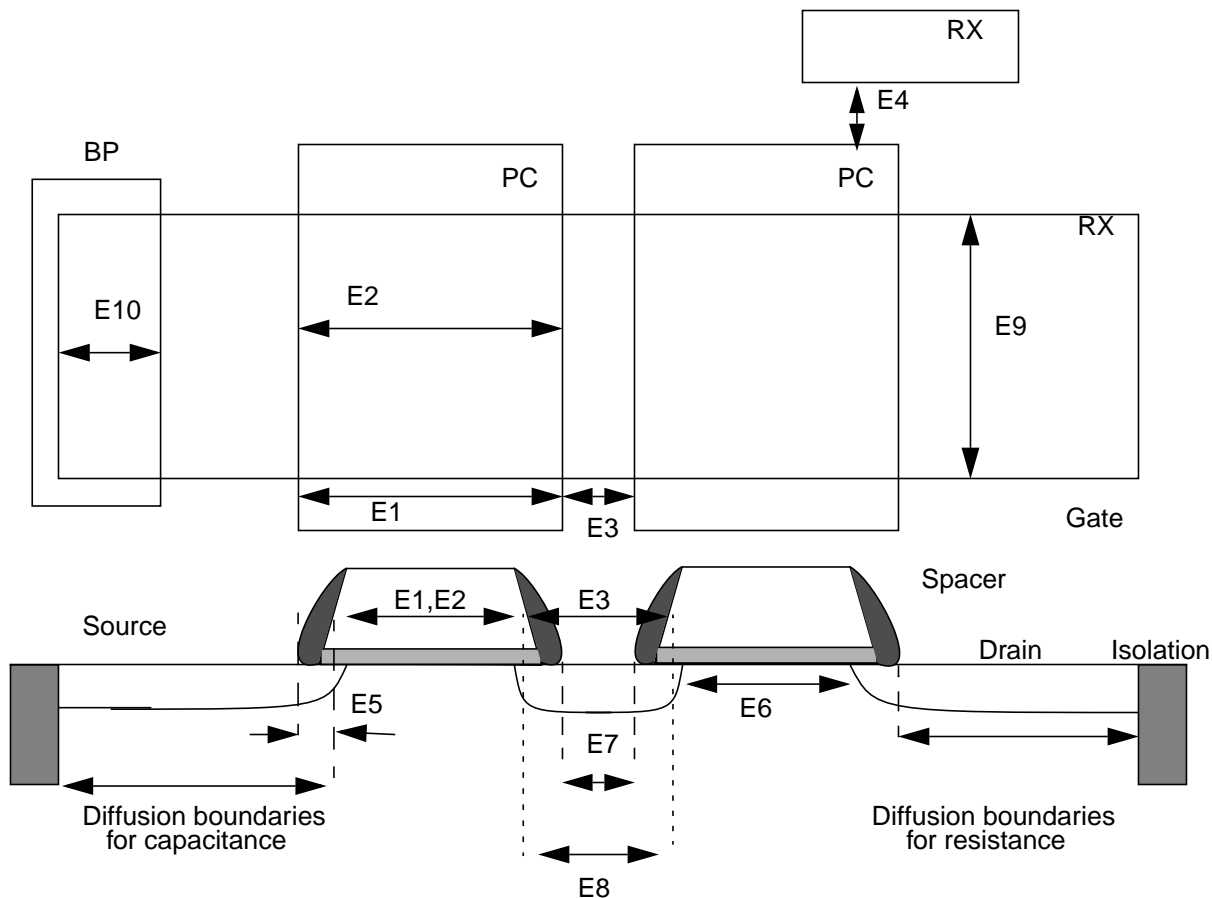


Figure 4-6. Extraction parameters

4.15 Electrical Moat Parameters

By designing a BFMOAT level, the designer may insert a resistive element between different regions of the substrate. This may be useful to reduce the coupling of substrate noise between two regions on the same chip. Table 4-41, “Moat Parameters” indicates how much resistive isolation may be obtained for a given moat width.

For example, if a square region of 500 μm on a side were to be surrounded by a moat 100 μm long, the total substrate resistance between the two regions would be:

Width of moat = 100 μm ; $R_{\text{moat}} = 500,000 \text{ ohm-}\mu\text{m}$

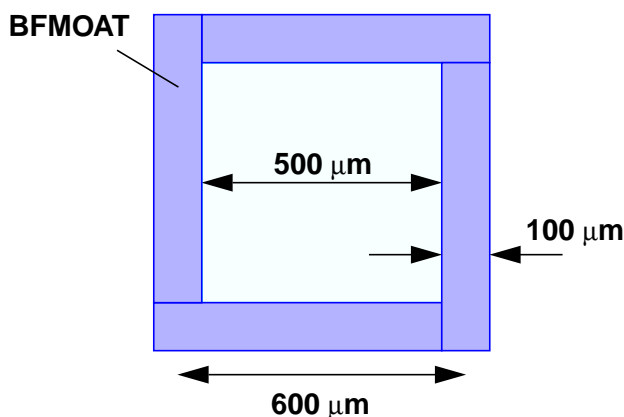
Effective Length of moat = $[500 \mu\text{m} + (100 \mu\text{m} \times 0.56)] \times 4 = 2224 \mu\text{m}$ (corner pieces contribute 0.56 squares to the total length)

Resistance = $500,000 / 2224 = 225 \text{ ohms}$

Table 4-41. Moat Parameters	
Moat length (μm)	Moat resistance (ohm- μm)
10	230,000
20	300,000
30	330,000
50	400,000
100	500,000

The data in Table 4-41, “Moat Parameters” is based on a model of a process using substrate similar to that used in the CMOS 7SF technology. Data for this technology is not yet available.

Figure 4-7. Moat Example





This Page Intentionally Left Blank

4.16 Inductor Models

The BiCMOS8HP technology currently supports symmetric (differential) inductors and standard spiral single layer inductors, AM metal over deep trench (DT) lattice and AM metal over M1 groundplane (M1). The outer dimension for ind ranges from 60.7 μm to 300 μm and from 50 μm to 300 μm for symind. Supported line widths for ind are from 5 μm to 25 μm and from 6.48 μm to 25 μm for symind. Line to line spacing can vary from 3 μm to 5 μm . These geometries yield inductance values ranging from 0.08nH to 35nH for ind and 0.06nH to 23nH for symind. See Table 4-42, on page 297.

The vertical cross section of the standard spiral inductor consists of a metal spiral on the top metal layer (AM) with an underpass to the central spiral at the second metal layer (LY). This underpass is connected to the spiral through vias (AV). The symmetric inductor has crossovers at LY and an optional center tap at MQ. The DT groundplane spiral has a cross hatch of deep trench under it to reduce the capacitance to substrate. The M1 groundplane spiral has a comb shaped M1 shield to reduce the substrate loss.

Note: The inductors have all been modelled assuming final passivation is covering the top of the spirals. If the design is offered with no passivation, then the peak Q that is achieved (and in some cases peak Q frequency and self-resonance frequency) will be slightly higher from the model's predicted value. In general, this increase will be less than 5%.

4.16.1 Inductor Design Considerations

Due to the fact that the inductor is fabricated over a conductive silicon substrate, the actual inductance and quality factor seen in a circuit vary considerably with frequency. At low frequencies, the inductor behaves as a pure inductance with a series resistance (metal resistance). At higher frequencies, however, the inductor is shunted not only by the parasitic capacitance from turn to turn, but by the capacitance that exists between the metal layers and the substrate itself. In this technology the silicon substrate is conductive (11-16 $\Omega\text{-cm}$). This conductive substrate begins to cause power loss in the inductor structure at higher frequencies due to the mentioned capacitance effect. This interplay between the inductance and the parasitic capacitance and resistance causes the quality factor (Q) to rise at low frequencies, peak and then fall off at high frequencies. The peak Q and the frequency at which it falls off will be lower than an equivalent inductor realized in a process utilizing a semi-insulating substrate such as GaAs (all other factors being equal. i.e. metal sheet rho).

Depending on which inductor you choose the point at which Q peaks may vary from approximately 500 MHz to over 40 GHz, with the higher frequency peaks occurring for the lower values of inductance. The single layer spiral inductor is realized over a DT to maximize the self resonant frequency or a M1 comb to maximize Q.

Table 4-42. Inductor Design Specifications

Specification	DT/M1 Inductor (ind)	DT/M1 Inductor (symind)
Inductance (nH)	0.08 to 35	0.06 to 23
Supported Turn Widths (μm)	5 to 25	6.48 to 25
Supported Outer Diameters (μm)	60.7 to 300	50 to 300
Turn-Turn Space (μm)	3 to 5	3 to 5
Number of Turns	1 to filled-in; 1/4 turn increments for standard	1 to filled-in; 1 turn increments for symmetric

4.16.2 Inductor Ground Connection Notes (simulation and layout)

Simulation

Proper connection to the ground node of the spiral inductor during simulation is critically important to achieving accurate simulation results.

The DT version of the spiral inductor has a ground node that must be connected to an ideal AC ground in order to provide accurate simulations. This ideal ground connection does not represent an actual physical connection to the P- substrate underneath the inductor and therefore should not contain series resistance representing the resistance present between the inductor and any adjacent substrate contacts. The requirement for an ideal AC ground represents a limitation of representing a large, distributed spiral with a lumped element circuit.

The M1 groundplane inductor model has an explicit ground connection representing the physical connection to the M1 groundplane. This node should not be connected to an ideal ground as in the DT groundplane case described above. It should be connected to the physical node representing the AC ground potential used to ground the M1. This way, the actual impedance of the ground plane connection can be included in the simulation.

Layout

In order for the ideal AC ground connection to the ground node of the DT inductor to be a valid representation of the physical layout, all substrate contacts must be placed at least 80 μ m from the spiral. This ensures that the resistance between the spiral and the substrate contacts is large enough to decouple the spiral from those substrate contacts.

Additionally, spacing between inductors where magnetic coupling is to be minimized should be no less than one radius of the larger inductor. There is no modeling of magnetic coupling between inductors.

4.16.3 Inductor to Wirebond/C4 Spacing Recommendations

In applications that require the highest possible Q for a given inductor layout, the proximity of the inductor to adjacent metal areas is important. Adjacent metal areas that are tied to an AC ground (DC supplies) will add capacitance in parallel with the inductance, lowering the self resonance. Large planes or closed loops of metal placed close to an inductor will support eddy and loop currents that will lower the peak Q. In addition to the obvious sources of nearby metal in the metal interconnect levels, the orientation of wirebond and C4 pads should also be considered.

A C4 solder ball will actually extend beyond the edge of the LV shape defining it due to its inherently spherical shape. This may cause the C4 ball to end up closer to an inductor than is expected. In addition, an AM wirebond pad may also extend beyond the defining AM shape. Due to these concerns, and C4 “splattering” concerns, it is recommended to maintain a spacing of 110 μ m between C4 solder balls and inductors, or 83 μ m to wirebond pads, to avoid unwanted coupling and power loss. These recommendations are not enforced for inductors since some designs are chip area limited and/or do not require high Q inductors. On these types of designs, it is not necessary to follow the recommendations above.

Please note that a C4 solder ball may also be present when there is no active connection required. This type of C4 ball is defined by the LVDUMMY layer (see Dummy C4 Terminals on page 198). Dummy C4 balls are provided for mechanical rigidity in certain packaging applications.

4.17 Rfline Device Models

The BiCMOS8HP technology currently supports rflines consisting of AM metal over DT lattice. The rfline width can range from 4 μ m to 25 μ m. The length of the line is limited to be within the range from 100 μ m to 1500 μ m. If a longer line is desired, two or more smaller rflines should be connected in series. A true microstrip line (with a low resistance groundplane) is also offered. The rfline, as it is offered, is intended to be used as an inductor with a very low inductance value and a high Q factor.

The vertical cross section of the rfline consists of a metal line on the top metal layer (AM) with a cross hatch of deep trench (DT). The structure sits in a bed of BB (Bipolar Block Level) so that the relatively low resistance PWELL is not under the rfline. No other design levels are currently allowed under the rfline.

4.17.1 Rfline Design Considerations

Table 4-43. Rfline Design Specifications

Specification	Rfline w/DT
Inductance (nH)	0.06 to 2.20
Oxide Area Capacitance (fF/ μ m ²) for 5 levels of metal (M1, M2, MQ, LY, AM)	0.0029
Oxide Fringe Capacitance (fF/ μ m) for 5 levels of metal (M1, M2, MQ, LY, AM)	0.0468
Supported Lengths (μ m)	100 to 1500
Supported Widths (μ m)	4 to 25

4.17.2 Rfline Ground Connection Notes (simulation and layout)

Simulation

Proper connection to the ground node of the rfline during simulation is critically important to achieving accurate simulation results.

The ground node must be connected to an ideal AC ground in order to provide accurate simulations. This ideal ground connection does not represent an actual physical connection to the P- substrate underneath the inductor and therefore should not contain series resistance representing the resistance present between the inductor and any adjacent substrate contacts. The requirement for an ideal AC ground represents a limitation of representing a distributed structure with a lumped element circuit.

Layout

In order for the ideal AC ground connection to the ground node of the rfline to be a valid representation of the physical layout, all substrate contacts must be placed at least 80 μ m from the rfline. This ensures that the resistance between the line and the substrate contacts is large enough to decouple the line from those substrate contacts.

4.17.3 Rfline to Wirebond/C4 Spacing Recommendations

In applications that require the lowest possible coupling for a given rfline layout, the proximity of the rfline to adjacent metal areas is important. Adjacent metal areas that are tied to an AC ground (DC supplies) will add capacitance in parallel with the rfline, increasing the capacitive coupling to ground. Large planes or closed loops of metal placed close to a rfline will support eddy and loop currents that will increase power loss. In addition to the obvious sources of nearby metal in the metal interconnect levels, the orientation of wirebond and C4 pads should also be considered.

A C4 solder ball will actually extend beyond the edge of the LV shape defining it due to its inherently spherical shape. This may cause the C4 ball to end up closer to a rfline than expected. In addition, an AM wirebond pad may also extend beyond the defining AM shape. Due to these concerns, and C4 “splattering” concerns, it is recommended to maintain a spacing of 110 μ m between C4 solder balls and rflines, or 83 μ m to wirebond pads, to avoid unwanted coupling and power loss. These rules are not enforced for rflines since some designs are chip area limited and/or do not require low loss rflines. On these types of designs, it is not necessary to follow the recommendations above.

Please note that a C4 solder ball may also be present when there is no active connection required. This type of C4 ball is defined by the LVDUMMY layer (see “Dummy C4 Terminals” on page 198). Dummy C4 balls are provided for mechanical rigidity in certain packaging applications.

4.18 Capacitive Loading/Transmission Line Effects for Arbitrarily Shaped Interconnects

The above mentioned rfline models (“Rfline Device Models” on page 299) are meant to simulate only straight, isolated metal lines over P- substrate. Many designs will require a comprehensive knowledge of the actual capacitive loading/transmission line effects for metal interconnects that do not fit the restrictive definition required for use of the provided rfline models (bends, Tee’s, embedded lines, crossovers, etc.). In these cases, it would be prudent to characterize the critical interconnects using an e-m solver (such as HP’s Momentum or Sonnet Software’s Sonnet, or one of many other similar software packages).

These types of solvers are optimized for planar multilayer/multiconductor simulations at high frequency. After describing the material properties of the substrate, interlayer dielectrics, and metal levels, a graphical layout is input and Maxwell’s equations are solved for the configuration of interest. S-parameter data over the simulated frequency range is the typical output. From these S-parameters, capacitance, inductance, and resistance may be extracted for use in a Spectre or Hspice netlist, or the S-parameters may be used directly if a linear simulator is being utilized.

In order to make effective use of one of these planar EM simulators, it is necessary to know the required material properties, such as permittivity, permeability, conductivity and loss tangents of the dielectrics and substrate and conductivity of the metal. Additionally, the vertical stack heights of the dielectrics, metal levels and substrate must be known. Table , on page 301 is intended as a summary of the types of inputs required for this type of EM simulation along with some values or suggestions on where to locate them.

Table 4-44. Summary of Inputs for e-m Simulation

Parameter	Value	Source
Dielectric Thickness	varies depending on layers of interest	Figure 4-5 on page 282
Metal Thickness	varies depending on layers of interest	Figure 4-5 on page 282 and Table 4-31, "Conducting Film Thicknesses and Sheet Resistances at 25°C," on page 284
Metal Sheet Resistivity ($\Omega/\text{sq.}$)	varies depending on metal level of interest	Table 4-31, "Conducting Film Thicknesses and Sheet Resistances at 25°C," on page 284
P- Silicon Substrate Conductivity (S/m)	7.41	Bulk resistivity of P- wafers of 13.5 $\Omega\text{-cm}$
P- Silicon Substrate Relativity Permittivity (ϵ_{rsi})	11.9	Property of intrinsic silicon bulk material
SiO_2 Conductivity (S/m)	0.00	nonconductive
SiO_2 Relative Permittivity (ϵ_{rsiO2})	4.10	BiCMOS8HP Technology Description
SiO_2 Dielectric Loss Tangent	0.00-0.001	Based upon comparison between simulation and measurement. (typically set to 0.00).
Polyimide Passivation Layer Conductivity (S/m)	0.00	nonconductive
Polyimide Passivation Layer Permittivity (ϵ_{poly})	3.4	BiCMOS8HP Technology Description
Polyimide Passivation Layer Loss Tangent	0.00-0.001	Based upon comparison between simulation and measurement. (typically set to 0.00).
All Dielectrics Relative Permeability (μ_r)	1.00	No magnetic materials in technology cross section
All Dielectrics Magnetic Loss Tangent	0.00	N/A

With the above information, simulations can be performed to characterize the characteristics of arbitrarily shaped pieces of interconnect metallization. If care is taken in setting up the simulation (including a thorough understanding of the limitations of your particular simulator), accurate results can be expected from any of the planar EM simulators on the market.

4.19 Bondpad Models

A bondpad model is offered that simulates the loading effect of an AM bondpad over an M1 groundplane or an NS groundplane.

4.19.1 Bondpad Design Considerations

Table 4-45. Bondpad Design Specifications

Specification	Bondpad over M1	Bondpad over NS
Oxide Area Capacitance (fF/ μm^2) for 5 levels of metal (M1, M2, MQ, LY, AM)	0.0032	0.0030
Oxide Fringe Capacitance (fF/ μm) for 5 levels of metal (M1, M2, MQ, LY, AM)	0.0336	0.0327

4.19.2 Floating Bondpad Concerns

Floating terminal pad design rules 908 and 953 require that a connection be made between bond/C4 pads and silicon. The purpose of these rules is to provide a **DC** connection between the bondpad and silicon in order to bleed off excess charge to the wafer substrate during wafer processing. If a bondpad is connected directly to a MIM capacitor, and it does not have a **DC** connection to the substrate, the MIM dielectric is very likely to be damaged during processing. So, always provide a **DC** connection to ground from any terminal pad to avoid charging induced damage during wafer processing.

4.20 Shielded Transmission Line (T-line) Interconnect Models

Shielded Transmission Line (T-line) interconnect models are offered.

4.20.1 Purpose

The offered Transmission Line devices refer to a definite set of parameterized shielded interconnect structures, which enable high predictability of their electrical behavior with high accuracy, and allow to predict parasitics effects due to interconnect both on early (schematic) design phase and at the post-layout stage. The T-lines enable users to design electromagnetic closed environment structures - where the line impedance, attenuation and phase shift are well controlled and known in advance. The T-lines are intended to be used both in microwave (frequency domain) designs as well as in high speed digital (time domain) designs. T-lines may be used for the design and modelling of all critical interconnect lines of a given design, as part of a comprehensive design methodology described below. The supported models are designed to cover the whole signal bandwidth from DC till 200[GHz] (Ft of BiCMOS8HP SiGe transistors) - as verified by VNA measurements up to 110[GHz] (for singlewire) and EM solver data up to 200[GHz]. Spectre and Hspice simulators are currently supported.

4.20.2 Supported Topologies

Current release includes models for the following (straight-wire) T-line topologies:

- single wire microstrip transmission line, thereafter referred to as TL1 (see Figure 4-8 and Figure 4-9)
- two coupled wires microstrip transmission line, thereafter referred to as TL2 (see Figure 4-10 and Figure 4-11).
- single wire coplanar waveguide ("singlecpw"), thereafter referred to as CPW1 (see Figure 4-12)
- two wires coplanar waveguide ("coupledcpw"), thereafter referred to as CPW2 (see Figure 4-13)

All models are symmetrical, as is shown on Figures 4-8, 4-9, 4-10, 4-11, 66, and 67.

4.20.3 Interconnect-Aware Design Methodology

The suggested stages of T-line models usage in the design flow are as follows.

- Based on the floor plan, major critical lines are identified (longer high speed clock distribution lines, high speed busses, sensitive supply lines, other longer high speed lines with tight spec requirements). In digital designs, the number of critical lines is a very small fraction of the number of lines. Generally speaking, critical lines in a given design are lines for which inductance related effects are not negligible, considering the given design requirements. A simple worst case criteria for this, which is based on our design experience in high speed digital design, is:

$$\text{risetime} < 10 * \text{time of flight} = 10 * \text{line length} / \text{propagation speed}$$

For microstrip and coplanar lines, the propagation speed can be assumed to be the speed of light in vacuum divided by the square root of the silicon oxide relative dielectric constant (4.1).

In some other cases, lines for which the capacitance/resistance has to be determined in the schematic design phase can also be modelled as T-lines. Though in the literature the above equation sometimes appears with a factor of 2 rather than 10, we have found in practice that signal integrity considerations in the higher harmonics and the fact that some lines run close to the silicon substrate with poor metallic return paths (slow wave effects) give rise to this higher worst case factor of 10. Moreover, in RF and microwave designs the threshold is even lower for choosing to model a given line as a T-line - since the requirement is often to have an exact phase difference across the line - such as in RF stub length, or to have the correct impedance of the short line. If we therefore use for RF designs a “0.5/(center frequency)” instead of “risetime” in the equation above, we will not be covering the worst case. The final decision therefore depends on the design niche and requirements.

For each critical line, the T-line topology and metal layers are specified; length and width values are estimated, based on possible floor plan constraints and required design specifications (impedance, minimal attenuation, minimal driver loading...). T-line geometries are DRC correct by construction.

- The defined T-line models are simulated as part of a design on the schematic (or higher) levels.
- In the layout phase, an LVS clean T-line layout view is generated as part of the Cadence Pcell. If all the lines with significant inductance effects are modelled as T-lines, then accurate RC extraction is sufficient for the rest of the wires for obtaining a reliable on-chip interconnect post layout simulation.

Post-layout simulation procedure and detailed discussion of the proposed design flow can be found in the user guide.

4.20.4 Transmission Line Models

The schematic level models can be used at schematic or higher level design phases, i.e. behavioral and mixed mode.

All offered models are suitable for time domain simulations, including both periodic steady state (pss) and true transient simulations, as well as frequency domain simulations (AC and S-parameters).

The offered modeling approach is correct regardless of whether impedance matching is used or not.

The models offered in the current release support usage of the Cadence Spectre, SpectreS and HspiceS simulators.

The new TL1 of this release includes an “impedance calculator” option, which receives a user input frequency (within the T-line bandwidth) and outputs the impedance (real and imaginary parts), attenuation (alpha) and phase shift (beta) all in the given frequency.

The TL2 model is intended mainly for differential designs, but the new model of this release has the same accuracy in both odd mode and even mode of operation.

While the TL2 and CPW2 models are intended primarily for differential designs, they can also be used in non-differential designs in order to model the electric and magnetic crosstalk between adjacent lines.

The new models of this release accept a variable bandwidth as user input (up to 200[GHz]). Lower bandwidth means a larger maximal length for one T-line device - the maximal T-line length is now limited to no more than a quarter of shortest wavelength in the given bandwidth. For longer lines, several T-line devices can be connected in series without losing accuracy. This change gives lower simulation time.

4.20.4.1 TL1 Model

The TL1 model consists of a metal signal line above a metallic return path, with optional side shielding. All legal metal level combinations as signal and shielding layers are permitted. This structure is shown in Figure 4-8 and Figure 4-9. Side shields are connected to the bottom shield by periodic vias. Information on the TL1 model parameters are given by pushing the “Info” button on the model user interface. The model considers the finite bottom shield width, and does not assume infinite shielding. This finite width depends on whether side shielding exists or not: If shields exist then $W_g = W + 2*S + 2*W_s$ otherwise $W_g = W + 2*h + 2*th$. The model considers the effect of the special slots generated by the layout view PCell on copper lines.

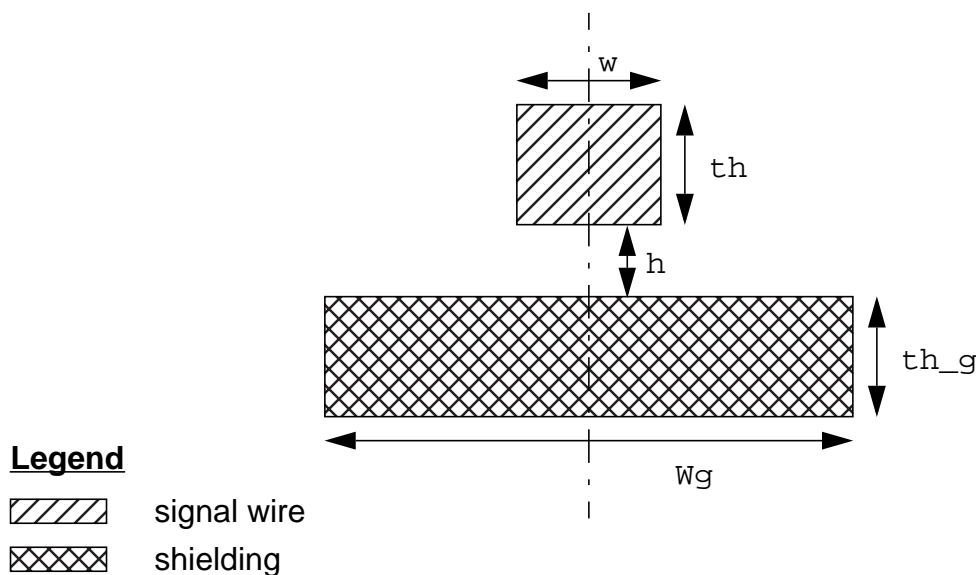


Figure 4-8. TL1 with width bottom shielding only: cross-section.

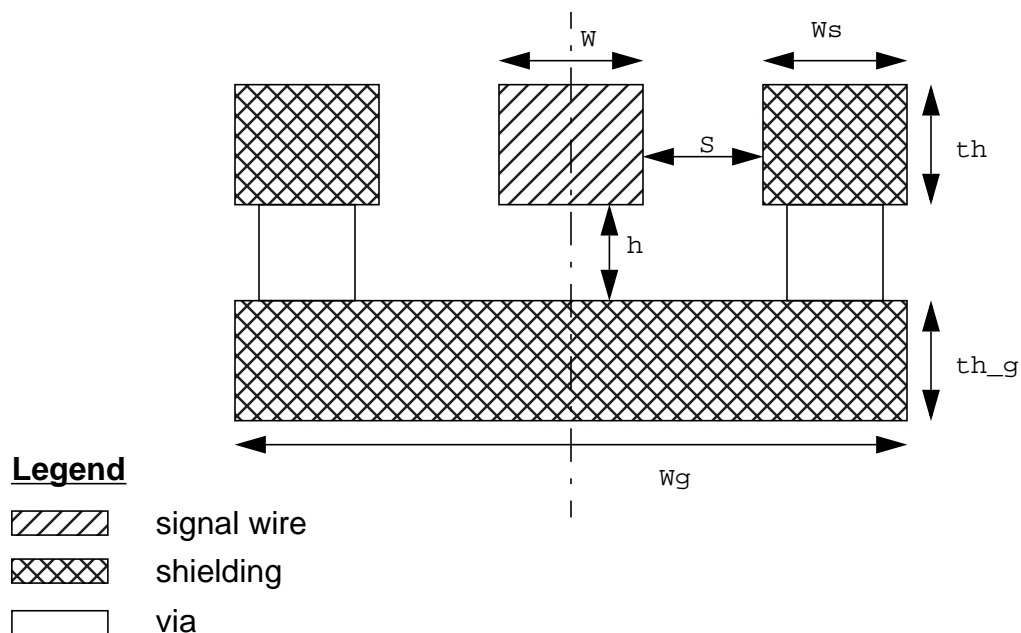


Figure 4-9. TL1 with both bottom and side shielding: cross-section

The single transmission line model describes the frequency dependent (complex) impedance, attenuation and phase shift in the full bandwidth from DC till the transistor F_t (200[GHz]). The model is a multi-segment passive ladder model (RLC filter network) which considers skin and proximity effects. The resistance per unit length includes the signal wire resistance and the resistance of the shielding return path, with their frequency dependence. The losses due to possible currents in the silicon substrate are effectively eliminated by the use of the bottom shield layer.

4.20.4.2 TL2 Model

The TL2 structure is two identical metal signal lines above a metallic return path, with optional side shielding. All legal metal level combinations as signal and shielding layers are permitted. This structure is given in Figure 4-10 and Figure 4-11, on page 307. Model parameters are described by pushing the “Info” button.

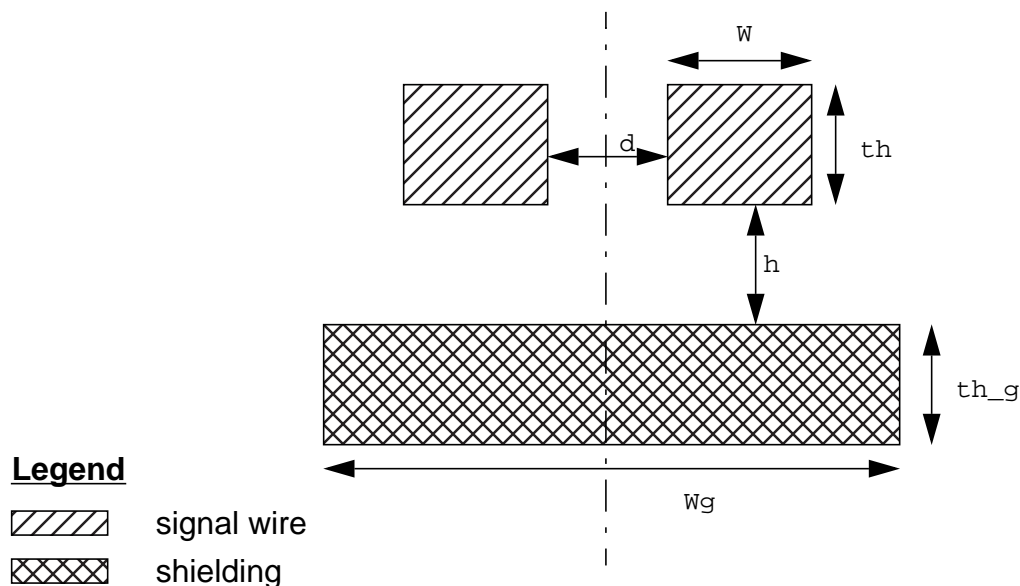


Figure 4-10. TL2 with bottom shielding only: cross section

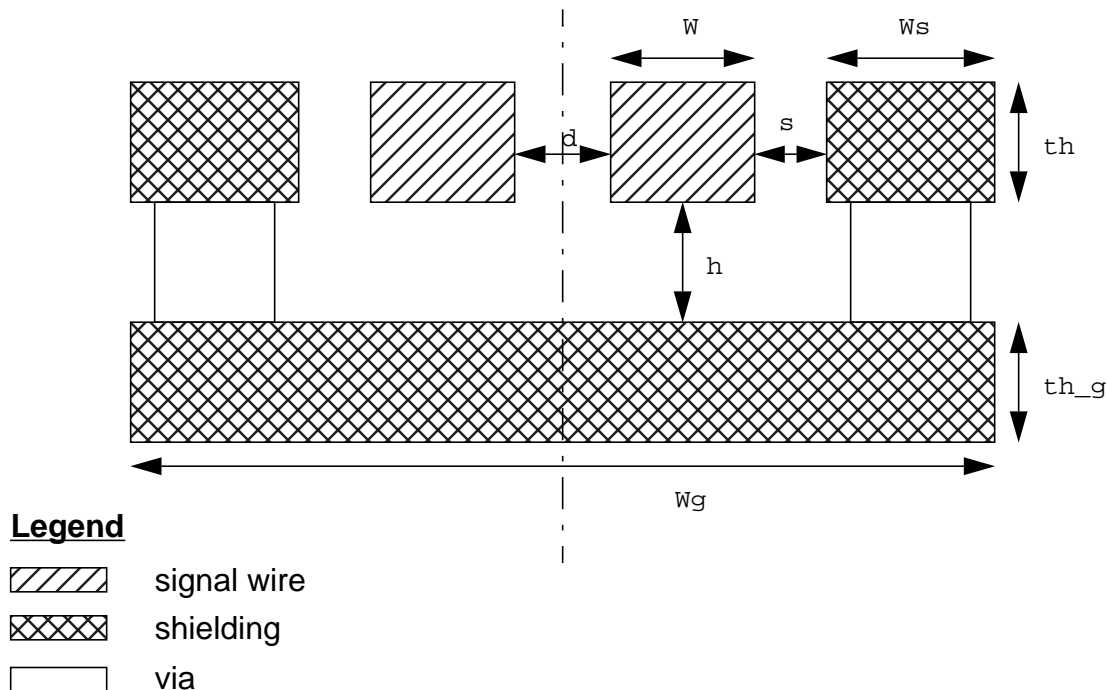


Figure 4-11. TL2 with both bottom and side shielding: cross-section

The TL2 is a passive ladder model which includes capacitance, resistance, inductance, cross capacitance, and mutual inductance per unit length of the two coupled signal lines above the common shielding return

path. The model considers the finite bottom shield width, and does not assume infinite shielding. This finite width depends on whether side shielding exists or not: If shields exist then $W_g = d + 2*W + 2*S + 2*W_s$ otherwise $W_g = d + 2*W + 2*h + 2*th$. The model considers the effect of the special slots generated by the layout view PCell on copper lines.

The model describes the frequency dependent (complex) impedance, attenuation and phase shift in the full bandwidth from DC till 200[GHz] in all modes of operation (even and odd). The model is implemented by a multi-segment RLC filter network + dependent sources and is designed and tested to be passive by construction. The losses due to possible currents in the silicon substrate are effectively screened by the use of the bottom shield layer.

The model describes accurately the full electric and magnetic crosstalk between the two signal lines, in all modes of signal propagation across the lines (odd mode, even mode and single mode, defined in section 4.20.5, "Transmission Line Geometry Design Considerations" on page 310. This means that the model can also be used in cases where common mode signal exists, or even in non-differential designs in order to model the electric and magnetic crosstalk between adjacent lines. Another correct usage is in high bandwidth transformer design between the two signal lines.

4.20.4.3 CPW1 Model

The CPW1 model consists of a metal signal line above a silicon substrate, with side shielding. This structure is shown in Figure 4-12. The CPW1 device can be at any legal metal level.

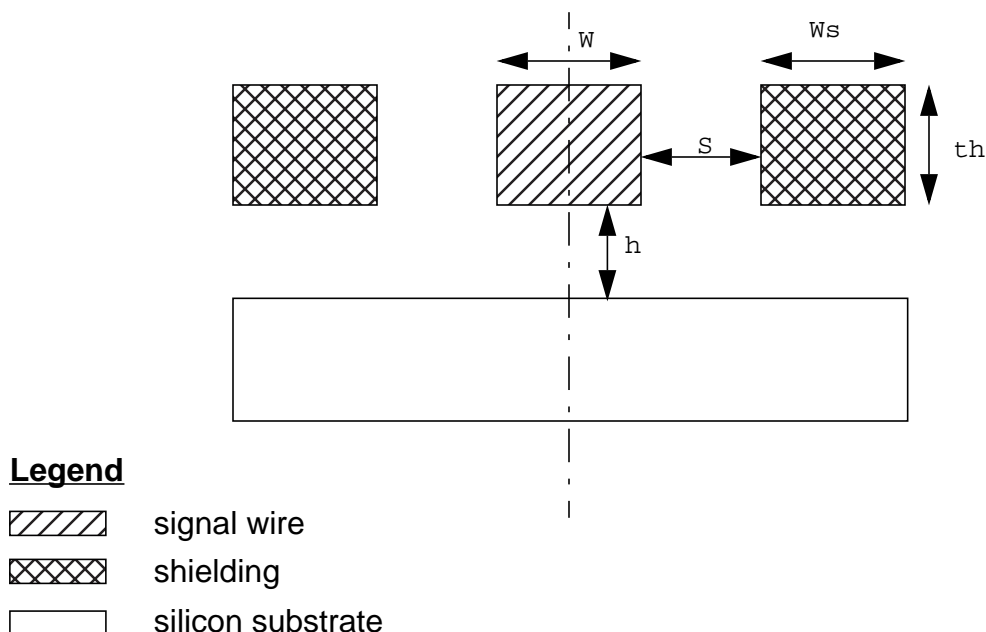


Figure 4-12. CPW1 with side shielding: cross-section

The single wire coplanar waveguide model is a passive ladder model. The inductance and the resistance per unit length both depend on frequency due to skin and proximity effects. The resistance per unit length includes the signal wire resistance and the resistance of the shielding return path, with their frequency dependence. Dielectric losses in the oxide layer are negligible and are therefore neglected. The losses due to possible currents in the silicon substrate are incorporated into model.

4.20.4.4 CPW2 Model

The CPW2 structure is two identical metal signal lines above a silicon substrate, with side shielding. This structure is given in Figure 4-13. The CPW2 device can be at any legal metal level.

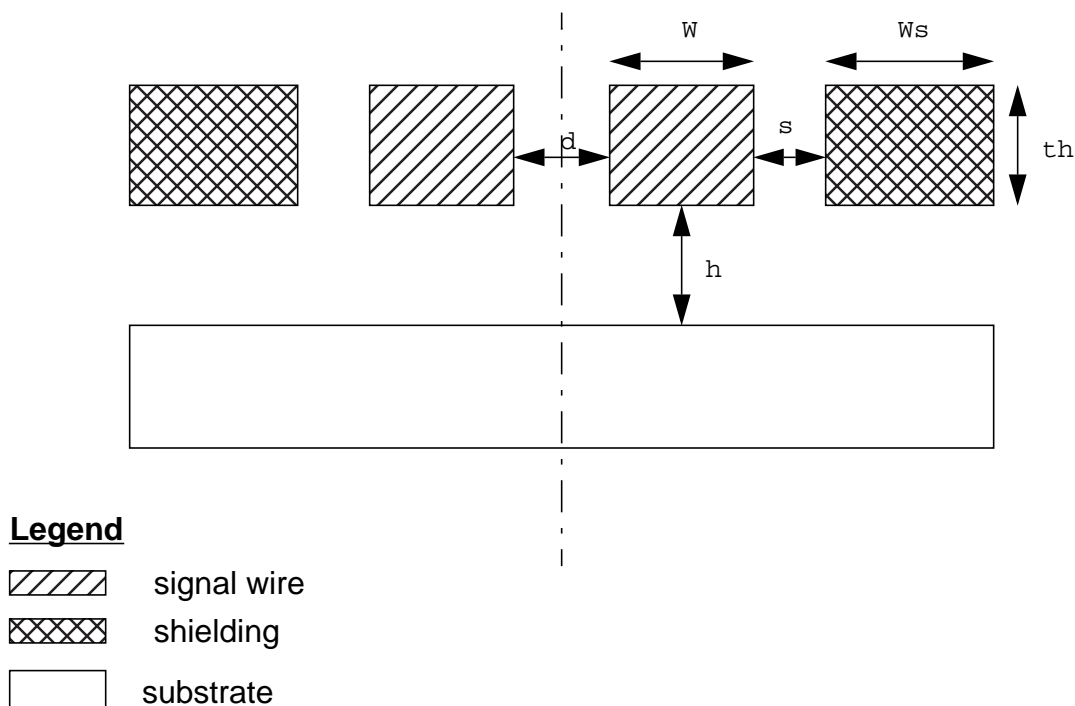


Figure 4-13. CPW2 with side shielding: cross-section

The CPW2 is a passive ladder model which includes capacitance, resistance, inductance, cross capacitance, and mutual inductance per unit length of the two coupled signal lines with the side shielding return path.

The model is frequency dependent, as specified below. The resistance per unit length includes only the signal wire resistance without the shielding return path resistance. This condition is exact for odd mode (differential) signals, and still serves as good approximation for other modes of signal propagation. Dielectric losses in the oxide layer are negligible and are therefore neglected. The losses due to possible currents in the silicon substrate are incorporated into model.

The model describes accurately the full electric and magnetic crosstalk between the two signal lines, in all modes of signal propagation across the lines (odd mode, even mode and single mode).

4.20.5 Transmission Line Geometry Design Considerations

There are some limitations on the geometry of interconnect structures supported by interconnect transmission line models. They are due to technology layout rules (DRC) as well as model limitations. We mention here just a few of them. For further details, please refer to section 3.7, “CA, Metals and Via Layout Rules” on page 96 in this manual.

Table 4-46. Transmission Line Design Specifications

Specification	Singlewire and Coupledwires Singlecpw and Coupledcpw
Supported Mx (x=2,3,4) Signal Line Widths (μm)	0.2 to 50
Supported MQ Signal Line Widths (μm)	0.4 to 50
Supported LY Signal Line Widths (μm)	1.52 and higher
Supported AM Signal Line Widths (μm)	2 and higher
Supported Lengths (μm)	up to $180[\mu\text{m}] * (200[\text{GHz}] / \text{input bandwidth})$

Note: If lines longer than supported lengths are required, they can be broken into smaller pieces and connected in series.

- The distance between signal and side shielding in a singlewire/singlecpw device layout (s) must be less than or equal to $20\mu\text{m}$
- The distance between signal and side shielding in a coupledwire/coupledcpw device layout (s) must be less than or equal to $20\mu\text{m}$
- The distance between two signal lines in a coupledwire/coupledcpw device layout (d) must be less than or equal to $20\mu\text{m}$
- When transmission lines are in close proximity to each other it is required to limit the minimum distance between their bottom ground shields to the minimum spacing allowed by layout rules for that metal level. However, the local pattern density rules on the Mx metal levels (x=1,2,3,4 or Q) must also be met, which may require adjacent transmission lines to be spaced further apart. Unifying the bottom shields of two adjacent T-lines (if possible by DRC rules) results in some modeling error in the lower frequencies (this error becomes negligible when the skin depth is much smaller than the bottom shield width).

4.20.6 T-line Ground Connection Guidelines

Proper AC grounding of the transmission line shielding during simulation is critical for achieving accurate simulation results. Proper grounding means two things:

- 1) The T-line shield has the correct reference potential with respect to the signal line(s) - electrical shielding.
- 2) The T-line shield carries the return current, so that the sum of currents in the T-line cross section is zero - magnetic shielding.

The first condition is essential for obtaining the correct T-line capacitive behavior (Y element) while the second condition is essential for obtaining the T-line inductive + resistive behavior (Z element). In actual designs, it is not always trivial to achieve these two conditions. Connecting the T-line shielding to an ideal ground in the schematics may therefore not describe the reality (though in most cases it is still a good approximation).

The T-line shielding should therefore be connected to the reference line (ground or supply) both on the near end and the far end. The near end grounding point should be a clean AC ground close as possible to the excitation signal, and the far end grounding point should be a clean AC ground close as possible to the receiving load. Imperfect grounding is, in most cases, better than having no grounding at all. Grounding at the near end is a must - and is more important than grounding at the far end.

In high bandwidth designs (tens of GHz) it is customary to use ground planes. Unifying the T-line shield with the ground plane is not a modeling error, provided that the base frequency resulting skin depth is much smaller than the T-line bottom shielding width. In other cases, it is better to keep the given limited bottom shield width.

The T-line models are one terminal shield models (one connection point to the shield line). This means that the shield resistance is “folded” into the signal line resistance - which means that the DC IR drop across the T-line signal line has some simulated error. This error is not significant in most design cases, except some cases (such as in DAC output). The model assumes that the shield carries the return current. Two terminal shield models are currently being developed to cover for these exceptional design cases.

This page intentionally left blank

4.21 Distributed Passive (DP) Devices

Distributed passive (DP) devices (compatible to TL1 or singlewire) are offered.

4.21.1 Purpose

The BiCMOS8HP kit currently supports multiple distributed passive models each supporting several metal combinations for signal and return paths. All the models are designed for microstrip configuration although side-shields option is available for most of the devices. Large metal planes such as shields and low impedance lines on copper layer in the layout PCell are cheesed or slotted within the guidelines set by manufacturing. The design methodology provides accurate control of the characteristic impedance (Z_0) and also isolates the signal line from silicon substrate. The supported distributed passive devices are designed to cover a bandwidth of DC till 120[GHz]. The models have been verified using full-wave EM solvers up to 120[GHz] and using VNA measurement up to 110[GHz]. Spectre and Hspice simulators are currently supported.

4.21.2 Distributed Passive Device List

The current design kit release includes models for the following DP devices:

- Bend junction discontinuity, thereafter referred to as bend.
- Tee junction discontinuity, thereafter referred to as tee.
- Step junction discontinuity, thereafter referred to as step.
- Y junction discontinuity, thereafter referred to as yjunction.
- Open stub, thereafter referred to as open.
- Short stub, thereafter referred to as short.
- Radial stub thereafter referred to as radialstub.
- Gap device, which has two transmission lines separated by a user controlled gap/spacing, thereafter referred to as gap.
- Taper device, which is an asymmetrical transmission line of two unequal widths, thereafter referred to as taper.
- Meander line which models the straight transmission line segments with bends for space optimization, thereafter referred to as meanderline1 (with one meander) and meanderline2 (with two meanders).
- Branch-line couplers are useful in signal coupling and isolation. Meander lines are used to construct this device to reduce the layout area for longer waves. This results in three variants of the Branch couplers, which thereafter are referred to as branchcoupler0, branchcoupler1, and branchcoupler2.
- Wilkinson power dividers provide users to split a signal into two ports or to combine two signals into one port. Similar to the Branch couplers, the meander lines are used and there three variants, which thereafter are referred to as powerdivider0, powerdivider1, and powerdivider2.
- Lange couplers, which are useful for broadband signal coupling, thereafter referred to as langecoupler.

- Rat Race hybrids, which are useful in signal coupling and isolation, as well as single-end to differential conversion. The devices thereafter are referred to as ratracehybrid.

4.21.3 Device Descriptions and Design Considerations

The following simulation and layout attributes of the DP models are to be considered:

- The distributed passive devices discussed previously are supported to a variety of metal combinations after careful consideration of insertion loss and design space minimization.
- All offered models are suitable for time domain simulations and frequency domain simulations.
- The offered modeling approach is correct regardless of whether closed-form expressions are used for modeling or curve-fitting.
- The models currently support Spectre and Hspice simulators.
- Most of the devices have an “impedance calculator” callback function that provides the user with the high frequency characteristic impedance of the ports/terminals for the device. The impedance calculator accounts for side-shields if they are turned on.
- For asymmetrical devices, the impedance calculator provides individual port/terminal impedances at each terminal depending on the cross-section dimension at the terminal.
- For the layout, a DRC clean layout view is generated. Specific layers are used for LVS to block the vendor parasitic extraction tools to extract the Pcells and thus avoid double-counting of parasitics.
- It is recommended that the individual bottom shields of the passive devices that are used in larger circuits be connected to a global/system ground and tied to the silicon substrate via substrate contacts to minimize spurious capacitive and inductive effects.

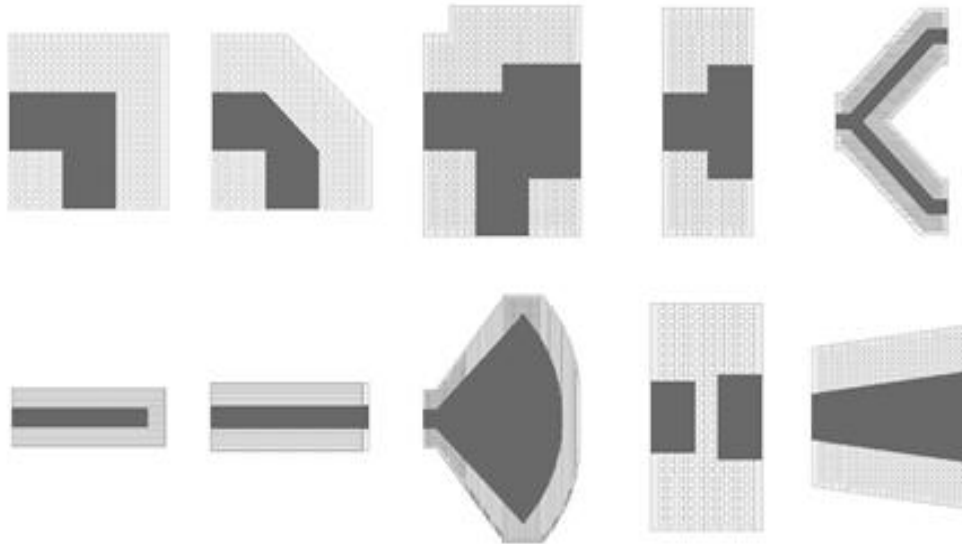


Figure 4-14. Layout shapes (left to right, top to bottom) of bend, bend with miter, tee, step, yjunction, open, short, radialstub, gap and taper.

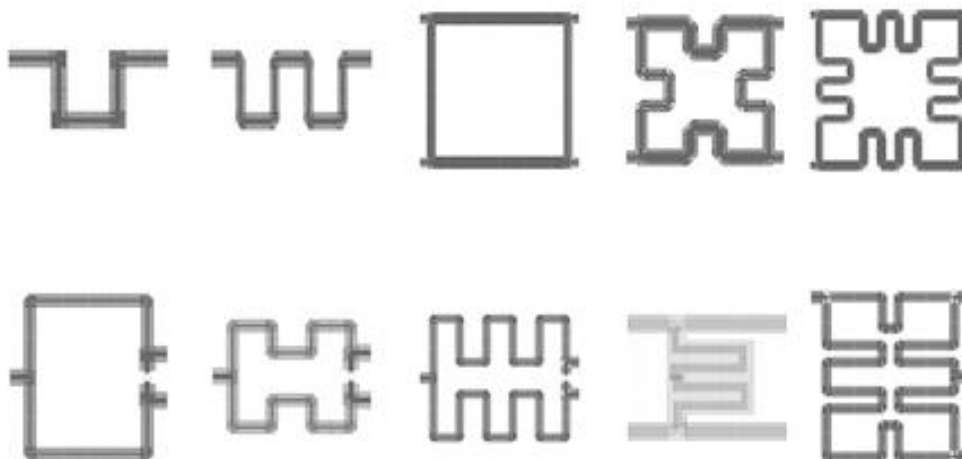


Figure 4-15. Layout shapes (left to right, top to bottom) of meanderline1, meanderline2, branchcoupler0, branchcoupler1, branchcoupler2, powerdivider0, powerdivider1, powerdivider2, langecoupler, ratracehybrid

4.21.3.1 bend

Purpose

The offered bend junction discontinuity devices refer to a 90 degree bend in the interconnection transmission line segments. The widths of the segments are usually kept the same before and after the bend. Such junctions are encountered in the RF/microwave/analog design where two orthogonal transmission lines join together. The models enable designers to precisely evaluate the performance of the component from DC up to 120[GHz].

bend Geometry Design Considerations

The bend junction models support all 3 metal stacks (nlev=5, 6, and 7) with all possible signal/return metal combinations. The models are valid over a large range of metal widths, spacing, and metal combinations with the following geometrical limitations:

1. Model supports signal metal width range from
 - a. 4 μm to 50 μm for the cases with AM as the signal metal
 - b. 1.52 μm to 50 μm for the cases with LY as the signal metal
 - c. 0.4 μm to 20 μm for the cases with MQ as the signal metal
 - d. 0.2 μm to 20 μm for the cases with Mx (x=4, 3, 2) as the signal metal
2. Model supports the spacing between signal metal and the side shields from 4 μm to 20 μm for signal on AM, 1.52 μm to 20 μm for signal on LY, 0.4 μm to 20 μm for signal on MQ, and 0.2 μm to 20 μm for signal on Mx (x=4, 3, 2).
3. The length of the bend varies with the width of the signal metal and the selection of signal and bottom ground shield metals.

4.21.3.2 tee

Purpose

The offered tee junction discontinuity device refers to a three-way junction for electrical connection, which may contain steps in width in either or all of sides of the junction. Such junctions are encountered in the RF/microwave/analog design where multiple different transmission lines need to be connected, usually of different widths. Directional couplers, matching networks, filters, and baluns are some of the examples where such discontinuities are present. The models enable designers to precisely evaluate the performance of the component from DC up to 120[GHz].

tee Geometry Design Considerations

The tee junction models are valid over a large range of metal widths, spacing, and metal combinations with the following limitations:

1. Present model release supports all 3 metal stacks (nlev=5, 6, and 7) with AM as signal path. A selection in return planes is provided depending on the metal stack (nlev) selected. The following return planes (bottom ground shield) are possible: (i) MQ or M2 for nlev=5 (5-metal stack), (ii) MQ or M3 for nlev=6 (6-metal stack), and (iii) MQ or M4 for nlev=7 (7-metal stack).
2. Model supports signal metal width from 4 μm to 50 μm .

3. Model supports the spacing between signal metal and the side shields from 4 μ m to 20 μ m.
4. The length of the tee varies with the width of the signal metal and the selection of signal and bottom ground shield metals.

4.21.3.3 step

Purpose

The offered step junction discontinuity device refers to a junction with a step in widths. Such junctions are encountered in the RF/microwave/analog design where two different transmission lines need to be connected, usually of different widths. Directional couplers, filters, and baluns are some of the examples where such discontinuities are present. The models enable designers to precisely evaluate the performance of the component from DC up to 120[GHz].

step Geometry Design Considerations

The step junction models are valid over a large range of metal widths, spacing, and metal combinations with the following limitations:

1. Present model release supports all 3 metal stacks (nlev=5, 6, and 7) with AM as signal path. A selection in return planes is provided depending on the metal stack selected. The following return planes (bottom ground shield) are possible: (i) MQ or M2 for nlev=5 (5-metal stack), (ii) MQ or M3 for nlev=6 (6-metal stack), and (iii) MQ or M4 for nlev=7 (7-metal stack).
2. Model supports signal metal width of 4 μ m to 50 μ m.
3. Model supports the spacing between signal metal and the side shields from 4 μ m to 20 μ m.
4. The total length of the step junction is 20 μ m.

4.21.3.4 yjunction

Purpose

The offered y-junction device refers to a three-way junction for electrical connection. Such junctions are encountered in the RF/microwave/analog design where multiple different transmission lines need to be connected, usually of different widths. Power dividers, baluns, and couplers are some of the examples where y-junctions can be present. The models enable designers to precisely evaluate the performance of the component from DC up to 120[GHz].

yjunction Geometry Design Considerations

The yjunction models are valid over a large range of metal widths, spacing, and metal combinations with the following limitations:

1. Present model release supports all 3 metal stacks (nlev=5, 6, and 7) with AM as signal path. A selection in return planes is provided depending on the metal stack selected. The following return planes (bottom ground shield) are possible: (i) MQ or M2 for nlev=5 (5-metal stack), (ii) MQ or M3 for nlev=6 (6-metal stack), and (iii) MQ or M4 for nlev=7 (7-metal stack).
2. Model supports signal metal width of 4 μ m to 50 μ m.
3. Model supports the spacing between signal metal and the side shields from 4 μ m to 20 μ m.
4. The separation between the two split arms can vary continuously from 5 μ m to 200 μ m.
5. The two y-arms are of the same width. Thus the user is required to input only two width values (w1 and

w2).

4.21.3.5 open

Purpose

The offered open stub device refers to one-port transmission line with its other end open circuited or left un-terminated. Such devices are very useful in RF/microwave/millimeter wave designs for impedance/admittance matching. The device finds applications in both shunt and series connection with other circuitry. The models enable designers to precisely evaluate the performance of the component from DC up to 120[GHz].

open Geometry Design Considerations

The open stub models are valid over a large range of metal widths, spacing, and metal combinations with the following limitations:

1. Present model release supports all 3 metal stacks (nlev=5, 6, and 7) with AM as signal path. A selection in return planes is provided depending on the metal stack selected. The following return planes (bottom ground shield) are possible: (i) MQ or M2 for nlev=5 (5-metal stack), (ii) MQ or M3 for nlev=6 (6-metal stack), and (iii) MQ or M4 for nlev=7 (7-metal stack).
2. Model supports signal metal width of 4 μm to 50 μm .
3. Model supports the spacing between signal metal and the side shields from 4 μm to 20 μm .

4.21.3.6 short

Purpose

The offered short stub device refers to a one-port transmission line with its other end short circuited to the bottom and side-shields. Such stubs are very useful in RF/microwave/millimeter wave designs for impedance or admittance matching. The models enable designers to precisely evaluate the performance of the component from DC up to 120[GHz].

short Geometry Design Considerations

The short stub models are valid over a large range of metal widths, spacing, and metal combinations with the following limitations:

1. Present model release supports all 3 metal stacks (nlev=5, 6, and 7) with AM as signal path. A selection in return planes is provided depending on the metal stack selected. The following return planes (bottom ground shield) are possible: (i) MQ or M2 for nlev=5 (5-metal stack), (ii) MQ or M3 for nlev=6 (6-metal stack), and (iii) MQ or M4 for nlev=7 (7-metal stack).
2. Model supports signal metal width of 4 μm to 50 μm .
3. Model supports the spacing between signal metal and the side shields from 4 μm to 20 μm .

4.21.3.7 radialstub

Purpose

The offered radial stub device refers to a one-port transmission line with its other end open circuited or un-terminated. It consists of a flared signal region with a bottom shield, which provides electrical reference and isolates the signal from silicon substrate. A radial stub finds many applications in circuit design, particularly as a

broad-band capacitor (RF matching), or as an ac short for isolating RF from DC. The radial stub, unlike the straight line open-stub, provides a stable capacitance value over its entire bandwidth. The design parameters for the radial stub, radius (r), input signal width (w), angle (θ), determine the capacitance and/or self-resonance frequency of the stub.

radialstub Geometrical Design Considerations

The radial stub models are valid over a large range of metal widths, side-shield spacing, and metal combinations with the following limitations:

1. Present model release supports all 3 metal stacks ($nlev=5, 6$, and 7) with AM as signal path. A selection in return planes is provided depending on the metal stack selected. The following return planes (bottom ground shield) are possible: (i) MQ or M2 for $nlev=5$ (5-metal stack), (ii) MQ or M3 for $nlev=6$ (6-metal stack), and (iii) MQ or M4 for $nlev=7$ (7-metal stack).
2. Model supports signal metal width from $4\mu m$ to $50\mu m$ at 45-degree, 60-degree and 90-degree angles.
3. Model has a minimum and maximum radial length of $100\mu m$ and $600\mu m$ respectively.
4. The model also provides provision for connecting to a device with side-shields. However, the radial stub does not itself have any side shields. The provision is for terminating the side-shields of the input line and for providing smooth transition for current.

4.21.3.8 gap

Purpose

The offered gap discontinuity devices refer to two sections of transmission lines that are separated by a user-defined gap or spacing. The gap provides capacitive coupling between the two lines. Such devices are useful for ac coupling in active circuits, matching networks, series/shunt capacitive loading especially useful in the RF/mmWave design. The models enable designers to precisely evaluate the performance of the component from DC up to $120[GHz]$.

gap Geometrical Design Considerations

The gap models are valid over a large range of metal widths, spacing, and metal combinations with the following limitations:

1. Present model release supports all 3 metal stacks ($nlev=5, 6$, and 7) with AM as signal path. A selection in return planes is provided depending on the metal stack selected. The following return planes (bottom ground shield) are possible: (i) MQ or M2 for $nlev=5$ (5-metal stack), (ii) MQ or M3 for $nlev=6$ (6-metal stack), and (iii) MQ or M4 for $nlev=7$ (7-metal stack).
2. Model supports the spacing between signal metal and the side shields from $4\mu m$ to $20\mu m$.
3. The widths of the two lines can be different and can vary continuously between $4\mu m$ and $50\mu m$.
4. The total length of the gap device is fixed to $20\mu m$.
5. The gap length can continuously vary between $4\mu m$ and $13\mu m$.

4.21.3.9 taper

Purpose

The offered taper device refer to a set of parameterized shielded interconnect structures that tapered in width. A taper device enables user to connect two metal wires of largely different widths and over a large bandwidth. Macroscopically, a taper can be thought of as a low loss step device with broad bandwidth.

Tapers find applications in many impedance matching networks, signal width transitions with low loss and broad bandwidth (based on the theory of multiple reflections). The models enable designers to precisely evaluate the performance of the component from DC up to 120[GHz].

taper Geometrical Design Considerations

The taper models are valid over a large range of metal widths, spacing, and metal combinations with the following limitations:

1. Present model release supports all 3 metal stacks (nlev=5, 6, and 7) with AM as signal path. A selection in return planes is provided depending on the metal stack selected. The following return planes (bottom ground shield) are possible: (i) MQ or M2 for nlev=5 (5-metal stack), (ii) MQ or M3 for nlev=6 (6-metal stack), and (iii) MQ or M4 for nlev=7 (7-metal stack).
2. Model supports signal metal width range from 4 μm to 50 μm
3. Model supports the spacing between signal metal and the side shields from 4 μm to 20 μm .
4. Minimum taper length is 10 μm and maximum taper length is restricted to 100 μm .

4.21.3.10 meanderlinex (x=1 or 2)

Purpose

The offered meander-line devices refer to a set of parameterized shielded interconnect structures that are meandered in-plane with accurate predictability of their electrical behavior and including the parasitic effects of interconnects both on early (schematic) design phase and at the post-layout stage. The meander-lines enable users to design electromagnetic closed environment structures - where the line impedance, attenuation and phase shift are well controlled and known in advance. The meander-lines are intended to be used both in microwave (frequency domain) designs as well as in high speed digital (time domain) designs. The models enable designers to precisely evaluate the performance of the component from DC up to 120[GHz].

meanderlinex (x=1 or 2) Geometrical Design Considerations

The meander-line models support all 3 metal stacks (nlev=5, 6, and 7) and all signal/return metal combinations. The models are valid over a large range of metal widths, spacing, and metal combinations with the following limitations:

1. Model supports signal metal width range from
 - a. 4 μm to 50 μm for the cases with AM as the signal metal
 - b. 1.52 μm to 50 μm for the cases with LY as the signal metal
 - c. 0.4 μm to 20 μm for the cases with MQ as the signal metal
 - d. 0.2 μm to 20 μm for the cases with Mx (x=2, 3, 4) as the signal metal
2. Model supports the spacing between signal metal and the side shields from 4 μm to 20 μm for signal on AM, 1.52 μm to 20 μm for signal on LY, 0.4 μm to 20 μm for signal on MQ, and 0.2 μm to 20 μm for signal on Mx (x=4, 3, 2).
3. There are limits built in the Pcell for the minimum total length which depend on the signal metal width, the signal/return metal selection, and with/without side shields.

4.21.3.11 branchcouplerx (x=0, 1 or 2)

Purpose

The offered branch couplers refer to a set of parameterized four-port symmetrical structures useful for controlled and characterized signal coupling into two branches. They are also known as quadrature hybrids in literature, where a 90° phase difference exists between the outputs of the through and coupled ports. The four ports, named clockwise started from the top-left as input, through, coupled, and isolation, are designed to have scalable characteristic impedances useful for design purposes for a broad range of systems. The length of the segments connecting the through and the input ports is 90° at the frequency of interest. The models enable designers to precisely evaluate the performance of the component from DC up to 120[GHz].

branchcouplerx (x=0, 1 or 2) Geometrical Design Considerations

The coupler models are valid over a large range of metal widths, spacing, and metal combinations with the following limitations:

1. Present model release supports all 3 metal stacks (nlev=5, 6, and 7) with AM as signal path. A selection in return planes is provided depending on the metal stack selected. The following return planes (bottom ground shield) are possible: (i) MQ or M2 for nlev=5 (5-metal stack), (ii) MQ or M3 for nlev=6 (6-metal stack), and (iii) MQ or M4 for nlev=7 (7-metal stack).
2. Model supports signal metal width of 4 μm to 50 μm.
3. Model supports the spacing between signal metal and the side shields from 4um to 20um.
4. In the device CDF, the length calculation for given center frequency is based on the ideal straight line without bend and tee effects. Using those lengths will not give the performance aligned to the given center frequency. Those lengths are only used for a starting point or for the one-click function to show the S-parameters in the CDF window. User need to override the length calculation to input a larger length to compensate the bend and tee effect for the given frequency.

4.21.3.12 powerdividerx (x=0, 1 or 2)

Purpose

The offered Wilkinson power dividers refer to a set of parameterized three-port, reciprocal, and symmetrical structures useful for controlled and characterized signal division into two branches. The three ports can be designed to have scalable characteristic impedances useful for design purposes for a broad range of systems. The length of the segments for the split arms equals to a quarter of wavelength for ideal design (90-degree at frequency of interest). The output ports are isolated by using a resistor as specified in the design and synthesis of Wilkinson power dividers. The models enable designers to precisely evaluate the performance of the component from DC up to 120 [GHz].

powerdividerx (x=0, 1 or 2) Geometrical Design Considerations

The divider models are valid over a large range of metal widths, spacing, and metal combinations with the following limitations:

1. Present model release supports all 3 metal stacks (nlev=5, 6, and 7) with AM as signal path. A selection in return planes is provided depending on the metal stack selected. The following return planes (bottom ground shield) are possible: (i) MQ or M2 for nlev=5 (5-metal stack), (ii) MQ or M3 for nlev=6 (6-metal stack), and (iii) MQ or M4 for nlev=7 (7-metal stack).
2. Model supports signal metal width of 4 um to 50um.

3. Model supports the spacing between signal metal and the side shields from 4um to 20um.
4. In the device CDF, the length calculation for given center frequency is based on the ideal straight line without bend and tee effects. Using those lengths will not give the performance aligned to the given center frequency. Those lengths are only used for a starting point or for the one-click function to show the S-parameters in the CDF window. User needs to override the length calculation to input a larger length to compensate the bend and tee effect for the given frequency.

4.21.3.13 **langecoupler**

Purpose

The offered Lange coupler refers to a set of parameterized four-port structures useful for controlled and characterized signal division or coupling into two branches with signals that are in phase quadrature. The current version of the coupler allows selection of device model designed and characterized at the three center frequencies, i.e. 60 [GHz], 77 [GHz] and 94 [GHz]. The coupler model provides accurate information on the delay, return loss, insertion loss, coupling, and directivity centered at any of the above stated three frequencies. Depending on the frequencies a choice of three lengths (signal arm length) are provided to the user. The model enables designers to precisely evaluate the performance of the component from DC up to 120[GHz].

langecoupler Geometrical Design Considerations

The Lange coupler model is valid over a large bandwidth with the following limitations:

1. Present model release supports all 3 metal stacks (nlev=5, 6, and 7) with LY as signal path. An auto-selection in return planes is done depending on the metal stack selected i.e. (i) M1 as return planes for nlev=5 (5-metal stack), (ii) M2 for nlev=6 (6-metal stack), and (iii) M3 for nlev=7 (7-metal stack).
2. AM layer is used for cross-over (air-bridge).
3. Model supports fixed metal widths and port widths to ensure matching with 50 ohms source and load impedance.
4. The choice of frequency can be made by selecting 580 um for coupler center frequency at 60[GHz], 450 um for center frequency at 77[GHz], and 370 um for center frequency at 94[GHz].
5. Model does not support any layout modification and neither uses any side-shields.

4.21.3.14 **ratracehybrid**

Purpose

The offered Rat Race Hybrids refer to a set of parameterized four-port structures useful for controlled and characterized signal coupling into two branches. They are also known as 180° hybrids in literature, where a 180° phase difference exists between the outputs of the through and coupled ports. The four ports namely, input, through, isolation and coupled, are designed to have scalable characteristic impedances useful for design purposes for a broad range of systems. The length of the segments connecting the through and the input ports is 90° at the frequency of interest. The models enable designers to precisely evaluate the performance of the component from DC up to 120[GHz].

ratracehybrid Geometrical Design Considerations

The hybrid models are valid over a large range of metal widths, spacing, and metal combinations with the following limitations:

1. Present model release supports all 3 metal stacks (nlev=5, 6, and 7) with AM as signal path. A selection in return planes is provided depending on the metal stack selected. The following return planes (bottom ground shield) are possible: (i) MQ or M2 for nlev=5 (5-metal stack), (ii) MQ or M3 for nlev=6 (6-metal stack), and (iii) MQ or M4 for nlev=7 (7-metal stack).
2. Model supports signal metal width of 4 μm to 50 μm .
3. Model supports the spacing between signal metal and the side shields from 4 μm to 20 μm .
4. In the device CDF, the length calculation for given center frequency is based on the ideal straight line without bend and tee effects. Using those lengths will not give the performance aligned to the given center frequency. Those lengths are only used for a starting point or for the one-click function to show the S-parameters in the CDF window. User need to override the length calculation to input a larger length to compensate the bend and tee effect for the given frequency.

4.21.4 Distributed Passive Connection Guidelines

The distributed passives: bend, tee, step, gap, taper, open, short, radialstub, yjunction and langecoupler can not be connected to each other or themselves directly. A segment of singlewire needs to be used for the connections. Otherwise, LVS will not be able to distinguish them.

The passive models at the schematic level provide only one terminal to the ground terminal (known as "vshield" in schematic symbol). In the case with devices with side-shields the resistance of the shield is accounted in the resistance calculated although only one terminal is provided. Therefore it is important to connect the side-shields in layout and the bottom shields using a global VDD or ground. This will ensure to minimize unwanted inductance in the return current path.

The distributed passive models provided a choice of different metal layers for the return path. Although not recommended, it might be possible that the designer might use different return metal levels for different devices. It is important to connect the return paths on multiple layers with vias and model the vias using full-wave EM solvers to minimize inaccuracies in the design stage.

The distributed passive models are created assuming an environment with no other structures close by. As a result, the model accuracy will be lost if multiple other devices are placed in close proximity (side-by-side) of the modeled devices. To minimize this effect it is necessary to keep a minimum distance between devices in the direction normal to their lengths if possible.

- For the case without side-shields the spacing between two devices (defined as the distance between the facing edges of the signal metals) should be the smaller of 6 times signal width or 50 μm , as long as the distance between edges of the bottom shields satisfies the minimum spacing rules for that metal layer.
- For the case with side-shields, the spacing between the edges of side-shields should be at least 10 μm .
- The guidelines are based on full-wave EM simulations to obtain a coupling factor of less than 30 dB between two 500 μm long transmission lines.

This Page Intentionally Left Blank

4.22 Mixed Voltage Interfaces

This section involves rules for mixed voltage interface (MVI) environments. The issues of interest are burn-in, dynamic voltage screen, enhanced voltage screen, hot electrons, dielectric breakdown, latch-up, snap-back, borderless CA and ESD protection.

The values for the thick oxide can be used for a rough estimate for V_{max} (dielectric integrity) as function of POH, T_j and area.

4.22.1 Latchup

Latchup susceptibility must be verified for the maximum voltage applied to the product under **any** conditions, including burn-in. For 2.5 V tolerant I/O, latchup testing should be evaluated for sensitivities above 2.5 V. For 1.2 V internal/ 2.5 V external two power-supply chips, latchup evaluations should be for voltages over 1.8 V. Product testing should quantify latch-up sensitivity to power-up and power-down sequencing. In general, the burn-in voltage is 1.5X operating voltage. Therefore, latchup evaluation should be done accordingly (for more information on burn-in).

4.22.2 Snap-back

The applied voltages must not exceed the sustaining voltage of the transistors in the circuitry. Overvoltages can be avoided by using NFET's in a series configuration (stacked transistors). Layout of interdigitated stacked NFET's may have a snap-back voltage lower than the sum of the two transistors.

4.22.3 ESD Protection

ESD protection circuits are provided for mixed voltage interface circuit applications. ESD rules for stacked NFET's are provided in the ESD section. For mixed voltage applications, ESD networks are needed between the different power supply rails. For 1.2/2.5 V two-power-supply chips, diode strings or self bias well ESD networks should be used between power supplies. See section 6.0 , "Electro-static Discharge (ESD) Protection" on page 369.

4.22.4 Hot Carrier Effects

Regular, LVT, and LP FET's which are exposed to source to drain bias higher than 1.5 V under nominal, normal operating conditions must be longer than the minimum channel length in design dimension. Thick oxide devices (Regular IO and ZVT thick NFET) which are exposed to source to drain bias higher than 2.5 V under nominal, normal operating conditions must be longer than the minimum channel length in design dimension. In addition, the circuits must be rigorously analyzed for all Hot Carrier stress types for all the devices. See section , "ac_characterisitcs" on page tables1.

4.22.5 Reliability Screening

The need for effective Burn-in and Reliability Screens places constraints on mixed voltage I/O design.

The following are additional design requirements for mixed voltage I/O circuit designs.

- For chips with I/O power supplies in addition to the 1.2 volt supply, design the chip and or application such that when V_{dd} is lost, the I/O power supply is also turned off. This is to prevent chip damage.
- Have the I/O design such that it does not depend on the voltage differential between V_{dd} and the I/O supply in order to function during Burn-in and voltage screens.
- Have the I/O design such that it does not draw DC power during Burn-in, DVS, EVS and I_{ddQ} testing.

4.22.6 Maximum Reverse Voltage

The maximum steady state voltage allowed between any two terminals (gate, source, drain, and body) of an FET can not exceed the V_{ddmax} as specified in Section 4.4 , “General FET Design Discussion” on page 247, Table 4-5. Exception: The maximum reverse-bias junction voltage allowed during steady state conditions is 3.6 volts only for the 5.2nm thick oxide devices. Please refer to section 5.2.1 , “Burn-in” on page 332 for more information.

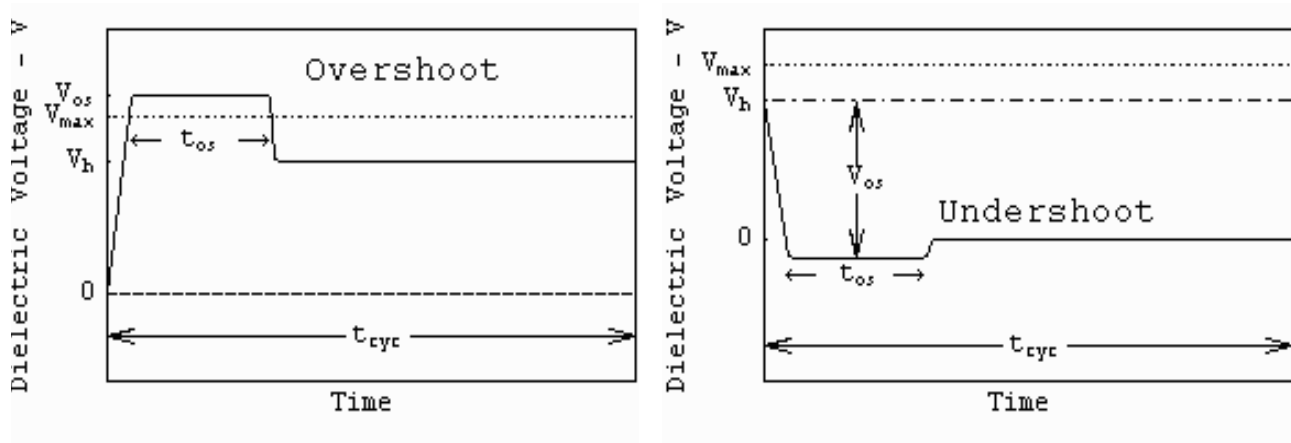
4.22.7 V_{max} and V_{os} for 2.2 nm Gate Dielectric

The BiCMOS8HP 2.2 nm gate dielectrics have been qualified for a maximum use voltage of 1.6 V at a temperature of 125° C, a total oxide area of 20 mm², a lifetime of 175 KPOH and a 100% duty factor. Furthermore, the maximum voltage is dependent on the application conditions and gate areas. For example, the absolute maximum voltage across the gate oxide at the aforementioned application conditions and an area of 0.2mm², is estimated to be 1.77 V for NFETs and 1.80 V for PFETs. Exceeding these maximum conditions may result in severe device degradation and gate oxide failure. Aside from gate oxide dielectric integrity and NBTI, other aspects to consider for applied voltages are described throughout Section 4.0 “Electrical Parameters and Models” on page 243.

The maximum allowed voltages across the gate dielectric are defined as follows.

V_{max} : maximum allowed dc voltage without transients (overshoot or undershoot)

V_{os} : maximum allowed transient voltage when used with a maximum “high level” of V_h ($V_h < V_{max}$)



Equations are provided below to calculate these maximum voltages as a function of lifetime (KPOH), maximum junction temperature (T_j) and total gate area for each device type listed in Table 4-47, “Maximum Voltage Parameters” on page 328. These equations are valid only for junction temperatures above 30° C. The values at 30° C should be used for applications below 30° C.

$$|V_{max}| = V_{ref} + \frac{1}{G} \left[\ln \frac{A_A \times A_T \times 175}{KPOH \times D_f} \right]$$

$$|V_{os}| = |V_h| + \frac{1}{G} \left[\ln \frac{A_A \times A_T \times A_V \times 175 - (KPOH \times D_f) + t_{os}}{t_{os}} \right]$$

$$A_A = \left[\frac{Area\{mm^2\}}{A_{ref}} \right]^{-1/B}$$

$$A_T = \exp \left[\frac{E_a}{8.62 \times 10^{-5}} \times \left(\frac{1}{273 + T_j\{^{\circ}C\}} - \frac{1}{398} \right) + \frac{E_b}{8.62 \times 10^{-5}} \times \left(\left\{ \frac{1}{273 + T_j\{^{\circ}C\}} \right\}^2 - \left\{ \frac{1}{398} \right\}^2 \right) \right]$$

$$t_{os} = KPOH \times S_f \times D_{os}$$

$$A_V = \exp[-G(|V_h| - V_{ref})]$$

The constants V_{ref} , A_{ref} , B , G , E_a and E_b are listed in Table 4-47, “Maximum Voltage Parameters” on page 328, for each device type and the following definitions apply:

D_f: Fraction of product lifetime with dielectric voltage at V_h or switching to V_h

S_f: Fraction of total cycles where,

- overshoot: a switch to V_h occurs
- undershoot: a switch to the low-level occur

D_{os}: Fraction of a switching cycle where voltage across the dielectric exceeds V_h

Table 4-47. Maximum Voltage Parameters						
Device	V_{ref}	A_{ref}	B	G	E_a	E_b
NFET, 2.2 nm	1.77	0.2	1.42	15.87	2.324	-290.7
PFET, 2.2 nm	1.80	0.2	1.42	13.53	1.608	-167.6
NFET, 5.2 nm	3.60	0.2	3.69	7.5	0.42	0
PFET, 5.2 nm	3.60	0.2	2.78	7.3	0.42	0

Table 4-48, “Sample V_{max} Calculations 2.2 nm FETs with a gate area of 0.2 mm² and a duty factor of 100%” on page 328, provides an example of V_{max} calculations for 2.2 nm FET applications with a gate area of 0.2 mm² and a duty factor of 100%. For evaluation of product-specific applications, please contact the IBM Technical Representative.

Table 4-48. Sample V_{max} Calculations 2.2 nm FETs with a gate area of 0.2 mm ² and a duty factor of 100%							
POH (hrs)	T_j (°C)	NFET	PFET	POH (hrs)	T_j (°C)	NFET	PFET
175K	125	1.77	1.80	60K	125	1.84	1.88
175K	105	1.85	1.88	60K	105	1.92	1.97
175K	85	1.93	1.98	60K	85	2.00	2.06
175K	65	2.01	2.07	60K	65	2.08	2.15
100K	125	1.81	1.84	40K	125	1.87	1.91
100K	105	1.89	1.93	40K	105	1.95	2.00
100K	85	1.97	2.02	40K	85	2.03	2.08

Table 4-48. Sample V_{max} Calculations 2.2 nm FETs with a gate area of 0.2 mm^2 and a duty factor of 100%

100K	65	2.05	2.11	40K	65	2.10	2.18
------	----	------	------	-----	----	------	------

4.22.8 V_{MAX} and V_{GS} for 5.2nm Gate Dielectric

The 5.2 nm gate oxides have been qualified for a maximum use voltage of 3.60 V at a temperature of 125° C, a total oxide area of 0.4 mm^2 , a lifetime of 175 KPOH and a 100% duty factor. For these conditions, the absolute maximum voltage is 3.6 V. Exceeding these maximum conditions may result in severe device degradation and gate oxide failure. The maximum allowed gate dielectric voltages under specific application conditions may be calculated using the equations from section 4.22.7 , “Vmax and Vos for 2.2 nm Gate Dielectric” on page 326 and the parameters for 5.2 nm FETs in Table 4-47, “Maximum Voltage Parameters” on page 328.

4.22.9 V_{MAX} for MIM Capacitor

The BiCMOS8HP MIM capacitor maximum allowed operating voltage is determined from the following equation:

$$|V_{max}| = \left[\frac{C_0 \cdot t}{[-\ln(1 - 10^{-6} \cdot PPM)]^{1.25} \cdot A^{-0.5624} \cdot \exp\left[\frac{3764.94}{273.15 + T}\right]} \right]^{-0.0306}$$

where t is time in Khours, PPM is parts per million failure criterion, T is the temperature in degrees centigrade, and A is the area in square microns. The value of C_0 for the single MIM is 1.87×10^{-49} . The tables below show the results of an example calculations given the following operation criterion.

4.22.9.1 MIM

Time: 100KPOH, 60KPOH, 40KPOH, 20KPOH

Fail Criterion: 1 PPM

Temperature: 125°C, 100°C, 85°C

Area: $1,000,000 \mu\text{m}^2$

T(°C)	V _{max} 100 KPOH	V _{max} 60 KPOH	V _{max} 40 KPOH	V _{max} 20 KPOH
125	16.8	16.9	17.2	17.5
100	17.0	17.3	17.5	17.9
85	17.2	17.5	17.7	18.1

5.0 Reliability Design Rules and Models

5.1 Guidelines for Optimal Reliability

CAUTION! The following guidelines do not replace the need for a thorough study of all of the rules in this manual. They are intended to provide a brief summary of design practices that will result in a more robust final product.

Recommendations:

- Stay below the specified limits of the power supply: $V_{dd} = 1.6$ V (maximum) for $T_{ox}=2.2$ nm, $V_{dd} = 2.7$ V (maximum) for regular I/O devices.
- Use power supplies with tighter tolerances (for example less than or equal to 1.5 ± 0.1 V, 2.5 ± 0.2 V) when possible. Most reliability mechanisms are strongly voltage dependent.
- Stay within the specified temperature range: -55 to 125° C
- Use minimum layout dimensions only when necessary.
- Use minimum device lengths only when necessary. Many reliability mechanisms are strongly length dependent.
- All circuits must be designed to be functional at the worst-case design burn-in conditions. The details of this are described in section 5.2 , “Reliability Screening” on page 332.
- Review wear-out mechanism ground rules
 - Hot Carriers
 - Critical circuits are those with highly loaded devices, high duty factors, critical matching, analog function or bidirectional operation
 - minimize switching times and currents in circuits
 - Electromigration
 - Critical circuits are those with highly loaded devices or high duty factors
- Contacts to polysilicon must occur over RX space (STI).
- A chip guard ring must be provided around the entire chip.
- Avoid large areas of thin oxide capacitors. These increase the likelihood of defect related chip failure.
- DC standby current screens are an effective means of detecting defects. Chips should be designed with minimal DC standby current. If DC current is required for a particular application, then that current should be brought to a separate pad.
- If device matching is a concern, place devices in close proximity with the same orientation. Allow for at least the minimum expected mismatch specified under Threshold Voltage Stability.
- Vertical interconnects are mechanical and electrical weak points. Maximize areas of vertical interconnects by using as much contact and via stud area as possible and by overlapping contacts and vias with as much metal as possible.
- Any device uses not specifically allowed by this manual must be reviewed with Reliability Engineering.

5.1.1 Reliability Limitations

5.1.1.1 NPN:

- Forward Bias emitter current density is limited to $15\text{mA}/\mu\text{m}^2$.
- Reverse Bias emitter junction voltage is limited to 1.75 Volts.
- Base-collector avalanche voltage is limited to 1.5 Volts.

5.1.1.2 Capacitors:

Maximum voltage across a MIM capacitor, see section 4.22.9 , “VMAX for MIM Capacitor” on page 329.

5.2 Reliability Screening

There are four reliability screens which require designer's attention. However not all systems require optimal reliability and hence do not have to pass all four screens. The four screens are:

1. Dynamic Voltage Screen (DVS)
2. Enhanced Voltage Screen (EVS)
3. Supply current screen (I_{dd})
4. Burn-in (100% of production) screens of the final packaged product

Either the first three or the last one must be addressed to achieve minimum reliability confidence. For maximum reliability, all four screens need to be addressed.

5.2.1 Burn-in

All circuits must be designed to be functional at the worst-case design burn-in conditions. IBM's requirement for burn-in conditions is $1.5X V_{dd} \pm 0.125 \text{ V}$ ($1.8 \pm 0.125 \text{ V}$) and 140° C . Therefore, the following conditions should be used to assess functionality at burn-in. Any deviation from these conditions must be discussed with IBM.

- $V_{dd} = 1.925\text{V}$ for 1.2V circuits, 2.375V for 1.5V circuits, and 3.875V for 2.5V circuits
- Temperature = 140° C
- $L_p = 0.092 \mu\text{m}$ NFET, $0.215 \mu\text{m}$ for DGNFET, $0.40\mu\text{m}$ for XNFET
- $L_p = 0.092 \mu\text{m}$ PFET, $0.215 \mu\text{m}$ for DGPFET, $0.40\mu\text{m}$ for XPFET
- $T_{cyc} = 200\text{-}500 \text{ ns}$
- $T_{rise,fall} = 60 \text{ ns}$
- Other variables are at nominal conditions

The standard devices in I/O circuits that drive and receive voltages higher than 1.2 V can NOT have more than 1.925 V across its terminals during burn-in. The reverse-bias junction voltages (N^+ to substrate, N-Well

to P^+), however, can be as high as 3.6 V. The thick oxide devices in I/O circuits that drive and receive voltages higher than 2.5V can NOT have more than 3.875 V across its terminals during burn-in.

Burn-in function at the indicated elevated conditions requires a robust voltage distribution (including N well and substrate contacts) and patterns which avoid large amounts of simultaneous switching.

Temperature control becomes a problem if the ICs themselves supply too much heat compared to the oven. Power dissipation over about 3 watts (average) may have to be corrected with special burn-in modes.

5.2.2 Wafer Screening

DVS, EVS, and I_{dd} screens are fully integrated as one test at wafer final test as a customer option. Support for the wafer screening options must be negotiated with IBM through the IBM product engineer. Dynamic Voltage Screen (DVS) stresses by writing with high pattern coverage at supply voltage ≈ 2.55 V (max, actual based on product testing, see “Vmax and Vos for 2.2 nm Gate Dielectric” on page 326 and “VMAX and VGS for 5.2nm Gate Dielectric” on page 329). EVS bumps the supply voltage to 3.0 V (max, actual based on product testing) at the completion of each DVS pattern. Supply current (I_{dd}) is used as the main indicator of DVS/EVS failure along with loss of functionality.

EVS is extremely effective with pre burn-in reliability shorting mode defects. The normally dominant shorting mode is reduced to a minority compared to open mode. Additional defect reduction is afforded since highly defective wafers can be identified and scrapped. In many cases EVS has been successfully substituted for burn-in.

5.2.2.1 Design Practices for Wafer Screening

Adherence to the following ground rules for voltage screening is highly recommended. EVS does not restrict channel length.

- Static data integrity with V_{dd} /Inputs at 3.0 V (maximum target, actual based on product testing).
- Dynamic functionality with V_{dd} /Inputs at 2.55 V (maximum target, actual based on product testing), $T_{cycle} = 200\text{-}1000$ ns.
- Experience has shown that products properly designed for the burn-in conditions above will meet the static/dynamic requirements for EVS/DVS.
- Supply low I_{dd} states with good node toggle and without DC current. Every potential DC path from V_{dd} to ground should be blocked by at least one NFET or PFET with $V_{gs}=0$. Supply True/Complement states for embedded SRAM and all latches.
- Pass gate circuitry design must satisfy this DC path blockage requirement e.g. be a pass gate feeding a latch, fully complementary pass gate design, or have an NFET pass gate pullup (half latch).
- Grounded PFET circuitry design must also be DC free. For example there should be a test pin to undo grounding of PFETs and an extra NFET pull down with gate tied to the same test pin. so that with the test pin high, the PFET is OFF and the NFET ties the potentially floating node to ground.
- The layout design and/or test design of MUX circuitry must be free of DC paths and floating nodes (inde-

terminate states).

- Input and I/O circuitry must be designed such that input highs can be received without DC paths at no more than V_{dd} volts during EVS where V_{dd} is projected at 3.0 V.

As with burn-in, DVS requires functionality at accelerated conditions of voltage and temperature. This functionality needs to be verified by whoever is responsible for wafer test on the earliest available hardware. With products becoming ever more complex, the conditions for this early assessment needs to be discussed with Reliability Engineering.

5.3 Front End Of Line (FEOL) Reliability Design Rules

5.3.1 Hot Carrier Effects

--NOTE-- Hot electron degradation can have a significant impact on circuit performance and functionality. It is imperative that circuit designers carefully review their designs for hot electron degradation. Cumulative degradation and process variation must be taken into account for both burn-in and field operation.

The burn-in conditions to use for simulations to assess functionality are determined from the worst case of the following:

- Case 1
 1. $V_{DD} = 1.925V$ (2.375V for 1.5V supply, 3.875 V for 2.5V supply)
 2. Temperature = 140° C
 3. $L_p = 0.092 \mu m$ for NFET and PFET (0.215 μm for DG devices)
 4. Duration = nominal burn in duration for your product; 200ns cycle time
 5. Other variables are at nominal
- Case 2
 1. $V_{DD} = 1.80 V$ (2.25V for 1.5V supply, 3.75 V for 2.5 supply)
 2. Temperature = 140° C
 3. $L_p = 0.081 \mu m$ for NFET and PFET (0.175 μm for DG devices)
 4. Duration = nominal burn-in duration for your product; 200 ns cycle time
 5. Other variables are at nominal
- Case 3
 1. $V_{DD} = 1.80V$ (2.25V for 1.5V supply, 3.75 V for 2.5 supply)
 2. Temperature = 140 C
 3. $L_p = 0.092 \mu m$ for NFET and PFET (0.215 μm for DG devices)
 4. Duration = worst case duration for product; 200 ns cycle time
 5. Other variables are at nominal with process variation (ACLV, V_t etc) included

The field operating conditions:

1. $V_{DD} = V_{DDmax}$ for your application
2. Temperature = lowest operating temperature for your application
3. $L_p = 0.081 \mu m$ for NFET and PFET ($0.175 \mu m$ for DG devices)
4. Appropriate lifetime and duty cycle
5. Other variables are at nominal with process variation

For these cases there should be no significant loss of functionality of the product. For any product requiring performance sorting at product test guardbands may be needed.

Minimum L_p typically produces the largest hot carrier shifts but may not be the most sensitive condition for circuit operation and performance. For example, chips with longer L_p that just meet time zero performance targets may degrade less than minimum L_p chips. With little or no performance margin, these chips are more likely to fail during life than chips with shorter L_p , large degradation and large time zero performance margin.

Mechanism

Hot carriers are holes or electrons which have been accelerated to a high energy by local electric fields. If such a carrier has kinetic energy in excess of the silicon-insulator barrier height, it may surmount the barrier and enter the insulator. Once in the insulator, the electron or hole may become trapped. High energy carriers can also produce interface states. The accumulation of trapped charge causes a shift in the V_t (threshold voltage) of the device and the accumulation of interface states can reduce device drain current, degrade sub-threshold slope and increase device leakage.

Hot carriers are categorized into two types dependent on the origin of the carrier. These are CHC (Channel Hot Carriers) and SHC (Substrate Hot Carriers). Channel hot carriers are broken down further into Conducting (Gate Voltage > Threshold Voltage) and Non-Conducting (Gate Voltage ~ 0).

5.3.1.1 Conducting Hot Carriers: Thin Oxide (2.2 nm) N-channel Devices

The NFET channel hot carrier effect is dominated by the generation of interface states. Significant degradation occurs when the gate voltage is above V_T , and V_{DS} is large. The device degradation is characterized by both a threshold voltage increase and a reduction in device drain current over time. The device damage is localized near the drain, resulting in an asymmetry in the post stress device characteristics.

The following is a model of the conducting NFET channel hot carrier effect. The model is derived at peak substrate current ($V_{GS} \sim V_{DS}/2$). This is the maximum degradation point for Leff's larger than nominal. For Leff's less than nominal, $V_{GS} = V_{DS}$ is the worst DC case. However, in actual use the degradation will peak near $V_{GS} \sim V_{DS}/2$ even for low L_{eff} since the dependence of the degradation on v_{GS} is not very strong for low L_{eff} and at $V_{GS} = V_{DS}$, v_{DS} normally will be significantly lower. This model does not include saturation effects, which tend to reduce the degradation above 50%. For $W_{design} < 1 \mu m$, or for temperatures above 30 C, corrections must be applied as indicated.

Degradation Equation:

The degradation is given in percent by:

$$\frac{\Delta I_D}{I_D} = A \times L_{eff}^m \times \exp\left(\frac{-V_0}{V_{DD}}\right) \times t_{eq}^n$$

in units of μm , volts, and seconds. The time t_{eq} is defined below. The parameters A , m , V_0 and n are given in Table 5-1, "NFET Hot Carrier Conducting Model Common Parameters $T_{ox}=2.2\text{nm}$ " and Table 5-2, "NFET Hot Carrier Conducting Model 'A' Parameter".

Table 5-1. NFET Hot Carrier Conducting Model Common Parameters
 $T_{ox}=2.2\text{nm}$

Use Mode	m	V_0	n
Forward Saturation	-2.82	28.2	0.52
Reverse Saturation	-2.82	28.2	0.52

Table 5-2. NFET Hot Carrier Conducting Model 'A' Parameter

Use Mode	Mean	Worst Case (+3 σ)
Forward Saturation	34.4	60.2
Reverse Saturation	60.2	114.4

Time Calculations: Hot carrier effects occur in NFET devices when v_{DS} is close to V_{DD} and appreciable i_D is flowing. For typical CMOS circuits, these conditions occur only during switching transients. In this case, equivalent stress time can be approximated by,

$$t_{eq} = D \times \left(\frac{f_{sw}}{f_{cl}} \right) \times t_{use}$$

where,

f_{sw} = average switching freq (CYCLES/sec)

f_{cl} = clock frequency

t_{use} = actual use time in sec and,

$D = 0.003$ for short v_{DS} transition times ($< 0.05 \times t_{cyc}$, 10-90%)

0.010 for moderate v_{DS} transition times (0.05 to $0.15 \times t_{cyc}$, 10-90%)

0.03 for long v_{DS} transition times (0.15 to $0.30 \times t_{cyc}$, 10-90%)

Another way of estimating t_{eq} is the total time spent between the following two waveform events: v_{GS} reaching V_T and v_{DS} falling to $V_{DD}/(1+(V_{DD}/2V_0))$.

Care must be taken when operating devices with persistent drain currents. In these cases, v_{DS} must be kept low, or associated circuits designed to tolerate significant degradations.

Narrow Device Correction: For device design widths of less than one μm , the calculated degradation should be multiplied by 1.75x

High Temperature Correction: For junction temperatures above 30 C, the calculated degradation does not require correction.

Device Characteristics: The observed effect of hot carrier injection on an NFET device is dependent on the measurement conditions applied after stress. Reverse mode refers to the situation where a device is measured with its source and drain connections reversed relative to those during stress. Thus, the reverse saturation degradation is important when a device is used bidirectionally, as in a pass gate. Observed I_D degradation as a function of V_{GS} increases as V_{GS} decreases (down to V_T). The net effect over the whole V_{GS} range (above V_T) can be approximated by a *simultaneous* current multiplier (given by a dependent current source), and an effective V_T shift (given by a voltage source). The current source J_{deg} is in parallel but opposite direction to the J_{ds} source in the device model (so as to lower the effective drain current), and the voltage source V_{deg} is in series with the gate, opposing the turn-on of the device (that is, negative towards the gate.) The values of J_{deg} and V_{deg} are given by:

$$J_{deg} = C \times \left(\frac{\Delta}{1 + \Delta} \right) \times J_{DS}$$

$$V_{deg} = B \times \Delta$$

where,

$\Delta = \Delta I_{ON}/I_{ON}$, expressed as a fraction, and the parameters C and B are given by:

Table 5-3. NFET Hot Carrier Degraded Model Parameters		
Device	C	B (V)
2.2nm Tox NFET	0.44	0.35
5.2nm Tox NFET	0.63	0.87

Note: Do not confuse V_{deg} with the *actual* threshold shift, which is larger than V_{deg} .

Example: A 2.2nm NFET in an inverter circuit is operated for 100,000 hour with switching transient of moderate transition times once every 10 ns clock cycle. $V_{DD} = 1.5$ v, and minimum $L_{eff} = 0.06 \mu m$. $t_{eq} = 0.01 \times (50 \text{ MHz}/100 \text{ MHz}) \times 3.6E8 \text{ sec} = 1.8E6 \text{ sec}$. Using the model parameters for forward saturation yields a Drain current degradation of 2.06% (WC A=60.2) for the NFET. $J_{deg}=0.009 \times J_{ds}$, $V_{deg}=7mV$.

Specific Device Concerns: The following are some specific NFET uses that must be examined in detail.

- Burn-in conditions
- Bidirectional devices - stressing a device in both directions is more severe than 2X the stress time in one direction
- D.C. current flow

- Heavily loaded circuits such as Off-chip Drivers (OCDs) and Clock Drivers
- Circuits such as OCDs which may see voltage overshoots or undershoots
- Mixed voltage interface circuits or any circuit using greater than 1.95 V.
- Circuits with long rise and/or fall times such as OCDs
- Circuits where V_T or I_D matching is critical

Transconductance (G_m)

The degradation is given in percent by:

$$\frac{\Delta G_m}{G_m} = A \times L_{eff}^m \times \exp\left(\frac{-V_0}{V_{DD}}\right) \times t_{eq}^n$$

The degradation was measured at $V_{DS} = 1.2V$ and $V_{GS} = 0.6V$.
The following values apply to forward saturation:

$A = 14$ (nominal)
 $A = 21$ (worst case, 3-sigma)
 $m = 2.9$
 $V_0 = 22.6$
 $n = 0.45$

Conductance (G_{ds})

The degradation is given in percent by:

$$\frac{\Delta G_{ds}}{G_{ds}} = A \times \exp\left(\frac{-V_0}{V_{DD}}\right) \times t_{eq}^n$$

The above degradation is worst case for devices upto 0.24 μm design channel length, and above this value, the degradation is negligible.

$A = 3.34 \times 10^{-4}$ (worst case)
 $V_0 = 26.6$
 $n = 0.48$

5.3.1.2 Conducting Hot Carriers: Regular I/O Thick Oxide (DG, 5.2 nm) N-channel Devices

The DGNFET channel hot carrier effect is dominated by the generation of interface states. Significant degradation occurs when the gate voltage is above V_T , and V_{DS} is large. The device degradation is characterized by both a threshold voltage increase and a reduction in device drain current over time. The device damage is localized near the drain, resulting in an asymmetry in the post stress device characteristics.

The following is a model of the conducting DGNFET channel hot carrier effect. The model is derived at peak substrate current ($V_{GS} \sim V_{DS}/2$). This is the maximum degradation point. This model does not include satura-

tion effects, which tend to reduce the degradation above 50%.

Degradation Equation:

The degradation is given in percent by:

$$\frac{\Delta I_D}{I_D} = A \times L_{eff}^m \times \exp\left(\frac{-V_0}{V_{DD}}\right) \times t_{eq}^n$$

in units of μm , volts, and seconds. The time t_{eq} is defined below. The parameters A, m, V_0 and n are given in Table 5-4, “NFET Hot Carrier Conducting Model Common Parameters $T_{ox}=5.2\text{nm}$ ” and Table 5-5, “NFET Hot Carrier Conducting Model ‘A’ Parameter”.

*Table 5-4. NFET Hot Carrier Conducting Model Common Parameters
 $T_{ox}=5.2\text{nm}$*

Use Mode	m	V_0	n
Forward Saturation	-2.64	41	.48
Reverse Saturation	-1.94	41	.48

Table 5-5. NFET Hot Carrier Conducting Model ‘A’ Parameter

Use Mode	Mean	Worst Case (+3 σ)
Forward Saturation	260	494
Reverse Saturation	1660	3154

Time Calculations: Hot carrier effects occur in NFET devices when v_{DS} is close to V_{DD} and appreciable i_D is flowing. For typical CMOS circuits, these conditions occur only during switching transients. In this case, equivalent stress time can be approximated by,

$$t_{eq} = D \times \left(\frac{f_{sw}}{f_{cl}}\right) \times t_{use}$$

where,

f_{sw} = average switching freq (CYCLES/sec)

f_{cl} = clock frequency

t_{use} = actual use time in sec and,

D = 0.003 for short v_{DS} transition times (< 0.05 x t_{cyc} , 10-90%)

0.010 for moderate v_{DS} transition times (0.05 to 0.15 x t_{cyc} , 10-90%)

0.03 for long v_{DS} transition times (0.15 to 0.30 x t_{cyc} , 10-90%)

Another way of estimating t_{eq} is the total time spent between the following two waveform events: V_{GS} reaching V_T and V_{DS} falling to $V_{DD}/(1+(V_{DD}/2V_0))$.

Care must be taken when operating devices with persistent drain currents. In these cases, v_{DS} must be kept

low, or associated circuits designed to tolerate significant degradations.

Narrow Device Correction: For device design widths of less than one μm , the calculated degradation should be multiplied by 1.25x

High Temperature Correction: For junction temperatures above 30 C, the calculated degradation does not require correction.

Device Characteristics: The observed effect of hot carrier injection on an NFET device is dependent on the measurement conditions applied after stress. Reverse mode refers to the situation where a device is measured with its source and drain connections reversed relative to those during stress. Thus, the reverse saturation degradation is important when a device is used bidirectionally, as in a pass gate. Observed I_D degradation is more severe than the average for V_{GS} near V_T and less severe for V_{GS} near V_{DD} . The increase in inverse average drain current approximates the increase in the delay (rising v_{GS} to falling v_{DS}).

Example: An inverter circuit is operated for 50,000 hour with switching transient of longer transition times once every 10 ns clock cycle. $V_{DD} = 2.5\text{v}$, and $L_{eff} = 0.17 \mu\text{m}$. $t_{eq} = 0.03 \times (50 \text{ MHz}/100 \text{ MHz}) \times 1.8\text{E}8 \text{ sec} = 2.7\text{E}6 \text{ sec}$. Using the model parameters for forward saturation yields a Drain current degradation = 4.9% ($A=494 \text{ WC}$).

Specific Device Concerns: The following are some specific NFET uses that must be examined in detail.

- When $V_{ds} > 2.75$ It is recommended to use stacked devices and/or longer channels
- Burn-in conditions
- Bidirectional devices - stressing a device in both directions is more severe than 2X the stress time in one direction
- D.C. current flow
- Heavily loaded circuits such as Off-chip Drivers (Odds) and Clock Drivers
- Circuits such as Odds which may see voltage overshoots or undershoots
- Mixed voltage interface circuits or any circuit using greater than 3.6 V.
- Circuits with long rise and/or fall times such as Odds
- Circuits where V_T or I_D matching is critical

5.3.1.3 Non-conducting hot carriers: Thin Oxide (2.2 nm) N-channel Devices

The non-conducting stress mode is one in which $V_{GS} = 0$ and V_{DS} is large. NFET devices in which significant subthreshold or punch through current flows can exhibit hot carrier effects. The physical mechanism is similar to the conducting NFET and is found in short channel length devices at elevated voltages and temperatures, especially under burn-in conditions.

The degradation is given in percent by:

$$\frac{\Delta I_D}{I_D} = A \times L_{eff}^{(b/V_D)} \times \exp\left(\frac{-V_0}{V_D}\right) \times (I_{off} \times t_{eq})^n$$

in units of μm , volts, seconds, and I_{off} in $\text{nA}/\mu\text{m}$ at stress condition (such as burn-in).

The parameters A, V_0 , b and n are given in Table 5-6, “NFET Hot Carrier Non-conducting Model Parameters”.

Table 5-6. NFET Hot Carrier Non-conducting Model Parameters

Use Mode	A (mean)	A (2σ WC)	b	V_0	n
Forward Saturation	72	288	-7.86	46.6	0.54
Reverse Saturation	180	720	-7.86	46.6	0.54

Narrow Device Correction: For device design widths of less than one μm , the multiplier 1.75x should be applied

Device Characteristics: The observed effect of hot carrier injection on an NFET device is dependent on the measurement conditions applied after stress. Reverse mode refers to the situation where a device is measured with its source and drain connections reversed relative to those during stress. Thus, the reverse saturation degradation is important when a device is used bidirectionally, as in a pass gate. Observed I_D degradation is more severe than the average for V_{GS} near V_T and less severe for V_{GS} near V_{DD} . The increase in inverse average drain current approximates the increase in the delay (rising v_{GS} to falling v_{DS}).

Example: A logic part is burned-in for 10 hours at 140 C with $V_D=1.8$ V. What is the worst case current degradation for a (normal V_T) device used unidirectionally? For minimum $L_{eff} = 0.075 \mu\text{m}$, $I_{off} = 80\text{nA}/\mu\text{m}$; assume 100% duty cycle worst case, $t=36,000$ sec. Using the model parameters for forward saturation yields a $\Delta I_D/I_D = 0.41\%$ for the NFETs.

5.3.1.4 Non-conducting hot carriers: Regular I/O Thick Oxide (DG, 52A) N-channel Devices

The non-conducting stress mode is one in which $v_{GS} = 0$ and v_{DS} is large. NFET devices in which significant subthreshold or punchthrough current flows can exhibit hot carrier effects. The physical mechanism is similar to the conducting NFET and is found in short channel length devices at elevated voltages and temperatures, especially under burn-in conditions. The degradation in I_D is projected to be less than 1% for a 48 hr. burn-in at $T = 140$ C, and $V_{DD} = 3.8$ V.

The degradation is given in percent by:

$$Y = A \times L_{eff}^{(b/V_D)} \times \exp\left(\frac{-V_0}{V_D}\right) \times (I_{off} \times t_{eq})^n$$

$$\Delta I_D = \frac{SAT \times Y}{SAT + Y}$$

in units of μm , volts, seconds, I_{off} in $\text{nA}/\mu\text{m}$ at stress condition (such as burn-in), Y in [%], SAT is a parameter to account for saturation effects.

The parameters A , V_0 , b and n are given in Table 5-7, “DG NFET Hot Carrier Non-conducting Model Parameters”.

Table 5-7. DG NFET Hot Carrier Non-conducting Model Parameters

Use Mode	A (mean)	A (2 σ WC)	b	V_0	n	SAT
Forward Saturation	530	954	-5.1	50	0.50	15
Reverse Saturation	3000	4590	-4.6	50	0.45	22

Narrow Device Correction: For device design widths of less than one μm , the multiplier 1.25x should be applied

Device Characteristics: The observed effect of hot carrier injection on an NFET device is dependent on the measurement conditions applied after stress. Reverse mode refers to the situation where a device is measured with its source and drain connections reversed relative to those during stress. Thus, the reverse saturation degradation is important when a device is used bidirectionally, as in a pass gate. Observed I_D degradation is more severe than the average for V_{GS} near V_T and less severe for V_{GS} near V_{DD} . The increase in inverse average drain current approximates the increase in the delay (rising v_{GS} to falling v_{DS}).

5.3.1.5 Conducting hot carriers: Thin Oxide (2.2 nm) P-channel Devices

The PFET channel hot carrier effect is due to a mixture of interface state generation and charge trapping, and is more complex than NFET behavior. Significant degradation occurs when the gate voltage is between V_T and V_{DS} , and V_{DS} is large. The device degradation is characterized by both a threshold voltage increase and a reduction in device drain current over time. The device damage is localized near the drain, resulting in an asymmetry in the post stress device characteristics.

The following is a model of the conducting PFET channel hot carrier effect. The model is derived at ($V_{GS} \sim V_{DS}$). This is the maximum degradation point for all I_{eff} 's. However, in actual use the degradation will peak somewhat below $v_{GS} \sim v_{DS}$, making the effective duty cycle (or $t_{\text{eq}} / t_{\text{use}}$) less than that for NFETs, as seen below in the time calculation section. This model does not include saturation effects, which tend to reduce the degradation above 50%. This equation covers all use temperatures and design widths.

Degradation Equation:

The degradation is given in percent by:

$$\frac{\Delta I_D}{I_D} = A \times L_{eff}^m \times \exp\left(\frac{-V_0}{V_{DD}}\right) \times t_{eq}^n$$

in units of μm , volts, and seconds. The time t_{eq} is defined below. The parameters A, m, V_0 and n are given in Table 5-8, “PFET Hot Carrier Conducting Model Common Parameters $T_{ox}=2.2\text{ nm}$ ” and Table 5-9, “PFET Hot Carrier Conducting Model ‘A’ Parameter for $T_{ox}=2.2\text{ nm}$ ”.

Table 5-8. PFET Hot Carrier Conducting Model Common Parameters $T_{ox}=2.2\text{ nm}$

Use Mode	m	V_0	n
Forward Saturation	- 3.14	20.3	.305
Reverse Saturation	-3.14	20.3	.305

Table 5-9. PFET Hot Carrier Conducting Model ‘A’ Parameter for $T_{ox}=2.2\text{ nm}$

Use Mode	Mean	Worst Case (+3 σ)
Forward Saturation	1.75	3.2
Reverse Saturation	2.2	4.18

Time Calculations: Hot carrier effects occur in PFET devices when V_{DS} is close to V_{DD} and appreciable I_D is flowing. For typical CMOS circuits, these conditions occur only during switching transients. In this case, equivalent stress time can be approximated by,

$$t_{eq} = D \times \left(\frac{f_{sw}}{f_{cl}}\right) \times t_{use}$$

where,

f_{sw} = average switching freq (CYCLES/sec)

f_{cl} = clock frequency

t_{use} = actual use time in sec and,

D= 0.001 for short V_{GS} and V_{DS} transition times (< 0.05 x t_{cyc} , 10-90%)

0.005 for moderate V_{GS} or V_{DS} transition times (0.05 to 0.15 x t_{cyc} , 10-90%)

0.05 for long V_{GS} or V_{DS} transition times (0.15 to 0.30 x t_{cyc} , 10-90%)

Another way of estimating t_{eq} is the total time spent between the following two waveform events: V_{GS} reaching V_T and $|V_{DS}|$ falling to $V_{DD}/(1+(V_{DD}/V_0))$, times the factor $\exp 2.0(V_{DD}^{-1}-|V_{DSCO}|^{-1})$, where V_{DSCO} is the voltage at which V_{DS} crosses V_{GS} .

Care must be taken when operating devices with persistent drain currents. In these cases, V_{DS} must be kept low, or associated circuits designed to tolerate significant degradations.

High Temperature Correction: For junction temperatures other than 30 C, the calculated degradation does not require correction.

Device Characteristics: The observed effect of hot carrier injection on an PFET device is dependent on the

measurement conditions applied after stress. Reverse mode refers to the situation where a device is measured with its source and drain connections reversed relative to those during stress. Thus, the reverse saturation degradation is important when a device is used bidirectionally, as in a pass gate. Observed I_D degradation as a function of V_{GS} increases as V_{GS} decreases (down to V_T). The net effect over the whole V_{GS} range (above V_T) can be approximated by a *simultaneous* current multiplier (given by a dependent current source), and an effective V_T shift (given by a voltage source). The current source J_{deg} is in parallel but opposite direction to the J_{ds} source in the device model (so as to lower the effective drain current), and the voltage source V_{deg} is in series with the gate, opposing the turn-on of the device (that is, negative towards the gate.) The values of J_{deg} and V_{deg} are given by:

$$J_{deg} = C \times \left(\frac{\Delta}{1 + \Delta} \right) \times J_{DS}$$

$$V_{deg} = B \times \Delta$$

where,

$\Delta = \Delta I_{ON}/I_{ON}$, expressed as a fraction, and the parameters C and B are given by:

Table 5-10. PFET Hot Carrier Degraded Model Parameters

Device	C	B (V)
2.2nm Tox NFET	0.37	0.35
5.2nm Tox NFET	0.55	0.72

Note: Do not confuse V_{deg} with the *actual* threshold shift, which is larger than V_{deg} .

Example: A 2.2nm Tox PFET in an inverter circuit is operated for 100,000 hour with switching transient of moderate transition times once every 10 ns clock cycle. $V_{DD} = 1.5$ V, and minimum $L_{eff} = 0.08$ μ m. $t_{eq} = 0.005 \times (50 \text{ MHz}/100 \text{ MHz}) \times 3.6E8 \text{ sec} = 900,000 \text{ sec}$. Using the model parameters for forward saturation yields a Drain current degradation= 0.77% ($A=3.2$ WC) for the PFET. $J_{deg}=0.003 \times J_{ds}$, $V_{deg}=2.5$ mV.

Specific Device Concerns: The following are some specific PFET uses that must be examined in detail.

- Burn-in conditions
- Bidirectional devices - stressing a device in both directions is more severe than 2X the stress time in one direction
- D.C. current flow
- Heavily loaded circuits such as Off-chip Drivers (OCD's) and Clock Drivers
- Circuits such as OCDs which may see voltage overshoots or undershoots
- Mixed voltage interface circuits or any circuit using greater than 1.95 V.

- Circuits with long rise and/or fall times such as OCDs
- Circuits where V_T or I_D matching is critical

5.3.1.6 Conducting hot carriers: Regular I/O Thick Oxide (DG, 5.2 nm) P-channel Devices

The DGPFET channel hot carrier effect is due to a mixture of interface state generation and charge trapping, and is more complex than NFET behavior. Significant degradation occurs when the gate voltage is between V_T and V_{DS} , and V_{DS} is large. The device degradation is characterized by both a threshold voltage increase and a reduction in device drain current over time. The device damage is localized near the drain, resulting in an asymmetry in the post stress device characteristics.

The following is a model of the conducting DGPFET channel hot carrier effect. The model is derived at ($V_{GS} \sim V_{DS}$). This is the maximum degradation point for all L_{eff} 's. However, in actual use the degradation will peak somewhat below $V_{GS} \sim V_{DS}$, making the effective duty cycle (or t_{eq} / t_{use}) less than that for NFETs, as seen below in the time calculation section. This model does not include saturation effects, which tend to reduce the degradation above 50%.

Degradation Equation:

The degradation is given in percent by:

$$\frac{\Delta I_D}{I_D} = A \times L_{eff}^m \times \exp\left(\frac{-V_0}{V_{DD}}\right) \times t_{eq}^n$$

in units of μm , volts, and seconds. The time t_{eq} is defined below. The parameters A , m , V_0 and n are given in Table 5-11, "PFET Hot Carrier Conducting Model Common Parameters $Tox=5.2nm$ " and Table 5-12, "PFET Hot Carrier Conducting Model 'A' Parameter for $Tox=5.2nm$ ".

Table 5-11. PFET Hot Carrier Conducting Model Common Parameters $Tox=5.2nm$

Use Mode	m	V_0	n
Forward Saturation	-3.56	46.2	.45
Reverse Saturation	-3.56	46.2	.45

Table 5-12. PFET Hot Carrier Conducting Model 'A' Parameter for $Tox=5.2nm$

Use Mode	Mean	Worst Case (+3 σ)
Forward Saturation	64.5	190
Reverse Saturation	85.5	252

Time Calculations: Hot carrier effects occur in PFET devices when v_{DS} is close to V_{DD} and appreciable i_D is flowing. For typical CMOS circuits, these conditions occur only during switching transients. In this case, equiv-

alent stress time can be approximated by,

$$t_{eq} = D \times \left(\frac{f_{sw}}{f_{cl}} \right) \times t_{use}$$

where,

f_{sw} = average switching freq (CYCLES/sec)

f_{cl} = clock frequency

t_{use} = actual use time in sec and,

$B = 0.001$ for short v_{GS} and v_{DS} transition times ($< 0.05 \times t_{cyc}$, 10-90%)

0.005 for moderate v_{GS} or v_{DS} transition times (0.05 to $0.15 \times t_{cyc}$, 10-90%)

0.05 for long v_{GS} or v_{DS} transition times (0.15 to $0.30 \times t_{cyc}$, 10-90%)

Another way of estimating t_{eq} is the total time spent between the following two waveform events: V_{GS} reaching V_T , and $|V_{DS}|$ falling to $V_{DD}/(1+(V_{DD}/V_0))$, times the factor $\exp 2.0(V_{DD}^{-1}-|V_{DSCO}|^{-1})$, where V_{DSCO} is the voltage at which V_{DS} crosses V_{GS} .

Care must be taken when operating devices with persistent drain currents. In these cases, V_{DS} must be kept low, or associated circuits designed to tolerate significant degradations.

High Temperature Correction: For junction temperatures other than 30 C, the calculated degradation does not require correction.

Device Characteristics: The observed effect of hot carrier injection on an PFET device is dependent on the measurement conditions applied after stress. Reverse mode refers to the situation where a device is measured with its source and drain connections reversed relative to those during stress. Thus, the reverse saturation degradation is important when a device is used bidirectionally, as in a pass gate. Observed I_D degradation is more severe than the average for V_{GS} near V_T and less severe for V_{GS} near V_{DD} . The increase in inverse average drain current approximates the increase in the delay (falling $|V_{GS}|$ to rising $|V_{DS}|$).

Example: An inverter circuit is operated for 50,000 hour with switching transient of longer transition times once every 10 ns clock cycle. $V_{DD} = 2.5$ V, and $L_{eff} = 0.17 \mu m$, $t_{eq} = 0.05 \times (50 \text{ MHz}/100 \text{ MHz}) \times 1.8E8 \text{ sec} = 4.5E6 \text{ sec}$. Using the model parameters for forward saturation yields a Drain current degradation = 0.48% (worst case, A equals 94.6) for the DGPFET.

Specific Device Concerns: The following are some specific PFET uses that must be examined in detail.

- When $V_{DS} > 2.75$ It is recommended to use stacked devices and/or longer channels
- Burn-in conditions
- Bidirectional devices - stressing a device in both directions is more severe than 2x the stress time in one direction
- D.C. current flow
- Heavily loaded circuits such as Off-chip Drivers (OCD's) and Clock Drivers
- Circuits such as OCDs which may see voltage overshoots or undershoots
- Mixed voltage interface circuits or any circuit using greater than 3.6 V.
- Devices operated with substantial n-well bias.
- Circuits with long rise and/or fall times such as OCDs

- Circuits where V_T or I_D matching is critical

5.3.1.7 Non-conducting hot carriers: Thin Oxide P-channel Devices

No significant shifts during the high voltage and high temperature stresses are expected.

5.3.1.8 Non-conducting hot carriers: Regular I/O Thick Oxide (DG) P-channel Devices

The V_t of DGP-FETs under this condition decreases (a current increase) due to electron trapping effects. For a wide device ($W > 5 \mu\text{m}$, each finger), the shift in I_D is projected to be less than 1% for a 48 hr. burn-in at $T = 140^\circ\text{C}$, and $V_{dd} = 3.8 \text{ V}$. For a narrow device, the shift can be larger, for example, for $W = 0.5 \mu\text{m}$, a shift as high as 2-3% is possible. This current increase will tend to decay with use operation, and the conducting degradation mechanism will dominate.

5.3.2 Gate Oxide Dielectric Integrity

Gate dielectric integrity is mainly driven by random process defects. Therefore, reliability failure rates will depend on the total gate oxide area. To reduce the impact of reliability fails caused by these defects, the following rules need to be observed. The more “RECOMMENDED” rules one follows, the lower the impact of gate oxide defects on overall chip reliability.

For maximum oxide voltages V_{max} in I/O design, see section 4.22 , “Mixed Voltage Interfaces” on page 325.

Below is a list of two general categories of capacitors and the reliability rules that need to be applied.

- Decoupling Capacitors
 - N-well to substrate capacitors are preferred for use as decoupling V_{dd} and ground
 - An alternative ‘nFET-in-nwell’ design, described in section 4.8 , “NCAP and DGNCAP Models” on page 273 has been qualified as well.
- Capacitors used in leakage sensitive analog circuitry. (ex. Phase Locked Loop)
 - Large area thin oxide capacitors **MUST** be designed by connecting small area ($230 \mu\text{m}^2$ maximum for polysilicon) plates in parallel. However, it is RECOMMENDED that $45 \mu\text{m}^2$ plates be used instead. (See Design Rules 132 and 132R)
 - All polysilicon gates (FETs and capacitors) **MUST** meet groundrules 130, 131 and 132.
 - It is RECOMMENDED that circuitry be implemented to allow voltage screen capability at wafer final test to reduce reliability impact during life.
 - To minimize the contribution of gate to diffusion related failures, capacitors **MUST** be designed to minimize gate to diffusion perimeter. (i.e. place polysilicon edges over isolation oxide where possible.)

- Avoid large areas of thin oxide capacitors. These increase the likelihood of defect related chip failure. A thin oxide capacitor device in the BiCMOS8HP technology is the PCDCAP (this device is also referred to as ncap or nFET-in-N-Well MOS Capacitor).

- Guidelines:

To assure that decoupling capacitors have a negligible effect on reliability and yield, it is recommended that:

1. Total Active Area with decoupling capacitors / Total active area without decoupling capacitors ≤ 1.02
2. If a design requires more decoupling capacitors, the failure rate will scale approximately with the ratio given above. For example: 100 K μm^2 total, including decoupling capacitors, divided by 90 K μm^2 results in a failure rate that is 11% higher than if no decoupling capacitors are used.

For the purpose of these guidelines, the following definitions apply:

- Decoupling capacitor
 - Any thin dielectric (oxide, nitride, or oxynitride) capacitor connected between a power supply and ground for the purpose of noise reduction. These may be implemented as MIM capacitors, or CMOS devices that are wired as capacitors (source and drain connected together as one electrode and the gate as the other electrode).
- Active Area
 - Total gate area of CMOS transistors + Total capacitor area + (if present in the technology) the total RX area of npn transistors and junction diodes.

5.3.3 Forward Bias Injection Threshold Shifts (FITS)

FITS refers to the trapping of carriers injected from forward biased junctions. Individual device degradation due to FITS is highly layout dependent. Use of circuits which result in forward biased junctions is not recommended because of FITS, Hot Carrier, and Latchup concerns.

5.3.4 Threshold Voltage Stability

5.3.4.1 Substrate Hot Carriers

The Substrate Hot Carrier mechanism refers to the device degradation that occurs as a result of thermally generated carriers in the depletion regions of reverse biased junctions. These carriers can be injected into the gate oxide of a device resulting in threshold voltage shifts. No significant shifts during the high voltage and high temperature stresses have been measured.

5.3.4.2 Ionic

The presence of ionic contaminants in MOS devices introduces parametric instabilities. The threshold voltage shifts caused by these mechanisms are listed in the following table. No ionic shifts have been observed to date in this technology. The following table for the 5.2 nm devices is based on theoretical line control capabilities. For the thin oxide (2.2 nm) shifts smaller than 1 mV are expected at end of life.

This table represents the maximum total shifts expected due to Substrate Hot Carriers and Ionic Contamination. Non-ionic shifts for PFETs are not included and must be treated independently. All circuits must be designed to tolerate the combined maximum shifts of all mechanisms.

<i>Table 5-13. End-of-Life V_t Shifts (100,000 Power-on Hours)</i>			
Device Type	Max V_t Shift	Max V_t Mismatch	
		Adjacent	Non-adjacent
5.2nm NFET	-35/ +15 mV	15 mV	35 mV
5.2nm PFET	-35/+35 mV	15 mV	35 mV

5.3.4.3 Non-Ionic (NBTI)

The PFET device exhibits an increase in non-mobile positive charge during symmetric (source=drain) stress which is named Negative Bias Temperature Instability (NBTI). This shift results in larger magnitude threshold voltages over time ($|I_D|$ decreases).

Thin oxide pFET devices with gate oxides in the 1.6-2.3 nm range

Nominal case is given by:

$$\Delta V_T(\text{millivolts}) = \frac{500 \times Z}{(500 + Z)}$$

Worst case is given by:

$$\Delta V_T(\text{millivolts}) = 1.6 \times \frac{500 \times Z}{(500 + Z)}$$

Where:

$$Z = 1312.5 \times \exp\left(\frac{-0.188}{k \times T_j}\right) \times \left(\frac{|V_g|}{t_{ox}}\right)^{2.976} \times t^{0.202} \times |V_{t0}|^{0.199} \times \left(1 + \frac{0.117}{W_D}\right)$$

NBTI is more pronounced in narrow device smaller 1 μm . The design width (WD) dependence is explicitly given in the expression above. Designer are required to simulate their circuits under these conditions.

Regular I/O DG 52A pFET devices with gate oxides in the 4.6-5.3nm range

Nominal case is given by

$$\Delta V_T(\text{millivolts}) = \frac{600 \times Z}{(600 + Z)}$$

Worst case is given by

$$\Delta V_T(\text{millivolts}) = 1.6 \times \frac{600 \times Z}{(600 + Z)}$$

Where:

$$Z = 1048 \times \exp\left(\frac{-0.183}{k \times T_j}\right) \times \left(\frac{|V_g|}{t_{ox}}\right)^{2.744} \times t^{0.253} \times \left(1 + \frac{0.072}{W_D}\right)$$

with

WD = device width in micrometers

V_g = gate to source stress bias in volts

T_{ox} = gate dielectric thickness (nm)

T_j = stress temperature in Kelvin

t = time in seconds

k = Boltzmann's constant (8.62E-5 eV/K)

V_{to} = Threshold voltage (at 70nA x W/L) at stress temperature.

Based on combined worst case conditions, all circuits must be designed to tolerate these maximum predicted shifts.

Example: A logic part is burned-in for 5 hours at 140 C. What is the worst case threshold shift for a 5.2 nm PFET with W = 2.0μm Worst case |V_{GS}| = 3.3V, t=18,000 sec. Using the model parameters yields a ΔV_T = 33.7 mV.

5.3.4.4 Corrections to the above DC Models:

The above models are developed under the conditions of a constant DC gate bias, and V_{DS} = 0V. Under typical AC conditions (for digital applications) in which the gate bias will switch off at least 10% of the time, a factor of 0.6 may be applied to these DC models (multiply by 0.6).

If the device is in saturation while the gate bias is applied (such as in an analog application), and LDES ≥ 2x L_{min}, then a factor of 0.5 may be applied. Caution: Analog modes such as power down, which apply high

gate bias and no drain bias, will see 100% of the DC model predictions.

5.3.5 Using Device Degradation Data

The threshold voltage shifts and current degradations presented in this section are not all directly additive. The ultimate threshold voltage or drain current is determined as follows:

NFET V_T at End of Life (EOL) = $V_T(t_0) + \Delta V_T$ (stability)

NFET or PFET I_D at EOL = $I_D(t_0) \times (1 - \Delta I_D)$

PFET V_T at EOL = $V_T(t_0) + \Delta V_T$ (stability) + ΔV_T (hot carriers)

Degradation for different V_D bias conditions (at a given stress mode: for instance, peak substrate current, or peak gate current) in equations that are not linear in time cannot be added linearly. The Hot Carrier and Non-Ionic Stability mechanisms fall into this category. In order to calculate total degradation for more than one stress condition within a given stress mechanism, the user must linearize the degradation for each condition by raising it to the '1/n' power where 'n' is the exponent in the time term (assuming all stress conditions have the same n). These linearized degradations can then be added and the result converted back to a final degradation by raising to the nth power. This is summarized below:

$$\Delta_{tot} = (\Delta_1^{1/n} + \Delta_2^{1/n} + \Delta_3^{1/n})^n$$

ΔV_T (Stability) is additive. Use ΔV_T (Ionic) plus ΔV_T (Non- Ionic).

PFET degradations from Negative Bias Temperature Instability and Hot Carrier mechanisms are directly additive. (Apply the threshold shift AND the current degradation.)

To add NFET degradations from non-conducting and conducting mechanisms, use the following approximation:

$$\Delta_{tot} = (\Delta_{NC}^2 + \Delta_C^2)^{1/2}$$

For bidirectional stress, however, the degradations from forward and reverse stresses should be directly added.

5.3.6 Soft Error Rate

The radiation induced soft error rate for all SRAM cells ($\geq 4K$ bits) **MUST** be modeled by computer simulation to estimate the fail rate, and thus the system impact. In this section, all dimensions are actual wafer dimension.

A soft error on a memory element occurs when a transient current spike flips a bit without physically damaging the chip. Memory elements which are known to experience soft errors include SRAM cells, DRAM cells, and some dynamic logic circuits. These errors typically result in a system error or crash, program error, or loss of data integrity. Soft errors result from naturally occurring ionizing radiation, including alpha particles

from the radioactive decay of heavy elements and by-products of collisions between cosmic rays and silicon nuclei.

The following table includes preliminary estimates of the Soft Error Rate (SER) for a particular BiCMOS8HP SRAM cell. By definition 1 FIT = 1×10^{-9} failures per hour.

<i>Table 5-14. Example of Modeled C4 alpha SER and Cosmic SER</i>			
2.48 μm^2 SRAM Cell	Cosmic	C4 (125 on 225)	Package Factor (1 alpha/cm²/Khr)
1.2 V	550 FIT/Mb	4000 FIT/Mb	2000 FIT/Mb
1.5 V	400 FIT/Mb	2000 FIT/Mb	1400 FIT/Mb

The largest alpha particle source on many logic chips is the lead-tin solder used to make C4 solder balls. Lead ²¹⁰Pb, which can not be practically separated from the other lead isotopes, decays through ²¹⁰Bi into ²¹⁰Po. ²¹⁰Po then decays with the emission of a 5.3 MeV alpha particle into ²⁰⁶Pb. Alpha particles interact with the silicon atomic lattice, losing energy with the creation of electron-hole pairs at the rate of 3.6 eV/pair (44fC/MeV). Linear charge densities approach 15fC/ μm along the alpha track, much of which is collected in 100 picoseconds. Low alpha lead may be available to minimize alpha SER to approximately one tenth the rate.

Some ceramic substrates emit alpha particles, but in most products these alphas are stopped before they reach active devices in the silicon with clean fillers (like epoxy) used between the chip and the substrate.

Most wirebond package materials have low alpha emissions. For most wirebond products, the alpha SER is insignificant relative to the cosmic ray-induced SER.

The alpha induced SER is expressed as FIT per C4 over the array of SRAM cells. The SER is calculated assuming a 4 mil C4, with epoxy used between the chip and the ceramic substrate. Chips with a 50% populated 4 mil C4 on a 9 mil pitch with the above cell sizes will have about 14 kbit per C4. If there are 5 C4s over an array of Cell7.0 cells on a chip with 4LM (4 Level Metal), the C4 SER component would be 5 C4s x 585 FIT/C4 = 2925 FIT. The C4 induced SER is very sensitive to the charge in the storage node (Qcrit). A 10% decrease in Qcrit (i.e. drop in voltage) will increase the C4 SER of Cell7.0 by approximately 50%. For this cell, approximately 0.1% of the C4 induced soft errors are multiple bit fails.

The sensitivity to cell design results from the high sensitivity of C4 SER on Qcrit. SER can drop more than 100X with a small change in cell area. C4 SER is more sensitive to design than cell area. This complex dependence on cell design explains why the SER needs to be modeled for each cell design. If the C4 alpha SER is less than the cosmic SER there would be little advantage in removing C4s from over an array.

The alpha SER is increasing with each new technology. With smaller cell designs, fewer alphas hit the cell area, but more of them cause fails. The charge produced by the alpha has not changed appreciably because the vertical profiles have not been changed appreciably as the dimensions and operating voltages decrease. Meanwhile, the capacitance and voltage on the SRAM node are decreasing, leading to a decreasing critical charge required to flip the cell. The trend of increasing C4 alpha SER needs to be taken into account for designs planning to migrate into future technologies.

Additional levels of wiring increase the amount of material between the C4 and the silicon. This reduces the

number of alphas reaching the silicon. When a filler is used between C4s (like epoxy), the alphas emitted from the side of the C4 are harmlessly absorbed by the filler. Any sensitive circuits which are more than 30 μ m from the edge of the C4 (30 μ m from the C4 ball, not the 47 μ m TV window) will not be affected by the alpha emitted from that C4. Thus, if alpha sensitive circuits are not placed under or near C4s, they will not suffer an increased level of SER (above the background cosmic SER level).

Other logic circuits (especially dynamic logic and latches) may also be susceptible to C4 induced soft errors. As a rough guide, circuits which can withstand 30fC of charge injected in a 50ps pulse (approx 5ps linear rise time, exponential decay with a time constant of 40ps) are probably not susceptible to C4 induced SER.

Cosmic rays reach the surface of the earth in the form of high energy protons and neutrons. These particles occasionally collide with silicon nuclei, producing alpha particles and heavier energetic nuclei. The heavier nuclei behave similar to alphas, except they can produce up to 10 times the charge density produced by alphas. Thus, circuits which are immune to alphas may still be sensitive to cosmic radiation. Shielding of cosmic radiation is not practical. Many dense cell designs have a cosmic SER of around 1FIT/kbit = 1 fails/1E12 bit hours = 1ppm/(kbit-kpoh). Cosmic ray induced SER is relatively insensitive to Qcrit. Evidence of the existence of cosmic ray induced SER was obtained by comparing soft fail rates of parts at high altitudes, sea level and underground (T. O’Gorman, IEEE Trans. ED, Vol 41, No 4, p. 553).

Logic circuits may also be susceptible to cosmic ray induced soft errors. As a rough guide, circuits which can withstand 200fC of charge injected in a 50ps pulse (approx 5ps linear rise time, exponential decay with a time constant of 40ps) are probably not susceptible to terrestrial cosmic rays.

Many suppliers do not include cosmic ray induced soft errors in their SER estimates. Cosmic SER estimates and sensitivities can not be determined from accelerated alpha particle testing.

Maximizing the critical charge required to flip the state of a node reduces the SER. The critical charge required to flip the state of SRAM cells is determined by the operating voltage, the capacitance of the internal nodes, and the current drive of the PFET in 6 device cells (4 NFET/2 PFET). Unit capacitance increases in low voltage technologies (thinner oxides, narrower depletion widths) tend to offset the impact of lower operating voltage on Qcrit. In 6 device cells, the charge collected by the NFET diffusions accounts for the majority of soft errors. This occurs because the NFET diffusions are larger than the PFET diffusions and the PFETs provide less current drive to maintain the node voltage. Wider PFETs reduce SER by increasing the current drive which restores hits on the NFET diffusions and increasing node capacitance without significantly increasing charge collection. Maximizing gate capacitance tied to a storage node will reduce the SER. Error recovery circuits can also be very effective for reducing SER. Arrays with error detection or recovery should be designed such that bits in the same error check word are physically separated to minimize the impact of multi-bit SER events. Parity detection may be used to protect data integrity.

5.3.7 Resistor Reliability

5.3.7.1 Front-End of Line Resistors

P+ polysilicon are limited to 0.4mA/ μ m unless further limited by metal electromigration as described below, under the assumption that the metal line is the same temperature as the resistor.

Resistors can heat up to a point where metal migration becomes an issue. Tabulated guidelines assume that the resistors are laid out with the metal leading to the resistor as wide as the resistor. This is for DC conditions for 100,000 hours of operation at the silicon temperature indicated.

P+ Polysilicon Resistor current limitations:

<i>Table 5-15. P+ Poly Resistor current limitations</i>		
SiTemp C	3.6V	5.5V
125	0.31 mA/μm	0.30 mA/μm
120	0.37 mA/μm	0.35 mA/μm
115	0.40 mA/μm	0.39 mA/μm
≤ 110	0.40 mA/μm	0.40 mA/μm

RR Polysilicon Resistor current limitations:

With the allowed current density of 0.1mA/μm and 1700 Ω/□, the maximum heat generated by the RR resistor will be less than 5 degrees C.

For P+ poly resistors, electromigration may be evaluated for specific cases by calculating the temperature rise for the resistor and using the electromigration limits from the Back-End-Of-Line reliability section under the assumption that the metal line is the same temperature as the resistor. AC operation can have a much relaxed criteria but 0.40 mA/μm absolute maximum should be maintained.

The formula for thermal resistance (THERMRES) is:

$$THERMRES = 144150 \times AREA2^{-0.87121}$$

where,

AREA2 = (AREA + 5 x WIDTH)

AREA is the area of the resistor (μm²)

WIDTH is the resistor width (μm)

The Resistor temperature (ResTemp) is then:

$$ResTemp = SiTemp + (THERMRES \times Power)$$

where, SiTEMP is the base silicon temperature (degrees C) and Power is the dissipated power in the resistor (Watts)

5.3.7.2 Back-End-Of-Line KQ Resistors

Caution: KQ resistors can produce high temperatures that can compromise integrity of metal lines leading up to the resistor as well as metal lines adjacent to the resistor. Adjacent resistors can heat each other compromising the resistor precision.

The maximum allowed current through any KQ resistor is 0.5mA/μm of width unless the metal leading to the resistor limits the current to a lower value or the change in resistance through life is more than the circuit can tolerate.

Table 5-16. KQ Resistor maximum current limits

Si Temp C	KQ maximum current limit (mA/μm) ¹ for each BEOL metal option		
	for 3 Levels of Copper Metal [M1, M2, MQ] (5 Total Levels of Metal)	for 4 Levels of Copper Metal [M1, M2, M3, MQ] (6 Total Levels of Metal)	for 5 Levels of Copper Metal [M1, M2, M3, M4, MQ] (7 Total Levels of Metal)
< 70	0.50	0.50	0.50
80	0.50	0.50	0.472
90C	0.474	0.444	0.422
100C	0.410	0.386	0.368
110C	0.341	0.324	0.310
120C	0.270	0.258	0.248
125C	0.233	0.224	0.217

1. Maximum KQ resistor current limit using a 30μm wide resistor and only the LY design level for its wiring. Limits in table are instantaneous peak, at no time should dc+ac current exceed values shown in table. If the resistor experiences an AC signal then, the peak current must be less than or equal to these limits. Values increase if AM and LY design level wiring are used in parallel for electromigration considerations or the KQ resistor width is less than 30μm. However, the maximum allowed current limit for any KQ resistor is 0.50 mA/μm.

Some layouts can tolerate higher current densities (all must be less than 0.5mA/μm). If the initial layout does not meet the critical current density above then the following calculations can be done.

Calculate thermal resistance ThR, which varies by the number of thin copper metal present:

$ThR = 7.514 \times 10^5 \times Area^{-0.8639}$ for 3 levels of copper metal, M1, M2, MQ (5 total levels of metal).

$ThR = 6.332 \times 10^5 \times Area^{-0.8220}$ for 4 levels of copper metal, M1, M2, M3, MQ (6 total levels of metal).

$ThR = 5.150 \times 10^5 \times Area^{-0.7801}$ for 5 levels of copper metal, M1, M2, M3, M4, MQ (7 total levels of metal).

Note: Total levels of metal is the sum of the copper metal levels (M1, M2, MQ plus optional M3 or M4) in addition to LY and AM metal levels.

Where Area is the area of the resistor in microns squared. ThR is in Degrees C/Watt. The power in the resistor should be calculated, then knowing the resistor area, the temperature increase of the resistor can be calculated. By adding the resistor temperature increase to the Base Silicon temperature the temperature of the resistor (and connecting metal) is then determined. The electromigration limitations for that temperature can be calculated from section 5.4.2. Using the equations in Section 5.4.2, "Structures of Concern: ILCs and Line Rules" on page 359 tradeoffs for duty cycle can also be made.

Metal lines or other resistors within 10 μ m of the heated resistor will see 40% of the increase in temperature caused by the heated resistor. Metal lines or resistors at 30 μ m away will see a temperature rise of 20% of the increase in temperature. Metal lines within these distances need to be designed wide enough to tolerate the higher temperatures. The metal lines above or below the KQ resistor must be designed to tolerate the same temperature as the heated resistor itself. Resistors requiring high precision should be kept far apart (>40 μ m) such that heating from adjacent resistors do not influence the high precision resistor value.

5.3.8 Bipolar Reliability

Design Analysis Strategy

NPN reliability is determined by the amount of current which is conducted in a forward bias mode and the voltage which is imposed on the Emitter-Base junction in a reverse bias mode. NPN stability is assured by limiting the amount of forward bias current and voltage imposed on the EB junction. It is the duty of the designer to adhere to the design limitations for all elements of the chip. The devices should be designed such that the contacts and metal coverage meet the reliability groundrules for intended operation conditions.

5.3.8.1 Exceptions

Because the device rules are generic and cover most conceivable designs, they contain certain embedded assumptions which might be overly conservative for particular designs. Thus, in addition to general adjustments of the rules based on different applications, a limited number of exceptions which allow marginal violations of the rules may be allowed in particular design circumstances. These will have to be approved by Reliability Engineering (Dept. 25M/AR1). **Please contact your IBM Product Engineer about any exceptions.**

5.3.8.2 NPN Forward Bias Degradation

Contact Limitations:

When designing with the small NPN device (such as 0.12x0.64 μ m), which has a 0.20 μ m x 0.60 μ m emitter contact bar, be sure to follow the electromigration guidelines for the emitter. You may want to consider having the emitter contacted through a vertical stack comprised of CEBAR, M1, V1 and M2. This will minimize the electromigration impact on this device. The 0.20 μ m x 0.60 μ m emitter contact stud is rated for a maximum current of 1.32mA at 125°C (6.54mA at 100°C).

Device Characteristic Changes With Time:

With current flow through the emitter device characteristics will change with time. For example, base current will increase. There is an oxide between the polysilicon and the crystal emitter Silicon. As current passes through this oxide, it is hypothesized that the interface properties are altered, changing the base current.

Other characteristics will change as well.

Over time, the base current is expected to shift to a maximum of 25% from its Tzero value in the typical device operating range. The change in the collector current should be within 5% of the initial Tzero value in the typical device operating range.

Designers must design their circuits to tolerate these parametric changes.

5.3.8.3 Emitter-Base Reverse Bias

The reverse bias of emitter-base junctions causes hot carriers damage at the junction. These hot carriers produce interface traps which increase the base leakage current and, thus, increase the base current non-ideality and decrease the gain of the device at low current level. Care must be exercised to ensure that the reverse bias across the emitter-base junction does not exceed 1.75 volts. Use above this limit results in device degradation, and the customer must contact IBM if the 1.75 Volt limit will be exceeded in the operation of any circuit.

5.3.8.4 Forward Bias Stability

Base current shift has been observed after high current forward bias stress. For applications where devices are biased at high J_c with sensitivity to low current beta shifts consult IBM Reliability.

5.3.8.5 Base-Collector Avalanche Bias Stability

The base-collector avalanche operation causes the increase of the base current non-ideality. As long you operate the devices with V_{BC} less than 1.5V, degradation is negligible, see section 5.1.1 , “Reliability Limitations” on page 332. In general, the bipolar reliability is limited by electromigration.

5.3.9 VPNP Bipolar Reliability

The Vertical PNP (VPNP) is limited to a maximum of $V_{ce}=3.6V$ (including power supply tolerances) and a maximum emitter current of $1.6ma/\mu m^2$.

The VPNP is susceptible to vertical hot electron effects from the collector base voltage and collector current. The net effect is to increase emitter current (decrease $F_{V_{be}}$) and also increase the base current as the hot electrons damage the perimeter of the base region. Voltage modeling indicates that for operation at $V_{cb}<2.6V$ ($V_{ce}<3.6V$) with an emitter current of $1.6ma/\mu m^2$ for 100000 hours the emitter current should increase less than 1.25%.

Base current can increase and the worst case added base current can be:

$$(\text{added } I_b) = 6.35E-14 \times \text{Area} \times \exp(V_{be} \times 38.61 / 2.54) \text{ amps}$$

where Area is the emitter area in μm^2

Circuits must be designed to tolerate the expected shift.

5.3.10 Metal to Metal Capacitor Dielectric Integrity

See section 4.22.9 , “VMAX for MIM Capacitor” on page 329

The total **maximum** MIMCAP area per chip is 1,000,000 μm^2 (exceptions are granted on a case by case basis. Please contact your IBM technical representative).

5.4 Back End Of Line (BEOL) Reliability Design Rules

5.4.1 Electromigration (EM)

5.4.1.1 Introduction

Electromigration refers to the gradual degradation of interconnects due to the combined effects of current and temperature. The following rules give designers the information needed to assure that electromigration will have a negligible impact on the reliability of BiCMOS8HP designs.

The rules do not address protection of circuits against extraordinary current/temperature situations like electrostatic discharge, electrical overloads, or latch up.

5.4.1.2 Design Analysis Strategy

Electromigration is analyzed by dividing interconnect networks into simplified elements: metal lines of a given width, contacts and vias which serve as interlevel connections to lines. It is a duty of the designer to make sure that the electromigration rules are followed for all elements of the design.

Designers should include the following activities in their design methodology:

- Use the Electromigration rule adjustments ("EM Rule Adjustments" on page 364) to determine the current limits for the circuit application being considered.
- Use the capacitive load of the circuit and the operating frequency to calculate the currents expected in the metal lines for comparison to the current limits. This simple check can be performed for each circuit node capacitance listed in the chip timing simulations.
- Use a circuit simulator to calculate the currents in the metal interconnects where an EM problem is suspected or where greater accuracy is required. Particular attention should be paid to the following cases (this is NOT an exhaustive list):
 - Off chip drivers, which may have to drive very large loads
 - Power buses. Check for hot spot where demands for current from several circuits may accumulate along the length of a bus line
 - Any circuit where a DC current is present.

Because the EM rules are generic, they contain imbedded assumptions which might be overly conservative for particular designs. Thus, in addition to general adjustments of the rules based on different applications, a **limited** number of exceptions which allow **marginal** violation of the rules may be allowed in particular design circumstances.

5.4.1.3 Application Assumptions and Rule Adjustments

The rules as listed are based on an assumed product life of 100,000 hours and an assumed **junction temperature of 100°C**, unless stated otherwise. Adjustment factors for other life times and temperatures are given. When applications are more stringent, the adjustment factors **must** be applied. When applications are less stringent, adjustment factors should be used **only** when it is absolutely certain that the designs will never be used at more stringent conditions.

5.4.1.4 Terminology and Symbol Definitions

- **Contact (CA):** stud connection from M1 to diffusion and polysilicon.
- **Via:** connection between any 2 metal levels (M1 and above).
- **Interlevel Connection (ILC):** general term for a contact or via
- **Fully Bordered ILC:** ILC designed with enough metal bordering to assure full line/ILC intersection even when maximum allowed line/ILC misalignment occurs.
- **Operating Switching Time (t_{sw}):** minimum time between successive current switching operations.
- **Current Operating Frequency (f_{sw}):** $1/t_{sw}$
- **Switching Factor (s):** fraction of operating cycles over the life of the product during which a given circuit switches.
- **Equivalent Average DC Current (I_{dc}):** $\frac{s}{t_{sw}} \int_0^{t_{sw}} i(t) dt$ **Note that for the case of pure ac current, I_{dc} is zero. For pure ac applications, the maximum current is defined by the I_{rms} limit.**
- **RMS Current (I_{rms}):** $\sqrt{s f_{sw} \int_0^{t_{sw}} i^2(t) dt}$
- **nLM:** n levels of metal technology, where n is an integer (e.g., 3LM is a 3 level metal technology).
- **LM:** planarized last metal.

5.4.2 Structures of Concern: ILCs and Line Rules

In general, the structural elements of concern are at or near interlevel connections (ILCs) to lines. The physical dimensions of importance are the cross sectional area of the line and the situation of the ILC with respect to the end of the line. **There is a significant penalty in allowed use current for the case of ILCs designed using minimum design rules. These limits are outlined in the following sections. In the future there may be a demonstrable benefit for ILCs designed with a full metal border or a metal extension as part of robust design practice.**

5.4.2.1 EM Fail Types and Corresponding Currents

Rules are given to protect against two types of current-induced fails: standard EM and local-heating enhanced EM.

For standard EM, the rules define a maximum I_{dc} .

For local-heating enhanced EM, the rules define a maximum I_{rms} .

The values of any calculated I_{dc} or I_{rms} in any simplified elements of an interconnection network must not

exceed the values given in the tables.

5.4.2.2 Equivalent dc Average Current Translations into Capacitances

For the typical CMOS situation where circuits are used to charge and discharge capacitances, the following

formula may be used to translate I_{dc} limits into capacitance limits:
$$C_{max} = \frac{I_{dc}}{s \times f_{sw} \times V}$$

For the case of pure ac current:
$$C_{max} = \frac{I_{rms}}{s \times f_{sw} \times V}$$

5.4.2.3 General Rules at 100C/100K POH

The following current limit values are subject to revision when additional qualification data has become available.

Table 5-1, “Current Limits at (100/125) degrees C (for PC, M1, M2, M3, M4, MQ, LY, AM)” on page 362 provides the maximum allowed I_{dc} and I_{rms} for each of the wiring levels. Note that no I_{dc} limit is stated for PC since it is not believed that standard EM is a concern for these levels. **Exceptions to these rules are listed in Table 5-2, “Exceptions to General Idc and Irms Current Limits for Contacts and Vias at (100/125) C”.** The general rules apply for all cases which are not listed in the exceptions tables.

In case of narrow stripes where a single via or contact is permitted along the width, the general rules can be applied by using the maximum number of contacts or vias along the line length. The general rules can be applied for cases of wide lines, provided the maximum number of contacts or vias allowed along the width are used. For a wide line crossing over a wide line, the general rules can be applied by using the maximum number of contacts or vias to create an L shaped array (See Figure 5-1). Additional redundant vias are recommended for use, where possible, subject to the constraints in section H.1.1, “Estimated Pattern Density Generation” on page 425.

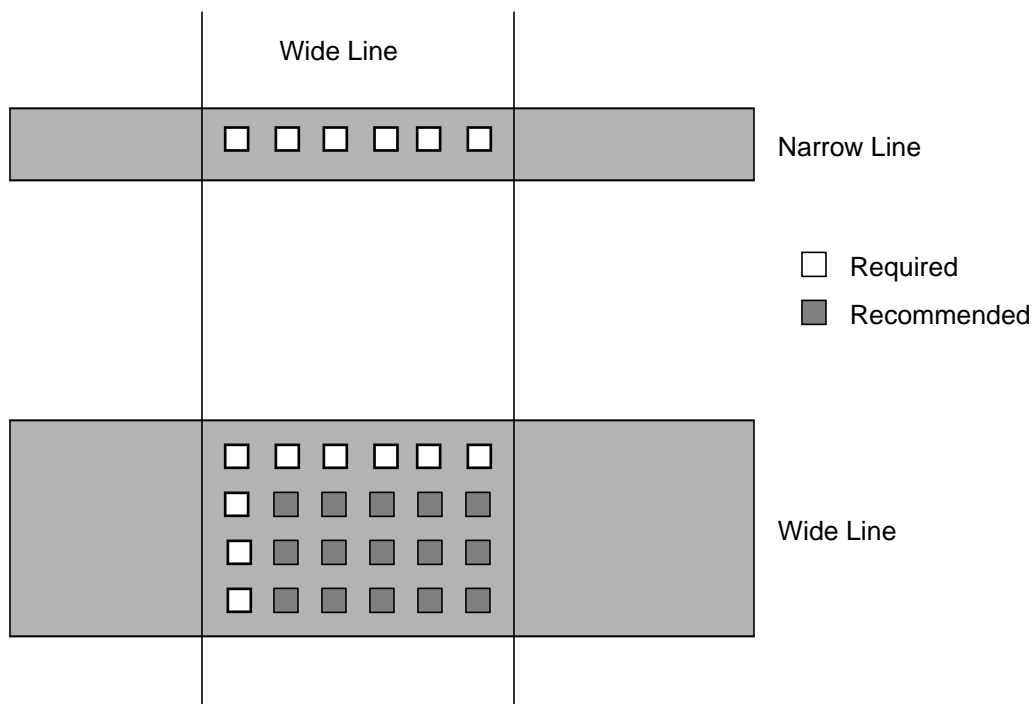


Figure 5-1. Recommended Via Placement for Wide Lines

5.4.2.4

Table 5-1. Current Limits at (100/125) ¹ degrees C (for PC, M1, M2, M3, M4, MQ, LY, AM) ²						
Metal Level	I _{dc} (mA) ³ at 100 C	I _{dc} (mA) ³ at 125 C	I _{rms} (mA) ³	I _{dc} ³ (mA) min. W at 100C	I _{dc} ³ (mA) min. W at 125C	I _{rms} ³ (mA) min. W
PC ⁴	N/A	N/A	$(0.61(W - 0.015))\sqrt{3.77 + \frac{4.54}{(W - 0.015)}}$	N/A	N/A	0.44
M1	2.80 (W - 0.06)	0.57 (W - 0.06)	$(7.52(W - 0.06))\sqrt{1.23 + \frac{3.56}{(W - 0.06)}}$	0.28	0.06	4.56
M2,	3.12 (W - 0.06)	0.63 (W - 0.06)	$(7.90(W - 0.06))\sqrt{0.69 + \frac{3.07}{(W - 0.060)}}$	0.44	0.09	5.26
M3	3.12 (W - 0.06)	0.63 (W - 0.06)	$(7.90(W - 0.06))\sqrt{0.47 + \frac{2.75}{(W - 0.060)}}$	0.44	0.09	4.96
M4	3.12 (W - 0.06)	0.63 (W - 0.06)	$(7.90(W - 0.06))\sqrt{0.36 + \frac{2.53}{(W - 0.060)}}$	0.44	0.09	4.75
MQ	5.40 (W - 0.07)	1.10 (W - 0.07)	$(10.35(W - 0.06))\sqrt{0.27 + \frac{2.45}{(W - 0.06)}}$	1.84	0.37	9.62
LY	1.78 (W - 0.04)	0.71 (W - 0.04)	$(11.71(W - 0.04))\sqrt{0.12 + \frac{2.11}{(W - 0.04)}}$	2.63	1.05	21.5
AM	5.70 (W - 0.11)	2.27 (W - 0.11)	$(20.94(W - 0.11))\sqrt{0.07 + \frac{2.16}{(W - 0.11)}}$	10.77	5.23	43.58

1. The correct I_{dc} values for the proper reference temperature must be used with the corresponding adjustment factors given in Table 5-4, "Adjustment Factors for I_{dc} only, for Temperature and Time, based on 100C and for 100,000 POH lifetime" on page 364 to obtain the correct current values for temperatures other than 100 or 125 degrees C.

2. The information shown supersedes the NPN device current ratings from the device properties.

3. W = design width. These numbers do not include the effects of tiling. For wires containing Metal HOLE shapes, the linewidth W must be replaced by the Effective Linewidth, W_{Eff}, as calculated from Table 4-32, "Effective Linewidth for Wires with HOLE Shapes" on page 286.

4. Limits apply to silicided polysilicon. For OP resistors, the current limits are identified in Table 4-17, "Resistor Design Specifications," on page 265 and Section 5.3.7, "Resistor Reliability" on page 353

5.4.2.5 Exceptions to General Rules for Vias

The following tables describe the exceptions to the general rules for vias. The allowable limit for the dc and rms current per via is given in Table 5-2. For multiple vias the allowed dc and rms currents are given by the allowable current per via times the number of vias. For the case of stacked vias or any other configuration of lines and vias, the current flowing through any single via may not exceed the values listed in Table 5-2. The current limit for the line rule given in Table 5-1, "Current Limits at (100/125) degrees C (for PC, M1, M2, M3, M4, MQ, LY, AM)" on page 362, must not be exceeded for any case.

<i>Table 5-2. Exceptions to General I_{dc} and I_{rms} Current Limits for Contacts and Vias at (100/125) °C</i>			
Level	I_{dc} Max Limit per Via at 100°C (mA)	I_{dc} Max Limit per Contact or Via at 125°C (mA)	I_{rms} Max Limit per Contact or Via (mA)
CA, V1	1.40	0.28	5.00
CABAR ¹	L x 10.9	L x 2.2	$(7.52(W + 0.02)) \sqrt{1.23 + \frac{3.56}{(W + 0.02)}}$
CEBAR ¹	L x 10.9	L x 2.2	$(7.52(W + 0.28)) \sqrt{1.23 + \frac{3.56}{(W + 0.28)}}$
V2,V3	1.40	0.28	7.85
VL	6.16	1.25	18.4
VY	9.18	1.86	34.4
VYBAR ¹	L x 7.4	L x 1.5	$(11.71(W + 2.6)) \sqrt{0.12 + \frac{2.11}{(W + 2.6)}}$
AV	8.62	3.4	33.0
AVBAR ¹	L x 7.0	L x 2.8	$(20.94(W + 2.5)) \sqrt{0.07 + \frac{2.16}{(W + 2.5)}}$

1. L = length of via bar.

<i>Table 5-3. Rules for C4 Terminals at 125 degrees C</i>			
Design Size LV DIA	Line into C4 pad	Width of line into C4 pad (μm)	Max I_{dc} (mA) at 125°C
47.0	AM	≥ 37	84 mA per C4

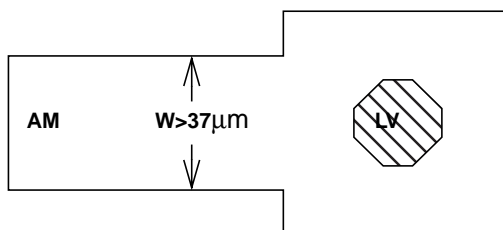


Figure 5-2. Examples of Designs which follow Exceptions Rules in Table 5-3, "Rules for C4 Terminals at 125 degrees C," on page 363.

5.4.2.6 EM Rule Adjustments

The I_{dc} limits in the preceding tables may be adjusted for cases of isolated lines, product life times other than 100,000 hours, and junction temperature limits different from 100°C as indicated in the following tables.

Notes:

1. No adjustment for the local-heating EM (I_{rms}) is allowed
2. Care must be taken to insure the adjusted I_{dc} current(s) in this section do not exceed the I_{rms} current values given in Table 5-1, "Current Limits at (100/125) degrees C (for PC, M1, M2, M3, M4, MQ, LY, AM)," on page 362 for the corresponding line widths.

Table 5-4. Adjustment Factors for $I(dc)$ only, for Temperature and Time, based on 100C and for 100,000 POH lifetime

Adjustment For:	Multiplier
Temperature for Cu Wiring including CA, Mx, Vx, VL, MQ, VY, and negative C4's where wires into the C4 pad are Cu	$F(T) = e^{\left(\frac{9495}{T_{max}(^{\circ}K)} - 25.45\right)}$
Time for Cu Wiring including CA, Mx, Vx, VL, MQ, VY, and negative C4's where wires into the C4 pad are Cu	$F(EOL_{actual}) = \left(\frac{110000}{10000 + EOL_{actual}}\right)^{0.909}$
Temperature for Al wiring including LY, AM, and negative C4's where wires into the C4 pad are Al	$F(T) = e^{\left(\frac{5461}{T_{max}(^{\circ}K)} - 14.64\right)}$
Time for Al wiring including LY, AV, AM, and negative C4's where wires into the C4 pad are Al	$F(EOL_{actual}) = \left(\frac{110000}{10000 + EOL_{actual}}\right)^{0.588}$
Temperature positive C4s only - (Vdd Pad)	$F(T) = e^{\left(\frac{4255}{T_{max}(^{\circ}K)} - 11.4\right)}$

Table 5-4. Adjustment Factors for I_{dc} only, for Temperature and Time, based on 100C and for 100,000 POH lifetime

Adjustment For:	Multiplier
Time positive C4s only- (Vdd Pad)	$F(EOL_{actual}) = \left(\frac{110000}{10000 + EOL_{actual}} \right)^{0.555}$

NOTE: Using the temperature and life time adjustment factors to justify higher current usages should be contemplated **only** when the lower application end-of life or temperature is **absolutely certain**. Designing with such a derivation in effect inherently limits the applications of the product.

I_{dc} limit for interconnects for a given junction temperature, T, and for a given product lifetime, EOL_{actual} , can be calculated using the following relation:

$$I_{dc}(T, EOL_{actual}) = I_{dco} \times F(T) \times F(EOL_{actual})$$

where

$$(EOL_{actual}) = POH \times I_{dc}DutyFactor$$

$I_{dc}DutyFactor$ is the fractional part of POH during which the I_{dc} flows in metal/contact/via, and $I_{dco} = I_{dc}$ limit at 100°C and for 100,000 POH product Life. The values of F(T) and F(EOL_{actual}) for contacts, vias, and lines are given in the following tables.

Table 5-5. I_{dc} Temperature Adjustment Factors

Temperature (°C)	Cu Multiplier	Al Multiplier	Positive C4 Multiplier
50	51.7	9.65	5.89
60	21.4	5.81	3.97
70	9.32	3.60	2.73
80	4.25	2.29	1.92
90	2.03	1.50	1.38
100	1.00	1.00	1.00
110	0.517	0.683	0.748
120	0.275	0.475	0.564
125	0.203	0.399	0.492

Table 5-6. I_{dc} Time Adjustment Factors

POH	Cu Multiplier	Al Multiplier	Positive C4 Multiplier
40,000	2.05	1.59	1.55
50,000	1.73	1.43	1.40
75,000	1.26	1.16	1.15
100,000	1.00	1.00	1.00
110,000	0.924	0.950	0.953
150,000	0.711	0.802	0.812
200,000	0.556	0.684	0.698

5.4.2.7 I_{dc} Exceptions to General Rules for Short Lengths

Line lengths (**L**) <10 μm with widths (**W**) <2xWmin (Wmin = minimum line width) could have increased I_{dc} values. Any **Cu line on levels M1, M2, M3, M4, or MQ** within these limits can operate at a higher I_{dc} limit.

To calculate the I_{dc} limit:

Use calculated I_{dc} values from Table 5-1, “Current Limits at (100/125) degrees C (for PC, M1, M2, M3, M4, MQ, LY, AM),” on page 362 and Table 5-4, “Adjustment Factors for I_{dc} only, for Temperature and Time, based on 100C and for 100,000 POH lifetime,” on page 364.

If I_{dc} is less than the maximum current limits given in Table 5-7, “Maximum I_{dc} Current Limit for Short Length Applications”, apply the following equation:

$$I_{dc}(\text{Short Length}) = I_{dc}(\text{Calculated}) \times (10/L)$$

Table 5-7. Maximum I_{dc} Current Limit for Short Length Applications

Level	Max. Current Limit (mA)	I_{dc} , Max @ 2xWmin (mA)
M1	5.83(W-0.06)	1.52
M2, M3, M4	6.50(W-0.06)	2.21
MQ	11.25(W-0.07)	8.33

M1 wires with lengths (L) <10 μm could have another short-length exception for high temperature applications (e.g. >105C) regardless of their widths, and this exception is specifically for M1 connected to bipolar devices with elevated junction temperature up to 160C.

Use the following Table 5-8 to calculate the I_{dc} values with this M1 short-length exception for junction temperature up to 160C.

<i>Table 5-8. Maximum I_{dc} Current Limit for M1 Short Length Application at High Junction Temperature</i>		
Level	Max. Current Limit at 100C¹²	Max. Current Limit at 125C
M1	2.3(W-0.06)	2.3(W-0.06)

1. Note that in situations where this exception applies, the I_{dc} value calculated using the table above is independent of temperature up to 160C junction temperature during operation. It is critical to keep the junction temperature below 160C in order to utilize this exception. No further increase in I_{dc} value is allowed based on this exception, and the only adjustment necessary and required is for “Time for Cu Wiring” in Table 5-4 on page 364 to decrease I_{dc} value for lifetime > 100,000 POH.

2. It is absolutely important for designers to follow the current limits of contacts and vias connecting M1. Although this M1 short-length exception is temperature independent up to 160C junction temperature, the current limits of contacts (CA and CABAR) and vias (V1) have to scale with temperature following Table 5-2 on page 363

5.4.3 Metal Corrosion

For corrosion protection, no exposed metal lines (other than wirebond pads, if applicable) are allowed.

5.4.4 No Polyimide Feature

While the use of the No Polyimide Feature is not believed to have a significant impact on the Reliability of the part, IBM makes no claims to the reliability of the product when the No Polyimide feature is utilized.



6.0 Electro-static Discharge (ESD) Protection

The ESD kit is provided as part of the BiCMOS8HP device library. A brief description of ESD primitive Parameterized Cells (PCells) is in Table 6-1. A brief description of ESD hierarchical Parameterized Cells (PCells) is in Table 6-2.

<i>Table 6-1. ESD Primitive Pcell</i>	
ESD Primitive Pcell	Description
esdndsx	N+ Diffusion to Substrate Diode
esdnwsx	N-Well Diffusion to Substrate Diode
esdvpnp	P+ Diffusion to N-Well Diode

<i>Table 6-2. ESD Hierarchical Pcell</i>	
ESD Primitive Pcell	Description
double_diode_n	Double Diode
antiparallel_diodes	Anti-parallel Diodes
rc_clamp	1.5 V RC Triggered (PFET Resistor) ESD Clamp
rc_clamp25	2.5 V RC Triggered (PFET Resistor) ESD Clamp
darlington_clamp	SiGe Darlington ESD Clamp

6.1 General

Protection networks and proper circuit design are required on all external pins to prevent damage from an Electro-Static Discharge (ESD) event. The ESD event used for qualification is the Human Body Model (HBM) in positive and negative pulse mode defined by the EOS/ESD standards committee. For designs with wide market applications, ESD conformance should be demonstrated to military (MIL-STD-883D Method 3015.7), JEDEC (JC-14.1-92-103), and EOS/ESD Association (EOS/ESD-S5.1-1993) standards. This is achievable by providing good pin-to-rail, pin-to-pin and rail-to-rail ESD protection.

Full compliance may not be practical for RF and sensitive analog pins. In this case, the maximum practical ESD protection should be achieved consistent with performance requirements.

6.1.1 IBM Designs

The IBM HBM objective for ESD protection is to withstand 4000 volts without 50% pin degradation and/or chip functional failure, relative to each independent power supply rail (e.g. V_{dd} , V_{ss} , $V_{dd}(OCD)$, $V_{ss}(OCD)$). The IBM objective for machine model (MM) is 400 V. The IBM objective for charged device model (CDM) is 1000 V. For CDM testing, functional testing is mandatory for evaluation.

All I/O circuitry designs, power bus architecture and ESD design implementation **MUST** be reviewed with the ESD design manual owner prior to design definition, design submission, redesigns and until design sign-off is complete as part of the design checkpoint process.

6.1.2 OEM/Foundry Designs

Digital, supply, and ground pins are required to meet a minimum of 2kV HBM. IBM will review designs for ESD protection on request.

RF and sensitive analog pins which do not have the recommended ESD protection device, or do not comply with the guidelines of this document, *must* be reviewed with IBM to assure that low protection levels will not compromise manufacturing yield. Contact IBM Technical Representative to arrange this review.

6.2 Usage Rules

1. ESD PAD RULE: All chip pads that have external connections must be connected to an ESD Protect Circuit or an IBM-supplied self-protecting I/O cell.

RF and sensitive analog pins which cannot achieve functional objectives when used with ESD protect devices, due to ESD capacitance loading must review circuit implementations with the ESD design manual owner or IBM Applications Engineering and address ESD protection by improving the ESD robustness of the RF pins by self-protecting concepts and other ESD techniques. ESD robustness of these pins can not be guaranteed without ESD device usage.

2. ESD POWER CLAMP: ESD Power Clamps **MUST** be placed on all chips whose capacitance is less than 100 nF between V_{cc} and V_{ss} .
3. MULTIPLE POWER DOMAINS: An ESD device must exist between separate power domains. In the case where no element is desired between power domains, an ESD Power Clamp must be placed between the power and ground rails. See section 6.4.3 , “ESD Power Clamps” on page 374.
4. MULTIPLE SUPPLY VOLTAGES: When multiple supply voltages exist on a chip (e.g., on-chip 3.3V power pin and a 2.5 V internal supply voltage) an ESD device **MUST** be used so that a current path exists between all pins and BOTH power supplies. If this is not possible, an ESD Power Clamp must be placed between the power supply and ground rails. Supply-to-supply ESD protection circuits improve pin-to-supply protection levels and allow for pin-to-pin ESD testing
5. MULTIPLE GROUND DOMAINS: When multiple ground buses exist (e.g. off chip driver noisy bus V_{ss} (OCD) and substrate chip ground V_{ss}), an ESD device **MUST** be used between the V_{ss} and $V_{ss}(OCD)$ power buses.
6. ANALOG-TO-DIGITAL DOMAINS: Analog and Digital Power Domains must be intercoupled by ESD devices. A diode, diode string, or sequence -independent ESD devices can be used. If analog and digital power grids can not be coupled for noise reasons, then an ESD POWER CLAMP must be used between the Analog VDD and VSS, and between V_{cc} and V_{ss} .

7. **INTERNAL VOLTAGE REGULATORS:** Internal voltage regulators must have an ESD bypass circuit element which allows current transfer from V_{cc} to V_{dd} . This is achieved with an NFET based voltage regulator, diode string or an “off” NFET in parallel with the PFET based voltage regulator.
8. **CDM CONSIDERATIONS:** CDM events will impact inductors, capacitors and SiGe npn transistors on input circuitry in receivers and off-chip-drivers. Elements must be sized to address the current magnitude associated with CDM events. See EOS/ESD CDM specification.

A p-n diode **MUST** be placed near any structure that needs ESD protection (e.g. CMOS receiver gate that is far from an input pad). In this case, a p-n diode or grounded gate NFET must be placed between the n-channel source and gate. If the n-channel source is attached to a V_{ss} rail which is not chip substrate then the p-n diode must be connected to the said power rail. A resistor element must also be used in series with the gate to limit the current in the CDM test mode.
9. **PROGRAMMABLE VDD:** Programmable V_{dd} which contains active circuitry must have its own ESD protection circuit or ESD protection on the V_{dd} power supply. Programmable V_{dd} that does not wire out to a wire bond pad must have sufficient floating gate tie downs and self protection to avoid Electrical Over-stress (EOS) or /ESD damage in the probing and manufacturing sectors. Wirebonding to the V_{dd} should precede wire bonding to the programmable V_{dd} pad. *Programmable V_{dd} should be connected to chip substrate if possible when not in use.*
10. **ACTIVE CLAMPS:** Active clamp networks, used for high performance applications to avoid system level ringing, must use ESD networks to adequately protect the active clamp. Active clamp NFET's should be wider than 80 microns. Small active NFET clamps tied to V_{dd} and V_{ss} have shown to destruct in ESD testing.
11. **MULTIPLE CHIPS IN A MODULE:** Chips used in Multiple Chip Modules (MCM) may omit full ESD protection on intra-module connections, but adequate protection must exist to prevent damage during test and assembly. Pads connecting two chips in a given module which are connected to an external pin must have an ESD device contained within one of the two chips when there exists a current path to both chips V_{dd} and V_{ss} power grids. When the V_{dd} and V_{ss} power grids are disconnected, an ESD device must exist on both chips. If multiple implementations are available in the chip design, the unused designs should be connected to chip substrate.

6.3 Placement and Wiring

1. **ESD DEVICES UNDER PADS:** ESD devices may be placed under C4 and wire bond pads, though wire bond pads have some restrictions.
2. **WIRING/VIA SIZING:** All connections between pad and the ESD protect circuit must comply with section 6.10 , “Electro-static Discharge (ESD) Wiring Rules” on page 386.
3. **WIRING ORDER:** ESD protect device **MUST** be wired first except in the case of inductor elements. In this case, the inductors must follow the ESD Wiring Rule and ESD Via and Contact Rule Sections. When routing between C4 solder ball or pad structure, the ESD protection should precede any active circuitry if possible.
4. **ESD SHARING:** Input receivers connected to a common pad can share ESD devices if the V_{dd} and V_{ss} bus resistances are less than 3Ω to all input receivers connected to the common pad. A supply-to-supply ESD protect device can be shared by up to 25 I/O buffers. Diode string ESD protect devices can be shared among I/O to the V_{dd} power supply. Metal busing **MUST** be less than 1Ω between the I/O pad diode and the common node of the diode string.
5. **ESD POWER CLAMP PLACEMENT:** should be used for low capacitance chips, chips with multiple power supplies, power supply sequence independent applications, and to improve ESD protection on output pins. ESD Power Clamps can be placed in the corners of small chips (less than 3 mm edge) but it is best

to have ESD Power Clamps distributed along the power grid as much as possible to reduce power bus resistance losses between the ESD Power clamp and the ESD network. It is recommended to keep the power bus resistance between an ESD device (in the farthest cell from the ESD power clamp) and the closest ESD power clamp under 3 Ohms.

6. I/O TO RAIL ESD PLACEMENT RULE: Supply-to-supply ESD Protection devices must be placed less than 1000 μm from all I/O pads.
7. COMMON RAIL: ESD devices used on all driver pads should use the same V_{ss} rail and V_{dd} rail that is physically connected to the drivers (e.g., $V_{ss(I/O)}$ and $V_{dd(I/O)}$).
8. RESISTOR SHARING RULE: Receivers and drivers can share the same ESD resistor element.
9. ESD-TO-I/O PLACEMENT: ESD devices should be placed within 200 μm of the I/O cell. It is best to place the ESD device in the I/O cell.
10. DECOUPLING CAPACITORS: Placement of decoupling capacitors attached to the V_{dd} supply near the ESD device is recommended for improved ESD robustness. On chip decoupling between the power supply and ground should be maximized.
11. KEEPER CIRCUITS/FEEDBACK PFETs: Feedback PFET's that recouple to the input node must have high N-well series resistance to the V_{dd} power supply so the P+ drain does not forward bias during positive polarity ESD impulses. The PFET channel length should be at least 1 μm . The PFET well diode-series resistance should be greater than 500 ohms. A second solution is to introduce a self-biased well PFET to prevent forward biasing.
12. FEEDBACK NETWORKS: Activation of feedback networks by ESD events can occur. Adequate resistance isolation should be provided from the power grid in these types of networks.
13. BUS RESISTANCE: Power/ground bus resistance from the ESD device to nearest power/ground pad MUST be less than 3 Ω .
14. $V_{ss}(\text{OCD})$ RESISTANCE: Ground buses (e.g. $V_{ss}(\text{OCD})$) between the OCD circuit and the $V_{ss}(\text{OCD})$ pad must be kept below 1 Ω . Experimental results show rapid degradation in ESD protection as a function of $V_{ss}(\text{OCD})$ bus resistance.
15. $V_{ss}(\text{OCD})$ GUARD RING: An N-well guard ring tied to $V_{ss}(\text{OCD})$ around the NFET circuitry driver for split bus configurations protects NFETs from negative mode HBM impulses from adjacent pins when no $V_{ss}(\text{OCD})$ solution exists on the adjacent pin.

6.4 ESD Protection Circuits

A set of standard ESD protection circuits is available

If standard circuits are to be used as a basis for custom designs, these should employ devices from the BiCMOS8HP library to assure simulation and LVS support, and should be reviewed with IBM.

6.4.1 Single Supply Voltage ESD Protect Circuit

For I/O pads whose inputs do not exceed a diode voltage above the power supply, the double-diode network is used. Double diode networks are available with CMOS junctions (P+ to n-well and n-well to substrate diodes), SiGe junctions (npns), and Pwell to subcollector junction varactors. Custom networks can also be constructed. Designers should use supported pcells to maintain high frequency modeling capability.

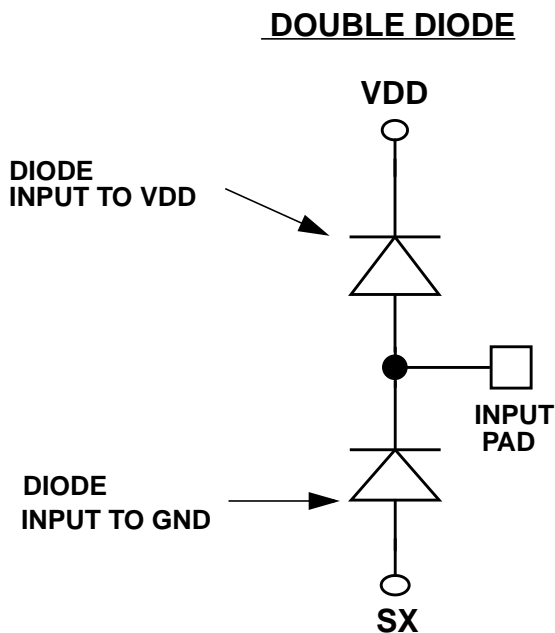


Figure 6-1. Double Diode ESD Network (Pcell name: double_diode_n)

Diode Size	Number of Anode Fingers	HBM ESD Failure (Volts)	TLP Failure (A)
28 μ m	1	1150	1.13
	2	2200	1.90
	3	3200	2.53
	4	4100	3.15
	6	5950	4.42

Table 6-3. Double Diode ESD Results (TLP Pulse Width = 100ns)

6.4.2 Supply-to-Supply ESD Protect Device

The Anti-parallel Diodes hierarchical pcell (refer to Table 6-2 on page 369) uses CMOS-based elements for this application. Back-to-back configurations to establish bi-directional current paths and maintain noise isolation needs can be achieved using the specific designs. It is the responsibility of the designer to determine the number of diodes necessary for noise, sequencing requirements and burn-in qualification.

6.4.3 ESD Power Clamps

ESD power clamps are to be used between power rails and ground (e.g. VDD and VSS) in low total capacitance chips, low capacitance power rails, multiple power supply chips, and chips with analog-digital noise isolation. These are also important to improve pin ESD protection for high frequency applications where the ESD network on the input pin is scaled down for performance reasons. Several options are available including grounded gate NFET, RC triggered, and bipolar elements.

RC Triggered (NFET Resistor) ESD Power Clamp

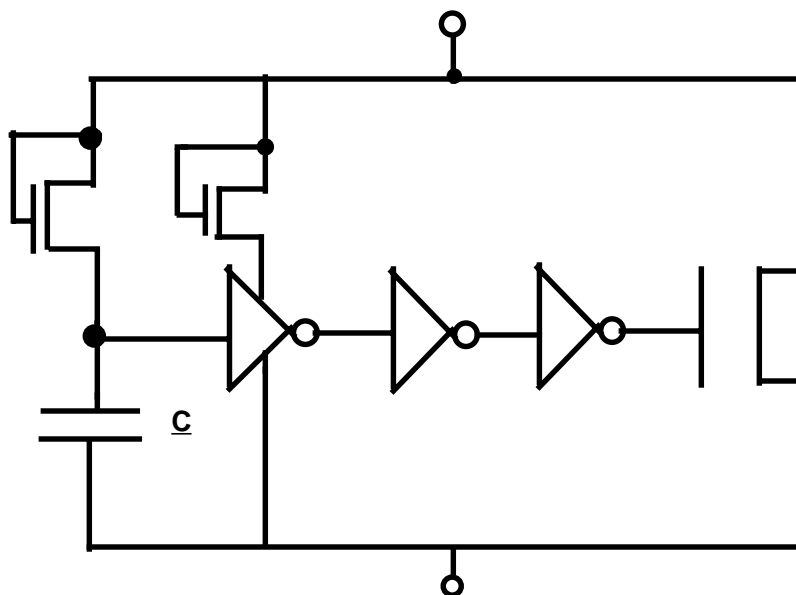


Figure 6-2. RC Triggered (NFET Resistor) CMOS Based ESD Power Clamp (pcell not offered in the design kit)

MOSFET-Width (um)	HBM ESD Failure of ESD Clamp (Volts)	MM ESD Failure of ESD Clamp (Volts)	TLP ESD Failure of ESD Clamp (Amps)
1000	1000	500	1.0
2000	3000	750	2.0
4000	5500	1000	4.0
8000	> 6000	> 1000	5.0

Table 6-4. RC Triggered (NFET Resistor) CMOS Based ESD Power Clamp HBM ESD Results

RC Triggered (PFET Resistor) ESD Power Clamp

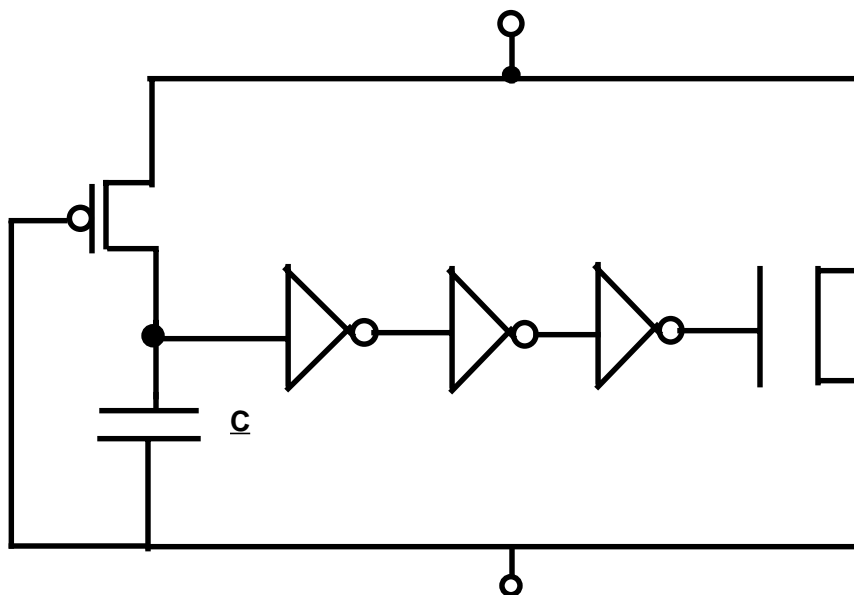


Figure 6-3. RC Triggered (PFET Resistor) ESD Power Clamp (pcell names: rc_clamp or rc_clamp25)

MOSFET-Width (um)	HBM ESD Failure of ESD Clamp (Volts)	MM ESD Failure of ESD Clamp (Volts)	TLP ESD Failure of ESD Clamp (Amps)
For estimated results, see Table 6-4 on page 374			

Table 6-5. RC Triggered (PFET Resistor) ESD Power Clamp HBM ESD Results

High Voltage RC Triggered ESD Power Clamp

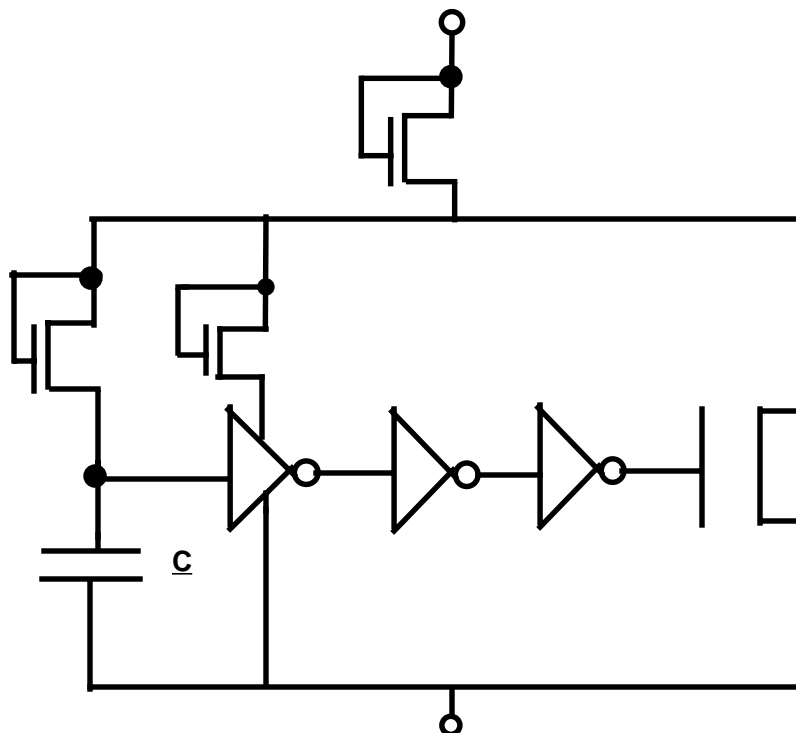


Figure 6-4. High Voltage RC Triggered CMOS Based ESD Power Clamp (pcell not offered in the design kit)

MOSFET-Width (um)	HBM ESD Failure of ESD Clamp (Volts)	MM ESD Failure of ESD Clamp (Volts)	TLP ESD Failure of ESD Clamp (Amps)
1000	1000	400	1.0
2000	3000	800	2.0
4000	5500	1000	3.0
8000	> 6000	> 1000	5.0

Table 6-6. High Voltage RC Triggered CMOS Based ESD Power Clamp HBM ESD Results

High Voltage RC Triggered (PFET Resistor) ESD Power Clamp

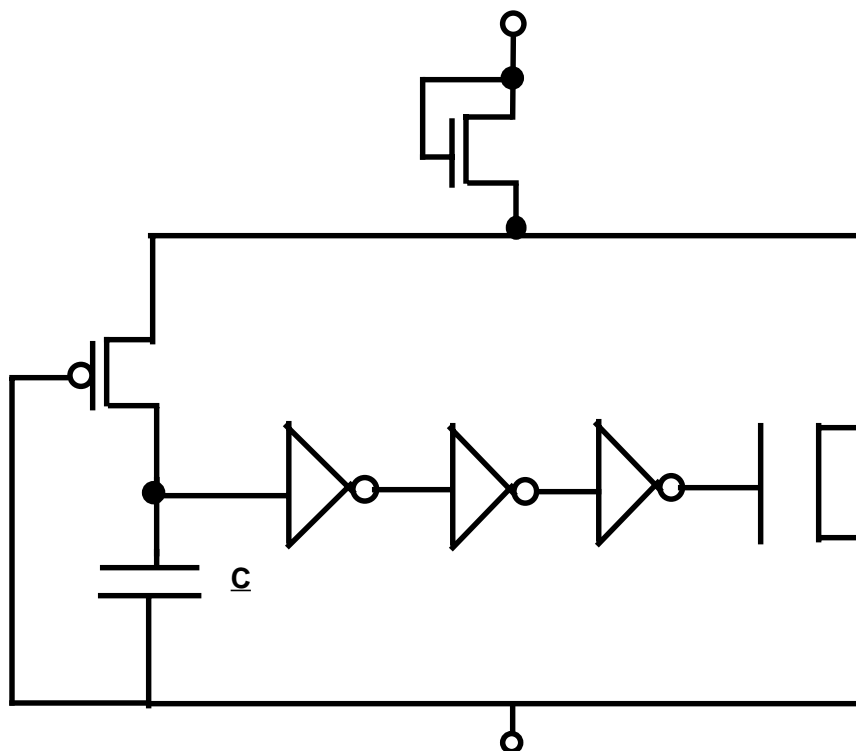


Figure 6-5. High Voltage RC Triggered (PFET Resistor) ESD Power Clamp (pcell not offered in the design kit)

MOSFET-Width (um)	HBM ESD Failure of ESD Clamp (Volts)	MM ESD Failure of ESD Clamp (Volts)	TLP ESD Failure of ESD Clamp (Amps)
For estimated results, see Table 6-6 on page 376			

Table 6-7. High Voltage RC Triggered (PFET Resistor) ESD Power Clamp HBM ESD Results

SiGe Darlington ESD Power Clamp

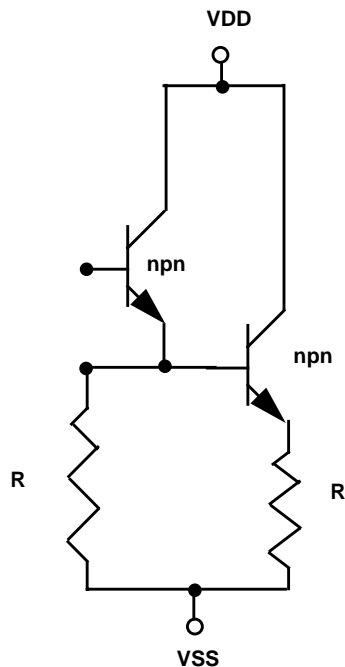


Figure 6-6. SiGe Darlington ESD Power Clamp (pcell name: darlington_clamp)

SiGe Darlington Variable Trigger ESD Power Clamp

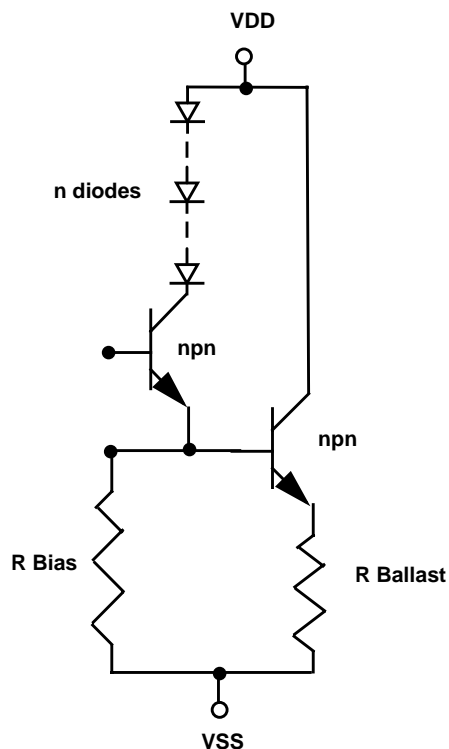


Figure 6-7. SiGe Darlington Variable Trigger ESD Power Clamp (pcell not offered in the design kit)

Trigger Transistor	Clamp Transistor	Number of Diodes (n)	Clamp Length (um)	HBM ESD Failure (Volts)	MM ESD Failure (Volts)	TLP Failure (A)
High Ft, Low BVceo	High BVceo, Low Ft	0	250	5900	630	2.1
		1	250	4700	540	1.6
		2	250	4400	540	1.3
		3	250	3900	510	1.0

Table 6-8. SiGe Darlington Variable Trigger ESD Power Clamp HBM, MM and TLP ESD Results (Preliminary data based on earlier generation technology offering)

Antiparallel Diodes

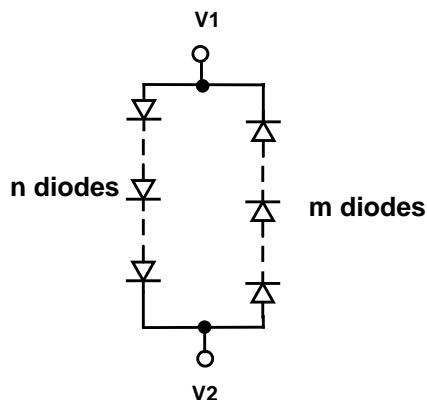


Figure 6-8. Antiparallel Diodes (pcell name: antiparallel_diodes)

Number of Diodes (m)	Number of Diodes (n)	Number of P+/NW Fingers (W = 28um)	HBM ESD Failure (Volts)	TLP Failure (A)
1	3	8	4300	3.95
1	3	6	3350	3.45
1	3	4	2350	2.70
1	3	2	1600	1.85
1	3	1	-	1.15
1	2	8	4300	4.80
1	2	6	4200	4.56
1	2	4	3450	3.84
1	2	2	2150	2.97
1	3	1	-	1.36
1	1	8	3600	4.64
1	1	6	3600	4.63

Number of Diodes (m)	Number of Diodes (n)	Number of P+/NW Fingers (W = 28um)	HBM ESD Failure (Volts)	TLP Failure (A)
1	1	4	3250	3.81
1	1	2	2000	2.19
1	1	1	-	1.32

Table 6-9. Antiparallel Diodes ESD Results (TLP Pulse Width = 100ns)

6.5 Device Considerations

CMOS-BASED DIODES: Stand-alone diodes may be constructed from CMOS-based junctions such as p+/N-well, n+/substrate, and N-Well/Substrate.

SIGE TRANSISTORS: Silicon Germanium transistors can be used as ESD elements in common-emitter, and emitter- collector modes for ESD protection. SIGE npn transistors can also be used in base-emitter modes, and base-collector modes in diode configurations. Experimental results shows that base-collector configurations are advantageous and will provide higher ESD robustness. Results also demonstrate that connection of both the emitter and collector as the cathode of the diode is not advantageous over base-collector diode configuration. Use only device library elements for ESD elements in order to insure dc and s-parameter support.

SiGe VARACTORS: SiGe Varactors can be used for ESD protection in a forward bias mode of operation. ESD results are linear in the width, but non-linear in the length dimension. Note that there is significant ESD roll-off for device longer than 10 um long.

Table 6-10. SiGe Varactor ESD Results			
Device (Varactor)	Width (μm)	Length (μm)	TLP Failure (A)
Width Study	1.0	20	0.4
	1.2	20	0.53
	1.4	20	0.576
	1.6	20	0.7
	1.8	20	0.793
	2.0	20	0.836
Length Study	2.2	20	0.965
	2.0	5	0.55
	2.0	10	0.9
	2.0	15	0.96
	2.0	20	0.97

RESISTORS: Resistor elements should be chosen to achieve linearity in the functional regime, and such that the resistors undergo velocity saturation in the high current ESD regime. Resistors should also be chosen to avoid breakdown during ESD events. It is suggested to use any of the supported resistors as defined in Section 4.7 “Resistor Models” on page 265. Use only supported resistor elements of the technology library elements in order to obtain model support. Nwell resistors are not supported in the BiCMOS8HP technology (see Section “List of devices or features that are not supported in the BiCMOS8HP technology:” on page 11). Do not use salicided polysilicon films as resistive elements for ESD protection (salicided resistors that do not use OP to block the salicide are not supported elements).

INDUCTORS: Inductors on input pads must be designed to withstand ESD events. Estimation of inductor ESD robustness can be evaluated from the critical-current-to-failure J_{crit} of an interconnect film. Use the LM metal level for the coil and only one level below for the underpass connections (LM, LM-1 levels). Underpass connection metal widths should be the same physical cross sectional area of the coil to avoid both resistive and ESD failure in the underpass wire interconnect. The number of vias in the inductors should also follow the ESD via rules.

CAPACITORS: **MIM and MOS decoupling capacitors are extremely sensitive to ESD. Unprotected MIMCAPs have failed at less than 100V HBM stress.** MIMCAP Capacitor elements can be used for RC Triggered networks or I/O applications where precision capacitance and voltage tolerance is required. MIMCAP capacitors should be designed to avoid interaction with adjacent circuitry when used in ESD applications.

ISOLATED FETS: Isolated Transistors can be used for ESD circuitry for low voltage trigger ESD networks and ESD Power Clamps.

6.6 SiGe NPN Transistors

ESD robustness of SiGe npn transistors is equivalent for pedestal and high breakdown devices. However, the different characteristics of these devices lead to different uses in ESD networks. The pedestal npn, with a lower breakdown voltage, should be used where this is advantageous, such as a trigger element for other elements. The high breakdown SiGe npn transistors can withstand larger applied voltages and have lower parasitic capacitance. These are well suited to BiCMOS based ESD Power clamps. Trench defined devices eliminate parasitic device concerns and allow for a more compact design. Though the thermal resistance is higher than non-isolated structures, no degradation in ESD performance has been observed.

6.6.1 SiGe NPN Transistor Receiver Design

Connections to the base and emitter should be broadside wired to avoid nonuniform current flow. Negative mode ESD performance improves with increase in the size of the receiver structure. Placing a second transistor in a cascode configuration below the emitter of the receiver will improve ESD robustness of the SiGe receiver. Adding a supported resistor element in series with the SiGe base improves ESD robustness of the transistor receiver. Adding resistance in series with the npn emitter improves ESD robustness and improves thermal stability of the SiGe npn receiver. Silicon Germanium npn transistors undergo velocity saturation for structures under 10 μm long enabling self ballasting effects in the base-collector or base-emitter junction. By introducing a plurality of parallel elements, as opposed to a single npn element, significant ESD ballasting can also be initiated.

High Breakdown NPN (no pedestal) and standard NPN can both be used on I/O networks. Both are acceptable to address functional loading vs. ESD tradeoffs

6.6.2 SiGe NPN Transistor Driver Design

A SiGe transistor driver should be wired broad side to avoid lateral voltage drops across the emitter or collector regions. Lateral bussing of the npn element will lead to current crowding and lower ESD results. If the base is being used to drive the bipolar current, use a second metal for the base, and connect the bipolar element broadside as well on the second level of metal. The wiring and vias should satisfy the ESD Wire and Via

Resistor ballasting for SiGe transistors in a common-emitter mode can be achieved by using a device library supported resistor element in series with each individual SiGe transistor. Resistor elements which have high linearity in the functional regime and undergo velocity saturation in a high current regime will be the most suitable resistor elements. Low doped silicon based resistors will provide the earliest saturation. Resistors in series with the collector will limit the voltage stress in common collector mode. Resistors in the emitter will improve the thermal stability of the SiGe transistor.

6.7 CMOS Receiver Circuits

The following rules are to prevent gate input failure:

1. All input pads should use the same V_{ss} rail and V_{dd} rail that is physically connected to the receiver (e.g., $V_{ss(I/O)}$ and $V_{dd(I/O)}$).
2. It is recommended to use a bidirectional I/O instead of stand-alone receivers where the driver is disabled by connecting the driver gate NFET and PFET's to V_{ss} and V_{dd} respectively through a soft inverter dummy load. The dummy inverter can not be tied to the V_{dd} of the output stage.
3. STAND ALONE RECEIVERS: Stand alone receivers should use a 250 Ω resistor in series with the receiver gate and a grounded gate NFET transistor connected to ground for best ESD robustness.
4. SHARING RESISTOR ELEMENTS: In Bi-directional I/O circuitry, the driver and receiver can be attached to a common resistor element.

6.8 ESD CMOS FET OCD Design Rules

Optimal results will be achieved by layout practices resulting in maximum uniformity of current and thermal distributions.

6.8.1 CHANNEL LENGTH

I/O devices can use channel lengths of any supported length. Longer channel lengths will have higher snap-back voltages. Devices with multiple gate fingers must be designed with uniform channel length.

Gate conductor gate-to-gate spacings in OCD circuitry must be uniform to avoid pitch-dependent linewidth bias variations between gate fingers. DO NOT design a multi-finger NFET with variable gate-to-gate spacings. This is for the case of either single NFETs or stacked NFETs.

6.8.2 CHANNEL WIDTH

Multi-finger NFETs must have identical device widths for all fingers except in the case of variable impedance drivers. Variable impedance driver networks should add local resistor ballasting to avoid this concern. Where multiple FETs are tied to the same node, it is preferable to use identical widths and tie off the unused gates.

6.8.3 CONTACTS AND VIAS

Contact density should be maximum and contact-to-contact spacing must be uniform. N-channel Devices connected to external pads **MUST** be designed with 1.5X larger than the minimum gate-to-contact spacing on the n-channel node tied to the pad.

DO NOT place V_{dd} or V_{ss} bus vias or contacts over the NFET or PFET device. This leads to non-uniform thermal breakdown.

Minimize the distance from the N-well contacts to the PFET junction(s) connected to the I/O pad. Similarly, minimize distance from the substrate contact to the NFET junction(s) connected to the I/O pad. Best results will be obtained if N-well contacts are placed between PFETs and substrate contacts are placed between NFETs in the OCD.

6.8.4 WIRING

FETs in receiver networks should be broadside wired to avoid voltage drops along the length of the MOSFET during an ESD event. If this is not possible, such as when multiple gate fingers are used, the connections should be wired such that the current flow of the source and drain in the interconnects enters and exits opposite ends of the FET, and the wire width should be such to minimize voltage drops along the length of the MOSFET.

M2-to-M1 via placement must be uniform when wiring multi-finger NFET structures. Equal via numbers should be used for each set of NFET fingers.

6.8.5 RESISTOR BALLASTING

Resistor ballasting of FETs will improve ESD robustness. Use SBLK resistor elements. These are diffusion resistors with contacts on only one side, the other side being abutted to the source or drain of the FET. Ballast resistors should be placed close to the FET, and can be used on the drain or source terminal. Best results are obtained when both terminals are ballasted.

6.8.6 SERIES CASCODED N-CHANNEL FET's

Gate-to-gate spacing of series NFETs sharing the same RX area must be at least of 1.25 μm , to with 1.75 μm preferred. The source of the upper NFET must be separated from the drain of an adjacent NFET by at least 2 μm to avoid interactions leading to anomalously low snapback voltage.

DO NOT use NFET stack OCD designs where the NFET's are separated spatially in two areas and whose source is tied to V_{ss} (OCD) in conjunction with a double diode ESD design whose diode is between V_{dd} and V_{ss} , when V_{ss} and V_{ss} (OCD) are not connected on chip. Severe ESD damage will occur in negative and positive HBM modes to V_{ss} (OCD).

In drivers employing series NFETs, where the gate of the device connected to the pad is tied to Vdd, n+ diffusion floating gate tie down diodes must be located at least 2 μm from the NFET drain junction.

For mixed voltage interface networks, a series resistor of at least 5 Ω is required to achieve good ESD results.

6.8.7 ESD Self-protecting OCD Circuits

OCD designs which have sufficient robustness to meet ESD objectives without the need for an additional protection device are said to be “self-protecting”. These self-protecting features are advised even ESD protect structures are employed. For GTL/HSTL and variable impedance drivers, some of these techniques can be adapted where suitable>.

STANDARD CMOS DRIVERS

For the NFET, self protection is achievable using individual resistor ballast elements with each finger of the NFET driver. A resistor is integrated with each finger of the NFET OCD driver circuit. For self protecting I/O, the resistor can not be placed in front of the PFET. For the PFET, enclosed PFET transistors will be superior to non-enclosed PFET gate layouts. This is achieved using a polysilicon ring around the PFET drain. For the PFET, a local N⁺ N-well contact for each PFET finger must be used according to the specific layout as shown. Additional self protecting layouts will be supported when ESD robustness is demonstrated on product chips. The above layout integrates the resistor elements into the NFET design layout. Layouts with individual resistors in series with NFET fingers are in the process of demonstration. In the case where a resistor element is connected prior to the PFET, an ESD device is mandatory.

CMOS SELF-BIASED WELL, MIXED-VOLTAGE INTERFACE DRIVERS

For self-biased well drivers (which uses PFET control circuitry for well bias control), self protecting features can be implemented by integrating resistors with each finger of the NFET series stacked OCD transistor. For self bias well PFET's, it is not necessary to have a local N⁺ N-well contact between each PFET finger in the PFET of the OCD. The specific NFET layout should be used of the self protecting driver unit cell. Six cells are advised for good ESD robustness. Good design practices should be employed in the PFET layout.

SELF-PROTECTING CMOS I/O CELL

INTEGRATED RESISTOR IMPLEMENTATION

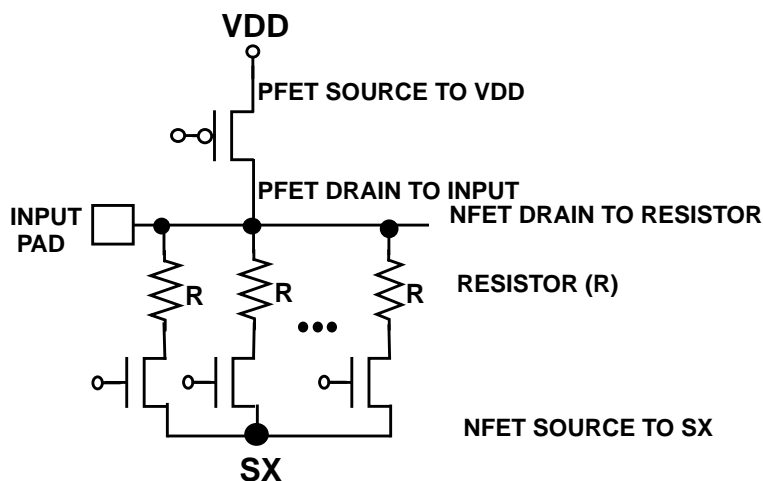


Figure 6-9. Self-Protecting OCD ESD Protection. This demonstrates the usage of resistor ballasting in CMOS drivers. The resistors used are any supported resistor element in the technology.

6.9 Miscellaneous I/O Elements

NFET PASS TRANSISTORS: Connection of NFET pass transistors should be wired in a broad side fashion and follow the NFET OCD layout design rules.

6.10 Electro-static Discharge (ESD) Wiring Rules

In this section, the BEOL design rules are provided to guarantee that ESD pulses do not melt conducting film levels prior to the ESD impulse being discharged by the ESD protect circuitry. This wiring section is relevant to the BEOL requirements between the pad and the ESD protection circuit. These requirements are to be used in conjunction with the existing BEOL electromigration (EM) requirements (see BEOL Reliability ground rules --these design rules do not negate the BEOL reliability EM requirements). Inductor structures must satisfy these rules if placed between the pad and the ESD network. The rules apply to both the coil and under-pass connections.

The requirements established are based on the ability to discharge a Human Body Model (HBM) ESD pulse, which assumes discharge of a 100 pF capacitor through a 1500Ω resistor. Sheet resistance and conducting film thickness values are obtained from section 4.14 , "Wiring Resistance and Capacitance Models" on page 282. General rules and design guidelines below are MINIMUM to allow ESD circuits to perform to an ESD specification of 4 kV.

6.10.1 Conducting Films Requirements

Conducting films from I/O pads to the ESD protect device must satisfy the following line widths:

Table 6-11. Conducting Film Width ESD Requirements

Level	Hole Shapes (Yes / No)	Minimum Effective ¹ Line Width (W_eff μm)	Minimum Design Line Width (μm)	Recommended Effective ¹ Line Width (W_eff μm)	Recommended Design Line Width (μm)
M1	Yes	8.1	11.1	16.2	22.6
M2,M3,M4	Yes	6.4	8.6	12.8	17.8
MQ	Yes	4.6	5.6	9.2	12.2
LY	No	6.08	6.08	9.2	9.2
AM	No	4.0	4.0	4.0	4.0

1. For explanation of M1, M2, M3, M4, and MQ Effective Line Width (W_eff), see Table 4-32 on page 286.

It is RECOMMENDED that the ESD protect circuit is wired to the pad at the M2 wiring level instead of M1 wiring level to insure that metal line connection does not limit the ESD protection.

6.10.2 Via and Contact Requirements

Vias and contacts that are in the current path of the ESD protection device from I/O pads connecting the films between (MT) and M1 must satisfy the following rules.

Table 6-12. Via/Contact ESD Requirements.

Via/contacts	Minimum Number
CA	50
V1	60
V2	60
V3	60
VL	16
VY	3
VYBAR ¹	3 (minimum equivalent, see below)
AV	3

Table 6-12. Via/Contact ESD Requirements.

Via/contacts	Minimum Number
AVBAR ¹	3 (minimum equivalent, see below)

1. The number of bars can be decreased when the equivalent area is greater than 3 times the minimum VYBAR or AVBAR length. For example, 1 AVBAR of width 1.24 μ m and length 3.72 μ m is equivalent area of 3 AVBAR minimum (1.24 μ m x 1.24 μ m).

It is RECOMMENDED that the number of vias and contacts are larger than these requirements for improved ESD performance.

6.11 Salicide-blocked FETs for ESD

To enhance the ESD robustness of I/O transistors it is recommended to add an OP layer to the transistor.

See Table 2-8, “Design Truth Table” on page 49 for a list of devices where special salicide blocking can be applied.

ESDIODE is not supported within T3 isolation well. Salicide block ESD nfets (thin ox, thick ox 2.5-V) are allowed to be placed over T3 isolation well.

To simulate the silicide-blocked FET use two calls to the sblkndres model (one for the source-side resistor, one for the drain-side resistor) in series with the appropriate FET model (e.g. the “nfet” model for the thin-oxide FET) as shown in the below lumped sub-circuit. The sblkndres model is identical to the opndres model, except that the end resistance is removed from the side connected to the FET and also the parasitic capacitance outside the non-silicided region is removed for extraction purposes. Note, the sblkndres model is asymmetric with the three nodes ordered as follows: INPUT, FET, SX (i.e. connect the second node to the FET).

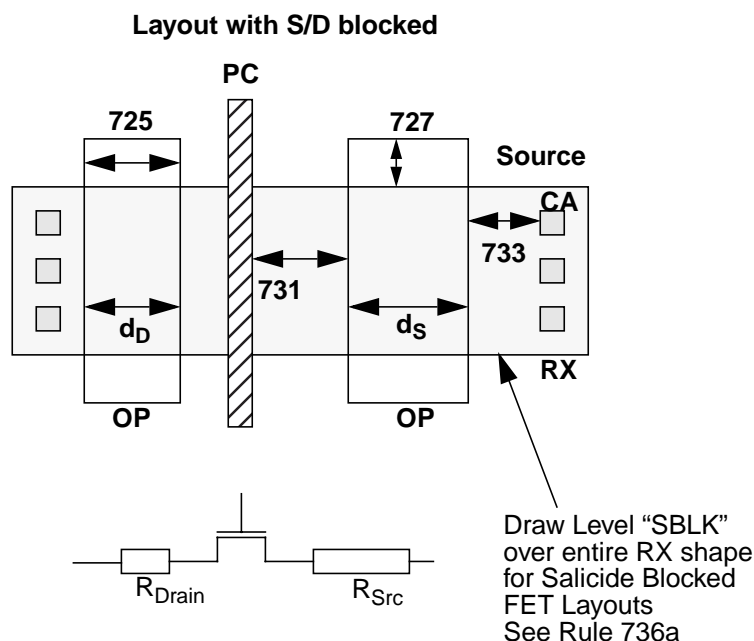


Figure 6-10. Salicide Blocked FET Layouts

6.12 ESD Background and Experimental Data

Refer to the separate ESD Reference Guide document.

Note: The Design Manual ES# and EC# does not apply to the separate ESD Reference Guide, as this document is independent of the Design Manual.

6.13 ESD Schematic level checks

6.13.1 General

This chapter of the design guide covers ESD design requirement to be checked using a schematic level checking tool.

6.13.2 Definitions

LC power supply pad: Low-capacitance (< 100nF) power supply pad

6.13.3 ESD Schematic Checks

Table 6-13. ESD Schematic Rules

Rule	Description		Des Min.
ESD0e	<p>All LC power supply pads must be connected to one of the below combination:</p> <ul style="list-style-type: none"> — A single HBM down diode satisfying rule ESD01a and one or more HBM up diode satisfying rule ESD01b, or — A single HBM down diode satisfying rule ESD01a and one ESD NFET satisfying rule ESD01c, or — A RC-triggered Power clamp satisfying rule ESD01d and a single HBM down diode satisfying rule ESD01a. <p>See Figure 6-12. “ESD Schematic Rule ESD0e” on page 393 for additional information.</p>	≡	-
ESD0d	<p>All I/O signal pads must be connected to one of the below combination:</p> <ul style="list-style-type: none"> — One HBM down diode satisfying rule ESD01a and one or more HBM up diode satisfying rule ESD01b, or — One HBM down diode satisfying rule ESD01a and one ESD NFET satisfying rule ESD01c. <p>See Figure 6-14. “ESD Schematic Rule ESD0d” on page 393 for additional information.</p>	≡	-
ESD0f	<p>Any two different types of ground pads (e.g. Digital/Logic Ground and Analog Ground) must be connected with an ESD Back-to-Back diode with the following combination:</p> <ul style="list-style-type: none"> — A single HBM diode satisfying rule ESD01a and a single HBM diode satisfying rule ESD01b. <p>See Figure 6-15. “ESD Schematic Rule ESD0f” on page 393 for additional information.</p>	≡	-
ESD01a	HBM down diode minimum perimeter.	≥	110
ESD01b	HBM up diode minimum perimeter.	≥	220
ESD01c	HBM NFET minimum width.	≥	200
ESD01d	Minimum sum of the widths of the Big NFETs of all instances of RC-triggered power clamps.	≥	4000
ESD11a	1.2/1.5V driver NFET minimum gate length.	≥	0.15
ESD11bR	2.5V driver NFET minimum gate length.	≥	0.30
ESD11dR	1.2/1.5V ESD NFET maximum gate length.	≤	0.15
ESD11eR	2.5V ESD NFET maximum gate length.	≤	0.30

Table 6-13. ESD Schematic Rules

Rule	Description		Des Min.
ESD15a	HBM down diode maximum anode to cathode spacing.	≤	1.00
ESD15b	HBM up diode maximum anode to cathode spacing.	≤	1.00
ESD21	Only the following ESD FET options are permitted: — Drain/Source silicide-blocked, gate-silicided (GS) single NFET.	≡	-
ESD23	ESD NFETs SBLK width.	≡	0.44
ESD24	1.2/1.5V ESD NFETs minimum SBLK width	≥	2.00
ESD24a	2.5V ESD NFETs minimum SBLK width	≥	3.00
ESD30	All receiver gates connected to an I/O signal pad must be connected to a CDM resistor and CDM devices.	≡	-

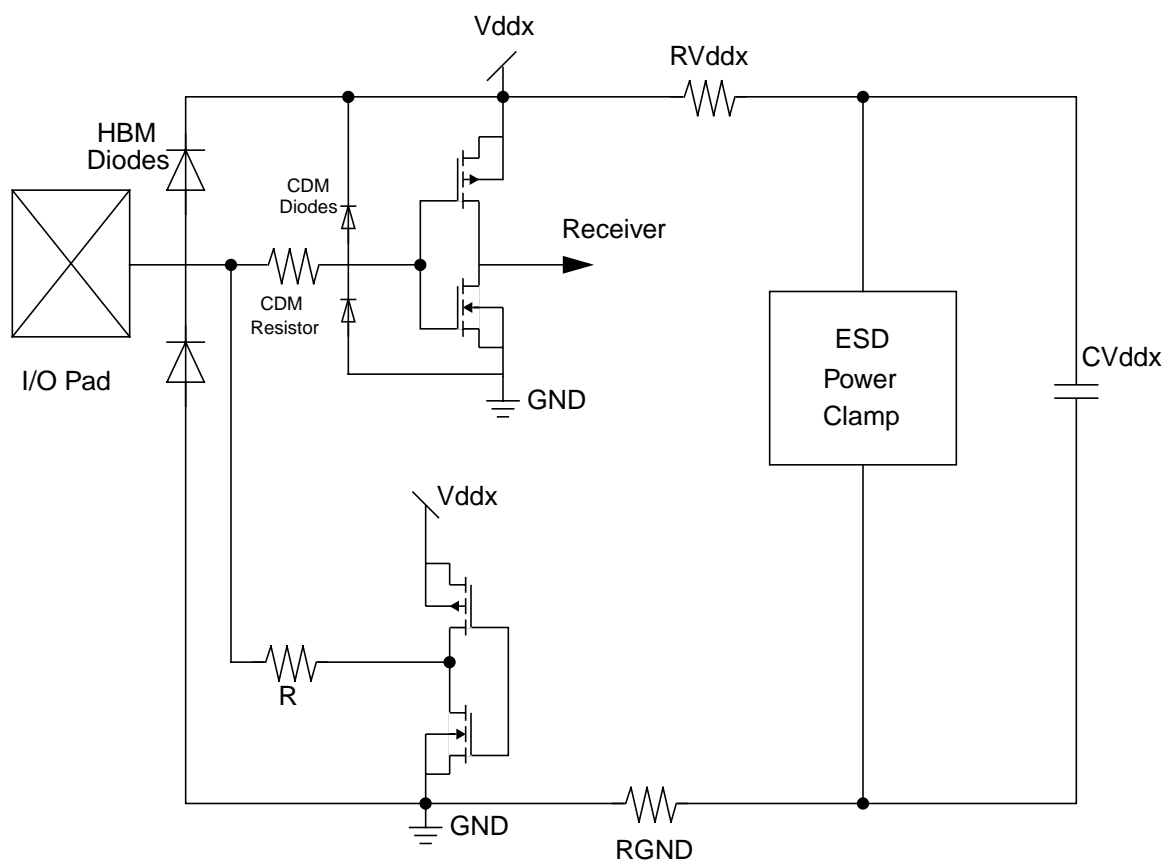


Figure 6-11. Schematic showing bi-directional I/O signal pad with HBM and CDM double diodes. Schematic also shows ESD Power Clamp connected to Power bus.

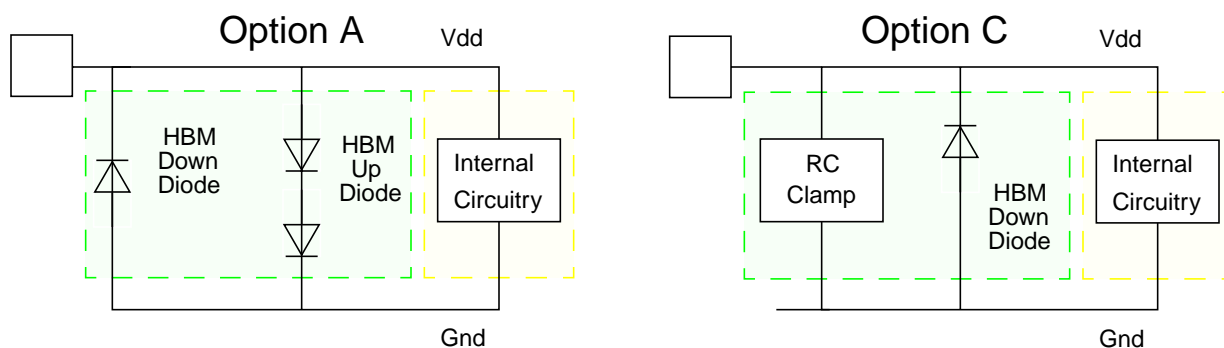


Figure 6-12. ESD Schematic Rule ESD0e

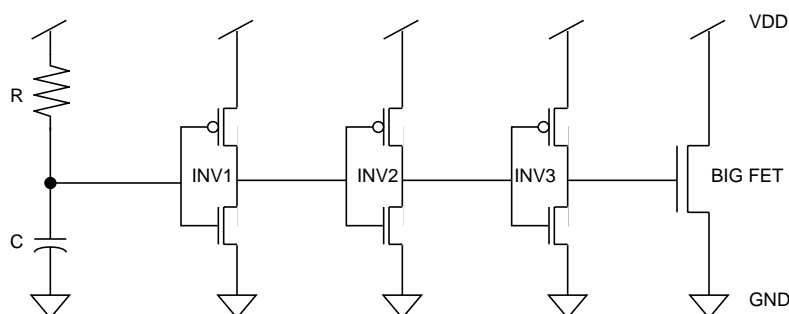


Figure 6-13. Typical RC-Triggered Power Clamps: Single RC-triggered Power clamp (rc_clamp)

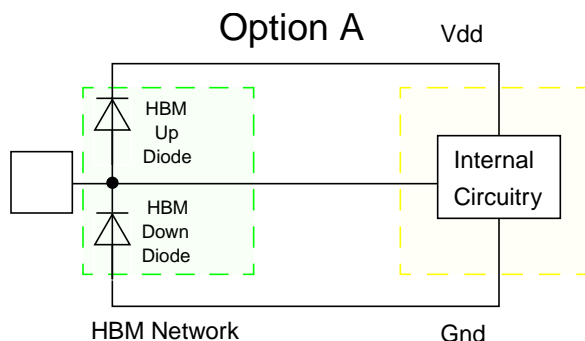


Figure 6-14. ESD Schematic Rule ESD0d

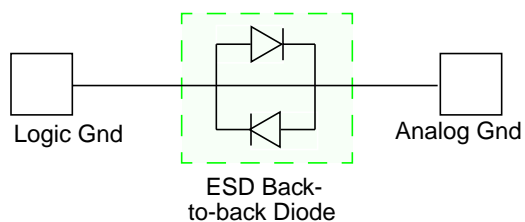


Figure 6-15. ESD Schematic Rule ESD0f



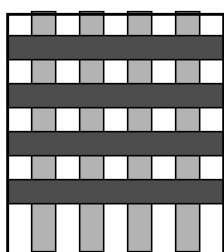
7.0 Design for Manufactureability

7.1 Yield Enhancement Design Techniques

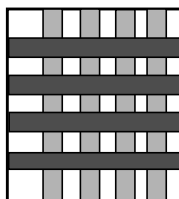
This section describes seven approaches that designers can use to make designs less sensitive to the random manufacturing defects that impact wafer yield. These design optimization guidelines were generated following the development and use of critical area analysis tools on a wide variety of designs

1. Make designs as small as possible.

Smaller designs have just as good yield as larger designs, and allow more to be fit on a wafer. Use minimum design rules when it makes the design smaller.



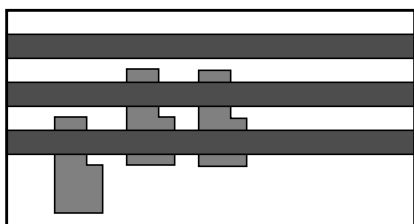
Good



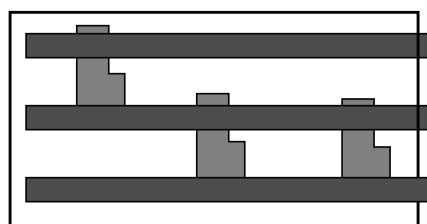
Better

2. Space out elements as much as possible.

Unless this approach grows the design beyond the available space, move elements as far apart as possible. If the design is wiring limited, spread out the devices, and vice versa. If white space exists, use it.



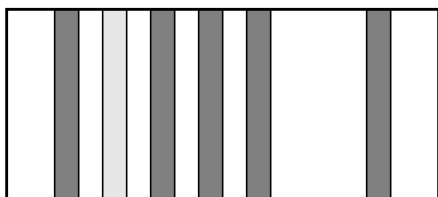
Good



Better

3. Even out the wiring.

Within a layer, **spread out the wires**, and **balance the wiring between levels**. Avoid a very dense level matched with a very sparse level.



Good



Better

4. Avoid shorts.

Wiring shorts are a worse problem than open circuits; so, when space is tight, widen the spacing rather than the wire.



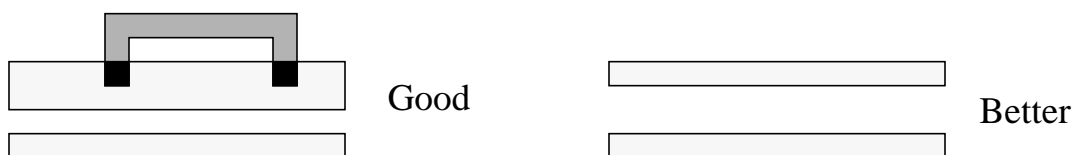
5. Avoid open circuits.

Most opens occur at contacts or vias, so use redundant contacts and vias.



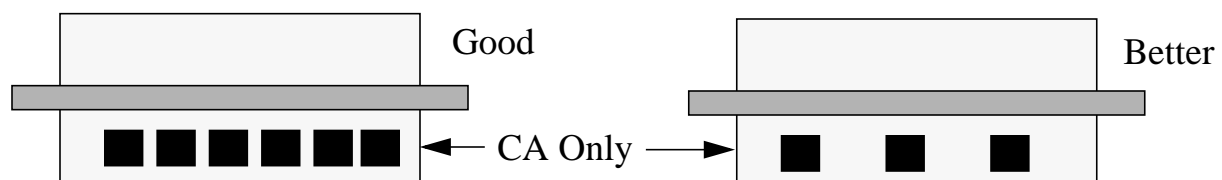
6. Do not add unnecessary wiring.

Without a specific electromigration or performance requirement, **avoid redundant wires** or fattening existing wires. If you find a better way to make a connection, delete the old connection. Resistance of local wiring is normally negligible compared to device conductance.



7. Do not add excess contacts.

Two or three contacts are sufficient redundancy. Contacts placed a few microns away from salicide are sufficient for low resistance. So, **do not create unnecessary risks of CA-PC shorts**.



7.1.1 Recommended Non-minimum Design Rules for Yield Enhancement

Follow rule 2 (“Space out elements as much as possible.” on page 395) and always use larger than minimum design dimensions whenever possible, unless it results in increased chip size or decreased performance. Using the following recommended rules will result in improved yields.

Table 7-1. Recommended Non-minimum Design Rules

Item	Priority ¹	Description	Non-minimum Design	
50R	1	RX width	≥	0.24
51R	1	RX area (μm^2)	≥	0.14
52R	1	RX to RX space	≥	0.26
100R	3	PC width not over RX	≥	0.19
102R	3	PC to PC space	≥	0.26
104R	2	(PC to PC) over RX	≥	0.26
110R	2	RX overlap PC	≥	0.33
111R	2	PC overlap past RX, when [(PC intersect RX) to RX corner $\geq 0.08\mu\text{m}$] and [PC(END) area not over RX $< 0.046\mu\text{m}^2$]	≥	0.25
112R	4	PC overlap past RX, when (PC intersect RX) to RX corner $< 0.08\mu\text{m}$	≥	0.30
113R	4	PC to RX for low PC wiring capacitance (except where PC is tied to RX)	≥	0.08
114R	4	PC to RX corner, for constant W_{eff}	≥	0.24
115R	4	PC corner to RX, when gate corner and RX are on same FET; for constant L_{eff} .	≥	0.24
132R	3	(PC intersect RX) must have an area (μm^2)	≤	45.00
204R	3	CA within RX for no border leakage	≥	0.14
207R	1	CA (over RX) to adjacent PC	≥	0.14
209R	3	CA within PC	≥	0.09

Table 7-1. Recommended Non-minimum Design Rules

Item	Priority ¹	Description	Non-minimum Design	
214R	2	Maximum percent (%) union (CA, CABAR, CEBAR) permitted over a 25 μ m x 25 μ m localized area stepped in 12.5 μ m increments	\leq	10
252dR	2	NW-NW space for area >300 μ m ² and NW width >6.0 μ m	\geq	1.48
260aR	1	RX P+ within NW for [NW width \geq 18.0 μ m and ((not NW) width \geq 18.0 μ m)]	\geq	0.52
265aR	2	RX n+ to adjacent NW for (NW width \geq 18.0 μ m)	\geq	0.52
266R	-	RX Substrate Contact to NW - Recommended for low resistance contact	\geq	0.20
504R	1	M1 to M1 space; (if at least one metal line is >1.04 μ m wide)	\geq	0.36
506aR	2	M1 overlap past CA for two opposite sides	\geq	0.06
571aR	2	M1 overlap past V1 for two opposite sides	\geq	0.06
604R	1	M2 to M2, M3 to M3, M4 to M4, space; (if at least one metal line is >1.0 μ m wide)	\geq	0.36
609R ^{2,3}	1	[(Mx width > 2.8 μ m) intersect M(x+1)] density must be \leq 50% over local 200 μ m x 200 μ m areas, stepped in 100 μ m increments, where Mx = M1,M2, M3,M4, and where M(x+1) = M2, M3, M4, MQ.	=	-
610R	2	Vx must be within Mx, for two opposite sides, where x = 2,3	\geq	0.09
612R	1	At least 2 vias must connect metal below to metal above when metal width is \geq 1.04 μ m.	=	-

Table 7-1. Recommended Non-minimum Design Rules

Item	Priority ¹	Description	Non-minimum Design	
MXPL4R	1	M1PLANE to M2PLANE space (for designs with 5LM, 6LM, or 7LM) M2PLANE to M3PLANE space (for designs with 6LM or 7LM) M3PLANE to M4PLANE space (for designs with 7LM) M2PLANE to MQPLANE space (for designs with 5LM) M3PLANE to MQPLANE space (for designs with 6LM) M4PLANE to MQPLANE space (for designs with 7LM)	≥	10.00
DG8cR	3	(PC touching DG) minimum space to adjacent PC		0.30

1. A design rule with a lower number in this column is more important for yield enhancement than a design rule with a higher number. This list is based on experience with prior CMOS generations.
2. This local density requirement is calculated using the intersection of consecutive metal shapes over which the checking box is stepped. When the box steps over the chip boundary, the box is moved back in bounds. The metal density is calculated using design layout data prior to IBM design services MxHOLE or MxFILL. See also Table 2-7, "Back End Of Line (BEOL) Metallization Options" on page 49.
3. This local density requirement limits the stacked metal pattern (directly above and below) using an intersection methodology for compatibility with available checking tools.

7.2 Design for Manufactureability Initiatives

A key semiconductor manufacturing metric is good modules (packaged devices) per wafer start. This metric is defined as follows:

$$(\text{wafers to test/wafers started}) \times (\text{die to test/wafers to test}) \times (\text{good die / die to test}) \times (\text{modules to test / good die}) \times (\text{modules to burn-in / modules to test}) \times (\text{good modules out / modules to burn-in}) = \text{good modules / wafer start.}$$

Each of these ratios is either completely controlled by design team or jointly controlled by the design and manufacturing teams. Good modules per wafer start really measures both design productivity and manufacturing operations productivity.

Significant productivity enhancements can be achieved by incorporating the following Design For Manufactureability (DFM) initiatives into product designs. Tables through Table provide a brief description of the DFM design actions: for further detail, consult your IBM technical representative.

Table 7-2. Design for Manufactureability Initiatives - Physical Design

DFM Item Number	Description
1.1	AdjCheck (Paint) routing tool used on the back-end-of-line (BEOL) design to improve product electrical performance and productivity.
1.2	Metal fill (and hole for copper) tools used to fill white space and cheese wide copper lines with IBM-generated patterns to improve uniformity and productivity.
1.3	IBM electronic design automation (EDA) XRouter routing tool, with wire spreading enabled, used on the BEOL design to improve product electrical performance and productivity.
1.4	Larger than minimum spacing used between wide metal bus lines and adjacent lines to improve productivity.
1.5	IBM EDA Wirebender tool used on the BEOL design to improve product electrical performance and productivity.
1.6	Redundant CAs and vias used wherever possible. IBM EDA via redundancy tool used on the BEOL design to improve product reliability.
1.7	IBM-generated shapes used on front-end-of-line (FEOL) design at PC/RX levels to improve uniformity and productivity.
1.8	Optimized WL/BL/subarray redundancy employed on array products and on imbedded cache arrays in logic products. I _{DDQ} test specifications consider the impact of failing bits.
1.9	Design optimized to improve defect resistance by using critical area analysis tools on array cells and logic macros. Approved SRAM cells used.
1.10	Not applicable
1.11	Product migration strategy (for example, photo shrinks) defined for both silicon and package as part of the high-level product design step.
1.12	A cleanup design pass, test program update, and qualification scheduled for the production-level design.
1.13	A chip size and chip aspect ratio that maximize the number of chips per wafer and the number of chips within a stepper field have been chosen.
1.14	Polysilicon width expanded at PC/BP intersections to improve local PC series resistor (R_s) control at intersection point.
1.15	Process monitoring structures included on-chip for failure analysis characterization and post-dicing process history determination. Discrete devices wired to last metal within the chip parameter can be probed to determine, for example, V_t and L_{eff} .
1.16	The design of test clock trees optimized to provide minimum scan path propagation delays, and to allow minimum scan cycle times to reduce test time.

Table 7-2. Design for Manufactureability Initiatives - Physical Design

DFM Item Number	Description
1.17	A suite of programs, Swampfinder, can be run to identify design sensitivities not covered by design rule checking.
1.18	Customization of standard products is performed as late in the process as possible to maximize inventory flexibility and minimize post customization turnaround time.
1.19	Levels affected by RTM B have been minimized by reusing C4 and design levels to reduce post customization turnaround time.

Table 7-3. Design for Manufactureability Initiatives - Electrical Design

DFM Item	Description
2.1	Simulations demonstrate that the design will have 100% circuit limited yield (CLY) at functional test conditions (that is, the design is process window clean at all process corners: nominal, best case, and worst case).
2.2	Simulations indicate that critical design components and macros are functional at all process, voltage, and temperature corners and at test, DVS, EVS, and BI applied conditions. Use of tools such as ASX/Q encouraged.
2.3	Product performance at nominal process and V_{DD} conditions is higher than the market performance objective. Performance 2s above the target market performance requirement is the objective so that line tailoring is unnecessary and sort requirements can be minimized.
2.4	If this design is a follow-on design (for example, GR to GQ to GP, and so forth), then the new design incorporates fixes for all functionality and CLY issues documented in the previous product's integrated product development (IPD) problem log.
2.5	Performance monitoring techniques are included on-chip for die-by-die performance screening. Monitor techniques capable of detecting both FEOL and BEOL performance contributions are recommended. A minimum of five flushable scan chains are included to enable across-chip performance measurements at wafer level functional test.
2.6	Logic synthesis tools such as IBM BooleDozer II% are used for improved product performance, time to market, and productivity.
2.7	Array products, and logic products with large cache designs, selectively use V_t adjustment implants to control I_{off} and I_{DD} . Contact your IBM technical representative for information on the availability of V_t adjustment process options for the technology of interest.
2.8	Electronic chip ID (ECID) circuitry is integrated into a scan chain design so that lot, wafer, and chip ID are available at chip and module assembly points post fuse blow. ECID latches are located at the end of a scan chain.

Table 7-3. Design for Manufactureability Initiatives - Electrical Design

DFM Item	Description
2.9	The design supports I_{DDQ} testing by eliminating dc paths in logic other than reference voltage generation and limited ground-to-PFET NOR structures. An I_{DDQ} “control pin” is used to shut off components such as all I_{DD} paths, ratioed logic, PLLs, other internal oscillators, and resistors.
2.10	A thorough analysis of the impact of noise upon product function has been completed. Noise limits have been established for OVDD, AVDD, and V_{DD} . The impact of the BEOL attributes (for example, wire length, parallel wiring runs, IR drops at interconnects, and asynchronous coupling voltages) upon noise generation have been considered and found acceptable.
2.11	For analog and mixed-signal designs, a full four-corner simulation has been conducted around critical parameter pairs (for example, beta and resistance).
2.12	Dual-port arrays have been replaced by single-port double-clocked arrays to reduce critical area for equivalent function.
2.13	I/O reduction techniques on I/O-limited designs have been considered.

Table 7-4. Design for Manufactureability Initiatives - Test / Characterization Design

DFM Item	Description
3.1	Array and logic products with large caches employ physical, electrical, and test design approaches that enable filibuster testing to detect and eliminate V_{DD} to ground shorts within the array.
3.2	Array and logic products with caches of 32 K bits or larger follow array built-in self test (ABIST) diagnosable design rules, so that bit mapping of memory defects is possible at wafer level testing.
3.3	Prefuse testing of redundant elements is conducted on all redundant elements in array and logic products.
3.4	For high-performance products, maximum di/dt during test has been used to validate DIB design to eliminate yield losses resulting from V_{DD} drop during testing.
3.5	Forward-bias contact tests have been designed with sufficiently high I_{force} to ensure acceptable (that is, low) levels of contact resistance for the device under test.
3.6	Product T2/SQ characterization plan includes sufficient hardware and process splits to generate the data necessary to support the launch DCP and the required manufacturing volume ramp.

Table 7-4. Design for Manufactureability Initiatives - Test / Characterization Design

DFM Item	Description
3.7	Product design supports level-sensitive scan design (LSSD) testing to enable high fault coverage, reduced test engineering resources, and improved problem resolution turnaround time. The number of scan chains must fit the target tester, and the scan chains must contain a balanced number of latches to minimize test times. Scan-in and scan-out operations should be overlapped.
3.8	Built-in self-test (BIST) is used for embedded SRAM and DRAM, logic, and analog macros to reduce test equipment requirements and enable parallel test.
3.9	The number of test vectors should be minimized, and vector order and I _{DDQ} tests should be optimized to reduce test cost on high-volume programs. (Diagnostic considerations may dictate alternate solutions to support initial program debug and failure analysis.)
3.10	The test design includes reduced pin count test (RPCT), I/O wrap, pin dotting, pin banking, and parallel test (multi-DUT).
3.11	AC testing is most efficiently implemented using LSSD-based delay testing to provide high fault coverage with reasonable test equipment requirements. The product design enables ac delay testing by including on-product clock generation (OPCG), and ac I/O wrap.
3.12	For all ac or at-speed testing, the test environment is completely modeled and understood.
3.13	Test methodology for the design, including embedded digital and analog macros, has been reviewed with the DFT team and approved by test analysis engineering.
3.14	For high-volume programs, consider the Reliability Optimized for Characterization, "Kost," and Yield (ROCKY) process, where additional data is collected before volume ramp and statistical data analysis are used to determine the optimal test screens and limits.

Table 7-5. Design for Manufactureability Initiatives - Diagnostics / Debug / FA-Friendly Design

DFM Item	Description
4.1	The design includes a diagnostic/failure analysis (FA) strategy jointly developed by the product design, test, diagnostics (D/G42), and failure analysis groups. The design adheres to the scan rules as verified by IBM TestBench TSV, and BIST design rules maintained by G42. Deliverables to the BTV manufacturing and FA team include logical and physical design descriptions, L2L logical to physical cross-mapping database, and information required to perform wafer-scale electrical and physical failure analysis of failures.
4.2	A diagnostic solution has been identified and documented in manufacturing for each AVP test.

Table 7-5. Design for Manufactureability Initiatives - Diagnostics / Debug / FA-Friendly Design

DFM Item	Description
4.3	On-chip structures that facilitate FIB device modification are in the design where appropriate. These include backside and/or frontside structures to support FIB work, such as navigation references, memory address verification marks, probe points, severable links, spare wires, spare logic, and backside FIB DM circuits. Fill-shape exclusion zones are used to protect FIB areas as needed.
4.4	ABIST test patterns are available that enable logical-to-physical bit failure map verification using a photon emission technique to view the activated cell. This technique has an improved turnaround time compared to traditional FIB verification techniques.
4.5	Physical failure analysis design data and documentation requirements: <ul style="list-style-type: none"> • L2L logical to physical cross-mapping database • Design description document describing test modes, scan chain configurations, pattern odometers for I_{DDQ} patterns. • Shapes (gl1 or gds2)

Table 7-6. Design for Manufactureability Initiatives - Packaging Design

DFM Item	Description
5.1	The design uses an existing off-the-shelf package.
5.2	Newly designed package lids are designed for automation.
5.3	New chip/package designs maximize interconnect pitches where possible without creating I/O limited designs and increasing die area.
5.4	The design employs a shrink invariant wire-bond pad footprint.
5.5	The design employs a shrink invariant C4 pad footprint.
5.6	The design uses a common pad footprint for wire-bond designs.
5.7	The design uses a common pad footprint for C4 designs.
5.8	The design uses optimized C4 diameter/design for the specific package chosen.
5.9	An economic analysis of system-on-a-chip (SoC) versus system-in-package (SiP) architecture has been completed.
5.10	An economic analysis of wire-bond versus C4 options has been conducted.

<i>Table 7-6. Design for Manufactureability Initiatives - Packaging Design</i>	
DFM Item	Description
5.11	Enable reuse of existing C4 masks by using an existing image/package



Appendix A. Guidelines for Optimal Model-Hardware Correlation

Listed below are some general guidelines (not all-inclusive) for achieving good model-to-hardware correlation.

1. Avoid device widths less than 0.24 μm .
2. Include N-well sheet resistance in simulations to reflect local transient bias variations.
3. Avoid using minimum width polysilicon and diffusions where resistance is critical to performance. Sheet resistance is generally higher and more variable in minimum width lines. (See “Conducting Film Thickness” on page 282.)
4. Avoid using single source or drain contact placement on wide devices. Avoid situations where any PC gate edge is greater than 1 μm from a contact. The FET’s drive current is particularly sensitive to extra resistances coming from CA and silicide at the source side. It is a good practice to put as many CA’s as possible at a relaxed PC to CA distance of 0.14 μm . The area junction capacitance of the source side in general does not contribute to the capacitive loading, so increase the source side diffusion area to avoid CA’s landing partially on STI under worst case process tolerances. This reduces the CA resistance tolerance.
5. Avoid minimum values of rules 114 and 115; use the recommended rules 114R and 115R. Minimum values of these rules result in device width uncertainties.
6. Avoid use of bent gates. Although permitted, bent gates can degrade models.
7. Model long runs of wire as distributed wire delays.
8. Ensure that n-well proximity effects are either negligible (that is the n-well edge is at least 3 μm from the FET). Additional information on dummy design level VTSENS is in Table 3-6, “VTSENS (Threshold Voltage) Layout Rules,” on page 89. Note that the thick oxide devices are very sensitive to proximity effects as described in Section 4.4.6.3 , “Threshold Voltage Effect Near NW Edge” on page 251, and “Well Proximity” on page 254.
9. Consider the impact of mechanical stress induced during wafer processing on FET devices (see Section 4.4.7.4 , “Isolation Proximity Effect on FETs” on page 253).

Appendix B. Total Standby Current (I_{dd})

The standby current in short channel MOSFET's ($L_{poly} > 0.07 \mu m$) due to subthreshold leakage may be approximated by $I_{off}(L_p)$ for $W > 0.4 \mu m$ and $0.9 V \leq V_{ds} \leq 2.1 V$:

$$I_{off}(L_p) = (I_1(T)e^{-(L_p - dL)/L_1} + I_2(T)e^{-(L_p - dL)/L_2})(1 + \alpha) \quad (1)$$

where, $\alpha = A1 \exp(-A2((L_p - dL))) \exp(V_{ds} - 0.9) \exp(A3(25 - T))(V_{ds} - 0.9)$

$$I_1(T) = I_{10} e^{B1(T - 140^\circ C)} \quad (A/\mu m) \quad (2)$$

$$I_2(T) = I_{20} e^{B2(T - 140^\circ C)} \quad (A/\mu m) \quad (3)$$

$$L1 = L11 + L12(T - 140)$$

$$L2 = L21 + L22(T - 140)$$

and where L_p is the (wafer level) gate length, $dL = -0.003$, and I_1 and I_2 are a function of temperature (T). A die centered at an L_p of $L_{die-mean}$ contains MOSFET's with L_p varying about this mean by an amount described by the ACLV specifications in Table 4-9, "Gate Length Variation for thin oxide FET (3s)" on page 251. Integration of this ACLV distribution (presumed to be gaussian) against the above I_{off} equation summed with the leakage component yields:

$$I_{ddFET} = W_{tot}(C1 + C2) \quad (4)$$

$$C1 = I_1(T) \times e^{-(L_p - dL)/L_1} \times e^{\frac{1}{2}(\sigma_{ACLV}/L_1)^2} + I_2(T) \times e^{-(L_p - dL)/L_2} \times e^{\frac{1}{2}(\sigma_{ACLV}/L_2)^2}$$

$$C2 = \frac{\alpha}{\exp(-A2L_p)} \times \left(I_1(T) \times e^{-(L_p - dL)/L_3} \times e^{\frac{1}{2}(\sigma_{ACLV}/L_3)^2} + I_2(T) \times e^{-(L_p - dL)/L_4} \times e^{\frac{1}{2}(\sigma_{ACLV}/L_4)^2} \right)$$

with

$$L3 = \frac{L1}{1 + L1A2}$$

$$L4 = \frac{L2}{1 + L2A2}$$

where σ_{ACLV} is $ACLV/3$ ($ACLV$ is a 3-sigma number). Table 4-9, "Gate Length Variation for thin oxide FET (3s)" on page 251, characterizes the variation in MOSFET channel length about the die-mean L_p . W_{tot} is the total width of all MOSFET's in standby state per device type.

Table B-1. I_{dd} Parameters

Device type	I ₁₀ (A/μm)	I ₂₀ (A/μm)	L ₁₁ (μm)	L ₁₂ (μm)	B1 (/°C)	B2 (/°C)	L ₂₁ (μm)	L ₂₂ (μm)	A1 (-)	A2 (1/μm)	A3 (1/C)
Reg Vt NFET	0.0015	2.1e-8	0.0065	2e-5	-0.019	0.038	0.12	0.0	100	50	0.0005
Reg Vt PFET	0.005	7e-8	0.006	1.5e-5	-0.006	0.025	0.05	1.6e-4	15	30	0.0005

The following is an example of how the standby current I_{dd} would be calculated for a chip with W_{total}=10⁷μm per device type, nFET L_{die-mean}=0.07/0.081/0.092 μm at T=85°C. For simplicity, the total width of MOSFET's that have V_{DS}=1.5V in the standby state is assumed to divide evenly between NFET and PFET.

The chip standby current caused by the regular-Vt FET's can be calculated from equation (4) where:

$$\begin{aligned}
 L_{\text{die-mean}} &= 0.07\mu\text{m}, 0.081\mu\text{m}, 0.092\mu\text{m} \\
 W_{\text{total}} &= 10^7\mu\text{m of NFETs} + 10^7\mu\text{m of PFETs} \\
 \sigma_{\text{ACLV}} &= 1 \text{ sigma of ACLV} = 0.014/3\mu\text{m} = 0.0047
 \end{aligned}$$

The total standby current is calculated to be 750mA, 144mA, and 64mA respectively. We used for ACLV 14nm instead of the target of 11nm. This larger number is to be used for chips entering the technology in the pre-production mode. During maturity of the technology, this will go down to the target.

For some other leakage components, the following guidelines can be used (3-sigma values are given) per unit design width (@25C):

Fet I_{off} : 600pA/μm

I_{gate} : 25 pA/μm

I_{GIDL} : 5 pA/μm

junction : 1 pA/μm

Minimum design rules are assumed. Check Section 4.0 , "Electrical Parameters and Models" on page 243 for more detailed numbers.

Appendix C. Design Hierarchy Guidelines

The following general guidelines and practices significantly improve hierarchical verification run time and ease of debugging. Not following these guidelines can adversely impact mask house and data preparation turn around time.

1. Wherever possible, design to facilitate reuse of circuits. For example, if a 2 way NAND gate is needed, reuse one that is already designed if possible.
2. Put all needed shapes to make a circuit in the same cell. Don't create transistors by bumping poly from one cell over RX in another cell. Put the NW and BP shapes in the cell where the transistors are formed.
3. Make each cell ground rule correct. For example, don't place contacts in a cell without metal covering them.
4. When a cell lower in the hierarchy must be intruded upon, do it as low in the hierarchy as possible. For example, don't wait until the prime cell to program decoders. Place the programmed decoders in the next higher level of the hierarchy.
5. Strive for rectangular shaped circuits. "L" shaped circuit layouts have lots of intrusions which slow down the checker.
6. Don't do anything at the top (prime) cell which changes things like transistor width, length or connectivity at the bottom.
7. Large hollow structures like substrate rings (which basically intrude on the entire chip) should be built by placing 4 cells in the prime. One would be the "top" one might be the "left", the "right" and the "bottom". This way there is no interference with anything these cells don't actually come near.
8. Avoid any names with special characters. Use 0-9 and a-z on cell names, level names and port names. Always start with an alphabetic character.
9. Make connections as low in the hierarchy as possible. The closer to the prime, the harder it will be to debug any wiring errors.
10. Avoid 'holding levels' of hierarchy where there are only transforms and no shapes. Some tools spend a lot of time resolving nothing.
11. Too much hierarchy of the wrong kind may be a problem. For example, circuits laid out with each individual shape residing in it's own cell would be self-defeating.
12. Only output 1 prime cell. Some design tools (like IBM's IGS) allow multiple primes to be output.
13. Nest each large discrete design component (such as a cache or FPU) as an individually named model. This is particularly helpful if the structure occupies a large fraction of the chip (20 percent or more). Also, nest repeated sub-units of large discrete design components as individually named models.
14. Avoid overlapping large models. For instance, avoid using overlapping "registration marks" to align models.
15. For large chips ($>200 \text{ mm}^2$), making preliminary data available to the mask house is strongly encouraged.

Appendix D. Rule Syntax (Definitions)

The terms below are useful in understanding and applying the layout ground rules.

- 45 DEGREE - When applied to an edge of a shape, it means an edge that is 45 degrees from the X/Y design grid axis. When applied to a shape, it means a shape with a 45 degree edge.
- ABUTS - Specifies the condition whereby a shape on one level(A) shares an edge with any shape on another level(B) such that the shapes do not have any area in common, and they only touch along a common edge.
- AREA - Rule applies to shape area, not a linear dimension. See Figure D-1, "Figures for Definitions" on page 413.
- BUTTING - See ABUTS.
- CENTER - Describes the center point of a shape. Most commonly used for the center of a circle or octagon.
- COINCIDENT - The condition whereby a shape on one level (A) shares an edge with any shape on another level (B) such that the shapes have area in common.
- COMMON RUN - Distance that two shapes run parallel. This applies even if the shapes turn, so long as the minimum space between them does not effectively change. (UNBENDED COMMON RUN refers to the distance of run segments that do not turn.) This applies to one or two shapes, not more than two. See Figure D-1, "Figures for Definitions" on page 413.
- COVERED, COVERED BY, MUST BE COVERED, MUST BE COVERED BY, See WITHIN or MUST BE WITHIN
- DIFFERENCE - Used in Section 2.5 , "Level Generation and Design Preparation" on page 44, where difference (A,B) can be interpreted as either (A minus B) or (B subtracted from A). If shape B intersects shape A, the remainder after the boolean operation is the area of shape A with the area of shape B removed (subtracted) from it. Same as A not over B.
- ENCLOSED AREA - See Figure D-1, "Figures for Definitions" on page 413.
- EXACT - rule can have no other values than that specified exactly
- FLOATING GATE - A gate that is not electrically connected to N⁺ or P⁺ junction by M1.
- INTERSECT - Boolean "AND". See Figure D-1, "Figures for Definitions" on page 413.
- LENGTH - The long dimension of a rectangle.
- NOTCH - Space from outside edge to outside edge on a single polygon
- OVER - Equivalent to INTERSECT. "NOT OVER" implies the inverse of OVER, or COMPLIMENT INTERSECT.
- OVERLAP OF - The minimum distance from the inside of shape L to the inside edge of M when L intersects M. See Figure D-1, "Figures for Definitions" on page 413.
- OVERLAP PAST - The minimum distance from the outside edge of J to the inside edge of K when J intersects K. See Figure D-1, "Figures for Definitions" on page 413. For example, M1 overlap past CA for at

least two sides 0.10 means that M1 and CA intersect, and that the M1 must extend beyond two or more sides of the CA square by 0.10 μm .

- PC - PC is a vector of length less than or equal to Rule-102 at design dimension measured between two 90 degree corners inside the shape.
- SPACE - see TO.
- STRADDLES - Crosses the border of a shape. For example, RX straddles NW means that part of the RX shape overlaps the NW and part of the RX shape extends beyond the edge of the NW.
- TO - Distance between two shapes. See Figure D-1, "Figures for Definitions" on page 413. This fixes a space (>zero) between two shapes. A spacing =0.00 is not allowed unless explicitly stated.
- TO ADJACENT (WHEN SHAPES DO NOT INTERSECT) - Same as "TO" except shapes that intersect are not subject to checking.
- TO ADJACENT (DIFFERENT NET) - Same as "TO" except that shapes which are electrically on the same net are not subject to checking. The net connection may be through any level up through the final level of metal.
- TOUCH, TOUCHING - When any part of one shape shares any part of the area or edge or even point of another shape, they are 'touching'. They are touching even if they only share one common vertex. TOUCH is also sometimes referred to as "HIT".
- UNDER - Equivalent to INTERSECT.
- UNION - Boolean "OR". See Figure D-1, "Figures for Definitions" on page 413.
- VERTEX/VERTICES/CORNER - Intersection of two edges of same shape. Includes 45 and 90 degree corners.
- WIDTH - Distance between inside edges of a shape. Width is measured on edges that are parallel or form an angle of less than 90 degrees.
- WITHIN - For example, CA within M1 0.10 means that shape M1 encompasses shape CA and that every point of CA must be at least 0.10 inside the nearest point on shape M1.

WITHIN (or COVERED or COVEREDBY) means that either of the two shapes can be present by itself without the other shape being present.

- MUST BE WITHIN (or COVERED or COVEREDBY)- This is the same as WITHIN except that, for example, CA must be within M1 requires each and every CA shape to have an M1. CA cannot exist without M1. However M1 can be present without CA.

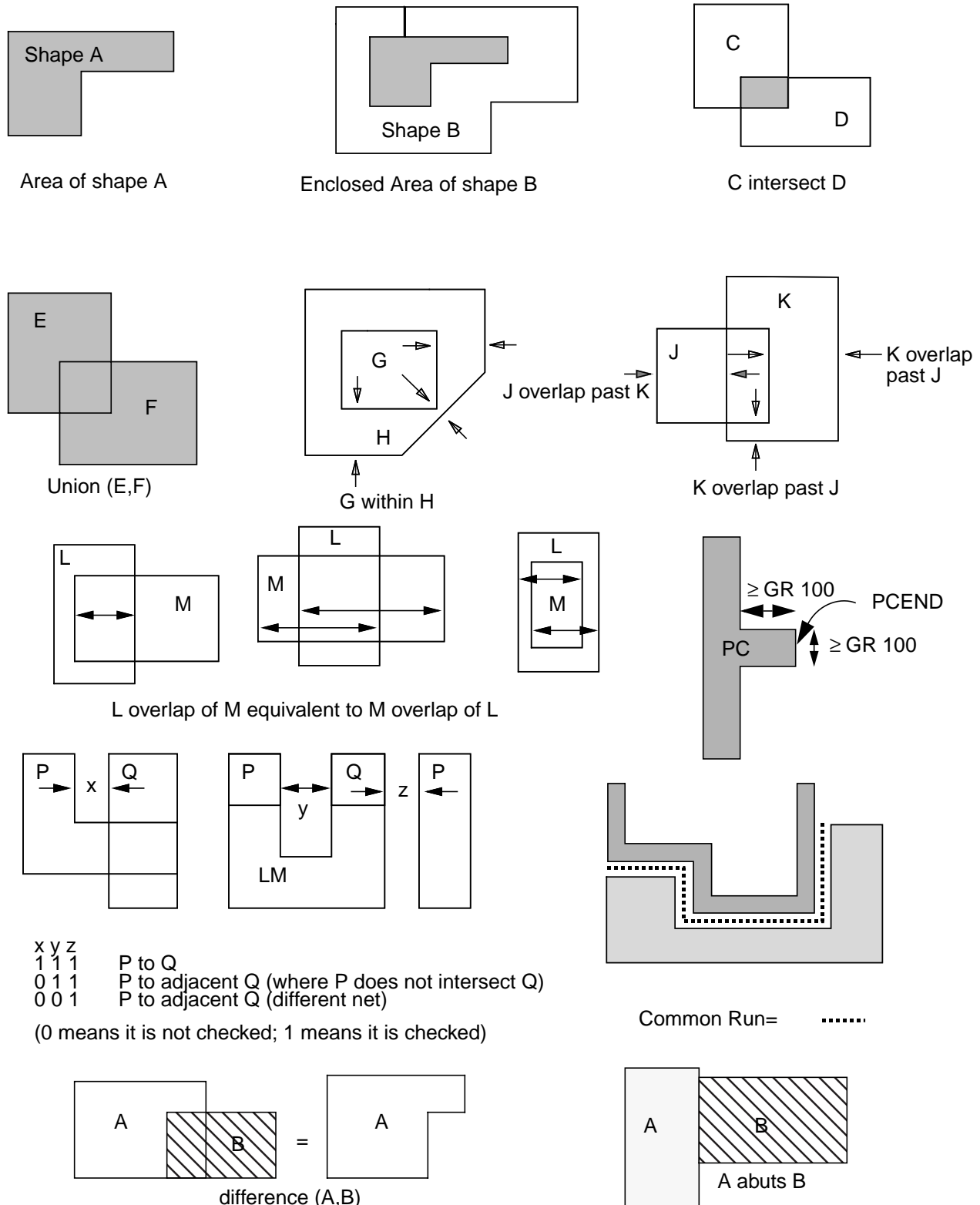


Figure D-1. Figures for Definitions

Appendix E. Definitions of Process-Related Terms

- BIAS - Bias is the difference between the design dimension and the nominal wafer dimension:
Bias = Wafer Nominal (WAF NOM) - Design Dimension (DES DIM) (GL1)
- BIAS SIGN - A positive bias means the dimension of the image on the wafer is **bigger** than the corresponding design shape in GL1. A negative bias means the dimension of the image on the wafer is **smaller** than the corresponding design shape in GL1.
- BLM: Bump Limiting Metallurgy
- DESIGN MINIMUM (DES MIN) - The minimum design dimension allowed by photo, etch, fill and electrical considerations. This is the design minimum given in the layout rules.
- FORESHORTENING - A more negative bias at the end of a narrow line than at the sides.
- HOLE - Where resist is removed by the photo process.
- ISLAND - Where resist remains after photo process.
- LDD - Lightly Doped Drain
- NET BIAS AND TOLERANCE - The bias and tolerance used in "Layout Rules" are the net biases and tolerances. For bias, this is the algebraic sum of the component biases. For tolerance, this is the root-sum-square (RSS) of the component tolerances. Components are photo, etch, slope, film thickness, etc.
- TOLERANCE (TOL) - Variation in the process gives rise to variation in the feature dimension specified in the layout rules tables. The extent of this variation above or below the nominal is called the tolerance. Tolerance as used in this publication means "net tolerance". The "Tol" specified in this document is a 3σ value. For calculating layout ground rules, the Tol is multiplied by $4/3$ to arrive at a " 4σ " value, which is approximated to be the 4.5σ for a batch population that is used in the Motorola " 6σ " methodology.
- TOTAL BIAS - Same as "Net Bias".
- UBM - Under Bump Metallurgy
- WAFER NOMINAL or WAF NOM or WAF or NOM - The nominal or target dimension of a design shape as measured on the wafer.

Appendix F. Migration into Future Technologies

There are concerns for migrating designs into future technologies that are known but cannot be fully quantified at this time. The following is a list of concerns for migrating designs into future technologies.

1. There are a number of PC line interactions over oxide that could be problematic for implementing future mask techniques. PC rules are only now being developed for future technologies. In general, one should use a more relaxed PC width when it is used for PC *wiring* (over oxide). PC *wiring* can be defined as $PC \geq (\text{Rule\#115R})$ away from RX. As these complex rules evolve, more design conditions could be forbidden. Also, PC wiring rule mentioned above may be too restrictive in some design cases.
2. Device interactions for rules like 111, 112, 113, 114, 115, 207 and 208 have been difficult to shrink into subsequent technologies. These rules should be relaxed if such scaling is desired.
3. As in past technology migrations, the Terminal Metal (LV, DV,) rules do not scale. In general, this impacts Fuse, C4, Wirebond and Chip Guard Ring rules.
4. ESD rules will not scale into future technologies.
5. Other IO related devices have not been scaled in the past; OP and DG rules should be relaxed if future scaling is desired.

Appendix G. Design Preparation

Section 2.5 , “Level Generation and Design Preparation” on page 44 as well as this section briefly describes the pre-mask DataPrep routines required prior to mask build. Compensations are given in μm per edge.

G.1 Complex Optical Manipulations

OPC (Optical Proximity Correction), SLB (Selective Linewidth Bias) and other complex optical manipulations are outside the scope of this document. Information may be obtained from your technical representative.

G.2 Dense SRAM Design (Not Offered)

The Dataprep for Dense SRAM builds may require the generation of D1 and CF and VE levels for M1 and CA and V1 mask layers, respectively. Consult your technical representative for more detail.

G.3 PC

Other more complex OPC manipulations are done for PC layer. Consult the Data Preparation Specification or your technical representative for more detail.

G.3.1 DGxxGATE

DGNGATE = [([PC over (RX sized by 0.08)] over DG} not over BP)] sized by 0.005
DGP GATE = [([PC over (RX sized by 0.08)] over DG} over BP)] sized by 0.005

G.3.2 PC Fuse

The PCFUSE shape is merged onto the PC mask in DataPrep.

G.4 Far BEOL Manipulation

For LV, U and TM, see Table 2-6, “Shape Manipulation Prior to Mask Write,” on page 44

Appendix H. Pattern Fill Rules

The information herein may not be current. Consult your technical representative for more details

H.1 xxFILL and xxHOLE Generation

These rules are included to provide the designer guidance when checking and simulating designs that have received IBM generated RX, PC and Metal FILL, and Metal HOLE shapes. For more information Section 2.10 , “Pattern Density Rules” on page 62. For designs using the IBM Mask House facility, these routines will be run within IBM; consult your PE representative for more detail.

Note that any nominal violations of these rules indicate a deficiency with the IBM FILL and HOLE generation tools. Nominal violations of these rules are primarily the responsibility of IBM Manufacturing and IBM Design Services to resolve, particularly rules PD1a, PD2, PD4a, PD4a1 and PD4b. The customer will only be asked to reexamine the design if a nominal violation can not be waived and can not be brought into compliance by modifications to the Design Services Shapes Generation tools. Such problems can be best avoided by careful attention to the rules in section H.1.1 , “Estimated Pattern Density Generation” on page 425.

Table H-1. xxFILL Rules

Rule	Description	Design Min		Current Practice.	
DS100	RXFILL must not touch {RXFILL, RX, PC, PCING, PCFUSE, (LOGOBND ¹ not touching CHIPEDGE), PROTECT, KERFEXCL, RXEXCLUD}	–	–	–	–
DS101	RXFILL minimum space to RX	≥	0.40	≥	0.60
DS102	RXFILL minimum space to {PC, PCING, LOGOBND, PROTECT, KERFEXCL, RXEXCLUD}	≥	0.20	≥	0.60
DS102a	RXFILL within (LOGOBND ¹ touching CHIPEDGE).	≥	0.40	≥	0.60
DS104	RXFILL minimum space to PCFUSE	≥	2.00	≥	3.00
DS105	RXFILL minimum space	≥	0.20	≥	0.30
DS105a ²	(RXFILL touching (BFMOAT or IND_FILT or BONDPAD)) minimum space	≥	0.20	≥	0.60
DS106	(RXFILL not touching (BFMOAT or IND_FILT or BONDPAD)) minimum width	≥	0.32	≡	0.90
DS107	(RXFILL not touching (BFMOAT or IND_FILT or BONDPAD)) maximum width	≤	1.80	≡	0.90
DS108	(RXFILL touching (BFMOAT or IND_FILT or BONDPAD)) minimum width	≥	0.32	≡	0.60

Table H-1. xxFILL Rules

Rule	Description	Design Min	Current Practice.
DS109	(RXFILL touching (BFMOAT or IND_FILT or BONDPAD)) maximum width	≤ 1.80	≡ 0.60
DS110	RXFILL within NW	≥ 0.30	≥ 0.40
DS111	RXFILL minimum space to NW with straddling prohibited	≥ 0.30	≥ 0.40
DS112PD ³	RXFILL minimum within BFMOAT	= -	≥ 0.60
DS113PD ³	RXFILL minimum space to BFMOAT with straddling prohibited	= -	≥ 0.60
DS114PD ³	RXFILL minimum within (IND_FILT, BONDPAD)	= -	≥ 0.60
DS115PD ³	RXFILL minimum space to (IND_FILT, BONDPAD) with straddling prohibited	= -	≥ 0.60
DS120	RXFILL within JD	≥ 0.80	≥ 0.80
DS121	RXFILL minimum space to JD with straddling prohibited	≥ 3.00	≥ 3.00
DS122	RXFILL within BB	≥ 1.50	≥ 1.50
DS123	RXFILL minimum space to BB with straddling prohibited	≥ 0.56	≥ 0.56
DS124	RXFILL must not touch {DT, PB, NP, LE, RN, NSR, OZ}	- -	- -
DS125	RXFILL minimum space to {DT, PB, NSR, OZ}	≥ 0.24	≥ 1.00
DS126	RXFILL minimum space to {NP, LE}	≥ 1.00	≥ 1.00
DS127	RXFILL minimum space to RN	≥ 0.36	≥ 1.00
DS198	RXFILL must be square	- -	- -
DS199	Rule Deleted	- -	- -
DS199a	RXFILL must be within (least enclosing rectangle of CHIPEDGE)	≥ 0.00	≥ 0.30
DS200	PCFILL must not touch (PCFILL, RX, PC, PCFUSE, LOGOBND, PROTECT, KERFEXCL, PCING, PCEXCLUD)	- -	- -
DS201	PCFILL minimum space to (PC, PCING)	≥ 0.40	≥ 0.60
DS202	PCFILL minimum space to (RX, LOGOBND, PROTECT, KERFEXCL, PCEXCLUD)	≥ 0.20	≥ 0.60
DS204	PCFILL minimum space to PCFUSE	≥ 2.00	≥ 3.00
DS205	PCFILL minimum space	≥ 0.20	≥ 0.52
DS205a ²	(PCFILL not touching (BFMOAT or IND_FILT or TLINE or BONDPAD) minimum space	≥ 0.20	≥ 0.52
DS205b ²	(PCFILL touching BFMOAT minimum space	≥ 0.20	≥ 0.60

Table H-1. xxFILL Rules

Rule	Description	Design Min		Current Practice.	
DS205c ²	(PCFILL touching (IND_FILT or TLINE or BONDPAD)) minimum space	≥	0.20	≥	0.68
DS205d	Rule Deleted	–	–	–	–
DS206	(PCFILL not touching (BFMOAT or IND_FILT or TLINE or BONDPAD)) minimum width	≥	0.33	≡	0.68
DS207	(PCFILL not touching (BFMOAT or IND_FILT or TLINE or BONDPAD)) maximum width	≤	1.80	≡	0.68
DS208	(PCFILL (touching (BFMOAT not over (IND_FILT or TLINE or BONDPAD))) minimum width	≥	0.33	≡	0.60
DS209	(PCFILL (touching (BFMOAT not over (IND_FILT or TLINE or BONDPAD))) maximum width	≤	1.80	≡	0.60
DS210	(PCFILL touching ((IND_FILT or TLINE or BONDPAD) or (BFMOAT over (IND_FILT or TLINE or BONDPAD)))) minimum width	≥	0.33	≡	0.52
DS211	(PCFILL touching ((IND_FILT or TLINE or BONDPAD) or (BFMOAT over (IND_FILT or TLINE or BONDPAD)))) maximum width	≤	1.80	≡	0.52
DS212PD ³	PCFILL minimum within BFMOAT	=	–	≥	0.60
DS213PD ³	PCFILL minimum space to BFMOAT with straddling prohibited	=	–	≥	0.60
DS214PD ³	PCFILL minimum within (IND_FILT, BONDPAD, TLINE)	=	–	≥	0.60
DS215PD ³	PCFILL minimum space to (IND_FILT, BONDPAD, TLINE) with straddling prohibited	=	–	≥	0.60
DS220	PCFILL must not touch JD	–	–	–	–
DS221	PCFILL minimum space to JD with straddling prohibited	≥	3.00	≥	3.00
DS222	PCFILL within BB	≥	1.50	≥	1.50
DS223	PCFILL minimum space to BB with straddling prohibited	≥	1.50	≥	1.50
DS224	PCFILL must not touch {DT, PB, PX, RN, (BB touching OZ)}	–	–	–	–
DS225	PCFILL minimum space to {DT, PB, PX, (BB touching OZ)}	≥	1.00	≥	1.00
DS227	PCFILL minimum space to RN	≥	0.50	≥	1.00
DS298	PCFILL must be square	–	–	–	–
DS299	Rule Deleted	–	–	–	–
DS299a	PCFILL must be within (least enclosing rectangle of CHIPEDGE)	≥	0.00	≥	0.30

Table H-1. xxFILL Rules					
Rule	Description	Design Min		Current Practice.	
DS500	MxFILL must not touch (Mx, MxFILL, KERFEXCL, LOGOBND, PROTECT, MxEXCLUD); Mx = M1-M4, MQ	–	–	–	–
DS502	(M1FILL, M2FILL) minimum space to PCFUSE with touching prohibited	≥	2.00	≥	3.00
DS511	MxFILL minimum space to Mx; Mx = M1-M4	≥	0.30	≥	0.40
DS511a	MxFILL minimum space to (Mx intersect MxPLANE); Mx = M1-M4, MQ	≥	10.00	≥	10.00
DS512	MxFILL minimum space to (LOGOBND, PROTECT, KERFEXCL, MxEXCLUD); Mx = M1-M4	≥	0.20	≥	0.40
DS512aa	MxFILL minimum space to BONDPAD with straddling prohibited; Mx=M1-M4	≥	4.90	≥	4.90
DS515	MxFILL minimum space; Mx = M1- M4	≥	0.20	≥	0.30
DS515a ²	(MxFILL touching (IND_FILT or BONDPAD)) minimum space; Mx = M1- M4	≥	0.20	≥	1.20
DS516	(MxFILL not touching (IND_FILT or BONDPAD)) minimum width; Mx = M1- M4	≥	0.35	≡	0.90
DS517	(MxFILL not touching (IND_FILT or BONDPAD)) maximum width; Mx = M1- M4	≤	2.40	≡	0.90
DS518	(MxFILL touching (IND_FILT or BONDPAD)) minimum width; Mx = M1- M4	≥	0.35	≡	0.60
DS519	(MxFILL touching (IND_FILT or BONDPAD)) maximum width; Mx = M1- M4	≤	2.40	≡	0.60
Note:	See Rule DS500 for MQ must not touch requirements	–	–	–	–
DS521	MQFILL minimum space to MQ	≥	0.40	≥	0.80
Note:	See Rule DS511a for MQ to (MQ over MQPLANE) requirements	–	–	–	–
DS522	MQFILL minimum space to (KERFEXCL, LOGOBND, PROTECT, MQEXCLUD)	≥	0.40	≥	0.80
DS522aa	MQFILL minimum space to BONDPAD with straddling prohibited	≥	4.90	≥	4.90
DS525	MQFILL minimum space	≥	0.40	≥	0.40
DS525a ²	(MQFILL not touching (IND_FILT or BONDPAD)) minimum space	≥	0.40	≥	0.40
DS525c ²	(MQFILL touching (IND_FILT or BONDPAD)) minimum space	≥	0.40	≥	1.20
DS525e	MQFILL minimum space to KQ with touching prohibited	≥	1.00	≥	1.25
DS526	(MQFILL not touching (IND_FILT or BONDPAD)) minimum width	≥	0.70	≡	1.20

Table H-1. xxFILL Rules

Rule	Description	Design Min	Current Practice.
DS527	(MQFILL not touching (IND_FILT or BONDPAD)) maximum width	≤ 3.20	≡ 1.20
DS528	(MQFILL touching (IND_FILT or BONDPAD)) minimum width	≥ 0.70	≡ 0.80
DS529	(MQFILL touching (IND_FILT or BONDPAD)) maximum width	≤ 3.20	≡ 0.80
DS530	LYFILL must not touch (LY, LYFILL, KERFEXCL, LOGOBND, PROTECT, LYEXCLUD, IND_FILT, BONDPAD, TLINE)	–	–
DS531	LYFILL minimum space to LY	≥ 1.52	≥ 4.00
DS532	LYFILL minimum space to (KERFEXCL, LOGOBND, PROTECT, LYEXCLUD, IND_FILT, TLINE)	≥ 1.52	≥ 4.00
DS532ba	LYFILL minimum space to (DV covered by AM)	≥ 6.50	≥ 10.50
DS532bb	LYFILL must not touch (DV sized by 6.5μm)	–	–
DS532cc	LYFILL minimum space to BONDPAD with straddling prohibited	≥ 4.90	≥ 4.90
DS535	LYFILL minimum space	≥ 1.52	≥ 1.80
DS536	LYFILL minimum width	≥ 1.52	≡ 1.80
DS537	LYFILL maximum width	≤ 10.00	≡ 1.80
DS570	AMFILL must not touch (AM, AMFILL, KERFEXCL, LOGOBND, PROTECT, AMEXCLUD, IND_FILT, BONDPAD, TLINE)	–	–
DS571	AMFILL minimum space to AM	≥ 5.00	≥ 8.00
DS572	AMFILL minimum space to (LOGOBND, PROTECT, KERFEXCL, AMEXCLUD, IND_FILT, BONDPAD, TLINE)	≥ 5.00	≥ 8.00
DS572b	AMFILL minimum space to (DV covered by AM) with touching prohibited	≥ 14.50	≥ 14.50
DS575	AMFILL minimum space	≥ 2.80	≥ 4.50
DS576	AMFILL minimum width	≥ 3.20	≡ 4.50
DS577	AMFILL maximum width	≤ 12.00	≡ 4.50
DS598	xxFILL must be square; where xx = M1- M4, MQ, LY, AM	–	–
DS599	Rule Deleted	–	–
DS599a	xxFILL must be within (least enclosing rectangle of CHIPEDGE), where xx = M1- M4, MQ, LY, AM	≥ 0.00	≥ 0.00

1. LOGOBND within CHIPEDGE receives RXFILL. LOGOBND used in the IBM KERF shall not receive RXFILL (with straddling prohibited).

2. Rule is not required to be verified in IBM Design Services Design Rule Checking (DRC) deck. Rule is included to document that as xxFILL is width is reduced, when xxFILL is touching specific Dummy Design and Utility Levels to intentionally lower the pattern density in the chip design. the xxFILL space is increased the same incremental amount.

3. Rules not DRC verified. Rules included for predictive local pattern density verification only.

Table H-2. xxHOLE Rules					
Rule	Description	Design Min		Current Practice.	
NOTE ¹	The term incurring is used in this table, and the syntax for incurring is defined as: A incurring B means A such that A has any area in common with B	–	–	–	–
DS600	MxHOLE must not touch (MxHOLE, MxCHEXCL); Mx = M1-M4, MQ	–	–	–	–
DS608	M1HOLE must not touch (CABAR, V1BAR)	–	–	–	–
DS608a	M1HOLE must not touch CEBAR	–	–	–	–
DS608b ²	M1HOLE minimum space to (CEBAR, CABAR, V1BAR)	>	0.00	≥	0.01
DS609	MxHOLE must not touch (VxBAR, VwBAR); Mx = M2-M4, MQ; Vx = via level above Mx; not including VYBAR above MQ. Vw = via level below Mx	–	–	–	–
DS609b	MQHOLE must not touch (VYBAR touching GUARDRNG)	–	–	–	–
DS611	MxHOLE must be within Mx; Mx = M1-M4	≥	0.30	≥	0.40
DS612	MxHOLE minimum space to MxCHEXCL; Mx = M1-M4	>	0.00	>	0.00
DS615	(MxHOLE not touching MxPLANE) minimum space; Mx = M1-M4	≥	0.60	≥	0.60
DS616	(MxHOLE not touching MxPLANE) minimum width; Mx = M1-M4	≥	0.60	≡	0.60
DS617	(MxHOLE not touching MxPLANE) maximum width; Mx = M1-M4	≤	0.60	≡	0.60
DS618	(CA touching (((M1HOLE not touching M1PLANE) or ((M1HOLE touching M1PLANE) sized by -0.07μm))) must touch (((CA not touching ((M1HOLE not touching M1PLANE) or ((M1HOLE touching M1PLANE) sized by -0.07μm))) sized by 1.80μm) over RX) over M1) not PC)	–	–	–	–
DS619	(Vx incurring (((MxHOLE not touching MxPLANE) or ((MxHOLE touching MxPLANE) sized by -0.07μm)) or ((MyHOLE not touching MyPLANE) or ((MyHOLE touching MyPLANE) sized by -0.07μm)))) must touch (((Vx not incurring (((MxHOLE not touching MxPLANE) or ((MxHOLE touching MxPLANE) sized by -0.07μm)) or ((MyHOLE not touching MyPLANE) or ((MyHOLE touching MyPLANE) sized by -0.07μm)))) sized by 1.80μm) over Mx) over My); Vx = V1-V3; Mx = metal below Vx; My = metal above Vx, and where the smallest chord connecting the two vias lies entirely within Mx and My.	–	–	–	–

Table H-2. xxHOLE Rules

Rule	Description	Design Min		Current Practice.	
DS620 ³	[Vx touching (((MyHOLE not touching MyPLANE) sized by -0.10μm) or ((MyHOLE touching MyPLANE) sized by -0.17μm)))] must touch [{ ([Vx not touching (((MyHOLE not touching MyPLANE) sized by -0.10μm) or ((MyHOLE touching MyPLANE) sized by -0.17μm)))] not incurring ((MxHOLE not touching MxPLANE) or ((MxHOLE touching MxPLANE) sized by -0.07μm))) sized by 1.80μm } over intersection (Mx, My)] Vx = V1-V3; Mx = metal below Vx; My = metal above Vx.	–	–	–	–
DS621	MQHOLE must be within MQ	≥	0.40	≥	0.80
DS622	MQHOLE minimum space to MQCHEXCL	>	0.00	>	0.00
DS625	MQHOLE minimum space	≥	0.60	≥	0.80
DS626	(MQHOLE not touching MQPLANE) minimum width	≥	0.80	≡	0.80
DS627	(MQHOLE not touching MQPLANE) maximum width	≤	0.80	≡	0.80
DS630	(VL incurring ((MxHOLE not touching MxPLANE) or ((MxHOLE touching MxPLANE) sized by -0.07μm))) must touch (((VL not incurring ((MxHOLE not touching MxPLANE) or ((MxHOLE touching MxPLANE) sized by -0.07μm))) sized by 1.80μm) over Mx) over MQ); Mx = metal below VL, and where the smallest chord connecting the two vias lies entirely within Mx and MQ.	–	–	–	–
DS631	(VL incurring ((MQHOLE not touching MQPLANE) or ((MQHOLE touching MQPLANE) sized by -0.09μm))) must touch (((VL not incurring ((MQHOLE not touching MQPLANE) or ((MQHOLE touching MQPLANE) sized by -0.09μm))) sized by 2.40μm) over Mx) over MQ); Mx = metal below VL, and where the smallest chord connecting the two vias lies entirely within Mx and MQ.	–	–	–	–
DS632 ⁴	(VL touching (((MQHOLE not touching MQPLANE) sized by -0.09μm) or ((MQHOLE touching MQPLANE) sized by -0.29μm))) must touch (((((VL not touching (((MQHOLE not touching MQPLANE) sized by -0.09μm) or ((MQHOLE touching MQPLANE) sized by -0.29μm))) not incurring ((MxHOLE not touching MxPLANE) or ((MxHOLE touching MxPLANE) sized by -0.07μm))) sized by 2.40μm) over Mx) over MQ); Mx = metal below VL, and where the smallest chord connecting the two vias lies entirely within Mx and MQ.	–	–	–	–
DS633	Any ((M1 over RX) not PC) that has a CA incurring M1HOLE must have at least 3 CA's that do not incur M1HOLE	–	–	–	–

Table H-2. xxHOLE Rules

Rule	Description	Design Min		Current Practice.	
DS634	Any (Mx over My) that has a Vx incurring on either (MxHOLE or MyHOLE) must have at least 3 Vx that do not incur on either (MxHOLE or MyHOLE). Vx = V1-V3, VL; Mx = metal below Vx; My = metal above Vx	–	–	–	–
DS634a ⁵	Any (MQ over LY) that has a VY incurring on either MQHOLE must have at least 4 VY that do not incur on MQHOLE	–	–	–	–
DS634aa	Rule deleted	–	–	–	–
DS635	(MxHOLE touching MxPLANE) minimum space; Mx = M1-M4	≥	0.46	≥	0.46
DS635a	(MxHOLE touching MxPLANE) to (MxHOLE not touching MxPLANE) minimum space; Mx = M1-M4	≥	0.46	≥	0.46
DS636	(MxHOLE touching MxPLANE) minimum width; Mx = M1-M4	≥	0.74	≡	0.74
DS637	(MxHOLE touching MxPLANE) maximum width; Mx = M1-M4	≤	0.74	≡	0.74
DS655	(MQHOLE touching MQPLANE) minimum space	≥	0.62	≥	0.62
DS656	(MQHOLE touching MQPLANE) minimum width	≥	0.98	≡	0.98
DS657	(MQHOLE touching MQPLANE) maximum width	≤	0.98	≡	0.98
DS698	MxHOLE must be square; Mx = M1-M4, MQ	–	–	–	–
DS810	VxHOLE must be within Vx; Vx = V1-V3 VL	≡	0	≡	0
DS820	VxHOLE must be within MyHole; Vx = V2,V3; My = metal level above Vx	≥	0.00	>	0.00
DS821	V1HOLE must be within M2HOLE	≥	0.00	>	0.00
DS830	VLHOLE must be within MQHOLE	≥	-0.19	≥	-0.19

1. This is not a Rule. It is included in this table as a unique definition to aid in verification of the DSxxx Rule in Design Rule Checking (DRC).
2. Rule 608b is shaded GRAY background and is not required to be checked in DRC, as its criteria is met by Rules DS608 and DS608a
3. For Vx, DS620 is a more relaxed check of DS619 in the event of a DS619 error.
4. For VQ and VG, DS632 is a more relaxed check for DS628 in the event of a DS628 error.
5. MQHOLE shapes are allowed to incur or cover certain VY vias, as long as those vias are strictly redundant, by virtue of sufficient unobstructed connections between the same segments of wide metal. MQHOLE shapes can not touch any VY perimeter vias, in a via array. MQHOLE shapes are not prohibited from touching VYBAR vias within CHIPEDGE, except MQHOLE shapes must not touch VYBAR vias in the chip guard ring (touching GUARDRNG) per Rule DS609b. The via resistance specified in Table 4-30, "Via Resistance," on page 283 is met for any collection of redundant via shapes, even in the presence of MQHOLE shapes. Contact your PE or Dept. G39 for further details.

Table H-3. Pattern Density Rules

Rule	Description	Design Min		Current Practice.	
PD1a	(RX, RXFILL) minimum density(%) with 126μm tiling ¹	≥	20	≥	20
PD1b	(RX, RXFILL) minimum global density(%)	≥	25	≥	25
PD2	(PC, PCFILL) minimum density (%) within CHIPEDGE.	≥	15	≥	15
PD2aR ²	(PC, PCFILL) minimum density (%) with 126μm tiling. Exemption: Tile touching LOGOBND, PROTECT.	≥	5	≥	5
PD4a	(Mx, MxFILL) minimum density (%) with 126μm tiling. Mx = M1, M2, M3, M4, MQ Exemption: Tile touching IND_FILT, BONDPAD, LOGOBND.	≥	10	≥	10
PD4a1	(Mx, MxFILL) minimum density (%) with 126μm tiling for all tiles touching IND_FILT, BONDPAD. Mx = M1, M2, M3, M4, MQ.	≥	8	≥	8
PD4b ³	(Mx not over MxHOLE) maximum density (%) with 50μm tiling Mx = M1, M2, M3, M4, MQ.	≤	85	≤	85
PD5a	(LY, LYFILL) minimum global density (%).	≥	23	≥	23
PD5m	(AM, AMFILL) minimum global density (%).	≥	23	≥	23

1. For this local density requirement, the checking box is 126μm x 126μm stepped in 63μm increments. Rule PD1a is not in force for any checking box that touches corner chamfers and PROTECT regions which are outside of CHIPEDGE. IBM includes RXFILL within LOGOBND regions. If a designer places an RXEXCLUD within LOGOBND, it is expected that the checking box touching the (RXEXCLUD over LOGOBND) still comply with the minimum density value specified. The only exception for RX local density is within the IBM KERF LOGOBND area, since RXFILL is not automatically included in this region. The interpretation of (RX, RXFILL) in this description is the equivalent of Union (RX, RXFILL), which is the sum of the Design Level RX and the Reserved Level RXFILL, for checking purposes of this rule. The Current Practice value specified is the value that is to be coded into the IBM Release Team Design Rule checking decks used by IBM, and represents the minimum density acceptable after Design Services is applied to a chip during the IBM release process.
2. Rule PD2aR is recommended rules. These rules are not required to be verified in the external customer technology design kit. This rule is only coded using a recommended rule switch or other coding methods for IBM internal post design services validation tools.
3. For this local density requirement, the checking box is 50μm x 50μm stepped in 25μm increments. The Current Practice value specified is the value that is to be coded into the IBM Release Team Design Rule checking decks used by IBM, and represents the maximum density acceptable after Design Services is applied to a chip during the IBM release process. However, predictive density tools in the Technology Design Kit may actually be on the order of 5% lower than the Current Practice specified, to account for tool-to-tool consistency considerations.

H.1.1 Estimated Pattern Density Generation

Estimated pattern density algorithms are listed in the tables below, to assist with verification during design layout. These algorithms estimate the final design pattern density after IBM Design Services FILL shapes have been added to a layout. These density estimations provide an early warning to customers for regions of low density. The algorithms are provided in detail below in order to provide designers additional understanding of how various layout shapes affect the placement of IBM generated FILL.

Devices and Design Levels receiving RXFILL less than 45% local density:

- P+ polysilicon OP resistors, NS resistors (NSR), deep trench (DT), electrical fuses (PCFUSE), NPNs or similar structures (PB, NP, LE, RN) and RXEXCLUD are excluded from RXFILL.
- BF moat regions (BFMOAT) and BEOL inductors (IND_FILT) and modelled bondpads (BONDPAD) have RXFILL = 20% local density.

Devices and design levels receiving PCFILL less than 25% local density:

- N+ diffusion OP resistors, n-well to substrate capacitors, p+/n-well junction varactors, HA varactors, deep trench (DT), NPNs or similar structures (PB, PX, RN) and PCEXCLUD are excluded from PCFILL.
- BF moat regions (BFMOAT) have PCFILL = 20% local density.
- BEOL inductors (IND_FILT), modelled rlines (TLINE) and bondpads (BONDPAD) have PCFILL = 15% local density

Devices and design levels receiving MQFILL less than 45% local density:

- BEOL resistors (KQ) have MQFILL = 0% local density
- BEOL inductors (IND_FILT) and bondpads (BONDPAD) have MQFILL = 8.8% local density

Table H-4. Estimated Pattern Density Rules

Rule	Notes	Description
RX Estimated Pattern Density Checking Details		<p>DS101=0.60, DS102=0.60, DS102a=0.60, DS104=3.00, DS105=0.30, DS105a=0.60, DS106=0.90, DS110=0.40, DS11xPD=0.60, DS111=0.40, DS120=0.80, DS121=3.00, DS122=1.50, DS123=0.56, DS125=1.00, DS126=1.00, DS127=1.00.</p> <p>IN_SHAPE=union(BONDPAD, IND_FILT, BFMOAT) RX_EXP = Union(RX, PC) sized by +50 RXEX_FRAME = CHIPEDGE sized by -50 RXEX_AREA_TO_FILL = difference(RXEX_FRAME, RX_EXP) sized by -500 then sized by +500</p> <p>A = rx_ds102 = (union{ PC, PCING, (BONDPAD touching PC), (LOGOBND not touching CHIPEDGE), PROTECT, KERFEXCL, RXEXCLUD }) sized by +DS102 B = rx_ds101 = (RX sized by +DS101) C = rx_fuse_excl = (PCFUSE sized by +DS104) D = rx_nw_excl = difference [(NW sized by +DS111), (NW sized by -DS110)] E = rx_jd_excl = difference [(JD sized by +DS121), (JD sized by -DS120)] F = rx_bb_excl = difference [(BB sized by +DS123), (BB sized by -DS122)] G = rx_ds125 = (union{DT, PB, NSR}) sized by +DS125 H = rx_ds126 = (union{NP, LE}) sized by +DS126 I = rx_rn_excl = (RN sized by +DS127) J = rx_ind_excl = difference [(IN_SHAPE sized by DS11xPD), (IN_SHAPE sized by -DS11xPD)] K = rx_ds102a = difference [(LOGOBND sized by +DS102a), (LOGOBND sized by -DS102a)] L = rx_ce_excl = difference [(CHIPEDGE sized by +0.40),(CHIPEDGE sized by -0.40)]</p> <p>rx_pitch = (DS105 + DS106) / 2 rx_limit = (DS106 + rx_pitch) rx_slivr = rx_pitch / 6</p> <p>rx_no_fill = (union {A,B,C,D,E,F,G,H,I,J,K,L} sized by +(rx_limit/2)) sized by -(rx_pitch/2 - rx_slivr) rx_std_fill_region = difference [(Least enclosing rectangle of CHIPEDGE) , union {rx_no_fill, IN_SHAPE}] rx_std_fill = difference(rx_std_fill_region, RXEX_AREA_TO_FILL) rx_std_fill_po = intersection(rx_std_fill_region, RXEX_AREA_TO_FILL) rx_low_fill = difference [IN_SHAPE, rx_no_fill]</p>
EPDL_RX_min	1	<p>(rx_estimated) local density with 126μm tiling stepped in 63μm increments within CHIPEDGE >= 20% where rx_estimated = [area(RX) + (0.45 * area(rx_std_fill)) + (0.405 * area(rx_std_fill_po)) + (0.20 * area(rx_low_fill))] / area(126 * 126)</p>
EPDG_RX_min		<p>(rx_estimated) global density within CHIPEDGE >= 25% where rx_estimated = [area(RX) + (0.45 * area(rx_std_fill)) + (0.405 * area(rx_std_fill_po)) + (0.20 * area(rx_low_fill))] / area(CHIPEDGE)</p>

Table H-4. Estimated Pattern Density Rules

Rule	Notes	Description
PC Estimated Pattern Density Checking Details		<p>DS201=0.60, DS202=0.60, DS204=3.00, DS205=0.52, DS205a=0.52, DS205b=0.60, DS206=0.68, DS210=0.52, DS211=0.52, DS220=0.80, DS221=3.00, DS222=1.50, DS223=1.50, DS225=1.00, DS227=1.00, DS299a=0.30</p> <p>IN_SHAPE=union(BONDPAD, IND_FILT, TLINE)</p> <p>A = pc_ds202 = (union{ RX, LOGOBND, PROTECT, KERFEXCL, PCEXCLUD }) sized by +DS202 B = pc_ds201 = (union{ PC, PCING} sized by +DS201) C = pc_fuse_excl = (PCFUSE sized by +DS204) D = pc_jd_excl = (JD sized by +DS221) E = pc_bb_excl = difference [(BB sized by +DS223), (BB sized by -DS222)] F = pc_bfm_excl = difference [(BFMOAT sized by DS205b), (BFMOAT sized by -DS205b)] G = pc_rn_excl = (RN sized by +DS227) H = pc_ds225_excl = (union{DT,PB,PX,(BB touching OZ) } sized by +DS225) I = pc_ind_excl = difference [(IN_SHAPE sized by DS205b), (IN_SHAPE sized by -DS205b)] J = pc_ce_excl = difference [(CHIPEDGE sized by +0.60),(CHIPEDGE sized by -0.60)]</p> <p>pc_pitch = (DS206 + DS205a) / 2 pc_limit = (DS206 + pc_pitch) pc_slivr = pc_pitch / 6</p> <p>pc_no_fill = (union {A,B,C,D,E,F,G,H,I,J} sized by +(pc_limit/2)) sized by -(pc_pitch/2 - pc_slivr) pc_std_fill = difference [(Least enclosing rectangle of CHIPEDGE) , union {pc_no_fill, IN_SHAPE, BFMOAT}] pc_bfm_fill = difference [BFMOAT, union(pc_no_fill, IN_SHAPE)] pc_low_fill = difference [IN_SHAPE, pc_no_fill]</p>
EPDG_PC_min	2,3	<p>(pc_estimated) global density within CHIPEDGE >= 15%</p> <p>where pc_estimated = [area(PC) + area(PCING) + (0.257 * area(pc_std_fill)) + (0.15 * area(pc_low_fill)) + (0.2 * area(pc_bfm_fill))] / area(CHIPEDGE)</p>
EPDL_PC_minR		<p>(pc_estimated) local density with 126μm tiling stepped in 63μm increments within CHIPEDGE >= 5%</p> <p>Exemption: Checking boxes that touch LOGOBND or PROTECT.</p> <p>where pc_estimated = [area(PC) + area(PCING) + (0.257 * area(pc_std_fill)) + (0.15 * area(pc_low_fill)) + (0.2 * area(pc_bfm_fill))] / (126 * 126)</p>

Table H-4. Estimated Pattern Density Rules

Rule	Notes	Description
Mx Estimated Pattern Density Checking Details (where x=1 or 2)		<p>DS502=3.00, DS511=0.40, DS511a=10.00, DS512=0.40, DS512aa=4.90 DS515=0.30, DS516=0.90. mx_planei= intersection of Mx, MxPLANE</p> <p>A=mx_ds511 = Mx sized by +DS511 B=mx_ds512 = (union{ LOGOBND,PROTECT, KERFEXCL, MxEXCLUD }) sized by +DS512 C=mx_ds502 = PCFUSE sized by +DS502 D=mx_planei sized by +DS511a E=mx_bondpad = difference{(BONDPAD sized by +DS512aa),(BONDPAD sized by -DS512)} F=mx_ind= difference{(IND_FILT sized by +DS512),(IND_FILT sized by -DS512)} G=mx_ce_excl = difference [(CHIPEDGE sized by +DS512),(CHIPEDGE sized by -DS512)</p> <p>mx_pitch = (DS516 + DS515) / 2 mx_limit = (DS516 + mx_pitch) mx_slivr = mx_pitch / 6 mx_no_fill = (union{A,B,C,D,E,F,G} sized by +(mx_limit/2)) sized by -(mx_pitch/2 - mx_slivr) mx_in_shape = union { BONDPAD, IND_FILT } mx_std_fill = difference [(Least enclosing rectangle of CHIPEDGE) , union{mx_no_fill, mx_in_shape}] mx_low_fill = difference [mx_in_shape, mx_no_fill]</p>
EPDL_M1_min		<p>(m1_estimated) local density with 126μm tiling stepped in 63μm increments within CHIPEDGE >= 10% Exemption: Checking boxes that touch LOGOBND, BONDPAD or IND_FILT. where m1_estimated = area(M1) + 0.45 * area(m1_std_fill) + 0.089 * area(m1_low_fill)] / (126 * 126)</p>
EPDLi_M1_min		<p>(m1_estimated) local density with 126μm tiling stepped in 63μm increments within CHIPEDGE >= 8% Requirement: Checking boxes must touch IND_FILT or BONDPAD. where m1_estimated = area(M1) + 0.45 * area(m1_std_fill) + 0.089 * area(m1_low_fill)] / (126 * 126)</p>
EPDL_M2_min		<p>(m2_estimated) local density with 126μm tiling stepped in 63μm increments within CHIPEDGE >= 10% Exemption: Checking boxes that touch LOGOBND, BONDPAD or IND_FILT. where m2_estimated = area(M2) + 0.45 * area(m2_std_fill) + 0.089 * area(m2_low_fill)] / (126 * 126)</p>

Table H-4. Estimated Pattern Density Rules

Rule	Notes	Description
EPDLi_M2_min		<p>(m2_estimated) local density with 126μm tiling stepped in 63μm increments within CHIPEDGE >= 8%</p> <p>Requirement: Checking boxes must touch IND_FILT or BONDPAD.</p> <p>where $m2_estimated = area(M2) + 0.45 * area(m2_std_fill) + 0.089 * area(m2_low_fill)] / (126 * 126)$</p>
Mz Estimated Pattern Density Checking Details (where z=3 or 4)		<p>DS511=0.40, DS511a=10.00, DS512=0.40, DS512aa=4.90 DS515=0.30, DS516=0.90.</p> <p>mz_planei= intersection of Mz, MzPLANE</p> <p>A = mz_ds511 = union{ Mz, MzRV} sized by +DS511</p> <p>B = mz_ds512 = (union{ LOGOBND,PROTECT, KERFEXCL, MzEXCLUD }) sized by +DS512</p> <p>D = mz_planei sized by +DS511a</p> <p>E = mz_bondpad = difference{(BONDPAD sized by +DS512aa),(BONDPAD sized by -DS512)}</p> <p>F = mz_ind = difference{(IND_FILT sized by +DS512),(IND_FILT sized by -DS512)}</p> <p>G = mz_ce_excl = difference [(CHIPEDGE sized by +DS512),(CHIPEDGE sized by -DS512)</p> <p>mz_pitch = (DS516 + DS515) / 2</p> <p>mz_limit = (DS516 + mz_pitch)</p> <p>mz_slivr = mz_pitch / 6</p> <p>mz_no_fill = (union{A,B,D,E,F,G} sized by +(mz_limit/2)) sized by -(mz_pitch/2 - mz_slivr)</p> <p>mz_in_shape = union { BONDPAD, IND_FILT }</p> <p>mz_std_fill = difference [(Least enclosing rectangle of CHIPEDGE) , union{mz_no_fill, mz_in_shape}]</p> <p>mz_low_fill = difference [mz_in_shape, mz_no_fill]</p>
EPDL_M3_min		<p>(m3_estimated) local density with 126μm tiling stepped in 63μm increments within CHIPEDGE >= 10%</p> <p>Exemption: Checking boxes that touch LOGOBND, BONDPAD or IND_FILT.</p> <p>where $m3_estimated = area(M3) + 0.45 * area(m3_std_fill) + 0.089 * area(m3_low_fill)] / (126 * 126)$</p>
EPDLi_M3_min		<p>(m3_estimated) local density with 126μm tiling stepped in 63μm increments within CHIPEDGE >= 8%</p> <p>Requirement: Checking boxes must touch IND_FILT or BONDPAD.</p> <p>where $m3_estimated = area(M3) + 0.45 * area(m3_std_fill) + 0.089 * area(m3_low_fill)] / (126 * 126)$</p>

Table H-4. Estimated Pattern Density Rules

Rule	Notes	Description
EPDL_M4_min		(m4_estimated) local density with 126μm tiling stepped in 63μm increments within CHIPEDGE >= 10% Exemption: Checking boxes that touch LOGOBND, BONDPAD or IND_FILT. where m4_estimated = area(M4) + 0.45 * area(m4_std_fill) + 0.089 * area(m4_low_fill)] / (126 * 126)
EPDLi_M4_min		(m4_estimated) local density with 126μm tiling stepped in 63μm increments within CHIPEDGE >= 8% Requirement: Checking boxes must touch IND_FILT or BONDPAD. where m4_estimated = area(M4) + 0.45 * area(m4_std_fill) + 0.089 * area(m4_low_fill)] / (126 * 126)
MQ Estimated Pattern Density Checking Details		<p>DS511a=10.00, DS521=0.80, DS522=0.80, DS522aa=4.90, DS525=0.40, DS526=1.20. mq_planei= intersection of MQ, MQPLANE</p> <p>A = mq_ds521 = union{ MQ, MQRV} sized by +DS521 B = mq_ds522 = (union{ LOGOBND,PROTECT, KERFEXCL, MQEXCLUD }) sized by +DS522 D = mq_planei sized by +DS511a E = mq_bondpad = difference{(BONDPAD sized by +DS522aa),(BONDPAD sized by -DS522) F = mq_ind = difference{(IND_FILT sized by +DS522),(IND_FILT sized by -DS522)} G = mq_ce_excl = difference [(CHIPEDGE sized by +DS522),(CHIPEDGE sized by -DS522)</p> <p>mq_pitch = (DS526 + DS525) / 2 mq_limit = (DS526 + mq_pitch) mq_slivr = mq_pitch / 6 mq_no_fill = (union{A,B,D,E,F,G} sized by +(mq_limit/2)) sized by -(mq_pitch/2 - mq_slivr) mq_in_shape = union { BONDPAD, IND_FILT } mq_std_fill = difference [(Least enclosing rectangle of CHIPEDGE) , union{mq_no_fill, mq_in_shape}] mq_low_fill = difference [mq_in_shape, mq_no_fill]</p>
EPDL_MQ_min		(mq_estimated) local density with 126μm tiling stepped in 63μm increments within CHIPEDGE >= 10% Exemption: Checking boxes that touch LOGOBND, BONDPAD or IND_FILT. where mq_estimated = area(MQ) + 0.45 * area(mq_std_fill) + 0.089 * area(mq_low_fill)] / (126 * 126)

Table H-4. Estimated Pattern Density Rules

Rule	Notes	Description
EPDLi_MQ_min		<p>(mq_estimated) local density with 126μm tiling stepped in 63μm increments within CHIPEDGE >= 8%</p> <p>Requirement: Checking boxes must touch IND_FILT or BONDPAD.</p> <p>where $mq_estimated = \text{area}(MQ) + 0.45 * \text{area}(mq_std_fill) + 0.089 * \text{area}(mq_low_fill)] / (126 * 126)$</p>

1. See Rule 40, design minimum column, in Table 3-1, "Polysilicon and Isolation Layout Rules," on page 69.
2. See Rule PDPC, design minimum column, in Table 2-15, "Pattern Density Rules," on page 62.
3. Use the Current Practice column rule values listed in Table H-1. "xxFILL Rules" on page 417 for the DSxxx layout rule numbers referenced in the predictive density rule table.

H.2 Recommended Design Practices Related to Generated FILL and HOLES Shapes

Designers are encouraged to follow the following recommendations. Disregard for these recommendations may result in designs that cannot be adequately treated by the IBM FILL and HOLE generation tools. Violations of rules PD1a, PD2, PD4a, PD4a1 or PD4b may occur, resulting in potential delays of the product. Certain of the discouraged design practices enumerated below can be tolerated if their extent is small and the distance between them is large. If the recommended Design Practices can not be observed in every case, contact IBM Product Engineering for assistance defining acceptable limits and assessing the encumbent risks to the design.

- **Avoid long or dense runs of RX wiring or PC wiring.** RX and PC wiring inhibit the placement of RXFILL and PCFILL generated shapes, potentially leading to violations of PD1 and PD2. RX wiring and PC wiring are generally inefficient current-carrying members, by virtue of the high resistance and high Rs tolerances, relative to M1 or other general-purpose metal wiring levels. Long or dense runs of RX wiring or PC wiring are generally discouraged, apart from the mentioned pattern-density issues.
- **Avoid the use of "dummy" shapes on RX, PC, and all metal levels.** Designer-added dummy shapes inhibit the placement of IBM-generated FILL shapes, potentially leading to violations of PD1, PD2, and PD4a. IBM-generated Fill shapes are structurally and hierarchically optimized to provide maximum yield and manufacturability improvement with minimum perturbation to the circuit. Large designer-added dummy shapes are less useful to manufacturing, and more disruptive to the circuit. Small designer-added dummy shapes are more burdensome for Design Services, DataPrep and Mask Manufacturing, and can be also be problematic for wafer manufacturing.
- **Avoid the use of slotted or otherwise "precheesed" wiring for Copper levels.** Slotted or precheesed metal inhibits the effective placement of Metal Hole shapes, potentially leading to violations of PD4b. IBM-generated Metal Hole shapes are structurally and hierarchically optimized to provide maximum yield and manufacturability improvement with minimum penalty. Precheesed metal can greatly increase the computational burden for Design Services and Data Prep, increasing the cycle time for these processes, or causing the job steps to fail completely. For practical wiring structures, IBM-generated Metal Hole shapes provide lower resistance and Rs tolerance than any allowable slotted or precheesed structure.
- Whenever possible, it is recommended that collections of vias connecting the same two pieces of metal

be drawn as simple linear or 2D arrays. For linear arrays, it is recommended that the individual vias have zero offset from one another in one dimension, and be evenly spaced in the other. For 2D arrays of redundant vias, it is not necessary to use the same pitch in the X and Y directions, but it is strongly recommended that the vias be drawn so as to neatly line up in each direction. Double or single rings of vias are an acceptable alternative to regular 2D arrays of redundant vias.

- Whenever possible, it is recommended that collections of vias on adjacent levels be drawn so as to line up vertically. It is not recommended to have collections of vias on adjacent levels be offset from one another, except where such an arrangement is unavoidable. Vertical alignment is not necessary for VL and the via level immediately beneath it.

Appendix I. MxPLANE Information

I.1 Introduction

The BiCMOS8HP technology supports copper Mx ($x=1,2,3,4,Q$) wire widths $> 50\mu\text{m}$. However, experience manufacturing designs using copper Mx wire widths $> 50\mu\text{m}$ is evolving in contrast to long term experience manufacturing copper Mx wire widths $\leq 50\mu\text{m}$.

Mx wire widths $> 50\mu\text{m}$ must be covered by its corresponding MxPLANE Dummy Design and Utility Level ($x=1,2,3,4,Q$). See MxPLANE in Table 2-4, “Dummy Design Levels and Utility Levels,” on page 36 ($x=1,2,3,4,Q$). See also Rules 500b, 500c, and 500e in Table 3-9, “CA, M1 Metal and Via Layout Rules,” on page 96 and Rules 600b, 600c, and 600e in Table 3-10, “Mx ($x=2,3,4$) Metal and Via Layout Rules,” on page 103, and Rules 690b, 690c and 690e in Table 3-12, “MQ (Thick Metal) Layout Rules,” on page 109.

Designs including copper Mx ($x=1,2,3,4,Q$) wire widths $> 50\mu\text{m}$ must be communicated to your IBM Product Engineer.

Design wide wires or “planes” using either the (LY or AM) aluminum metal levels rather than Mx ($x=1,2,3,4,Q$) copper metal levels for improved manufactureability and process tolerance (better Rs and interdielectric thickness control).

The discussion in this section only applies to the Mx ($x=1,2,3,4,Q$) metal levels. Additional layout rules or process variation does not occur for LY or AM wires that vary from design minimum to very large widths.

I.2 Definitions

Equivalent terminology for Mx wire widths $> 50\mu\text{m}$ (MxPLANEs) in contrast to Mx wire widths $\leq 50\mu\text{m}$ ($x=1,2,3,4,Q$) are:

- Mx wires widths $> 50\mu\text{m}$ = (Mx over MxPLANE) = MxPLANE = Mx “plane”, where ($x=1,2,3,4,Q$)
- Mx wire widths $\leq 50\mu\text{m}$ = Mx = (Mx not covered by MxPLANE) and are also sometimes referred to as narrow or wide wires (but not “planes”) where ($x= 1,2,3,4,Q$)

I.3 Design Considerations

Designers including Mx wires widths $> 50\mu\text{m}$ (i.e., planes) should consider the following aspects in contrast to designing with Mx wire widths $\leq 50\mu\text{m}$ ($x=1,2,3,4,Q$):

- Wire thickness variation
- Interlevel dielectric thickness variation
- Mx effective linewidth calculation (resulting from IBM generated Metal Hole Generation)
- Electromigration considerations
- Layout spacing of (Mx) versus (Mx over MxPLANE) wires

- Layout identification of Mx wire widths > 50 μ m
- FEOL device wiring using MxPLANE
- BEOL wiring using MxPLANE

See additional information in see section I.4 , “Design Guidelines” on page 435.

I.4 Design Guidelines

The following information is provided for layout design using Mx wires widths > 50 μ m in contrast to, or concurrently with, Mx wire widths \leq 50 μ m (x=1,2,3,4,Q) in a chip design.

I.4.1 Mx effective linewidth calculation (and MxHOLE Generation)

Mx wire widths > 50 μ m receive larger MxHOLE shapes, that are automatically generated by IBM, in contrast to Mx wire widths \leq 50 μ m (x=1,2,3,4,Q). The MxHOLE size generated is controlled by the presence or absence of the MxPLANE Dummy Design and Utility Level over the Mx wires.

For Mx wire widths \leq 50 μ m (i.e., Mx not covered by MxPLANE) effective linewidth calculation in contrast to Mx wires widths > 50 μ m (Mx over MxPLANE), see:

- Section Table 4-32., “Effective Linewidth for Wires with HOLE Shapes” on page 286:
 - See rows identified as (Mx) versus (Mx over MxPLANE), where x=1,2,3,4,Q

I.4.1.1 MxHOLE Size Information

For additional information about the sizes of the IBM generated MxHOLE shapes, see:

- Table H-2, “xxHOLE Rules,” on page 422:
 - Rules DS616, DS617, DS626, DS627 for (Mx) wire widths \leq 50 μ m, where x=1,2,3,4, Q
 - Rules DS636, DS637, DS656, DS657 for (Mx over MxPLANE) wire widths > 50 μ m, where x=1,2,3,4,Q

I.4.2 Electromigration considerations

Wire current handling capacity is lower for Mx wire widths > 50 μ m compared to Mx wire widths \leq 50 μ m as a result of the decreased effective linewidth (i.e., increase in MxHOLE size).

For Mx wire widths \leq 50 μ m (i.e., Mx not covered by MxPLANE) effective linewidth calculation in contrast to Mx wire widths > 50 μ m (Mx over MxPLANE), see:

- Section Table 4-32., “Effective Linewidth for Wires with HOLE Shapes” on page 286, using rows identified as (Mx) versus (Mx over MxPLANE), where x=1,2,3,4,Q and Table 5.4.1, “Electromigration (EM),” on page 358.

I.4.3 Layout spacing of (Mx) versus (Mx over MxPLANE) wires

This section applies to wiring consideration on the same Mx metal level ($x=1,2,3,4,Q$)

Spacing between Mx wires is dependent on Mx wire width, including (Mx over MxPLANE) wires.

For Mx wire widths $\leq 50\mu\text{m}$ (i.e., Mx not covered by MxPLANE) spacing to Mx wires widths $> 50\mu\text{m}$ (Mx over MxPLANE), see:

- For M1, see Rules 502, 504, 504b, 504c and 504b in contrast to Rules 504e and 504f in Table 3-9, “CA, M1 Metal and Via Layout Rules,” on page 96.
- For M2, M3 and M4, see Rules 602, 604, 604b, 604c, 604d in contrast to Rules 604e and 604f in Table 3-10, “Mx ($x=2,3,4$) Metal and Via Layout Rules,” on page 103.
- For MQ, see Rules 692, 694, 694b and 694c in contrast to Rules 694e and 694f in Table 3-12, “MQ (Thick Metal) Layout Rules,” on page 109.

I.4.4 Layout identification of Mx wires $> 50\mu\text{m}$

Use of MxPLANE Dummy Design and Utility Level is needed to allow Mx wire widths $> 50\mu\text{m}$ in the BiCMOS8HP technology.

As stated in section I.1 , “Introduction” on page 434, Mx wires $> 50\mu\text{m}$ must be covered by its corresponding MxPLANE Dummy Design and Utility Level ($x=1,2,3,4,Q$). See MxPLANE in Table 2-4, “Dummy Design Levels and Utility Levels,” on page 36 ($x=1,2,3,4,Q$). See also Rules 500b, 500c, and 500e in Table 3-9, “CA, M1 Metal and Via Layout Rules,” on page 96 and Rules 600b, 600c, 600e in Table 3-10, “Mx ($x=2,3,4$) Metal and Via Layout Rules,” on page 103, and Rules 690b, 690c and 690e in Table 3-12, “MQ (Thick Metal) Layout Rules,” on page 109.

I.4.5 FEOL device wiring using MxPLANE

Wiring to FEOL devices is not allowed using M1 wire widths $> 50\mu\text{m}$ (i.e., M1 planes). See Rule 505c in Table 3-9, “CA, M1 Metal and Via Layout Rules,” on page 96. Use M1 wires widths $\leq 50\mu\text{m}$ (M1 not covered by M1PLANE) extending from M1 wires widths $> 50\mu\text{m}$ (M1 over M1PLANE) or use M1 $\leq 50\mu\text{m}$ strapped by (V1 or Vx) where ($x = 2,3,L$) vias to (Mx over MxPLANE) where ($x = 2,3,4,Q$) for device interconnection.

I.4.6 BEOL wiring using MxPLANE

I.4.6.1 Notes and Recommendations

1. As stated in section I.4.1.1 , “MxHOLE Size Information” on page 435, auto-generated MxHOLE shapes are different sizes for Mx wire widths $\leq 50\mu\text{m}$ compared to (Mx over MxPLANE) wire widths $> 50\mu\text{m}$. Additionally, autogenerated MxFILL will be automatically suppressed in the transition region between adjacent (Mx) and (Mx over MxPLANE) wires on the same wiring level ($x=1,2,3,4,Q$). The minimum distance that MxFILL will be excluded between adjacent Mx and (Mx over MxPLANE) wires is defined in Table H-1, “xxFILL Rules,” on page 417.

Additionally, MxFILL between adjacent (Mx over MxPLANE) large “planes”, on the same wiring level, will be suppressed. MxFILL will be suppressed near the Dummy Design and Utility Level MxPLANE or completely between the adjacent (Mx over MxPLANE) areas based on the actual space used by the designer, in contrast to the minimum wiring spacing requirements. For more information, see:

- Rule 504e in Table 3-9 on page 96 and Rule DS511a in Table H-1 on page 417 (for M1).
- Rule 604e in Table 3-10 on page 103 and Rule DS511a in Table H-1 on page 417 (for M2, M3, M4).
- Rule 694e in Table 3-12 on page 109 and Rule DS511a in Table H-1 on page 417 (for MT).

Algorithm development for placement of autogenerated MxFILL between adjacent (Mx over MxPLANE) large planes, on the same wiring level, is under development.

Rule DS511a is not checked in DRC. This rule is used internal to IBM during the release process.

2. Maximum (Mx over MxPLANE) width that IBM has evaluated is specified in:

- Recommended Rule: 500dR in Table 3-9 on page 96 (for M1)
- Recommended Rule: 600dR in Table 3-10 on page 103 (for M2, M3, M4)
- Recommended Rule: 640dR in Table 3-12 on page 109 (for MQ)

At this time, IBM is not restricting the maximum width of (Mx over MxPLANE) on each BEOL metal level (x=1,2,3,4,Q). However, it is NOT recommended to use (Mx over MxPLANE) excessively across a chip design. If (Mx over MxPLANE) is used excessively, it is recommended that Designers conservatively use the effective linewidth results for (Mx over MxPLANE) defined in Section Table 4-32., “Effective Linewidth for Wires with HOLE Shapes” on page 286 for all Mx wire widths, on the BEOL levels where large “planes” exist within the chip design, including those Mx wires widths that are $\leq 50\mu\text{m}$.

3. Pass through cutouts are allowed within “planes”, meaning that (Mx over MxPLANE) can be in the form of a donut, or enclose or surround a smaller Mx wires or active circuit area (x=1,2,3,4,Q).

- Rule 501cR in Table 3-9 on page 96 as well as Rules 601cR and 691cR are provided as an IBM guideline for pass-through layout. Use of this feature description helps to identify such structures. However, at this time, IBM is not enforcing the use of this structure from a technology perspective, so the rules are identified as “Recommended”.
- Wire widths $\leq 50\mu\text{m}$ that are enclosed within a “plane” or wire widths $\leq 50\mu\text{m}$ outside or adjacent to a “plane” must be spaced per Rules 504e, 504f, 604e, 604f, 694e, and 694f (for more information, see section I.4.3 , “Layout spacing of (Mx) versus (Mx over MxPLANE) wires” on page 436).

4. MxPLANE can not be used in the chip guard ring. See Rules 505c, 505dR in Table 3-9 on page 96 as well as Rule 605d in Table 3-10 on page 103 and 695d in Table 3-12 on page 109.

5. IBM requires (Vx or VL or VY) vias to be further within the outer edges of (Mx over MxPLANE) than the Design Minimum values used for (Mx not over MxPLANE) ((x=1,2,3,4, Q).

6. Use of “planes” (Mx over MxPLANE) is strongly encouraged in contrast to layout design using either:

- a. criss-crossing Mx wires using widths $\leq 50\mu\text{m}$.
- b. Mx wires having widths $\leq 50\mu\text{m}$ with sparsely distributed cutouts or slots in the metal to produce a large continuous Mx conductive area.
- c. Large Mx copper wiring areas ((Mx not over MxPLANE) widths approaching $50\mu\text{m}$) where Mx local pattern densities exceed 80 percent.

Use of (Mx over MxPLANE) should result in improved manufactureability as well as efficiency of IBM's data preparation algorithms used during the release process prior to mask build.

7. All global pattern density considerations defined in Section 2.10.1 , “Global Pattern Density” on page 62 or additional layout rules or local pattern density aspects defined in Section 2.10.2 , “Local Pattern Density” on page 64 must be met when using “planes” (Mx over MxPLANE, x=1,2,3,4,Q).
 - Use of MxPLANE over MxCHEXCL is not allowed (x=1,2,3,4,Q).
8. MxPLANE should not be drawn across all Mx wires on a single metal level since it may result in layout rule errors (see Rule 500e in Table 3-9 on page 96 as well as Rule 600e in Table 3-10 on page 103 and Rule 694e in Table 3-12 on page 109).
9. Do not use (Mx over MxPLANE) to replace IBM generated MxFILL (x = 1,2,3,4,Q) in the BEOL. Large copper planes (Mx over MxPLANE) was intended for use for electrically active wiring purposes.
10. Use of MQPLANE is not recommended, especially if KQ resistors are included in the chip design. However, use of (MQ over MQPLANE) with KQ resistors is allowed within the same chip design, but is not preferred.
11. Use of consecutive BEOL MxPLANE levels of (i.e., (Mx over MxPLANE) and (M(x+1) over M(x+1)PLANE)) is NOT recommended (where x=1,2,3,4 or Q). Use of M(x+2) MxPLANE separation is preferred for improved manufactureability.

Examples:

- For a 7LM (i.e., M1, M2, M3, M4, MQ LY, AM) chip design, use of (M2 over M2PLANE) and (M3 over M3PLANE) may result in reduced manufactureability compared to using (M2 over M2PLANE) with (M4 over M4PLANE).
12. Do not use MxPLANE below INDUCTORS or Wirebond pads, see Rule MXPL2 in Table 3-17 on page 117
 13. Using (M1 over M1PLANE) is not recommended.

Index

A

AM Layout Rules 116
Antenna Rules 78
AV and AVBAR Layout Rules 115

B

base feature devices 9
BB Layout Rules 128
bend junction 316
BFMOAT 294
BFMOAT Layout Rules 169
Bipolar Transistor 244
BONDPAD Layout Rules 193
Bondpad Models 302
BP Layout Rules 90
branch couplers 321
Butted Junction Layout Rules 94

C

C4 Layout Rules 196
C4 Terminals 194
Capacitor Models 275
CEBAR Layout Rules 120
Chamfer 203
Check List 18
Chip Guard Ring 203
Chip Guard Ring Layout Rules 205
Chip Size, Maximum 218
CHIPEDGE 37
Complex Optical Manipulations (OPC, SLB) 416
Conducting Film Thickness 282
Contact Layout Rules 80
Contact Resistance 283
coplanar waveguide 303
Copyright Notice 215
Crackstop 213
Cross Section 21
Current Limits 362
CX Layout Rules 124

D

Definitions of Ground Rule Terms 411
Design for Manufactureability 395
Design Guidelines 59
Design Level 25
Design Preparation 44
Device Models 243
DG Layout Rules 170

DI Layout Rules 155
Diodes 260
Distributed Passive Devices 313
DS Layout Rules 132
Dummy C4 Terminals 198
Dummy Design Levels 36
DV Layout Rules 109
Dynamic circuits 59

E

e-fuse specifications 180
Electrical Fuse 180
Electromigration 358
EM Rule Adjustments 364
ESD 369
ESD Layout Rules 142
ESDIODE Layout Rules 153
EX Layout Rules 119
External Latchup 240
Extraction Parameters 291

F

Feature Part Number 12
FET 247
Fill Rules 417
Film Thickness 284
Final Passivation 290
Forward-Biased Diode 154
Forward-Biased Diodes 263
Fuse Design 180

G

gap discontinuity 319
Gate oxide 248
Gate Oxide Dielectric Integrity 347
Generated Levels 43
Geometry Restrictions 56
Global Pattern Density 62
Grid 25
Guard Ring 203
Guard Ring Layout 225

H

HA Varactor 275
HA Varactor Layout Rules 185
HOLE Rules 422
Hot Carrier 334

I

Inductor Layout Rules 189
Inductor Models 297
Isolation Layout Rules 69

J

JD Layout Rules 185
Junction Layout Rules 83

K

KQ Layout Rules 167
KQ Resistor 166

L

Labels 213
Lange coupler 322
Latchup 221
Latchup Rules 232
Layout Rules 69
LE Layout Rules 119
Local Pattern Density 64
LOGOBNL Layout Rules 214
LV Layout Rules 109
LY Layout Rules 113

M

M1 Layout Rules 96
Mask Level 25
Mask Level Identification 216
Maskwork Notice 215
meander-line device 320
Metal Layout Rules 96
Metallization Options 49
MIM Capacitor 276, 277
MIM Dielectric Integrity 357
MIM Layout Rules 186
Mixed Voltage Interfaces 325
Models 243
MQ Layout Rules 109
Multiple DUT 201
Mx Metal Layout Rules 103
MxPLANE 434
MxPLANE Layout Rules 117

N

NBTI 349
nFET-in-Nwell Layout Rules 173
Non-Design Levels 43
NP Layout Rules 121
NPN Forward Bias Degradation 356
NPN, High Breakdown 245
NPN, High Performance 245
NS Layout Rules 130
NS Resistor Layout Rules 163
Nwell Layout Rules 83

O

OP Layout Rules 158

open stub 318
Optimal Model-Hardware Correlation 407
optional devices 10
Ordering Information 11
Origin 61

P

Packaging Restrictions 200
Pad Identification 147
Passive 313
Pattern Density Rules 62, 425
PCI 139
PCING Layout Rules 139
PD Layout Rules 163
PI Layout Rules 175
Polysilicon Layout Rules 69
power dividers 321
Process-Related Terms 414
Product Labels 213
Protect Layer 208
Proximity Effect 253
PX Layout Rules 126

Q

QY Layout Rules 187

R

radial stub 318
Rat Race Hybrid 322
Recommended rules 61
Regular FET 256
Regular IO FET 259
Reliability 331
 Bipolar 356
 Resistor 353
Reliability (BEOL) 358
Reliability (FEOL) 334
Reliability Limitations 332
Reliability Screening 326, 332
Resistance
 Sheet 284
Resistor Models 265
Restricted Level 30
Reverse Voltage 326
RF Interconnect 192
Rflin Models 299
RN Layout Rules 125
RR Layout Rules 164

S

Sheet Resistance 284
short stub 318

Size, Allowable Chip 218

Slots in Wide Metal 202

Specifications

 Resistor 265

step junction 317

supported devices 10

T

taper device 319

Technology Features 9

Technology Introduction 9

tee junction 316

temperature range 11

Terminal, C4 and Wirebonds 193

Threshold Voltage Rules 89

Threshold Voltage Stability 348

Total Standby Current (I_{dd}) 408

Transmission Line 191

Transmission Line Models 303

Triple Well NFET 258

Triple Well NFET Layout Rules 175

Truth Table 49, 52, 54, 55, 56

U

Utility Levels 36

V

VAR Layout Rules 173

Via Layout Rules 96

Via Resistance 283

VL Via Layout Rules 103

V_{max}

 Gate Dielectric (2.2nm) 326

 Gate Dielectric (5.2nm) 329

V_{max} for MIM 329

voltage range 11

VY and VYBAR Layout Rules 112

W

Wirebond Layout Rules 199

Wiring capacitance 287

Wiring Resistance 282

Y

y-junction 317

END OF DOCUMENT