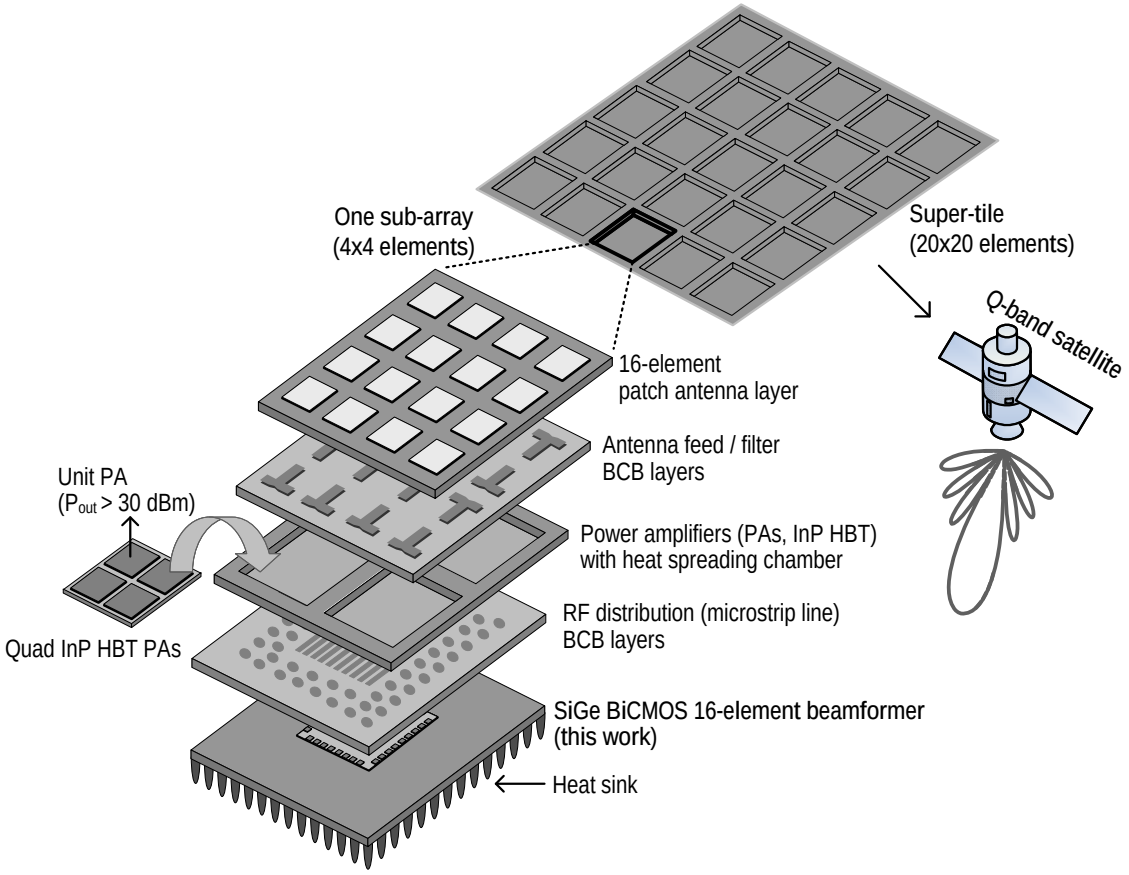


Fig. 1. A tile-based array architecture. One super-tile is composed of 5×5 tiles (sub-arrays) and each tile contains 16 elements (4×4). Multi-layer integration allows the optimization of each layer in terms of thermal, mechanical and electrical performances.

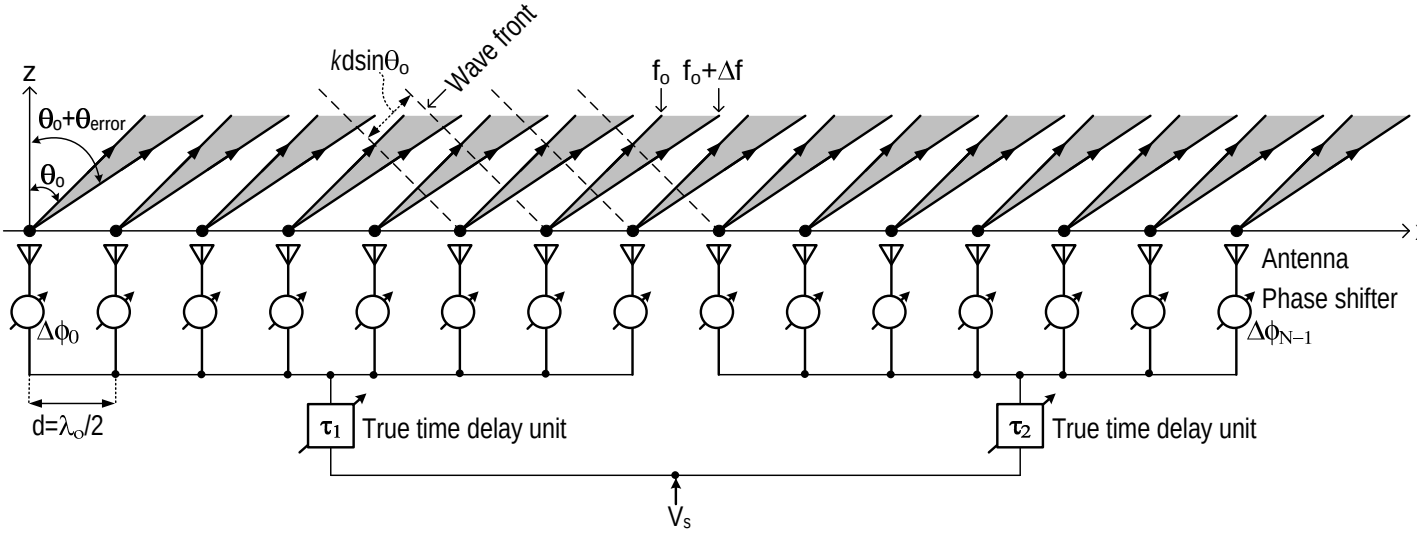


Fig. 2. 16-element phased-array with a combination of phase shifters at the element level and true time delay (TTD) units at the sub-array level for wideband operation (N=16).

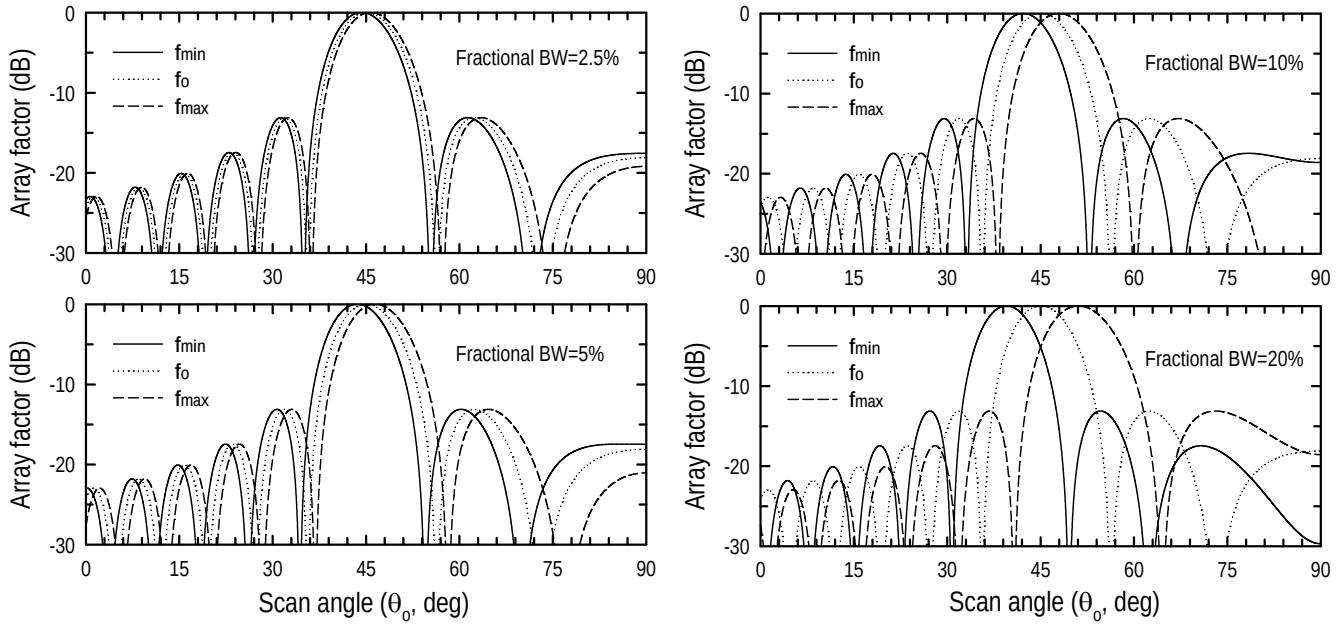


Fig. 3. Array factors for a 16-element linear phased-array for different fractional bandwidths (scan angle=45^{o}).

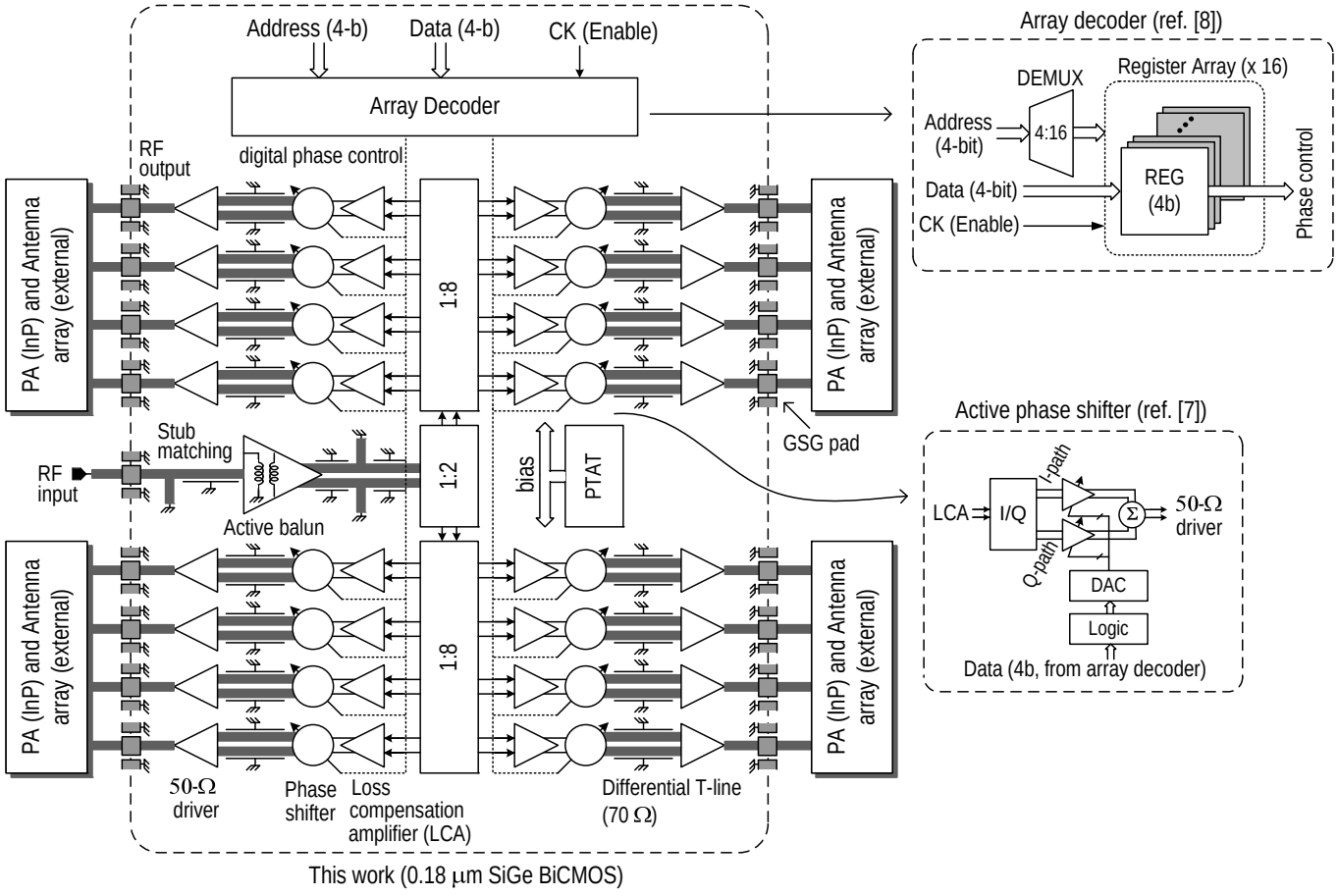


Fig. 4. The functional block of the 16-element phased-array beamformer in 0.18-μm SiGe BiCMOS technology.

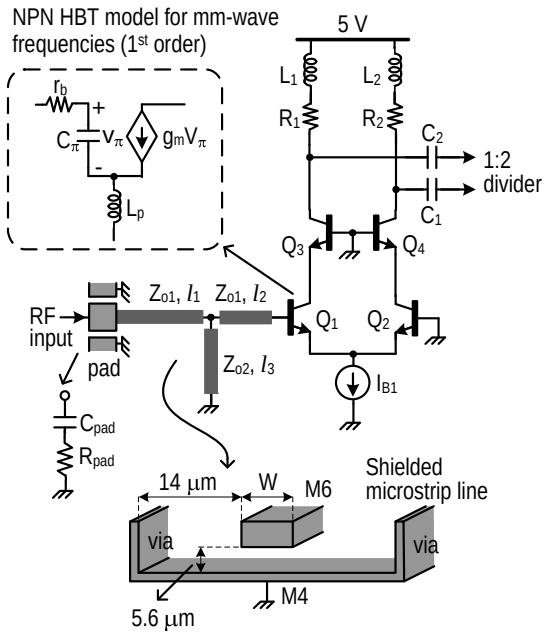


Fig. 5. The active balun amplifier, microstrip line structure (not to scale) and small signal NPN HBT model which includes an inductance, L_p, to account for parasitic layout inductance for this work.

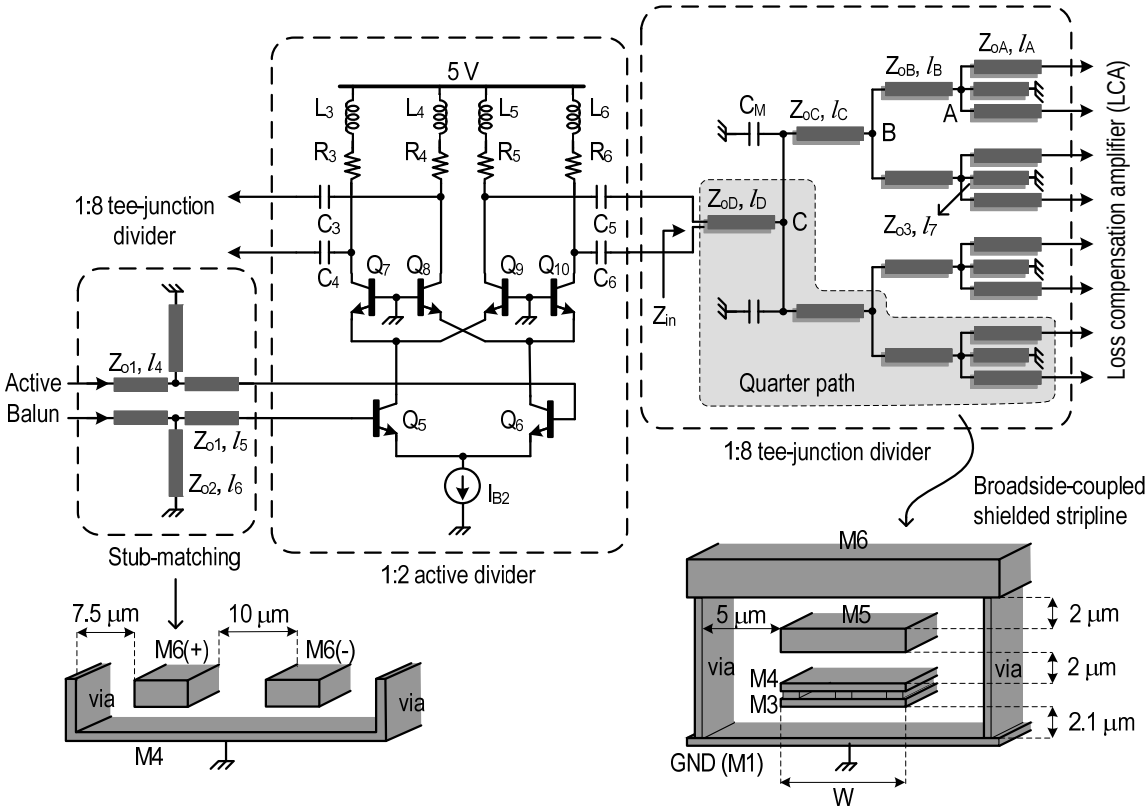


Fig. 6. The 1:2 active divider, differential microstrip line structure (not to scale), 1:8 passive tee-junction dividers (only one is shown) and broadside-coupled stripline structure (scaled, M5 thickness: 1.6 μm, thickness of M4 and M3 with vias: 1.9 μm).

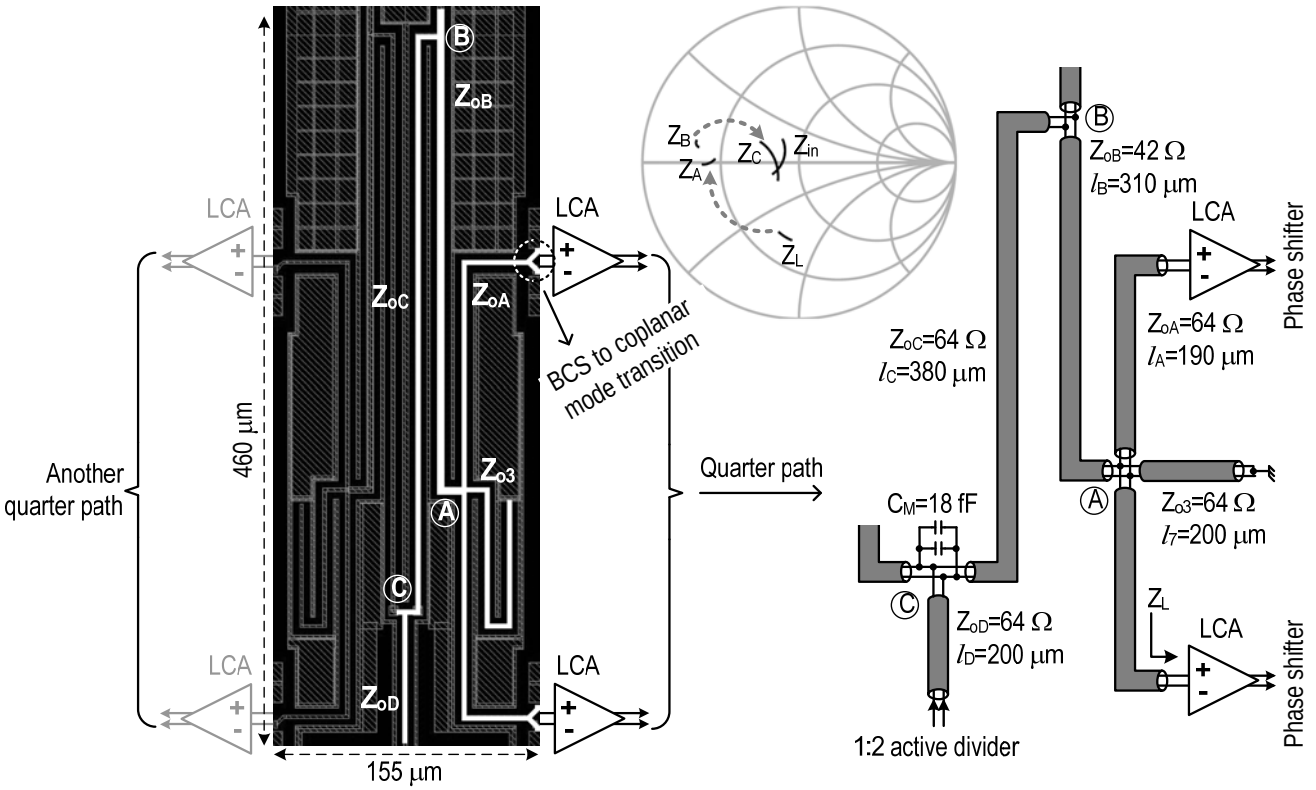


Fig. 7. The layout of the quarter path shown in Fig. 6 and its detailed description (all impedances are odd-mode impedances). The frequency range of the impedances in the Smith chart (Z_o=100 Ω) is 40-50 GHz.

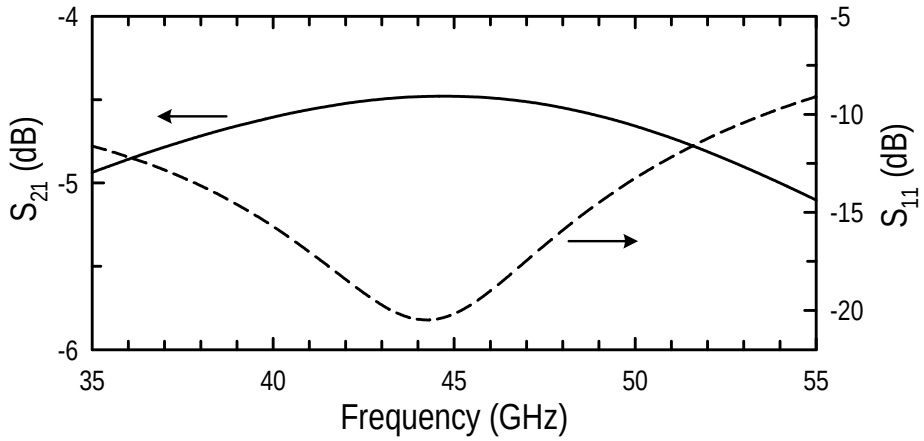


Fig. 8. The simulated S_{21} and input reflection coefficient (S_{11}) of the passive 1:8 tee-junction divider. Input port impedance=100 Ω and output load impedance=55-*j*65 Ω at 45 GHz. The S_{21} does not include the 9 dB 1:8 splitter loss. (Port-1: input port, Port-2: one of the 8 output ports).

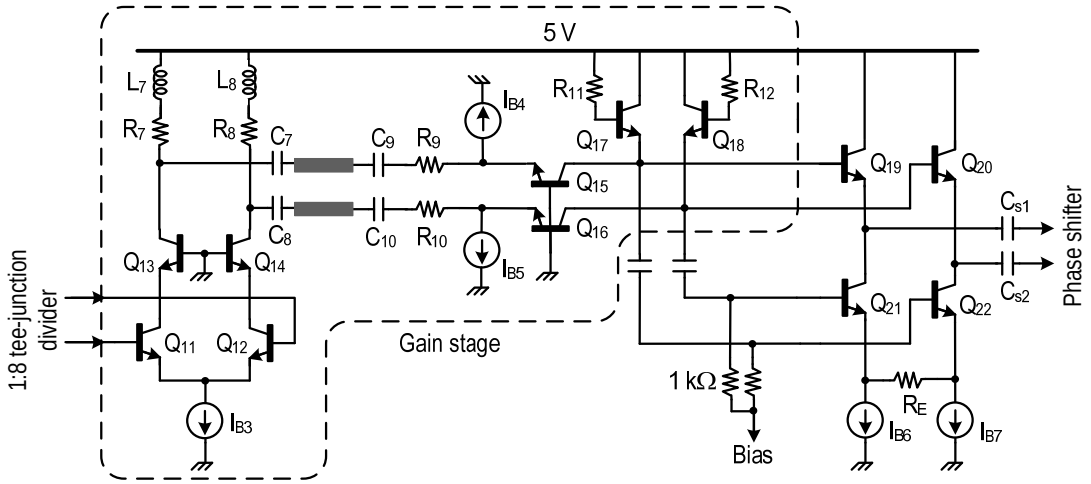


Fig. 9. The loss compensation amplifier (LCA) composed of gain stage (common emitter and common base stage) and an output low-impedance driver for the following phase shifter.

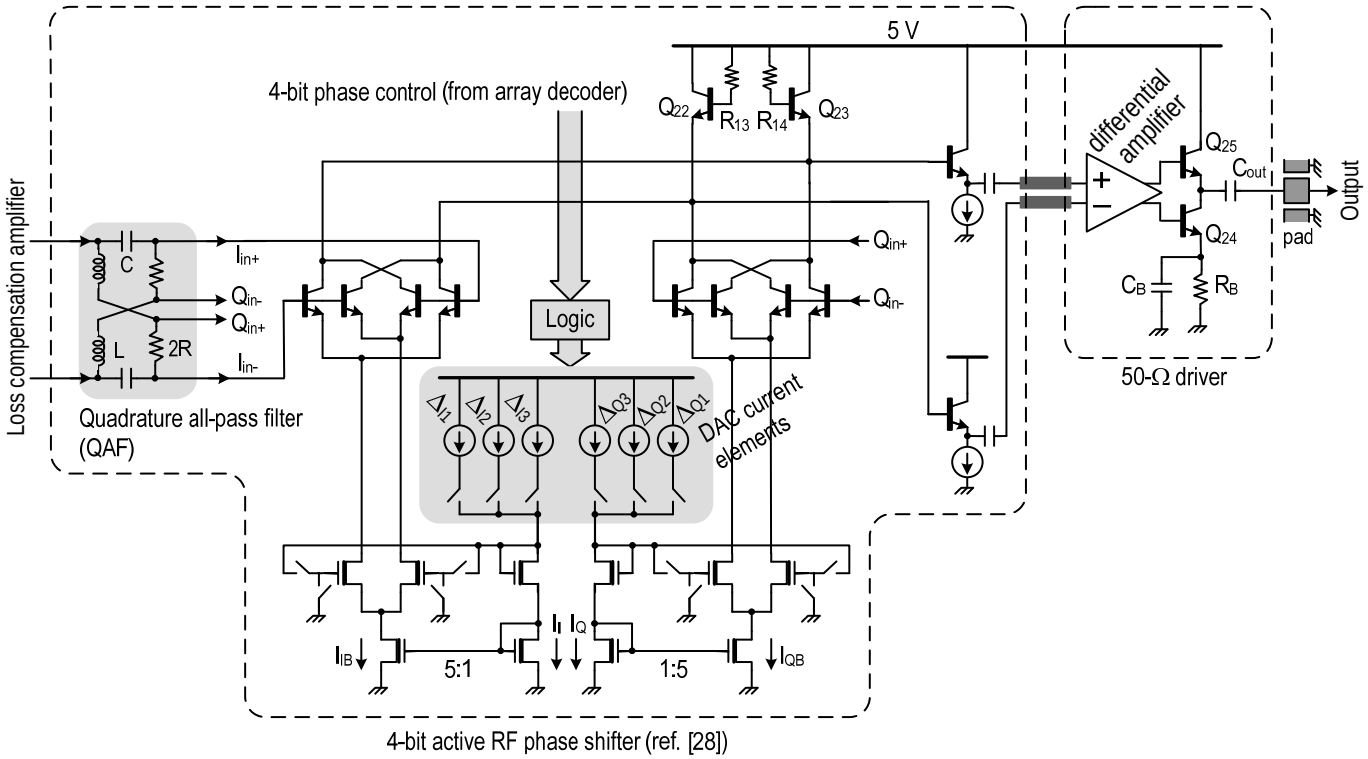


Fig. 10. The active 4-bit RF phase shifter and 50-Ω output driver.

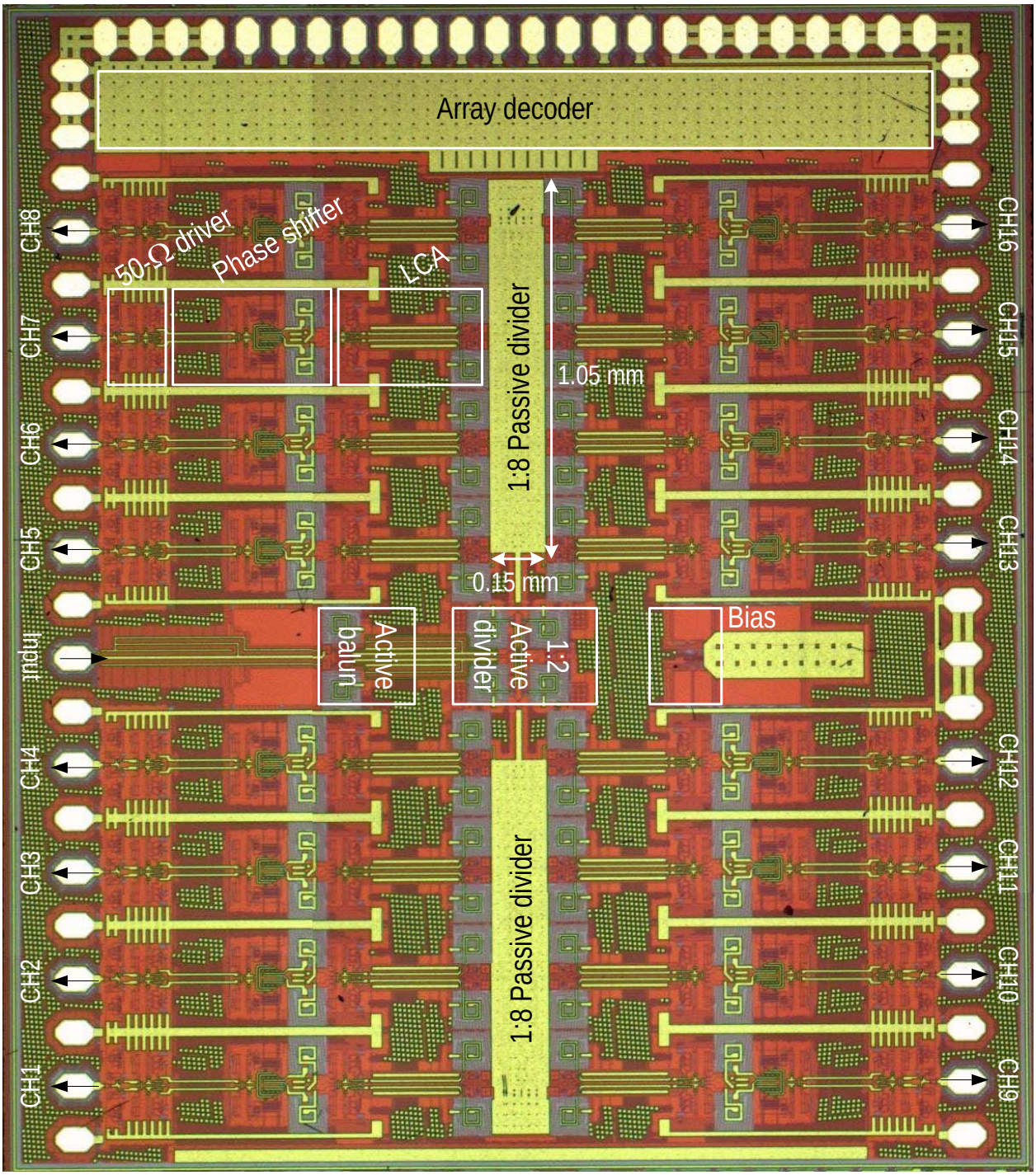


Fig. 11. Chip photograph of the 16-element Q-band phased-array transmitter (area=2.6×3.2 mm^2).

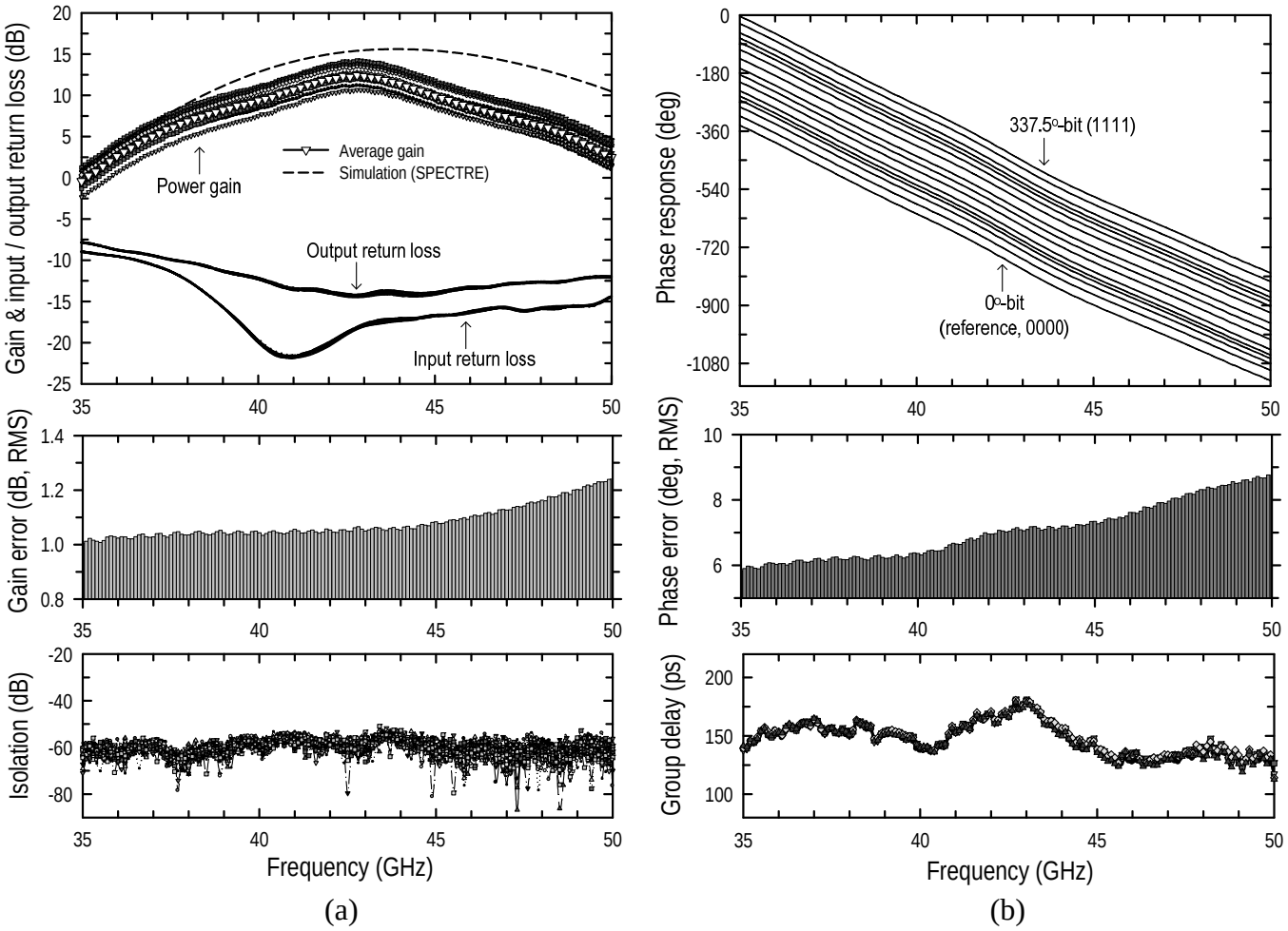


Fig. 12. The measured single channel (*Channel-1*) characteristics: (a) input and output matching, power gain, RMS gain error and output-to-input isolation characteristics for all 4-bit phase states. (b) 4-bit phase responses, RMS phase error (from ideal 4-bit phases) and averaged group delays for 0^o, 22.5^o, 45^o, 67.5^o and 90^o-bit phase states.

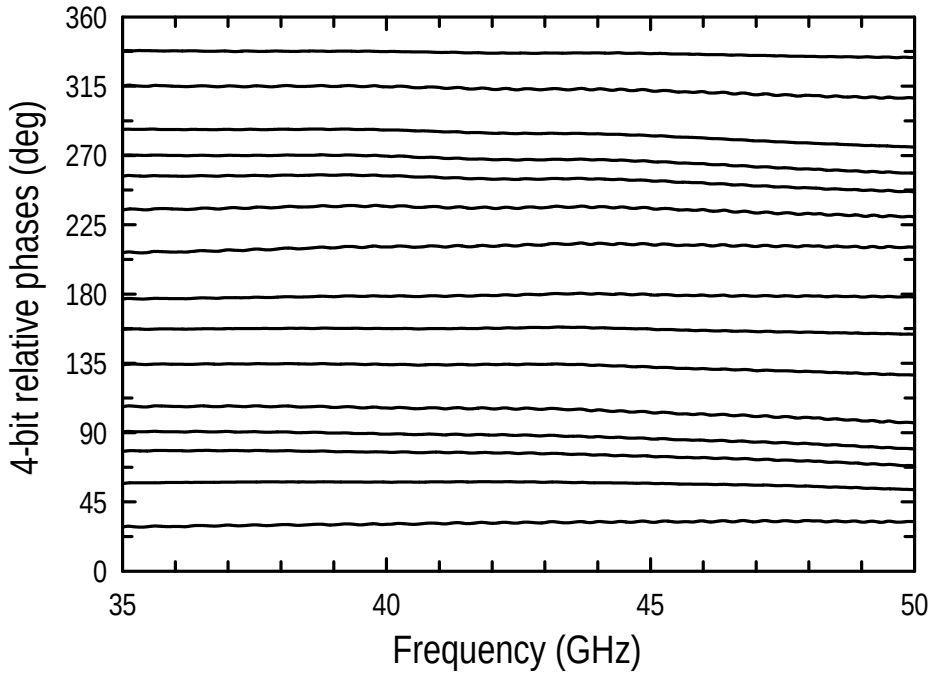


Fig. 13. The measured 4-bit relative phase states (reference: 0^{o}-bit phase state in Fig. 12(b)).

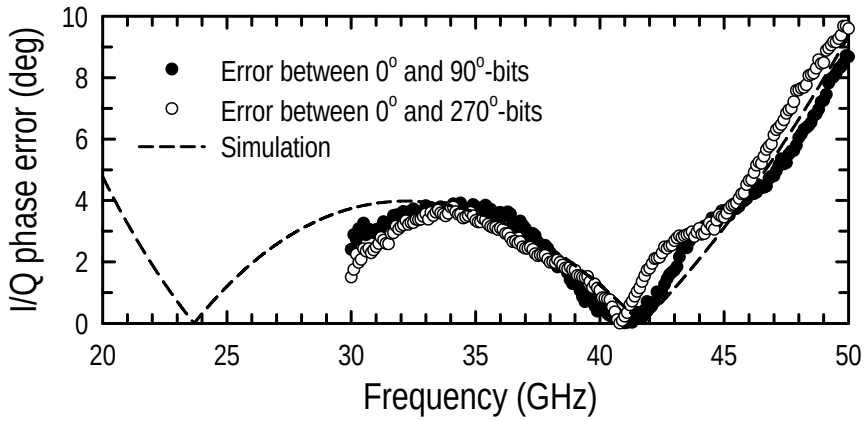


Fig. 14. The measured I/Q phase imbalance in the QAF.

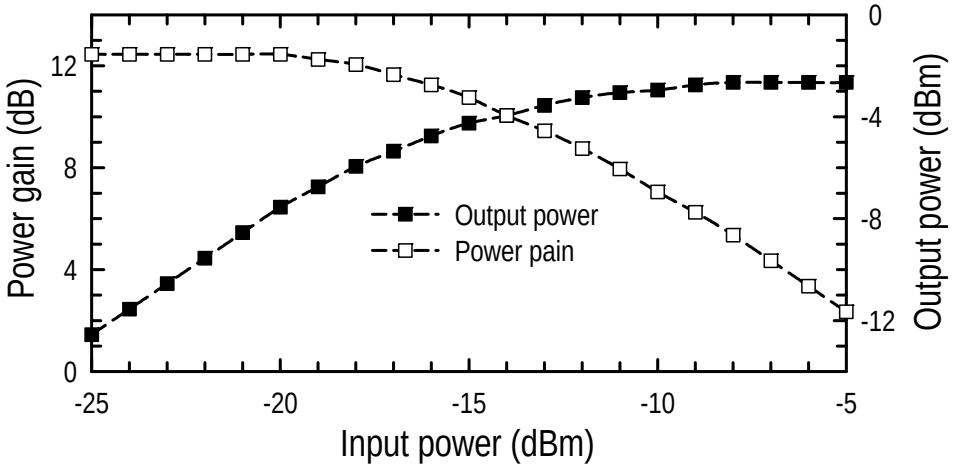


Fig. 15. The measured nominal power gain and output power per channel at 42.5 GHz versus RF input power.

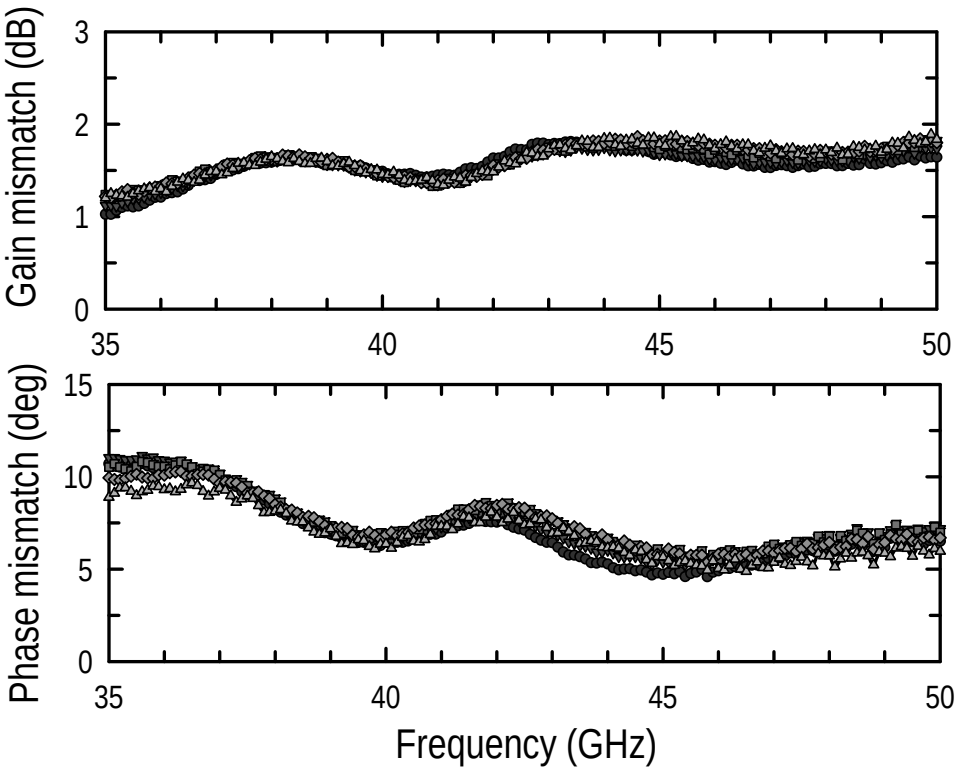


Fig. 16. The measured channel-to-channel RMS gain and phase mismatches between the 16 channels for 5 different phase states (0^o, 22.5^o, 45^o, 67.5^o and 90^o-bit phase states).

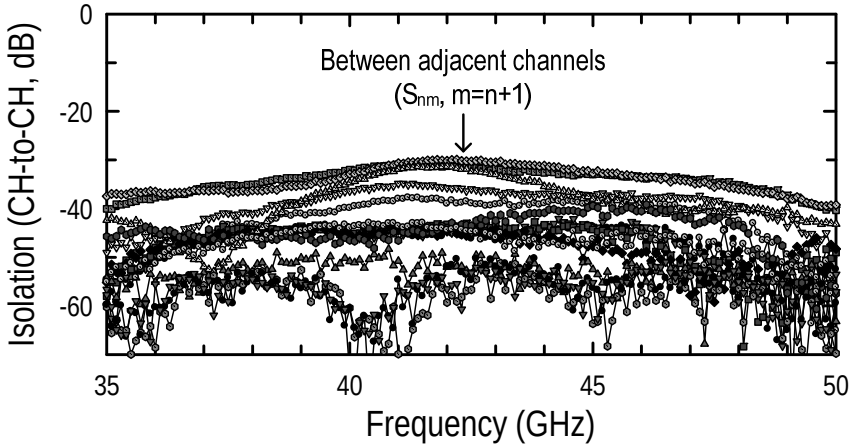
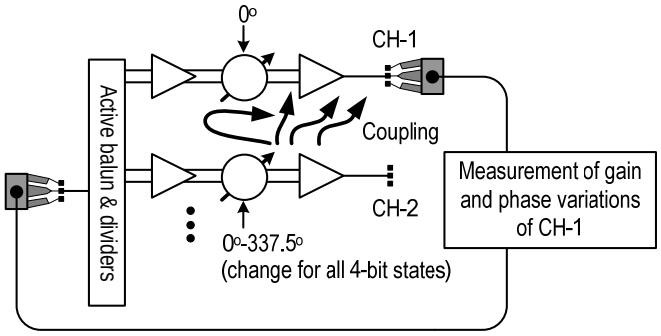
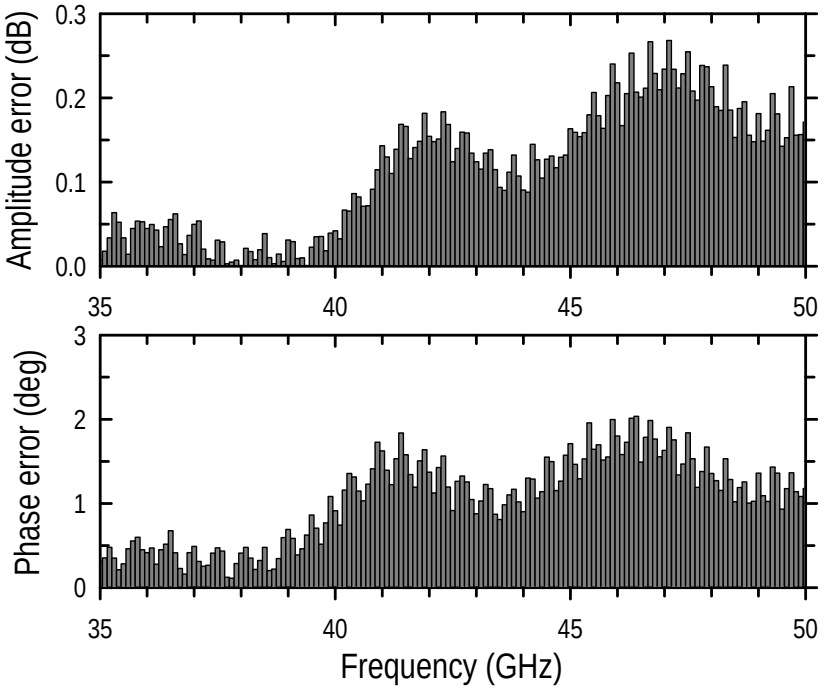


Fig. 17. The measured isolation between channel to channel. The worst case occurs between adjacent channels (n=1-15).

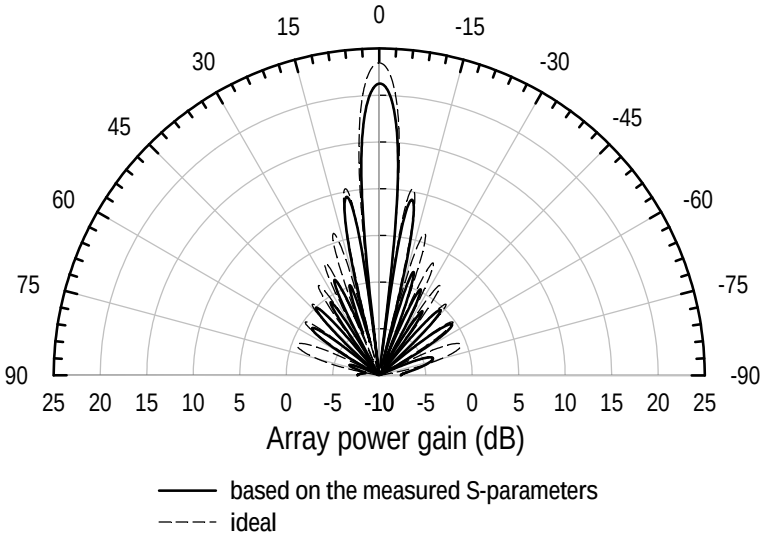


(a)

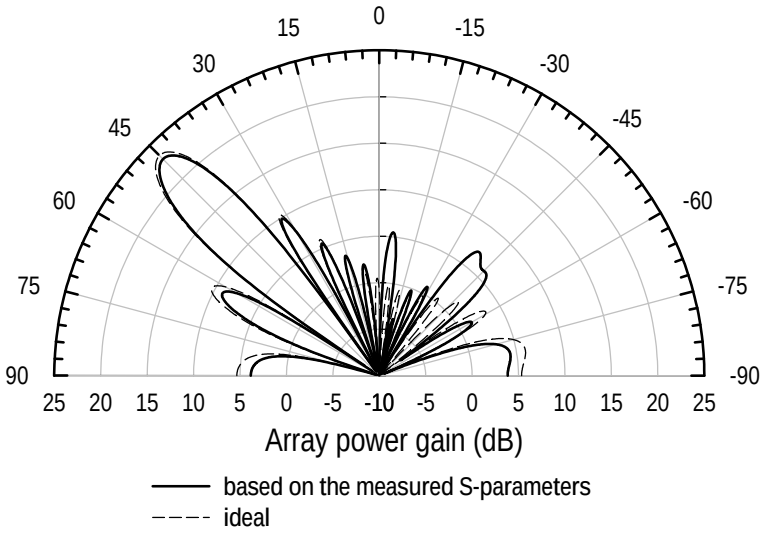


(b)

Fig. 18. Coupling characterization: (a) coupling test setup, (b) the measured output signal errors (amplitude error and phase error).



(a)



(b)

Fig. 19. Array beam scanning characteristics: (a) broadside scan, (b) 45^{o} scan angle at 44 GHz.

TABLE I. SUMMARY OF THE BEAMFORMER PERFORMANCE

Technology	0.18μm SiGe BiCMOS (Jazz SiGe120, 1P6M)
Frequency band	Q-Band (40-45 GHz)
Supply voltage	5 V (analog), 3.3 V (digital)
Current consumption	720 mA
Chip area	2.6x3.2 mm^2
Single Path Characteristics	
Input return loss	$\leq$ -10 dB @ 36.6-50 GHz
Output return loss	$\leq$ -10 dB @ 37.6-50 GHz
Channel power gain (*ave*)	12.5 dB @ 42.5 GHz (3-dB BW: 40-45 GHz)
Phase resolution	4-bit
Gain variation (for 4-bit phase states)	< 1.3 dB (RMS) @ 35-50 GHz
Phase error (for 4-bit phase states)	< 8.8° (RMS) @ 35-50 GHz
Output P_{1dB}	-5±1.5 dBm @ 42.5 GHz
Maximum output power (P_{sat})	-2.5±1.5 dBm @ 42.5 GHz
Isolation (output-to-input)	$\leq$ -55 dB @ 35-50 GHz
Array Characteristics	
Phase mismatch (RMS)	$\leq$ 7° @ 40-50 GHz (between all channels)
Amplitude mismatch (RMS)	$\leq$ 1.8 dB @ 40-50 GHz (between all channels)
Isolation (channel-to-channel)	$\leq$ -30 dB @ 35-50 GHz
Array factor directivity	12 dB (16 elements)