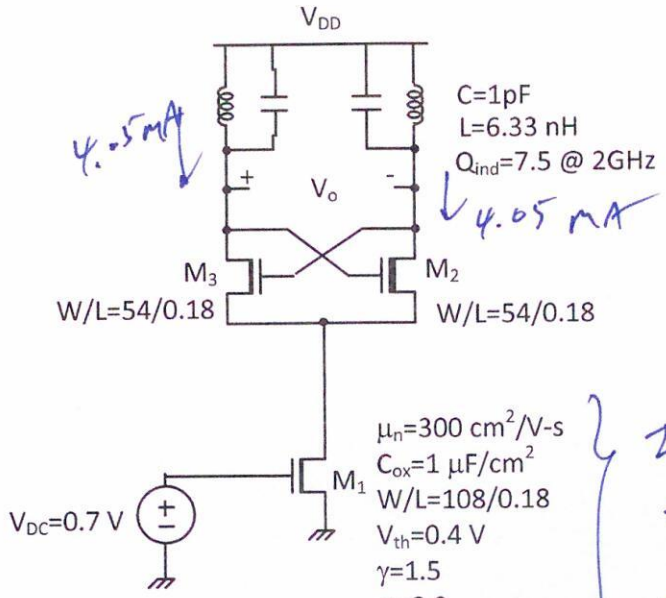
2. In the VCO shown below, DC characteristic of the NMOS, M1-3, is set by square-law characteristic,

$$I_{DS} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2.$$

Assume that Cgs of M2-3 is negligible compared with C in the LC-tank. For simplicity, let's further assume that dominant noise sources are M1 and parasitic resistance from LC-tank, and noises from M2-3 are negligible. M1 has only drain thermal noise current, i.e., no gate induced noise and parasitic gate resistance.



4.05 mA

4.05 mA

$Q_{ind} = 7.5$

$\Rightarrow R_{ind} = Q_{ind} \cdot W_{osc} \cdot L$

$= 7.5 \times 2\pi \cdot 2G \cdot 6.33nH$

$= 596.59\ \Omega$

$I_{DC} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{th})^2$

$= \frac{1}{2} \cdot 300 \times 1\mu \times \frac{1.8}{0.18} \times 0.3^2$

$= 8.1\,mA$

$\Rightarrow g_{m1} = \mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{th})$

$= 54\,m\Omega$

1) Calculate the possible maximum output signal swing in peak-to-peak value and set minimum supply voltage VDD that allows the maximum output swing (5 pt).
(Note: Each NMOS needs at least minimum $V_{ds,sat}$ during full output swing excursion to sustain oscillation.)

$(V_{ds,sat})_{M1} = V_{GS} - V_{th} = 0.7 - 0.4 = 0.3\,V$

because stage of M_2, M_3 is half of M_1.

$(V_{ds,sat})_{M2,M3}$ @ $I_{DS} = 8.1\,mA = (V_{ds,sat})_{M1} \times \sqrt{2}$

$= 0.424\,V$

$\frac{1}{2} I_{DC} \times R_{ind} \times \frac{2}{\pi} = \frac{1}{2} \times 8.1m \times 596.59\Omega \times \frac{2}{\pi}$

$V_{DD,min} = 1.538\,V$

$(V_{ds,sat})_{M1} + (V_{ds,sat})_{M2,M3} = 0.724\,V$

$\therefore V_{DD,min} = 1.538 + 0.724 = 2.262\,V$