methan and hydrogen was used. Secondly, the cleaning step is the result of several contamination investigations. For a clear insight into the efficiency of our cleaning procedure, atomic force microscope (AFM) measurements were performed just after epitaxy (Fig. 2). A comparison with AFM measurements obtained on the same wafer when processed as described above is reported in Fig. 3. Note that the surface morphology before and after technology is the same on a nanometer depth scale and reveals the terraces formed on epitaxial materials. Moreover, X-ray photoelecton spectroscopy (XPS) and secondary ion mass spectroscopy (SIMS) measurements confirmed these results and have shown that oxygen and carbon contamination were very low, being reduced to the dose corresponding to natural contamination.

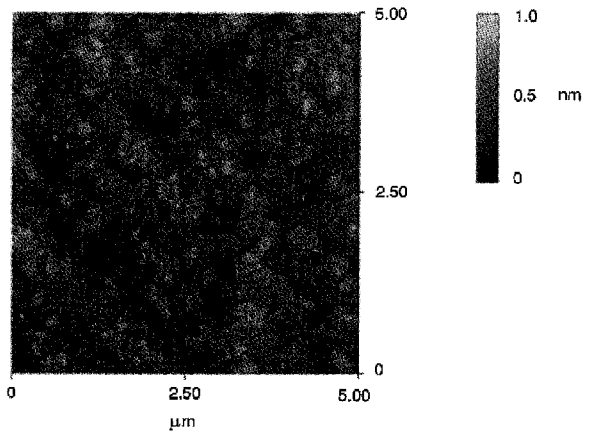

Fig. 3 *AFM picture of surface at end of process (etching and cleaning)*

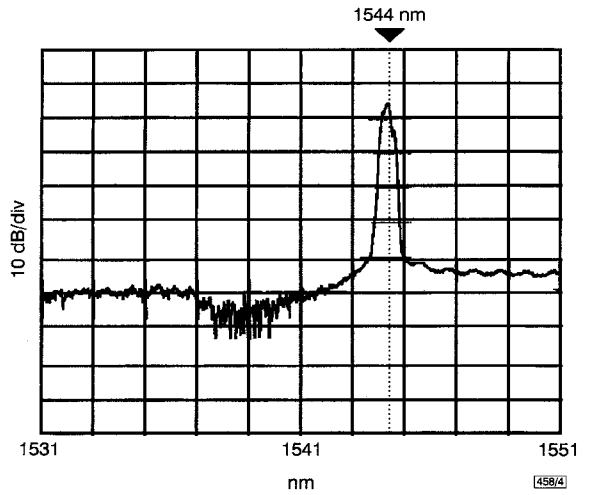

Fig. 4 *Measured emission spectra on broad area laser (300µm × 100µm)*

Results: The measured broad area lasers have shown threshold current densities in the range 700–800A/cm^2 which is, to our knowledge, the best value reported to date. In [5], low thresholds are also reported, although the threshold current density is unknown. However, the gain grating was realised using wet etching, while in our case, RIE was used to gain a better control of the grating etching. From this point of view, the results presented are very promising with regard to reproducibility and homogeneity for industrial applications. The calculated T_0 value is ~52K, which compares favourably to the value obtained for the same vertical structure on index-coupled DFB lasers (≃ 42K). The external quantum efficiency was measured to be 0.27W/A, even though the measured index coupling from the Bragg stop-band is in the range of 300cm^{-1}.

We also measured the emission spectra under a pulsed excitation current (Fig. 4). As predicted by theory, the oscillation occurs on the long wavelength side of the Bragg stop-band, which is indeed the case for in-phase gain-gratings.

Conclusion: We have realised very low threshold current density gain-coupled DFB lasers; they are the result of an efficient technology for gain grating formation based on AFM, XPS and SIMS measurements.

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N. Aberkane, B. Thedrez, J.L. Gentner, A. Pinquier, V. Voiriot, L. Le Gouezigou and B. Fernier (*Alcatel Alsthom Recherche, Route de Nozay, 91460 Marcoussis, France*)

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Design of lumped element quadrature hybrid

Y.C. Chiang and C.Y. Chen

At the lower microwave frequency range, distributed element hybrids consume too great a circuit area. To reduce the surface area without degrading electrical performance, a lumped element hybrid can be used. A new lumped hybrid design method is presented which uses a combination of T-networks and π-networks to achieve an improved magnitude balance. A prototype of the lumped element hybrid is fabricated by using the conventional microwave integrated circuit technique to verify the design concept. The measurement results show good agreement with the theoretical prediction. This quadrature hybrid structure is compact and applicable to monolithic microwave integrated circuit realisation.

Introduction: Quadrature hybrids are widely used in the design of balanced amplifiers and mixers for achieving good input, and output matching and power combining, as well as isolation between ports. The most commonly used quadrature hybrids are the branch line and the Lange coupler, which consist of four or several coupled λ/4 transmission lines [1, 2]. When the operating frequency is < 3GHz, the length of a quarter wavelength transmission line on a 25 mil alumina substrate is > 10mm. So, the distributed quadrature hybrids consume too much circuit area to be realised on a monolithic microwave integrated circuit (MMIC) or microwave integrated circuit (MIC) chip. The conventional distributed rat-racing balun, which consists of three λ/4 transmission line sections and one 3λ/4 transmission line section, is also unsuitable for MMIC or MIC realisation. For constructing the rat-racing balun on a single MMIC substrate, a lumped balun design technique has been proposed by Parisi. This lumped balun cannot only be realised on a single substrate within a smaller chip area, but also has a wider operation bandwidth than can be obtained using the distributed approach [3]. The lumped balun is then used in the design of a ·2.4GHz MMIC balanced mixer and demonstrates a fractional bandwidth of > 66% [4]. Following Parisi's method to construct a lumped branch-line hybrid, we sequentially connect four sections of the π-network to simulate two transmission line sections with a characteristic impedance of Z_0, the others having a characteristic impedance of $Z_0/\sqrt{2}$. However, we found

that although Parisi's approach to designing the branch-line hybrid gives a small size, the operation bandwidth is still the same as that of the distributed hybrid. In this Letter, we will propose an alternative lumped quadrature hybrid structure, which provides a wider operation bandwidth and still retains a small circuit area.

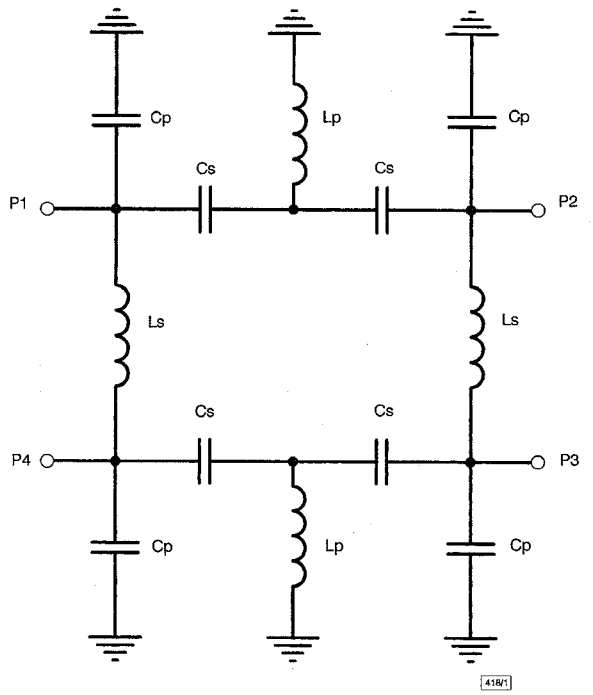

Fig. 1 *Schematic diagram of lumped quadrature hybrid realised by combining lumped element π-network and T-network*

The technique employed to increase bandwidth is to replace two sections of lowpass π-networks in Parisi's approach by the appropriate highpass T-networks. Fig. 1 shows a schematic diagram of the new quadrature hybrid. Owing to the symmetry of the branch-line hybrid, replacing the π-network by the T-network will only change the phase between port 1 and port 2 and port 4 and port 3. However, the phase relationship between port 2 and port 3 still has a 90° phase difference when the signal input is from port 1 and port 4. The simulated S-parameters of the new lumped quadrature hybrid are shown in Fig. 2.

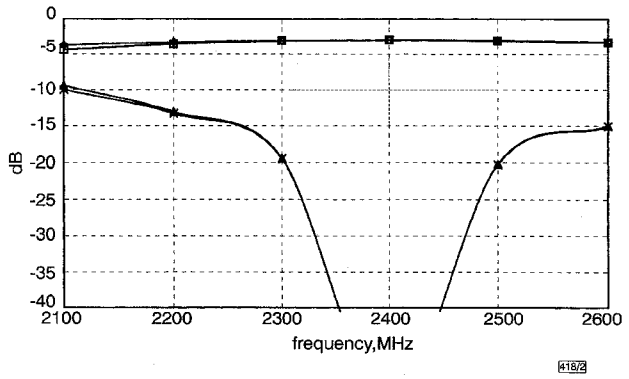

Fig. 2 *Simulated S-parameters of lumped quadrature hybrid*

△ MS11
□ MS21
◇ MS31
× MS41

Design of 2.4GHz lumped quadrature hybrid prototype: To prove the proposed design concept, an MIC lumped quadrature hybrid prototype operated at 2.4GHz was designed and fabricated. The shunt and series lumped elements of the hybrids in Fig. 1 are given by $C_p = 1/(Z_0\omega)$, $L_s = Z_0/\omega$, $L_p = Z_0/\omega\sqrt{2}$, $C_s = \sqrt{2}/(Z_0\omega)$. Fig. 3 shows a photograph of the 2.4GHz quadrature hybrid prototype fabricated on a 25mil alumina substrate. The overall size of the hybrid prototype is ~5mm × 5mm. The meander-line inductors and interdigital capacitors are used to realise the requested lumped elements. The physical dimensions of each inductor and capacitor are determined by systematically analysing the different lumped element feature by using commercial EM software: Sonnet EM. Four large metal plates and the parasitic shunt capacitances of the spiral inductor and interdigital capacitor are used to realise the shunt capacitance of the π-networks. A very narrow metal line is used to connect the interdigital capacitors and the shunt inductor and to minimise the parasitic shunt capacitance which will degrade the requested characteristics of the T-network. The predicted circuit performance is obtained by cascading the simulated S-parameters of individual lumped elements. Owing to the metal loss and dielectric loss of the MIC substrate, $|S_{21}|$ and $|S_{31}|$ are ~1.5dB lower than their ideal values. However, the magnitude difference between port 2 and port 3 is < 0.1dB, the phase difference is kept in the range 90° ± 1° at 2.1 – 2.6GHz.

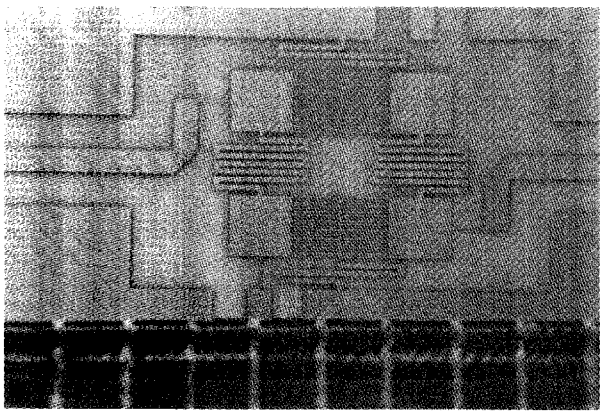

Fig. 3 *Photograph of 2.4GHz lumped hybrid constructed on 25mil alumina substrate*

Measurement of quadrature MIC hybrid: The measurement results of the prototype of the quadrature hybrid are obtained by mounting the prototype circuit on the Arnitsu/Wiltron 3680 MIC test fixture with two extra right-angle adapters. Two of the four ports are terminated by a 50Ω terminator and the S-parameters of the

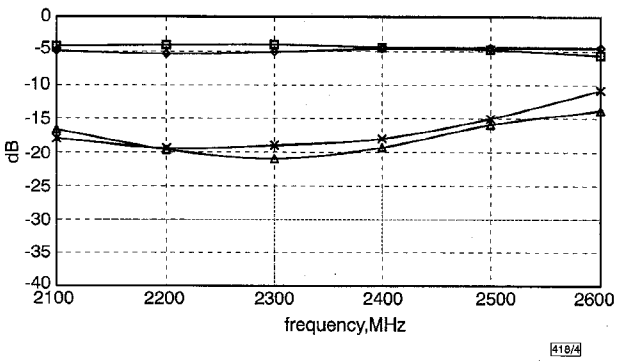

Fig. 4 *Measured S-parameters of lumped hybrid prototype of Fig. 3*

△ MS11
□ MS21
◇ MS31
× MS41

other two ports are measured by connecting the test fixture to an HP8753D network analyser through the coaxial cables. Since calibration of ports in a non-colinear form is difficult to achieve, the calibration is therefore carried out only between the 3.5mm connectors of the coaxial cables. The estimated loss of the adapter due to connection of the circuit and coaxial cables is ~0.3dB. The measurement results are superimposed in Fig. 4. The operational bandwidth shows a very good agreement between measurement and theory. If the effects of the adapter and the transitions between the connectors and the real circuit are excluded from the measurement results, the measurement results would be very close indeed to the theoretical prediction.

Conclusion: A technique for the design of quadrature lumped element hybrids has been described and proven by an MIC prototype circuit. The proposed design approach yields an electrical charac-

teristic which is better than the distributed version, but which uses a much smaller area and provides an inherent DC blocking between input and output ports. This technique is also applicable to the realisation of a quadrature hybrid on an MMIC within a very small circuit area.

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Y.C. Chiang and C.Y. Chen (*Institute of Electrical Engineering, Chang Gung University, 259 Wen-hwa 1st road, Kwei-San, Tao-Yuan, Taiwan, Republic of China*)

E-mail: ycchiang@cguaplo.cgu.edu.tw

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HBT IC process with copper substrate

J. Guthrie, D. Mensa, B. Agarwal, Q. Lee, R. Pullela and M.J.W. Rodwell

The authors have demonstrated a copper/polymer substrate HBT integrated circuit technology which offers a low loss microstrip transmission line environment, continuous back-side ground planes, and enhanced thermal performance.

Parasitic ground lead inductance and large dissipated power densities represent critical obstacles to successful design and packaging of microwave and millimetre-wave integrated circuits. While coplanar waveguide transmission lines offer processing simplicity, the layout and packaging of complex microwave circuits with low ground return inductance are problematic. Layout is simplified by the adoption of microstrip transmission lines, and their continuous ground plane over the wafer back surface eliminates the package-ground parasitic inductance. Critical wafer thinning steps and the handling of fragile thinned wafers are involved in the widely employed through wafer via processes that produce microstrip transmission lines. To maximise bandwidths, HBTs are generally biased at current densities in the order of 10^5 A/cm^2. Large power densities, and the inferior thermal conductivity of compound semiconductor substrates, create a difficult heat-sinking problem.

We earlier reported a transferred substrate HBT process which reduces device parasitic capacitances, and consequently results in increased power gain bandwidth f_{max} [1]. HBTs have been reported [2] with $f_{max} > 400$GHz, integrated with interconnects on a low ϵ dielectric. Here, we report a new process that retains these device enhancements, while extending the continuous ground plane of earlier work to form an entirely metallic substrate. Previous realisations of HBT ICs with microstrip transmission lines have generally used the semiconductor substrate as the microstrip dielectric [3, 4]. Here, benzocyclobutene (BCB): a low dielectric constant ($\epsilon_r \simeq 2.7$), low millimetre-wave loss polymer, is used as the microstrip dielectric. The ground plane is formed by electro-plating on the BCB film and into vias in it. An initial layer of gold in the ground plane is supplemented with sufficient electro-plated copper to make the ground plane itself mechanically robust, and the InP growth substrate is then removed by selective etching. Fig. 1 shows three schematic steps in the processing sequence. Note that the final substrate promises greatly improved heat-sinking: InP, with a thermal conductivity of ~75Wm^{-1}K^{-1}, is replaced with copper, having a thermal conductivity of ~400Wm^{-1}K^{-1}.

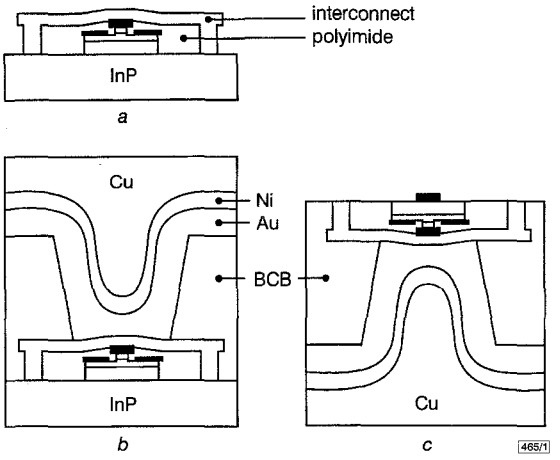

Fig. 1 *Schematic diagram of wafer at three stages of processing*

a Plated gold interconnections run over polyimide passivation
b Au, Ni and Cu plated over wafer into vias in BCB, grounding an emitter in this case
c Metallisation defines collectors after InP growth substrate has been removed

Copper was electro-plated in this work from a $CuSO_4$ solution. This widely used electrolyte generally produces deposits with low intrinsic film stress. The thermal expansivity of copper is badly mismatched to those of the semiconductors used here. In the final structure, however, only single device sized areas of epitaxial material remain fixed to the copper substrate, and the strain energy developed in the semiconductor by thermal cycles is thus limited.

The InAlAs/InGaAs epitaxial structure in the present work is as reported in [2]. Emitter up devices are fabricated in a double mesa process, with electro-plated interconnects, as in [5] up until the substrate transfer step. A film of benzocyclobutene (BCB) resin is deposited on the partially processed wafer by spin deposition. The BCB resin is then oven cured under N_2 ambient to a final thickness of approximately 13μm. Grounding vias in this dielectric are etched by RIE, down to the emitter interconnect and ground pad areas. Thin layers of titanium and gold are deposited over the entire wafer by sputtering. The wafer is then loaded in a custom fixture, made of PTFE, which provides electrical contacts and mechanical seals to the front surface of the wafer, controlling the gross distribution of plated metal in subsequent steps. Gold is electro-plated from a commercial sodium gold sulphite solution, followed by a nickel diffusion barrier plated from a commercial nickel sulphamate solution. Copper is plated, from a solution prepared from $CuSO_4$ and H_2SO_4, to a thickness of ~200μm. The

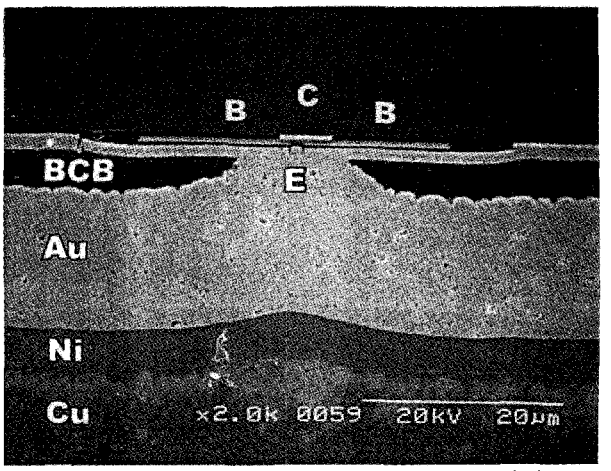

Fig. 2 *SEM cross-section of test wafer, showing layers of plated substrate*

A via through BCB grounds emitter interconnect of discrete device in this image. Locations of emitter, base and collector contacts are indicated by letters E, B, and C, respectively