Chapter 4
Amplifiers and Mixers

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4.1 60 GHz Low-Noise Amplifiers: What's Different?

The key performance requirements of the 60 GHz low-noise amplifier (LNA) are power gain, noise figure, linearity, stability, impedance matching, power dissipation, bandwidth, and design robustness to process/voltage/temperature variation. These basic requirements are universal for LNAs, and as will be shown, the basic design methodologies at 60 GHz are not all that different than those at much lower frequencies. The circuit topologies, however, will be different to account for the three fundamental differences of 60 GHz design compared to lower frequency design, which are (1) designing using transistors operating much closer to their cutoff frequencies[1], (2) operating with signals with small wavelengths resulting in distributed effects within actual components of the circuit, and (3) designing with parasitic elements which represent a much larger portion of the total impedance or admittance on a given node. The implications of these three differences are now briefly discussed, and then illustrated through circuit examples later on in the chapter.

4.1.1 Transistors Closer to Cutoff

Transistors operating closer to their cutoff frequencies have less gain and higher noise figure. A useful way to estimate the maximum available power gain, G_{MAG}, in the transistor near cutoff is to compute how many decades below cutoff the operating

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[1] True at least at the time of this writing.

frequency lies and then multiplying by 20 dB, as follows:

$$G_{MAG} \approx 20\log_{10}\left(\frac{f_{MAX}}{f_o}\right), \tag{4.1}$$

where f_o is the operating frequency and f_{max} is the unity power-gain frequency. Note that this is valid only near cut-off where the available power gain in the transistor is equal to the maximum available gain. At lower frequencies, the transistor has enough gain to be potentially unstable; thus, the suitable power-gain metric is the maximum stable gain (MSG) which no longer has the 20-dB/decade slope.[2] As an example, a transistor with an f_{max} of 240 GHz should have a G_{MAG} of approximately 12 dB at 60 GHz.

As a result of the lower available gain per transistor, multi-stage topologies are likely required to provide enough gain to suitably deemphasize the noise contribution from the mixer and subsequent stages. Multi-stage amplifiers consume more power and area, have poorer linearity, and have more internal nodes which require stability checks. The noise performance of a multi-stage amplifier may or may not deviate from the minimum achievable noise performance in the technology, depending on whether or not each gain stage is designed for minimum noise or maximum gain. Reduced transistor gain means less margin for process/temperature/voltage variations, less margin for de-Q'ing output loads (for broader bandwidth response), and less margin for series or shunt feedback. A multi-stage amplifier will have more cascaded tuned amplifier responses, each with their own temperature degradation. As a result, a larger temperature variation can be expected. In summary, operating closer to device cutoff means poorer performance across the board for the LNA.

4.1.2 Small Wavelengths

At 60 GHz the wavelength of light in free-space is approximately 5 mm. In SiO_2, the wavelength is roughly halved or 2.5 mm. When signals traverse components which are an appreciable size of a wavelength, then they actually betray their true nature of being waves rather than simple stationary voltages and currents, resulting in a noticeable phase delay across that component. As a result, distributed effects must be considered as part of the design process. One rule-of-thumb for the distance which signifies the *lumped/distributed* boundary is 5% of the wavelength, or 125 μm at 60 GHz in SiO_2. In practice this boundary has been reduced to about 1% of the wavelength, or 25μm at 60 GHz in SiO_2, to accurately model the circuit performance.

Operating in the distributed regime is nothing to fear. Anyone who has designed circuit boards in the low GHz frequency range is already familiar with the fundamentals and the basic toolbox. One implication of the distributed regime is that

[2] Alternately, the unilateral power gain or Mason's gain can be used with this simple equation, (4.1).

impedance matching is required on internal mm-wave nodes within the circuit to ensure maximum power transfer. Another implication is that any interconnect within the circuit which is an appreciable size of a wavelength should be treated as a transmission line and accurately modeled. Transmission lines, therefore, become very important elements in the entire millimeter-wave portion of the radio, as they are used as both interconnects and to realize passive components. A final implication (or benefit, actually) of operating in the distributed regime is that many traditional microwave structures, such as hybrid couplers, now become viable on-chip. Thus, the 60 GHz circuit designer has a wider pallet of devices at his or her disposal, each with certain trade-offs.

4.1.3 Parasitics at 60 GHz

The parasitic reactive components one cares about in a circuit are shunt capacitance on a node, creating an admittance which is proportional to frequency, and series inductance on a node, creating an impedance proportional to frequency. Both of these worsen as frequency increases. As an example, a lumped capacitance value at 60 GHz may be $\sim$30 fF (or -j88 Ω). A parasitic capacitance of 3 fF represents 10% of the total capacitance on that node and can therefore shift the resonant frequency by $\sqrt{1.1}$ or 5%. Clearly, 3 fF parasitic capacitances are commonplace in any design, and they must therefore be accurately extracted and modeled. Turning to an inductor example, a lumped inductor value at 60 GHz may be 150 pH (or +j56 Ω); thus, 15 pH represents 10% of the total series inductance on that node. Technologies with reasonably thick back-ends-of-the-line (say, 10 μm) can have large vias from the top level metal to the front-end devices, and this via can exhibit a noticeable inductance. As an example, a via inductance of $\sim$4 pH was found both empirically and through electromagnetic simulation for a via of 4-μm height. This value of 1 pH/μm is equivalent to the 1-nH/mm rule-of-thumb for bondwires.

Another parasitic component which is relevant is series resistance. At 60 GHz the skin-depth in the copper and aluminum metal alloys used in most foundries is approximately 0.5 μm. Top-level metals thicker than this will exhibit frequency-dependent losses, but these layers will have the smallest loss per unit width. Also, ground planes thinner than the skin depth will not completely terminate electromagnetic fields from above; thus, additional current can flow beneath these very thin ground planes in other layers which may be more resistive (like the silicon substrate), resulting in more loss than intended.

4.2 Low-Noise Amplifier Design Methodology

Let us now review some basic relationships between gain, noise figure and linearity. As its name suggest, the low-noise amplifier should provide moderate to high power

gain while introducing a minimal amount of noise. The gain in the LNA deemphasizes noise contributions from subsequent receiver stages by amplifying the noise present at the input by a large enough value such that subsequent noise contributions are small by comparison. Therefore, the signal-to-noise ratio (SNR) of the entire receiver is effectively set to the SNR at the output of the LNA. This can be seen through Friis formula for cascaded noise factor, as follows [1]:

$$F = \frac{(S/N)_{IN}}{(S/N)_{OUT}} = F_{LNA} + \frac{F_2 - 1}{G_{LNA}} + \frac{F_3 - 1}{G_{LNA} \cdot G_2} + \cdots \tag{4.2}$$

where F_i and G_i are the noise factors and available power gains, respectively, of individual stages in the receiver. Thus, to minimize the total receiver noise figure, the first stage in the receiver should amplify the input signal by as large an amount as possible while adding minimal noise.

The LNA gain cannot be arbitrarily increased, however, due to its negative impact on large-signal performance. Clearly, the gain present in the LNA makes it more difficult for subsequent receiver stages, such as the mixer, to remain linear. Linearity is often quantified in terms of a third-order intercept point (IP3) as well as a 1-dB compression point. The expression for the total IIP3 for a cascaded system can be expressed as follows [2]:

$$\frac{1}{iIP3_T} = \frac{1}{iIP3_{LNA}} + \frac{G_{LNA}}{iIP3_2} + \frac{G_{LNA} \cdot G_2}{iIP3_3} + ... \tag{4.3}$$

where iIP3i and Gi are the input-referred IP3 (in watts) and the power gain (in watts/watt) of each individual stage of the receiver. For gains greater than one, the linearity of latter stages will dominate the total receiver linearity. Therefore, to maximize the receiver's IIP3, the latter stages' linearity should be maximized while reducing or limiting the total preceding gain.

Equations (4.2) and (4.3) imply an acceptable range of LNA gains which will meet both the system's noise figure and linearity requirements. It should be pointed out that these requirements do not always have to be met concurrently, in which case it is possible to design the LNA to have adjustable or switched gains to allow for a wider receiver dynamic range.

4.2.1 Input Match Optimization for Noise and Power

The heart of any LNA design is the input impedance match which is optimized for minimum noise factor together with maximum power transfer. A *fundamental objective of the LNA is to achieve a coincident input power match and input noise*

match. The most insightful way to examine power and noise matching trade-offs is to utilize noise parameters. Any two-port network can be represented with four noise parameters which describe how the noise factor behaves with respect to the input match [3]. A variety of noise factors can be used, with the three most common sets shown below.

$$F = F_{\min} + \frac{R_n}{G_S} \left| Y_S - Y_{opt} \right|^2 \tag{4.4}$$

$$F = F_{\min} + \frac{G_n}{R_S} \left| Z_S - Z_{opt} \right|^2 \tag{4.5}$$

$$F = F_{\min} + 4r_n \frac{\left| \Gamma_S - \Gamma_{opt} \right|^2}{\left| 1 + \Gamma_{opt} \right|^2 \left(1 - \left| \Gamma_S \right|^2 \right)} \tag{4.6}$$

In all three, the noise factor reaches a minimum value, F_{min}, at the optimum input impedance match, expressed in either admittance (Y_{opt}), impedance (Z_{opt}), or reflection coefficient (Γ_{opt}). The sensitivity of noise factor with respect to impedance mismatch is captured by either the noise resistance (R_n) or noise conductance (G_n), depending on whether the admittance or impedance domain is used. Larger noise resistances (or conductances) result in greater sensitivity to noise mismatch.

To obtain a low noise factor, the LNA design should first provide for the minimum F_{min} possible by selecting the optimum bias point for the transistor, the optimum layout for that transistor, and of course the appropriate base technology for the transistor with suitable f_T/f_{max}. Second, the LNA design should provide an input matching network which transforms the source impedance (admittance) to Z_{opt} (Y_{opt}), where Z_{opt} should be designed to coincide with the matching condition for maximum power transfer. This is to say that Z_{opt} *should be the complex conjugate of the input impedance to the amplifier,* Z_{in}. Failing to make the noise match and power match coincident results in either sub-optimal input return loss or sub-optimal noise figure. Noise figure calculations which directly compute F for a 50 Ω source obscure the existence and relevance of Z_{opt} (Y_{opt}) and hide the fundamental trade-off which exists between noise and power matching.

The noise and power match requirement is illustrated in Fig. 4.1, for reflection coefficients rather than input impedances. Here, the basic input-match requirement for the LNA is to make the power and noise match coincident, meaning that Γ_{in} and Γ_{opt} should be complex conjugates of one another.

4.2.2 Transistor Noise Parameters

The noise parameters of the transistor can be derived by equating the basic "noisy" circuit network with a "noiseless" network with input voltage and current noise sources, v_n, and i_n, as shown in Fig. 4.2. By equating the short-circuit output current in both networks for open-circuited and short-circuited input conditions, i_n and v_n can be derived, respectively [4].

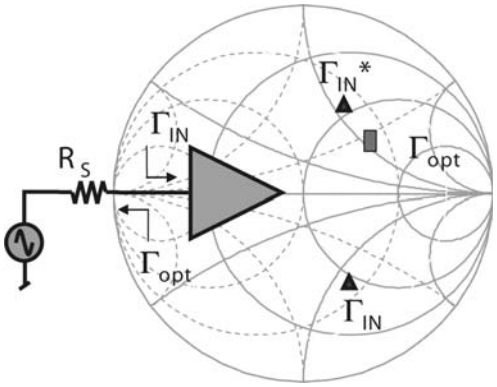


Fig. 4.1 Illustration of impedance matching requirements for LNA together with Smith chart. The input reflection coefficient Γ_{in} should be the complex conjugate of the the optimum noise reflection coefficient Γ_{opt}.

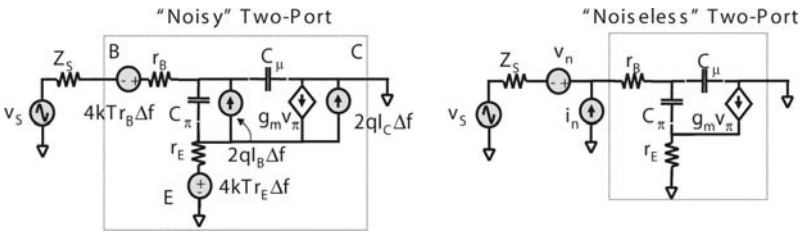


Fig. 4.2 Schematic of BJT with dominant noise sources defined (left) and equivalent input noise generators (right).

Figure 4.2 shows the dominant noise sources for a BJT[3]. The noise resistance and conductance which define the noise power in v_n and i_n, respectively, can be readily derived to be

$$R_n = \frac{\overline{v_n^2}}{4kT\Delta f} \approx \frac{1}{2g_m} + r_B + r_E \tag{4.7}$$

$$G_n = \frac{\overline{i_n^2}}{4kT\Delta f} \approx \frac{g_m}{2}\left(\frac{\omega}{\omega_T}\right)^2 \tag{4.8}$$

Since these two equivalent input noise sources (v_n and i_n) originate from the same noise sources in the circuit (e.g., shot noise and thermal noise), they are necessarily correlated. A noise correlation power, C_n, can be defined as

[3] Note that the noise sources for a CMOS transistor are located in the same positions, where the collector and base shot noises should be replaced with thermal noise in the channel lumped to the drain or the gate (also known as gate-induced noise), respectively, and base/emitter resistance should be replaced with gate/source resistance [5].

$$C_n = \frac{\overline{i_n^* v_n}}{4kT\Delta f} \approx \frac{-j}{2}\left(\frac{\omega}{\omega_T}\right). \tag{4.9}$$

Note that these parameters, R_n, G_n, and C_n, are another valid set of noise parameters, where C_n can have both real and imaginary components. These four noise parameters can be translated into the noise parameters of interest in (4.5), through the following formulas [6]:

$$F_{\min} = 1 + 2Re(C_n) + 2\sqrt{G_n R_n - [Im(C_n)]^2} \tag{4.10}$$

$$Z_{opt} = \sqrt{\frac{R_n}{G_n} - [Im(C_n)]^2} - jIm(C_n). \tag{4.11}$$

Substitution of (4.7)-(4.9) into (4.10) and (4.11), yields

$$F_{\min} \approx 1 + \left(\frac{\omega}{\omega_T}\right)\sqrt{2g_m(r_B + r_E)} \tag{4.12}$$

$$Z_{opt} \approx \left(\frac{\omega_T}{\omega}\right)\sqrt{\frac{2(r_B + r_E)}{g_m}} + \frac{j}{\omega(C_\pi + C_\mu)} \tag{4.13}$$

Equation (4.13) is an important result from this exercise, as the optimal LNA should have a Z_{opt} equal to the complex conjugate of the input impedance, Z_{in}.

4.2.3 Common-Base vs. Common-Emitter

Using (4.12) and (4.13), we can now compare the basic input stages for an amplifier in terms of noise and power match, namely the common-base and the common-emitter stages, depicted in Fig. 4.3. The noise parameters in either configuration are identical; however, the input impedances are quite different.

A common-base stage has an input conductance equal to the device transconductance, g_m. If a shunt inductor is used to resonate out the input capacitance, then Z_{in} is simply $1/g_m$. This cannot be made to be equal to the real part of Z_{opt} of (4.13); thus, a common-base LNA input stage suffers from either a poor noise match or a poor power match. This is commonly recognized at lower frequencies and persists at millimeter-wave frequencies.

A common-emitter amplifier without any feedback suffers from a very high quality-factor (low resistance) input impedance which is difficult to impedance match. As a result, feedback is typically employed, with emitter degeneration quite

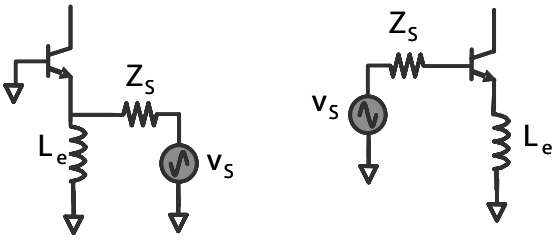


Fig. 4.3 Basic schematic of common-base input stage and common-emitter with degeneration input stage.

common. The common-emitter amplifier with inductive degeneration can achieve a coincident noise and power match, as the emitter inductor provides a degree of freedom. The input impedance of this configuration can be easily derived by reflecting the emitter impedance into the base by multiplying it by one plus the current gain ($\beta(\omega) = \omega_T/j\omega$). As a result,

$$Z_{in} = \omega_T L_e + j\omega L_e + \frac{1}{j\omega(C_\pi + C_\mu)} \tag{4.14}$$

It can be shown that the noise parameters of a network with ideal feedback are identical with respect to F_{min} and R_{opt}, where only X_{opt} has been reduced by the series feedback (i.e., the impedance in the emitter) [7]. Examining (4.13) and (4.14), it can then be seen that the noise and power match can be made coincident by selecting the emitter degeneration to form the real part of the input impedance (typically 50 Ω) and then by selecting the size of the transistor to make R_{opt} 50 Ω as well.

The simple design procedure for the LNA input stage can be summarized as follows:

1. Simulate noise measure (NM)[4] versus collector current density (J_C) to choose optimal *range* of collector current density (J_C) for minimum noise measure.
2. Scale emitter length such that R_{opt} = 50 Ω , increasing device size (emitter length) to reduce the optimum noise impedance.
3. Add degeneration inductor to create real input impedance for power match.
4. Complete input match with series inductor in the base.

It should be pointed out that this is the same design methodology advocated at lower frequencies by Voinigescu [5], and it has been found to work at mm-wave frequencies as well. At mm-wave, the device physics of the transistor have not changed;

[4] Noise measure is the noise figure of an arbitrarily long cascade of identical amplifiers. It is a more useful metric for noise performance of amplifiers with low gain, since noise contributions from second-, third-, etc. stage amplifiers becomes relevant [3].

thus, it should come as no surprise that the methodology to achieve optimum noise performance has not changed as well. Note that the procedure listed about is bipolar-centric; however, the same procedure also applies to MOSFETs as well, with the appropriate substitution of noise parameter quantities and device nomenclature.

Finally, one additional qualification for this design methodology is required. This procedure assumes that the amplifier is unilateral. That is, it assumes that the reverse isolation is quite good, meaning that the output impedance matching network does not change the input impedance. This is typically true of cascade amplifiers; however for single-transistor amplifiers, particularly at 60 GHz, the reverse isolation can be low. As a result, the concept of simultaneous conjugate input and output matching can be adopted [3]. This means that the input power matching goal of 50 Ω should be replaced with a goal of achieving the simultaneous conjugate match condition. This then requires that the output matching network for the amplifier be designed as well for simultaneous conjugate matching.

4.3 Low-Noise Amplifier Examples

Several bipolar and CMOS LNAs are now presented. We begin with two bipolar amplifiers, one with a common-base input stage and one with a degenerated common-emitter input stage. Next we consider several CMOS amplifier design approaches. These examples show mm-wave LNA design techniques and topologies and also illustrate the performance differences between the various approaches.

4.3.1 Bipolar LNA (v1), Common-Base Input

A simplified schematic of the first version of a bipolar 60 GHz LNA is shown in Fig. 4.4 [8], [9], [10]. This amplifier was implemented in a 0.13-μm bipolar-only process with NPN HBTs with 200 GHz f_T and 280GHz f_{max} [11]. The input stage is a common-base amplifier, which exhibits higher gain compared to the degenerated common-emitter [5]. Also, its high reverse isolation decouples the input and inter-stage matching networks. The second stage of the LNA is a common-emitter cascode amplifier with emitter degeneration. Each stage provides ∼8 dB of gain when biased at 3 mA and V_{CC} = 1.8 V.

Impedance matching at the input, inter-stage, and output are realized with single-stub tuners. This is an example of a distributed-based network topology. An advantage of the single-stub tuner is that it does not require prohibitively small series capacitors, since the network is realized solely with transmission lines. Operation of the tuner is best described through an example of matching a given admittance, $Y_{L,}$ to 50 Ω. The series line first transforms Y_L to $Y' = 0.02 + jB$, i.e., rotating along a constant

[5] Portions of this text is taken from [10], (© IEEE 2005)

VSWR circle on the Smith chart. The shunt stub then generates an admittance of *–jB* which adds directly to Y', i.e., moving along the $0.02\,\Omega^{-1}$ conductance circle to the center of the Smith chart, resulting in a matched condition. The stub lengths are $\sim$100 μm ($\mathrm{TL}_{4,7}$) while the series transmission line lengths are $\sim$300 μm ($\mathrm{TL}_{3,6}$). Additionally, this amplifier uses metal-insulator-meal (MIM) AC coupling capacitors ($\mathrm{C}_{2,3}$) operating beyond self-resonance are used between the two stages and at the output.

At 60 GHz, the silicon substrate exhibits low impedance; thus, care was taken in circuit design and layout to ensure adequate reverse isolation and stability. Metal-1 ground shields are used throughout the amplifier, and substrate ties are included wherever possible. Also, metal-2 V_{CC} planes are used together with many MIM bypass capacitors to realize a low-impedance supply. A die photograph of the LNA is shown in Fig. 4.5. The die size is 0.9×0.6 mm^2. Diamond-shaped pads are used at the input and output to reduce the parasitic capacitance of the pad.

The measured S-parameters for the LNA are shown in Fig. 4.6, together with the simulated results. The LNA is unconditionally stable over 30-110 GHz. At 61.5 GHz, the gain is 14.7 dB and the reverse isolation is 40 dB, when biased at 6 mA from a 1.8-V supply. The input return loss is 6 dB, while the output return loss is 17 dB. Model-to-hardware correlation is excellent for S_{21}, S_{12}, and S_{22}. The miss in S_{11}, though, was not expected, particularly given that the output match was right on target. An alternate version of the LNA which had coplanar waveguide (CPW) tapers at the input and output [9] showed S_{11} and S_{22} better than -12 dB, as expected. Since the CPW taper absorbs pad parasitics, the miss in input match for the *pad-LNA* is attributed to the input bondpad transition.

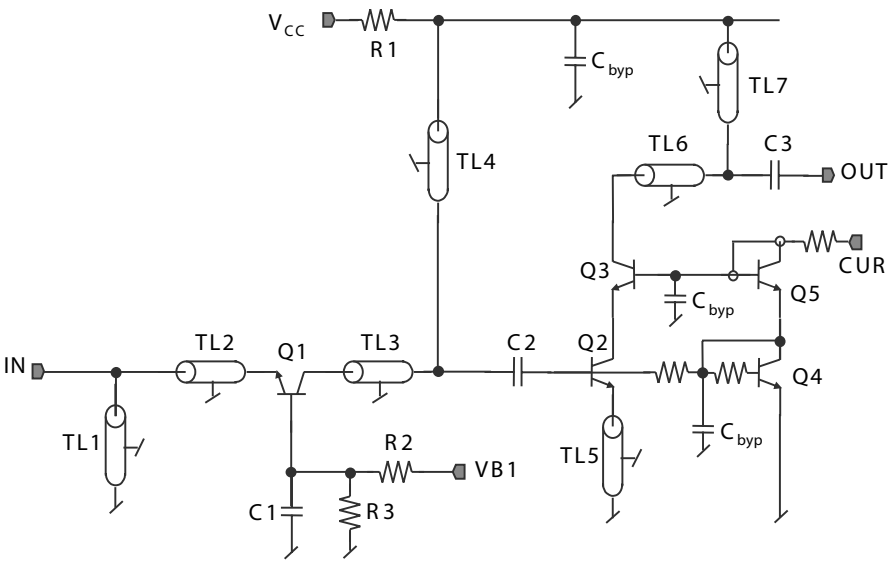


Fig. 4.4 Simplified schematic of bipolar LNA, version 1, common-base input [10] (© IEEE 2005).

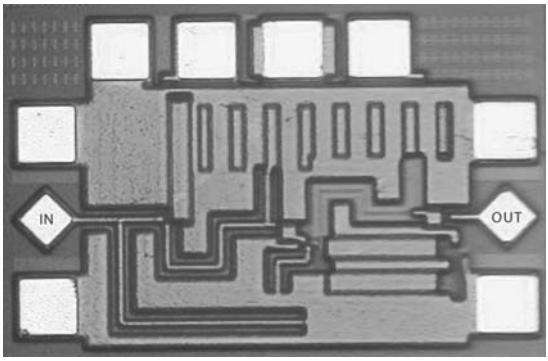


Fig. 4.5 Die micrograph of the common-base 60 GHz LNA, version 1 [10] (© IEEE 2005).

Figure 4.7 shows the measured and simulated NF of the LNA (with pads) at 6 mA and 1.8 V. No on-chip loss has been de-embedded from this result. The measured NF is 4.5 dB at 61.5 GHz, while the simulated NF is 4.6 dB. The taper-LNA also has a NF of 4.5 dB when the insertion loss of the tapers is de-embedded. The simulated minimum NF of the LNA is 4.2 dB, while the NF_{min} of a single transistor is 3.1 dB. From simulation, the input common-base device contributes 80% of the added noise (split nearly equally between collector shot noise and thermal noise from base resistance), while the second-stage cascode contributes 10%. The remaining 10% comes from other assorted sources. As expected, under this good noise matching condition, the input power match is poor, with an input return loss of only 6 dB. Table 4.1 summarizes the other performance metrics for this LNA, including linearity, power consumption, and reverse isolation.

Table 4.1 Comparison between bipolar 60 GHz LNAs, version 1 and 2

LNA	**Version 1**	**Version 2**
Topology	2-stage: Common-Base Cascode	4-stage: Common-Emitter (x2) Cascode (x2)
Spot Freq.	61.5 GHz	61.5 GHz
Gain	15 dB	20 dB
Image Rejection	$>$ 15 dB	$>$ 26 dB
NF	4-6 dB	4.8-6.2 dB
S11	-6 dB	-15 dB
S22	-17 dB	-15 dB
iCP1dB	-20 dBm	-29 dBm
VCC	1.8 V	2.7 V
Current	6 mA	10 mA

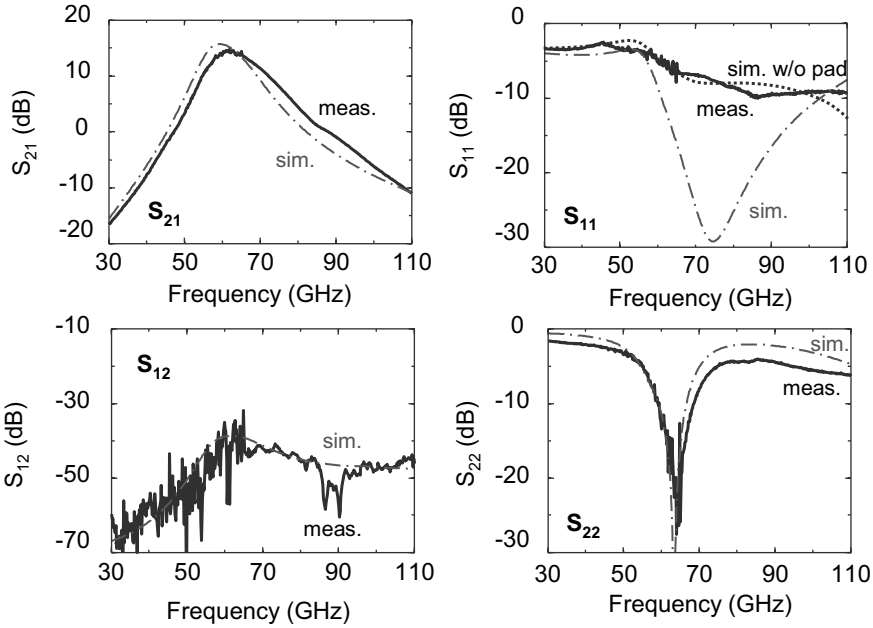


Fig. 4.6 Measured and simulated S-parameters for common-base 60 GHz LNA, version 1 [10] (© IEEE 2005).

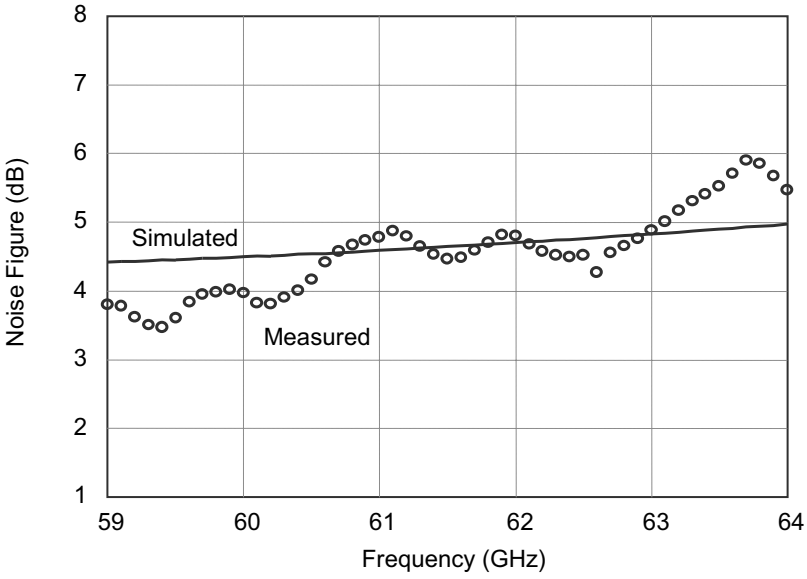


Fig. 4.7 Measured and simulated noise figure of 60 GHz common-base LNA, version 1 [10] (© IEEE 2005).

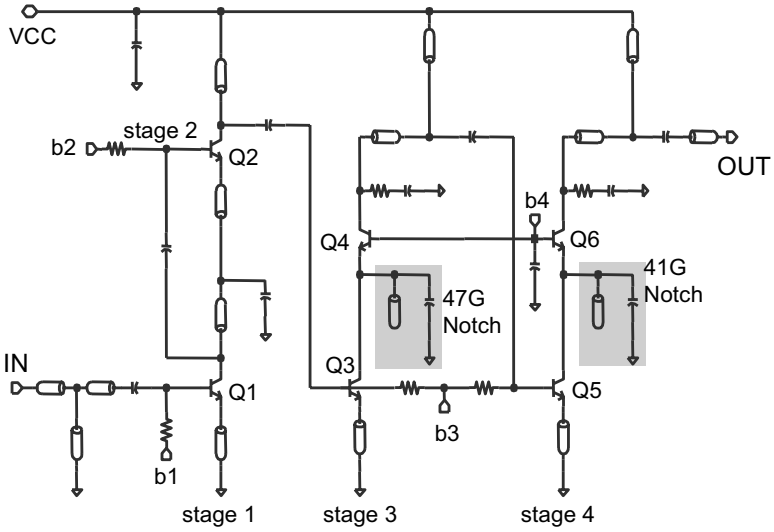


Fig. 4.8 Simplified schematic of 4-stage, 60 GHz bipolar LNA, version 2, common-emitter input [14] (© IEEE 2006).

4.3.2 Bipolar LNA (v2), Common-Emitter Input

Fig. 4.8 shows a simplified schematic of a second version of a bipolar 60 GHz LNA [12], [13], [14]. This LNA was implemented in a 0.13-μm SiGe BiCMOS technology which features NPN HBTs with 200 GHz f_T and 265 GHz f_{MAX}. This LNA was designed for a complete 60 GHz receiver; thus, it has additional features and requirements. First, it was designed to have $\sim$20 dB of gain to achieve the lowest possible noise figure for the receiver. Second, it was designed to include embedded image-reject notch filters, since the receiver employs a superheterodyne topology. In the receiver, the image frequency is between 42 and 46 GHz; hence, notches were designed at 41 and 47 GHz to bracket this image band. Finally, the LNA was designed to work with the receiver's 2.7-V supply voltage.

The LNA is a four-stage design. The first two stages (transistors Q1 and Q2) are inductively-degenerated common-emitter amplifiers. These amplifiers are designed for minimum noise figure at $\sim$4dB per stage and provide roughly 5 dB of gain in each stage. Stages 1 and 2 are stacked one on top of the other for current re-use. Stages 3 and 4 in the LNA are cascode amplifiers. Image rejection is provided in these two stages by notch filters at 47 and 41 GHz. Each notch filter, placed at the junction between the two cascode devices (Q3-Q4 and Q5-Q6), contains an open-circuited microstrip transmission-line stub, $\lambda/4$ in length at the notch frequency. The quarter-wavelength transforms the open-circuit on the far end of the line to a short-circuit at a the near end of the line; therefore, all small-signal current coming out of the common-emitter stage of the cascade is shunted to ground. An additional shunt capacitor is included with the stub to resonate out the incremental inductance which

exists at the RF frequency (60 GHz). The resultant response from the filter is a series resonance to ground at the image and a parallel resonance at RF.

The noise figure (NF) of each cascode amplifier is approximately 6 dB; hence, stages 1 and 2, each with 5 to 6-dB gain and approximately 4-dB NF, were added to reduce the cascaded NF and increase gain. Fig. 4.9 shows the measured and simulated S-parameters of the LNA while Fig. 4.10 shows the measured noise figure. The measurements indicate 5 to 6.2-dB NF and 20-dB gain. Additional LNA measurements are summarized in Table 4.1, including power consumption, linearity, return loss, and image rejection.

Comparing versions 1 and 2 of the bipolar LNAs (see Table 4.1), we see that the common-emitter and common-base amplifiers have very similar noise figure performance, achieving in the realm of 5-dB noise figure. However, the common-base input stage has a poor input return loss of only 6 dB, while the degenerated common-emitter amplifier has a good input return loss of about 12 dB. This confirms our earlier assertion that the degenerated common-emitter topology provides a better input power *and* noise match than the common-base topology. Both amplifiers provide adequate RF power gain while consuming 10 to 30 mW of dc power.

4.3.3 CMOS Common Source Amplifiers

In this section we describe the design of two common source mm-wave amplifiers reported in [15]. A low power LNA was designed to operate in the 60 GHz band, while a prototype 104 GHz amplifier demonstrates the possibility of designing a linear circuit at a frequency higher than the f_T of the technology node[6].

Many reported mm-wave CMOS amplifiers use cascode devices [17] [18] [19]. One advantage of the cascode device is that they can be made unconditionally stable at the operating frequency, making the design more robust and simplifying matching networks. However the noise figure of a cascade is relatively high compared to common source device when operating close to f_T due to the reduced degeneration on the cascade device at high frequencies. For this reason, common source devices are preferred for ultra low noise designs close to the limits of activity. The round-table common source device described in Section 3.2.2 are conditionally unstable up to 95 GHz, requiring careful design of the source and load networks. Consequently for the 60 GHz LNA, the source/load impedance for each stage should be selected to be as far as possible from the instability regions while maintaining a good gain/noise performance [3]. The maximum stable gain of common source devices with similar layout methods is more or less independent of the width, enabling low power design by using smaller devices.

CPW transmission lines are used extensively in the design for impedance matching, interconnect wiring, and the bias networks. Transmission line lengths are kept much shorter than $\lambda/4$ in order to reduce losses and minimize the noise contributions

[6] Portions of this section are taken from [15] and [16], (© IEEE 2007)

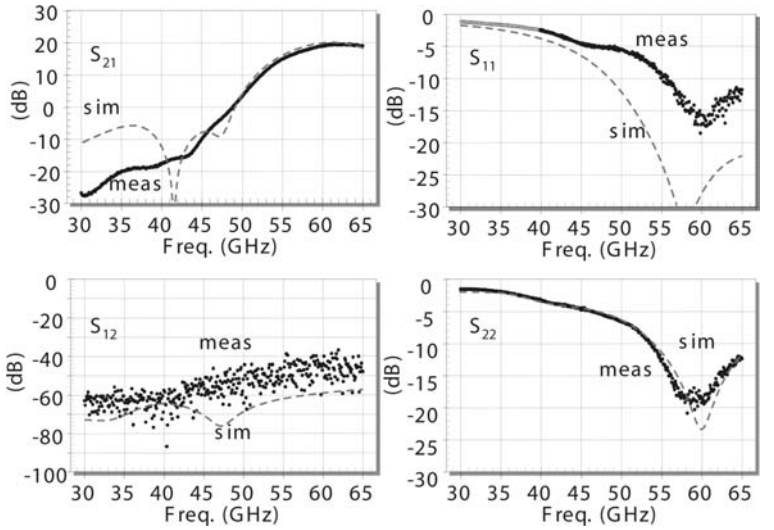


Fig. 4.9 Measured and simulated S-parameters of 4-stage 60 GHz bipolar LNA, version 2, common-emitter input.

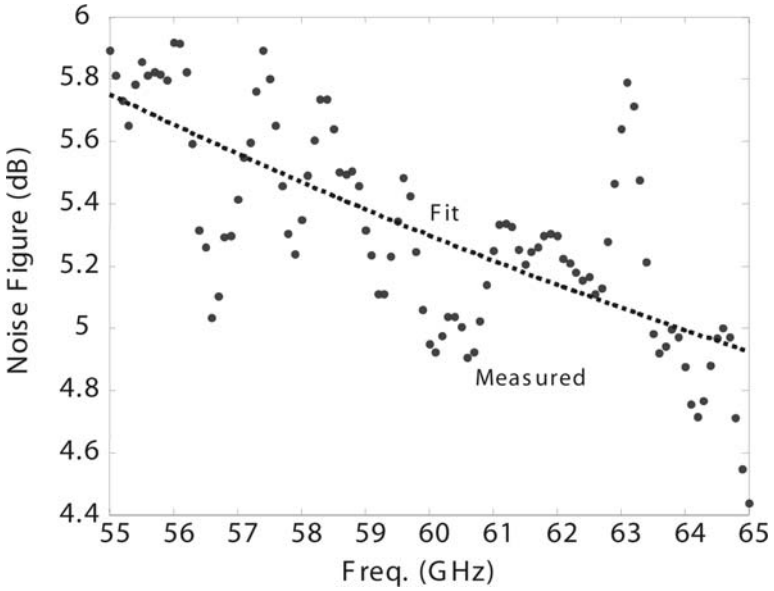


Fig. 4.10 Measured noise figure of 4-stage 60 GHz bipolar LNA, version 2, common-emitter input.

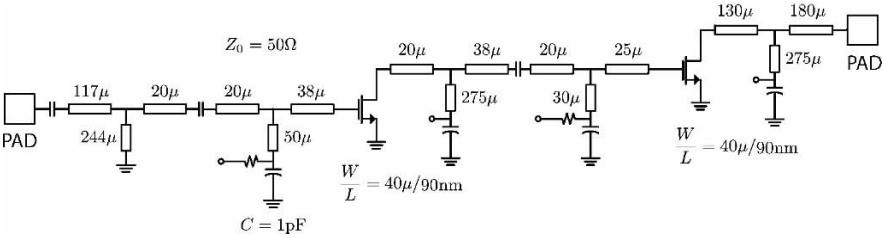


Fig. 4.11 Schematic of 60 GHz common source amplifier [15] (© IEEE 2007).

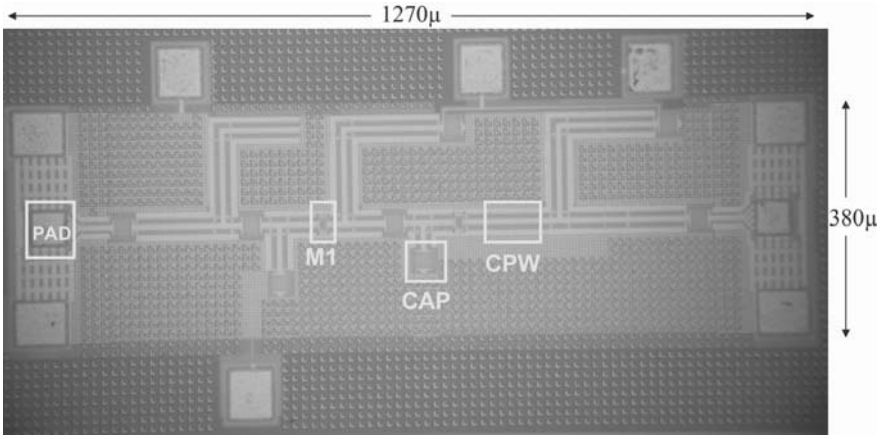


Fig. 4.12 Die photo of 60 GHz common source amplifier [15] (© IEEE 2007).

at the input of the amplifier. Finger MOM capacitors are used for ac-coupling of the input and output as well as between stages. They are also used as bypass capacitors for the DC feed lines. These capacitors are non-ideal and behave inductively at 60 GHz due to their low self-resonance frequency (47 GHz). This does not cause any issue as long as they are well modeled and used as a part of the matching network to shorten the length of transmission lines.

The schematic and the microphotograph of the 60 GHz LNA is shown in Fig. 4.11 and Fig. 4.12. Two $W = 40\,\mu\text{m}$ round-table devices are used running 6.5mA and 4mA from a 1V power supply. A grounded transmission line is used in before the first stage to suppress low frequency gain peaking of the circuit. Input and output pads are also modeled and used as part of matching networks. The output port is designed to match to $50\,\Omega$. The input matching network is simultaneously optimized for noise and power to get at least $-10\,\text{dB}$ of input reflection and $6\,\text{dB}$ of noise figure at the center frequency.

The 104 GHz prototype amplifier is essentially very similar to the 60 GHz LNA. NMOS devices $W = 50\,\mu\text{m}$ width are unconditionally stable at this frequency and employed in three amplification stages. Compared to the 60 GHz amplifier, the length

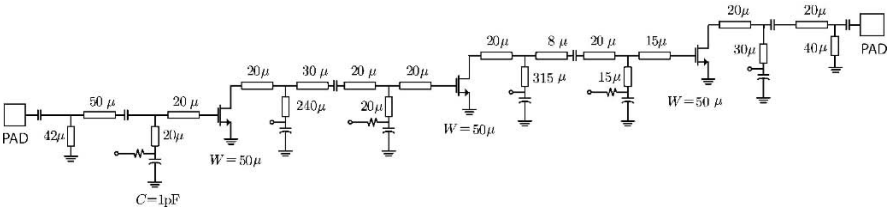


Fig. 4.13 Schematic of 100 GHz common source amplifier [16] (© IEEE 2007).

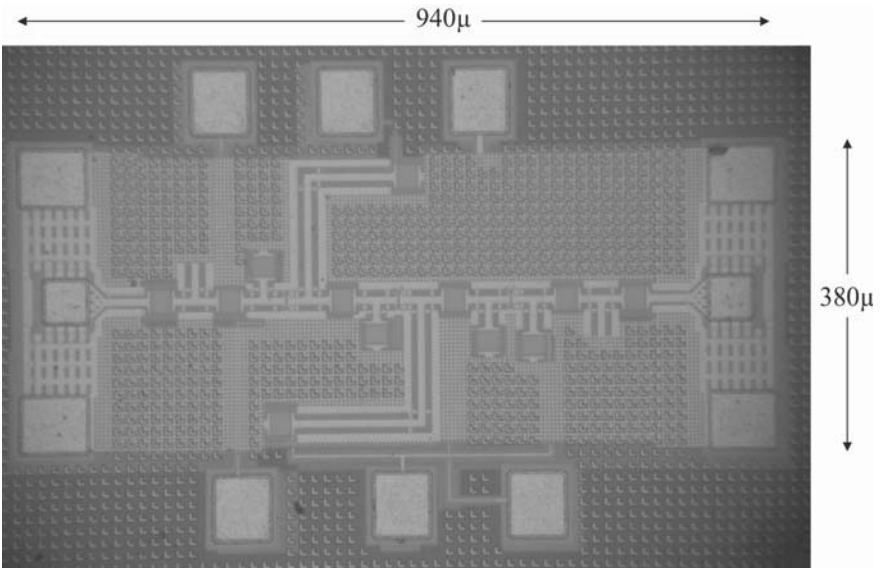


Fig. 4.14 Die photo of 100 GHz common source amplifier [15] (© IEEE 2007).

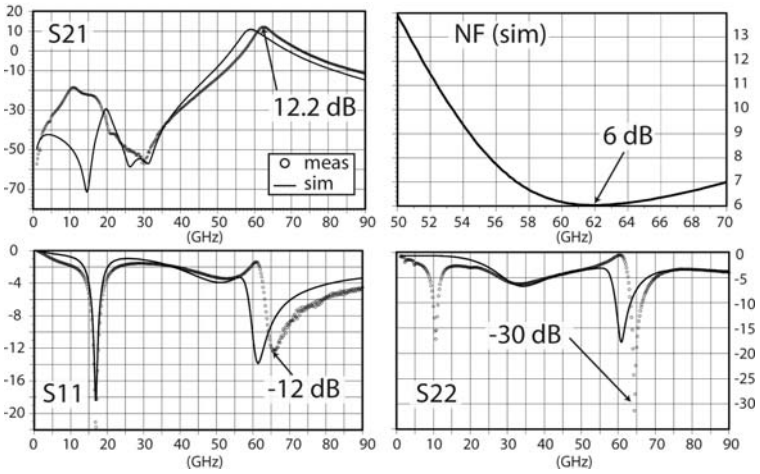


Fig. 4.15 Measured and modeled S-parameters for the 60 GHz common source amplifier [15] (© IEEE 2007).

of transmission lines are naturally shorter and a significant part of matching networks is also now realized through the series inductance of coupling and bypass capacitors. This design was based on de-embedded measurement data of the active devices and models of passive devices. Fig. 4.13-4.14 show the schematic and micrograph of the circuit

The measured and modeled S-parameters for the 60 GHz amplifier are shown in Fig. 4.15. The amplifier achieves a peak power gain of 12.2 dB at 63 GHz and the input and output return losses are -13 dB and -25 dB respectively. The measurement is in a good agreement with the simulation with 1 GHz of frequency mismatch. Also the output match of the circuit has discrepancy with the simulated result, pushing the circuit to the edge of instability. Process variation could explain the frequency mismatch, and based on the post measurement simulations, it was verified that a 5% reduction in T_{ox} could match the measured center frequency with the simulation. The source of mismatch in the S_{22} is not completely clear; however a variation in the drain to body capacitance could also explain this discrepancy. As the drain to body capacitance decreases, a larger share of the signal flows to the output and causes S_{22} to increase. This also causes output gain circles and load stability circles to approach each other. A model of the transistor with T_{ox} and C_{db} variation was compared to the measurements results and shown in Fig. 4.16a-b, which qualitatively resembles the observed deviations in S_{11} and S_{22}.

Fig. 4.17a shows the power sweep measurement of the LNA. The circuit has a measured +4 dBm 1-dB compression point which matches the predicted value based on the large signal model of the device. This translates into 23% of power added efficiency, making it suitable as a pre-driver for a power amplifier or the output stage of a short-range transmitter. The simulated noise figure is 6 dB (Fig. 4.17b) in the pass band of the amplifier while the measured noise figure is 6.5 dB. The measurements is done using a similar amplifier driving a down-conversion mixer and the effect of the mixer noise and cable losses were de-embedded[7].

The measured S-parameters of the 104 GHz amplifier are shown in Fig. 4.18. The amplifier has the peak gain of 9.34 dB at 103.8 GHz. The input and output reflection coefficients are -9.8 dB and -5.5 dB respectively. The circuit draws 22mA from a 1V power supply.

4.3.4 CMOS Common Gate Amplifiers

Common gate amplifiers are seen much less frequently at mm-wave frequencies, despite the fact that they provide an active broadband input impedance match. The downside of the common gate amplifier is much lower power gain (since the current gain is unity) and much higher noise. The full drain noise flows into the input circuit without attenuation (due to unity current gain). Under an input match condition, $1/g_m = R_0$, the drain current contributes nearly equal noise to the output as the

[7] The amplifier also featured a small amount of inductive degeneration added for stability. The simulated noise figure was the same as the tested amplifier.

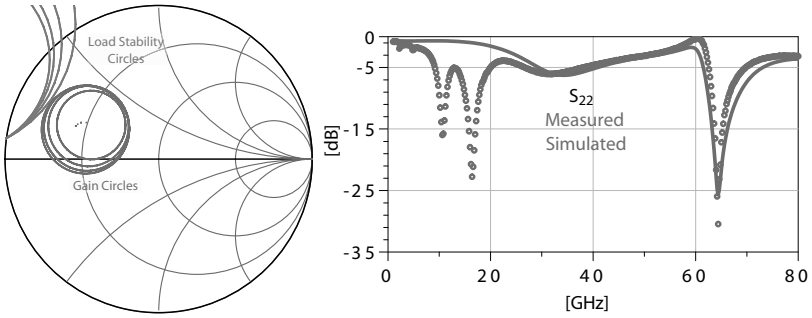


Fig. 4.16 The effect of the drain-body capacitor on gain and stability circles (left) and output scattering parameter S_{22} (right) for 20% variation in C_{db} [16] (© IEEE 2007).

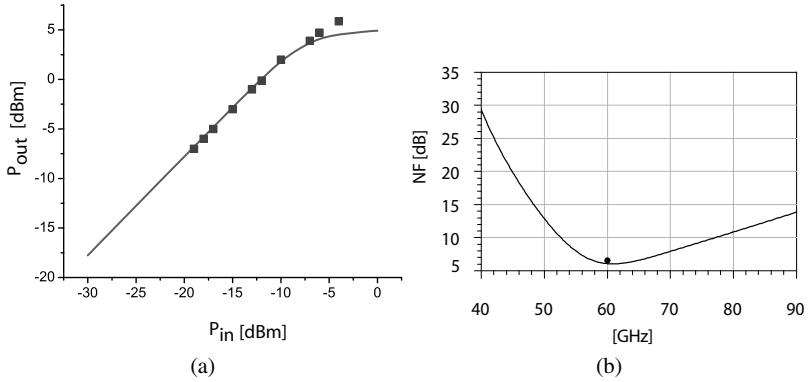


Fig. 4.17 a) Measurement of the output power of the 60 GHz common source amplifier. (b) Simulated and measured (single data point) noise figure of LNA [16] (© IEEE 2007).

source, setting a lower limit to the noise figure at 3dB. Despite these shortcomings, some researchers have found the performance to be adequate at microwave frequencies and advocate the use of the common gate amplifier [20]. It should be noted that the maximum unilateral gain of a transistor is invariant property, regardless of which terminal is taken as common. Thus the f_{max} of a common gate is equal to a common source or common drain amplifier. Thus one can always increase the gain of a common gate amplifier by using an input matching network.

4.3.5 Differential Pair Amplifiers

Differential amplifiers are used extensively in analog and RF circuit design. Differential operation has several benefits, including common mode rejection at the input and

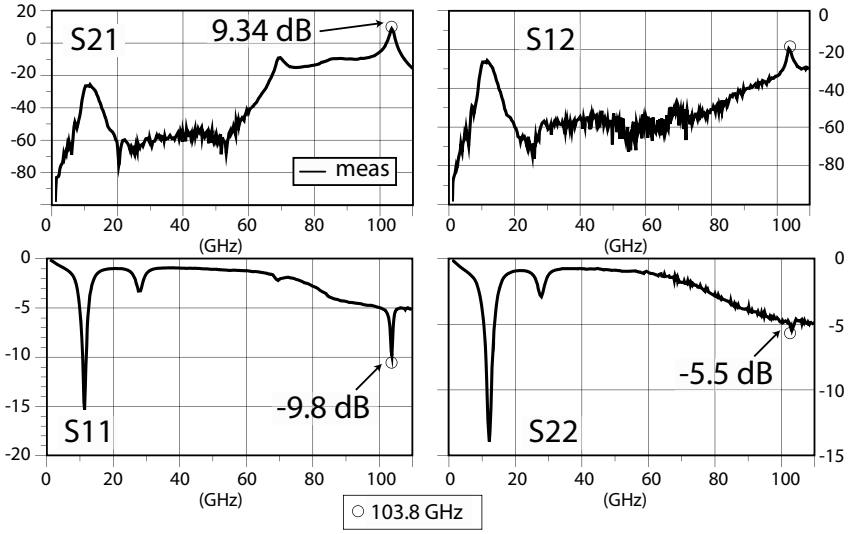


Fig. 4.18 Measurement of the S-parameters of the 100 GHz common source amplifier [15] (© IEEE 2007).

power/ground noise rejection for fully balanced circuits. Since the integrated circuit environment is noisy as a result of high levels of integration, digital switching noise can be rejected using a balanced approach. This argument is quite valid for the VCO and non-linear or time-varying circuits where lower frequency noise can couple to RF, but given the frequency isolation between the mm-wave band and the baseband operating at the low GHz range, the benefits of a differential amplifier at mm-wave are not so much for isolation but for other reasons. Since fully balanced circuits form virtual ground nodes, the physical ground connection is much less problematic for differential circuits. This is a big benefit in mm-wave design since it is difficult to realize a low impedance ground plane in a modern IC process.

A downside of differential and balanced circuits is the doubling of current and the requirement to operate with differential signals. Today most test equipment is designed to operate into a single-ended environment, making it difficult to directly characterize differential circuits. This limitation is temporary and true differential mm-wave equipment will be introduced in the near future. Even if off-chip signals are single-ended, transformers (baluns) can be used quite easily to convert signals to differential form. Another advantage of a differential amplifier is the higher output swing, which is beneficial in improving the dynamic range of amplifiers. Several groups have demonstrated differential amplifiers at mm-wave frequencies [21] [22].

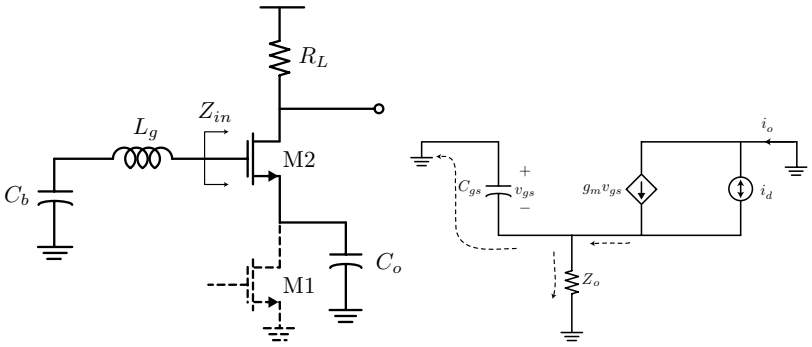


Fig. 4.19 The high-frequency degeneration of a cascode device produces noise and potential instability.

4.3.6 Multi-Stage Amplifier Design

The design of multi-stage amplifiers requires a careful choice in the topology and biasing of each stage. In receiver applications, the input stage should be designed for low noise, preferring single stage (common source or gate) rather than cascode stages. The reduced gain of a single stage amplifier, though, can result in a lower distortion intercept point, since more cascade amplifiers are required to retain the gain. Here we review a few different amplifier approaches with some examples from CMOS. We begin with cascode amplifiers, which can almost be treated as single stage amplifiers, except at high frequencies when we desire to improve the performance.

4.3.6.1 Cascode Noise and Stability

Cascode devices play a crucial role in analog circuit design. At lower frequencies, the main reason for using a cascode transistor is the increase in gain. At mm-wave frequencies, the major benefit is a reduction of the reverse gain S_{12} which in turn results in an increase of the MSG for a given frequency, and which lowers the frequency for which the stability factor k becomes larger than one (unconditional stable device). Regular cascode transistors, however, have a large parasitic capacitance on the interstage node. This capacitance will short-circuit the small signal current at higher frequencies, thus reducing the gain of the cascode structure.

With reference to Fig. 4.19, to calculate the contribution of the cascode device to the noise of the transistor, we can see that the noise has two paths to ground, one through the transistor itself and one through the load, which produces output noise. When the impedance looking into the transistor is much smaller than the current through the load, which occurs at low frequencies, the current circulates through the transistor and has virtually no impact on the output noise. However, as the impedance of the transconductance stage drops due to the capacitance at the shared junction node, the current divides and an appreciable fraction flows to the output

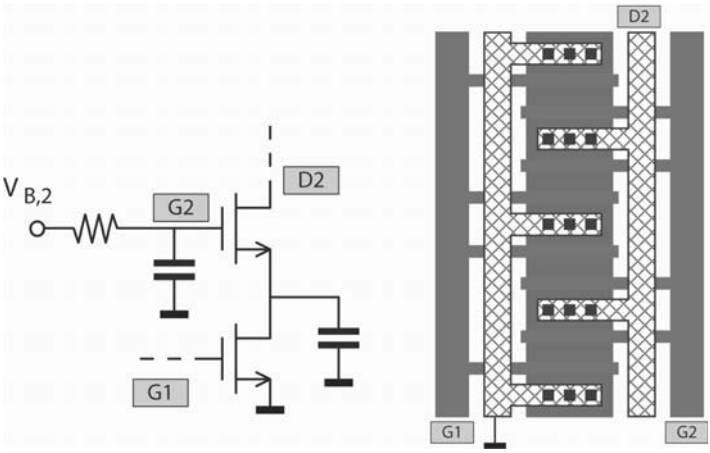


Fig. 4.20 Layout of a shared-junction cascode device [23] (© IEEE 2007).

$$i_o = i_d \frac{1/g_m}{1/g_m + Z_o} = i_d \frac{1}{1 + g_m Z_o} \tag{4.15}$$

$$\overline{i_o^2} = \overline{i_d^2} \left| \frac{1/g_m}{1/g_m + Z_o} \right|^2 = \overline{i_d^2} \left| \frac{1}{1 + g_m Z_o} \right|^2 \tag{4.16}$$

At low frequencies $Z_o \approx r_o$, which makes the noise contribution small. At higher frequncies, $Z_0 \approx 1/j\omega C_{gs}$, which shows that at frequencies approaching the device f_T, the noise contribution increases appreciably.

The stability of cascode amplifiers requires special considerations, particularly due to the high frequency capacitive degeneration on the cascode device due to the output capacitance of the transconductance stage. As shown in Fig. 4.19, the impedance looking into the gate of the top transistor at high frequencies is easily shown to be

$$Z_{in} = \frac{1}{j\omega C_o} + \frac{1}{j\omega C_{gs}} - \frac{g_m}{\omega^2 C_o C_{gs}} \tag{4.17}$$

which means that in order to make the circuit stable, enough resistance must be present at the gate node at frequencies where the input impedance has a negative real part. In practice this can come from a physical resistor or it can be realized through of the losses of the bypass capacitor.

4.3.6.2 Shared-Junction Cascode

To overcome the problems of the cascode device, a shared-junction cascode should be used to improve the mm-wave performance. Shared junction devices are used very commonly in analog circuits to reduce the capacitance of the device. The layout

of such a structure is shown in figure 4.20. The gate of the cascode device needs to be properly biased and should be connected to a low-impedance AC ground. This is done by using a small bypass capacitance to ground, placed as close as possible to the gate of the cascode transistor. Additional low frequency bypass should be provided by a large MOS or MIM capacitor. Fig. 4.21 shows the measured MSG of a 20μm shared-junction nMOS cascode, compared to a common-source transistor. It can clearly be seen that below about 40GHz, the cascode structure achieves a higher power gain. However, at 60GHz, the performance of the cascode device is similar to that of the 20μm regular multi-finger device. Also note that the cascode device is unconditionally stable above 30GHz ($k > 1$)[8].

For the cascode models, a custom large signal model has been developed. For a shared-junction cascode, the substrate is shared by the two devices, which is clearly visible in figure 4.22. Figure 4.23 show a comparison between the measurements and the model of a 40 μm shared-junction cascode device. A good agreement between both is achieved, which validates the modeling approach.

4.3.6.3 A 60GHz Cascode Amplifier with Interstage Matching

The shared-junction cascode still has a non-negligible parasitic capacitance at the interstage node. This capacitance will reduce the gain at higher frequencies, making the cascode less beneficial at mm-wave. This can clearly be seen in figure 4.21. Indeed, at 60GHz, the MSG of the round-table common-source transistor is the same as the MAG of the shared-junction cascode device.

A different approach followed in [23], is to create a cascode structure with two round-table transistors, and to place an interstage matching network between the common-source and the common-gate stage. This circuit combines the excellent mm-wave performance of the round-table layout with the DC current re-use of a cascode topology. This solution also achieves a lower DC power consumption compared to a two-stage cascade amplifier with two round-table common-source transistors. It also achieves more gain for the same DC power consumption when compared to a shared-junction cascode transistor.

Fig. 4.24 shows the simulated MSG and k-factor of a cascode amplifier, composed of two 40 μm round-table devices, with an interstage matching. At 60 GHz, a gain of 11.5 dB is achieved with a DC power consumption of only 6.7 mW. This figure includes the power loss of the interstage matching network. As a comparison, the two-stage cascaded amplifier described in section 4.3.3 achieves a similar gain of 12dB, but at a higher power consumption of 10.4 mW. Also, this compound device compares favorable to a regular shared-junction cascode device that achieves an MSG of 8.5dB for the same power consumption of 6.7mW. Clearly, the current re-use and interstage matching allows one to achieve more gain for a given DC power consumption. The proposed schematic, using this compound cascode device, is shown in figure 4.25.

[8] Portions of this section are taken from [23] (© IEEE 2007)

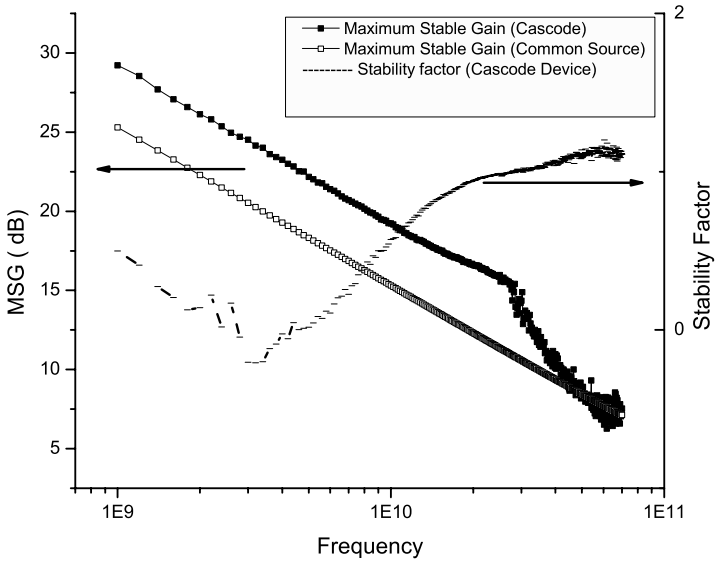


Fig. 4.21 Measured MSG of a 20μm shared-junction cascode and a 20μm round-table common-source device [23] (© IEEE 2007).

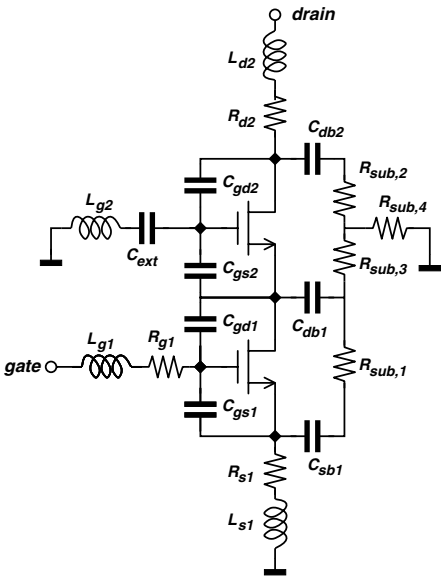


Fig. 4.22 Measurement-based small-signal model of the shared-junction cascode device [23] (© IEEE 2007).

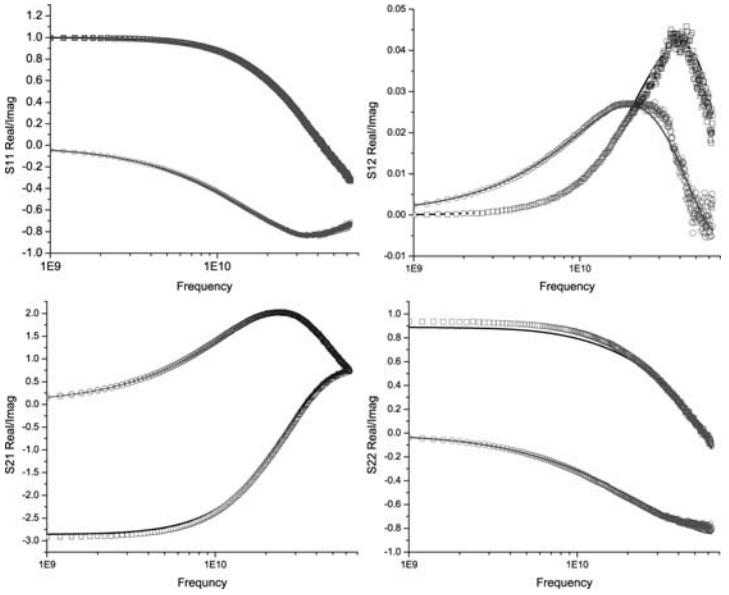


Fig. 4.23 Measured S-parameters versus model of a 40 μm shared-junction cascode device [23] (© IEEE 2007).

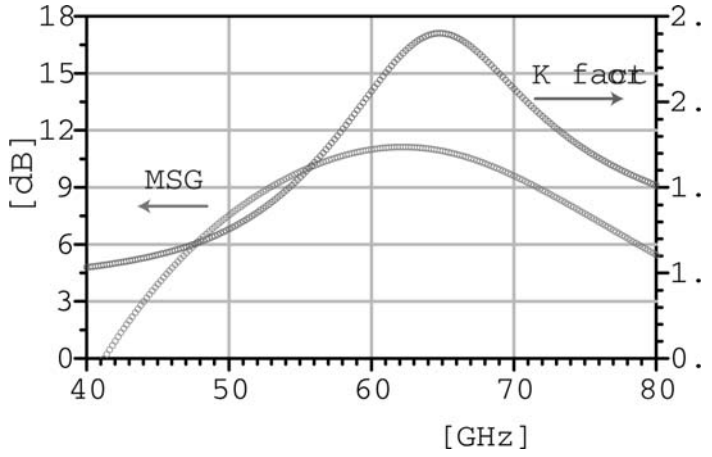


Fig. 4.24 Simulated MSG and k-factor of cascode amplifier [23] (© IEEE 2007).

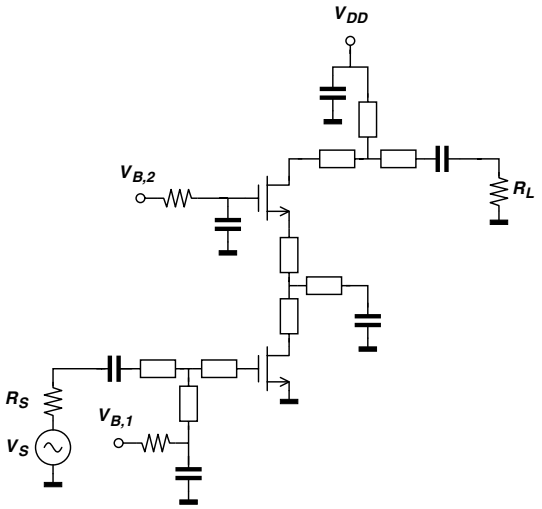


Fig. 4.25 Schematic of the cascode amplifier [23] (© IEEE 2007).

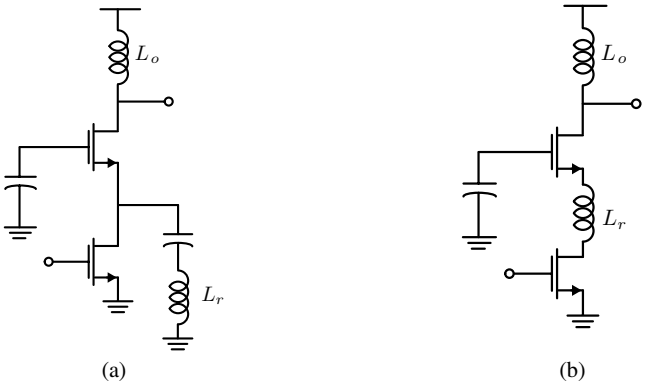


Fig. 4.26 Two techniques to reduce the impact of the cascode shared junction capacitance. Raising this impedance (a) through a resonant LC tank or through a (b) series inductor improves the noise figure of the cascode device.

Similar to previous designs, coplanar transmission lines were used for both input, output and interstage matching.

Another approach is to resonate out the capacitance at the shared junction node, as reported in [24] and shown in Fig. 4.26a. A short section of transmission line or an inductor can be used to realize a low Q resonant circuit around the frequency of interest. An alternative approach is to place a series inductor between the devices, as shown in Fig. 4.26b [25]. This is the preferred way to improve the noise as the technique rejects noise over a broad range of frequencies and is less sensitive to process variations.

4.3.7 A Two-Stage 30 GHz Amplifier

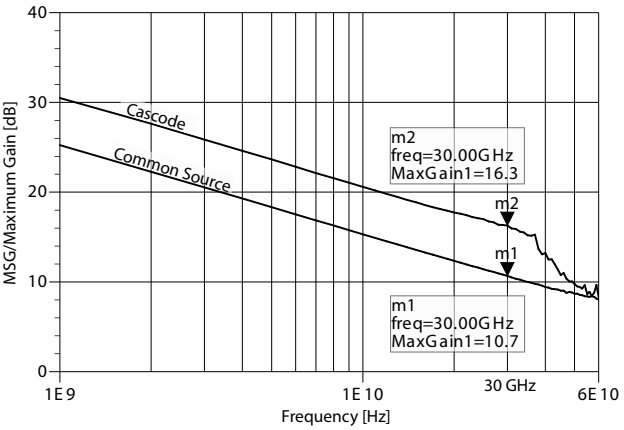


Fig. 4.27 Maximum stable gain for 40μm wide common source and cascode transistors biased at 0.2mA/μm [26] (© IEEE 2007).

A two-stage 30 GHz amplifier was designed in a 90nm CMOS process with the goal of obtaining low noise amplification and unconditional stability, allowing the amplifier to be used as a general purpose building block. A good output compression point is also useful for applications such as an LO buffer[9].

The selection of the active devices is the first critical step. Fig. 4.27 shows maximum stable (MSG) gain plots for 40μm wide round table common source transistor and also a 40μm wide cascode device both biased at 0.2mA/μm which is a good compromise bias point for both high MSG and low NF_{min}. As depicted in the figure at 30 GHz the CS has a MSG=10.7 dB whereas the cascode has a substantially higher MSG of 16.2 dB. The frequency of operation is below the pole of the cascode device results from a compact shared-junction layout discussed previously.

Similar to previous designs, the amplifier uses CPW transmission lines extensively. Coplanar waveguide structure was used rather than microstrip due to higher achievable Z_o. To reduce the conductive losses, two top metal layers were strapped together. A $Z_0 = 51\,\Omega$ was obtained by setting the signal line width to 10μm and gap spacing to 7μm. A typical custom MOM capacitor employed in the design has an area of 25μm $\times$ 25μm and 914 fF of capacitance, with a measured resonance frequency of 41 GHz.

As depicted in the Fig. 4.28, the amplifier consists of two stages. Since a single transistor has a better noise performance over a cascode, the first stage is an amplifier with a single round table transistor. Due to the large gain of the first stage, the noise of the second stage is only of marginal concern and thus a cascode amplifier was placed in the second stage to improve the gain and isolation of the overall amplifier.

[9] Portions of this section are taken from [26] (© IEEE 2007)

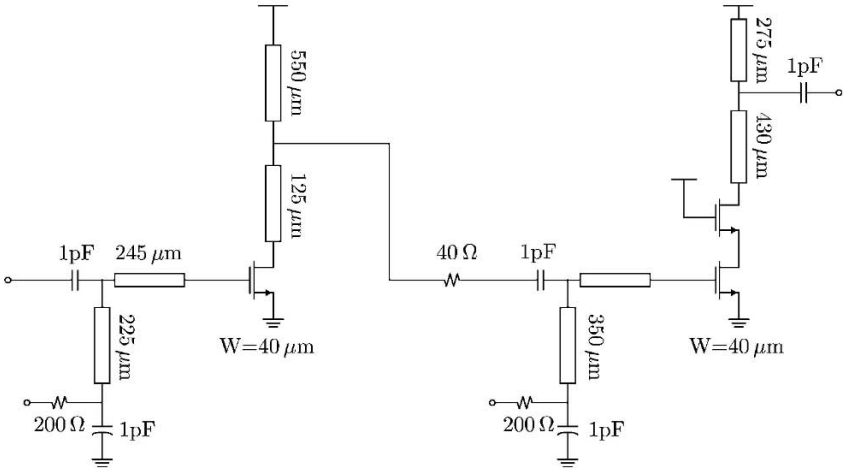


Fig. 4.28 Schematic of the two-stage 30 GHz LNA [26] (© IEEE 2007).

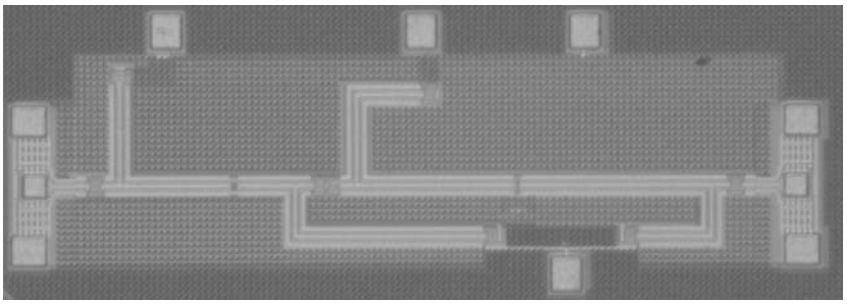


Fig. 4.29 Two-stage 30 GHz amplifier die photo implemented in a 90nm CMOS process [26] (© IEEE 2007).

At 30 GHz the cascode device is not unconditionally stable and therefore to realize a robust and stable amplifier a 40 Ω stabilizing resistor was used in the signal path between the two stages. This resistor lowers the gain but has a little effect on the noise since the first stage has a 12 dB of voltage gain. Due to non-negligible gain at an unwanted band around 5 GHz, 200 Ω resistors were used in the gate bias lines to de-Q the matching network and dampen the gain at 5 GHz.

The fabricated prototype, shown in Fig. 4.29, has been characterized. Measurements were taken directly using wafer probes. The measured S-parameters are shown in Fig. 4.30, displaying good match between measurements and simulation. The amplifier has a peak gain of 20 dB at 28.5 GHz and 3-dB bandwidth from 27.6 GHz to 30.2 GHz. The amplifier is well matched, with input and output return loss better than 15 dB and 20 dB respectively over the 3 dB bandwidth. The large signal and

distortion measurements verify +2 dBm of output power at the 1-dB compression point (input P_{1dB}=-17 dBm) and -7.5 dBm of IIP3.

Noise measurements were performed using the gain method. The input of the amplifier is matched and the output noise power is measured on a spectrum analyzer. The spectrum analyzer noise floor was too high (-140dBm/Hz) for a direct measurement, so a second amplifier module with 28 dB of gain at 30 GHz was used to raise the output noise higher than the spectrum analyzer noise floor (around -127.5 dBm). The noise figure is calculated at a few points across the band and we find the minimum noise figure of 2.9 dB at 28 GHZ (where the gain is close to its peak) and the NF is lower than 4.2 dB over the bandwidth of the amplifier (Fig. 4.31a). The amplifier consumes 16.25 mW of power from a 1V supply voltage. The current is nearly evenly divided between the stages. Linearity is satisfactory for a 1 V design (Fig. 4.31b).

4.4 Mixers and Frequency Translation

Mixers are key components of an RF front-end, translating the IF signal to a carrier frequency for transmission and from an RF carrier back down to IF for detection. Mixers can be categorized into two families, active and passive mixers. Active mixer have power gain whereas passive mixers have insertion loss. Each mixer essentially modulations either the transconductance of an amplifier or the resistance of a switch to produce the mixing action through time-varying mechanism. The devices are usually modulated with a large LO signal to maximize the conversion gain. At mm-wave frequencies it is very difficult to get a large LO power out of a silicon devices, especially with CMOS technology. Even though the device non-linearity will produce mixing products even with a weak LO, the conversion gain is too small when mixers are operated in such a fashion. Hence, the conversion gain and noise figure requirements must be obtained at a reasonable LO power level ($\sim$0 dBm). Also the design goal of low-noise, together with mm-wave modeling difficulties, limits the use of complex mixer topologies.

4.4.1 Single Transistor Mixers

Single-gate GaAs FET mixers with good conversion gain and noise figure have been used successfully for mm-wave applications [28]. The use of standard CMOS for single-gate mixers at mm-wave range has been explored in [27] where we reported a 60 GHz quadrature-balanced single-gate mixer implemented in a main stream CMOS technology.[10].

[10] Portions of this section are taken from [27] (© IEEE 2005)

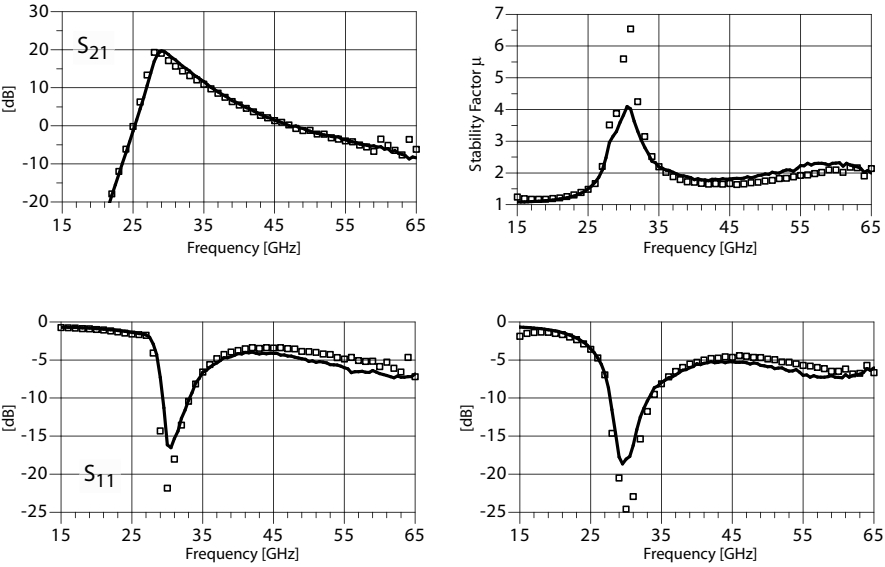


Fig. 4.30 Measured and simulated S-parameters and stability factor μ of two-stage 30 GHz amplifier [26] (© IEEE 2007).

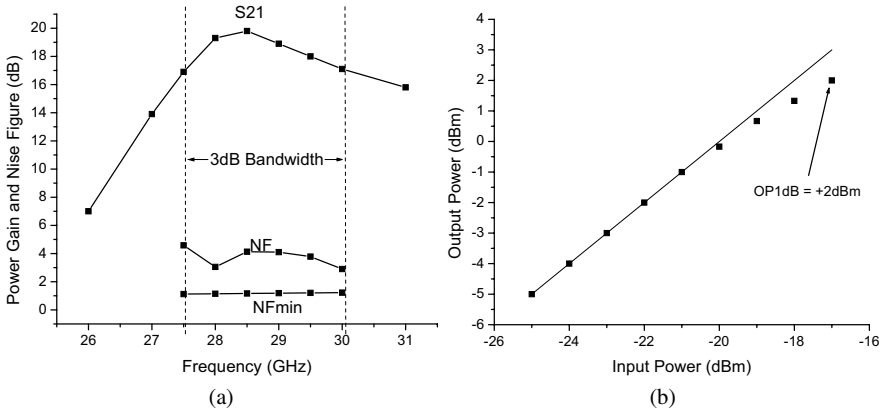


Fig. 4.31 Measurements of two stage 30 GHz amplifier (a) noise figure and (b) compression characteristics [26] (© IEEE 2007).

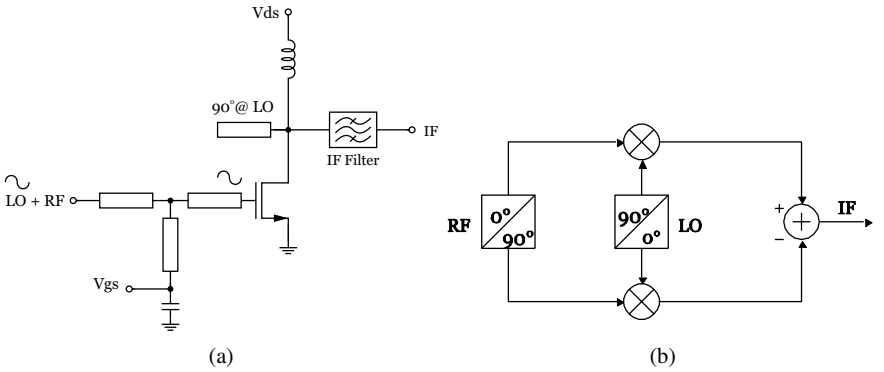


Fig. 4.32 (a) Simplified single-gate mixer. (b) Quadrature balanced architecture [27] (© IEEE 2005).

A simple single-gate mixer architecture is shown in Fig. 4.32a. It is a transconductance mixer, as the time-varying $g_m(t) = g_m(t + T_{LO})$ of the common-source stage is the main source of frequency conversion. The LO signal, applied at the gate of the transistor together with the RF signal, varies the g_m around the dc bias point, and therefore modulates the RF gain of the common-source stage and consequently provides frequency conversion.

For a standard CMOS process, as shown in Fig. 4.33, the region close to the threshold voltage exhibits a steep change of transconductance vs. the gate-source voltage. The large LO signal can efficiently modulate the g_m of a transistor biased in this region. Moreover, by choosing the bias point close to V_T, minimal dc power consumption is achievable. Using only one common-source NMOS transistor promises a good noise figure at mm-wave frequencies. Also, because the mixer is effectively a common-source device, it is very easy to model with a simple transistor structure.

Single-gate mixers have one major practical implementation problem: they require a hybrid or elaborate power combining circuit to combine the LO and RF signals. Typically the hybrids are bulky, and their insertion-loss adds directly to the mixer's noise figure. Fortunately, due to the high frequency of operation at 60 GHz, the hybrid can be easily integrated on-chip. Also, by using a balanced architecture, as shown in Fig. 4.32b, better spurious response and LO noise rejection can be obtained [29].

The quadrature balanced mixer that consists of two unit single-gate mixers, and a 90° branch-line hybrid is shown in Fig. 4.34. The mixer was designed to down-convert from the nominal RF frequency of 60 GHz to a low-gigahertz IF of 2 GHz using a 58 GHz, 0-dBm LO. In this particular CMOS process, choosing a gate source voltage, V_{GS}, slightly above the threshold voltage, V_T, of the $80 \times 1\,\mu\text{m}/0.13\,\mu\text{m}$ device maximizes the fundamental frequency component of g_m. The nonlinear device model was then used in ADS harmonic balance simulations to estimate the optimum large-signal matching impedances for the gate at 60 GHz for this bias point. By taking advantage of the intrinsic device capacitances, it is possible to provide the

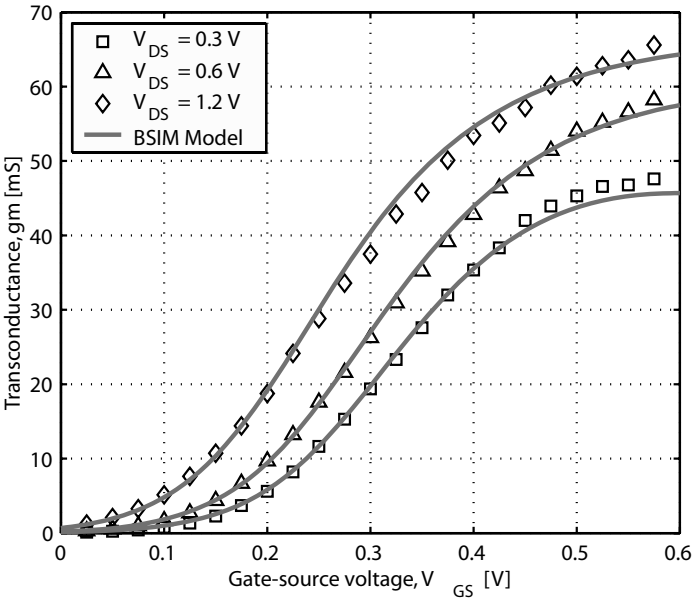


Fig. 4.33 Measured and modeled g_m versus V_{GS} [27] (© IEEE 2005).

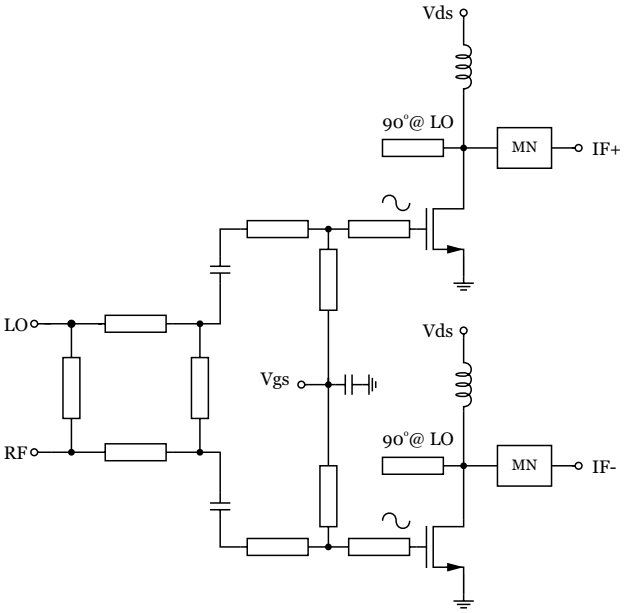


Fig. 4.34 Simplified circuit diagram of the single-gate quadrature balanced mixer [27] (© IEEE 2005).

required 90° phase shift by using transmission lines shorter than $\lambda/8$. This significantly reduces the insertion-loss and the physical size of the hybrid. The IF matching network consists of on-chip lumped LC components. At 2 GHz, a quality factor of 7 was measured for the main spiral inductor.

Simulations accounting for parasitics indicate that the core of the NMOS single-gate mixer is only conditionally stable up to 60 GHz due to the large Miller capacitance. Short-circuiting the drain node at mm-wave frequencies breaks the feedback loop (through C_{gd}) and improves the stability. Using an open quarter-wave stub is a popular and practical technique. Moreover, suppressing the LO at the drain minimizes the variation of drain-source voltage V_{DS}, and consequently minimizes the performance degradation due to other nonlinear elements such as C_{db} and g_{ds}.

The nonlinear device model described in Section 3.2.4 along with the transmission line electrical models were implemented in ADS environment. The harmonic balance and small-signal simulators along with an optimizer were used to fine tune the transmission line lengths and optimize the performance of the mixer. From the simulations, a SSB noise figure of 11.5 dB is expected for the mixer (RF=60 GHz, IF=2 GHz, PLO=0 dBm).

The mixer was fabricated using a 6-metal layer, 130-nm digital CMOS process, and the chip area is 1.6×1.7 mm^2, including pads. The die photo of the fabricated mixer is shown in Fig. 4.35. All the measurements were taken on wafer by using GSG probes on a Cascade Summit probe station. Fig. 4.36a shows the conversion gain of the mixer for different LO power levels. The RF frequency is 60 GHz, the IF frequency is 2 GHz, and the RF input power is -25 dBm. Conversion loss of better than 2 dB was achievable for a low LO power of 0 dBm.

The RF and LO frequencies were also varied to obtain the frequency characteristics of the mixer for fixed IF frequency of 2 GHz and LO power of 0 dBm. As shown in Fig. 4.36b, the 3-dB RF bandwidth of the mixer is more than 6 GHz. Fig. 4.37a shows the small-signal input return loss of the mixer. The center frequency is slightly below the targeted frequency, but there is still better than 15-dB return loss at 60 GHz. The LO-RF leakage performance, shown in Fig. 4.37b, is adequate for typical mm-wave receiver systems as additional isolation comes from the LO buffer and multi-stage LNA. The measured input-referred 1-dB compression point is -3.5 dBm. Power consumption is only 2 mA from a 1.2-V supply.

4.4.2 Dual Gate Mixers

The “dual-gate" mixer, shown in Fig. 4.38, consists of a cascode transistor driven by the RF signal at the input stage and the LO signal at the cascode stage. Since the LO and RF ports do not need to be combined, this mixer is more compact than a FET mixer discussed above. The transconductance of the input device is modulated by the LO signal, which alters the drain to source voltage. The LO bias effectively modulates the S_{21} of the cascode device, producting a time-varying transconductance stage. The input stage is biased in saturation but near the triode region, where the sensitivity

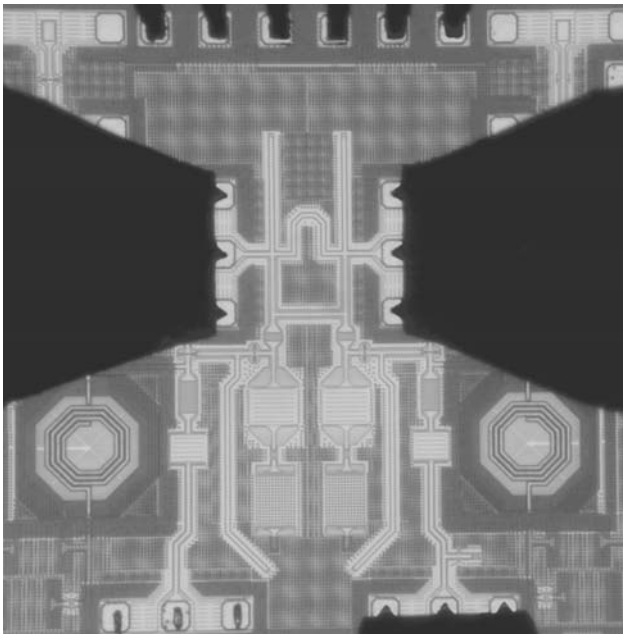
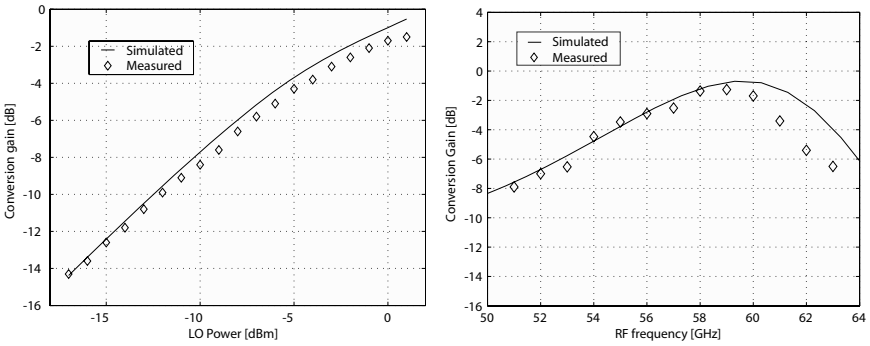


Fig. 4.35 Chip photo of single-gate quadrature balanced mixer [27] (© IEEE 2005).



(a) (b)

Fig. 4.36 Single gate quadrature balance mixer results. (a) Mixer conversion gain vs. LO power (RF = 60 GHz, IF = 2 GHz, VGS = 200 mV, PRF = -25 dBm). (b) Conversion gain vs. RF frequency (IF = 2 GHz, VGS = 200 mV, PRF = -25 dBm, PLO = 0 dBm) [27] (© IEEE 2005).

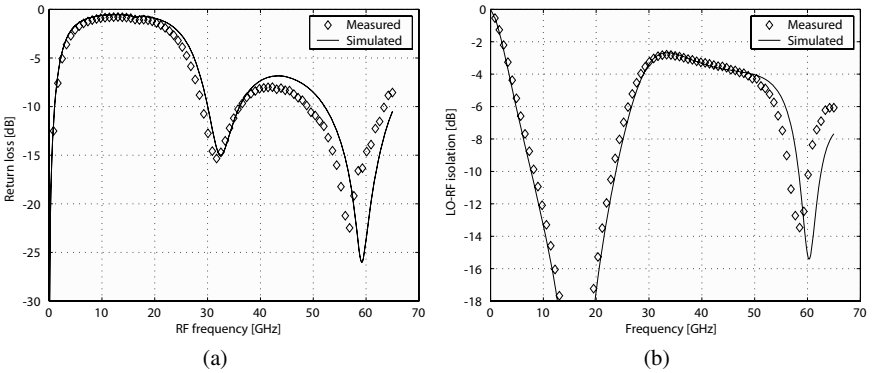


Fig. 4.37 Single-gate quadrature balanced mixer measurement results. (a) Input return-loss frequency characteristics. (b) LO-RF isolation frequency characteristics [27] (© IEEE 2005).

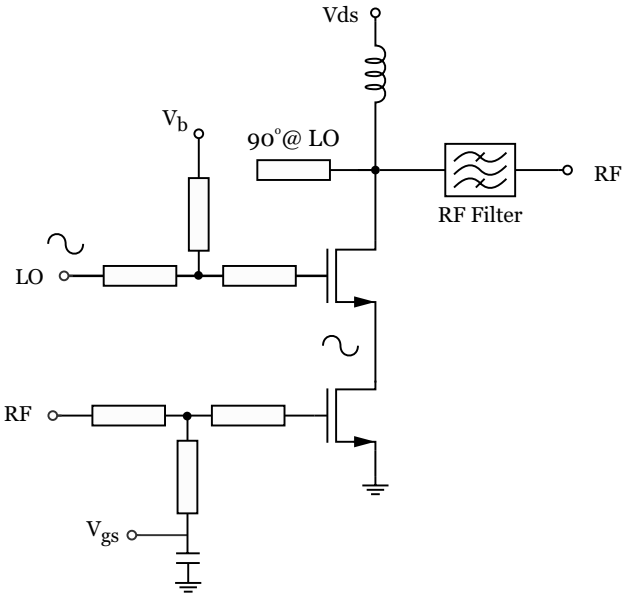


Fig. 4.38 A “dual gate" mixer is implemented in standard CMOS technology with a cascode configuration.

of the transconductance is maximized. This also has a side benefit of reducing the power consumption of the mixer. The RF and LO ports are matched to 50 Ω through co-planar transmission lines. The LO signal is matched at 40 GHz and the RF is matched at 60 GHz. The DC bias stub shorts the LO leaking into the RF, and an LO stub likewise shorts the RF signals at the LO port. This results in good isolation and improved stability. An IF filter is designed at 20 GHz for further processing of the signal. Since the LO and RF signal are widely separated, the image signal at 80 GHz is of little concern, and it is naturally filtered by the LNA and mixer passband response.

A layout of the mixer in 130nm technology appears in Fig. 4.39. The chip area is 0.8 mm × 1.5 mm. The measured performance has better than 3 dB conversion loss for an LO power of 0 dBm. The input referred 1-dB compression point is -4 dBm, with a return loss better than 15 dB at 60 GHz. Simulations indicate a noise figure of 12.5 dB. In summary, the dual gate mixer provides high LO-RF isolation, conversion gain, and obviates the need for a combiner. Even though the common source transistor is operated in the linear region to maximize the sensitivity of the transconductance to drain voltage, the cascode transistor acts as an IF amplifier. The stability of the design is carefully controlled by providing a reactive termination at the gate of the common gate transistor and through careful device modeling.

4.4.3 Gilbert Cell Mixers

Differential Gilbert cell type mixers are commonly used at RF frequencies but have several problems at mm-wave frequencies. The use of differential circuits is more risky because the core transistors are used as full three-port devices, including the influence of the body-effect due to the non-grounded source. Since most devices are characterized as two-ports with a common ground, one must rely more on the model rather than the measurements to employ devices in this configuration.

Consider a simple Gilbert-cell type single-balanced structure using a single-ended RF input to drive the Gm-stage and a differential switching stage for frequency conversion, shown schematically in Fig. 4.40. For example, the RF drive is at 60 GHz and LO modulation is at 58 GHz. The down converted 2 GHz IF signal is coupled through an output balun and finally a source follower is used to drive the 50 Ω output. The differential side of the output balun also serves as a high impedance load for the mixer. In a fully integrated mixer, the output balun can be omitted if a fully-balanced IF stage VGA is employed.

The mixer uses a resonant tuning network at the drain of the transconductance stage to resonate out all the parasitic at that node. At high frequencies the parasitics at that node will shunt the signal to ground resulting in signal attentuation. By adding the tank, one can recover a significant amount of conversion gain.

A single-turn coupled inductor structure is used for realizing the high frequency balun. Conventionally, at microwave frequencies “rat-race" couplers or distributed structures are used for single-ended to differential conversion. While transmission

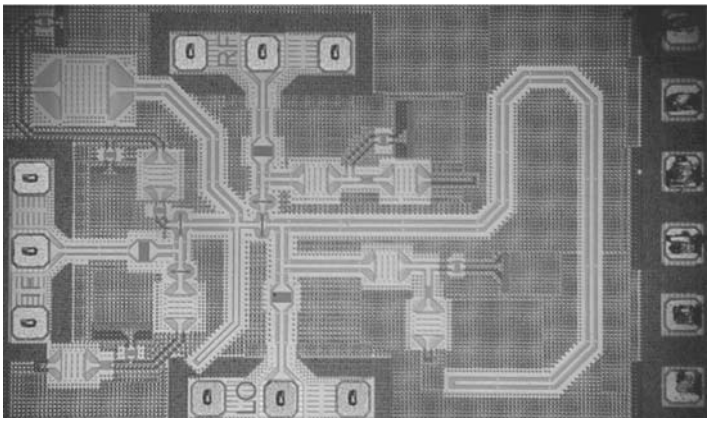


Fig. 4.39 Layout of 130nm CMOS “dual-gate" mixer.

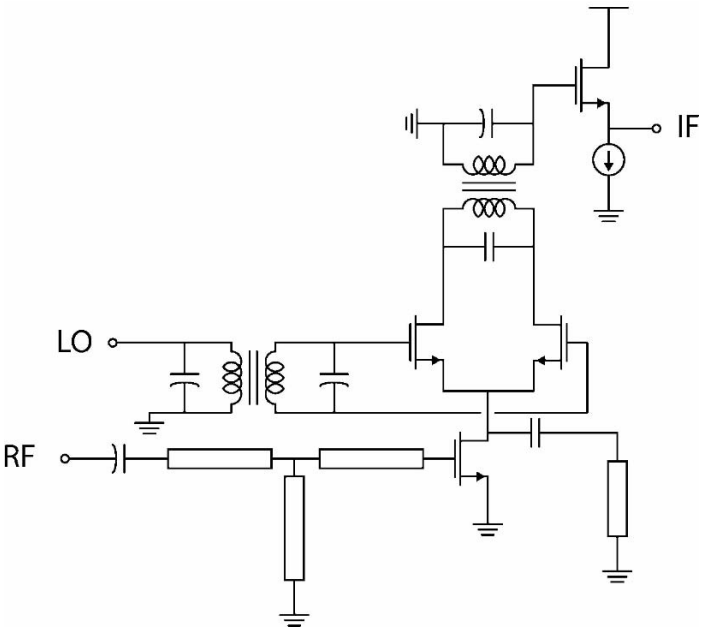


Fig. 4.40 Schematic of a single-balanced Gilbert cell mixer.

line couplers are very effective and offer good phase and amplitude balance, they are bulky (see Fig. 4.35). For example a “rat-race" balun needs arms spanning a quarter wave length. At 60 GHz in the Si substrate/oxide, this length is about $600\,\mu m$, resulting in very large balun and relatively high insertion loss. A loop inductor based

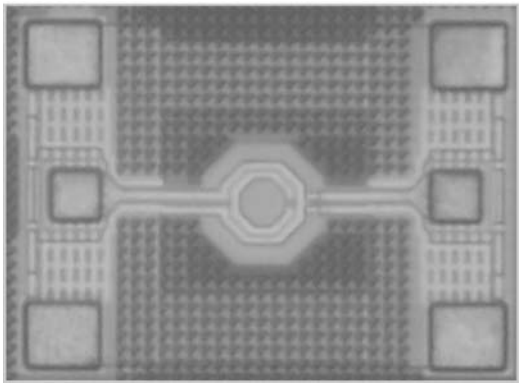


Fig. 4.41 Layout of a coupled ring transformer (die photo).

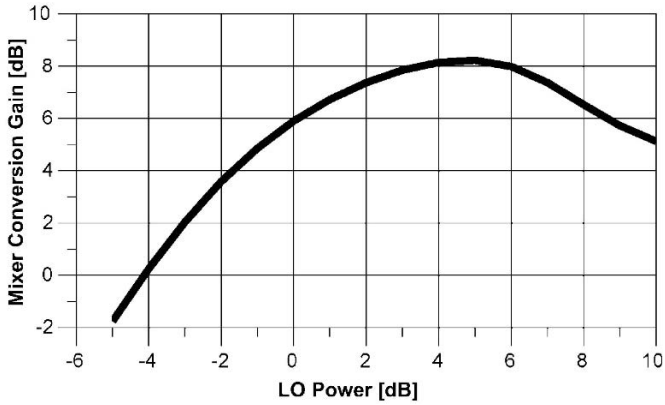


Fig. 4.42 Conversion gain of Gilbert cell mixer versus LO power (dBm).

balun uses arms of length 24μm and is realized in the area of the order of $80\times80\mu\text{m}^2$ and shown in Fig. 4.41.

In order to optimize and design the balun, the minimum insertion loss, related to the quality factor and coupling factor of the windings. For a bi-conjugate match, the transformer minimum insertion loss is given by [30]

$$IL_{min}(Q,k) = 1 + \frac{2}{Q^2k^2} - 2\sqrt{\frac{1}{Q^4k^4} + \frac{1}{Q^2k^2}} \tag{4.18}$$

Using this metric an optimal structure with a single turn and appropriate metal width and spacing has been designed. The tranformer balun has an insertion loss of 1 dB while providing a match at the LO port, maximizing the LO swing.

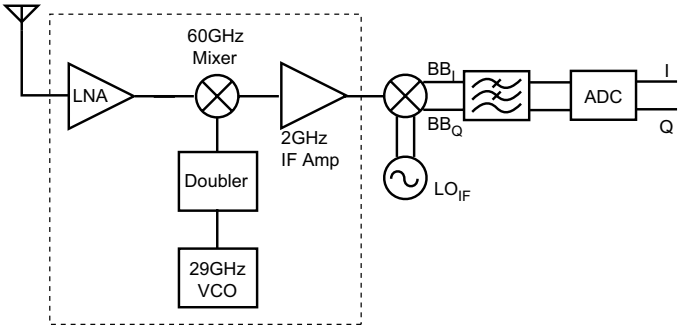


Fig. 4.43 Block diagram of a 60 GHz front-end implemented (red) in 130nm CMOS [31] (© IEEE 2007).

The simulated performance of such a mixer has 7 dB conversion gain, a linearity of iIP3 = -5 dBm, and a power consumption of 7 mW. The LO port needs to be driven with an LO power of 2 dBm to saturate the conversion gain. By increasing the LO power, the conversion gain increases up to a point and then drops, as shown in Fig. 4.42. In practice an LO power beyond 4 dBm is impractical and most likely the LO power will be around 0 dBm. The drop in gain is due to the change in operating point of the transconductance device due to operation in the triode region.

4.5 Examples of Integrated Front-Ends

4.5.1 CMOS 130nm 60 GHz Front-End

A highly-integrated 60 GHz CMOS front-end receiver consisting of an LNA, a quadrature balanced down-converting mixer, a 30 GHz VCO, and a frequency doubler, shown in Fig. 4.43. Individual circuit blocks were also fabricated to characterize their performance separately. The front-end is fabricated in a 130-nm standard digital CMOS technology, which has a substrate resistivity of 10 Ω-cm and 6 layers of metalization. Transit frequencies (f_T) and maximum frequencies of oscillation (f_{max}) of 85 GHz and 135 GHz, respectively, have been reported for NMOS devices in this process [17].[11].

The LNA topology consists of three stages of cascode devices with input, output, and interstage reactive matching, as shown in Fig. 4.44. Cascode transistors, used in order to reduce the Miller capacitance and improve stability, are biased at 150 $\mu\mathrm{A}/\,\mu\mathrm{m}$, and the MAG is 6.0 dB at 60 GHz per stage. CPW transmission lines are used extensively in the design for impedance matching, interconnect wiring, and the bias networks. All lines are kept as short as possible to minimize losses. Since the

[11] Portions of this section are taken from [31] (© IEEE 2007)

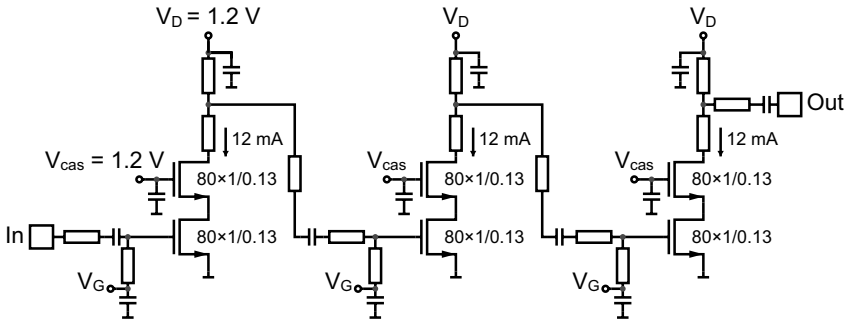


Fig. 4.44 Simplified schematic of the 60 GHz 3-stage amplifier using CPW transmission lines [31] (© IEEE 2007).

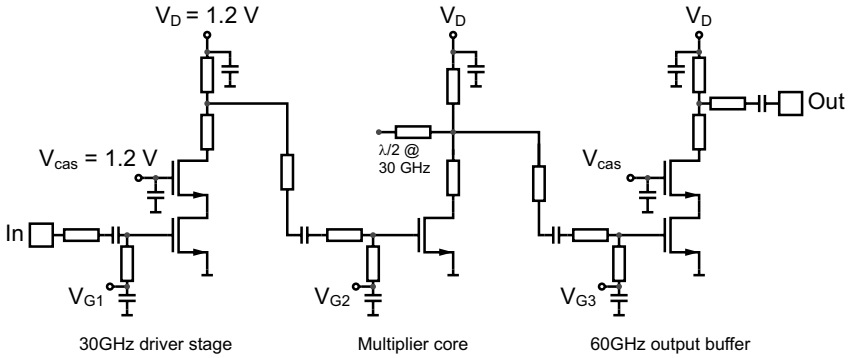


Fig. 4.45 Simplified circuit diagram of the frequency doubler [31] (© IEEE 2007).

integrated LNA output does not need to drive a pad or be matched to an off-chip 50 Ω load, it is matched directly to the input of the quadrature mixer, providing higher performance than the standalone amplifier reported in [17].

The quadrature balanced down-converting mixer described in Sec. 4.4.1 consists of two unit single-gate mixers, and a 90° branch-line hybrid. The mixer was designed to down-convert from the nominal RF frequency of 60 GHz to a low-gigahertz IF of 2 GHz using a 58 GHz, 0-dBm LO. The simplified schematic of the 3-stage frequency doubler is shown in Fig. 4.45. It consists of a 30 GHz input driver, the core multiplier, and the 60 GHz LO buffer. Cascode devices with input, output, and interstage reactive matching were used to implement the input driver and output buffer stages. The second stage is the frequency doubling stage. A common-source NMOS transistor is biased close to the threshold voltage to efficiently generate a second harmonic component. Therefore, the doubler can be considered as a half-wave rectifier. A combined matching network and fundamental frequency rejection filter at the drain of this transistor supports the generation of the 60 GHz component and rejects the 30 GHz input component. A standalone version of the doubler, matched to the off-

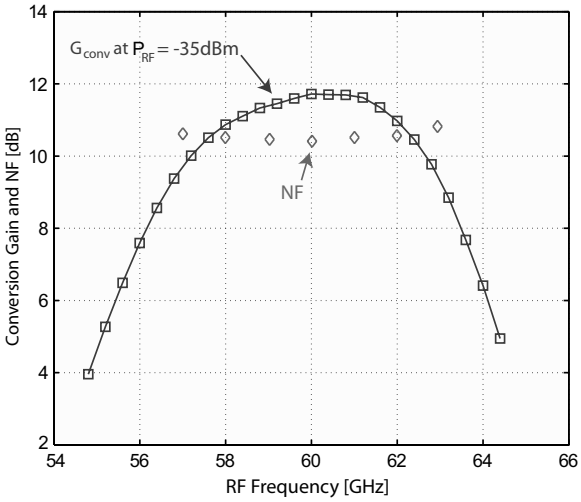


Fig. 4.46 Measured conversion-gain and NF of the integrated front-end [31] (© IEEE 2007).

chip 50Ω input (at 30 GHz) and output (at 60 GHz) with pads, is implemented and characterized separately. A -6-dBm, 29 GHz input signal is applied to the doubler and a conversion gain of the multiplier of 7.2 dB is measured at 58 GHz. The 3-dB bandwidth at this input power level is from 53 GHz to 62.5 GHz. The fundamental frequency at he output of the doubler is >35dB down. The doubler alone consumes 2 mA while the input and output stages consume 8 mA and 12 mA respectively.

A 28.4-29.4 GHz Pierce VCO is designed to generate the input signal to the frequency doubler . The stand-alone implementation of the VCO provides -3dBm output power to a 50Ω load at 29 GHz. The measured phase noise is around -93 dBc/Hz at 1 MHz offset. The integrated version of the VCO with the doubler is fabricated separately. The integrated VCO/doubler block provides 2 dBm output power at 58 GHz and the measured phase noise is -86 dBc/Hz at 1MHz offset.

Fig. 1.6 depicts the die photo of the integrated front end. The chip area is about $7\,\mathrm{mm}^2$ including pads. On-wafer measurements were performed using a Cascade Microtech probe station. An Anritsu 37397C VNA was used for S-parameter measurements. The input return loss at the RF port is better than 15 dB. Fig. 4.46 shows the conversion characteristics of the front-end with conversion gain of 11.8 dB at 60 GHz. The RF and LO frequencies were varied to obtain the frequency characteristics of the mixer for fixed IF frequency of 2 GHz. To obtain a broadband frequency characteristics, another fabricated version of the front-end with an external 30 GHz LO was used. The 3 dB RF bandwidth of the mixer is about 6 GHz. The measured input-referred 1-dB compression point of the front-end is -15.8 dBm at 60 GHz. Noise figure (NF) measurement of the integrated front-end was performed using a Millitech WR-15 noise source, WR-15 waveguide probes, and an Agilent N8973A NF measurement system. The measured NF of the downconverter is shown in Fig. 4.46. The

NF is 10.4 dB at 60 GHz. The total power dissipation of the integrated front-end is 64 mA from a 1.2 V supply.

4.5.2 SiGe Transceiver Chipset

A 60 GHz transceiver [14] has been realized in SiGe BiCMOS-8HP (0.13-μm) technology. A block diagram of the two-chip transceiver chipset is shown in Fig. 4.47. A dual-conversion superheterodyne radio architecture is selected over a homodyne approach due to its lower carrier feed-through in the transmitter and better IQ quadrature accuracy. The variable intermediate frequency (IF) frequency plan for the radio is based on a single 16 to 18 GHz local oscillator (LO) which is tripled to generate a 48 to 54 GHz LO for the mm-wave mixers or divided by two to provide a 8 to 9 GHz LO for the IF mixers. With an 8 to 9 GHz IF, the image frequency for the superheterodyne is 16 to 18 GHz below the RF frequency, which is sufficiently low enough to allow for low-Q on-chip image filters. Finally, the 16-18 GHz LO frequency results in a simpler frequency synthesizer design, since no high-frequency dynamic dividers are required. Also, the tuning-range and phase-noise requirements can be more easily met in a voltage controlled oscillator design at 18 GHz than at 54 GHz.

The receiver (Rx) chip begins with the image-reject low-noise amplifier from section 4.3.2, followed by a single-balanced Gilbert-cell mixer. This mixer provides about 9 dB of conversion gain with a cascaded upper single-sideband NF of 13 dB at 25°C (mixer + following stages). Following the mm-wave mixer is a variable-gain IF amplifier (IFVGA), which provides between -10 and +10 dB of gain. IF filtering is provided by tuned R-L-C loads at the mixer output and the IFVGA output. The IF signal is downconverted to baseband frequency through a pair of quadrature double-balanced Gilbert-cell mixers with unity gain. Following the IF mixers are unity-gain baseband output buffers to drive external 100 Ω differential loads. A harmonic frequency tripler generates the mm-wave LO signal at 48-54 GHz, while a standard emitter-coupled logic divide-by-two circuit provides the 8-9 GHz LO signal. Finally, the PLL is a type-II fourth-order PLL operating from a 520 to 610 MHz reference clock, and generating a 16.6 to 19.5 GHz output signal.

A die photograph of the Rx is shown in Fig. 4.48. The die size is 3.4×1.7 mm^2 to the outside of the pad frame. The LNA is at the lower left, and the spiral inductors in the Rx mixer and IFVGA are visible to the right of the LNA. The frequency tripler is in the center, and the PLL occupies the right third of the chip. The chip contains $>$ 300 NPNs, $>$ 1000 FETs, and $>$ 90 transmission lines and inductors.

On-wafer measurements were made on the full Rx with PLL. As shown in Fig. 4.49, at 25°C, the Rx power conversion gain is 38 to 40 dB and the NF is 5 to 6.7 dB. The image rejection is 30 to 40 dB, IIP3 is -30 dBm, and input P_{1dB} is -36 dBm, all shown in Fig. 4.50. The Rx consumes 195 mA from 2.7 V, 50 mA of which is in the baseband output buffers. At 85°C, NF remains below 8 dB while gain drops 5 to 6 dB relative to 25°C. The Rx and Tx PLL measurements show a VCO

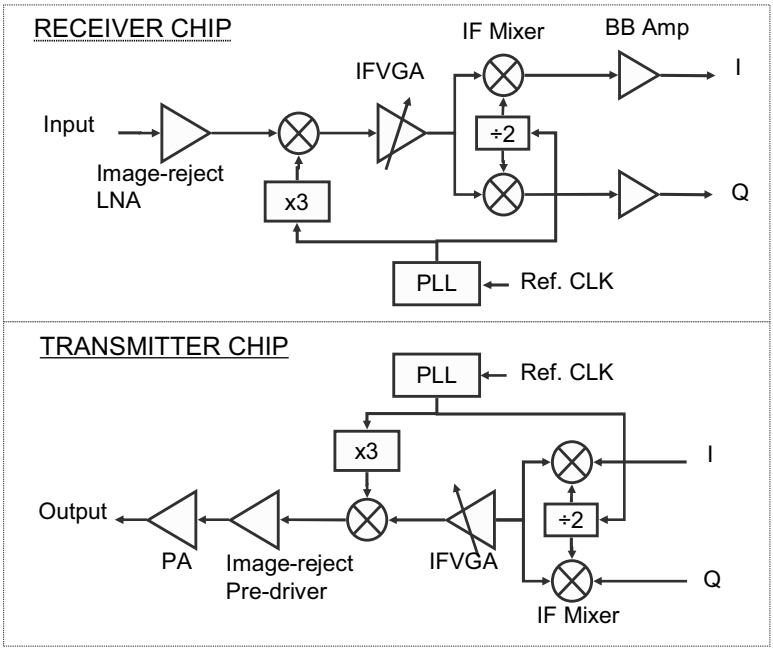


Fig. 4.47 Block diagram of 60 GHz transceiver chipset implemented in 0.13-μm SiGe BiCMOS technology [14] (© IEEE 2006). Dual-conversion superheterodyne architectures are used in both the receiver and transmitter.

phase noise of -115 to -120 dBc/Hz at 10-MHz offset with an RMS jitter less than 1.5° integrated over 0.1-1GHz. Additional receiver measurements are summarized in Table 4.2.

Table 4.2 Summary of measured receiver performance

Metric	**Measured Value**
Frequency Range	59-64 GHz
Gain	38-40 dB
Noise Figure	5-6.7 dB
S11, RF in	-15 dB
Image Rejection	$>$ 30 dB
P_{1dB} (in)	-36 dBm
IIP3	-30 dBm
Phase Noise (1MHz), tripled	-85 to -90 dBc/Hz $<$ -130 dBc/Hz floor
I/Q Balance	0-4 degrees, $<$1 dB
Power Dissipation	195 mA, 2.7 V

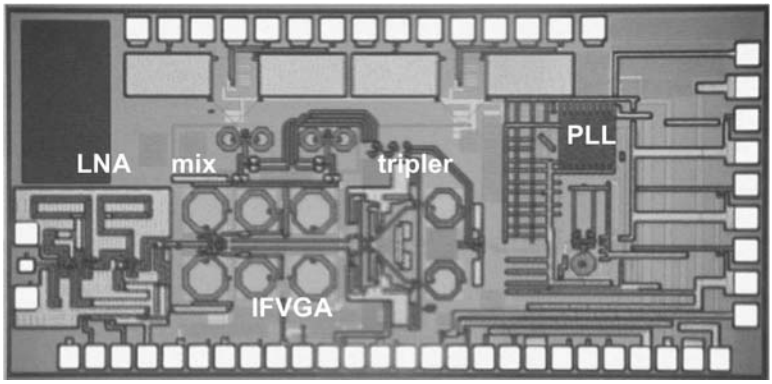


Fig. 4.48 Die photograph of 60 GHz receiver. The die size is 3.4 x 1.7 mm^2 [14] (© IEEE 2006).

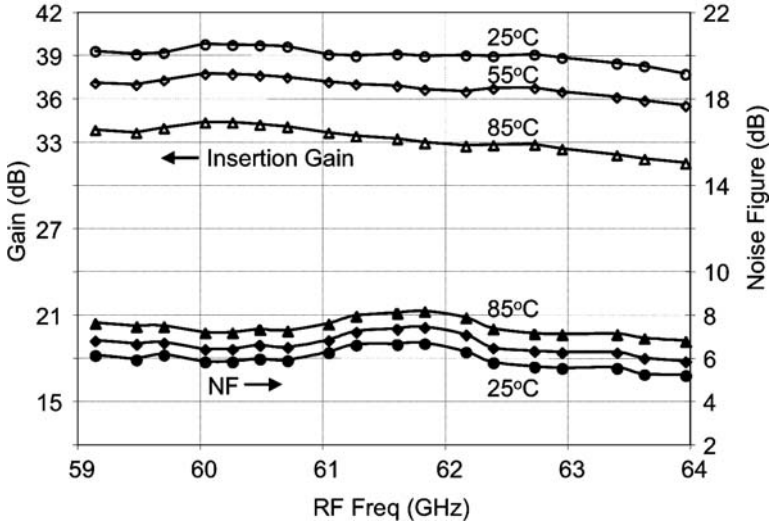


Fig. 4.49 Measured conversion gain and noise figure over temperature of 60 GHz receiver [14] (© IEEE 2006).

Referring to the block diagram in Fig. 4.47, the transmitter (Tx) chip includes a PA, an image-reject driver, an IF-to-RF upmixer, an IF amplifier strip, a quadrature baseband-to-IF mixer, a PLL, and a frequency tripler. The PA provides 15 dB of gain with 10.5-dBm P_{1dB} and 17-dBm P_{sat}. The image-reject driver provides 8-12 dB of gain, 6-8 dBm output P_{1dB}, and >25 dB image rejection. Finally, the IF and LO paths in the transmitter are the reverse of that in the receiver.

A die photograph of the Tx is shown in Fig. 4.51. The die size is 4.0 $\times$ 1.6 mm^2. The PA and the differential output pads are on the left, adjoined to the right by the

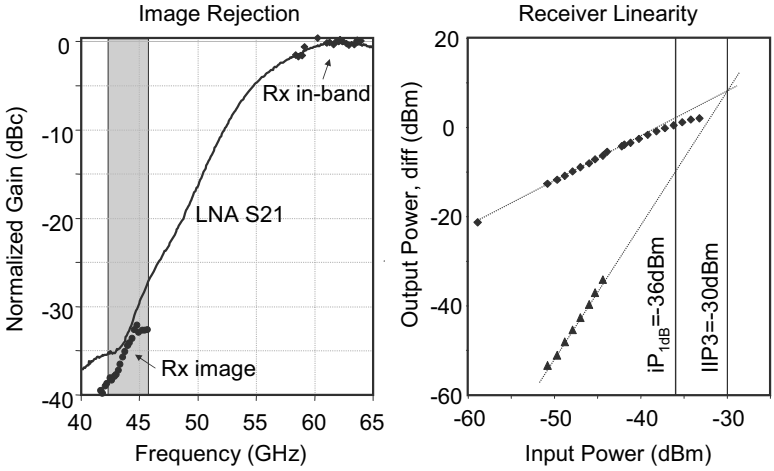


Fig. 4.50 Measured image rejection and linearity of 60 GHz receiver [14] (© IEEE 2006).

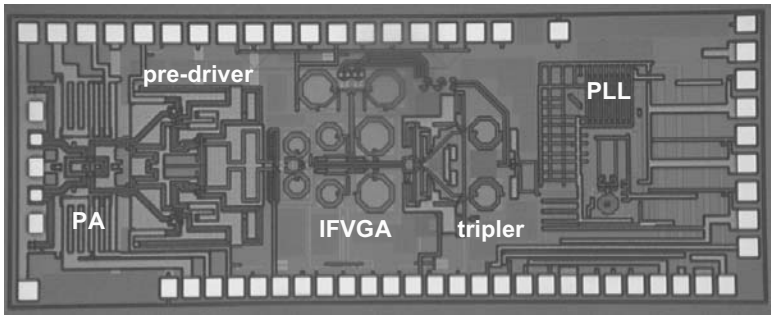


Fig. 4.51 Die photograph of 60 GHz transmitter. The die size is 4 x 1.6 mm^2 [14] (© IEEE 2006).

pre-driver, IF-to-RF mixer, IFVGA, and frequency tripler. The PLL occupies the right third of the chip, and the baseband-to-IF mixer contains the two spiral inductors at the top center. The Tx chip contains $>$ 300 NPNs, $>$ 1000 FETs, and $>$ 170 transmission lines and inductors.

On-wafer measurements were performed on the full transmitter with PLL. The Tx conversion gain is 42-36 dB. Fig. 4.52 shows the measured output power and conversion gain versus I/Q input power of a 100-MHz CW tone for three different bands (59, 61.5, and 64 GHz). P_{1dB}(out) is 10 to 12 dBm, while P_{sat} is 16 to 17 dBm, and the conversion gain is 34 to 37 dB. Across the temperature range from 5 to 85°C, P_{1dB} remains constant while gain drops 7 dB, as shown in Fig. 4.53. The spurious response of the Tx has been measured in 500-MHz steps across the band. At -25 dBm input power, which is near the P_{1dB}, 20 to 30 dB of image suppression, 20 to 25 dB of carrier suppression, and 20 to 25 dB of sideband suppression are observed. The

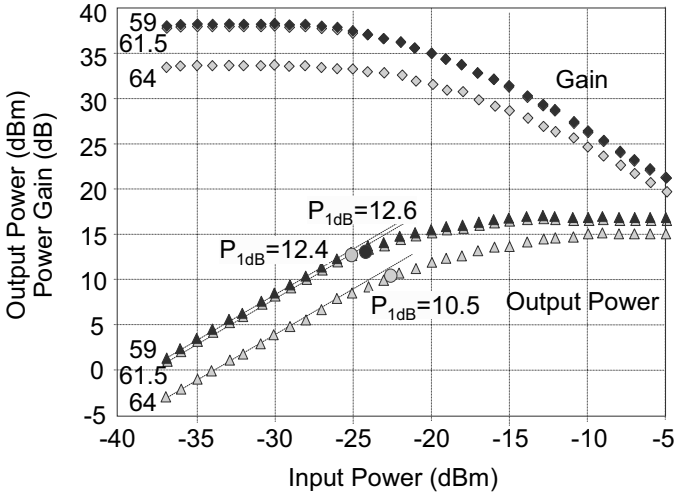


Fig. 4.52 Measured power gain and output power of transmitter [14] (© IEEE 2006).

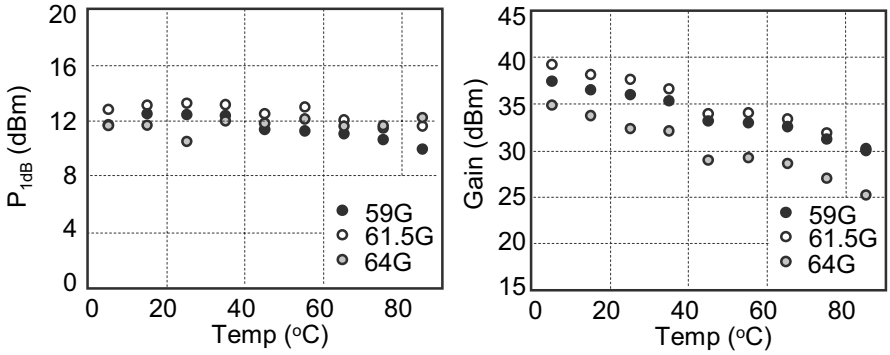


Fig. 4.53 Measured gain and output power of transmitter over temperature [14] (© IEEE 2006).

spur from 3×LO feedthrough is $<$ -20 dBm. With no DC offset correction applied, the external I/Q quadrature accuracy is within $\pm 2^{\circ}$. At P_{1dB}, the Tx consumes 190 mA from 2.7 V and 72 mA from 4 V (PA). Table 4.3 summarizes the Tx measured performance.

In summary, a highly-integrated receiver and transmitter chipset for data communications in the 60 GHz ISM band has been demonstrated. The Rx NF is approximately 6 dB and the Tx output P1dB is 10-12 dBm, with provides ample link budget for many applications. Robust performance is maintained at 85°C. The 500 mW Rx and 800 mW Tx power consumption, combined with the wide available bandwidth at 60 GHz, means that data can be transmitted with good energy efficiency, which is

Table 4.3 Summary of transmitter receiver performance

Metric	Measured Value
Frequency Range	59-64 GHz
Gain	34-37 dB
P_{1dB} (out)	10-12 dBm
P_{sat}	15-17 dBm
Image Rejection	20-30 dB
Carrier Suppression	21-25 dB
3xLO Spur	-25 to -20 dBm
Phase Noise, (1MHz) tripled	-85 to -90 dBc/Hz
	$<$ -130 dBc/Hz floor
I/Q Balance	$\pm$2 deg, $\pm$0.5 dB
Power Dissipation	190 mA, 2.7 V
	72 mA, 4.0 V

desirable for battery-operated devices. The chips are architecturally flexible enough to work with a range of modulation formats.

4.6 Conclusion

Basic communication building blocks such as low-noise amplifiers and down-conversion mixers have been discussed extensively in this chapter. Many of the considerations given here apply directly in the design of other building blocks involving gain and frequency translation. Using core building blocks such as transmission lines, capacitors, and transistors, the design is relatively straightforward and similar to RF design techniques. Transmission lines are more prominent due to the length scalable reactance and better predictability of ground currents. Compared to RF design, though, mm-wave gain stages have much less available gain, requiring matching networks to trade-off between gain, noise figure, and linearity. For the same reason, stability considerations are much more important due to the reduced isolation in amplifiers. Since gain cannot be sacrificed for stability, the matching networks must be carefully designed to avoid instability over process and temperature. The layout and design of cascode gain stages, the workhorse of RF amplifiers, also requires rethinking due to the role of the second high frequency pole of the amplifier cascade. Layout and tuning techniques were discussed to circumvent these problems. Several mixers designs were highlighted, such as a single gate mixer, a "dual gate" mixer, and a classic Gilbert cell mixer. Due to the low gain of the transconductors at mm-wave frequencies, the choice between the Gilbert cell mixer and other topologies is not obvious. Several simple mixers were highlighted which offer modest conversion loss and good linearity. Finally, case studies of the design of complete building blocks in CMOS and SiGe are provided to illustrated the achievable performance for silicon technology.

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