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Design Kit and Technology Training

BiCMOS8HP

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Preface

The BiCMOS8HP Technology and Design Kit Training book includes the following training sections/modules:

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Design Verification Tools

PEX Flows

Digital Library

The **IBM SiGe Technologies** section gives an introductory view of the IBM SiGe technologies. Comparison of the key aspects of the different SiGe technologies is also provided.

The **Technology Overview and Device Library** section consists of the active and passive devices available in the design kit for circuit design. For each device, pertinent performance parameters, its cross-section, layout view and a CDF (Component Description Form) property form are illustrated. This gives designers a quick overview of the device. A brief summary of the technology features, 8HP process cross-section and available metal stacks are included. Unique Millimeter Wave devices information are also included in the *bicmos8hp* PDK. Modeling information about each device class is also provided in this section except for the NPN and FET sub-circuit features that is included in the Models and Simulation section. In addition, some support pcells that are needed to complete the designs e.g., image/chip guard ring, crackstop, bondpad, etc., and that the designers should be familiar with are also described. Information about which devices can be placed under the pads for compact layouts is also provided.

The **ESD Protection and esd8hp Library** section includes the available ESD devices in the design kit as a tutorial on ESD protection. The ESD device pcells are mostly macros. Macro pcells are hierarchical that require use of a skill utility, IBM_PDK → ESD that is included in the design kit. The BiCMOS8HP Design Manual has detailed information about the ESD devices including the TLP (Transmission Line Pulse) measurement data. Using this section in conjunction with the Design Manual is expected to provide the requisite ESD design support for the designers.

The **Models** part of the **Models and Simulation** section provides the overview of the sub-circuit features of the NPN and FET models. This section includes only a very small subset of what is in the BiCMOS8HP Model Reference Guide. For detailed information, please see the

BiCMOS8HP Model Reference Guide. The **Simulation** part of the **Models and Simulation** section provides an overview of the supported simulators, how to set up the simulators, and how to account for the manufacturing process variations – both Monte Carlo and Fixed/Custom Corners in the designs. In addition to "Fixed (digital)" corners which are typically employed to analyze delays through digital circuits for timing closure, IBM provides many "Custom (fixed analog)" corners that a designer can judiciously use for analog functions thereby reducing the long Monte Carlo simulations. For simulation, the BiCMOS8HP design kit provides the Hspice and the Spectre models.

The **Layout Topics** section provides an overview of the BiCMOS8HP Design Manual and a series of layout topics including the ground rules that may not be obvious, such as, antenna rules and pattern density considerations. We describe floating gate, copper dendrite, the necessity of PCI marks, the techniques for noise minimization, proper use of substrate contacts and latchup prevention, proper layout techniques to achieve optimum device matching, and prevention of electromigration failure and unsatisfactory voltage drops through adequate sizing of conductors. At the end, we also include a few additional layout techniques for compact layouts including yield enhancement.

The **Design Kit Overview** section includes the procedure for downloading the BiCMOS8HP base design kit and "Add-On" components. The base design kit includes only the Assura DRC and LVS decks. The parasitic extraction deck Assura QRC is an "Add-On" component. It is downloaded in the same directory structure as the base design kit (/IBM_PDK/<technology>/<rel>/), however, this Add-On component has to be subscribed separately. The digital library and any IBM IP (Intellectual Property) are also regarded as Add-On components. Procedures are illustrated about creating/attaching library properties, version migration, implicit and explicit schematic entry representations, substrate methodology, multiplicity and some of the utilities provided in the design kit, such as, gds data streaming, parameter checks when migrating to a newer version etc. Designer is advised to go through the cdslib Release Notes. This section is only a small subset of it.

The **Design Verfication and PEX Flows** sections list the supported DRC, LVS and PEX tools. Designers should work with their tool vendors for running them. We only provide sample procedures for running these tools. Documentation in the tool subdirectories have associated Release Notes that list the tool version used to verify them and any known limitations.

The **Digital Library** gives an overview of the standard cell digital library, IOs and any other IP available. IBM ports digital library and other IP from IBM's Cu-11 ASIC libraries. If the designer needs a specific IP that may assist in the design, please contact your IBM Field Application Engineer (FAE) Alternately you can email at fdrytech@us.ibm.com.

Lastly, the **BiCMOS8HP Technology Training and Design Kit Training** book does not serve as a replacement for the Design Manual, the User Guide or the Model Reference Guide rather it explains each topic in a high level manner and constitutes a handy reference guide. Please

consult the Design Manual, the User Guide, or the Model Reference Guide for the technical reference. *For ease of readability, some material has been intentionally duplicated.*

Electronic Design Automation (EDA) tools and technology offerings change with time. Readers may find out the latest availability of EDA tools and Technology Features by sending inquiries to IBM at fdrytech@us.ibm.com.

Furthermore, reader has access to the various technical topics such as the application notes, the design submission guidelines etc., available on the ICC. Please visit the ICC website and use the technical library to user advantage.

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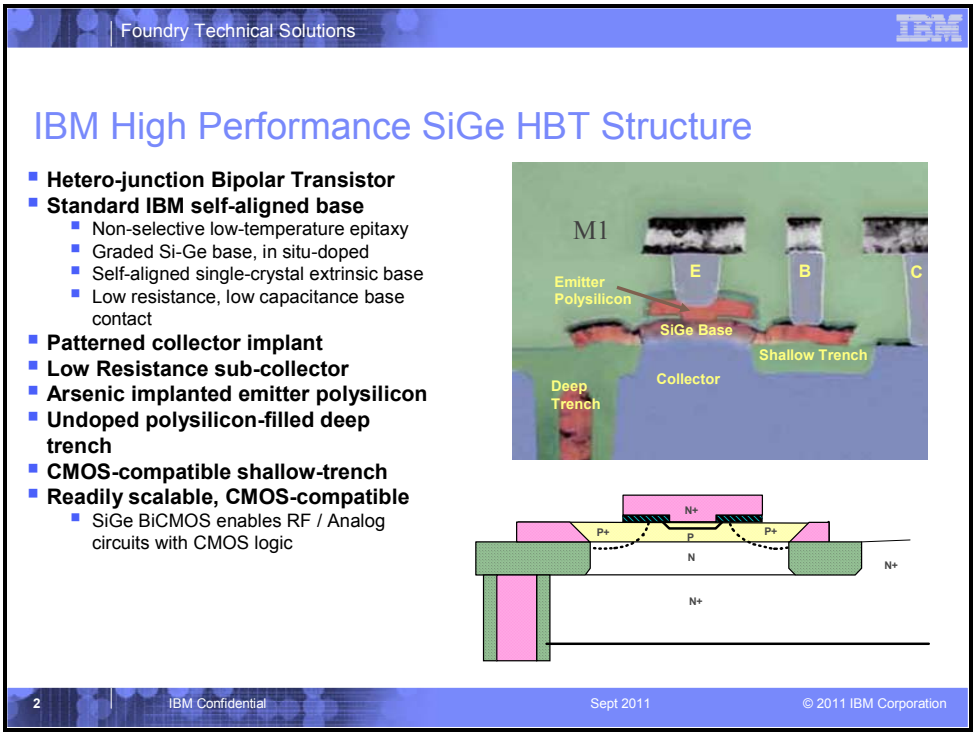
September 2011

Introduction to IBM SiGe Technologies

This section provides a brief introduction to IBM SiGe technologies. For more extensive background, please refer to either of the texts below and references there-in.

"Silicon-Germanium Heterojunction Bipolar Transistors" by John D. Cressler and Guofu Niu, Artech House, 2002

"Silicon Germanium, Technology, Modeling, and Design", by Raminderpal Singh, David L. Harame, and Modest M. Oprysko, IEEE Press, 2004

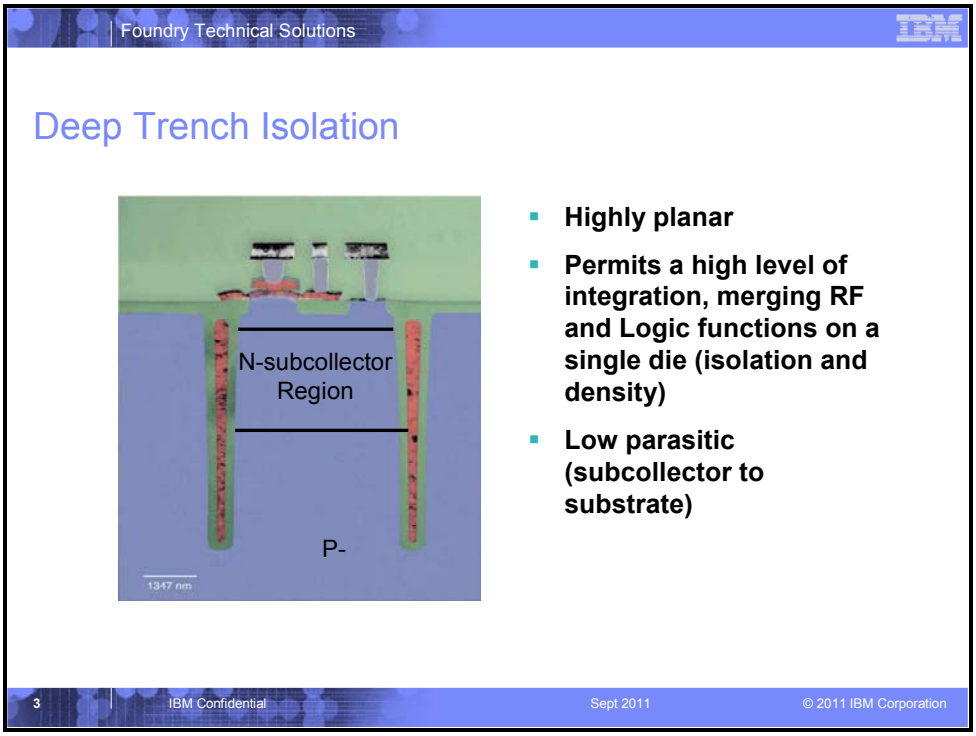


IBM High Performance SiGe HBT Structure

The high performance SiGe hetero-junction bipolar transistor (HBT) is shown in the cross-section above. This cross-section is from BiCMOS 6HP. Other HP technologies have similar structures. The emitter is self-aligned to the base region, with the extrinsic base implant offset from the active emitter-base junction by spacers. Non-selective low temperature epitaxy is employed to form the graded germanium content in the base, which is in-situ doped. The extrinsic base region is single crystal where formed over the silicon of the collector region, and is poly-crystalline over the oxide of the trench regions. The extrinsic base is heavily doped and is silicided for low base resistance. The base region is contacted over shallow trench which reduces the base to collector parasitic capacitance.

A patterned collector region is used, allowing for different collector doping levels for a trade-off of breakdown voltage and performance, discussed in later slides. A low resistance sub-collector is formed deeper in the silicon for low parasitic resistance.

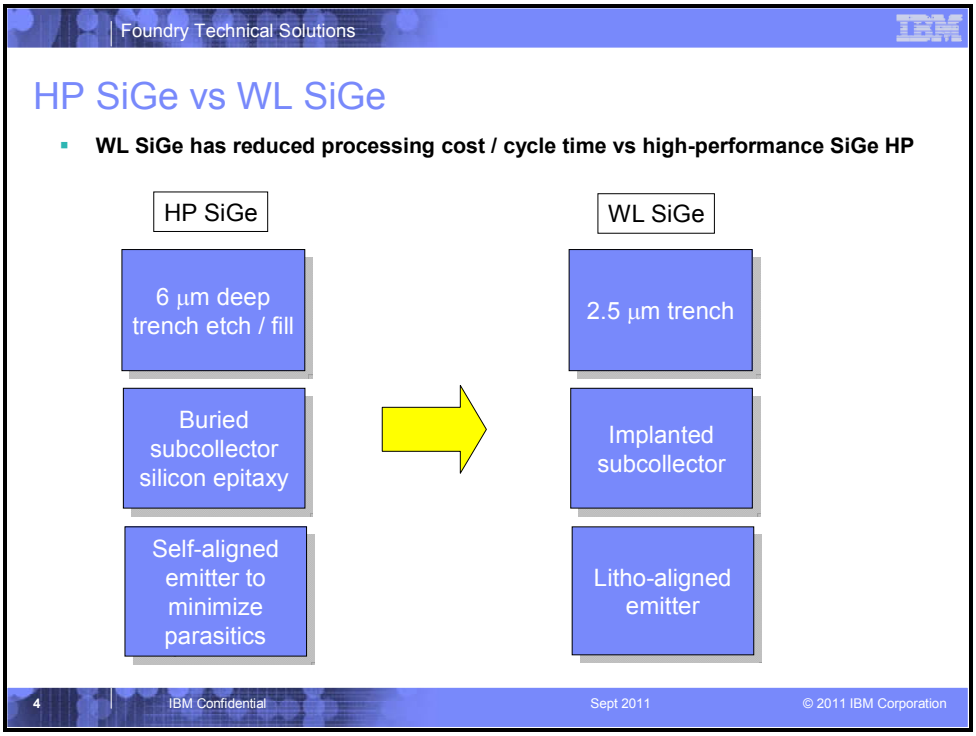
The high performance SiGe technologies use both deep trench and shallow trench isolation. The technologies are designed to enable integration of high performance CMOS devices with the SiGe HBT devices.



Deep Trench Isolation

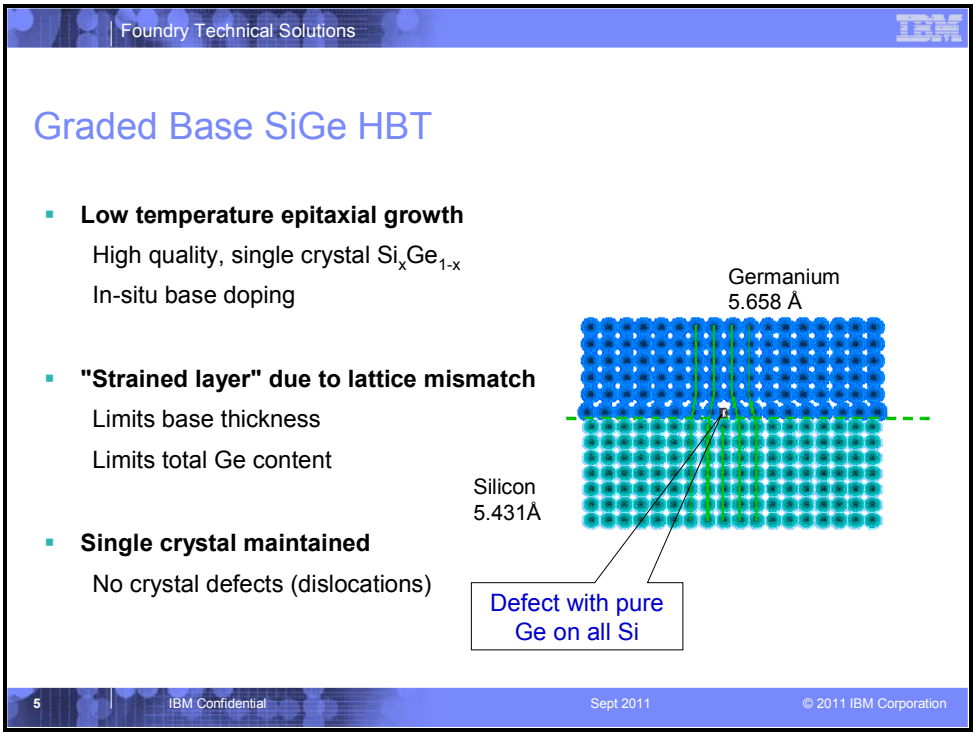
A requirement of modern integrated circuit processes is to maintain a highly planar surface, to enable the photolithographic imaging of subsequent mask levels. Note in the slide above, the contacts to the emitter, base and collector are all different heights, but the surface is planarized prior to contact etch and the subsequent metal one processing.

The HP technologies utilize a 6.0 µm deep trench to form the sidewall isolation from the n-type collector to the p- substrate. The trench is partially filled with oxide (green in the slide) and then the fill is complete with an intrinsic polysilicon. The heavily-doped n-subcollector is formed early in the process by implantation and subsequent epitaxial growth of silicon above. The deep trench minimizes the perimeter capacitance from collector to substrate. The area component of collector to substrate capacitance is minimized by the light p- substrate doping.



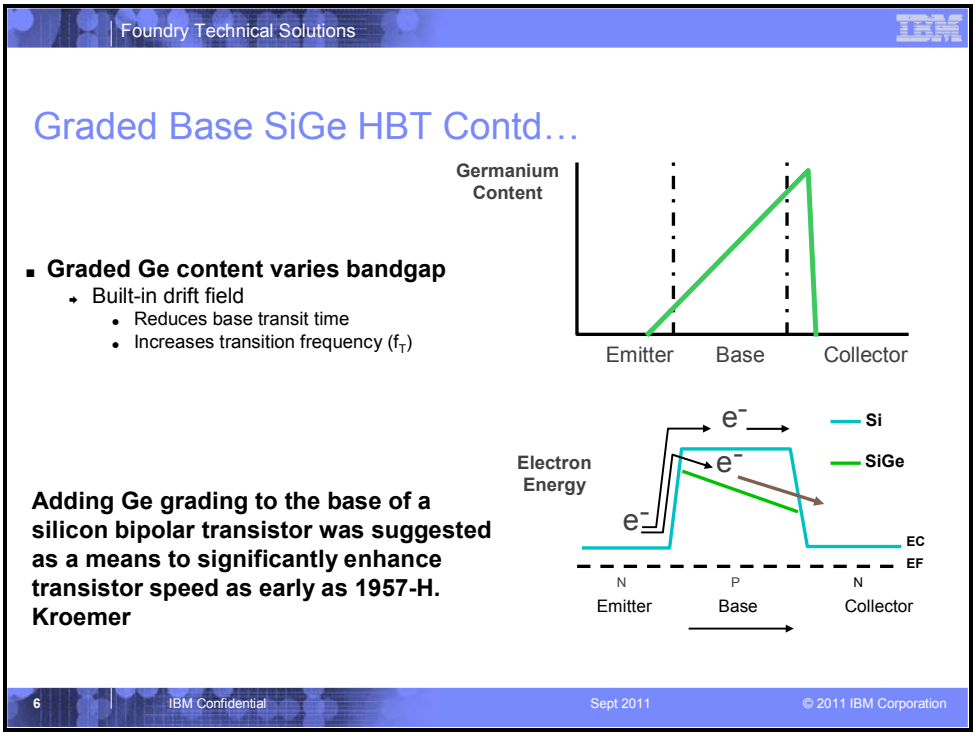
HP SiGe HP vs WL SiGe

Compared to the HP SiGe, the WL SiGe technologies have several cost-performance trade-offs built in to the process. Instead of the 6µm deep trench in HP, the WL utilizes a 2.5µm trench formed later in the process. The WL trench is filled with oxide rather than oxide and polysilicon in HP. The WL sub-collector is implanted from the surface, reducing the processing cycle time by not including the silicon epitaxial step present in the HP technologies. Additionally, process complexity is reduced by having the emitter alignment to the base defined by well-controlled photo-lithography, instead of the self-aligned HP process.



Graded Base SiGe HBT

The IBM SiGe HBTs use a graded concentration of germanium in the low temperature epitaxial base growth with in-situ p-type doping. The result is a high quality single crystal Si_XGe_{1-X} film. The base is a strained layer, due to the intrinsic difference in lattice constant between silicon (5.431Å) and germanium (5.658Å). Growth of strained layers places a limit on the film thickness and total germanium content before relaxation and the formation of crystal dislocations. The base layer is a thin film, and is scaled thinner each generation for device performance; the SiGe HBT is scalable for device performance advantages.

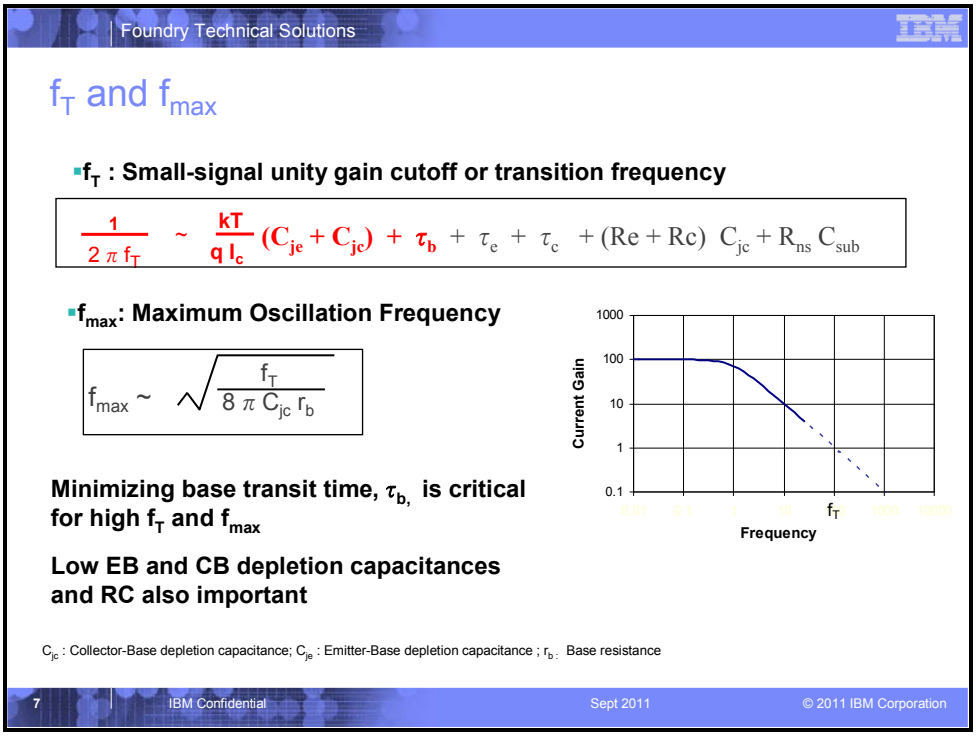


Graded Base SiGe HBT Contd…

The addition of Germanium to Silicon results in a lower bandgap, approximately 74meV for 10% Ge content. For the p+ base of the SiGe HBT npn, the Ge grading will show up in the conduction band. For a higher Ge content at the collector junction, the slope of the conduction band is such that it acts as an accelerating field for the minority carriers in the base, and electrons will move rapidly across the base due to this drift field. It is this "bandgap engineering" of the IBM SiGe HBT, with the resulting accelerating drift field which reduces the base transport time, that is key to the improved device speed compared to all silicon homo-junction bipolars.

In a homojunction silicon bipolar transistor, electron transport across the base is primarily by diffusion, a relatively slow process. In fact, in most silicon bipolar processes, the base region is formed by implantation, and the gradient in doping concentration across the base actually results in a somewhat retarding field for electrons.

The graded Ge concentration also improves current gain and "Early" voltage (output conductance) compared to a Silicon homojunction transistor, discussed towards the end of this module.

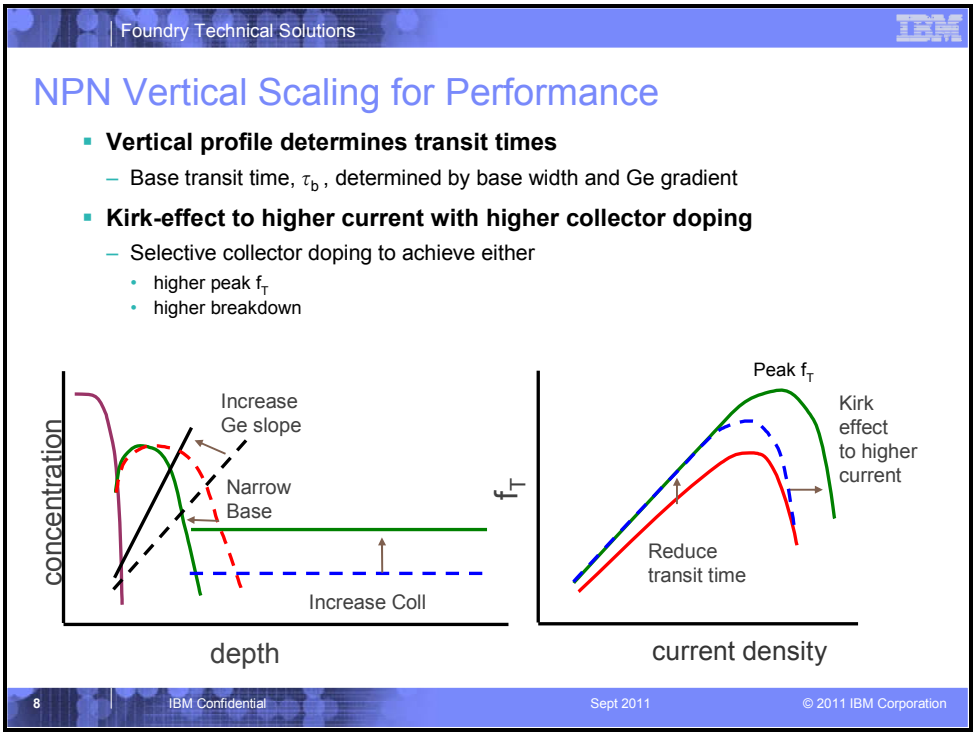


f_T and fmax

Transition frequency, f_T, is defined as the frequency for which the current gain extrapolates to unity. The equation in the slide is the approximate relationship for f_T which holds for low current density. The intrinsic transconductance, g_m, is qI_c/kT, and Cje and Cjc are the emitter-base and base-collector depletion capacitances. Increasing collector current increases f_T proportionally. Reducing the base transit time, τ_b, results a direct improvement in transition frequency at a given value of I_c. It is the base transit time that is reduced by the graded concentration of germanium in the base of the IBM SiGe HBT.

Also of importance for high f_T in the low injection (low Ic) region of operation are the emitter charge storage delay time (τ_e), collector transport time (τ_c), the emitter and collector resistances (R_e and R_c), the subcollector resistance (R_{ns}) and the collector to substrate capacitance, C_{sub}.

The maximum oscillation frequency, f_{max}, is often a more important parameter than f_T as a performance measure in real circuits. At f_{max}, the maximum power gain extrapolates to unity. Transition frequency f_T is independent of the base resistance, since it is dependent on current gain, but low base resistance is critical for high f_{max} and low noise factor. Two factors enable reduction of base resistance in SiGe HBTs in comparison to silicon homojunction transistors. First is the in-situ base doping during the base epitaxial growth allows for a more heavily doped base region. Second, the valence band offset due to the Ge content at the emitter base junction allows the base to be more heavily doped without significant impact to the emitter injection efficiency. This allows for a trade-off of low frequency current gain (β) versus base resistance not feasible in silicon homo-junction bipolar transistors.

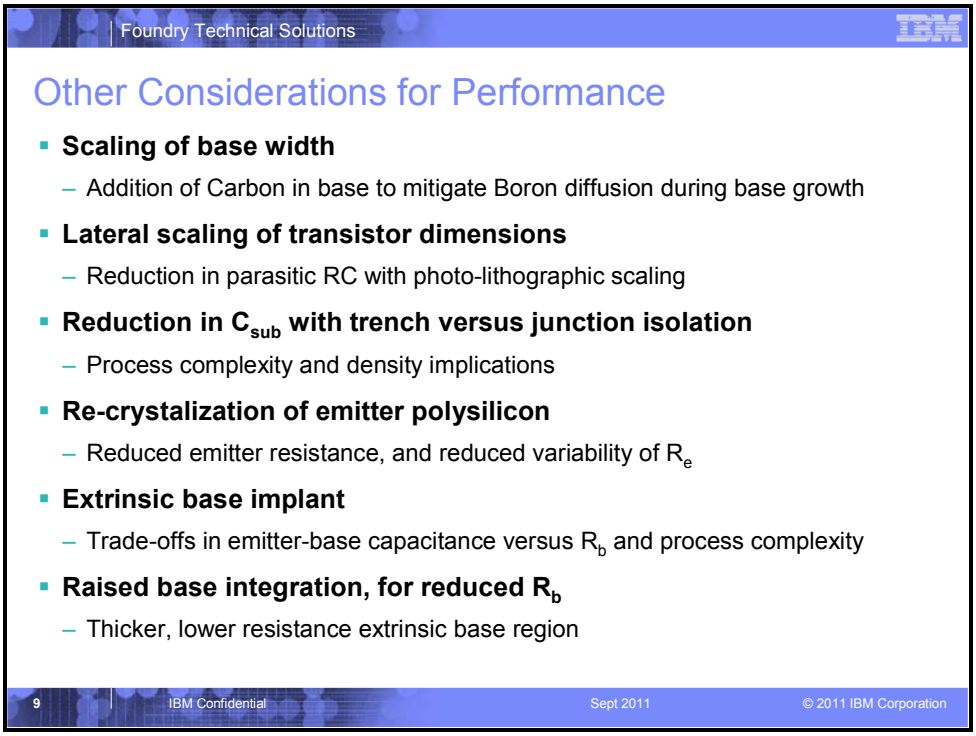


NPN Vertical Scaling for Performance

The vertical profile is dominant in setting the performance of an npn transistor. The base transit time is determined by the base width (how far electrons must travel from emitter to collector) and, in the case of a SiGe HBT, the Germanium gradient across the base (the electric field accelerating the carriers across the base).

At low currents, f_T improves linearly with current density. Reduced base transit time improves the f_T at a given current density. When the current density is high enough such that the minority carrier density is comparable to the collector doping concentration, the effective base width increases and the device becomes slower. This is known as the Kirk effect. Higher collector doping concentration moves the onset of the Kirk effect to higher current density, resulting in a higher peak f_T prior to the eventual roll-off in f_T at high injection.

High collector doping is desired for high peak f_T yet higher collector doping means lower collector base breakdown voltage. This fundamental trade-off is discussed later.



Other Considerations for Performance

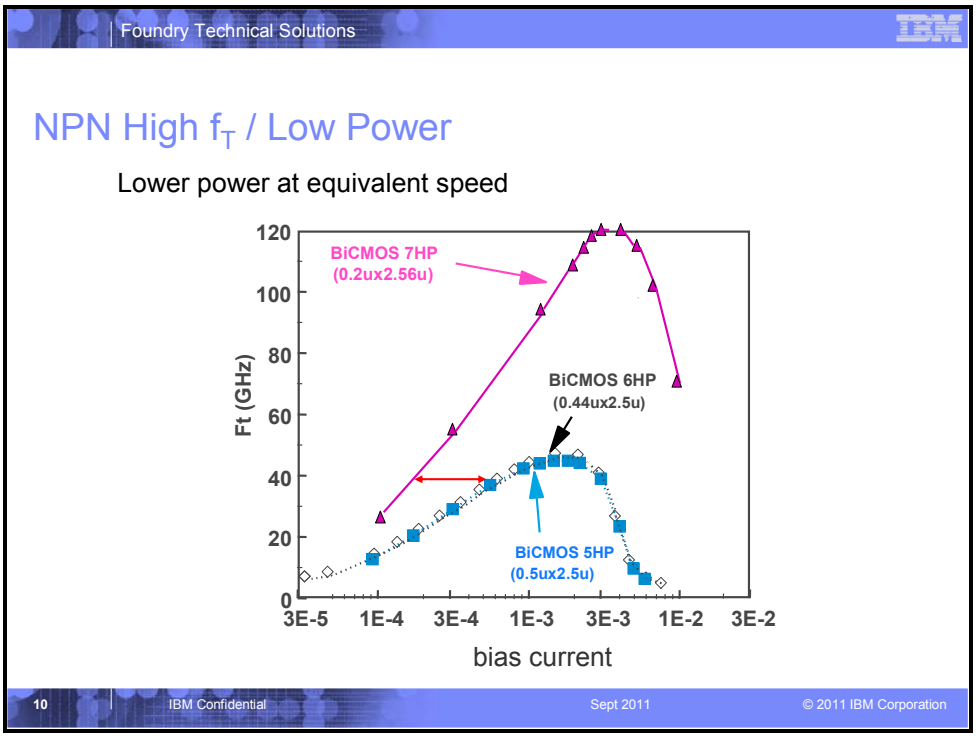
In addition to the performance obtained through the addition of Ge to the base region, there are numerous other considerations when scaling the SiGe HBT for performance and integrating the SiGe HBT into a BiCMOS technology. The previous slide emphasized increasing the Ge concentration gradient and decreasing the base width for improvements in performance through decreased base transit times. However, boron, used as a p-type dopant in the npn base region, diffuses at processing temperatures and limits the ability to form a narrow base. The addition of carbon is an effective method to reduce boron diffusion during thermal processing steps.

Lateral scaling of transistor dimensions is effective in reducing the parasitic resistances and capacitances which degrade the intrinsic device performance.

In the IBM SiGe HP technologies, a 6 µm deep trench, with a heavily doped p+ channel stop at the bottom of the trench, is used to provide density and performance advantages. The deep trench not only reduces the sidewall collector to substrate capacitance, but provides a density advantage by allowing sharing of the deep trench between adjacent npns. The depth of the trench, combined with the p+ channel stop, prevents punch-through between the adjacent collectors at different potentials. The BiCMOS 7WL technology, for example, uses a simplified deep trench process. This "TI" (trench isolation) trench is 2.5 µm deep and does not utilize a channel stop. The TI trench does accomplish the desired reduction in collector to substrate sidewall capacitance for performance, but a larger physical separation between collectors is required to prevent punch-through. Other IBM cost-performance technologies, such as BiCMOS 5HPE, do not utilize any deep trench, depending only on junction isolation and relatively large collector to collector spacing to prevent collector to collector punch-through.

The resistance associated with the polysilicon emitter also has an effect on performance. Partial re-crystallization of the poly emitter (also called re-alignment) helps reduce the emitter resistance and its variability. There are also trade-offs between emitter-base capacitance and base resistance which must be considered when optimizing the extrinsic base implant processing

scheme. A raised base, which provides for a thicker extrinsic base for low resistance with less capacitance impact, is another means of improving the device performance.

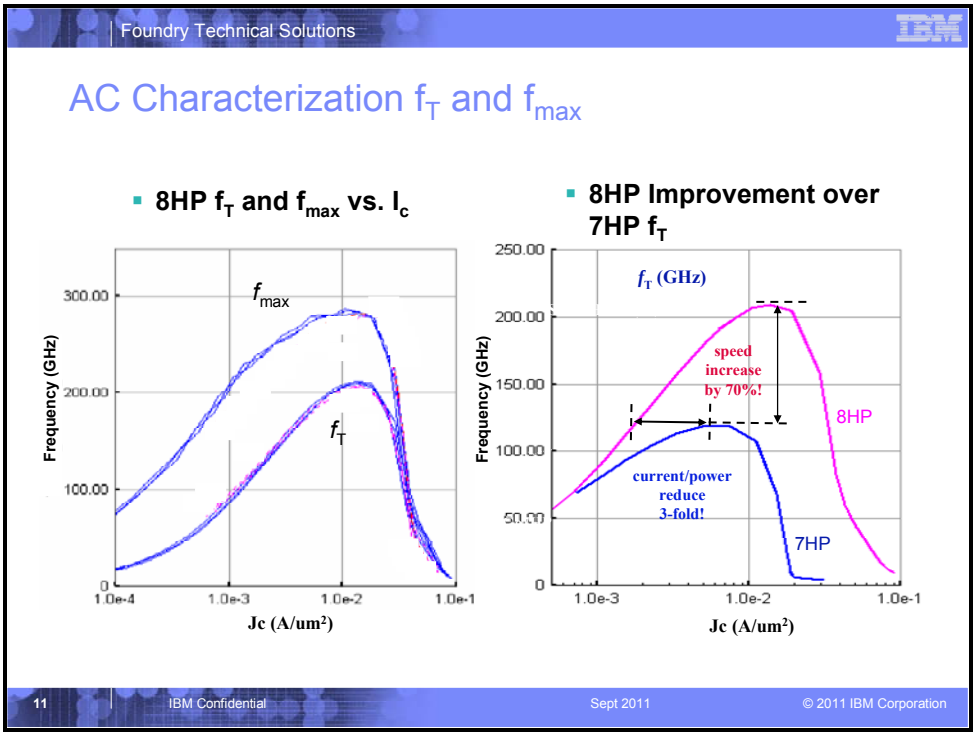


NPN High f_T / Low Power

The slide above shows f_T versus bias current for similarly sized devices in the IBM BiCMOS 5HP, BiCMOS 6HP and BiCMOS 7HP technologies. BiCMOS 5HP and BiCMOS 6HP npns are very similar, with the primary difference in the two technologies being density and performance benefits in the CMOS devices. BiCMOS 7HP features a dramatic increase in f_T due to a number of the scaling considerations discussed earlier. At a given low current bias, f_T is increased relative to the prior generation technologies due primarily to the base width reduction and increased Ge gradient. The Kirk effect is moved out to a higher current bias due to heavier collector doping.

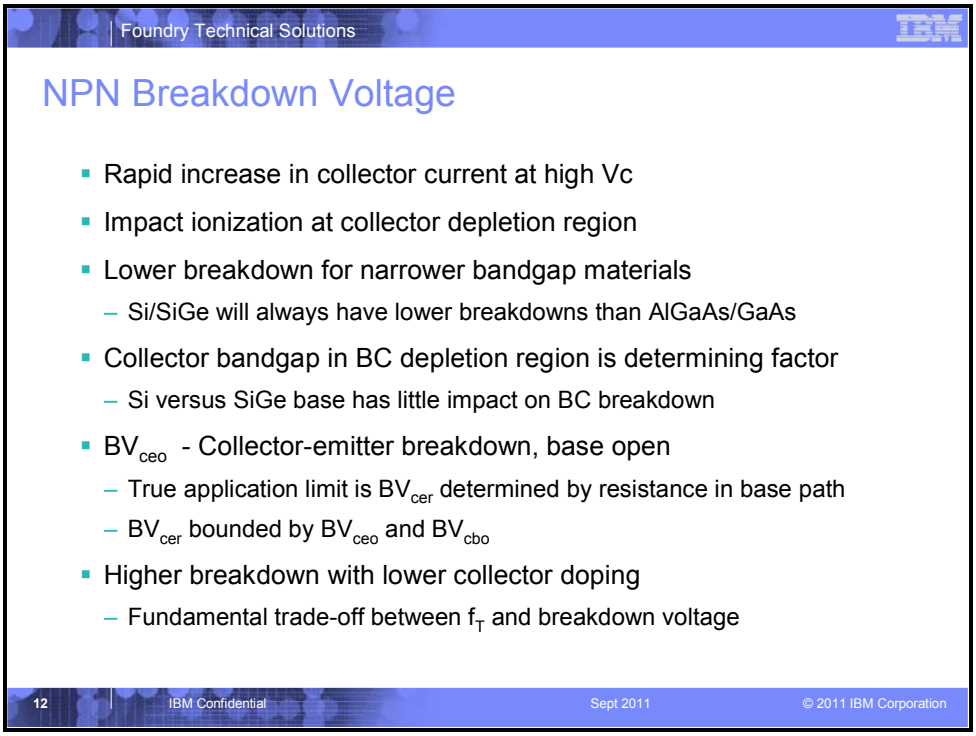
At any given bias level, a higher f_T is obtained in BiCMOS 7HP. For practical circuits, it is often more useful to consider the reduction in power at a given f_T which is obtained through a lower current bias operating point, rather than the increase in obtainable peak f_T.

Chart on next page shows further f_T and f_{max} improvements obtained in 8HP vs 7HP



AC Characterization f_T and f_{max}

f_T and f_{max} performance of the BiCMOS8HP NPNs are shown in the figure on the bottom left of this chart. Comparison of the 8HP f_T performance improvement with 7HP is shown in the figure on the right side of the chart. It shows that almost 2X f_T performance improvement is achieved in 8HP vs 7HP.

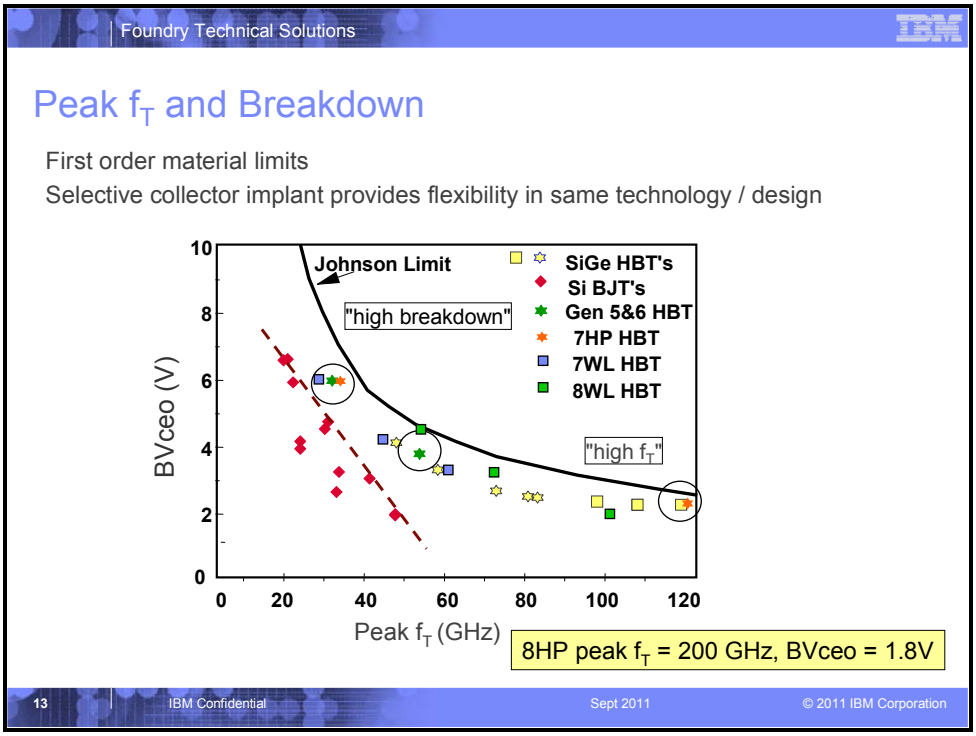


NPN Breakdown Voltage

A rapid increase in collector current with collector bias voltage occurs when the npn goes into breakdown. Physically this effect is due to impact ionization in the strongly reverse biased base-collector depletion region. Silicon and SiGe devices always have lower breakdown voltages than their III-V counterparts due to the wider bandgap of materials such as GaAs and AlGaAs. SiGe and Silicon npns have similar BV_{cbo} (base-collector breakdown, emitter open) since the bandgap in the depleted collector region is the determining factor, not the bandgap in the base region.

Both BV_{cbo} and BV_{ceo} (collector-emitter breakdown, base open) are routinely quoted as figures of merit for bipolar transistors. BV_{ceo} is generally much lower then BV_{cbo}, due to the dc current gain (β) of the device. However, in actual circuit operation, the base is rarely open, but rather at some finite impedance, and BV_{cer}, collector-emitter breakdown for a given base resistance, is the limiter for the voltage applied across the device. BV_{cer} is typically bounded on the low end by BV_{ceo} (base open) and BV_{cbo} (essentially equivalent to BV_{ces}, collector-emitter breakdown, base shorted to the emitter).

As mentioned previously, there is a fundamental trade-off between f_T and breakdown voltage, as both have a strong dependence on collector doping, discussed further next.

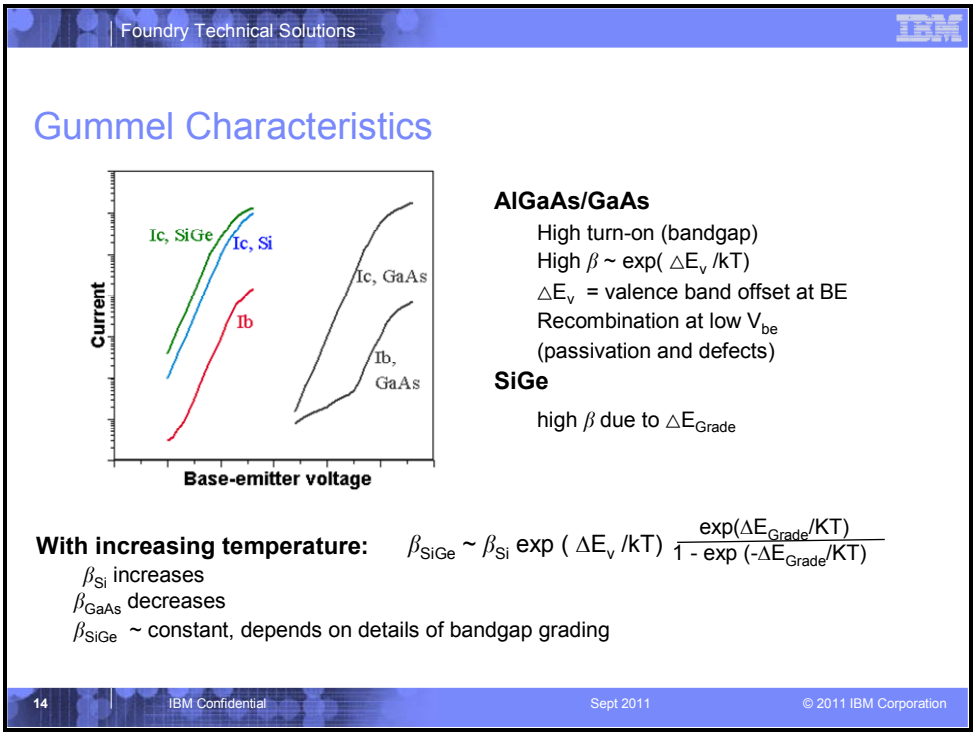


Peak f_T and Breakdown

BV_{ceo} is highest for light collector doping, but peak f_T is maximized by heavy collector doping in order to push out the current density at which the Kirk effect becomes significant. First order theory predicts a fundamental limit to the product of BV_{ceo} and f_T, the Johnson limit shown in the slide, based on first order material properties. Although some important physical phenomena are not captured in the first order theory of the Johnson limit, it is still illustrative of the fundamental tradeoff between BV_{ceo} and peak f_T.

The red diamonds are silicon homojunction npn point from various sources in the literature. The other symbols are for different SiGe HBT technologies. The SiGe HBTs are closer to the Johnson limit curve, especially at the higher f_T points where the device has been more aggressively scaled.

Selective doping of the collector allows the option of different device design points within the same chip. The circle in the upper left highlights the high breakdown device available in BiCMOS5HP, 6HP and 7HP. The center circle highlights the high f_T device in BiCMOS 5HP and 6HP obtained by a masked implant to the collector. The far right circle shows the BiCMOS 7HP high f_T npn. 8HP peak f_T and BV_{ceo} are not plotted in this chart- only figures are given.

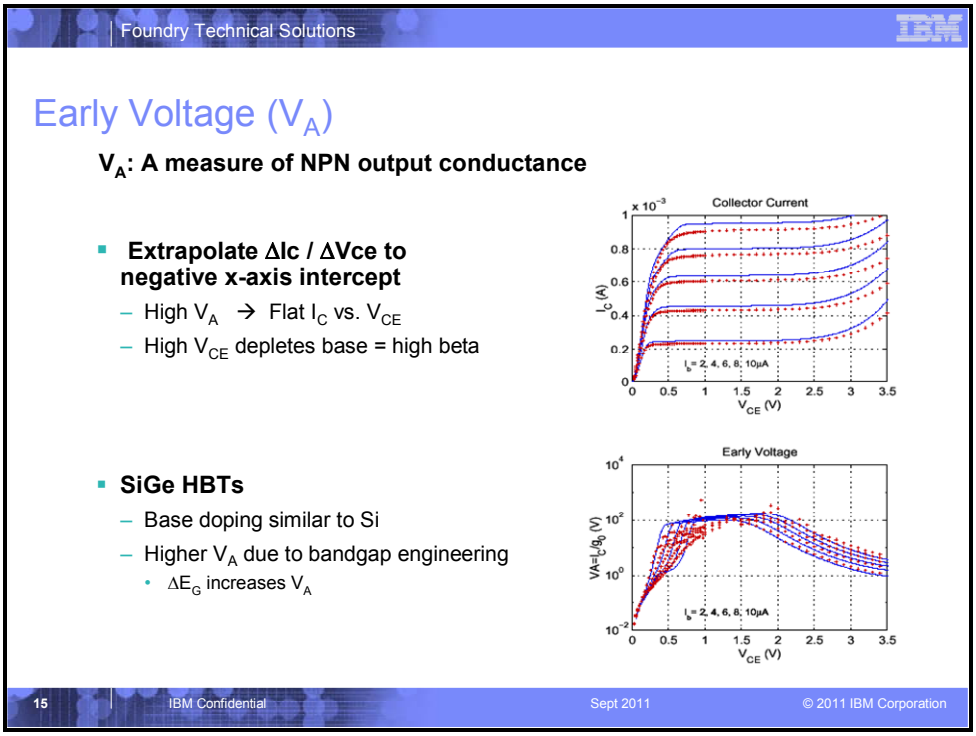


Gummel Characteristics

The slide above illustrates typically Gummel characteristics of AlGaAs/GaAs HBTs as well as SiGe HBTs and Si homojunction transistors. Vbe for a given current density is significantly higher for AlGaAs/GaAs, due to the higher bandgap material. The lower turn-on in Si and SiGe npns may have advantages for low power supply operation.

At low bias, significant deviation from ideal behavior is typically observed in the base current of III-V HBTs, resulting in a narrower range of semi-constant current gain. The current gain is high in AlGaAs/GaAs HBTs, due primarily to the bandgap offset between the AlGaAs emitter and the lower bandgap GaAs base region. SiGe HBTs also benefit from this bandgap difference at the emitter-base junction compared to their Si homojunction counterparts, though often this is traded off for higher base doping and hence lower base resistance.

The temperature dependence of current gain is dependent on the details of the bandgap grading in a SiGe HBT, but in general, the current gain is relatively constant, compared to Silicon npns where gain increases with temperature or AlGaAs/GaAs HBTs with a decreasing gain at higher temperatures.



Early Voltage

Early voltage is a measure of the output conductance of a transistor, as is defined as the negative x-axis intercept following the slope of I_c versus V_{ce}. High Early voltage means a flat I-V curve; low output conductance. The physical mechanism behind non-zero output conductance (non-infinite Early voltage) is the voltage dependence of the depletion region width into the base region. As the base depletes more at higher voltage, the effective base width is reduced. The collector current is proportional to the gradient of the minority carrier concentration in the base, which increases as the base narrows. In a silicon npn, for a given base doping level, a more heavily doped collector (desired for high peak f_T) will result in more depletion into the base region, and hence a degradation in Early voltage.

The dynamics of conduction in a SiGe HBT base with graded germanium content is quite different from a silicon bipolar device. Rather than being dependent on the base width, the current delivered to base by the emitter is determined by the device structure in the vicinity of the emitter-base junction. For typical base structures, the current depends very little on the location of the depletion edge on the collector side of the base. This is manifested as an increase in Early voltage (compared to a Silicon npn with equivalent doping levels) that is exponentially dependent on the bandgap gradient across the base.

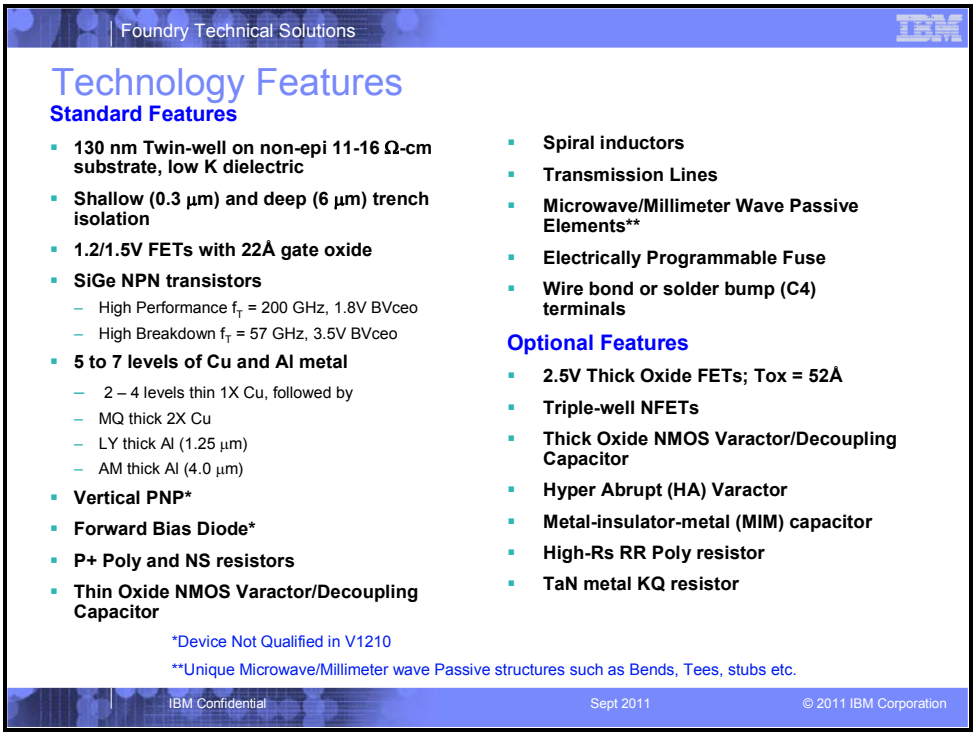
The plots shown in the slide are examples from an IBM model reference guide. The upper plot is the current-voltage characteristics. The lower plot is a calculation of Early voltage, determined at each V_{ce} point, versus V_{ce} on a log-linear plot. This type of plot makes it more obvious where the device enters the linear region with high, nearly constant Early voltage, and then at higher Vce, the degradation in effective Early voltage as the device enters breakdown.

Technology Overview and Device Library

This training module provides an overview of the BiCMOS8HP technology features and an introduction to the devices available in the BiCMOS8HP design kit.

This presentation is intended to be introductory rather than comprehensive. Design kit users are encouraged to consult the documentation shipped with the kit for more information. The layout rules, electrical specifications, and reliability rules are contained in the Design Manual. Model theory and equations are given in the Design Manual. Further model information is available in the Model Reference Guide that includes extensive model-to-hardware comparison plots. Additional design kit functional information may be found in the User's Guide. The Release Notes provide version-specific information on the design kit.

BiCMOS8HP is the IBM marketing as well as the design kit name that is used on the IBM Customer Connect (ICC) for this 0.13 µm technology. In some instances, SiGe8HP is also used as alternate designation. 8HP is the short name for this technology.

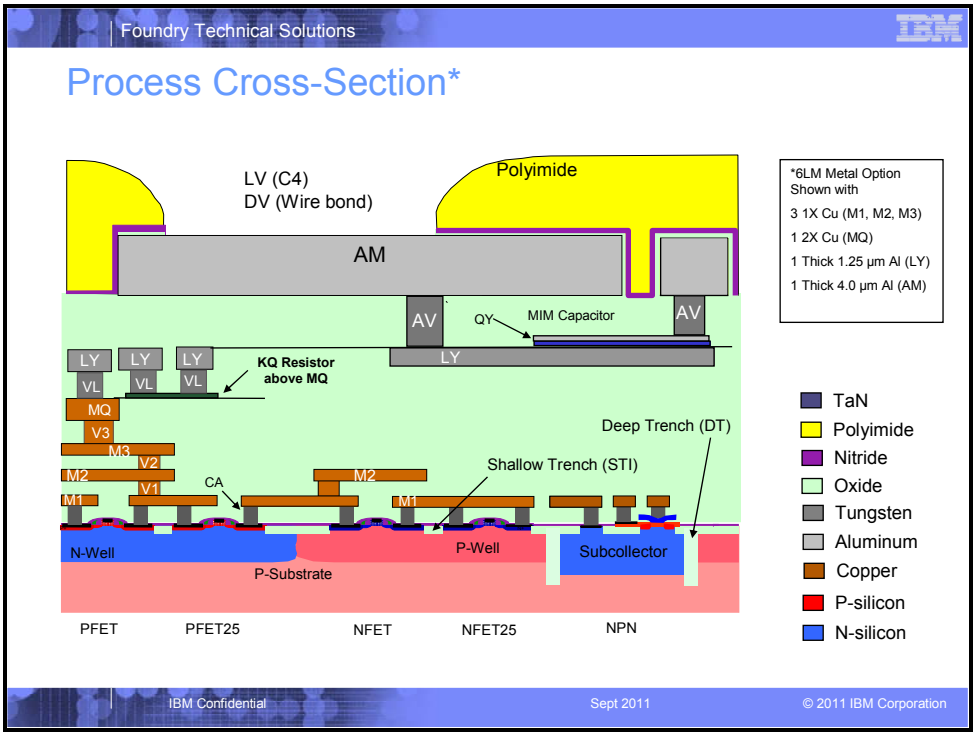


Technology Features

IBM's BiCMOS8HP technology starting wafer is doped p-type with a resistivity of 11-16 Ohm-cm. which provides improved noise isolation and inductor Q performance compared to the lower substrate resistivity. The lithography node is 130nm. The technology utilizes shallow trench isolation (STI), nominally 0.35 μm deep into the silicon, to provide a dense isolation between FETs and other devices. A deeper trench (DT), 6.0 μm deep, is also provided to reduce sidewall capacitance and improve isolation of NPN transistors and other devices that use the deep implanted subcollector. All diffusions and polysilicon are silicided for low resistivity unless the silicide formation is intentionally blocked e.g., to form a resistor.

BiCMOS8HP provides a comprehensive suite of devices including two different performance NPN bipolar transistors; 2.2 nm (thin) gate oxide 1.2/1.5 V regular FETs; 5.2 nm (thick) gate oxide 2.5V I/O FETs; triple well NFETs; nMOS and hyper-abrupt junction varactors; forward bias diode; thin and thick oxide decoupling capacitors; single nitride metal-insulator-metal (MIM) capacitor; diffusion, polysilicon and TaN resistors; programmable electronic fuse; high density and/or high Q series and parallel spiral inductors; transmission line and distributed passive RF elements, and wirebond and solder bump (C4) terminals.

Specific devices needed for a particular application are chosen from the technology options menu in the "Technology Introduction" section in the Design Manual. Some of the technology features are listed in the slide above. The left column titled **Standard Features** show devices/features associated with the standard manufacturing flow. In the right column **Optional Features** set of devices are listed that need additional masks, wafer processing, and/or characterization steps necessary to provide the desired optional features.



Process Cross-Section

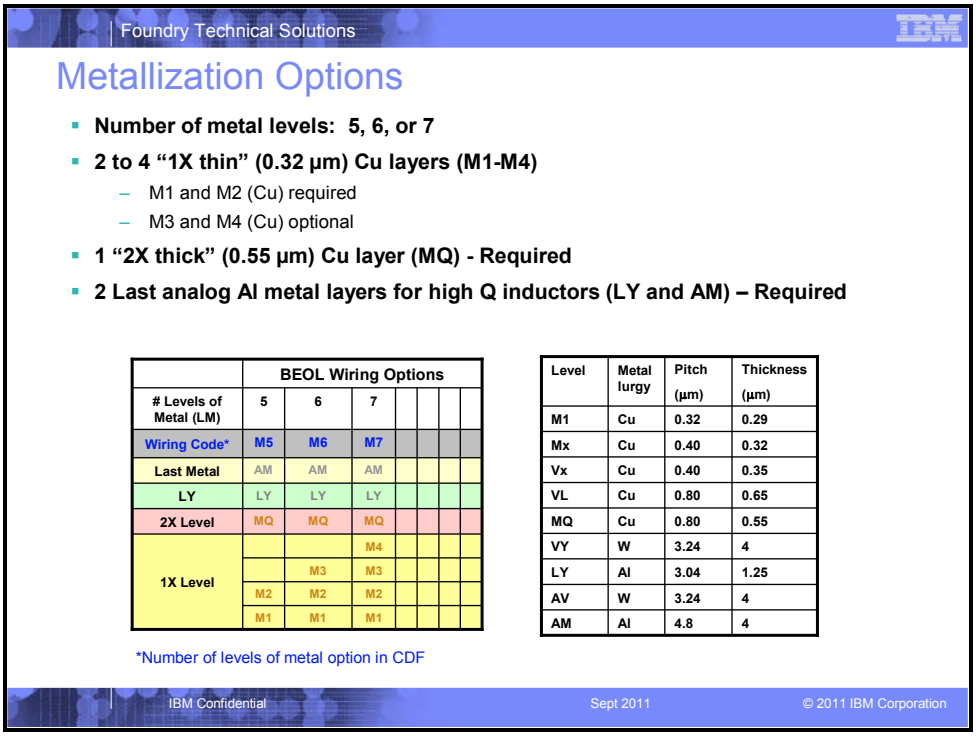
The diagram above shows the process cross-section with some of the features of the BiCMOS8HP technology. To help clarify the various layers used in the illustration of cross-sectional diagrams, color coding is used throughout the training material. N- and P-doped silicon is denoted by blue and red colors, respectively, with heavier doping represented by more saturated colors. FET devices are isolated by the shallow trenches (STI) and NPNs by the deep trenches (DT).

The diagram above depicts “6 Levels of Metal (6LM)” option with 3 layers of “1X wiring” (M1, M2, M3), 1 layer of “2X wiring” (MQ), and the two “RF wiring” layers (LY and AM), for a total of six levels of metal. A metal-insulator-metal (MIM) capacitor appears in its only allowed position above the LY wiring level. The KQ tantalum nitride resistor is between the 2X wire MQ and LY. Additional details of the wiring (metallization) options are shown on the next page.

IBM technologies use chemical mechanical polish (CMP) to provide planar surfaces throughout processing. The surface planarity allows better lithographic resolution than could be obtained with topography present, enabling smaller layout ground rules as well as stacked contacts and vias for better wiring density. To meet the CMP process requirements, automated fill routines are used during mask data preparation to create uniform active region (RX) and polysilicon (PC) pattern density for robust manufacturing. Copper metal layers, 1X thin (M1-M4) and 2X thick, MQ, receive both automated fill and hole generation to provide uniform metal pattern density.

Final chip passivation is formed by a sequence of oxide, nitride, and polyimide films. The nitride serves as an ionic contamination barrier while the polyimide provides mechanical protection.

IBM refers to the part of the wafer up to the contact layer CA as the front-end-of-line (FEOL) and the levels from CA through the polyimide as the back-end-of-line (BEOL).

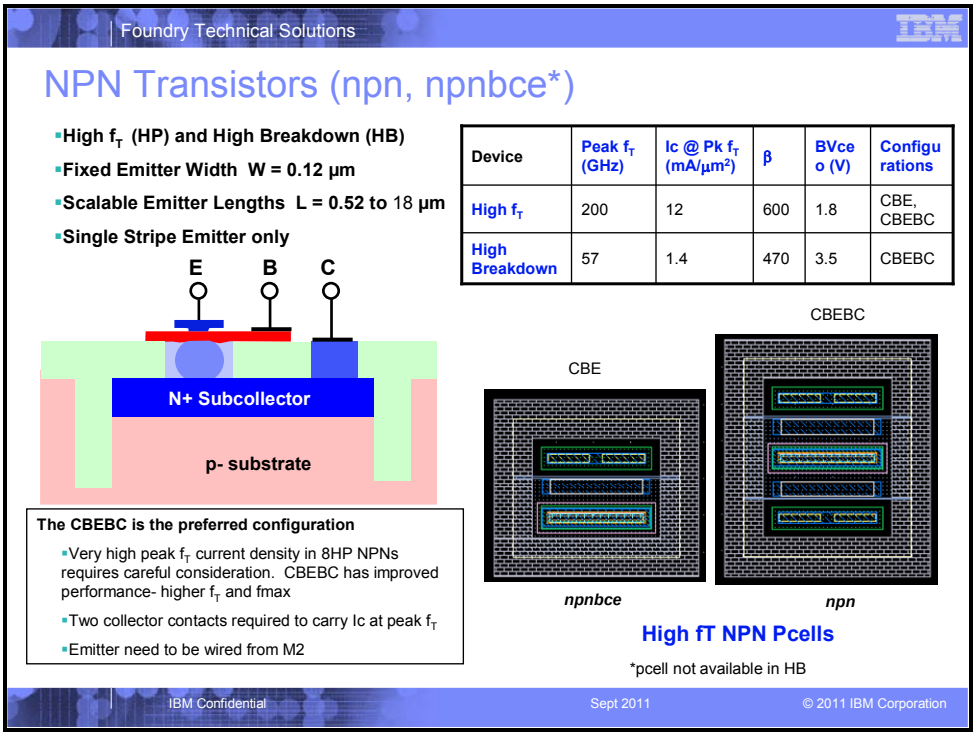


Metallization Options

Table shown on the bottom left summarizes the available BEOL wiring (metallization) options in the BICMOS8HP technology. The options cover between five and seven total levels of metal. Two layers of "1X thin" Cu metal wiring (M1 and M2), one layer of "2X thick" Cu metal wiring (MQ), one 1.25µm thick Al wiring level (LY) followed by a 4 µm thick Al layer (AM) are always required. Two 1X thin Cu wires, M3 and M4, are optional.

LY and AM are used for RF wiring. AM layer can be used for regular wiring also.

Number of levels of metal (5, 6 or 7) information shown in this Table is necessary for creating design library which will be described further in the Design Kit section.



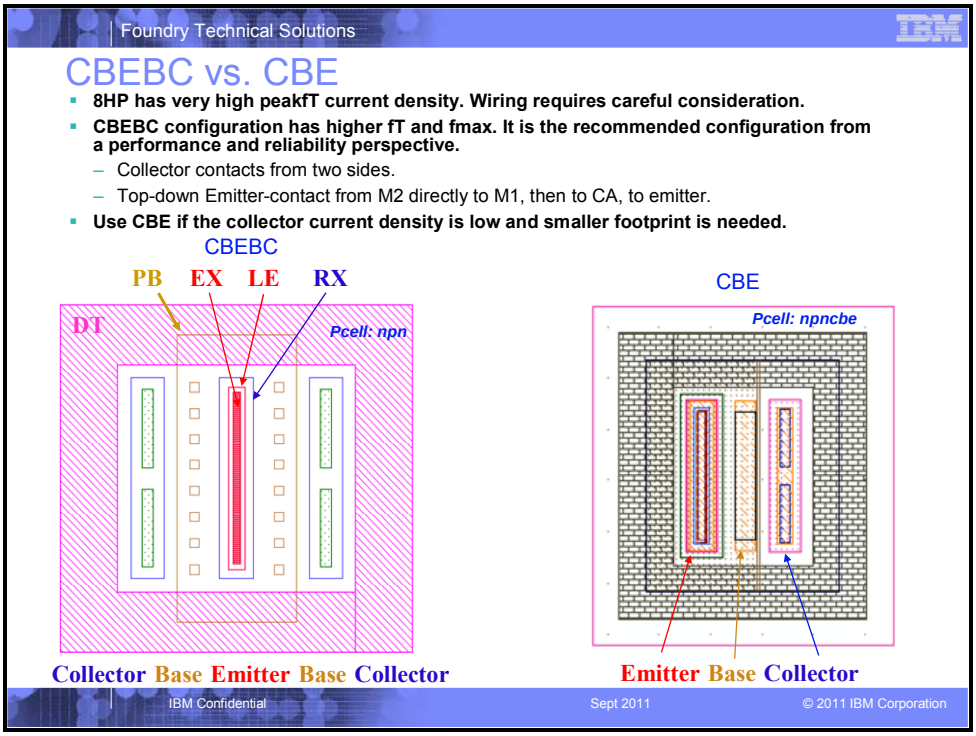
NPN Transistors

BiCMOS8HP offers two npn transistors representing different points in the f_T vs. breakdown voltage performance trade-off as shown in the chart above. Higher collector doping extends the frequency response by increasing the current level at which unity current gain occurs (Kirk effect), but lowers BV_{CBO} (collector-base breakdown voltage, emitter open) and BV_{CEO} (collector-emitter breakdown, base open).

IBM offers parameterized cells, called **pcells**, for facilitating the device layouts with different sizes, geometries and configurations. Both NPN devices are created using the same pcell, *npn*. (See next page NPN pcell properties form for details). The NPN transistor type High_f_T (HP) or High_Breakdown (HB) is selected by the "Performance/Breakdown" option in the properties form.

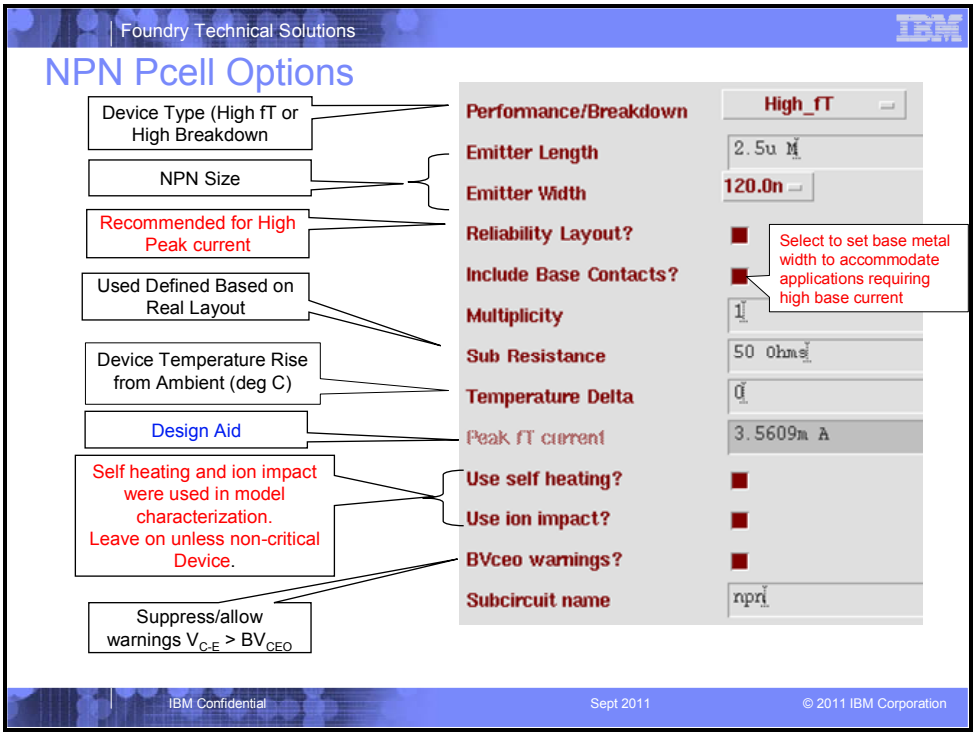
NPNs have fixed emitter width of 0.12 µm and single stripe only. These NPNs provide the lowest base resistance for low noise operation. The emitter length may be selected from 0.52 to 18 µm.

High f_T *npn* pcell has two configurations – CBE and CBEBC. CBEBC confirmation has a larger foot print, but this is the preferred layout recommended by IBM. (See next page for CBE vs CBEBC trade-offs). The high break down pcell has CBEBC configuration only.



CBE vs CBEBC Configurations

BiCMOS8HP has very high peak f_T current density. Therefore, wiring of the NPN needs careful consideration. The CBEBC configuration has higher f_T and $f_{max.}$ It is the recommended configuration from a performance and reliability perspective. In this layout version, the collector contacts from two sides and the emitter contact are from M2 directly top down to the M1, then to CA, to emitter. The CBEBC model accounts for these layout changes.



NPN Pcell Options

The various options that can be selected in the *npn* pcell properties form is shown in the chart above. The device type, High_f_T, or High_Breakdown, is selected using the **Performance/Breakdown** button. Device geometry is set by selecting the **Emitter Length**, the **Emitter Width** (it is fixed to 0.12 µm), the **Include Base Contacts** (for higher current density) and the **Multiplicity**. The **Reliability Layout** selection is provided for the high f_T CBEBC configuration. Current limit calculations should be performed to insure that electro-migration rules are met.

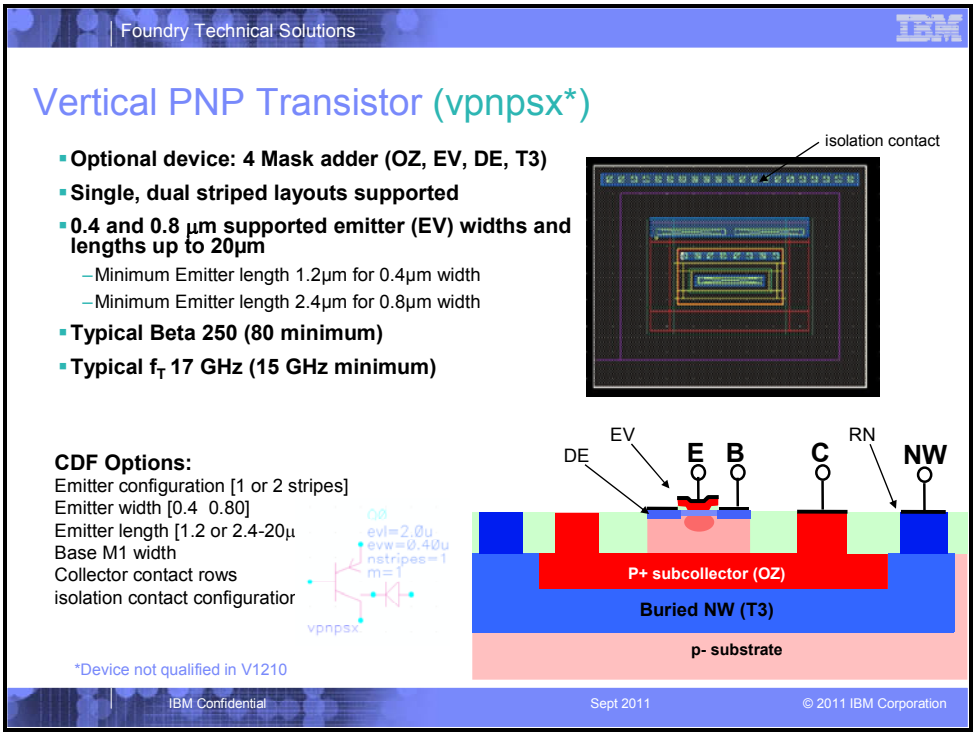
For simulation, fill-in the **Sub Resistance** box to the desired substrate resistance value. The **Temperature Delta** is set to a value above the ambient temperature if local heating may be present.

Use self-heating, **Use Ion Impact** and **BVceo warnings** switches are provided for control of the NPN simulation. *Self-heating* adjusts the device temperature relative to the overall simulation temperature based on the calculated power dissipation. It may not be necessary for low power devices and may be turned off to improve simulation time or convergence.

Impact ionization captures avalanche effects in the base-collector region. Devices operating at low voltage will not be subject to impact ionization and this part of the model may be turned off, again to improve simulation time.

The model displays a warning in the simulation whenever the collector-to-emitter voltage exceeds BVceo. This can be very helpful to screen for potential breakdown concerns in large designs, but can become cumbersome when devices are intentionally being operated above BVceo. *Since device breakdown depends on the impedance connected to the base, operation above BVceo does not necessarily present a problem, and designers may want to suppress these warnings.*

All of these settings are also controlled by global switches that may override the settings on individual devices. These will be discussed further in the Model and Simulation section.

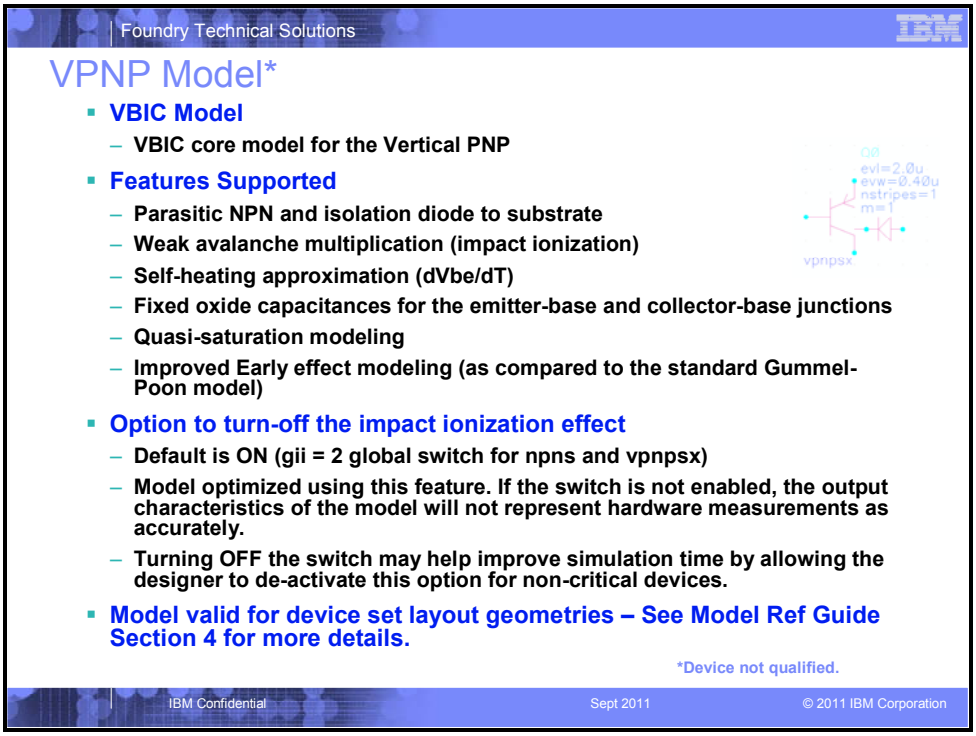


Vertical PNP Transistor (vpnpsx)

The vertical PNP transistor requires two unique additional masks: EV, to define the emitter, and OZ, to provide a deep p-type implant to form the collector. Two optional masks are shared with other devices: T3 for the collector-to-substrate isolation, and DE for the extrinsic base implant.

The vertical PNP transistor is not yet fully qualified. The simulation model should be considered “alpha” level. Please contact IBM if you intend to use this device.

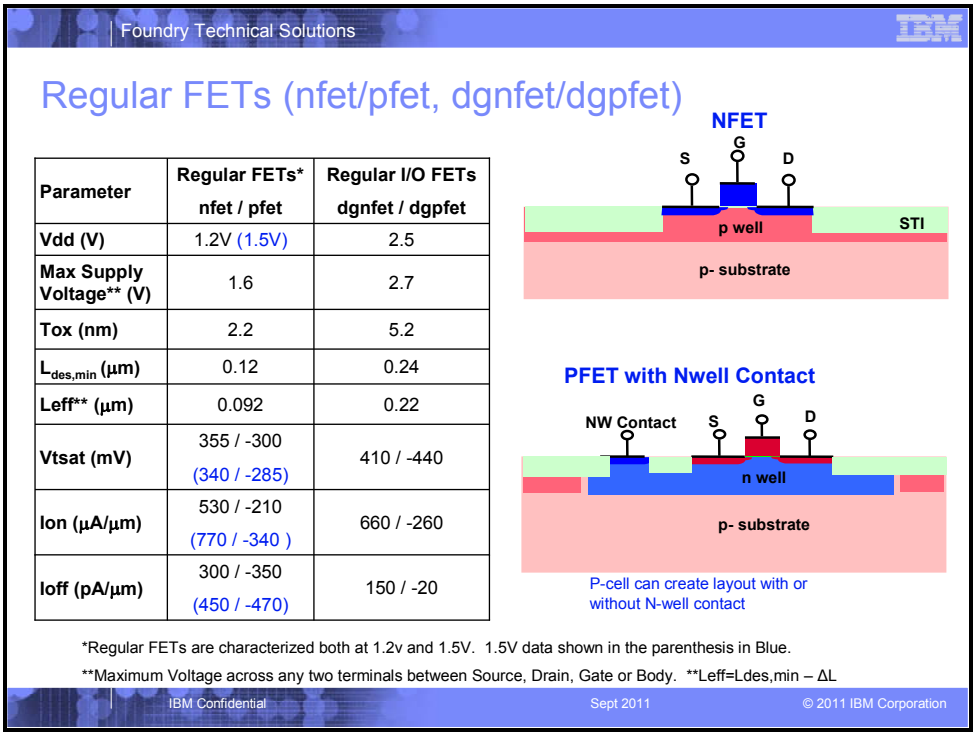
The pcell supports both single (shown) and dual emitter (C-B-**E**-B-C-B-**E**-B-C) layouts. Two emitter widths are available. The emitter length can be scaled to obtain the desired current rating, up to a maximum of 20 µm. The minimum emitter length is 1.2 µm for the 0.4 µm wide device, and 2.4 µm for the 0.8 µm wide device. The dc current gain is approximately 250 and f_T is about 17GHz.



VPNP Transistor Model

The vertical PNP transistor (vpnpsx) model uses separate VBIV elements for the vertical and lateral NPN components. Supported features of the VPNP VBIC model are shown in the chart above.

This device is not qualified at this time (PDK Version v1210). The model is restricted is to the set layout geometries.



Parameter	Regular FETs* nfet / pfet	Regular I/O FETs dgnfet / dgpfet
Vdd (V)	1.2V (1.5V)	2.5
Max Supply Voltage** (V)	1.6	2.7
Tox (nm)	2.2	5.2
$L_{des,min}$ (µm)	0.12	0.24
Leff** (µm)	0.092	0.22
Vtsat (mV)	355 / -300 (340 / -285)	410 / -440
Ion (µA/µm)	530 / -210 (770 / -340)	660 / -260
Ioff (pA/µm)	300 / -350 (450 / -470)	150 / -20

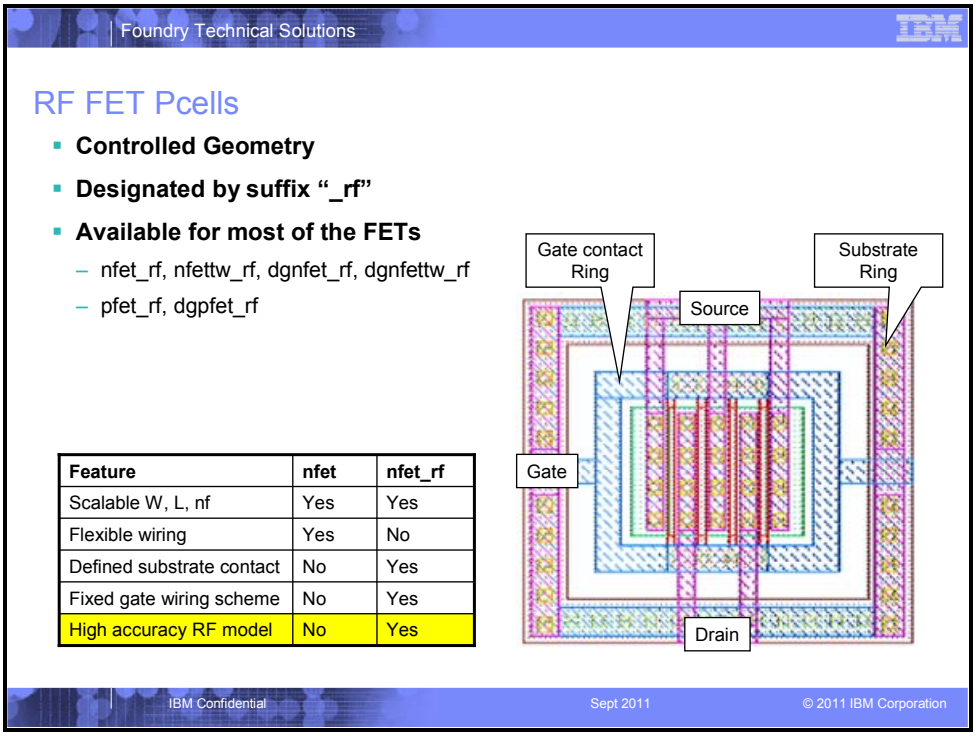
BiCMOS8HP FETs

BiCMOS8HP supports regular threshold voltage (Vt) FETs for both thin and thick gate oxides. The table above summarizes the key electrical parameters for these devices.

The thin oxide FETs have gate oxide thickness of 2.2 nm and minimum drawn channel length of 0.12 µm (0.092 µm effective channel length). They are characterized both at 1.2v and 1.5V. Maximum operating voltage is 1.6V for these FETs.

The thick oxide FETs have 5.2 nm gate oxide thickness and channel length of 0.240 µm. They can be operated to 2.7V maximum.

Questions sometimes arise about the meaning of the maximum voltage in the context of large source-to-body voltages. Maximum voltage means the largest allowed voltage, including power supply tolerance, allowed across any two terminals of the device. For example a thin oxide device may not operate with Vd=2.6V, Vs=1V and Vsub = 0V since the Vd-sub would be 2.6V.

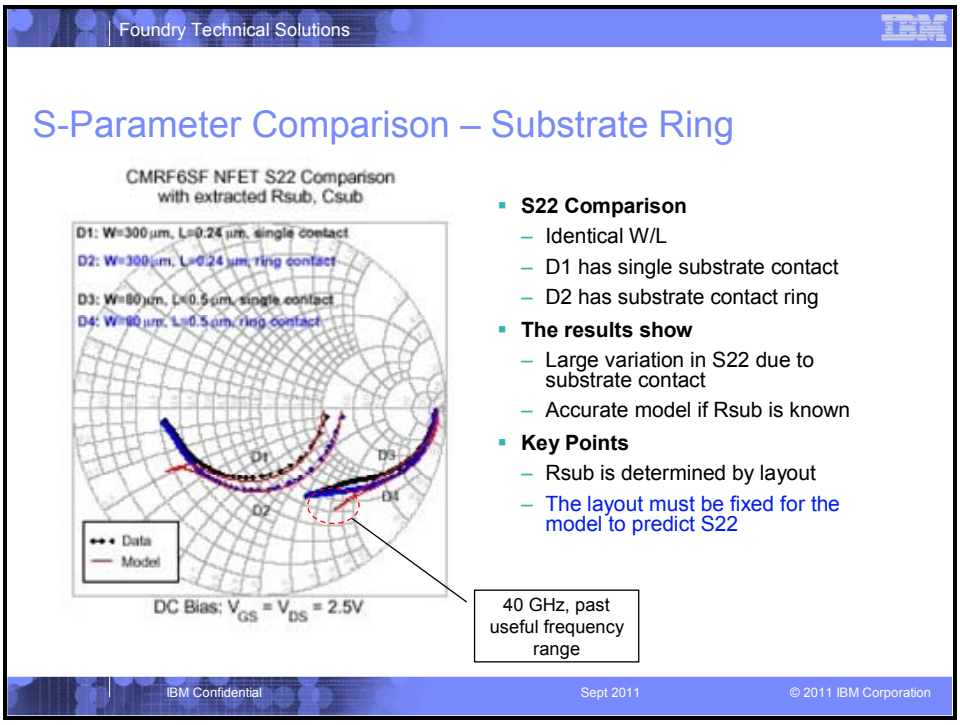


RF FET Pcells

An optional set of FET pcells is provided for RF applications. These RF layouts have low resistance gate connections on M1, source and drain connections on M2. These layouts invoke the parameter "rf" in the models which set the parasitic resistances and capacitances to the values specific to this controlled geometry in order to provide the most accurate simulation of electrical behavior.

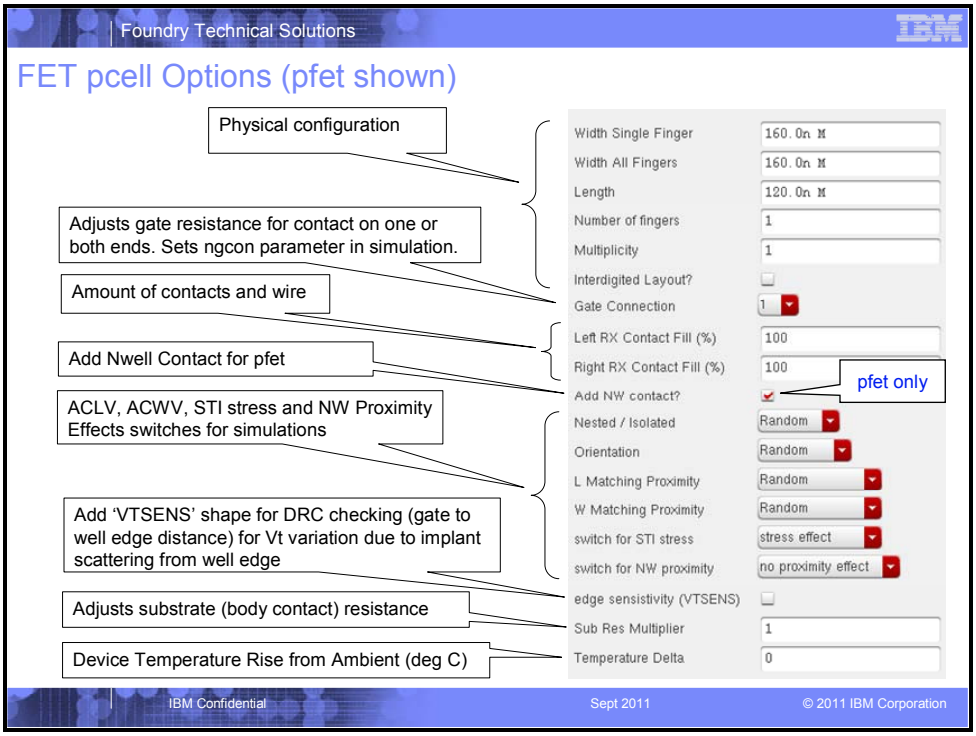
The RF layout model takes into account the parasitic effects of wiring within the pcell boundary. Additional wiring resistance and capacitance elements are added to the device only when the rf switch is on. Parasitic extraction does not extract additional elements inside the rf pcell.

The CDF properties form allows an input for substrate resistance, but any user entry is ignored since the substrate resistance is fixed by the layout and reflected in the model.



S-Parameter Comparison – Substrate Ring

The chart shows S22 S-Parameter data from standard and rf layouts in IBM's 0.250µm RF CMOS technology. The devices compared are of identical size and configuration with the exception of the substrate contact. In the devices D1 and D3, a *single contact* was placed in the vicinity of the device. In devices D2 and D4, *substrate contact rings* were employed. Note that the *substrate contact configuration* has a significant effect on S22 of the device. If accurate RF models are desired, it is necessary to use a layout with a known substrate contact configuration.



FET pcell Options

The Component Description Format (CDF) properties window for the FETs shown above exhibits the choices available for selecting the device options and parameters. PFET CDF is shown in the chart above. The PFET **length** and **width** are the primary pcell options. Multi-fingered layouts (multiple PC gates in parallel, within the same RX shape) are supported through the **Number of fingers** prompt in the properties form. The **Width All Fingers** parameter is the total width of the multiple fingers, and the **Width Single Finger** reflects the actual RX width. Nwell contact can be selected using the **Add NW contact?** Switch.

Multiple copies of the same device can be placed in the schematic as a single instance by setting the **Multiplicity** to the number of multiple copies to reduce simulation time. If multiplicity is selected the layout of the devices will have a dummy layer "MULTI" "DEV" to indicate that they are part of a multiple set.

To reduce the gate resistance of an FET, both sides of the gate of the device may be wired by selecting the **Gate Connection** appropriately. The associated FET model parameter "gcon" is set to one for a single gate connection and two for connections at both ends of the gate. In the layout the non-design layer "DRIVE" "DG" identifies the FET layout as having gcon = 2 and is conditionally included within the pcell depending on the gcon setting. LVS will insure that the layout is wired in agreement with the gcon parameter setting. If two gate connections are made they must be to the same electrical node. Do not wire through the gate since this will be a high resistance connection and may cause circuits sensitive to resistance to fail.

The FET pcells are designed to allow variability in the diffusion contacts. The parameters **Left RX Contact Fill (%)**, **Right RX Contact Fill (%)**, and for multi-fingered devices, **Center RX Contact Fill (%)** have been added. These parameters will control the diffusion contact configuration. Values within greater than 0 and up to 100 will draw the metal and contact according to the specified percentage of available space. A value of 0 will remove the contact and draw the diffusion to ground rule minimum dimensions. This configuration is one method of

constructing abutted devices. Alternatively, pcells support the Cadence auto-abutment feature in Layout XL that allows cell to be automatically aligned and overlapped if they are electrically connected in the corresponding schematic view; see the User Guide for more information.

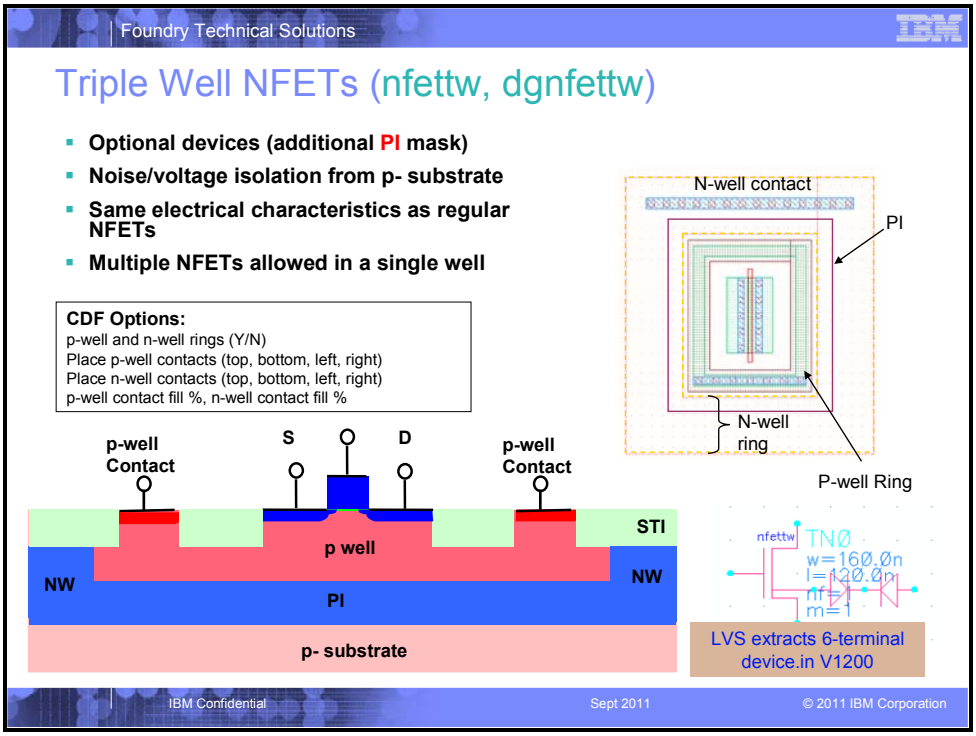
At 130 nm feature size, NW proximity effect is important. Set the switch for NW **Proximity effects** button to ON if this effect should be included in the schematic based simulations for the individual devices. The well proximity, STI stress and across chip line width variation (ACLV, ACWV) switches are discussed in the models and simulation section.

The VTSENS shape is a dummy layer placed in the layout that enforces a certain minimum distance from the nearest n-well boundary in DRC. The **Edge sensitivity (VTSENS)** switch is provided that adds 'VTSENS' shape for DRC checking. These devices are guaranteed to avoid Vt variation based on proximity to well boundaries. This will be described further in the Layout Topics section.

Substrate contact resistance may be of importance in accurate modeling. Designer can use a substrate contact resistance multiplier of choice by filling the appropriate value in the **Sub Res Multiplier** box.

The **Temperature Delta** switch is same as described in the *npn* pcell form. If local heating is of importance in simulation, fill in the appropriate value in the form.

There are "grayed out" values also shown on the CDF properties forms. These are calculated values from the skill code call-back routines for designer's aid only.



Triple Well NFETs

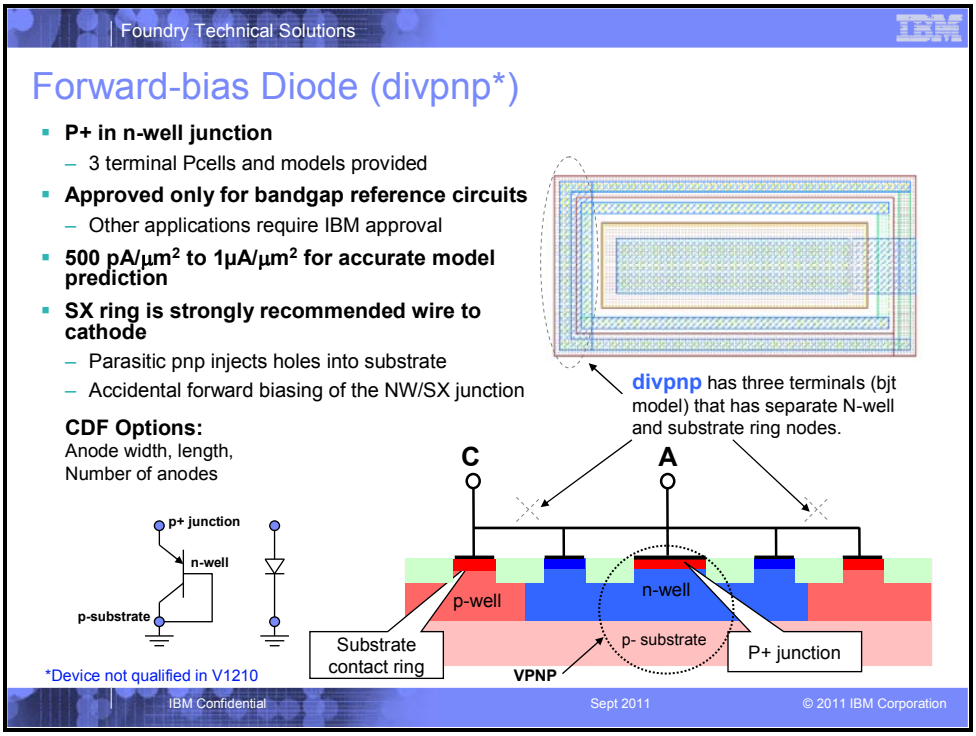
The triple-well devices provide NFETs within a p-well that is isolated from the substrate. Isolation is accomplished by inserting a buried n-type layer between the local p-well and the P-substrate. This layer is designated by the PI mask level. A ring of n-well provides lateral isolation and connects to the PI region.

The isolating n-type layer should be tied to a quiet power supply that is at a high enough potential to prevent forward biasing the PI/substrate or PI/p-well junctions.

The schematic symbol for the device includes the NFET with the parasitic diodes for p-well to PI (isolation) and PI to substrate. *All six terminals must be explicitly wired in the schematic. Only gate, source, drain, and p-well are LVS checked. The PI region and the substrate are not.*

The triple-well NFET pcells create an NFET in PI isolation and optionally adds p-well and n-well rings. The pcell also has option to create n- and p-well contacts as desired. The designer can specify how much of these contacts are covered by CA and metal using the “contact fill” options as a way to leave room for other wiring on M1 in the vicinity of the device. *LVS tools extract this device as an NFET (four terminals). The diodes represented within the symbol, that is the p-well/PI diode and the PI/substrate diode, will be extracted as parasitic elements when using one of the parasitic extraction tools.*

Triple-well NFETs are available for both the thin and thick oxide NFETs.

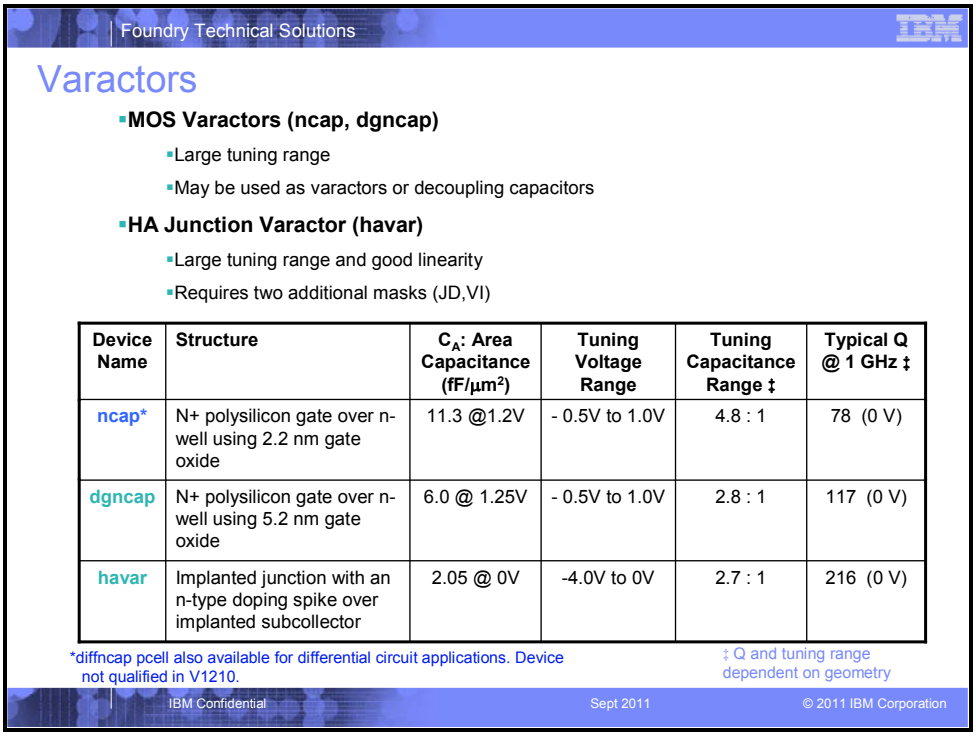


Forward-bias Diode (divpnp)

The general use of forward-biased diode as circuit elements is not supported. However, bandgap reference circuits employing forward-biased p-diffusions in a grounded n-well are allowed provided they adhere to the forward biased diode layout ground rules. Use the *divpnp* pcell in order to ensure a fully consistent device model. The width must be greater than or equal to 1µm.

This structure is actually a vertical pnp transistor as shown in the lower left, with the p+ junction, n-well, and substrate forming the emitter, base, and collector respectively. The *divpnp* model simulates the e P+/NW junction. It is a three terminal model (bjt model) that has separate N-well and substrate ring nodes. It is strongly recomended that these nodes be shorted together to prevent accidental forward biasing of the NW/SX junction. Contact IBM at fdrytech@us.ibm.com if you have an application that would require a different connection or form factor.

For exponential current-voltage dependence keep the current density within the limits specified.

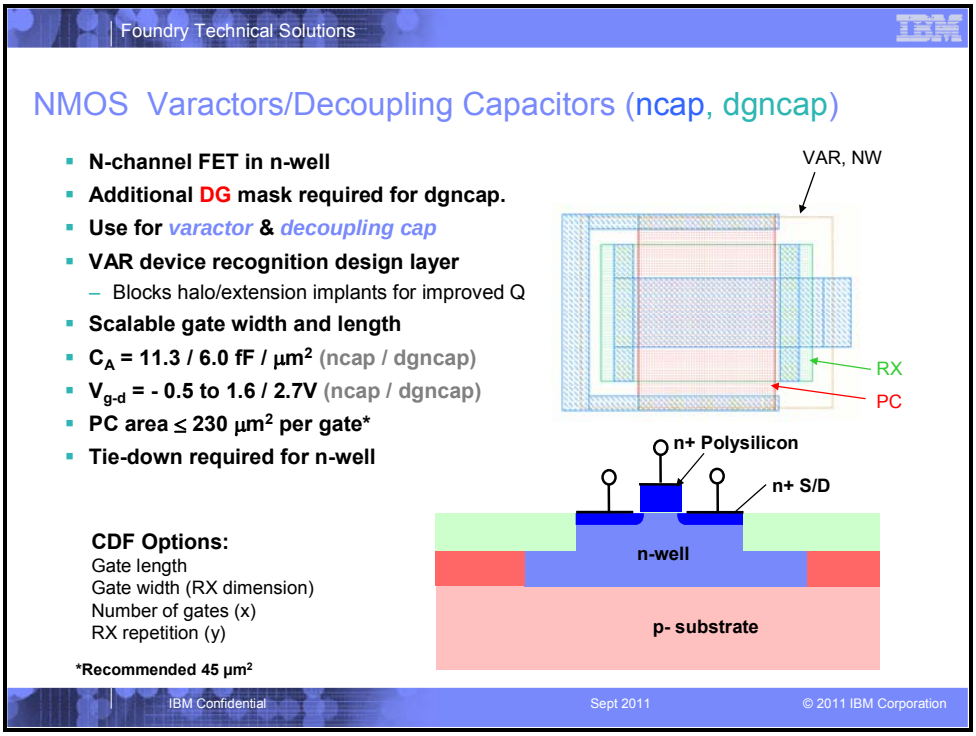


Varactors

Varactors are used as variable capacitors in applications such as voltage-controlled oscillators (VCO). The BiCMOS8HP technology provides a standard thin oxide nMOS varactor (*ncap*) and two optional varactors : a thick oxide nMOS varactor (*dgncap*) and a hyper-abrupt junction varactor (*havar*). A differential version of nMOS varactor *diffncap* is also avaible that is suitable for differential circuit applications. The nMOS varactors operate between depletion and accumulation. The hyper-abrupt varactor operates in the reverse-bias mode.

The table shown above compares characteristics of the different varactor devices. The physical size was chosen to produce approximately the same capacitance. Varactor tuning range and quality factor depend on device dimensions so values will differ from this table when using different choices for varactor physical parameters.

The varactor voltage ranges arise from different considerations. For the *havar*, the range is that for which the model provides a good fit to the measured electrical behavior. The lower voltage limit of the *ncap* and *dgncap* devices is to avoid biasing the device into deep depletion. Biasing this region leads to instability as the capacitance varies due to the slow thermal creation of holes. These biasing conditions refer to the DC bias values. AC modulation on top of DC bias can go below -0.5V.



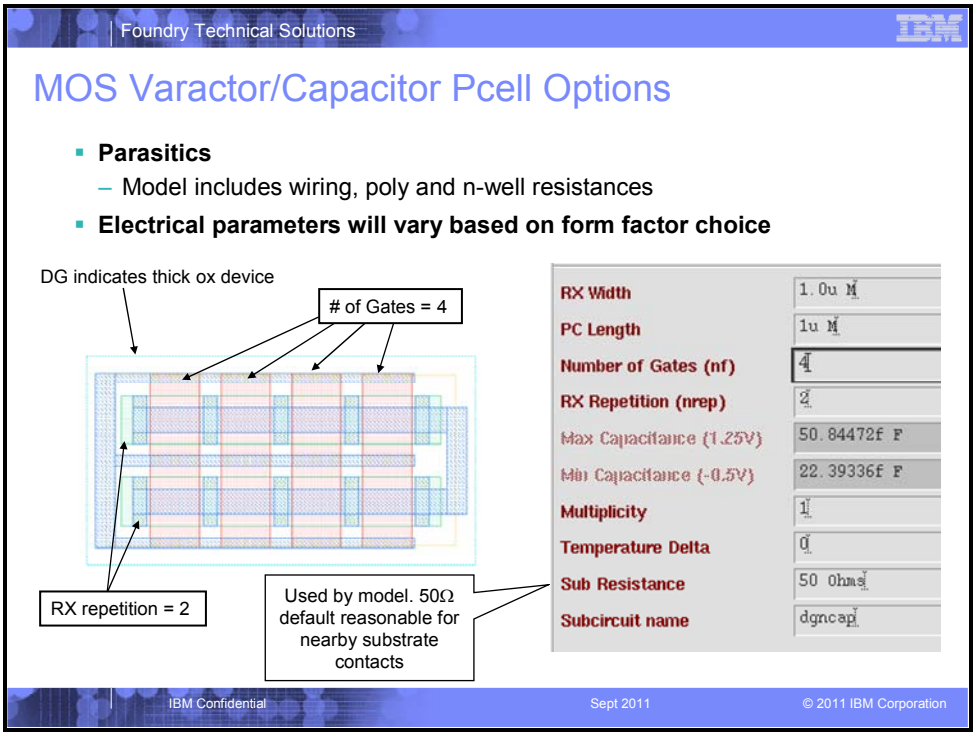
NMOS Varactors/Decoupling Capacitors (ncap, dgncap)

The NMOS capacitors, *ncap* and *dgncap* devices are created as a thin or thick oxide "NFET in n-well" structure. The well is the n-well used for the standard PFET.

The VAR shape blocks the halo and extension implants that would normally be placed in the PFET. (The Boolean operation creates the generated mask levels BH/PH and DE/DF in post-processing operations at IBM.) Blocking of the halo and extension implants improve the varactor Q. The device receives the NFET source and drain implants which also dope the polysilicon as n-type. The variable capacitance is achieved as the device is biased from depletion (gate negative) to accumulation (gate positive).

There are several layout practices, enforced through ground rule checking, that prevent damage from in-process charging. The n-well must be connected to an n+ /substrate junction at M1. The maximum thin oxide area for any single gate is limited to 230 μm^2 to prevent charging damage in the polysilicon etch, dielectric deposition, and contact etch processes (GR132). *The large area thin capacitors must be designed by connecting small area plates in parallel (230 μm^2 maximum for polysilicon, recommended 45μm^2).* There are additional gate tie-down rules that will be described in the Layout section.

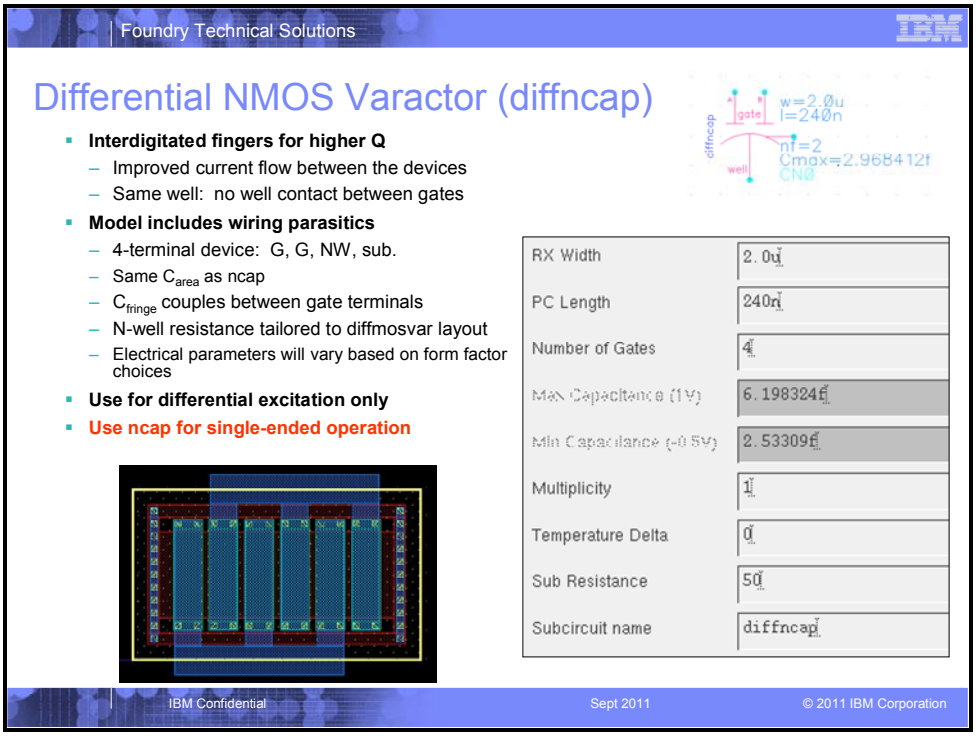
These NMOS capacitor devices are intended for both varactor and decoupling capacitor applications.



NMOS Varactor/Capacitor Pcell Options

The *ncap* and *dgncap* pcells generate an array of wired varactor gates. This example shows four gates by two diffusion islands for a total of eight varactor devices. Wiring parasitic resistance and capacitance corresponding to this array layout are included in the model.

Many of the devices accept an input for substrate resistance. This value represents the resistance between the device and the global substrate contact (often sub!). By default this is set to 50 Ohms, which is a reasonable value for most circumstances.

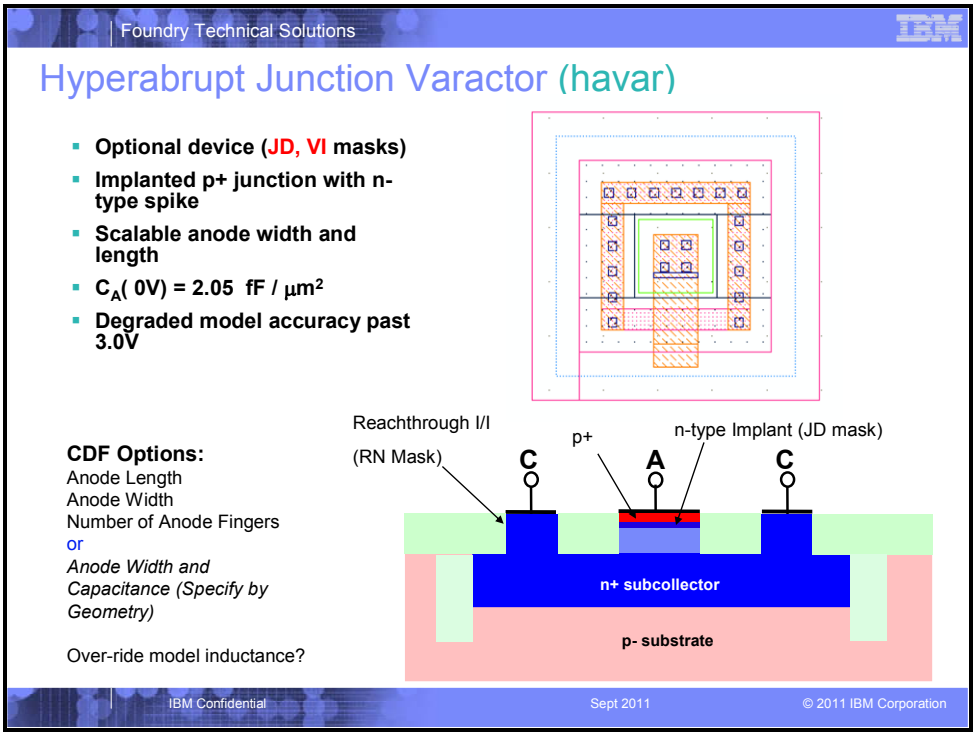


Differential NMOS Varactor (diffncap)

The NMOS structure of the *diffncap* is identical to that of the *ncap*. However, the differential NMOS varactor layout provides optimized performance for differential circuits. The two diodes share a common n-well so that the current path does not include the well contact resistance and higher Q is obtained.

The diffncap model includes wiring parasitics, gate-to-gate coupling, and n-well resistance. While the NMOS diode is the same as that in the ncap, ac characteristics will be different because of parasitic resistances and capacitances. The electrical parameters will be dependent on parameter choices.

The differential varactor is designed for "differential" applications only. They offer many advantages over the single-ended (regular) varactors, such as enhanced Q (~30-50% higher), reduced wiring resistance, better matching (devices are placed better in layout) and smaller footprint. However, for single-ended applications, the standard varactor (ncap) should be used. If the differential varactor is wired as a single-ended device, its Q will be much lower than the regular single-ended devices.

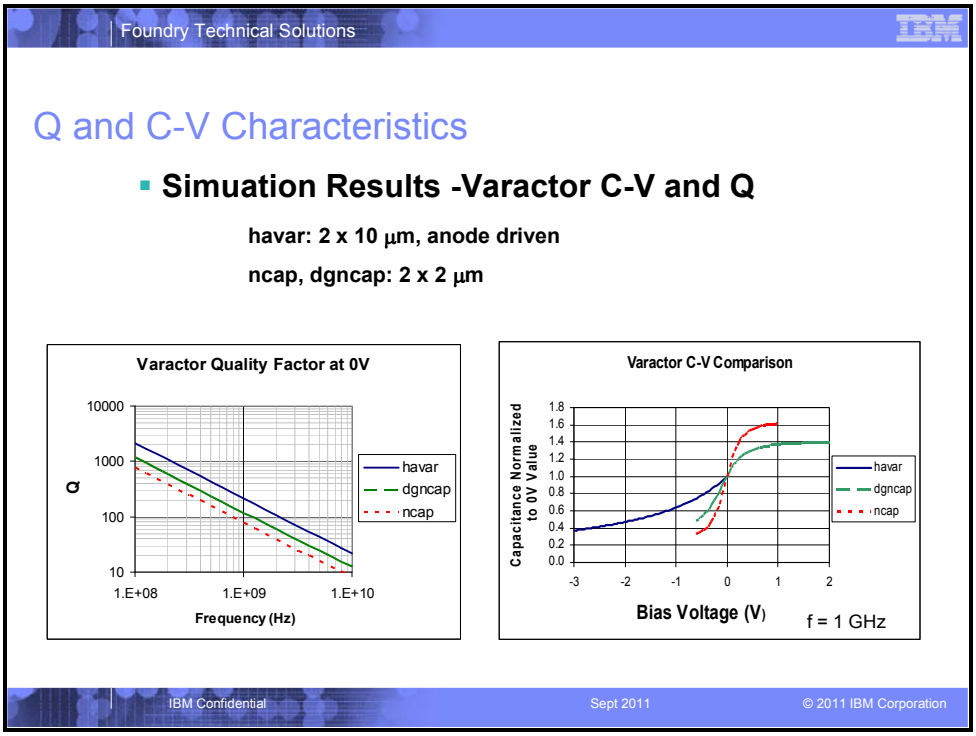


Hyperabrupt Varactor (havar)

The optional hyperabrupt varactor *havar* is a pn junction created from p+ S/D implant with an additional n-type implant just below the junction to create the hyperabrupt junction profile. This profile creates a more linear varactor with a large tuning range. The subcollector provides low resistance from the cathode contacts to the cathode side of the junction.

The *havar* model maintains a good fit to measured data through approximately 3V reverse bias. The fit is allowed to degrade beyond approximately 3V reverse bias in order to insure the best fit over the expected lower operating voltages.

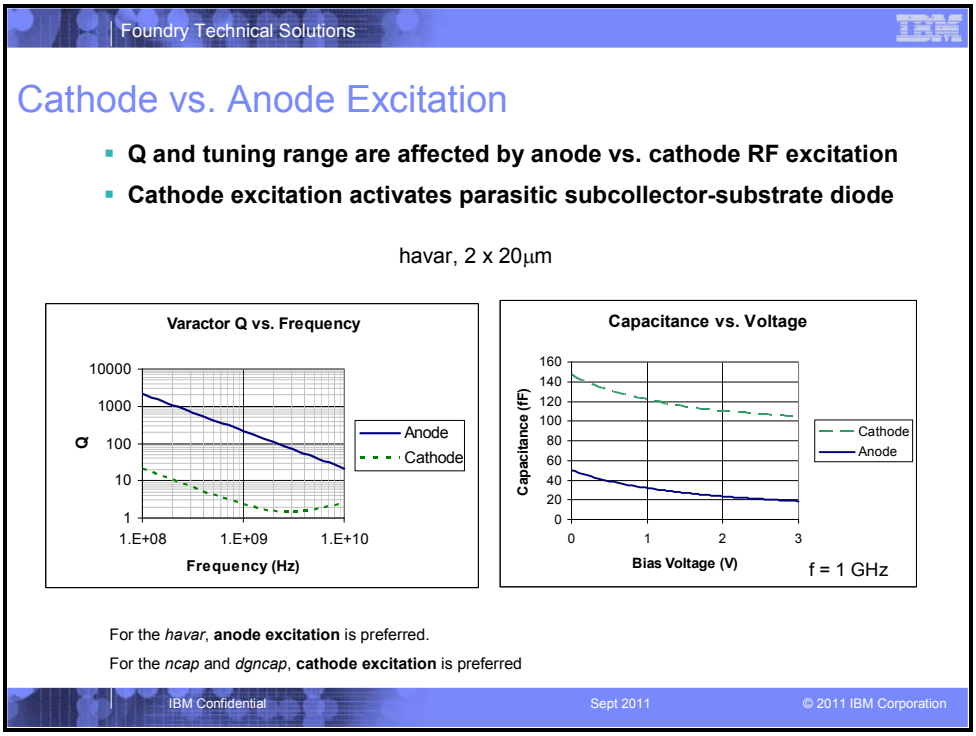
Note: This diode has not been characterized for high frequency forward biased operation.



Q and C-V Characteristics

The modeled quality factor and C-V relationships for the three varactors shown above illustrate the differences in the devices. The plots were generated using the same device sizes as described in the previous chart. The *havar* device has the highest Q factor. The MOS varactors have higher voltage tuning sensitivity than *havar*.

Varactor diode electrical characteristics depend on the physical form factor. Area and perimeter capacitances are different and will generally have different voltage dependencies. Also, wide devices have parasitic resistances between the terminals and the capacitance in the center of the device. These effects are included in the models, so designers will observe tuning range and Q differences based on form factor. Refer to the Model Reference Guide for additional plots and comparison of the models with measured results.

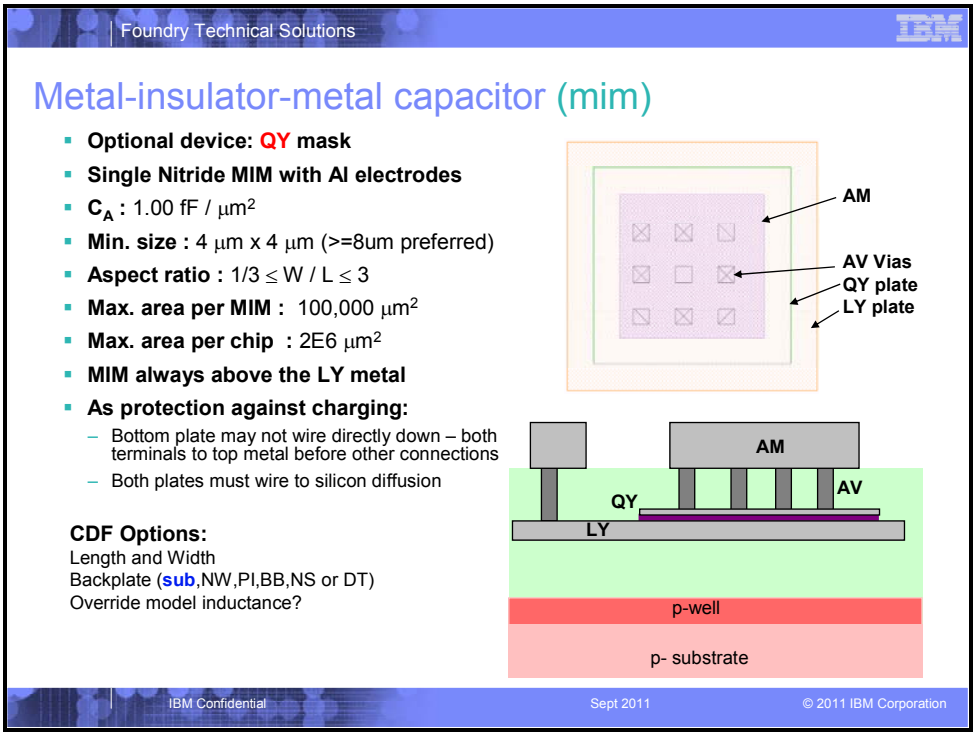


Cathode vs. Anode Excitation

All of the varactors have a significant parasitic junction between the n-type region and the substrate. For the *havar* this is the subcollector/substrate junction. For the nMOS devices the parasitic junction is between the n-well and the substrate.

Varactors should be operated with the n-type region at AC ground. Otherwise, the parasitic junction is excited in parallel with the varactor junction and the tuning properties and the quality factor are significantly affected.

The quality factor and C-V plots show the affects of the cathode vs. anode excitation on the *havar* device. For the *havar*, it can be seen that **anode excitation** is preferred. For the *ncap* and *dgncap*, the n-type region is the body, so **gate excitation** is preferred.



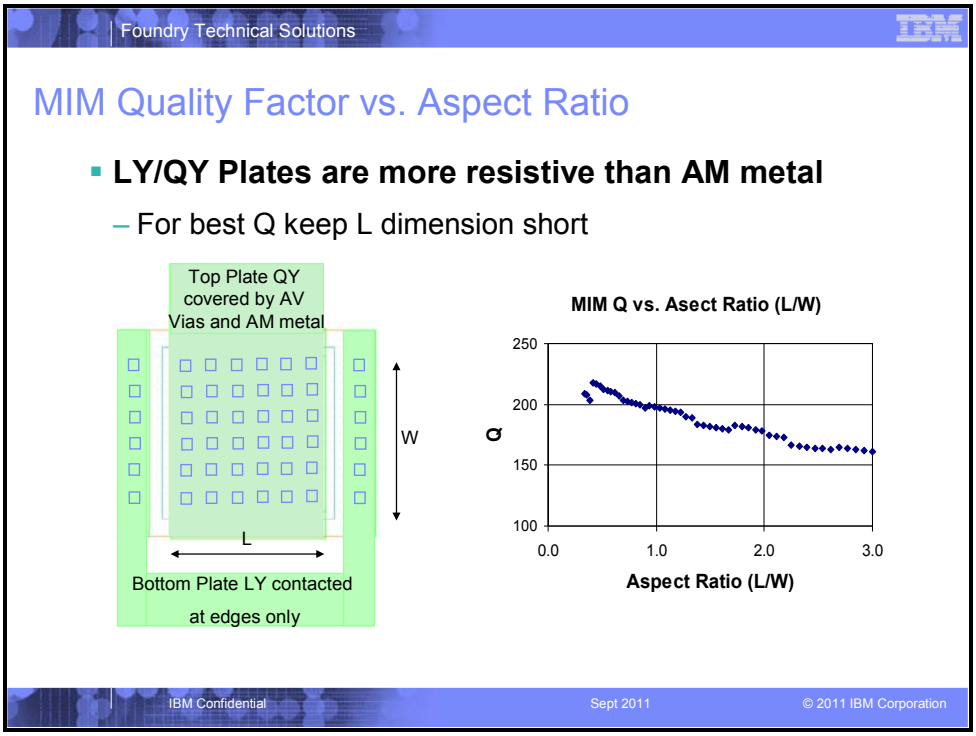
Metal-Insulator-Metal Capacitor (mim)

A single nitride metal-insulator-metal (MIM) is provided in the design kit. The MIM capacitor pcell *mim* uses an optional mask QY. QY defines the capacitor metal top plate which is separated from the LY aluminum metal level bottom plate by a thin nitride dielectric layer. The top capacitor plate is aluminum as well. The capacitance is 1.00 fF/μm^2.

The MIM aspect ratio may be no larger than 3:1 to assure accurate modeling. The maximum area of any single MIM is limited to 100,000 μm^2, and the total MIM area on any chip may be no more than 1 x 10^6 μm^2. These values were verified as meeting reliability targets at 3.3V, 85C, 100K power-on-hours and 10 FIT during the technology qualification. Further information and scaling to other reliability targets is given in the design manual.

In order to avoid charging damage during processing, the MIM bottom plate must be **c**onnected to the level of metal that is wired to the top MIM plate before connecting to lower metal levels. Damage is prevented since both plates of the capacitor float together during processing and avoid dielectric breakdown damage from plasma processes. Additionally, the MIM capacitor plates must be tied to a silicon diffusion once the capacitor is fully formed. MIMs are checked as part of the "Floating Gate/NW&Antenna". Tie-downs will be described further in the Layout Topics section.

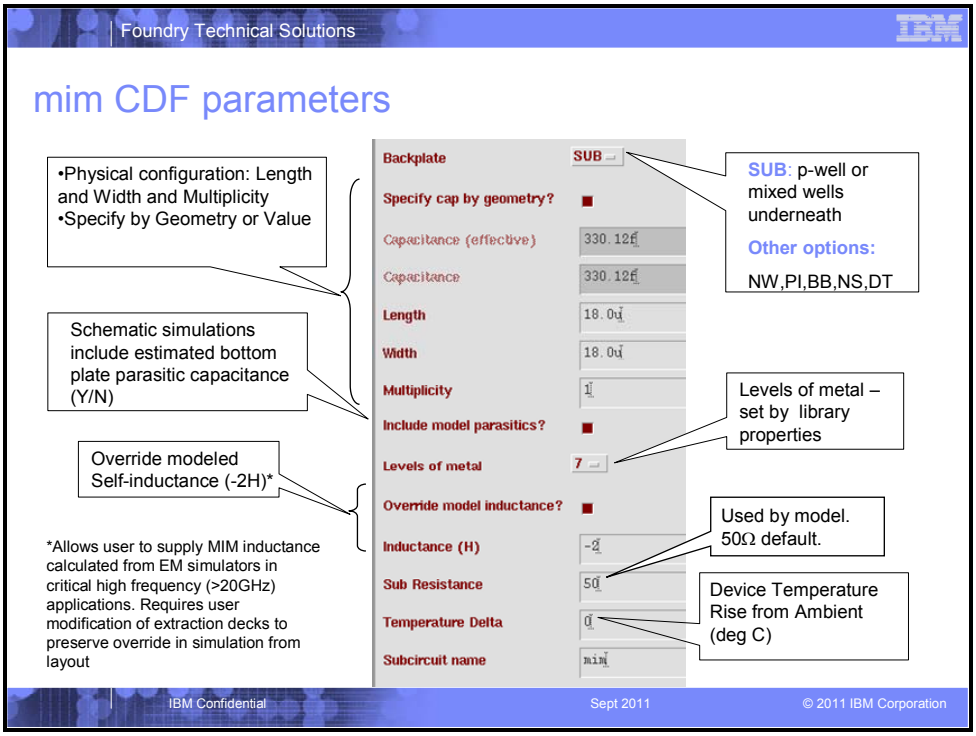
The *mim* pcell has many ground plane options: SUB, NW, PI, BB, NS or DT. The SUB option, shown in the slide, is used when the capacitor is placed over p-well regions, and for cases where the MIM is over mixed n- and p-wells (such as in CMOS logic books). The choice of ground plane is motivated by several factors. The NS option can aid in the reduction of noise coupling to and from the substrate by using the well as a shield. The SUB option is best when density is the primary concern, and the MIM is placed over circuitry using mixed n- and p-well, *e.g.*, CMOS logic. For the most accurate parasitic capacitance prediction, do not place the MIM over devices or wiring. The most accurate prediction of parasitic capacitance is when it is extracted from layout.



MIM Quality Factor vs. Aspect Ratio

MIM quality factor is dependent on aspect ratio. The following discussion refers to the pcell layout on the left of the slide. Top plate wiring is on level AM which is 4 µm thick copper. Connection to the top plate is through large AV vias distributed over the top plate area to form a low-resistance connection. The bottom plate connection is accomplished on the two ends of the device. Since the LY sheet resistance is much higher than the AM (sheet resistivity of QY is 1.8 Ω/sq, AM is 7 m Ω/sq, and LY is 23 m Ω/sq), this bottom plate path comprises the bulk of the device parasitic resistance. The best Q will be achieved when the W dimension is larger than the L dimension, which keeps the higher resistance path as short as possible. The W and L dimensions may be distinguished in the layout by the presence of a dummy shape "edgeLayer" "dg" which is placed by the pcell along the L dimension.

The effect of aspect ratio on Q is shown using simulation of a *mim* on the right of the slide. In this simulation, the dimensions were varied between 10 x 30 (LxW) and 30 x 10 keeping, within the limits of grid quantization, a constant capacitance.



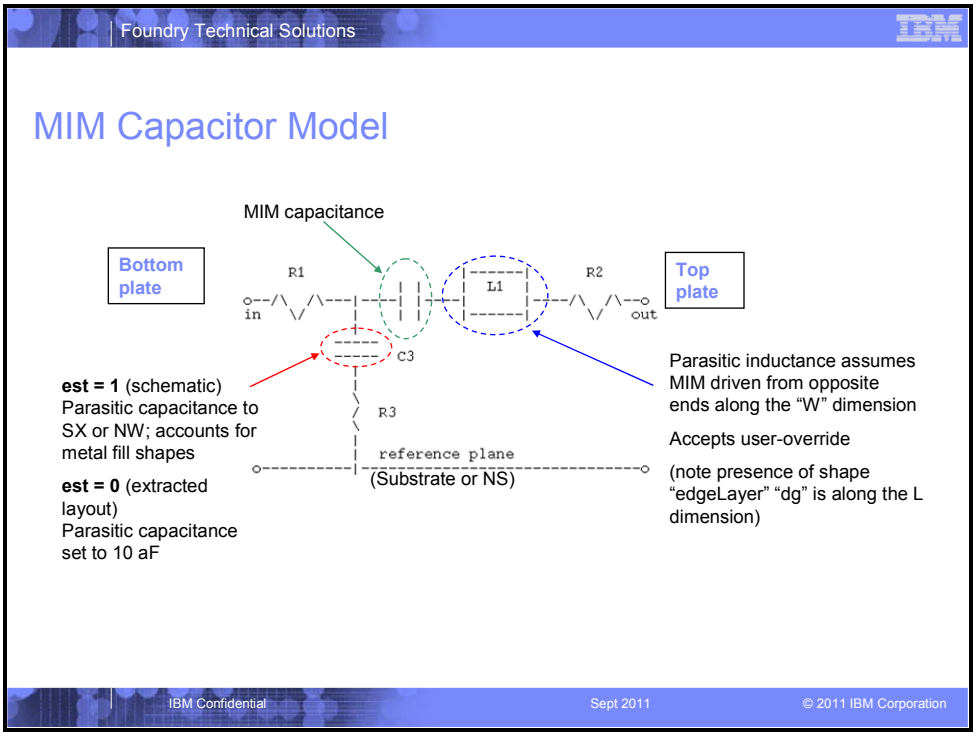
MIM Capacitor Parameters

The *mim* pcell offers multiple **Backplate** (ground plane) options. Physical configuration gives the length and width of the capacitor. The entry may be a combination of capacitance and length as shown or, by checking the **Specify cap by geometry?** box, the length and width can be provided. The form will also accept design variables.

Depressing the **Include Model Parasitics** button sets the model parameter “est”. When selected, the model will include the estimated bottom plate parasitic capacitance in the schematic simulation. When the device is simulated from layout, this switch is off and the parasitic capacitance must be extracted from the actual layout.

The **Override model inductance?** switch provides a means of overriding the parasitic inductance calculated by the model. This may be advantageous for very high frequency designs where the customer has access to a more accurate estimate of the MIM parasitic inductance obtained from an electromagnetic field solver. The “**-2H**” in the inductor override field is the default value in the cdf. The model file ignores negative values and uses the internally calculated parasitic inductance. When overriding the value, replace the **-2H** with the parasitic inductance calculated by other means.

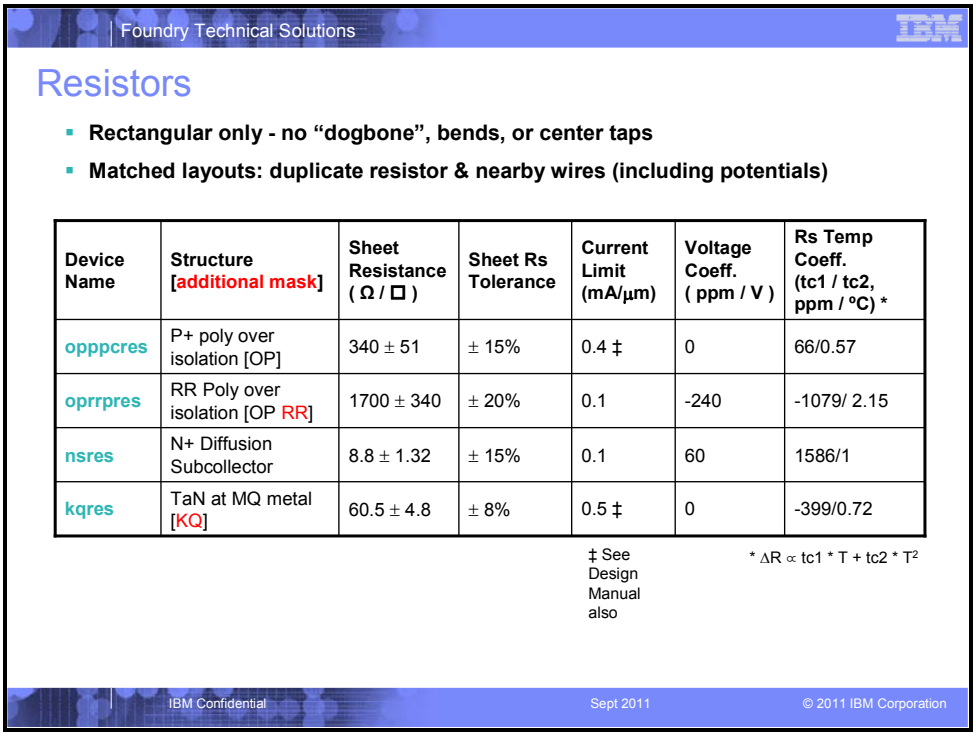
Many devices include the **Thin/Thick Metals** parameter in the properties form. This describes the levels of metal used in the design library and is used in simulation since the model needs information about the metal stack to determine the parasitic capacitance to the ground plane. The value is automatically set by the library properties.



MIM Capacitor Model

The MIM capacitor model topology is shown above. The MIM capacitor appears between the top and bottom plate terminals in series with metal resistance and the parasitic inductance element L1. The model calculates the parasitic inductance under the assumption that the capacitor is driven along the W dimension. For general applications the MIM inductance is dominated by the wiring and is not critical. Layout can be accomplished as most convenient. If the MIM inductance is critical, designers should wire the MIM as the model assumes, or override the inductance with a value computed using third-party electromagnetic simulation software.

The parasitic capacitance to substrate is captured by elements R3 and C3. The C3 term is controlled by the parameter "**est**." To include the bottom plate parasitics during schematic simulation, est is set to 1. In layout simulation, est is always set to 0. Parasitic extraction tools will compute the bottom plate capacitance terms from the layout information. IBM design preparation tools will automatically add RX, PC, and metal pattern fill under the MIM. Model calculations account for the presence of fill shapes.

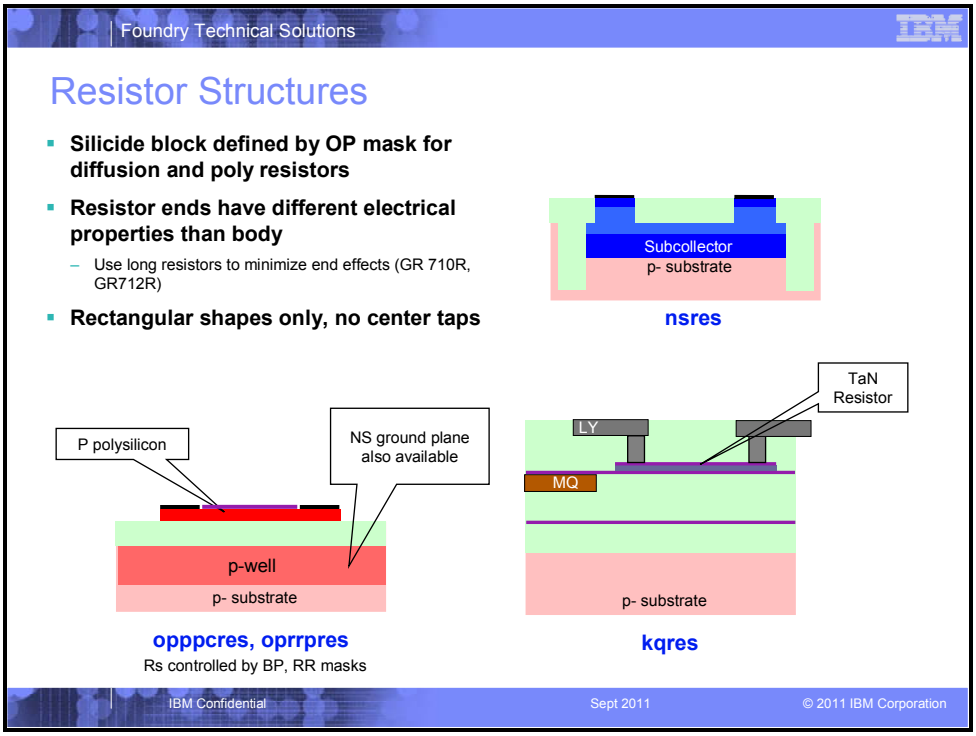


Resistors

BiCMOS8HP provides four types of resistors. The *opppcres* is an unsilicided polysilicon line that receives the same implants as a PFET gate. A high resistance polysilicon resistor, *oprrpres*, is available where a larger resistance value is needed. The *nsres* is an n+ "diffusion" subcollector resistor formed from an unsilicided NFET source/drain junction. The *kqres* is a tantalum nitride metal resistor that resides at the uppermost 1X wiring level, i.e. right below the 2X MQ wire level. The *oprrpres* and *kqres* resistors are process options requiring RR and KQ masks respectively.

Only rectangular resistors are allowed. Resistors may not be of a "dog bone" configuration or have bends. Only two sets of contacts are permitted. Two resistors can not share a single n-well, RX, polysilicon, or Kx shape by adding a third set of contacts in the middle of the resistor. Series resistors with separate shapes must be used instead.

The *opppcres* polysilicon resistor may be preferred over *nsres* because of its low temperature and voltage sensitivity, and the low capacitance to the ground plane below. In addition, any latch-up concerns are removed because the device does not include a parasitic diode junction. The *oprrpres* resistor has the highest sheet resistivity of the resistors, allowing for the most compact layout for high value resistors. The *kqres* has the best tolerance specification. The *nsres* has the lowest sheet resistivity which makes them more suitable for small value resistors.

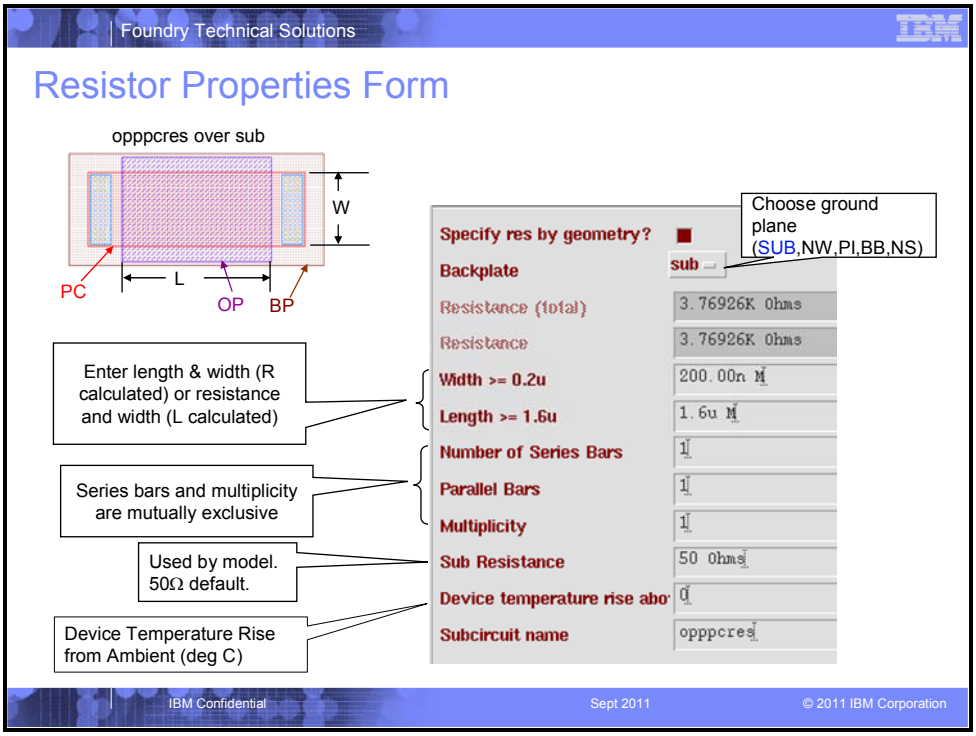


Resistor Structures

The cross-sectional diagrams of the n+ diffusion subcollector, polysilicon and tantalum nitride resistors are shown in the slide. The polysilicon resistor drawing shows the "SUB" ground plane option. Polysilicon resistors and the tantalum nitride resistor *kqres* may also be placed over n-well (NW), triple-well (PI), undopded substrate (BB) or n-subcollector (NS). The "SUB" option allows other devices underneath *kqres*. However, the MQ wiring is not permitted under kxres resistors (design rule KQ4).

To prevent shorting of the polysilicon resistor, silicide formation is blocked by a silicon nitride film (OP mask).

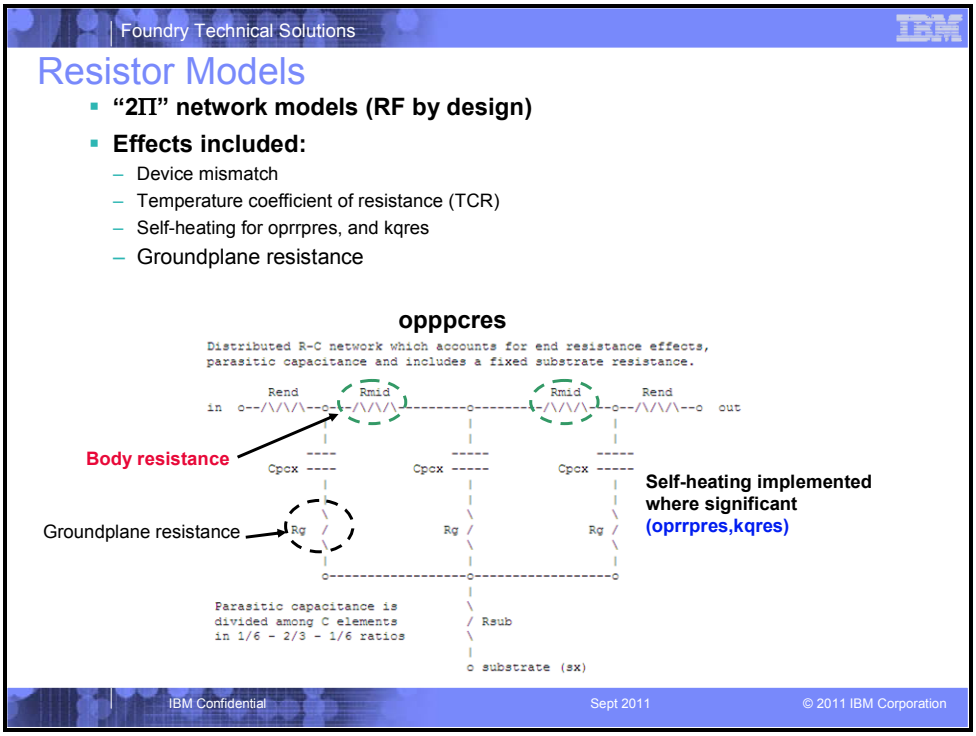
The resistor contact region at both ends can constitute a significant fraction of the total resistance. The end regions have different temperature dependence and tolerance than the body region. For best resistor tolerance and matching, design the resistor so that end effects are small relative to the total resistance value. Design rules 710R and 712R give suggested minimum resistor lengths.



Resistor Properties Form

The top view of a polysilicon resistor shown at the bottom right side of the slide depicts the placement of the mask layers used to define the device. PC defines the body. OP denotes areas that are blocked from silicide formation, and BP indicates that the area receives the p+ source/drain implant.

The polysilicon resistor properties form is shown in the slide above. The resistor properties form accepts geometrical inputs of length and width. Additionally, designers may specify the resistance and width, and the length will be calculated. The supported backplanes are SUB, NW, PI, BB and NS. NW, PI or NS is typically used to provide noise shielding from the substrate. SUB provides a lightly doped substrate region under the device to lower substrate coupling. The SUB option places the resistor over p-well. Series bars options places a set of resistors in series and wires them together on M1. The **Multiplicity** is also supported, but may not be used in combination with the **Number of Series Bars** option.

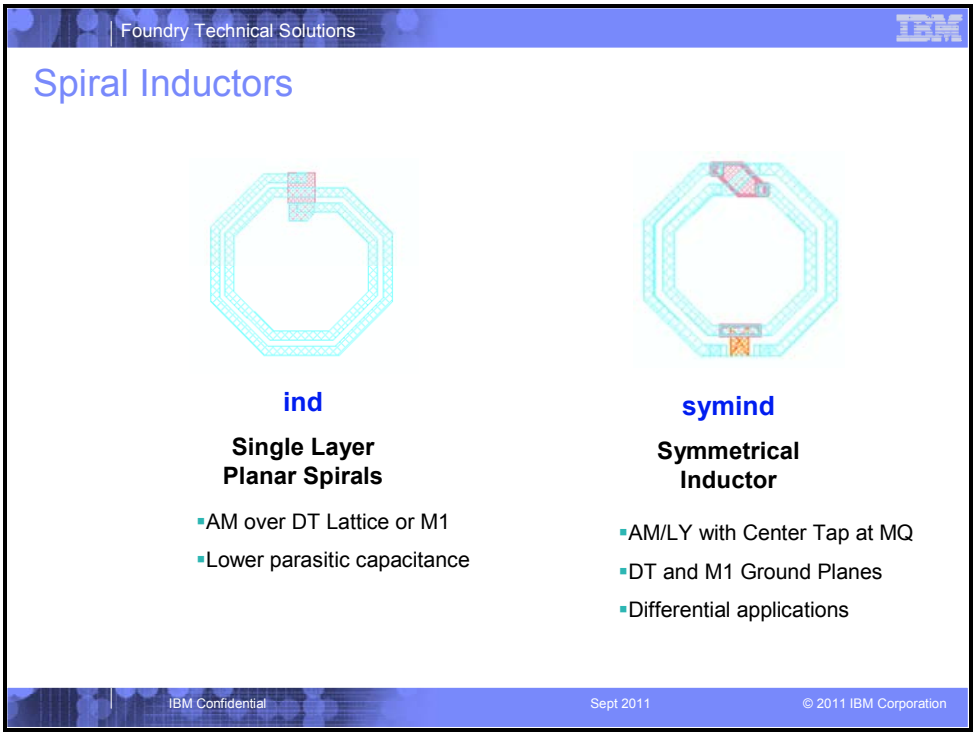


Resistor Models

IBM resistor models use a "2Π" topology as shown in the slide. Admittance to the substrate or backplane, represented by the diode junction for the *opppcres*, is divided into three components, with 2/3 in the center leg and 1/6 on each end. The end resistances appear in the "Rend" components. Body resistance is divided into two parts. The groundplane resistance is also modeled. The network provides good agreement with measurements at RF frequencies.

All resistor models include tolerance and mismatch parameters plus temperature coefficients relating resistance change with substrate temperature.

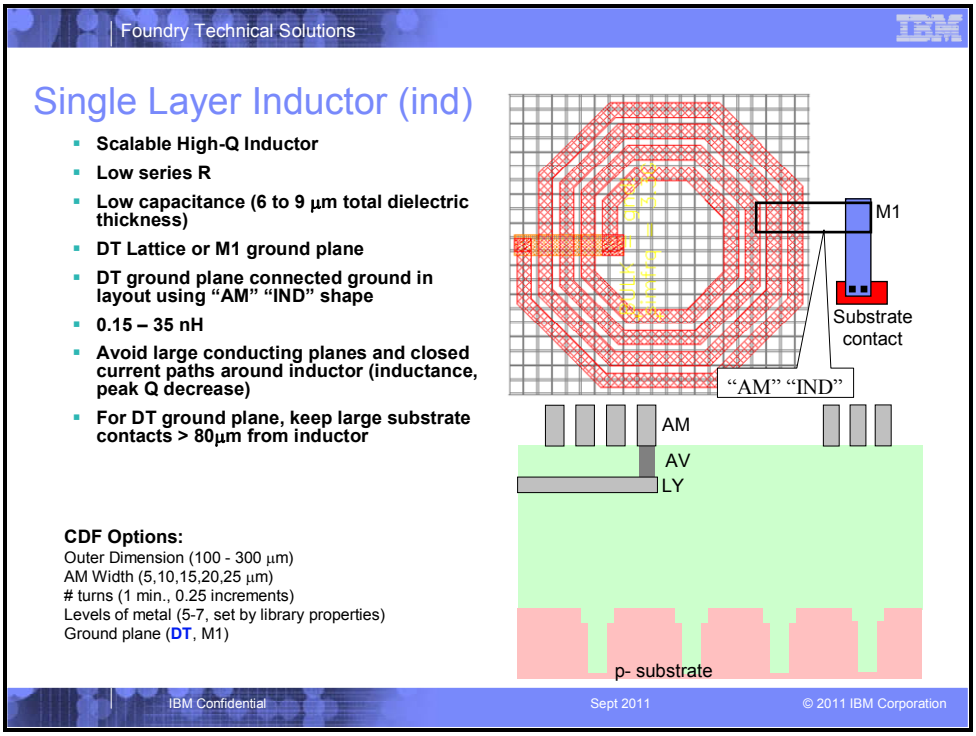
Additional effects are included where significant. Self heating is included in the models for *oprrpres* (the high-resistance polysilicon resistor), and *kqres*, since they have non-negligible self-heating effects.



Inductors

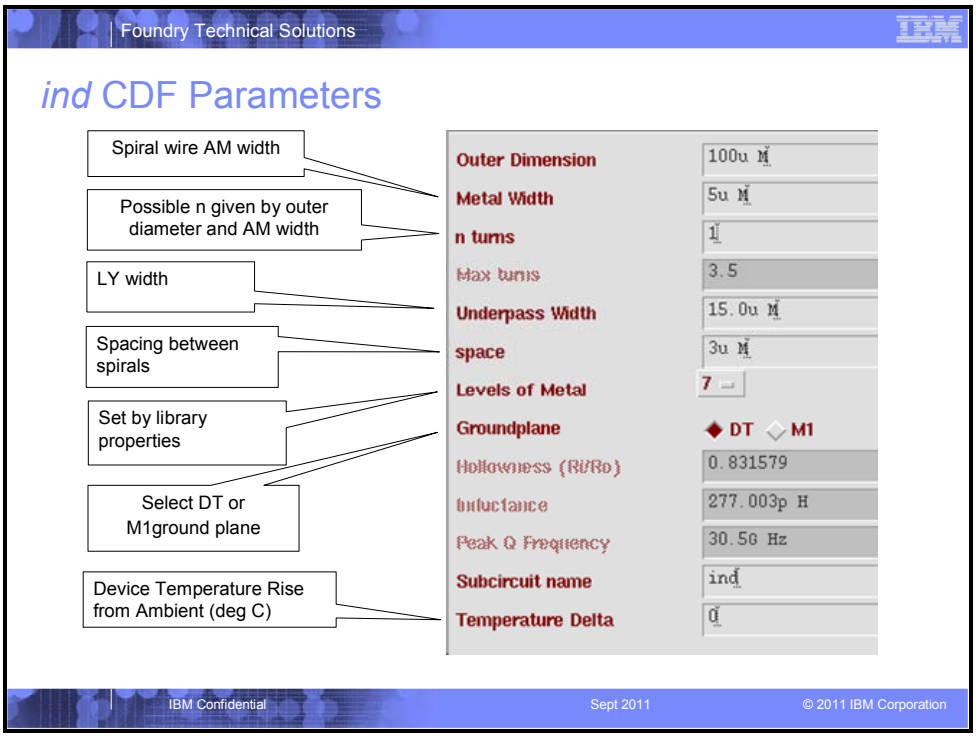
The BiCMOS8HP technology offers scalable, high-Q inductors with low parasitic capacitance.

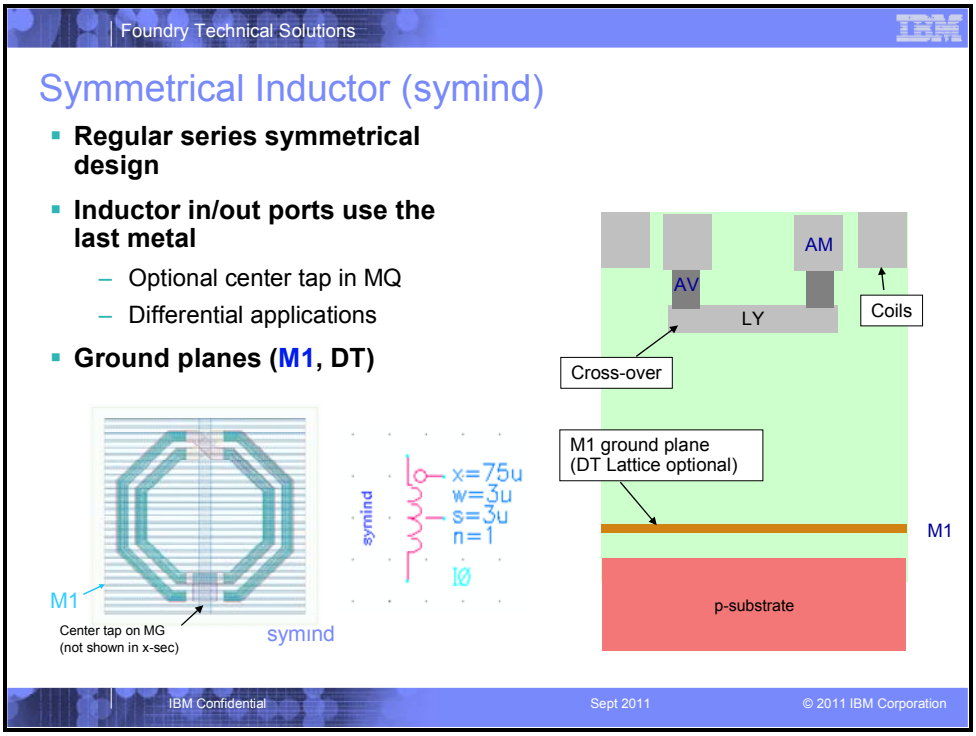
The *ind* device is the standard spiral where the innermost end of the coil is accessed through an underpass wire. This device offers the lower parasitic capacitance. The *symind* is a symmetrical single layer inductor using the LY and AM to create a symmetrical low resistance inductor that is ideally suited for use in differential circuits. As will be explained in an upcoming chart, differential excitation halves the parasitic admittance to the substrate and produces the highest Q for a given configuration.



Spiral Inductor (ind)

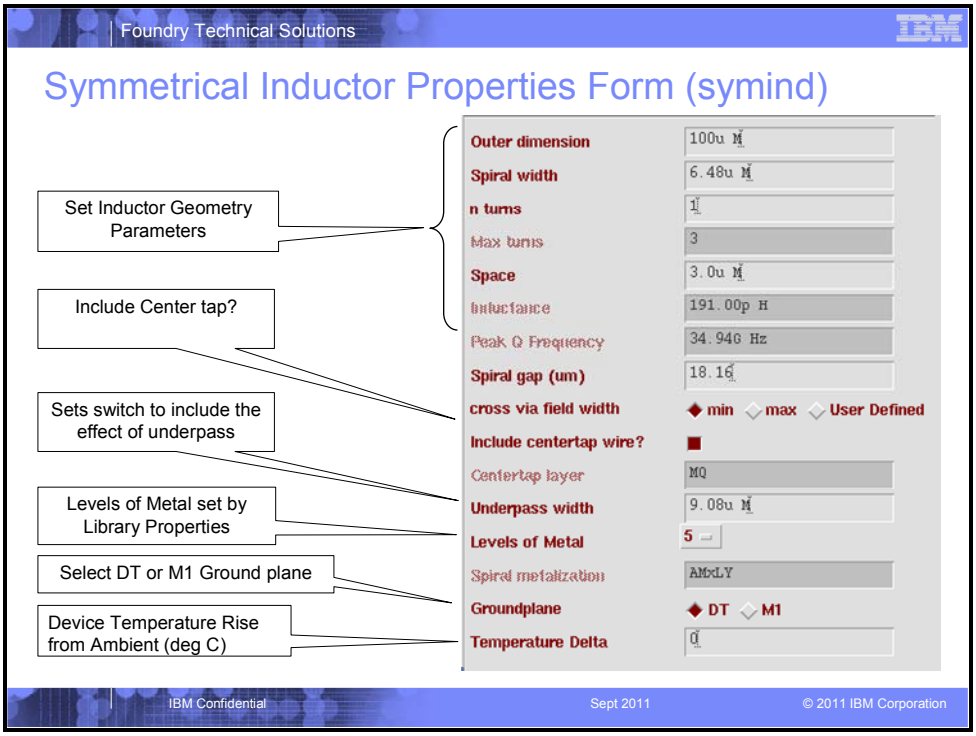
The spiral inductor pcell *ind* provides substantial flexibility: the outer diameter, inductor coil width, number of turns, underpass width, and ground plane can be varied to achieve the desired inductance and performance characteristics.





Symmetrical Inductor (symind)

The BiCMOS8HP technology offers scalable, high-Q symmetrical inductors with low parasitic capacitance, a regular single layer series inductor *symind.* The symmetrical layout is more compact than using two asymmetrical spiral inductors, and is more convenient to wire because the ports are adjacent to one another. A center tap connection is available in MQ.



Symmetrical Inductor Properties Form

The symmetrical inductor pcell *symind* provides substantial flexibility: the outer diameter, inductor coil width, and the number of turns can be varied to achieve the desired inductance.

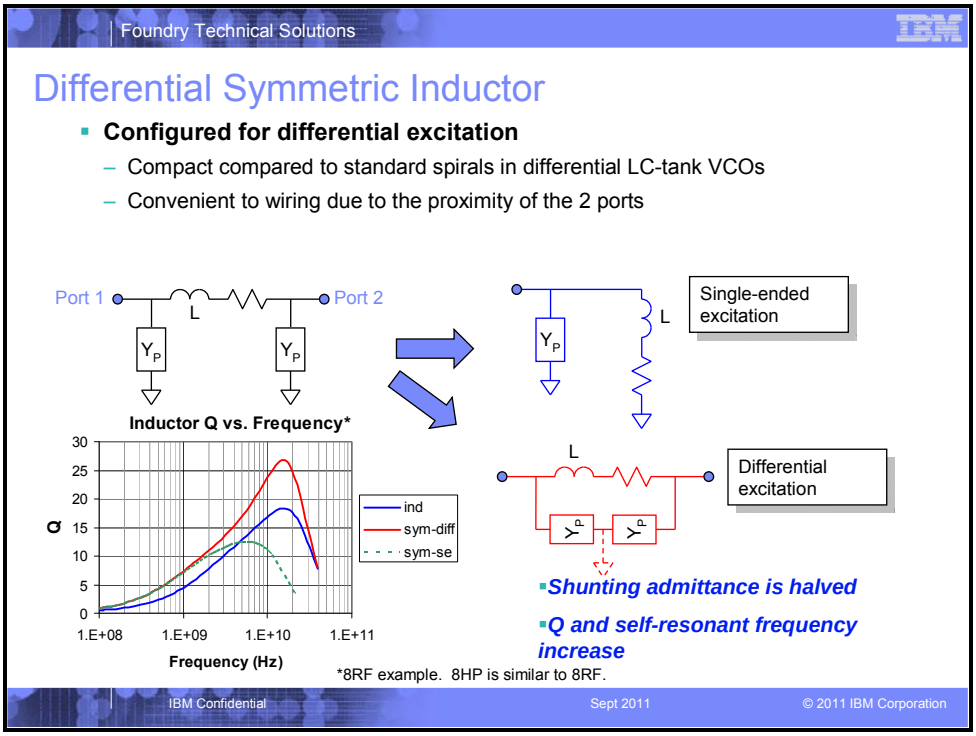
Inductor configuration is specified by the **Outer dimension**, the **Spiral width**, the **number of turns**, the **Space** of the inductor wire, and the **Underpass width.** The **Spiral gap** is automatically adjusted to pass the DRC rules or it can be set to a higher value if desired.

The metal layers used to build the inductors are fixed, AM/LY with optional center tap at MQ.

The **Level of Metal** is fixed since it is set by the library properties. It is displayed in the properties form for reference only. It can not be set by the user in the inductor properties form.

The **Groundplane** choices are M1 or DT. The choice criterion is discussed later on.

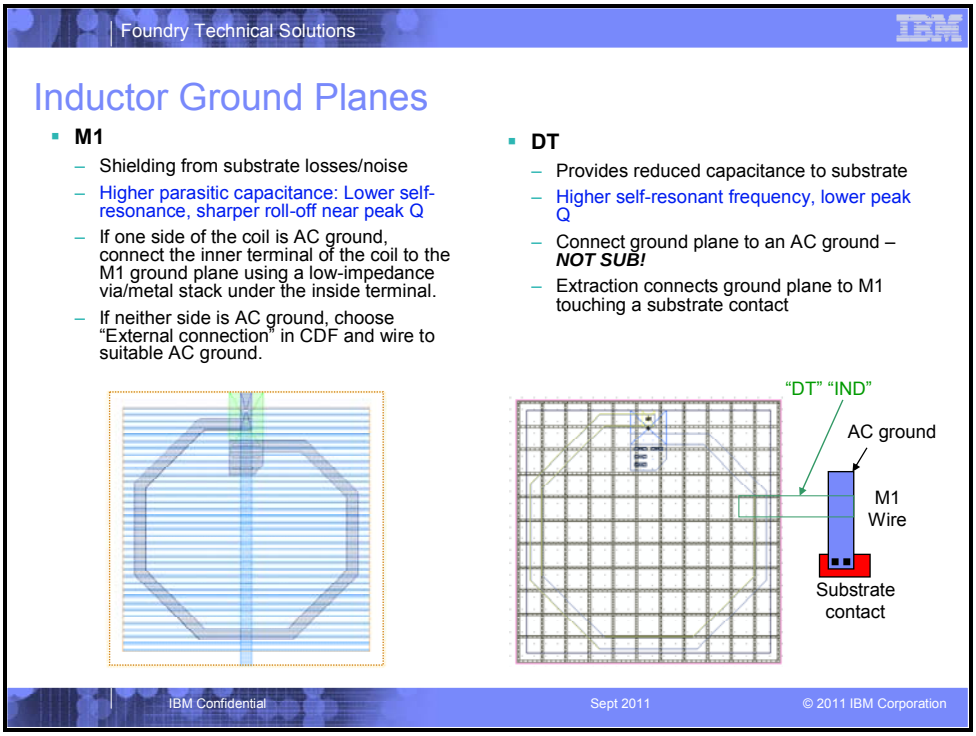
The Component Description Format (CDF) also provides several informational parameters: the approximate inductance, and the approximate peak Q frequency.



Differential Symmetric Inductor

The symmetric inductor *symind* can be wired for differential circuits. A differentially driven inductor will have better performance than a single-ended application.

Performance benefits of the differential configuration are shown in the bottom left figure. *This example is taken from the 8RF design kit. It is discussed here only to illustrate the difference between configurations using two asymmetrical planar inductors and symmetrical inductor.* Consider the simplified inductor schematic shown in the upper left of the chart. Included are the inductor, the parasitic series resistance, and the parasitic admittances to the substrate or ground plane (Y_P). The schematic representing single-ended excitation appears on the upper right. Port 2 is grounded and the inductor/resistor is in parallel with the parasitic admittance. Compare this to the schematic for differential excitation just below. In this configuration, the parasitic admittances appear in series such that the admittance is halved. The result is higher Q and self resonant frequency. The plot of simulated Q vs. frequency on the lower left of the chart shows this difference quantitatively. Three inductors use the same number of turns, coil width, and outer diameter. A standard spiral inductor (*ind*) is shown in the blue solid line achieving a peak Q of about 18. The red solid line applies to a symmetrical inductor driven differentially. Peak Q in this case is about 27. For comparison, the same symmetrical inductor driven in a single-ended fashion produces the dashed green line. Note the difference between peak Q and the frequency of peak Q depending on single-ended vs. differential excitation. The *ind* device falls between the two because it uses only a top metal coil and therefore has lower substrate parasitic coupling.



Inductor Ground Planes

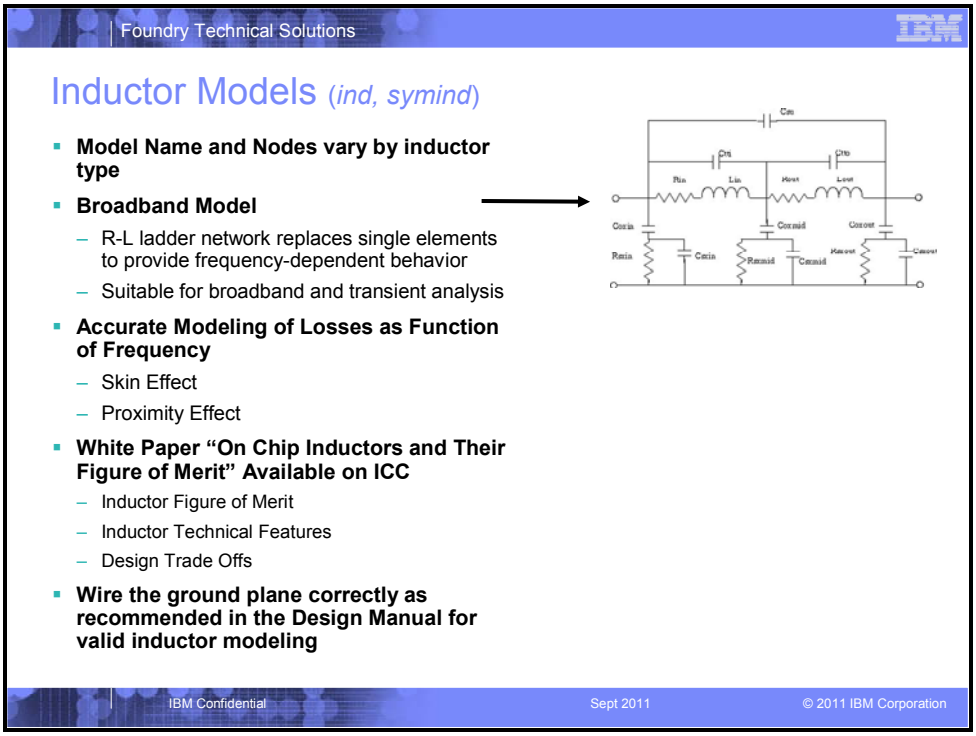
Depending on the self-resonance frequency and quality factor, Q, requirements, choose a ground plane appropriate for the particular application.

There are two ground plane choices available for the inductors in BiCMOS8HP: M1 and DT.

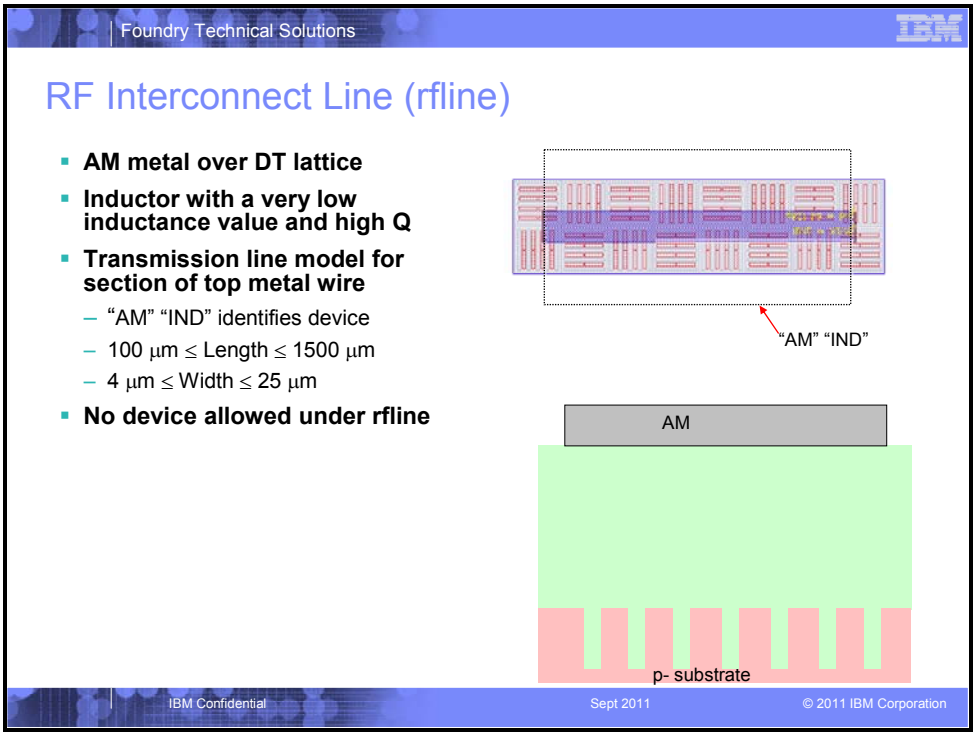
The M1 option, shown on the left, uses an array of M1 wires as a shield to isolate the inductor from substrate noise and prevents induced currents in the substrate which lead to lower Q. The drawbacks of the M1 ground plane are higher parasitic capacitance with resulting reduction in the self-resonant frequency, and a sharper roll-off of Q above the peak Q. When using the M1 ground plane and one side of the coil is AC ground, connect the inner terminal of the coil to the ground plane using a via/metal stack under the inside terminal.

The DT option is shown on the right. The DT is a deep trench mesh. It has higher self-resonance and lower peak Q compared to M1 ground plane.

Ground plane connections: When using the M1 ground plane the inductor backplane is defined as the M1 grid. For the DT backplane, the third terminal is defined as an ideal AC ground. Model results will be invalid if the DT backplane is connected to the substrate node (sub!). To indicate the AC ground backplane connection in layout for extraction and LVS purposes, use a pseudo-wire on level "DT" "IND" to connect the DT region to a nearby M1 line that is both an AC ground and connected to a substrate contact. The "DT" "IND" dummy layer does not control any physical features on the wafer.



Inductor Models

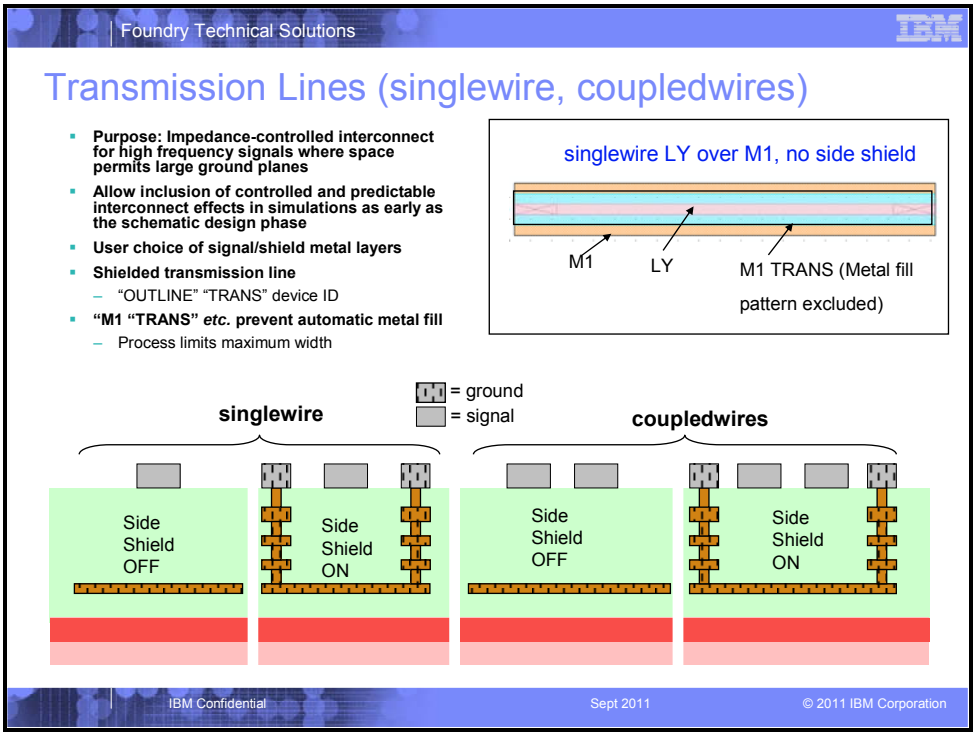


RF Interconnect Line (rfline)

The *rfline* device provides a transmission line structure with an accurate high frequency model. It is typically used as an inductive element for applications requiring low inductance with relatively high quality factor.

The transmission line is on level AM. Device recognition for extraction and LVS is accomplished using a marker shape on dummy layer "AM" "rfline."

The line length must be between 100 and 1500 μm long, between 4 and 25 μm wide, and is placed over BFMOAT. The device receives reduced auto-generated pattern fill on levels RX and PC. The model includes the effect the pattern fill (or exclusions) that the device receives in IBM data preparation.

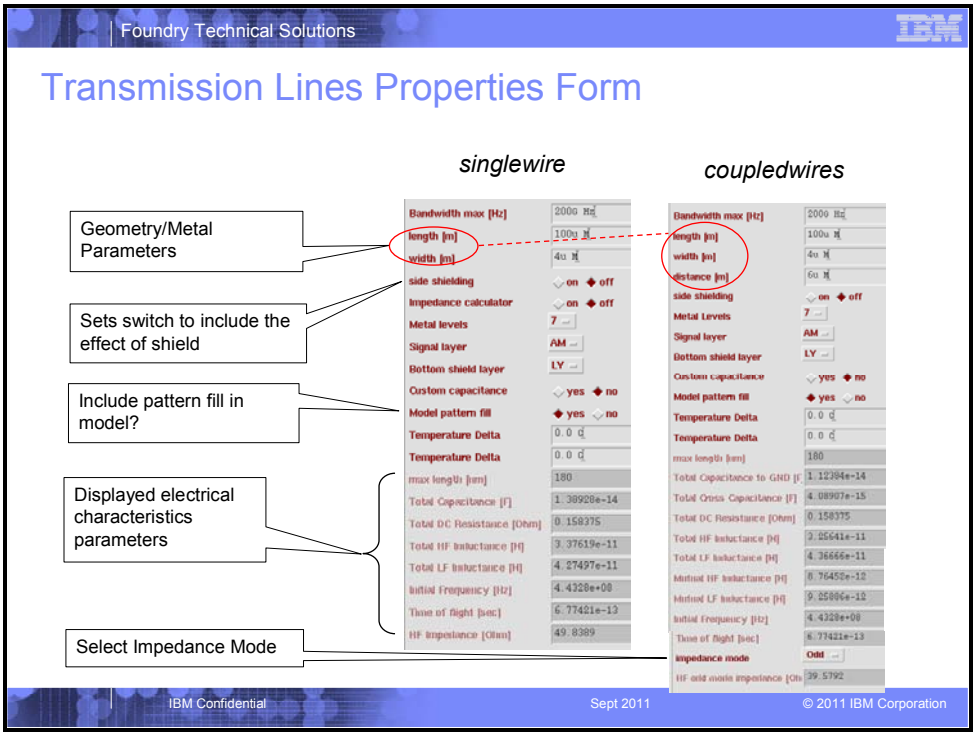


Transmission Lines (singlewire, coupledwires)

The elements *singlewire* and *coupledwires* are microstrip transmission line structures that incorporate one or two wires, a metal ground plane, and optional side shields. These microstrip transmission lines are most appropriate for applications where precise impedance and phase characteristics are desired, and where defined ground planes may be placed in the layout, such as for routing of RF signals between RF circuit blocks. These devices offer controlled and predictable transmission line effects to be included in simulations as early as the schematic design phase.

The line and ground plane are on the levels chosen by the designer. The ground plane and signal lines on 1X and 2X levels are slotted lengthwise to enable BEOL polish processes. Optional side shields are composed of a wire on each side of the transmission line(s) that is connected to the ground plane every 50µm by stacked vias.

In order to assure repeatable electrical characteristics, automatic metal fill shapes are excluded on the wire layer, and layers between the wire and the ground plane. This is accomplished by the shapes on "Mx" "TRANS." Device recognition is accomplished through the dummy shape on "OUTLINE" "TRANS."



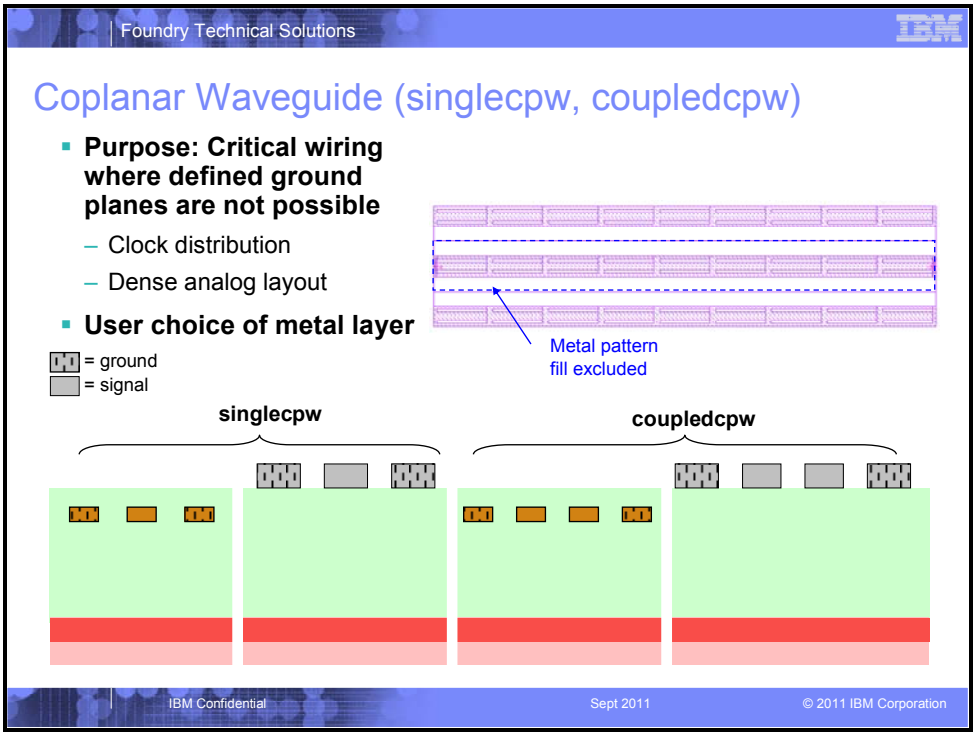
Transmission Lines Properties Form

The transmission lines (*singlewire* and *coupledwires)* properties forms are shown above. Select the transmission line geometry and metal layers using the **length**, the **width**, the **Signal layer**, the **Bottom shield layer** and the **distance** (for coupledwires only). The **Side shielding** may be optionally selected if desired. The width of the ground plane is a function of the input parameters and is limited by the maximum allowed width of the ground plane wire (50 µm for M1 etc.). Other width and placement limitations may arise because “Mx” “TRANS” shapes may impede metal fill to the degree that local pattern density will be too low.

There are many pertinent electrical characteristics displayed for designer’s aid at the bottom of the parameter form.

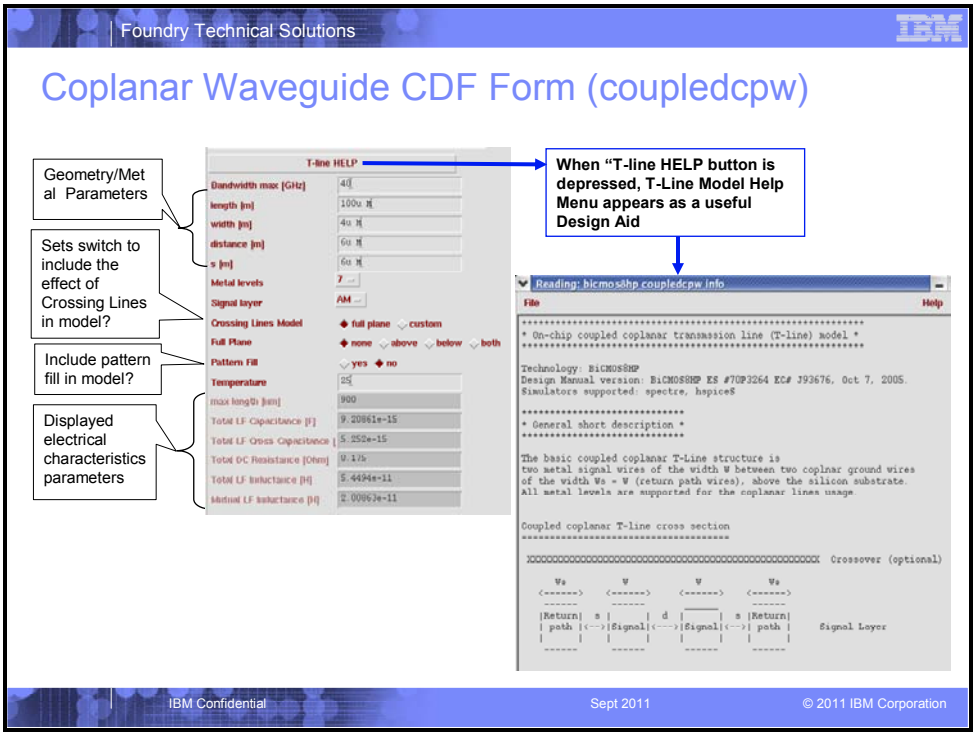
If the **Impedance calculator** switch is set to “on” (*singlewire* only) then additional parameters are displayed at the frequency of interest.

For *coupledwires*, there is an additional switch, the **Impedance Mode,** for calculating the impedance. Choices are the **even**, the **odd** and the **hybrid**. Select the correct mode depending on the excitation.



Coplanar Waveguide (singlecpw, coupledcpw)

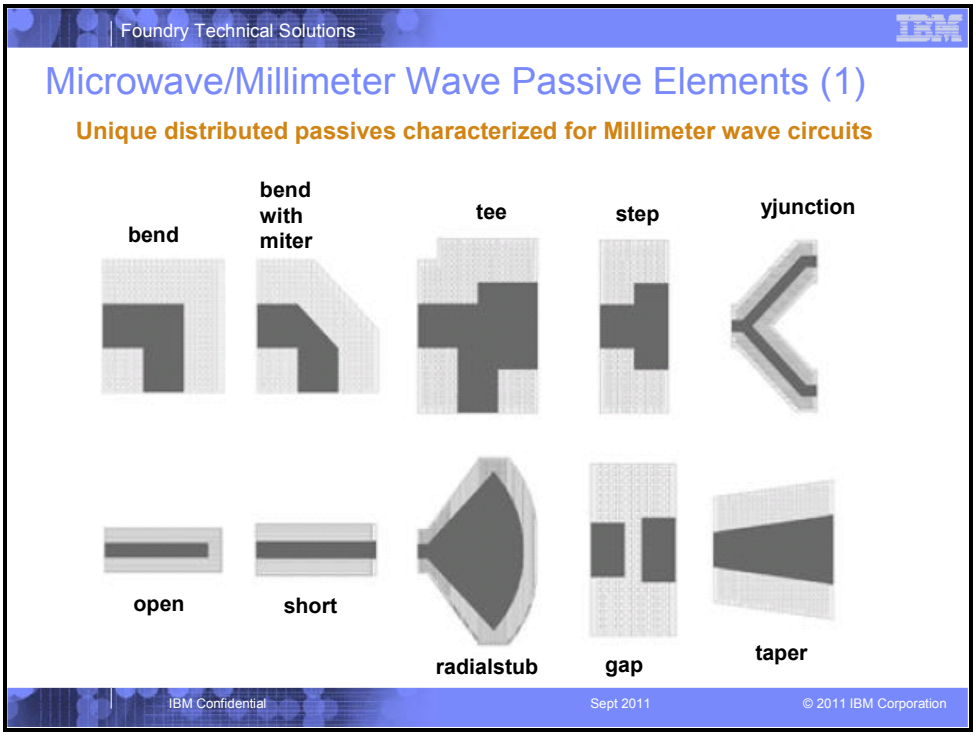
Coplanar waveguide devices offer a transmission line structure for critical signals where it is not possible to provide defined RF ground planes. Examples of these applications are high speed clock distribution networks and routing of signals in dense analog circuit blocks. The signal line and ground lines occupy the same metal level. The *singlecpw* has one signal line between two ground lines while the *coupledcpw* structure has two signal lines between two ground lines. The designer may choose the metal level used for the transmission lines.

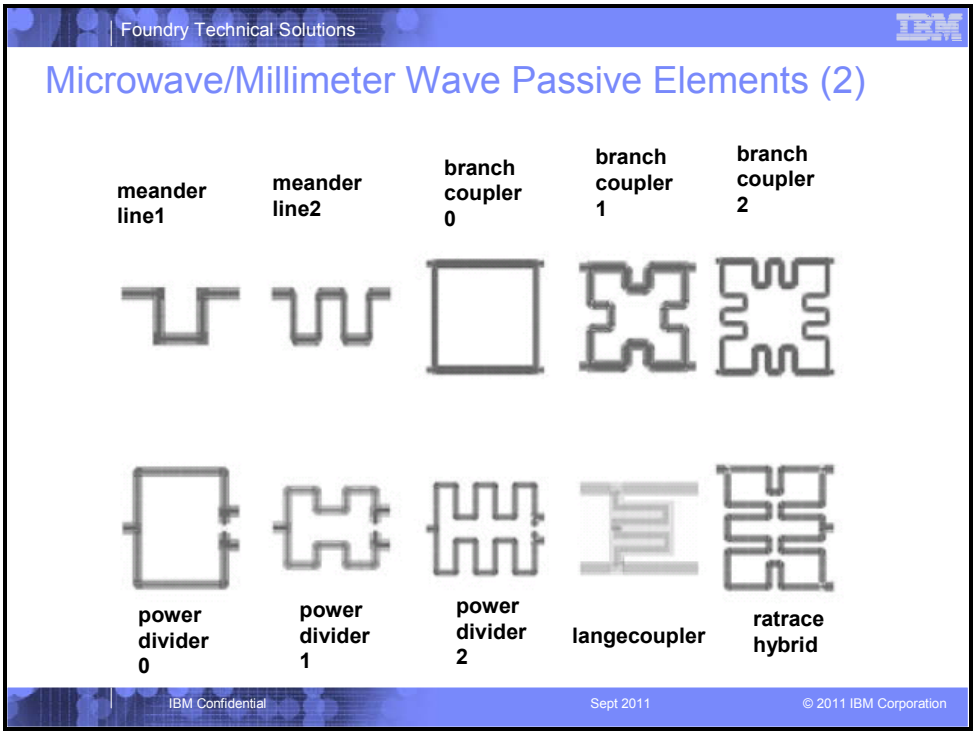


Coplanar Waveguide CDF Form

The CDF form for the coplanar waveguide *coupledcpw* is shown the chart above. Device geometry is facilitated using the waveguide **length**, **width**, **distance** and **spacing** selections. If model should include the effect of crossing lines and pattern fill, then **Crossing Lines Model** and **Pattern Fill** fields should be set to **Full Plane** and **Yes** respectively. As an aid to designer, many electrical parameters from the call backs are also displayed in gray for quick reference.

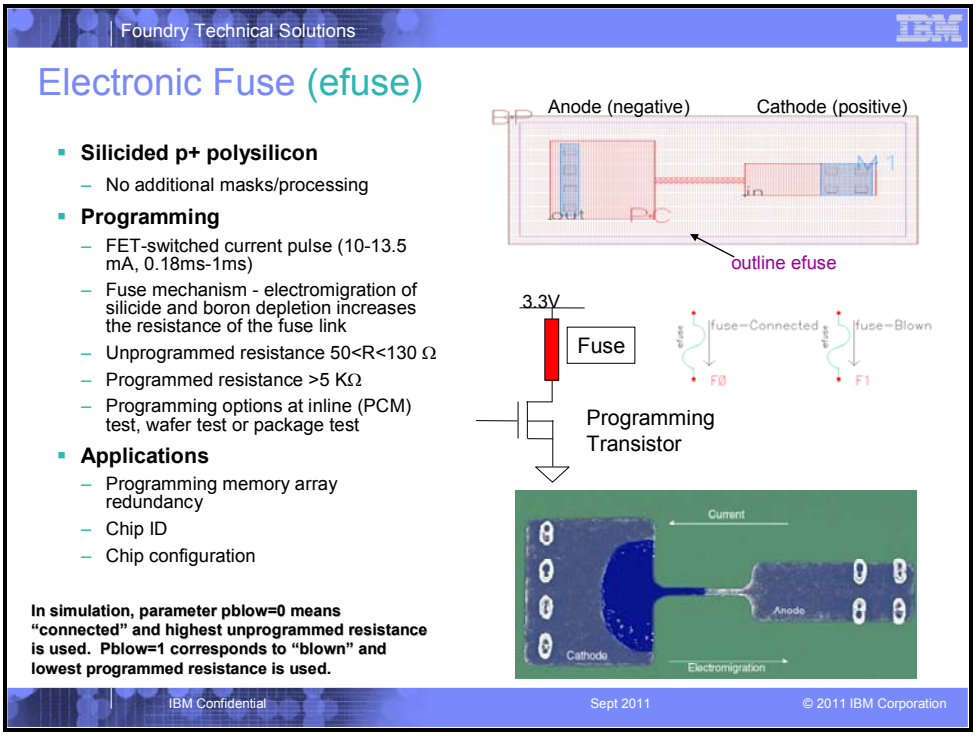
Transmission model aspects are also displayed by depressing the **T-line Help** switch.





Microwave/Millimeter Wave Distributed Passive Devices

BiCMOS8HP offers many modeled RF passive devices for RF/Microwave/Millimeter wave designs including bends, tees, step, junction, open, short, stub, gap, taper, meander lines, branch and Lange couplers, power dividers and retrace hybrids. All device models are hardware correlated to 110 GHz. Please see Section 4.16 in Design Manual for more details.



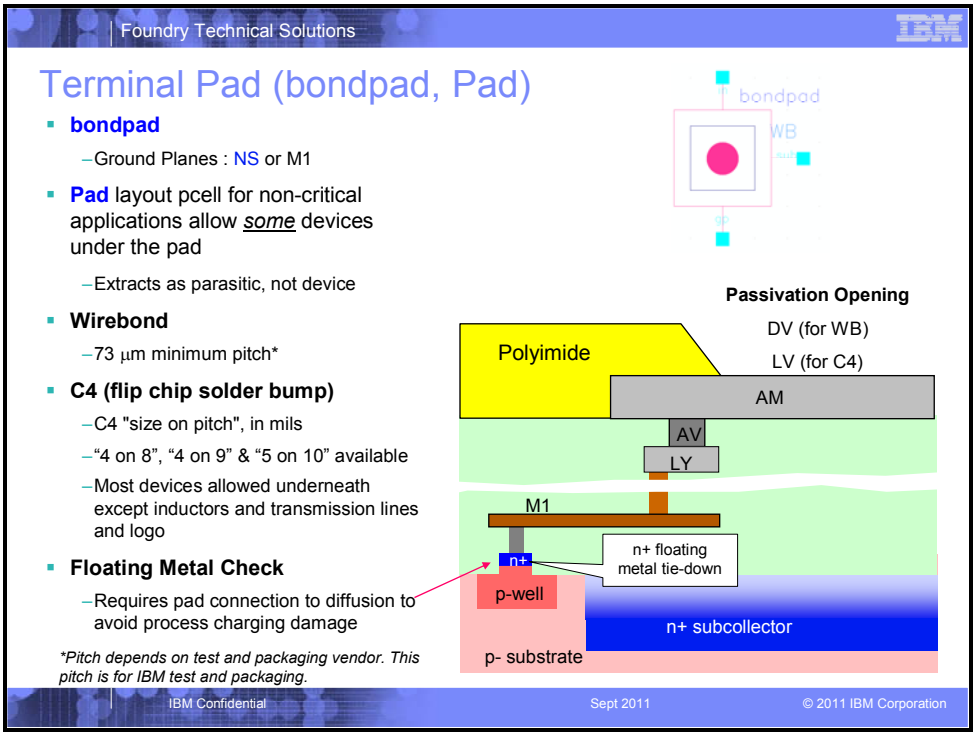
Electronic Fuse (efuse)

The electrically programmable fuse device *efuse* takes advantage of the electromigration properties in silicided polysilicon. No additional processing is necessary to create the fuse structure.

The efuse is blown by passing a current pulse of 10-13.5mA through the fuse for a period of 0.18-1ms. This is accomplished by switching the fuse between 3.3V and ground using a large programming transistor. The resulting current and heating causes alteration of the silicide layer and the polysilicon. This creates change in the fuse resistance from less than 130 Ω to greater than 5 KΩ. The fuse state is read by detecting the resistance in relation to a fixed reference and latching the state into a buffer at power-up.

The efuse can be used to personalize individual chips with digital data that can be used for ECID (Electrical Chip Identification), memory redundancy, or chip configuration. While taking up a relatively small amount of silicon area, the fuses can be integrated into any VLSI component without restricting wiring area. The fuses may be programmed electrically at wafer or module level. This provides significant component flexibility.

The fuse may be designated as blown or connected for schematic simulation. The state of the fuse is not extracted from layout so simulation from layout will consider the fuse to be connected.



Wirebond Pad (bondpad, Pad)

Wire bond pads are available through the *bondpad* pcell with type set to "WB." Supported pitch is 73 µm for LD pads. If IBM will not be performing testing or packaging, other pitches can be supported on a waiver basis. Contact fdrytech@us.ibm.com for additional information.

Pads may be placed over NS or M1 ground planes. For accurate bond pad modeling, the layout of the region under the pad must be strictly controlled. The *bondpad* pcell contains a shape on the "PAD" "DEV" design level to trigger the extraction of the bond pad as a *bondpad* device for simulation and invoke model-related DRC rules. *This shape prohibits placement of any devices or wires under the pad in order to ensure model accuracy*.

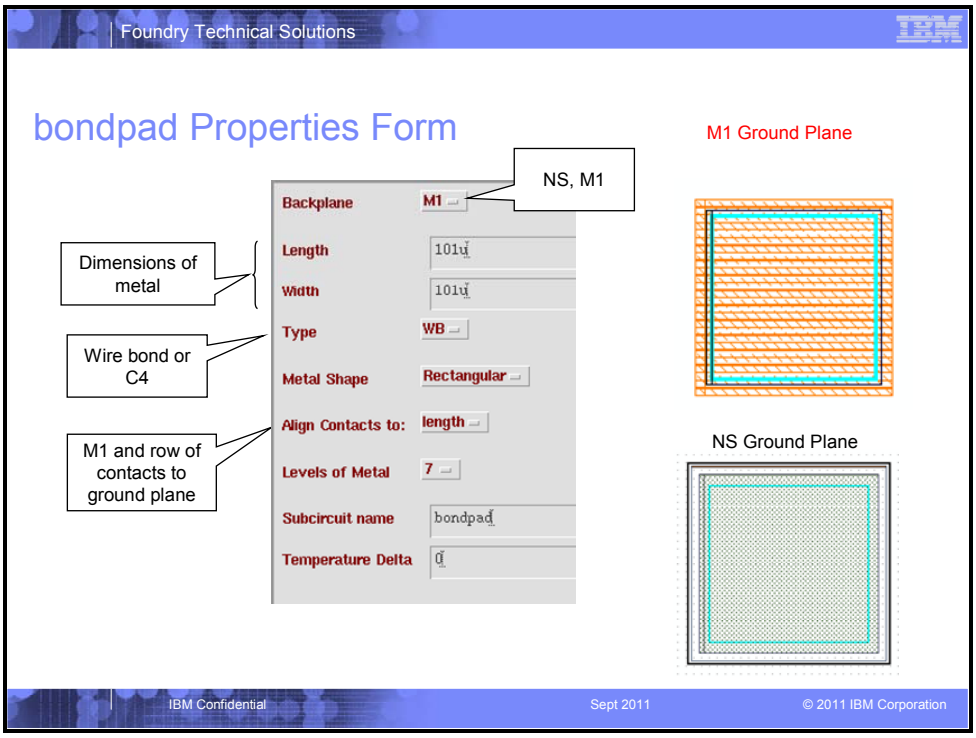
When devices or wires are to be placed under the terminal pads, use the *Pad* pcell instead of *bondpad*. The former is a layout-only cell which does not extract as a device and therefore does not appear in the schematic. There are restrictions as to what may be placed under a terminal pad, and these are most restrictive for wire bond pads. This is explained further in an upcoming slide. Terminal capacitance can be extracted from the layout during parasitic extraction.

C4 (solder bump) terminals are created using the *bondpad* or *Pad* pcells as well with the "Type" selection set to "C4." C4 options are specified as *ball diameter* on *ball pitch*. For example, a "4 on 8" C4 is a four mil (1 mil = 25.4µm) ball on an eight mil pitch. The C4 passivation opening is made up of two coincident octagonal shapes on levels "LV" "DG" and "C4" "DG." These octagonal shapes must be a fixed size as defined by the C4 ground rules and do not scale with the pcell bond pad dimensions.C4 pads are not limited to the perimeter of the chip; arrays of C4 pads may be placed throughout the chip area.

To prevent charging damage during processing, wire bond and C4 pads must have a DC path to a diffusion in substrate (GR 953 for wirebond, GR LD908 for C4).

The *bondpad* model and circuit symbol contains three terminals: the pad (*in*), the ground plane (*gp*), and the substrate (*sub*). The substrate terminal is the substrate region under the bond pad.

None of the ground plane options supported in BiCMOS8HP couple significant energy into the substrate terminal, but the terminal was retained to allow for commonality and re-use of design kit elements among different IBM technologies. In the BiCMOS8HP *bondpad* model, the substrate terminal is decoupled from the pad and ground plane terminals using a very large resistor. The terminal still needs to be connected for LVS purposes.

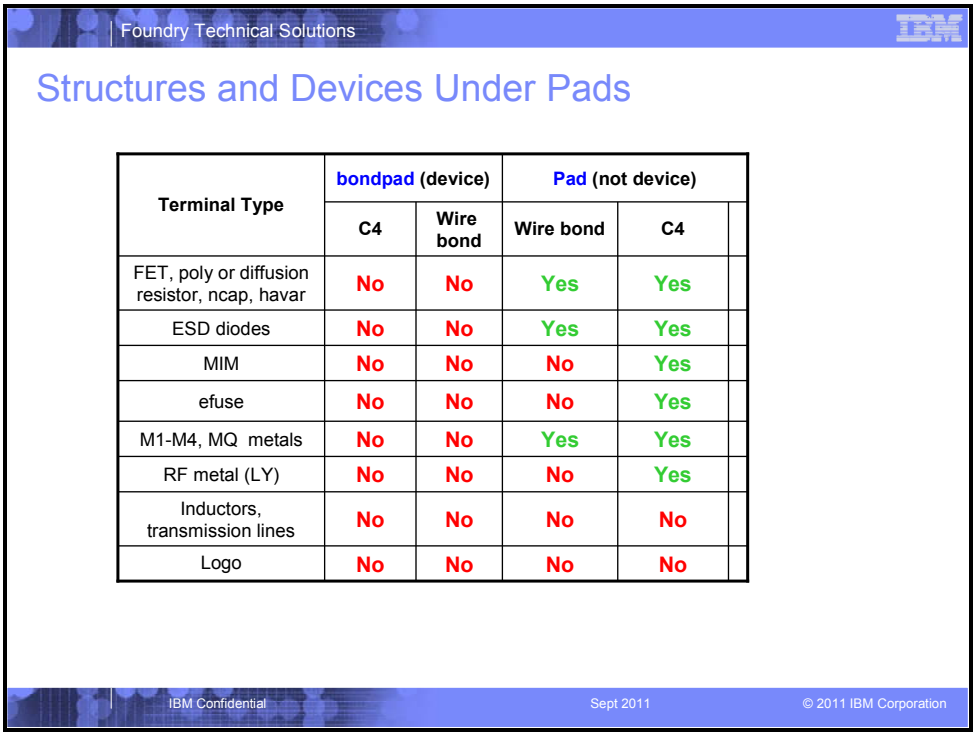


bondpad Properties Form

The *bondpad* properties form is shown in the slide above. The designer specifies the **Ground Plane** (NS or TI), the Legnth, the Width and the (terminal) **Type** (WB or C4). For C4, the pad metal shape may be selected as either rectangular or octagonal. For WB pads, **Add NS contact to Pcell?** option is also included.

A strip of M1 metal is provided for the ground plane connection for both ground plane options. An **Align Contact to** switch is provided to control whether this contact strip is along the length or width dimension of the *bondpad*.

The substrate connection for the *bondpad* does not appear in the pcell layout. The substrate terminal of the *bondpad* will be extracted to the local substrate domain, either sub! or a named domain created by the designer.



Terminal Type	bondpad (device)		Pad (not device)	
	C4	Wire bond	Wire bond	C4
FET, poly or diffusion resistor, ncap, havar	No	No	Yes	Yes
ESD diodes	No	No	Yes	Yes
MIM	No	No	No	Yes
efuse	No	No	No	Yes
M1-M4, MQ metals	No	No	Yes	Yes
RF metal (LY)	No	No	No	Yes
Inductors, transmission lines	No	No	No	No
Logo	No	No	No	No

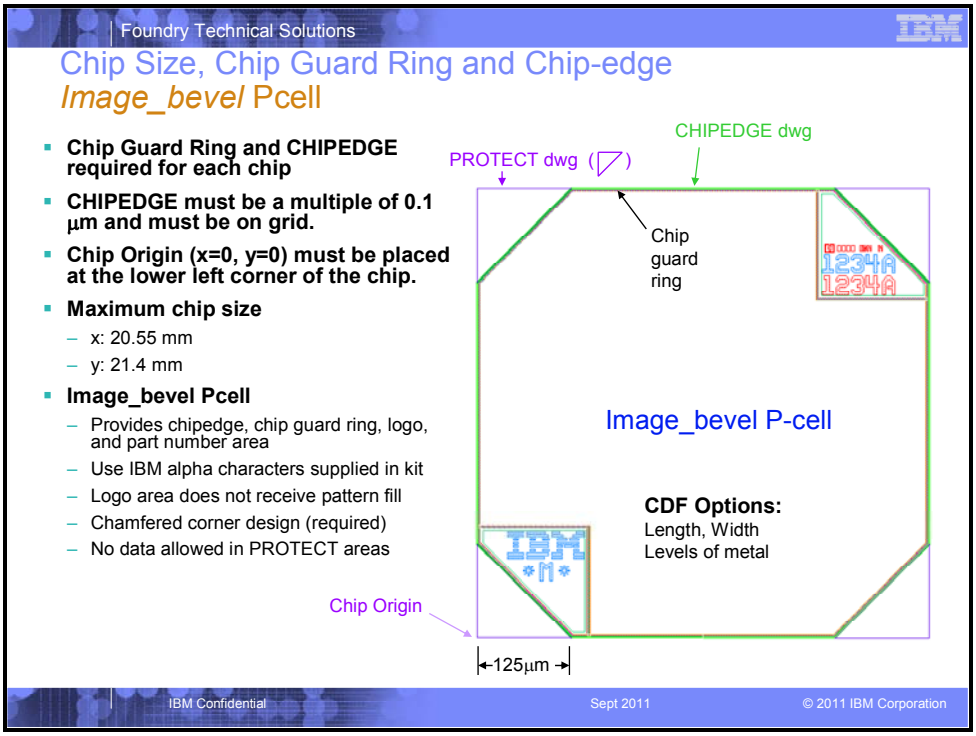
Structures and Devices under Pads

Design rules allow certain devices under wire bond pads. Permissible structures depend on whether the *bondpad* or P*ad* pcell is used, and whether the terminal type is wire bond or C4. The left two columns show that the *bondpad* device does not allow any devices or wiring under the pad. This is to insure that the ground plane is well-defined (controlled) so that the simulation model can provide an accurate prediction of parasitic capacitance.

Restrictions applying to the *Pad* pcell are shown in the last two columns of the table. The P*ad* pcell is not a device and does not have a simulation model or schematic symbol. Parasitic capacitance is determined by a parasitic extraction tool.

When the *Pad* pcell is used to create a wire bond terminal, FETs, poly or diffused resistors, mos and hyperabrupt varactors and esd diodes can be placed under the pad. Wiring is allowed on M1-M4 and MQ levels, though some layout restrictions may apply.

The C4 terminal defined by the *Pad* pcell may be placed over most devices and wiring. The exceptions are inductors and transmission lines, and the logo area. C4 terminals should not be placed over inductors and transmission lines because they degrade RF performance. Inductors should be at least 110 µm away from C4 pads. This prohibition is good design practice but is not coded in DRC. C4 pads are prohibited over the logo area to prevent obscuring part numbers and other markings.



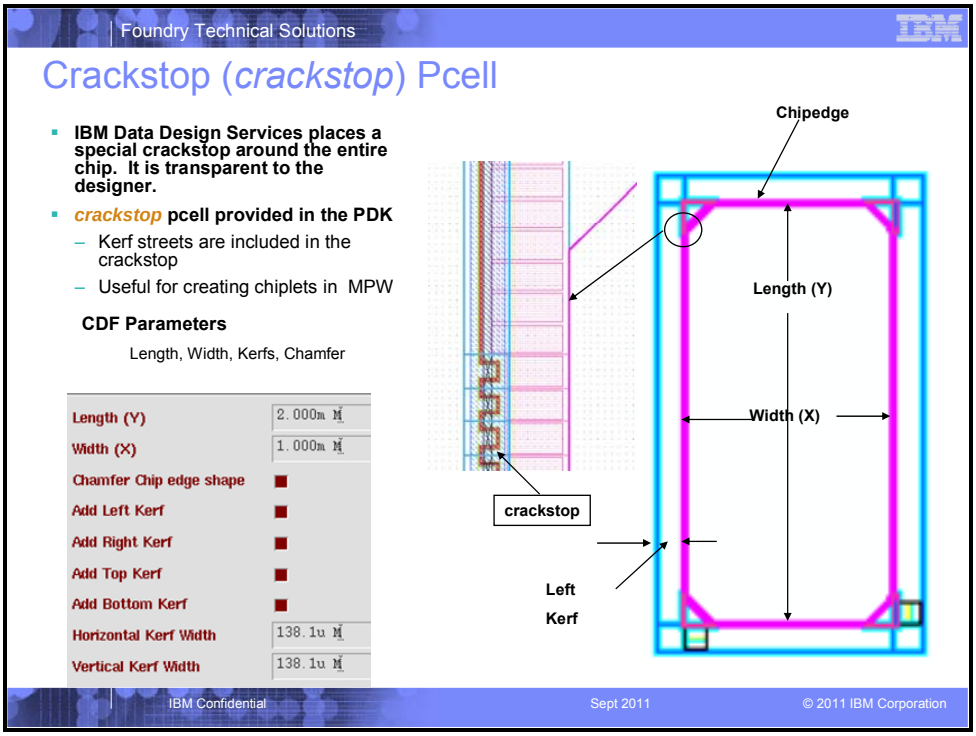
Chip Size, Chip Guard Ring and Chip-Edge (Image_bevel)

Designers need to include chip guard ring for preventing ionic contamination and place chip edge around the chips. The die size specified to IBM on the Foundry Questionnaire is determined by the dimensions of the CHIPEDGE shape.

The chip origin (x=0, y=0) must be placed at the lower left corner of the chip. CHIPEDGE must be bounded at X=0 on the left side of the chip (not in the chamfer area), and bounded at Y=0 at the bottom of the chip. The X and Y dimensions of CHIPEDGE must be a multiple of 0.1 µm and must be on grid. The maximum chip size allowed is 20.55 mm in the x-direction and 21.4 mm in the y-direction.

The *Image_bevel* pcell in the BiCMOS8HP PDK provides the CHIPEDGE, the ionic contamination guard ring and the logo and part number areas. The *Image_bevel* pcell should be placed using the chip dimensions then flattened in order to customize the logo and part number area. IBM requirements for part numbers are given in the Design Manual and DRC-clean alpha-numeric layouts of various sizes are supplied in the *alpha12, alpha20, alpha25 and alpha40* cells in the BiCMOS8HP library.

Beveled (chamfered) corners are required on all chips. Four triangular shapes on level "PROTECT" "dwg" are placed with the pcell to allow DRC checking to ensure that no customer shapes are placed in the chamfer area.

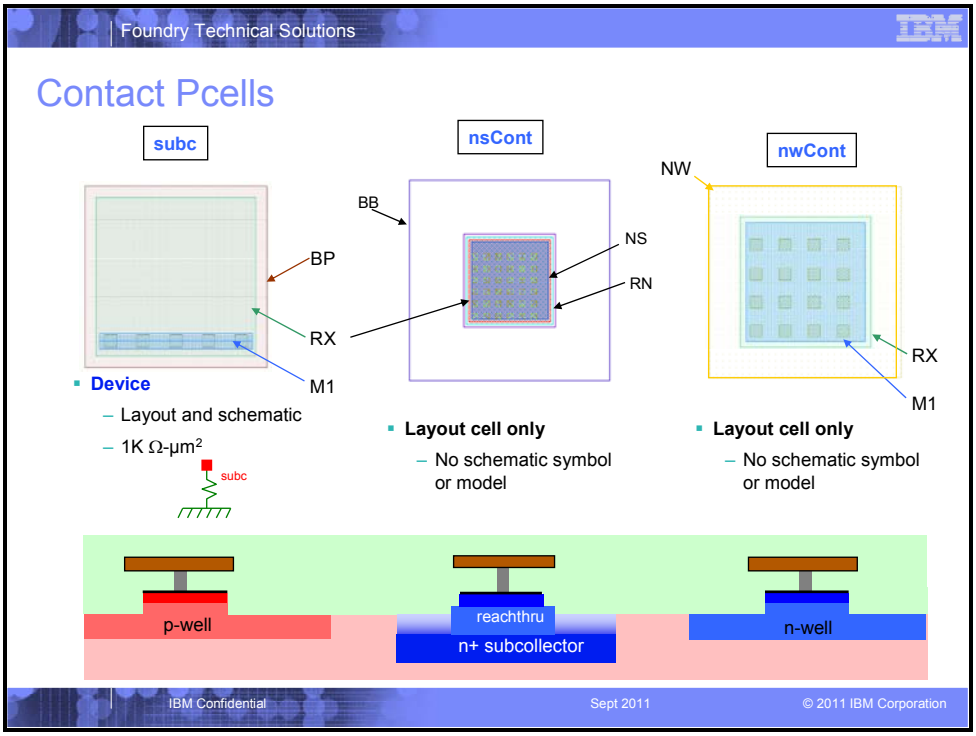


Crackstop

A *crackstop* pcell is also included in this design kit. Crackstop is a special design that is placed around the entire chip. This is done by Design Services and is transparent for designers. For designers, it is useful for placing chiplets (multiple chips) in the same design.

The crackstop pcell is very flexible. Users can select the chip length, width and the kerf sizes. The kerf can be optionally added to any side by selecting the “Add Kerf”.

This pcell is very useful when creating your own MPW with chiplets. There is an Application Note posted on ICC that describes the how to create a MPW.

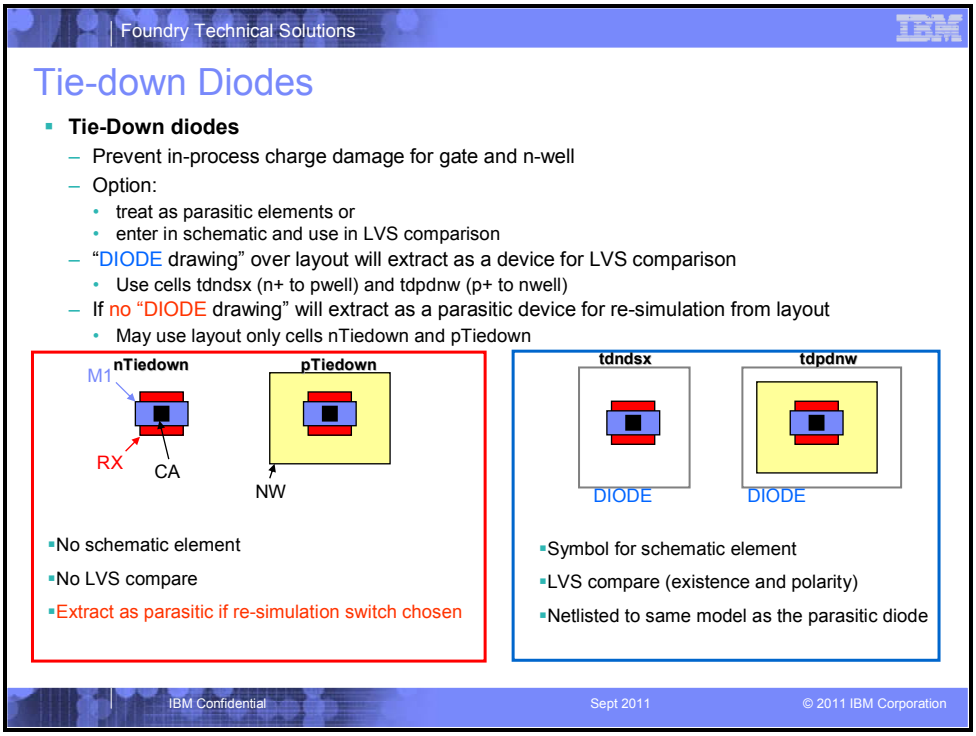


Contact pcells

The design kit contains several support pcells that facilitate making contact to the substrate, subcollector and n-well.

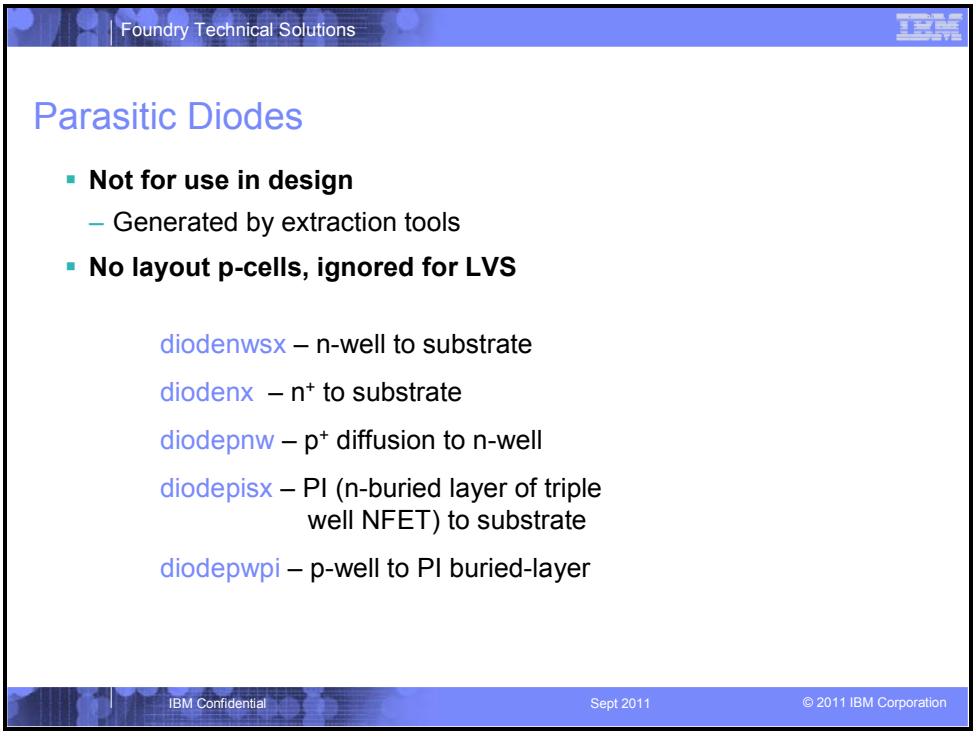
The substrate contact *subc* is a device, having both a schematic and layout representation. LVS will check to insure that at least one substrate contact is present in the layout to correspond to a substrate contact on a given net in the schematic. It will allow the contacts to be different sizes, and it will allow additional substrate contacts in the layout as long as they are attached to the same net. The terminal of the symbol represents the M1 contact. The lower part of the symbol, the "chassis ground" symbol, represents the region of substrate beneath the device. The vertical resistance from the metal to the substrate region is 1K Ω-μm^2, so substrate contacts need to be fairly large to be effective.

The *nsCont* and *nwCont* pcells are also provided for layout convenience. They have no symbol view and do not appear in circuit schematics.



Tie-down and Parasitic Diodes

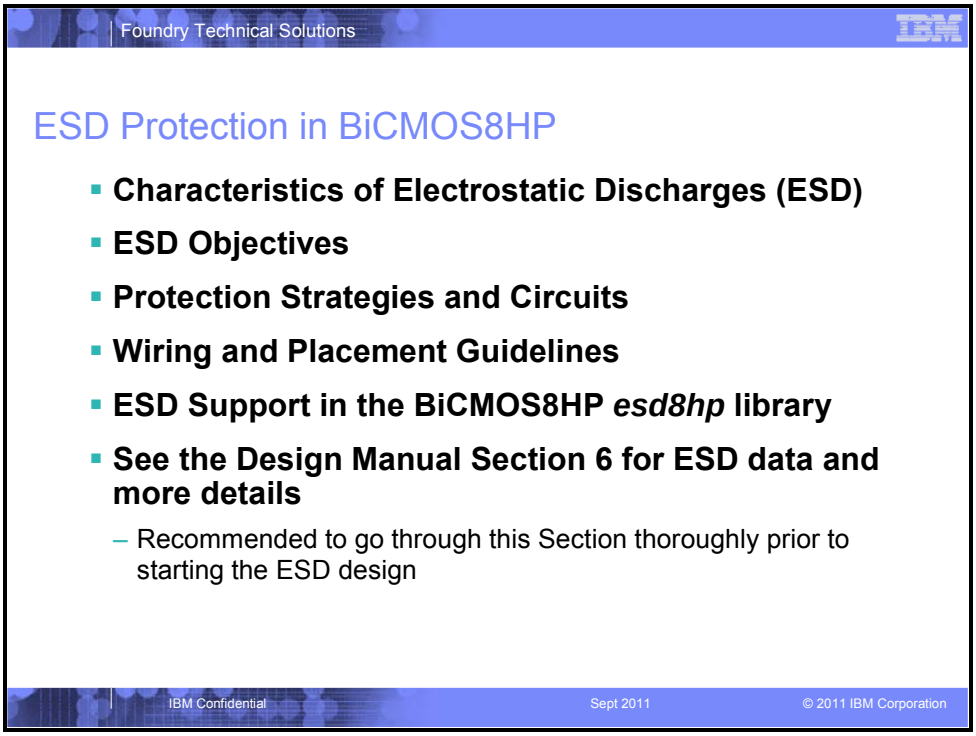
The BiCMOS8HP library contains layout-only cells, as well as cells with LVS support, for tie-down diodes as described in the slide above. Additionally, device models are provided for each of the parasitic diode junctions in the technology with an associated device name and model as shown below. The cells *tdndsx* and *tdpdnw* are for schematic simulation and netlist to the diodendsx and diodepdnw models respectively. The other diodes appear in netlists for parasitic resimulation only; they are not used in circuit schematics.



ESD Protection and esd8hp Library

Device miniaturization has made electronic devices more vulnerable to damage from electrostatic discharge (ESD). All operations where the chip (or module) is handled or probed (wafer test, dice and pick operations, shipping, packaging, module testing, card assembly, and customer handling) can cause ESD damage. Low tolerance to ESD events will cause problems in qualification, manufacturing, test and assembly operations, and can lead to field failures.

This module addresses electrostatic discharge (ESD) protection for the IBM BiCMOS8HP technology. It covers the basics of electrostatic discharge, ESD Protection Targets and Requirements, ESD tolerance of unprotected devices, protection strategies and circuits, and ESD design support provided in the BiCMOS8HP design kit.

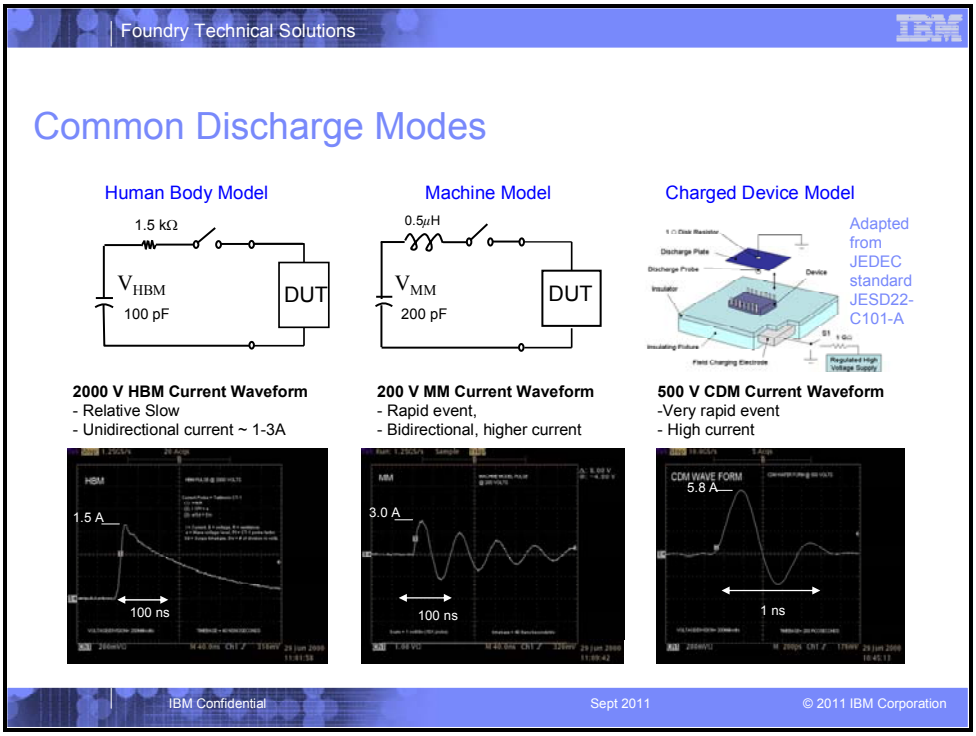


ESD Protection in BiCMOS8HP

ESD is an important consideration in chip design and needs to be addressed from the start of the design process. Viewing ESD as a last minute addition often leads to unsatisfactory ESD protection or degraded chip specifications.

ESD targets and requirements may have to be compromised to meet performance requirements on sensitive pins. However, the design benefits by implementing the most effective ESD protection possible on all pins. *All pins, even high speed or sensitive analog pins, must have a protection strategy.*

Section 6 in the BiCMOS8HP Design Manual has details about ESD design, layout, devices in *esd8hp* library, and measured data. Designers are strongly advised to read this section thoroughly before starting the ESD design. Further help is available in the form of ESD Design Review that IBM can provide at designer's request. If this is desired, please contact fdrytech@us.ibm.com .



Common Discharge Modes

ESD is a high current event that can affect chips at various stages of processing and/or handling. There are three primary ESD models considered in the microelectronics industry: Human Body Model (HBM), Machine Model (MM) and Charged Device Model (CDM).

The human body model represents a human body discharging through the IC module to ground. The equivalent circuit for HBM is a 1.5kΩ resistor in series with a 100pF capacitor as shown. The capacitor is charged to the specified ESD voltage, and then the switch is closed and the current flows through the Device Under Test (DUT). An HBM ESD event occurs between any two pins on a module. HBM has the longest duration of the three primary models, but it has the lowest current for a given ESD voltage. Specialized ESD testers equipped with the appropriate resistor and capacitor network are used to apply an HBM stress to a module to determine its robustness. HBM can be done at wafer level on individual structures during technology development, and at module level for product chip qualification.

Similar to HBM, the MM ESD event occurs across any two pins on a module. MM however, simulates a tool discharging across the two pins. This event is more rapid than HBM and has a higher current level. The waveform is also quite a bit different – the MM wave form is a bi-directional damped oscillation. The test procedure for MM is similar to HBM, but the MM is represented by a capacitor in series with an inductor.

Unlike HBM and MM, CDM ESD events only involve a single pin on the module. Modules can develop charge through triboelectric (frictional) effects. When this occurs, unless a high resistive path is used to discharge the module, it may be exposed to a CDM ESD event. The CDM event charges a chip and then discharges to ground out of a single pin. CDM is a very high current event, but occurs in a very short time interval. CDM testing is generally accomplished only on packaged chips. A field plate is used to induce a specified charge on the module, and then a probe with a low resistance path to ground is brought into contact with a single pin to discharge the module. This procedure is repeated for each pin on the module, and a

functional test is employed after CDM stressing is completed to determine if the module has been damaged. The slide shows a conceptual diagram of a CDM tester from the JEDEC standard JESD22-C101-A together with the current waveform. The procedure for applying a CDM pulse is as follows:

1. The device is placed on the tester with the pins pointing up.

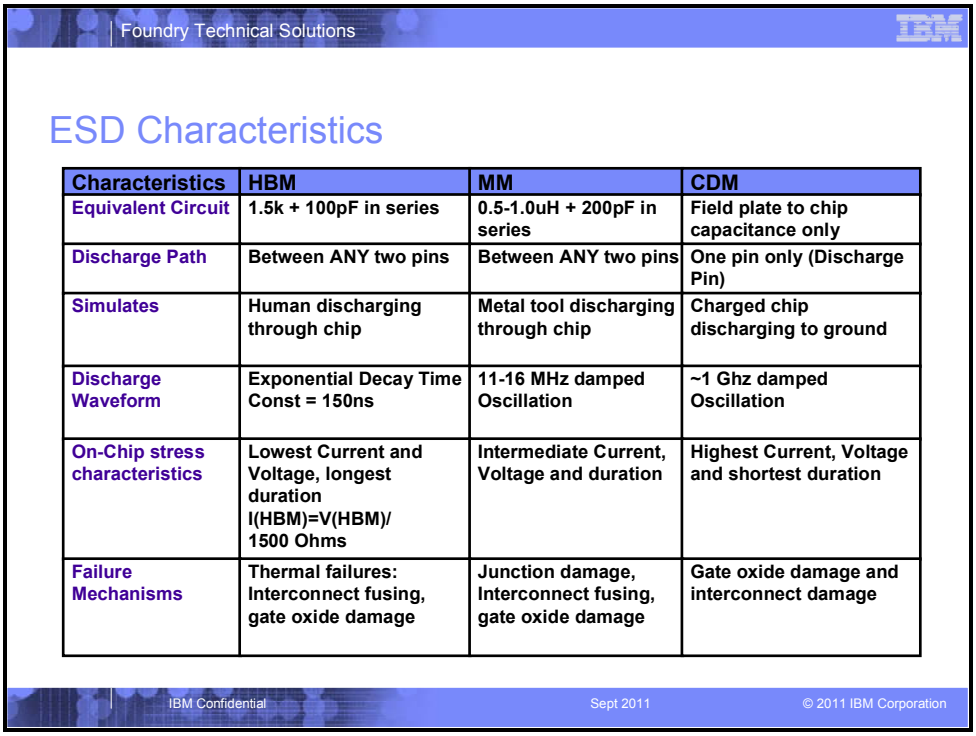
2. The discharge probe is brought in contact with the first pin to be tested, and the field charging electrode is brought to the negative test voltage.

3. This causes the module to draw current through the probe such that the test voltage is developed across the insulating fixture between the device under test and the field charging electrode.

4. The probe is then disconnected. The field plate is returned to ground, leaving the module positively charged.

5. The discharge occurs when the grounded discharge probe is again brought in contact with the pin under test, and the charged module is returned to ground potential through the pin.

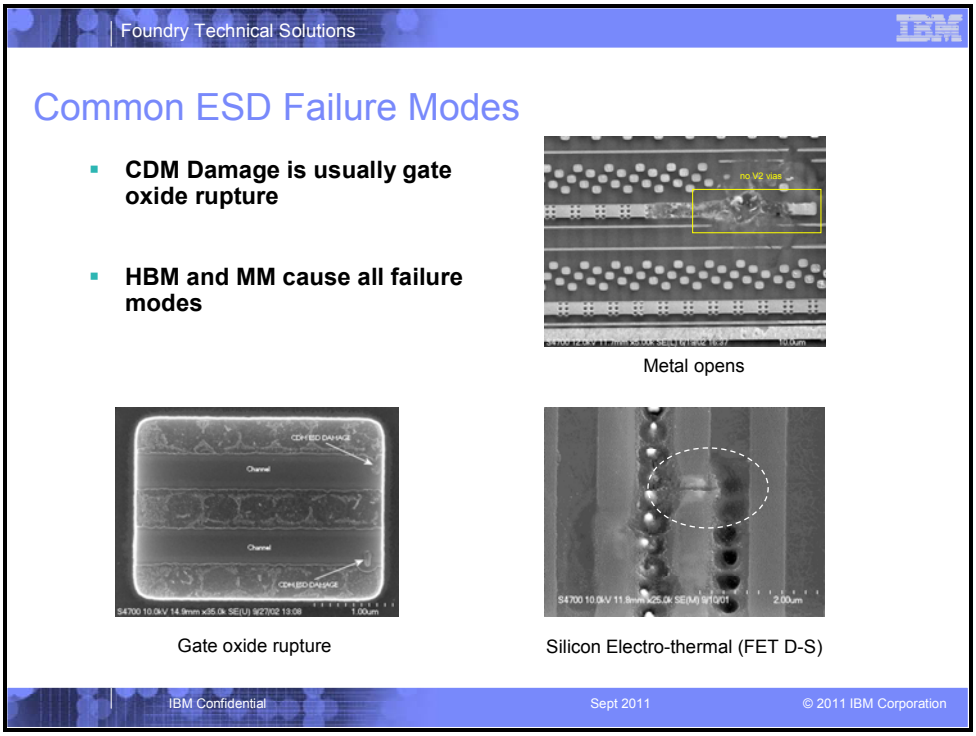
In contrast to HBM, there is no extrinsic resistance in this discharge path, so the current is a bidirectional, rapidly decaying oscillation. Other key differences from HBM are that the results are strongly package dependent, and the discharge current is more distributed throughout the chip. CDM is quoted in volts, and reflects the voltage to which the device is charged. The rise times are typically a few hundred picoseconds, and ESD duration is 1 to 2 ns. Peak current is 1 to 2 A per 100 V, depending on the die size and package type, in contrast to 67 mA per 100V for HBM.



Characteristics	HBM	MM	CDM
Equivalent Circuit	1.5k + 100pF in series	0.5-1.0uH + 200pF in series	Field plate to chip capacitance only
Discharge Path	Between ANY two pins	Between ANY two pins	One pin only (Discharge Pin)
Simulates	Human discharging through chip	Metal tool discharging through chip	Charged chip discharging to ground
Discharge Waveform	Exponential Decay Time Const = 150ns	11-16 MHz damped Oscillation	~1 Ghz damped Oscillation
On-Chip stress characteristics	Lowest Current and Voltage, longest duration I(HBM)=V(HBM)/ 1500 Ohms	Intermediate Current, Voltage and duration	Highest Current, Voltage and shortest duration
Failure Mechanisms	Thermal failures: Interconnect fusing, gate oxide damage	Junction damage, Interconnect fusing, gate oxide damage	Gate oxide damage and interconnect damage

ESD characteristics

Most chips have specified requirements and/or targets for protection levels to these various models. The basic characteristics of each event are summarized in the table above.



Common ESD Failure Modes

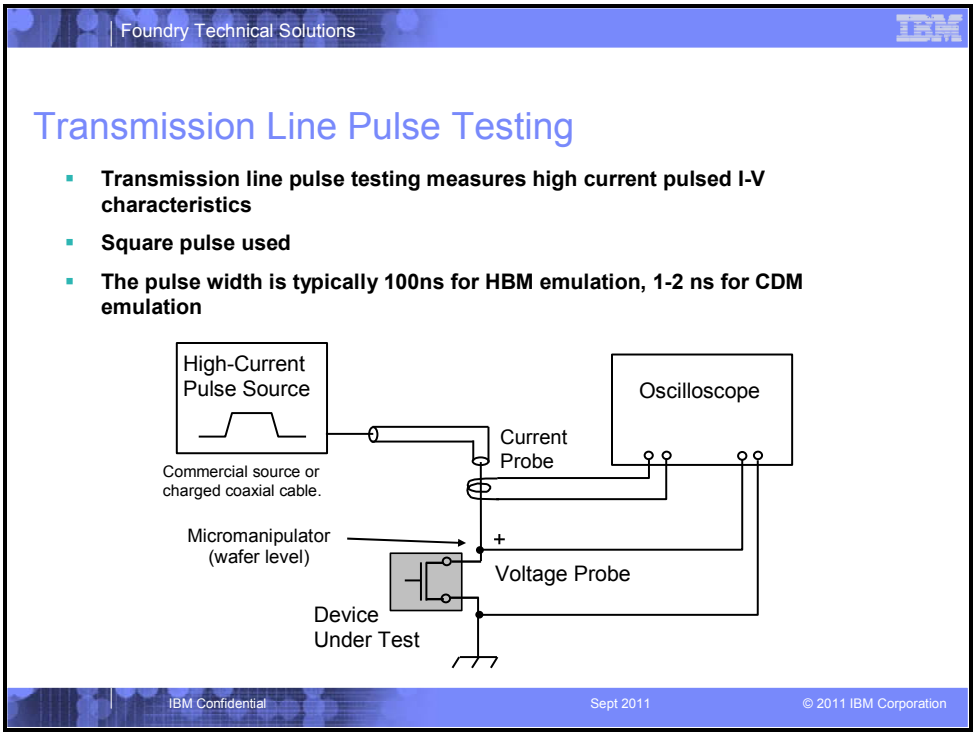
ESD failures are categorized into gate oxide rupture, metal opens, or silicon electrothermal failure. The failure modes are illustrated by the scanning electron microscope (SEM) micrographs above.

The lower left picture shows a field-effect transistor (FET) that has suffered gate oxide rupture. The FET, which has two gate stripes, is shown with the polysilicon gate removed. Two locations of oxide damage can be seen in the right side of the device near the edge of each channel.

The picture in the upper right shows a metal wire that was melted by high currents during a discharge event.

The lower right shows an FET that has been destroyed by silicon electrothermal failure during snapback. This sample has been processed to remove the polysilicon gate. The channel region can be seen as the center stripe. The holes on either side of the channel are an artifact of the sample preparation. The ESD damage occurred when drain-to-source voltage exceeded the snapback voltage and the discharge current passed through the FET channel.

CDM typically (though not always) causes gate oxide rupture. HBM and MM can cause all three failure modes.



Transmission Line Pulse Testing

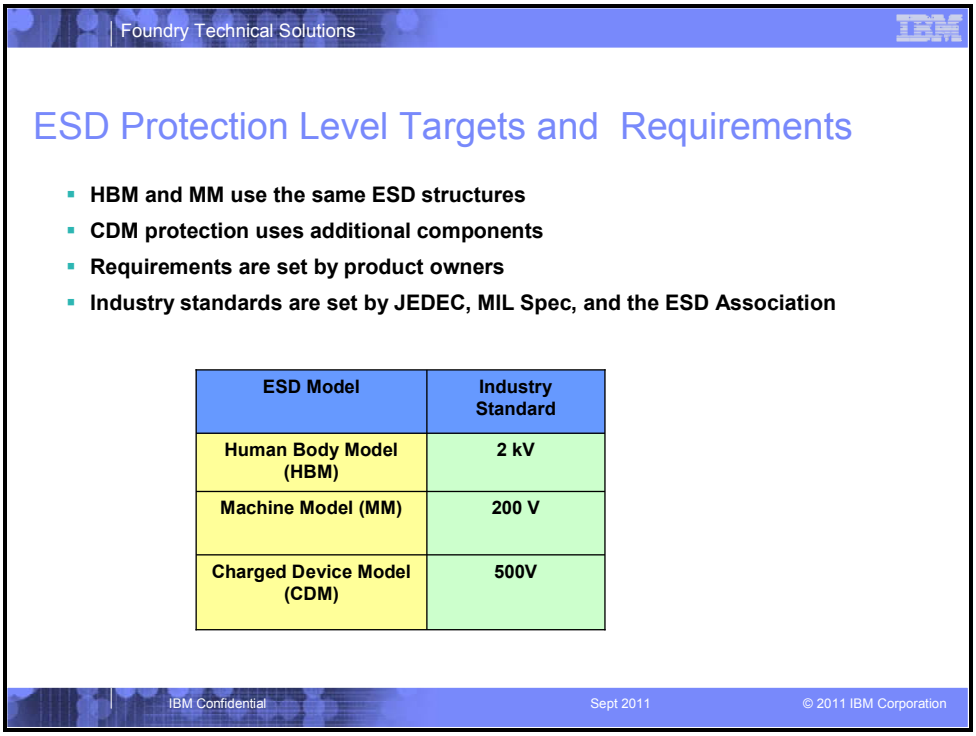
Transmission Line Pulse (TLP) measurements are not ESD specifications, but rather a diagnostic tool used to understand the behavior of devices under the very high current conditions encountered in an ESD event. Pulsed measurements replicate the temporal behavior of the ESD event and avoid energy levels that would destroy the device in a DC measurement.

Since an ESD discharge behaves like a current pulse it is reasonable to replace the charged capacitor by either a pulsed current source or a charged coaxial cable, either of which will create a rectangular current pulse. An oscilloscope is used to measure the current and voltage across the device during the discharge. The pulse width can be varied to study different types of discharge events or to gain additional understanding about the temporal dependence of device behavior at very high current levels.

TLP data for many of the IBM ESD components is provided in the Design Manual.

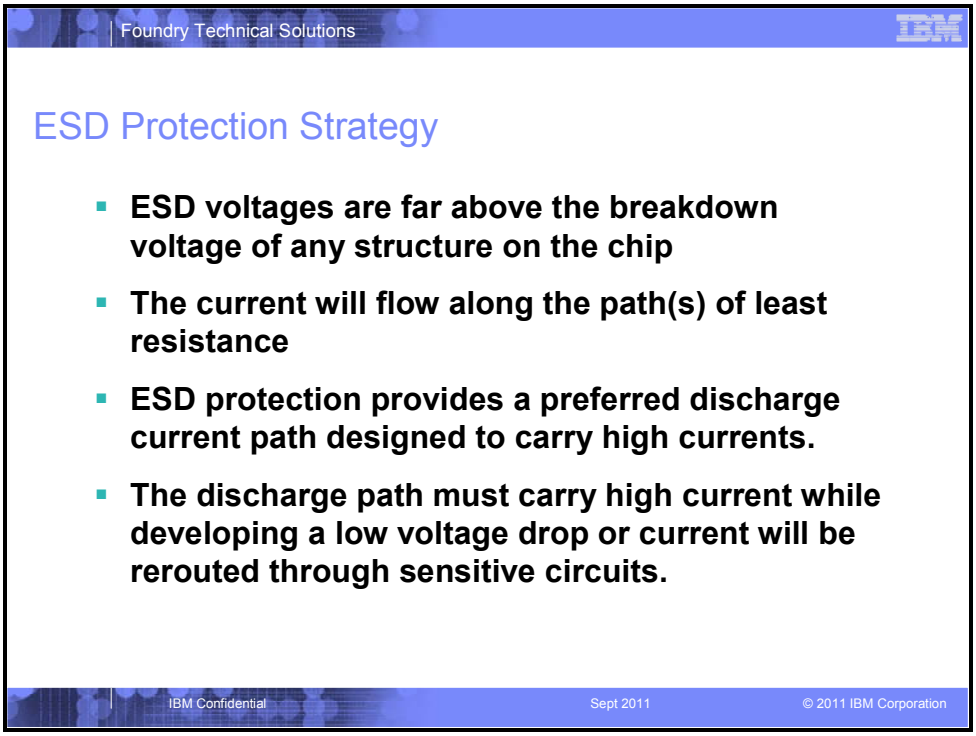
One hundred nanosecond TLP results are loosely correlated to HBM tolerance by the relation:

HBM (V) ≃ TLP (A) * 1500



ESD Protection Level Targets and Requirements

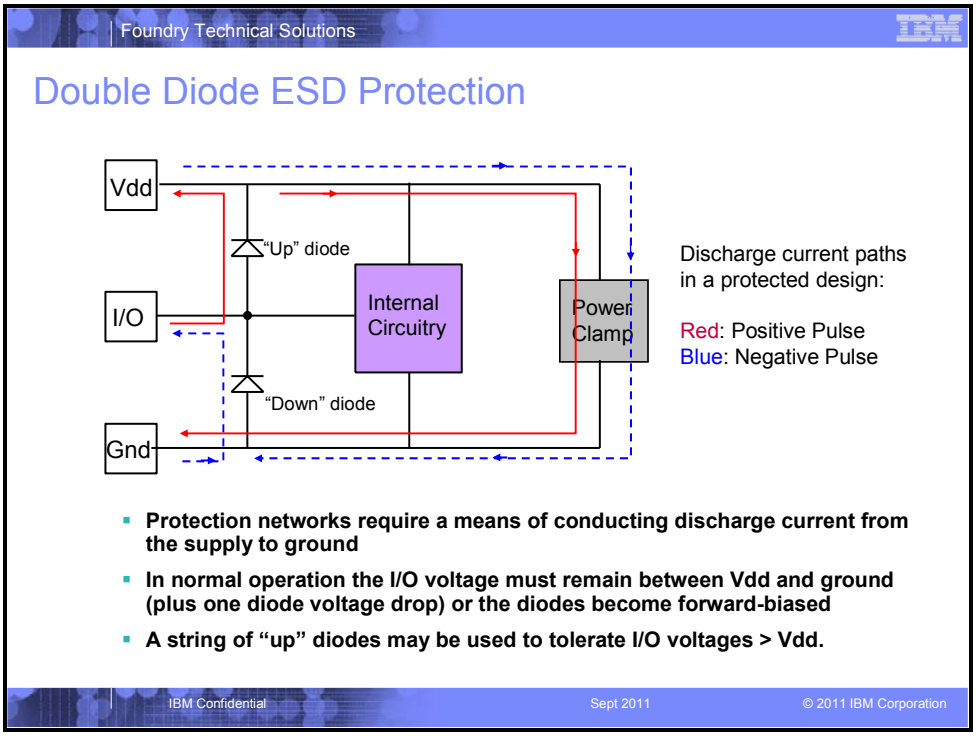
ESD protection levels are generally set by product owners based on how well the environments where the chips will be handled are controlled and by the requirements of the customers of the chips. The standard protection levels seen in the industry are recorded in the table above. Some products require more or some require less protection depending on their specific circumstances. It is important to understand the required protection levels for a given chip. The ESD ground rules found in the IBM Design Manuals are based on achieving the industry standard ESD protection levels as outlined in the slide above.



ESD Protection Strategy

Consider that the highest junction breakdown voltage on the wafer is of the order of 10 to 15 V. Compare this to the hundreds or thousands of volts applied during an ESD event, and it is clear that discharge current will flow through the chip. The objective of ESD protection is not to prevent the discharge current from flowing, but rather to redirect it through structures that have been sized to withstand large currents without failure. The designer must analyze the possible discharge modes; where the current will enter and leave the circuit with both possible polarities of the discharge. Then the designer creates a protection network in which these currents will preferentially flow without developing large voltage (IR) drops that can cause damaging currents to flow in the internal circuits. The solution is analogous to placing a lightning rod on a building.

The protection circuit must be designed so that the discharge path is not active for normal signal levels, but preferential for discharge events. The discharge current paths are activated by voltages or currents outside of the expected levels or polarities operational signals.



Double Diode ESD Protection

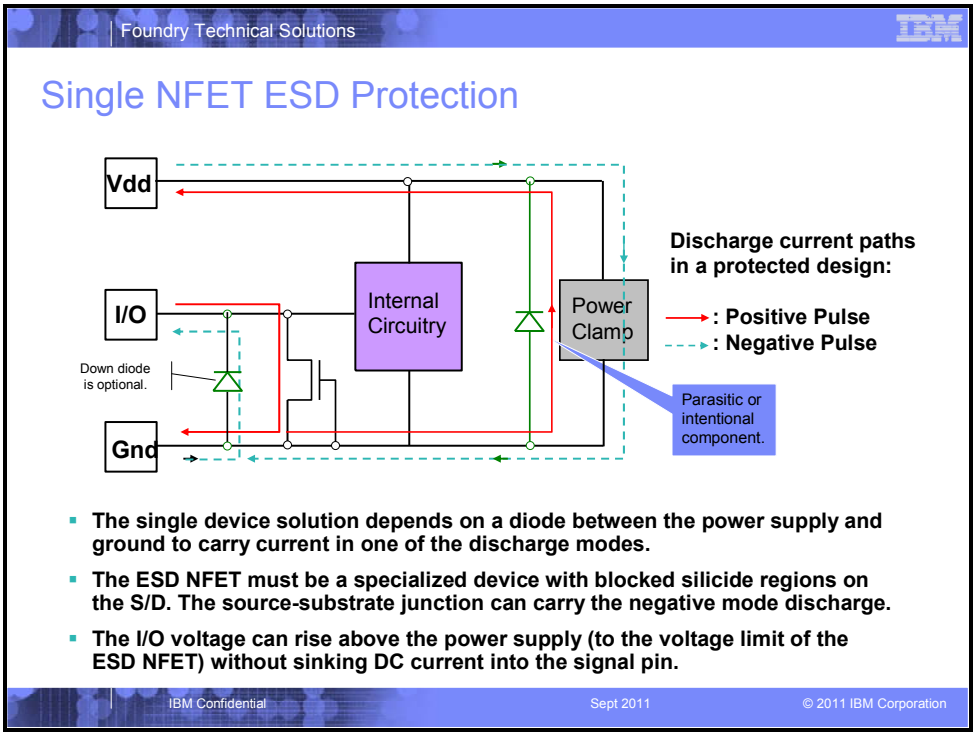
One of the most commonly used ESD protection strategies is to use two diodes on the pin, one to the supply bus and the other to the ground bus. This diagram shows the current paths in the chip for the four possible discharges between the pin and its supply and ground busses. The power clamps will be discussed later in more detail, but essentially they are turned off during normal operation and turn on during an ESD event to provide a very low resistance discharge path.

For a positive pulse with respect to Vdd, the current passes through the upper diode to the supply pin. For a negative pulse with respect to Vdd, the current enters the supply pin, goes through the power clamp, and then passes through the diode connected from the pin to ground (some ESD protection networks utilize parasitic lateral transistor action to conduct the current directly from Vdd to the pin).

For a positive pulse with respect to ground, the current passes through the upper diode, along the supply rail to the power clamp, through the clamp, and out the ground pin. For a negative pulse with respect to ground, the current passes through the lower diode and out the signal pin.

If the I/O signal can rise above the power supply, as in a mixed-voltage interface circuit, the upper diode should be replaced by a diode string. Both dc leakage current at the input and the effect of stored charge in the diodes during the transient response of the pin must be considered when determining the number of diodes to place in series. A diode under forward bias stores the minority carrier charge adjacent to the depletion regions.

Because the diodes appear as parasitic capacitance on the input/output node, the designer may have to balance ESD protection against circuit performance.



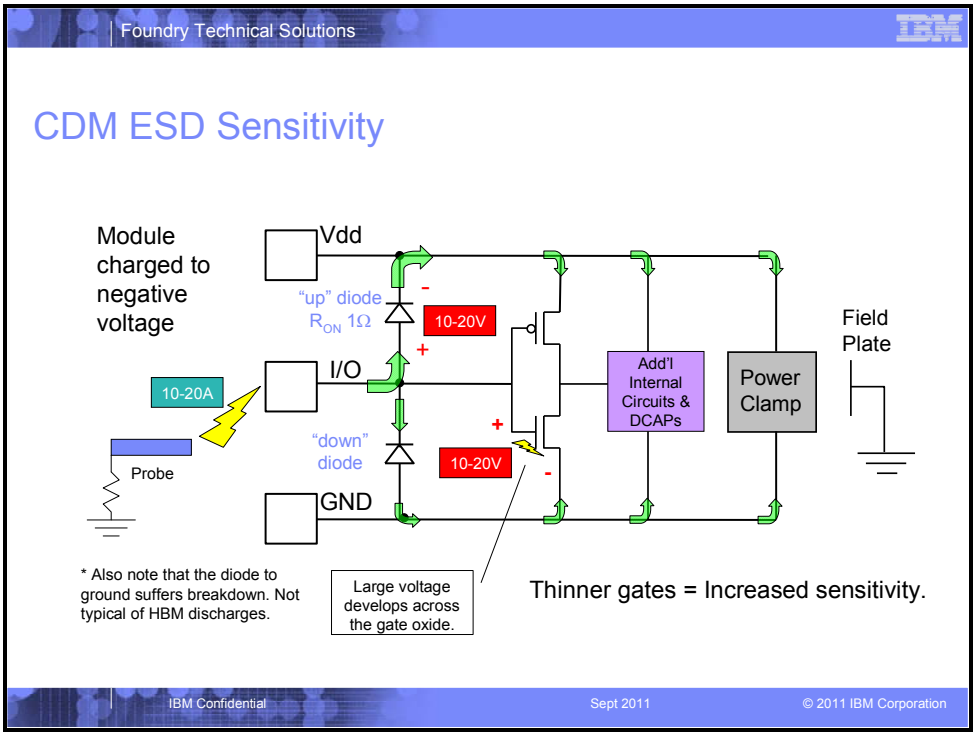
Single NFET ESD Protection

In another typical ESD protection circuit topology, a non-silicided grounded gate NFET device is used instead of a pair of diodes to carry the discharge current. The grounded gate NFET is a specialized device in which the silicide is not formed on parts of the source and drain diffusions enabling the device to have much better current carrying capability than a standard silicided NFET.

For a positive pulse with respect to Vdd, the current passes through the ESD NFET to the ground bus, then to the power supply either through the power clamp, an explicit ESD diode in parallel with the power clamp, or a parasitic diode such as N-well to substrate junctions. For a negative pulse with respect to Vdd, the current enters the supply pin, goes through the power clamp, and then passes through either an explicit ESD diode in parallel with the ESD NFET, or through the parasitic drain-to-substrate junction of the ESD NFET, and out the signal pin.

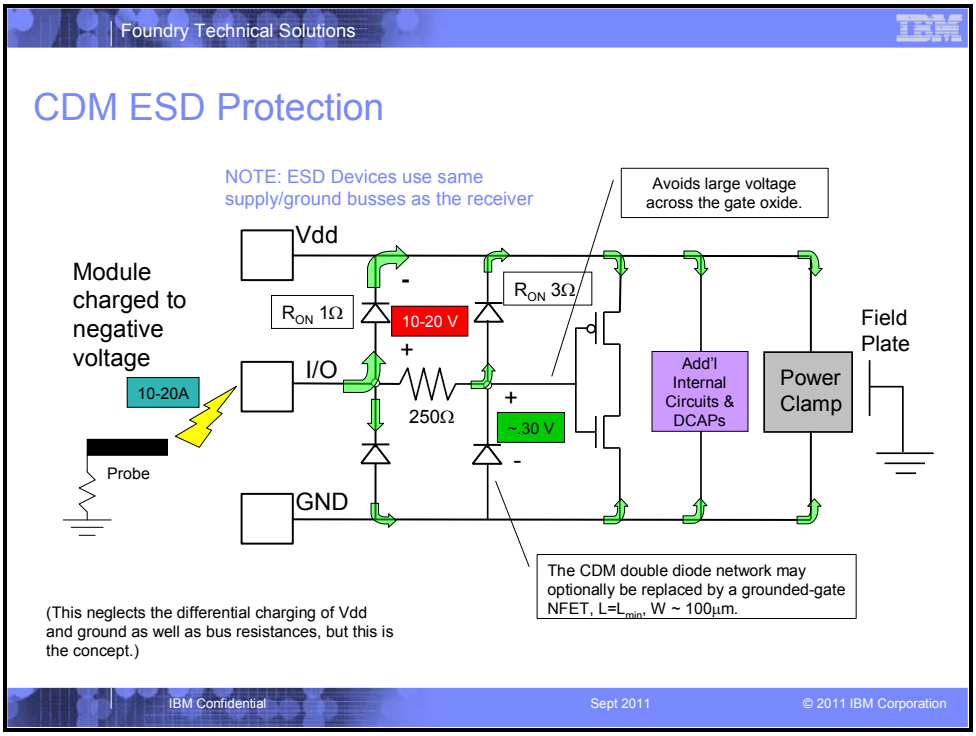
For a positive pulse with respect to ground, the current passes through the ESD NFET and out the ground pin. For a negative pulse with respect to ground, the current passes through either an explicit ESD diode in parallel with the ESD NFET, or through the parasitic drain-to-substrate junction of the ESD NFET, and out the signal pin.

An advantage of this topology is that the I/O pin can rise above the power supply voltage without forward-biasing the up diode of the double diode circuit as shown.



CDM ESD Sensitivity

In a CDM discharge, the entire chip is charged to a voltage then discharged through a single pin. The circuit diagram shown in the slide illustrates the current flow in the chip and explains why the HBM circuit is not sufficient protection. The device under test contains a CMOS receiver connected to the I/O pin, followed by additional circuitry. The HBM protection diodes are present as is the power clamp. Consider the module charged to a negative voltage and then discharged through the I/O pin. If the module is unpowered, all buses and devices start at the same potential. The current flowing into the pin has two paths to charge the chip: through the "up" diode to the supply bus, or in the reverse direction through the down diode to the ground bus. The preferred path is through the up diode. A very robust HBM diode has an on-resistance of about 1 Ω. The CDM current is in the range of 10 to 20 A, which develops a voltage of 10 to 20 V between the I/O pin (also the MOS gate) and the power supply and ground buses. This voltage will be large enough to force some current through the reverse-biased "down" diode. More critically, the voltage will break down the gate oxide and destroy the receiver. HBM protection is clearly not adequate for the high currents present in CDM discharges.

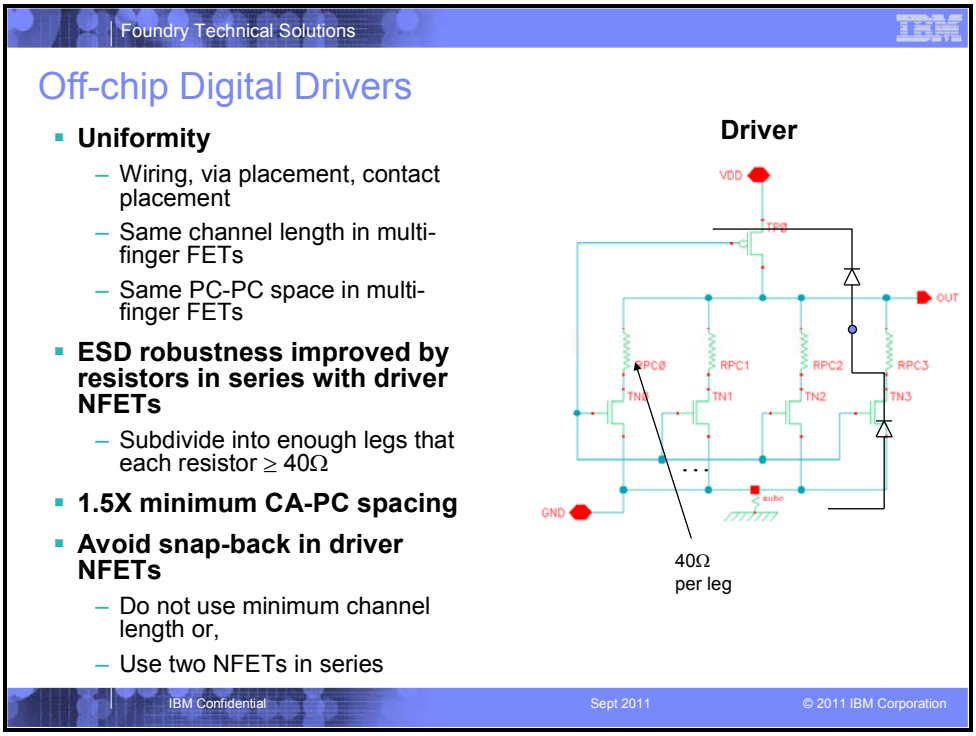


CDM ESD Protection

CDM protection is achieved by adding a voltage divider between the I/O pin and the MOS gates. This is implemented by a series resistor and another set of ESD devices. The resistor should be in the neighborhood of 50 to 250 Ω. In normal operation, the resistor is in series with the input impedance of the receiver and the load capacitance of the additional ESD devices and does not significantly affect the speed of the gate. Consider the same scenario as before where the module is charged to a negative voltage and discharged through the I/O pin. Again, a large voltage develops between the pin and the power supply and ground buses, but the resistor and the forward-biased “up” diode divide this voltage based on the proportion of the resistor value and the diode on-resistance.

The second set of double diodes may be much smaller than the HBM diodes since they do not carry nearly as much current. The double diodes may be replaced by a grounded-gate NFET that uses minimum design channel length and a channel width of at least 100 μm.

This treatment neglects some of the effects (such as, the resistance of the power and ground buses and the fact that the power supply bus will lead the ground bus in returning to ground potential) but it captures the essentials of the situation.

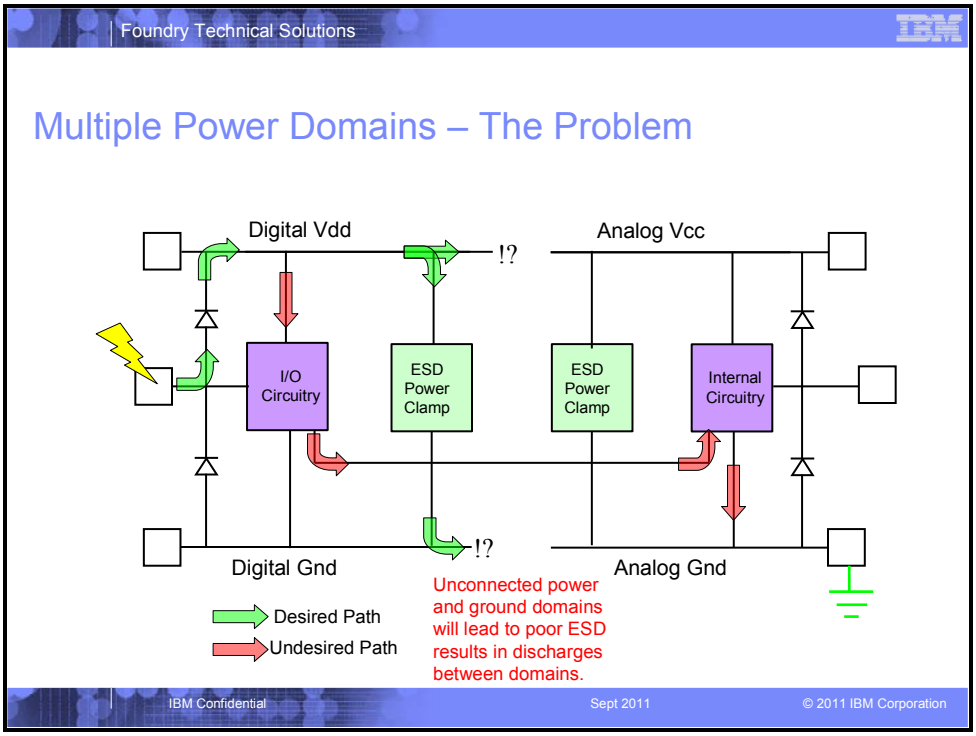


Digital Drivers

Optimal results will be achieved when using layout practices that result in maximum uniformity of current and thermal distributions. Use broadside wiring if possible and place vias and contacts uniformly across the driver device(s) so as to encourage uniform current distribution. Multi-finger FETs should use the same channel length and gate-to-gate spacing for all fingers.

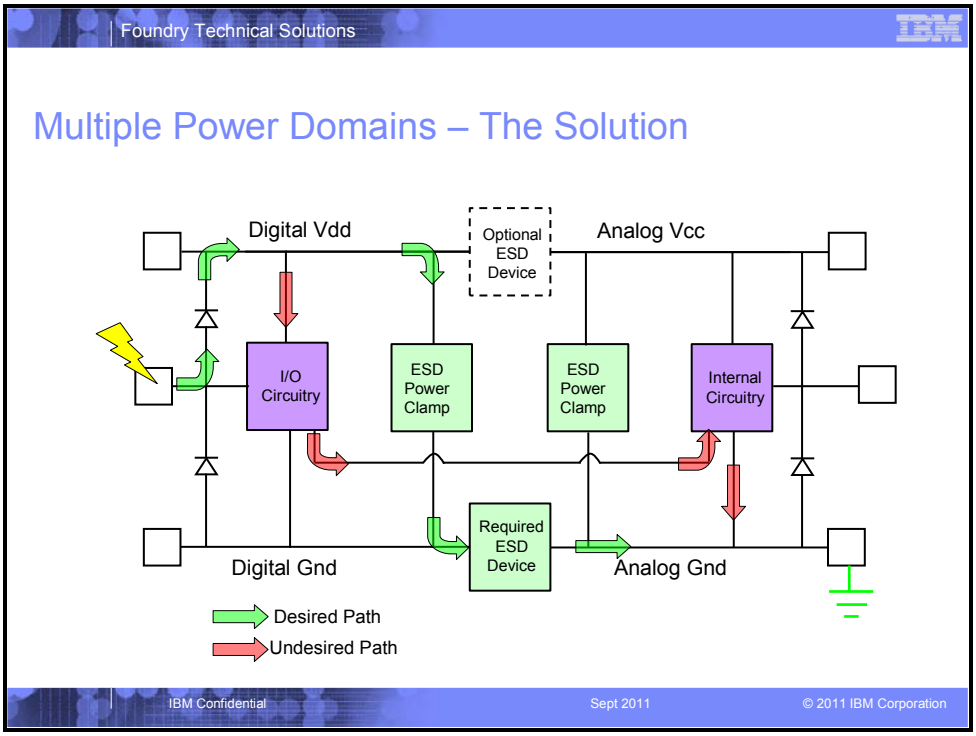
ESD robustness of digital off-chip drivers will be improved by the addition of resistors in series with the driver NFETs. The resistor will limit the NFET current in the event that the pin voltage rises high enough to put the device into snap-back. A driver device should be partitioned such that the resistance on each leg is greater than or equal to 40Ω.

The possibility of destructive NFET breakdown through snap-back can be markedly reduced by avoiding minimum design channel length on the drivers, or better, using series NFETs in the driver circuit.



Multiple Power Domains – The Problem

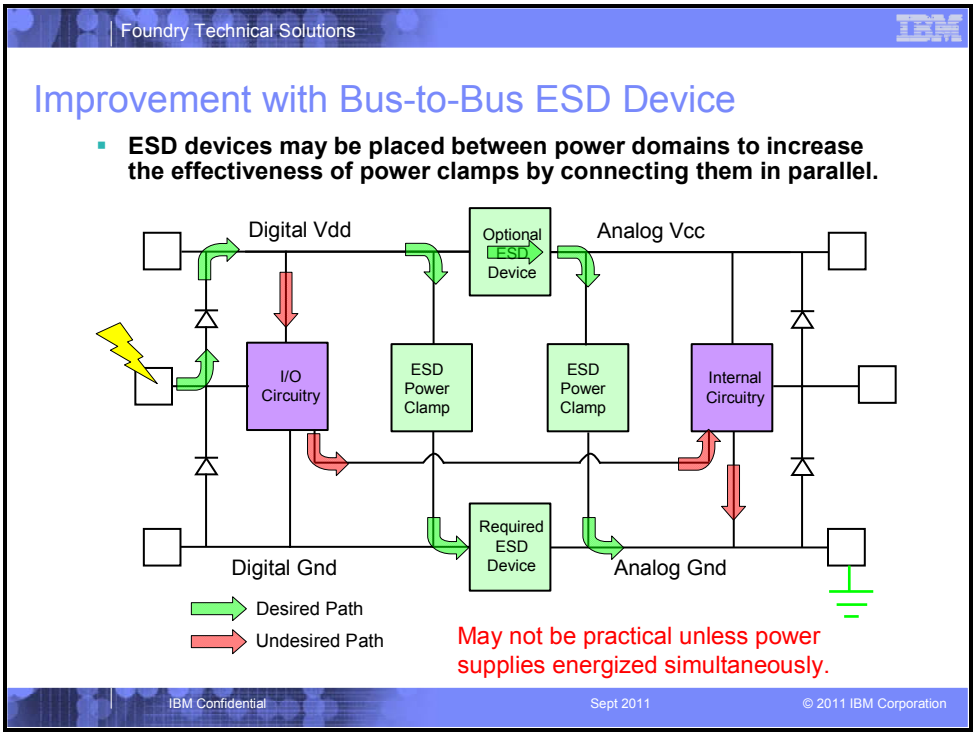
The previous slide showed ESD protection for a chip with a single power and ground domain. We will now explore protection of chips with multiple power and/or ground domains. Consider a chip with two separate power supply and ground domains as shown. Each power supply domain has the required ESD devices and power clamps. This circuit will exhibit good ESD performance as long as the discharges do not cross supply domain boundaries. If a discharge occurs between the digital I/O pin and the ground of the analog domain, the device will fail at low ESD voltage. The current enters the digital I/O pin and follows the forward-biased up diode to the logic power supply. From that point, the only path to the analog ground bus is through the logic circuitry, along the connection between the digital circuitry and the analog circuitry, and then to the analog ground. None of these paths are designed for high current, so the failure voltage will be unacceptably low.



Multiple Power Domains – The Solution

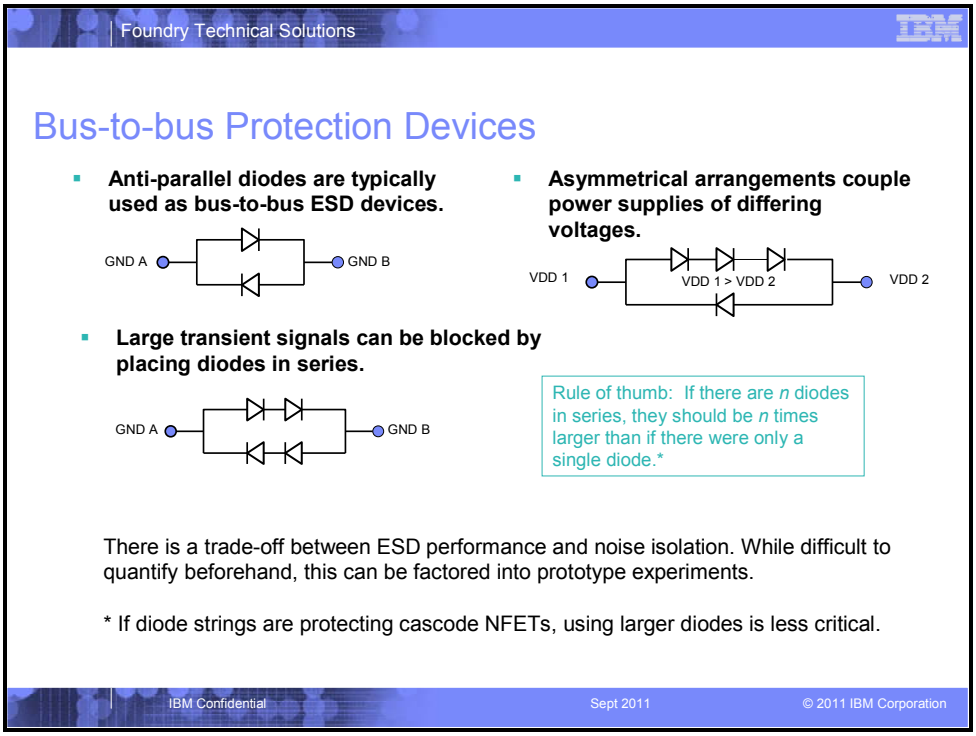
A correct design for ESD protection and the resulting discharge path between supply domains is shown in the above slide. This design connects the ground domains with an ESD device. This device is typically implemented with a set of anti-parallel diodes (diodes wired in parallel but with opposite polarity). The current enters the digital I/O pin and travels to the digital Vdd bus. The power clamp in the digital supply domain conducts the current to the digital ground bus, and the added ESD device allows that current to flow to the analog ground bus. The designer can also add an ESD device between the power supply buses as shown by the box bounded by dashed lines. The advantage provided by this element is shown in the next slide.

One situation that deserves mention is that where multiple ground domains are unconnected on the die, but later wired together at the package level (for example if the module has a ground paddle). It is preferable to have the ground domains connected by ESD devices on the die, but it is acceptable to leave them unconnected on the chip as long as they are connected together at the package. Ground domains must be wired together or connected by ESD devices at the module level. The ESD penalty of isolated ground domains is severe.



Improvement with Bus-to-Bus ESD Device

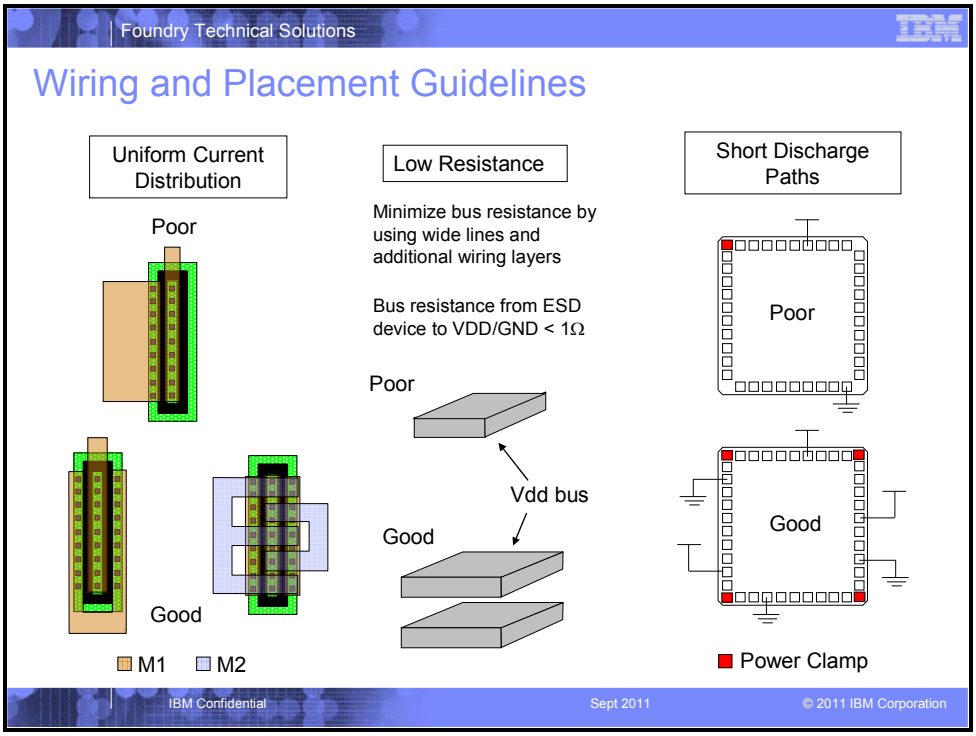
Previously it was shown that an ESD path can be provided by connecting only the ground buses with an ESD device. Additional advantage may be gained by placing an ESD device between power rails. This device provides a second path to the analog ground pin through the second ESD power clamp. This increases the current that can be tolerated without damage and lowers the voltage that is developed on the digital I/O pin.



Bus-to-Bus Protection Devices

The ESD devices connecting power supplies and grounds are simply various configurations of anti-parallel diodes. The most straightforward arrangement is shown in the upper left: two diodes connected in parallel with opposite polarity. Use the asymmetrical circuit in the upper right when connecting power supplies with different voltages. The number of diodes in series is chosen to prevent current from flowing between power supplies. If one of the power supplies or ground buses has large transient signals diodes may be placed in series as shown in the schematic on the lower left side of the page. When diodes are wired in series, the on-resistance of the series string can become so large as to develop harmful voltages across the circuitry being protected. This can be avoided by increasing the diode perimeter for the individual diodes in series strings. As a general rule of thumb, use n times the diode perimeter if you wire n diodes in series. This is most important when the device is protecting single NFETs as they will be destroyed if the voltage exceeds the snap-back voltage. Cascoded NFETs are less vulnerable because the snap-back voltage of the series pair is higher than a single device.

The presence of ESD devices between power supplies will influence power supply sequencing requirements for the design. If one domain is unpowered the ESD device will conduct current from the powered to the unpowered domain. Of course, generally the reason why the supplies are separated is to alleviate noise or crosstalk concerns. The junction capacitances of ESD diodes re-couple the buses to some degree; there will be a trade-off between ESD performance and isolation.



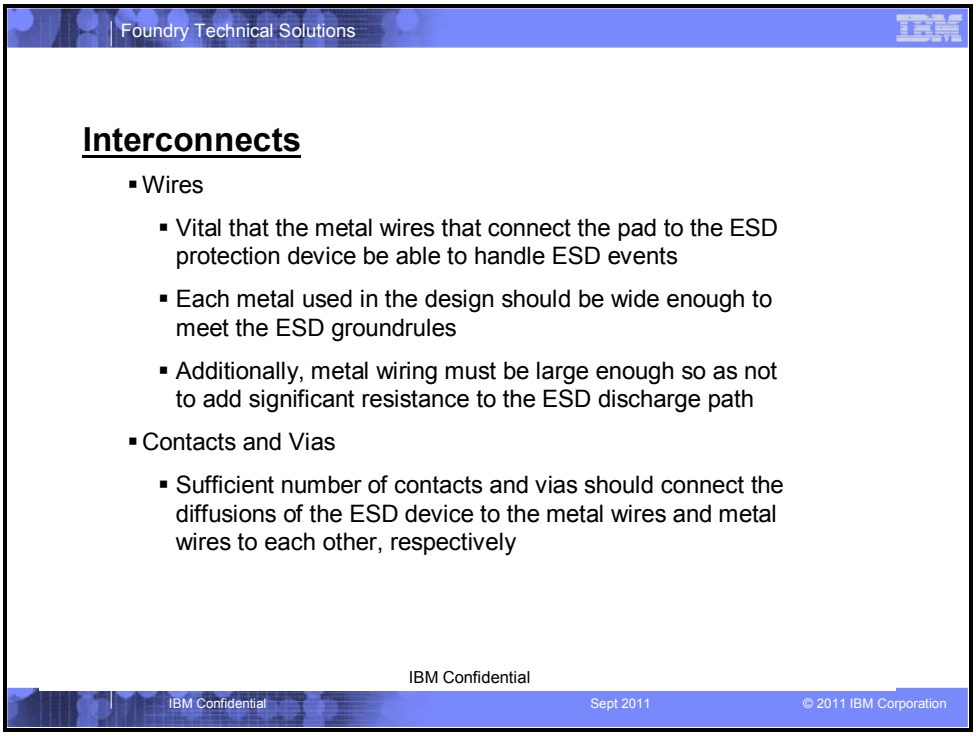
Wiring and Placement Guidelines

Successful ESD results require: wiring configurations that result in uniform current distribution, low wiring resistance, and chip floor planning that creates short discharge paths.

When wiring any device in the discharge path, ensure that the wiring arrangement does not cause current crowding. In the “poor” wiring example, note how the wiring will encourage most of the current to flow in the upper left corner of the diode. This will cause higher than expected series resistance and early thermal failure since the power dissipation is concentrated in that region of the device. The two good examples show arrangements that lead to more uniform current distribution. In the example on the lower left, any of the paths through the diode have approximately the same metal resistance (although the narrow wires may limit current handling). The example on the lower right shows the uses the first level of metal to equalize the potential along the anode and cathode stripes, and wires the anodes and cathodes out to terminals on the second metal level.

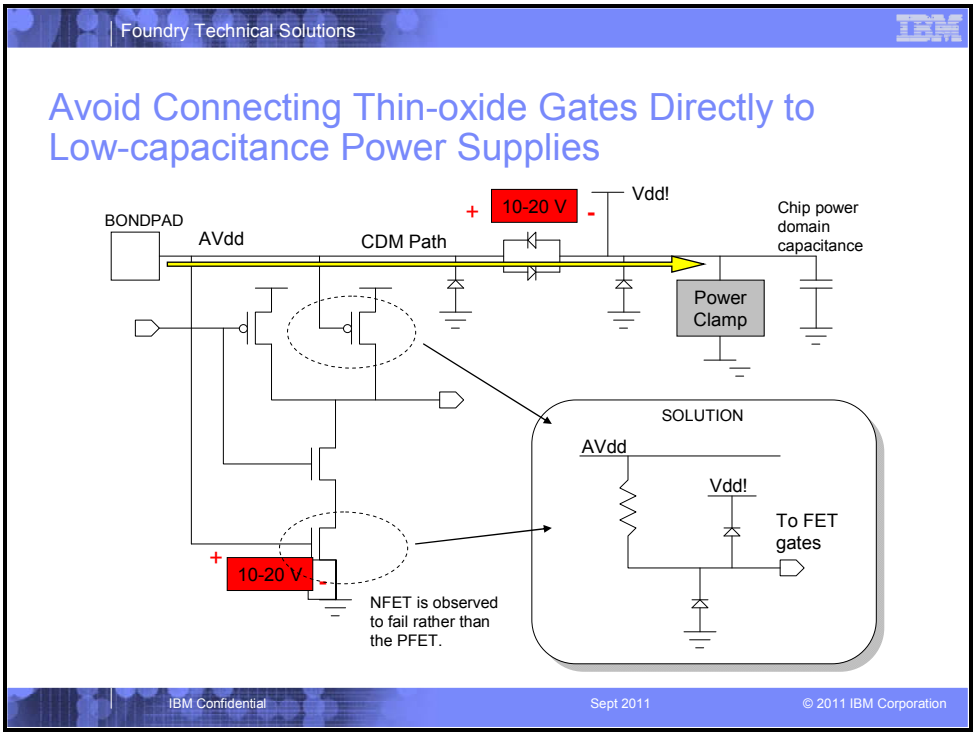
The second principle is to minimize wiring resistance. This can be difficult in power and ground buses of large chips. Use wide metal lines and additional levels of metal if possible. If additional space is available in the vicinity of wiring buses, use it to add metal and reduce the bus resistance. Strive to keep the bus resistance <1Ω in any discharge path.

The discharge path length is the distance from the I/O pad and “up” diode to the power clamp along the VDD bus, through the power clamp, then along the ground bus to the ground pin. Power clamps, power pins, and ground pins should be uniformly distributed along the chip perimeter to keep these paths as short as possible.



Interconnects Wiring Rules

All interconnects such as wires, contacts and vias that connect the ESD protection device to the pad, should be designed to handle ESD events. Wires and vias must be adequately sized to withstand the discharge currents and prevent large I×R voltage drops.



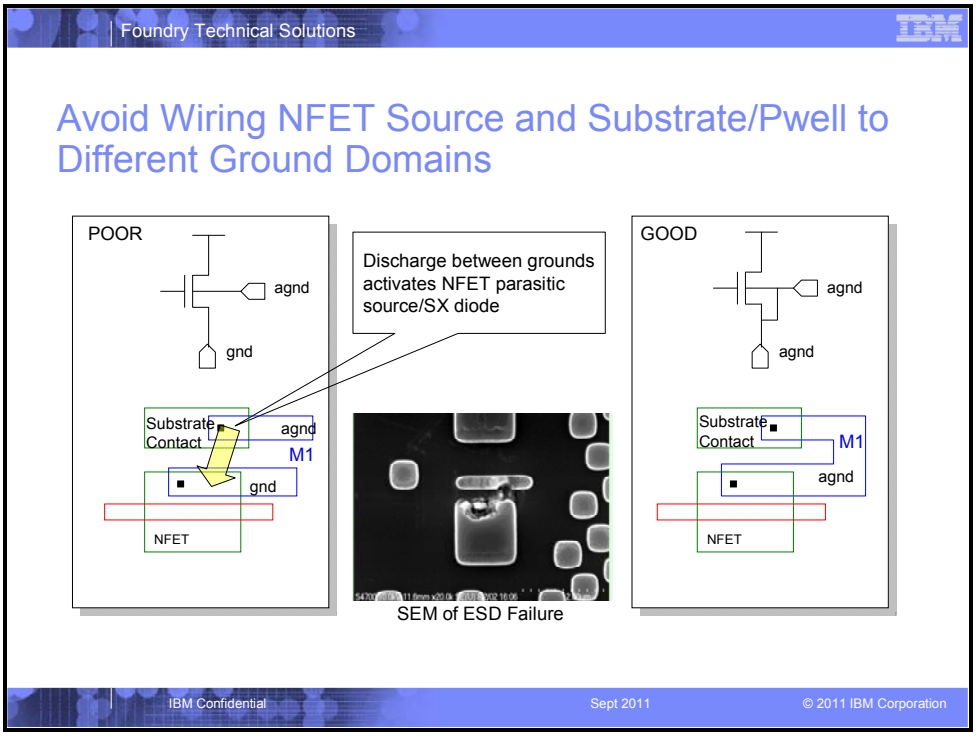
Avoid Connecting Thin-oxide Gates Directly to Low-capacitance Power Supplies

When it is necessary to connect the gate of a thin-oxide FET to Vdd, do not wire the gate directly to the power supply bus, unless these devices are ESD protection devices and are covered by ESD_HBM or ESD_CDM levels. This practice of connecting the gate directly to power supply bus can lead to low CDM failure voltages.

Consider a chip with two power supply domains as shown in this schematic diagram. The circuit function calls for one of the inputs to the NAND gate to be tied high, so it was connected directly to the AVdd power supply. Now assume that the bulk of the chip operated from the Vdd! Supply. Therefore most of the chip capacitance will be connected to that domain. The ESD design was done correctly in that the supplies share a common ground bus, the supply busses are connected using an ESD device, and there is a power clamp on the Vdd! power supply.

Now let the chip be charged to a negative voltage and grounded through the package pin connected to BONDPAD. The CDM current will flow through the anti-parallel diodes to the Vdd! bus to charge the chip. Since the peak CDM current will be 10- 20A, the AVdd bus will develop 10 – 20V with respect to ground. This will break down the gate oxide of the NAND NFET.

The solution is to tie the NAND input high through a CDM protection network as shown in the inset. When the AVdd bus voltage rises during the CDM event, a much smaller voltage develops across the gate oxide.



Avoid Wiring NFET Source and Substrate/Pwell to Different Ground Domains

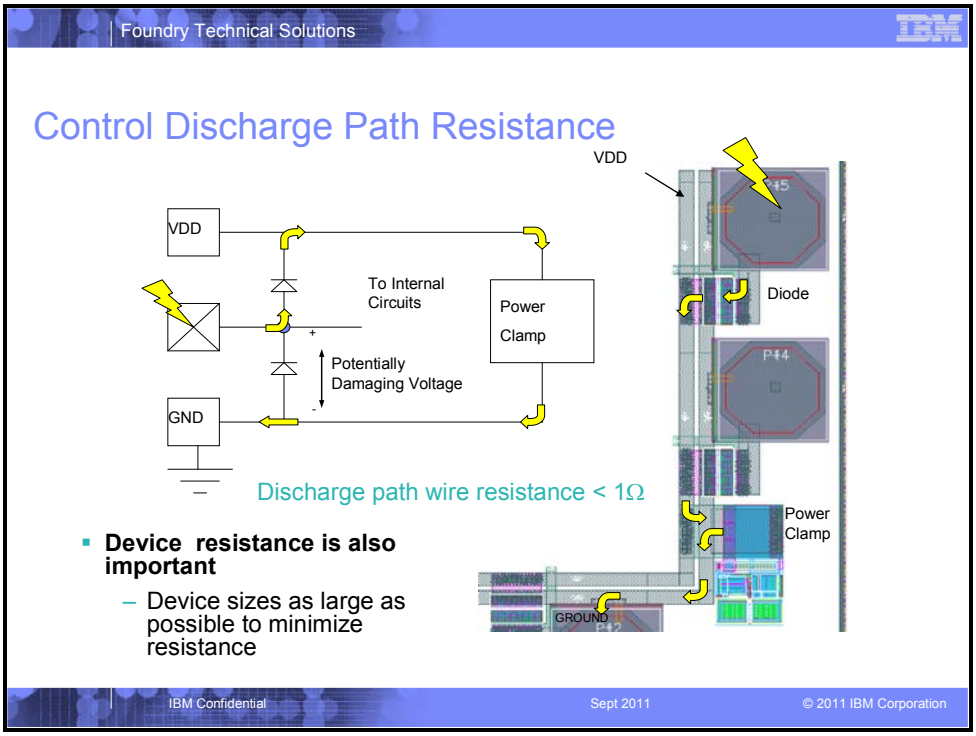
If a chip has multiple ground domains, ensure that the source and substrate/pwell of the NFET are connected to the same domain. If an NFET has the source on one domain and the substrate/pwell connected to a different domain, low ESD failure voltages can result.

Consider a chip with two ground domains: *agnd* and *gnd*. The schematic and layout on the left show the source and substrate/pwell connected to different grounds because of the proximity of the *gnd* substrate contact to the device. During an ESD discharge from *gnd* to *agnd*, the parasitic n+/substrate diode becomes forward biased and can carry a substantial portion of the discharge current. Failure analysis of this device (center) shows the damage to the device as a result of ESD conducted between the substrate contact and the FET source junction.

The correct design is shown in the schematic and layout on the right. The local substrate is connected to the same ground as the source.

Be especially careful at boundaries between circuit blocks where devices may be in close proximity to substrate contacts wired to a different ground domain. If necessary, use BFMOAT regions to increase the resistance between the substrate contact and the parasitic junction.

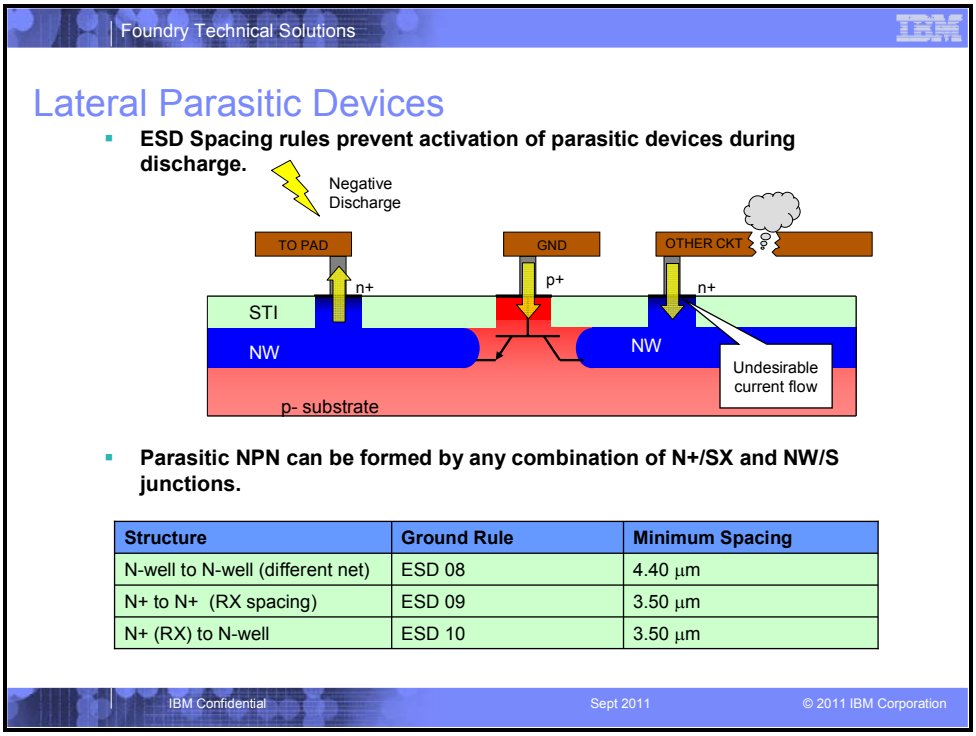
Similarly, designers should avoid connecting PFET Source and Nwell to different power domains.



Control Discharge Path Resistance

The design demonstrates good design practices using the principles of a short discharge path, adequate wire width, use of a power clamp, and broadside wiring to ESD devices for uniform current distribution.

To avoid developing a large voltage across internal circuitry, the resistance through the ESD diode, the power clamps, and the power and ground buses must be kept as low as possible.

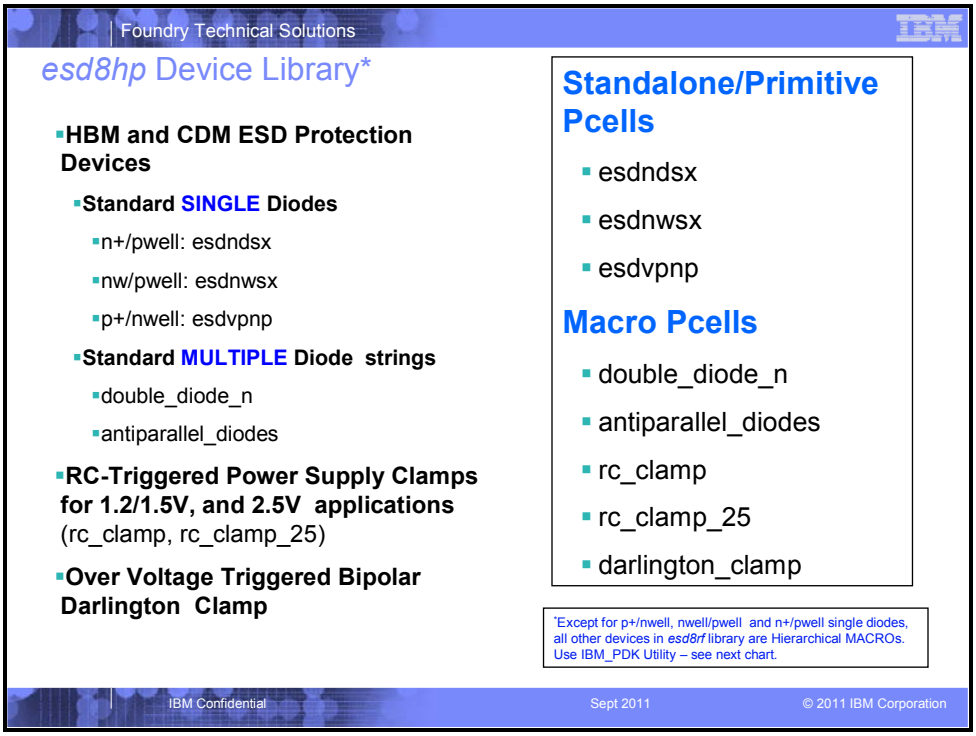


Lateral Parasitic Devices

CMOS device structures contain parasitic bipolar devices that cause latch-up. These same devices can also cause ESD vulnerabilities. Consider the two closely spaced n-wells shown in the slide

The n-well on the left is an n-well connected to the I/O pad. The adjacent n-well represents an unrelated circuit that is placed in close proximity to the first n-well. This structure forms a parasitic NPN transistor with the pad-connected n-well forming the emitter, the substrate as the base, and the adjacent n-well as the collector. During a negative discharge pulse, a large current will be drawn from the first n-well terminal as indicated by the yellow arrow. Bipolar transistor action will cause a large current to flow from the adjacent n-well, which is not designed to carry ESD currents. The resulting failure will occur at a much lower voltage than the circuit could otherwise tolerate. This effect can occur between any combination of closely spaced n+ junctions and n-wells.

The table summarizes the ESD design rules that govern the minimum spacing between n+ junctions and n-wells when one of the junctions is connected to an I/O pad.



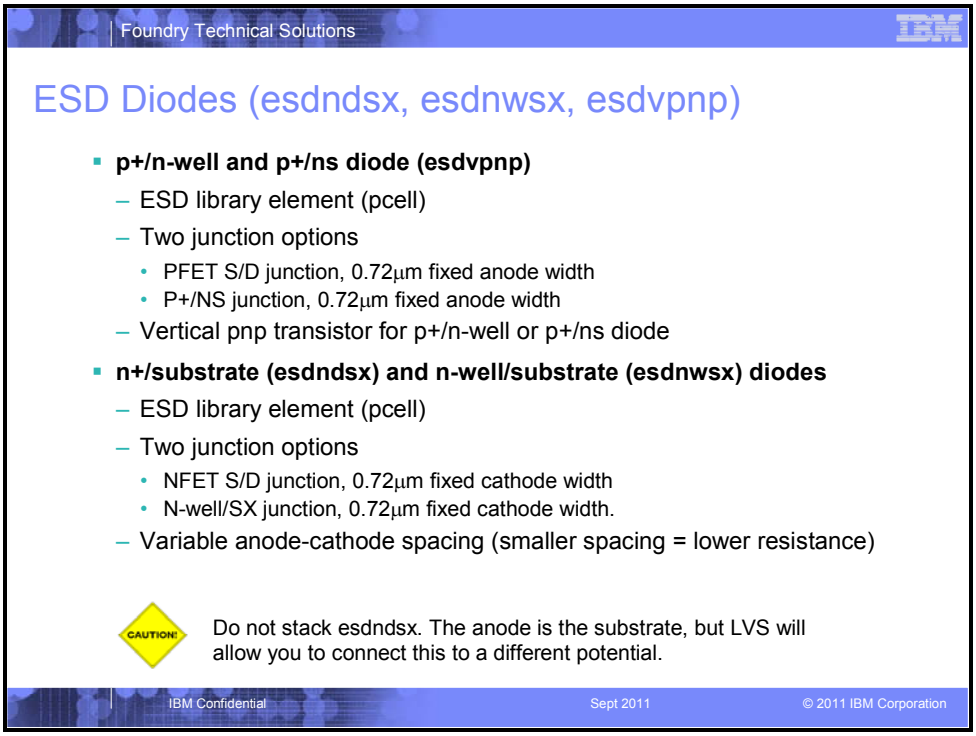
esd8hp Device Library

This slide depicts the *esd8hp* cdslib library standalone and macro pcells. In addition to these, there are other support pcells also in the *esd8hp* library; however, they are not for customer design purpose. They are needed to build the esd macros.

Standalone/primitive pcells: *esdndsx, esdnwsx* and *esdvpnp* are the ESD diode provided in the library. These ESD primitive pcells can be used directly to instantiate into the schematic and layout views.

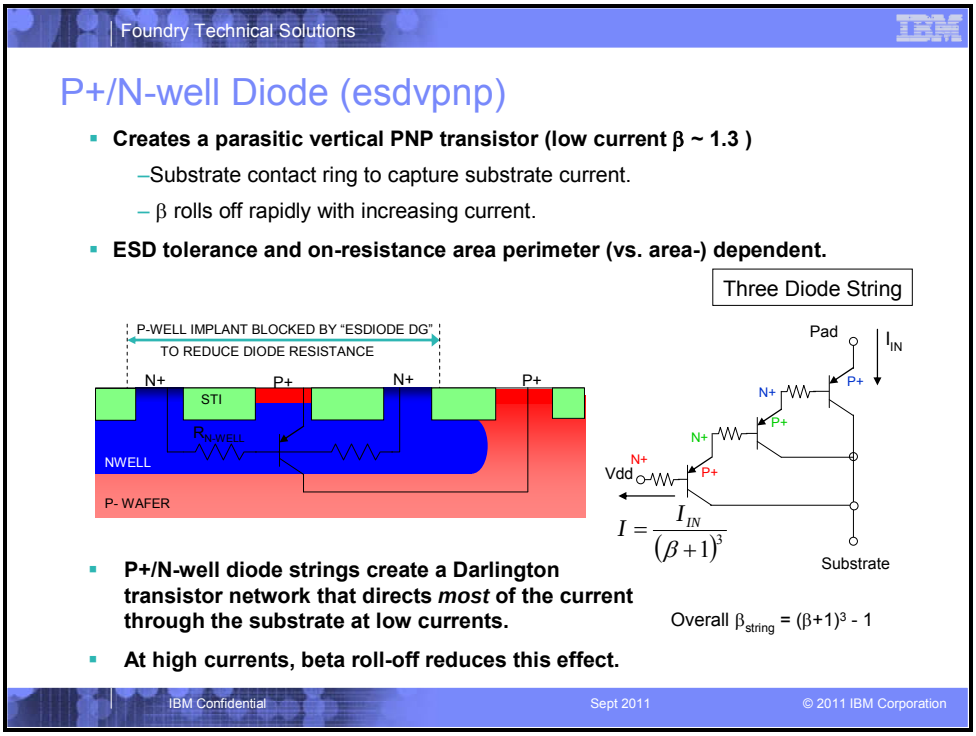
Macro pcells : All other esd devices in the *esd8hp* library– diode strings (*double_diode_n, antiparallel_diodes*), RC clamps (*rc_clamp, rc_clamp_25)* and Bipolar Darlington Clamp (*darlington_clamp*) are macro pcells. These macro pcells are created by using the Skill utility under the IBM_PDK (see next page).

Details of the esd8hp pcells (standalone and macro) are described in following pages.



Recommended ESD Diodes

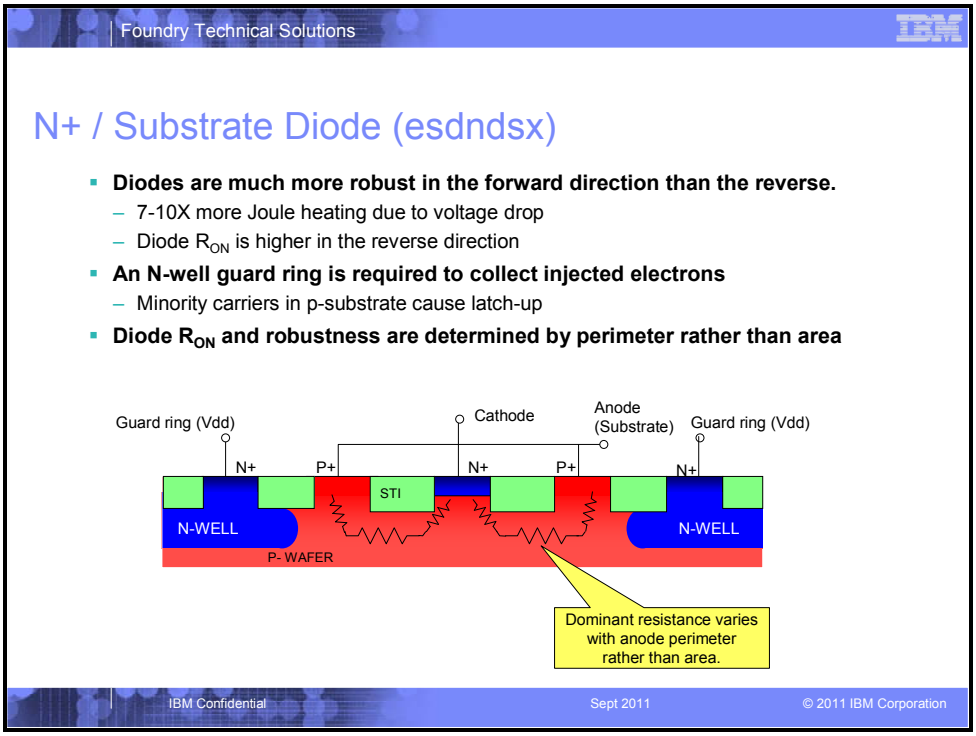
The recommended ESD diodes are the p+/n-well or p+/ns diode, and the n+/substrate or n-well/substrate diode. Each device has a dedicated model that provides accurate simulation results at RF frequencies. Models do not include forward-bias charge storage effects or high current (ESD) effects.



P+/NW Diode (esdvpnp)

A diode string is formed by series connection of P+/NW diodes. Shown in the slide above is formation of a Darlington amplifier using three (ESD) P+/NW diode strings. The Darlington amplifier can cause significant substrate current to be generated and only a small percentage of the current injected at the input may actually come out of the output terminal. The remaining goes to the substrate. The exact amount of current going to the substrate once again depends on the parasitic PNP beta. The bipolar gain rolls off rapidly with increasing current. This effect will be most pronounced at low currents because of the beta roll-off with current density.

A cross-section of the P+/NW diode (PNP transistor) is also shown in the slide above. The anode is the p+ region in the center which is placed in an N-well. The N-well contact forms a ring around the anode. Because the P+/NW and N-well/substrate junctions are in close proximity, bipolar action is observed and a portion of the current entering the p+ anode is injected into the substrate. The substrate contact forms a ring around the N-well to capture this current and prevent the local substrate voltage from rising. Only one side of the substrate contact is shown.

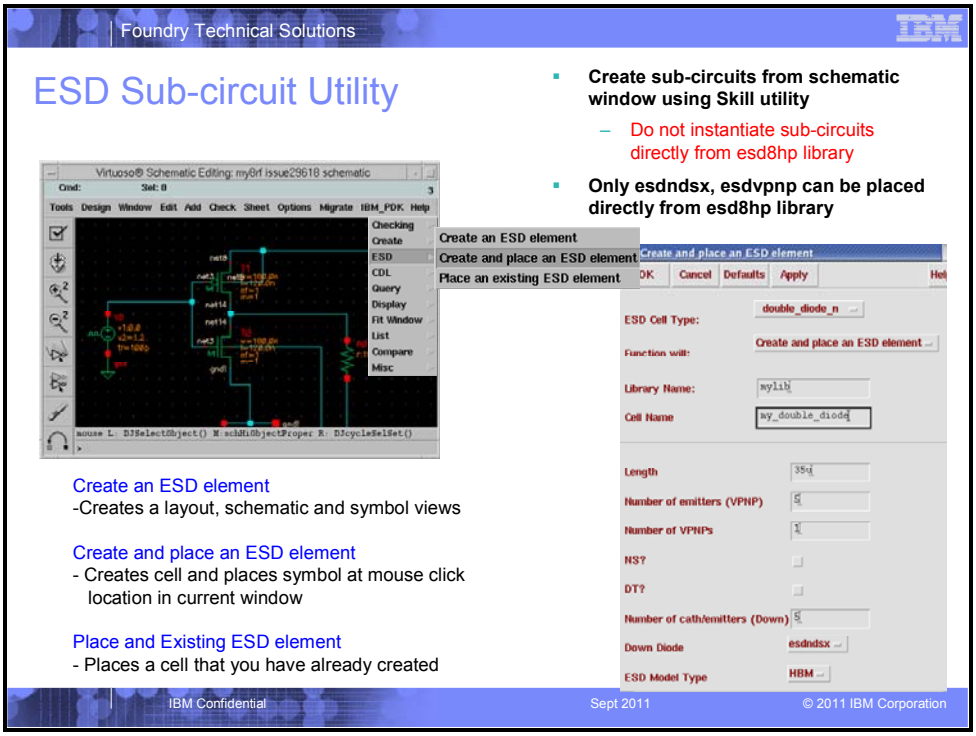


N+/Substrate Diode (esdndsx)

Another type of diode which can be used for ESD protection is the N+/SX diode. The cross section of the N+/SX diode is shown in the slide above. The center stripe is the cathode. The anode connection to the substrate is made by a substrate contact ring around the cathode. The entire structure is surrounded by an N-well guard ring to collect electrons that are injected by the n+ cathode under forward bias. In normal operation, the anode is grounded, the N-well guard ring is connected to Vdd and the cathode is connected to the I/O pin.

Diodes are far more tolerant of ESD pulses in the forward direction than in the reverse direction. Recall that an ESD discharge can be considered as a current source. The joule heating of the diode will be proportional to the product of the discharge current and the voltage developed across the diode. The differential or on-resistance of the diode is much higher in the reverse direction. This causes more heating within the diode itself and endangers other circuits because of the large voltage developed across the diode.

The N+/Substrate *esdndsx* diodes are very efficient in terms of chip layout area and provide the lowest capacitive loading.

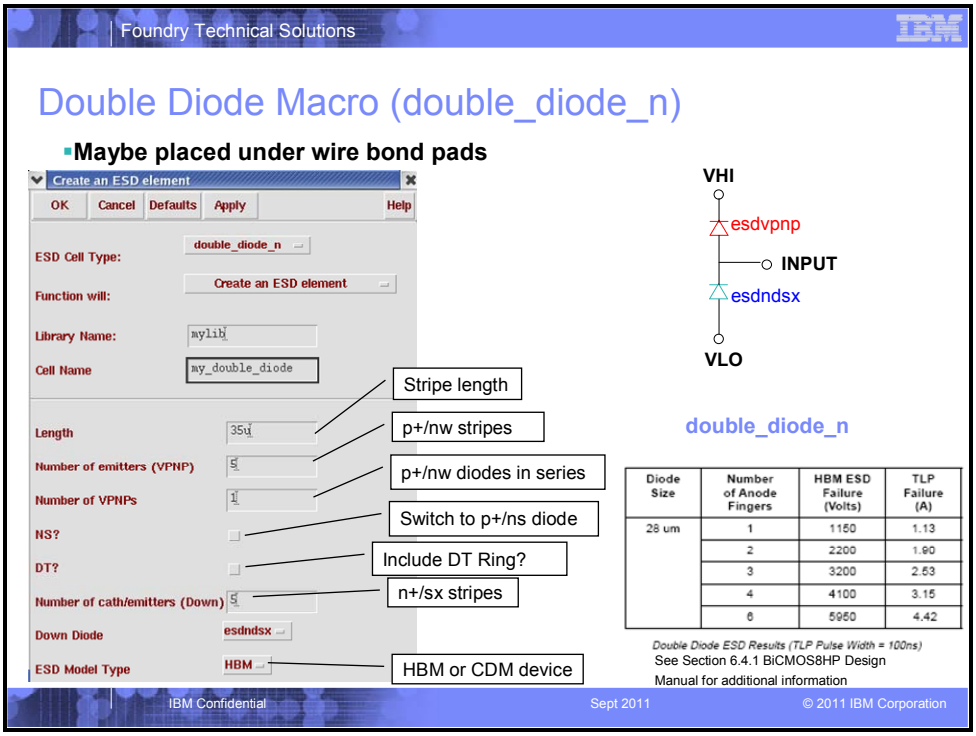


ESD Sub-circuit Utility

IBM provides a utility to create ESD sub-circuits (also termed hierarchical macros) from a schematic window. The purpose of the utility is to automatically create a customized ESD cell complete with schematic, layout, and symbol views. This new cell is created in an existing library of the designer's choosing. The utility must be used to create customized cell views from subcircuit hierarchical pcells in the *esd8hp* library. Instantiating the ESD networks (**double_diode_n, rc_clamp,** *etc.*, directly from the *esd8hp* library will cause LVS errors. ESD primitives (**esdndsx, esdnwsx and esdvpnp**) are instantiated directly from the *esd8hp* library.

As shown in the slide above, the utility is invoked from the schematic window using **IBM_PDK →ESD**. There are three choices from this menu. "**Create an ESD element**" will create the ESD cell for later use in the design. "**Create and place an ESD element**" creates the cell and then places a schematic symbol at the location designated by clicking the left mouse button in the open schematic window. "**Place an existing ESD element**" allows the designer to select and place in the open schematic window a cell that has been created previously. While the ESD cell must be created using this utility, cells created already may be placed in a design the conventional way, either as a symbol view in a schematic or as a layout view in a layout. The ESD cell symbols are compatible with Layout XL, so schematics using ESD symbols may be used to synthesize layout views.

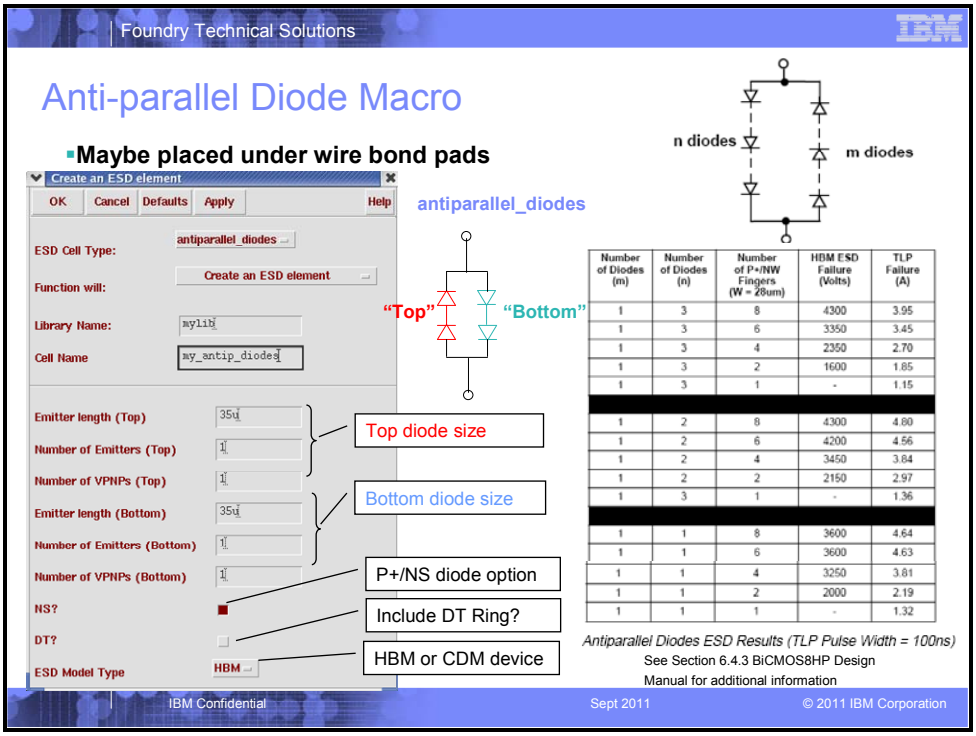
In summary, from the displayed form, choose the type of macro pcells from the pull-down menu. Provide the library name in which the element is to be created, and enter the desired optional parameters. The options for each macro pcell will be discussed in the next few slides. OK the form to create the cell. If the action is to place a cell, left-click the mouse in the open schematic window to place the symbol view and complete the action.



CMOS Double Diode (double_diode_n)

The CMOS double diode macro is created by the *double_diode_n* hierarchical pcell. It uses p+/n-well or p+/ns diodes for “up” devices and uses n+/sub or nw/sub for “down” devices. The designer may choose the number of “up” diodes in series – since more than one may be needed if the input signal can exceed the power supply voltage – and the number of anode stripes on both the “up” and “down” diodes. Anode length is adjusted by choosing the number of cathode wires.

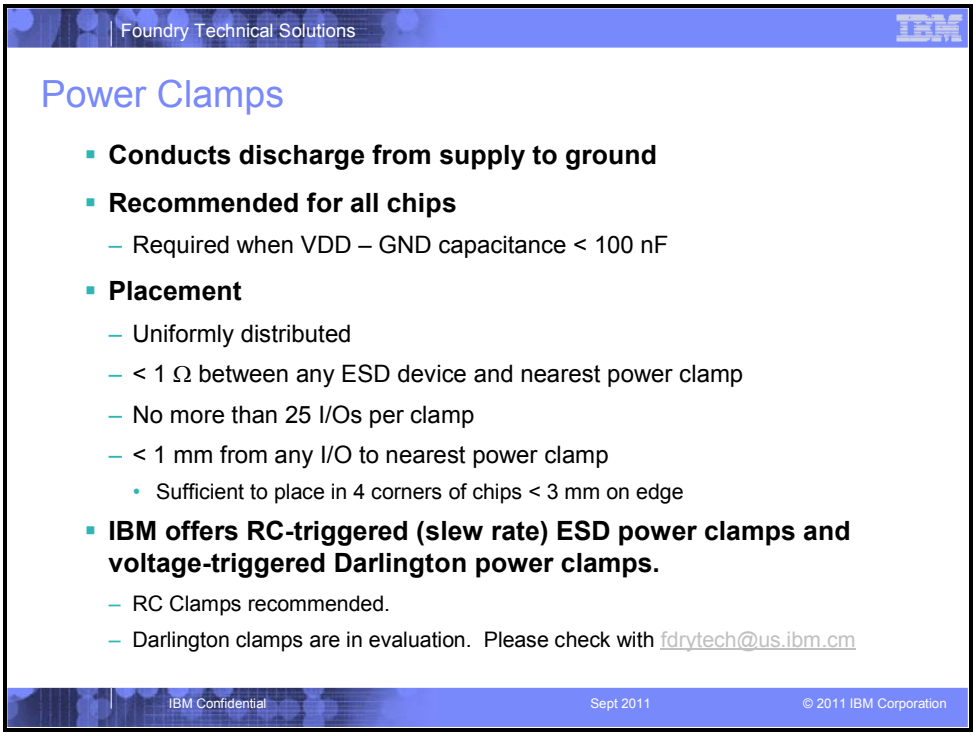
See Section 6.4.1 in the BiCMOS8HP Design Manual for additional information and measured TLP data.



Anti-parallel Diode Macro

Anti-parallel diode pcell can be created with the *antiparallel_diode* macro. Like the double diode macros, these are created using the IBM_PDK utility.

See Section 6.4.3 in the BiCMOS8HP Design Manual for additional information and measured TLP data.



Power Clamps

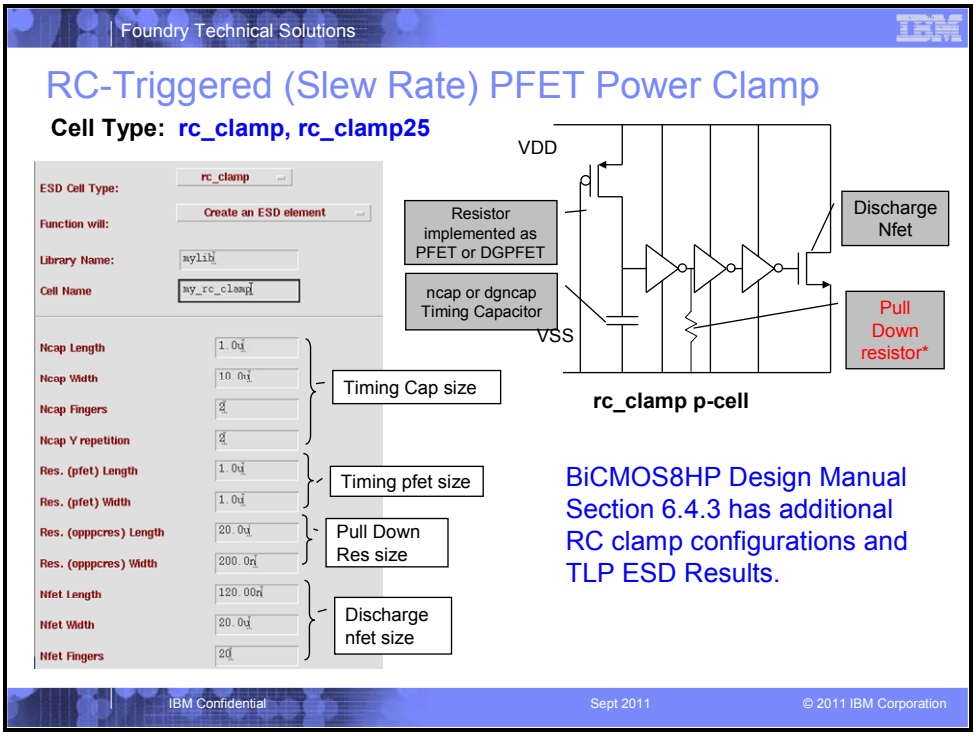
Power clamps perform a crucial role in conducting discharge current from the power supply to ground during an ESD event. The ideal power clamp should not conduct current except during an ESD discharge, and would develop very little voltage at high currents when activated. Capacitance is not a concern since the power clamp is wired between the power supply and ground. Instead, physical size is generally the limiting factor in the design.

Power clamps are recommended for all chips. However, clamps can be omitted on chips or individual power domains that have supply-to-ground capacitance greater than 100 nF. Large supply-ground capacitance is capable of bypassing the ESD discharge without the power clamp.

For larger chips, place power clamps uniformly along the edge so that no more than 1Ω wiring resistance occurs between an ESD device and the nearest power clamp. As a general rule use at least one power clamp per 25 I/Os and do not allow more than 1 mm distance between any I/O and the nearest power clamp. For small chips, less than 3 mm on a side, it is generally sufficient to place a power clamp in each corner of the chip.

The BiCMOS8HP design kit offers two types of ESD power clamps: bipolar transistor clamps that trigger on an over-voltage condition and PFET clamps that trigger when the power supply voltage is raised rapidly (slew rate,).

It is recommended to use RC clamps. Darlington clamps are in evaluation. Please contact fdrytech@us.ibm.com .



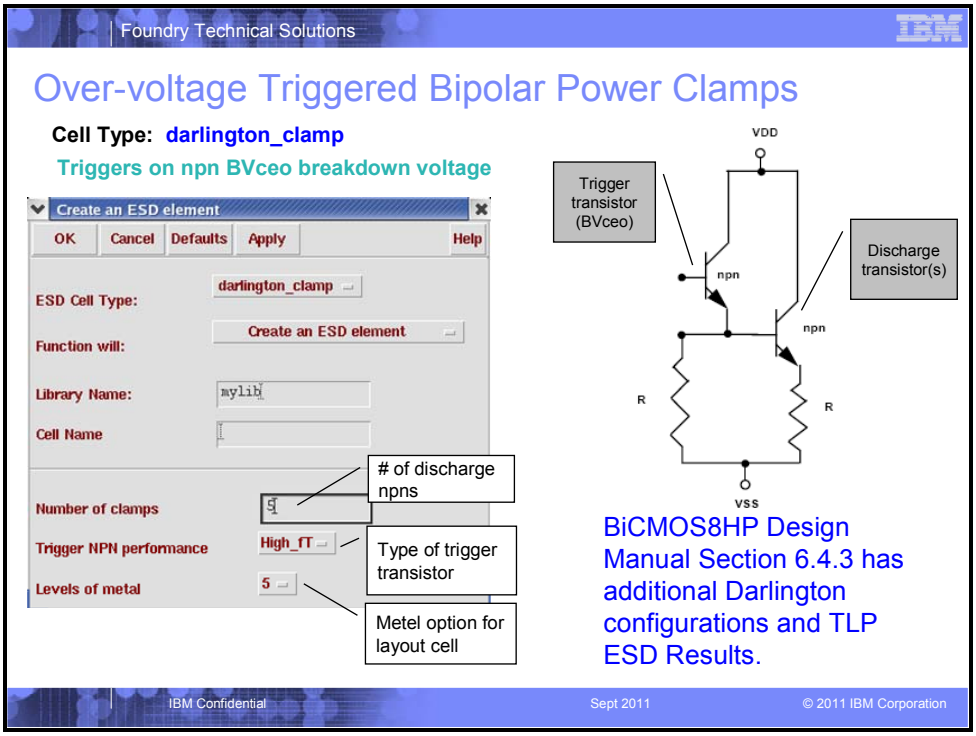
RC-Triggered (Slew Rate) PFET Power Clamps

The slew rate triggered power clamp circuit can be understood by considering it in three parts. The discharge device, a large NFET, is on the right hand side. Working towards the left, this NFET is controlled by three inverter stages. The input of the first inverter stage is a RC trigger controlling the discharge NFET's on time during an ESD event. The resistor is formed by a PFET with the gate tied to ground. At steady state, the capacitor is charged to supply voltage, which represents a logic “high” to the first inverter. This translates through the inverter chain to a “low” signal to the discharge NFET. If the supply voltage is suddenly raised, such as during an ESD event, the capacitor maintains the steady state voltage at the input of the first inverter, and this now represents a logic “low” at the new higher power supply level. A logic “high” is then presented to the discharge NFET, which conducts the discharge current to ground.

Power clamps are offered to work at 1.5V and 2.5V. These power clamps are offered for use on various voltage power buses. A power clamp with the appropriate NFET width should be used, such as to maintain the I/O pad voltage below the snapback or gate breakdown voltage of the devices connected to the I/O pad.

Hot plug environments can cause problems because a very rapid power-up will trigger the discharge transistor. Simulate the clamp with the expected power-up slew rate to insure there will be no false triggering.

See Section 6.4.3 for additional RC-triggered power clamp configurations and measured TLP ESD data.



Over-voltage Triggered Bipolar Power Clamp

In the bipolar power clamp (Darlington clamp), the trigger and discharge devices are open-base high f_T NPN transistors. When the supply bus reaches BV_{CEO} for the trigger transistor, it starts to conduct, developing a voltage across the resistor to ground. When the resistor voltage reaches approximately 0.8V, which is to say, when the total applied voltage reaches BV_{CEO} + 0.8V, the discharge transistors are turned on.

There is only one bipolar power clamp macro, *darlington_clamp*, available:in the *esd8hp* library.

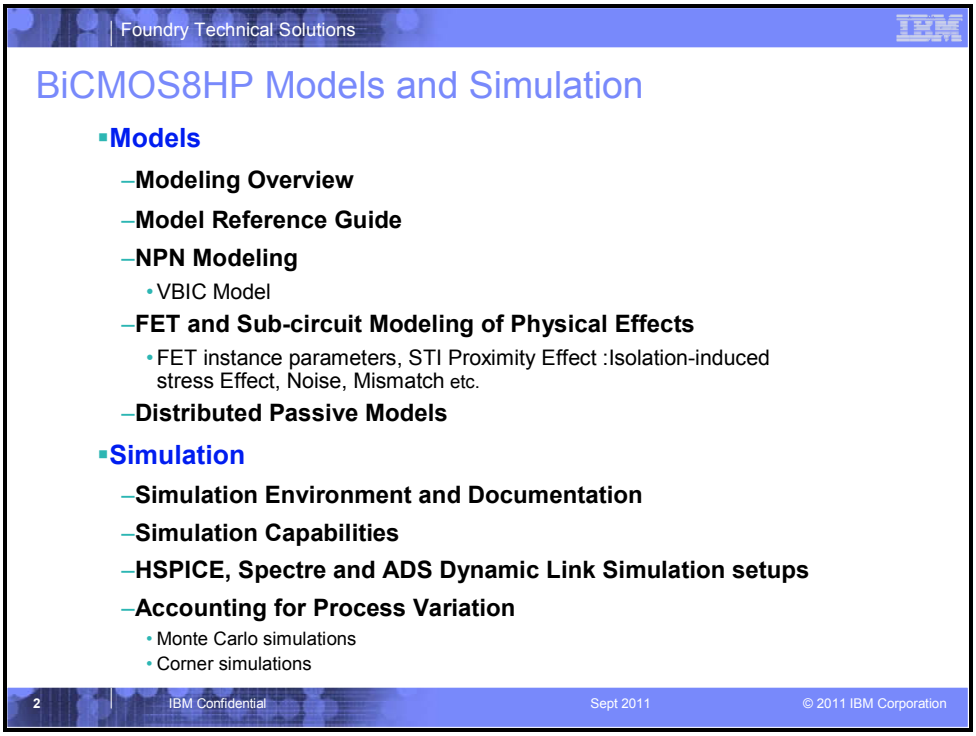
A variable trigger Darlington power clamp is described in the Section 6.4.3 of the BiCMOS8HP Design Manual which shows how to incorporate one or more diodes in series with the open-base transistor to raise the trigger voltage. For a typical application that is expected to operate to 125°C, each diode represents approximately 0.5V increase in trigger voltage *from a leakage perspective*. From an ESD perspective, each diode represents about 1V higher voltage drop during a discharge. This difference is because of the current levels that are important for leakage vs. ESD.

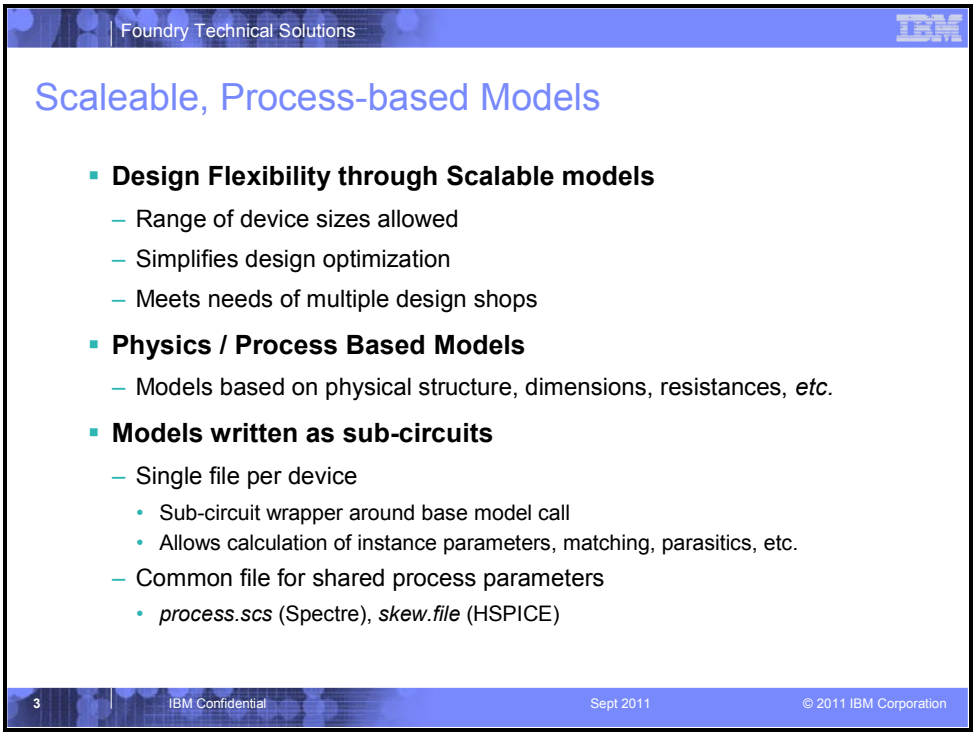
The bipolar clamp must be created using the IBM_PDK utility.

See Section 6.4.3 for measured TLP ESD data.

Models and Simulation

This section provides an overview of the modeling and simulation support provided within the BiCMOS8HP design kit. Many aspects of the passive device models have already been presented in the Technology and Device Library Overview section, so emphasis here is on the Monte Carlo and corner simulations, and the physical effects included in the NPN and FET models. We also explained some enhanced distributed passive device simulation capability.

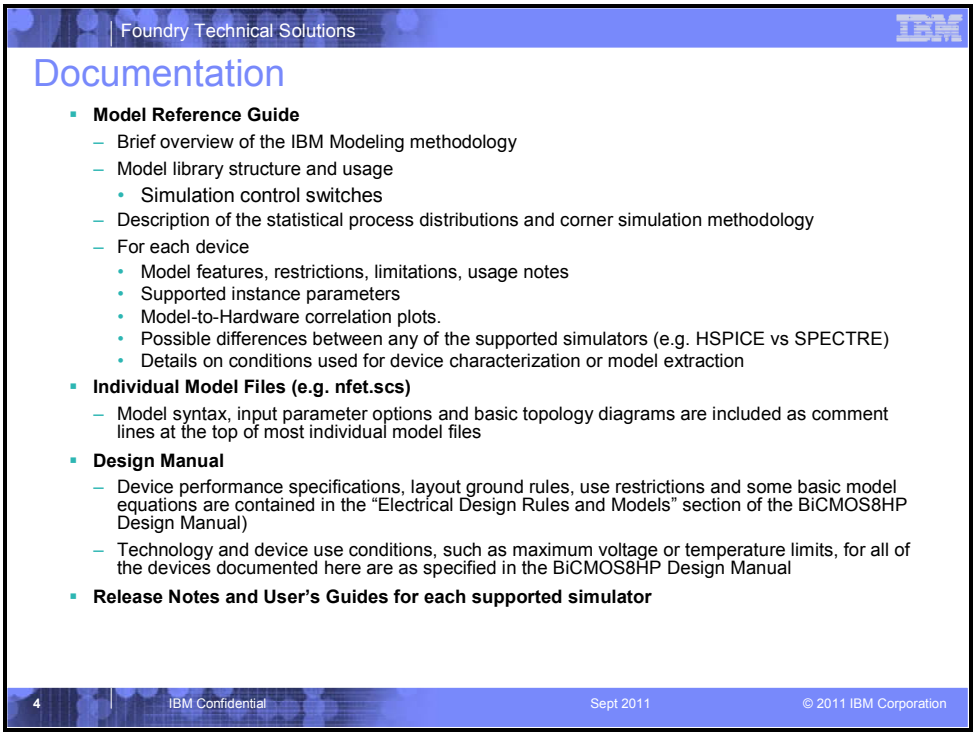




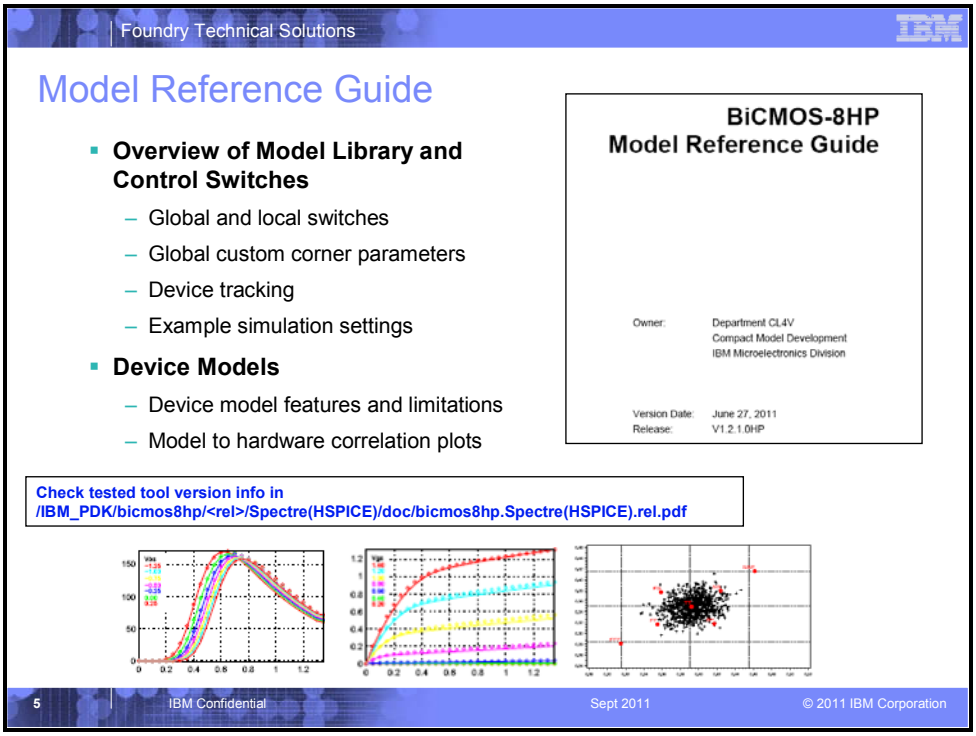
Scalable, Process-based Models

The models in the IBM design kits are scalable to a range of device sizes and options. Therefore, they cover a variety of device sizes without "binning." Scalable models in conjunction with the associated parameterized cells support varied design styles and circuit types. The models are based on relevant device physics and process parameters. This assures that models have the correct dependence on geometry and process parameters. Models are validated against hardware measurements over a range of device geometries.

IBM devices are modeled as sub-circuits using standard device models embedded in networks containing primitive circuit elements (R, L, C, diodes, *etc.*) to properly model parasitic elements such as junction capacitance or series resistance. Sub-circuit networks are also employed to properly represent the effects of distributed resistance and capacitance for accurate high-frequency prediction. Common process parameters are stored in a single file; **process.scs** for Spectre and **skew.file** for HSPICE.

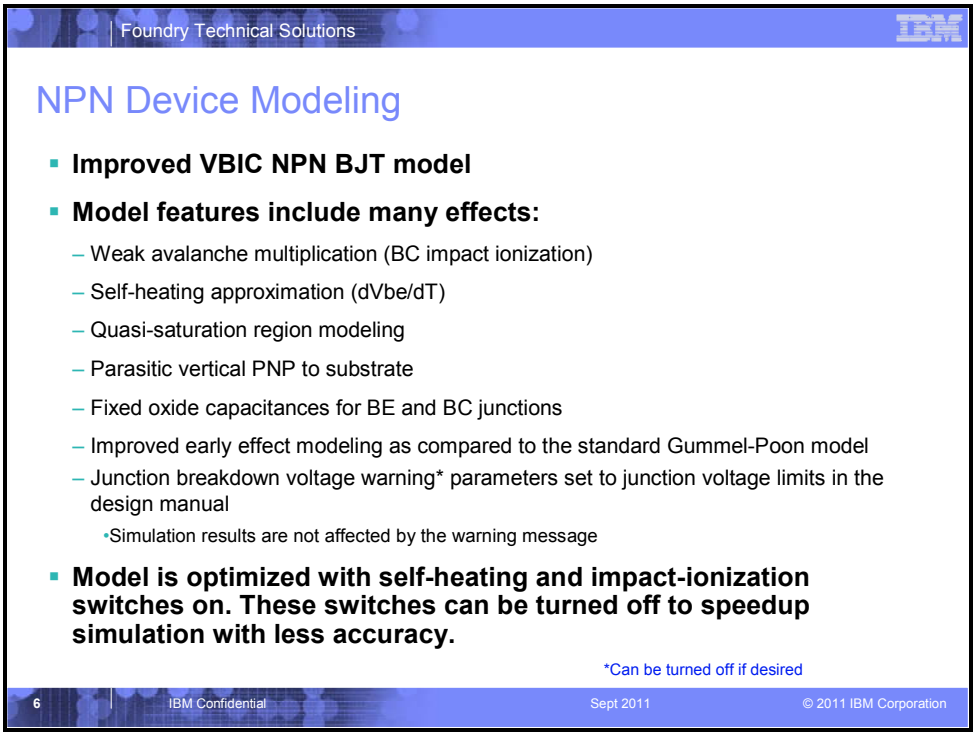


Documentation



Model Reference Guide

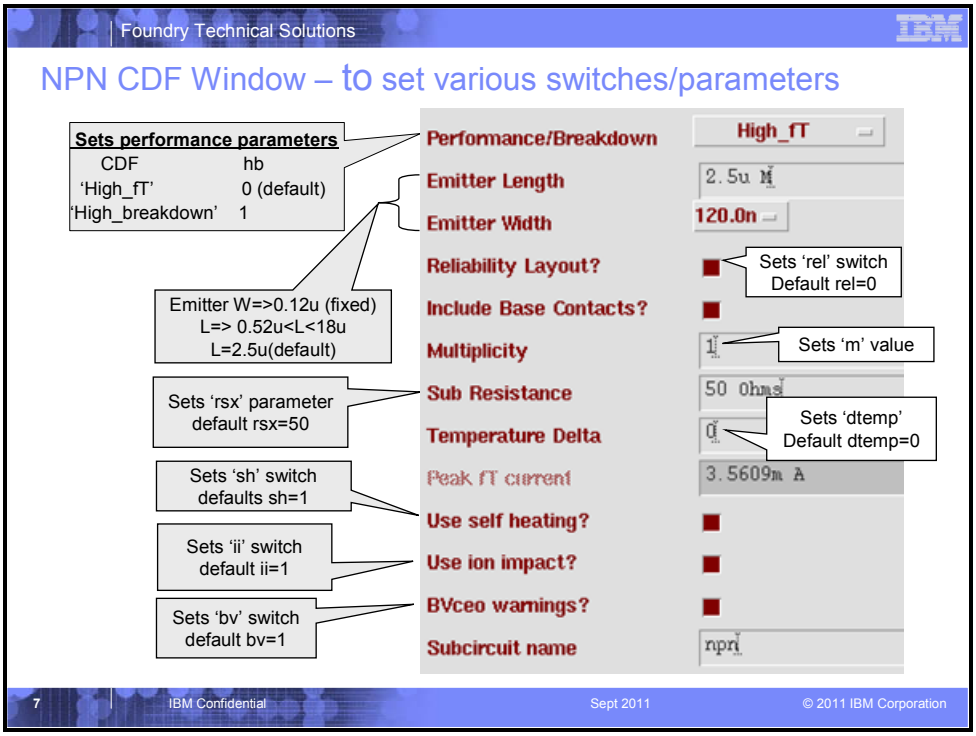
The Model Reference Guide, which can be found in the design kit in the **/IBM_PDK/bicmos8hp/relHP/doc** folder provides detailed correlation of models to hardware and notes on any model limitations such as maxim/minimum size sizes or verified frequency ranges. It is also the best resource for the simulation setup examples, all global and local switch usages, and custom corner information.



NPN Device Modeling

The IBM BiCMOS8HP PDK supports Vertical Bipolar Inter-Company (VBIC) model.

The improved VBIC model included many effects such as weak avalanche, quasi-saturation region modeling and self-heating. Please refer to the Model Reference Guide for additional details on the VBIC model. There is a switch in CDF of HBT devices to issue warnings when the voltage exceeds the breakdown voltage of junctions, set by the BVceo or BVcbo. The warnings are intended to be a design aid as the device's breakdown voltage in the circuit such as BVcer may improve due to lower base impedance presented. The simulation results are not affected by the warnings.



NPN CDF Window

The slide shown above shows a portion of the CDF window for the NPN. Within this window there are several switches and parameters that can be set by the designer. This slide shows the correlation between the switches and the netlisted parameters that appear on the next page.

The default values for the High Performance (hp) and the High Breakdown (hb) NPN configurations are zero that shows that the High_fT NPN configuration is selected. The emitter width is fixed (0.12um). The emitter length can be set between 0.52um to 18um.

The NPN models have optional switches to turn-off the self-heating and impact ionization effects. By default, these options are enabled (checked box). Model is optimized using these features. If these switches are not enabled, the output characteristics of the model will not accurately represent the hardware measurements. The switches may help improve simulation time by allowing the designer to de-activate these options for non-critical devices. NPN breakdown check feature (using switch 'bv') is only functional with the VBIC model.

FET Subcircuit Modeling of Physical Effects

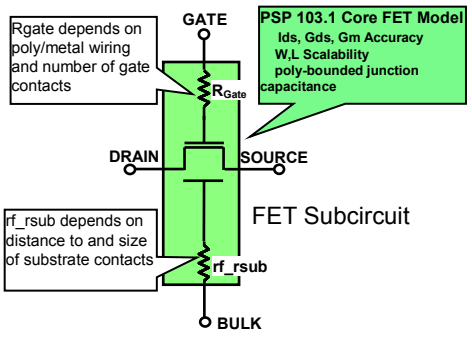
- **PSP 103.1 core FET model, with sub-circuit wrapper**
- **AS/AD/PS/PD must be calculated and netlisted**
  - Internal estimation of junction area/perimeter not supported
- **STI proximity effect : Isolation-induced stress**
  - Affects mobility and threshold voltage
- **Components of FET mismatch**
  - Dopant variations
  - Geometric variations
- **Oxide breakdown warning switch (gbv)**

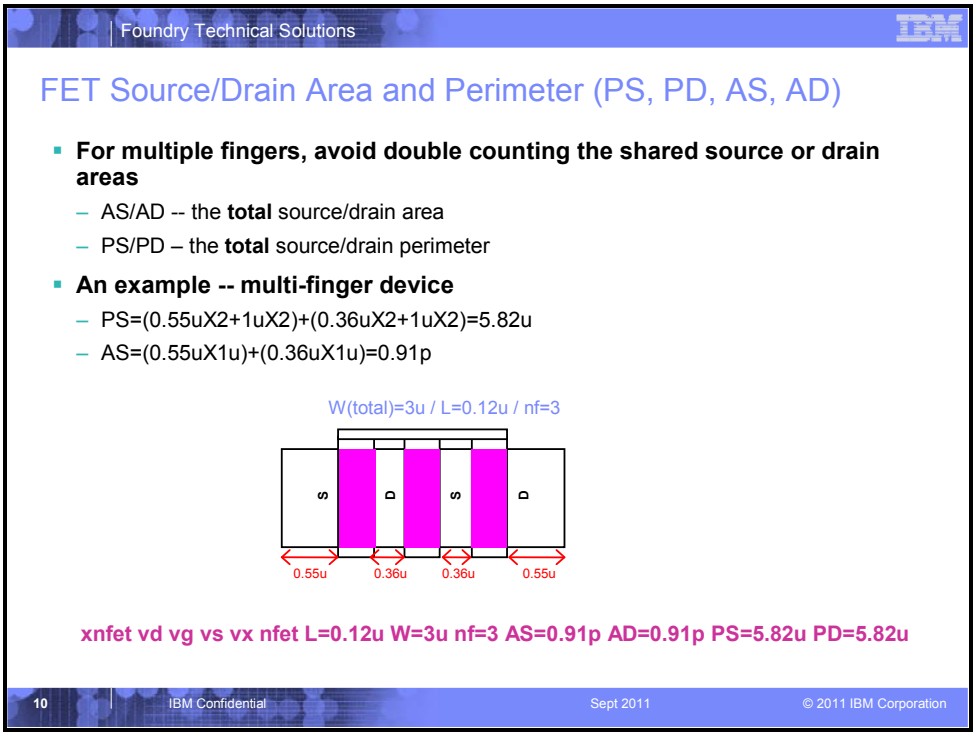
FET Sub-circuit Modeling of Physical Effects

The FET subcircuit has the BSIM4 model as its core, with a wrapper that includes the calculation of various model parameters based on global switch values, instance parameters, and the type of simulation (process and/or mismatch Monte Carlo or nominal or corner simulation).

FET Model

- **Wrapper around PSP 103.1 model**
- **PSP 103.1 features include**
  - Intrinsic gate resistance that consists of both the NQS (Non-Quasi Static) channel resistance and the distributed resistance of gates contacted from one or both ends using the instance parameter "ngcon"
  - User-defined, layout dependent extrinsic substrate resistance (rf_rsub) for accurate modeling of the substrate resistance
  - Use of the PSP thermal and 1/f noise equations
  - Modeling of impact ionization
  - Includes device mismatch as a function of threshold voltage and mobility mismatch, and Shallow Trench Isolation (STI) stress effects





FET Source/Drain Area and Perimeter

The FET models require that the source and drain area and perimeter are netlisted. The model uses the BSIM4 convention where the parameters as, ad, ps and pd represent the total area and perimeter for multi-fingered devices. The models do not estimate these parameters by themselves. The as, ad, ps, and pd parameters are either calculated in the CDF and netlisted to the model (schematic simulation) or extracted from the layout.

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STI Proximity Effect : Isolation-Induced Stress

- **Shallow trench isolation (STI) edges introduce compressive strain in silicon**
  - Decrease NFET drain current
  - Increase PFET drain current
  - Function of width, length, proximity of STI edges

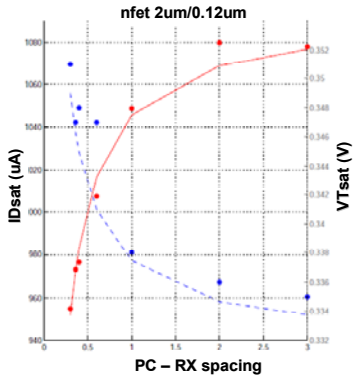

Table 49. Isolation Proximity Effect Example

Device (Geometry)	Bias	Idsat	Vtsat
NFET (5µm x 0.12µm x 1)	$V_{GS} = V_{DS} = 1.5V$	-12.5%	+3.7%
PFET (5µm x 0.12µm x 1)	$V_{GS} - V_{DS} = 1.5V$	+10.5%	-2.8%
DGNFET (5µm x 0.24µm x 1)	$V_{GS} = V_{DS} = 2.5V$	-6.5%	+5.4%
DGPFET (5µm x 0.24µm x 1)	$V_{GS} = V_{DS} = 2.5V$	+7.3%	-1.5%

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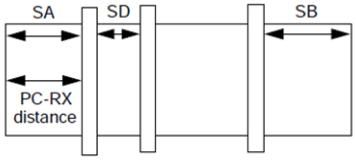
Isolation-Induced Stress

An important physical effect included in the FET models is the compressive strain that the shallow trench isolation induces in the silicon. The strain alters the mobility, causing an decrease in the magnitude of drain current for NFETs and an increase for PFETs. The isolation stress model is utilized with instance parameters SA, SB and SD. The CDF will netlist appropriate values for these parameters assuming pcell default dimensions. A global switch "gstis" is available to control the effect as shown above.

Foundry Technical Solutions

Isolation-Induced Stress Effect / continued

- **built-in STI stress model is utilized**
  - SA, SB, SD replace previous stress model parameters PAM1 and PAM2
  - Models the STI stress effect by adjusting mobility and threshold
  - Supports multi-finger (nf>1) schematic simulation



- **Extraction for re-simulation post layout**
  - Extract SA/SB for each PC finger individually, no SD
  - SA, SB averaged for non-rectangular layouts
- **Global switch "gstis"**
  - Default: gstis = 2 (isolation-induced stress effect enabled through non-zero SA/SB/SD)
  - gstis = 0 (globally disable isolation-induced stress effect, for analysis purposes)
  - gstis = 1 (STI stress effects are enabled on an instance by instance basis (istis=1))

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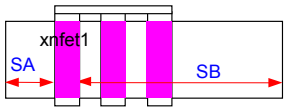
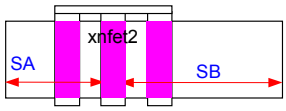
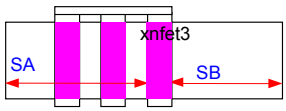
Isolation Induced Stress – extraction from layout



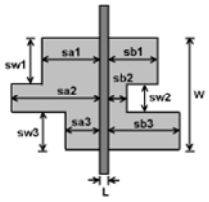




- **Extract each finger individually post-layout**
  - Series fets, multi-finger, etc
  - Also enables calculation of well proximity effects
- **Average SA, SB for irregular layouts**
  - BSIM 4.40 documentation:

$$\frac{1}{SA_{eff}+0.5\cdot L_{drawn}} = \sum_{i=1}^{n}\frac{sw_i}{W_{drawn}}\cdot\frac{1}{sa_i+0.5\cdot L_{drawn}}$$

$$\frac{1}{SB_{eff}+0.5\cdot L_{drawn}} = \sum_{i=1}^{n}\frac{sw_i}{W_{drawn}}\cdot\frac{1}{sb_i+0.5\cdot L_{drawn}}$$



xnfet1 vd vg vs vx nfet L=0.10u W=0.25u nf=1 SA=0.6u SB=2.20u
xnfet2 vd vg vs vx nfet L=0.10u W=0.25u nf=1 SA=1.10u SB=1.70u
xnfet3 vd vg vs vx nfet L=0.10u W=0.25u nf=1 SA=1.60u SB=1.2u

Isolation-Induced Stress – Extraction from Layout

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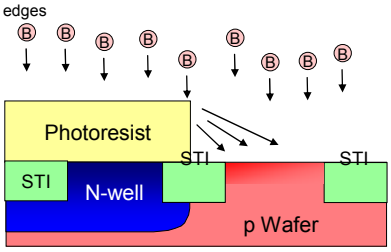
Well Proximity Effect

- **The root cause for well proximity effect**
  - High energy well implant -- dopant atom scattering at the photoresist edges changes the effective doping of the adjacent devices
  - Increases magnitude of Vt
  - NFETs/PFETs closer than ~3um from n-well and triple-well edges are affected
- **Option in CDF to add "VTSENS" layer to layout**
  - DRC will then force gates to be >= 3.0um from well edges
- **IBM well proximity effect model calculations dependent on**
  - Device dimensions, Device type, Device orientation
  - Distance of the device gate to the well edge
  - Number of proximate well edges



Example: P-well implant for the NFET

Threshold is increased near the N-well edge

Well Proximity Effect

Another effect is the well edge proximity. The high energy well implants result in significant scattering of dopants at the well edge, increasing the net doping level and hence threshold voltage for FETs near a well edge.

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Well Proximity Effect

Global switch "gwells" controls well proximity effect

gwells = 1 If instance parameter lnws=1, the well proximity effect is calculated using the provided instance parameters. (panw1..panw10).

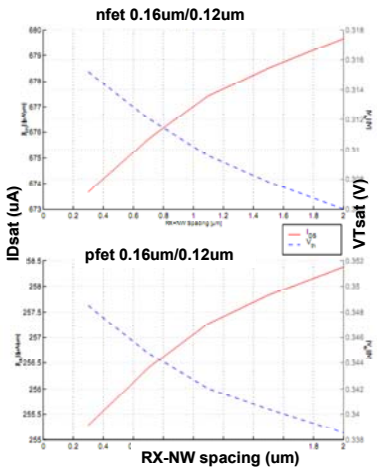
--Useful when instance parameters are available (ie, post-layout extraction)

gwells = 0 Disable the well proximity model, independent of any FET netlist instance parameters.

--Useful for comparison in post-layout simulations

gwells = 2 (default) Nwell proximity effect is calculated based on instance parameters provided in each FET netlist.

--Useful in pre-layout analysis to determine sensitivities



- **A method for adjusting the threshold voltage of the device based on the distance to a well edge**
- **Information about the circuit layout needs to be passed to the model (panw1-10)**

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Modeling of Well Proximity Effect

- Vt adjustment comes through body effect parameter k1
- panw# instance parameters based on layout information

$$k_{1\,shift} = \left(\frac{A}{l \cdot w}\right) \cdot \left[panw\ 1\ /(X\,1 - B) + panw\ 2\ /(X\,2 - B) + \cdots + panw\ 10\ /(X\,10 - B)\right]$$

where *A* and *B* are fitting parameters

and *X1….X10* are midpoint values of each band shown on next page

- Default model parameters "PANW#" set to zero (negligible well proximity)
- Effect is additive for well edges on more than one side of a device
- Model is only an estimation of the effect for a given layout
  - Variation in alignment, on wafer distances, etc not modeled
  - Follow good design practices for sensitive devices
    - Spacing to nwell, identical orientation with respect to well edge
- Well proximity and nf > 1 will not yield the correct results
  - Orientation with respect to well edge unknown for schematic simulation
  - FETs are extracted from layout as individual fingers, nf=1

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Well Proximity Effect – Modeling and Layout Extraction

Parameters PANW1-10 represent the area of the gate within discrete partitions away from the well edge. These parameters are extracted from layout and affect the device threshold voltage.

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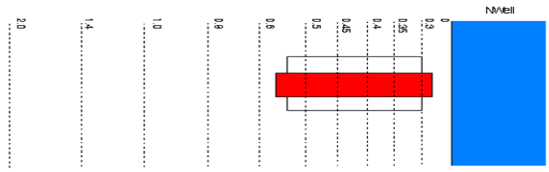
Extracted Layout Information – well proximity

The layout information needs to be passed to the FET models thought the model instance parameters:

PANW1 – the intersection of PC and RX of the device within **0 to 0.3um** of the nwell edge
PANW2 – the intersection of PC and RX of the device within **0.3um to 0.35um** of the nwell edge
PANW3 – the intersection of PC and RX of the device within **0.35um to 0.4um** of the nwell edge
PANW4 – the intersection of PC and RX of the device within **0.4um to 0.45um** of the nwell edge
PANW5 – the intersection of PC and RX of the device within **0.45um to 0.5um** of the nwell edge
PANW6 – the intersection of PC and RX of the device within **0.5um to 0.6um** of the nwell edge
PANW7 – the intersection of PC and RX of the device within **0.6um to 0.8um** of the nwell edge
PANW8 – the intersection of PC and RX of the device within **0.8um to 1.0um** of the nwell edge
PANW9 – the intersection of PC and RX of the device within **1.0um to 1.4um** of the nwell edge
PANW10 – the intersection of PC and RX of the device within **1.4um to 2.0um** of the nwell edge



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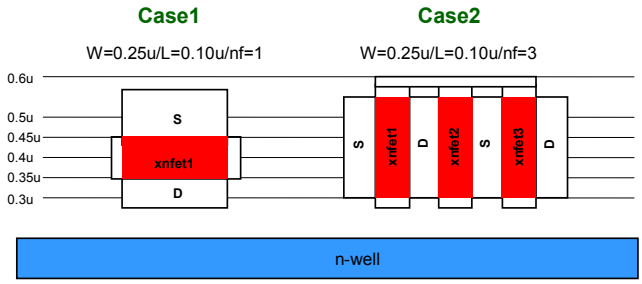
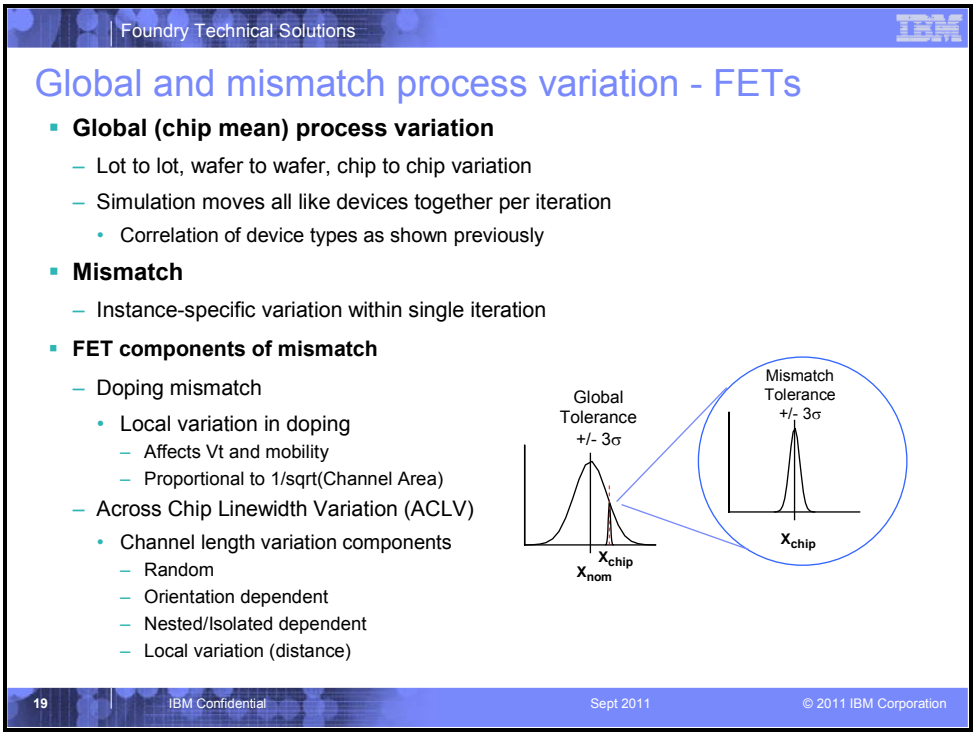
Well Proximity Effect --- testcases



Case1 ➔ **xnfet1 vd vg vs vx nfet L=0.10u W=0.25u nf=1**
+ PANW1=0 PANW2=0 PANW3=0.0125p PANW4=0.0125p PANW5=0 PANW6=0

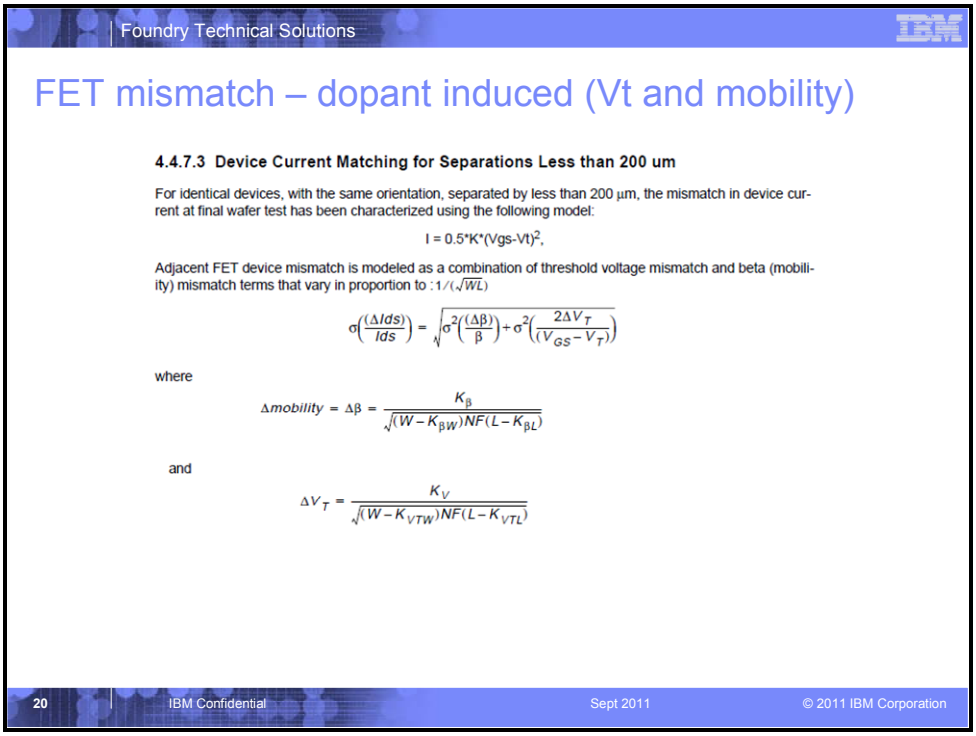
Case2 ➔ **xnfet1 vd vg vs vx nfet L=0.10u W=0.25u nf=1**
+ PANW1=0 PANW2=0.005p PANW3=0.005p PANW4=0.005p PANW5=0.005p PANW6=0.005p
xnfet2 vd vg vs vx nfet L=0.10u W=0.25u nf=1
+ PANW1=0 PANW2=0.005p PANW3=0.005p PANW4=0.005p PANW5=0.005p PANW6=0.005p
xnfet3 vd vg vs vx nfet L=0.10u W=0.25u nf=1
+ PANW1=0 PANW2=0.005p PANW3=0.005p PANW4=0.005p PANW5=0.005p PANW6=0.005p



Global and Mismatch Process Variations in FETs

As discussed previously, the model files include both global and mismatch distributions in statistical simulations. Global process variation includes lot-to-lot, wafer-to-wafer, and chip-to-chip variations. The simulator will move all like devices together in each iteration.

Mismatch refers to the instance specific variation within a single iteration. For FET devices, there are two main components to mismatch. Local variations in doping give rise to a variation in threshold voltage and mobility which is roughly inversely proportional to the square root of the channel area. The other main component is geometric, referred to as Across Chip Variation (ACV). The dominant geometric variation is the gate polysilicon length, and is called Across Chip Linewidth Variation (ACLV). ACLV has a component that is random, and also has systematic dependencies on orientation, local environment (nested with other polysilicon gates, or an isolated line), and distance. The systematic components can be controlled by the designer through careful attention to layout of critical devices for matching.



FET Mismatch – Dopant Induced

Random fluctuation in dopant level induces variation in device threshold voltage and mobility. The device models implement these mismatch components as described in the design manual.

Across Chip Length Variation Component Contributions

Component	Description	Linewidth Variation within 200 µm (µm)	Cross-Chip Variation (µm)
Site to Site variation	Identical lines w/ same spacing and environment.	**±0.005** systematic	**±0.0085**
Horizontal vs. veritcal lines (orientation)	Orientation variation in otherwise identical devices.	**±0.0045** systematic	
Nested to Isolated	Device variation induced by different layout configurations (e.g. space, density, pitch)	**±0.0053** systematic	
Total Length Variation	RSS of Site to Site, Horizontal vs. Vertical and Nested to Isolated	**±0.011**	

Designers have control over the systematic sources of variation with model switches

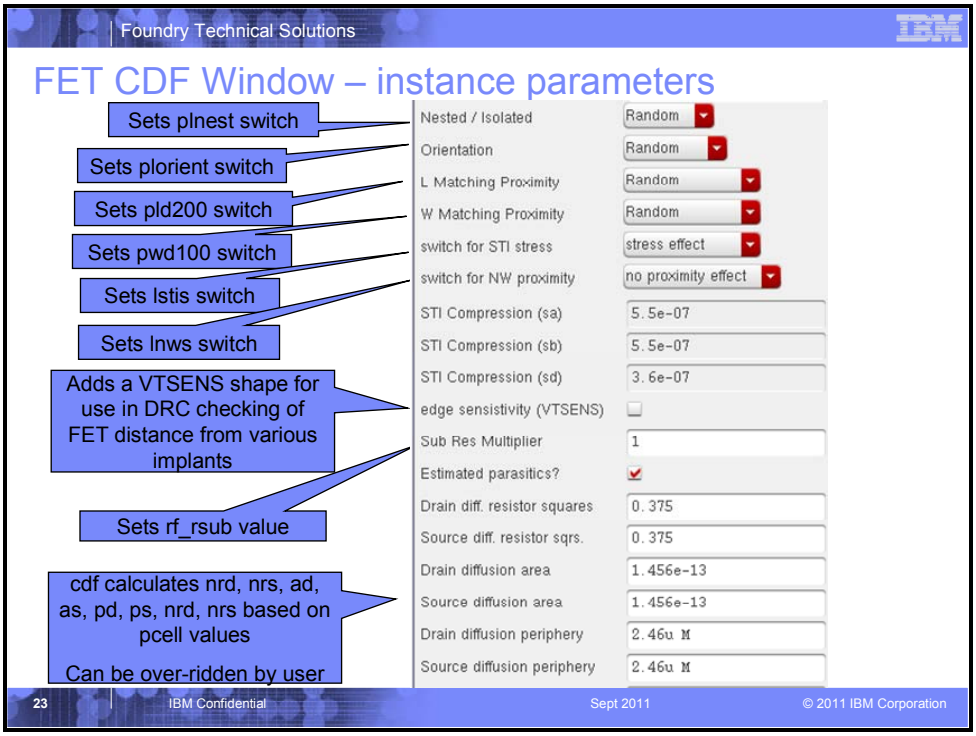
See § 4.3, "Device Length Variation" and Table 117, "Gate Length Variation for thin oxide FETs" in Design Manual

FET Mismatch – Geometric

ACV Global Switches and Instance Parameters

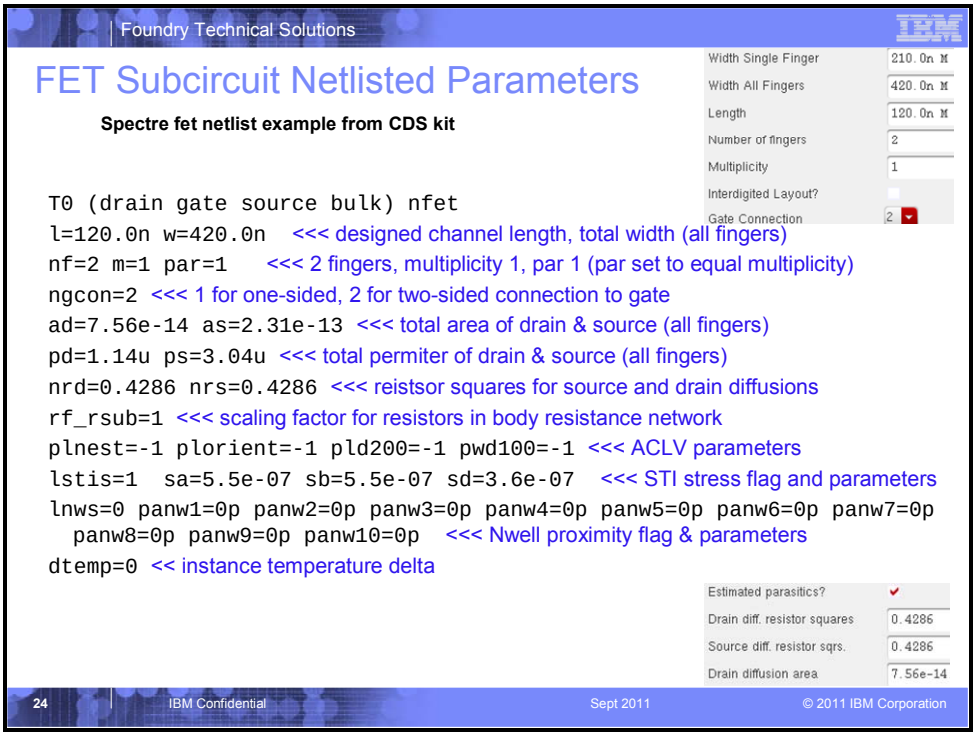
Global Switch	Effect and Related Instance Parameters
mc_global	Sets combination of global and matching parameters that will vary randomly in Monte Carlo
fet_dop_mis	Global control for dopant mismatch
fet_geo_mis	Global control for geometric mismatch (ACLV)
pc_nest	Global control for the systematic ACLV component -- Through Pitch
	Instance Parameter **plnest**: instance is nested, or isolated, or random
pc_orient	Global control for the systematic ACLV component – Orientation
	Instance Parameter **plorient**: instance is vertical, or horizontal, or random
pc_dist	Global control for the systematic ACLV component -- Distance
	Instance Parameter **pld200**: instance is within 200um, or not, or random
rx_dist	Global control for the systematic ACWV component -- Distance
	Instance Parameter **pwd100**: instance is within 100um, or not, or random

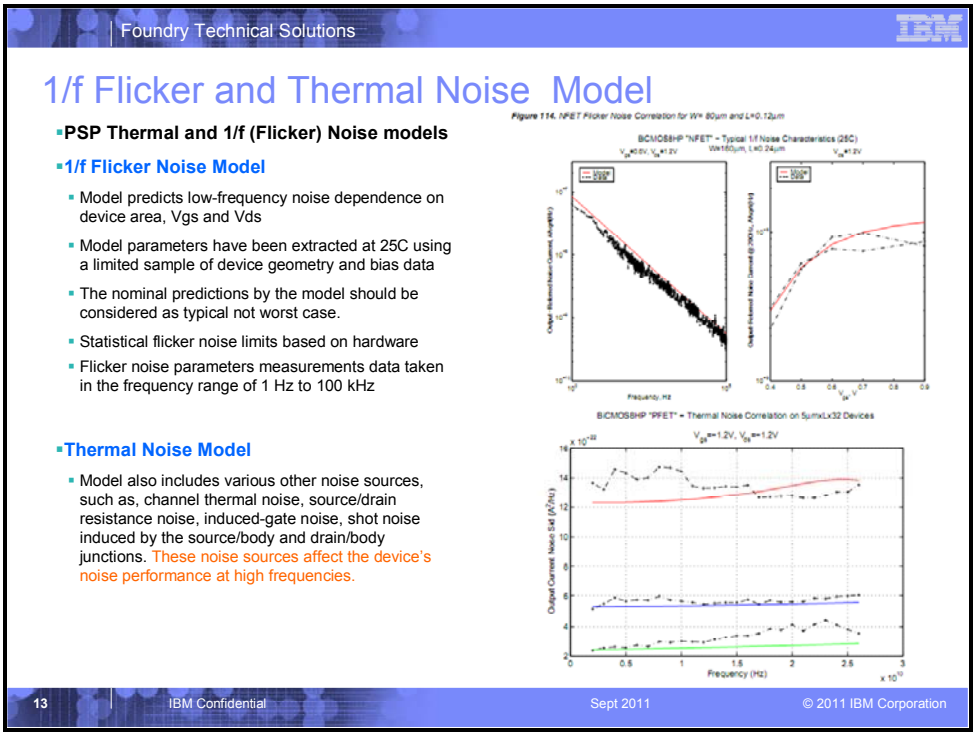
plnest, plorient, pld200, and pwd100 instance parameters are available through the FET CDF



FET CDF and Netlisted Parameters

The slide shown above shows a portion of the CDF window for the FET. Within this window there are several switches that can be set by the designer. Below, a netlist is shown, with the various inputs highlighted.

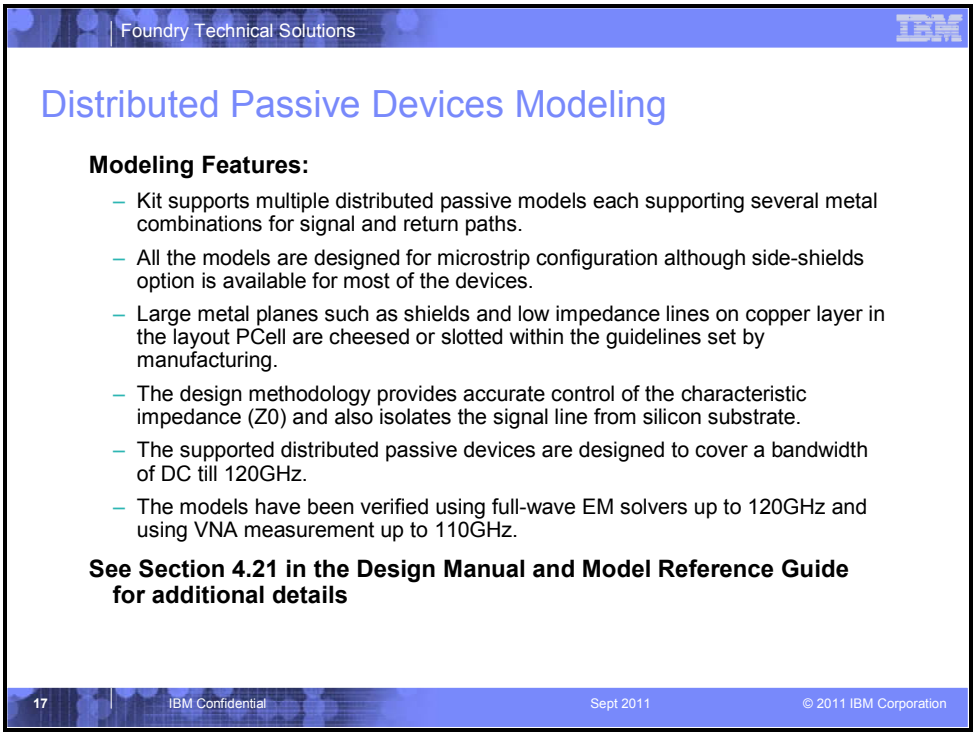




Flicker (1/f) and Thermal Noise

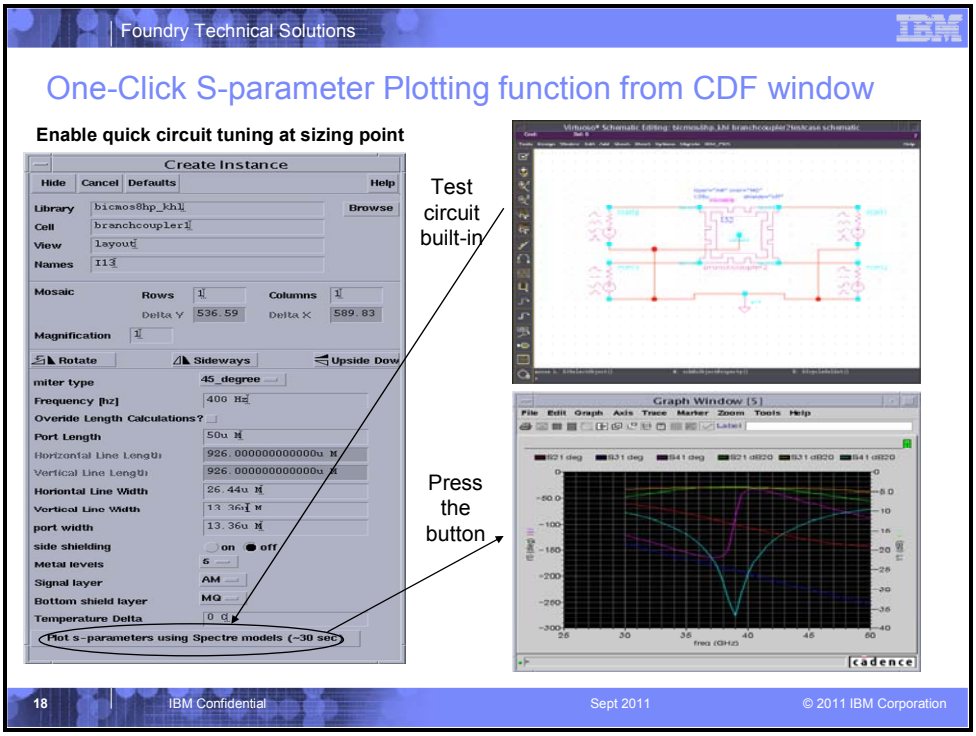
Low frequency 1/f (flicker) noise has been modeled using the PSP 1/f noise model. The model predicts low-frequency noise dependence on device area, Vgs and Vds. The model parameters have been extracted at 25 °C using a limited sample of device geometry and bias data.

The thermal noise model is also PSP. The model includes various other noise sources, such as: channel thermal noise, source/drain resistance noise, induced-gate noise, shot noise induced by the source/body and drain/body junctions. These noise sources affect the device's noise performance at high frequencies.



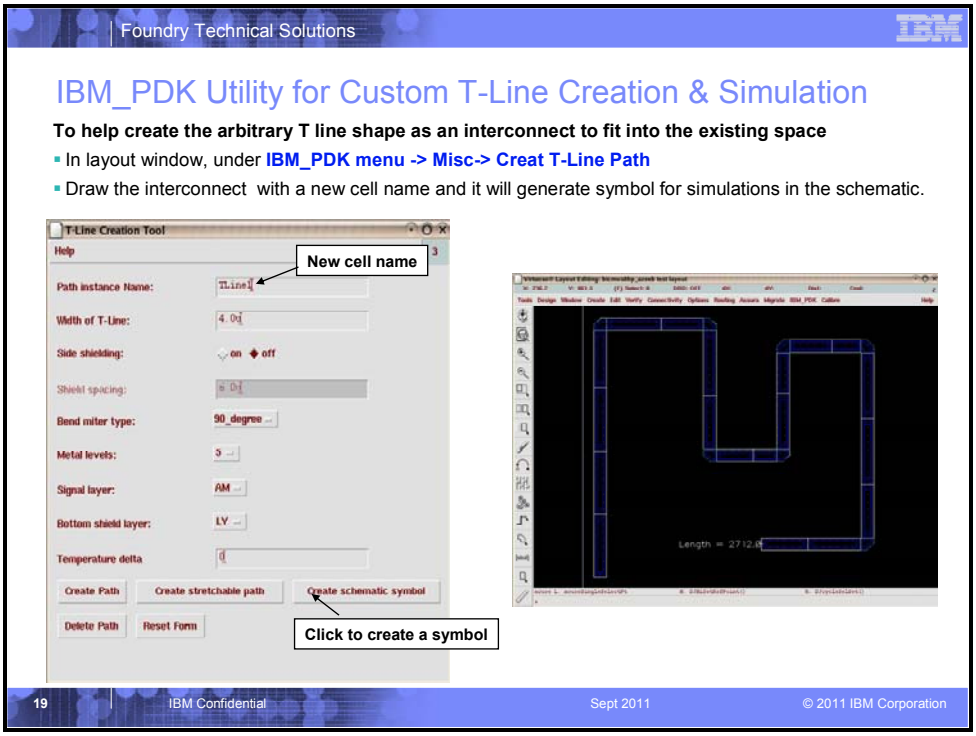
Distributed Passive Devices Modeling

IBM BiCMOS8HP PDK offers one of the most comprehensive distributed passive devices well suited for mmWave circuit designs. The heart of this offering is our proprietary accurate transmission line model, verified by the hardware from DC up to 110GHz.



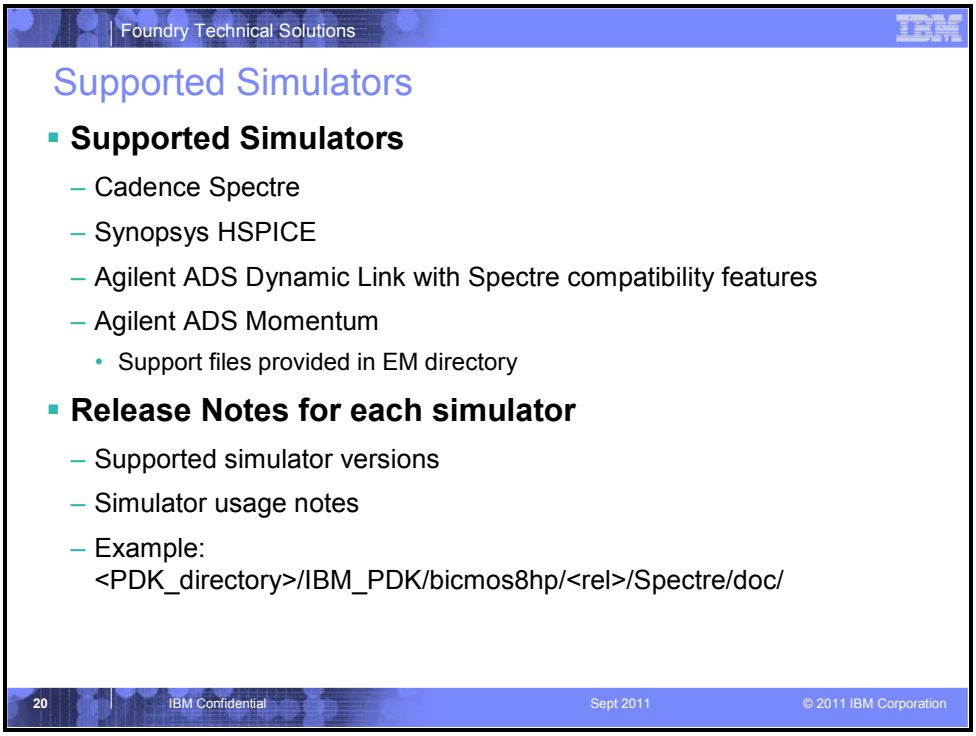
Built-in S-parameter Plot

For some of the hieratical distributed device such as branch coupler, IBM BiCMOS8HP PDK offers one unique simulation/plotting capability built in the CDF of the instance. This facilitates a quick feedback to better tune the circuit to the desired frequency during the sizing phase. The simulation may take about 30 seconds to complete.



Custom T-line Design and simulation

IBM BiCMOS8HP PDK allows the designers to make custom T-line with multiple bends and turns to achieve the desired the interconnect between the circuit blocks in the layout space allowed. Starting from the layout view, going to **IBM_PDK-> misc->Create T-line path** will allow the users to create a new cell to draw any T-line design. A symbol will be created for this new cell, thus to be used for the schematic simulation.



Supported Simulators

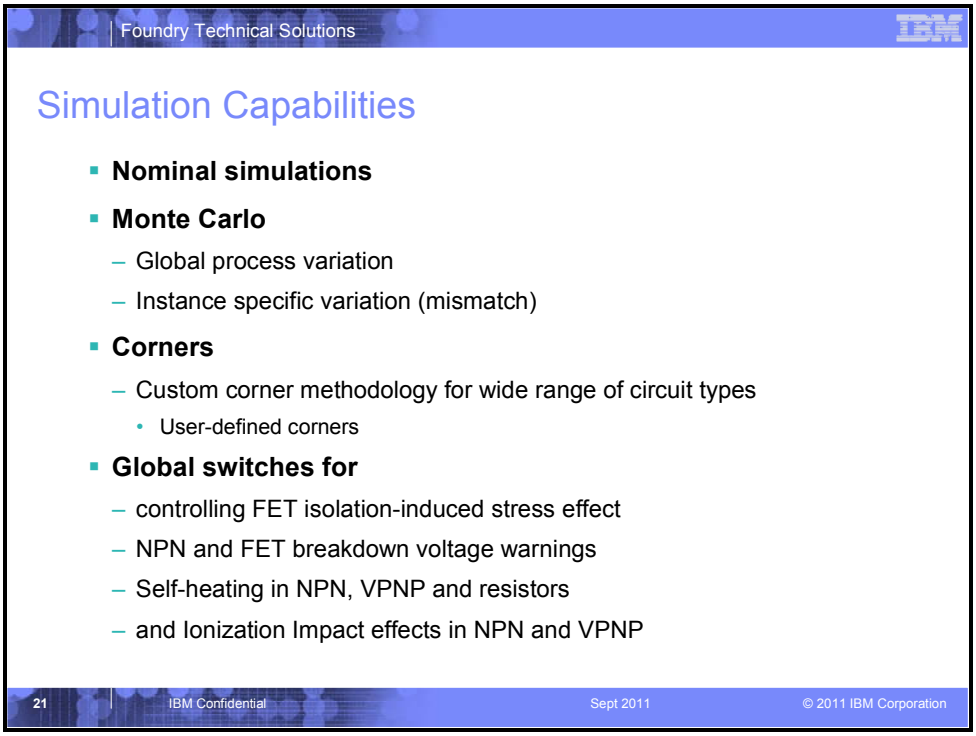
The IBM BiCMOS8HP design kit supports the Spectre (Cadence), ADS (Agilent), and HSPICE (Synopsys) simulation platforms

The HSPICE and Spectre simulators are run in the “direct” mode through the Cadence Analog Design Environment. The *direct* simulators bypass the cdsSpice socket and directly allow the simulator to run in an interactive mode, not launching a child process and a separate license check out. Spectre and HSPICE are only supported in the direct mode in BiCMOS8HP.

Simulators may be operated from within the Cadence Analog Design Environment or stand-alone using netlists generated from within Cadence.

DC operating points, model parameters, and currents displayed on the schematic form after simulation are controlled by the Component Description Format (CDF) specification defined for each device type.

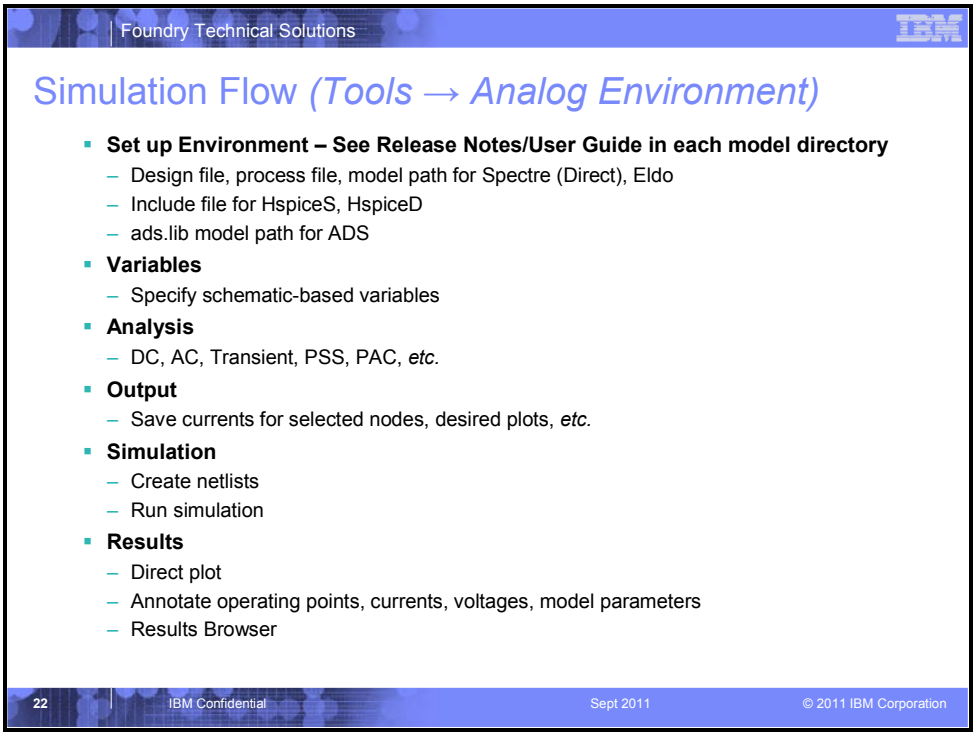
Please pay attentions to the proper tool versions used in the PDK testing, which is documented in the release notes for each tool, together with the known limitations. The updated tool versions will be used typically in conjunction with each major kit release.



Simulation Capabilities

The design kit supports simulation of nominal process conditions, statistical simulations using the Monte Carlo technique to explore the effects of process variation and/or mismatch between devices, and corner simulations that quickly evaluate the circuit response to specific process and operating conditions. In addition, twelve custom corner parameters are provided to give the designer quasi-independent control over different device groups. This provides the flexibility to accommodate circuits from straightforward digital logic gates to complex analog and RF functions.

The models have the ability to include complex effects that may not be important in all situations, and these may be controlled using a combination of local and global switches. For example, circuits operating at low power may not experience significant self-heating and that part of the model may be turned off to improve simulation time. This will be discussed in more detail later in the presentation.



Simulation Flow

The flow for a simulation is to set up the environment, set the analysis type, input any design variables, select specific outputs, run the simulation, then analyze the results. The simulation flow is described in detail in the User's Guide document which may be found in the directory path **/IBM_PDK/bicmos8hp/<rel>/cdslib/doc.**

Spectre Simulation Setup

include "/<user_directory>/design.scs"

include "/<LIBRARY_PATH>/allModels.scs“ section=XX

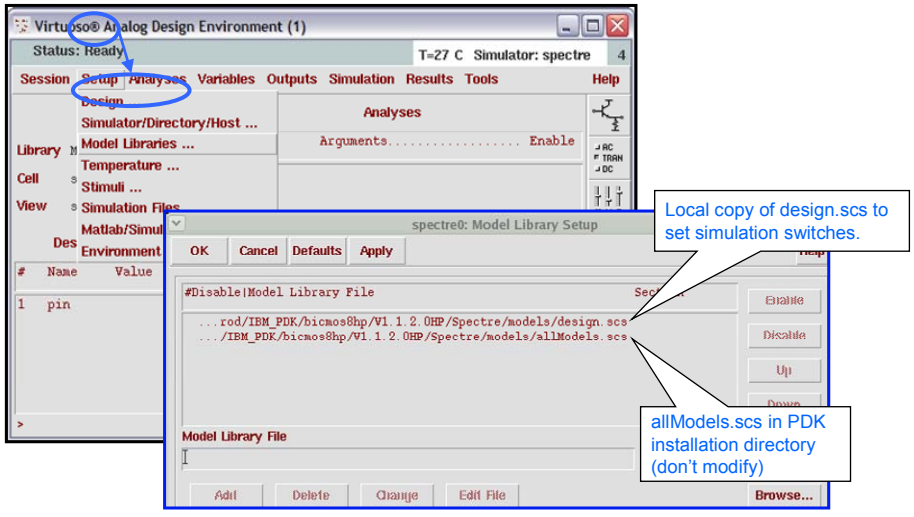
ORDER IS IMPORTANT!! design.scs must come before allModels.scs

- **design.scs**
  - Contains global switches, corner parameters and other user-defined settings for simulations.
  - Copy and edit switches as desired for simulations.
- **allModels.scs**
  - File to specify all model include statements to support nominal, custom process corner and Monte Carlo simulation analysis options.
  - Includes calls to other model files

Spectre Simulation Setup

First, the simulator should be set to “spectre” under **Simulator/Directory/Host**. The design.scs file is available for customizing the simulation settings. The two required files may be specified in the Analog Design Environment → Setup → Model Libraries as shown below. To employ these models, both “design.scs" and "process.scs" need to be invoked. A local copy of design.scs is useful for changing the simulation switch or setting up custom corners.

Analog Design Environment (ADE)



Foundry Technical Solutions

HSPICE Simulation Setup

Control files:

- **design.inc (global switches and corner parameters)**
  - Copy to local directory and customize as desired
  - Change include statement to point to local file

Include File:

/IBM_PDK/bicmos8hp/<rel>/HSPICE/models/allModels.inc XX

- File to specify all model include statements to support nominal, custom process corner and Monte Carlo simulation analysis options
- Includes skew.file (skew parameters, process distributions, corner parameters)
- Includes models.inc separate device model files

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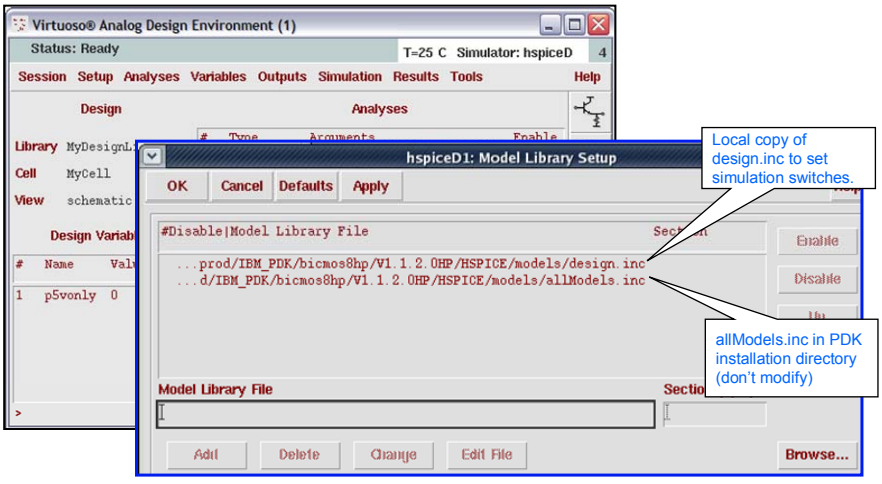
HSPICE Simulation Setup

The HSPICE include file contains include statements to incorporate other files into the simulation run. The design kit provides sample files **hspice_example.include** and **hspice_example.param** that can serve as starting points for user customization.

Foundry Technical Solutions

HSPICE Required Files

- **Analog Environment set-up for HSPICE Direct required file**



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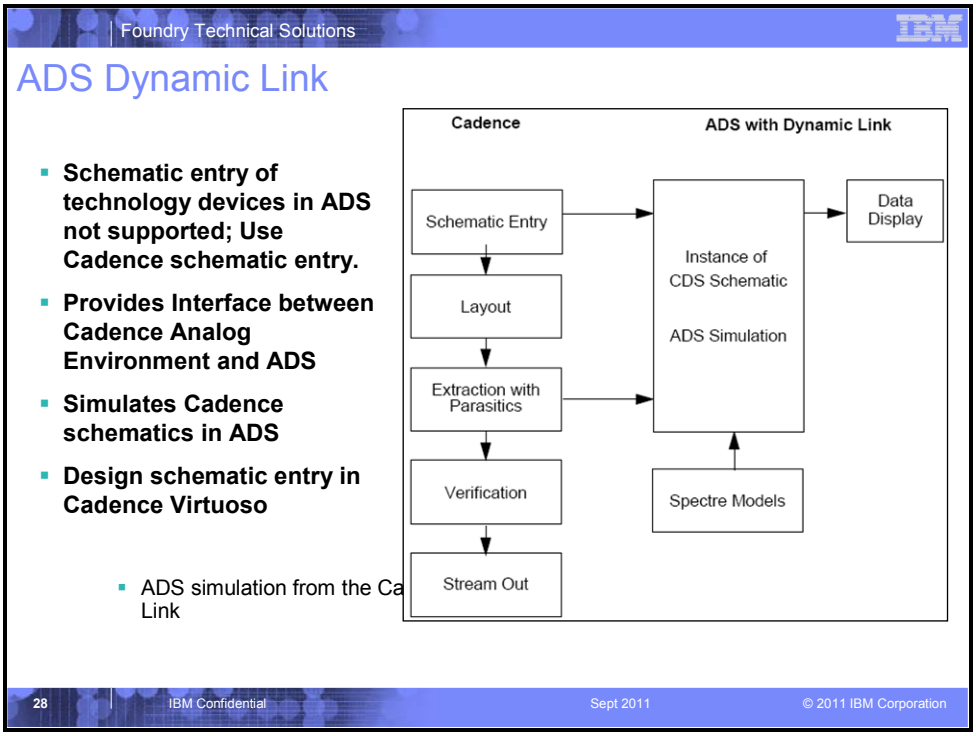


ADS Dynamic Link

ADS simulations are run from the Cadence Analog Environment through the RFIC Dynamic Link (also known as Integrated Design Format – IDF). ADS support files are located in the ADS directory /**IBM_PDK/bicmos8hp/<rel>/ADS**

The interface between Cadence and ADS is controlled by Agilent "RFIC Dynamic Link" software. Design schematics are entered in the Cadence Virtuoso schematic editor. Simulation is performed in ADS.

The Dynamic Link tool presents an ADS user interface. The Cadence design schematic is instantiated in an ADS simulation schematic. Sources, passives (DC blocks, RF chokes), and any other ADS components are added and the simulation is performed in ADS.

ADS Dynamic Link Simulation Setup

- **Set user's environment variables as specified by Agilent.**
  - See "Customizing Environment Variables" in ADS Documentation.
    - For Korn shell, include in user's ~/.profile:

```
EXPORT HPEESOF_DIR = <ADS_intstall_dir>
EXPORT PATH=$PATH:$HPEESOF_DIR/bin
```

    - For C shell, include in user's ~/.cshrc:

```
setenv HPEESOF_DIR <ADS_intstall_dir>
setenv PATH $PATH:$HPEESOF_DIR/bin
```

- **The Dynamic Link kit is loaded from the user's ads.lib file. Copy ads.lib from <pdk_path>/IBM_PDK/bicmos8hp/<rel>/ADS/design_kit/ads.lib to user's $HOME/hpeesof/design_kit directory.**
  - ads.lib

```
BICMOS8HP_IDF | path_to_design_kit | de/ael/bicmos8hp_idf_boot | V1.2.1.0HP
;BICMOS8HP_IDF | /<pdk_path>/IBM_PDK/bicmos8hp/V1.2.1.0HP/ADS |
  de/ael/bicmos8hp_idf_boot | V1.2.1.0HP
```

- **Add this line to user's .cdsinit:**

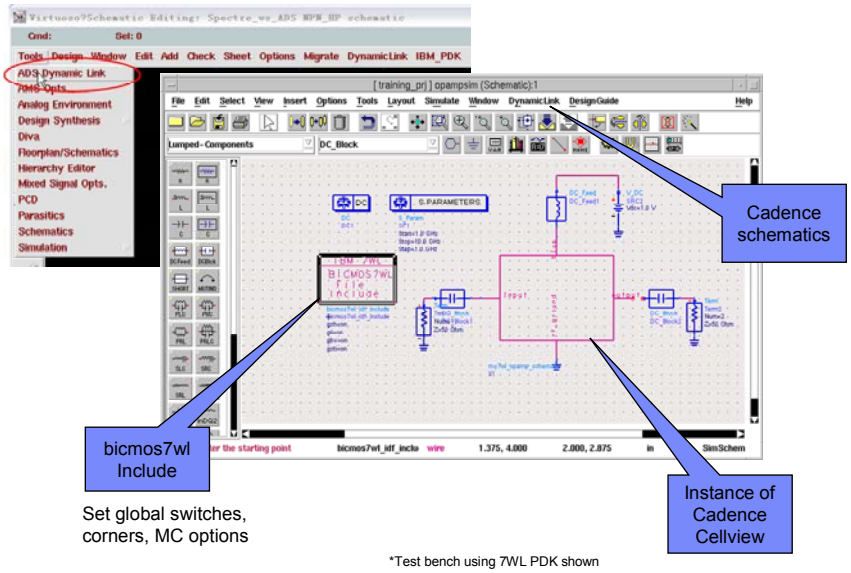
```
load strcat(getShellEnvVar("HPEESOF_DIR") "/idf/config/.cdsinit")
```


ADS Dynamic Link Simulation Setup

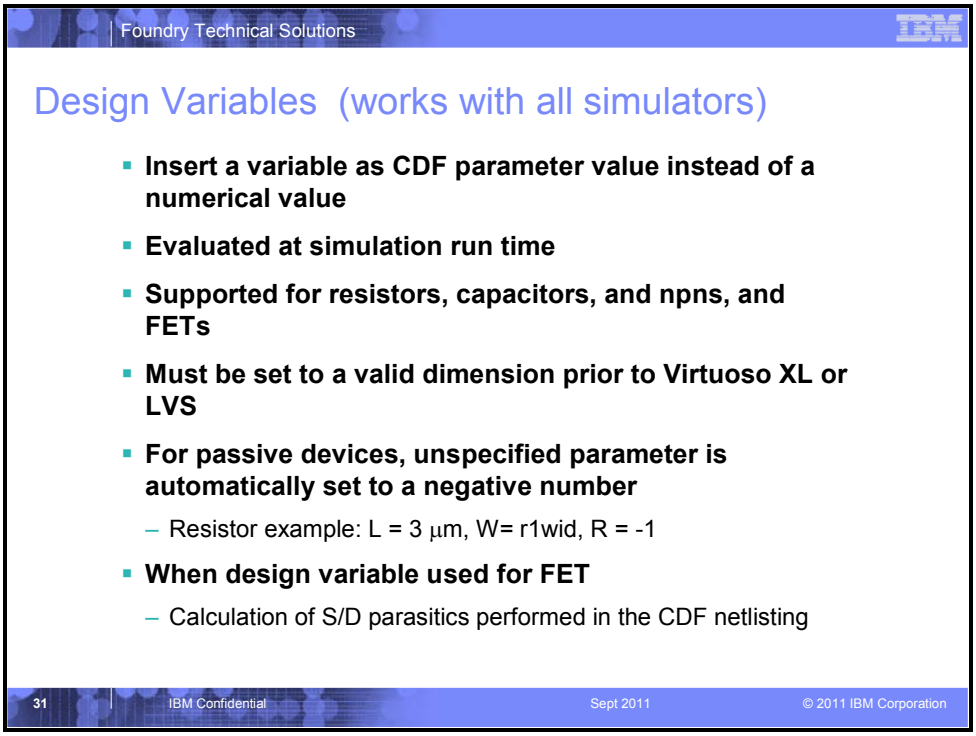
Select the Dynamic Link mode by choosing **Tools → ADS Dynamic Link** from the Composer schematic window. An ADS session will be started.

Cadence schematics are instantiated from the "Dynamic Link" menu in the ADS schematic window. The BiCMOS8HP File Include component provides the simulation information from the bicmos8hp library including global switch and corner settings, Monte Carlo options, and models.

ADS Dynamic Link Test Bench Example*



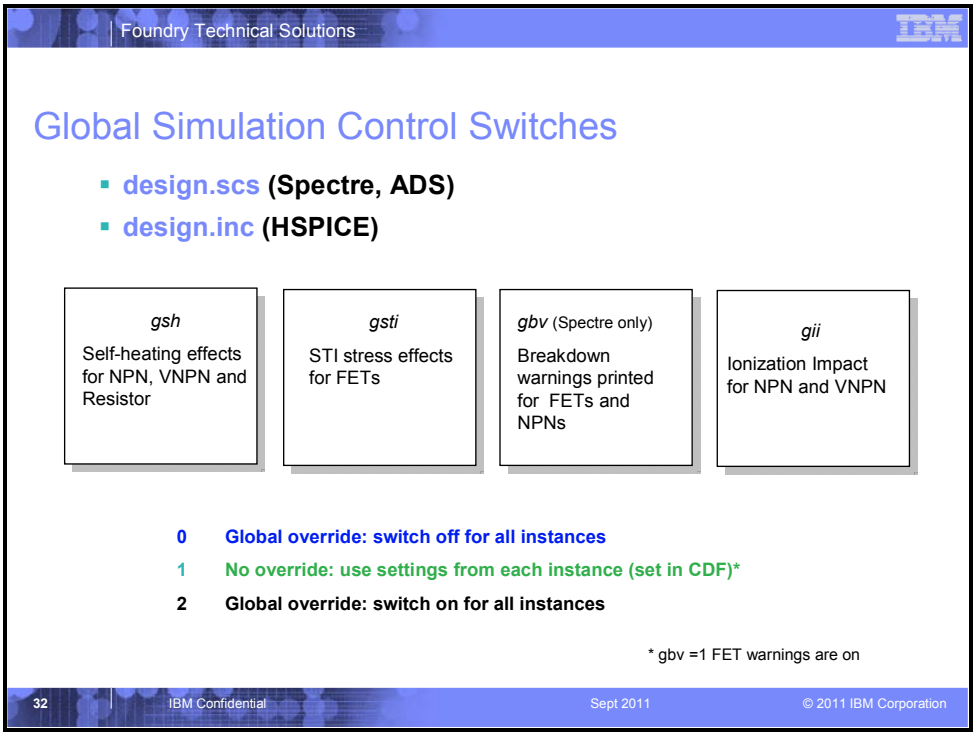
*Test bench using 7WL PDK shown



Design Variables

Design variables are useful for sweeping devices size parameters during simulation.

Resistors and capacitors may be specified “by geometry”, or by the resistance or capacitance value and one of the physical dimensions. Three parameters are passed to the model in the netlist: length, width, and the component values (resistance or capacitance). The CDF normally provides all three. When a design variable is used for the component value, the CDF sets the unspecified dimension to a negative number. Since one of the dimensions is unavailable, the model will use the component value and the one specified dimension to calculate the missing dimension.



Global Simulation Control Switches

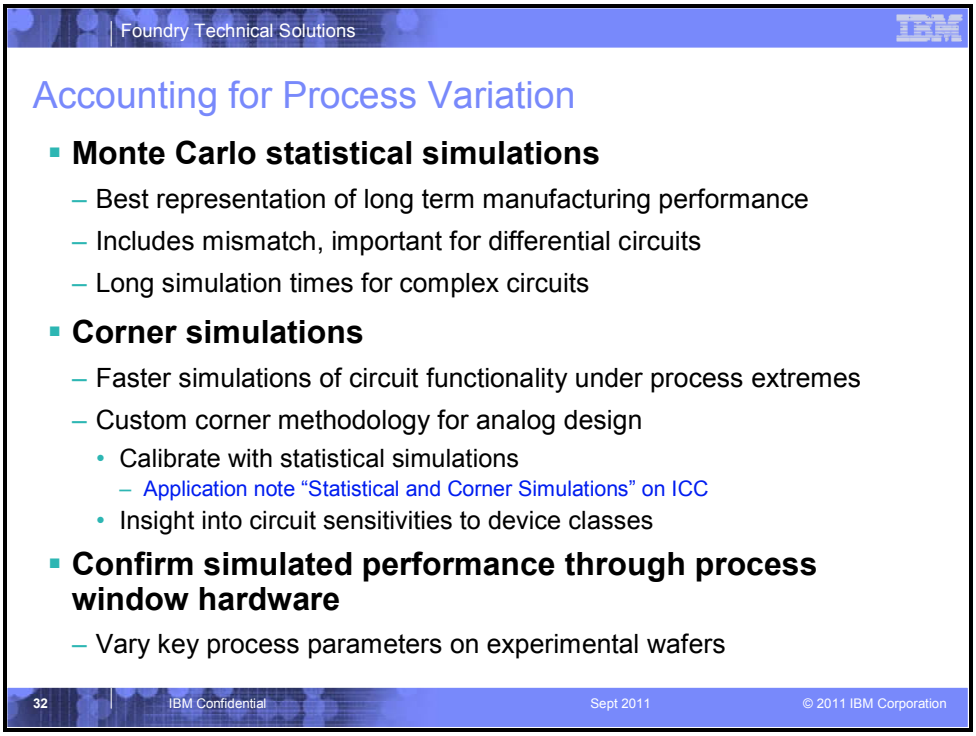
The design kit provides global control switches to customize simulator behavior.

The RR Poly and K1 resistor models include self-heating effects. The global switch parameter gsh controls whether self-heating is calculated (gsh=2, default) or ignored (gsh=0) in the simulation.

HSPICE and Spectre thin oxide regular nfet and nfettw models contain calculations for the STI stress effect. These calculations are controlled by the global switch parameter “gsti.”

For Spectre simulations (not supported in HSPICE), the FET models include operating region warning control parameters. The global switch “gbv” can be set to turn these checks on or off to print or suppress the oxide breakdown voltage warning messages for FETs.

Setting the global switch to “2” turns the effect on for all devices. The setting of “0” turns the effect off for all devices. Setting the variable to “1” defers to a corresponding parameter for each instance, the name of which is the global parameter minus the “g”. For example, gbv=1 defers to the instance parameter “bv.”



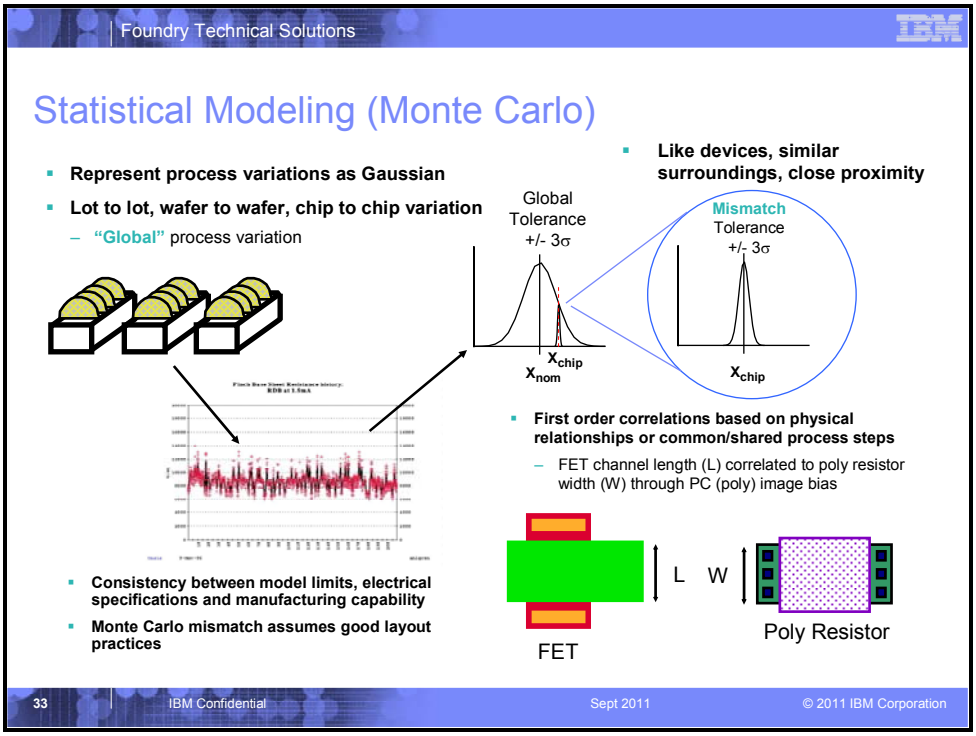
Accounting for Process Variation

Designers must assure that the circuit will function over the full range of expected process variation during manufacturing as well as over the allowed temperature and voltage range.

Monte Carlo statistical simulations provide the best approximation of the circuit performance variation over the manufacturing process window. Multiple simulations are run to randomly vary process and hence device parameters within the expected distributions. Statistical simulations can also explore the effects of mismatch between like devices within a chip. Mismatch simulation is especially important for differential designs where device tracking is critical. Although statistical analysis is the preferred method for examining circuit sensitivity to process variations, it is not always feasible for large designs or complex analyses due to the many runs required for statistically significant results.

Corner simulations provide an expedient way to assess circuit functionality at process extremes using only a few simulation runs. Mismatch effects are not included. The success of this technique is very dependent on choosing a complete set of corner cases that probe the performance extremes. It is important to calibrate the corner cases to the 3-sigma variation predicted by statistical simulations. IBM provides an application note describing a technique for doing this calibration. See "Statistical and Corner Simulations," available on IBM Customer Connect (ICC) www.ibm.com/technologyconnect. Corners are organized among device classes such that a sensitivity analysis can provide insight into how particular circuit types are influenced by certain classes of devices.

It is highly desirable to verify the process window by running wafers where key process parameters have been deliberately skewed from their nominal values. This provides a final check to insure that the part is suitable for volume manufacturing.



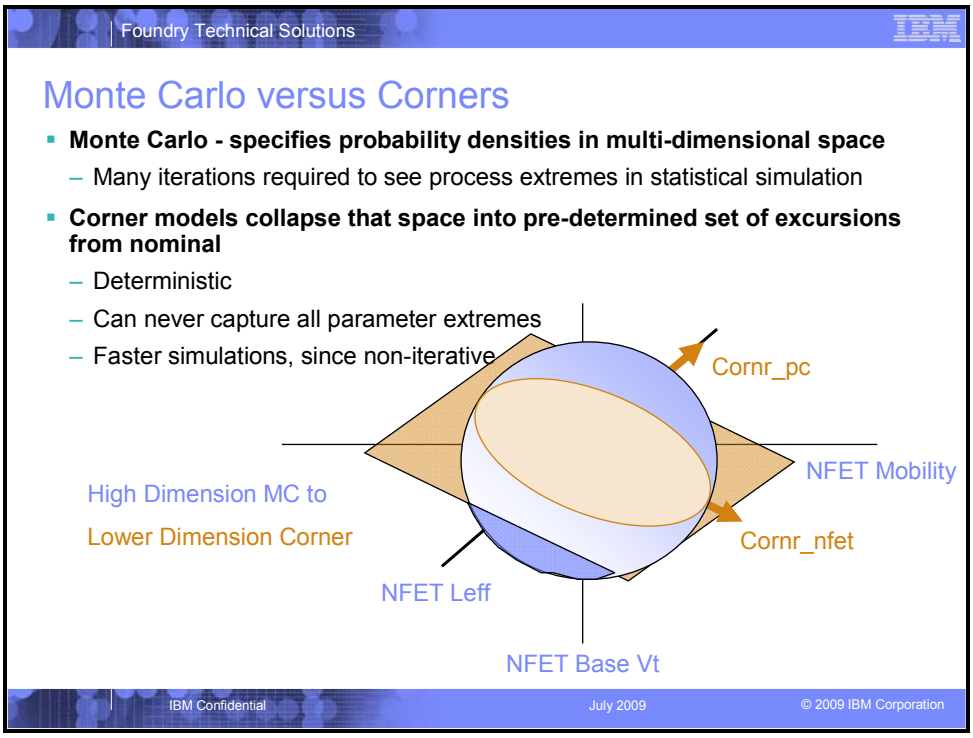
Statistical Modeling (Monte Carlo)

Parameters used by IBM device models are provided with statistical distributions that represent long-term process variation during manufacturing. Separate distributions describe global and mismatch variations. The global variations apply to device performance over the total manufacturing process window. Mismatch distributions, typically much smaller, generate different device parameters for each device instance within in a single Monte Carlo iteration. Mismatch distributions apply to devices in close proximity following good layout practices (*e.g.* same orientation, symmetric wiring). Mismatch values as defined are "typical", not worst case, so as not to be too pessimistic for practical use in design.

The mismatch variation assumes that the designer has placed devices for which matching is critical in close proximity on the chip. Results will be optimistic for devices far from one another.

As a fundamental process parameter is varied it will influence all devices that physically depend on that parameter. For example, a change in poly image bias will affect not only FET channel length, but also polysilicon resistors and FET threshold voltage. Application of independent distributions to physical parameters assures that proper correlations between various devices are preserved through the use of those parameters in the model equations.

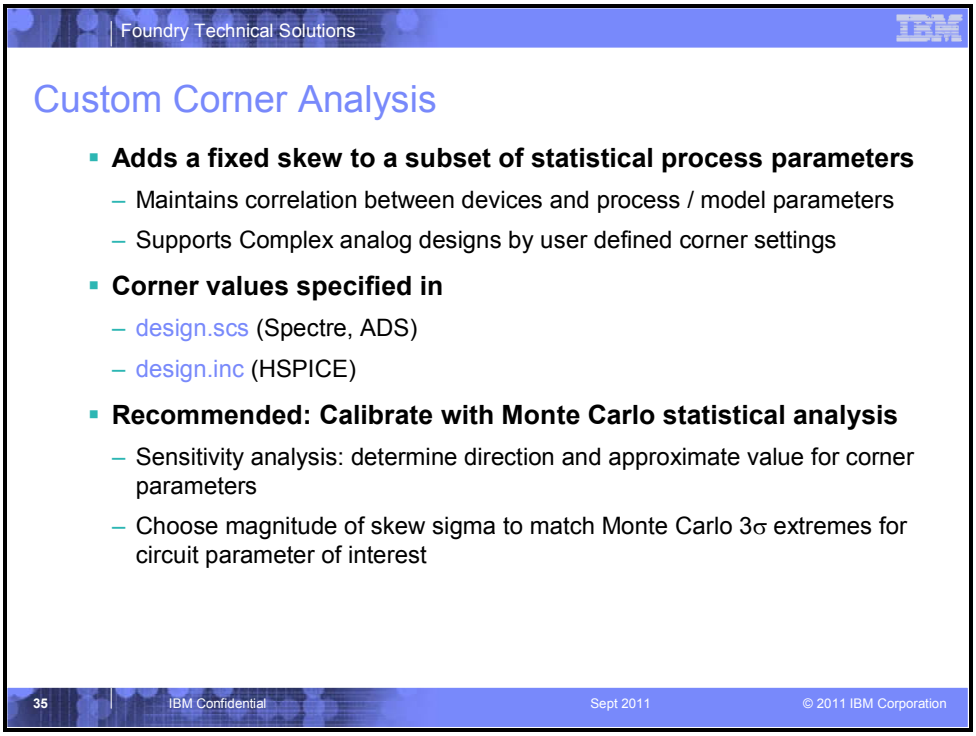
Parameter statistical variation is chosen to insure that the three-sigma Monte Carlo extremes of key device characteristics will be consistent with electrical specifications and with manufacturing capability.



Monte Carlo versus Corners

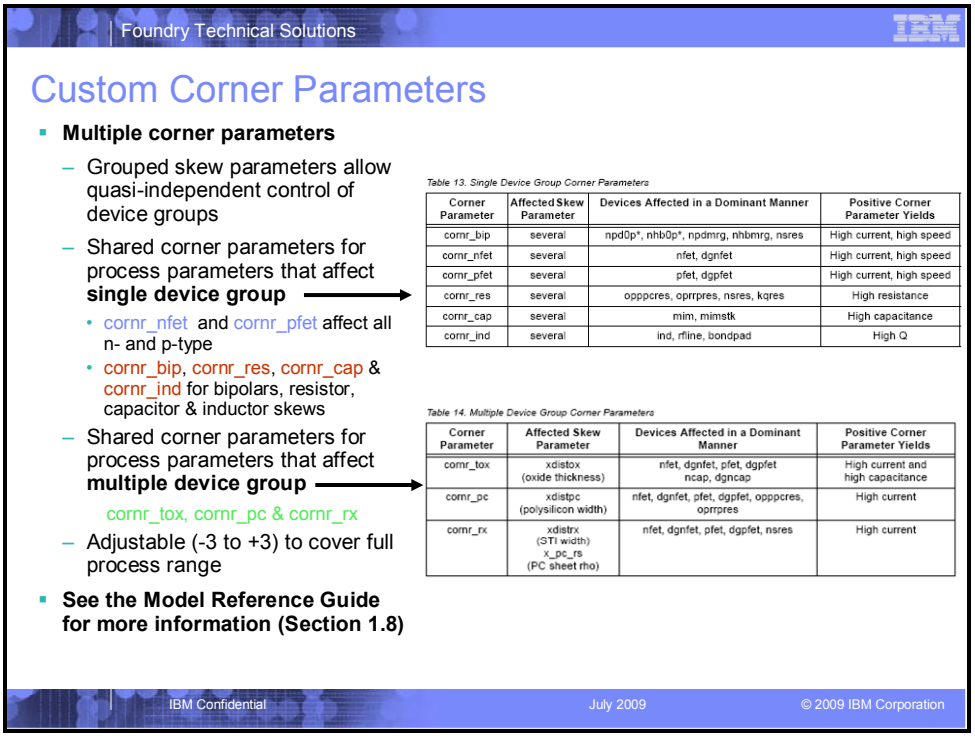
In order to see the effect of multiple process extremes, a Monte Carlo statistical simulation requires many iterations. Corner models collapse the multi-dimensional space into a pre-determined set of excursions from the nominal process. Corner simulations allow for much faster simulations, since they are pre-defined and not statistically varied, but can never capture all possible combinations of process extremes.

The custom corners also provide the benefits for designers to check the circuit sensitivity to certain device families.



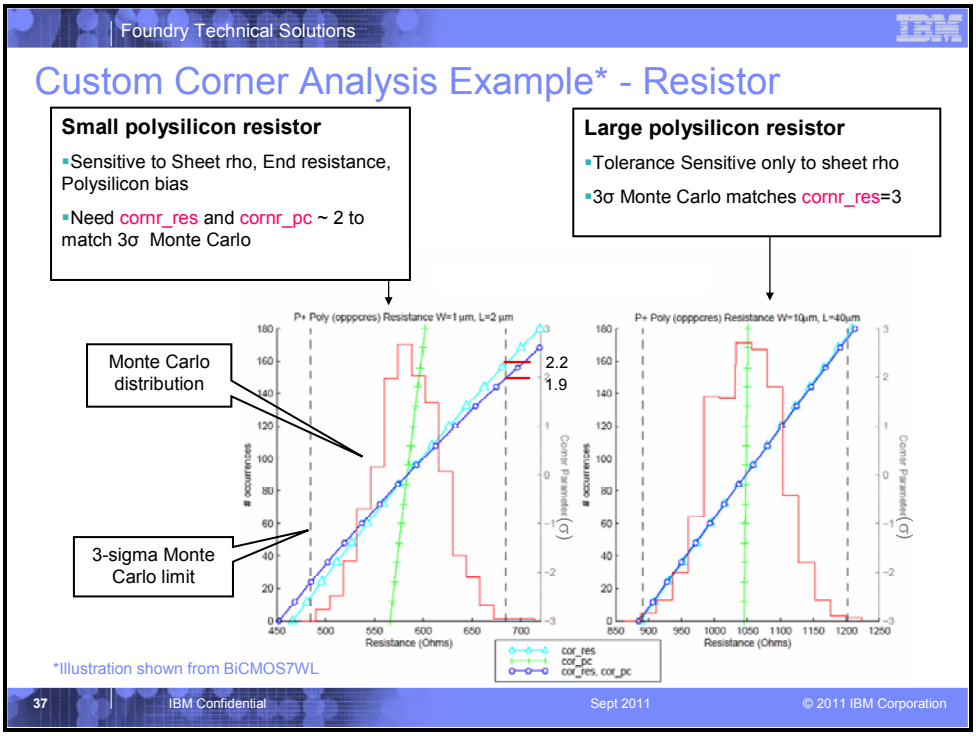
Custom Corner Analysis

The custom corner methodology supports multiple corner parameters that vary different device types as independently as possible. This type of corner simulation approach allows designers to determine if a circuit is more sensitive to a particular device type, to skew different device types in different directions, and construct best case and worst case corner files. The proper direction and magnitude for a corner setting for a best case or worst case analysis depends on the class of circuit as well as the specific performance under consideration, such as, speed, power, noise , the device sizes, and bias conditions. It is highly recommended that best and worst case combinations be calibrated to the 3-sigma variation in the circuit performance using a full Monte Carlo statistical analysis. The corner parameters must be set appropriately to match the excursions predicted by Monte Carlo simulations.



Custom Corner Parameters

The custom corners group the model parameters by device type to provide quasi-independent control. Process parameters that affect multiple device types (i.e. gate oxide thickness, polysilicon bias and active area bias) have unique corner switches. A single model parameter may be affected by multiple corner switches. For example the FET threshold voltage will be affected by cornr_pc and cornr_tox.



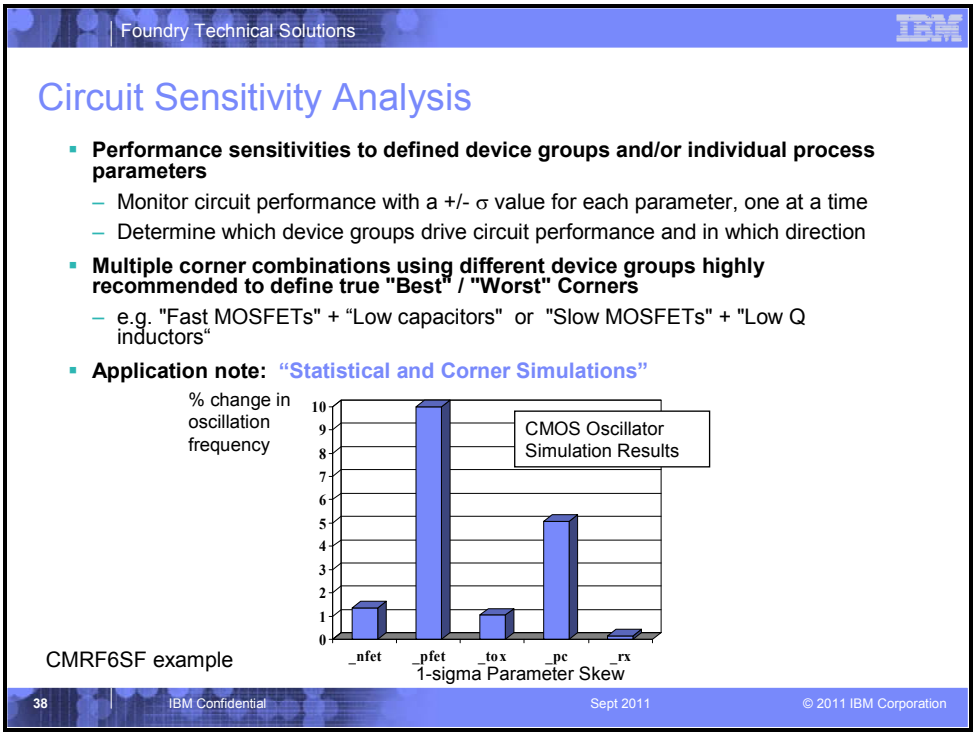
Corner Analysis Example - Resistor

When a component value is predominantly dependent on only one process parameter, setting that parameter to plus or minus three-sigma will be representative of expected process variation. If the resistor value depends on multiple process parameters, then setting all of them to three-sigma will create overly pessimistic situation. The custom corner parameters contain multiple process parameters, so they will typically not be set to 3σ.

The concept may be illustrated by comparing the variation in resistance determined through Monte Carlo statistical modeling and through corner analysis for two different sizes of polysilicon resistors. The Monte Carlo results are shown as histograms with the left y-axis denoting the frequency of occurrence of the resistance value plotted on the x-axis. The right y-axis reflects the corner parameter setting which results in the x-axis value. The corner parameters to be varied are *cornr_pc* (polysilicon line width) and *cornr_res* (sheet resistance and resistor end resistance).

Consider a long, wide resistor represented by the plot on the right. This device will not be sensitive to resistor end effects or variation in polysilicon line width. Changing the *cornr_res* parameter only affects the device through one process parameter (sheet resistance); therefore using *cornr_res* at the ± 3σ values accurately reflects the expected resistance variation predicted by Monte Carlo. The resistance is essentially independent of *cornr_pc*.

The plot on the left shows a small resistor for which end resistance and poly variation are significant. When the *cornr_res* parameter is adjusted, two process parameters (end resistance and sheet resistance) are changed. Now, the *cornr_res* provides three-sigma resistance when set to 2.2σ. If another process parameter is added through *cornr_pc*, the three-sigma resistance is attained when both corner parameters are at 1.9σ.



Circuit Sensitivity Analysis

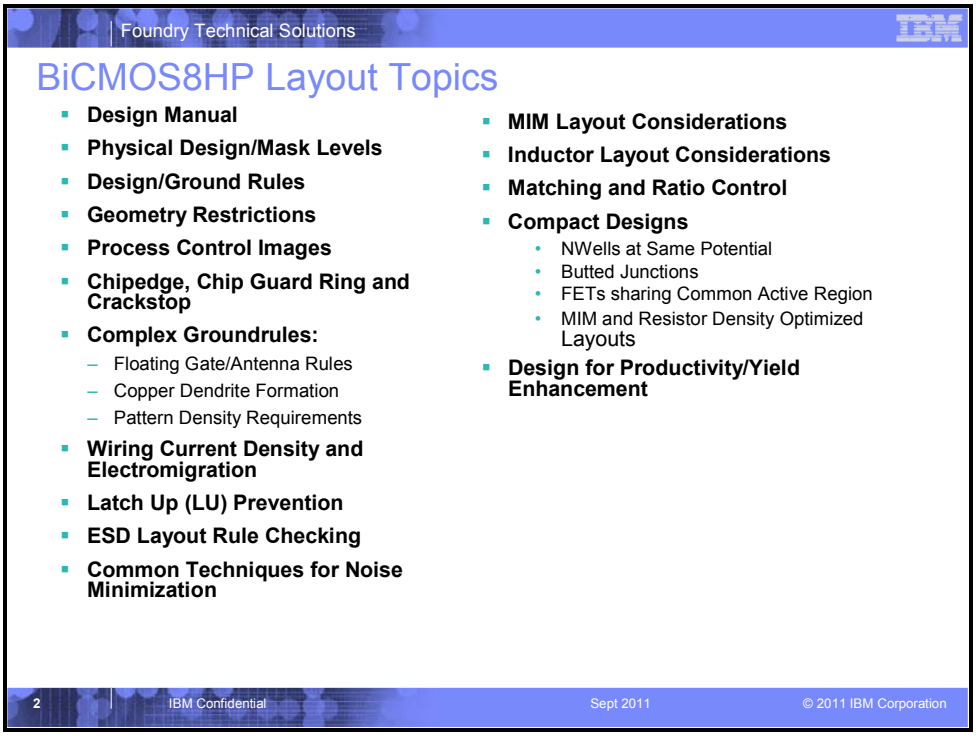
The first step in defining corner parameters for a particular circuit is to determine the signs of the shifts that result in negative and positive shifts for the circuit performance relative to its nominal value. Nominal simulation is run by setting all of the corner parameters to zero. Then, one at a time, each corner parameter is set to a non-zero value (such as +1 or -1, giving 1-sigma variations in the affected skew parameters) while the other corner parameters are zero. The simulation results are compared against the nominal simulation run. The total number of simulation runs is twice the number of corner parameters examined. This will determine what device groups drive circuit performance and in which direction. The corner vector representing best or worst cases is assembled using the insight gained by this exercise.

This chart shows the results of CMOS oscillator frequency arising from a 1-sigma shift in nfet, pfet, tox, pc, and rx corner parameters. Note that the oscillator displays pronounced sensitivity to the PFET device group and the pc corner parameter, while being less influenced by tox and rx corners. For some circuit characteristics, worst case may be represented by corner parameters; for example, by fast NFETs and low capacitors.

A full procedure for generating corner files is discussed in the application note "Statistical and Corner Simulations", posted IBM Customer Connect (ICC) website.

Layout Topics

This training module covers the BiCMOS8HP Design Manual Overview and a series of layout topics including the ground rules that may not be obvious, such as, antenna rules and pattern density considerations. We describe floating gate, copper dendrite, the necessity of PCI marks, the techniques for noise minimization, proper use of substrate contacts and latchup prevention, proper layout techniques to achieve optimum device matching, and prevention of electromigration failure and unsatisfactory voltage drops through adequate sizing of conductors. At the end we also include additional layout techniques for compact layouts.


Foundry Technical Solutions
BiCMOS8HP Layout Topics
Design Manual
Physical Design/Mask Levels
Design/Ground Rules
Geometry Restrictions
Process Control Images
Chipedge, Chip Guard Ring and Crackstop
Complex Groundrules:
Floating Gate/Antenna Rules
Copper Dendrite Formation
Pattern Density Requirements
Wiring Current Density and Electromigration
Latch Up (LU) Prevention
ESD Layout Rule Checking
Common Techniques for Noise Minimization
MIM Layout Considerations
Inductor Layout Considerations
Matching and Ratio Control
Compact Designs
NWells at Same Potential
Butted Junctions
FETs sharing Common Active Region
MIM and Resistor Density Optimized Layouts
Design for Productivity/Yield Enhancement
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Sept 2011
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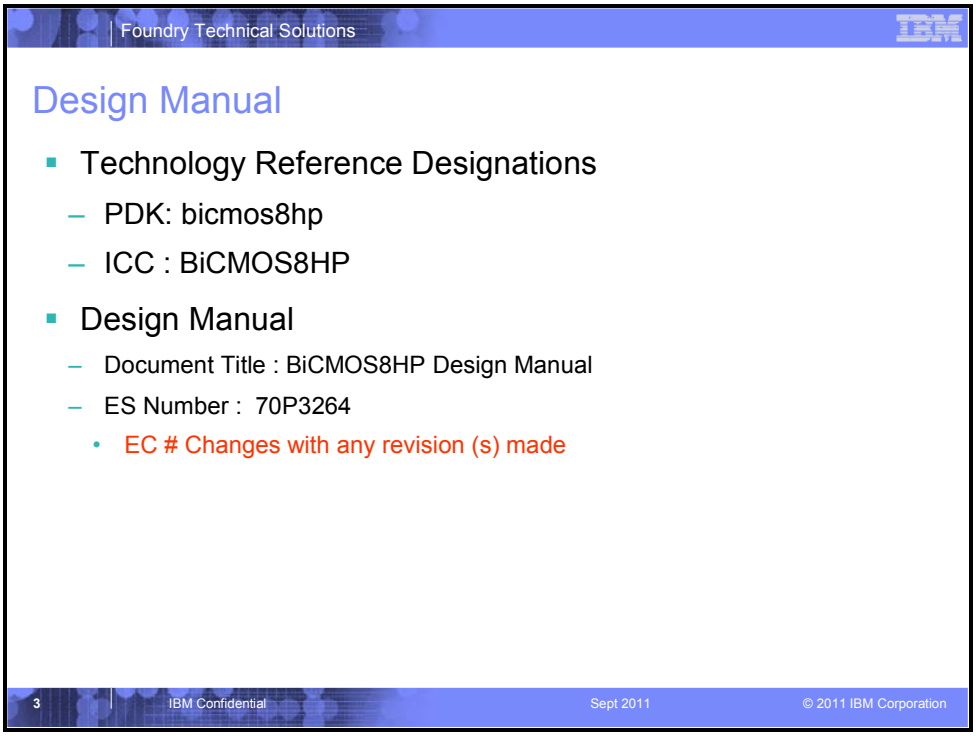
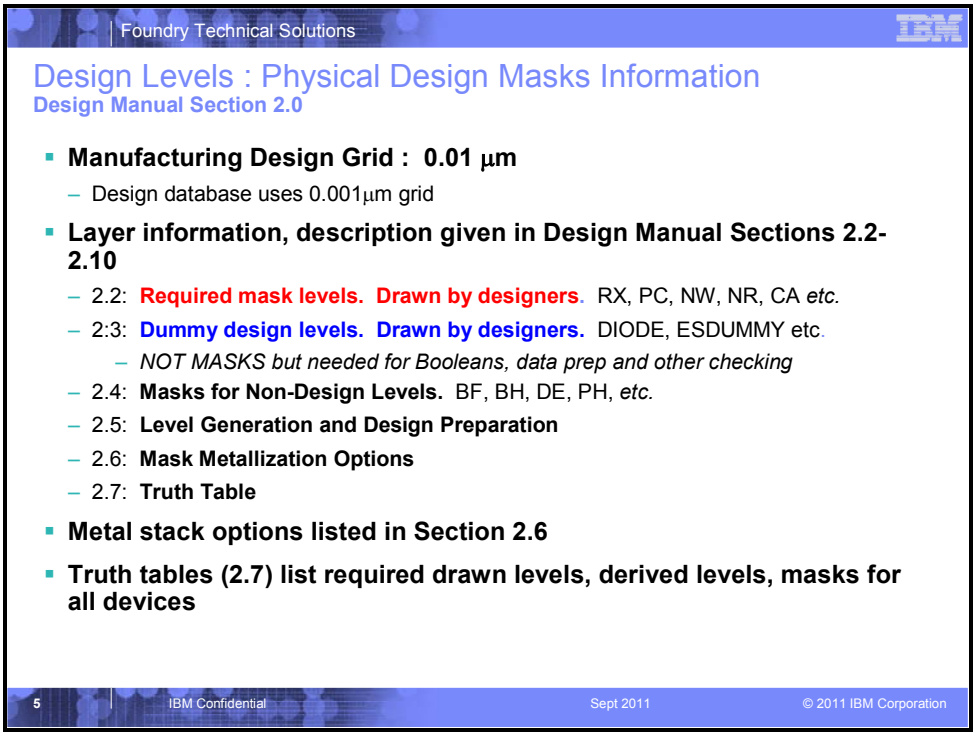


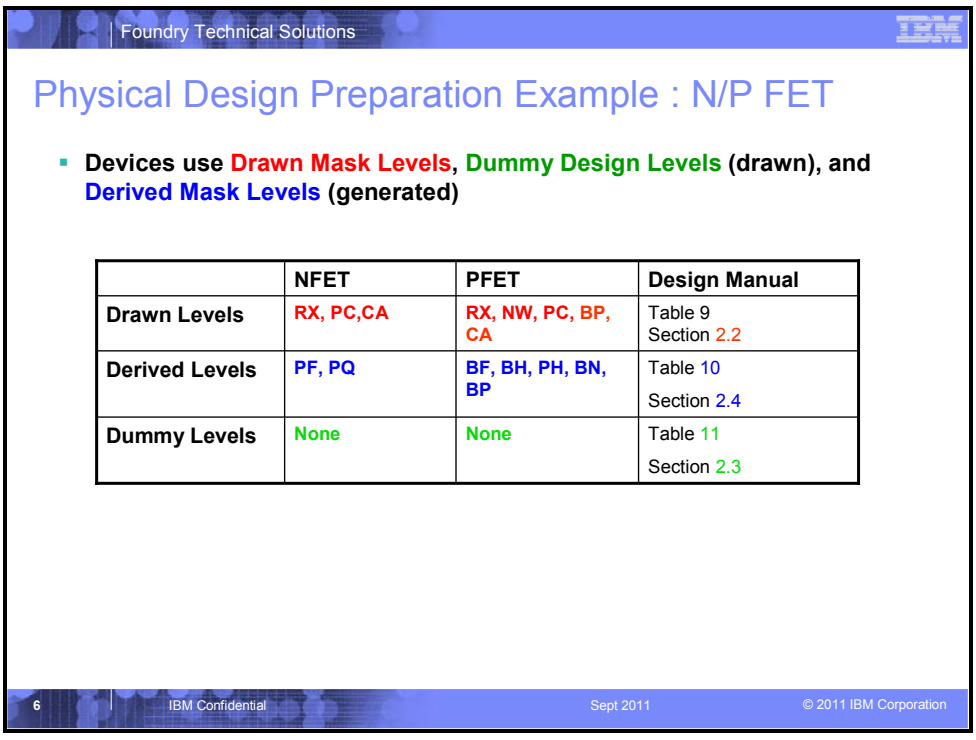
BiCMOS8HP Design Manual

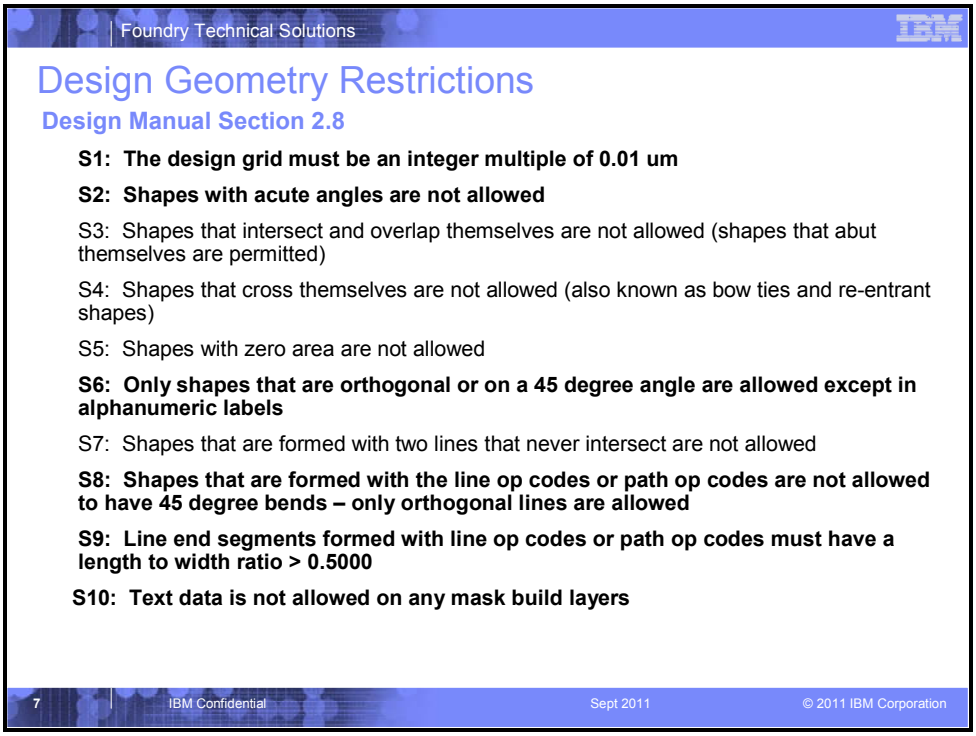
The contents in this presentation mostly can be found in this design manual. The reference document number (ES 70P3264) is used for document control purpose. **Please note that the EC# changes with any revision changes maid to the design manual.**



Physical Design (Masks)

Section 2 in the design manual gives the necessary details for understanding masks required for physical designs including the available metal stack options. Mask levels in Section 2.2 and 2.3 are required drawn design levels by the designers. Mask levels described in Section 2.4 are called 'Derived Levels". These masks are build masks derived from Boolean operations. Designers do not draw them. A typical example is shown on the slide below with all design levels and associated masks required for regular N/P FETs (nfet, pfet).





Design Geometry Restrictions

Section 2.8 and 2.9 of the design manual includes the design geometry restrictions listed in the slide above and important design guidelines. Some of these geometries are prevented within the Cadence layout editor itself.

The most common errors are shown in bold in the slide above. Rule S1 states that the design grid must be an integer multiple of 0.01um to avoid off-grid errors. Care needs to be taken with paths: Ortho-normal path widths should be an integer multiple of 0.01um. Otherwise, off-grid errors will result.

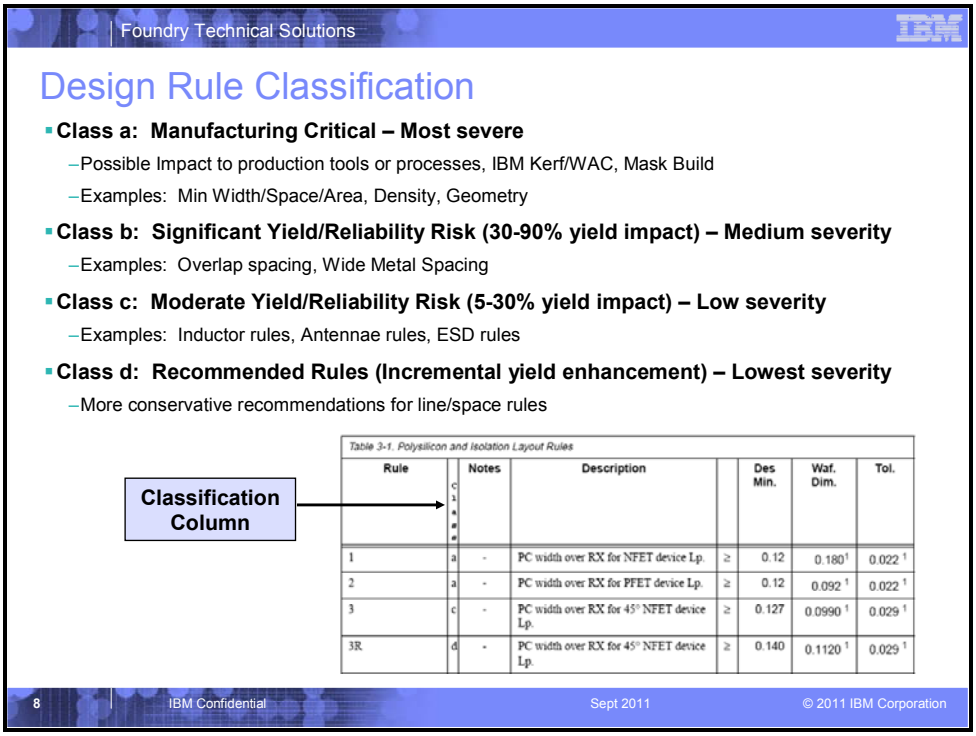
Shapes with acute angles are not allowed (S2), including shapes for company logos. Only orthogonal or 45 degree angle shapes are allowed. Design rule correct alphanumeric shapes are included in the *bicmos8hp* library (alpha12, alpha20, alpha25 and alpha40 cells, where the numeric suffix indicates the height in microns of the shapes).

Paths are not allowed on 45 degrees (S8); the Cadence “Convert to polygon” layout utility may be used to convert paths to polygons. This may however result in off-grid errors that need correction, depending on the original path width.

When terminating a path, the Cadence layout editor will issue a warning pop-up box for S9 errors (“First or last segment of created path should be not less than half the path width”).

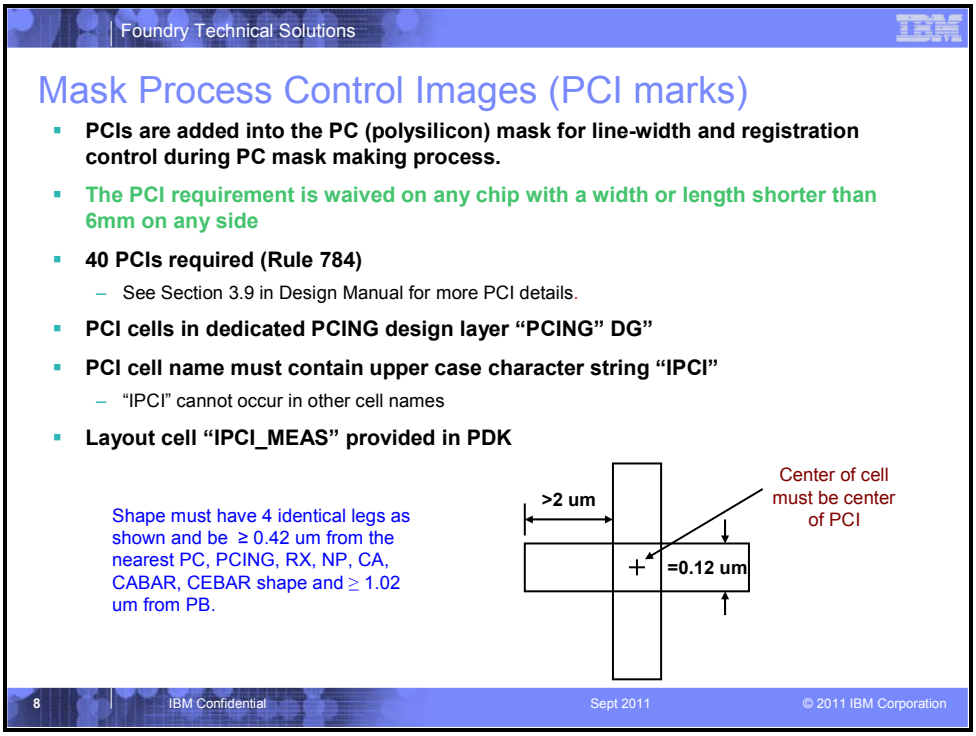
Text data is not allowed on mask build levels (S10). A Skill utility is included in the design kit which will convert any text data associated with pins to the “TEXT” “DG” layer. This utility is executed on stream-out if the default option “Convert PIN labels to text layer?” is selected.

These rules are checked by the DRC verification decks.



Design Rule Classification

Section 3.1 of the Design Manual defines classifications for the design rules. These are discussed further in the Verification section of this training. Designer should meet Class a and b rules and may exercise discretion for Class c rules and follow Class d "recommended" rule if space is permitted and performance is not compromised.

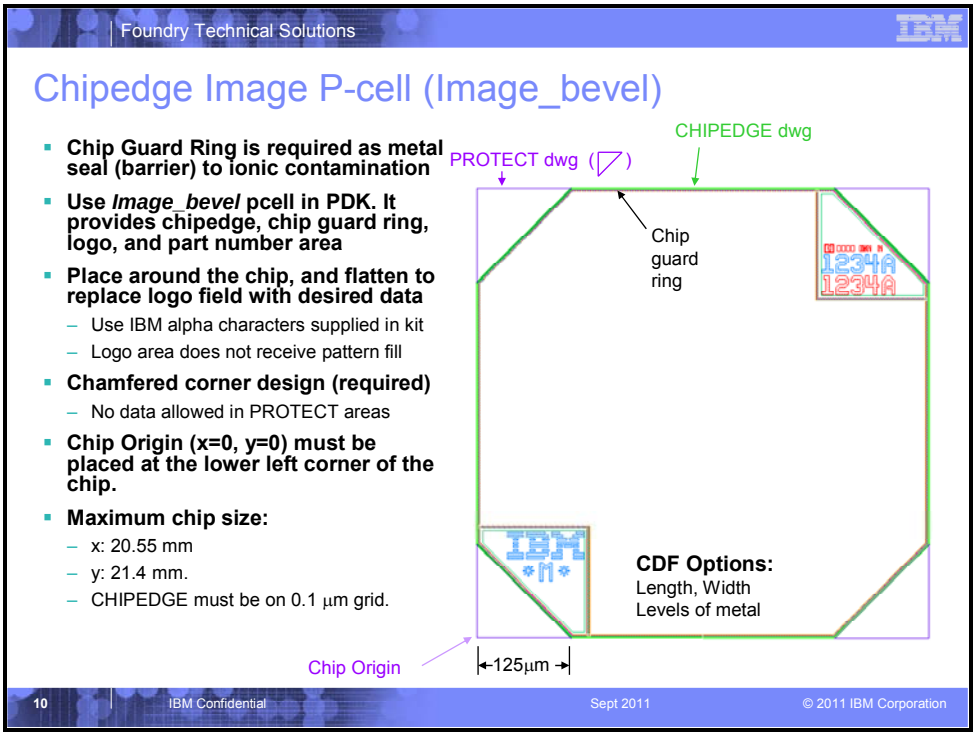


Process Control Images (PCI)

PCI marks are standard shapes added to a design for the purpose of controlling line width and registration during the mask making process. Minimum sized features *on chip* often have assist features or mask compensation applied to them during the data preparation process. For this reason, standard shapes are often not useful for controlling the mask manufacturing process. PCI marks are added to all mask levels in the IBM kerf (scribe line) region. Adding of the PCI marks inside the chip is required for PC level only.

It is recommended that customers add the PCI marks. Alternately IBM Data Preparation Services will place them.

PCI marks are required only for large chips (>6 mm on side).



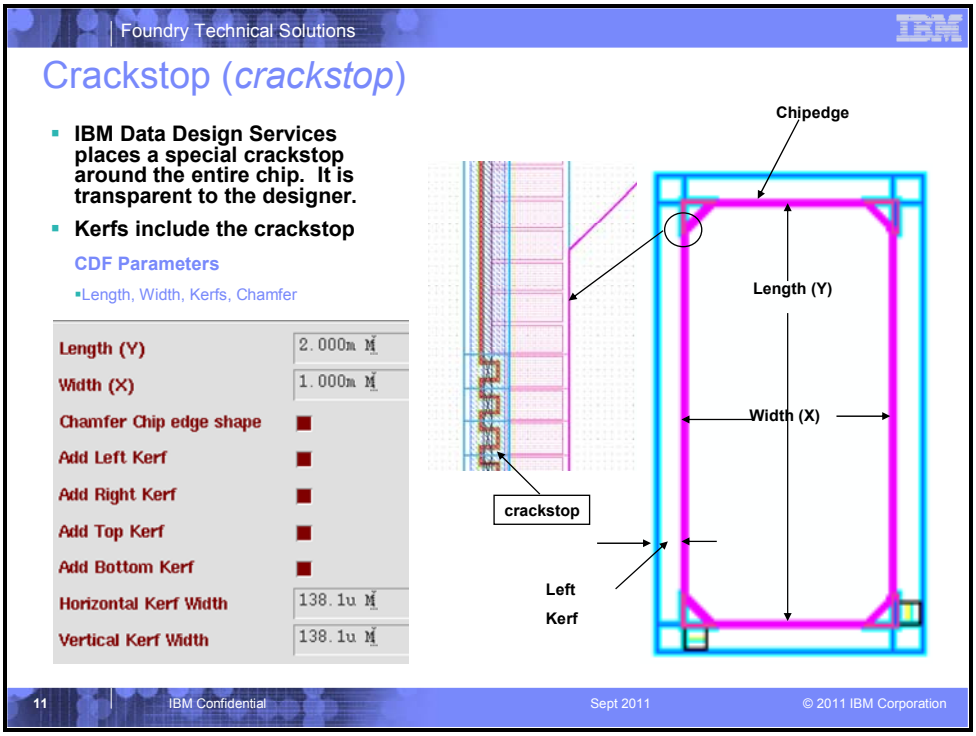
Chip Size, Chip Guard Ring and Chip-Edge (Image_bevel)

Designers need to include chip guard ring for preventing ionic contamination and place chip edge around the chips. The die size specified to IBM on the Foundry Questionnaire is determined by the dimensions of the CHIPEDGE shape.

The chip origin (x=0, y=0) must be placed at the lower left corner of the chip. CHIPEDGE must be bounded at X=0 on the left side of the chip (not in the chamfer area), and bounded at Y=0 at the bottom of the chip. The X and Y dimensions of CHIPEDGE must be a multiple of 0.1 µm and must be on grid. The maximum chip size allowed is 20.55 mm in the x-direction and 21.4 mm in the y-direction.

The *Image_bevel* pcell in the BiCMOS8HP PDK provides the CHIPEDGE, the ionic contamination guard ring and the logo and part number areas. The *Image_bevel* pcell should be placed using the chip dimensions then flattened in order to customize the logo and part number area. IBM requirements for part numbers are given in the Design Manual and DRC-clean alpha-numeric layouts of various sizes are supplied in the *alpha12, alpha20, alpha25 and alpha40* cells in the BiCMOS8HP library.

Beveled (chamfered) corners are required on all chips. Four triangular shapes on level "PROTECT" "dwg" are placed with the pcell to allow DRC checking to ensure that no customer shapes are placed in the chamfer area.

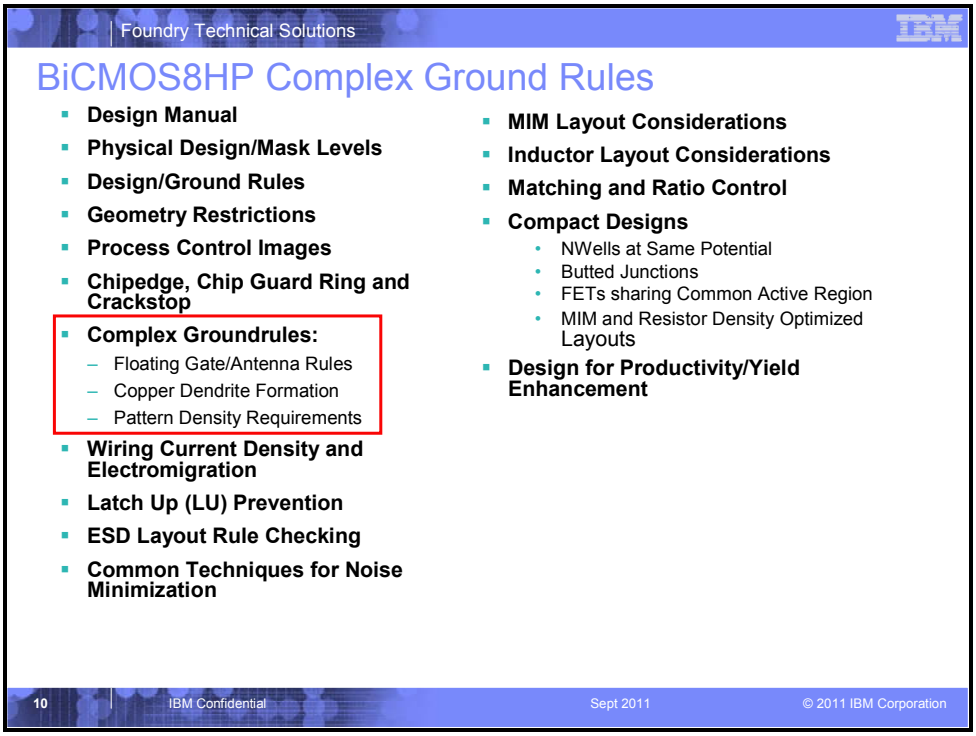


Crackstop

A *crackstop* pcell is also included in this design kit. Crackstop is a special design that is placed around the entire chip. This is done by Design Services and is transparent for designers. For designers, it is useful for placing chiplets (multiple chips) in the same design.

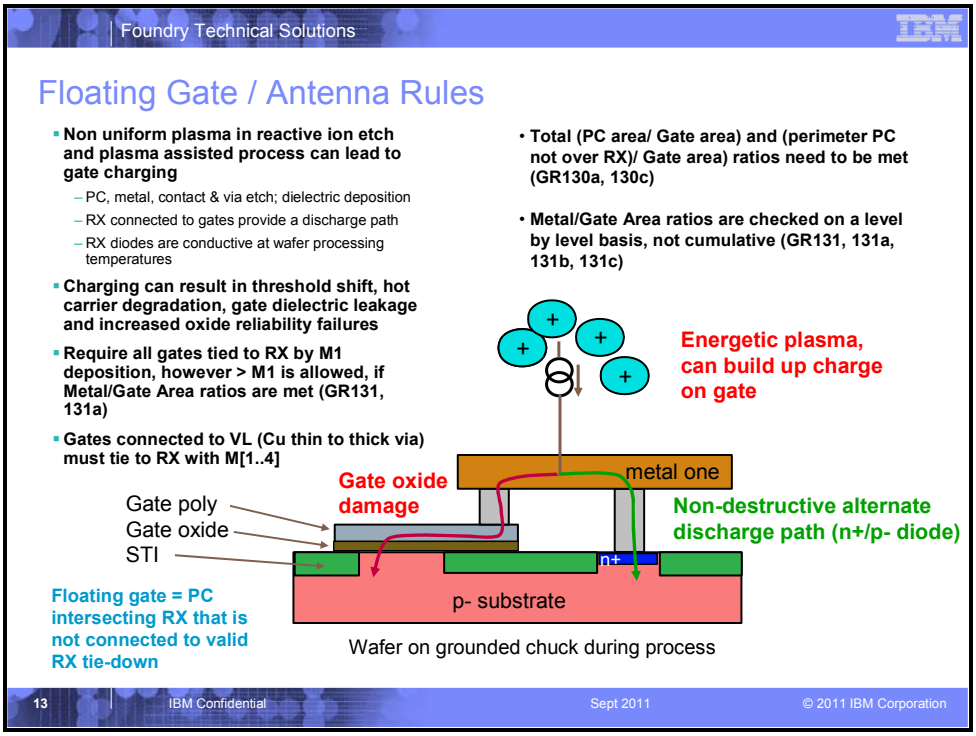
The crackstop pcell is very flexible. Users can select the chip length, width and the kerf sizes. The kerf can be optionally added to any side by selecting the “Add Kerf”.

This pcell is very useful when creating your own MPW with chiplets. There is an Application Note posted on ICC that describes the how to create a MPW - “Chip Matrix and Multi-Project Wafer (MPW) Methodology”.



Complex Groundrules

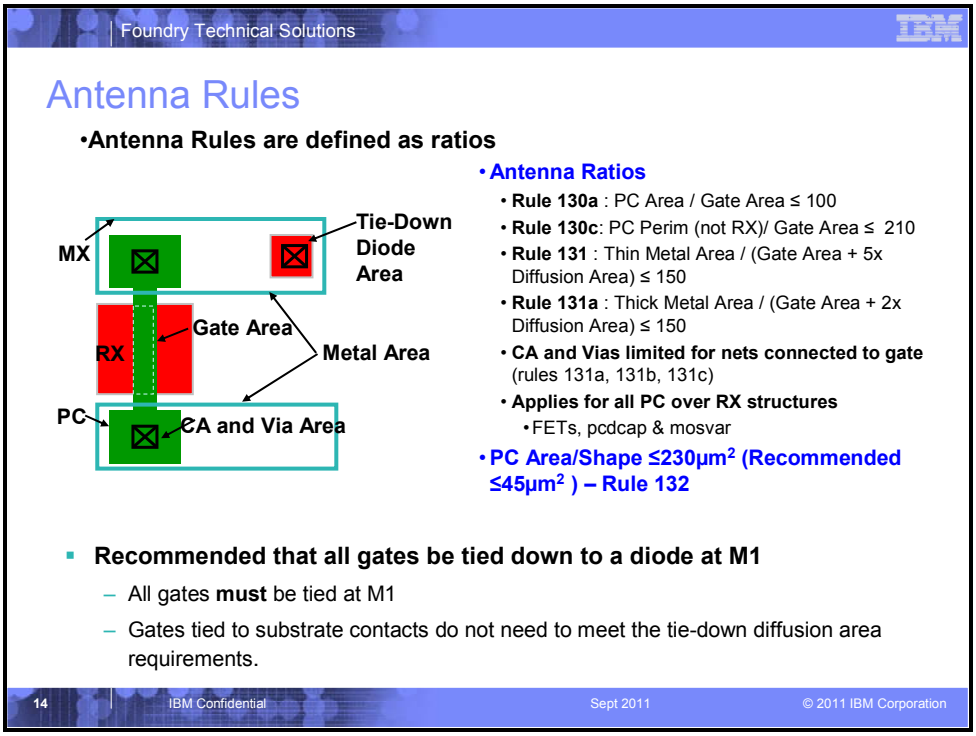
Many of the groundrules are straightforward line width and space checks. However, certain rules are more complex in nature, and the intent of the rule may not be immediately discerned from the definition which is detailed in the Design Manual for DRC coding. Here we discuss antenna rules, which are required to protect gate oxides during processing. Metal dendrite formation during copper processing is minimized through the groundrules. Pattern density rules are required in order to prevent systematic sensitivities.



Floating Gates, Antenna Ratios and Tie Downs

Thin gate oxides are subject to charging damage during wafer processing. Energetic process steps such as reactive ion etching (RIE) and plasma deposition may lead to a build up of charge on the gate relative to the wafer substrate on the grounded chuck. If the gate charges to a sufficient potential, the gate oxide will break down. The resultant current flow through the gate dielectric causes an increase in trap states and thus an increased susceptibility of the device to hot carrier effects. Gate oxide damage results in a degradation of device reliability, with increased gate current, transconductance and threshold voltage shifts over time.

Gate oxide damage due to charging is avoided by providing an alternate discharge path from the gate node to the substrate. A diode to substrate, shown in the above slide, is an effective means to prevent charge build up across the gate dielectric. At wafer processing temperatures, the diode is sufficiently conductive to prevent any charge build up. At normal circuit operation temperatures, the diode is in a low-leakage, low-capacitance reverse biased state.



Antenna Rules

In the BiCMOS8HP technology, it is highly recommended that all gates be tied to a diode by M1. This floating gate tie down protects the FETs during subsequent metal and oxide RIE etch and plasma deposition. FETs used in circuit applications which are insensitive to device shifts (such as digital logic gates) may be exempted from the floating gate tie down requirement if they can withstand the threshold shift.

Regardless of whether a gate is treated as “analog” or “digital”, the amount of charge build-up on the gate dielectric must be limited by restricting the size of the metal and vias that are exposed to the energetic process environment. Layout rules protect oxides from unacceptable damage by specifying the maximum area of connected metal wire in relation to the thin oxide area and the size of the tie-down diode (if present). The ratio is not cumulative. The antenna ratio at M1 does not contribute or affect the antenna ratio at M2.

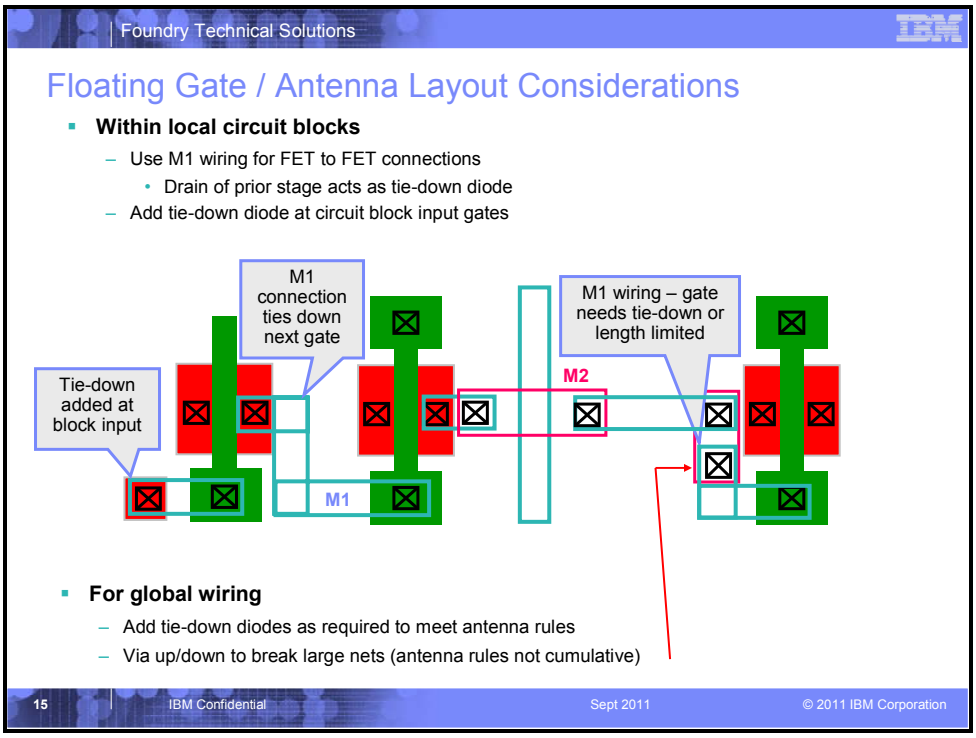
Gate charging damage before metal one deposition is prevented through the PC antenna rule, which limits the ratio of polysilicon conductor area to gate area to be less than 210 to 1.

Gate charging damage before metal one deposition is prevented through the PC antenna rule, which limits the ratio of polysilicon conductor area to gate area to be less than 100 to 1. GR 132, which limits the size of a single PC shape to <= 230µm^2, is also for protection from excessive charging of the thin gate oxide. For circuits very sensitive to device shifts, it is recommended to follow the more stringent rule 132R (<= 45µm^2) which further limits the gate area of a single PC shape.

See Design Manual Section 3.1 “Antenna Rules” and Polysilicon and Isolation Layout Rules” for more details

In addition to gates, N-well regions must be tied to (N+ diffusion / substrate) diodes to prevent charge buildup in the well (GR267). Leakage (during processing) between (N+ diffusion / substrate) is higher than between (N-well / substrate) and will prevent excess charge buildup in

the well. These contacts can be made either by contacting (N+ diffusion / N-well) to (N+ diffusion / substrate) through M1 or by intersecting an N+ diffusion with an NW shape.



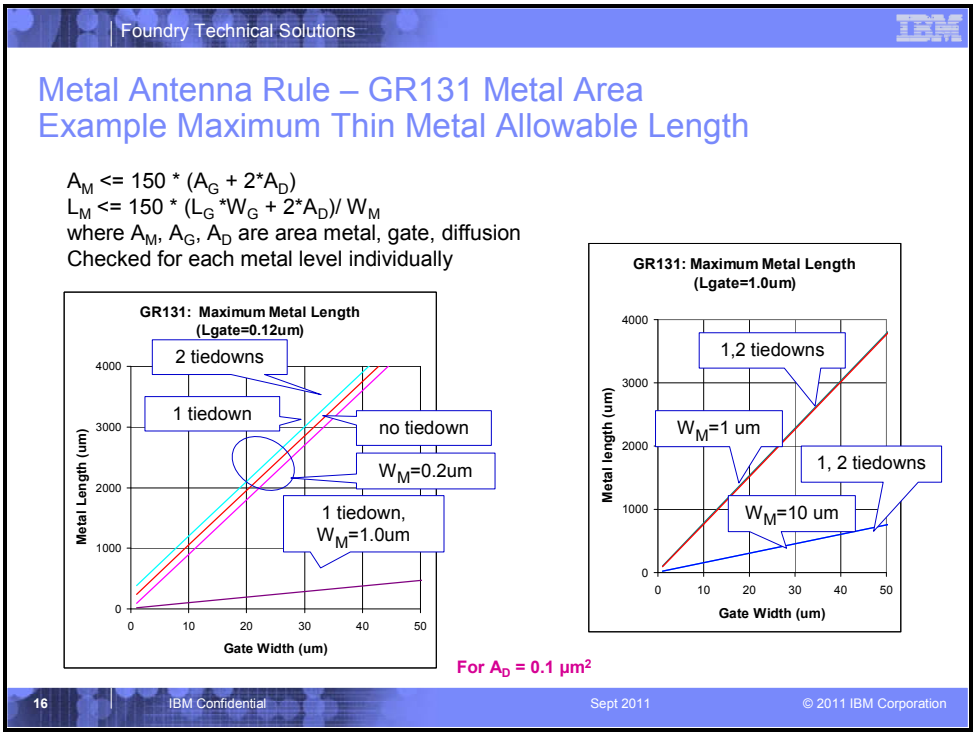
Floating Gate/ Antenna Layout Consideration

The drain diffusion of the prior stage acts as a tie-down diode for FET gates. If the wiring is done with metal one, then gates will pass the floating gate. The center gate in the figure above is tied with metal one to the drain of the FET on the left. If however the wiring goes up to M2 (as shown on the right), either a tie-down diode (connected to the gate by M1) needs to be added or the metal area must be carefully managed. It is advisable to add a tie-down to the input gates of all circuit blocks to avoid floating gate and antenna errors later in the chip design cycle.

In the example on the right hand side the contribution of M1 for floating gates was minimized by introducing a “hop” up to M2. The M1 past the “hop” does not contribute since there is no connection. The connection was made at M2 at which time the M1 wiring does not contribute to floating gate charging.

The contact to gate area ratio is limited by groundrule 131c. The ratio of via area to gate area is limited by 131a (DG oxide) and 131b (thin oxide gates); if the via to gate area ratio is exceeded, RX diffusion must be added to satisfy the ratio.

Nets that are connected to substrate are exempt from GR131a, b, the gate/via check. Finally all nets must be tied to RX before the MQ level.

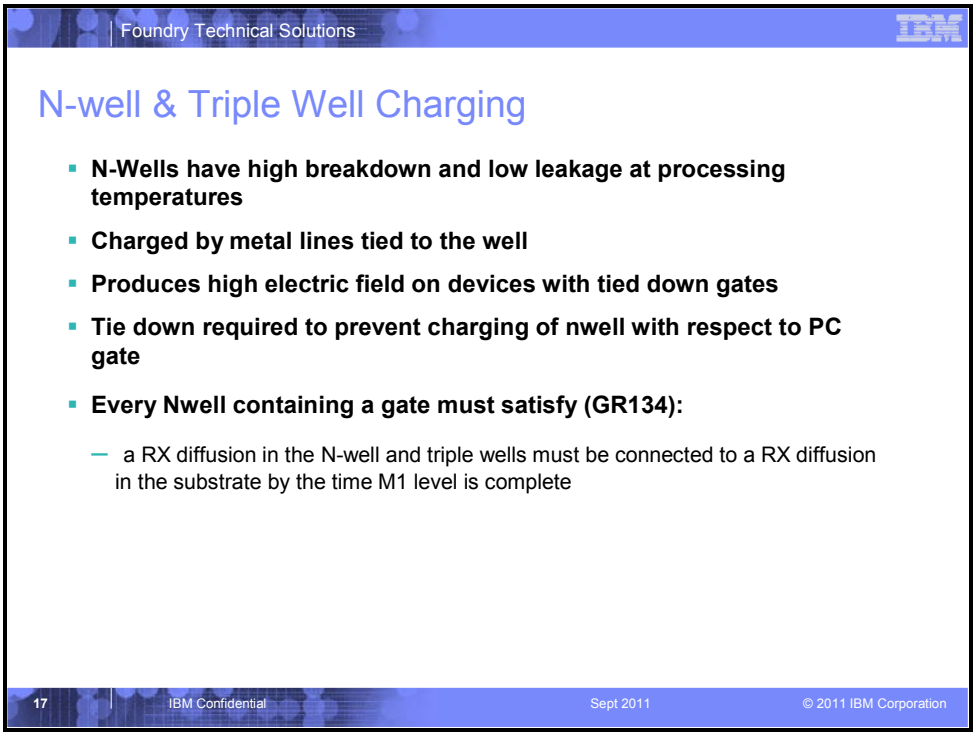


Metal Antenna Rule – GR131

Groundrule 131 limits the area ratio of metal to (gate + (5* diffusion) area (M[1..4]). Each metal level is considered individually, for example, the rule applies to the ratio of M1 to (gate + 5* diffusion) for the net formed by CA connections down to RX (diffusion) and PC over RX (gate). The rule also applies to the area ratio of M2 to (gate +5* diffusion), considering the connections from M2 down to RX and gate through V1, M1 and CA, but the M1 metal does not contribute to the M2 area ratio.

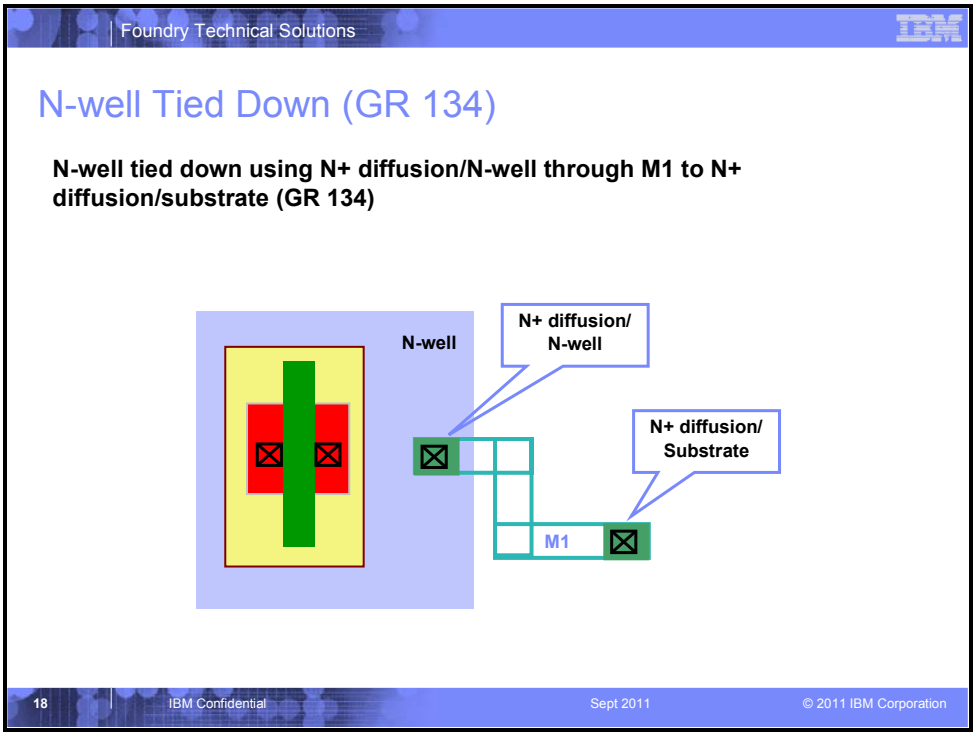
The charts above show the maximum length of metal that can be connected to a gate versus total gate width on the net for various conditions. On the left, all gates are minimum channel length (0.12um), and for the top 3 lines, the metal width is the minimum, 0.20um. These three curves are meant to represent typical digital logic circuit connections. With no tie-down, 0.9mm of minimum width wiring can be connected to a 10um/0.12um gate before violating GR131. For longer wire lengths, a tie-down diode would need to be added to the net (or the net could via up or down to another metal level). The maximum length for a 1um wide metal wire is reduced since it is the metal area involved in the rule.

On the right graph, the gate channel length is 1um. The top two curves are again a metal width of 1um, for 1 and 2 tie-down diodes on the net. For these longer gate lengths, the maximum metal length (area) is increased. Tie-down diodes are less effective at increasing allowed wire run length because of the increased wire width. For long channels and wide metal widths (1um gate length and 10um metal width shown in the lower most curve on the right hand chart), small tie-down diodes have little value. For these “analog” types of layouts, keep circuit blocks in close proximity, or if that is not possible, via up or down to minimize the metal area connected to the gates at any given metal level processing.



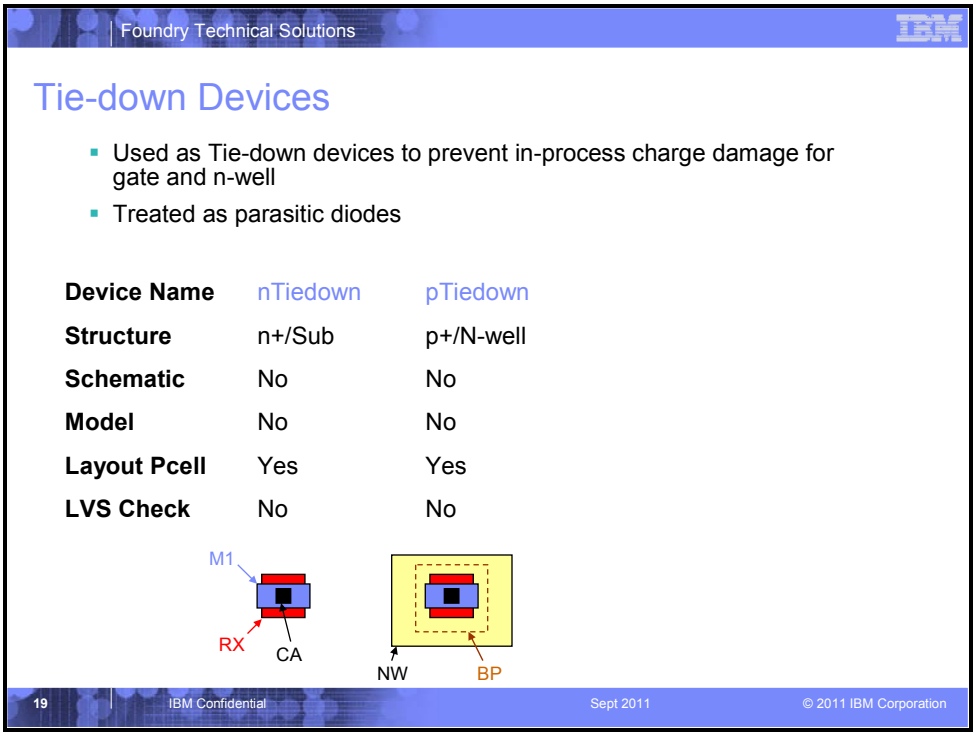
N-well and Triple Well Charging

In addition to gates, n-well regions containing a gate must be tied to (n+ diffusion / substrate) diodes to prevent charge buildup in the well (GR134). Leakage (during processing) between n+ diffusion/substrate is higher than between n-well/substrate and the tie down will prevent excess charge buildup in the well.



N-well Tie Down

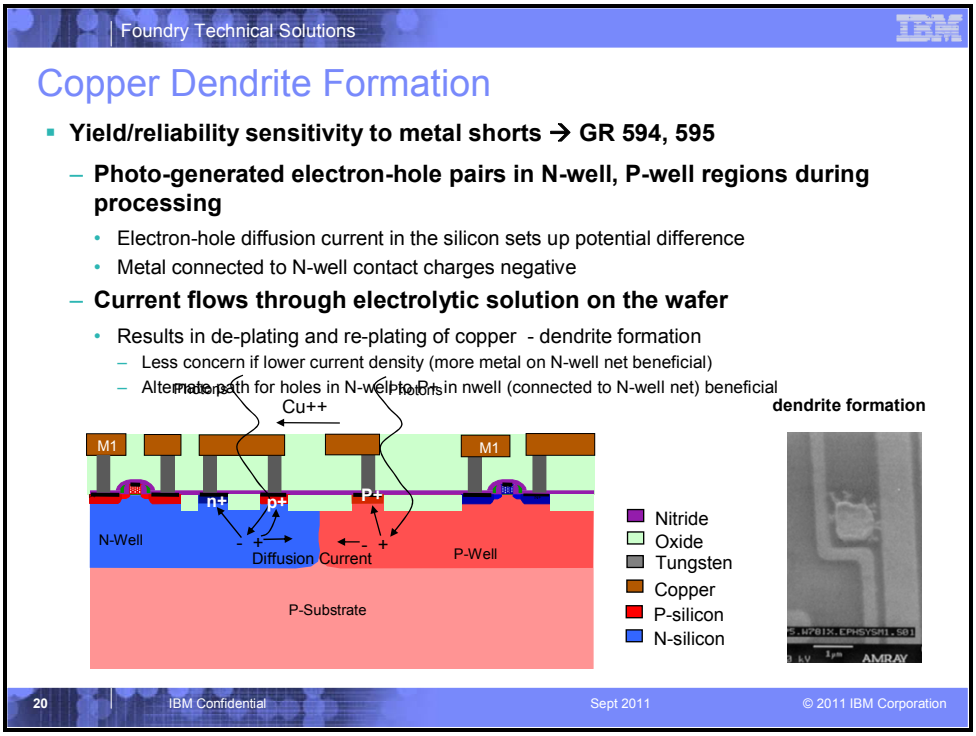
The above slide shows an acceptable connection through M1. An n-well can also be tied down by intersecting an n+ diffusion with an n-well region and a p-well region.



Tie-down Devices

Some devices require a current path to prevent charge build-up and damage during wafer processing. The current path is typically provided by a reverse-biased diode called a “tie-down” diode. These are typically n+/substrate or p+/n-well diodes.

Layout pcells *nTiedown* and *pTiedown* are provided in the design kit for creating the tie-down diodes. They are treated as parasitic diodes by the design tools.

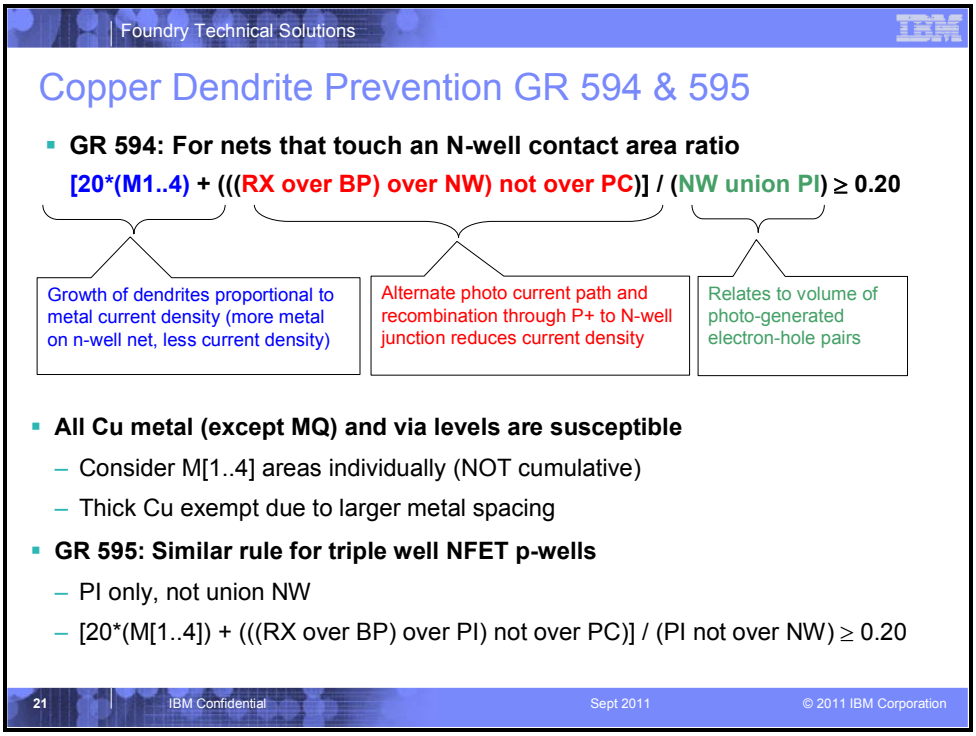


Copper Dendrites Formation

During processing of copper metal levels, a local potential difference created at the wafer surface can drive an electrochemical reaction in an electrolytic solution on the wafer. If a sufficiently high potential difference exists de-plating and re-plating of copper can occur. This metal migration can lead to degraded reliability or yield loss due to shorts or metal opens.

In the example shown above the potential difference is photon generated (photo current) during the copper polish step. For electron hole pairs generated in the p-well or p- substrate the holes are majority carriers that remain in the region and are collected at the p+ contact as photo current. The electrons in this region diffuse and drift to the n-well region where they are collected as photo current at the n+ contact. Likewise for electron hole pairs generated in the n-well, the holes diffuse and drift to the p+ contact and the holes are collected as photo current at the p+ contact. The result is the metal connected to the p-well becomes positively charged with respect to the metal connected to the n-well and current flows through the electrolytic solution used for copper polishing. This current flow causes de-plating and re-plating of the copper metal level being processed. Potential differences can also exist due to wafer brush cleaning which is a cleaning operation performed after chemical-mechanical polishing. These potentials form due to wafer spin and frictional contact.

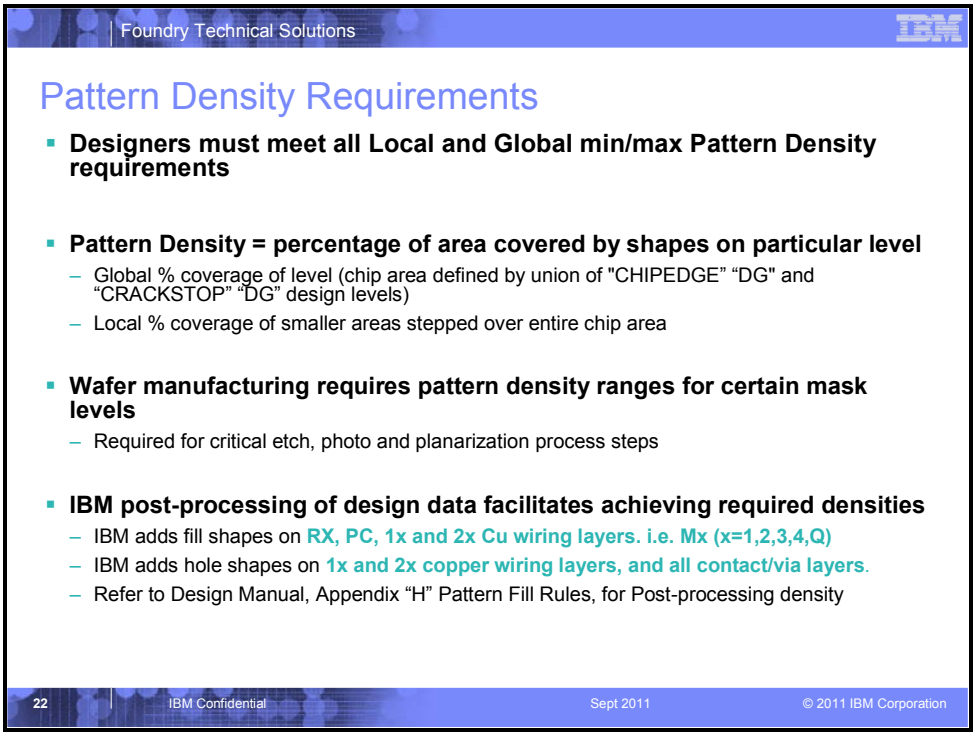
The probability of dendrite formation on metal lines connected directly to n-wells will be directly proportional to the size of the n-well and inversely proportional to the size of the metal. In addition, placing a p+ diffusion in the n-well that is wired to the n-well contact reduces the current flowing from metal to metal. This p+ diffusion collects some of the minority generated holes in the n-well and allows them to recombine with the majority electrons without adding to the metal to metal current.

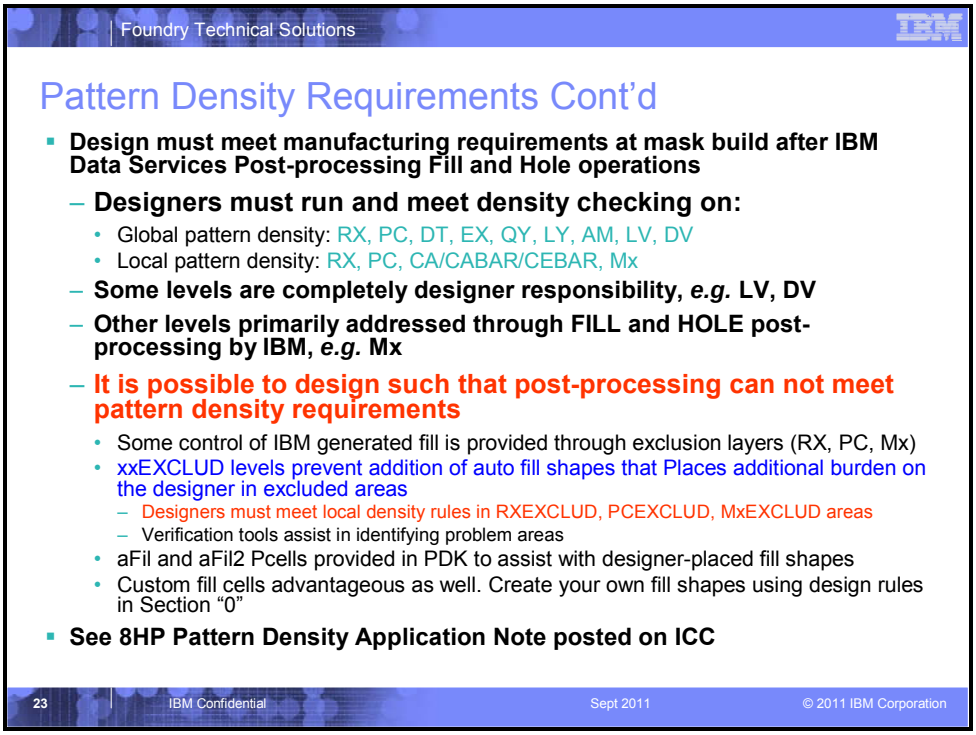


Dendrite Prevention: Ground Rules 594 and 595

Groundrule 594 checks the metal area and p+ diffusions wired to n-well contact such that dendrite formation and the associated yield and reliability concerns are mitigated. Similarly, groundrule 595 checks the metal area and n+ diffusions wired to the triple well p-well contact.

The slide highlights the two numerator terms (20* copper metal area, and the p+ diffusion in n-well) and the n-well area (or PI, the deep n-type buried layer which isolates the p-well of triple well NFETs from the substrate) in the denominator of GR594. The primary layout consideration to avoid copper dendrites and being flagged for groundrule 594 is the use of sufficient metal in the net connecting to n-well. This is advantageous for other electrical considerations such as latch-up prevention as well. Additionally, connecting PFET source connection to the n-well potential through the copper metals will assist in meeting the required ratio.





Pattern Density Requirements

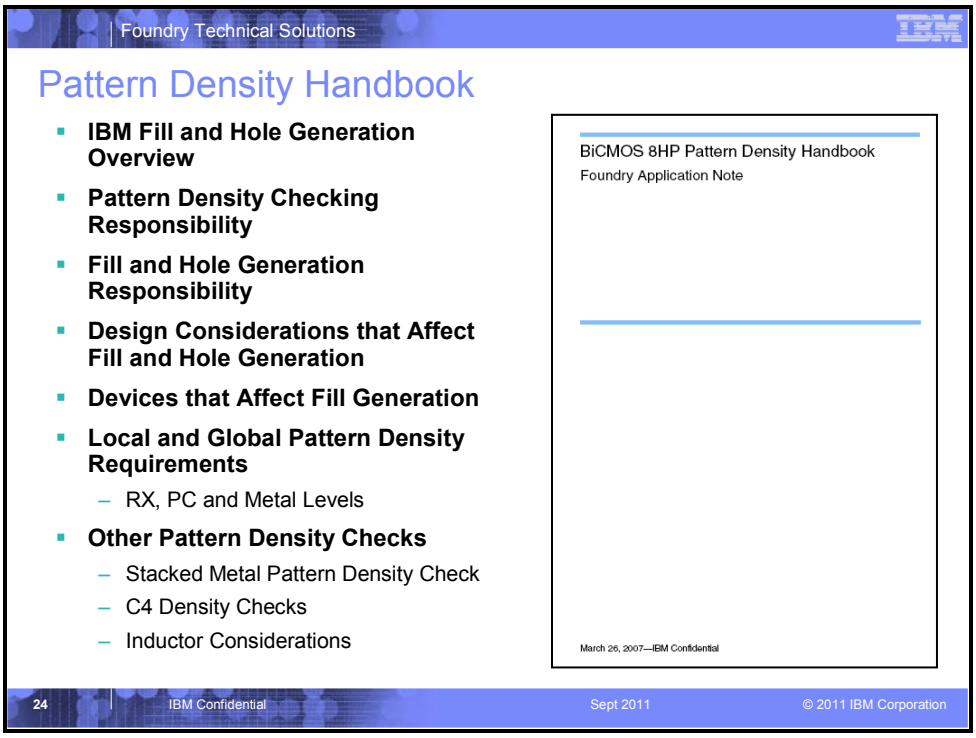
Pattern density refers to the percentage of area covered by shapes on a particular level. It can be specified globally for the entire chip, or locally over a smaller area. Both specifications may be used depending on the mask level. Many wafer processing steps have been optimized to perform over a particular range of pattern densities. Typical steps with pattern sensitivities are chemical-mechanical polishing (CMP), reactive ion etch (RIE), and when pattern density creates wafer topography, lithographic imaging.

IBM utilizes post-processing algorithms on levels PC, RX, and metals M1-M4 and MQ to facilitate the task of meeting manufacturing pattern density requirements. This involves adding fill shapes for M2-M4 and MQ. In addition to fill shapes, holes are generated in wide M1 metal lines to enable copper polishing processes.

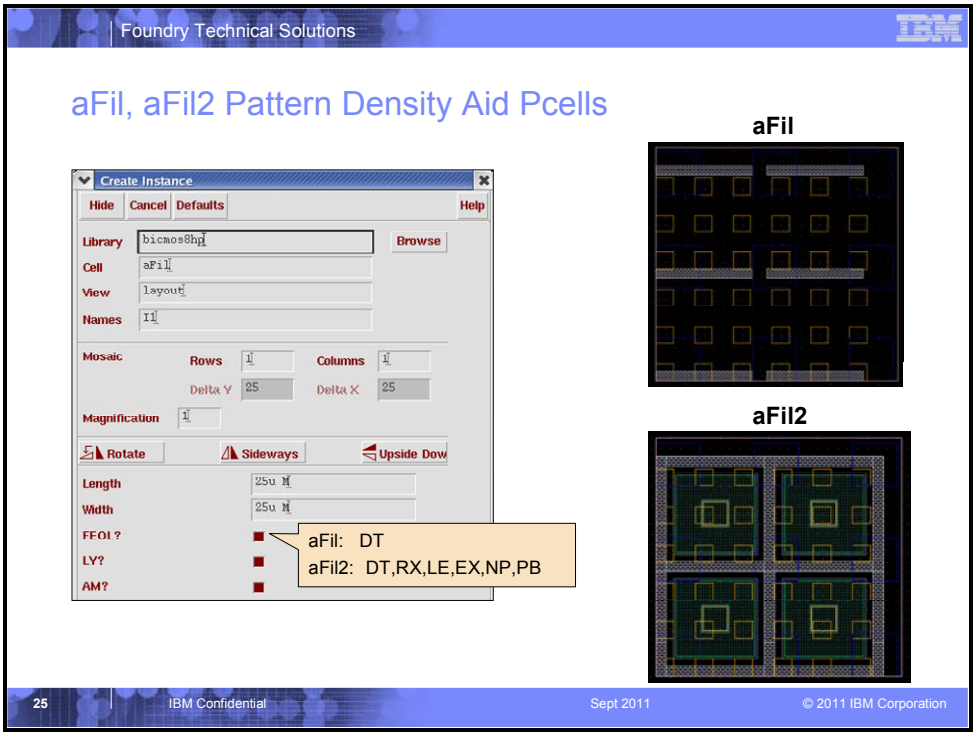
It is possible to design in such a way as to prevent post-processing routines from achieving the pattern density specifications. This could occur if design pattern density is too high, or if automatic fill is blocked by exclude layers or large congregations of devices which prohibit fill (such as KQ resistors preventing MQ fill). When the verification tools identify these situations, designer intervention is required.

The technology affords some control of IBM fill shapes by providing levels RXECLUD, PCEXLUD, MxEXCLUD (x=1,2,3,4,Q) to suppress automatic fill the corresponding layer. Use of these shapes places an additional burden on the designer to assure that pattern density in the excluded area meets requirements. Two fill cells, aFil and aFil2, have been provided as an designer's aid to meet the pattern density requirements.

An Application Note is available on IBM Customer Connect (ICC) that delineates the pattern requirements including who is responsible, IBM or designer, and which design levels, to meet the pattern density requirements.



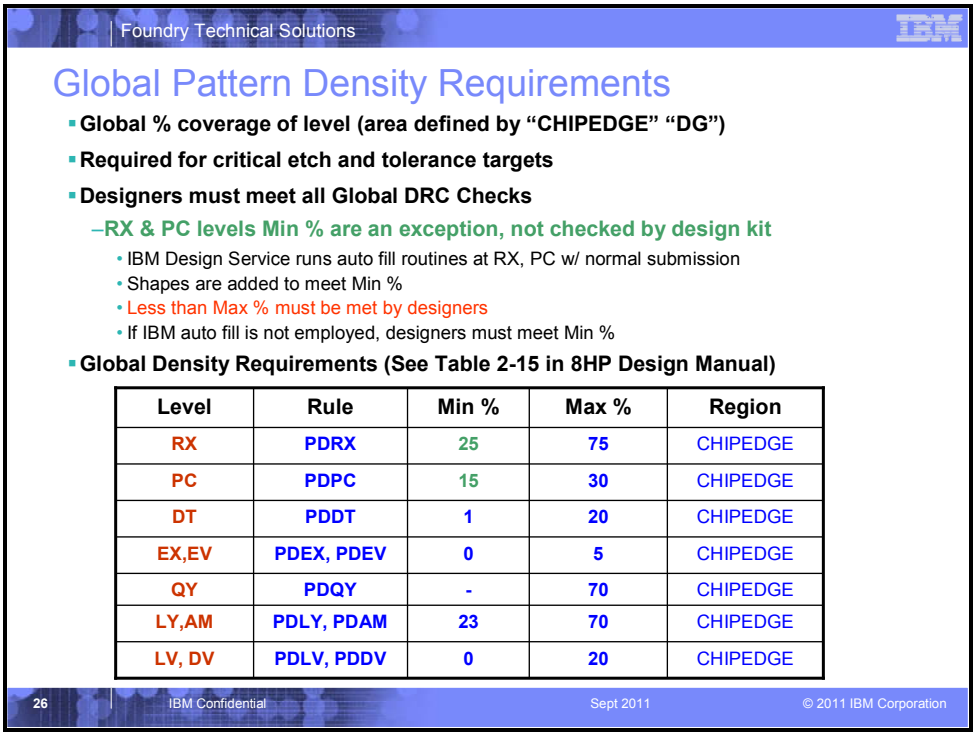
Pattern Density Handbook



aFil, aFil2 Pattern Density Aid Pcells

Two fill cells, *aFil* and *aFil2*, have been provided as an aid in meeting pattern density. The *aFil* pcell contains DT plus wiring levels. The DT level may be switched on or off as a group while the wiring levels may be switched independently. The *aFil2* pcell is similar to the *aFil* with the addition of the bipolar FEOL levels. When a large size is selected, the shapes are automatically fractured to meet maximum size rules for pattern fill shapes.

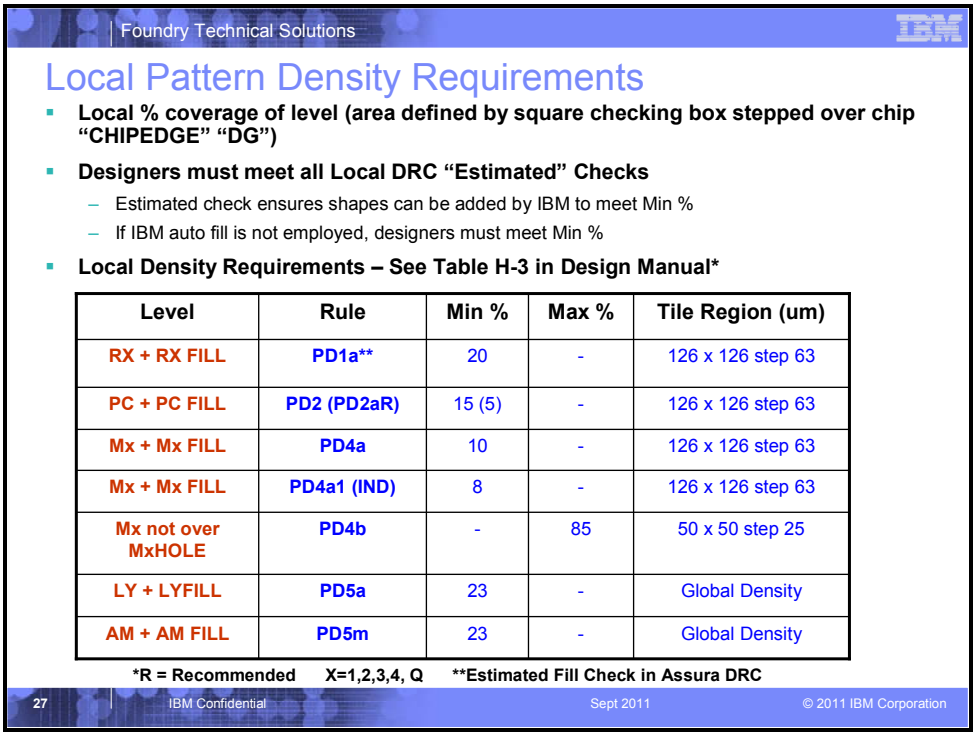
These fill cells are particularly useful in meeting minimum pattern density in areas that will not be automatically filled, for example areas under IND_FILT, xxEXCLUD, LOGOBND.



Global Pattern Density Requirements

Global pattern density refers to the total area on the mask level relative to the total chip area (chip edge boundary). For some mask levels, pattern density must fall within a specified range to enable IBM to manufacture the part.

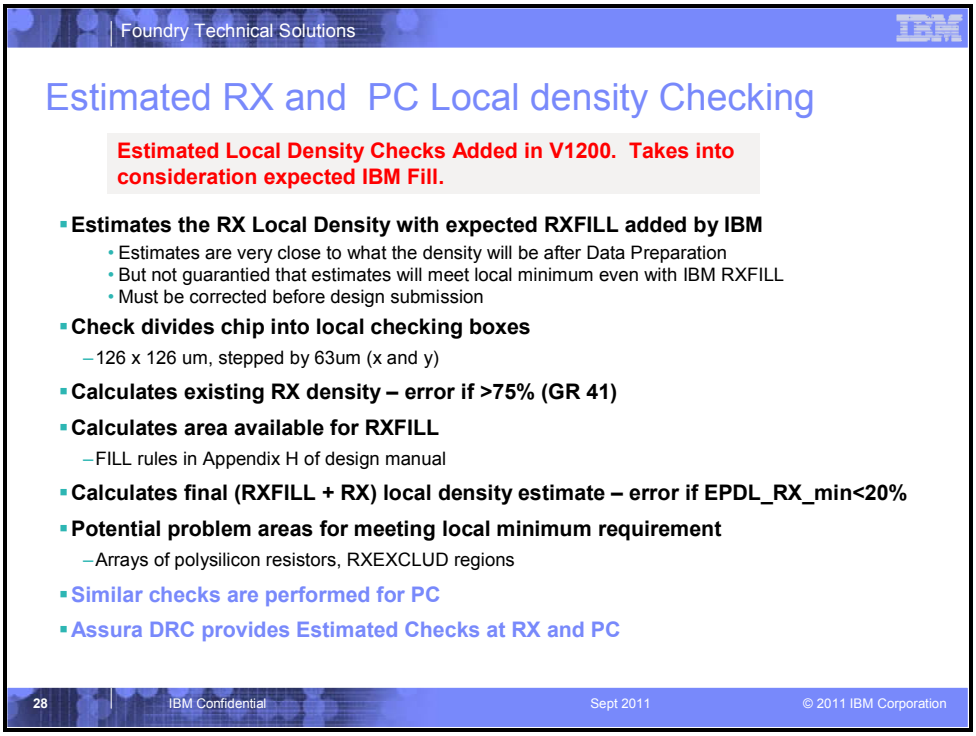
The RX and PC Design Min (minimum) Global Pattern Density rule is not checked in the Design Kit. IBM prefers that RX and PC minimum Global Pattern Density not be checked by the customer, or attempted to be met by the customer, prior to submission of the chip design to IBM. The RX and PC minimum Global Pattern Density for the chip design will be verified by the IBM release team after IBM-generated RXFILL is applied to the chip design, which is part of the IBM release process.



Local Pattern Density Requirements

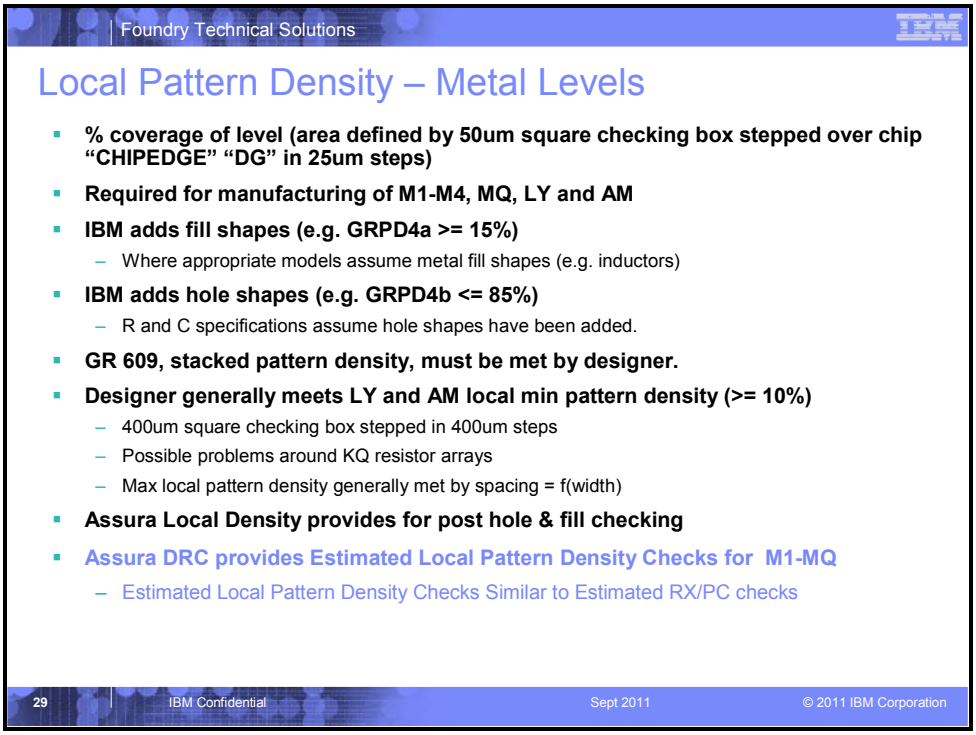
RX, PC, Copper and Aluminum mask levels have local pattern density requirements to help ensure that the pattern density within local regions of the mask is sufficient to prevent processing errors. IBM provides pattern density checks that partition the chip into multiple regions and apply a minimum pattern density criterion within each region or window.

Estimated RX fill check is available in the Assura DRC deck.

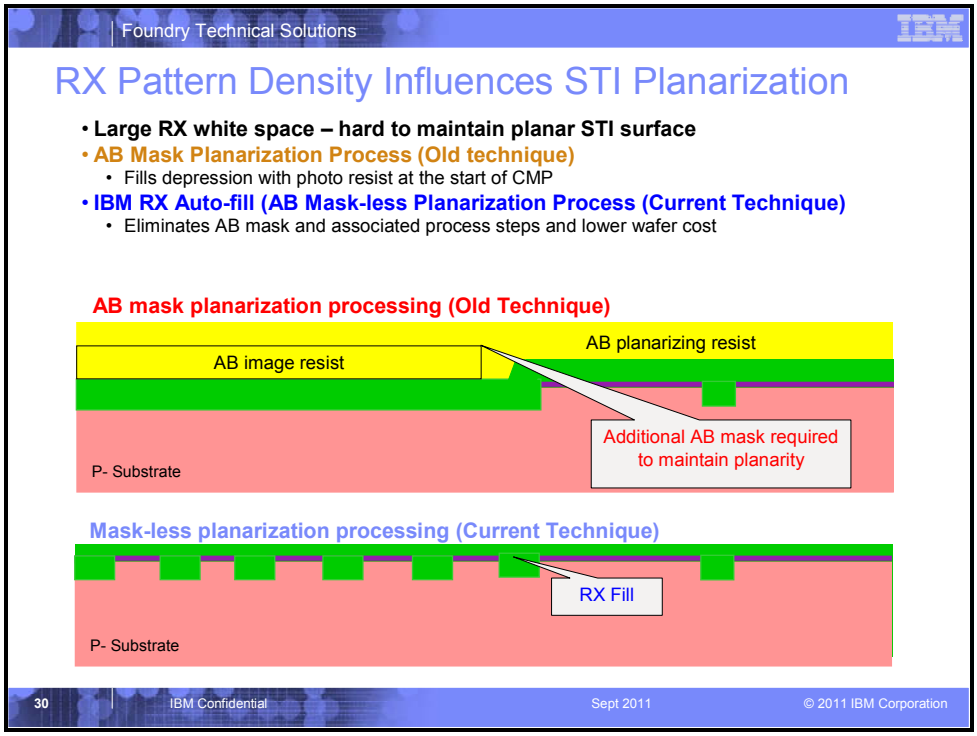


Estimated RX and PC Local Density Checking

BiCMOS8HP design kit DRC rule decks now include estimated RX and PC local density checks. These checks include IBM auto-fill.

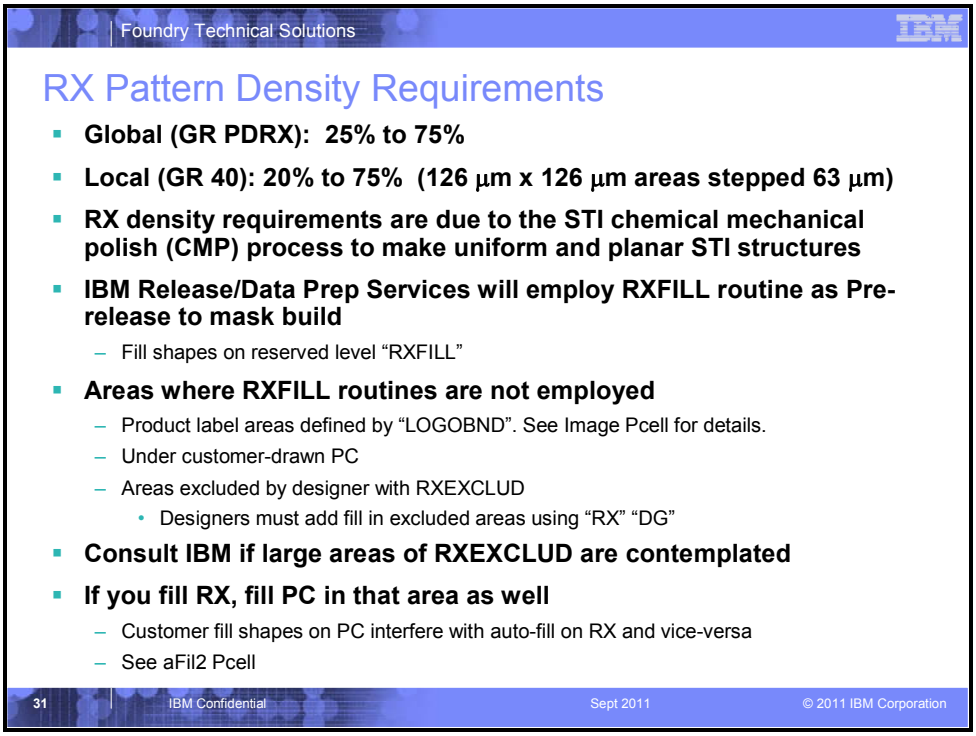


Estimated Metal Levels Local Density Checking



RX Pattern Density Influences STI Planarization

In prior IBM processes the difficulties presented by large areas of RX white space were solved by constructing a mask (AB) that would “fill” the depression in the oxide with photoresist. The photoresist created a planar surface at the start of the CMP process. The addition of the RX fill shapes allowed the omission of the AB mask process, reducing process complexity.

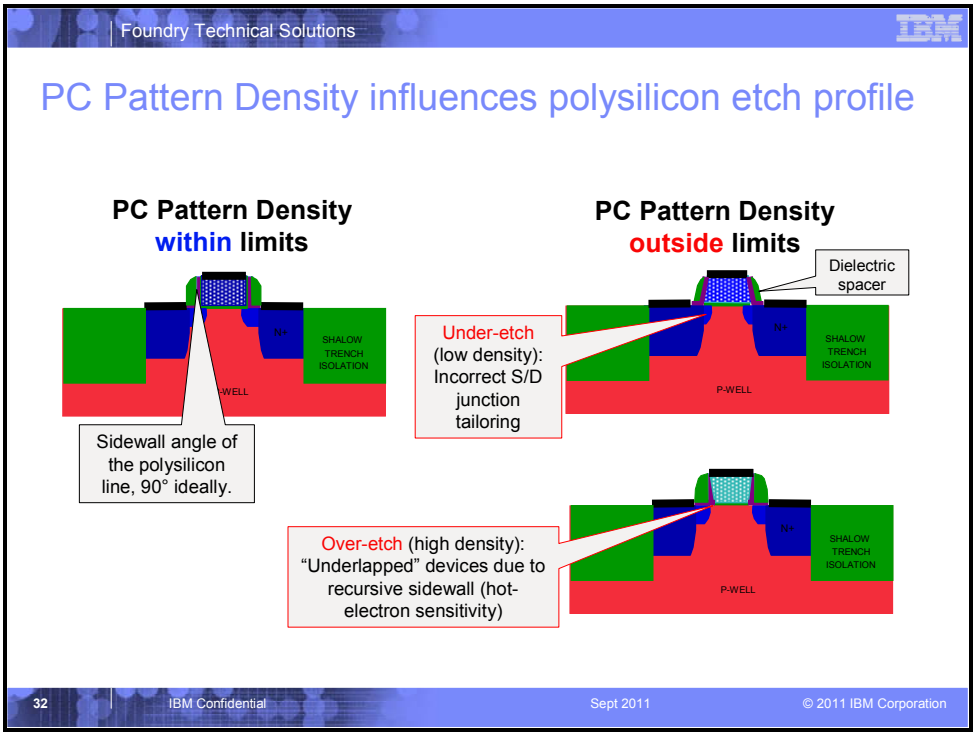


RX Pattern Density Requirements

At RX level a pattern factor requirement is in place to ensure that the process for creating shallow trench isolation (STI) can do so without dishing out the trench areas and/or damaging the active RX area. The goal of any STI process is to leave as planar a structure as possible without any damage to the RX. The BiCMOS8HP technology uses a deposition of STI oxide, followed by chemical mechanical polish (CMP). Areas with insufficient RX density will be over polished resulting in damaged devices and dished out white areas. The dished out STI or non-planar STI can create PC shorts and leakage paths between substrate and N+ source/drain or between N-well and P+ source/drain. Excessive pattern density can create a situation where the CMP operation cannot remove all the STI field oxide from the active RX areas. Residual oxide left at this stage in the process cannot be removed subsequently without removing excessive oxide in other areas.

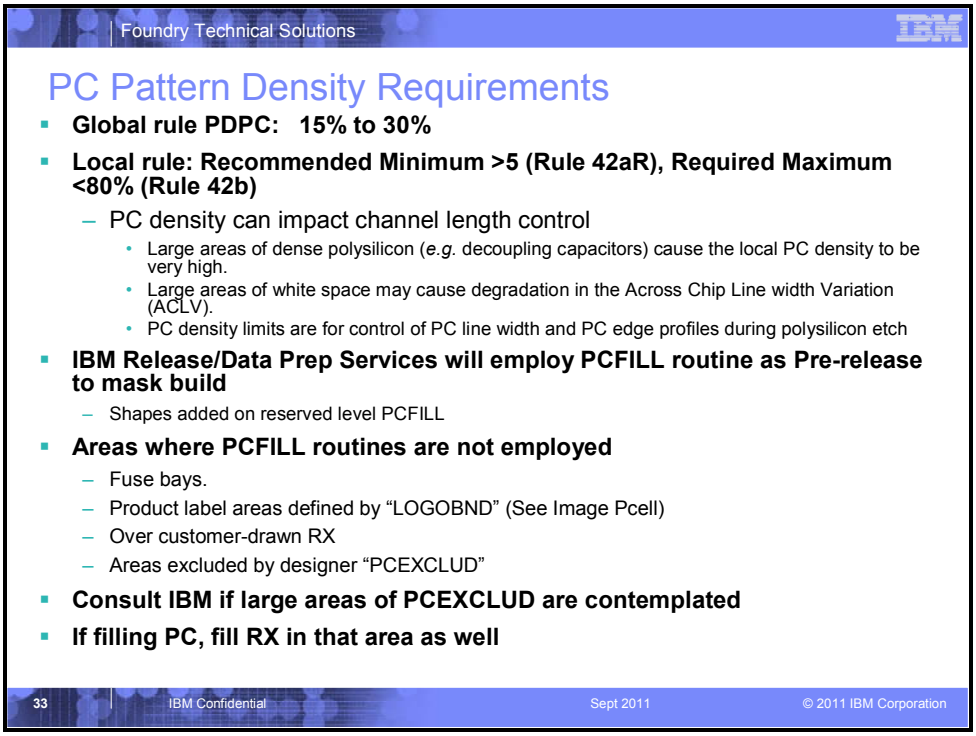
As described above, IBM Release/Data Prep Services Engineering will place RX fill shapes using an automated routine. Automated fill will not be placed under designer-drawn PC, in logo areas defined by "LOGOBND" or in regions covered by "RXECLUD." RX exclude regions may be used to suppress fill in areas designers deem too sensitive to allow machine-generated shapes. It is the responsibility of the designer to add fill as required such that the local pattern density rules are met in those excluded areas. Fill shapes should be on "RX" "DG." RXEXCLUD should only be used for small areas.

If designers add RX or PC fill, they should add both in the same area. Customer fill shapes on either of these levels will interfere with IBM automatic fill on the other. The aFil2 pcell is provided in the design kit for this purpose.



Polysilicon (PC) Pattern Density

Pattern factor influences the sidewall slope of the polysilicon line, which is ideally 90°. With pattern factor out of specification, recursive or tapered side wall slopes can occur. These conditions are shown in the above figure. Although a potential reliability concern is that voids could form under a recursive slope overhang, FET electrical characteristics are the main consideration with respect to pattern density at the polysilicon gate level. After the polysilicon is deposited and etched, dielectric spacers are formed on the gate sidewalls by depositing and etching the spacer films. N- or p-type dopants are implanted to define the source/drain regions of the FETs. The polysilicon sidewall angle is critical in defining spacer width and, as a result, achieving the specified gate overlap capacitance, intrinsic source/drain series resistance, electrical channel length, and hot electron immunity.



PC Pattern Density Requirements

Global PC density must be between 15 and 30%. There is no local rule for minimum; however, 5% minimum is recommended (Rule 42aR). Local density should be <80% (Rule 42b)

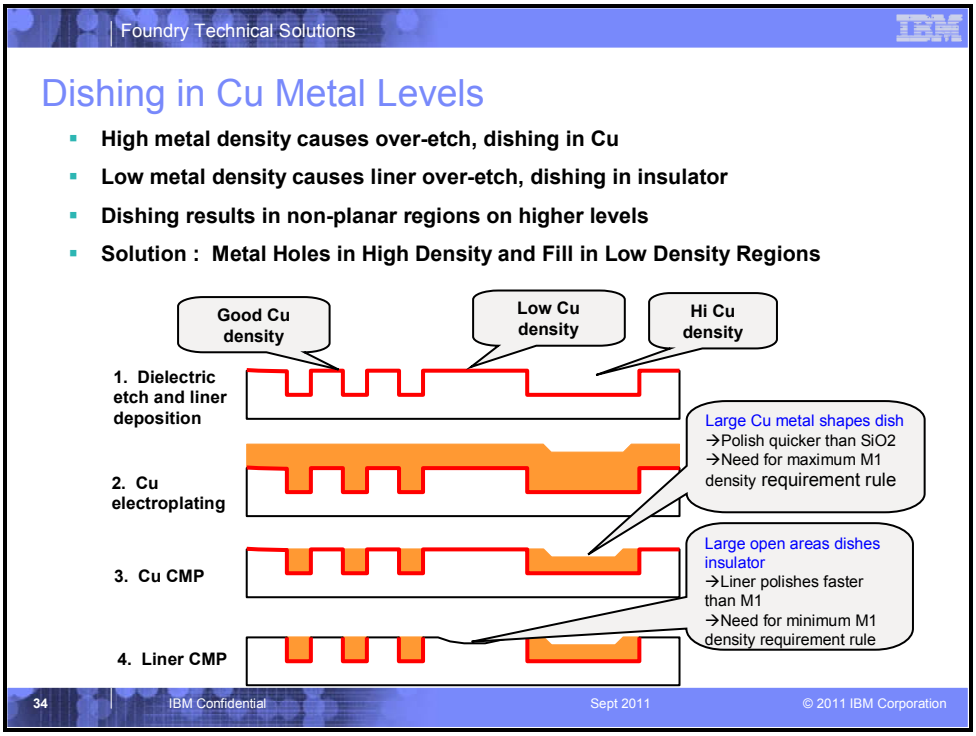
Channel length control can be affected by regions of very high or very low density. Polysilicon etch depends on pattern factor limits to maintain process centering, achieve line width uniformity across the wafer, and for sidewall slope control.

PC line width has a direct effect on fundamental FET device characteristics like Vt and Idsat. Process bias varies with pattern density; therefore it is important that all products in the manufacturing line fall within a specified range.

The dry etch process used to create PC shapes after they are printed is sensitive to pattern density. Consumption of reactive species and generation of byproducts can locally affect the rate and properties of the dry etch. Identical images in excessively high and low density areas can have different line width. Uniformity of etched features, in particular the relationship between isolated and tightly grouped poly line widths, is also a function of pattern factor. Processes are designed and monitored to assure that there will be minimal offset between these two types of features. Wafers outside of specified bounds can have large line-width offsets.

IBM Release/Data Prep Services Engineering will place PC fill shapes using an automated routine. Automated fill will not be placed in fuse bays, over designer-drawn RX, in logo areas defined by "LOGOBND" or in regions covered by "PCEXCLUD." PC exclude regions may be used to suppress fill in areas designers deem too sensitive to allow machine-generated shapes. It is the responsibility of the designer to add fill as required such that the local pattern density rules are met in those excluded areas. Fill shapes should be on "PC" "DG." PCEXCLUD should only be used for small areas.

If designers add PC fill, they should add RX fill in the same area. Customer fill shapes on PC will interfere with IBM automatic fill on RX. The aFil and aFil2 pcells are provided in the design kit for this purpose.



Copper Damascene Processing and Pattern Density

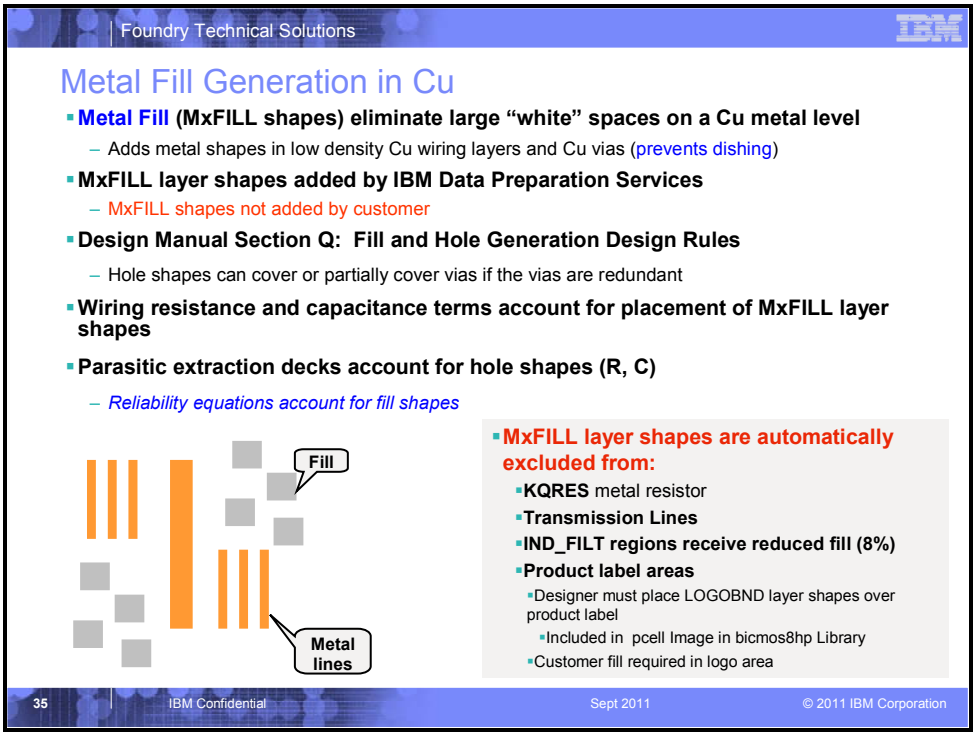
The BiCMOS8HP Damascene copper process begins with an application and patterning of photo resist over a level insulator surface. The subsequent etch process defines channels or groves in the SiO_2 where the Cu metal lines will be formed. First, a liner then Cu is deposited over the entire surface. The surface is polished to the point where only the liner and Cu in the channels remains. Another layer of insulator is deposited and the process of forming the metal lines begins anew.

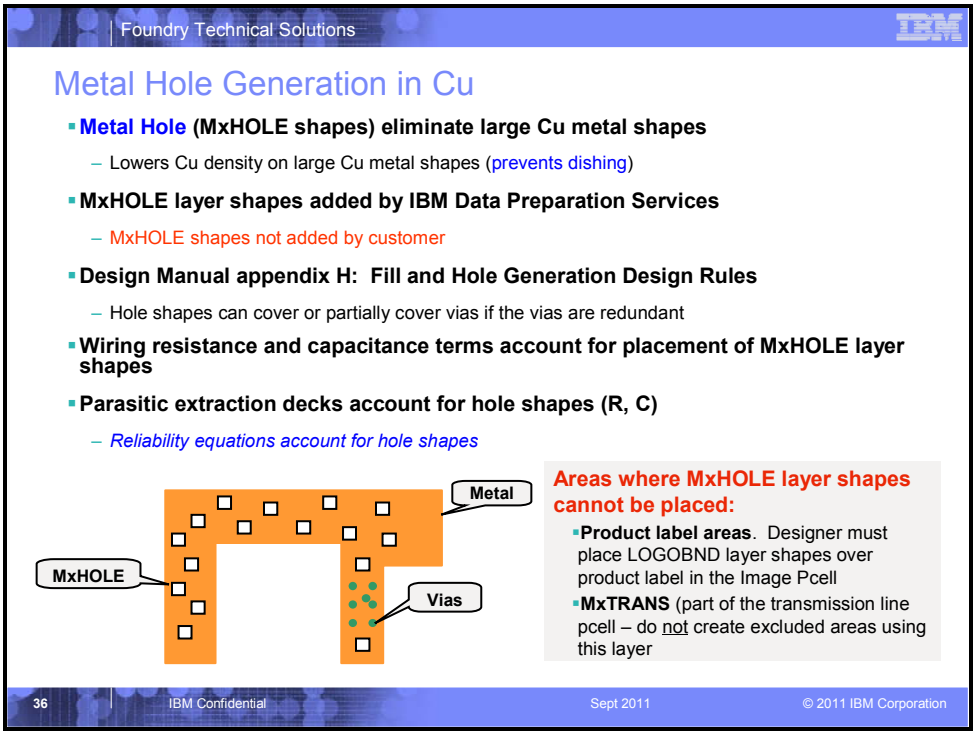
As one would think the correct amount of Cu polishing is key to the Damascene process. Insufficient polishing would result in a layer Cu over the entire surface and massive line-to-line shorting would result. On the other extreme excessive polishing would remove the Cu in the etched channels. Between those two extremes there are subtler problems.

In the case of wide metal lines the Cu, which polishes quicker than the SiO_2, is dished out. The dishing results in a thinner conductor and higher resistance wiring. Additionally, the lack of planarity can lead to problems at higher metal levels. Dishing will also be present in areas of high local metal pattern density.

Wide spaces have a different problem. A residual TaN metal liner remains after the Cu polish. The subsequent liner polish is very selective to Cu and dishing of the oxide will result over wide spaces or areas of very low Cu pattern density. Again, the lack of planarity can lead to problems at higher metal levels.

The local metal density must be kept between limits that allow the process to work correctly. Not only would this be a very tedious task if done manually, it would greatly increase the data volume of the design and result in design checking problems. Therefore, the issue is resolved by using the hole and fill generation post process as explained in the next page.



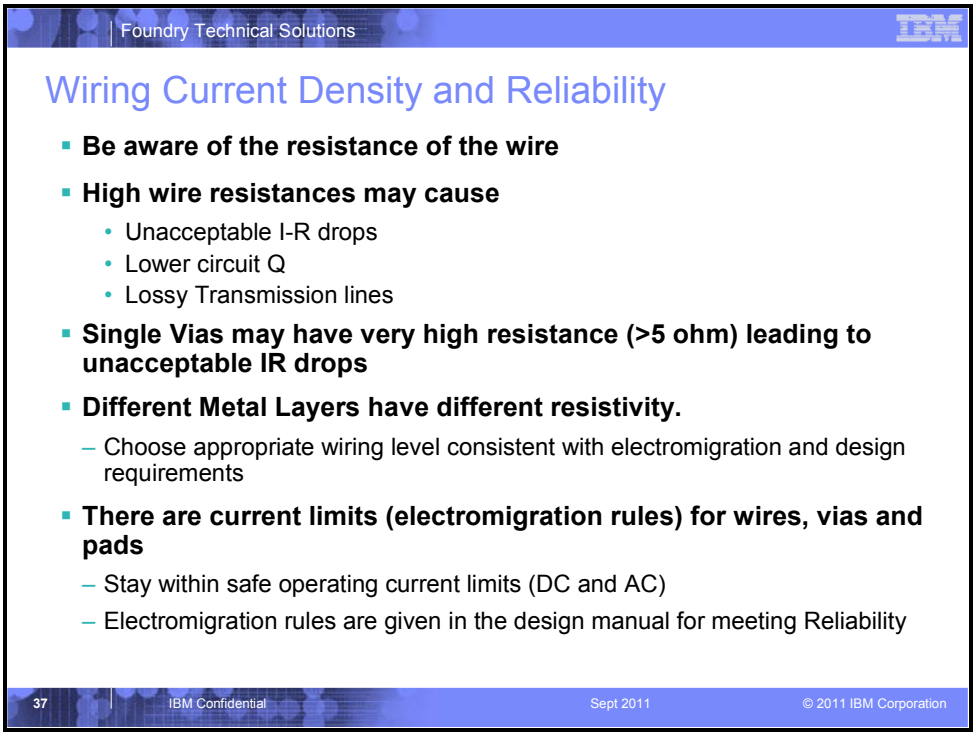


Metal Fill and Hole Generation

IBM adds fill to white space on a copper metal level to maintain the uniform local metal pattern density. The machine-generated shapes are placed on the reserved layer MxFILL.

Holes are subtracted from the large metal shapes to reduce the local pattern density. They are subtracted with some general guidelines shown in the diagram. IBM generated Metal HOLE shapes do not obstruct single vias or contacts, single rows of vias or contacts, or double rows of vias or contacts. For example, M1HOLE shapes are allowed to touch or intersect vias or contacts

directly above or below M1 if those vias or contacts are strictly redundant by virtue of their placement in the interior of an array of vias or contacts. Via hole generation is required for all copper via levels. VxHOLE shapes are used to remove from the design those few redundant vias that are covered or nearly-covered by a metal hole on the level immediately above..



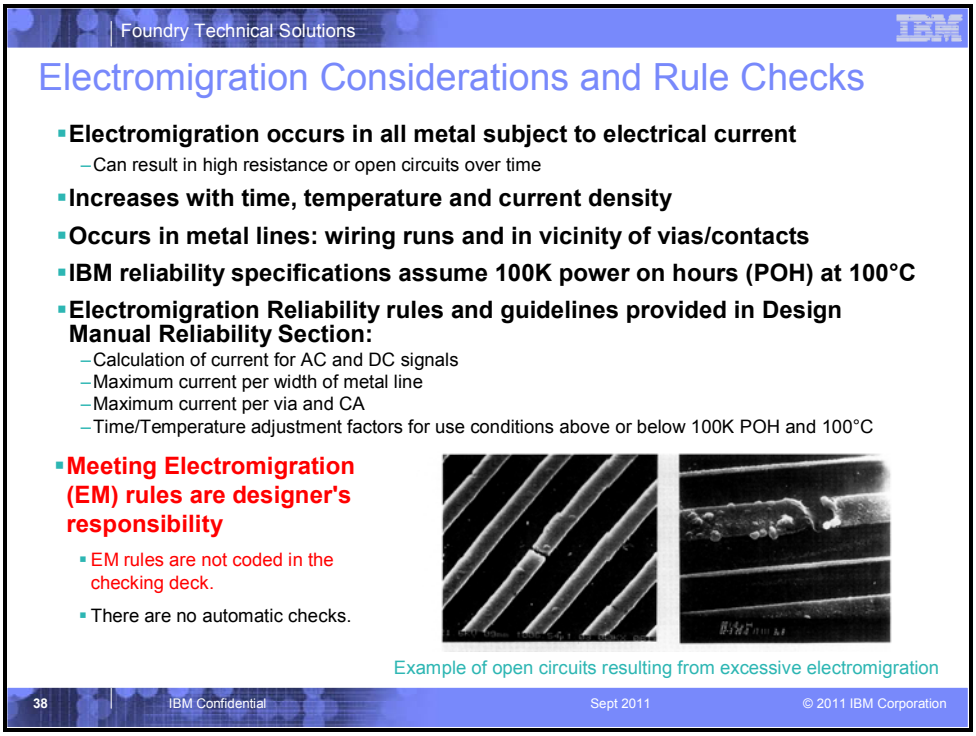
Wiring Current Density and Reliability

It is important to choose the appropriate wiring level.

High current densities in wiring can cause many problems. The first of these is simple voltage drops (I-R drops) due to the resistance of the wire. Even a small amount of resistance (<1 Ohm) has a profound effect on high-Q circuits such as resonators. Individual via resistance can be 5 Ohms or more. Long wiring runs or transmission lines can cause large signal loss if resistance is not controlled. Be aware that different metal layers have different sheet resistances.

There are current limitations (electromigration rules) for wires, vias and pads as described in the design manual to meet the Reliability requirements. These rules are not coded in the checking decks. It is the designer's responsibility that the electromigration rules are adhered to.

Electromigration is further described on next page.

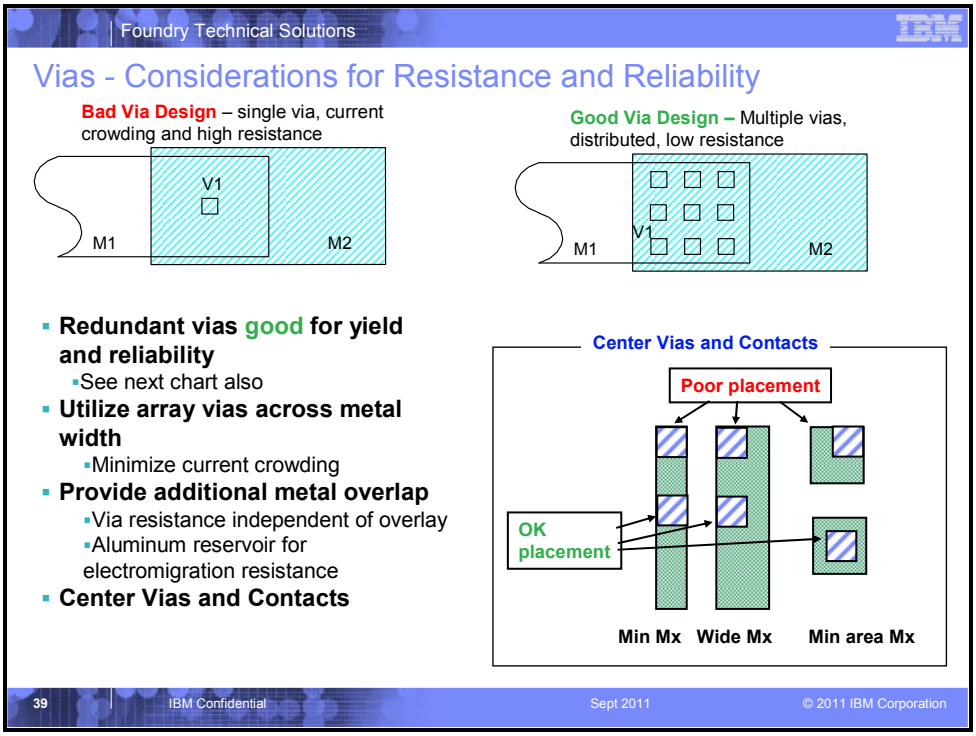


Electromigraton Rule Checks

As mentioned in the previous slide, the designers need to pay attention to the electromigration. There is no automated check to insure that metal wires have been adequately sized for the current they will carry, so it is up to the designer to know what currents are flowing in the circuit and insure that wires are large enough to carry those currents without failure.

Electromigration rules can be found in the Reliability section of the Design Manual. These rules take into consideration for the various adjustments for the temperature, the DC vs. AC current, and the specified operating lifetime of the design.

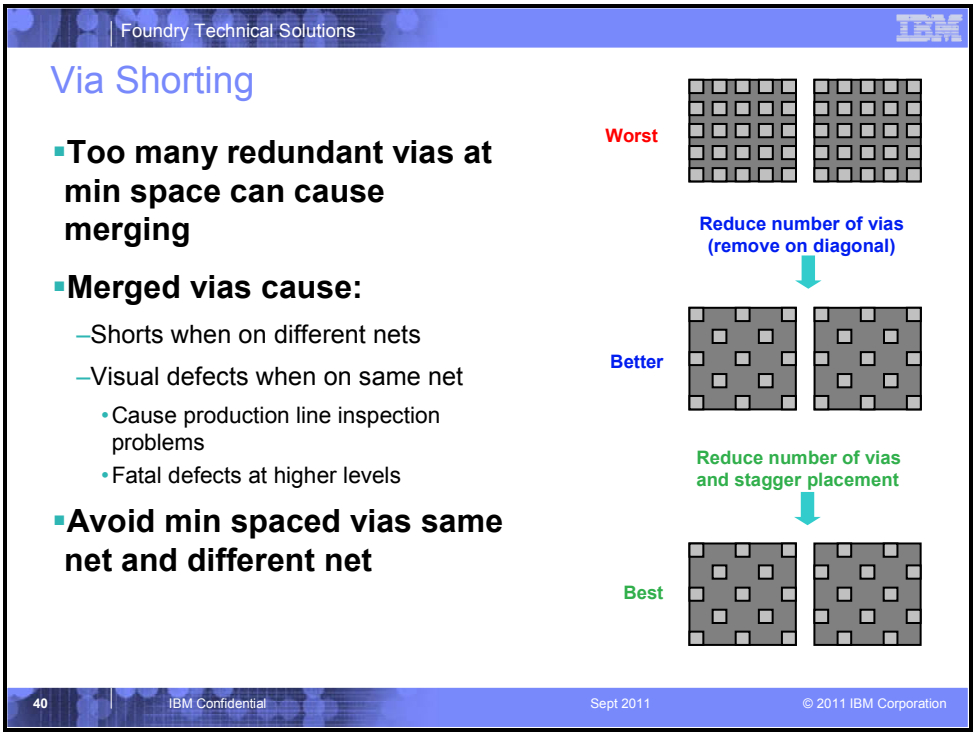
The rules are given for 100KPOH at 100°C. For other operating conditions, correction factors are also given in the Reliability Section of the Design Manual.



Via Considerations for Resistance and Reliability

Resistance of single vias is very difficult to control in manufacturing and the tolerance of via resistance is large. In analog designs, there is rarely a justification for using single vias, because there is usually enough space to place more. The configuration shown at the top of this slide demonstrates poor via design practice. The single via will exhibit current crowding and high resistance, and in addition, create an unnecessary yield risk. Resistance can be overlay-dependent when single vias are placed on minimum geometry lines

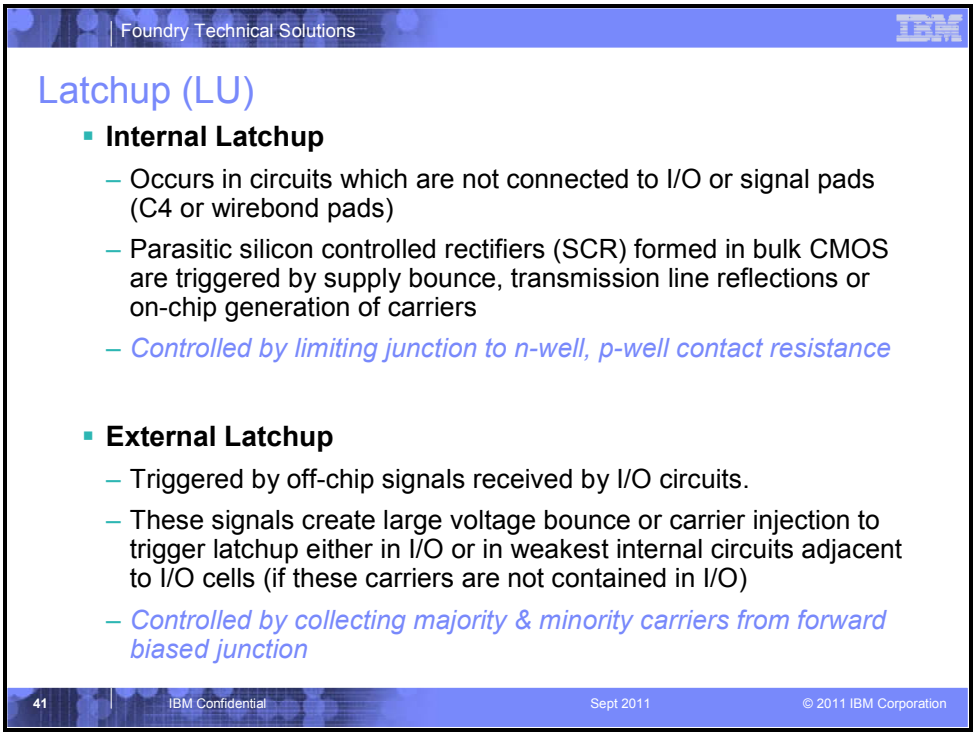
Centering vias is important to increase the likelihood that they land fully on the metal level above or below. The same is true for CAs. Metal lines will foreshorten and round due to photolithographic characteristics of the tools used to print these shapes. The example shown shows a real occurrence where foreshortening at M1 and a CA placed in the corner created an open circuit and a fatal defect.



Via Shorting

While it is in general good to use redundant vias, the use of via "farms" using many minimum-spaced vias often increases the chance of shorting vias and via visual defects. Typically, two or three redundant vias will suffice for low current density. Via farms risk shorting when they are placed minimum spaced to neighboring via farms. The diagram shows how deleting diagonal rows of vias reduce the number of vias by about one half. If the neighboring farms are reduced in a similar fashion and the nearest neighbor vias are staggered between the two nets, the best use practice is realized.

In addition to increasing the likelihood of fatal, shorting defects, tightly packed via farms can create visual defects if they are locally under-polished and leave residual liner material or Cu metal puddles. IBM uses in-line optical inspection tools to inspect for defects. They work by comparing the optical image of neighboring chips. Non-repeating liner or Cu puddles will be detected as defects. Cosmetic defects will be flagged as well as real, yield-limiting defects, sometimes driving extra processing or engineering intervention. Reducing cosmetic defects makes it easier to focus on real yield detractors.

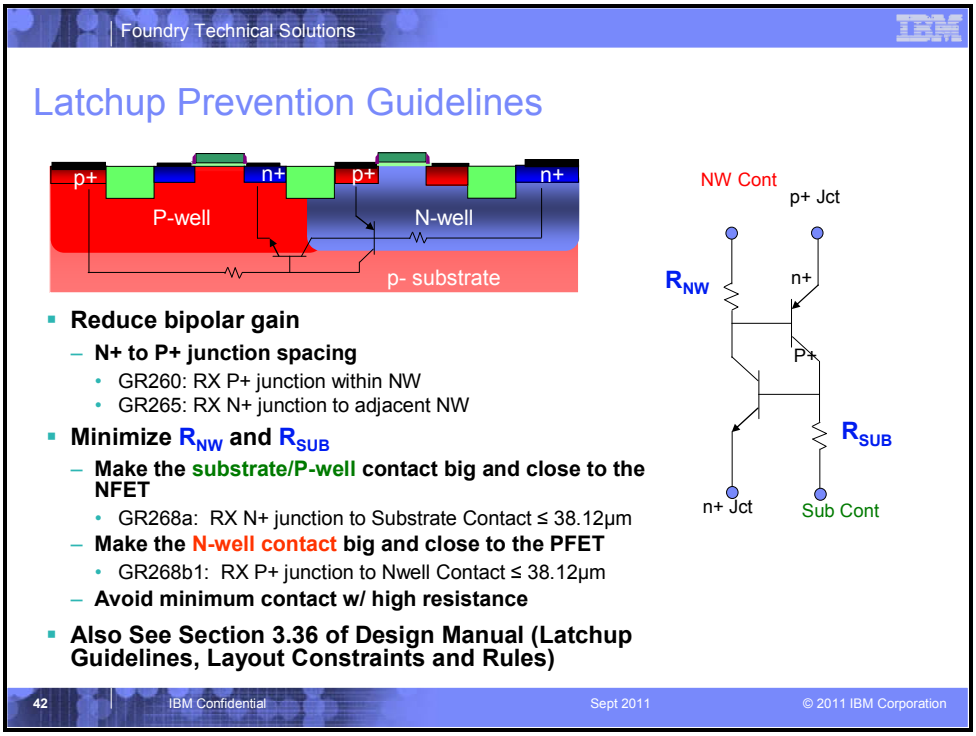


Latchup Prevention

Latch up is controlled by limiting the resistance between the base and the emitter of the parasitic bipolar devices and limiting the current that can flow through these resistors.

The Internal Latchup Rules limit the resistors by first defining a maximum distance between the diode and the p-well or n-well contact. The second criterion is the limit placed on the spreading resistance of the p-well or n-well contact. Ground Rules LUP09-12 use tiling to ensure that the area of the contact is commensurate with the possible sources of the current, such as the gate area where the source of the current is possible impact ionization.

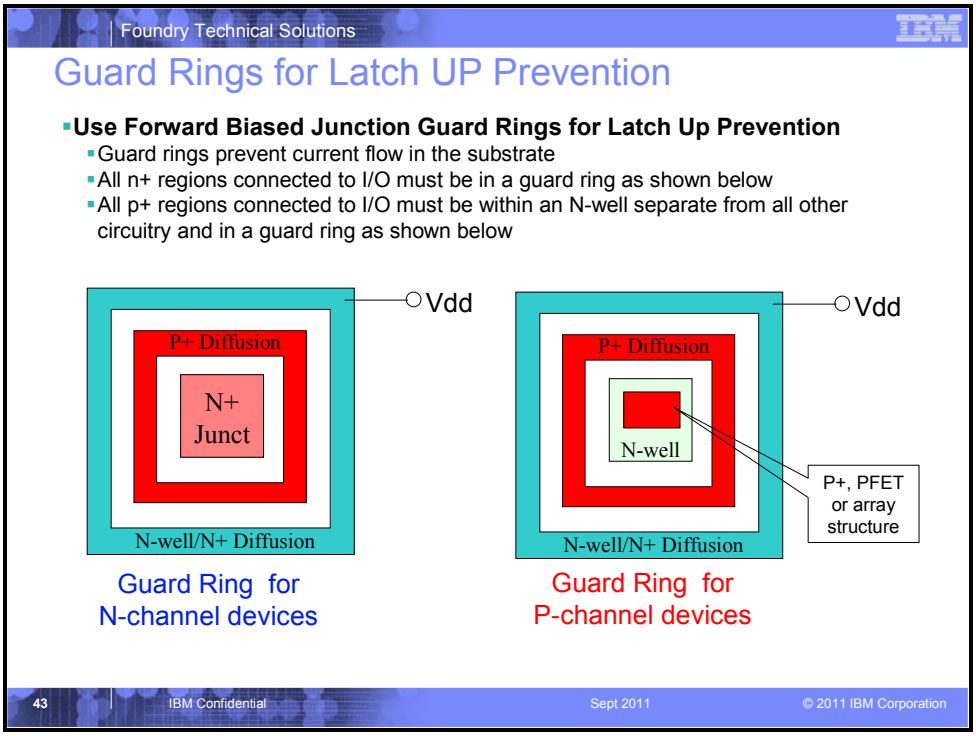
The External Latchup Rules recognize that in some circumstances diodes will be forward biased and minority carriers will be injected. These forward biased diodes are not only required to have a guard ring that will attempt to collect these minority carriers, but more stringent limits are placed on the Internal Latch Up rule of maximum distance from a p-well or n-well contact and a diffusion.



Latchup Guidelines

Latchup occurs when a parasitic pnpn device inherent in CMOS designs gets turned on by forward biasing of the source to substrate junction in an NFET or the source to N-well junction in a PFET. Limiting substrate resistance (and N-well resistance) plays a key role in latchup prevention. Contributors to substrate resistance include vertical resistances through the P+ diffusion region and horizontal resistance through the P substrate.

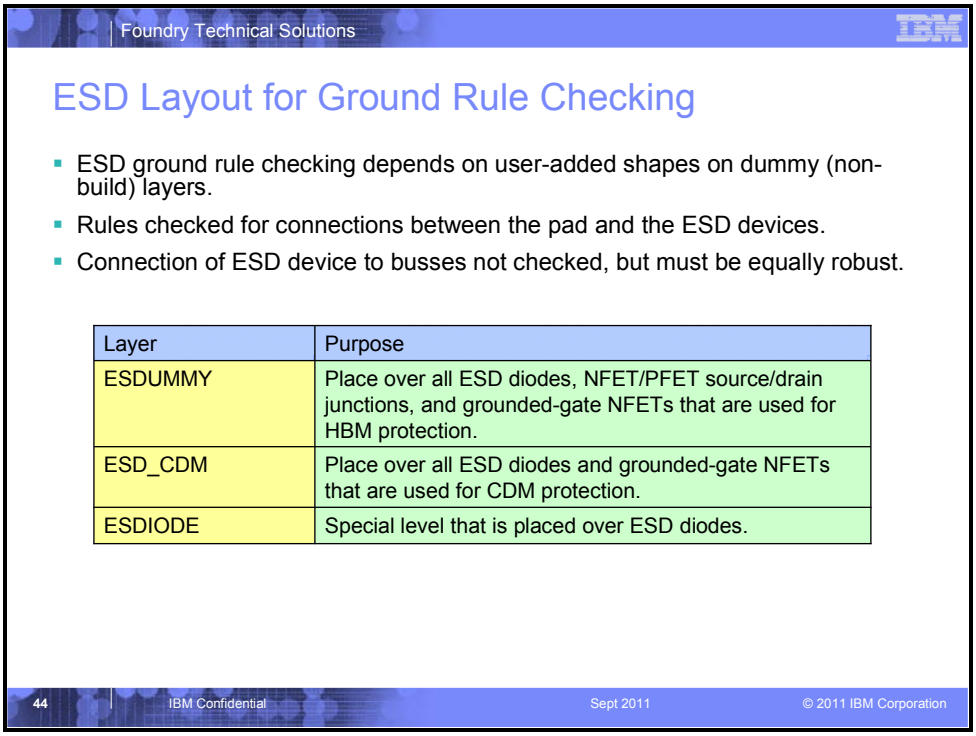
Layout rules addressing these resistances have been defined specifically to prevent latchup. These rules are prefixed with LUP and in some instances reference other layout rules in the Design Manual. Groundrule LUP02R, which controls the horizontal resistance by limiting the distance NFET devices and P+ substrate contacts is checked as GR268b. Even though groundrules LUP01R to LUP08R are denoted as “R” (recommended) rules they reference other groundrules and are in fact checked by the DRC deck. To minimize horizontal resistance, LUP02 and 04 address the distance between NFET devices and P+ substrate contacts. To minimize the vertical resistance the ratio of P+ substrate contact area to N+ source/drain area has been maximized. Similar rules exist for N-well contacts and P+ source drains.



Guard Rings for Latch Up Prevention

A part of latch up prevention is to construct guard rings around forward biased diodes to contain minority carriers. These are necessary whenever circuit transients may cause a p-n junction to become forward biased, such as signal or ground bounce on an off-chip driver or receiver. For example, signal bounce below ground on the drain of an NFET can forward bias the drain-substrate junction, causing electrons to be injected into the substrate. These carriers can cause latch-up, or migrate through the wafer to another device and be collected, causing leakage and FET threshold shift.

The N-well is biased to the positive supply voltage. The electric field in the N-well/Substrate junction is in the direction to collect electrons. The substrate contact ring insures that the local substrate potential is not raised substantially by the injection of electrons.



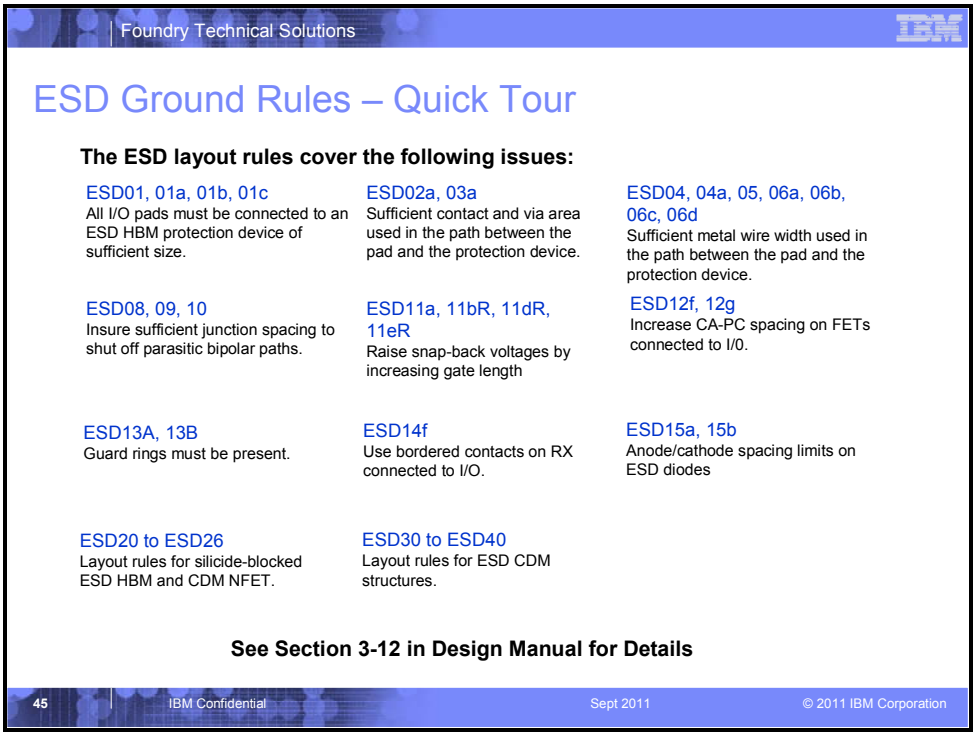
ESD Layout for Ground Rule Checking

ESD ground rules are coded in DRC decks. Ground rule checking depends on certain shapes and labels drawn on dummy, that is, non-build layers.

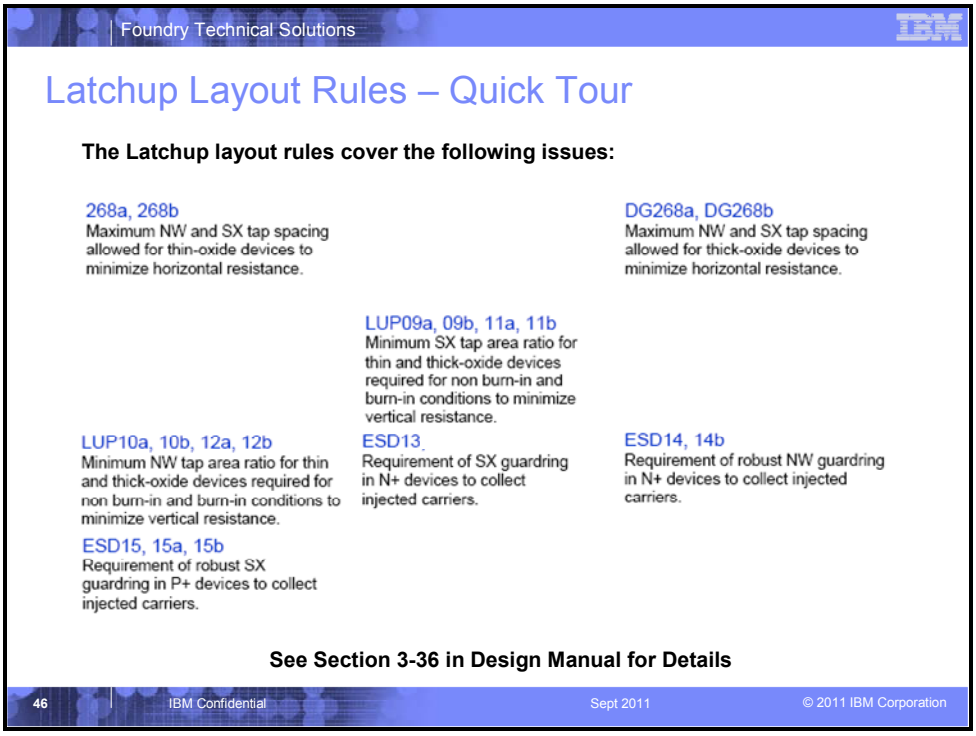
ESD diodes or grounded-gate NFETs that are to be used as HBM protection must be covered by shapes on level “ESDUMMY.” In the self-protecting strategy where the driver drain-to-well junctions are used as ESD diodes, the ESDUMMY shape should be drawn over those junctions.

Diodes or grounded-gate NFETs used for CDM protection must be covered by shape on level “ESD_CDM.”

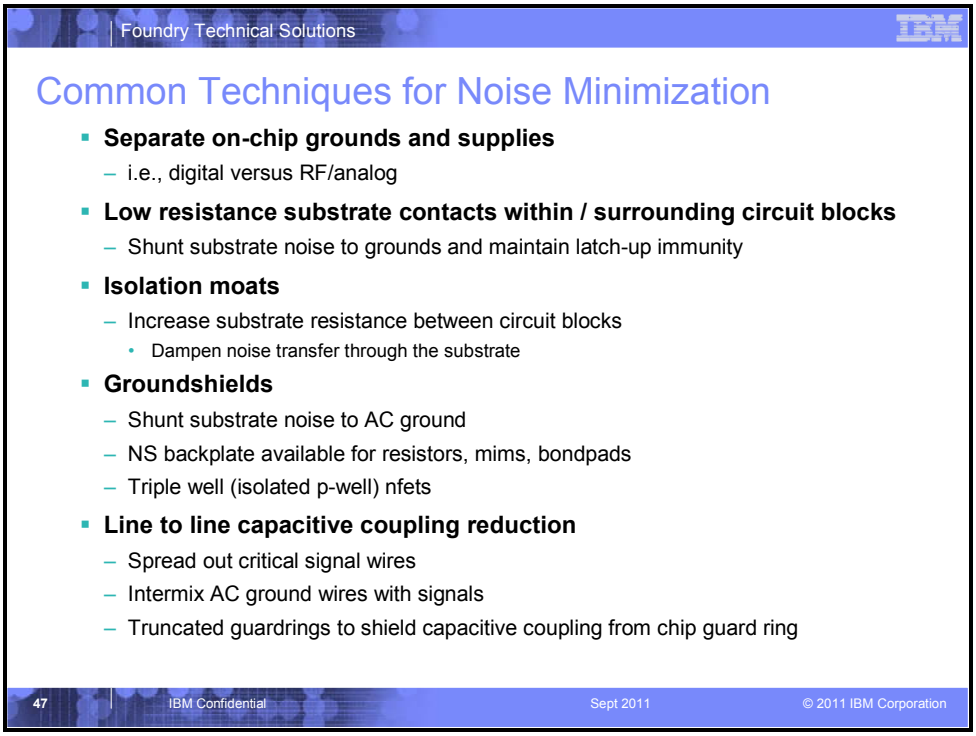
Also special level “ESDIODE” shape is requested for ESD diodes.



ESD Ground Rules – Quick Tour



Latchup Layout Rules – Quick Tour



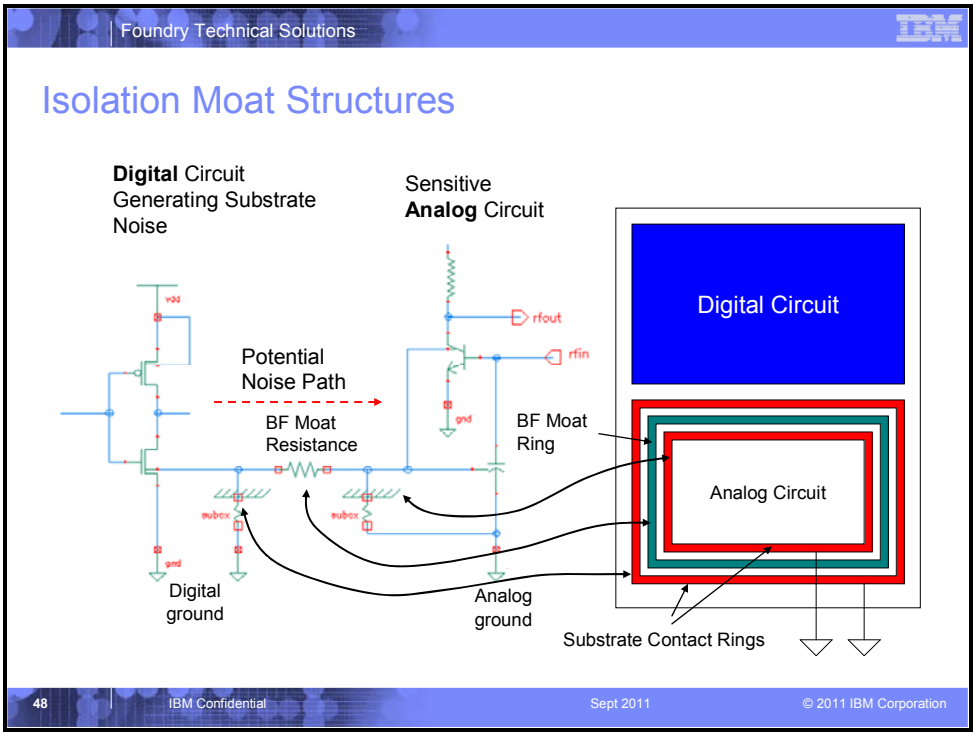
Common Techniques for Noise Minimization

There are many common techniques for minimizing noise on chip. Often the on-chip ground and supply voltages are kept separate between analog and digital circuit blocks in order to minimize noise. For robust electro-static discharge (ESD) protection, these ground and power supplies are isolated on chip through anti-parallel diodes, as described in the ESD section.

Within circuit blocks, strong contacting to the substrate is important not only to shunt substrate noise to the grounds, but also for latch-up prevention. Between circuit blocks, isolation moats are a way of dampening noise transfer through the substrate, discussed in the next two slides.

Ground shields are another way to shunt substrate noise away from devices such as resistors, mims and bondpads. Triple well NFETS have the bulk node isolated from the substrate by the buried n-type PI level. This is discussed briefly here.

To reduce capacitive coupling, space critical signal wires further apart, or separate them by ground or supply wiring. A truncated guardring is one example of using capacitive shielding for noise reduction shown here in a later slide.



Isolation Moat Structures

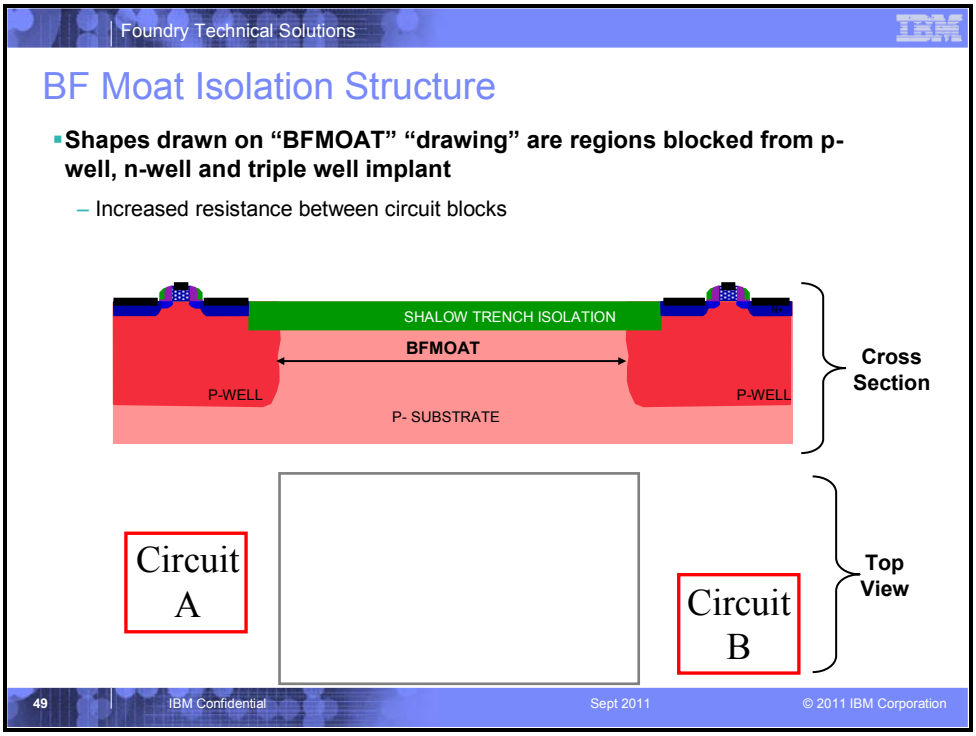
The purpose of an isolation moat is to place a region of high resistance between two circuits, or separate areas of the chip, to reduce noise or signal coupling through the substrate. This is shown in the conceptual circuit diagram on the left.

Digital circuits generate significant switching noise, which is coupled into the substrate through the source/drain junction capacitances, bulk terminals, and wiring. This noise signal can travel through the substrate, where it is introduced into sensitive analog circuits though various paths. Some examples shown here are resistor body terminals and the body connection of the NFET. The noise filter is constructed in the substrate as “pi” circuit with the shunt branches consisting of grounded substrate contact rings, and the series branch formed by a high resistance moat structure. The effectiveness is dependent on keeping the resistance of the shunt branches low compared to that of the series branch such that noise is shunted to the respective ground.

The appearance of the isolation structure on the wafer is shown in the diagram on the right. The red rings represent the substrate contacts, which are connected to ground or the negative power supply if the substrate is not at ground. The isolation moat is shown in blue between the two substrate rings. The next chart will describe how the moat is constructed to maximize the series resistance.

Other considerations associated with moat isolation are;

- Minimize number of signal lines crossing moat region
- Run lines on upper metal levels
  - Reduce capacitive coupling
- Separate supplies for quiet vs. noisy circuit blocks
- Insure adequate substrate contact within isolated regions

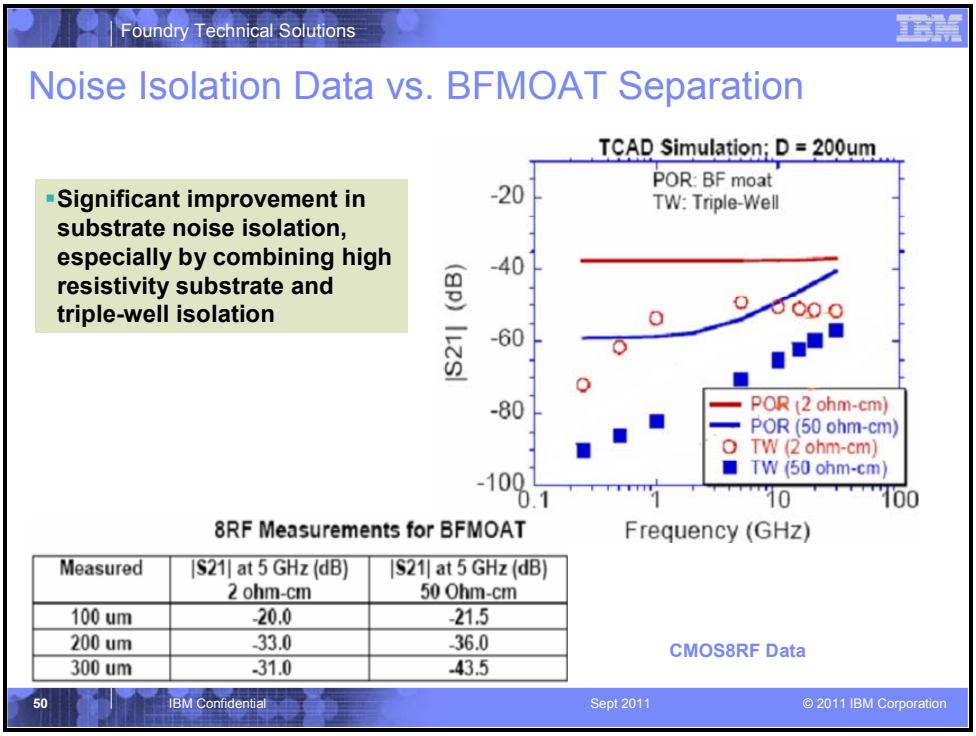


BF Moat Isolation

The process cross-section and mask levels of a BF moat structure are shown in this slide. The low-doped region is created using layer "OUTLINE" purpose "BFMOAT", which creates the p-well implant block shape on the BF lithography mask. The "BB" "drawing " also gets merged onto the BF mask level, but BFMOAT is preferred as additional rules appropriate for moat regions are checked.

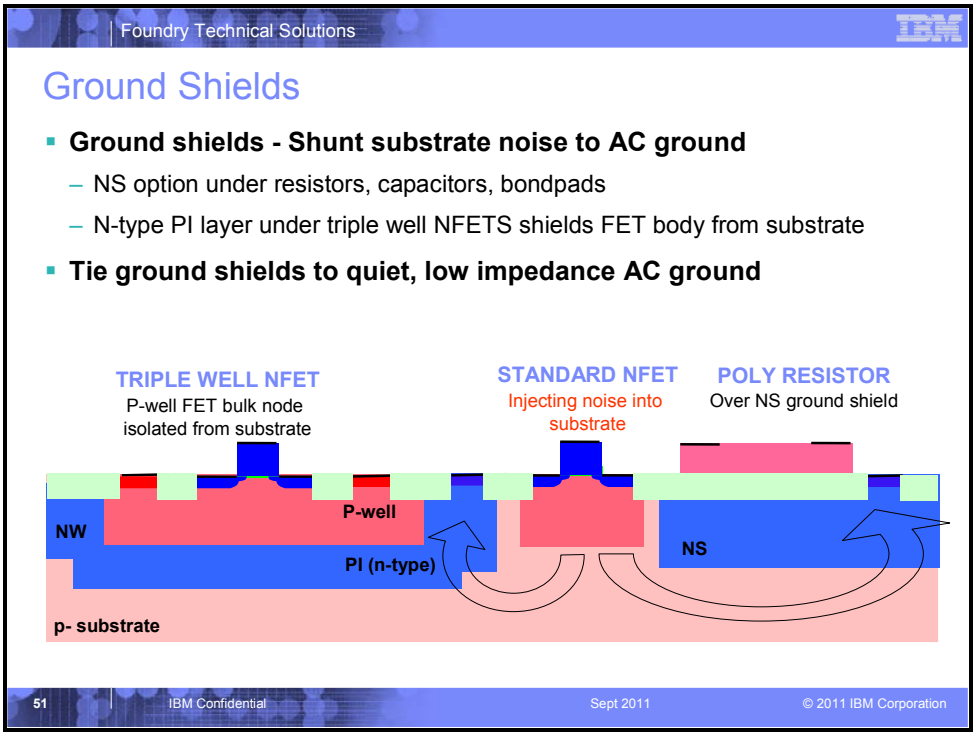
Without the p-well implants the P- wafer remains as the only conductive path through the substrate between circuits A and B. RX is prohibited in the moat region so the moat is covered by shallow trench isolation. In addition any M1 lines over the BFMOAT region must be tied to the chip's lowest DC potential. The RX fill algorithm is also adjusted in the BFMOAT regions to minimize its affect on isolation.

Some improvement in isolation is achieved by adding DT in or at the edges of moat regions, since it forces the current flow deeper in the p- substrate.



Measured	|S21| at 5 GHz (dB) 2 ohm-cm	|S21| at 5 GHz (dB) 50 Ohm-cm
100 um	-20.0	-21.5
200 um	-33.0	-36.0
300 um	-31.0	-43.5

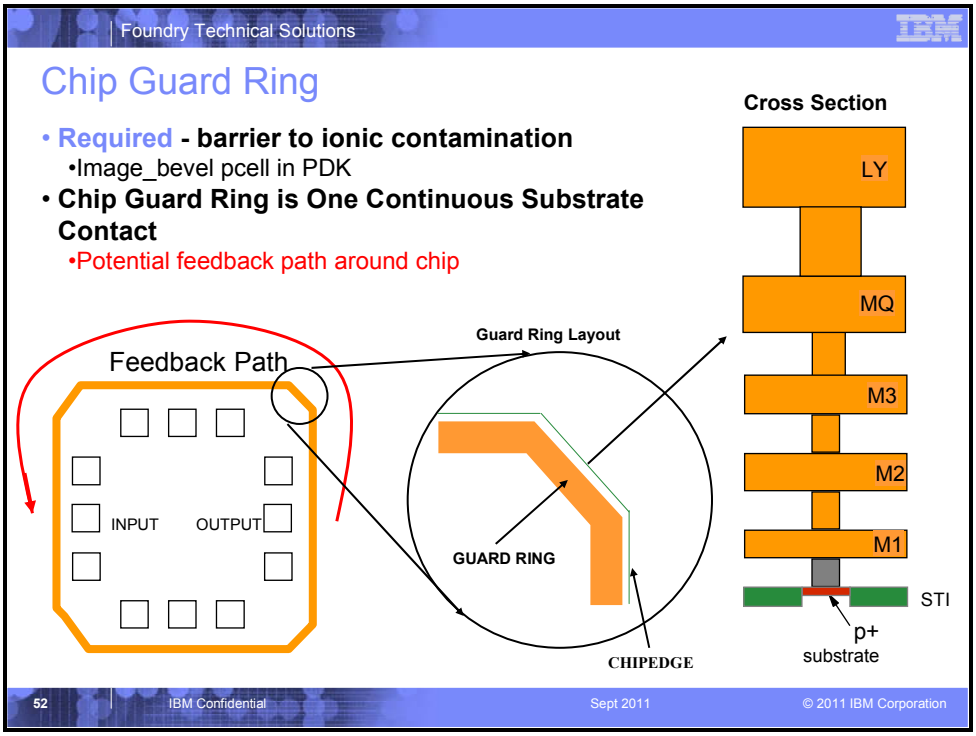
BFMOAT Noise isolation Data



Ground Shields

Ground shields are another method to shunt substrate noise away from critical devices or circuits. Many devices such as resistors, capacitors and the bondpads are offered over a n-type (N-subcollector) ground shield. The deep buried n-layer (defined by PI mask) of the triple well NFETs acts as a ground shield as well. Substrate noise can capacitively couple to the n-type shielding layer across the junction, but is then shunted to the supply to which the shield is tied.

In the example shown above, noise is injected into the substrate by the standard NFET, but the bulk node of the triple well NFET and the body of the poly resistor are shielded from the noise.

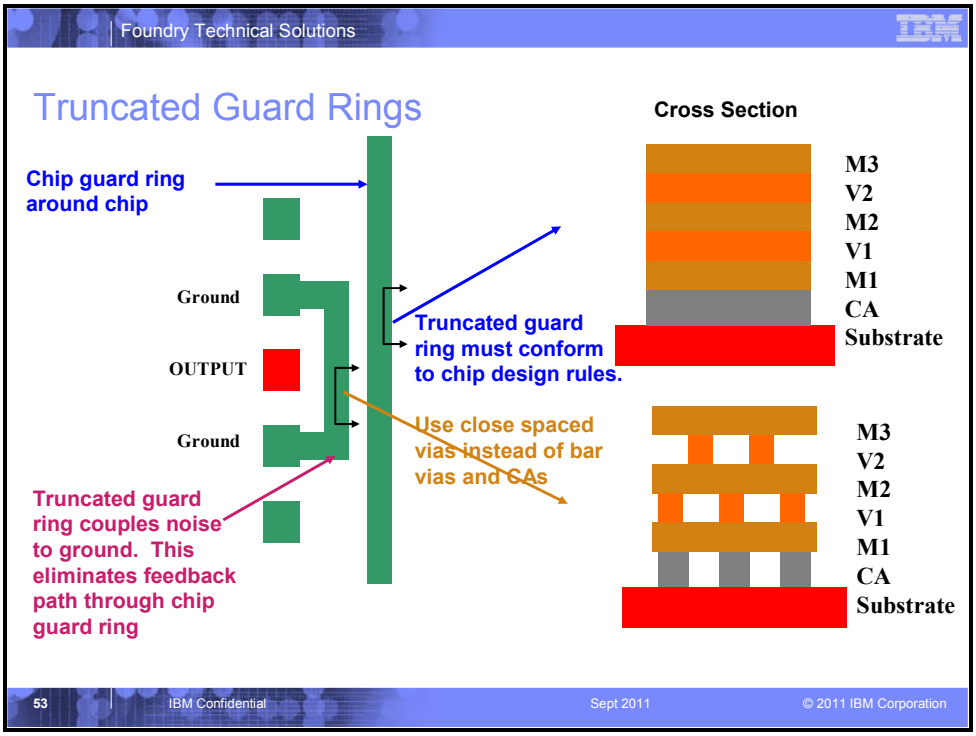


Chip Guard Ring

The chip guard ring, also called the substrate ring, is required to enclose the entire chip. It forms a barrier to the ingress of ionic contaminants, which are quite mobile in silicon dioxide, by surrounding the die with a wall of metal.

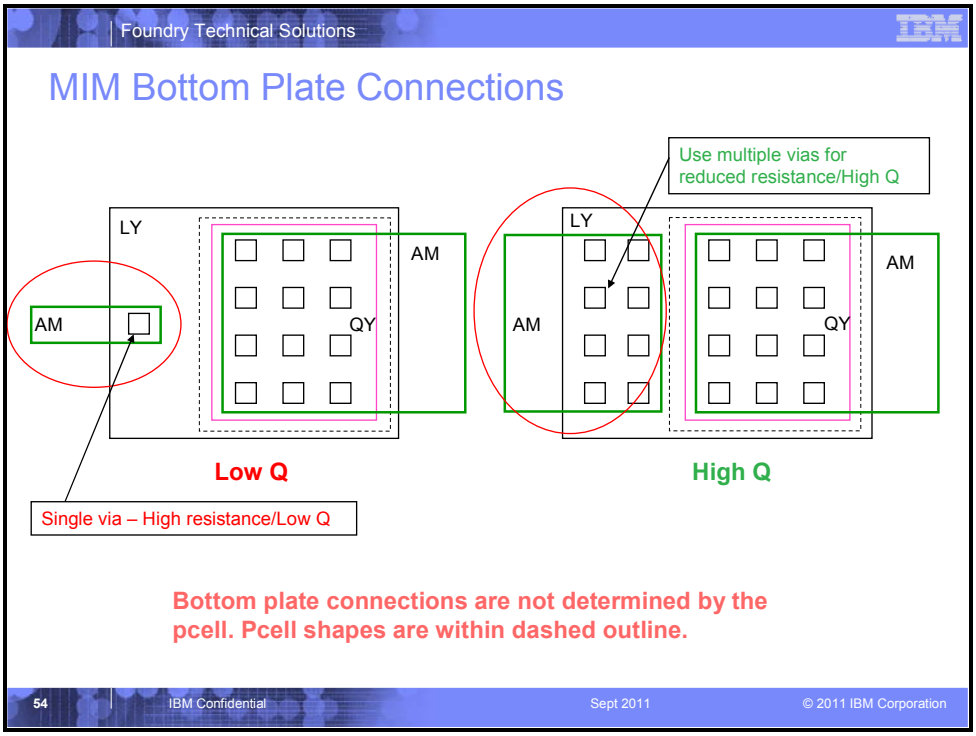
The cross section at right shows the layers that make up the guard ring in BiCMOS8HP technology. A ring of silicided P+ diffusion is placed at the edge of the die. The ring itself is composed of vertically stacked metal wires connected by continuous bar vias. This is the only place where the ground rules allow continuous bar vias as opposed to square vias. The metal ring is connected to the substrate through a continuous substrate contact ring.

Be aware that the chip guard ring can conduct signals or noise from one part of the die to another. As illustrated, this may form an unanticipated feedback path for high-gain circuits. Nevertheless, because of its importance for long-term reliability, the chip guard ring is required in all designs. Shielding methods must be used to isolate signals from the ring where necessary.



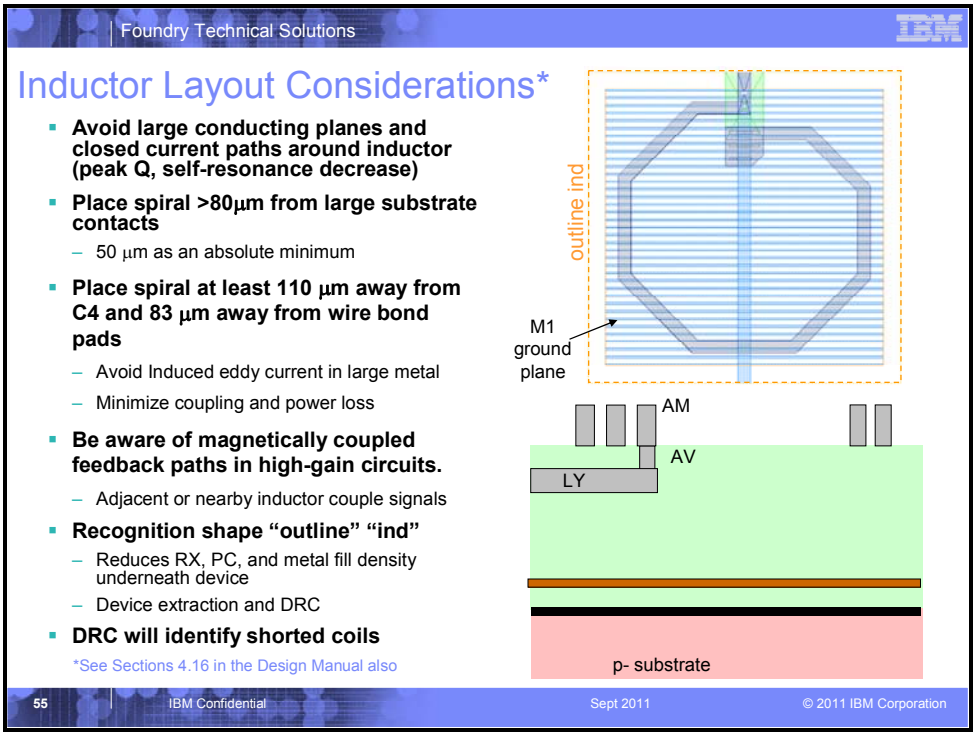
Truncated Guard Ring

One possible shielding arrangement to prevent coupling to the chip guard ring is to interpose a truncated guard ring between the circuit and the actual chip guard ring. In this case, the truncated ring would conform to ground rules by using multiple square vias at minimum pitch instead of full-length bars as allowed in the chip guard ring. If the truncated ring is provided with a good low-inductance AC ground, signal coupling to the main chip guard ring will be reduced.



MIM Bottom Plate Connections

MIM bottom plate connections require attention to insure that the capacitor Q is not compromised by too few vias. In the chart above, the pink squares represent the upper capacitor plate. The bottom plate is black, and the AM connections green. The IBM pcell places the vias connecting the top MIM plate (QY) to AM. The designer must make the connection from the bottom plate (LY) to the AM connection. It is possible to do this using only one via, as on the left, but this places a significant resistance in series with the capacitor. Good design practice, as on the right, uses multiple vias to keep the series resistance low.



Spiral Inductor Layouts

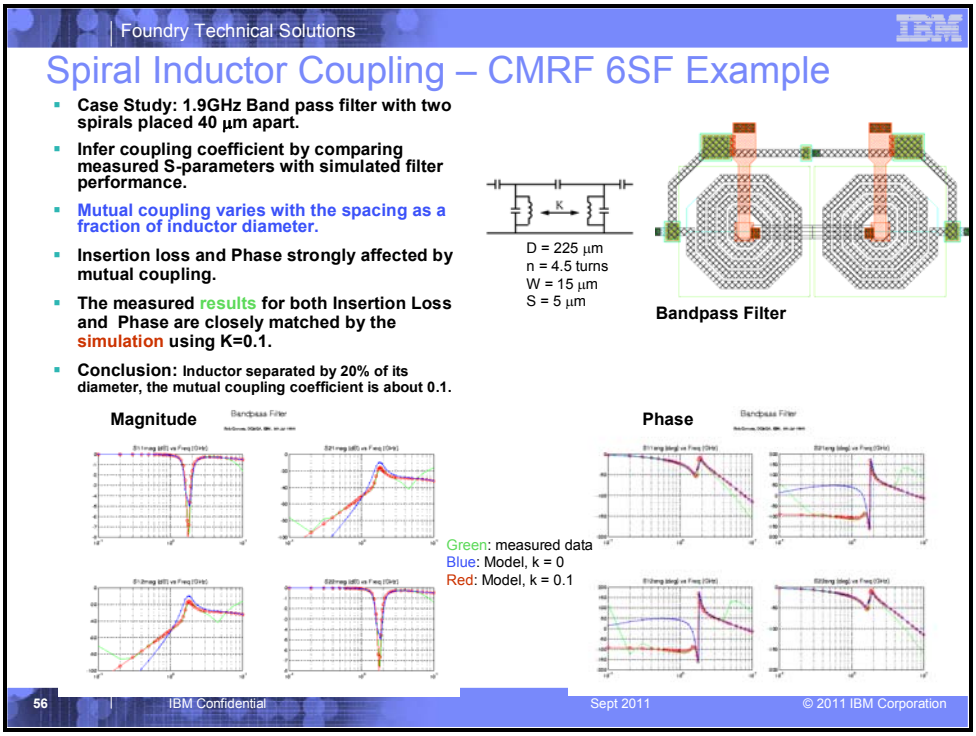
Spiral inductors depend on good layout practices in order to achieve good correlation between simulation and actual circuit performance.

Do not surround inductors with electrically continuous rings of conductive material such as wires, polysilicon, or diffusion (RX). The inductor magnetic field will induce current flow in the ring and cause lower quality factor and lower inductance.

Keep inductors at least 80 µm away from substrate contacts. Large area substrate contacts in close proximity increase power loss through enhanced substrate coupling. 80 µm is the recommended spacing. 50 µm is the absolute minimum. The degree of concern increases with the total area of the contacts.

Inductors can induce eddy currents in large metal features such as wirebond pads and C4 bumps. Separate inductors from these structures when possible (Section 4.11.2 and 4.11.3).

Adjacent or nearby inductors will couple signals. In high-gain circuits this effect can produce significant un-modeled feedback and cause circuit performance to deviate from predictions.



Spiral Inductor Coupling – 6RF Case Study

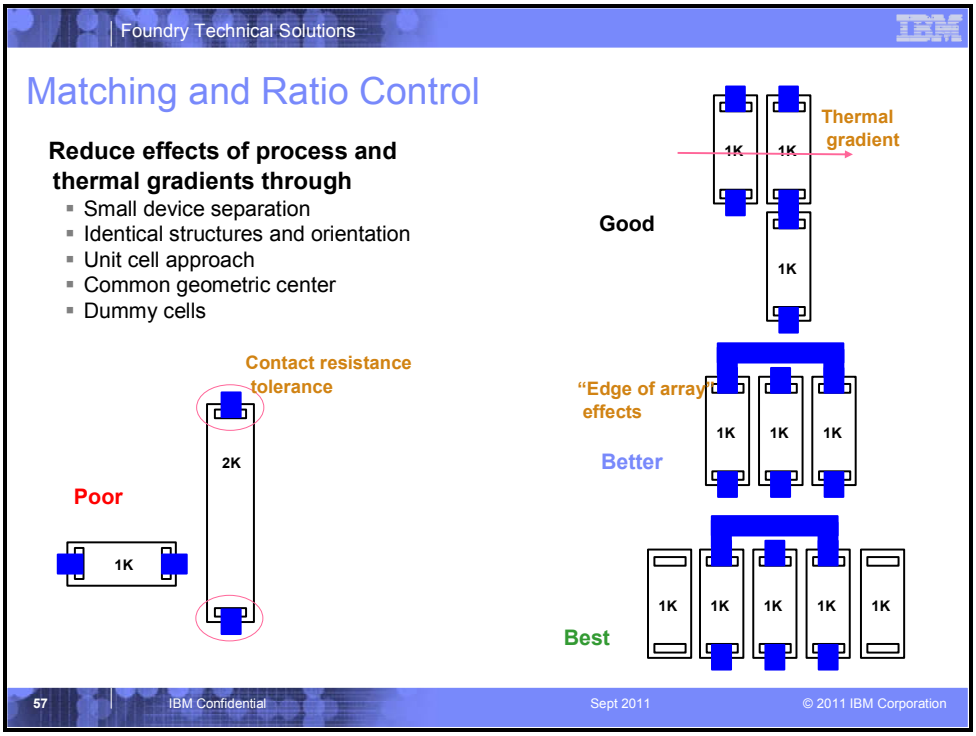
Spiral inductor coupling has not yet been systematically characterized but some important insight can be gained by a particular case study. In this experiment, two inductors that were elements of a 1.9 GHz band-pass filter were placed 40 µm apart. The S-parameters of the filter were measured and compared to the simulated performance with the mutual coupling left as a simulation parameter. This example is from the CMRF 6SF technology where hardware measurements exist.

The inductor outer diameter was 225 µm with a wire width and spacing of 15 and 5 µm respectively. The inductors had 4.5 turns.

To estimate mutual coupling, the dimension of interest is the spacing as a fraction of inductor diameter.

Magnitude of the measured and simulated bandpass filter S-parameters, |S11|, |S12|, |S12|, and |S22|, are shown on the bottom left figure and Phase S-parameters, ∠S11, ∠S12, ∠S12, and ∠S22 in the right side of the bottom. The green line is the measured data, blue shows the simulation results assuming that the inductors are uncoupled, and red shows simulation results with an assumed coupling coefficient of 0.1. Both Insertion loss and phase are strongly affected by inductor coupling. Note that the measured results are closely matched by the simulation using K=0.1.

The conclusion: When inductors are separated by 20% of the inductor diameter, the mutual coupling coefficient is approximately 0.1.



Matching and Ratio Control

Non-uniformities within a chip are unavoidable in semiconductor processing. These take the form of feature size differences due to lithography and etch processes, conductivity gradients due to hot process steps such as thermal anneals and oxidations, and thickness differences due to polish non-uniformity. In addition, the thermal distribution across the chip during operation will cause mismatches in device behavior.

With good layout practices, the effect of these non-uniformities can be minimized. Device matching statistics in the Monte Carlo simulation tools assume that good design layout practices have been followed. When devices must be matched or have fixed ratios, these practices must be followed if the hardware variability is to be accurately represented by the model statistics.

Good matching and ratio control are achieved by keeping matched devices very close together (adjacent if possible), placing groups of devices around a common geometric center, orienting devices in the same direction, placing devices in identical surroundings, and using identical device layouts.

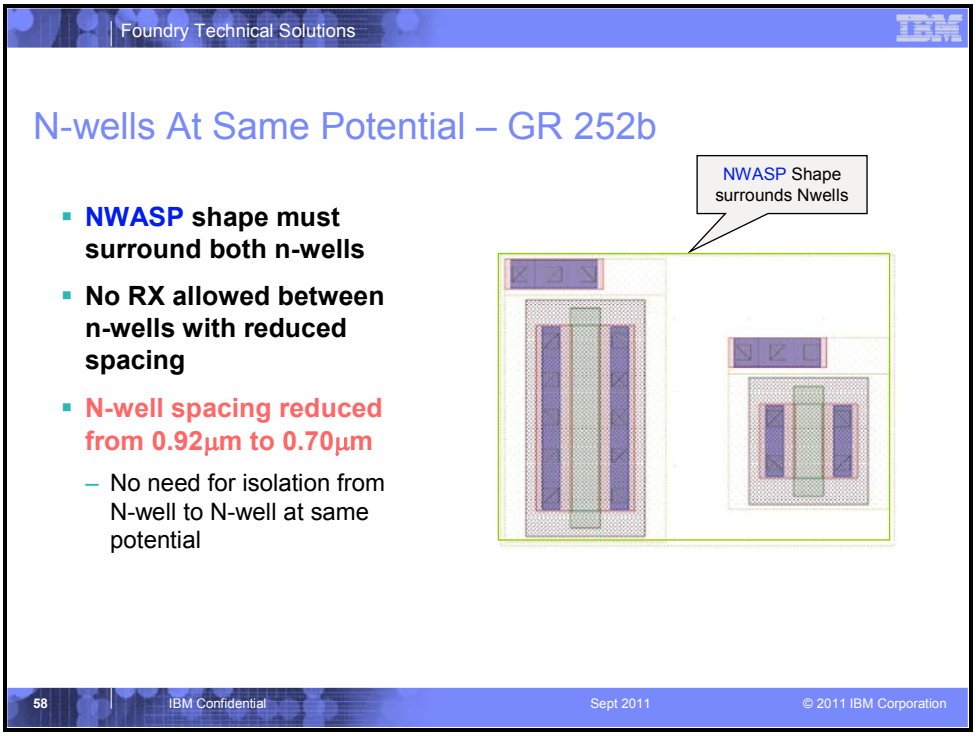
The slide above shows four examples of a design that intends to create a resistance ratio of 2:1. The design on the upper left is poor. Consider the result if the end and spreading contact resistance increases by ΔR_e due to process variation. The 1KΩ resistor would increase by $2\Delta R_e$. The 2KΩ resistor would also increase by $2\Delta R_e$ while the desired increase to maintain the 2:1 ratio would be $4\Delta R_e$. The second problem with the layout is that a thermal gradient from left to right would cause one resistor to shift more than the other.

The most effective layout will use unit cells to achieve the design ratio required. Place three identical unit cells, and then wire two of them in series to form the larger resistor as shown in the design on the upper right of the chart. All devices should have the same orientation to insure that they print as identically as possible during the lithography process.

A common centroid approach will provide some immunity to thermal or process gradients on the wafer. This layout is illustrated in the middle right of the chart. Gradient effects will be averaged out of the 2KΩ resistor because half of the resistance is on each side of the 1KΩ resistor.

This unit cell approach leads to an array of devices. The fabrication process will always result in the devices on the edge of the array being slightly different from those in the center. Placing dummy devices on the edges of the array will keep these “edge of array” effects away from your circuit. This is shown in the layout in the lower right. Using pattern fill near critical structures can reduce edge effects further.

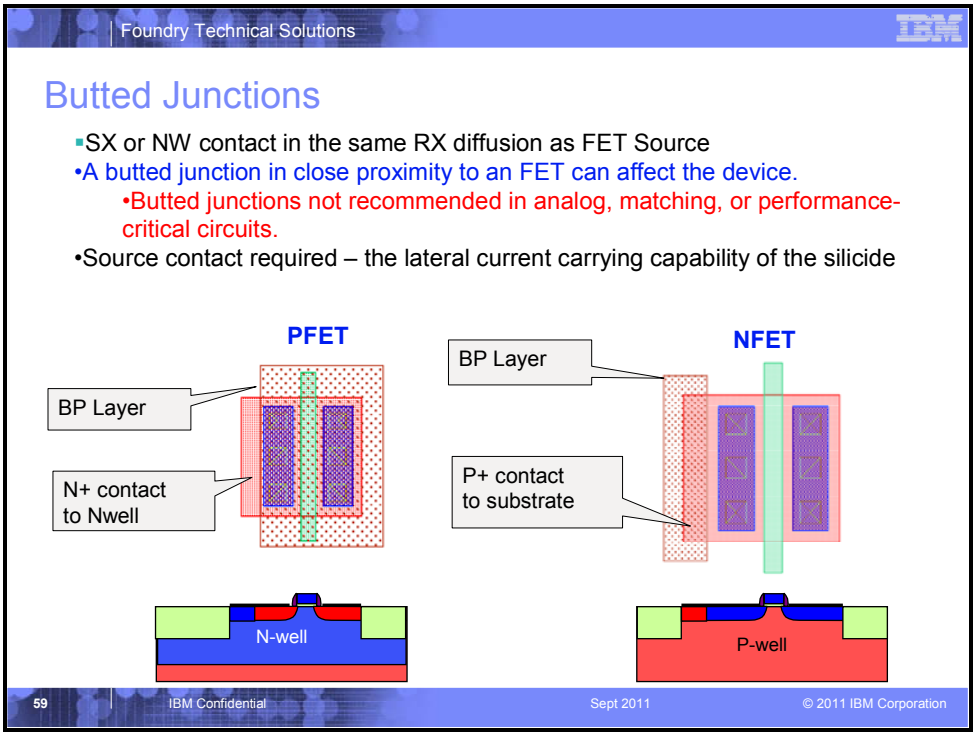
If wiring capacitance must be matched, place the critical wiring in areas having similar surrounding metal density. The wiring insulator is deposited, and then mechanically polished flat. Therefore, it is thicker over areas where there is a lot of metal density than it is over a small isolated wire. Pattern fill can be used to insure that metal coverage is similar in areas where capacitances must be matched.



N-wells at Same Potential

When adjacent N-wells are at the same voltage there is not a requirement for isolation from N-well to N-well and the space may be reduced. In order for the ground rule checking program to recognize this situation a utility level “NWASP” “DG” is drawn such that it totally surrounds both N-wells that are being checked for ground rule GR 252b.

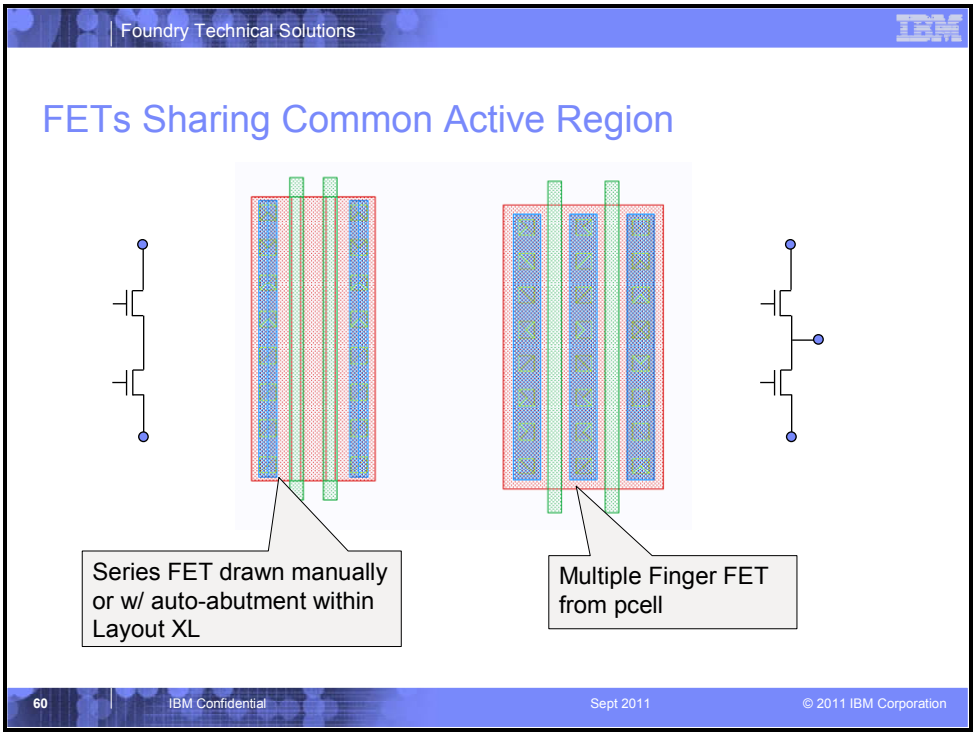
No RX may be placed between the two n-wells when using the NWASP feature.



Butted Junctions

Butted junctions, where a well or substrate contact and the source of a FET are formed in the same RX active shape, are allowed in BiCMOS8HP (Section 3.6 Design Manual). **However, a butted junction in close proximity to an FET can alter the characteristics of the device. Therefore, the use of butted junctions is not recommended in analog, matching, or performance-critical circuits.**

Contacts are required on the FET source portion of the butted contact diffusion, and are optional on the well or substrate side of the butted contact diffusion. The figures above show contacts to only the source portion of the butted contact diffusion. The FET source contact requirement arises from electrical and reliability concerns associated with the lateral current carrying capability of the silicide when it bridges n-type and p-type diffusions.

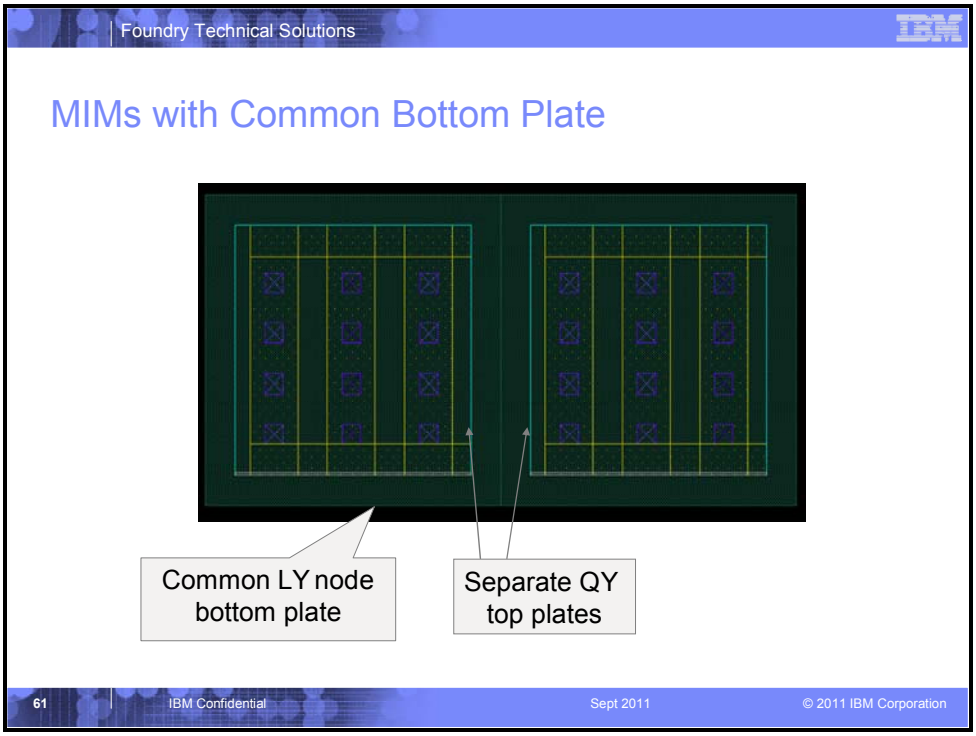


FETs Sharing Common Active Region

Multiple NFETs or PFETs may be formed within a single active region, as shown above. The multi-fingered FET device shown below is fully supported through the layout Pcells. Contacts are provided and the common sources and drains may be wired directly.

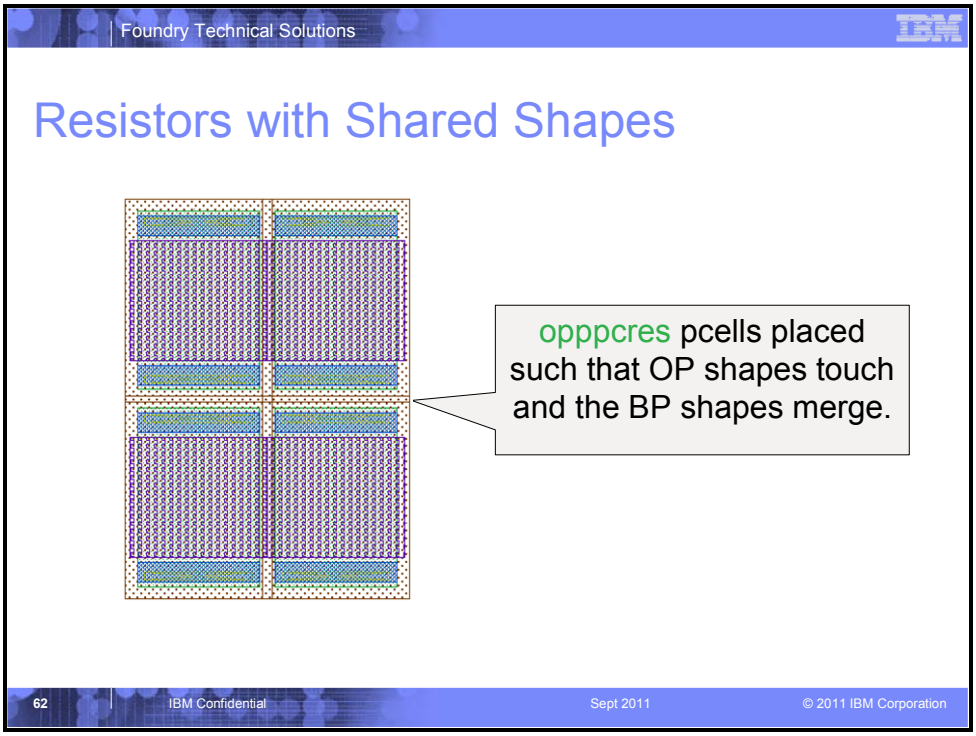
The series FET on the left side of the chart was created using the Cadence auto-abutment capability within Layout XL.

The device on the right demonstrates how the multi-finger layout pcell can represent two FETs in the schematic.



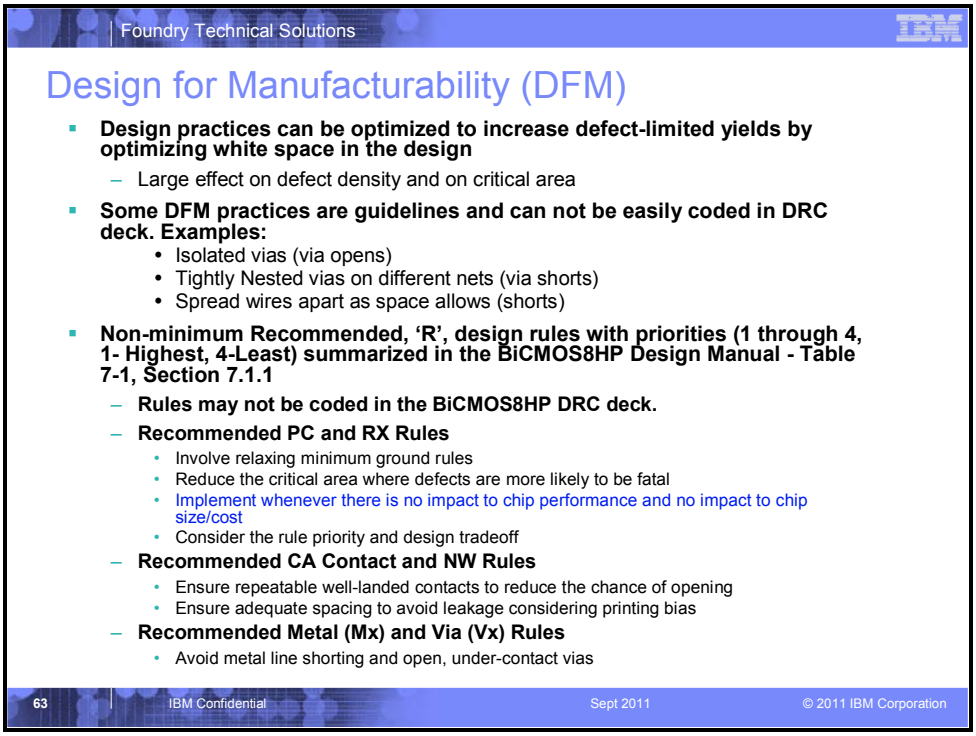
MIMs with Common Bottom Plate

Significant area savings can be realized for circuit applications where the bottom plates of the MIMs share a common node. A larger LY shape can be manually added to multiple placements of the MIM capacitor, avoiding the need to wire to each MIM bottom plate individually. The above figure was constructed by placing 2 MIM pcells, with abutted LY.



Resistors with Shared Shapes

An array of polysilicon resistors may be instantiated in a compact fashion by sharing the OP and BP shapes. In the example above the resistors were designed with their OP shapes touching and the BP shapes merging. This technique is applicable with either a sub or BB backplane. If the common resistor area layout requires separation on the OP and BP levels for specific resistors the BB level may either overlap, abut or be filled to reduce overall area requirements.



Design for Manufacturability

The following pages describe some practices that can be used to optimize product yield and thereby reduce chip cost. Defect-limited yield is one key driver in overall chip yield and layout practices can have a large effect on defect density and on critical area where defects are more likely to cause serious failures.

The most straightforward means of reducing critical area and defect density is to follow the recommended "R" rules in Table 144 in the BiCMOS8HP design manual in Section 7.1.1. These rules were compiled by the manufacturing organization. They are drawn from a long history of dealing with defects in this and in older technologies. They have been categorized with priorities 1 through 4. Priotiy 1 has most impact on yield and priority 4 has the least. Other less obvious guidelines should be given careful attention. These recommendations can not be coded in the DRC deck.

Recommended 'R' PC and RX Rules

In general, the recommended 'R' PC and RX rules involve relaxing minimum ground rules. This reduces the critical area where defects are more likely to be fatal. These rules predominantly make shorting less likely between RX-to-RX, RX-to-PC and PC-to-PC structures. These rules will grow device, and possibly chip size. These rules should be implemented whenever there is NO IMPACT TO CHIP PERFORMANCE and NO IMPACT TO CHIP SIZE/COST. The list prioritizes the rules so that designers can manage which 'R' rules to follow and which to trade off if device size grows unacceptably by following all the rules.

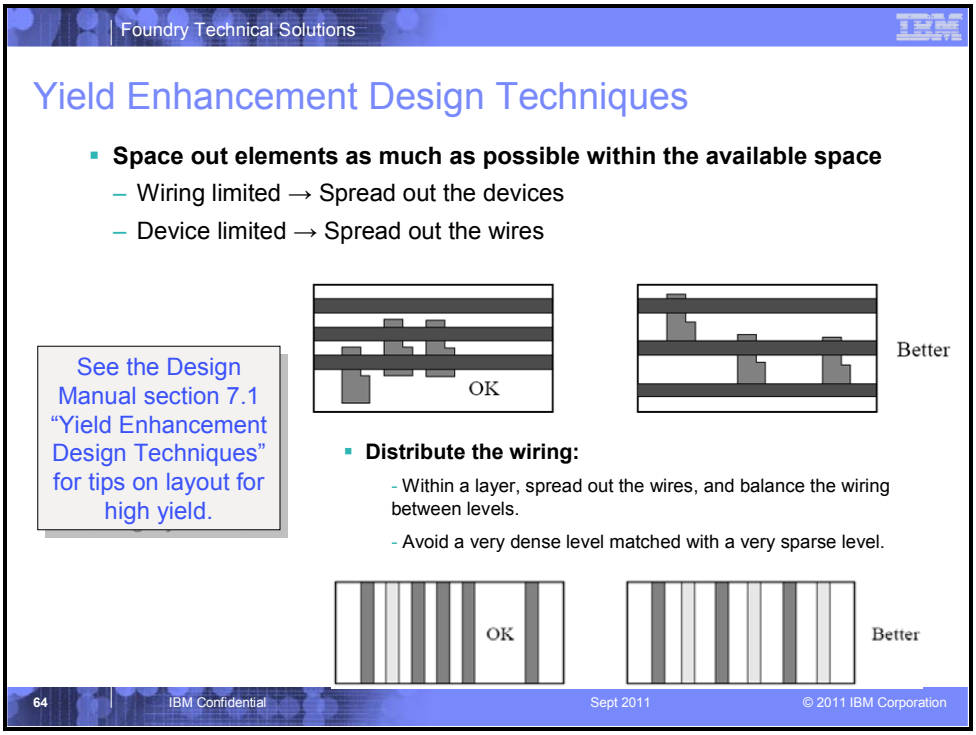
Recommended 'R' Contact (CA) and NW Rules

Where the RX and PC rules generally relax minimum spacing to reduce the chance of shorting, the CA contact recommended rules are to ensure repeatable, well-landed contacts to PC, RX or M1 shapes. If a CA is not well centered and only partially overlaps with the shape above or below high contact resistance can result or reduced yield due to open contacts.

The N-well spacing rules are to ensure adequate distance between N-well to N+ regions and substrate to P+ regions. Leakage between them can occur if they get too close and this can affect chip yield. Printing bias of large shapes is different than for small shapes. Larger N-well shapes will tend to be larger and spacing to P+ and N+ needs to be adjusted to account for the bias. The N-well 'R' rules address this phenomenon.

Mx and Vx 'R' Rules

The Mx and Vx rules apply to metal levels and via levels. They help avoid shorting between metal lines and open, under-contacted vias. In particular, shorting between lines becomes more likely when the lines are wide and with minimum spacing to neighboring lines. Print biasing and local non-uniformities during CMP increase the chance of shorting.

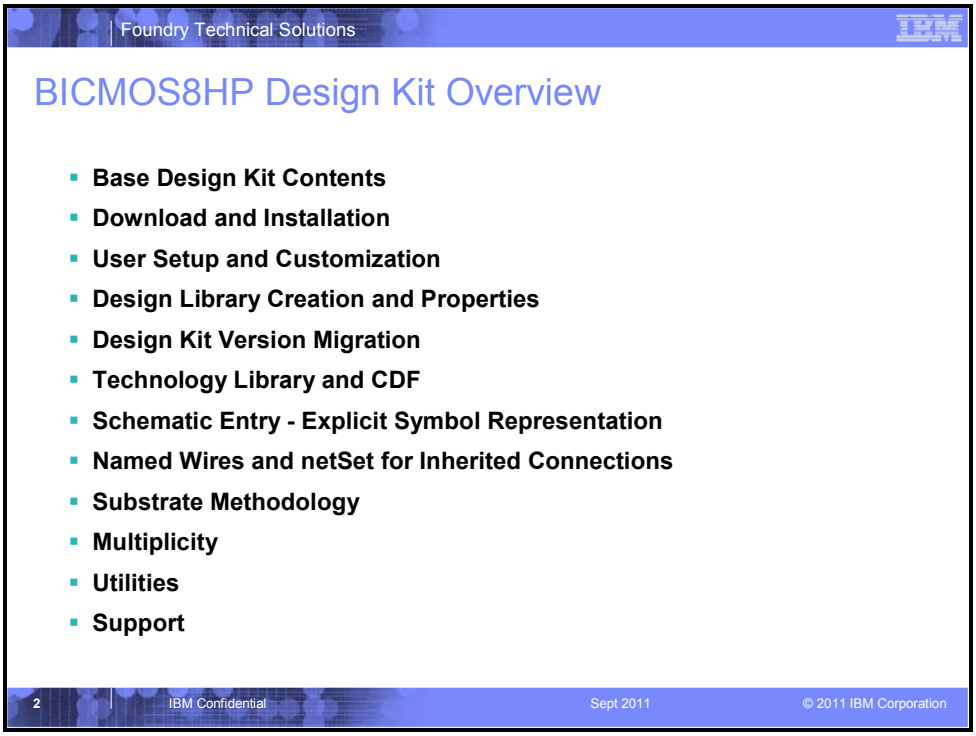


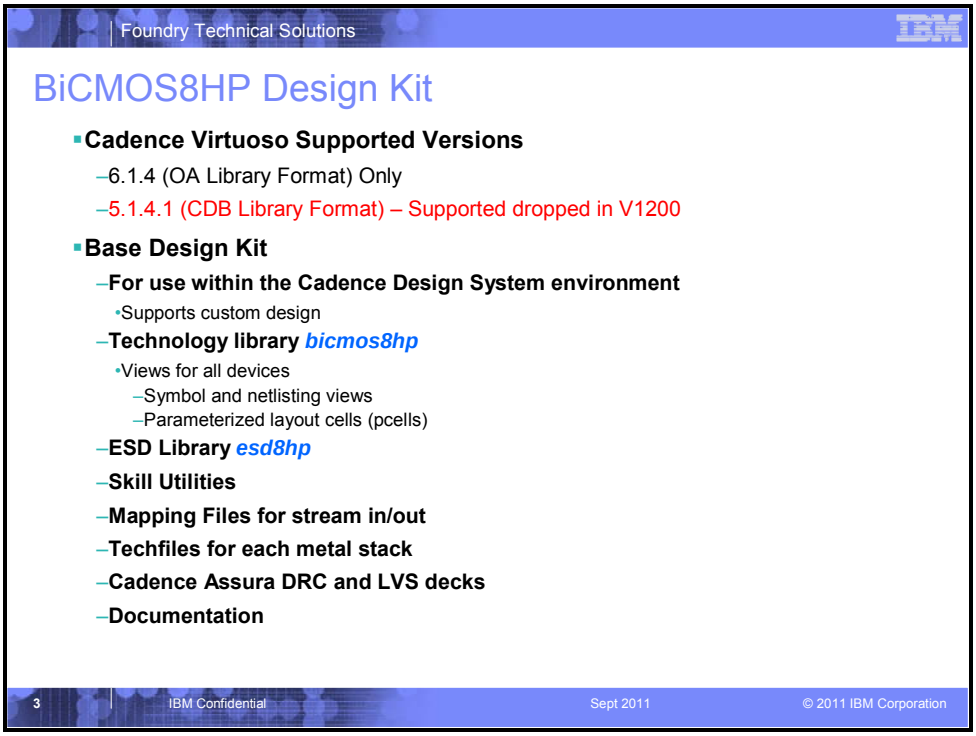
Yield Enhancement Design Techniques

Section 7.1 in the Design Manual describes the layout techniques that will optimize yield during manufacturing .

Design Kit Overview

This section describes some of the basics of the IBM design kit for the BiCMOS8HP technology. The design kit is Cadence based, with "add-on" point tools for design rule checking (DRC), layout versus schematic (LVS) and parasitic extraction. The base Cadence design kit contents, download, installation and set up are presented here, as well as highlights of the bicmos8hp technology library involving schematic entry, layout and other utilities.





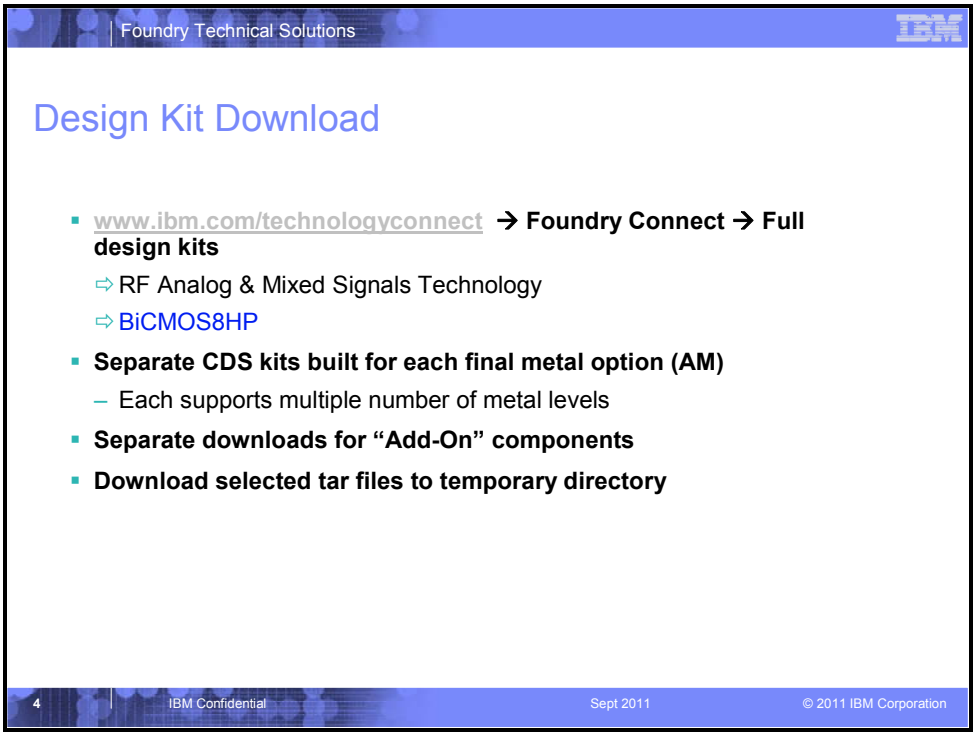
Base Design Kit

The base design kit is for use with the Cadence Design System (CDS) environment. Additional point tool support is available in add-on installations. The IBM supplied CDS kit features the *bicmos8hp* technology library including various views for all offered devices. In addition to the parameterized cell (pcell) layout view and symbol view for schematic entry, many different netlist views are supported:

auLvs	used in CDS diva extraction, for Diva LVS
spectre	spectre direct simulation
hspiceD	hspice direct simulation
auCdl	Component Description Language (CDL), for alternate LVS tools

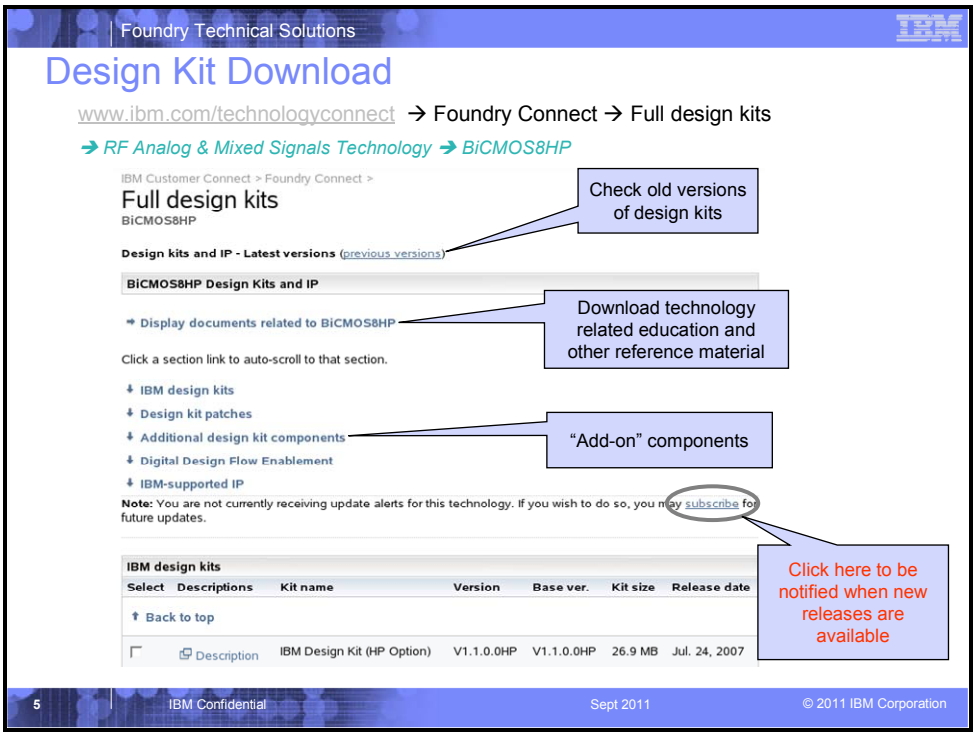
Also included in the CDS design kit are Skill functions compiled for execution within the CDS environment. These functions are those associated with the *bicmos8hp* technology library, including the callbacks for the component description format (CDF) of each device, as well as global utilities for pre-setting various CDS menus for launching verification jobs and other purposes.

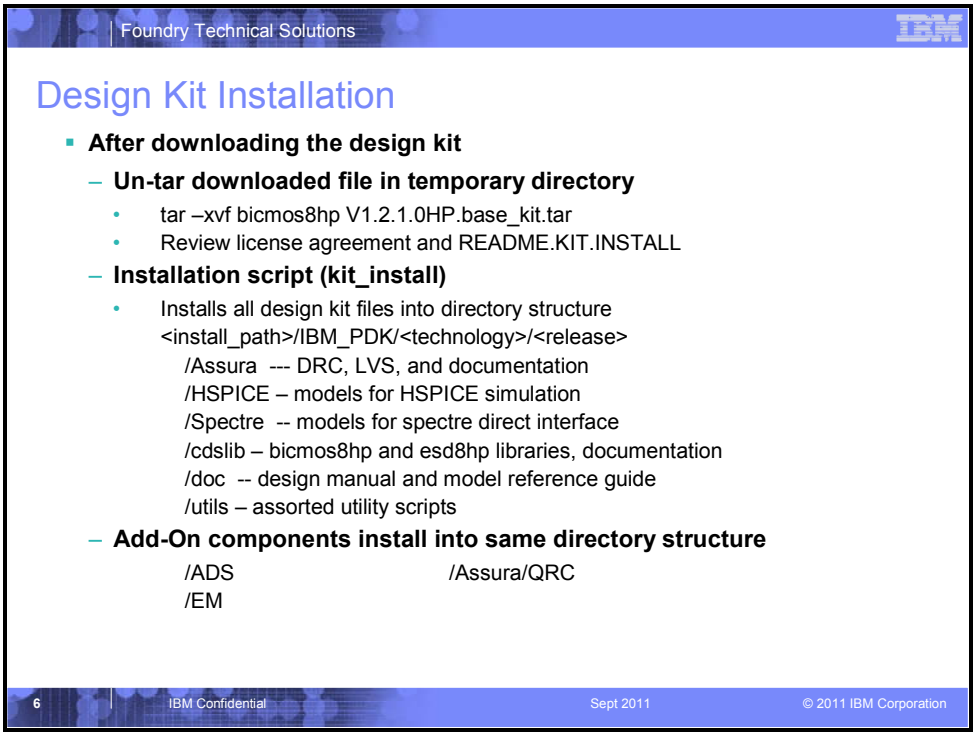
Mapping files to convert Cadence layout data to and from gds are supplied in the design kit, as well as Cadence technology files (techfiles) specific to each metal stack. The techfiles are supplied as ASCII files, and can be customized if required to support additional CDS tools. Cadence library documentation and technology reference materials are shipped along with the base design kit package as well.



Design Kit Download

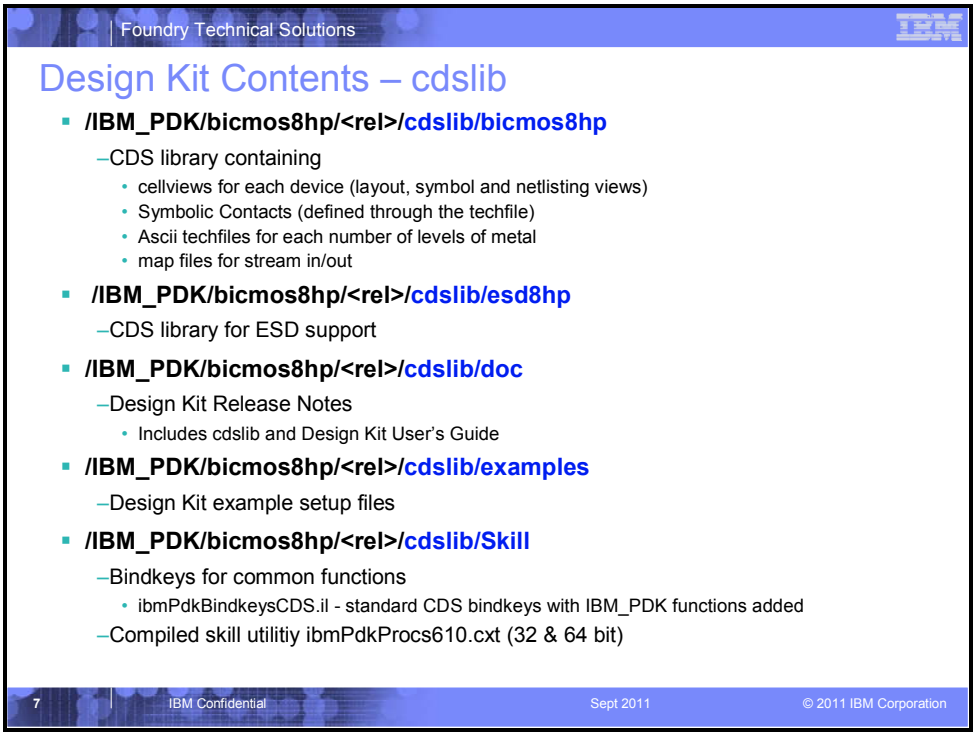
The IBM Customer Connect web site is used to download all design kits. The BiCMOS8HP CDS kit supports the multiple numbers of metal levels available in the technology. The add-on components, such as Cadence Assura QRC (for parasitic extraction) is available for download from the same web page. Selected design kits are downloaded as tar files into a temporary directory. To receive update alerts for the PDK new releases, click "**subscribe**" in the design kit download page.

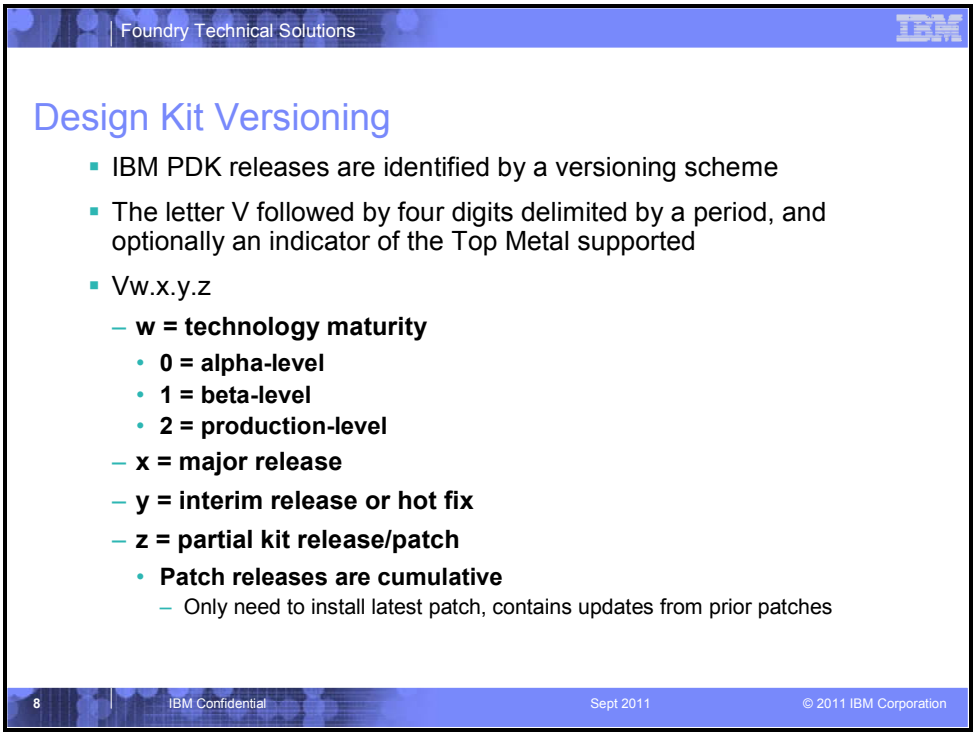


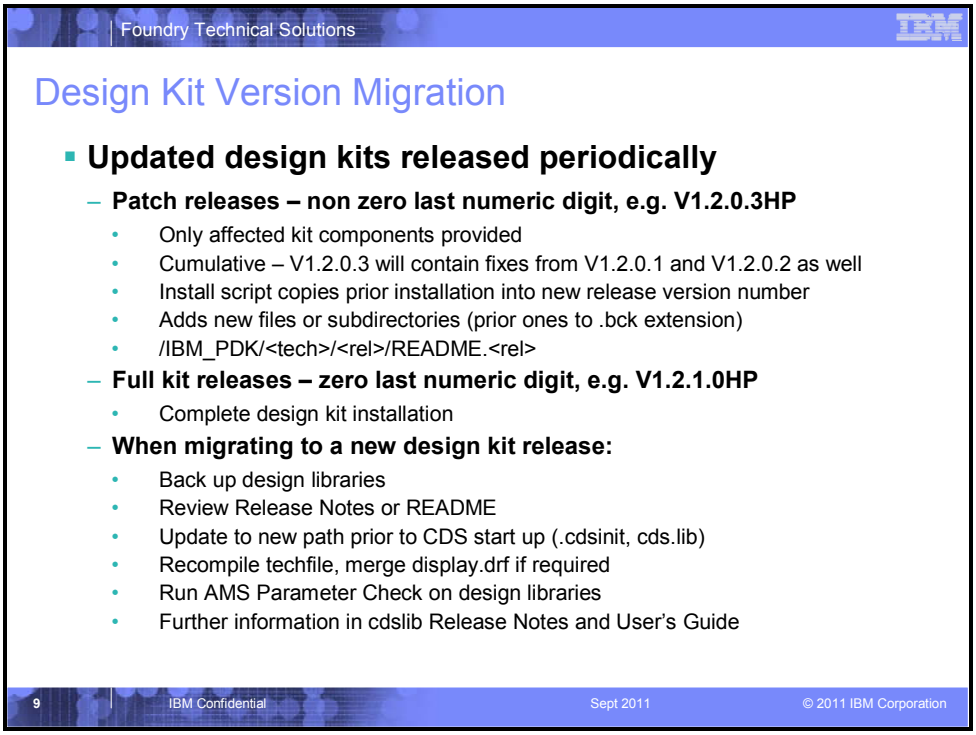


Design Kit Installation and Contents

Once the design kit is downloaded, it may be un-tarred and installed. The kit_install script is used for installing the design kit into the <path>/IBM_PDK/<technology>/<release> standardized directory structure. "Add-on" design kit components also include installation scripts which install the files into sub-directories in the same directory structure.

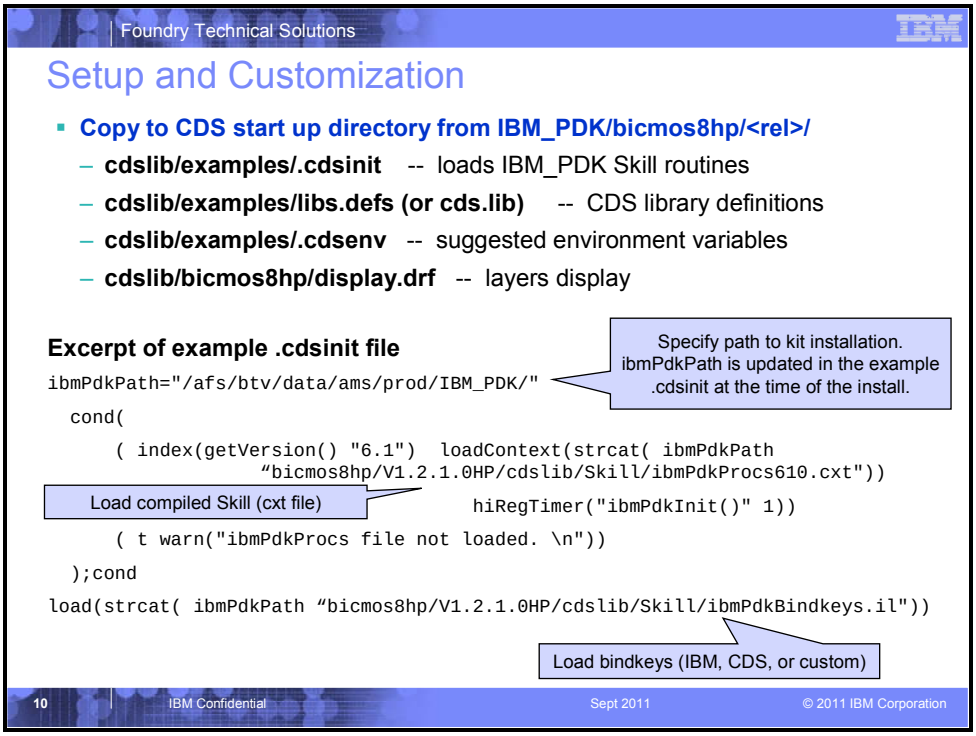






Design Kit Versioning and Version Migration

Design kit updates are made available periodically and are either patch releases (with a non-zero last numeric digit) or full kit releases. Always review the README or Release Notes prior to migrating to a new design kit release. The README file will often have supplemental information beyond what the Release Notes contain. The typical README contents will include which files were updated and instructions on how to install the update.

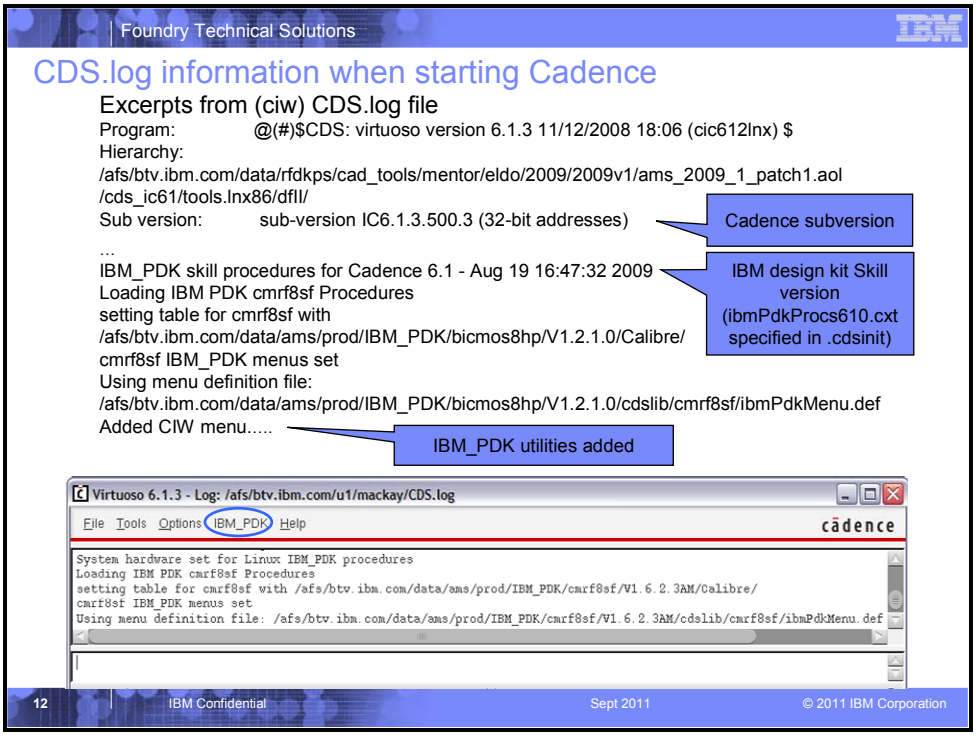


Setup and Customization

Example files are provided within the design kit that aid in first time startup of Cadence with the IBM supplied CDS design kit. These files are customized for the design kit full path during design kit installation, or can be updated later for the full path with the utility script available in /IBM_PDK/<tech>/<rel>/utils/update_pathname.pl. The example .cdsinit file needs to be copied into the user's Cadence startup directory. This file contains the code that conditionally loads the compiled Skill global utilities based on which CDS version is used. Bindkeys, which are shortcut methods of executing various Cadence and IBM Skill routines, can also be loaded from the .cdsinit file. Two different bindkey files are provided; bindkeysAMS.il has the shortcut keys set up consistent with prior IBM internal tools and bindkeysCDS.il has the basic Cadence default bindkeys, augmented with some of the more useful IBM added utilities. Either of these files can be used as a base and a user or CAD group administer can modify as desired.

The cds.lib example file is also customized for the installation path during the design kit install process. This file contains the library definitions for the bicmos8hp technology library, the esd8hp library for electro-static discharge (ESD) devices, and various Cadence libraries such as analogLib and basic. The path to the Cadence libraries is defined by the variable CDSPath so that it is always consistent with the version of Cadence utilized.

The display.drf can either be copied into the user's startup directory, or merged later through the Cadence menus. The example .cdsenv file should be placed in the user's root directory, or important lines from the example file can be added to an existing .cdsenv file. More information on the .cdsenv settings required for proper design kit operation may be found in the User's Guide for the cdslib component, located in /IBM_PDK/bicmos8hp/<rel>/cdslib/doc/bicmos8hp.cdslib.users_guide.pdf.



CDS.log Information

Once the appropriate files are copied into the user's startup directory and customized as desired, Cadence can be started in the usual fashion. The Cadence log file (CDS.log by default, in the user's root directory) is echoed in the Command Interpreter Window (CIW) and contains information that is often helpful to ensure proper design kit setup.

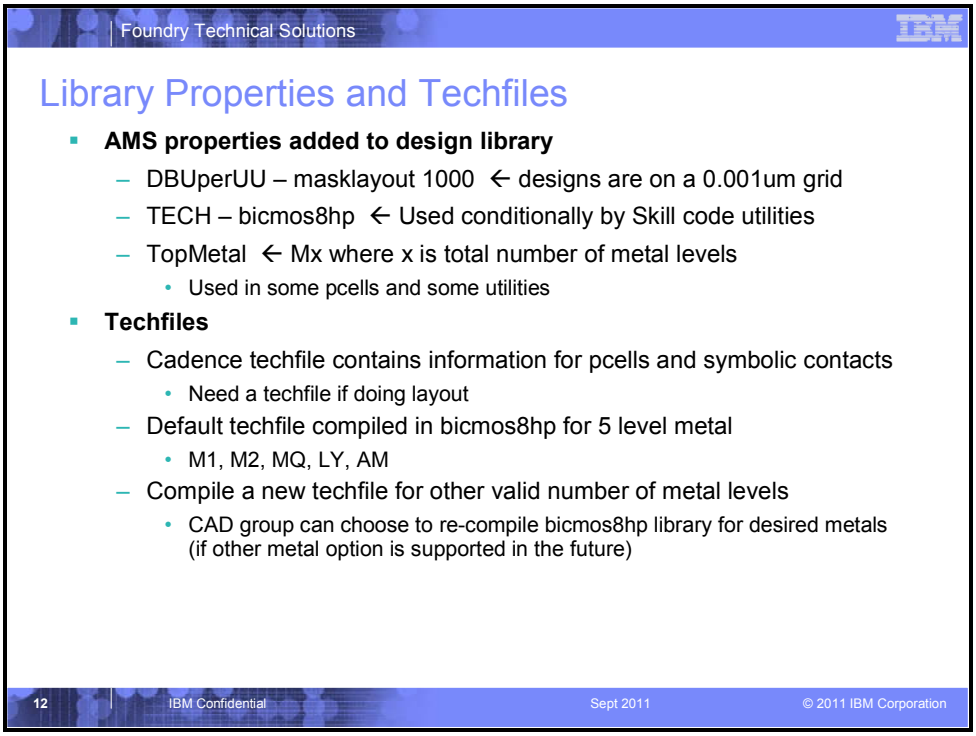
The CDS.log file will contain information regarding the Cadence subversion used, as well as a release version and date for the IBM supplied compiled Skill utility file (procAMSxxx.cxt, where xxx represents a CDS version) loaded.

Once the IBM Skill is loaded, an additional entry on the CIW banner, IBM_PDK, is available. The IBM_PDK entry can also be added with the command

placeAMSMenu()

entered in the CIW.

Information on adding custom user menus in addition to the IBM_PDK pull down is given in the cdslib User's Guide section "IBM_PDK Trigger Function".



Library Properties and Techfiles

Design libraries can be easily created from the ciw IBM_PDK → Library → Create pull down. Properties are automatically added to the design library when it is created through the IBM_PDK pull-down, or alternatively, the design library can be created from standard CDS menus, and the properties added through IBM_PDK → Library → Add AMS Library Properties. These library properties are important for proper functionality with the design kit. The Cadence database must be set to a DBUperUU (database units per user units) of 1000, which means a 0.001um grid in the layout. The snap spacing (set in the .cdsinit file) is set to the 0.01um mask-build grid The TECH and TopMetal properties are used by the Skill utilities and some pcells.

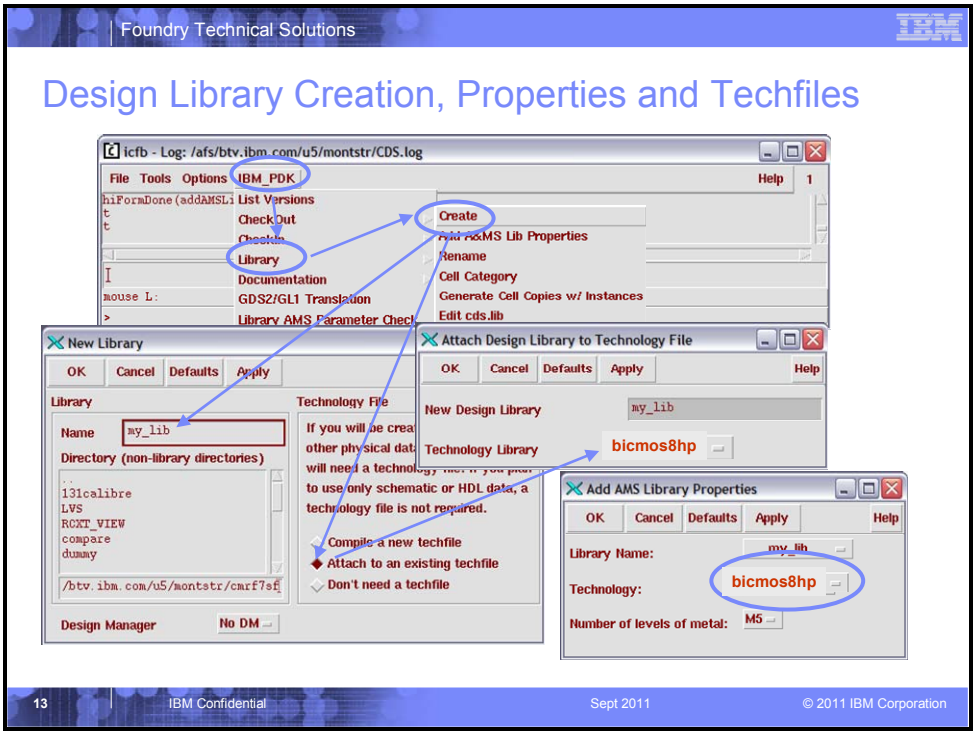
Each library requires a technology file (techfile) to specify layer definitions, device definitions, layer physical and electrical rules, and rules specific to individual Cadence applications. The *bicmos8hp* library is shipped with a technology file compiled for five levels of metal. When a new library is created through the Cadence ciw → IBM_PDK → Library → Create pulldown, the user has an option of "Compile a new techfile", "Attach to an existing techfile", or "Don't need a techfile." A techfile is required for layout.

If symbolic contacts are used in the layout, the techfile must be compiled for the appropriate number of metal levels. The library property for the number of metal layers does not control the symbolic contacts; this information is contained in the techfile. The compile option creates a techfile in the design library for the number of metals desired, while the attach option provides a pointer to another library which has a techfile.

If the number of metal levels used in the design is equal to the default compiled in the design kit, "Attach to an existing techfile" may be chosen to attach the design library to the techfile in the technology library. If the number of metals used in the design is not equal to the default, there are two choices. (1) Design libraries may be created with the option "Compile a new techfile," and the appropriate ascii technology file specified or (2) the system administrator may recompile the techfile in the bicmos8hp library for the desired number of metal levels. Recompiling

eliminates some typing on some of the Diva verification menus (the rules library defaults to the design library if it contains a compiled techfile). This method assumes all designers using the technology will be using the same number of metal levels.

Design Library Creation – Attach to an existing techfile



Existing Libraries – Compiling or Attaching Techfiles

Several ascii techfiles are supplied with the design kit -- one for each of the possible numbers of metal layers supported by the technology. The techfiles located in /IBM_PDK/bicmos8hp/<rel>/cdslib/bicmos8hp and are called techfile5.asc for five layers of metal.

For an existing library, the techfile may be recompiled or reattached using the procedures below. Here, the design library refers to the library that is receiving the new technology file (either a user's design library, or the bicmos8hp library).

Compiling a technology file:
1. From the Cadence CIW, select Tools → Technology File Manager → Load. The "Load Technology File" window will appear.
2. Specify the following:
ASCII Technology File: /IBM_PDK/bicmos8hp/rel/cdslib/techfile*.asc
Classes: Choose Select All. This will load all the classes or objects in the techfile.
Technology Library: Choose the design library to which you want the techfile compiled to. If your design library does not appear in the listing, it is because it doesn't yet have a techfile. Create a file in the physical subdirectory location named techfile.cds to force it to appear .
Mode: Select Replace. When you choose replace, the software replaces the entire technology file with the technology data defined in the replacement technology file.

Attaching a technology file:
1. From the Cadence CIW, select Tools → Technology File Manager → Attach.
2. Specify the following:

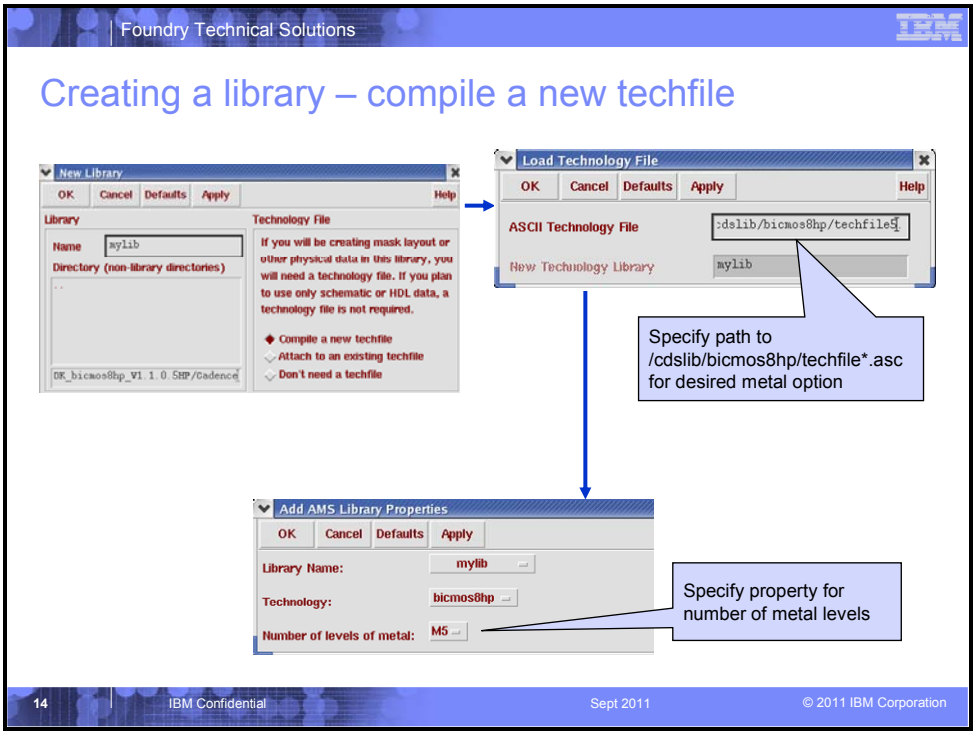
Design Library: Choose the design library.
Technology Library: The library containing the techfile you wish to attach the design library to.

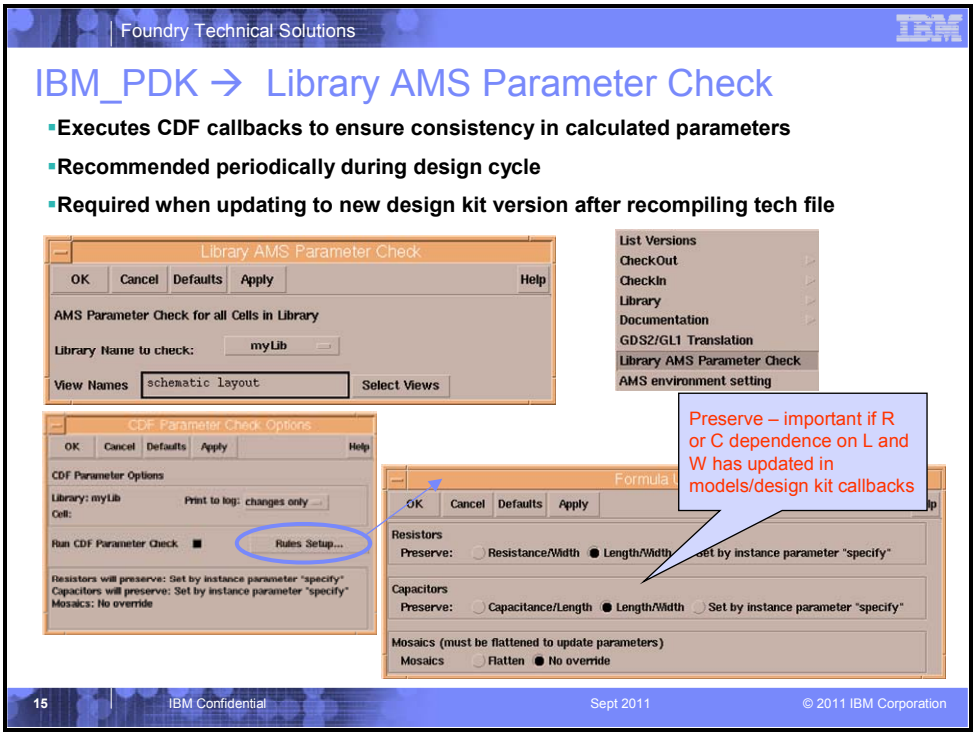
Setting the "techLibName";
To insure that the "techLibName" is set properly, follow the steps shown below.
1. From the Cadence CIW, select Tools →Library Manager. The Library Manager: Directory Form will appear.
2. From the Library Manager:Directory form,select the design library.
3. From the Library Manager:Directory form. → Edit → Properties. The Library Property Editor will appear.
4. Specify the following:
name: Select the design library
TECH: Choose the technology you are using.
TopMetal: Choose the number of metal layers for your design.
techLibName: This should be set to design library if the techfile is compiled. If the techfile is attached, the library it is attached to appears in this field.

Setting the library properties:
1. From the Cadence CIW, select IBM_PDK → Library → Add A&MS Lib Properties.
2. 2. Specify the following:
Library Name: Select the name of the design library.
Technology: The technology you are using.
Number of levels of metal: select the number of levels for your design (M5).

When a techfile is re-compiled, new symbolic contacts may be created. However, existing symbolics are not automatically removed. These can be deleted manually.

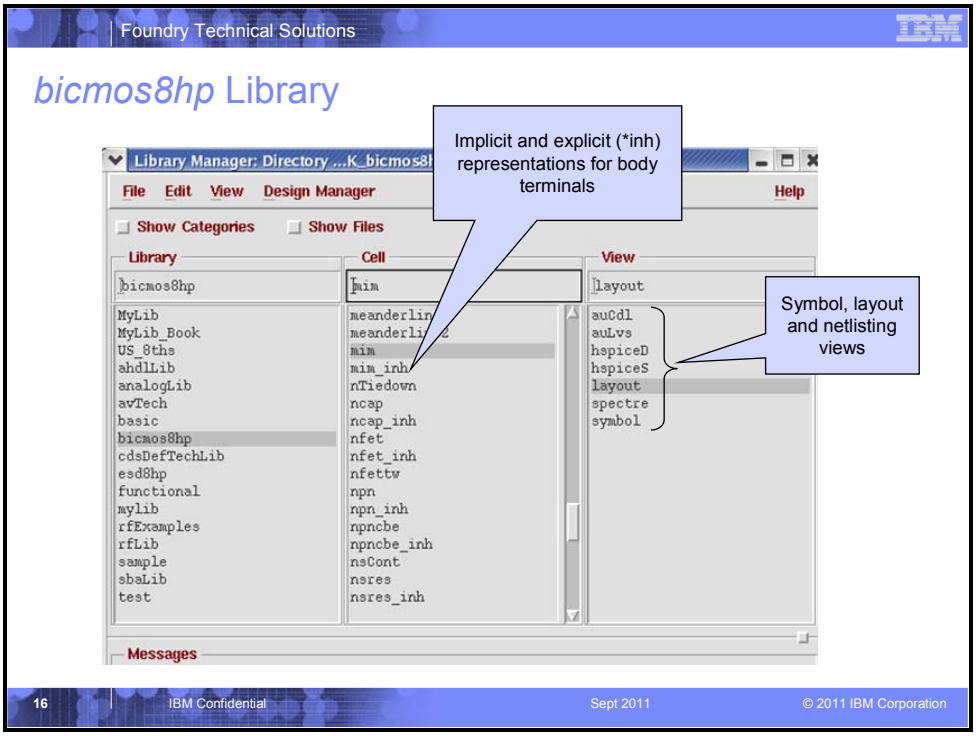
Design Library Creation – Compile a new techfile





Library AMS Parameter Check

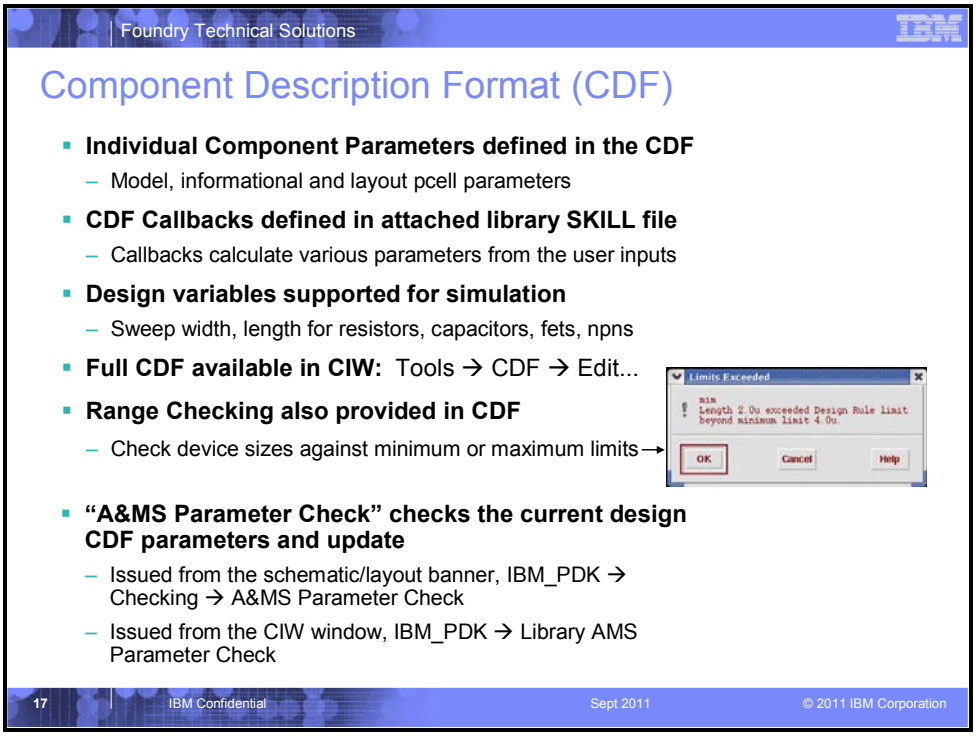
After migrating to a new technology, you can check and update your CDF callback parameters. Whole library callbacks may be done from the CIW IBM_PDK → Library AMS Parameter check. Single cell or device checks and updates can be executed from the IBM_PDK schematic banner → Checking → AMS Parameter Check.



bicmos8hp Library

The *bicmos8hp* library contains the symbol, layout and netlisting views for all the devices, as well as many layout-only entries. The ciw → Tools → Library Manager screen is shown in the slide above. The "Show Categories" option is particularly useful when first learning the bicmos8hp library element names. The devices available and relevant options are discussed in detail in the BiCMOS8HP Device Library section.

Most library elements support both an implicit and an explicit representation for schematic entry, with the explicit representation denoted with the "inh" suffix; for example, mim is the implicit 2-terminal metal-insulator-metal capacitor, and mim_inh is the explicit 3-terminal capacitor. Although only 2 terminals show in the schematic for the mim, the third terminal is implicitly defined as discussed later in this material. The extra terminal is the substrate or ground plane node.

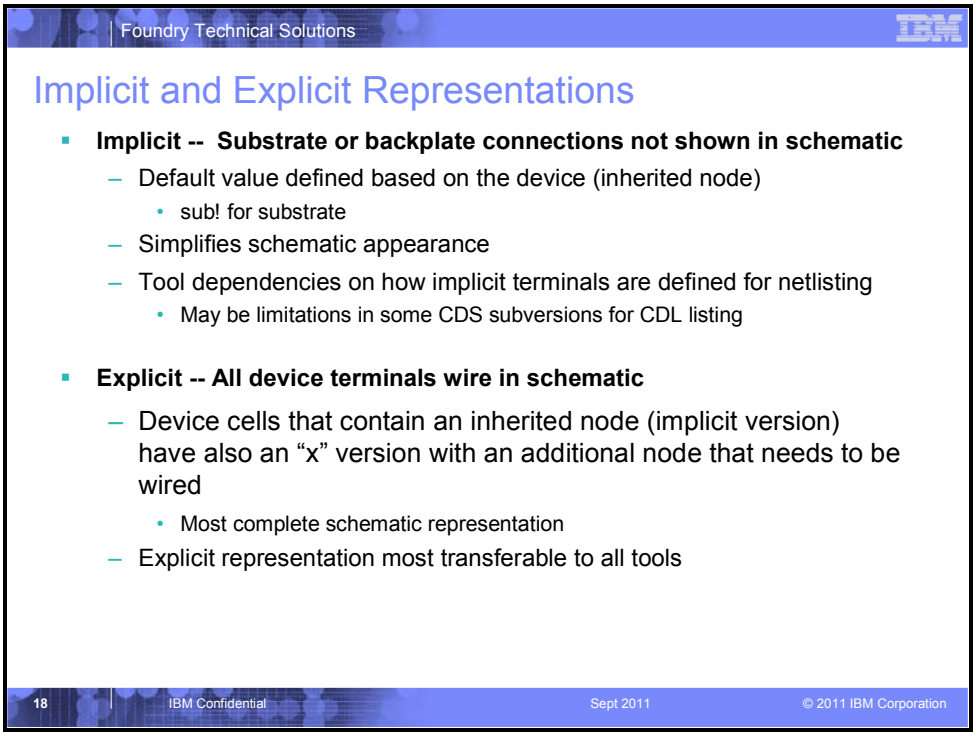


Component Description Format (CDF)

The Cadence CDF defines many important parameters for every device. Some parameters are entered directly by the user when adding or editing an instance, and others are calculated through callbacks, based on the entered parameters. Design variables are supported for simulation, but the parameters must be set to proper numeric values prior to schematic driven layout (Layout XL) or LVS comparison. Passive components such as capacitors may be either specified by length and width, or capacitance and width.

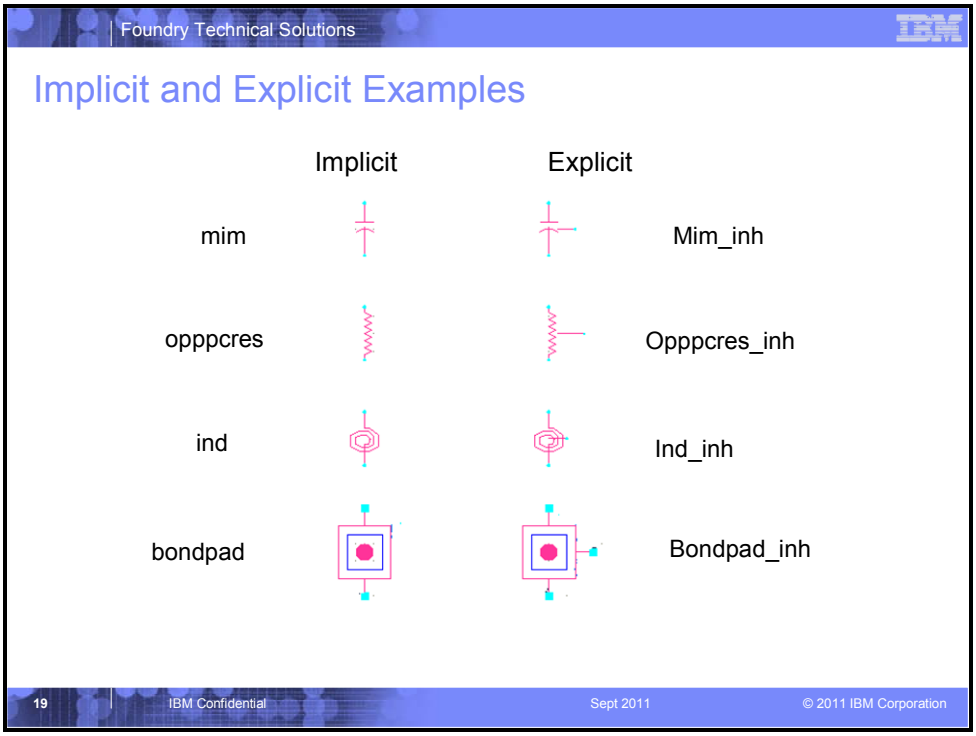
A procedure to reissue the CDF callbacks can be found in the schematic/layout window, IBM_PDK → Checking → AMS Parameter Check. It is recommended to run this procedure when an existing instance is being altered to a new device name, or translating designs to new kit version. It is mandatory when migrating design among different last metal design kits, (as an example, from relHP 5lm to relHP 7lm).

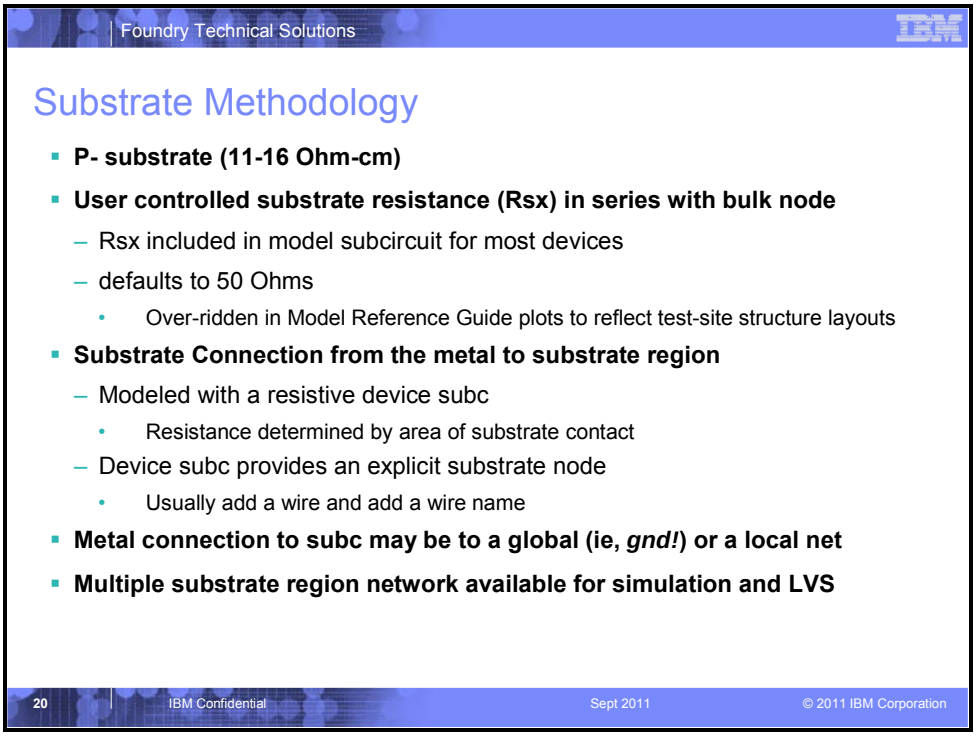
To update a whole design library with multiple cells, a library AMS parameter check can be issued from the CIW IBM_PDK → Library AMS Parameter Check.



Implicit and Explicit Representations

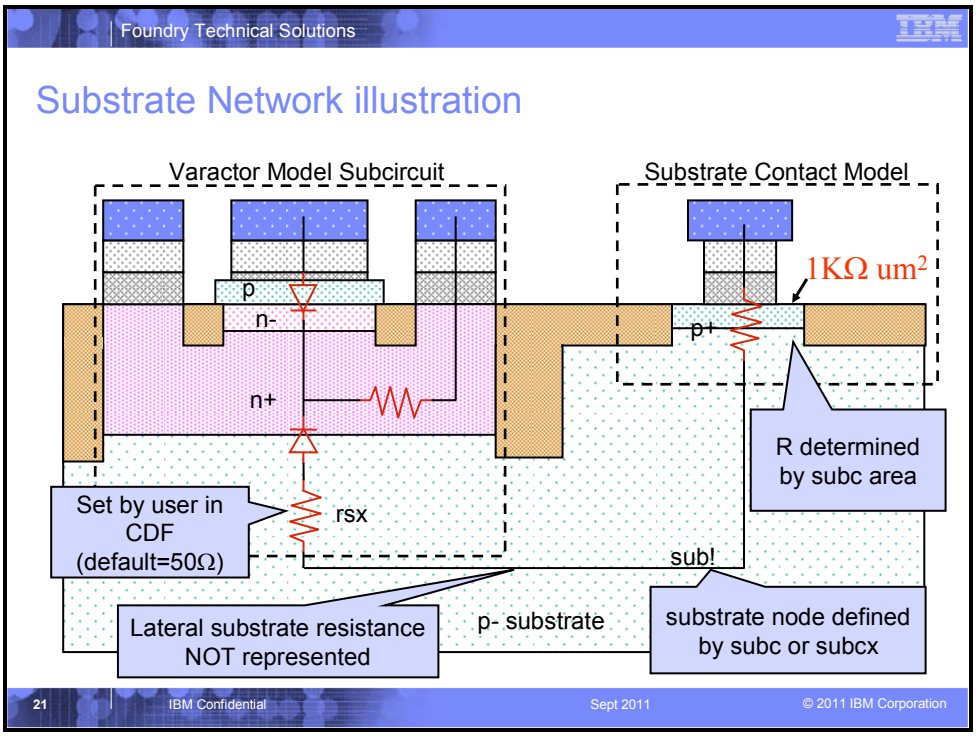
Both implicit and explicit representations are supported for most library elements. Implicit symbols make for a simpler-looking schematic, but explicit symbols convey all terminal information and are more compatible with all netlisters.

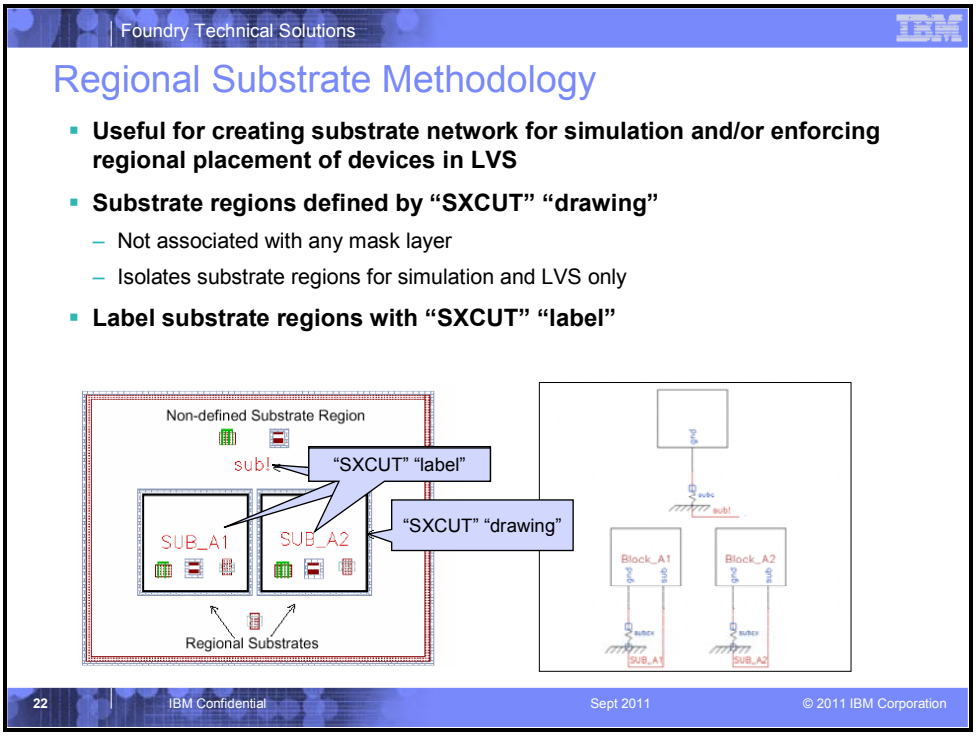




Substrate Methodology

RF designs are sometimes sensitive to substrate impedance. The bicmos8hp design kit elements support a partial substrate methodology that may be useful for analysis of substrate sensitivities. Individual device models contain an estimate of substrate resistance, and the substrate contact (subc element) is treated as a resistive device. Lateral substrate resistance between two substrate regions is NOT included in the extraction, but may be included manually in simulations if the regional substrate methodology is used. Refer to the Model Ref Guide for more information.





Regional Substrate Methodology

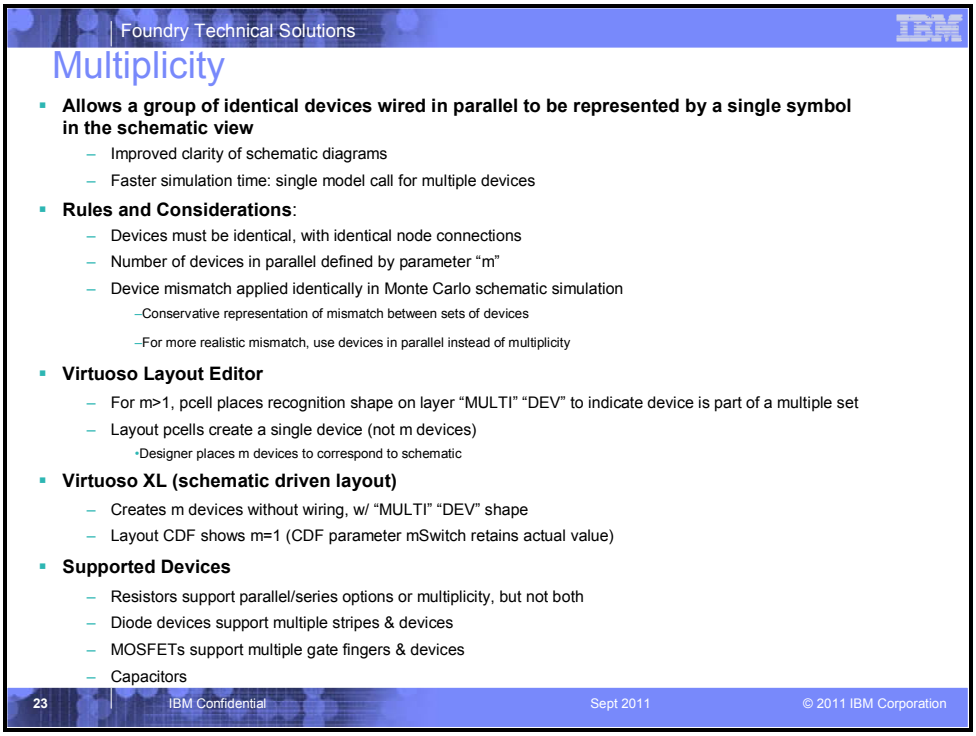
The "SXCUT" "DG" level may be used to isolate substrate regions for the purposes of simulation and LVS. "SXCUT" "DG" does not map to any mask build layer and has no affect on actual substrate impedance. For simulation purposes, a substrate network can be manually created between the otherwise ideally isolated regions.

Areas without SXCUT are given an SXCUT implicitly.

The Layout training module has additional information on changes you can make to the layout to increase substrate isolation.

Substrate regions separated by the "SXCUT" "DG" layer may be named with a label on the level "SXCUT" "LL". Most LVS tools map labels to pins automatically. Proper labeling allows the simulation substrate node, used for noise analysis, to be mapped into the LVS compare and ensure the layout agrees with the circuit under simulation.

Further information on the regional substrate methodology is in the PDK User's Guide.



Multiplicity

Multiplicity may be used to simplify schematics and reduce schematic simulation time. In your layout and schematic views, you will see a simplified representation – where one device is shown and representing many devices in parallel. Simulation is faster because there is one device call instead of the many in parallel. However, Monte Carlo mismatch simulations will be conservative because identical variation is applied to each of the "m" devices in multiplicity. If you want a more accurate representation of mismatch, do not use multiplicity.

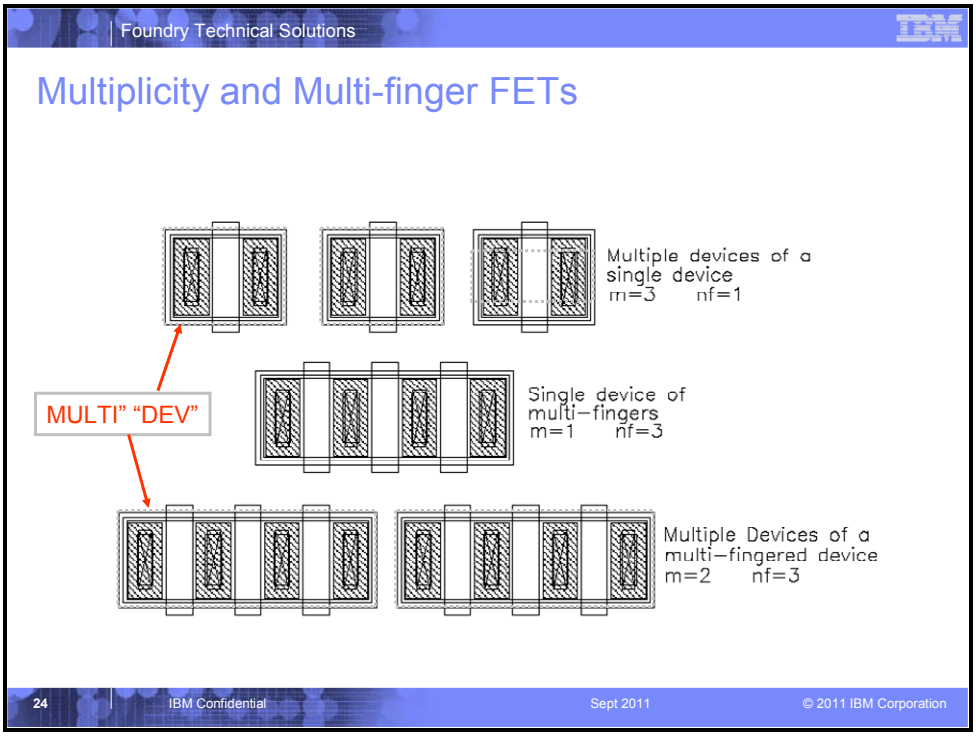
To use multiplicity, the devices must be identical in size and in their node connections. The number of devices in parallel is represented by the parameter "m" in CDF.

If multiplicity is employed, users should be aware of the different behavior between manually placing the layout pcell in the Virtuso Layout editor versus using schematic driven layout (Virtuso XL).

The Layout Editor will place one device with the recognition shape over it. However, it will only create one device no matter what you set the "m" parameter to in the CDF. You need to replicate the device for the required number to reach "m".

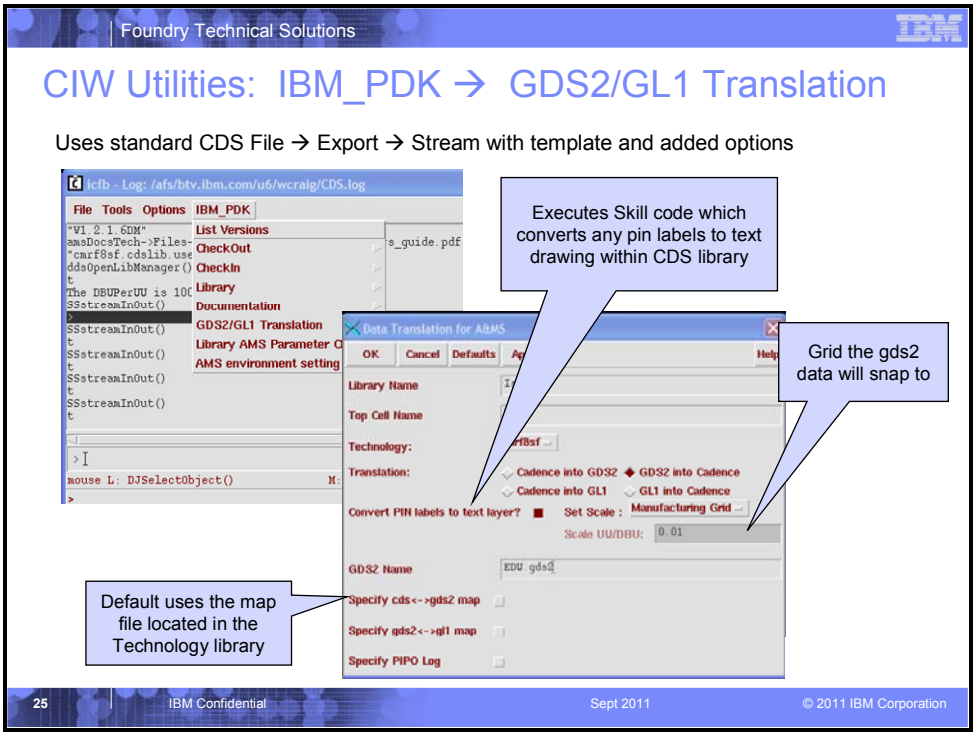
Virtuoso XL will create all "m" devices. It will also include the recognition shape. Each device will have an "m"=1, in the Layout CDF; however the CDF parameter mSwitch will have the actual value. This will allow the layout to match the schematic properly in LVS.

Not all devices allow multiplicity. Resistors, diodes, MOSFETs, and capacitors all allow multiplicity.



Multiplicity and Multi-finger FETs

FET devices support both multiplicity and multi-fingered devices. The "MULTI" DEV" shape surrounds the RX (active) region of devices in multiplicity. Multi-fingered devices are recognized through the multiple PC (polysilicon) shapes associated with a single RX shape.



CIW Utilities: Stream Out / Stream In Translation

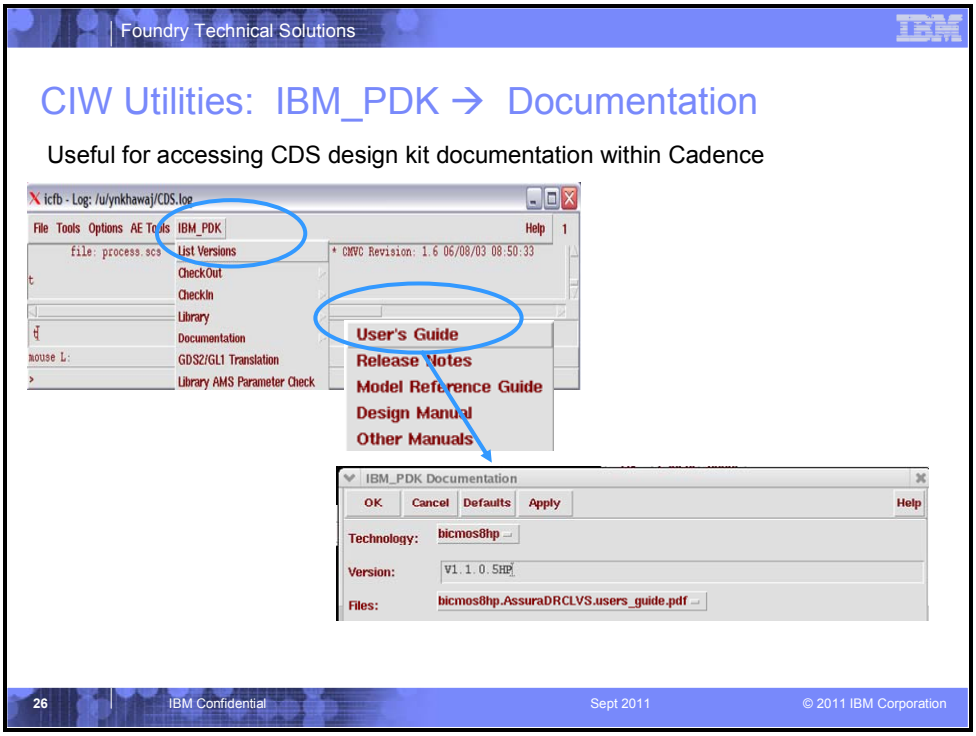
The IBM_PDK pull down from the CIW has many useful utilities not offered by the standard Cadence design kit. One of those is the utility used to stream in gds to layout, and stream out layouts to gds.

The CIW IBM_PDK → GDS2/GL1 Translation uses the standard Cadence File → Export → Stream with a template customized for BiCMOS8HP and various user settable options. By default, data will be streamed out on the manufacturing (technology mask build) grid of 0.01 micron. If no map file is specified, the cds2gds.map (for stream out, or gds2cds.map, for stream in) -located in the bicmos8hp library subdirectory- is used.

"Convert PIN labels to text layer?" executes Skill code which converts any text on a mask build level (associated with a pin) to the "TEXT" "DG" level within the CDS database. Text data is not allowed on any mask build level (design geometry restriction S10 in section 2.8 of the design manual).

The PIPO log (a record of stream-in/stream-out information, warnings and errors) file name can optionally be specified. Always review the PIPO log for errors or warnings.

Note: GL1 is an IBM data format used internally for data manipulations prior to mask build. The Cadence into GL1 and GL1 into Cadence translations are two step processes, with gds2 data as the intermediate step. The translation to and from GL1 is only used internally at IBM and may be ignored by the customer.



CIW Utilities: Documentation

Documentation that is shipped with the BiCMOS8HP design kit is available from the CIW IBM_PDK → Documentation pulldown. These are the same files that are located in IBM_PDK/bicmos8hp/<relHP>/doc.

Documentation and Technical Support

Design Manual and Model reference Guide, Release Notes are available from the Cadence CIW or IBM_PDK. Tool specific Release Notes are in the IBM_PDK tool sub-directories.

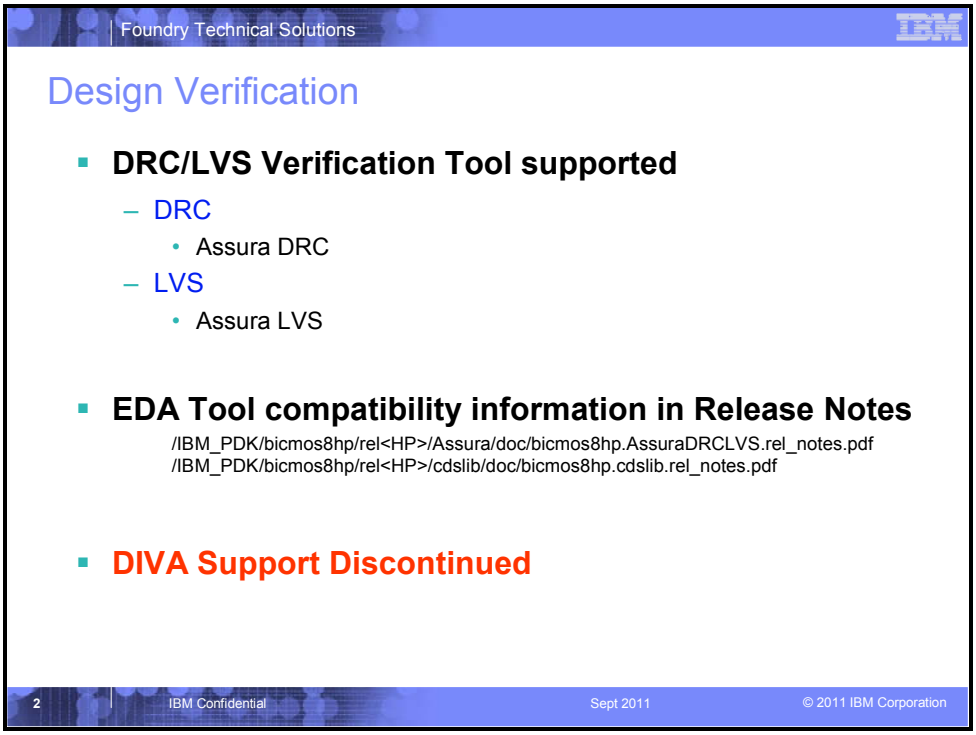
For technical support, contact MOSIS if using their design services. MOSIS customers are those who tape out through MOSIS They can be contacted at support@mosis.com .

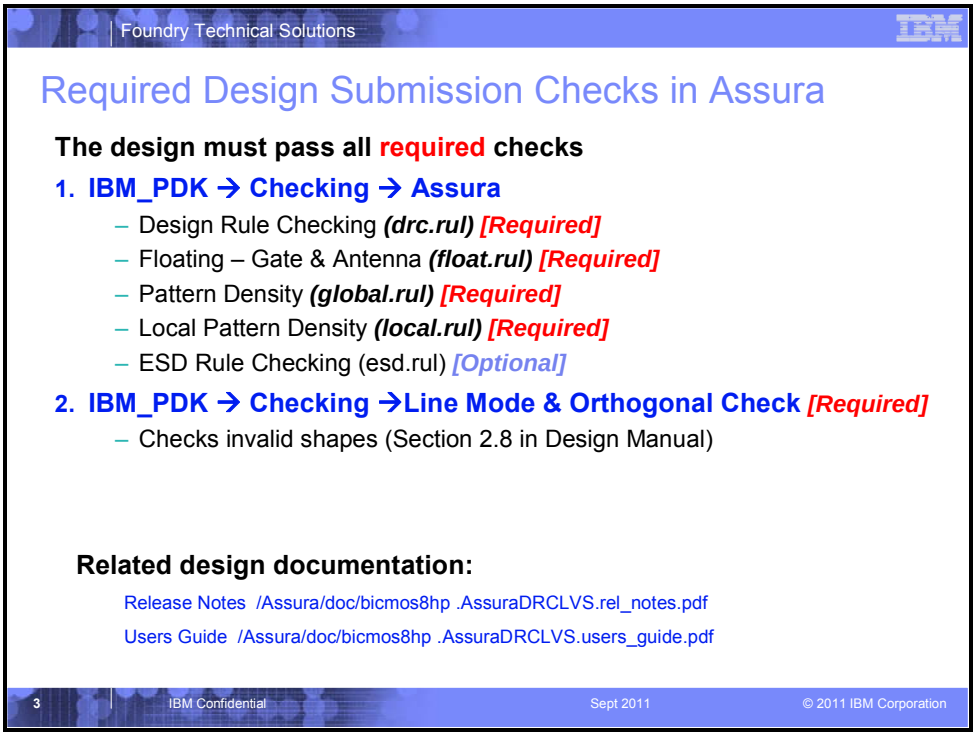
All other customers may contact IBM Foundry Technical Support through the web page or email fdrytech@us.ibm.com.

If you're not sure if you are a MOSIS customer, contact fdrytech@us.ibm.com, and we'll let you know if you are.

Design Verification

This module describes the availability and proper operation of the BiCMOS8HP design verification tools. The Cadence Assura tools are available for both the design rule checking (DRC) and the layout versus schematic (LVS). DIVA DRC and LVS are not supported.



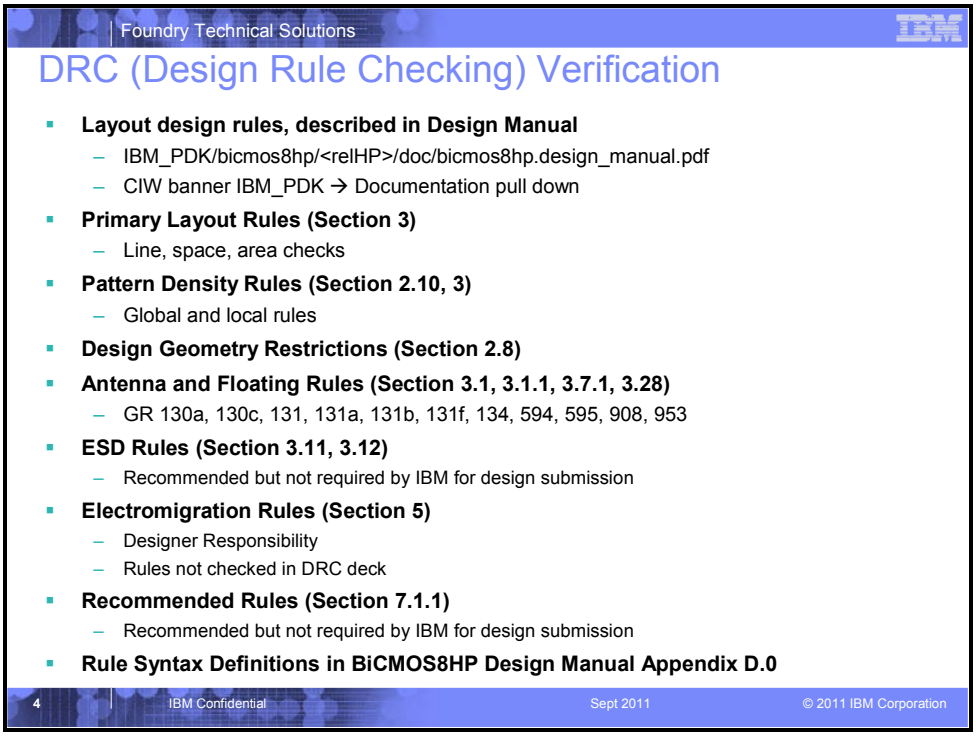


Required Checks for Design Submission

Prior to design data submission, design needs to comply with the chip design check list, which has been given in above slide if the Assura tool is used. Submitted design gds should be checked using the latest release of the design kit. The Skill utility is available from IBM_PDK → Checking → Line Mode & Orthogonal Check is available to highlight GRS6, GRS8 and GRS9 errors. It also checks instances and paths for off grid placement.

ESD rule checks are not required. The detailed design submission procedure information are available from IBM Customer Connect Website.

Assura DRC deck breaks the layout design rules into different groups, checked by separate verification routines. The directory '/bicmos8hp/<rel>/Assura/doc' contains supporting material for Assura. Each Assura deck includes the release notes. The Release Notes provide information about the tested tool versions, supported features, known limitations, etc.



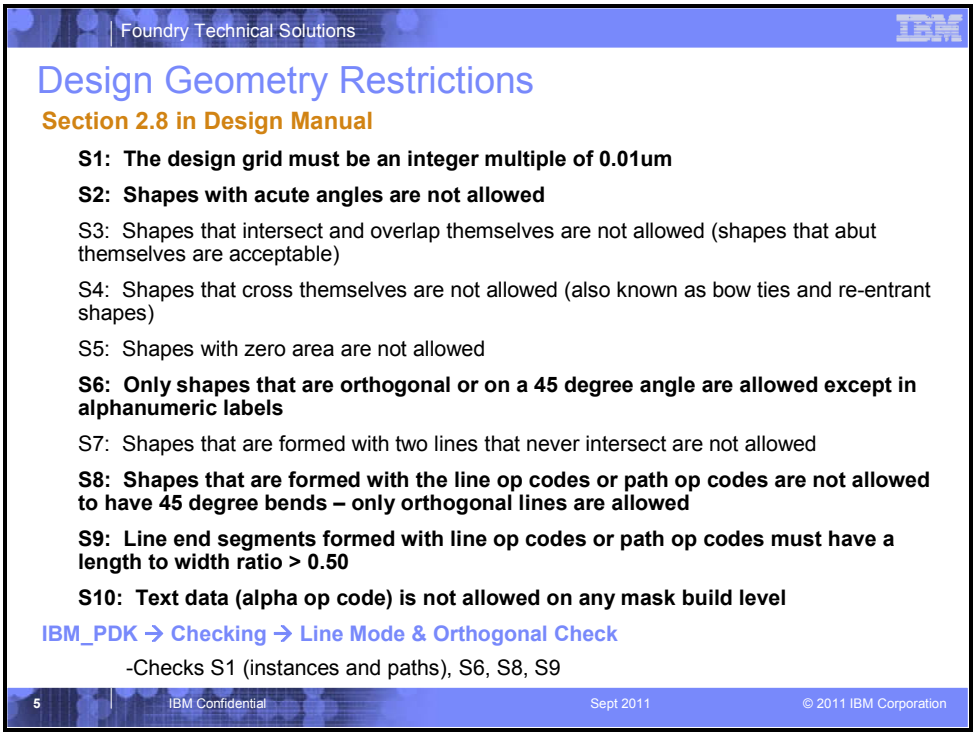
DRC (Design Rule Checking) Verification

The layout ground rules are described in the technology design manual which is provided as part of the design kit. The rules can roughly be broken down as primary design rules; pattern density rules, including both global and local requirements; design geometry requirements, such as design grid and ortho-45 restrictions; antenna and floating gate rules; electro-static discharge (ESD) rules; and recommended rules. The relevant sections of the design manual are noted in the slide above.

The robustness of an Input/Output (I/O) pad to electro-static discharge (ESD) events is very sensitive to the layout. Layout rules to ensure robustness are in the design manual section 3.12. ESD checking results are not used as part of the design submission criteria.

Relaxed layouts may result in higher yields. More conservative rules are provided in the design manual for yield enhancement. However, these should not be employed at the expense of chip area or performance. Recommended rules are optional and not used as part of the design submission criteria.

To assist in understanding and applying the layout ground rules, the definitions of rule syntax are provided in Appendix D.0 in the design manual.



Design Geometry Restrictions

Section 2.8 of the design manual includes the design geometry restrictions listed in the slide above. Some of these geometries are prevented within the Cadence layout editor itself.

The most common errors are given in bold in the slide above.

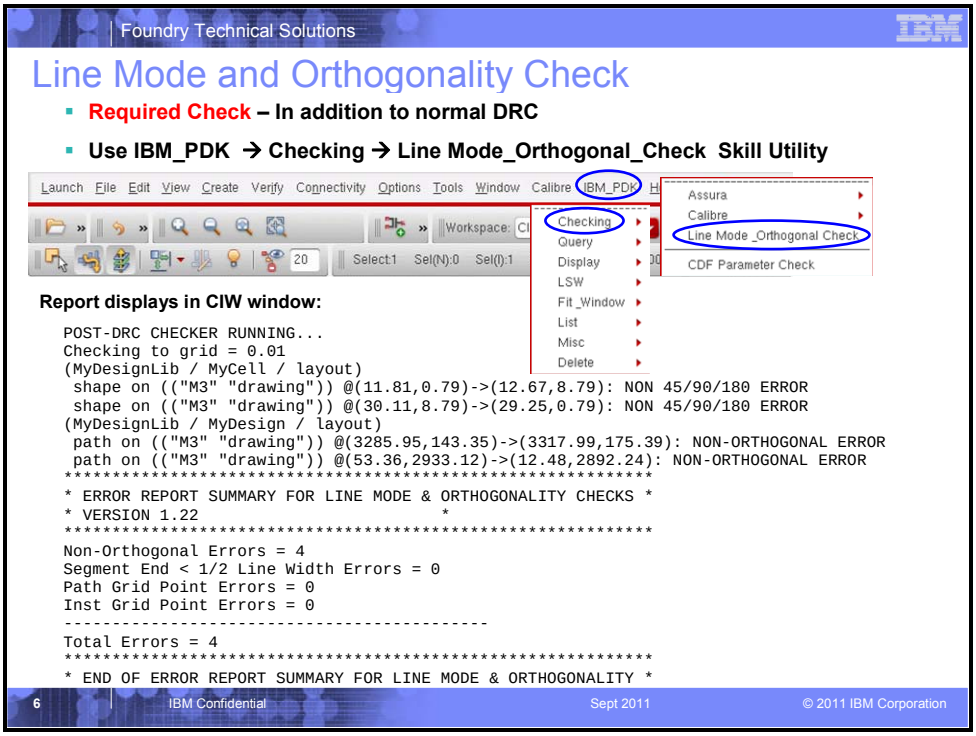
Rule S1 states that the design grid must be an integer multiple of 0.01um. The cadence database (database units per user units) is set-up on a 0.001um grid, so the layout editor grid snapping must be set appropriately (to 0.01um, or an integer multiple of 0.01) to avoid off-grid errors. Care needs to be taken with paths: Ortho-normal path widths need to be an integer multiple of 0.02um, or off-grid errors will result.

Shapes with acute angles are not allowed (S2), including shapes for company logos. Shapes that are orthogonal, or on a 45 degree angle only are allowed. The exception is alphanumeric labels, though this is discouraged. Design rule correct alphanumeric shapes are included in the bicmos8hp library (alpha12, alpha20, alpha25 and alpha40 cells, where the numeric suffix indicates the height in microns of the shapes).

Paths are not allowed on 45 degrees (S8); the Cadence “Convert to polygon” layout utility may be used to convert paths to polygons. This may however result in off-grid errors that need correction, depending on the original path width.

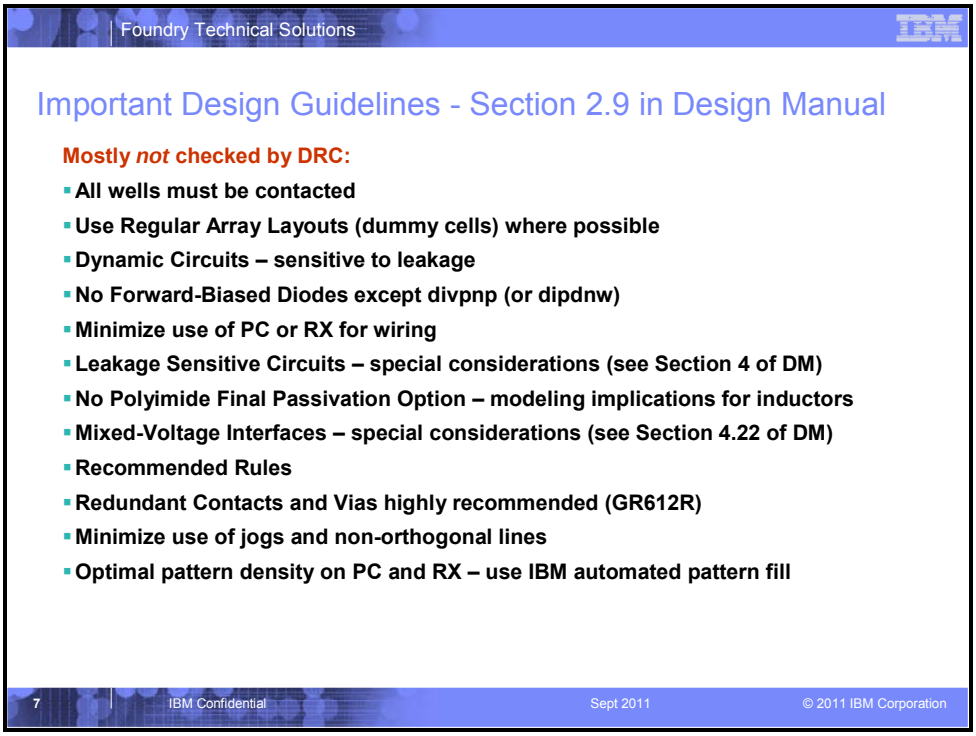
When terminating a path, the Cadence layout editor will issue a warning pop-up box for S9 errors (“First or last segment of created path should be not less than half the path width”).

Text data is not allowed on mask build levels (S10). A Skill utility is included in the design kit which will convert any text data associated with pins to the “TEXT” “DG” layer. This utility is executed on stream-out if the default option “Convert PIN labels to text layer?” is selected.

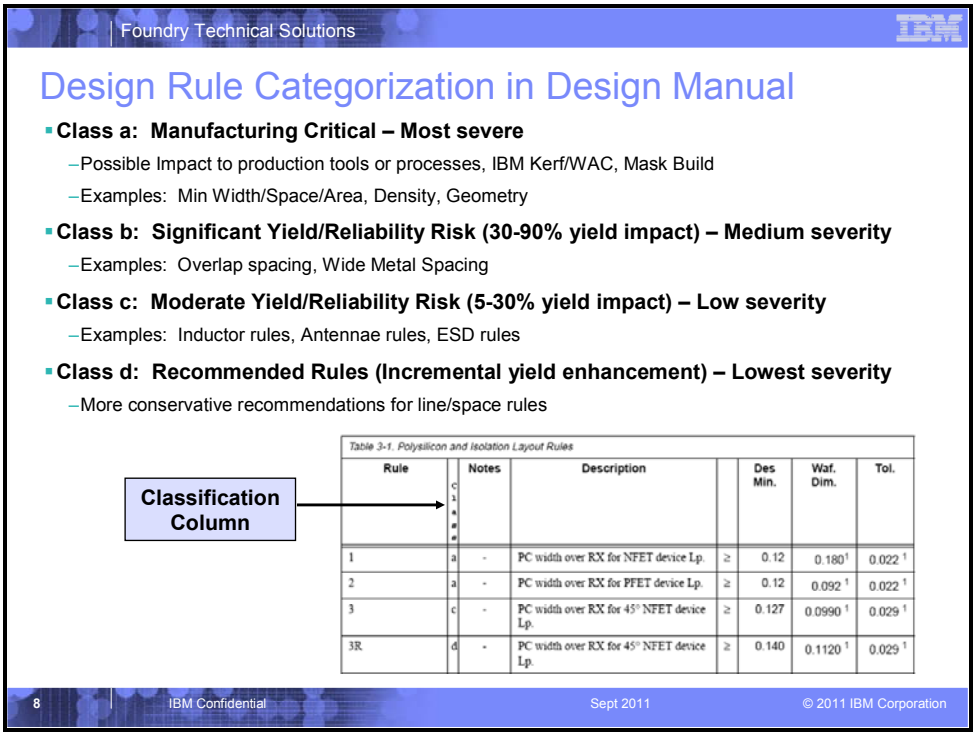


Line Mode and Orthogonality Checks

The Skill utility available from IBM_PDK → Checking → Line Mode & Orthogonal Check is available to highlight S6, S8 and S9 errors. It also checks instances and paths for off grid placement.



Important Design Guidelines

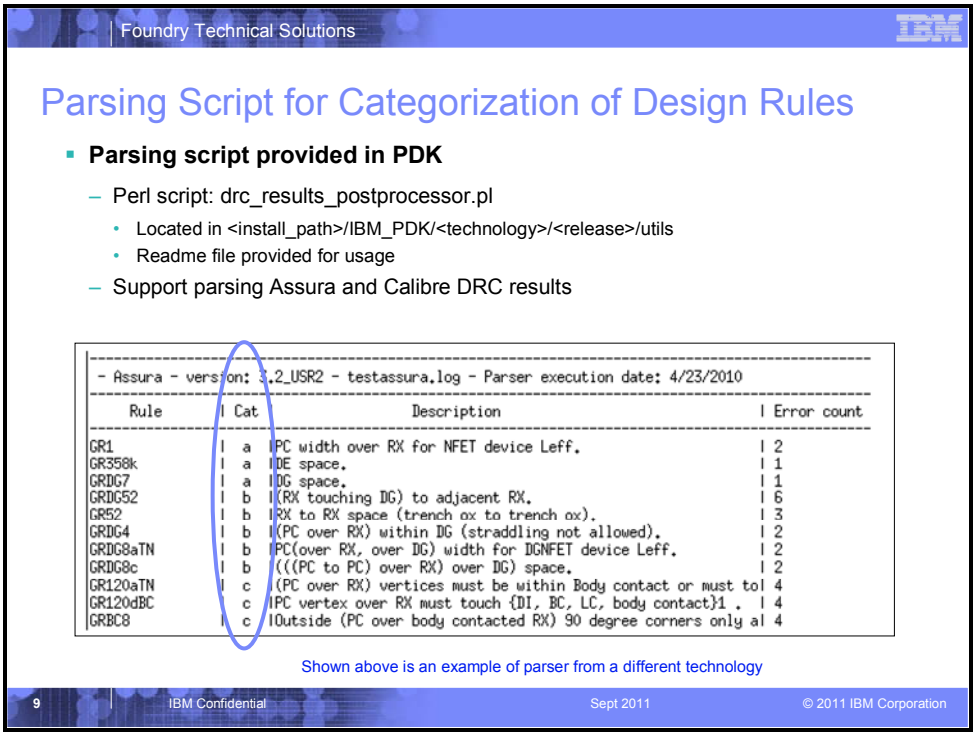


Design Rule Categorization in Design Manual

All design rules in the design manual are categorized in four classes by the severity of the rule impacting manufacturing process and yield. **Class a** rules are the most severe. They are critical for manufacturing. They must be met by the designers. These rules cannot be waived.

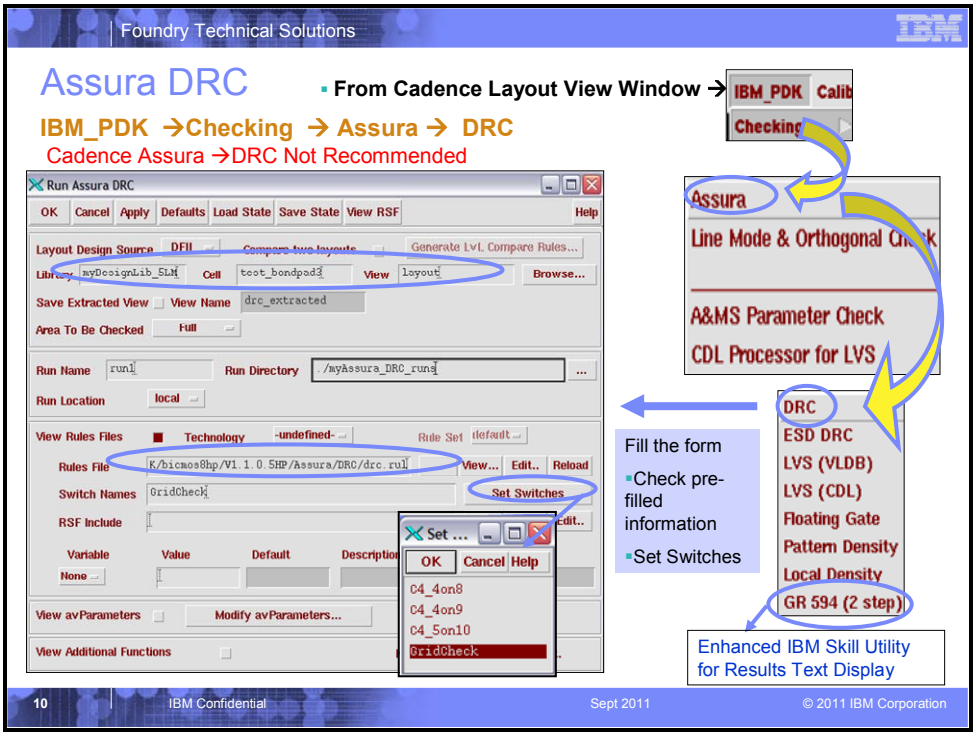
Class b and **Class c** design rules impact the yield. Class a rules have more adverse impact on the yield (30-90% impact) than Class b rules (5-30% impact). It is recommended that customer make all attempts to meet the Class b rules. Class c rules may be more appropriate for waivers based on the customer's choice to fix them. **Class b and Class c rules can be waived only at designer's risk.**

Class d rules are the recommended rules. They are for yield enhancement only. These rules are not checked by the Release Engineering prior to Release-To-Mask (RTM) checks. Designers are encouraged to meet these rules if the chip size and performance are not compromised.



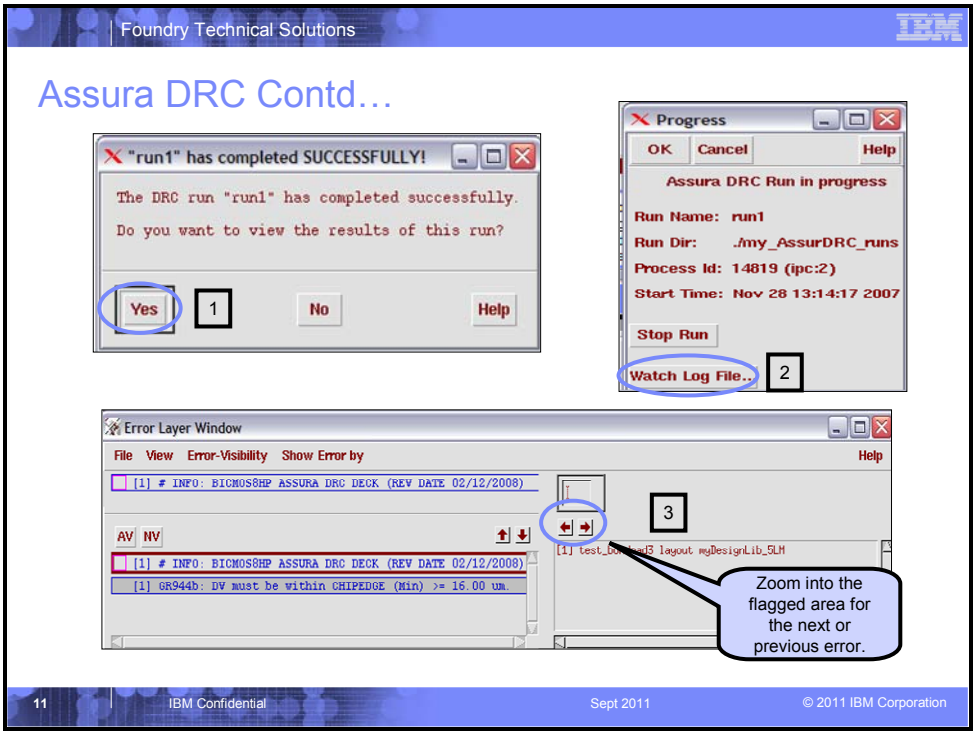
Parsing Script for Categorization of Design rules

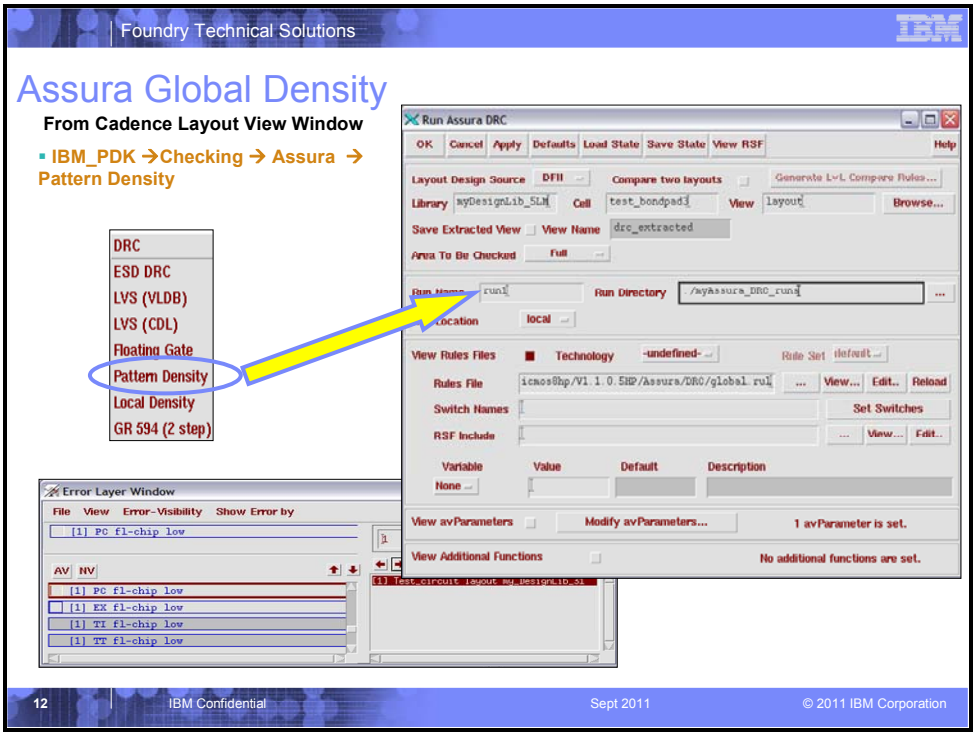
A parsing script is provided in the design kit to view the results of DRC violations by the category/class type as an aid for analyzing them. For cmrf8sf, the provided perl script handles both Assura DRC and Calibre DRC output.



Assura DRC

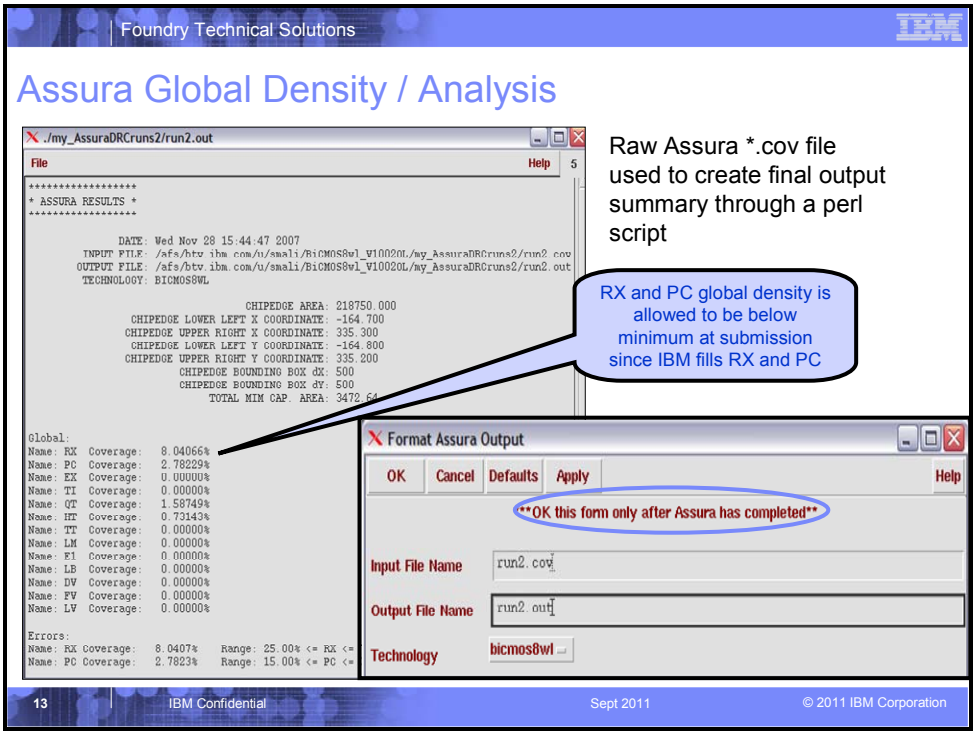
Assura is Cadence's hierarchical verification tool. Launching Assura DRC through the IBM_PDK → Assura banner entry is preferred over using the Cadence Assura entry. With the IBM_PDK method, the Run Assura DRC menu is pre-filled with the correct Rules File path and other default settings. Errors are displayed graphically and are written to the .log and .err files. ESD rules are included in a separate file, IBM_PDK → Checking →Assura → ESD DRC.

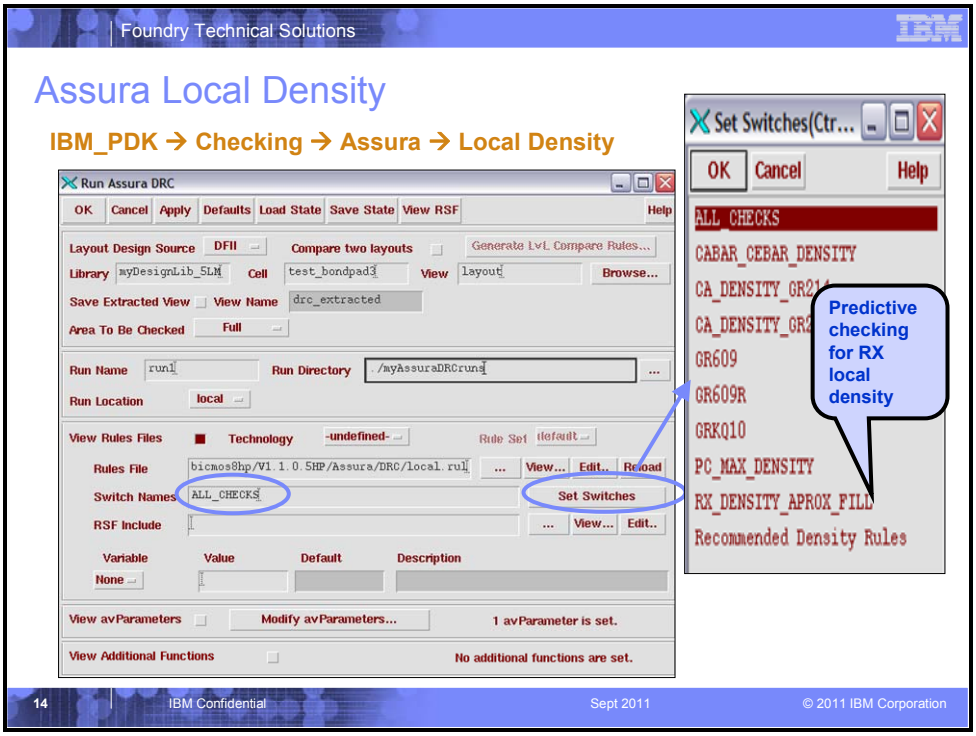




Assura Global Pattern Density

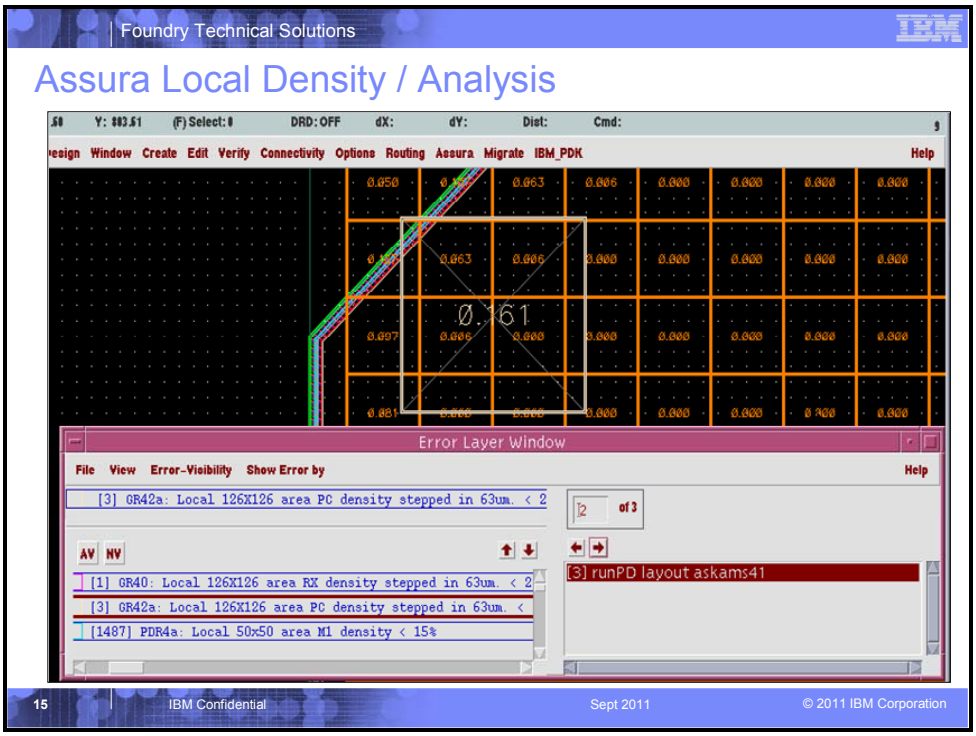
IBM_PDK → Checking → Assura → Pattern Density executes the global density checks. No switches are needed for this verification. After the Assura run completes, the raw data from the .cov file is processed through a perl script which writes a summary file of the final results. The perl script is located in /IBM_PDK/bicmos8hp/<relHP>/utils/density.pl and may be run stand-alone.

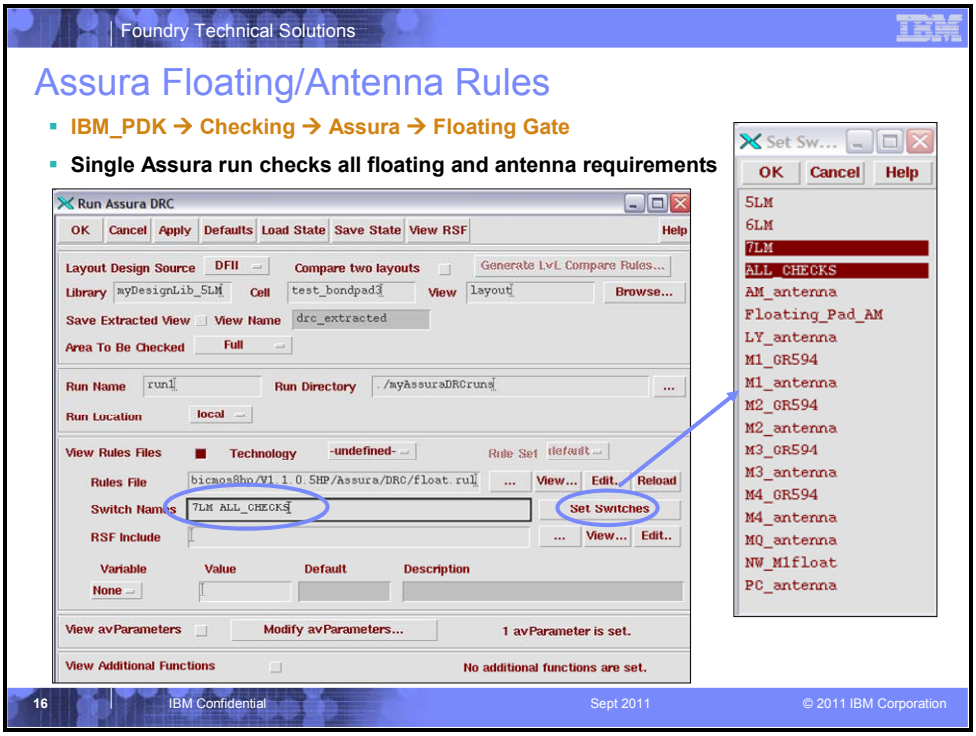




Assura Local Pattern Density

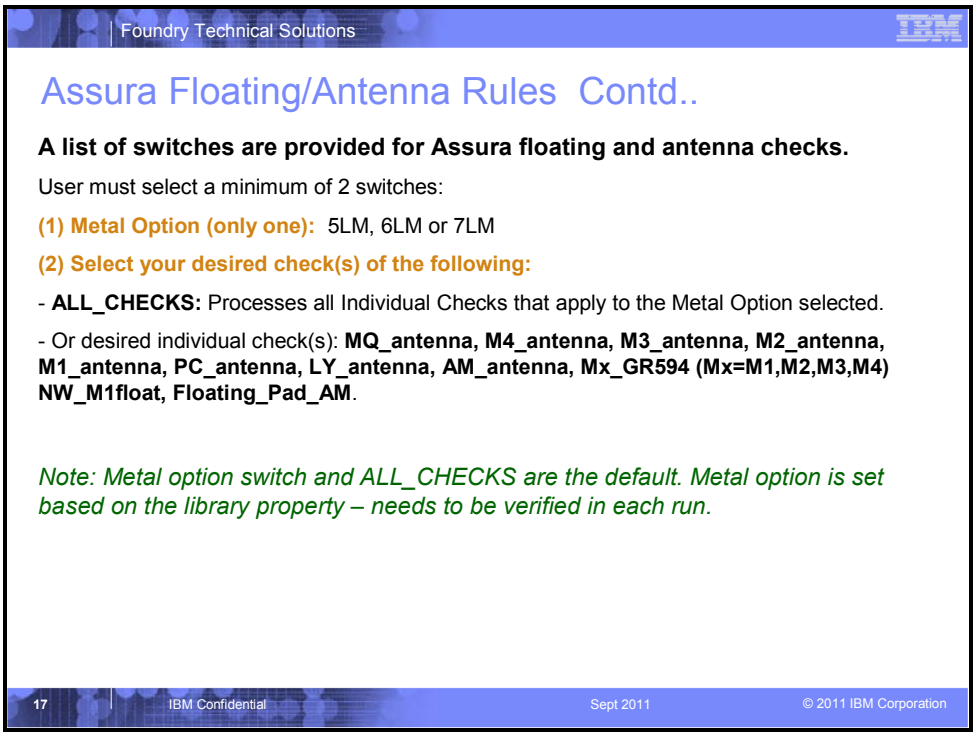
Assura local density checks are coded in a single rule file, controlled by individual switches and the default "ALL_CHECKS" switch. Actual densities are displayed numerically on the layout, and error locations are written to the .err output file. The Assura local RX, PC checking is predictive. Areas of the chip that exceed the local maximum for RX and PC will be flagged. Areas that are blocked such that IBM will not be able to add sufficient fill will also be highlighted as errors and must be corrected prior to design submission.

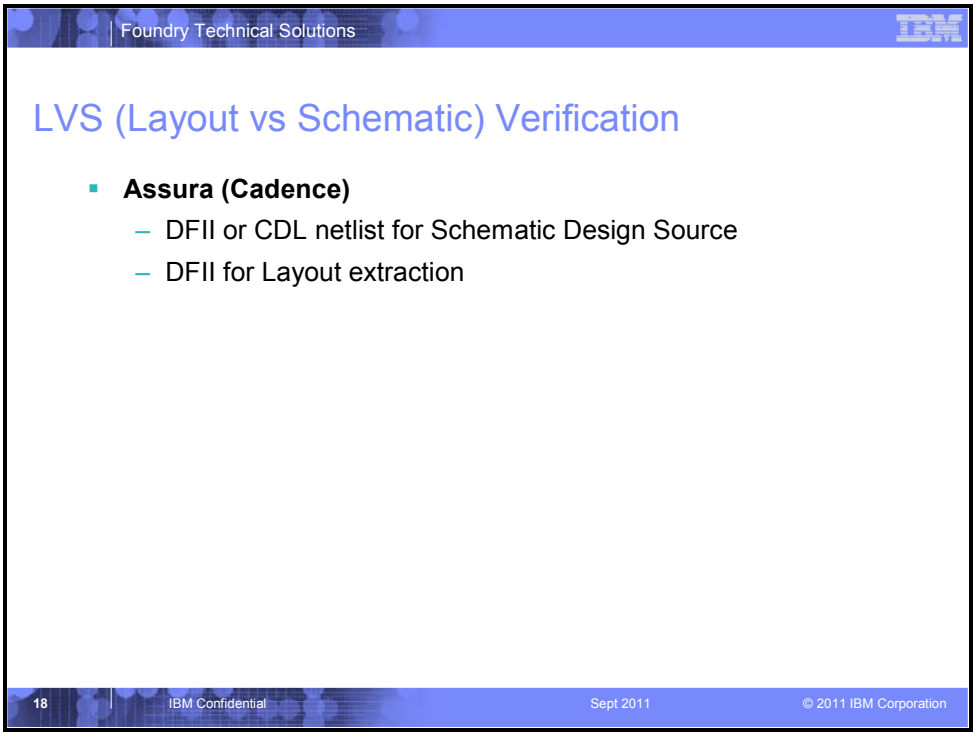




Assura Floating/Antenna Rules

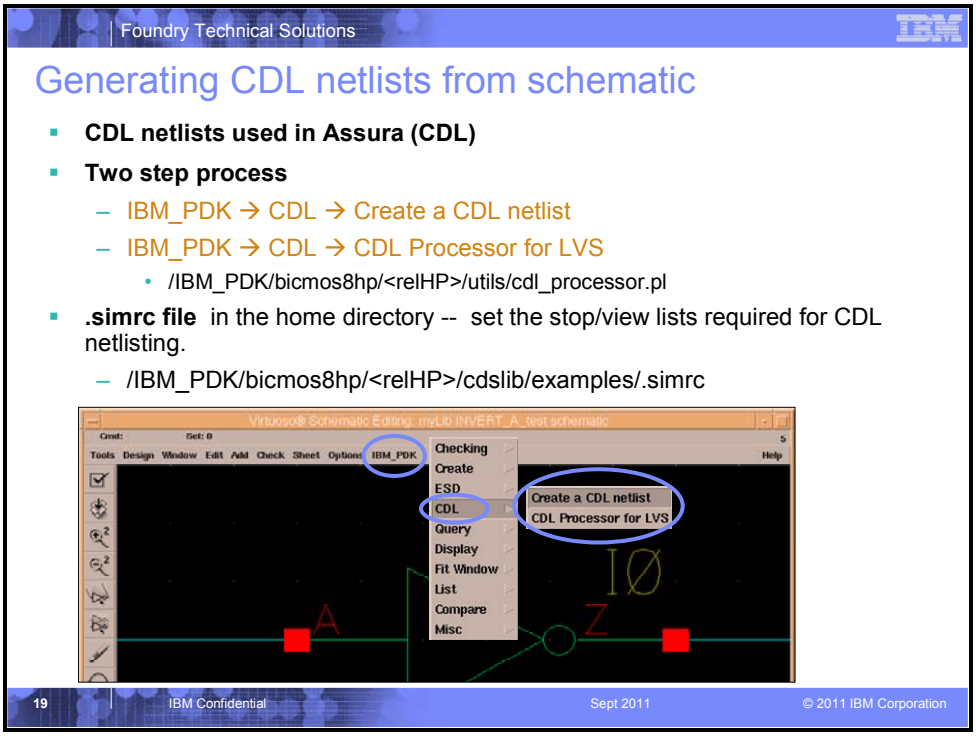
The multiple ground rules involving floating gates, n-wells and metal pads, and the antenna rules may all be checked in Assura through IBM_PDK → Assura → Floating Gate. Switch settings may be used to run only a sub-set of the rules. "bicmos8hp.AssuraDRCLVS.users_guide.pdf" and "bicmos8hp.AssuraDRCLVS.rel_notes.pdf" are supported in /libraries/IBM_PDK/bicmos8hp/<relHP>/Assura/doc, including the detailed info of the decks, such as tested tool version, usage, features, known limitations, etc.





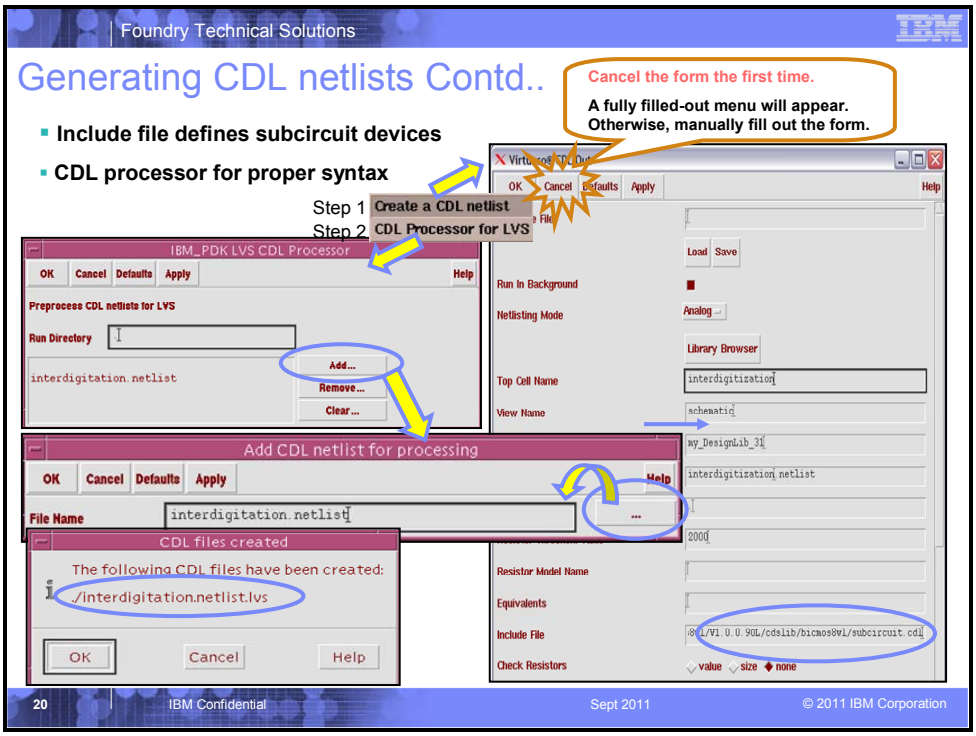
LVS (Layout versus Schematic) Verification

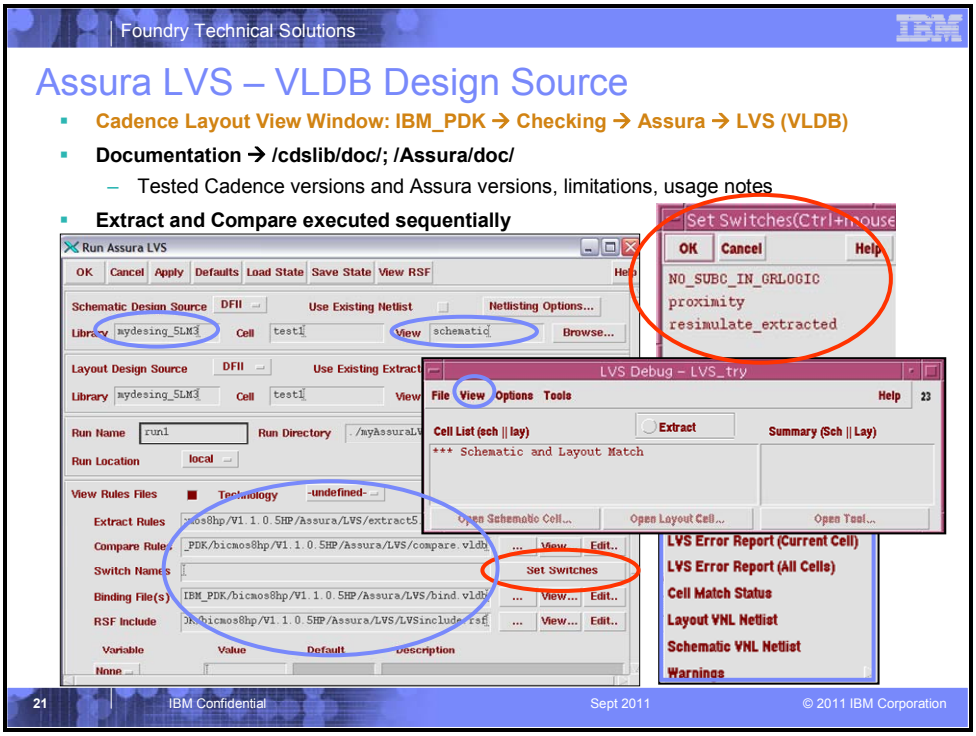
The bicmos8hp design kit supports LVS checking using Assura within Cadence utilizing the design framework II (DFII) Cadence layout and schematic data. Assura LVS also supports the usage of CDL (Component Description Language) netlists for the schematic design source. Using gds2 as the layout source is not supported in the bicmos8hp design kit for Assura LVS.



Generating CDL Netlists from Schematic

The bicmos8hp library supports the auCdl view. CDL netlists are most easily created from the schematic banner IBM_PDK → CDL → Create a CDL netlists. Due to a Cadence issue, you need to cancel out the pop up window at the first time, then the pre-filled CDL out form will appear with the design library, view, et cetera and the proper include file for devices treated as subcircuits. A CDL processor is required in order to properly format the CDL for subsequent LVS submissions. The script is located in the utils subdirectory and may also be run standalone.





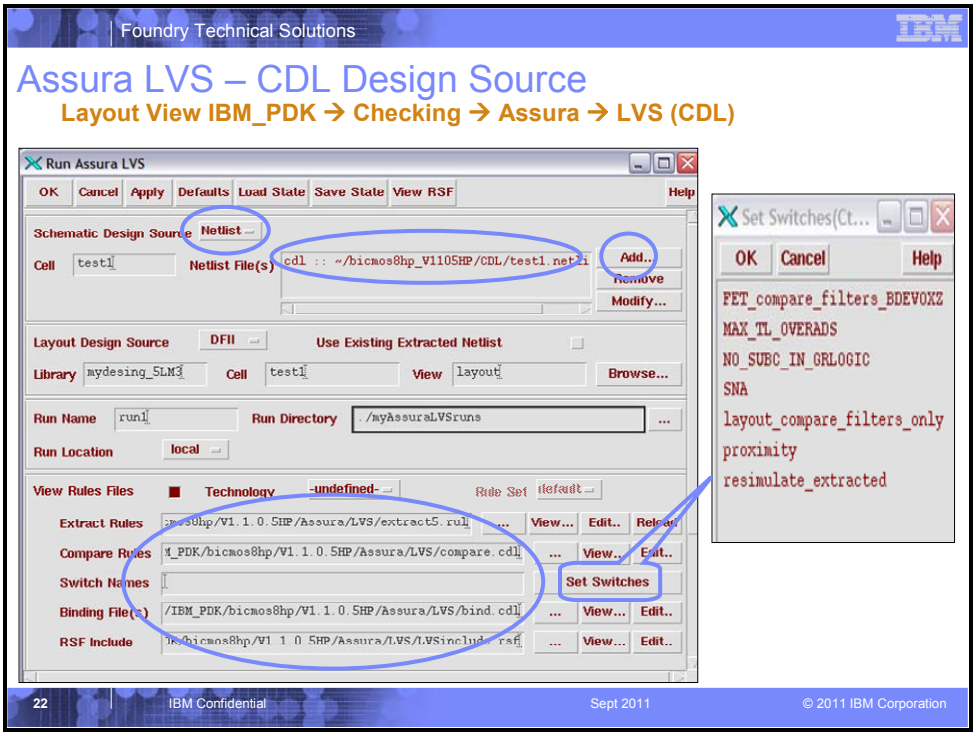
Assura LVS – VLDB or CDL Schematic Design Source

Assura LVS in bicmos8hp can utilize either the Cadence Assura schematic database (interchangeably referred to as DFII or VLDB in the menus), or a previously created CDL (Component Description Language) netlist. In either case, Assura is launched from the layout view IBM_PDK → Checking → Assura. Extraction from layout and the comparison to the schematic design source are performed sequentially. The Run Assura LVS menus are pre-filled based on the design library properties for the appropriate number of levels of metal and top metal.

Switches are provided for suppressing substrate contact device recognition in GRLOGIC regions, and for post-layout re-simulation. “Proximity” and “resimulate_extracted” switches will be explained in the “Parasitic Extraction” training section.

The slide above shows the menu obtained through IBM_PDK → Assura → LVS (VLDB).

Documentation which includes the Assura version used in deck development and testing, known limitations and usage notes is included in /IBM_PDK/bicmos8hp/<relHP>/Assura/doc.

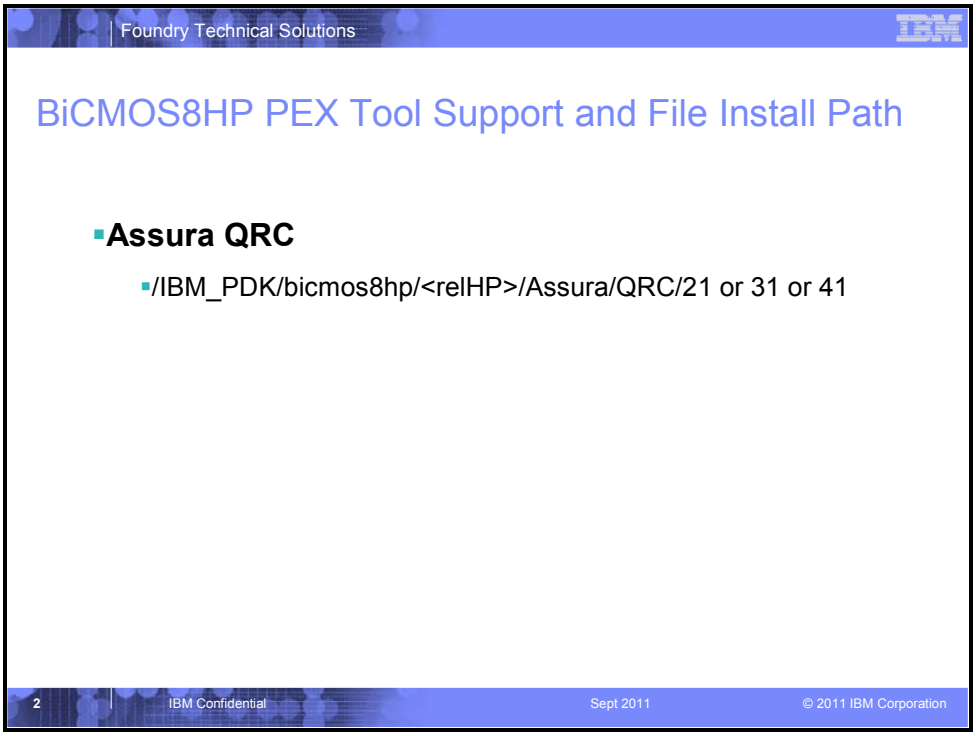


Assura LVS – CDL Design Source

The slide above shows the pre-filled menu when Assura LVS is invoked with CDL as the design source (IBM_PDK → Checking → Assura → **LVS (CDL)**.)

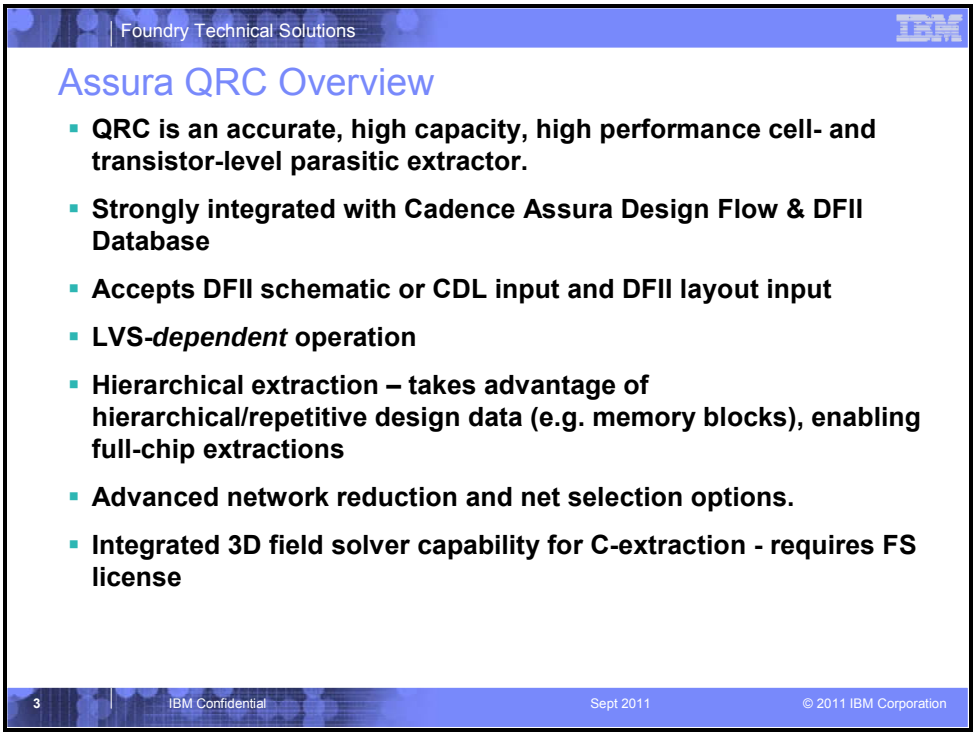
Parasitic Extraction Flows

BiCMOS8HP design kit provides support for the Cadence Assura QRC parasitic extraction tool. This module describes use of this support tool in the IBM bicmos8hp PDK.



PEX Tool Support

BiCMOS8HP PDK supports Assura QRC parasitic extraction (PEX) tool. This tool requires associated technology files for the accurate extraction of the interconnect parasitics. These files are typically packaged as separate design kit components available for download from the IBM Customer Connect (ICC) website. Once downloaded, the files can be installed using the included install script. The script places the technology files under the base design kit directory structure, as shown in the slide. The release documentation contains important information regarding the technology files, such as feature descriptions, known limitations, tool version requirements, etc. Users are encouraged to familiarize themselves with the necessary information to insure proper use of the decks. For detailed usage of extraction tools, please refer to the documentations or user's guide from tool venders.



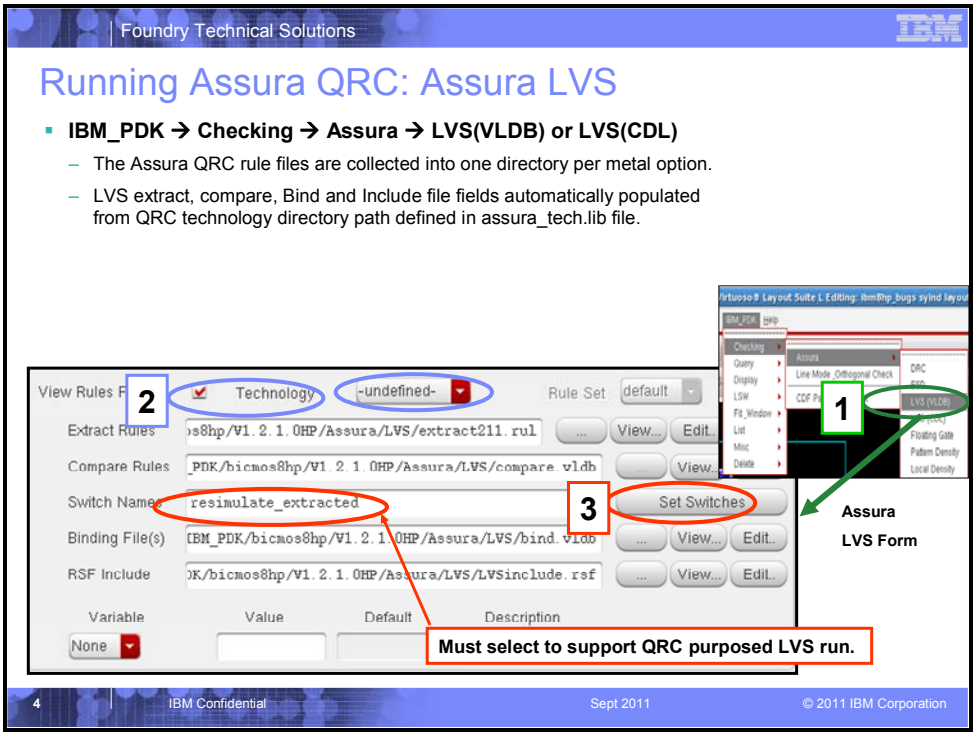
Assura QRC Overview

Assura QRC is an accurate, high capacity, high-performance cell and transistor-level parasitic extractor that is fast enough to use after every detailed routing session. QRC performs capacitance, resistance, and inductance extraction for both cell-level and transistor-level designs. It supports digital, analog, and RF designs. It performs hierarchical and flat extraction for the whole design or selected nets, for block-level or top-down design extractions.

It offers a number of extraction types (R-only, C-only, RC–decoupled, etc.), net selection options, netlist reduction options, output database formats, and process modeling capabilities. Capacitance and resistance accuracy verification has been performed by IBM. Assura QRC requires a database input that contains device and connectivity information. As a result, Assura LVS must be run prior to Assura QRC. The LVS extract rules provide device and connectivity database needed for QRC.

Assura QRC deck release note can be found in /IBM_PDK/bicmos8hp/<rel>/Assura/doc. For further information regarding Assura QRC, consult Assura User Guide from Cadence.

Assura QRC support may not be available for all supported metal options. Please check with fdrytech@us.ibm.com for available QRC metal options. If a desired metal option support is not available, please contact your IBM FAE.



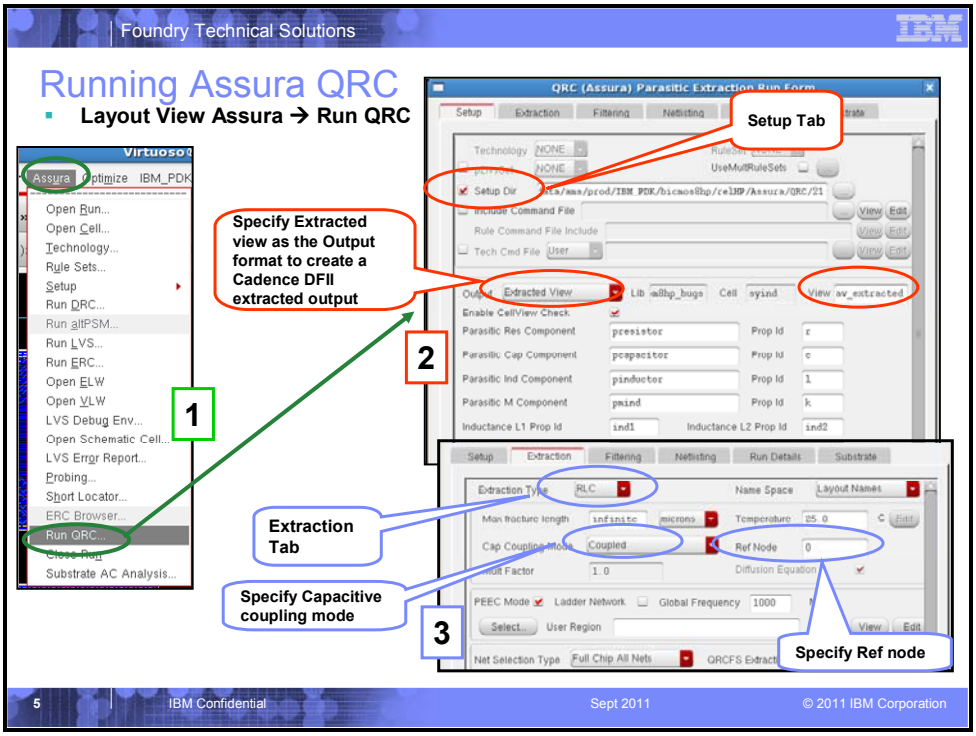
Running Assura QRC: Asuura LVS

Assura LVS needs to be run first to extract parasitics. A number of BiCMOS8HP technology related files are needed to run Assura LVS. These files are a combination of standard Assura LVS rule files and QRC technology files. These LVS/QRC rule files must be contained in the same directory structure. To accommodate this requirement, the design kit Assura/QRC/<metal_stack> kit directory contains the appropriate QRC technology files and symbolic links to the appropriate LVS rules files found in the Assura/LVS directory. To run the LVS portion of QRC extraction, users should reference the Assura/QRC/<metal_stack> kit directory as the source for LVS run.

Assura LVS run can be initiated from a pull-down menu in the Cadence layout editor, as shown in the slide above. Rather than require the user to enter a number of Assura LVS files in the Assura form fields, a method of managing the form field inputs is made possible by the definition of an ‘assura_tech.lib” file, defined in the user’s Cadence run directory. Assura reads the path definition in this file and semi-automatically (the user must select the “Technology” option in the Assura form) populates the Assura LVS form fields with the appropriate LVS file definitions.

The *resimulate_extracted* switch must be specified by the user in the Switches field. The switch will enable LVS to extract parasitic diodes.

With the primary inputs to the Assura form defined, the user can execute Assura LVS run to obtain the extracted database needed for the subsequent QRC run. Further information on Assura LVS may be found in the “Verification” training presentation.



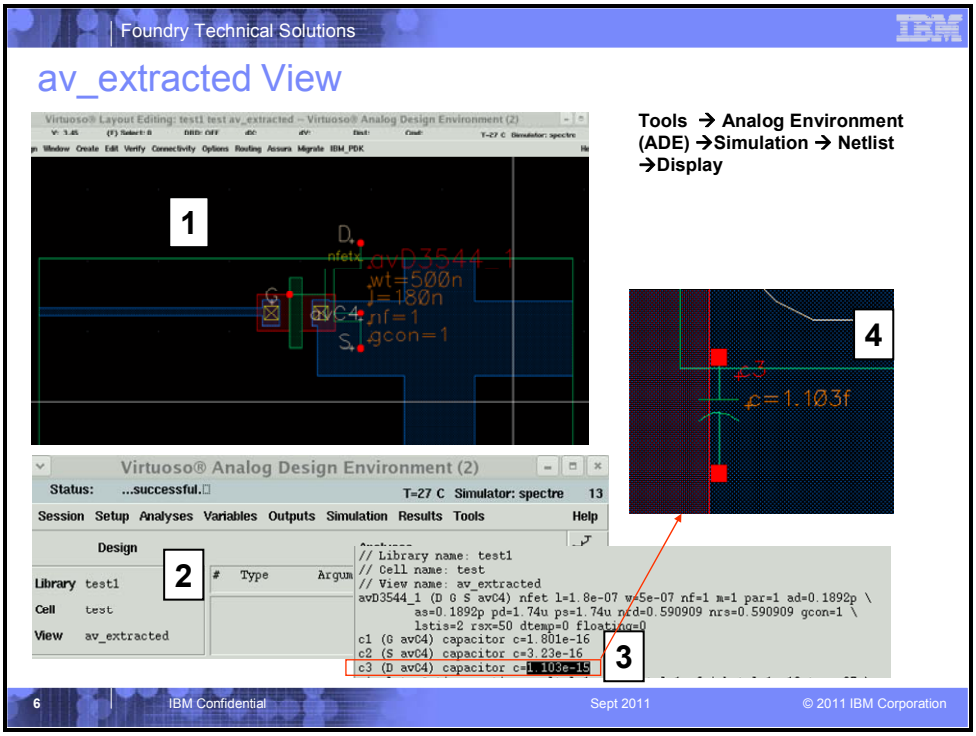
Running Assura QRC

With the layout extracted database available to QRC, the *Run QRC* menu command option is enabled in the user's layout editor window (For an initial QRC run, the user may have to open the extracted database through the Assura→Open run command available in the layout window). Selecting the *Run RCX* menu command opens the Assura QRC GUI. The QRC GUI, shown above, contains several tabs that are used to specify various QRC run options.

Briefly, the minimum QRC extraction options require the user to specify the desired *Output* database format, *Extraction Mode* (R, C, RC, etc.), *Cap Extraction Mode* (decoupled or coupled), and *Ref Node*. *Ref Node* is needed for any form of capacitance extraction and must represent a physical node in the layout, usually the substrate. *Ref Node* is used as a reference net for the decoupled capacitance extraction option.

A typical Cadence flow output format is *Extracted View*, which creates a DFII database. The *Extracted View* output contains interconnect shapes, device recognition shapes, symbolic designed devices, symbolic parasitics devices, and connectivity information.

Further explanations of QRC (and LVS) options are available in the Assura User's Guide.



av_extracted view

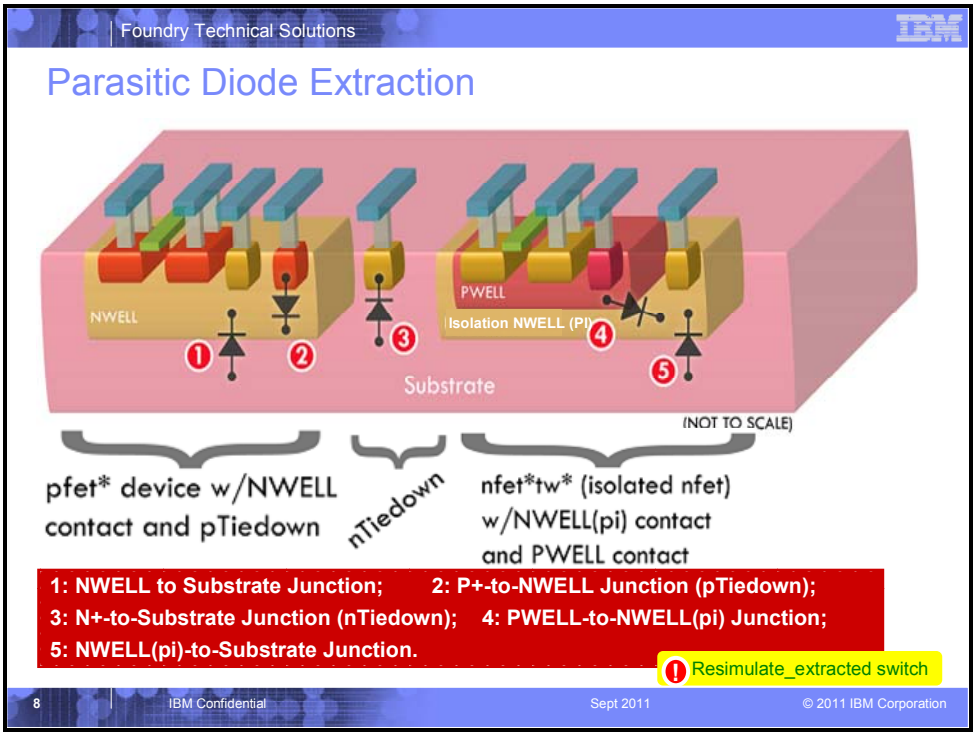
av_extracted view is an Assura QRC output format used to produce a DFII database. The symbolic parasitic R, C and L are sourced from Cadence analogLib library by default. Parasitic diffusion diodes are sourced from the bicmos8hp technology library.

If the "substrate" cell is extracted into the av_extracted view, with only a Spice view available, this extracted view can be netlisted by the Hierarchy Editor tool for re-simulation purpose. The procedure will be addressed at the end of this training session.

The BiCMOS8HP design kit supports a list of utilities to query, display, zoom in and list desired extracted design device instances as well as parasitic elements for the information of properties, location, connectivity, etc. Those useful utilities are described in above slide.

BiCMOS8HP Parasitic Extraction: Special Topics

- **Parasitic Diodes**
- **MIM Bottom Plate Parasitics**
- **Bondpad Parasitic Modeling**
- **Parasitic Simulation Netlisting**



Parasitic Diode Extraction

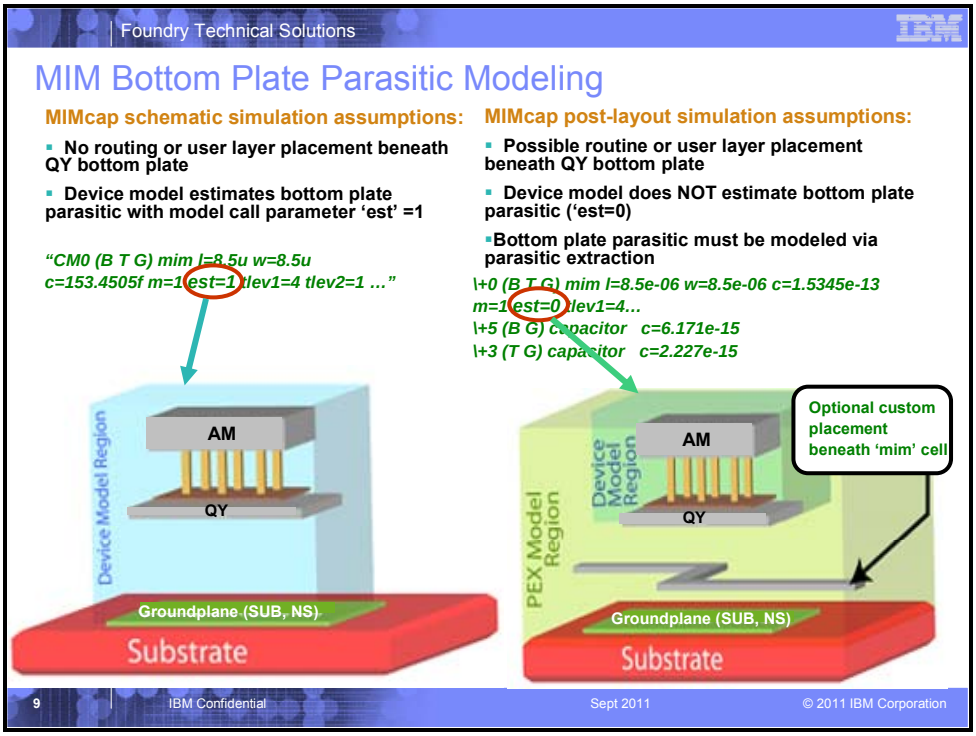
A number of different PN diode junctions are formed when designed devices or tie down elements are placed in a layout. Some of them form intrinsic portions of a designed device, and therefore their electrical behavior is accounted for in the device model.

There are, however, a number of PN junctions that either belong to no intrinsic device model (e.g. tie down diodes) or have size parametrics that can only be definitively established in the layout phase of the design cycle (e.g. an NWELL enclosing an arbitrary number of PFETs). Five types of PN junctions shown in the above slide are typically associated with the PFETs, isolated NFETs, and tie-down devices.

To account for their electrical behavior, these types of PN junctions are extracted as parasitic diodes with appropriate perimeter and area parameters consistent with the junction dimensions. (Make sure **resimulate_extracted** switch is selected when using Assura extraction flow.)

Parasitic diodes extraction is important for the following considerations:

- Large area junction diodes can contribute significantly to node capacitance, causing measurable circuit performance degradation.
- Because of the nature of junction capacitance, the capacitive load is non-linear with respect to the applied signal, causing linearity degradation on signals sensitive to capacitive loading.
- Parasitic diodes must not enter a forward bias condition in normal operation. Since forward biased operation or parasitic diodes typically yields significant changes in simulated circuit performance, extraction and re-simulation with parasitic diodes can high-light unanticipated forward biasing of these junctions, and prompt corrective action prior to design sign-off.



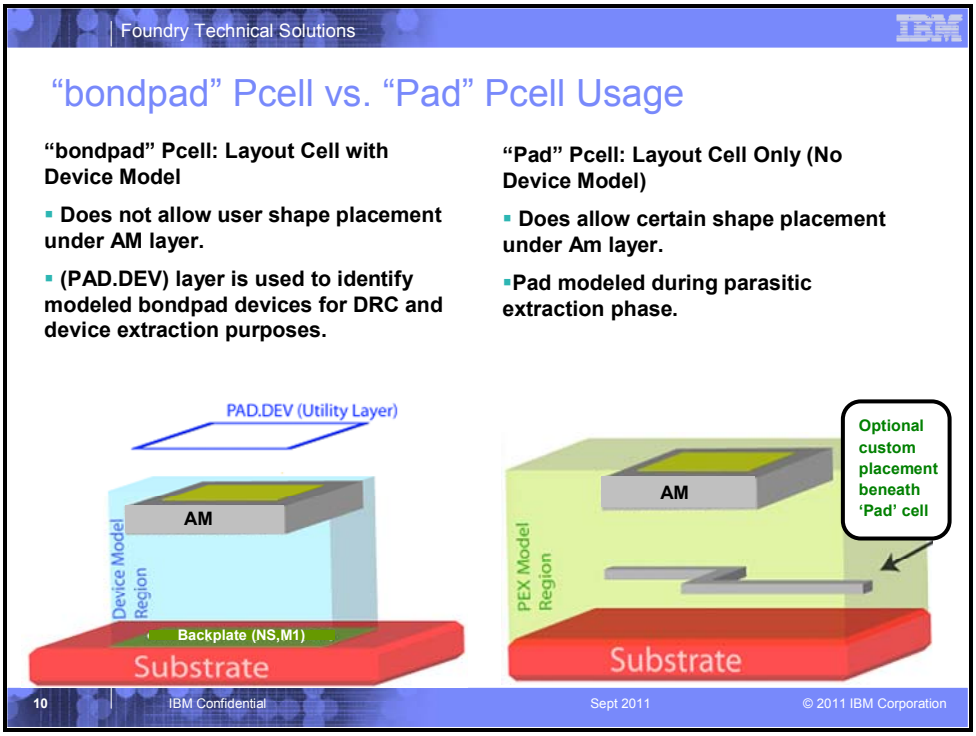
MIM Capacitor Bottom Plate Parasitic Modeling

In BiCMOS8HP technology, MIM capacitor model covers parasitic resistance of top plate (AM) and bottom plate (QY), via (AV) resistance and parasitic capacitance to substrate from the bottom plate. The bottom plate parasitic capacitance calculation can be turn on/off via mode instance switch (*est*).

In the above slide, the graphic on the left represent a MIM capacitor device as it is modeled for schematic simulation proposes. Of particular interest is that the QY bottom plate parasitic is included in the MIM device model. It is assumed no user shape placement is included below the MIM QY bottom plate. The bottom plate parasitic is included in the model by the device switch (*est*) which, when set to 1, included the parasitic in the model.

The graphic on the right in the slide above shows the case where this MIM device has been extracted from the layout. By design, the extracted MIM "*est*" device parameter is set to 0, indicating the MIM bottom plate parasitic is not included in subsequent device model calls. This feature allows the parasitic extraction tool to extract the bottom plate parasitic of the MIM device, regardless of layer placement beneath the QY bottom plate, allowing inclusion of parasitic affects that arise from shape placement beneath the device.

Simulation from a device-only extracted database will not include the MIM capacitor bottom plate parasitic (since est=0) and simulation results will differ from schematic simulation results for this reason.

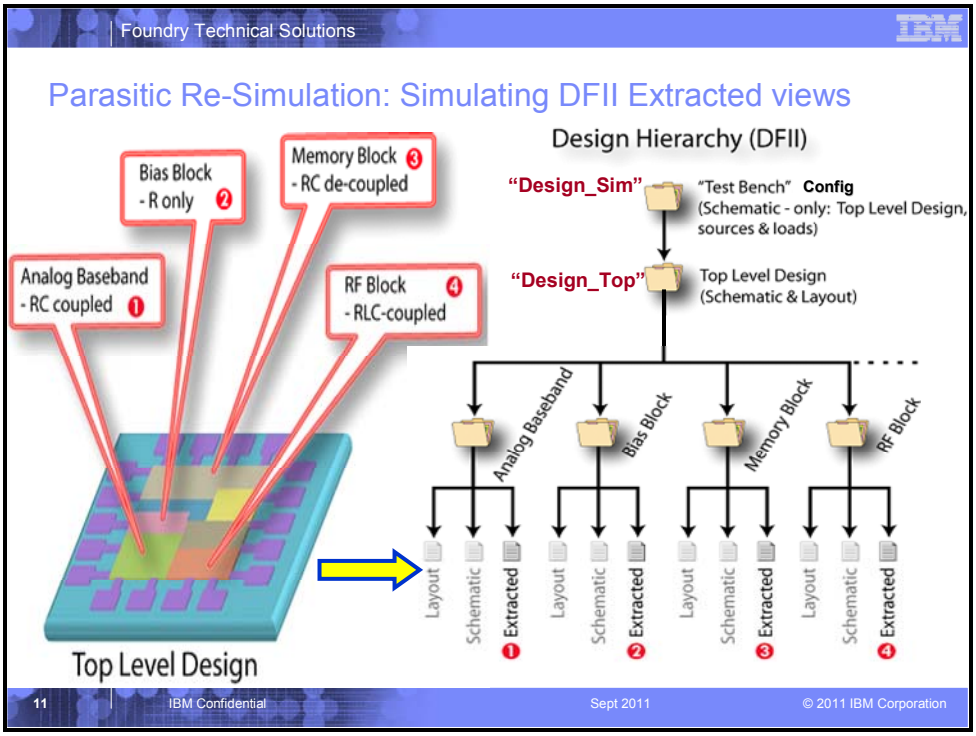


Bondpad Parasitic Modeling

Area under wirebond or C4 chip terminals can be used for interconnect routing or fill shape placement. However the design kit *bondpad* devices are modeled to include a parasitic from the pad metal to the selected device Backplate (NS or TI) Therefore, to protect the accuracy of the model, no shape placement is permitted beneath the design kit *bondpad* devices.

To accommodate layer placement under wirebond (or C4) devices, the *Pad* design kit library device is offered. The *Pad* device is a layout-only PCell with no model support. It has an option to support both wirebond and C4 pads. Modeling of the *Pad* cell is accounted for only during parasitic extraction, as the pad metal (LD) is treated as any other interconnect, and parasitic interaction with layers beneath the pad metal are taken into account.

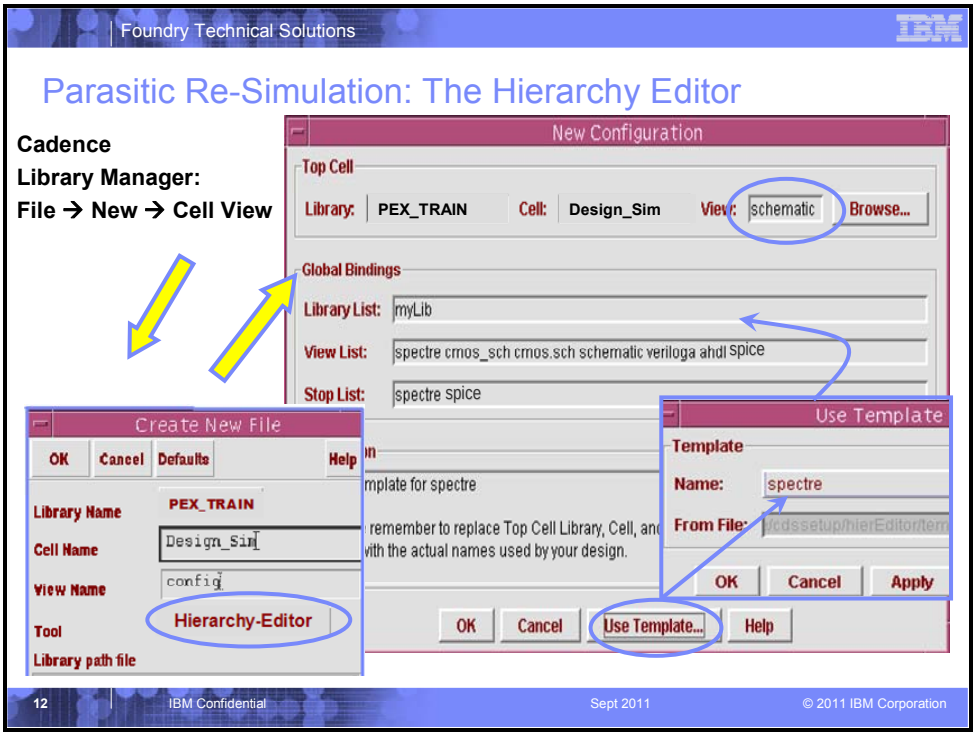
The primary distinguishing feature between the *bondpad* PCell and *Pad* PCell is a non-build utility layer (PAD.DEV), which is included in the *bondpad* cell and is used to identify modeled *bondpad* devices for DRC and device extraction purposes.



Parasitic Re-simulation – Simulating DFII Extracted Views

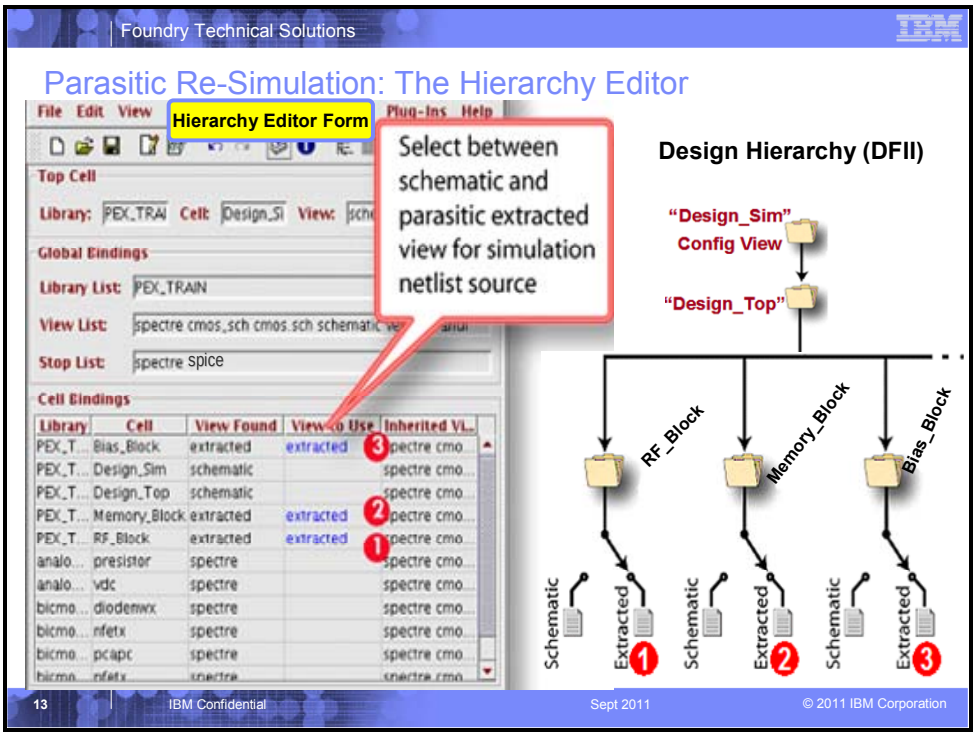
Detailed parasitic extracted netlists can introduce thousands of parasitic elements and additional circuit nodes within a design. Even with parasitic extraction tool netlist reduction features, netlists can become so unwieldy that top-level circuit simulations become practically impossible, as simulation times become unreasonably long.

A common method used to manage netlist complexity is to divide the top-level design into a hierarchy of circuit/system blocks, which typically have different parasitic extraction requirements. Minimal parasitic extraction on non-critical or parasitic insensitive circuits can significantly reduce the overall netlist size and complexity. The above slide demonstrates a chip-level design where a detailed extraction (RLC) is performed on an *RF* block, and RC de-coupled extraction is performed on the *Memory* block, and so on – resulting in a more manageable netlist size. The partitioned DFII database can then act as a source for the Cadence Hierarchy Editor (discussed next) to produce a top-level simulation netlist.

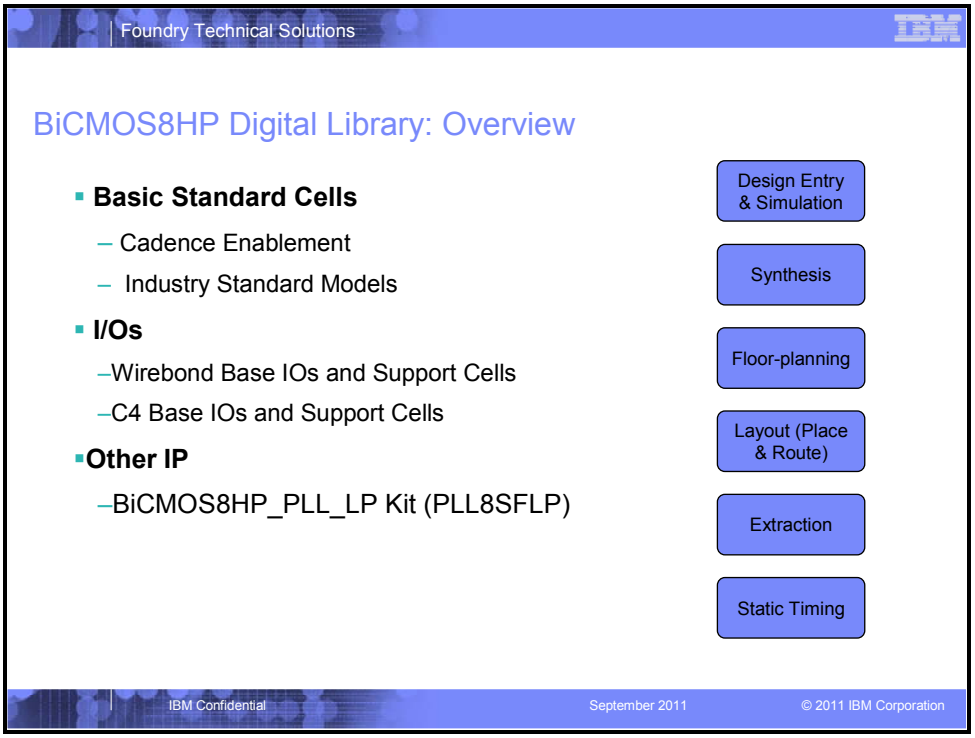


Parasitic Re-simulation: The Hierarchy Editor

The Hierarchy Editor is a flexible tool that allows for various combinations of views that can be used for simulation. User can specify parasitic extracted DFII database blocks for the source of top-level netlist creation, permitting re-simulation of the design with parasitics included. The slides on this page demonstrate how the hierarchy editor is used to refer to the parasitic extracted cellviews as the simulation netlist sources from top-level simulation testbench cell *Design_Sim*. For More information on the Hierarchy editor, consult the relevant Cadence documentation.



Digital Library

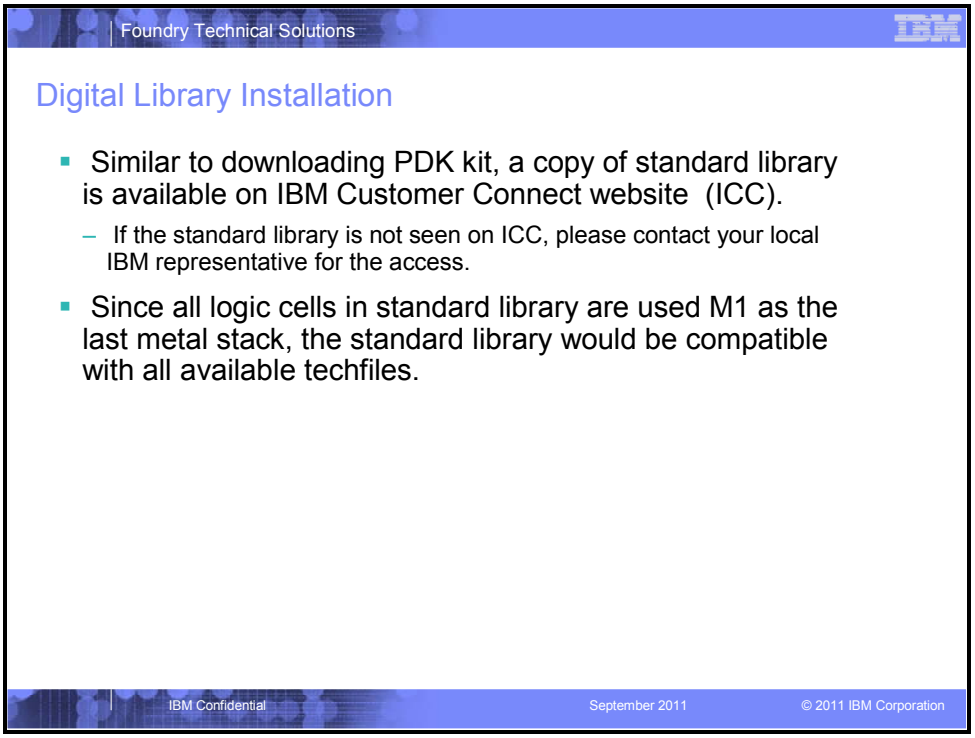


BiCMOS8HP Digital Library Overview

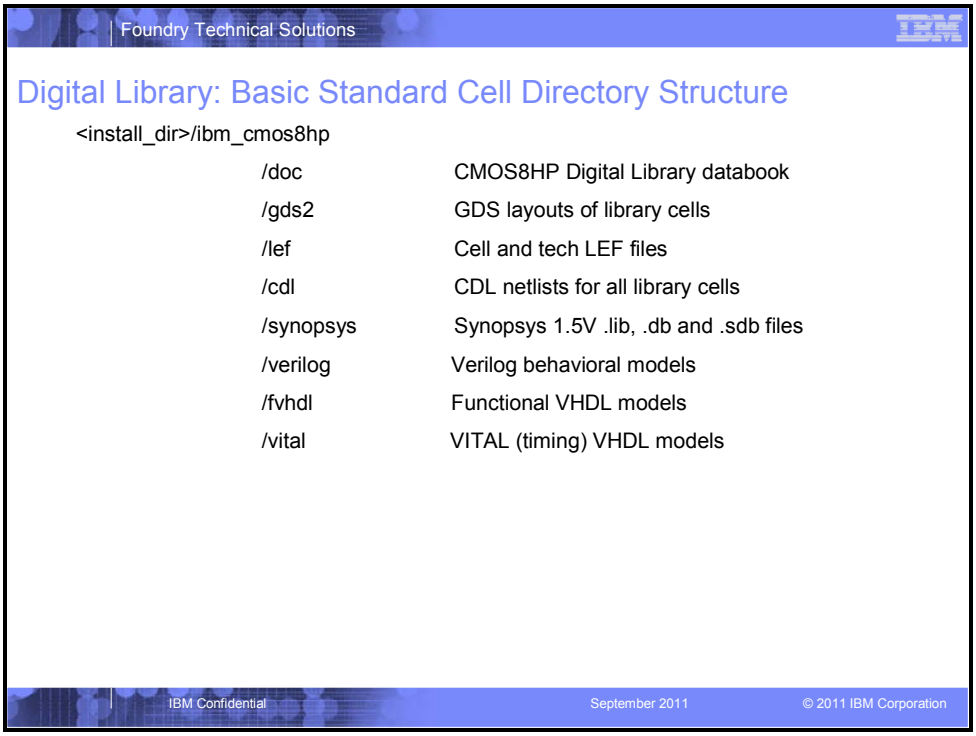
The digital design kit for BiCMOS8HP contains a robust set of standard cell circuits that are required for digital components of 0.13µm chip designs. Cadence enablement is provided to support mixed-signal circuit development and interfaces between digital and analog/RF circuitry.

Typical customer owned tooling (COT) flows can be quite variable. A simple flow is described in the diagram on the right. The digital design kit for BiCMOS8HP attempts to provide the most commonly used models (*e.g.* GDS2, LEF, .lib, *etc.*) required for each part of the flow. Models that aren't available in the initial digital design kit may be requested through your IBM Field Application Engineer (FAE).

IBM may optionally provide other digital IP (intellectual property) also. I/Os, Memories, Register Arrays, and microprocessors are ported from IBM's Cu-11 ASIC library. *If other metal stacks, I/O types, memories, register arrays, macros/cores or microprocessors than listed here are needed, they may be optionally made available by requesting through your IBM FAE.*

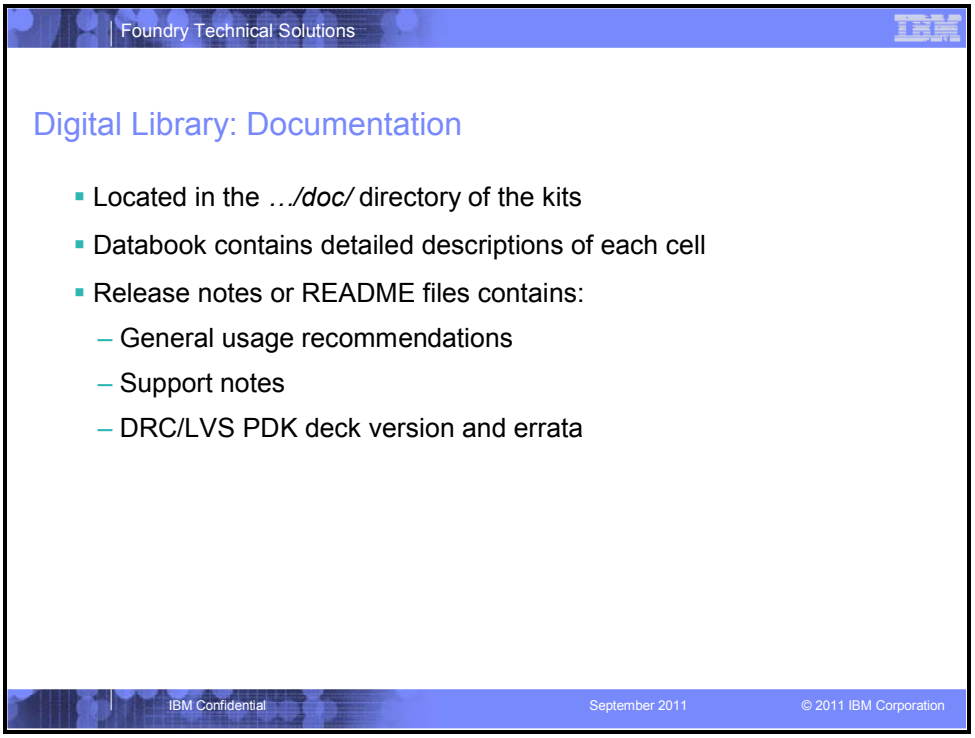


Digital Library Installation



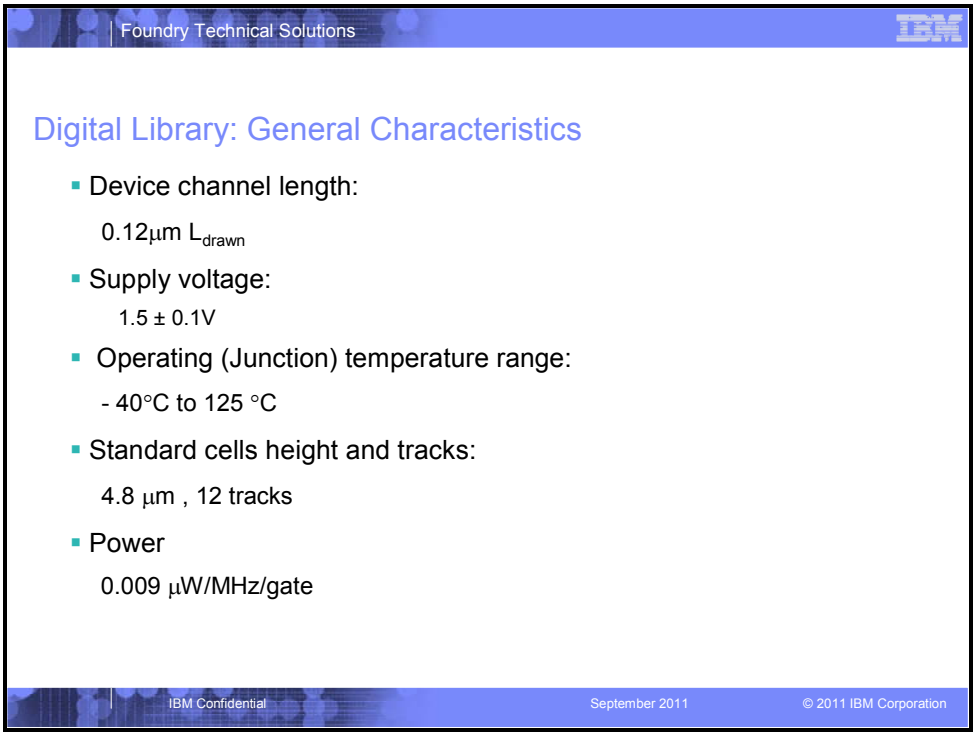
Basic Standard Cell Directory Structure

The digital design kit for the standard cells is provided as a group of directories as shown above. Each directory contains models for the basic standard cells and documentation.



Documentation

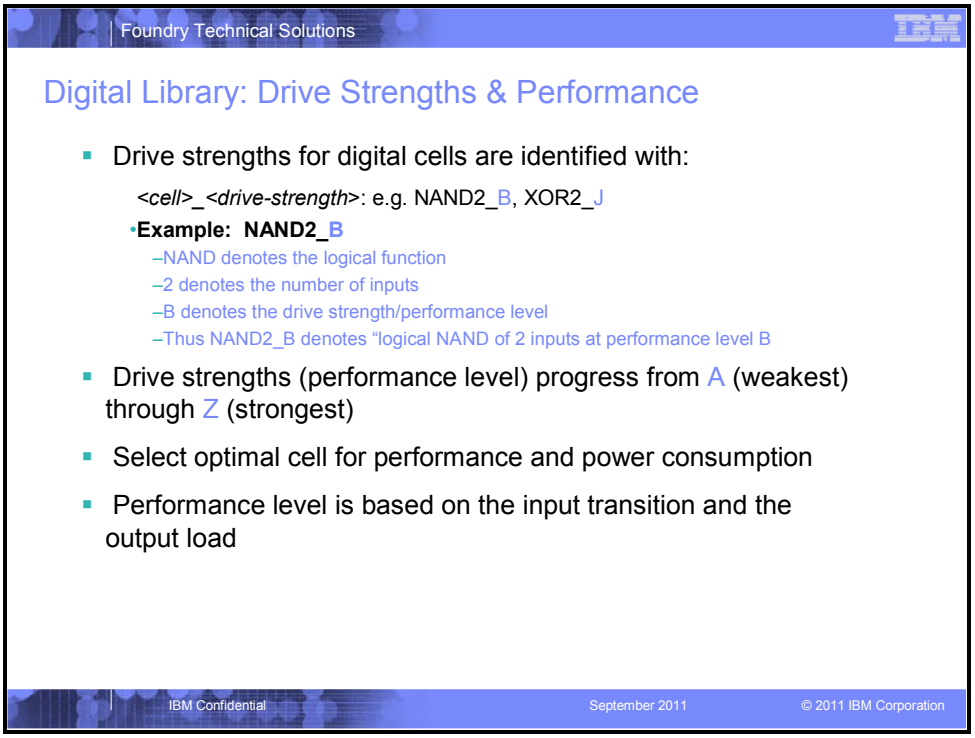
Documentation for the standard cell library can be found in the 'doc' directory. Release Notes and/or README files may be included in the kits that contain usage information, support notes, and errata regarding DRC and LVS runs on the intellectual property (IP).



General Characteristics

The standard cells are implemented in a 0.13µm lithography process for 1.5±0.1V supply voltage. Operating (junction) temperatures are from -40°C to 125°C.

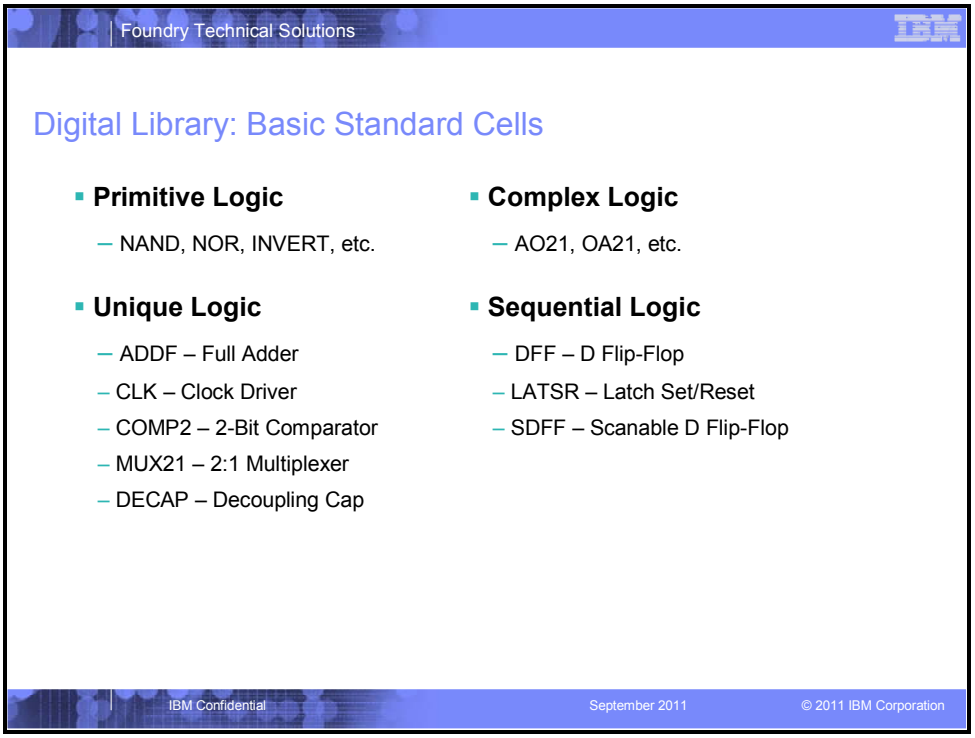
Each cell is designed as 4.8µm in height with 12 wiring tracks. The cells are optimized for overall performance and meet general applications requirement.



Drive Strengths and Performance

Cell drive strengths are identified with an underscore followed by a character after the name of the cell. For example, NAND2_A is the weakest (and smallest) NAND2 cell. NAND2_B, NAND2_C, *etc.* are progressively stronger cells. The robust sequence of performance options helps synthesis tools to optimize paths for both performance and power consumption.

Performance of a cell is a function of the input transition and the output load.



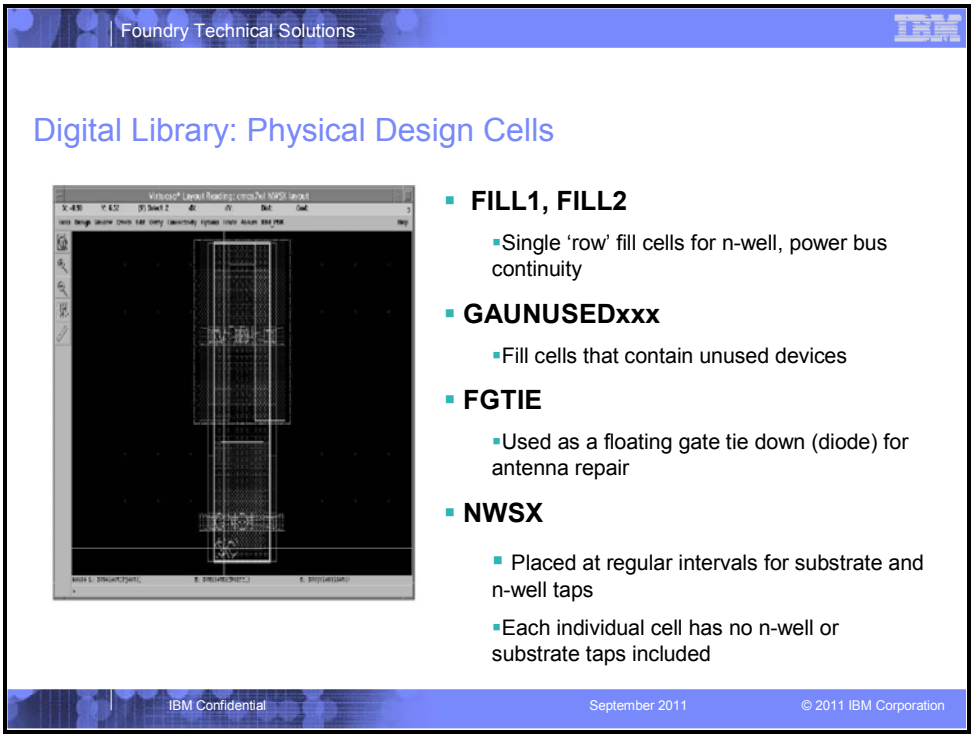
Basic Standard Cells

Basic standard cells of various drive strengths (*i.e.* performance) are provided in the digital design kit. These range from standard combinational logic gates like NAND, NOR, and INVERT cells to more complex logic gates, like a full adder cell (ADDF) and 2-bit comparator (COMP2).

Complex logic is provided to optimize performance and area for certain Boolean logic functions (*e.g.* AO21, AOI2222, OAI21, *etc.*).

Sequential logic is provided featuring standard flip-flops, scannable flip-flops, and latches.

For more information, see /<install dir>/ibm_cmos8hp/doc/cmos8hp_rvt_databook.pdf and README files.



Physical Design Cells

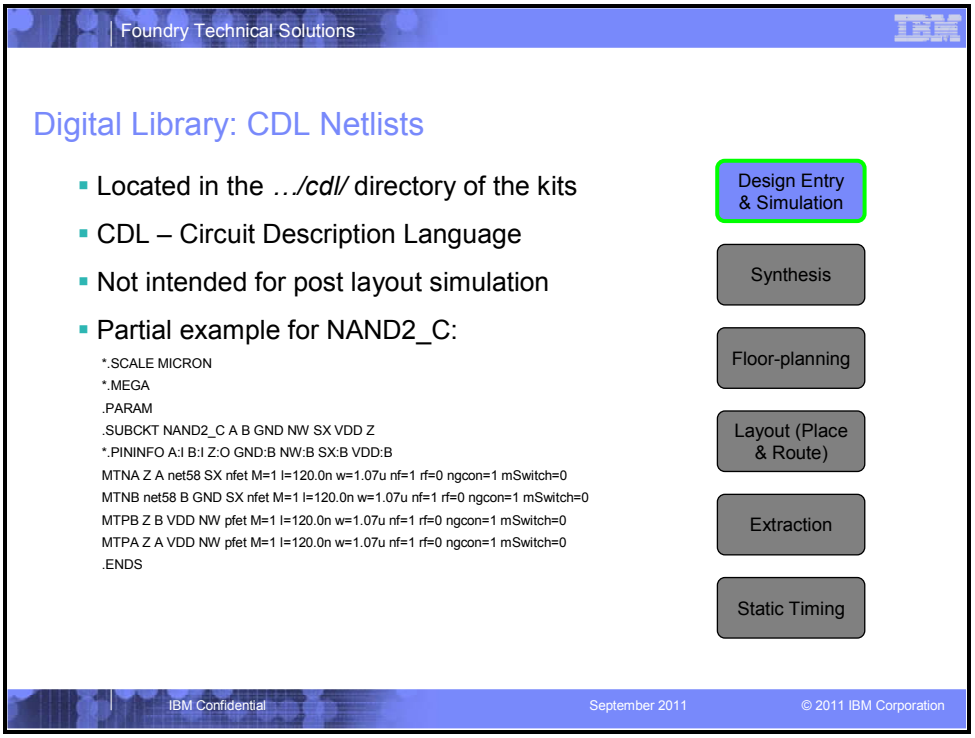
Physical design cells are provided for various operations.

The *FILL1* and *FILL2* cells are fill cells for the n-well and power bus continuity.

The *GAUNUSEDxxx* cells are larger cells that contain gate array background shapes including spare transistors for BEOL (back-end of the line) metal changes. Note that these cells are not intended to meet pattern density requirements. Rather, they are fill circuits for unused slots/sites in the chip design. The xxx stands for 000, 006, 012, 024, 048, 096.

The *FGTIE* cell can be used for repair of antenna violations.

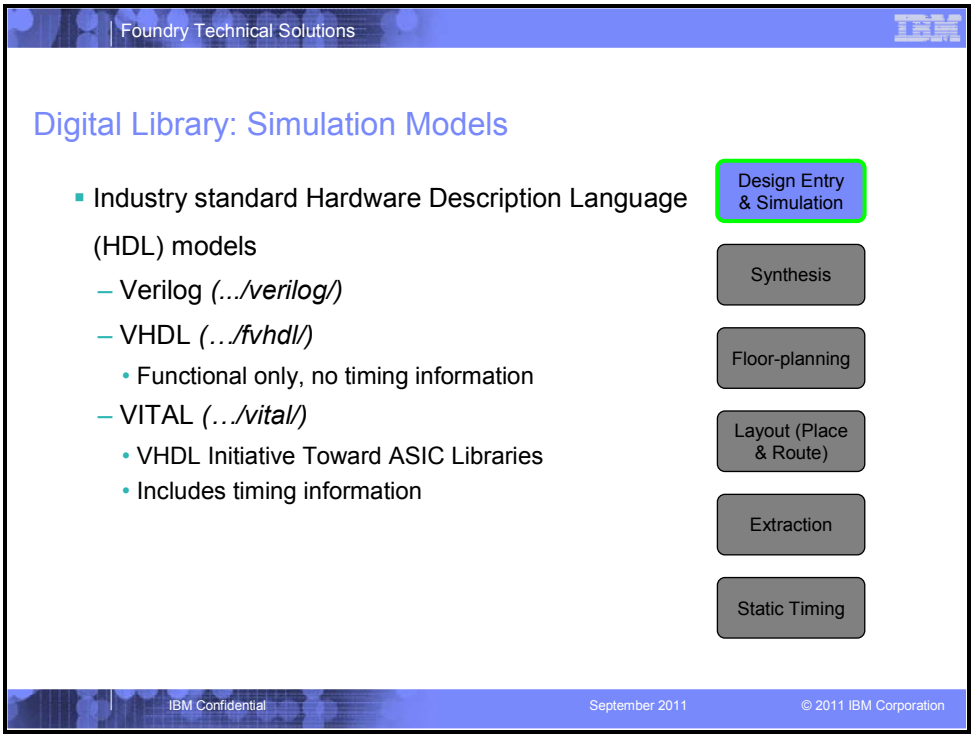
Finally, the *NWSX* cell needs to be placed at regular intervals to contact/tap the n-well and substrate to the power and ground bus, respectively, in order to meet the ground rules. Note that IBM's digital cells do not have n-well or substrate taps in each individual cell.



CDL Netlists

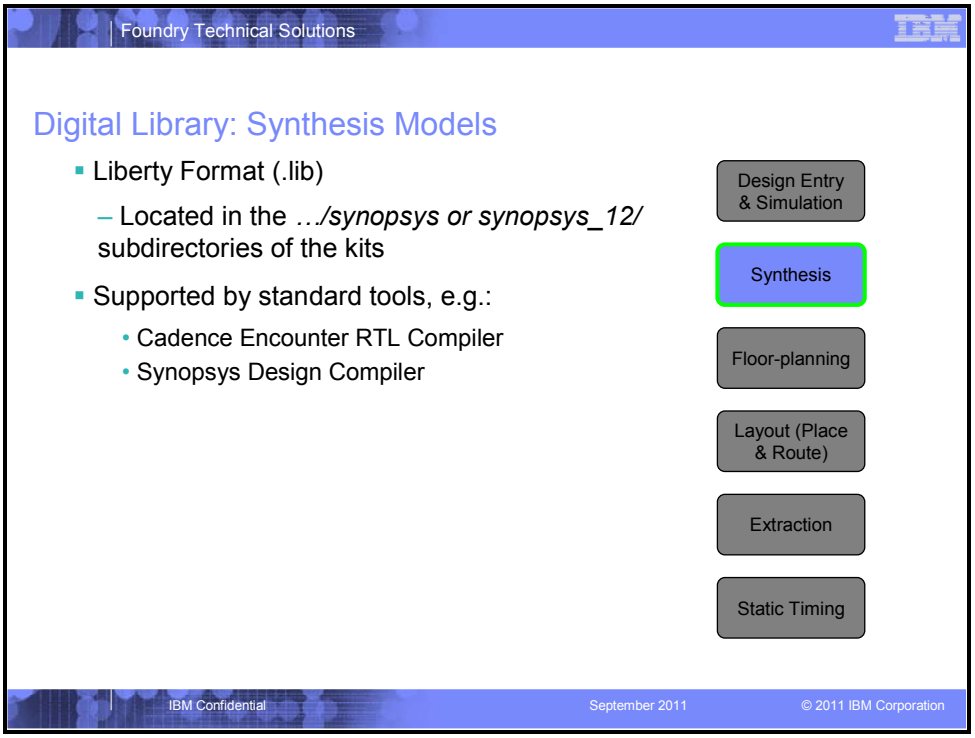
CDL netlists are provided as source/schematic representations of standard cells for LVS.

The BiCMOS8HP PDK supports Assura LVS which support CDL for the source netlist of the circuit.



Simulation Models

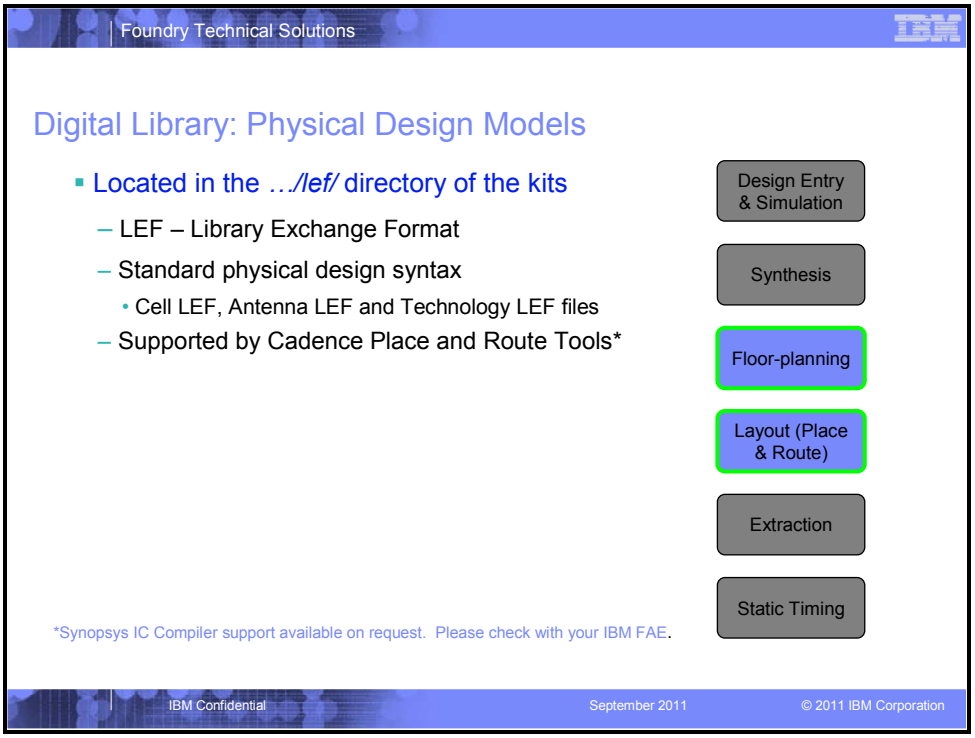
The simulation step of typical design flows selects circuits from the standard cell library to simulate the function of the chip netlist. For this step, standard Hardware Description Language (HDL) models—Verilog, VHDL, and VITAL--are provided in the digital design kit to model circuit functionality.



Synthesis Models

The physical synthesis step of typical design flows selects circuits from the standard cell library to implement the function of the chip netlist. The models are in Liberty format (.lib files).

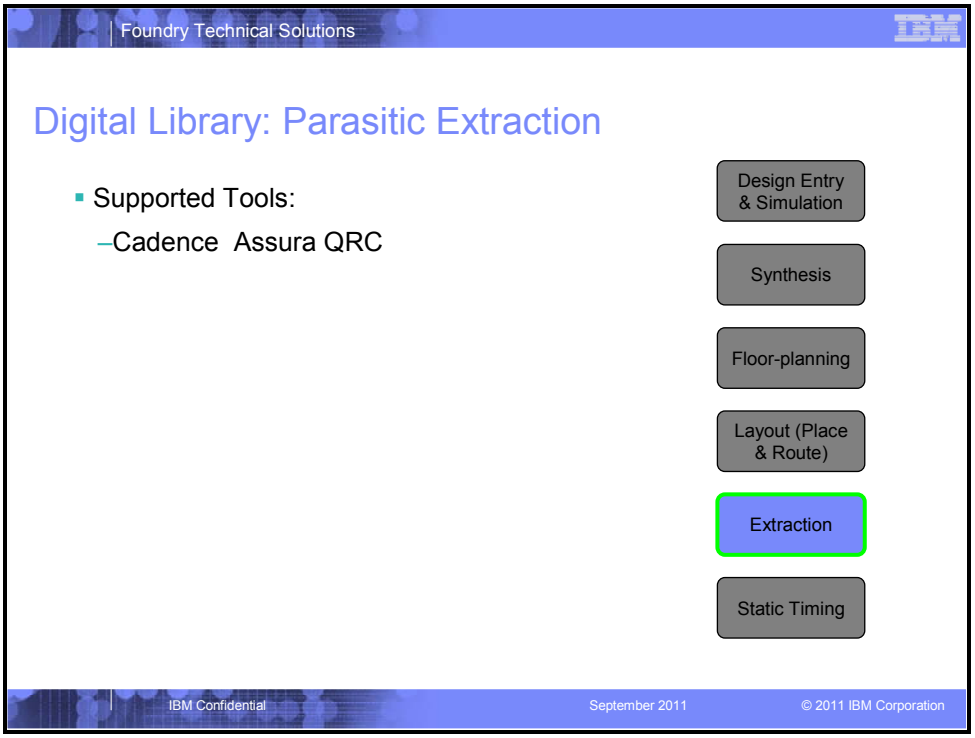
The models are supported by Cadence Encounter RTL Compiler and Synopsys Design Compiler.



Physical Design Models

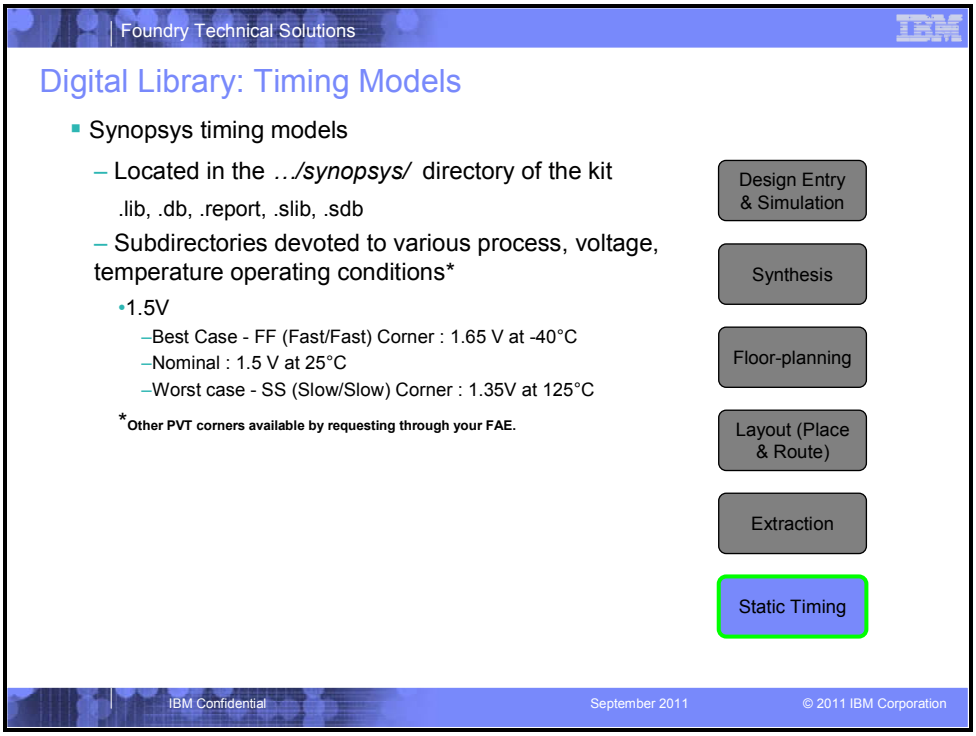
LEF models are provided which contain the input pin, output pin, power, ground, and antenna information necessary for physical design tools. Technology LEFs are provided that contain metal layer, via, and site rules for each enabled metal stack.

Synopsys IC Compiler support may be available on request. Please check with your IBM FAE.



Parasitic Extraction

The BiCMOS8HP PDK also contains extraction support for Cadence Assura QRC for device level parasitic extraction.

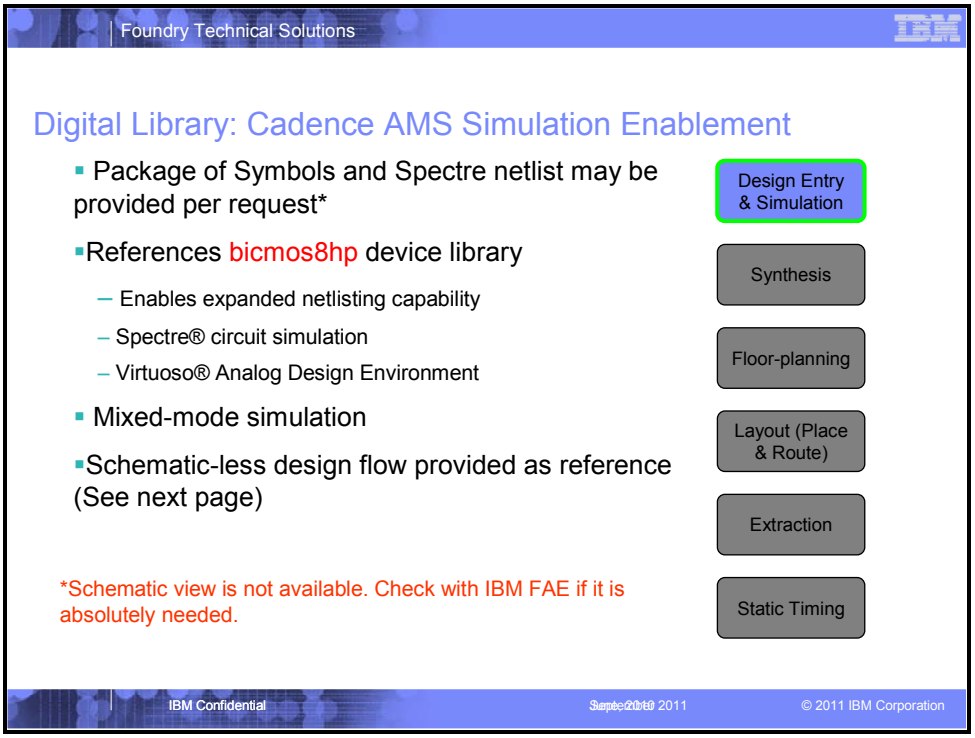


Timing Models

Synopsys models are provided that are characterized at three operating conditions (Best Case, Nominal and Worst Case):

For 1.5V cells, the best case FF (Fast/Fast) Corner 1.65V at -40°C, the nominal 1.5V at 25°C, and the worst case SS (Slow/Slow) corner 1.35V at 125°C are provided. Wire load models are available.

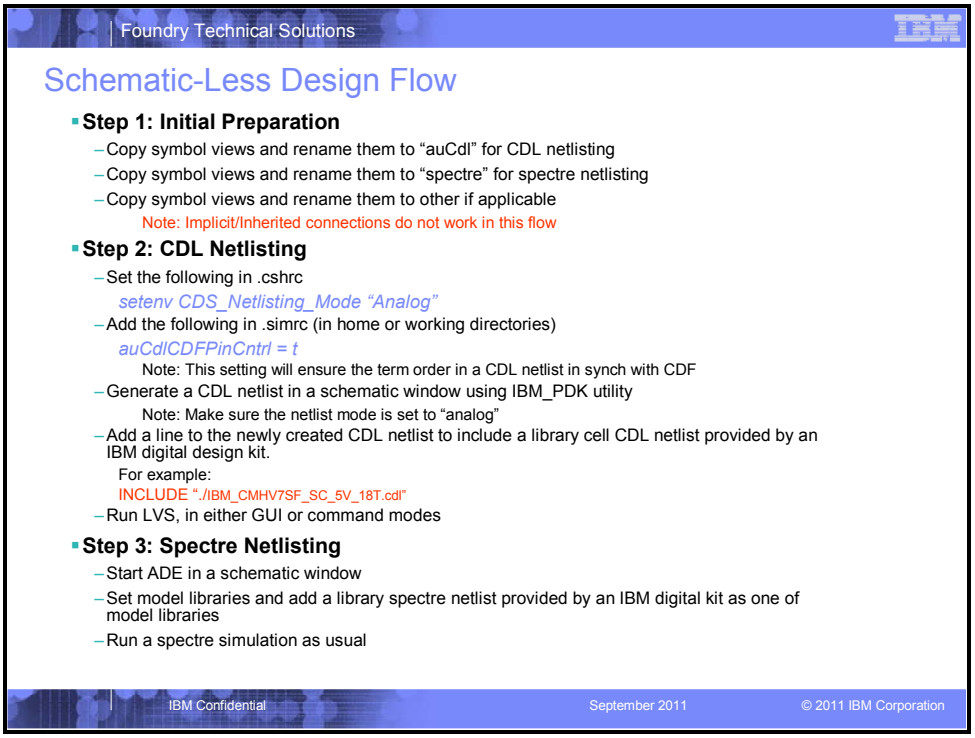
For accurate timing at other operating conditions, please contact your IBM FAE representative for models characterized at those conditions.



Cadence AMS Simulation Enablement

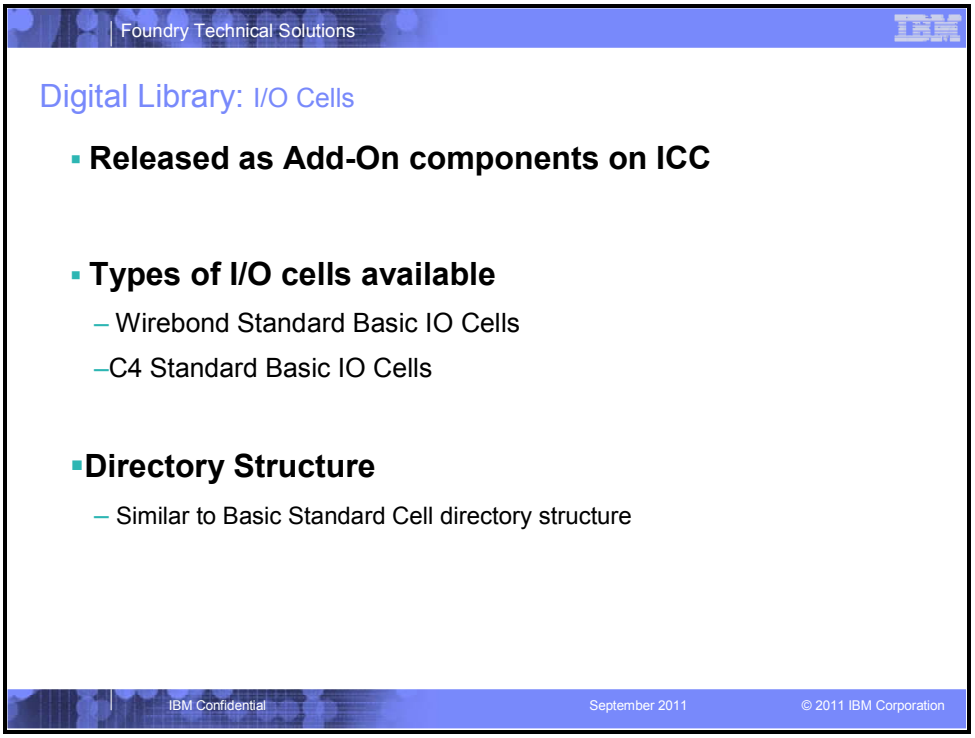
A Cadence library may be provided that contains symbol and Spectre netlist. The library references the device cellviews in the *bicmos8hp* Cadence library that is provided in the basic PDK provided by IBM. This enables netlisting capability for additional netlist formats (*e.g.* Spectre) along with use of the Virtuoso Analog Design Environment which provides Spectre simulation capability, waveform viewing, Monte Carlo analysis, etc.

Schematic view is not available. Chcek with your IBM FAE if it is absolutely needed. Please see next page that describes how the digital design flow is accomplished without schematics.



Schematic-Less Design Flow

In general, cdslib is not available for Cadence Enablement. In that case, the procedure described above can be used to perform digital designs.

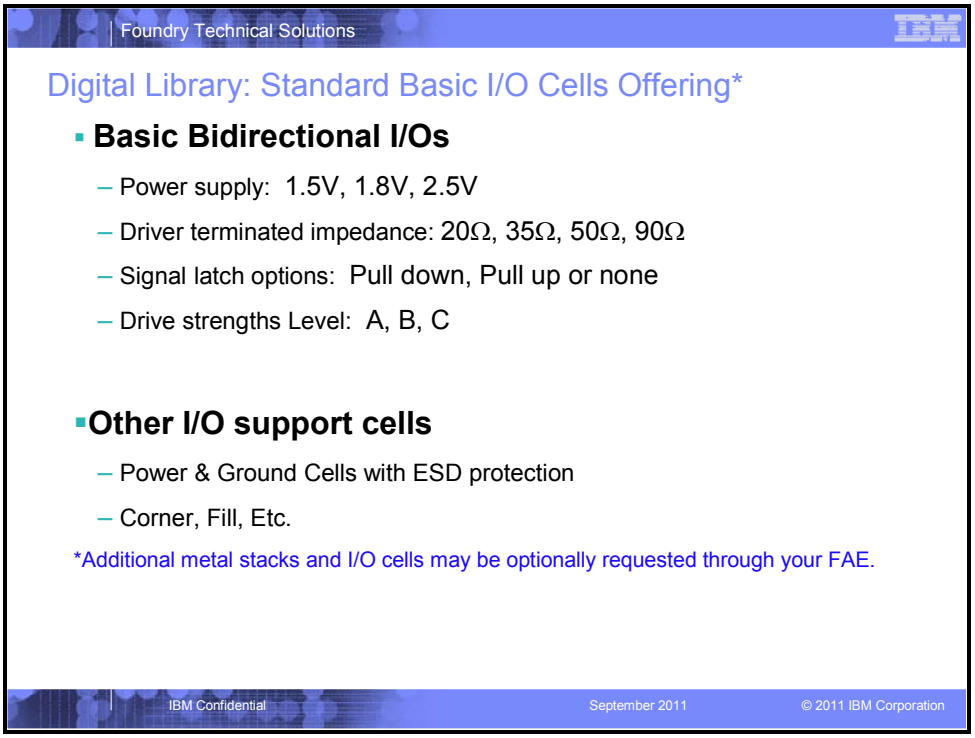


I/O Cells

The digital design kit for I/Os is provided in a separate group of directories structure similar as the standard cells. The kit is released as an adds-on component from the ICC web site.

Standard basic I/O cells are available for both C4 and wire bond.

If other I/O types are needed, please contact your IBM FAE.

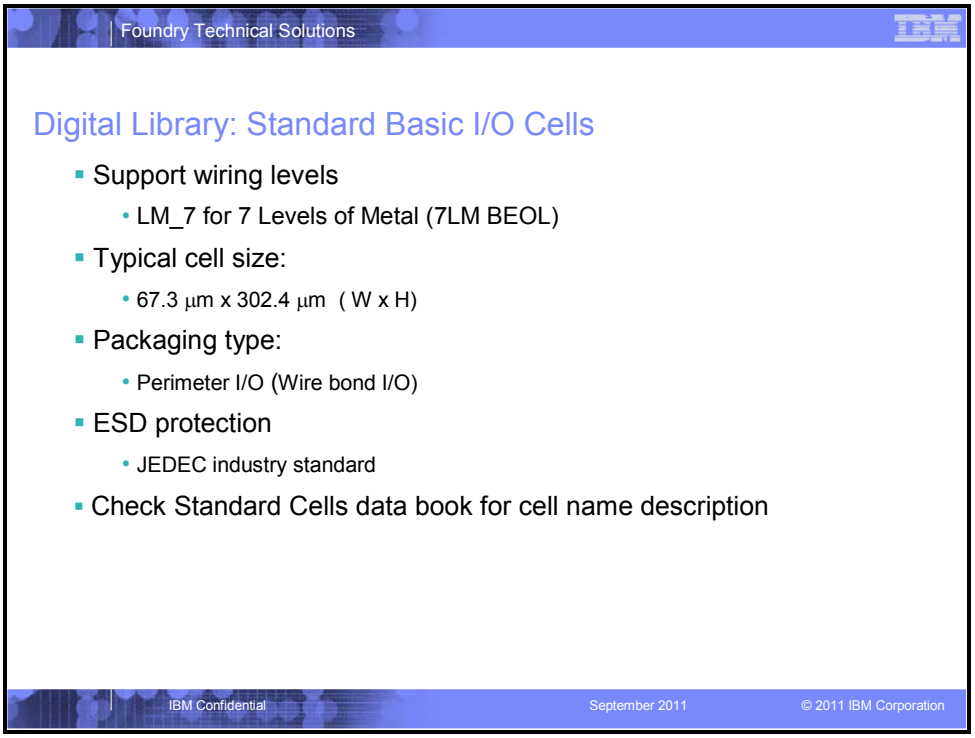


I/O Cells Offering

Basic bidirectional I/Os are provided for off-chip voltages of 1.5V, 1.8V and 2.5V. The drivers are source-terminated from 20Ω to 90Ω. With the pull-down and pull-up I/O cells the PAD pin can be set to logic '0' or '1', respectively, or in Hi-Z state.

I/O support cells are provided for I/O fill, corner, power (i.e. VDD, VDD250), and ground cells. The I/O fill cells handle empty I/O slots. The corner cells address the corners of the chip. The power cells bring power supply voltages on to the chip. The ground cells provide the ground voltage potential to the chip.

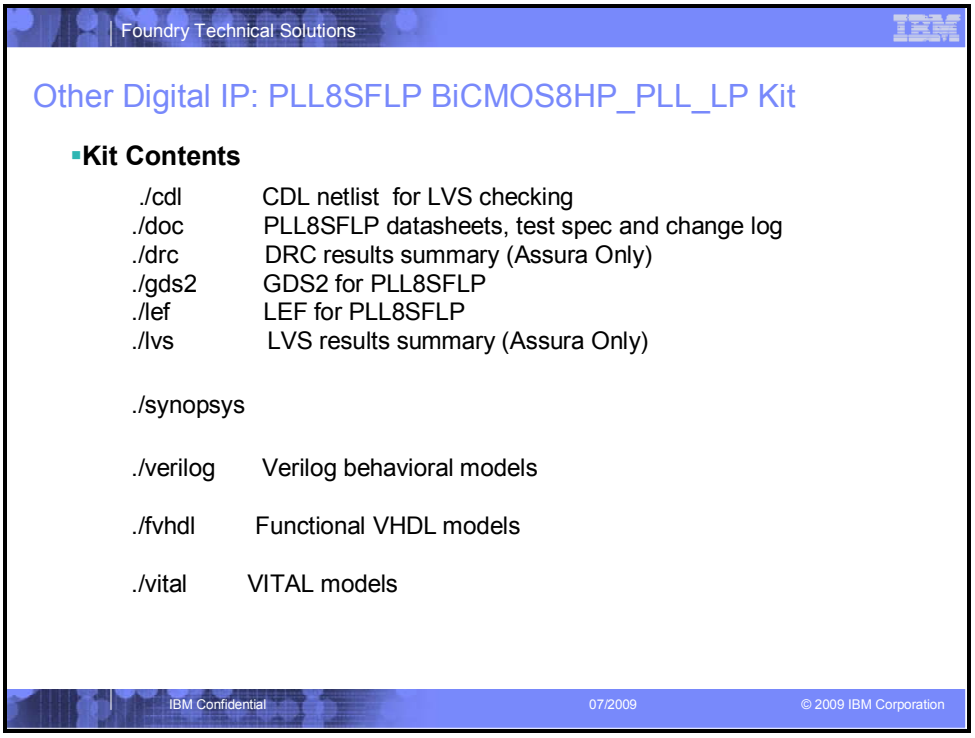
Other metal stacks and I/O types may be optionally made available by requesting through your IBM FAE.



Standard Basic WB I/O Cell Characteristics

The general information such as name description, electrical information are addressed in the standard cells data book.

All standard basic I/Os are perimeter I/Os used for wirebond. The current release supports the 7 levels of metal (7LM BEOL) stack only. Other metal stacks may be optionally made available by requesting through your IBM FAE.



Other IP – BiCMOS8HP (PLL8SFLP) PLL Kit

IBM offers a fully supported PLL kit for BiCMOS8HP with all requisite views and models including gds.

IBM Microelectronics