ECE 5205: Semiconductor Devices
Syllabus
Spring Term 2014
Tuesday and Thursday 11:00 – 12:15 DURHM 261

Lecture: ECE 5205 SEMICONDUCTOR DEVICES

Instructor: Prof. Marius Orlowski, ECE Department, 614 Whitemore Hall

Course Description:
The course covers device physics and selected semiconductor processing of pn junction diodes, MOSFET transistors, floating gate transistors, and non-volatile memory. The section on pn junction diode includes: breakdown, varactor, tunnel diode, and gated-diode structures. (Photodiodes, photodetectors, and light-emitting diodes are not included as they are covered in ECE 5206). The section on MOSFETs covers: properties of the metal-oxide-silicon system, ideal and non-ideal MOS systems, strong and weak inversion region, subthreshold conduction, mobility degradation and velocity saturation, long channel MOSFET, short channel effects (including reverse short channel effect), high field effects, impact ionization, substrate current, hot-carrier effects, gate current, lucky electron model, band-to-band tunneling, MOSFET degradation, Fowler Nordheim tunneling, direct tunneling. The section on Floating Gate Memory cell discusses: floating gate principle, programnming, reading and erasing of a FG-MOSFET, channel hot-electron injection, substrate hot-electron injection, source side injection, Fowler-Nordheim tunneling, band-to-band tunneling, oxide degradation and breakdown, basic cell structures.

Learning Objectives:
Having successfully completed the course 6984, students will be able:

- Understand **pn Junction Diodes:** electrostatics, capacitance, *I-V* characteristics, reverse breakdown, diode models, diode circuits, small-signal analysis.
- Calculate I-V characteristics of a **MOSFET** transistor
- Understand and estimate the parasitic leakage currents in n MOSFET
- Understand short channel effects of a MOSFET
- Understand scaling issues and challenges of MOSFETs
- Understand the operation of a **floating gate MOSFET** (FG-MOSFET)
- Understand programming, reading, and erasing operations of a memory cell based on FG-MOSFET

Prerequisites:
- ECE 4214: Semiconductor Device Fundamentals
- ECE 4234: Principles of Semiconductor Devices
- ECE 5200: Graduate-level semiconductor device courses

Scholar. Scholar (https://learn.vt.edu/) is the official web site and communications medium for ECE 2984. Students should check it before every class and are responsible for all information posted there.

Attendance and Participation.

- **Lecture Absences**: Students are responsible for all material covered in class, whether they were present or not. Students who are absent should make arrangements to obtain copies of the lecture notes from a classmate. Except where required for a special needs accommodation, Dr. Meehan will not provide copies of her lecture notes for students who missed class.
- **University Closings:** In case of snow or severe ice, students may call 231-6668 to find out if the University will be open. If the University is closed on a given day, homework due on that day will be collected at the next class meeting. If the University is closed on a scheduled test day, the test will be given at the next class meeting.
- **Test Absences:** Makeup tests will not be given. The test dates are specified in the course schedule. Students who will be absent on a test day must make advance arrangements to take the test. Students who miss a test for reasons other then hospitalization or other University-mandated last-minute emergency will receive a grade of zero.
- **Special Needs:** Students with special needs are encouraged to see Dr. Meehan during office hours or by appointment to arrange for accommodations.

Honor System: The tests and final examination will be conducted under a strict interpretation of the Honor Code. Any suspected violations will be dealt with promptly and without warning. **Reasonable discussion of, cooperation on, and assistance with homework problems are permitted; blatant copying or group solutions are not.** Suspected violators will be warned once.

Class Cancellation: class cancelation, if any, will be announced in due time in the class and on scholar.

Office Hours and Other Assistance.

- Dr. Orlowski's office hours are on Tuesday 4:00 pm – 6:00 pm in 614 Whittemore Hall

GTA: there is no GTA assigned to this class

Homework

There will be 10-11 homework assignments where the lowest grade on the assignments will be dropped when calculating the final grade. Homework must be submitted by the beginning of class on Wednesday per class schedule posted on Scholar. Late submission and e-mailed assignments will NOT be accepted and will receive a grade of 0. First homework assignment will be assigned on February 3, 2014 which is due to be turned in on February 12, 2014.

Final Grade Determination

The final grade is based on an overall score, computed as follows:

Midterm Exam	25% (March 18, 2014 11:00 am – 12:15 pm)
Final Exam	40% (May 9, 2014 10:05 am -12:05 pm)

Homework 35%

The mapping of an individual score into a final letter grade depends on what the score distribution actually is. In general, a score between 90 and 94 corresponds to an A-, and a score between 70 and 72 corresponds to a C-.

TEXTBOOKS AND LITERATURE

There is no required textbook for this course. Lecture notes will be provided.

Recommended Textbooks and Literature relevant to the course:

- S.M. Sze, Physics of Semiconductor Devices, 3rd ed. New York, Wiley, 2007
- Umesh Mishra and Jasprit Singh, Semiconductor Device Physics and Design, Springer 2008 (e-book available through www.lib.vt.edu)
- S. Wolf, Silicon Processing for the VLSI Era Volume 3 – The Submicron MOSFET, Lattice Press, 1995
- J.E. Brewer and M. Gill, Nonvolatile Memory Technologies with Emphasis on Flash, IEEE Press 2008
- R. Pierret, "Semiconductor Device Fundamentals, McGraw-Hill 2002
- Chung-You Hu, Bias Scheme of Program Inhibit For Random Programming in a NAND FLASH Memory" US Patent 5,715,194, 1998
- K-D Suh et al, " A 3.3 V 32 Mb NAND Flash Memory with Incremental Step Pulse Programming Scheme", IEEE Solid State Circuits, vol. 30, no. 11, p. 1149 (1005)
- T-S. Jung et al, "A 3.3V 128Mb Muli-Level NAND Flash Memory for Mass Storage Applications", ISSCC96 Conference, p.32 (1996)
- R. Bez et al, "Introduction to Flash Memory", Proceedings of the IEEE, vol. 91, no. 4, 2003
- P. Pavan et al, "Flash Memory Cells – An Overview", of the IEEE, vol. 85, no. 8, 1997

EDUCATIONAL OBJECTIVES

The lecture sessions provide learning opportunities that should enable students to do the following upon completion of this course:

- Develop understanding of MOSFET and Floating Gate cell operations.
- Understand the limitations of these devices
- Understand the architecture of NAND and NOR FLASH memories
- Understand the programing and erasure constraints of a FLASH memory cell
- The lecture serves as a basis for 6000 level courses on EEPROM, NAND and NOR technology challenges and issues.