ECE 5205
Basic Semiconductor Devices
Course Syllabus CRN 12462 and12463

Spring 2014 Semester
T R 11:00 am – 12:15 pm (Durham 261)

Marius Orlowski
Virginia Polytechnic Institute and State University

URL for recorded class: http://media1.vbs.vt.edu/content/classes/z3851 ???

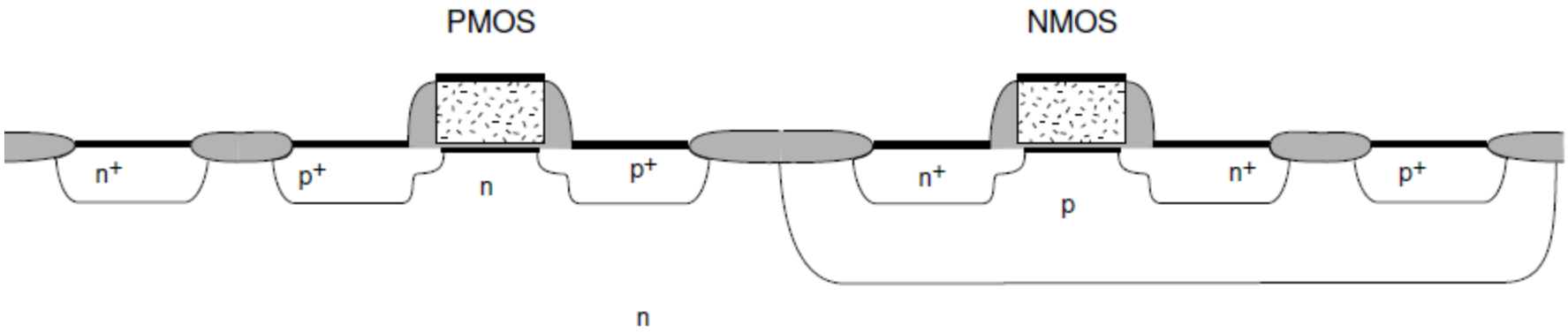
Overview of the Course

- p-n junction, diode - revisited
- metal-semiconductor junction - revisited
- MOS Structure and MOSFET
- Advanced MOSFET topics
- Floating Gate Transistor
- Non-volatile Memory (Flash Memory)

p-n Junctions

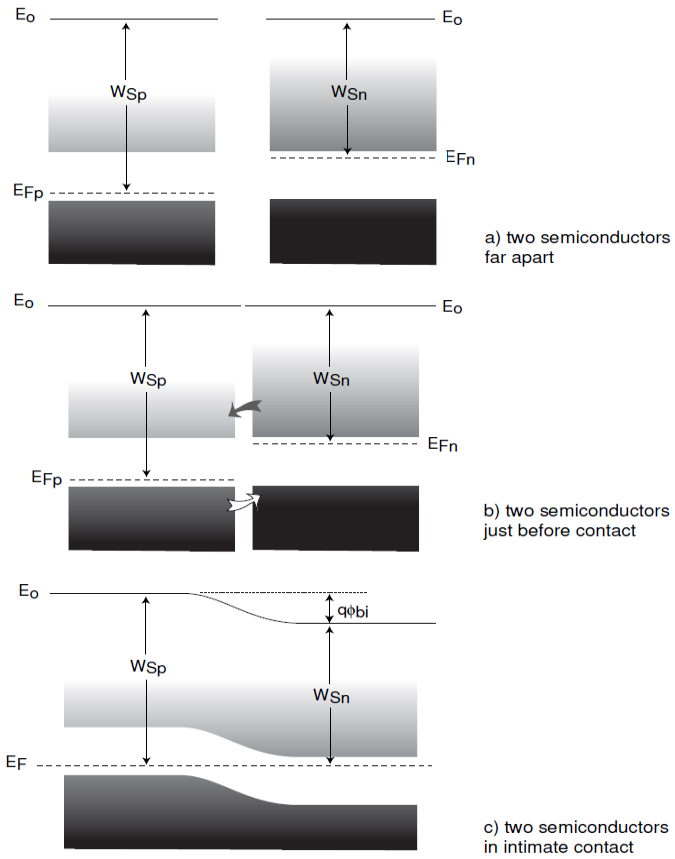
Motivation: pn junctions everywhere!

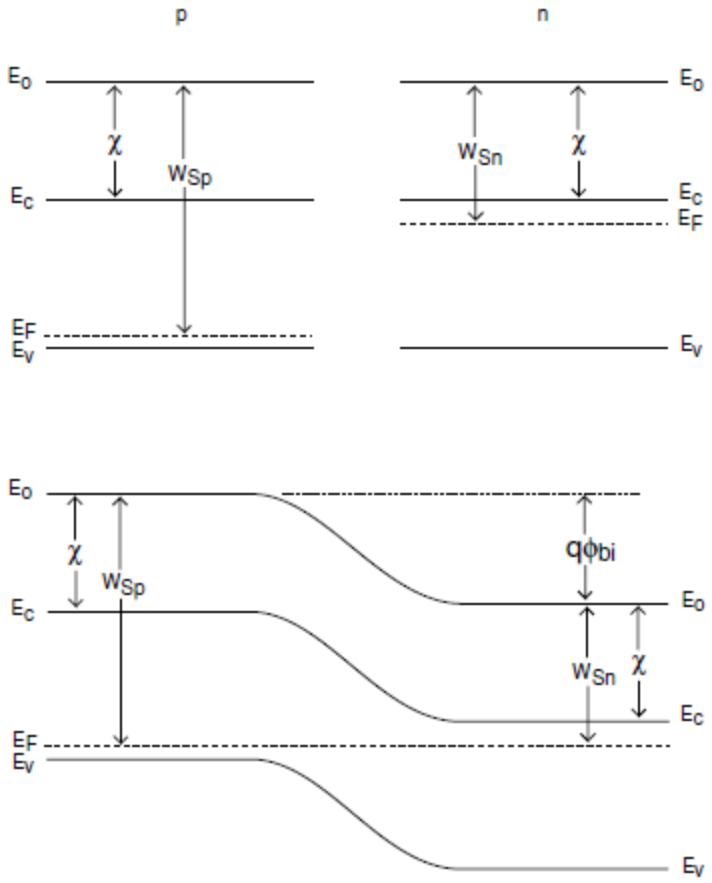
Example: CMOS



p-n Junctions

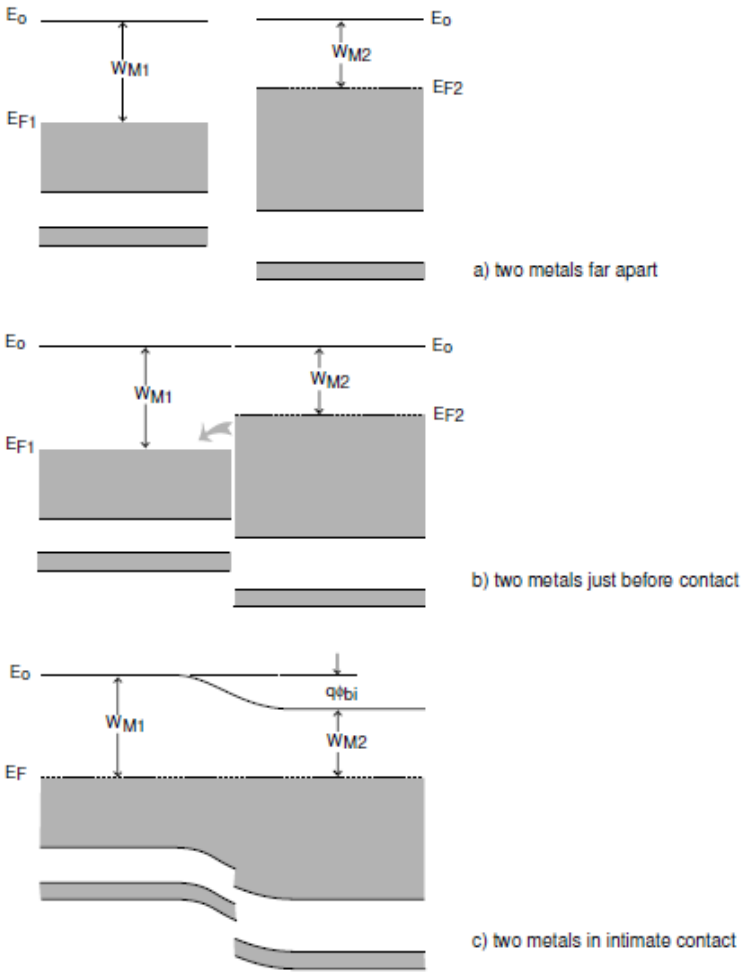
1. Ideal p-n junction in equilibrium



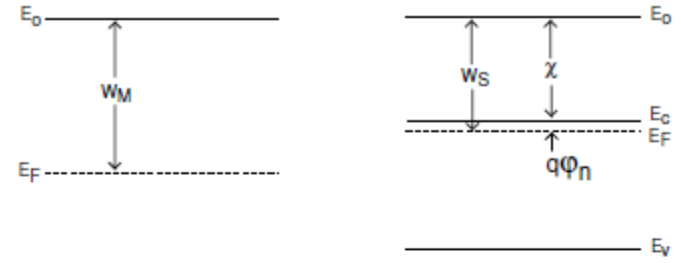


Metal-Semiconductor Junctions

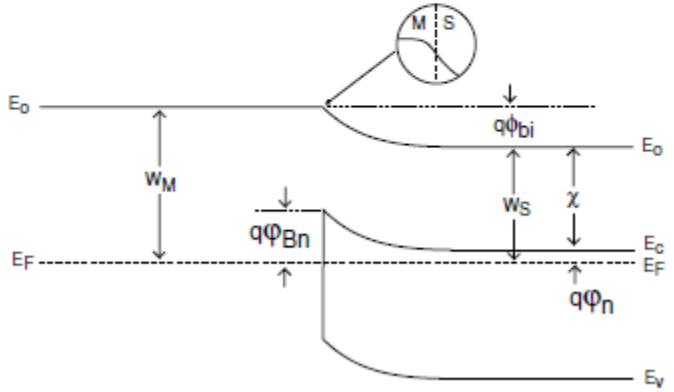
Metal-Metal Contact



Metal-Semiconductor Contact

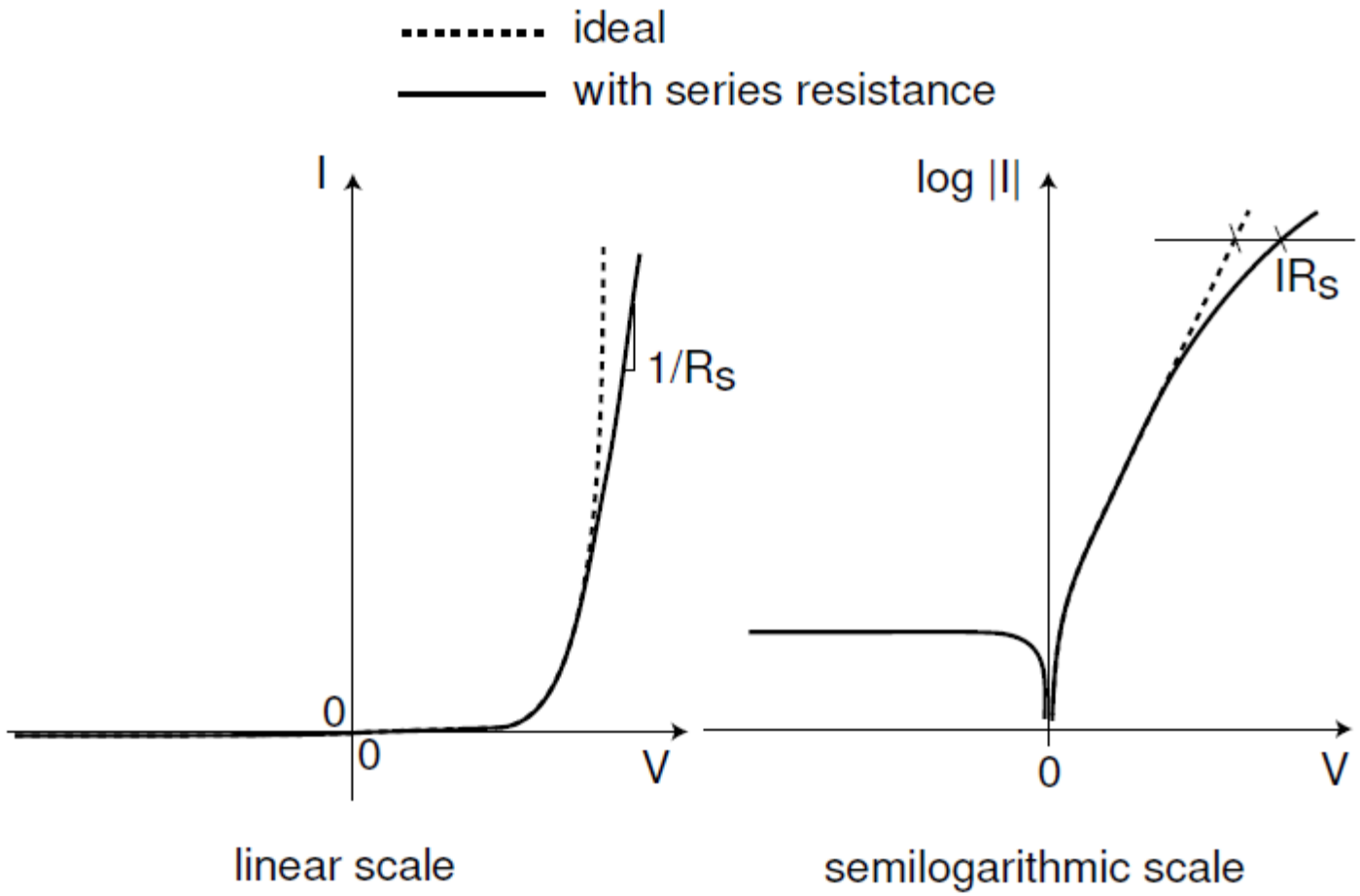


a) metal and semiconductor far apart



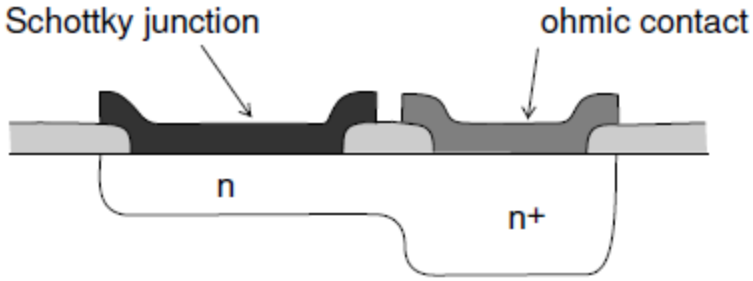
b) metal and semiconductor in intimate contact

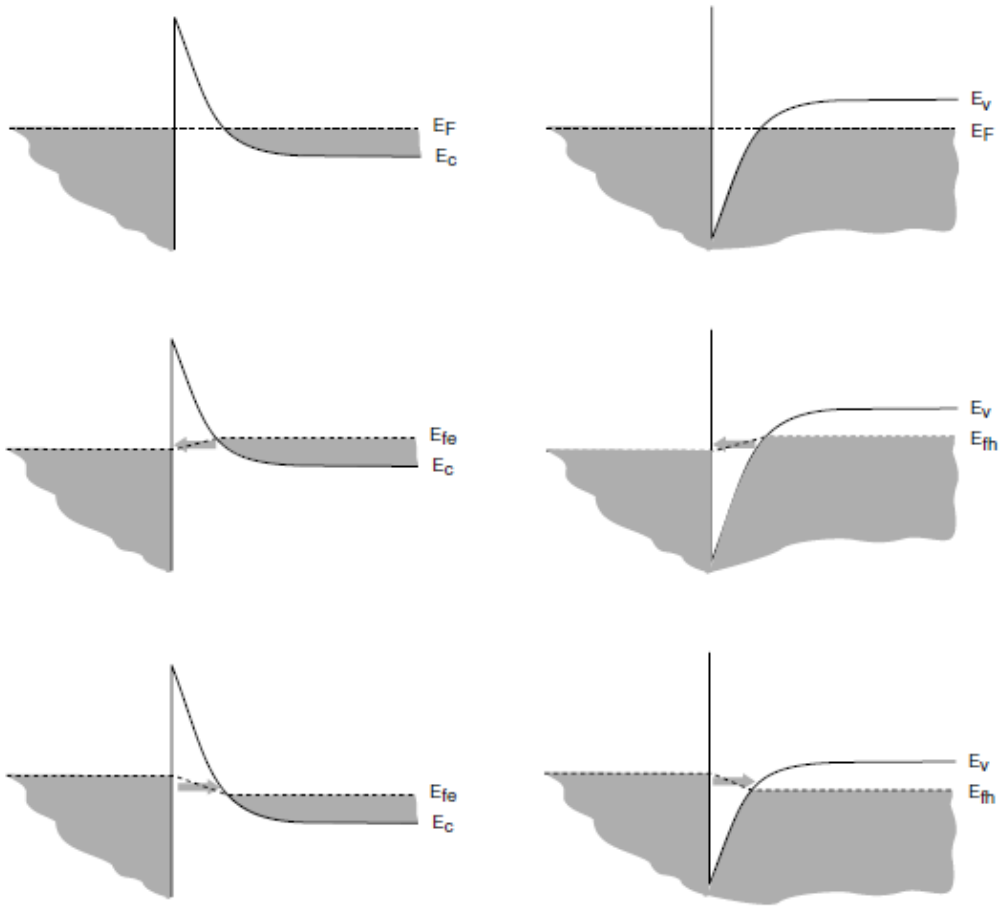
Schottky Diode



$$I = I_S[\exp \frac{q(V - IR_s)}{kT} - 1]$$

Schottky junction versus metal contact





ohmic contact to n-type semiconductor

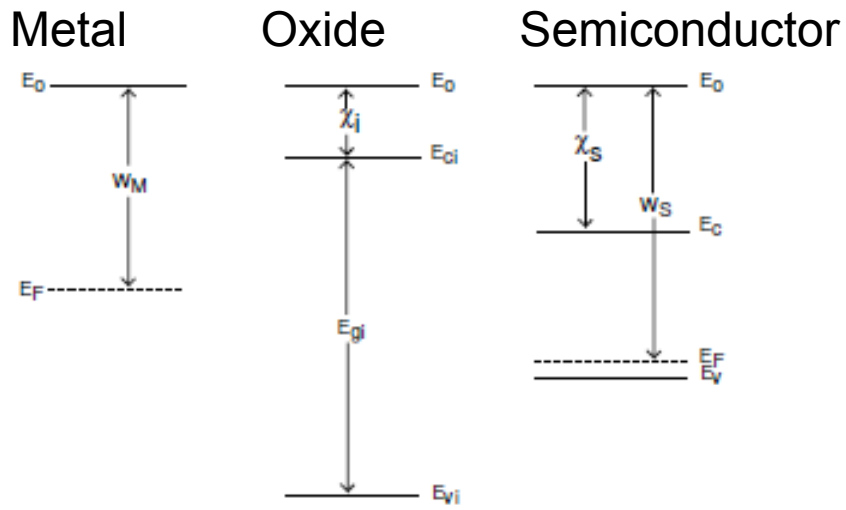
ohmic contact to p-type semiconductor

MOS Structure

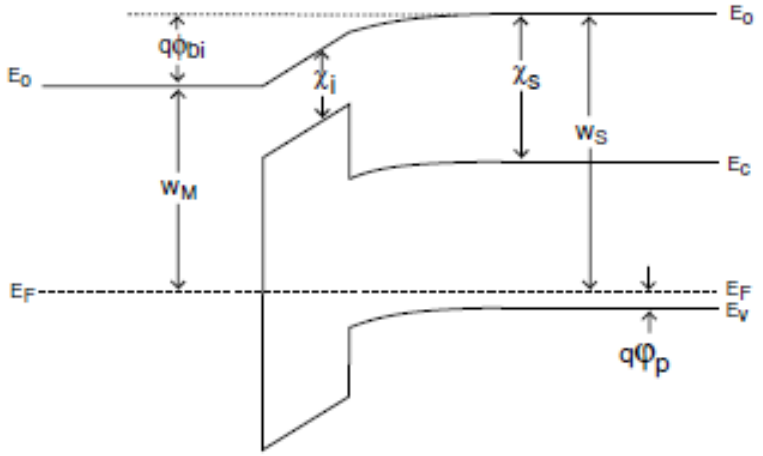
M – Metal

O – Oxide (Insulator)

S - Semiconductor



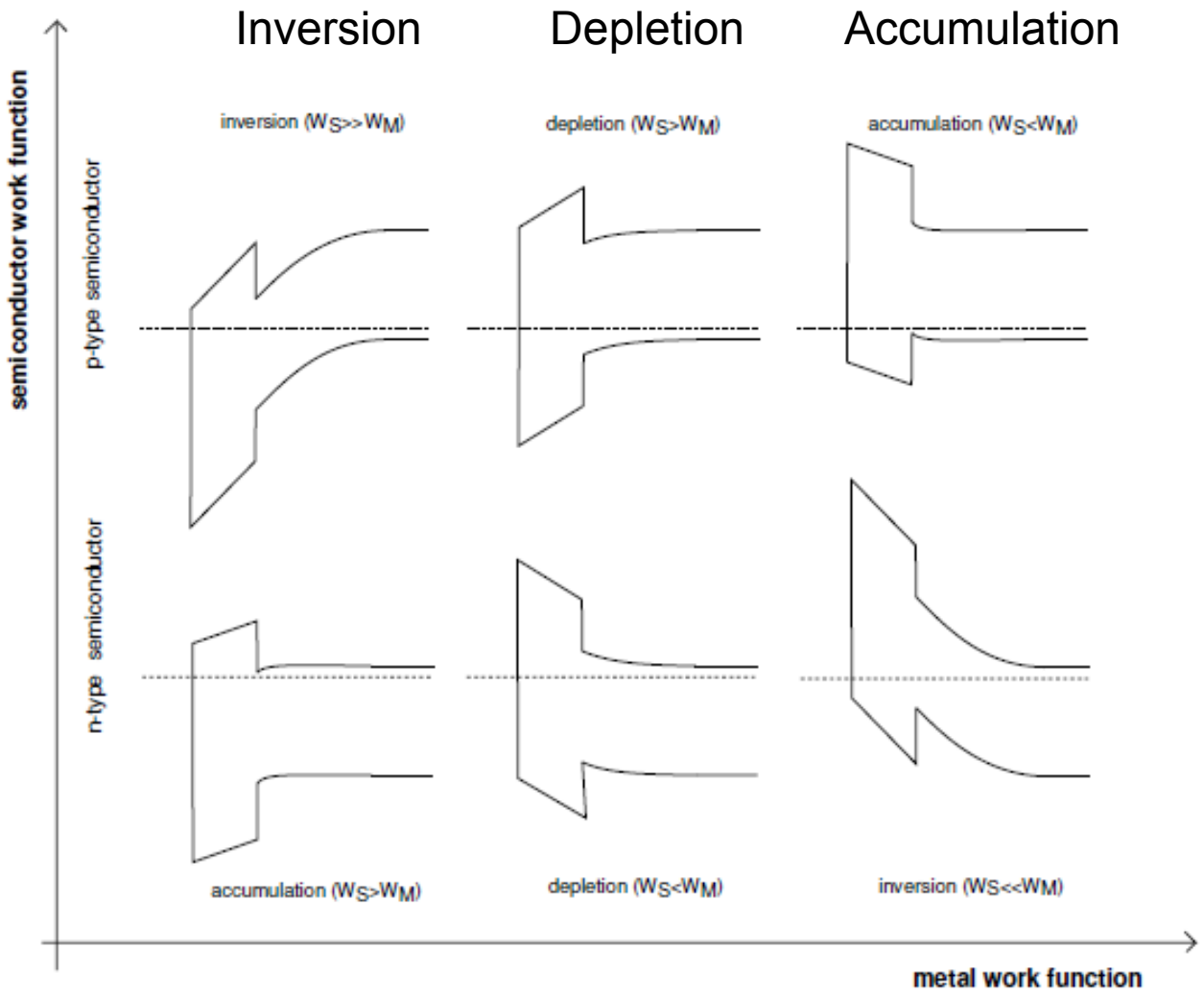
a) metal, insulator and semiconductor far apart



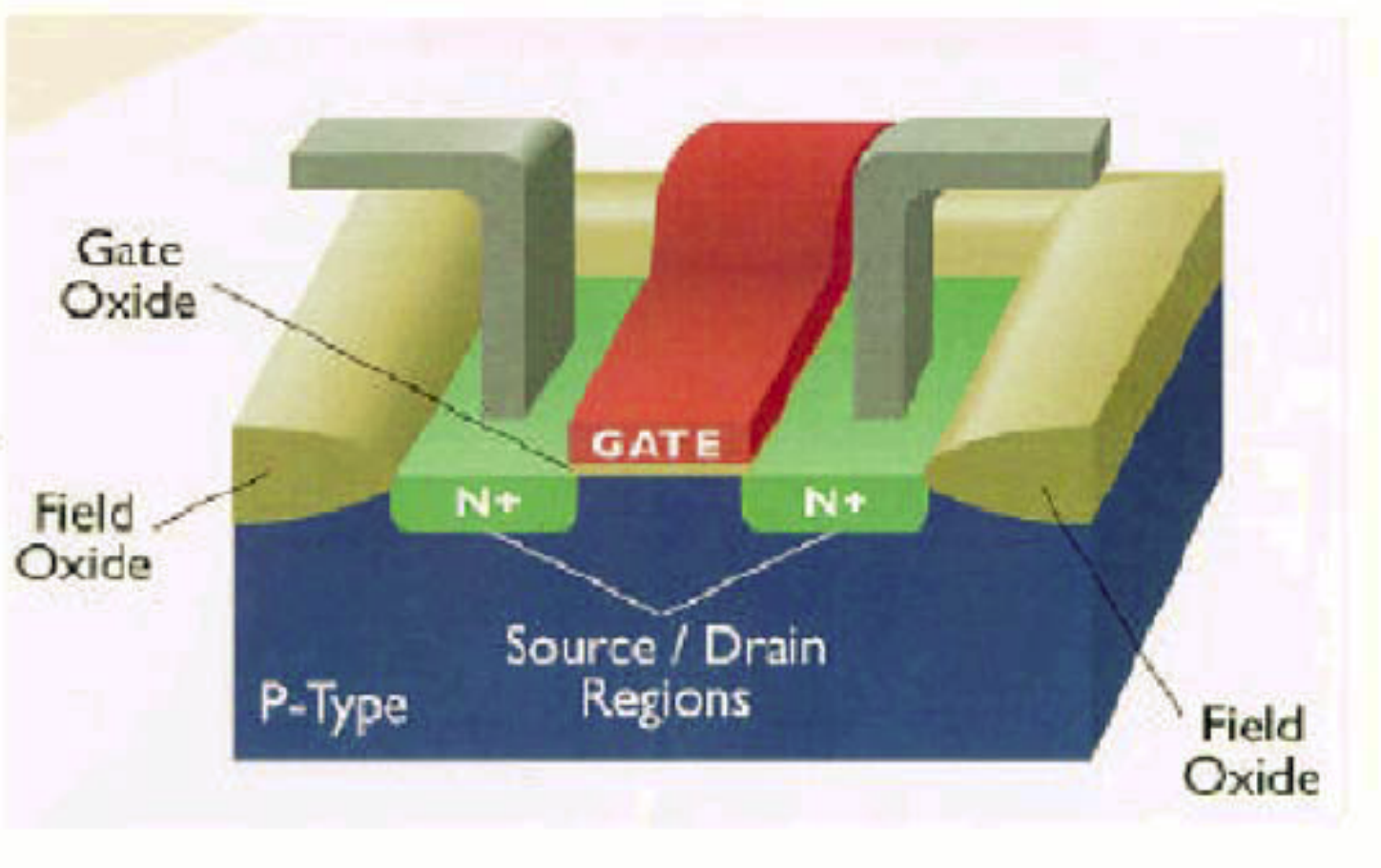
b) metal, insulator and semiconductor in intimate contact

MOS Structure

M – Metal
O – Oxide (Insulator)
S - Semiconductor



MOS Transistor 3D Structure



A specific architecture of
p-n junctions, MOS structure, and metal-semiconductor contacts

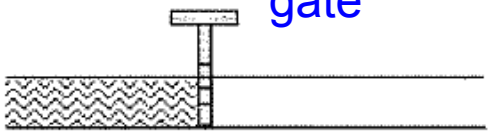
MOSFET ANALOGY

source

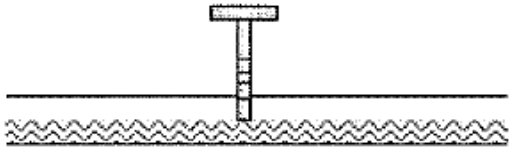
drain

Water flowing in a pipe

gate



A faucet to shut off
the channel flow



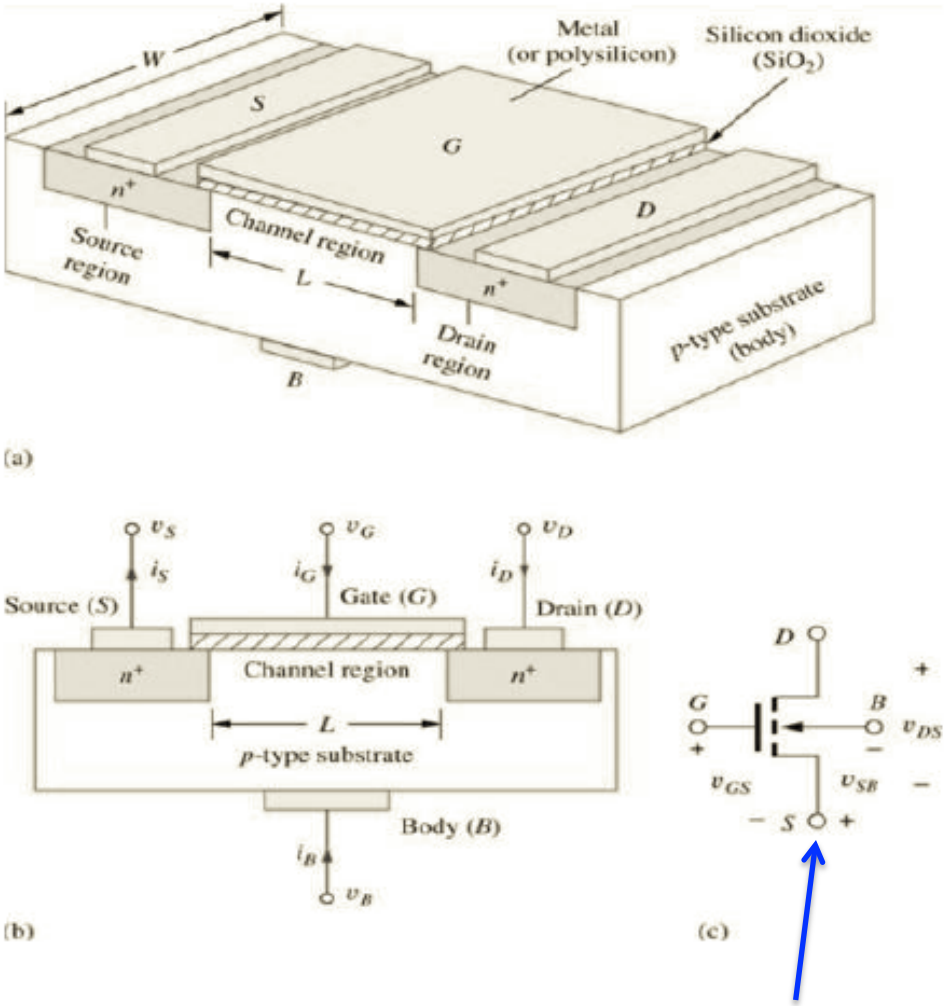
substrate

Water flows when the
constriction is reduced

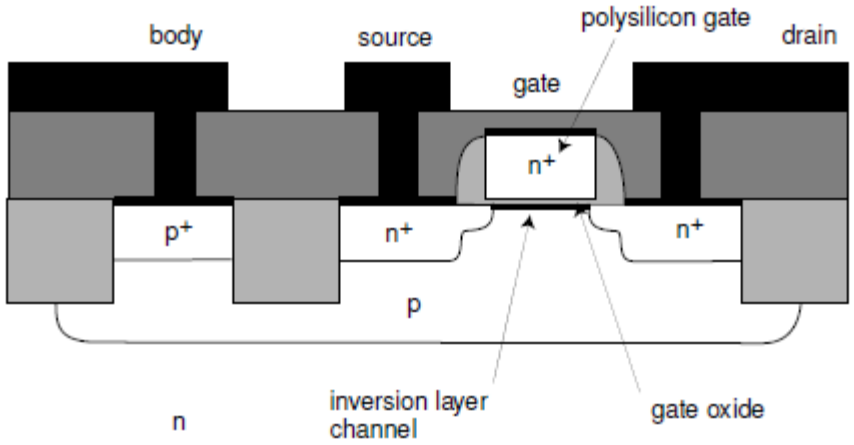
Field-effect transistors ⇒
channel constriction is
controlled by gate bias.

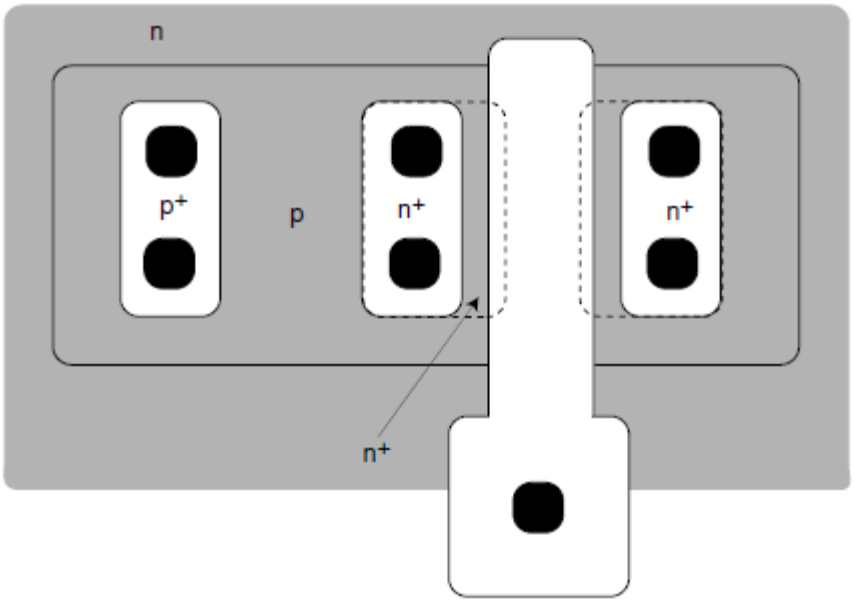
MOSFET – A Four Terminal Device

- 4 terminal device –Gate, Bulk, Source and Drain
- Biasing– V_{DS},V_{GS}, V_{BS}
- L, W, N_A,t_{OX}
- Source and drain regions form *pn* junctions with substrate



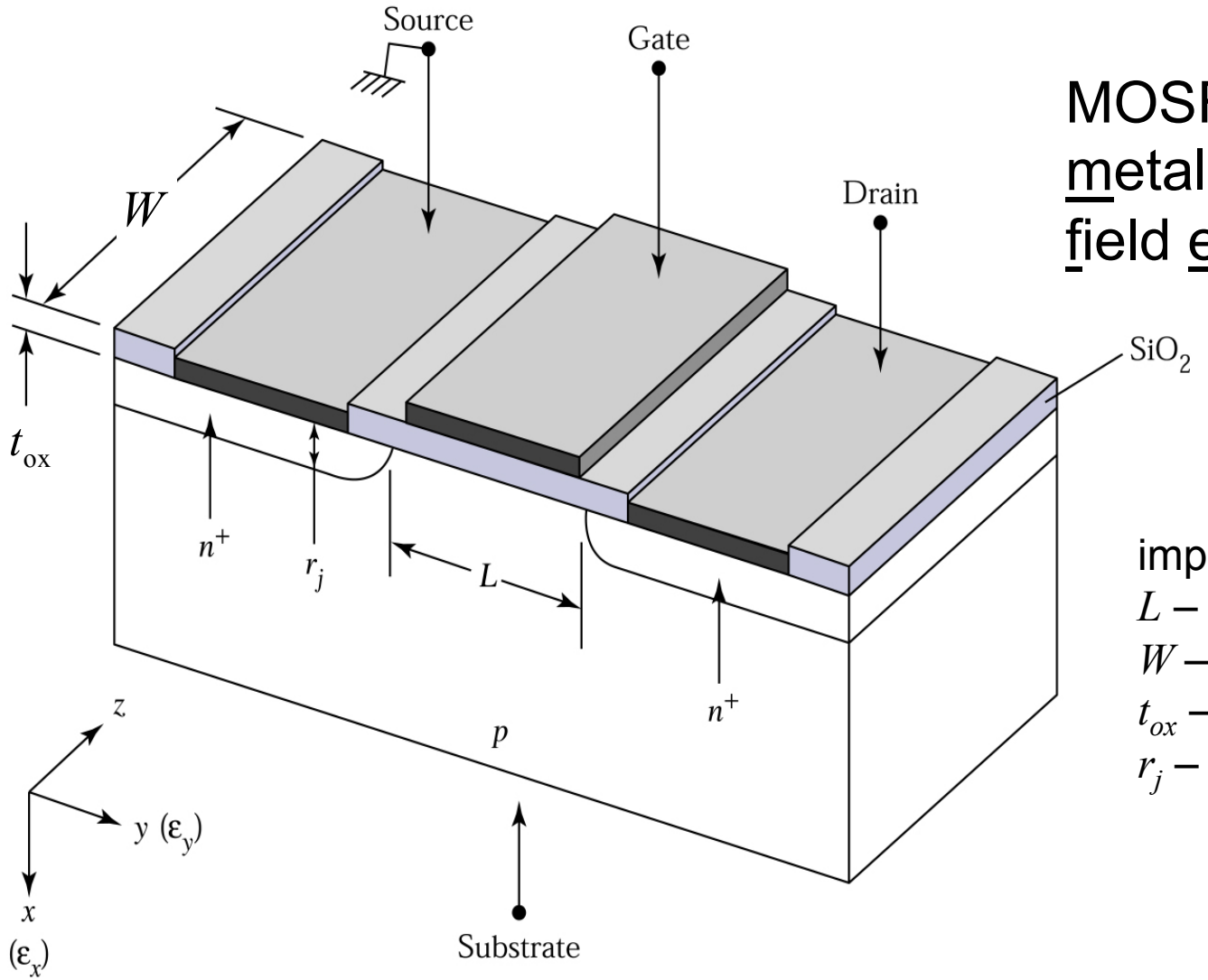
A MOS transistor layout





CMOS:
“planar” technology

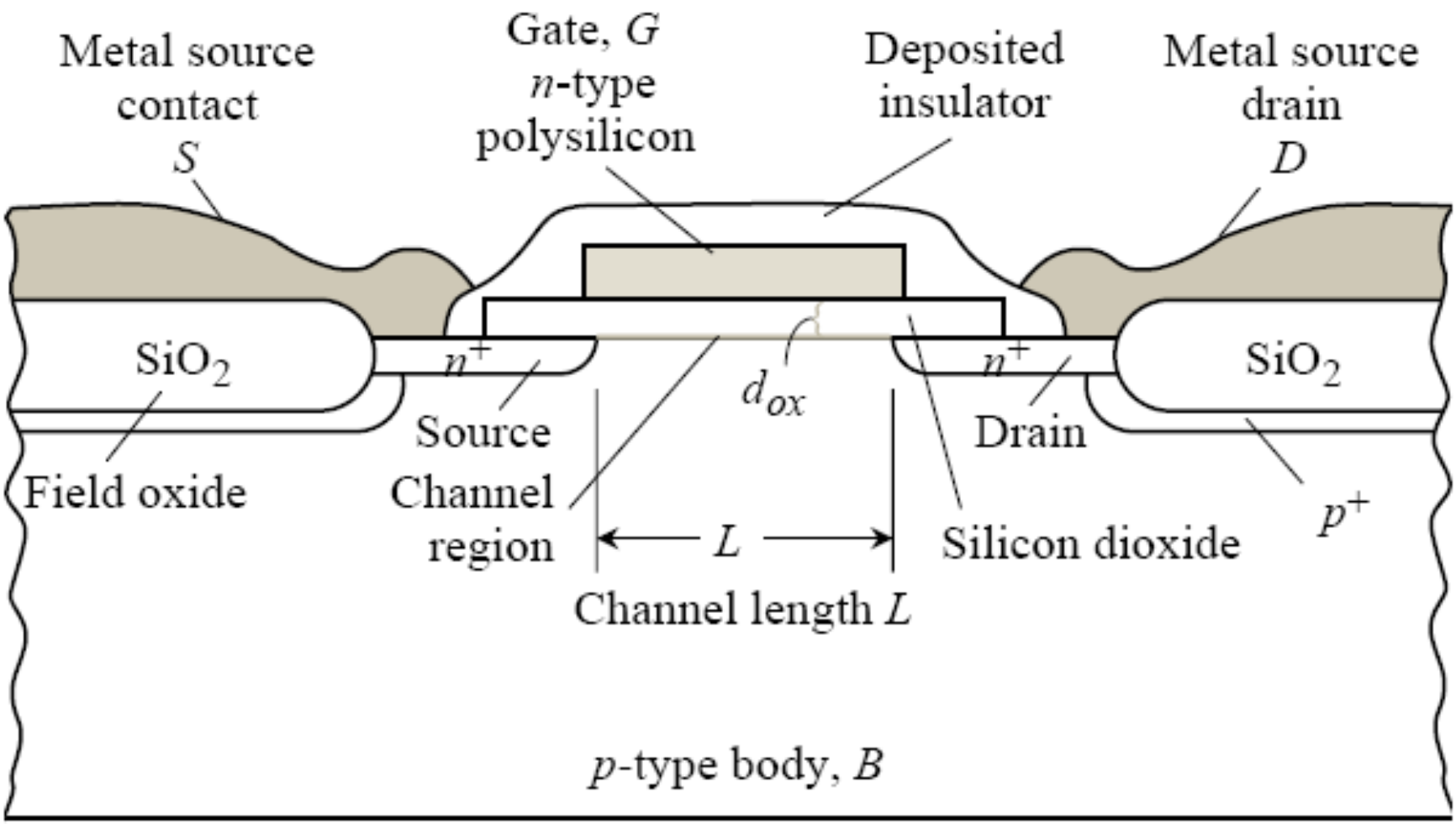
Perspective View of MOSFET



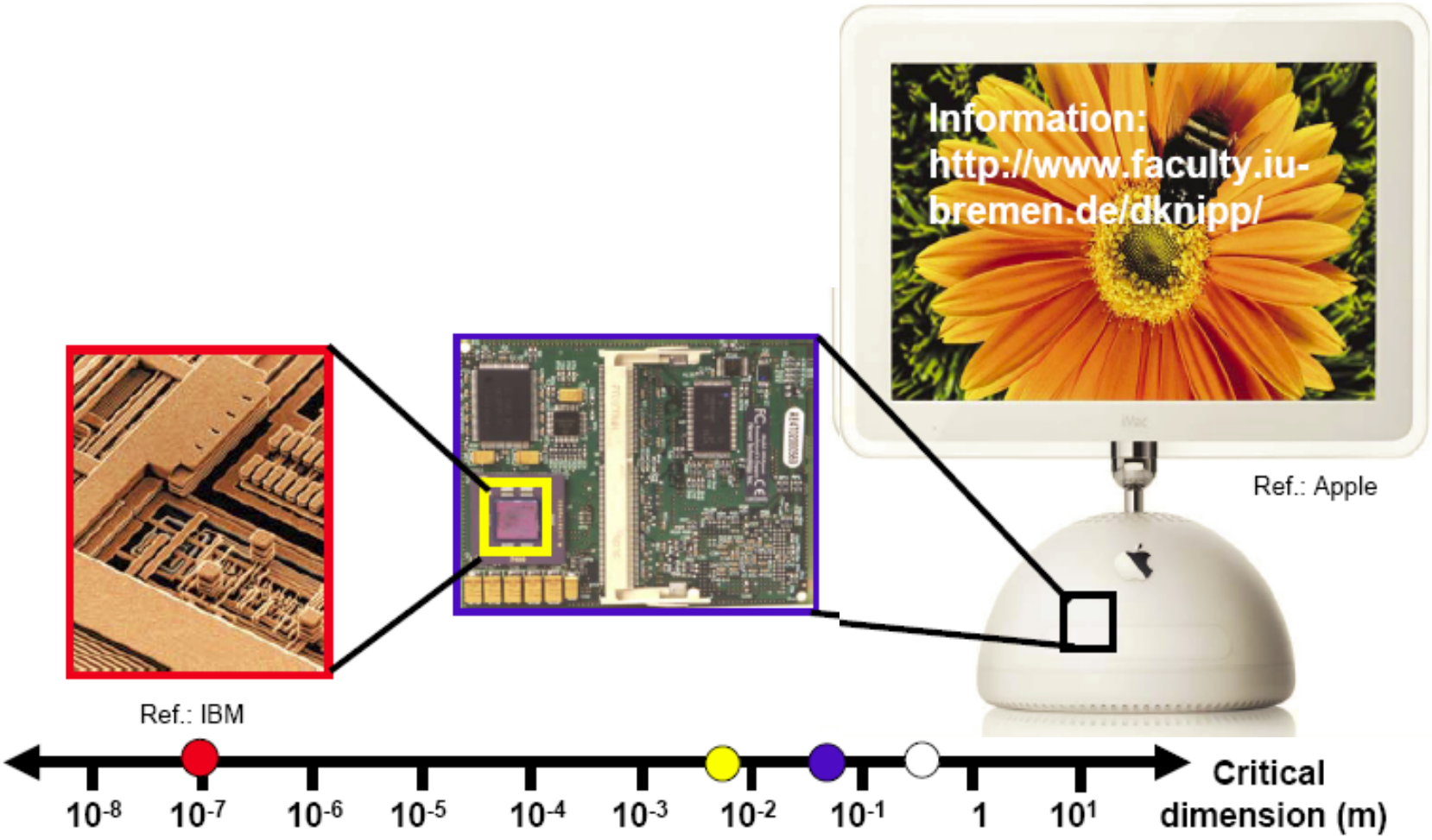
MOSFET
metal oxide silicon
field effect transistor

important dimensions:
L – the channel length
W – the channel width
t_{ox} – oxide thickness
r_j – junction depth

MOSFET and Conventional LOCOS Isolation



Dimensions and Scales



State-of-the-art MOSFET

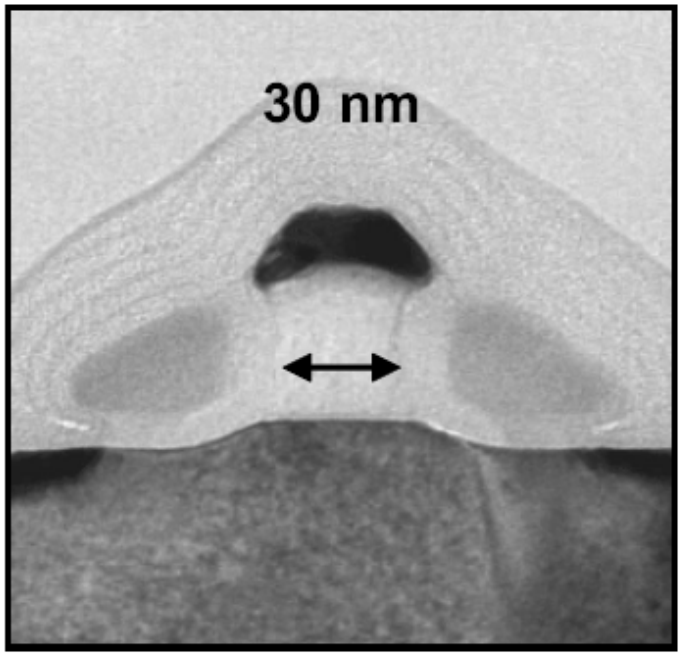
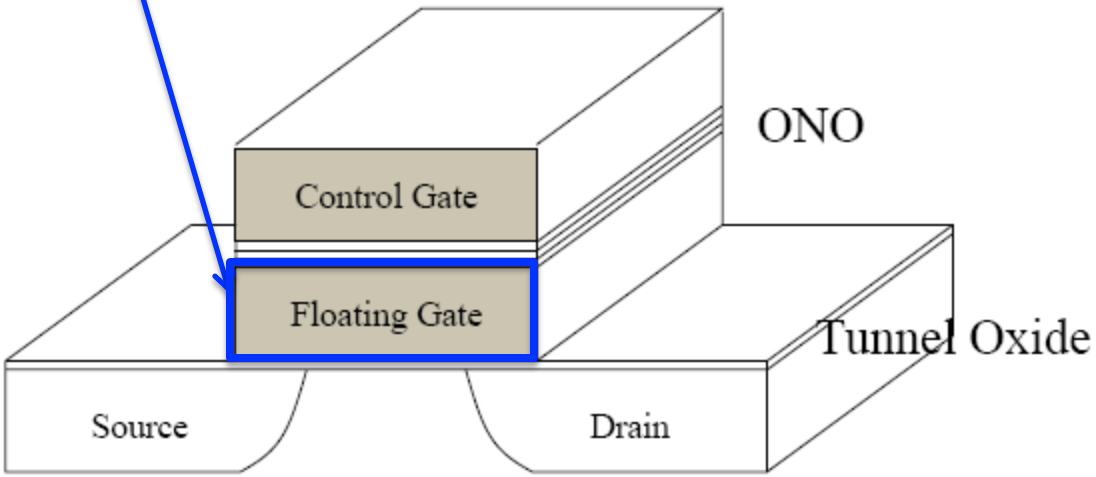


Figure 9.1: SEM cross-sectional image of a state-of-the-art MOSFET with a physical gate length of 30nm. Figure courtesy of R. Chau, Intel.

Lattice constant of Si is equal to 5.4307 (Å) Anstrom or 0.543 nm

Floating Gate Transistor and Non-volatile Memory



Threshold voltage of CMOS Device:

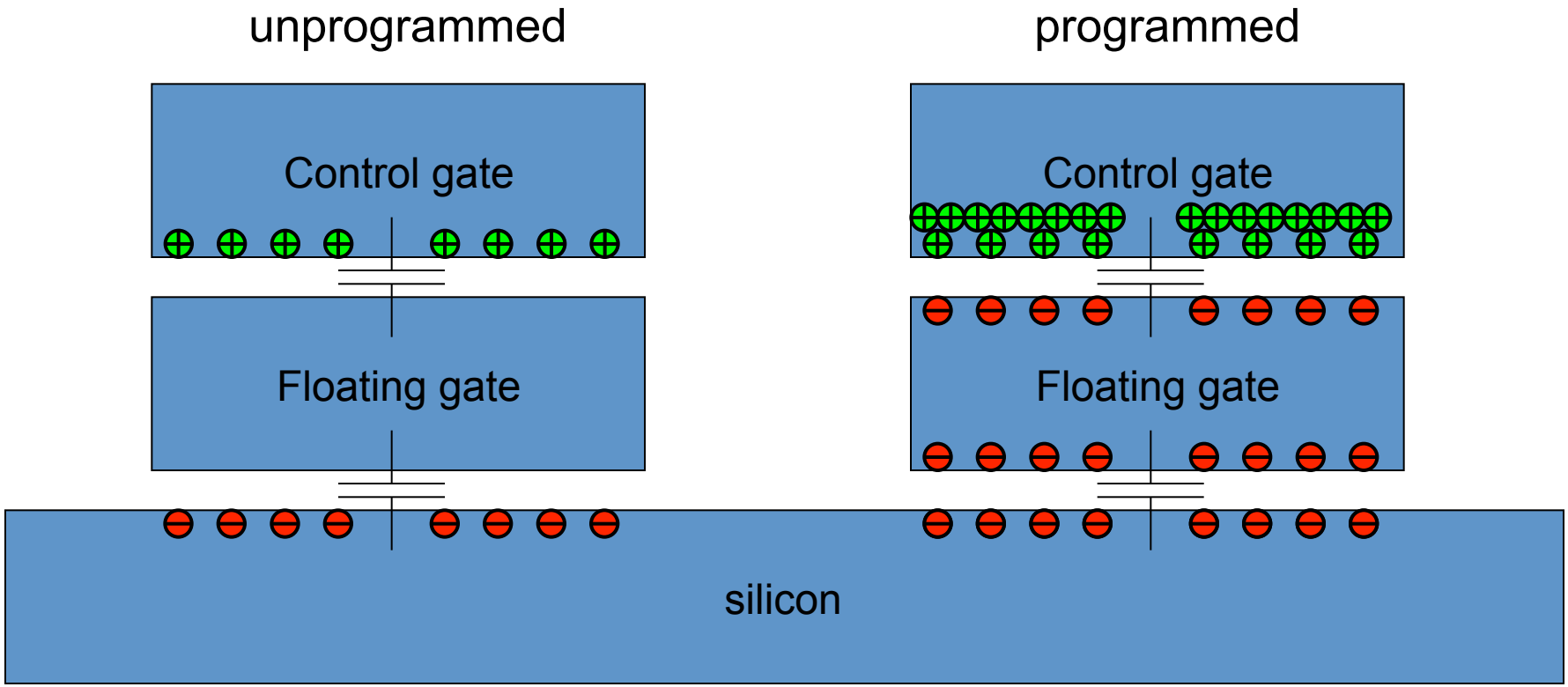
$$V_T = K - Q/C_{OX}$$

Non-Volatile Memories

- A non-volatile memory is a memory that can hold its information without the need for an external voltage supply. The data can be electrically cleared and rewritten

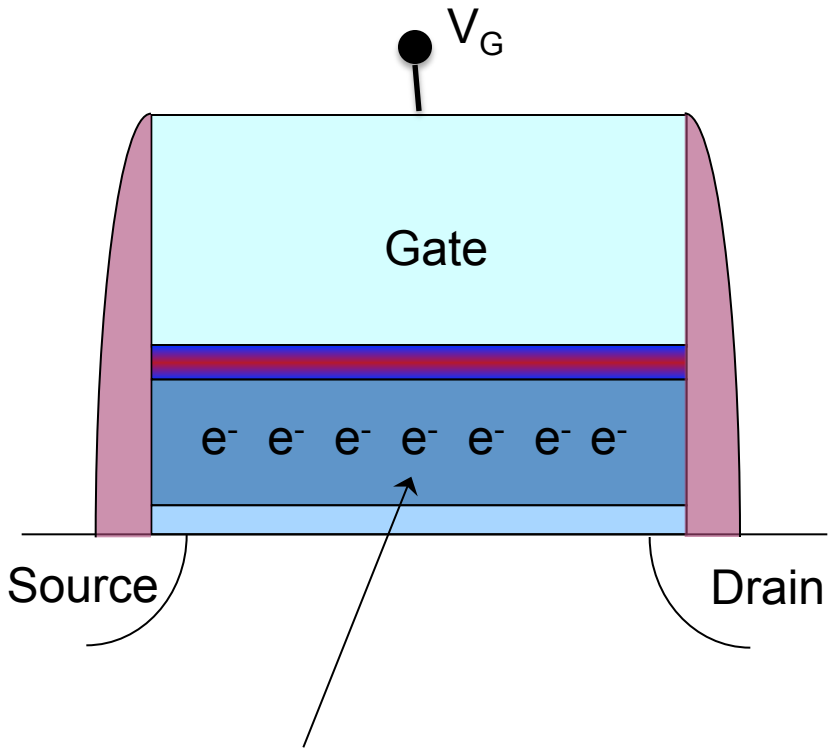
- Examples:
- Magnetic Core
- Hard-disk
- OTP: one-time programmable (diodes/fuses)
- EPROM: electrically programmable ROM
- EEPROM: electrically erasable and programmable ROM
- Flash

Channel charge in **floating** gate transistors

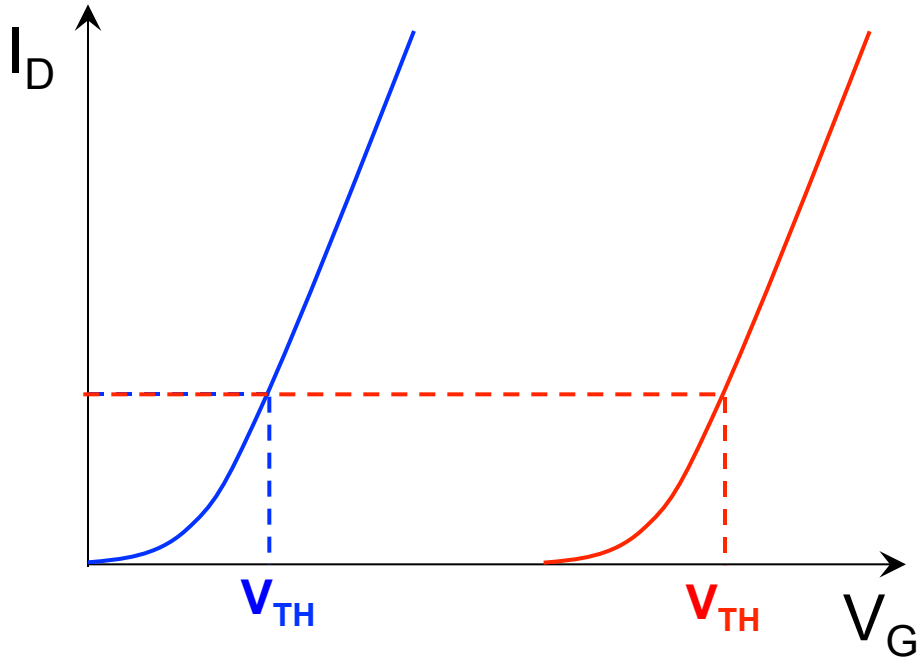


To obtain the same channel charge, the programmed gate needs a higher control-gate voltage than the unprogrammed gate

Program and Erased States



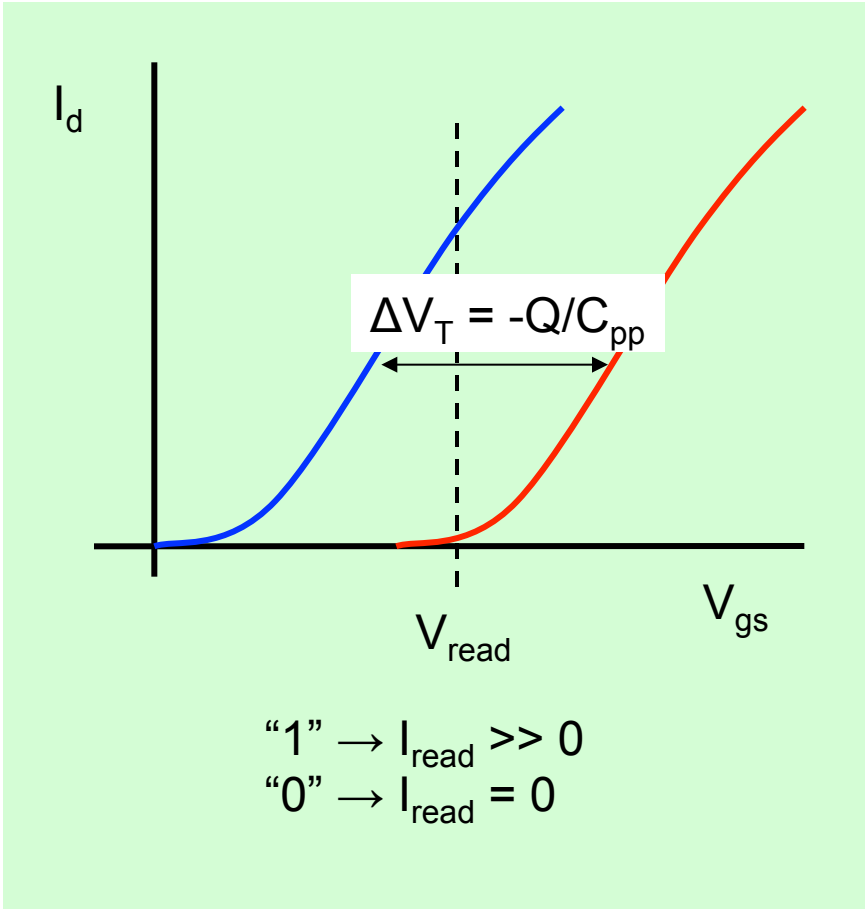
Isolated charge storage layer
- polysilicon, nitride, nanocrystals, etc.



Erase state
= “1”

Program state
= “0”

Logic “0” and “1”

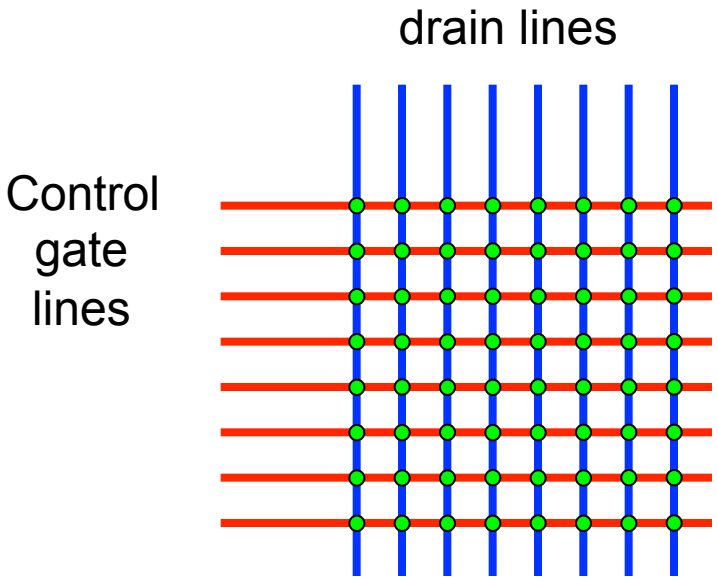


Reading a bit means:

1. Apply V_{read} on the control gate

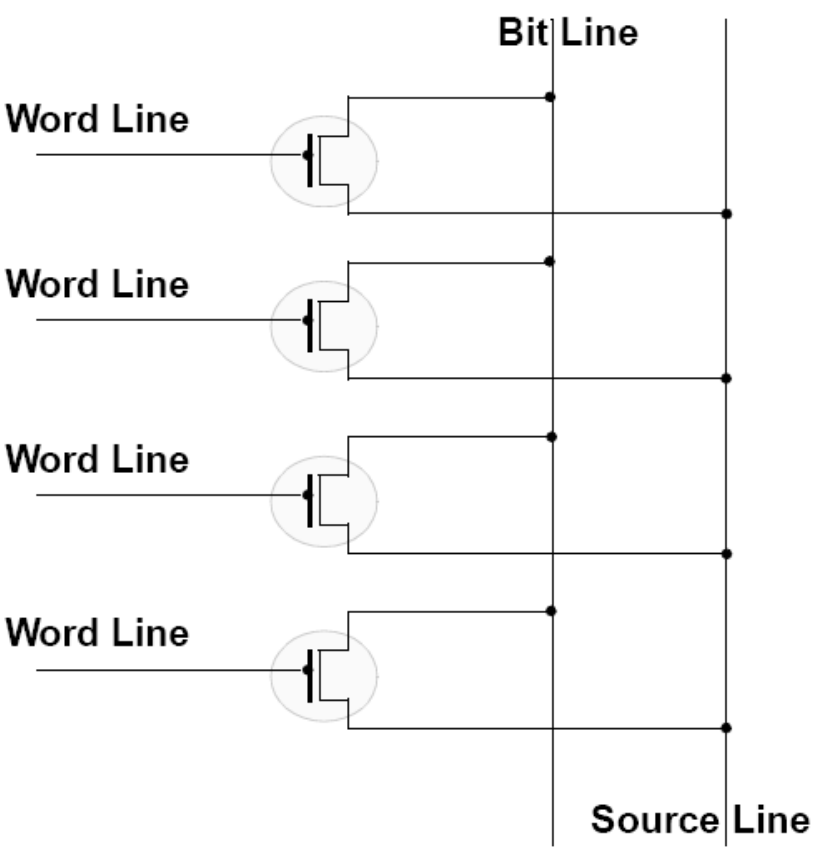
2. Measure drain current I_d of the floating-gate transistor

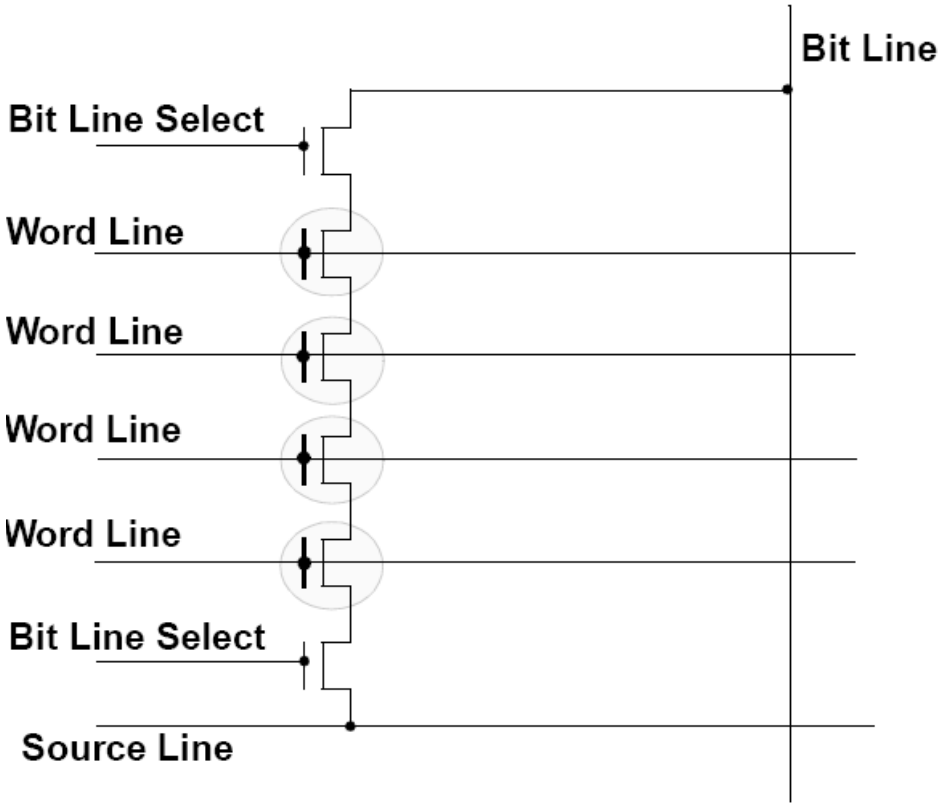
When cells are placed in a matrix:



Two flavors: NOR or NAND Organization

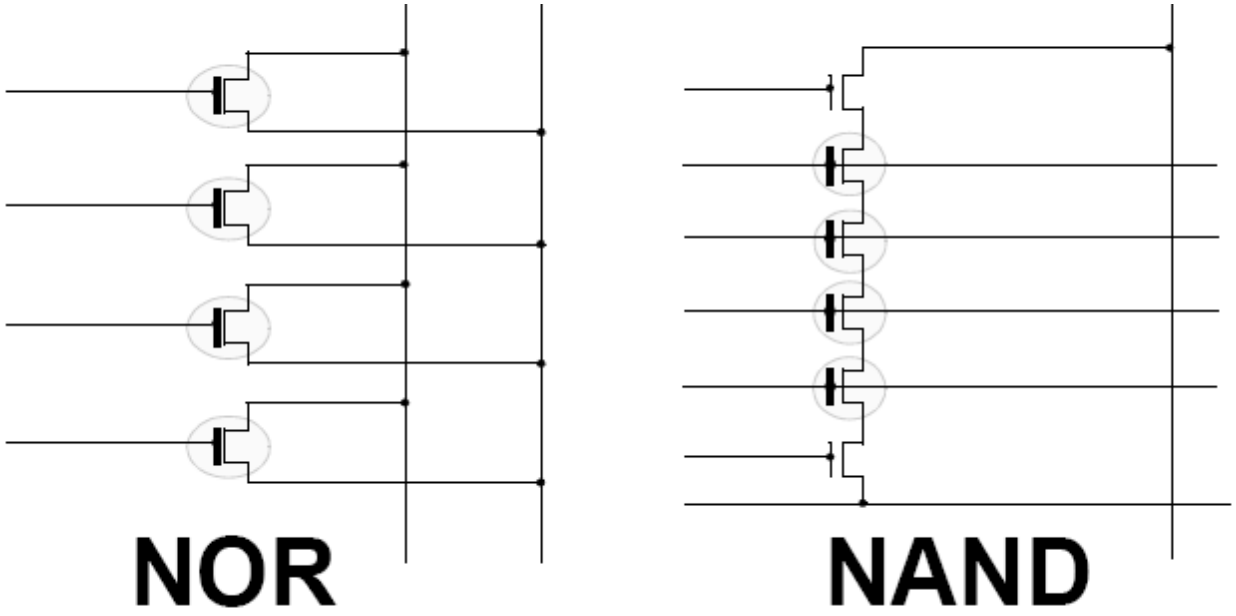
'Word' = control gate; 'bit' = drain





NOR **NAND**

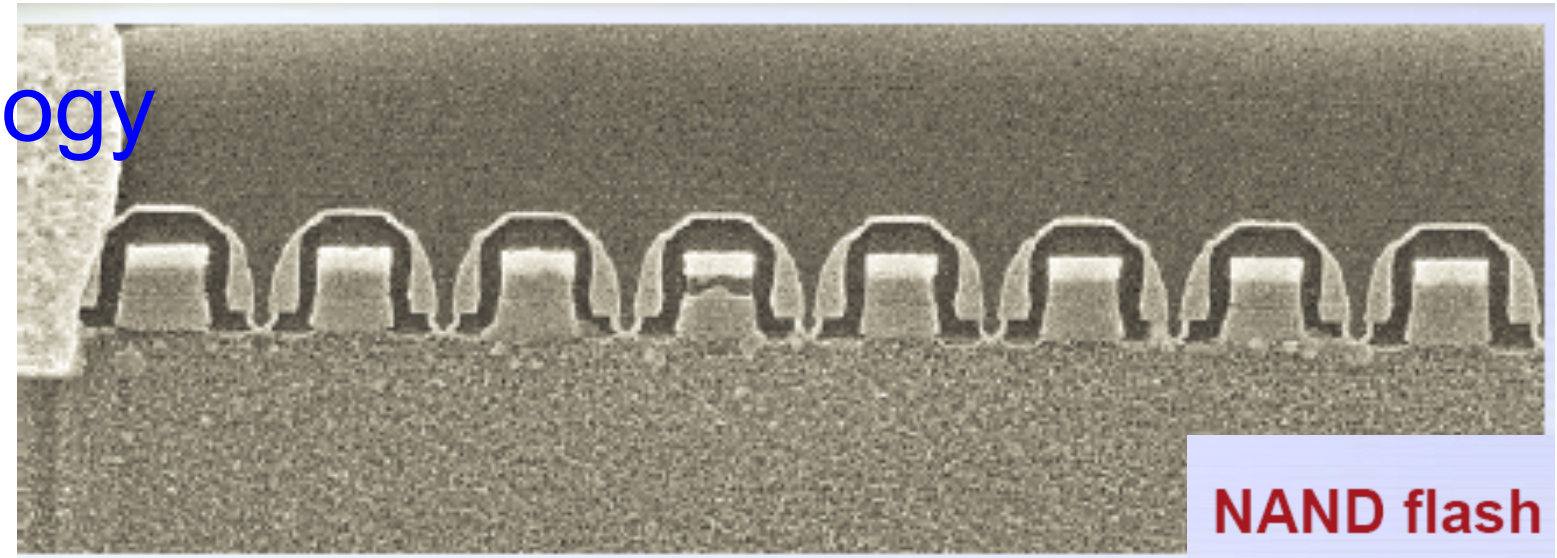
NAND versus NOR



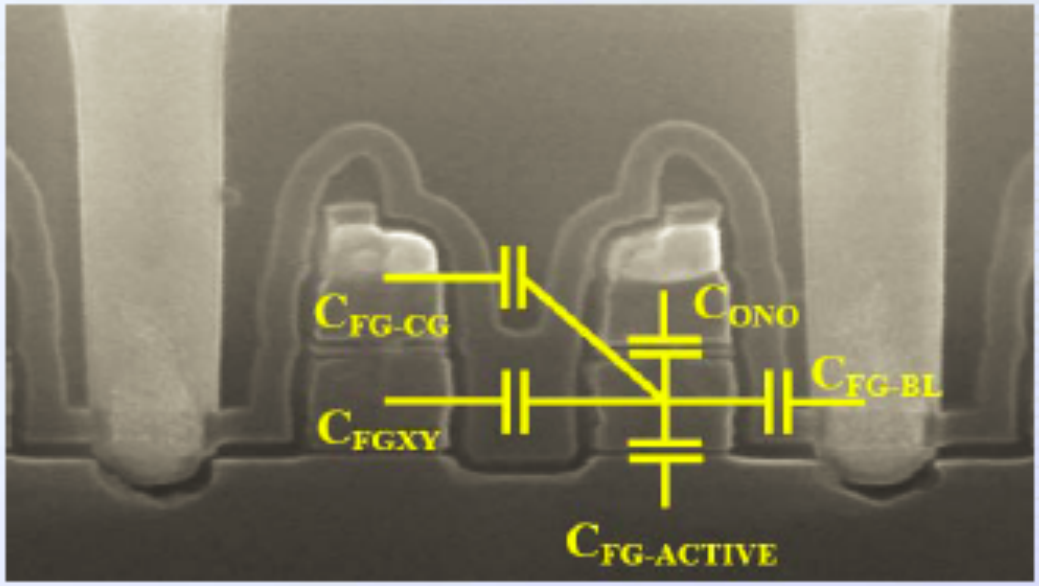
10x better endurance
Fast read (~100 ns)
Slow write (~10 µs)
Used for Code

Smaller cell size
Slow read (~1 µs)
Faster write (~1 µs)
Used for Data

Technology Issues



NOR flash



Electrical reliability issues

Capacitive coupling and cross-talk issues

Patent at Litigation between AMD/SPANSION vs SAMSUNG for ~ $500M in 2010

United States Patent [19]

Hu

[11] **Patent Number: 5,715,194**

[45] **Date of Patent: Feb. 3, 1998**

[54] **BIAS SCHEME OF PROGRAM INHIBIT FOR RANDOM PROGRAMMING IN A NAND FLASH MEMORY**

[75] Inventor: **Chung-You Hu**, Sunnyvale, Calif.

[73] Assignee: **Advanced Micro Devices, Inc.**, Sunnyvale, Calif.

[21] Appl. No.: **686,641**

[22] Filed: **Jul. 24, 1996**

[51] **Int. Cl.**[6] **G11C 11/34**

[52] **U.S. Cl.** **365/185.17**; 365/185.18

[58] **Field of Search** 365/185.17, 104, 365/185.33, 185.18

[56] **References Cited**

U.S. PATENT DOCUMENTS

5,572,464 11/1996 Iwasa 365/185.17

Primary Examiner—Joseph A. Popek

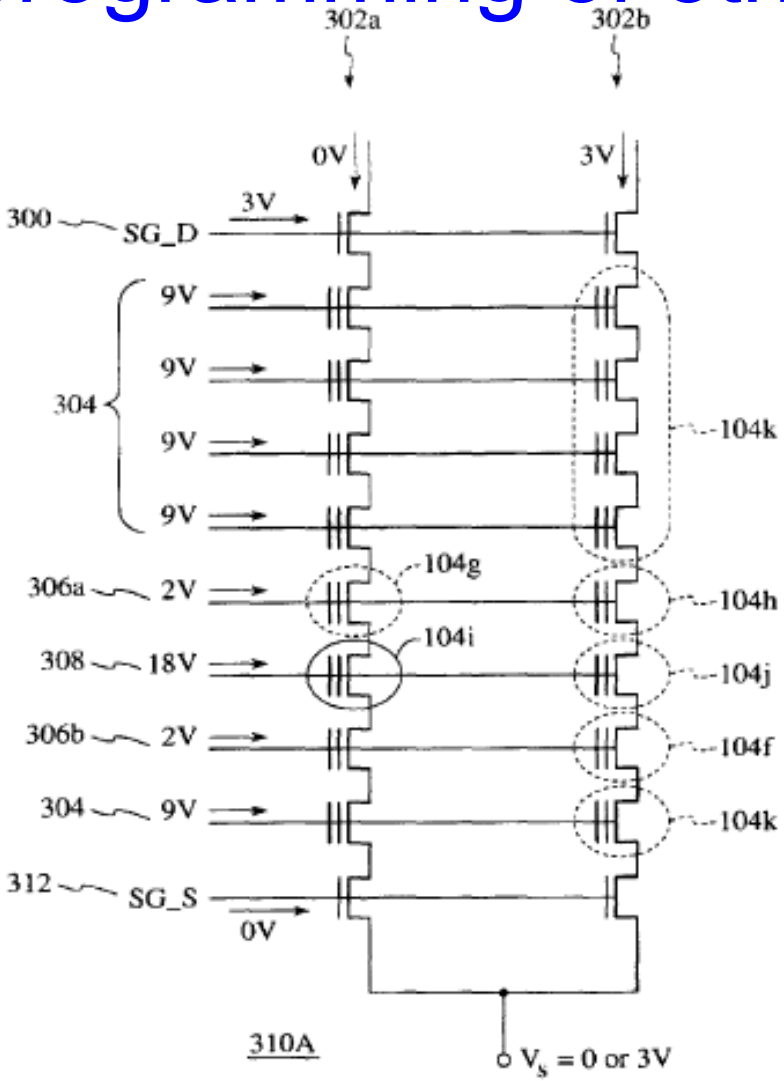
Attorney, Agent, or Firm—Sawyer & Associates

[57] **ABSTRACT**

The present invention is a system and method which allows random programming and avoids the problem with band-to-band tunneling current discussed above. In particular, the present invention applies a predetermined voltage along the wordlines adjacent to the programming wordline. A method of programming in a Flash memory system includes providing a first wordline coupled with a first device desired to be programmed, the first wordline also coupled with a second device desired to be program inhibited; electrically isolating the second device; programming the first device; and programming a third device coupled with a second wordline, the second wordline not being adjacent to the first wordline.

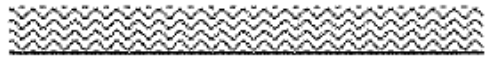
22 Claims, 8 Drawing Sheets

Random Programming of Memory Cells
How to program targeted cells without Accidental programming of other cells



Optional: Bipolar Transistor

Bipolar Flow Analogy



Water flowing over ground

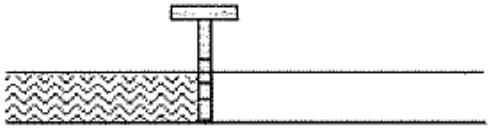
A "bump" in the ground
to shut off the flow

Water flows when the
"bump" is reduced

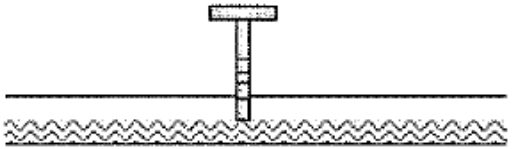
Bipolar devices ⇒ potential "bump" is controlled by base-emitter voltage.

MOSFET Flow Analogy

Water flowing in a pipe



A faucet to shut off
the channel flow



Water flows when the
constriction is reduced

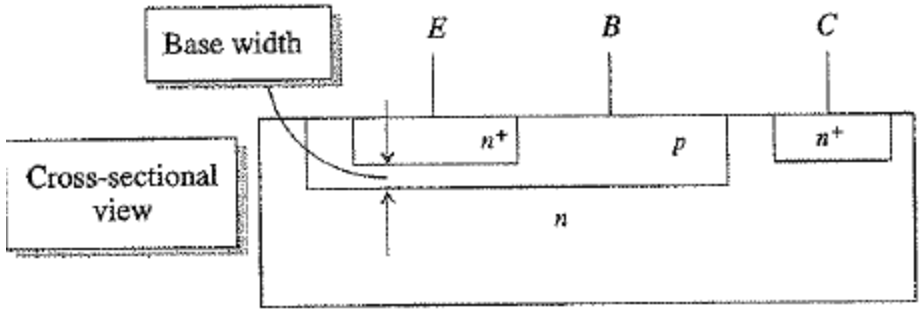
Field-effect transistors ⇒ channel constriction is controlled by gate bias.

Two different ways to control water flow.

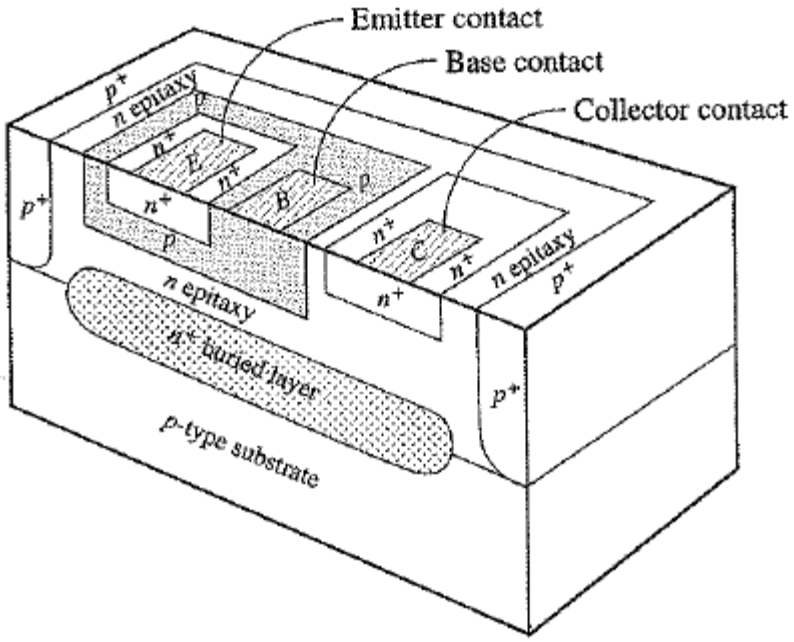
Bipolar and MOSFET use different approaches to control the current flow through the device.

History of Bipolar and MOSFET

Optional: Architecture of Bipolar Transistor



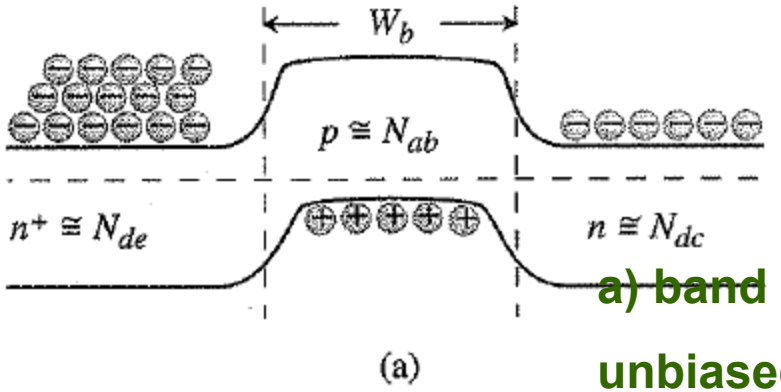
cross-section



3D view of a bipolar transistor

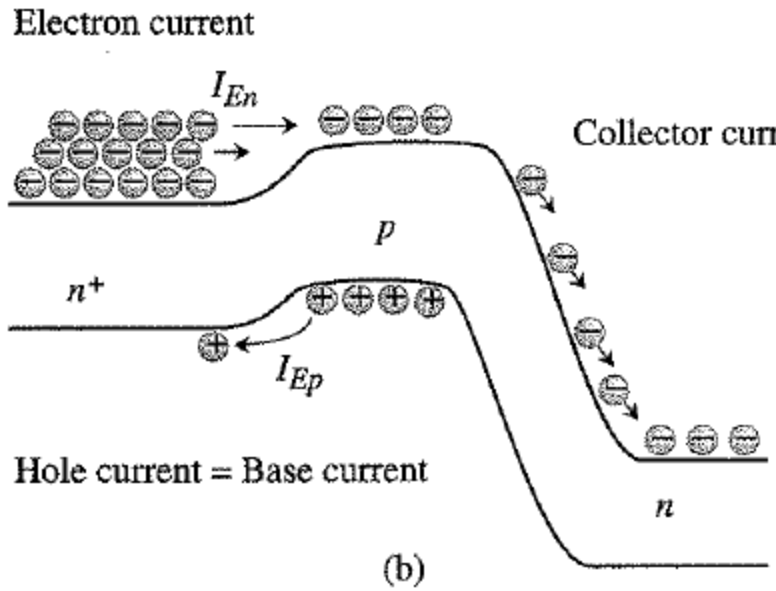
A schematic of the structure of a bipolar junction transistor with a simplified view of the cross-section.

Optional: The Operation principle of the Bipolar Transistor



$W_b \ll L_n$

a) band profile of an unbiased n+p BJT



$N_{de} >> N_{ab}$
$\Rightarrow I_{En} >> I_{Ep}$
$\Rightarrow \Delta I_C >> \Delta I_B$

b) band profile of a BJT in the forward active mode