Hot Carrier Effects

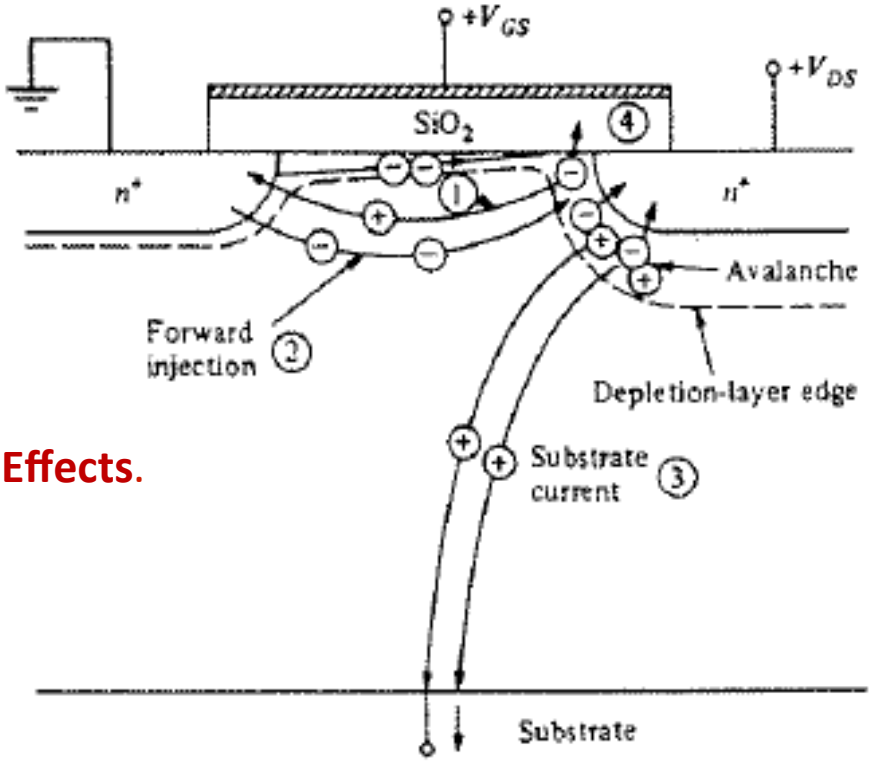
- As feature size decreases, at constant voltage bias electric field in channel region increases which leads to gain high kinetic energy by holes & electron (hot carriers) .

- High kinetic energy enables injection into the gate oxide and formation of interface states , which in turns causes degradation of circuit performance.

- Hot carriers are also the origin of substrate and gate currents.

What does "Hot" mean?
electron energy:
E=26 meV for T=300K

E=1 eV for T=1.2 10^4 K



- All these effects are called **Hot Carrier Effects**.

Hot Carrier Effects driven by high Electric Fields

$$E_{y\max} = (V_{ds} - V_{dssat})/l$$

Channel length
L dependence

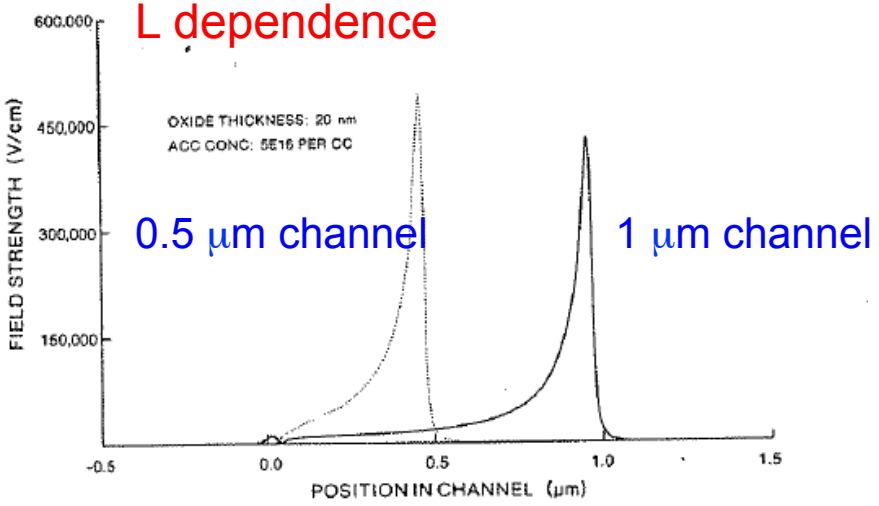


Fig. 9-2 $\mathcal{E}_y$ within an NMOSFET as a function of channel length for two devices with channel lengths of 1.0 μm and 0.5 μm, and the same value of t_{ox} = 20 nm.[146]

Oxide thickness
t_{ox} dependence

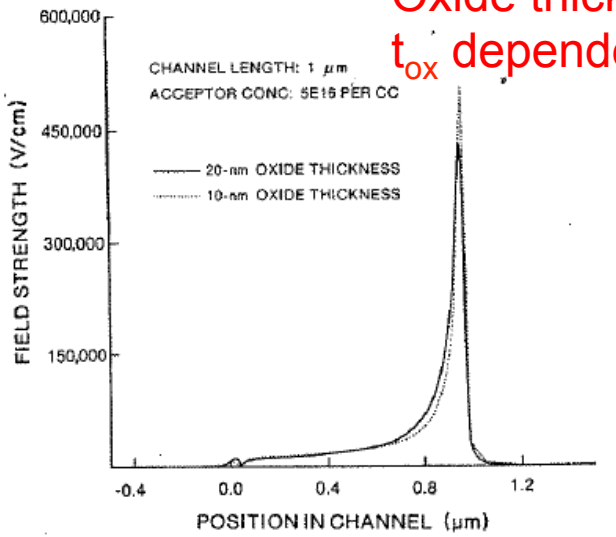


Fig. 9-3 $\mathcal{E}_y$ within an NMOSFET as a function of channel length and gate oxide thickness for two devices with a channel length (1.0 μm) and two values of t_{ox}, 10 and 20 nm.[146]

Empirical formulae for the width of the electrical field peak at the drain

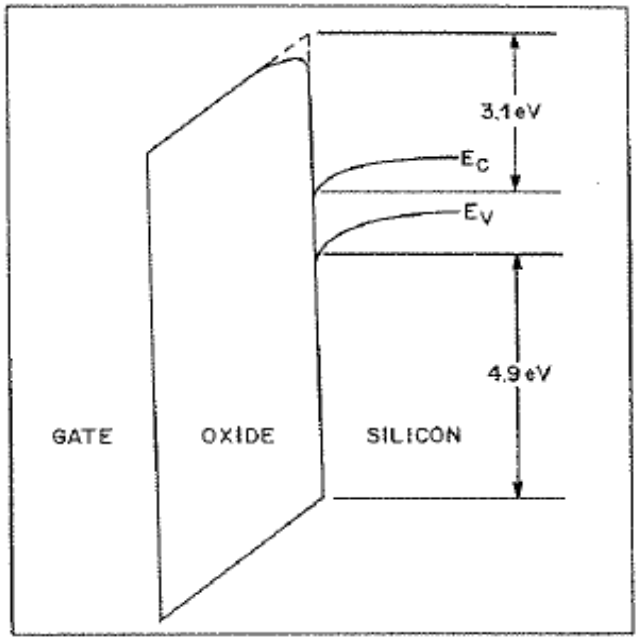
$$l = 0.22 \cdot t_{ox}^{1/3} r_j^{1/2} \quad for \quad t_{ox} \geq 15nm$$

r_j is the s/d junction depth

$$l = 1.7 \cdot 10^{-2} \cdot t_{ox}^{1/8} r_j^{1/3} L^{1/5} \quad for \quad t_{ox} < 15nm \ and \ L < 0.5\mu m$$

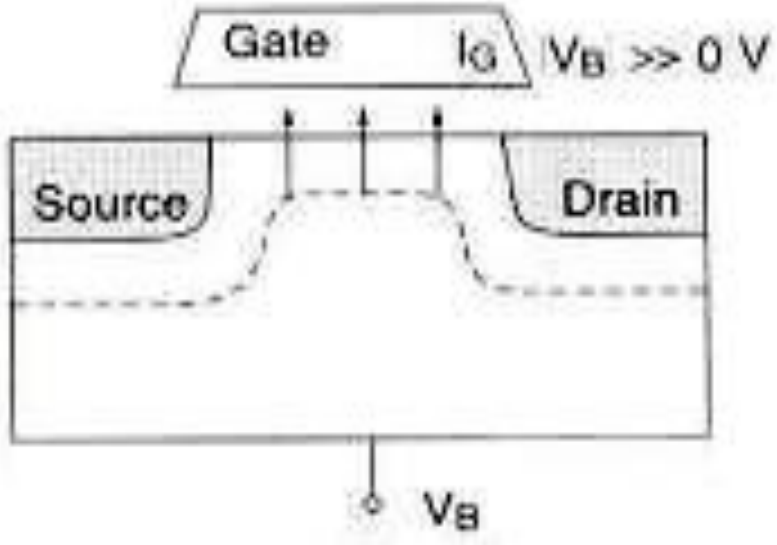
Different Type of Hot Carrier Injection

- Drain Avalanche Hot carrier (DAHC) Injection
- Channel Hot Electron (CHE) Injection
- Substrate Hot Electron (SHE) Injection
- Secondary generated hot electron (SGHE) injection



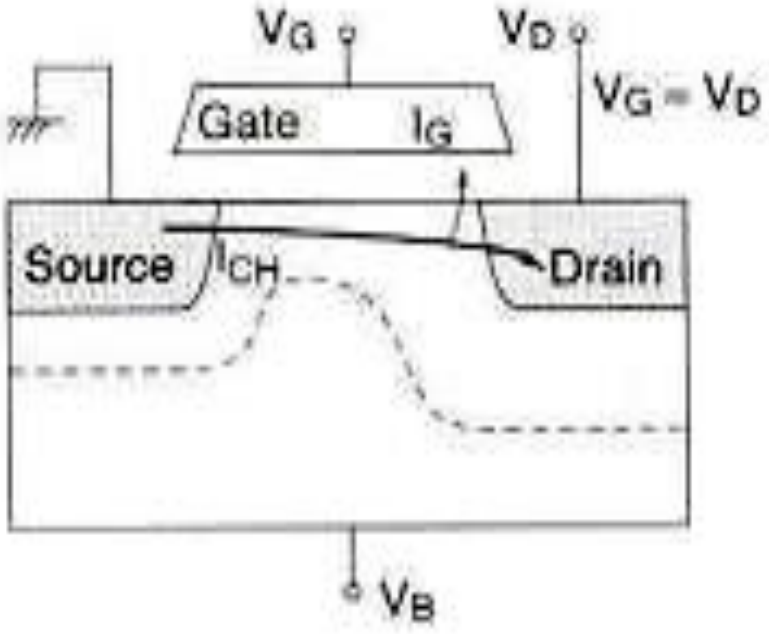
Substrate Hot Electron (SHE) Injection

- Occurs when the substrate back bias is very positive or very negative
- Carriers of one type in the substrate are driven by the substrate field toward the Si-SiO_2 interface.
- Gain high kinetic energy from strong electric fields and are injected into SiO_2.



Channel Hot Electron (CHE) Injection

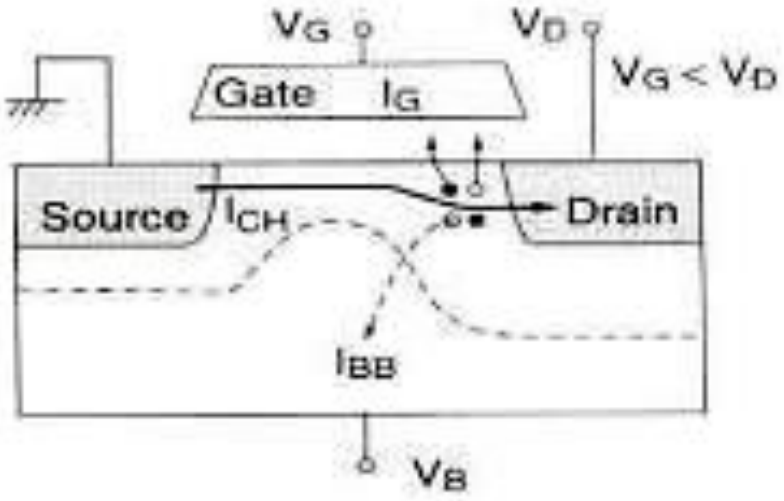
- When both $V_G = V_D$ higher than source voltage , some electrons are driven towards gate oxide
- Note that at these bias conditions electrons are attracted to the gate electrode



Drain Avalanche Hot carrier (DAHC) Injection

- When $V_D > V_G$, the acceleration of channel carrier causes Impact Ionization (avalanche).

- The generated electron – holes pair gain energy to break the barrier in Si-SiO_2 interface



Charge Generation inside Gate Dielectric (SiO_2)

- Negative charge generation
- Interface state (unsatisfied dangling bonds of Si) Q_i or D_{it} generation
- Positive charge generation

Hot Carriers and Substrate Current

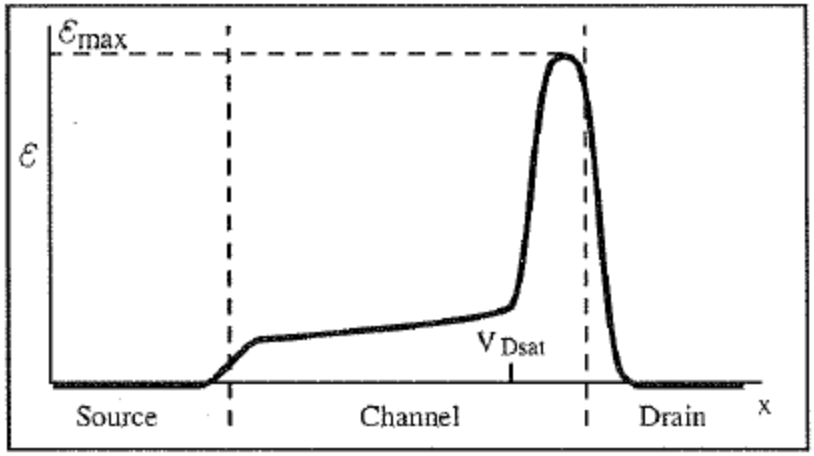


Figure 7.34: Lateral electric field, $\mathcal{E}$, at the surface of a MOSFET in saturation.[29]

In saturation regime electrons cross a very high lateral field region near the drain. They acquire high kinetic energy that they can cause impact ionization. Impact ionization leads to a high substrate current.

Highly energetic carriers create also permanent damage at the Si-SiO_2 interface and in the SiO_2. This damage alters the I-V characteristics of the MOSFET (degradation, reliability issue.
Some of the hot carriers may reach the gate and constitute gate current.

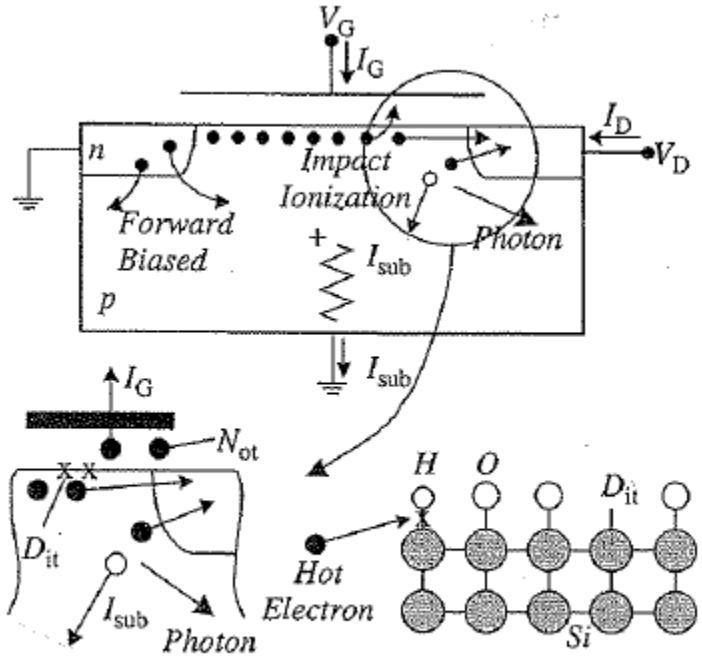
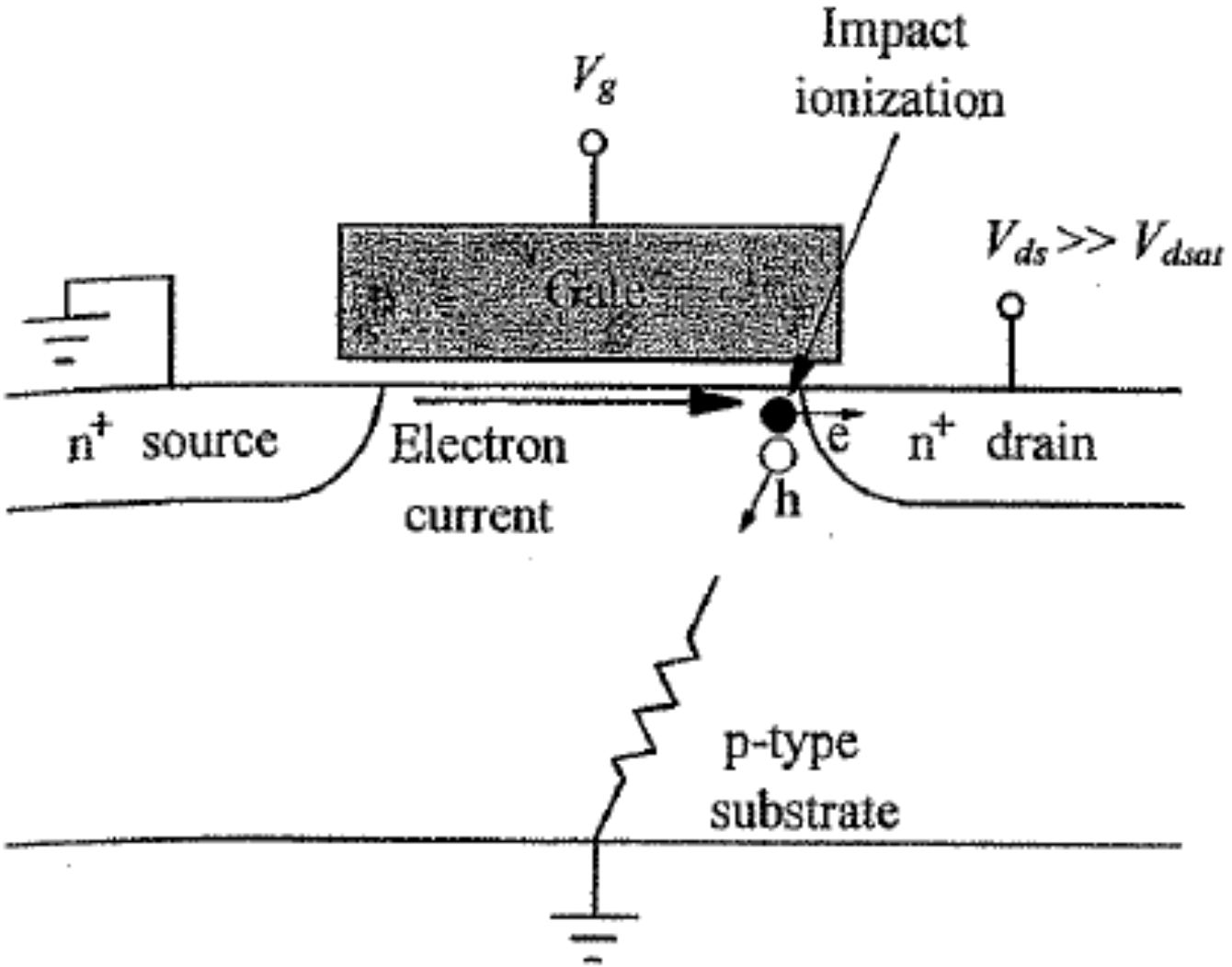


Fig. 12.8 Effect of hot electrons near the drain of MOSFETs.

Hot Electrons and Substrate Current



Hot Carriers

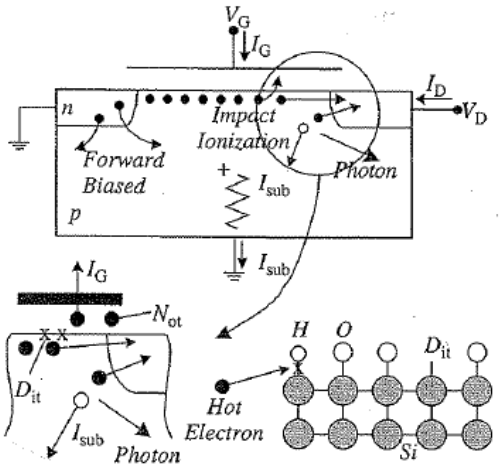


Fig. 12.8 Effect of hot electrons near the drain of MOSFE

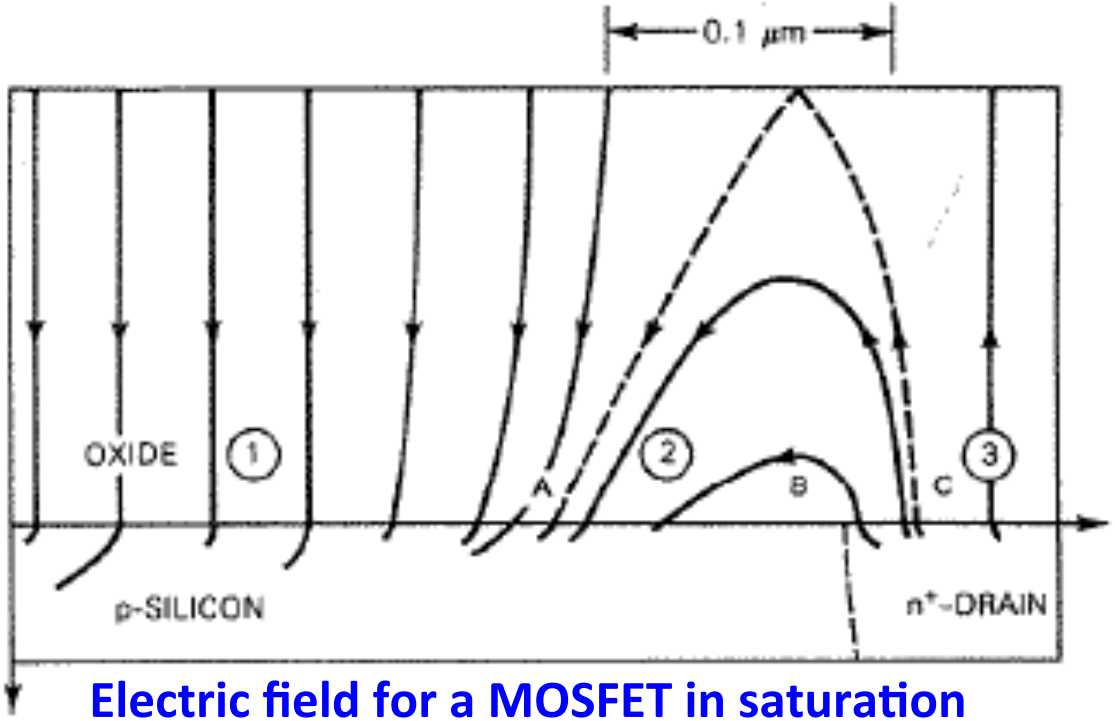
Electric field in the dielectric near the drain region determines the location of electron and hole injection into the oxide and into the gate.

Reversal of polarity of the vertical electric gate field :

Electrons are attracted by positive field;

Hole are attracted by negative field;

This determines the location of electron and hole injection.



Electric field for a MOSFET in saturation

Figure 6.8 Two-dimensional electric field distribution near the drain of an *n*MOS. $V_d = 8$ V, $V_g = 7$ V, $V_B = -2.5$ V, $L_{eff} = 1.3$ μm and $t_{ox} = 400$ Å (Ref. 26, © 1984 IEEE).

Hot Carriers and Substrate Current

4-10-2014

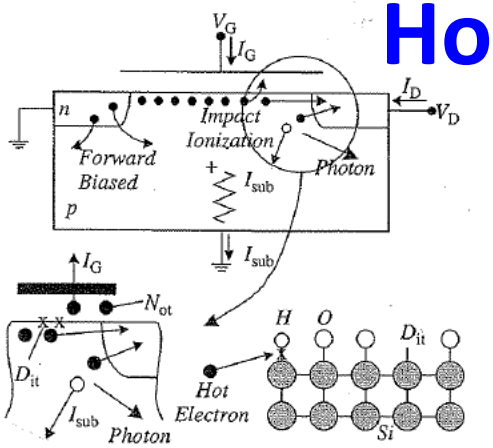
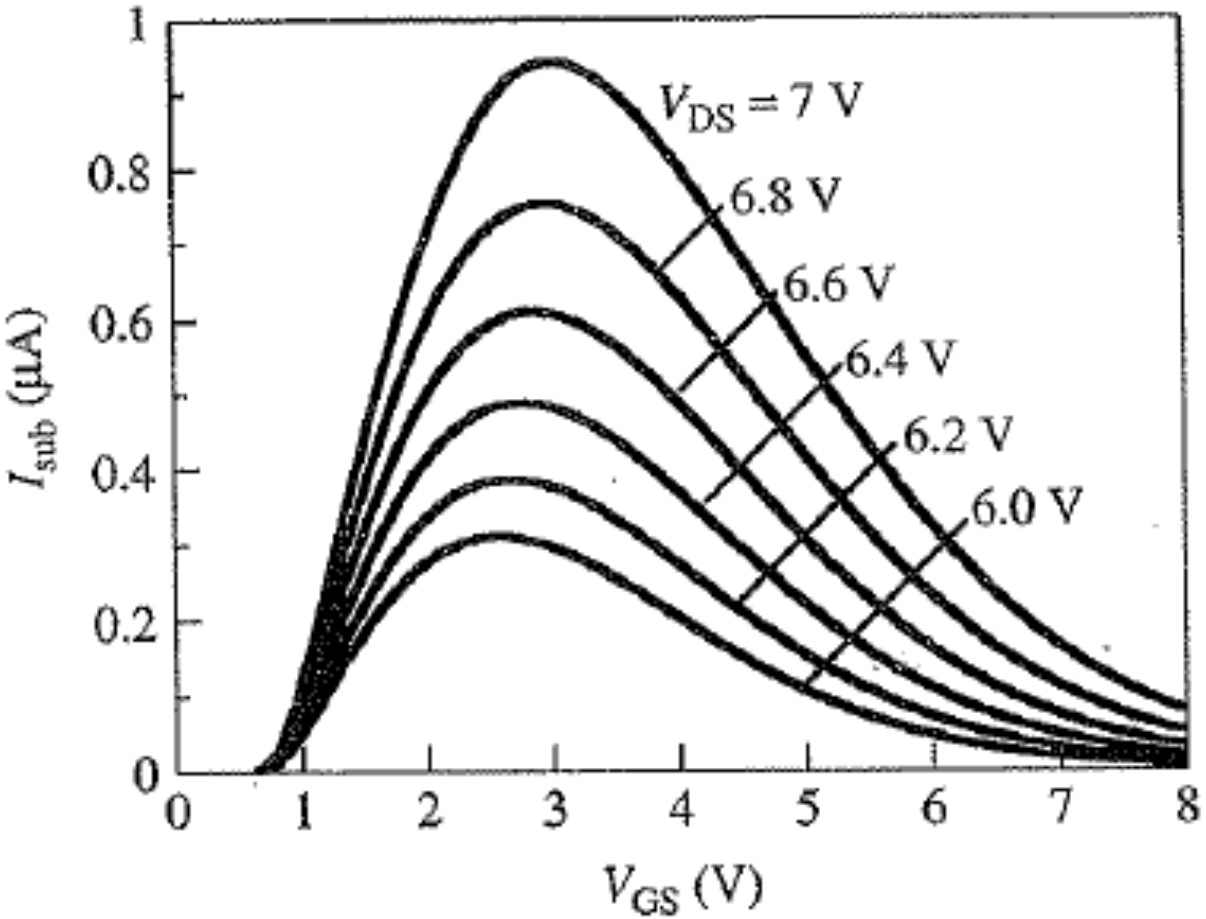


Fig. 12.8 Effect of hot electrons near the drain of MOSFETs.

The substrate current at a given drain bias, let say V_D=7V, increases first with the gate bias, because the current density increases. Note that the transistor operates in saturation regime and there is a high lateral field peak close to the drain where the impact ionization (II) is taking place. As the gate bias increases beyond the peak value the lateral electric field at the drain begins to decrease and consequently the impact ionization decreases as well.

For high impact ionization we need both a lot of carriers and a high electric field.



Substrate current dependence on drain and gate bias. Observe that the maximum of the substrate current takes place at about $V_{gs} \approx V_{ds}/3 - V_{ds}/2$.

Hot Carrier Effects

Hot carrier effects (including substrate current) are getting worse with scaling MOSFET to smaller dimensions because of increased local electric fields at the same voltages.

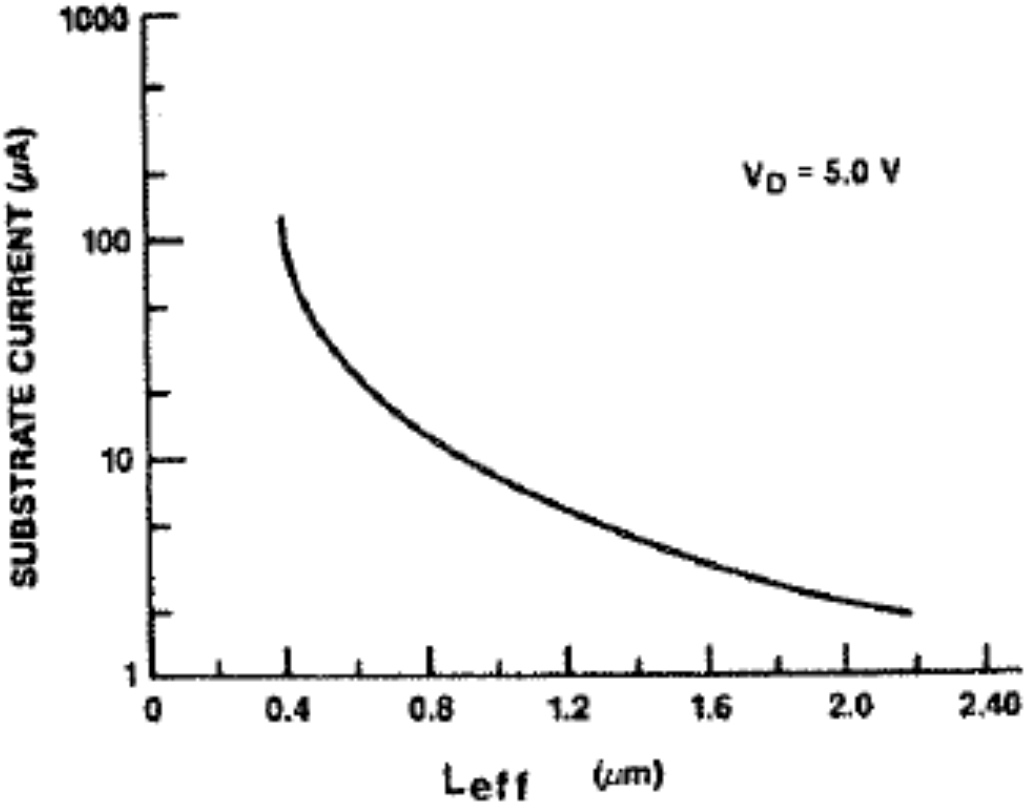
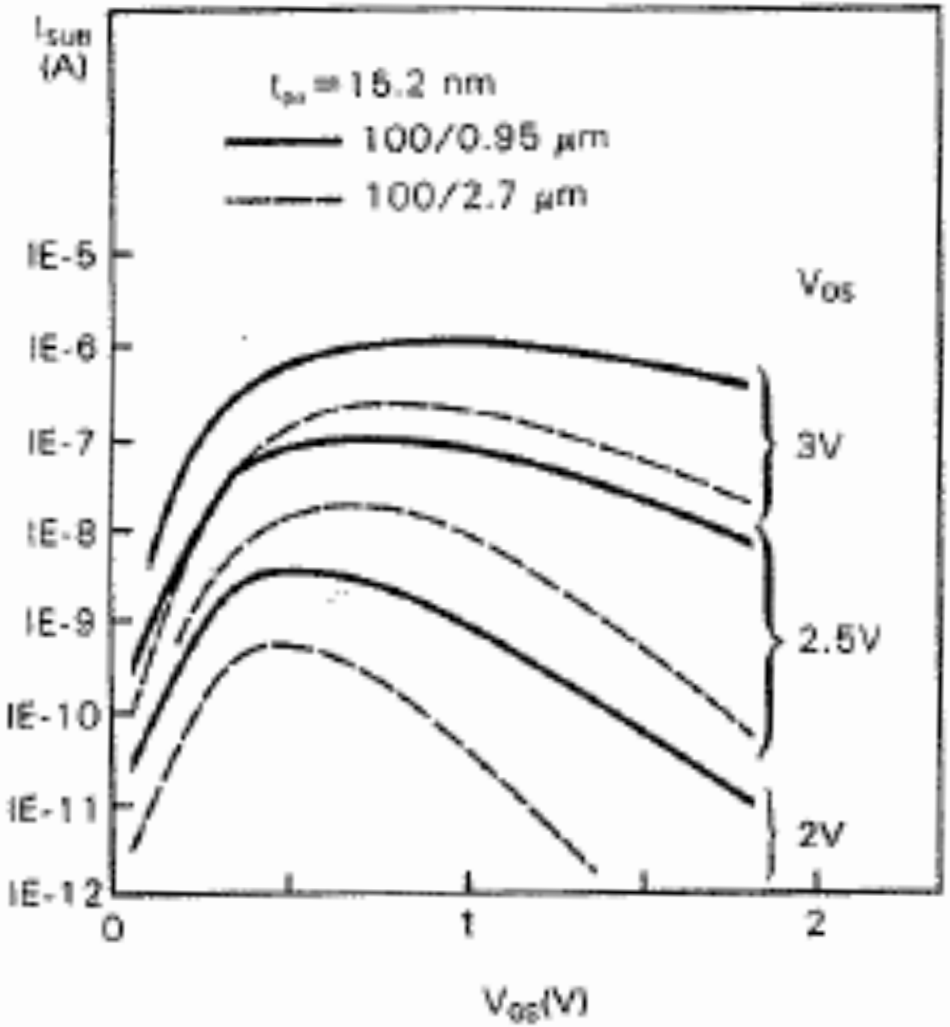


Fig. 9-4 The maximum substrate current due to impact ionization produced at a drain voltage of 5V vs. L_{eff} for MOSFETs with $t_{ox} = 250Å$.[6]

Hot Carriers and Substrate Current

Substrate current dependence on channel length: L=2.97 μm vs L=0.95 μm



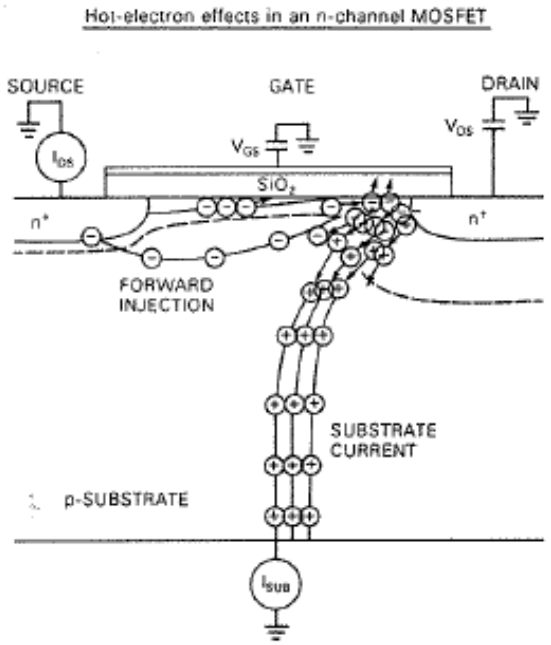
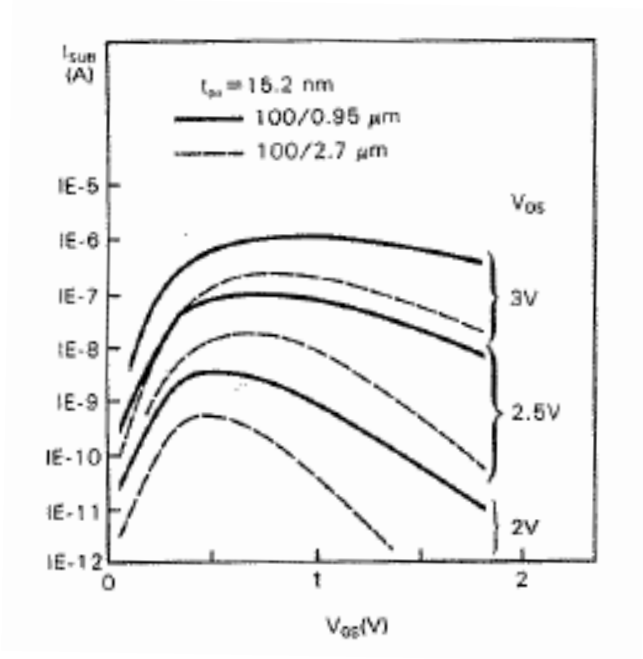


Figure 6.6 Schematic of hot-electron effects in an *n*-channel MOSFET.

Hot Carriers and Substrate Current and its Implications



Implications of excessive substrate current:

1) I_{sub} causes voltage drop in the resistive substrate on the order of 0.6V and forward biases the substrate-source junction. Electrons will then be injected from the source to the substrate. These electrons travel to drain and undergo impact ionization. A positive feedback loop is being established. It can lead to so called snapback breakdown.

2) The holes created in impact ionization travel back to the source and may undergo secondary impact ionization.

3) Latchup in CMOS circuits

Physics of the substrate current

$$I_{sub} \propto I_d$$

$$I_{sub} \propto \exp\left(-\frac{\Phi_i}{\lambda_e E_{y\max}}\right) = \exp\left(-\frac{\Phi_i}{kT_e}\right)$$

$$\rightarrow I_{sub} = C_1 I_d \exp\left(-\frac{\Phi_i}{\lambda_e E_{y\max}}\right)$$

$$E_{y\max} = (V_{ds} - V_{dssat})/l$$

$$l = 0.22 \cdot t_{ox}^{1/3} r_j^{1/2}$$

$$I_{sub} = C_1 I_d \exp\left(-\frac{0.22 \cdot t_{ox}^{1/3} r_j^{1/2} \Phi_i}{\lambda_e (V_{ds} - V_{dsat})}\right) = C_1 I_d \exp\left(-\frac{B_1}{(V_{ds} - V_{dsat})}\right)$$

Φ_i is the threshold energy for impact ionization, λ_e is the electron free mean path; so $\lambda_e E_{ymax}$ is the amount of energy gained by an electron before collision, and exp(- Φ_i / $\lambda_e E_{ymax}$) is the probability that an electron will cause impact ionization.

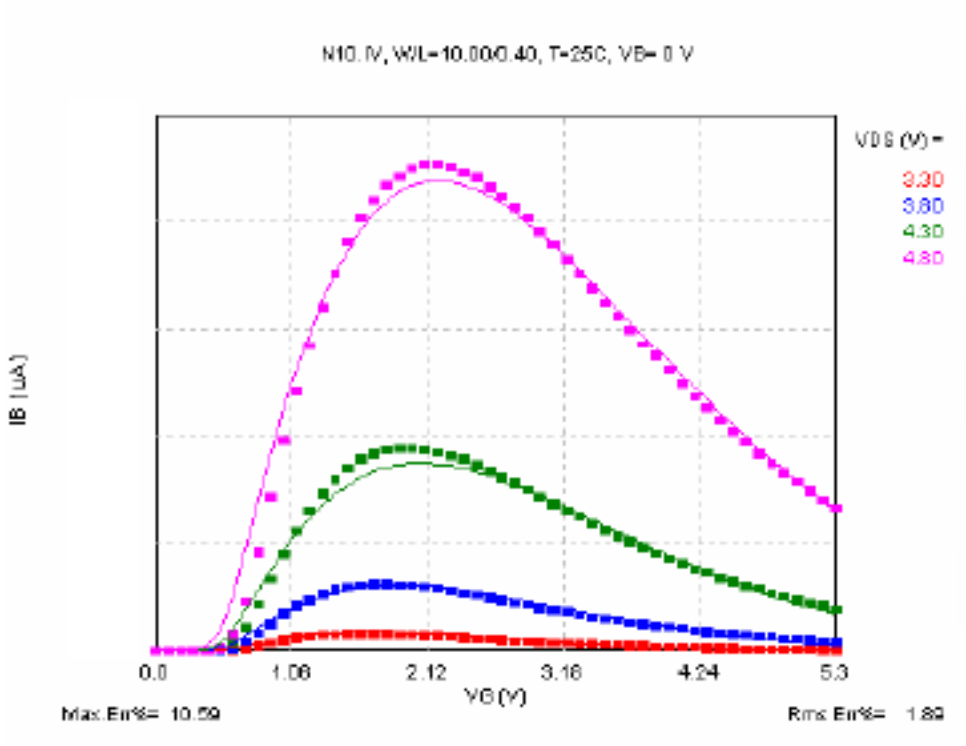
$\lambda_e E_{ymax}$ the kinetic energy of an electron, can be translated into electron temperature T_e. (Similar to Arrhenius law)

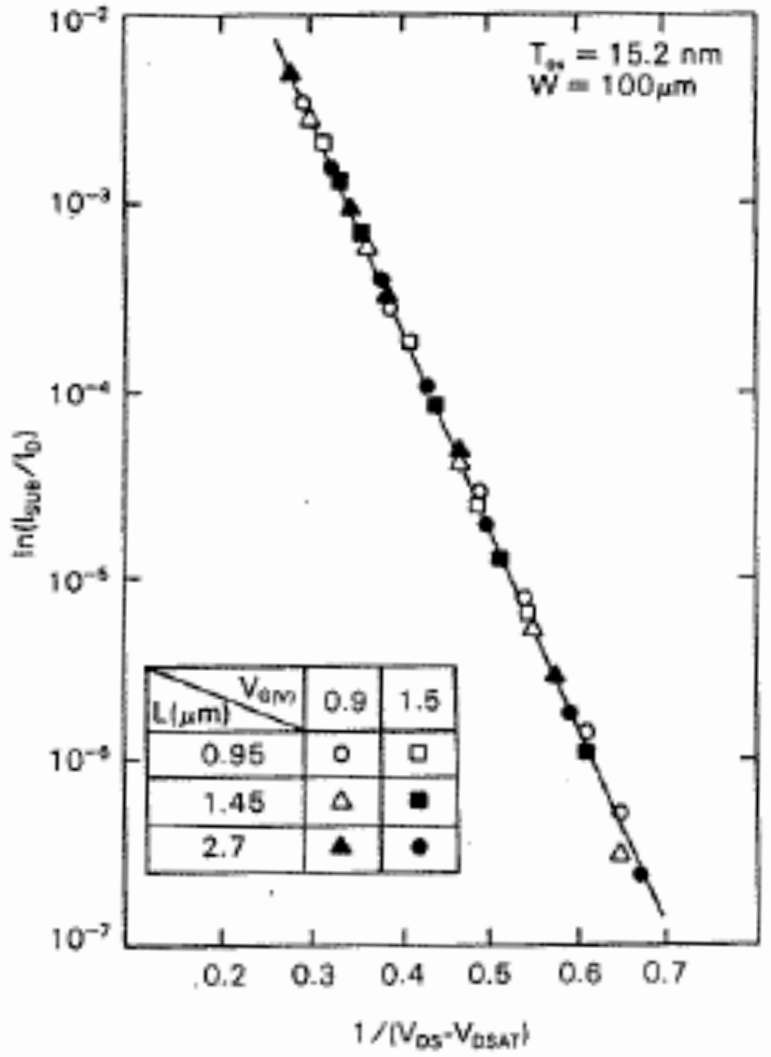
Hot Carriers and Substrate Current

Universal behavior of I_{sub} as a function of V_{ds}-V_{dsat}.

Slightly modified equation

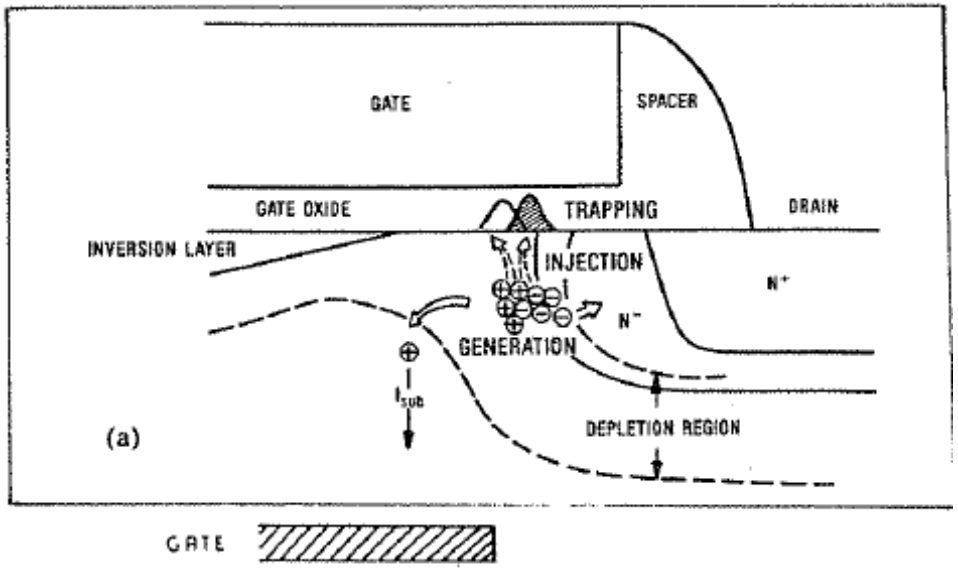
$$I_b = \frac{A_i}{B_i}(V_{ds} - V_{dsat}) I_d \exp\left(-\frac{B_i l_c}{V_{ds} - V_{dsat}}\right)$$





Universal nature of the curve gor all L and Vg

Injection of electrons and holes into the oxide. Degradation



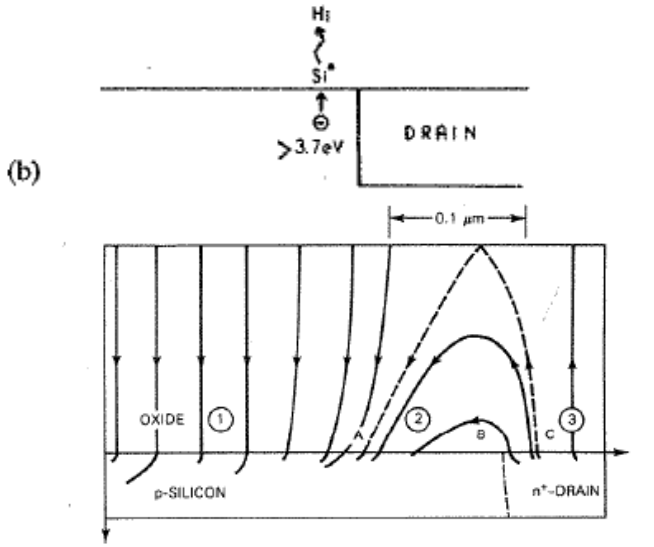


Figure 6.8 Two-dimensional electric field distribution near the drain of an *n*MOS. V_d = 8 V, V_g = 7 V, V_B = −2.5 V, L_{eff} = 1.3 μm and t_{ox} = 400 Å (Ref. 26, © 1984 IEEE).

Needed electron energy ~ 4eV:

Electron has to overcome Si-SiO_2 barrier 3.2eV

Has to break Si-H bond ~ 0.3 eV

Has to overcome repelling electric field 0.3 - 0.5 eV → together ~ 4eV

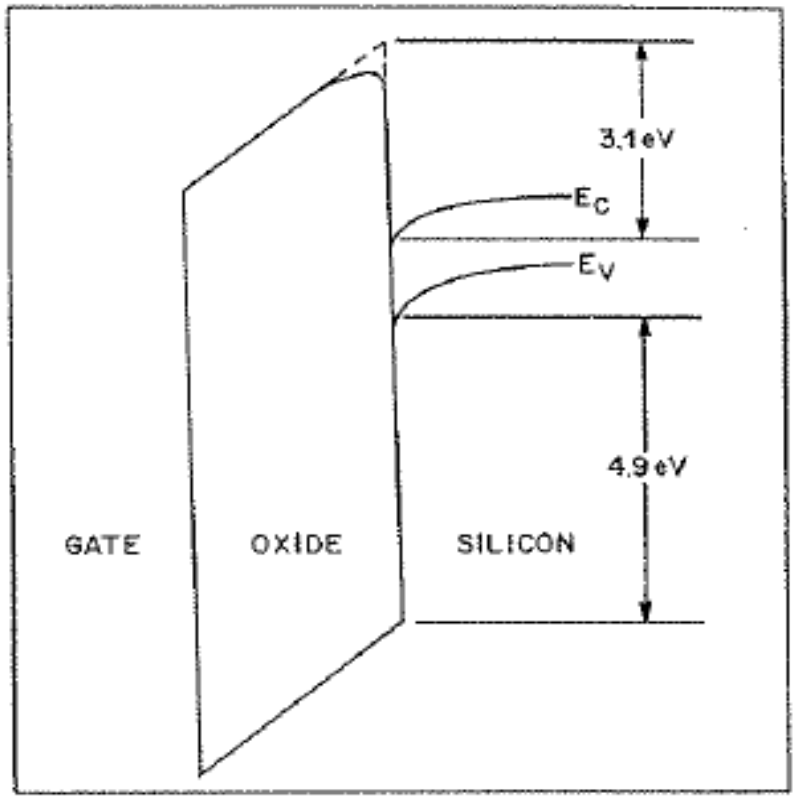
Situation for holes is more complicated:

Holes are not provided by the current but are generated during impact ionization; thus when created they are "cold". However, they accelerate in the local lateral field and acquire energy AND the vertical electric field is attractive for hole injection.

Hole has to overcome Si-SiO_2 barrier of 4.9V

Degradation (Exercise for ZrO_2)

Injection of electrons and holes into the oxide.



Needed electron energy ~ 4eV

Electron has to overcome Si-SiO_2 barrier 3.2eV

Has to break Si-H bond ~ 0.3 eV

Has to overcome repelling electric field 0.3 - 0.5 eV

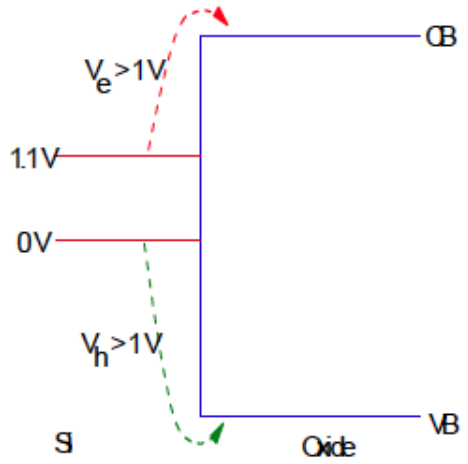
Situation for holes is more complicated:

Holes are not provided by the current but are generated during impact ionization; thus: when created they are cold. However, they accelerate in the local lateral field and the vertical electric field are attractive for hole injection.

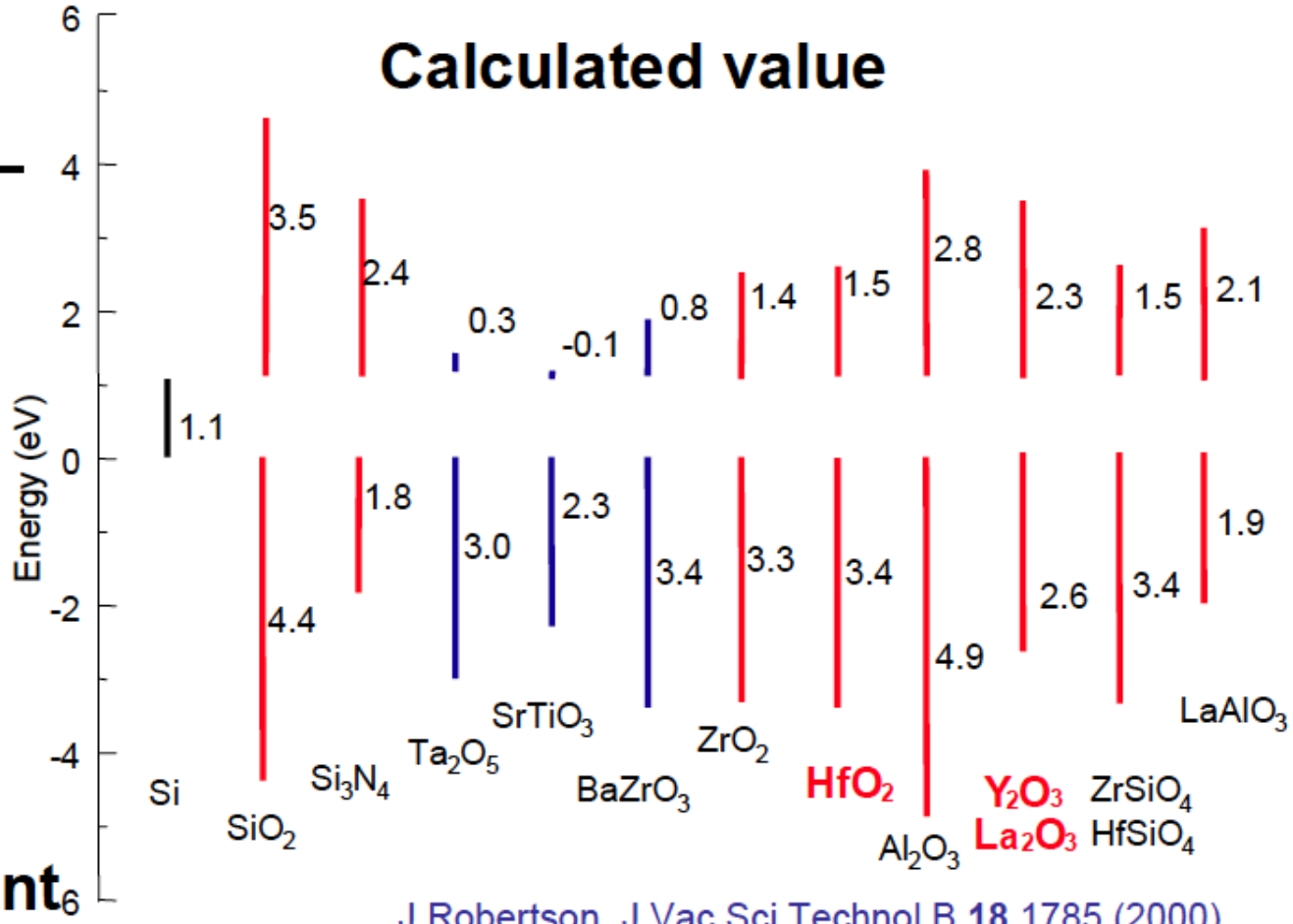
Hole has to overcome Si-SiO_2 barrier of 4.9V

High-k Dielectrics

Band Offsets



Dielectric constant



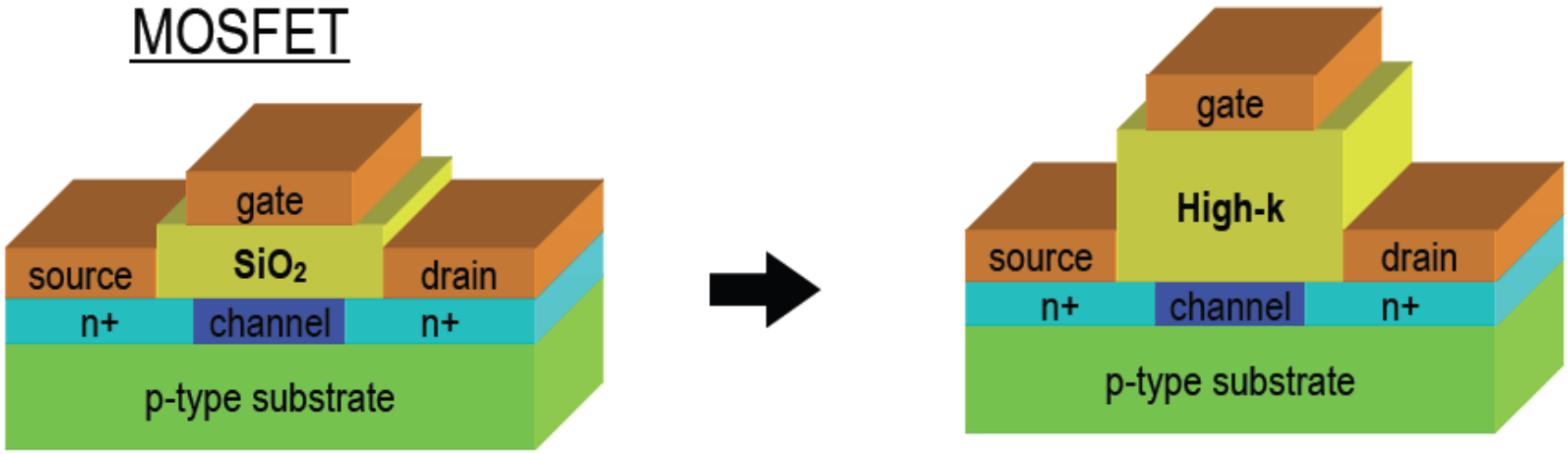
J Robertson, J Vac Sci Technol B **18** 1785 (2000)

SiO2; 4
Si3N4: ~ 7
Al2O3: ~ 9

Y2O3; ~10
Gd2O3: ~10

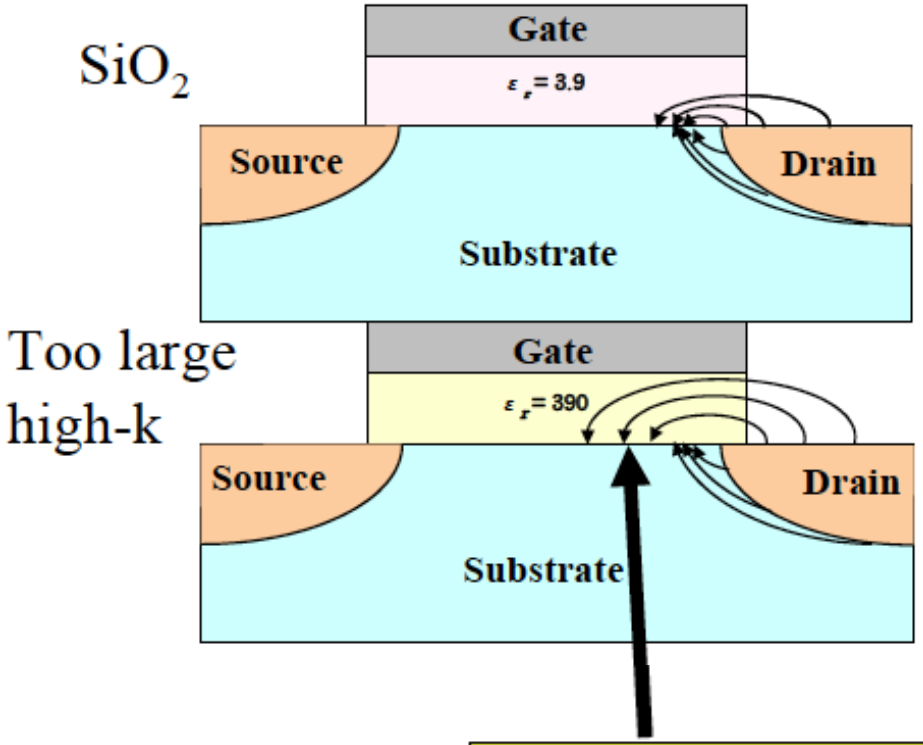
HfO2; ~23
La2O3: ~27

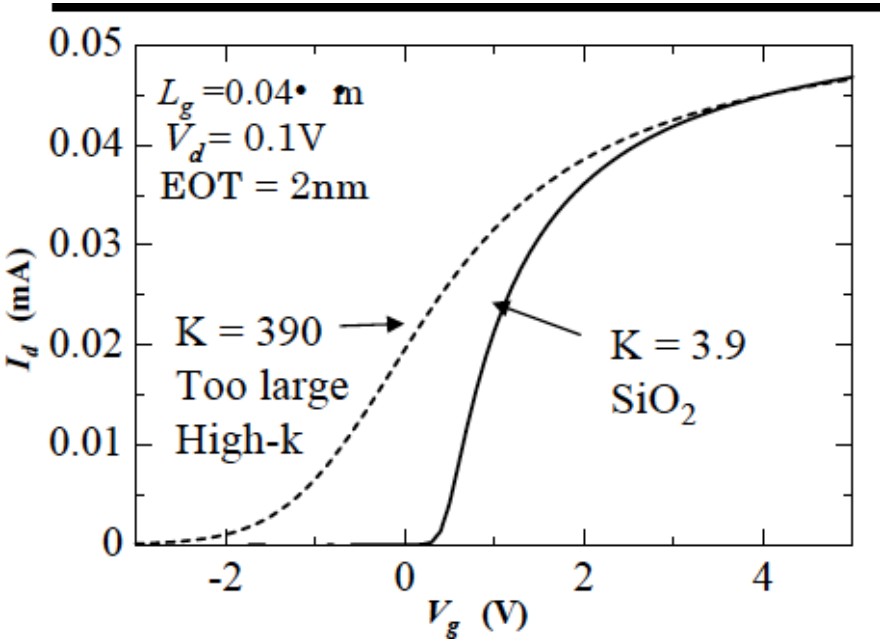
High-k Thin Film for Gate Insulator



	2005	2007	2009	2011
Physical Gate Length (nm)	32	25	20	16
Equivalent Oxide Thickness (nm)	1.2	1.1	0.9	0.5, 0.8(DG)

Too large high-k cause significant short channel effect

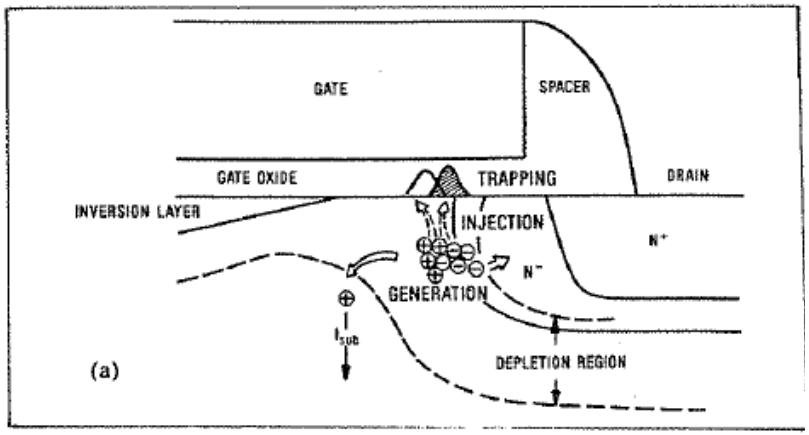


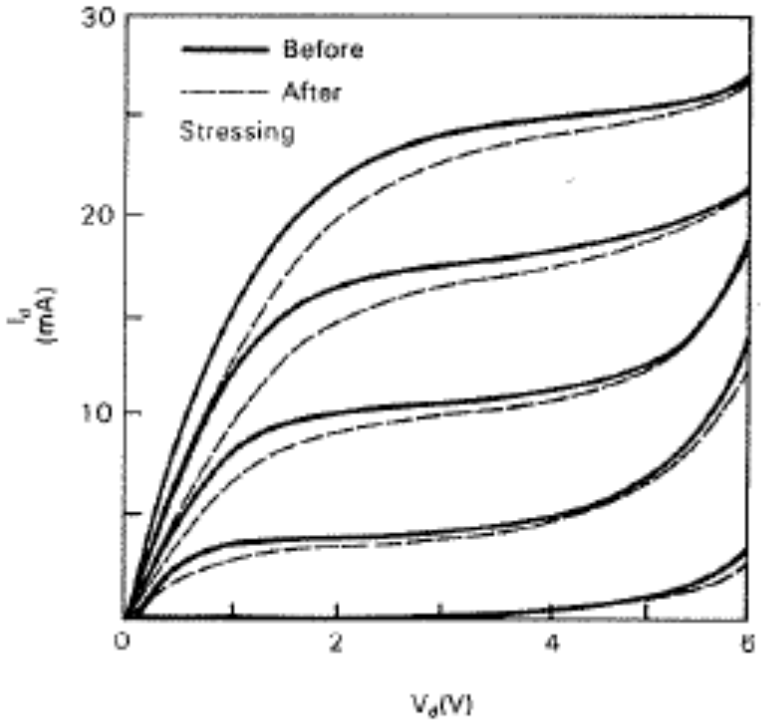


Penetration of lateral field from Drain through high-k causes significant short channel effects

Manifestation of Degradation

Characterization of degradation of a MOSFET transistor.





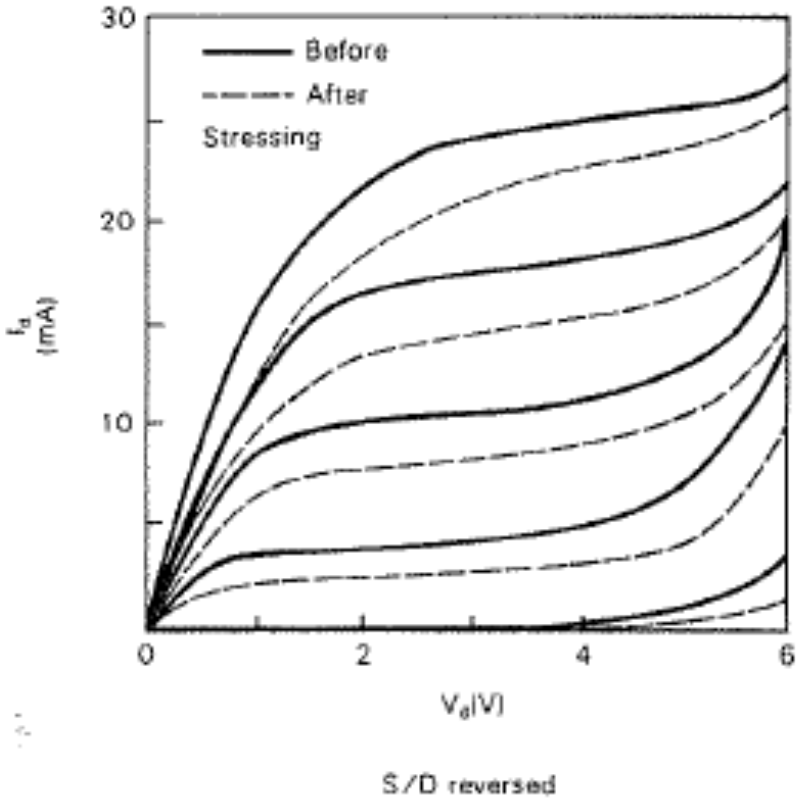


Figure 6.10 Degradation characteristics after stressing: (a) source/drain reversed during post-stress measurement; (b) source/drain unchanged during post-stress measurement (Ref. 29, © 1984 IEEE).

Substrate Current and carrier injection into the gate oxide are related as they both originate from the presence of **high electric fields.**

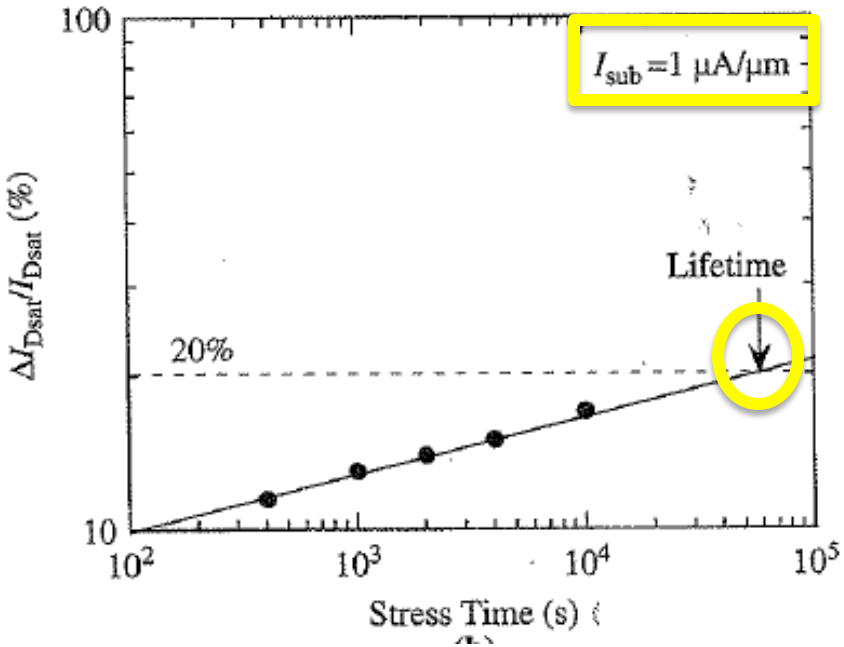
Actually, the substrate current which can be measured easily, has been chosen as the quantity to monitor gate oxide degradation.

Hot Carriers

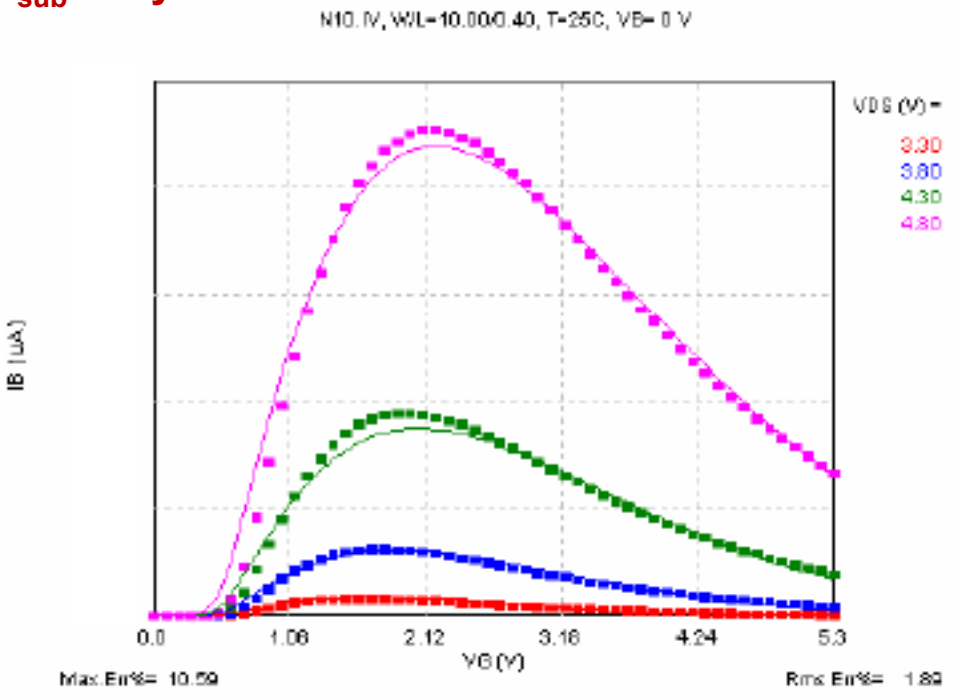
Substrate current and device lifetime

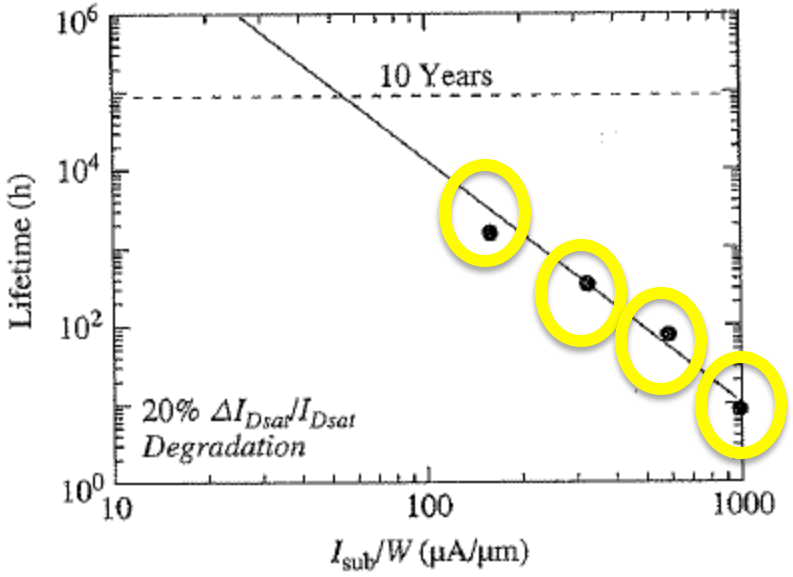
$$I_b = \frac{A_i}{B_i}(V_{ds} - V_{dsat}) I_d \exp\left(-\frac{B_i l_c}{V_{ds} - V_{dsat}}\right)$$

I_{sub} good indicator for degradation damage.
I_{sub} easy to measure



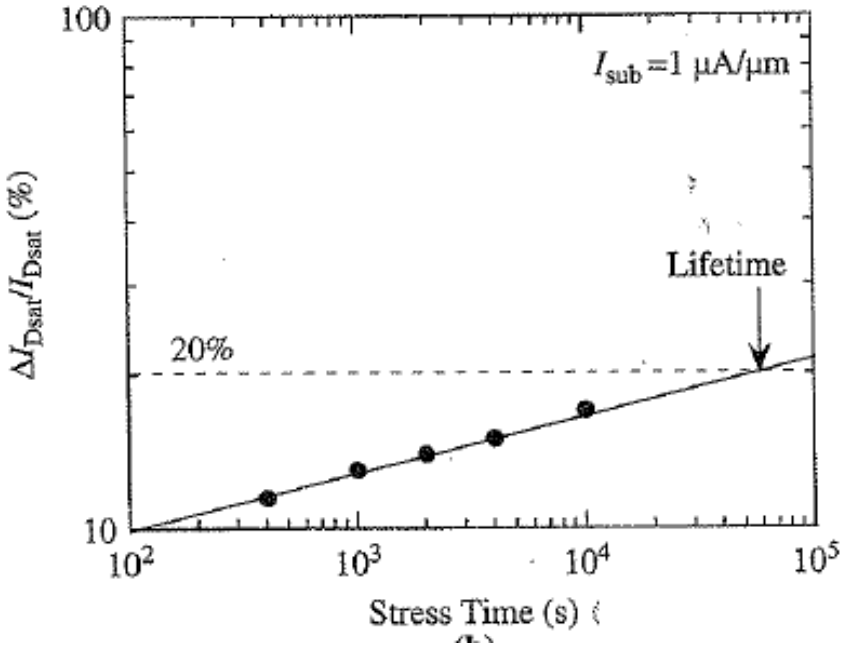
Bias at maximum substrate current



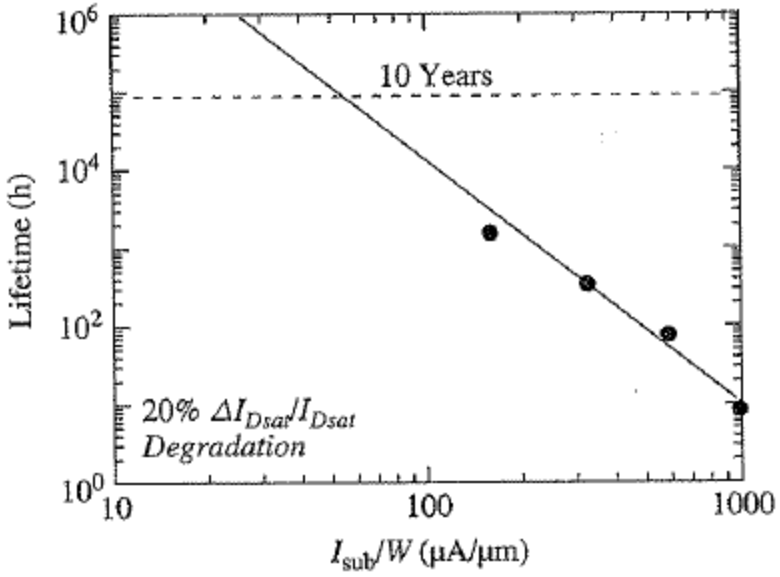


device lifetime determination:

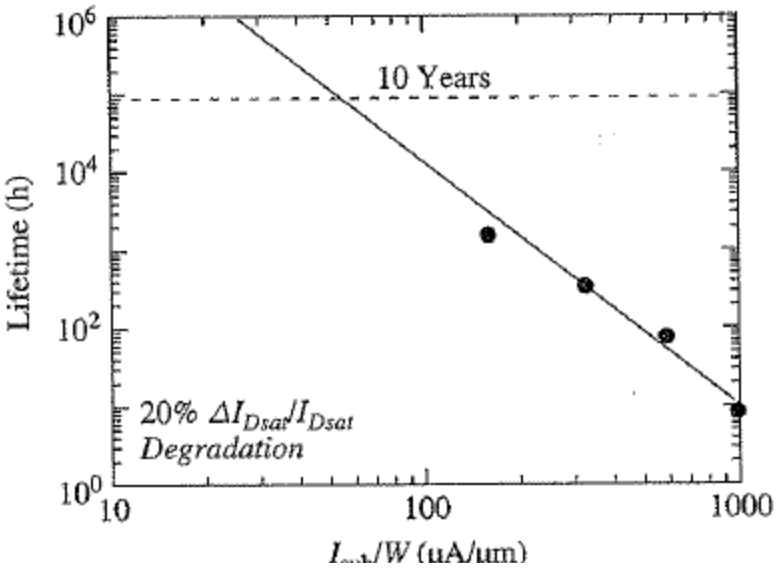
1) Monitor I_d or I_{dsat} as a function of stress time
2) Find expected time for a given change in current $\Delta I/I$
3) Determine a good indicator for stress (mostly I_{sub})
4) Plot the life time as a function of the stress indicator (I_{sub})
5) Your customer expects a product life time of 10 years
6) From your curves you can determine what is the average stress that the devices can tolerate without suffering a a specified degradation (here of $\Delta I/I$=20%)



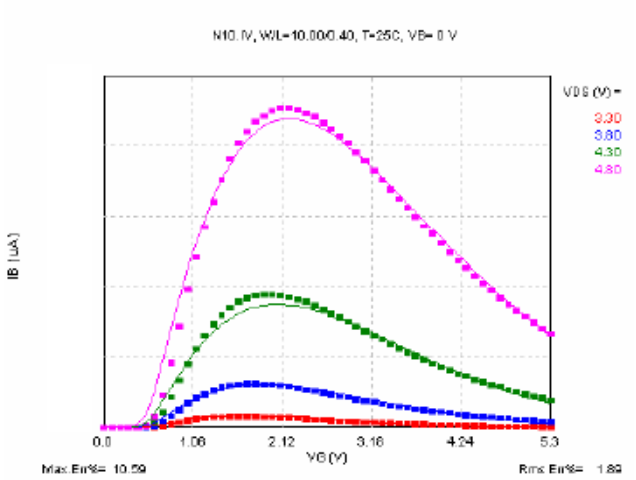
Bias at maximum substrate current



Substrate current and device lifetime



$$I_b = \frac{A_i}{B_i}(V_{ds} - V_{dsat}) I_d \exp\left(-\frac{B_i l_c}{V_{ds} - V_{dsat}}\right)$$



Hot carrier lifetime τ of the device:

$$\tau = K \frac{(I_{sub} / I_d)^{-m}}{I_d}$$

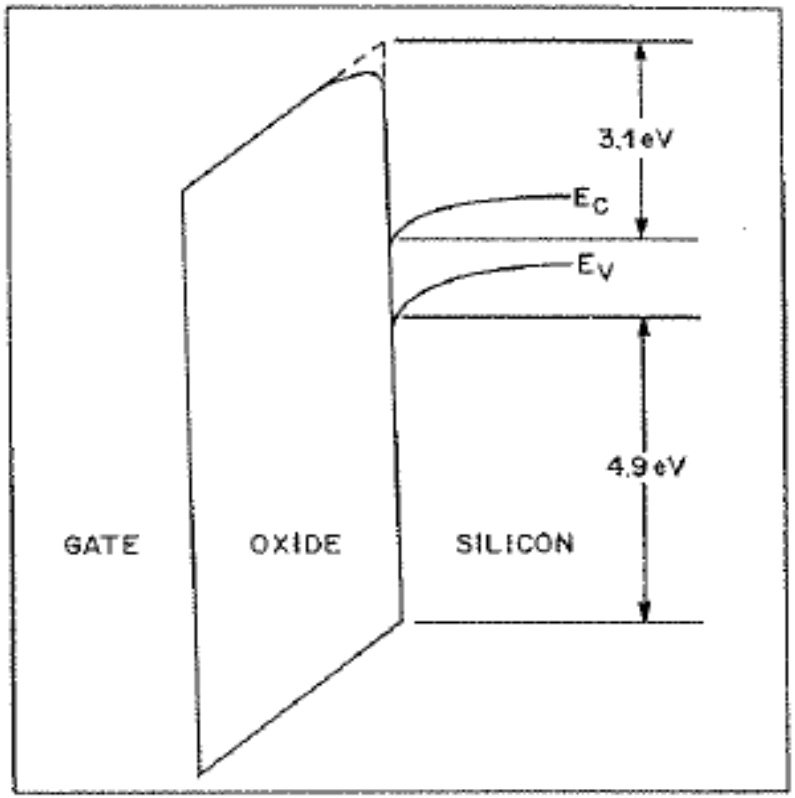
Or alternatively

$$\tau = K'(I_{sub} / I_d)^{-m}$$

Where m is approximately m=3
And K or K' are empirical constants.

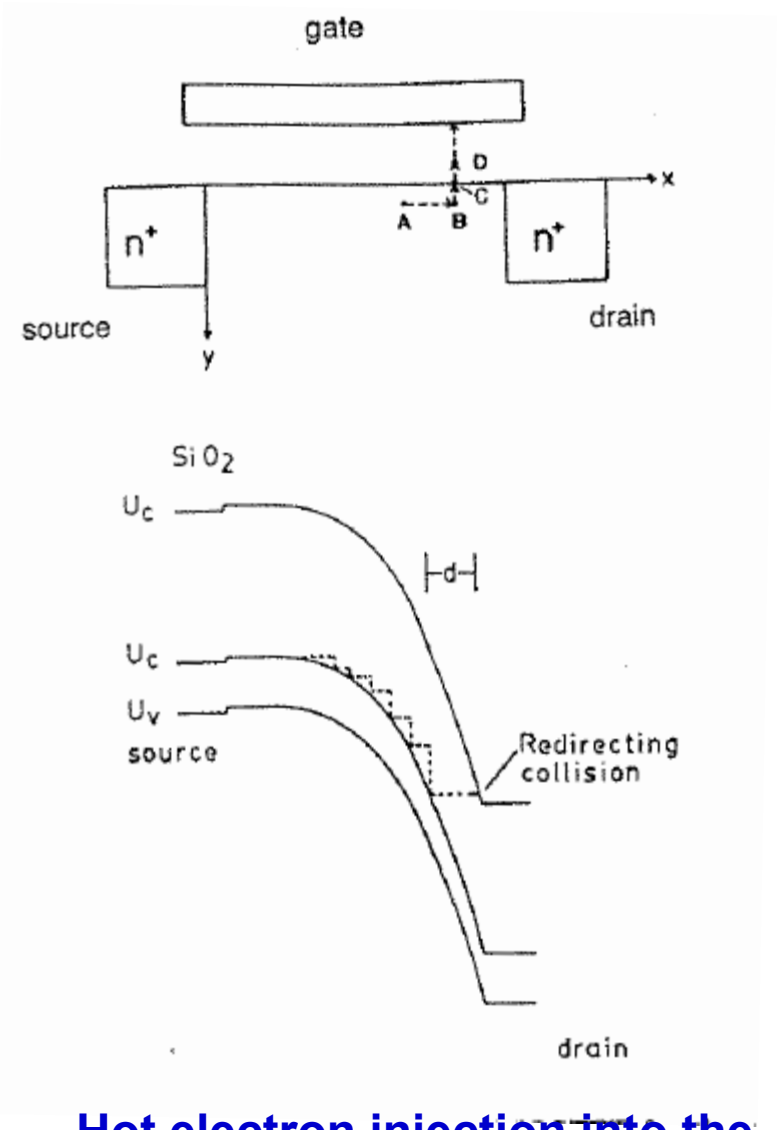
The equations were found to hold irrespective of the drain bias.

Gate Current



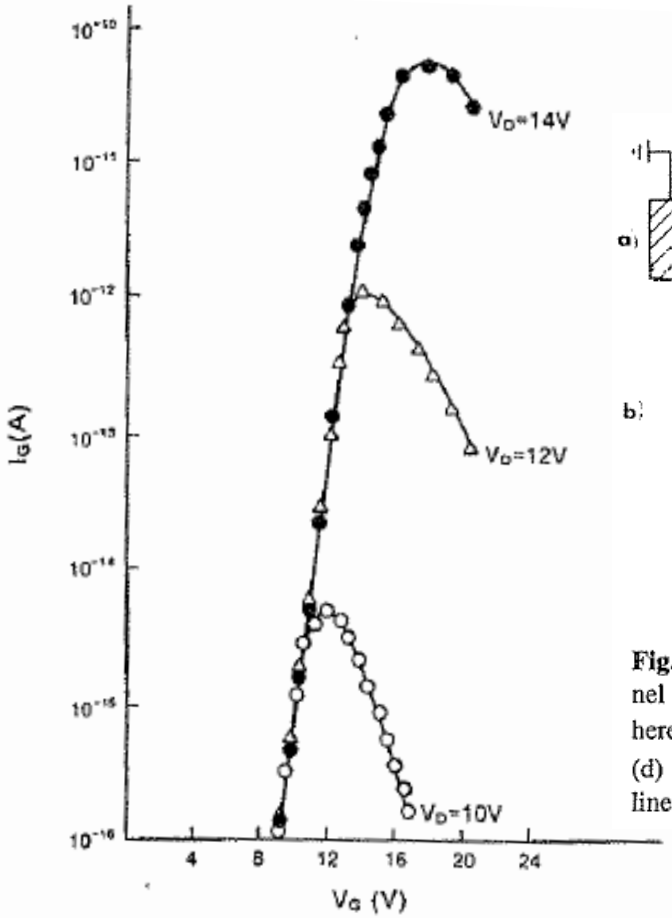
Barriers for electron and hole injection.

Channel hot electrons (CHE) are generally considered to be important, and channel hot hole injection is generally ignored.



Hot electron injection into the gate

Hot Electrons and Gate Current



Gate current due to channel hot electrons versus gate voltage, with V_{DS}

Saturation **linear regime**

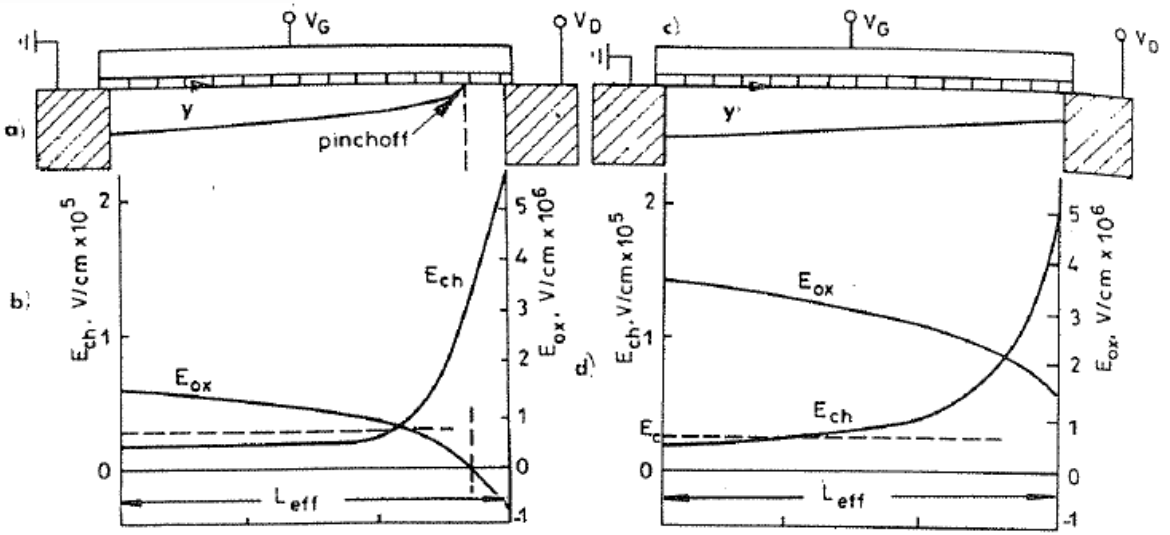
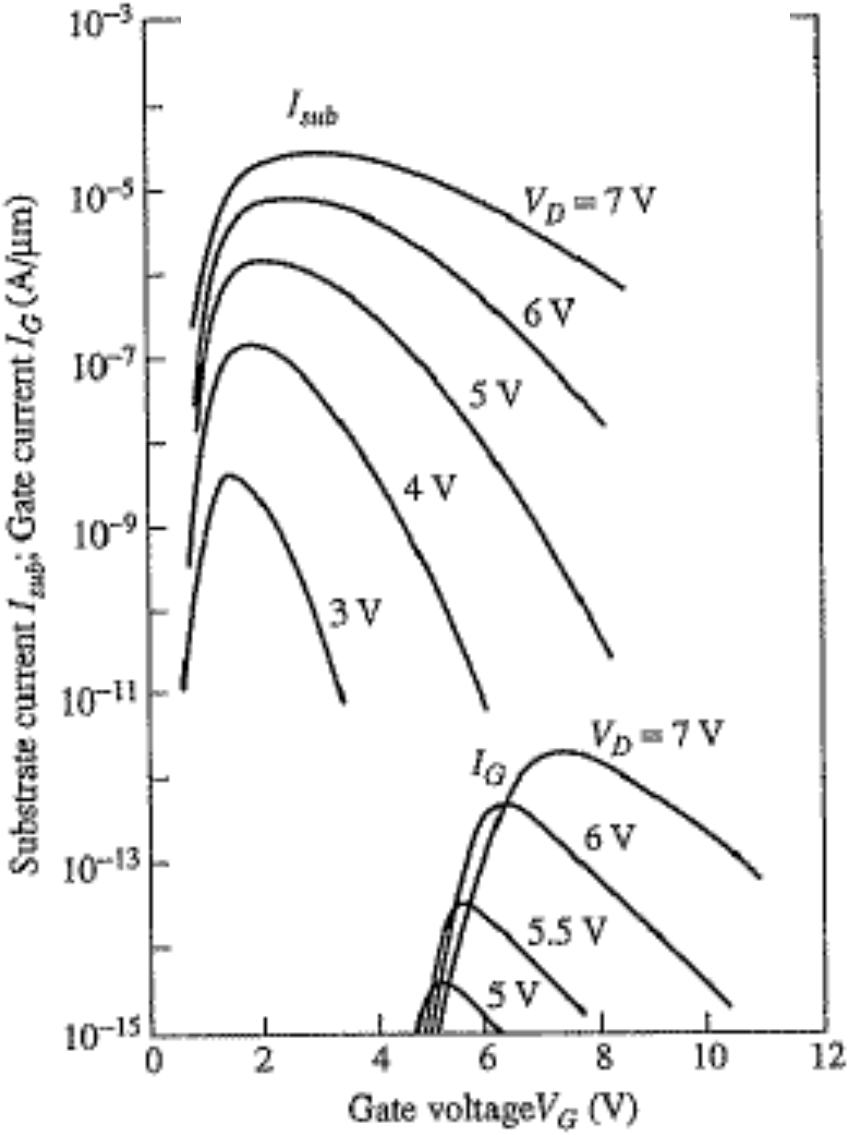


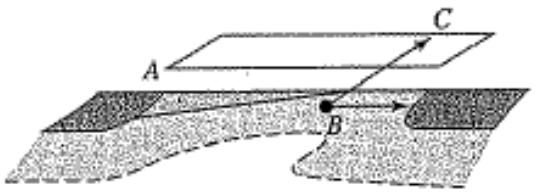
Fig. 7-8 (a) Cross section of MOS transistor operating in saturation. (b) The oxide and channel fields in the *y*-direction of the channel when the MOSFET is in saturation (i.e., $V_{GS}<V_{DS}$, here V_{GS} = 6V and V_{DS} = 8V). (c) Cross section of a MOS transistor operating in linear regime. (d) The oxide and channel fields in the *y*-direction of the channel when the MOSFET is in the linear regime (i.e., $V_{GS}>V_{DS}$, here V_{GS} = 15 V and V_{DS} = 8V).[119] (© IEEE 1991).

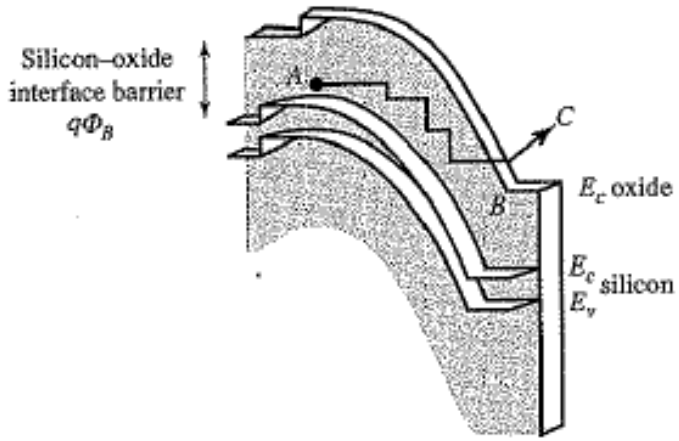
Initially, gate current increases with V_g due to increase in number of carriers. It peaks at about V_d=V_g; beyond this point $V_{gs}>V_{ds}$ the MOSFET is in linear region of operation and the electric field is rapidly reduced and few energetic electrons are produced.

Substrate and Gate Currents

$$I_G = I_D \int_0^L \exp\left(-\frac{\phi_B}{\mathscr{E}_y \lambda}\right) P(\mathscr{E}_{ox}) dy$$







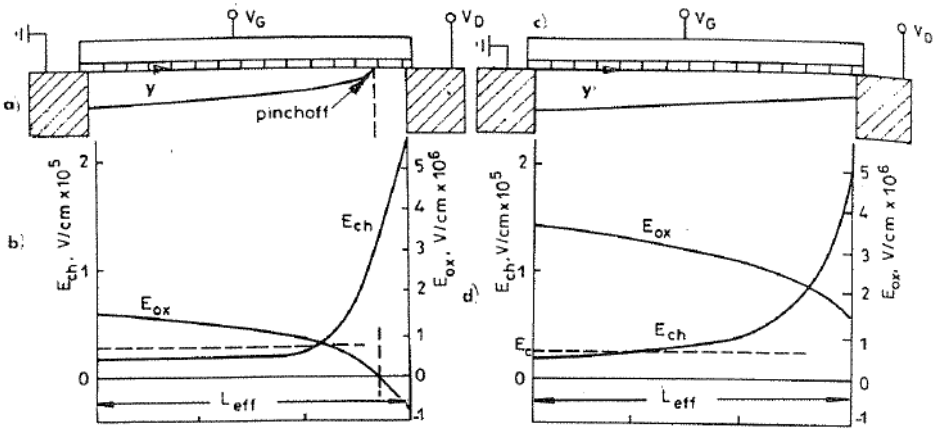


Fig. 7-8 (a) Cross section of MOS transistor operating in saturation. (b) The oxide and channel fields in the *y*-direction of the channel when the MOSFET is in saturation (i.e., $V_{GS}<V_{DS}$, here $V_{GS} = 6$V and $V_{DS} = 8$V). (c) Cross section of a MOS transistor operating in linear regime. (d) The oxide and channel fields in the *y*-direction of the channel when the MOSFET is in the linear regime (i.e., $V_{GS}>V_{DS}$, here $V_{GS} = 15$ V and $V_{DS} = 8$V).[119] (© IEEE 1991).

Modeling of the Gate Current

$$I_{gate} \propto I_d$$

$$I_{gate} \propto \exp\left(-\frac{\Phi_b}{\lambda_e E_{y\max}}\right) = \exp\left(-\frac{\Phi_b}{kT_e}\right)$$

$$I_{gate} = C_2(V_g, V_d) I_d \exp\left(-\frac{\Phi_b}{\lambda_e E_{y\max}}\right)$$

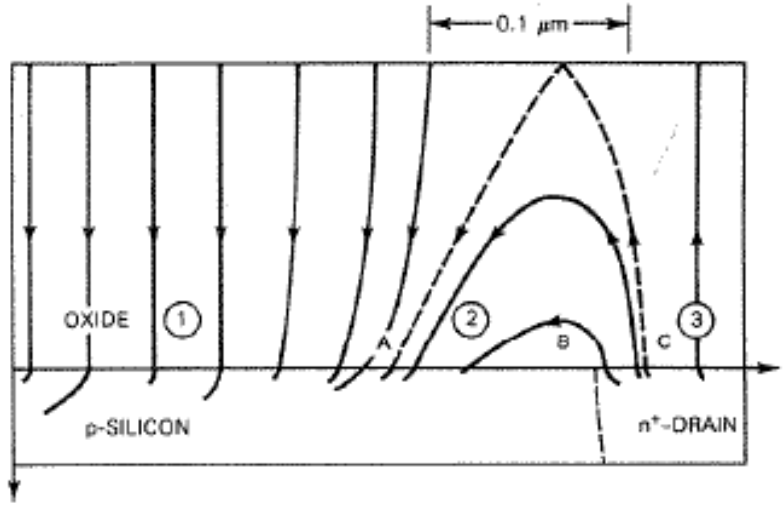


Figure 6.8 Two-dimensional electric field distribution near the drain of an *n*MOS. V_d = 8 V, V_g = 7 V, V_B = −2.5 V, L_{eff} = 1.3 μm and t_{ox} = 400 Å (Ref. 26, © 1984 IEEE).

Φ_b is the threshold energy Si-SiO_2 barrier, λ_e is the electron free mean path; so $\lambda_e E_{ymax}$ is the amount of energy gained by an electron before collision, and exp(- Φ_b / $\lambda_e E_{ymax}$) is the probability that an electron will overcome the Si/SiO2 barrier.

For V_g<V_d, C_2 decreases rapidly because the corresponding E_{ox} acts as a retarding field to prevent injected electrons from reaching the gate. For V_g>V_d $C_2 \approx 0.002$

Hot Carriers and Gate Current

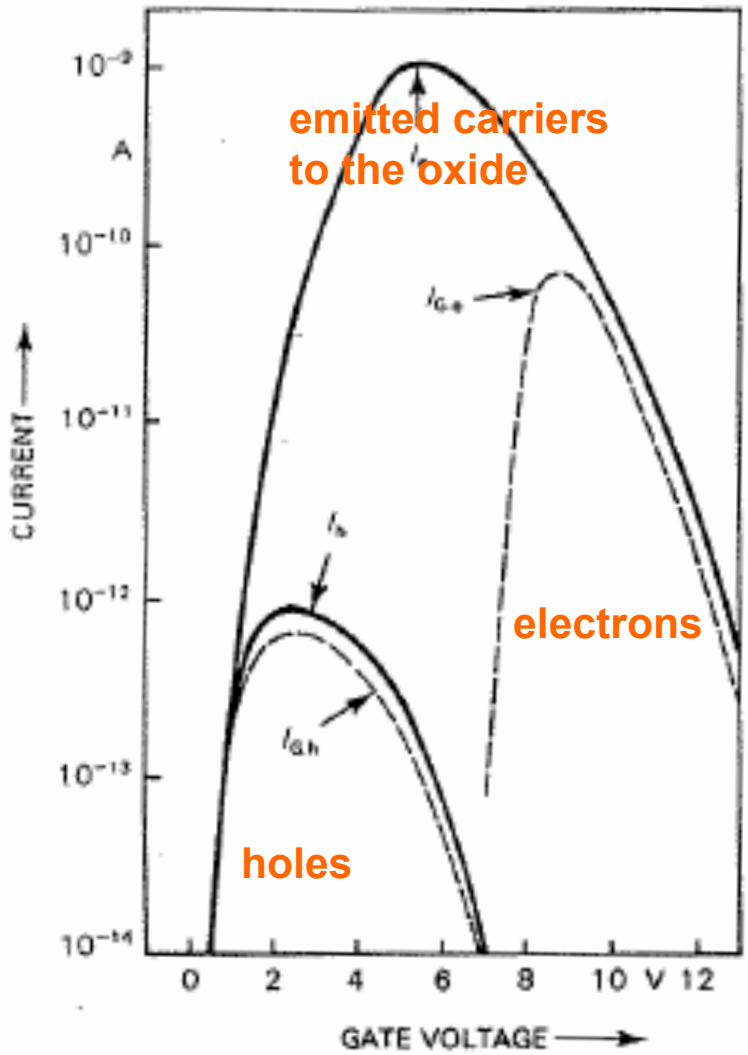


Figure 6.9 Calculated total emitted electron and hole current, I_e and I_h, as a function of gate voltage. $I_{G,e}$ is the electron gate current, and $I_{G,h}$ is the hole gate current. $V_d = 8$ V, $V_B = -2.5$ V, $W = 100$ μm, $L_{eff} = 1.8$ μm and $t_{ox} = 420$ Å (Ref. 26, © 1984 IEEE).

Only small fraction of the injected electrons reach gate. Especially at low gate bias, most injected electrons do not reach gate.

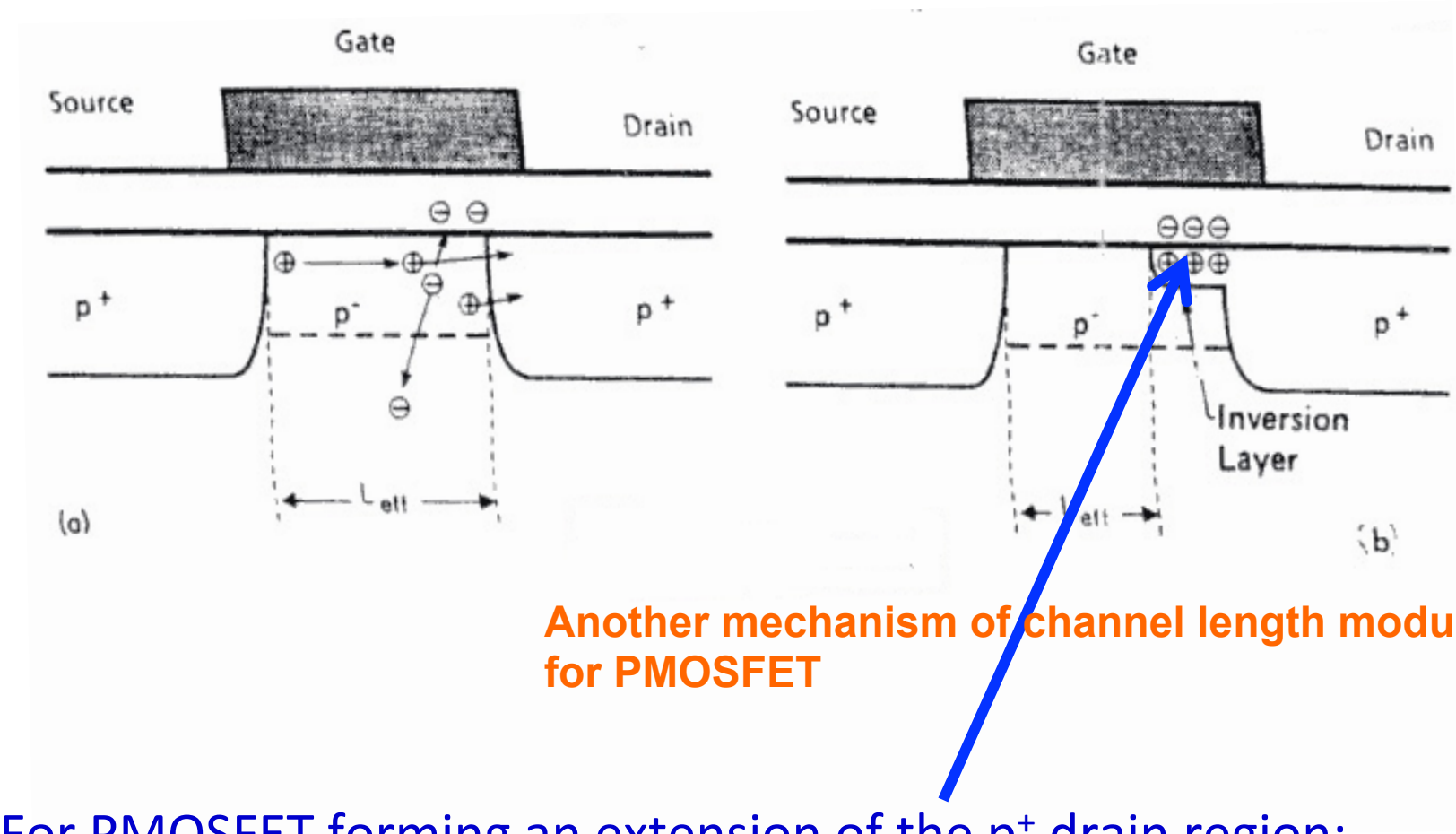
On the other hand, most hot holes, although at a much lower level, reach gate electrode when injecting into the oxide due to the attracting electric field in the oxide E_{ox} for $V_g<V_d$.

The injection efficiency for holes is lower than that of electrons because of the higher barrier (4.9 eV versus 3.1 eV for electrons).

The electron gate current is used for programming in non-volatile memory devices (floating gate devices).

Negative Charge Generation in PMOSFET

- Hot electron trapping results negative charge buildup in the oxide near the drain of a PMOSFET.



Another mechanism of channel length modulation for PMOSFET

For PMOSFET forming an extension of the p^+ drain region; resulting in channel length shortening

P-MOSFET Degradation

- Channel length Degradation
- Transconductance Degradation
- Threshold Shift degradation
- Shortening of L_{eff}

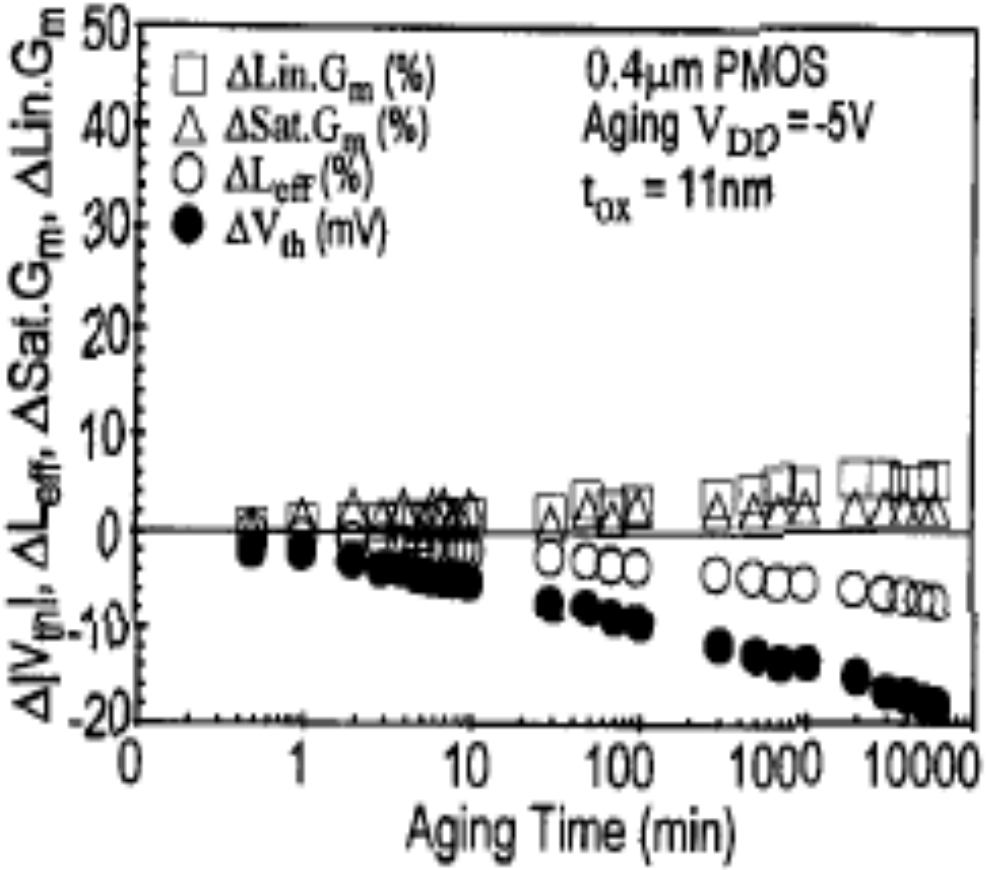


Fig.2 Hot carrier degradation of a 0.4μm PMOS. Both $|V_{th}|$ and L_{eff} decrease with the aging time. Saturation and linear G_m increase with time.

N-MOS Degradation

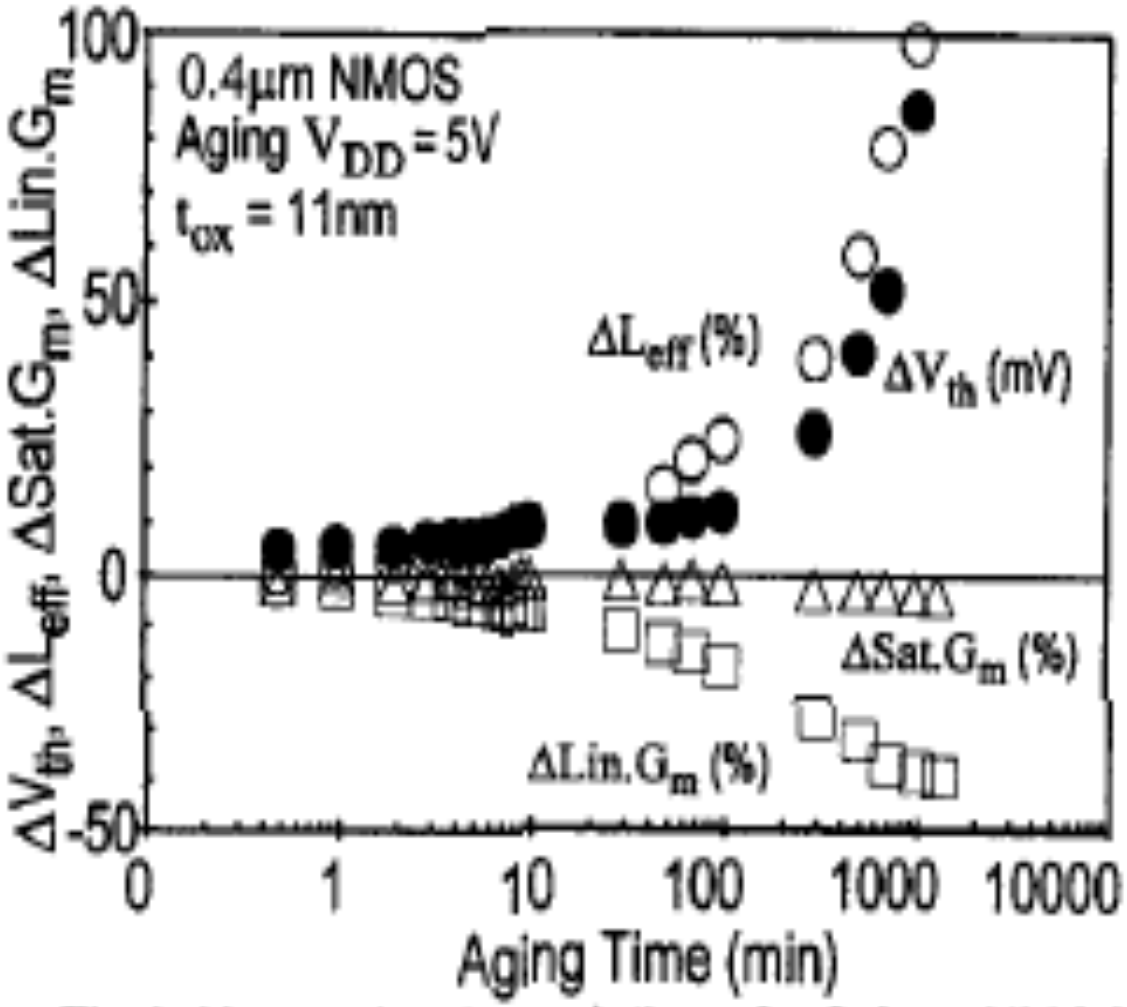


Fig.1 Hot carrier degradation of a 0.4μm NMOS. Both V_{th} and L_{eff} increase with the aging time. Saturation and linear G_m decrease with time.

- **Trapped electrons in the oxides result in the increase of V_T & L_{eff}**
- **… Opposite to PMOS**

Suppression of Hot Carrier Effect
(Device structure aspect)

- **Reduction of Hot-Carrier Generation**

❖ Reduce the high drain field

❖ Separate main current path away from maximum field .

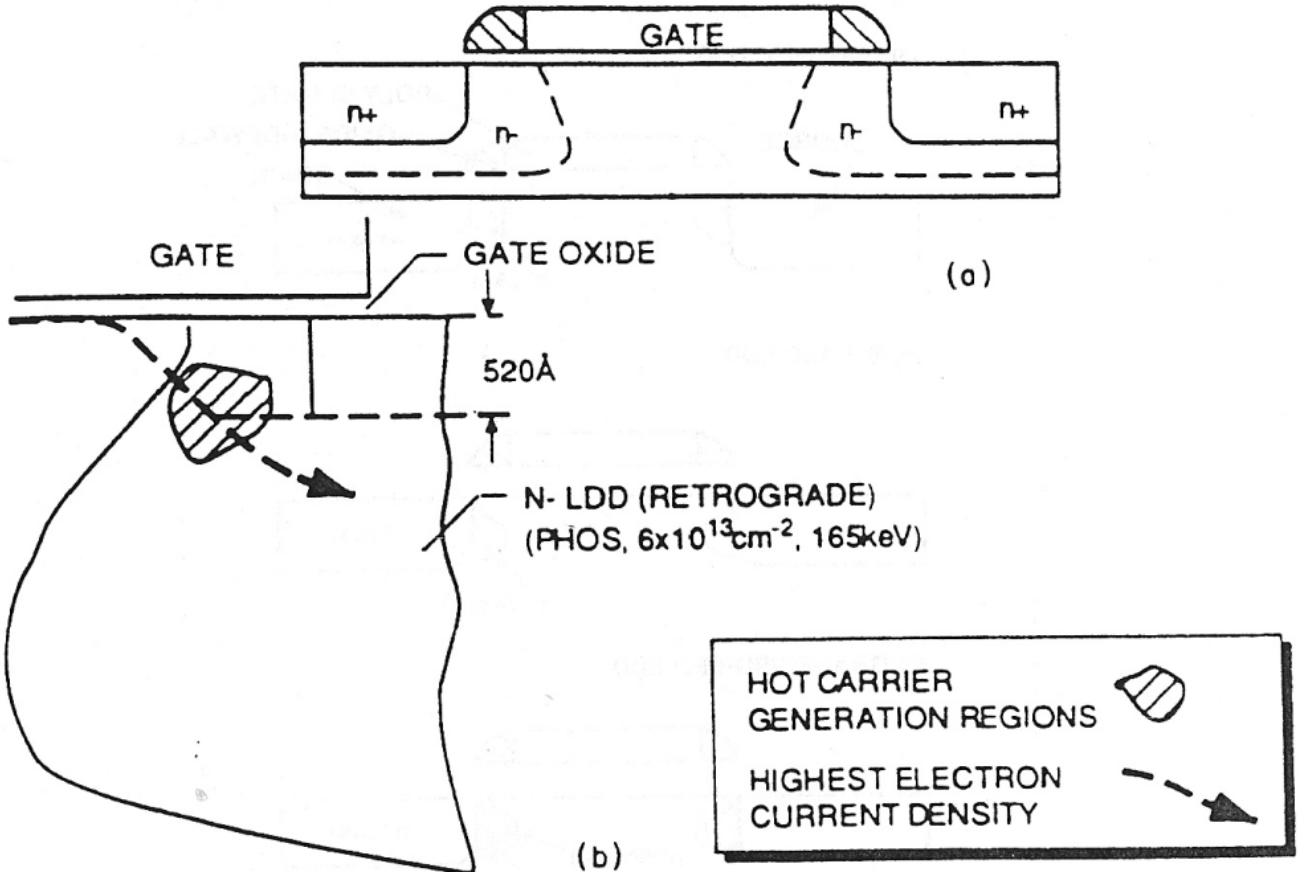
- **Reduction of Hot-Carrier Injection**

❖ Push impact ionization region deep into silicon.

❖ Position the injection point outside the gate

Suppression of Hot Carrier Effect

Separate main current path away from maximum field!



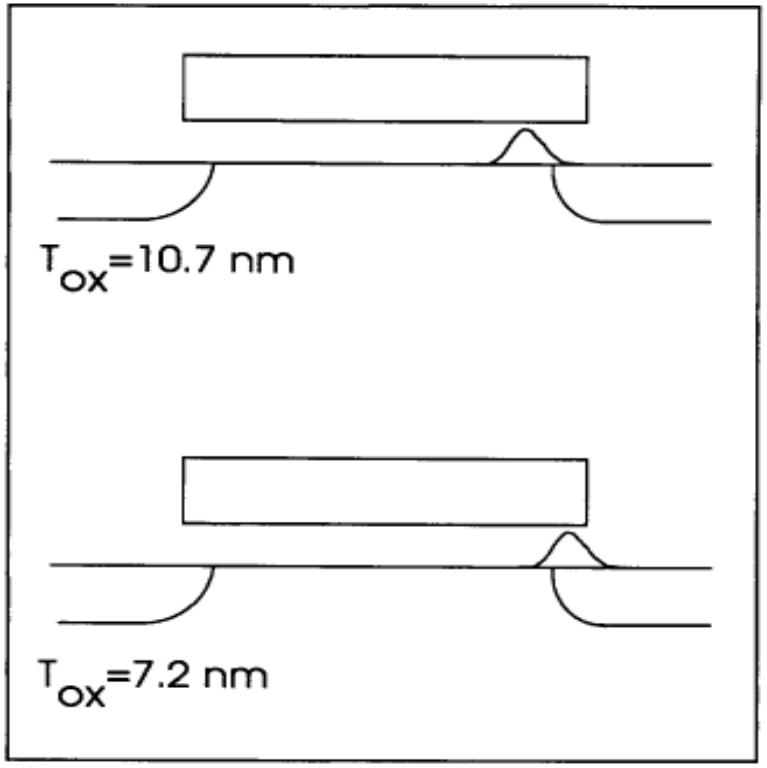
Debate whether I_{sub} is a good indicator for degradation for different technologies.

Hot Carrier Mitigation Technique

- Gate Oxide thickness reduction (reduction of lateral E_y)
- Lightly Doped MOSFET structure (LDD)
- Double Diffused MOSFET structure
- Deuterium Post –Metal Annealing

Gate Oxide thickness reduction (reduction of lateral field and shift of the injection point)

- As the oxide thickness is reduced , the point of peak of electron injection moves further into the drain region , the damage region over the channel is reduced



High Electrical Peaks and LDD Drain

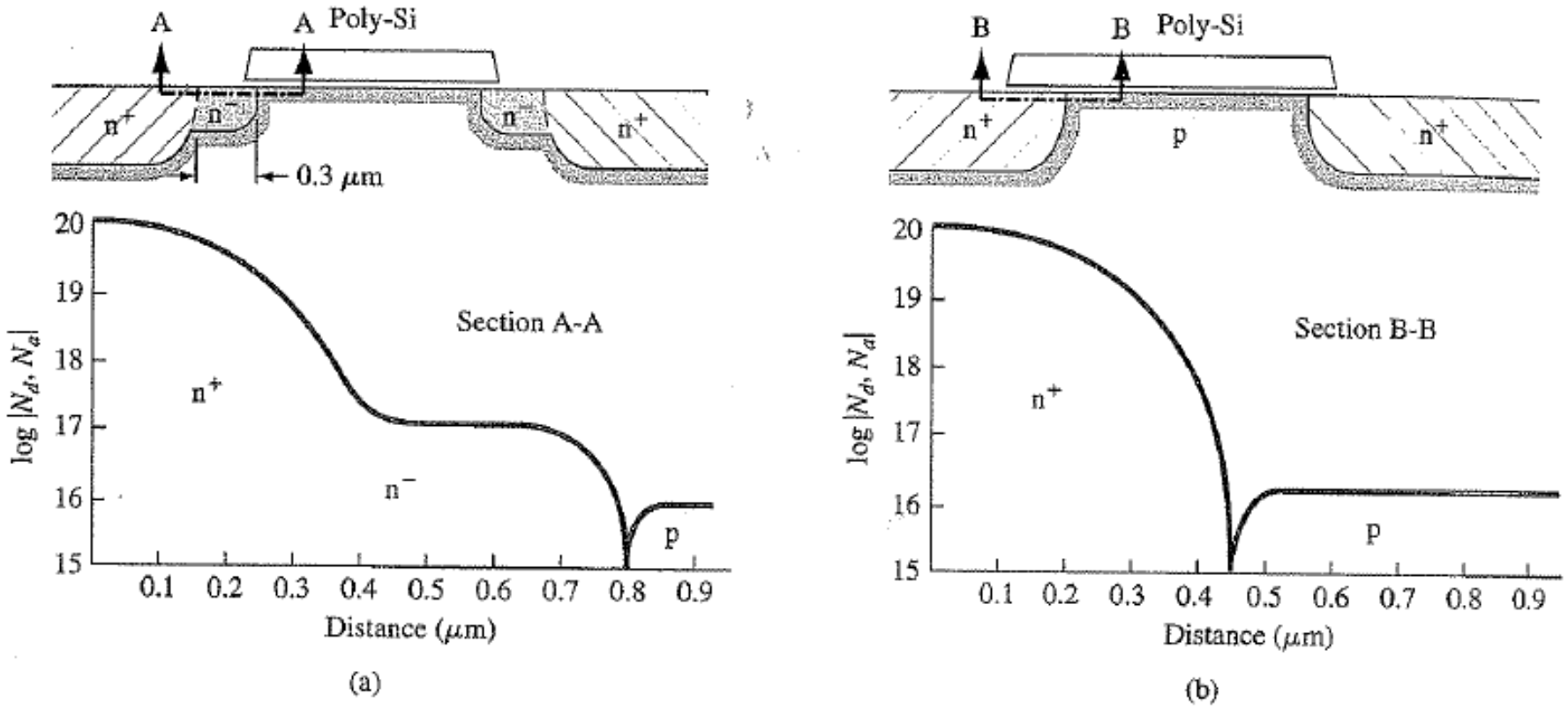
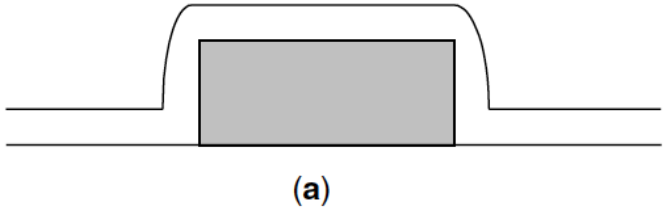


Figure 12.27 | (a) The lightly doped drain (LDD) structure. (b) Conventional structure.

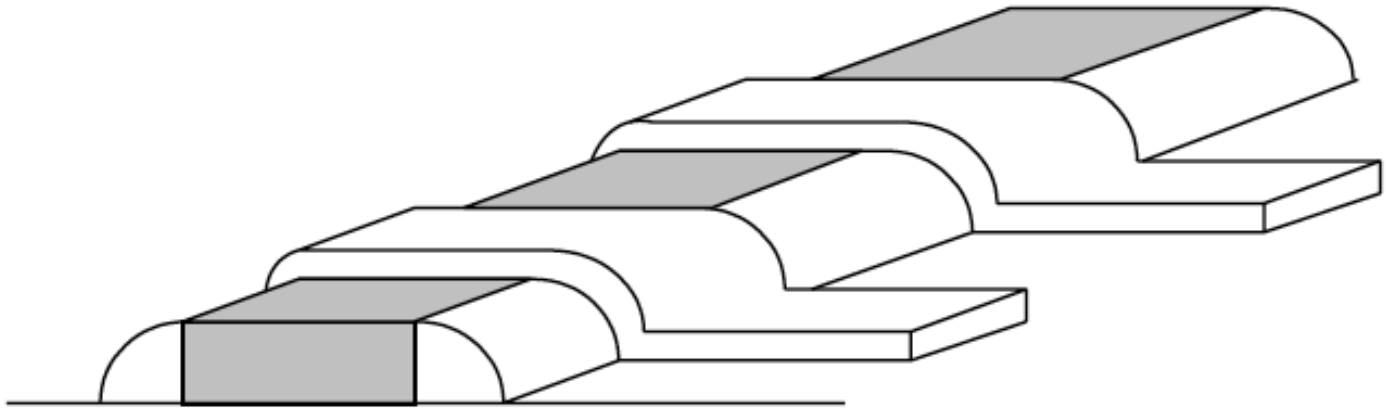
LDD drain structure **HDD drain structure**

Spacer Formation to Offset the LDD Drain



Conformal deposition over a step

Anisotropic etching for complete removal of film on horizontal planes



Use of anisotropic etching to creates sublithographic structures: spacer formation

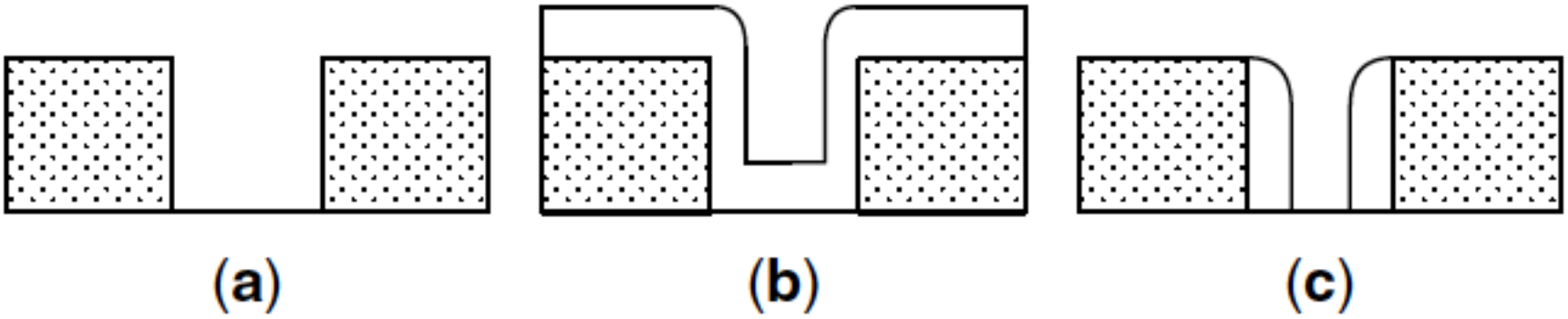
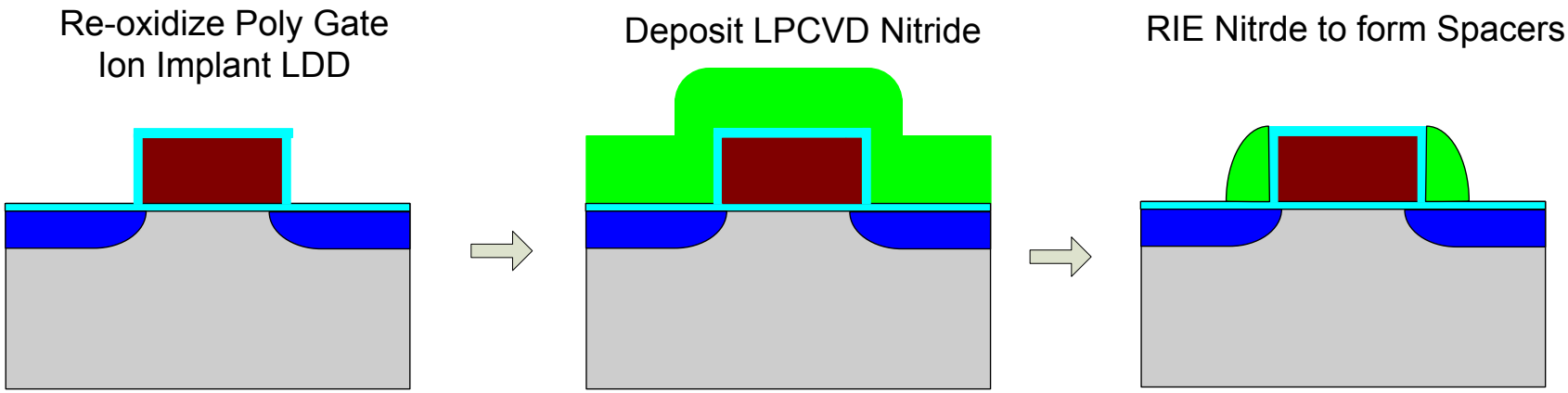


Figure 20.6 Inside spacer (**a**) initial structure; (**b**) after conformal deposition and (**c**) after anisotropic etching

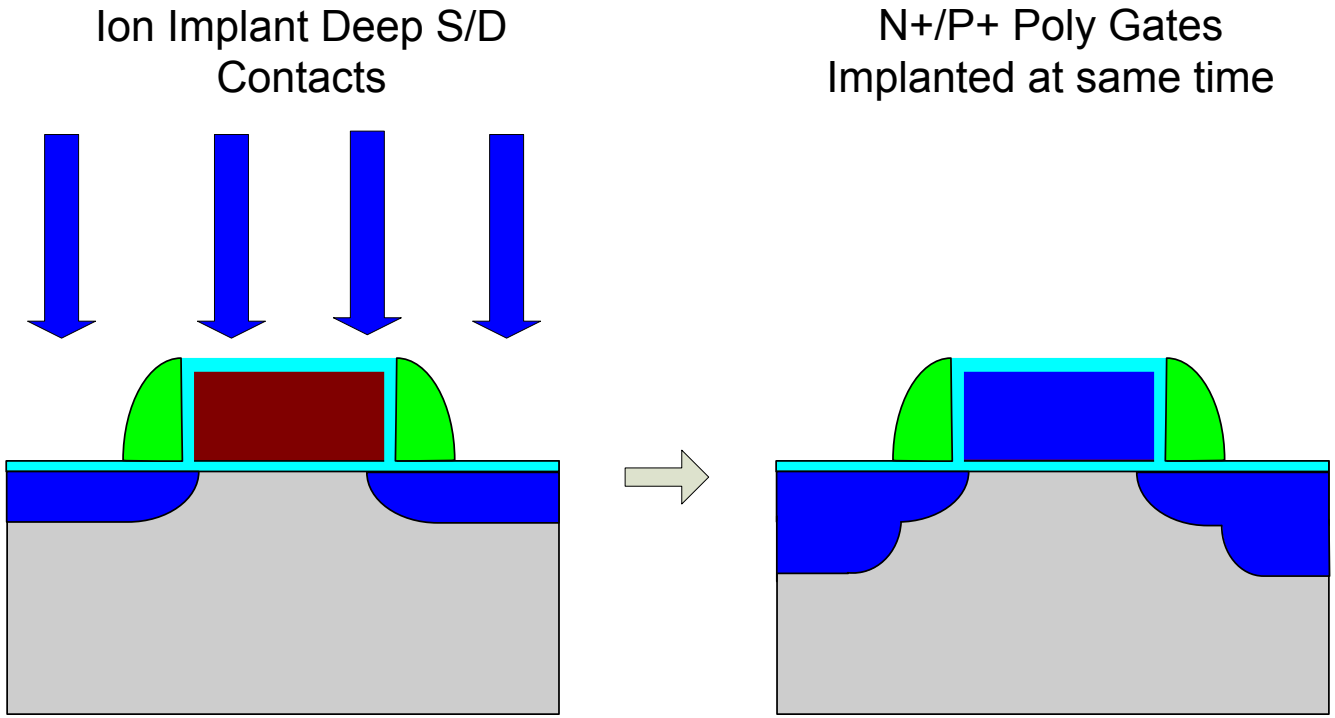
Use of anisotropic etching to creates sublithographic structures: spacer formation

- Sidewall spacers are formed after the LDD implants to create an offset region where a deeper source/drain contact region can be implanted.



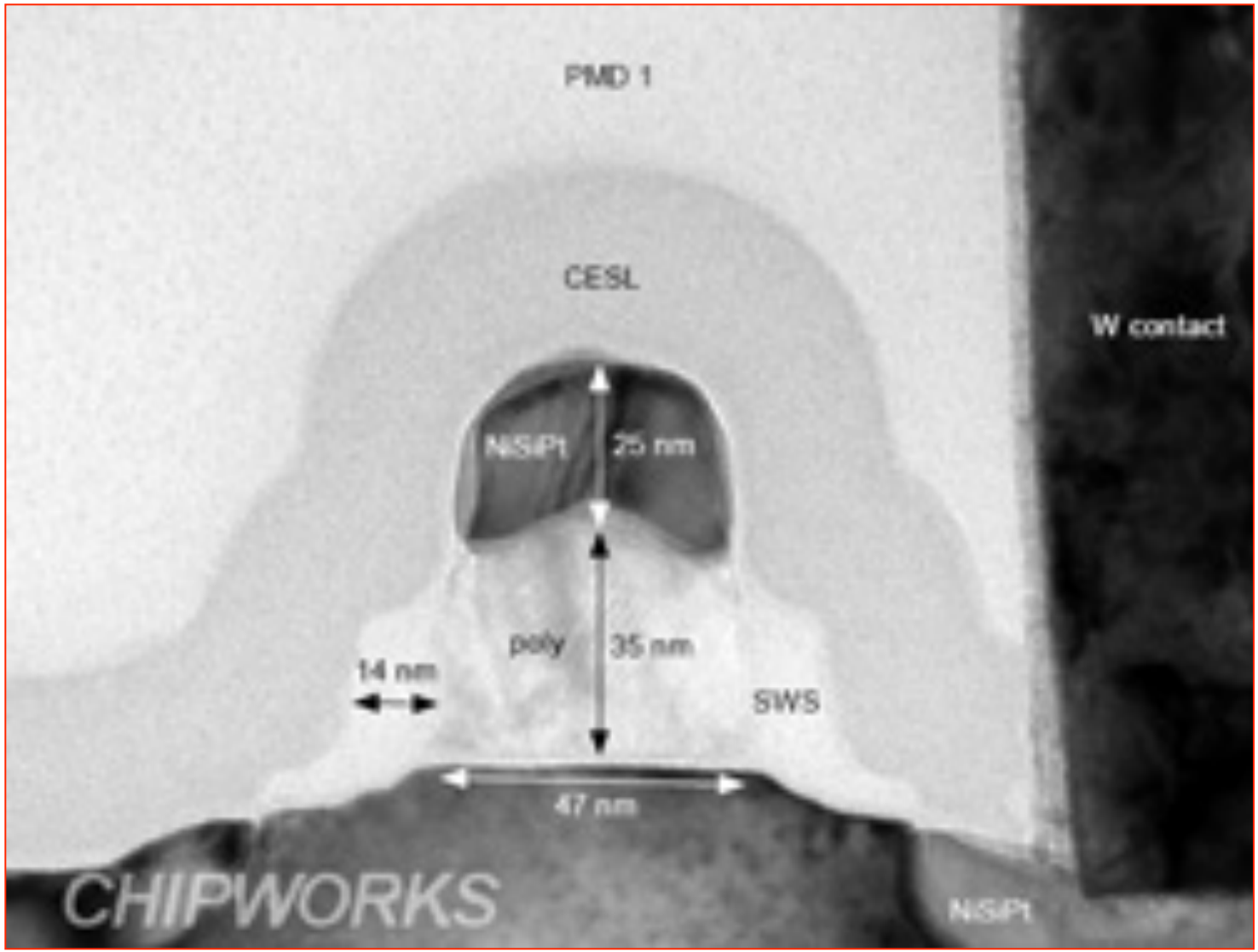
Use of anisotropic etching to creates sublithographic structures: spacer formation

Source/Drain contacts implanted after sidewall spacer formation and are self-aligned to the gate

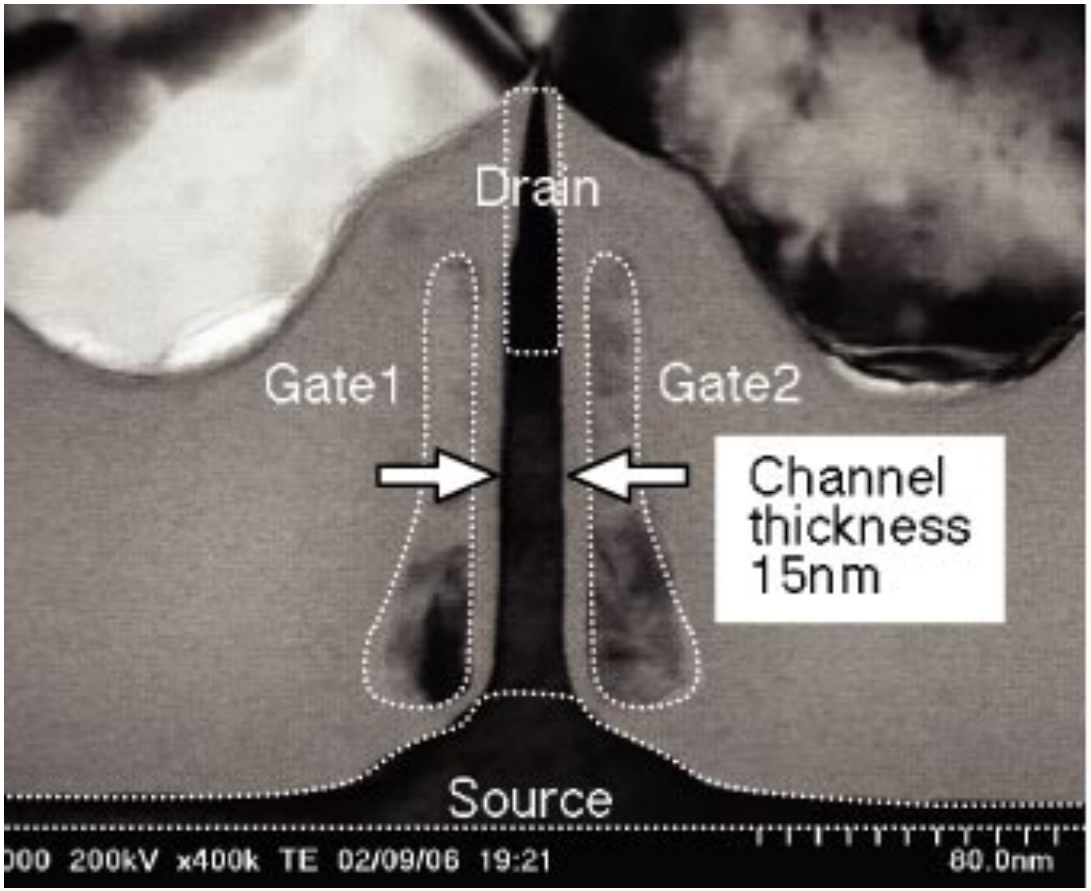


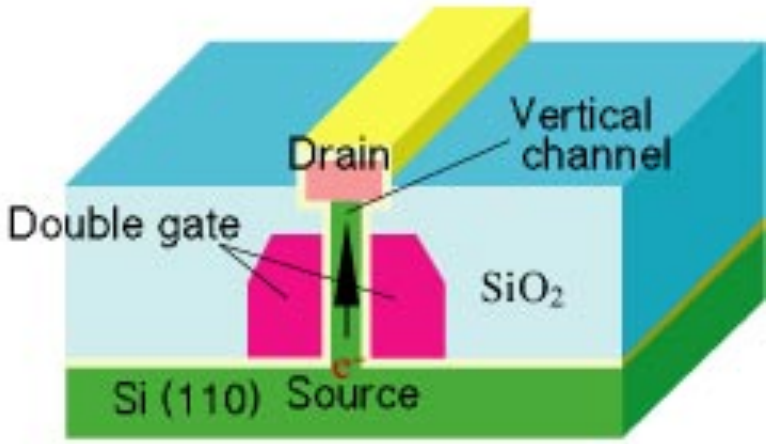
Source/Drain Contact and Gate Doping

Use of anisotropic etching to creates sublithographic structures: spacer formation

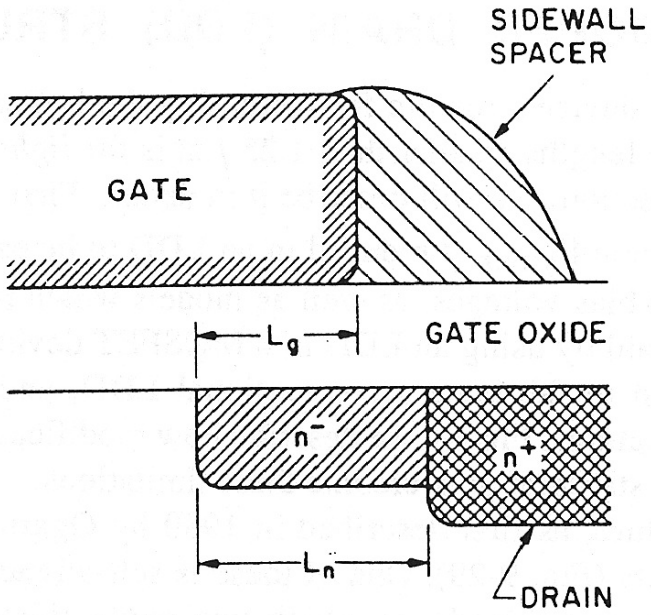


Use of anisotropic etching to creates sublithographic structures: spacer formation





High Electrical Peaks and LDD Drain



The price for LDD is a shorter channel length at the same gate length and increased possibility of punchthrough condition.

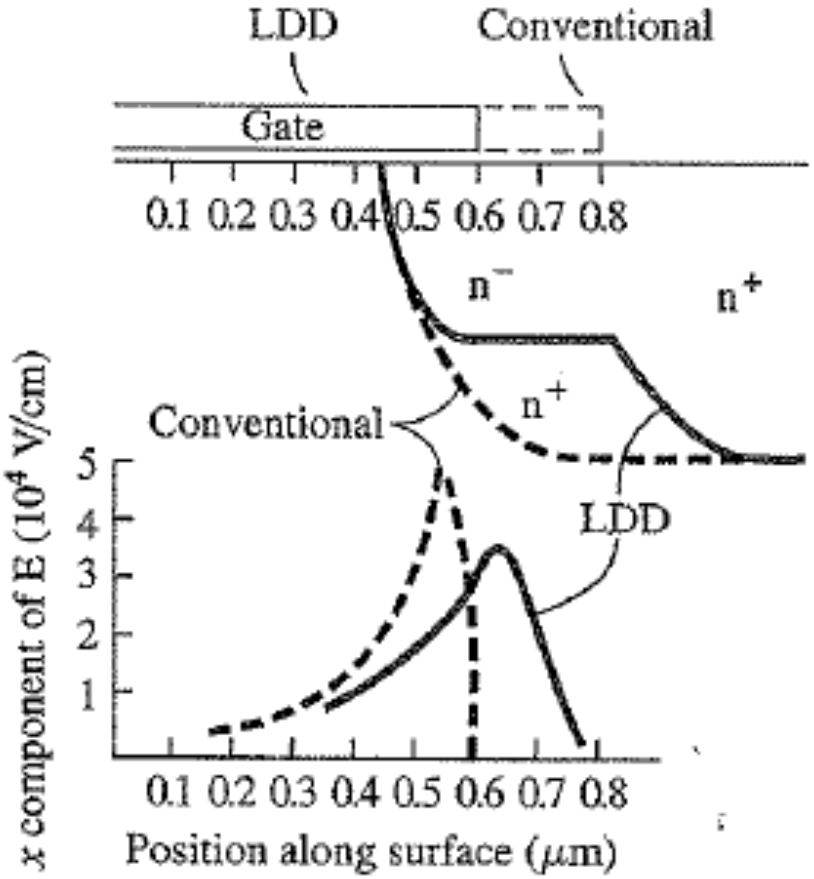


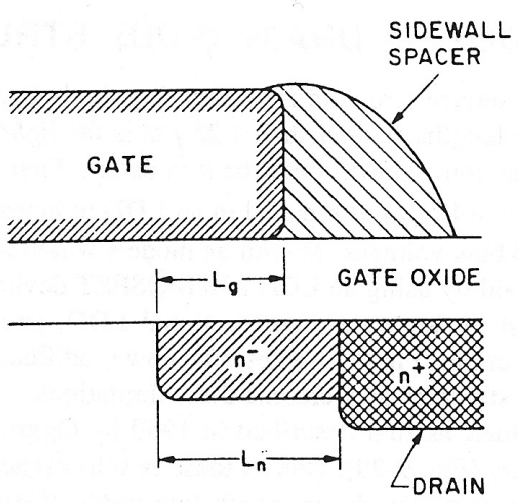
Figure 12.28 | Magnitude of the electric field at the Si–SiO_2 interface as a function of distance; $V_{DS} = 10$ V, $V_{SB} = 2$ V, $V_{GS} = V_T$.

High Electrical Peaks and LDD Drain

Modeling E_{ymax} in LDD MOSFETs

1. Simple model for estimating E_{ymax} in LDD MOSFETs

$$E_{ymax}\ (LDD) = (V_{DS}-V_{DSsat})/(0.22 t_{ox}^{1/3} r_j^{1/3} + L_{n-})$$



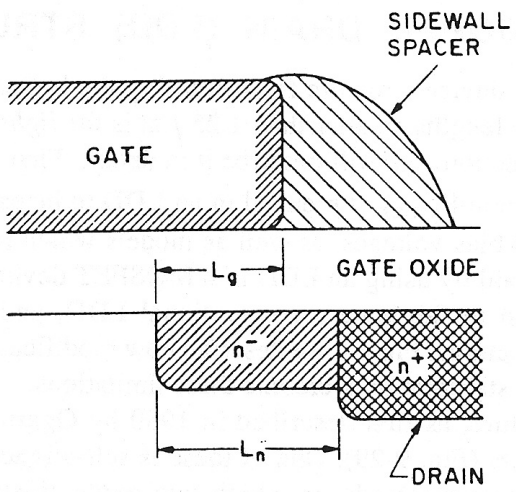
Tradeoff: With LDD we reduce electric fields and alleviate the hot electron problem, but we incur a larger parasitic source/drain resistances which decrease the drain current.

$R_{n-} = L_{n-}/(Zq\mu_n N_D rj)$ Parasitic resistance

Z: device width

μ_n: electron mobility in the n^- region

High Electrical Peaks and LDD Drain



Pros:

LDD → E_{ymax} ↓ → Hot-carrier↓
→ I_{sub} ↓ → hot-carrier reliability ↑

Cons:

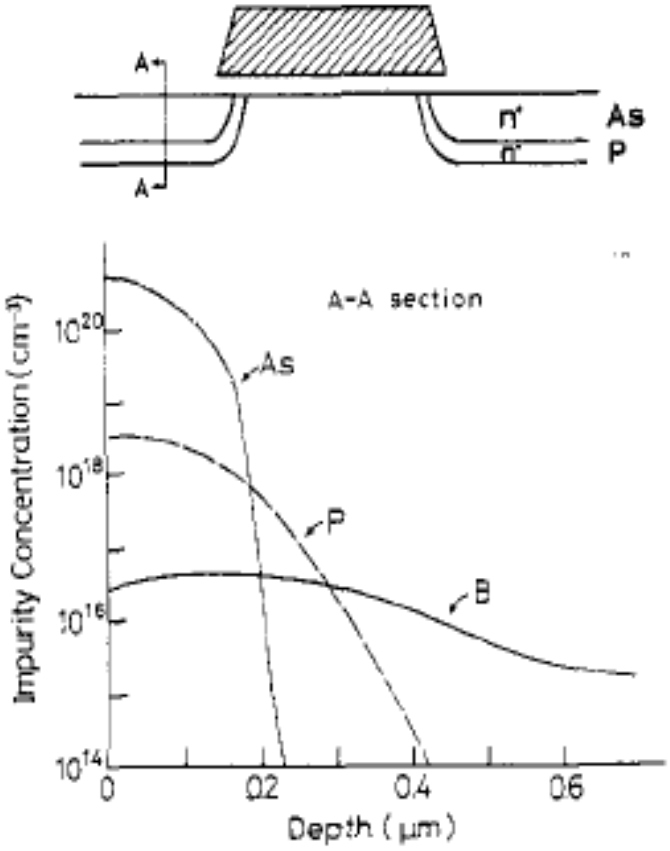
- LDD → I_d ↓
- Length scaling more difficult

- R_{n-} causes a 10~20% loss in both I_D and g_m compared to non-LDD devices.
- The drain R_{n-} and source R_{n-} act to decrease I_D in the linear region, while the source R_{n-} acts to decrease I_{Dsat}

- doping concentration of the n^- region ↑, L_{n-} length ↓ → R_{n-} ↓
- L_{n-} : neither too long, nor too short
- doping concentration of the n^- region : trade-off between performance and hot-carrier degradation

Double diffused MOSFET structure to mitigate hot carrier effects

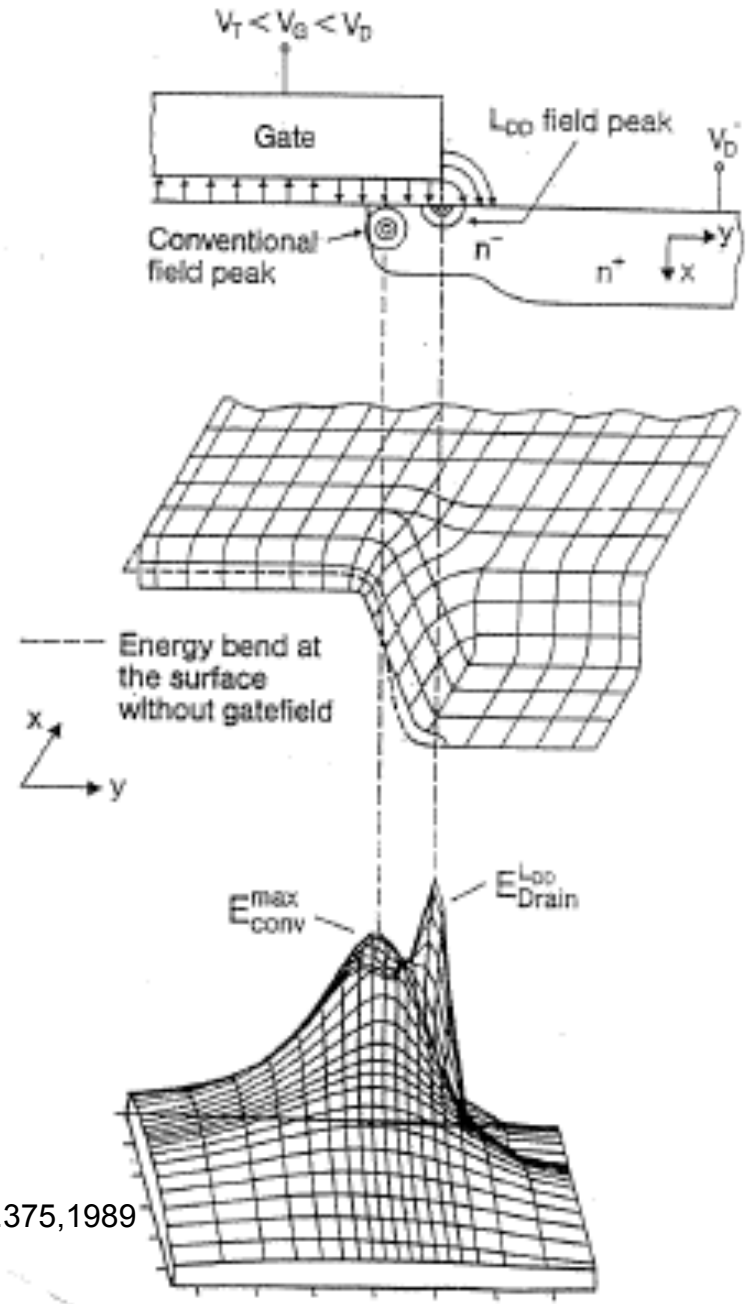
- Deeper n- phosphorous profile than N^+ As profile .
- The path of maximum current away from the position of the maximum field to reduce the impact ionization
- The disadvantage of double-diffused S/D regions over LDD regions is that one incurs a deeper junction depth running counter to scaling efforts



High electrical peaks and LDD Drain; secondary lateral field peaks

Origin of the LDD field peak:

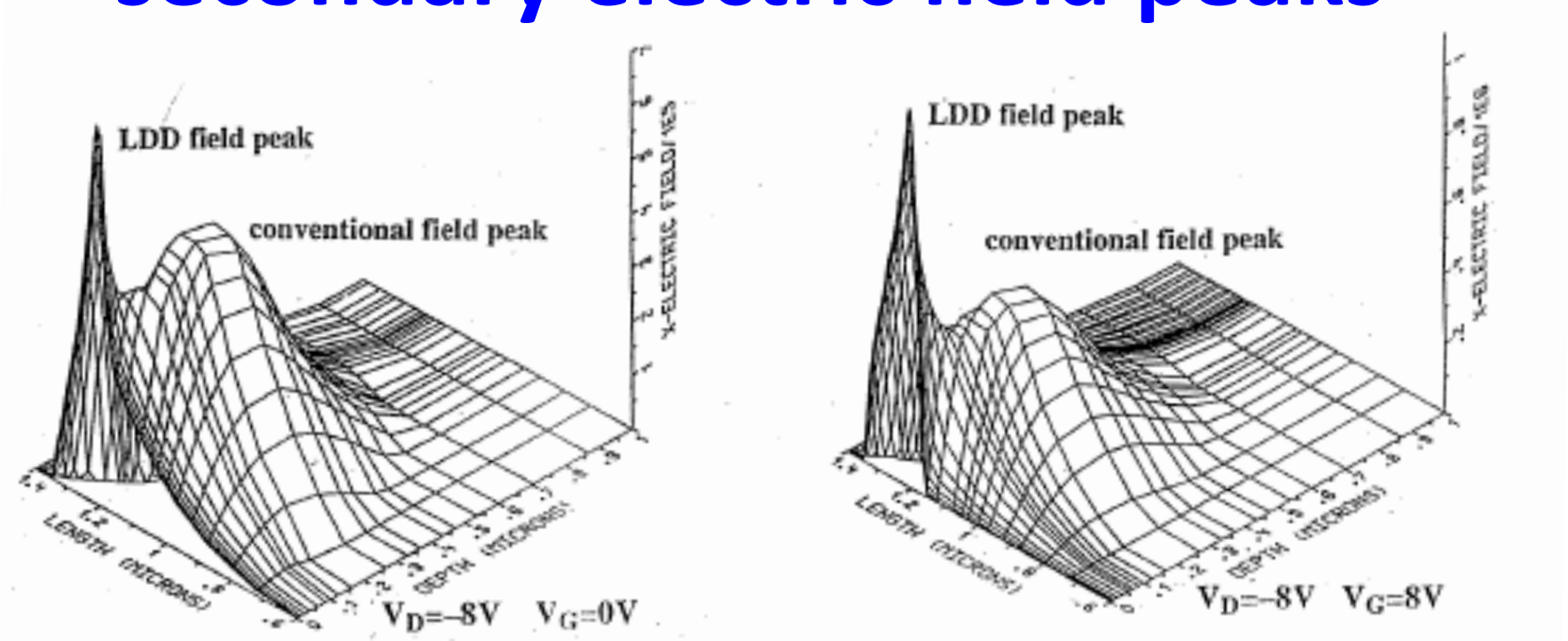
Lateral variation of the vertical electric field (gate oxide field) creates lateral field peak.



M.Orlowski et al, "Model for the Electric Fields in LDD MOSFET's - Part I: Field Peaks on the Source Side", IEEE TRANS.EL.. DEV. vol. 36(2) p.375,1989

M.Orlowski et al, "Model for the Electric Fields in LDD MOSFET's - Part II: Field Peaks on the Drain Side", IEEE TRANS.EL.. DEV. Vol. 36(2) p.382,1989

High Electrical Peaks and LDD Drain; secondary electric field peaks



Avalanche in subthreshold regime

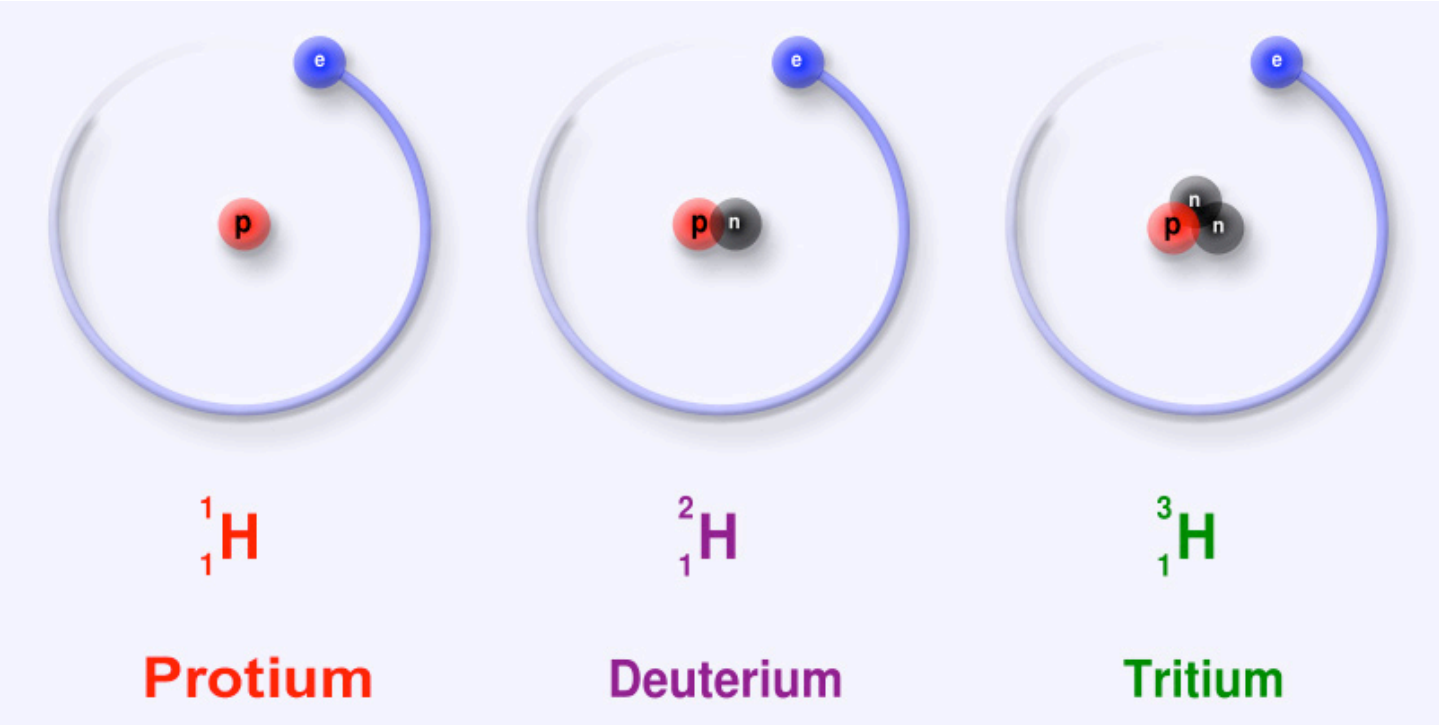
LDD: 6.5 MV/cm Conv.: 5.6 MV/cm **LDD: 12 MV/cm Conv.: 5.7 MV/cm**

⇒The avalanche in the deep off–regime is driven by the LDD field peak !!!

M.Orlowski et al, "Model for the Electric Fields in LDD MOSFET's - Part I: Field Peaks on the Source Side", IEEE TRANS.EL.. DEV. vol. 36(2) p.375 and p. 382,1989

Deuterium

Isotope Example: Hydrogen



H

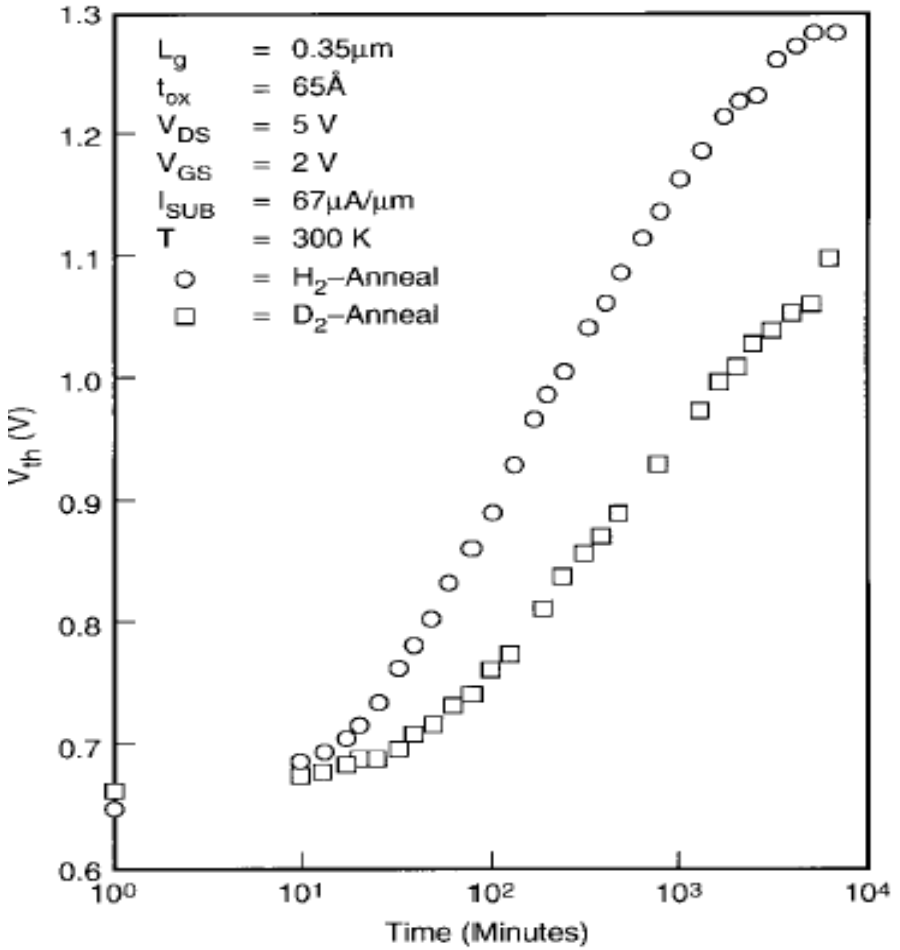
D (or heavy nitrogen) D_2O heavy water

Deuterium Post –Metal Annealing

Replace Si-H by Si-D bond

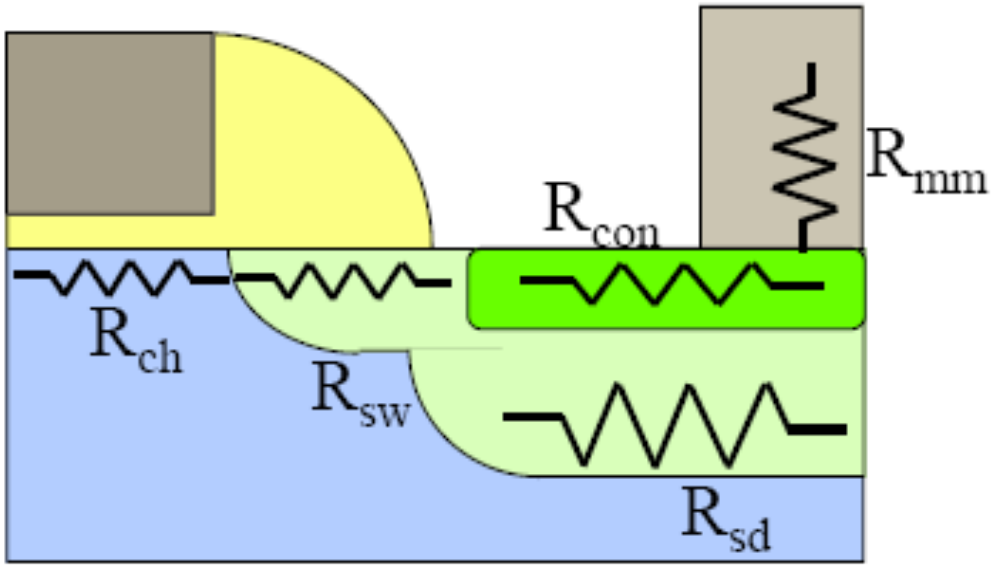
- Low temperature post metallization anneals in hydrogen ambient are critical in reducing Si-SiO_2 interface trap .
- Under Hot Carrier stress , bond to deuterium (^2H or D) are more difficult to break than bonds to protons

Evolution of V_{th} as function of stress time



Series Resistance in MOSFETs

Problems in Shallow Junction



- Many components of the transistor resistance
- Lot of effort spent to optimize each component

Accumulation/**Spreading Resistance**

4-17-2014

The spreading of current lines causes additional voltage drop

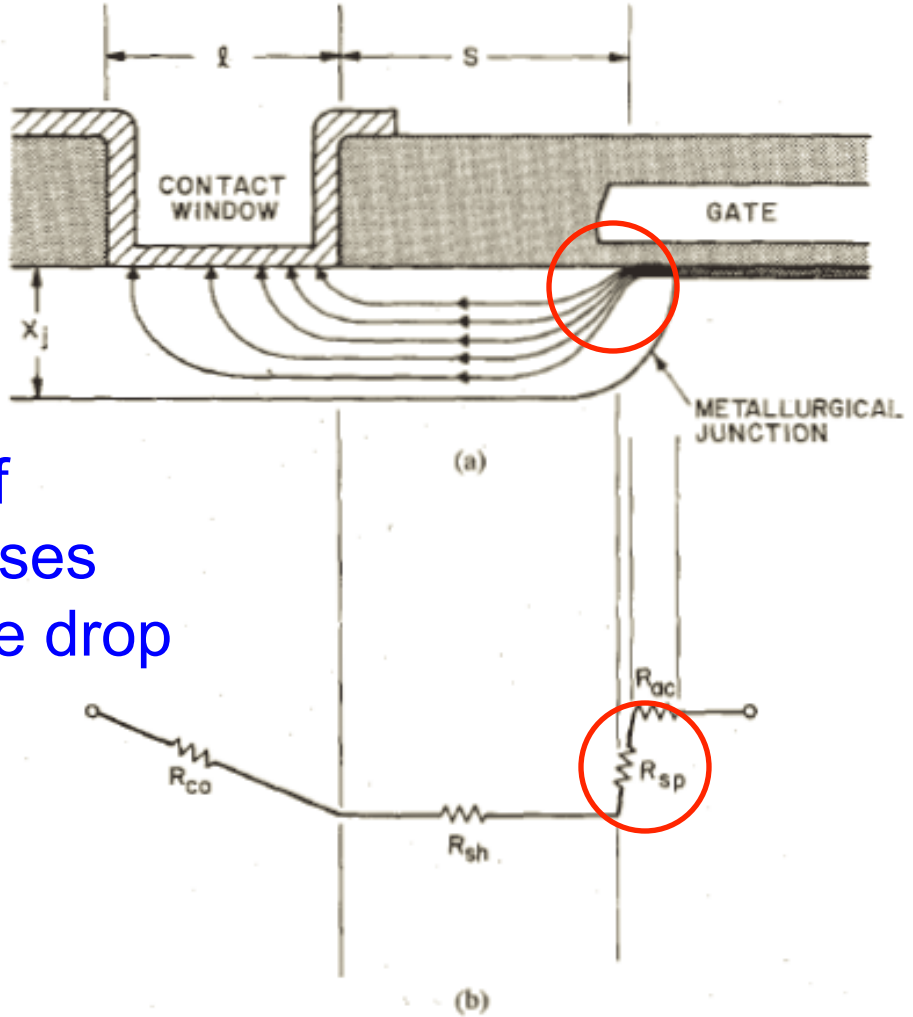
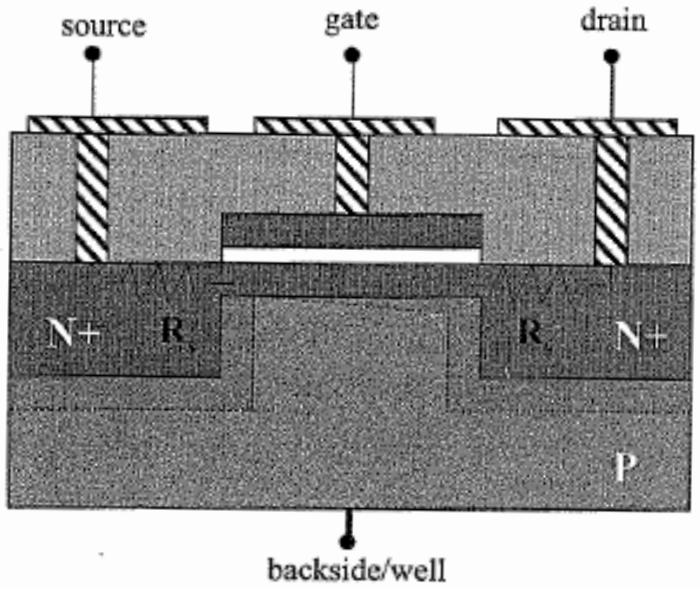
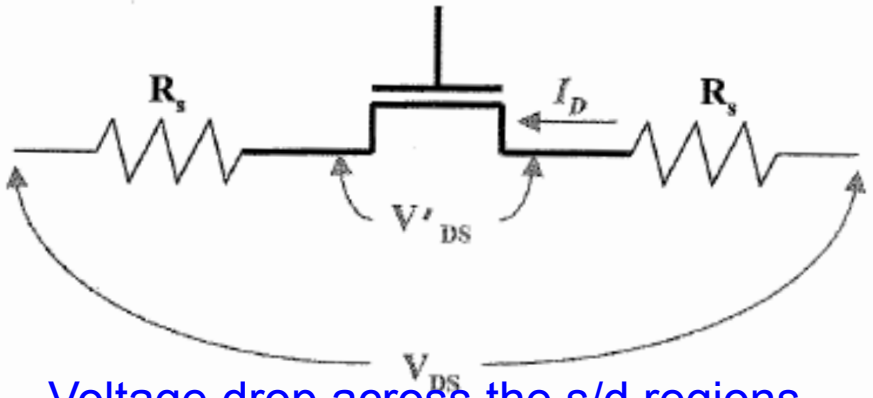


Fig. 1. Schematic diagrams for (a) current flow pattern in the source/drain region and (b) the associated resistance components.

Impact of Parasitic Resistance on MOSFET IV Characteristics





Voltage drop across the s/d regions reduces the voltage across the channel

$$V'_{DS} = V_{DS} - 2I_D R_s$$

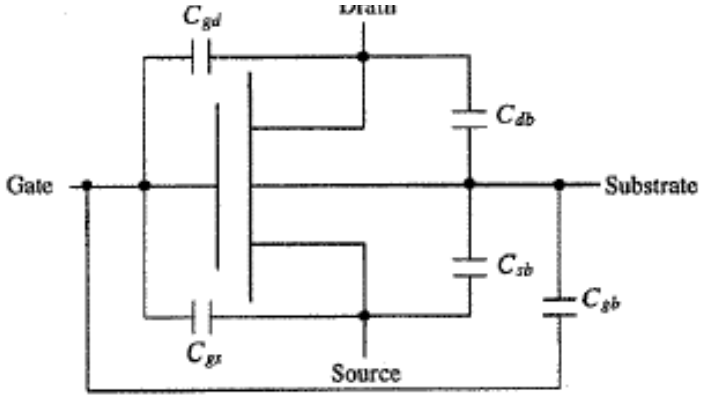
Thus the effective drain voltage is not The applied voltage V_{DS} but V'_{DS}.

$$I_D = \frac{Z\mu_{eff}C'_{OX}}{L}(V_{GS} - V_T)V'_{DS}$$

Resulting in:

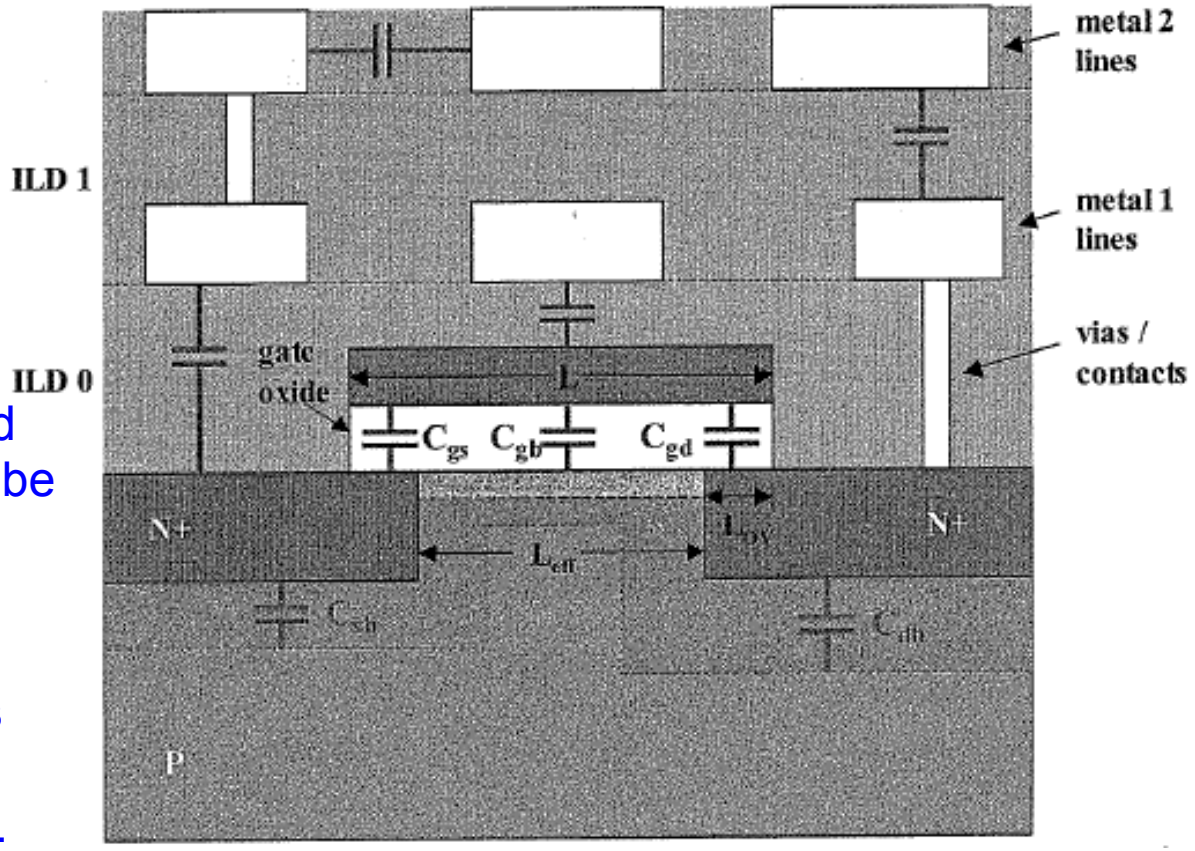
$$I_D = \frac{(Z/L)\mu_{eff}C'_{OX}}{1+\alpha_R(V_{GS}-V_T)}(V_{GS}-V_T)V_{DS} \qquad \text{where:} \quad \alpha_R = \frac{2\mu_{eff}C'_{OX}R_sZ}{L}$$

MOSFET Parasitic Capacitances

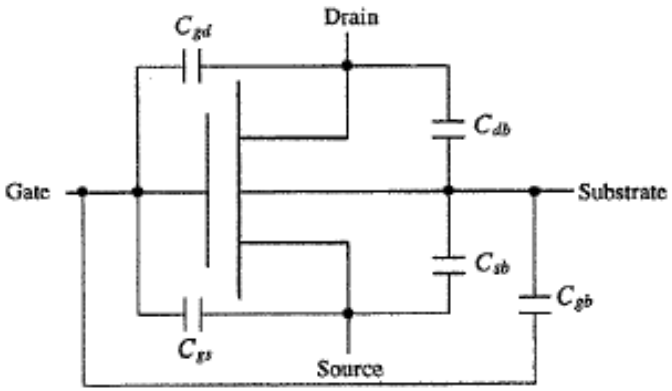


Capacitances are important for the switching speed of a MOSFET.

Every time V_G or $_{VD}$ are changed MOSFET capacitances have to be charged or discharged.
Capacitances are not instantaneously charged and discharged; there will be always some time delay.
This delay should be minimized.



MOSFET Parasitic Capacitances: affect switching speed differently in different regimes



	Off (subthreshold)	Linear (triode)	Saturation
C_{gs}	C_{ov}	$\frac{1}{2}C_{ox}+C_{ov}$	$\frac{2}{3}C_{ox}+C_{ov}$
C_{gd}	C_{ov}	$\frac{1}{2}C_{ox}+C_{ov}$	C_{ov}
C_{gb}	C_{ox}	0	0
C_{sb}	C_j	C_j	C_j
C_{db}	C_j	C_j	C_j

MOS Capacitor:
- Inversion layer is electrically isolated from the outside world
- Inversion charge comes from R-G of minority carriers
- Capacitance depends on frequency

MOSFET:
- Inversion layer (channel) is electrically connected to source/drain
- Source is an ample supply of electrons at any practical frequency
- Charge fluctuates on either side of gate oxide (like parallel-plate)
- MOSFET gate capacitance is $\varepsilon_{ox}A/t_{ox}$ at any practical frequency

?

what about the MOS capacitor C-V frequency dependence?

where:

$$C_{ov} = \frac{\varepsilon_{ox}}{t_{ox}} ZL_{ov}$$ overlap (Miller) capacitance

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} ZL_{eff}$$ gate capacitance

$$C_j = \frac{\varepsilon_s A_j}{W}$$ PN junction capacitance

Scaling - Most Simple Model: Constant Field Scaling

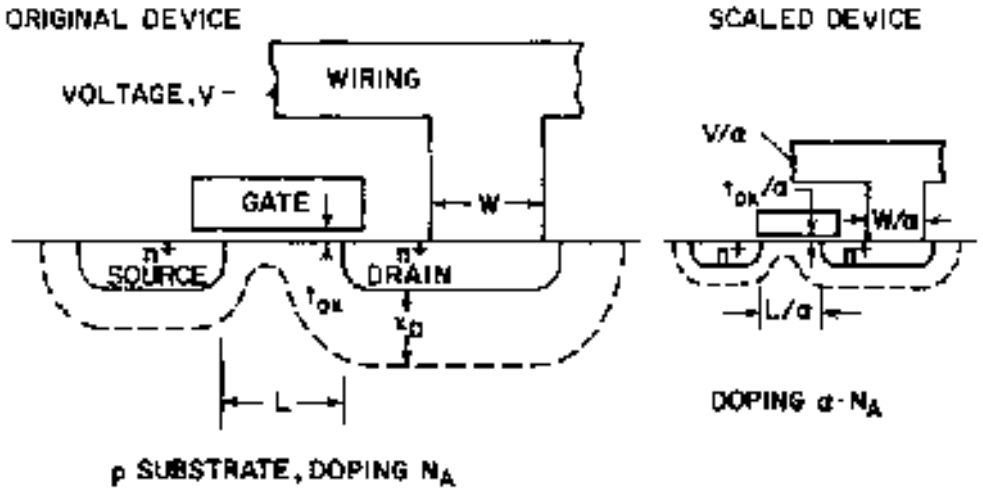


Fig. 1. Principles of constant-electric-field scaling for MOS transistors and integrated circuits.

$\mathcal{E} = V_{DD}/L$

after scaling becomes

$\mathcal{E} = (V_{DD}/\alpha)/(L/\alpha)$

…where $\alpha>1$

Table 1 Generalized Scaling Relationships

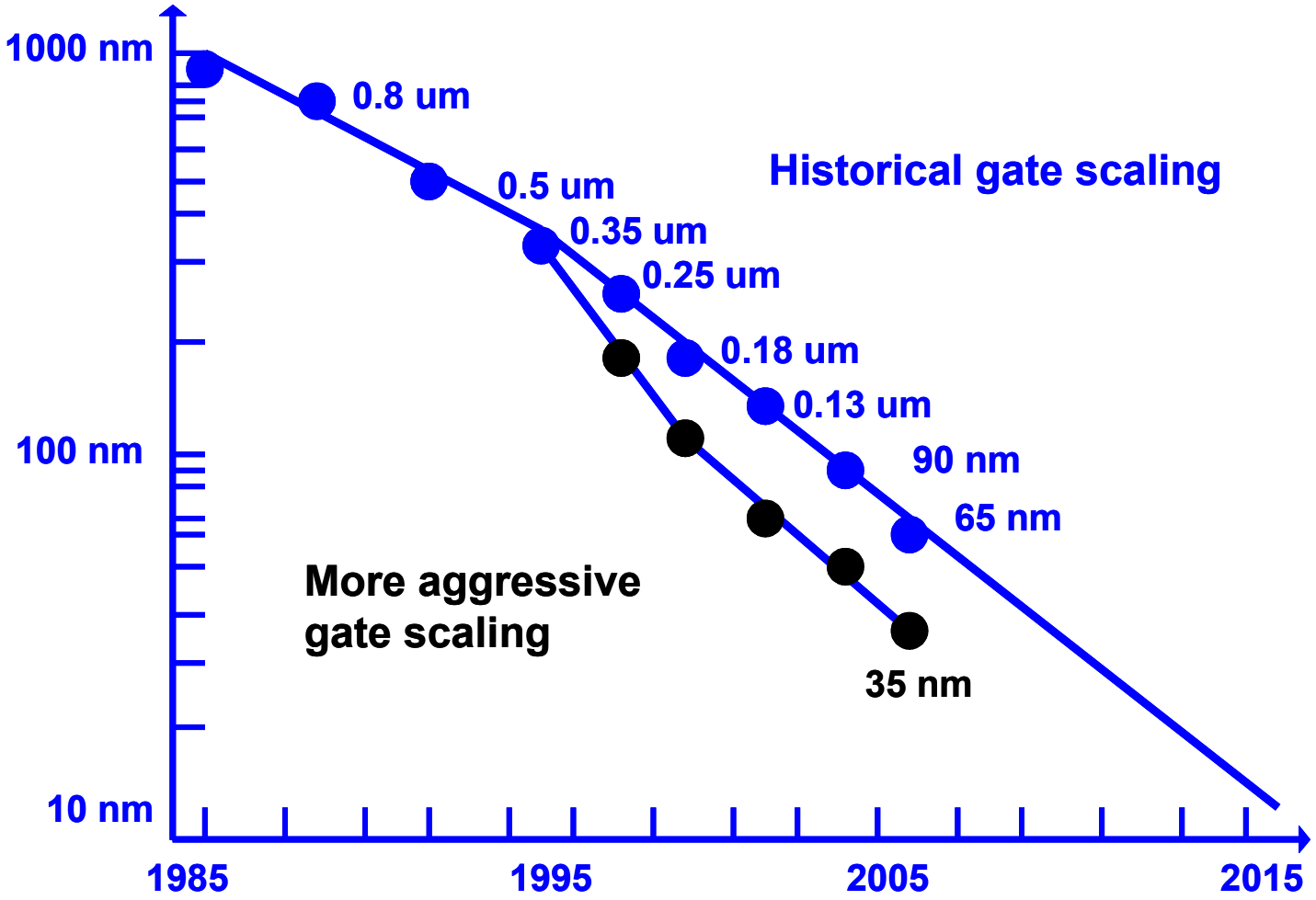
Physical Parameters	Constant-Electric Field Scaling Factor
Linear Dimensions	$1/\alpha$
Electric Field Intensity	1
Voltage (Potential)	$1/\alpha$
Impurity Concentration	α

CMOS Device Scaling decoupling of dimension and potential scaling

Parameters	Variables	Scaling Factor
Dimensions	W, L, x_{ox}, x_j	$1/\lambda$
Potentials	V_{ds}, V_{gs}	$1/k$
Doping Concentration	N	λ^2/k
Electric Field	E	λ/k
Current	I_{ds}	λ/k^2
Gate Delay	T	k/λ^2

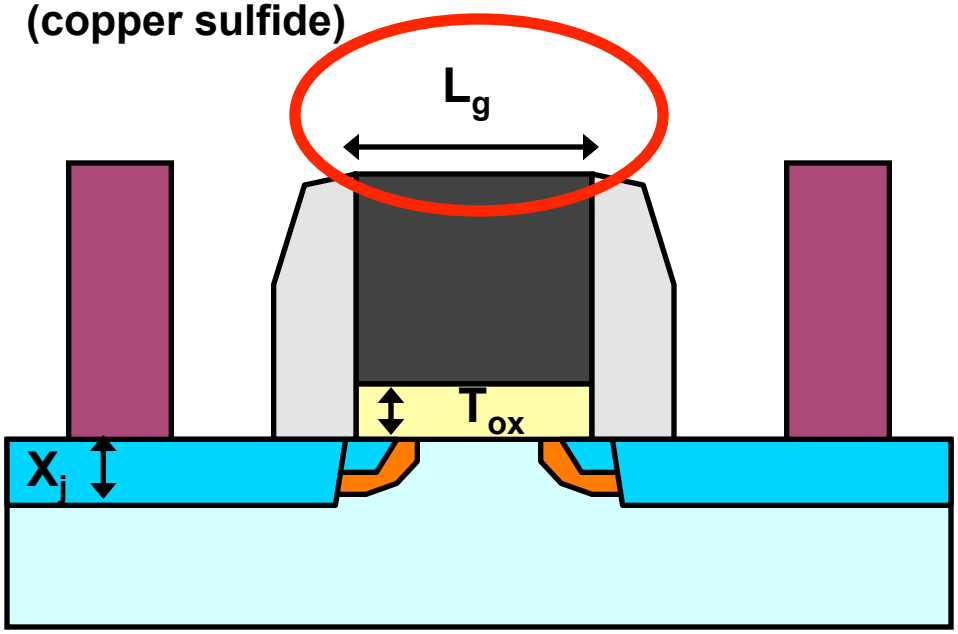
λ=dimensional scaling factor; k=supply voltage scaling factor

Constant Field Scaling: keep E constant in channel **k= λ**


1000 nm
100 nm
10 nm
1985
1995
2005
2015
0.8 um
0.5 um
0.35 um
0.25 um
0.18 um
0.13 um
90 nm
65 nm
35 nm
Historical gate scaling
More aggressive
gate scaling

MOSFET Transistor Scaling

MOSFET invented by Lilienfeld 1928 (copper sulfide)



L_g/α

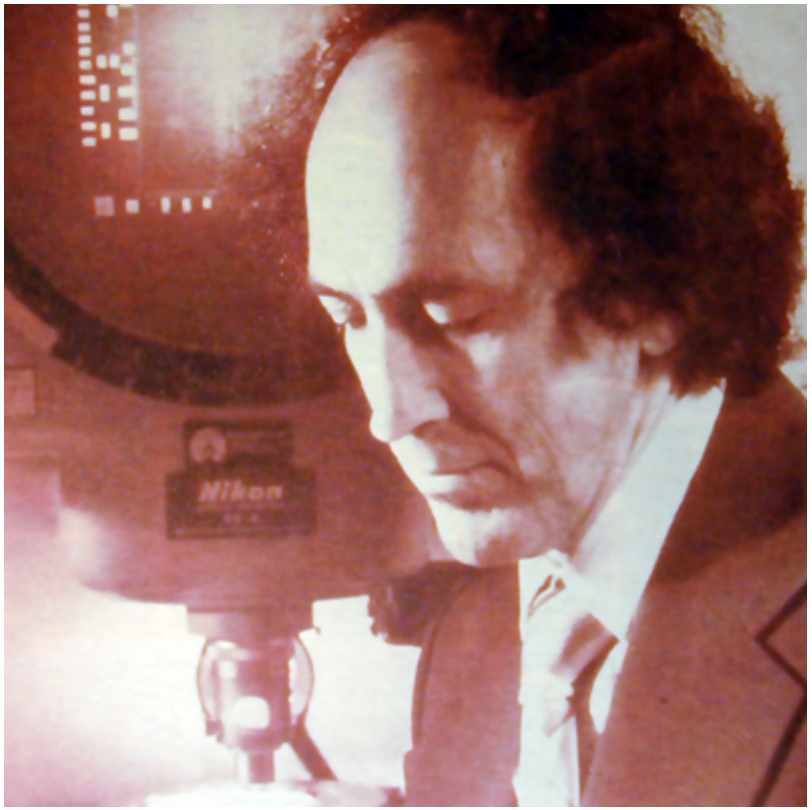
Original scaling approach

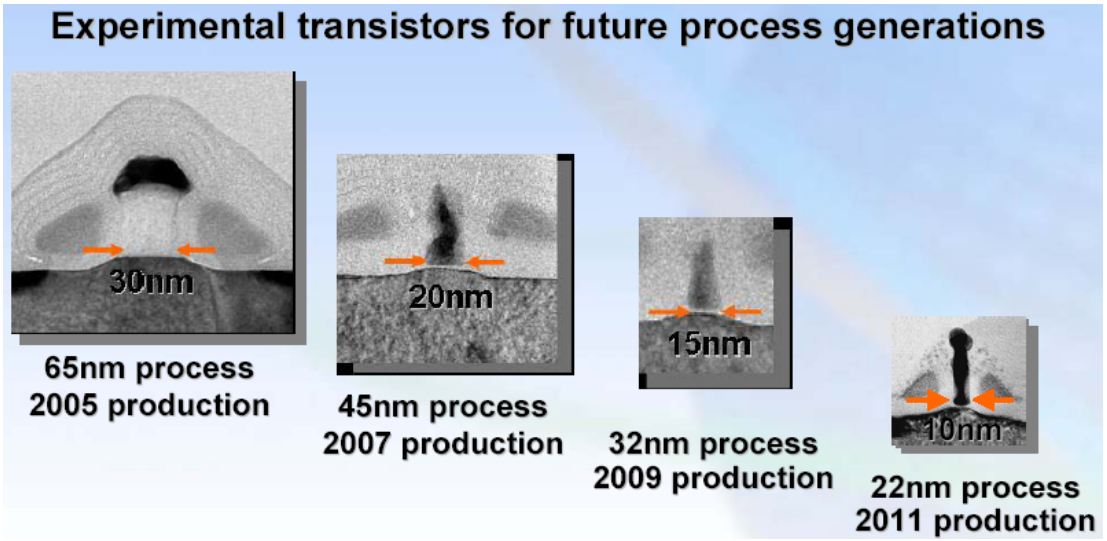
Parameter	Scaling Model Constant Field
Length	$1/\alpha$
Width	$1/\alpha$
Junction Depth	$1/\alpha$
Gate oxide thickness	$1/\alpha$
Supply Voltage	$1/\alpha$
Substrate Doping	α
Depletion layer thickness	$1/\alpha$
Current	$1/\alpha$
Transconductance	1
Electric Field across gate oxide	1
Load Capacitance	$1/\alpha$
Gate Delay	$1/\alpha$
DC power dissipation	$1/\alpha^2$
Dynamic power dissipation	$1/\alpha^2$
Power-delay product	$1/\alpha^3$

$\alpha \approx 1.4$ in two years

Scaling theory, Dennard 1974

MOSFET SCALING Dennard's Paper 1974





Bob Dennard (1-FET DRAM cell, 1968;
scaling theory with Fritz Gänsslen,1974)

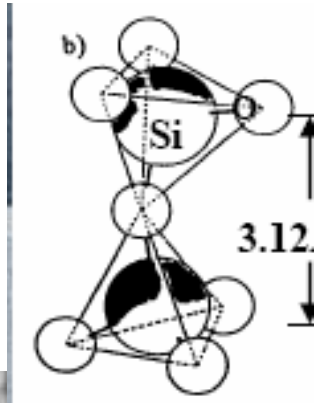
Implications of Scaling Theory

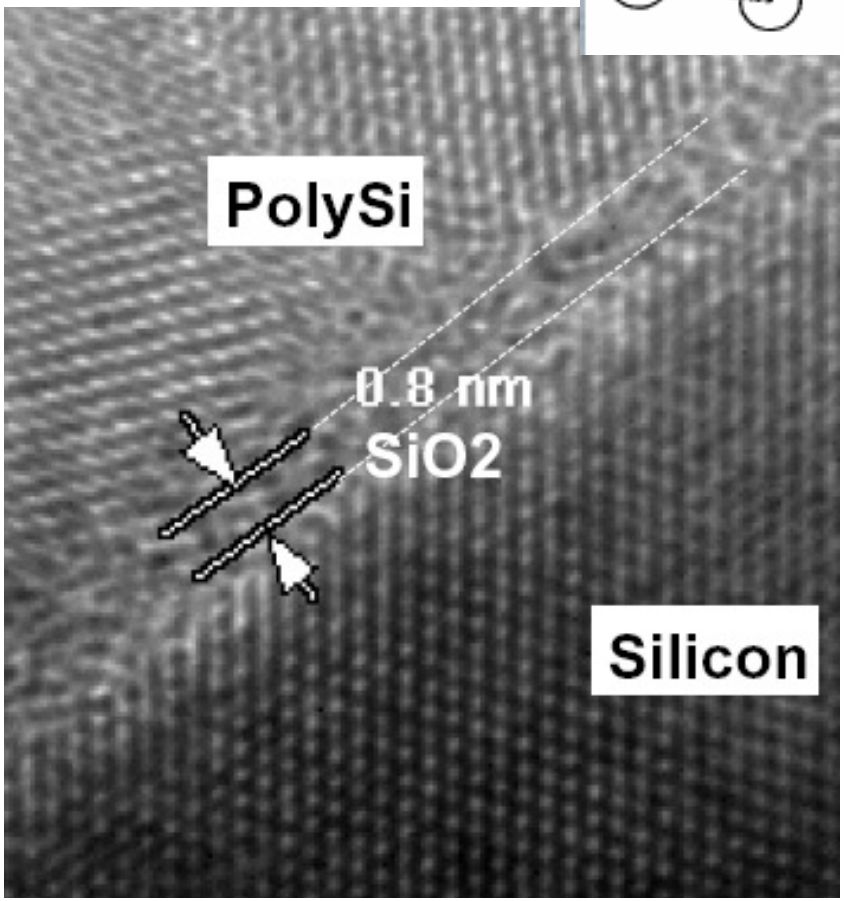
Scaling Factor α (traditionally $\alpha = 1.4 = \sqrt{2}$)

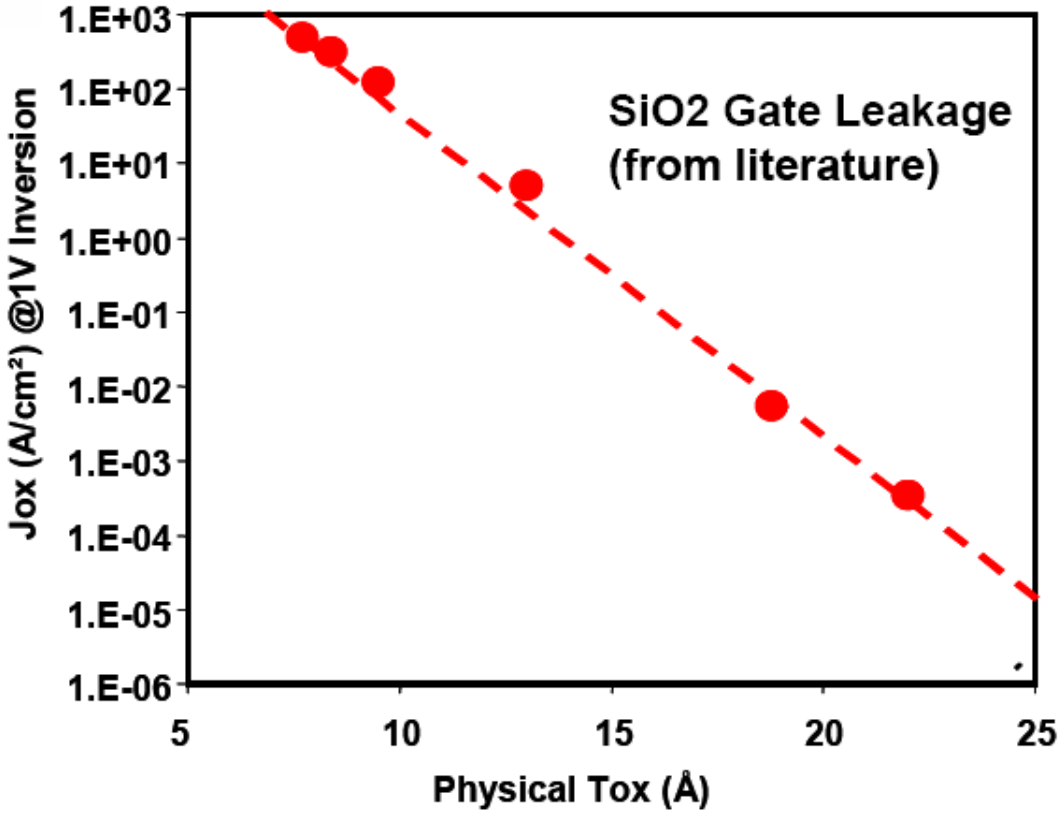
- Circuit density increases by α^2 (= 2)
- Circuit delay decreases by α
- Power/circuit decreases by α^2
- Power /unit area remains constant
- Price per function decreases $\alpha - \alpha^2$

Is there any oxide Left?

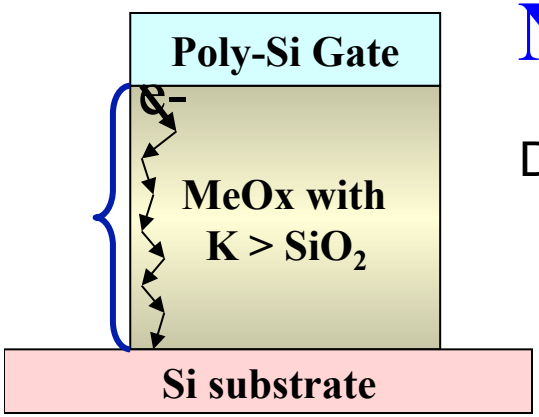
Gate oxide less than 3 atomic layers thick

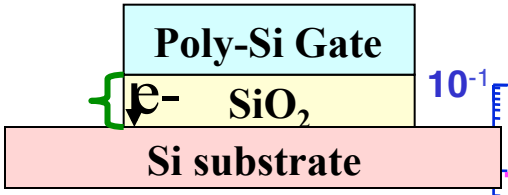




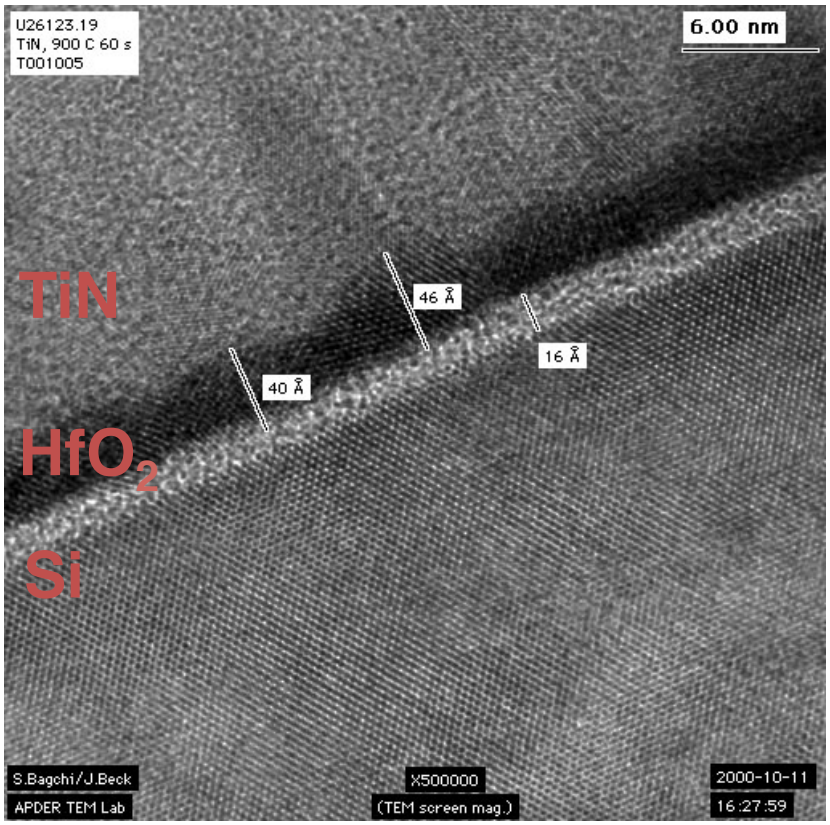


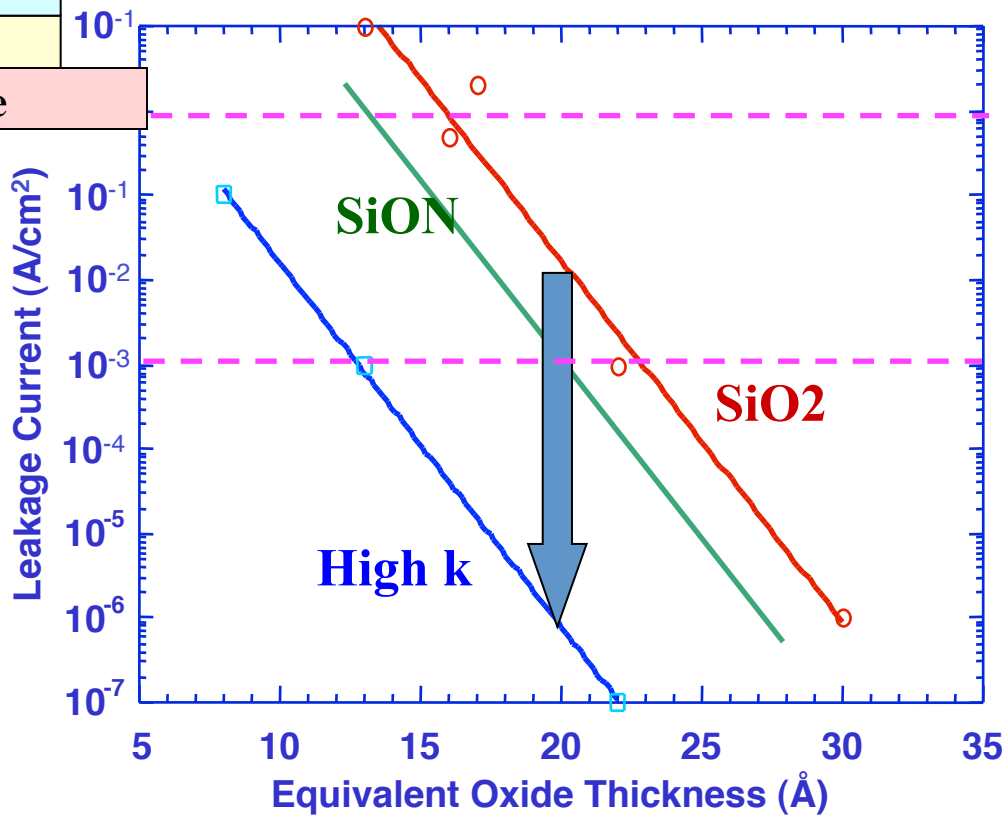
New Gate Dielectric Material Needed!



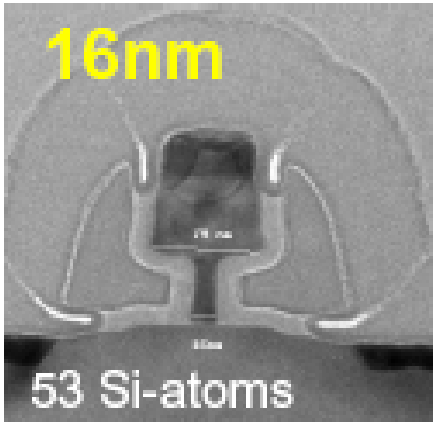


Dielectric constant k(HfO2)= 25 k(SiO2) = 4

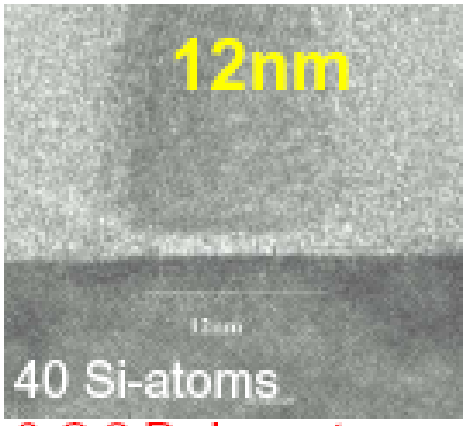




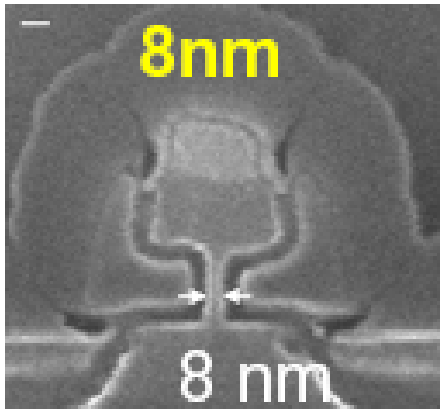
A MOSFET Limitation: Dopant Fluctuation



& 3.5 B-dopants
(1e19cm-3) under gate

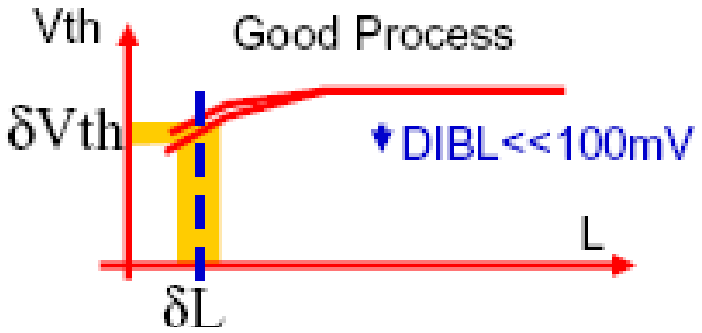


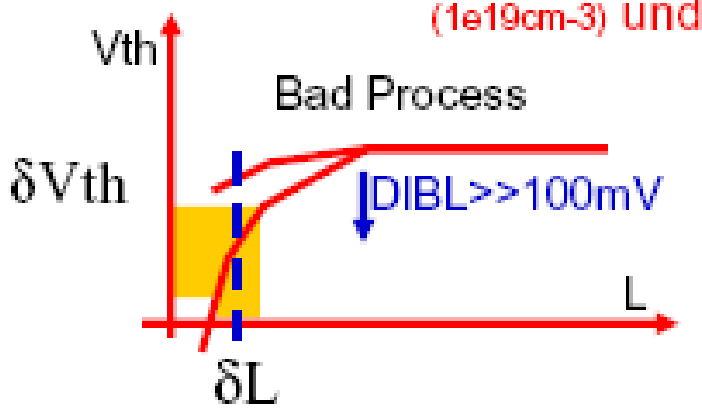
& 2.6 B-dopants
(1e19cm-3) under gate



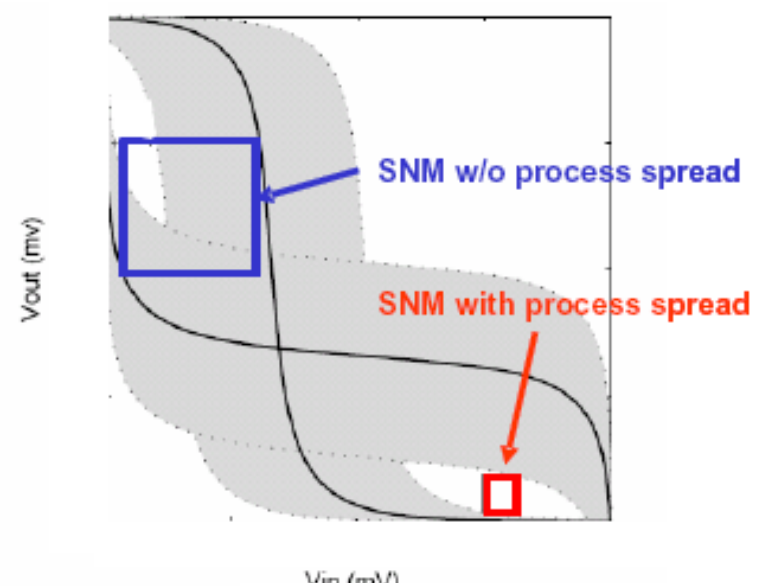
27 Si-atoms
& 1.7 B-dopants
(1e19cm-3) under gate

2) PROCESS DISPERSIONS:



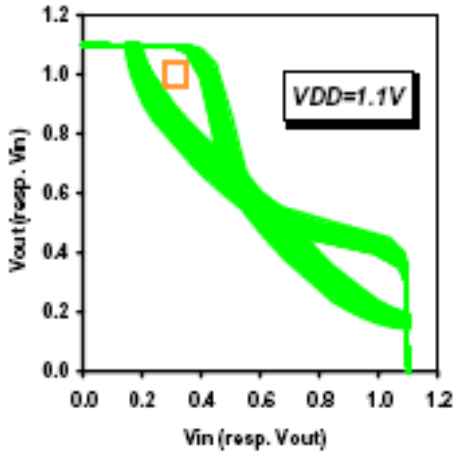


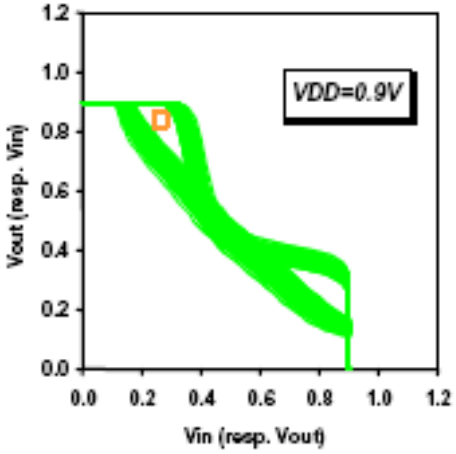
Fluctuations – Impact on SRAM Cell

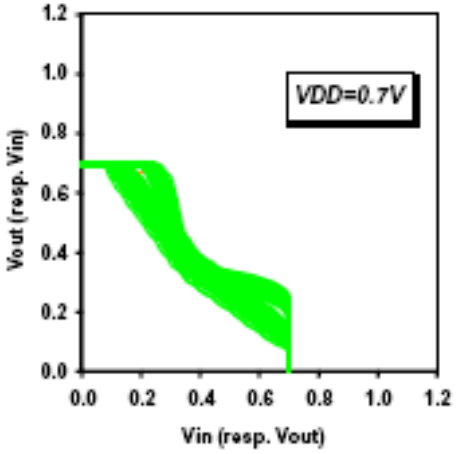


Solid lines represent ideal case with no process variation.

SNM decreases with Vdd, but fluctuations remain constant; the cell becomes unstable and inoperable.







Quantum Corrections to MOS Capacitor

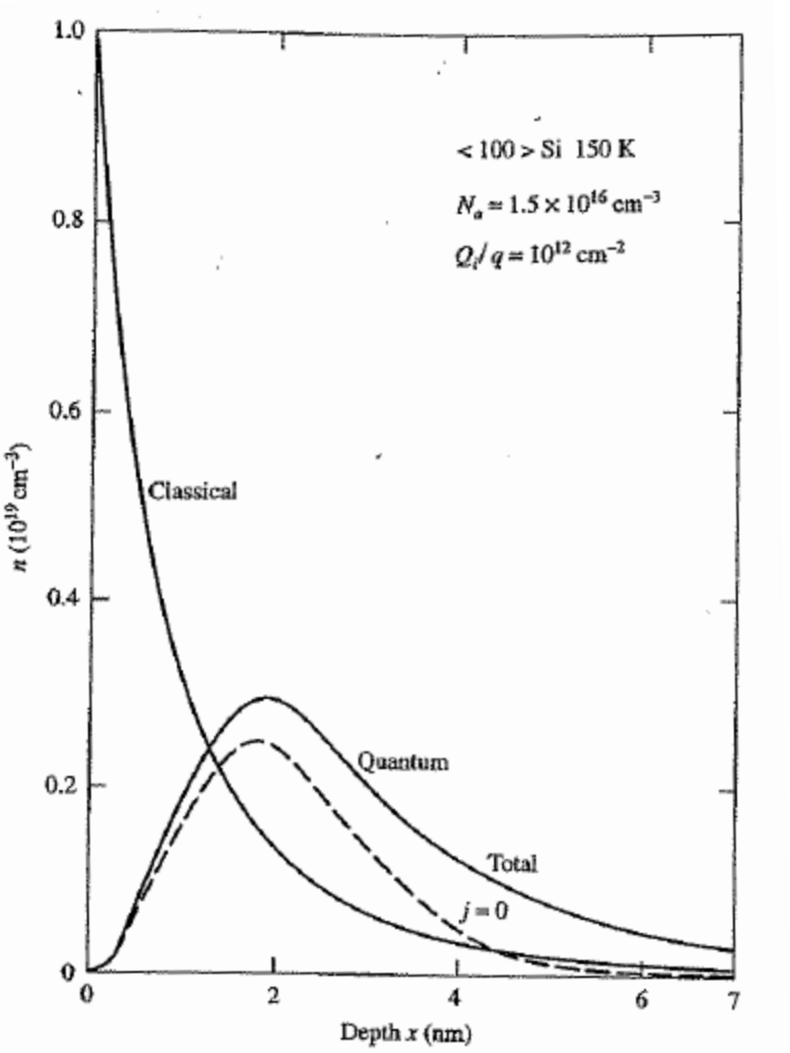
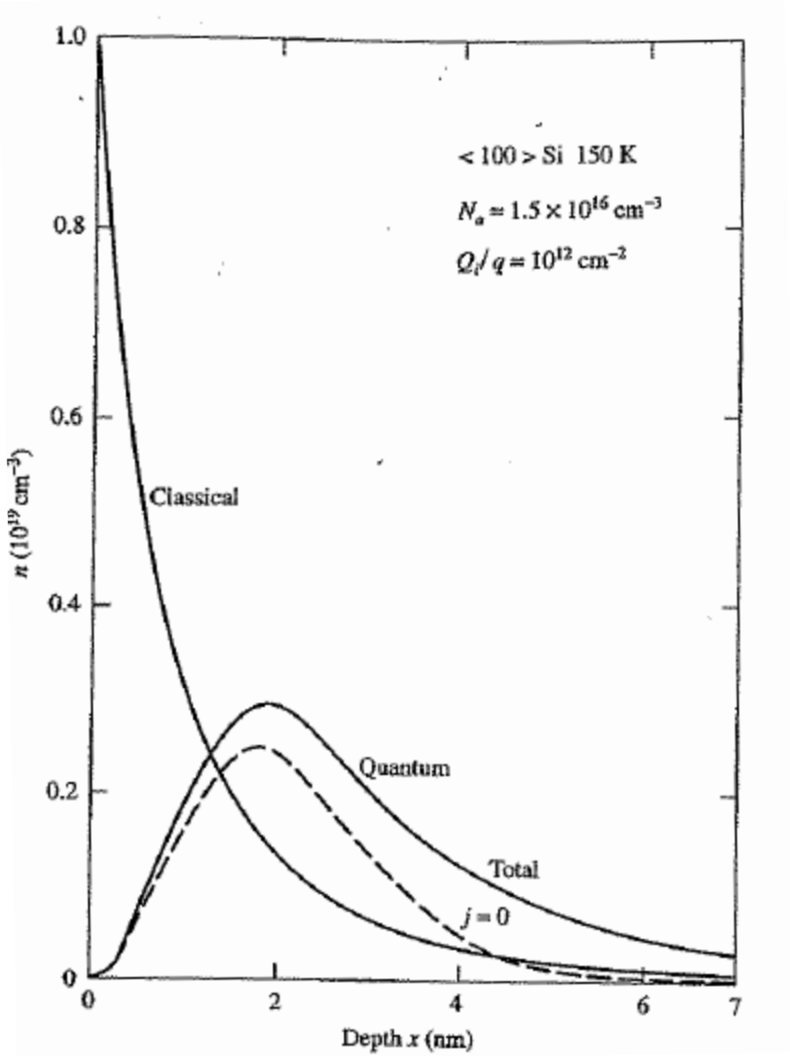


FIGURE 4.16. Classical and quantum-mechanical electron density versus depth for a ⟨100⟩ silicon inversion layer. The dashed curve shows the electron density distribution for the lowest subband. (After Stern, 1974.)



Important for the description of the surface scattering events in the channel (impact on mobility)

Quantum Corrections to MOS Capacitor

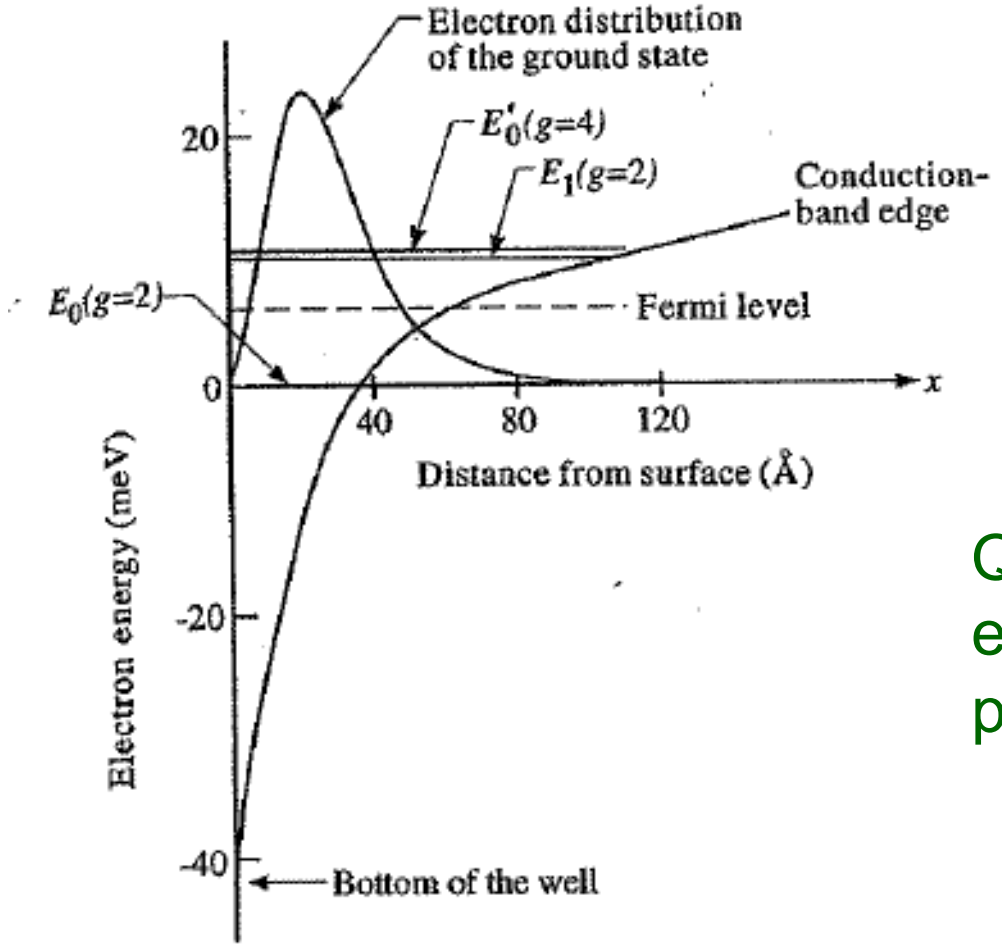


FIGURE 4.15. An example of quantum-mechanically calculated band bending and energy levels of inversion-layer electrons near the surface of an MOS device. The ground state is about 40 meV above the bottom of the conduction band at the surface. The dashed line indicates the Fermi level for 10^{12} electrons/cm^2 in the inversion layer. (After Stern and Howard, 1967.)

Quantum mechanics enters the MOSFET physics

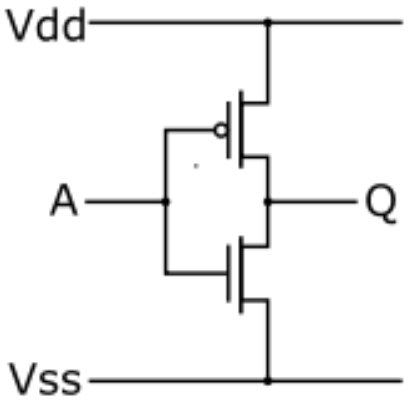
Maximum Switching Frequency (not in saturation)

$$\omega_{\max} = \frac{1}{L/v} = \frac{drift\ velocity}{channel\ length}$$

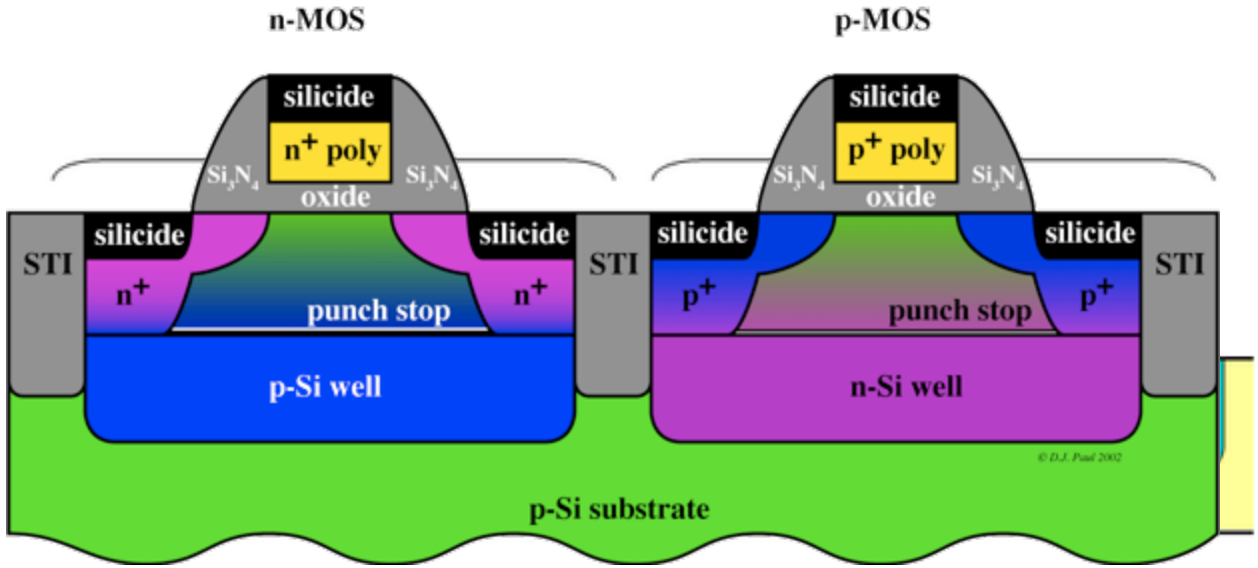
$$v = \mu V_D / L$$

$$f_{\max} = \frac{\mu_n V_D}{2\pi L^2}$$

Simple CMOS Circuits

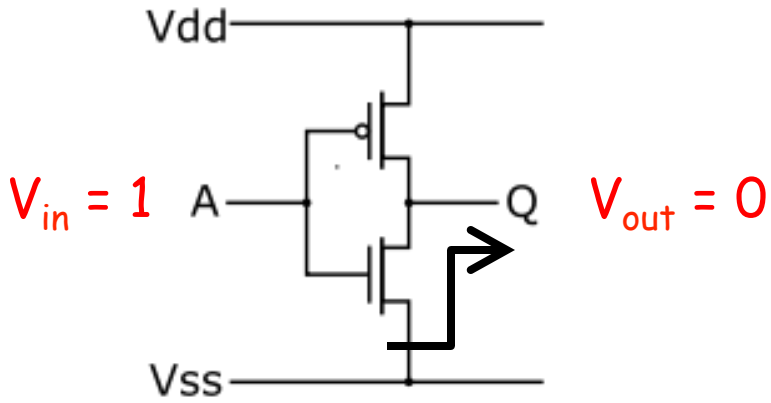


NOT gate
(inverter)



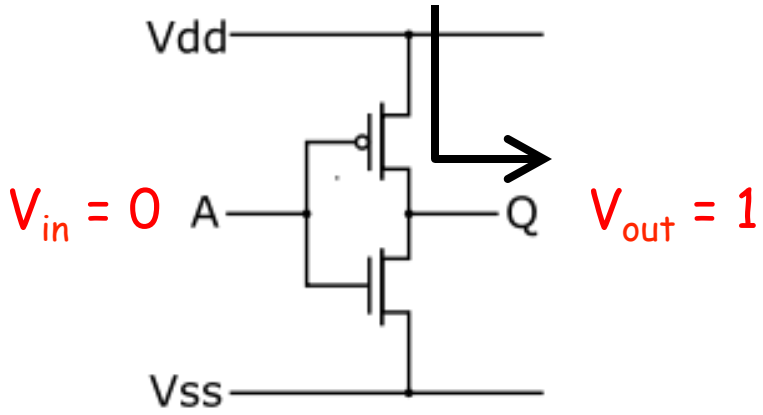
CMOS Circuits

Positive input (V_{in}) on the common gate turns nMOS on while PMOS is off.
NMOS is conductive and transmits the low voltage (ground) V_{ss} to the output.



NOT gate
(inverter)

CMOS Circuits



NOT gate
(inverter)

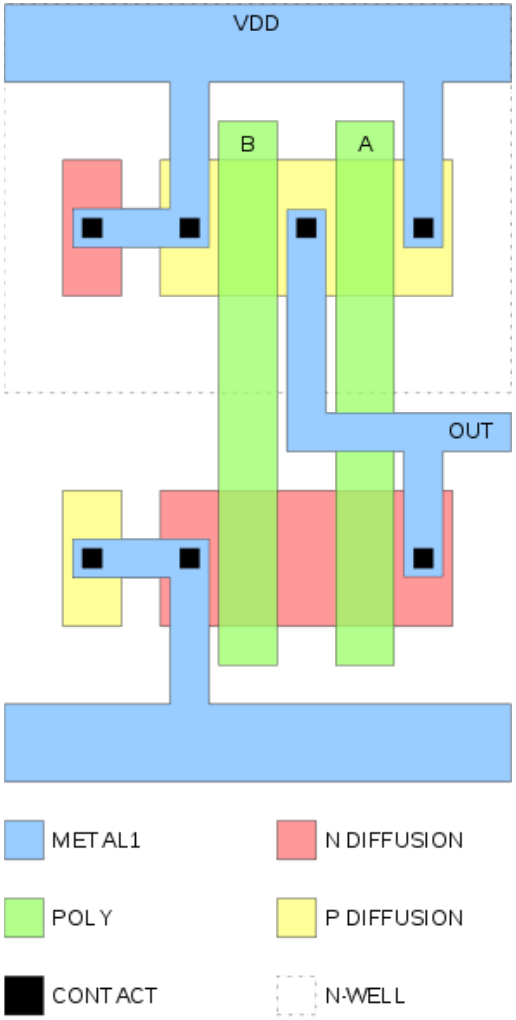
Negative input (V_{in}) on the common gate turns PMOS on while NMOS is off.

PMOS is conductive and transmits the high voltage (usually supply voltage) Vdd to the output.

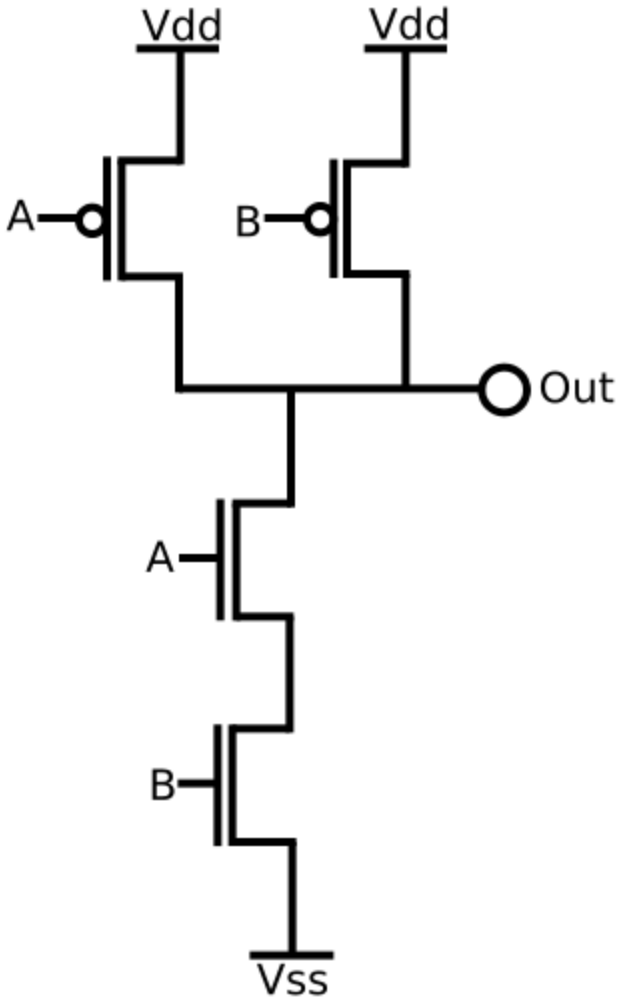
Importantly, since one is open and one is shut at steady state, **no current except during turn-on/turn-off**

→ Low power dissipation

CMOS Circuits



If we can create a NOT gate
we can create other gates (e.g. NAND, EXOR)



$$\overline{A \cdot B} = \overline{A} + \overline{B}$$

A	B	$\overline{A}$	$\overline{B}$	$\overline{A \cdot B}$	$\overline{A} + \overline{B}$
0	0	1	1	1	1
0	1	1	0	1	1
1	0	0	1	1	1
1	1	0	0	0	0