ECE 5205
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MOSFET Operation Part 2

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MOSFET Operation

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- Saturation velocity
- Mobility and mobility degradation
- Conductance and Transconductance
- Channel Length Modulation
- Short Channel Effects
- Reverse Short Channel Effects
- Drain Induced Barrier Lowering (DIBL)
- Narrow Width Effects
- Hot Carrier Effects

MOSFET Operation

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- **Gate Current**
- **Oxide Degradation**
- **High Electric Fields at the Drain**
- **Lightly Doped Drain Engineering (LDD)**
- **Quantum Corrections in Inversion Channel**

Short Channel Effect

Short channel effect (SCE) is the decrease of the MOSFET threshold voltage as the channel length is reduced. The short channel effect is especially pronounced when the drain bias is high.

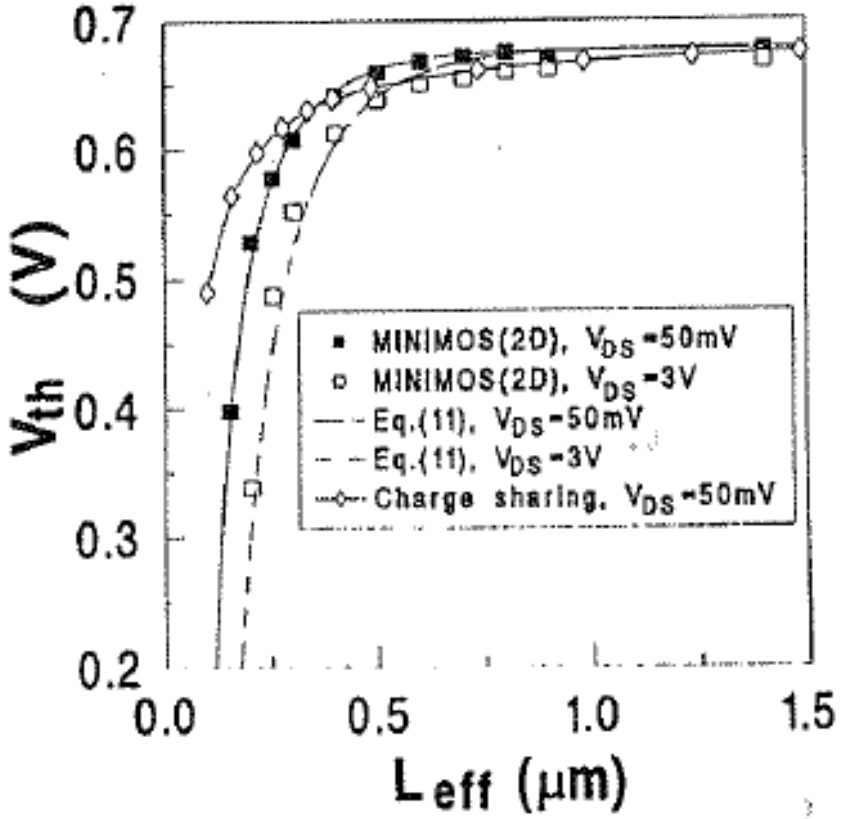


Fig. 5-7 Comparison of the V_T calculated using the charge sharing model, the two-dimensional numerical simulation (using MINIMOS), and the model of ref. 22. The device parameters are the same as those used in Fig. 5-5.[22] (© 1993 IEEE).

Short Channel Effect

When we derived the threshold voltage we have assumed that the sum of charges on the gate electrode and in the semiconductor adds up to zero. In other words, we have neglected any effects on threshold voltage that might occur due to source and drain space charge regions that extend into the channel region. These charges upend the balance of charges of an ideal MOS capacitor.

As the channel length decreases the fraction of charge in the channel region controlled by the gate decreases too. As the drain voltage increases, the reverse-biased space charge region at the drain end extends further into the channel area and the gate will control even less bulk charges.

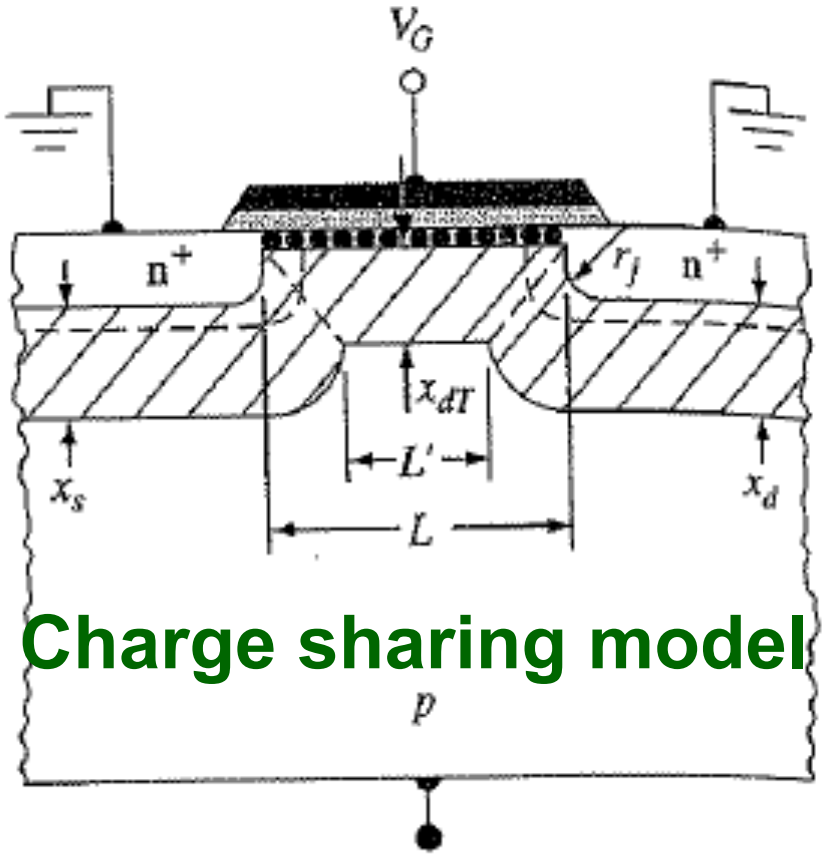
Recall

$$V_T = V_{FB} - 2\psi_B - \frac{\sqrt{4\psi_B \varepsilon_s q N_A}}{C_{ox}}$$

where the last term is the maximum depletion charge.

Short Channel Effect

We can determine the short-channel effect by considering parameters in the figure below. The s/d junctions are characterized by junction depth $r_j = x_{s/d}$. The simplifying mathematical assumption is that the bulk charge in the



Charge sharing model

Figure 12.15 | Charge sharing in the short-channel threshold voltage model. *(From Yau [26].)*

trapezoidal region under the gate is controlled by the gate. The potential difference across the space charge region is $2\psi_B$ at the inversion condition, and the built-in potential barrier height of the s/d junctions is also approximately $2\psi_B$, implying that the three space charge widths are essentially equal. We can then write

$x_s \approx x_d \approx x_{dT}$

Using the area of a trapezoid, the average bulk charge per unit area Q_B in the trapezoid is

$$\left|Q_B\right| \cdot L = qN_A x_{dT}\left(\frac{L+L'}{2}\right)$$

where $x_{dT} \equiv W_{\max}$ is the maximum depletion width

Short Channel Effect

$$|Q_B| \cdot L = qN_A x_{dT}\left(\frac{L+L'}{2}\right)$$

From the geometry, we can show that

$$\left(\frac{L+L'}{2L}\right) = \left[1 - \frac{r_j}{L}\left(\sqrt{1+\frac{2x_{dT}}{r_j}} - 1\right)\right]$$

Since $|Q_{dep}| = qN_A x_{dT}$

$$|Q_B| = qN_A x_{dT}\left[1 - \frac{r_j}{L}\left(\sqrt{1+\frac{2x_{dT}}{r_j}} - 1\right)\right]$$

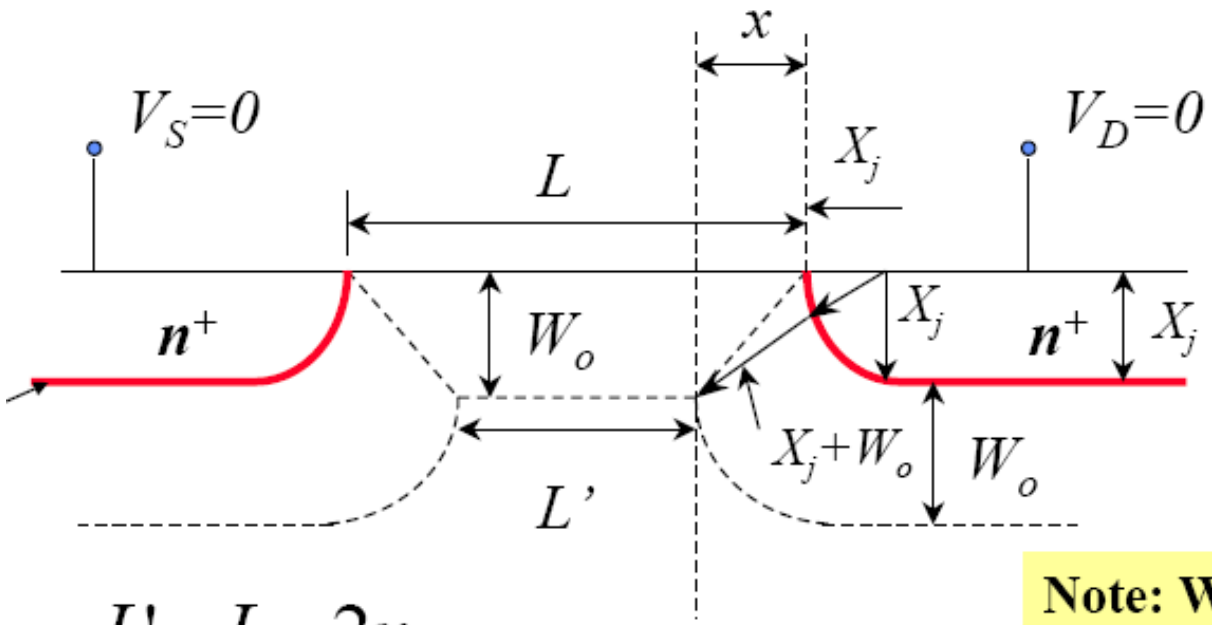
We can find ΔV_T as

$$\Delta V_T = \frac{qN_A x_{dT}}{C_{ox}} \cdot \frac{r_j}{L} \cdot \left(\sqrt{1+\frac{2x_{dT}}{r_j}} - 1\right)$$

$$\Delta V_T = V_{T(short\ \ channel)} - V_{T(long\ \ channel)}$$

As the channel length decreases, the threshold voltage shifts in the negative direction so that an n-channel MOSFET shifts toward depletion mode.

Short Channel Effect



Note: W_o is x_{dmax}

Geometrical considerations

$$L' = L - 2x$$

$$= L - 2\left[\sqrt{(X_j + W_o)^2 - W_o^2} - X_j\right]$$

$$= L - 2X_j\left[\sqrt{1 + \frac{2W_o}{X_j}} - 1\right]$$

Short Channel Effect

Area of gate charge distribution

$$= q \cdot N_a \cdot \frac{L + L_1}{2} \cdot W_o \cdot W$$

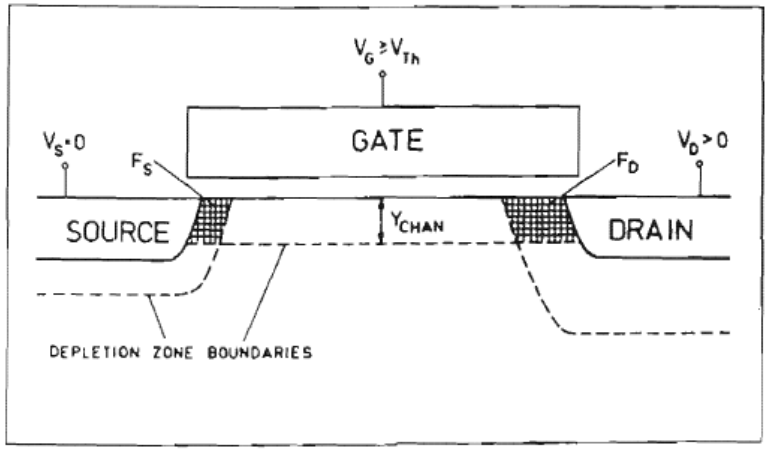
$$\therefore \frac{Q_{actual}}{Q_{ideal}} = \frac{\text{⏢}}{\text{▭}}$$

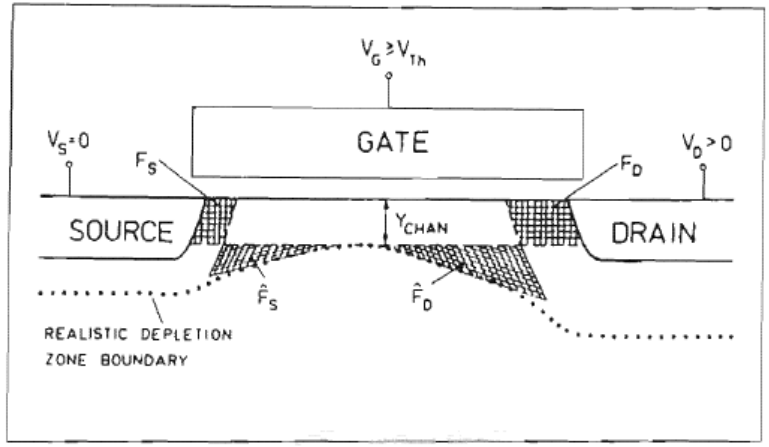
factor f

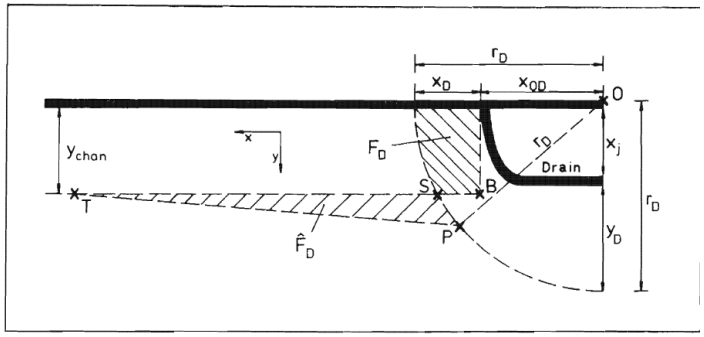
$$= 1 - \frac{X_j}{L}\left[\sqrt{1 + \frac{2W_o}{X_j}} - 1\right] \equiv f$$

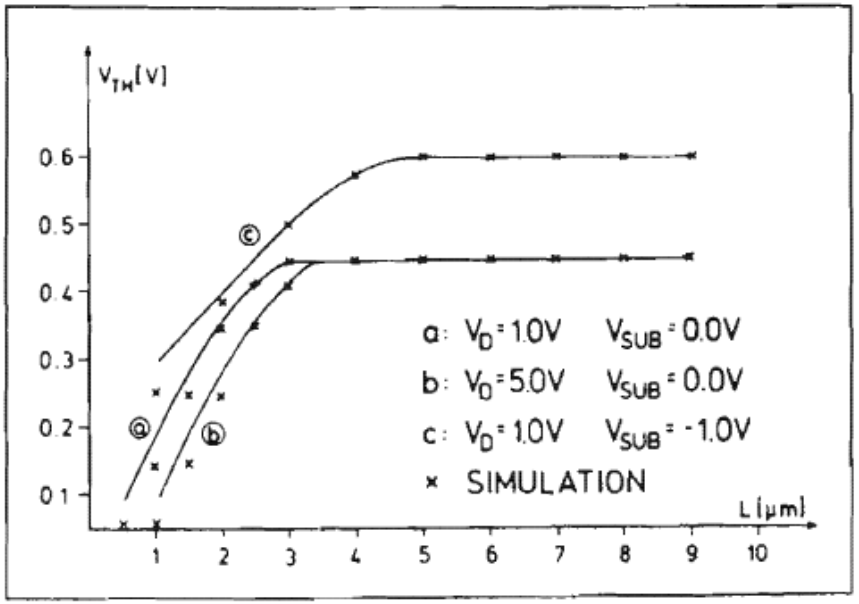
"Yau Model" for short-channel effect.

Improved Short Channel Model









M.Orlowski and Ch. Werner,
"**A Novel Realistic Model for Threshold Voltage of Short Channel MOSFETs"**
Solid State Device Research Conference,
1987. ESSDERC '87 p.547-550

Short Channel Effect Counter Measures

To make f → 1

→ X_j ↓

- Implantation at low energy
- Small Dt.
- Minimize channeling and transient enhance diffusion

→ W_o ↓

- Increase N_a

Short Channel Effect

Short channel effect (SCE) is the decrease of the MOSFET threshold voltage as the channel length is reduced. The short channel effect is especially pronounced when the drain bias is high.

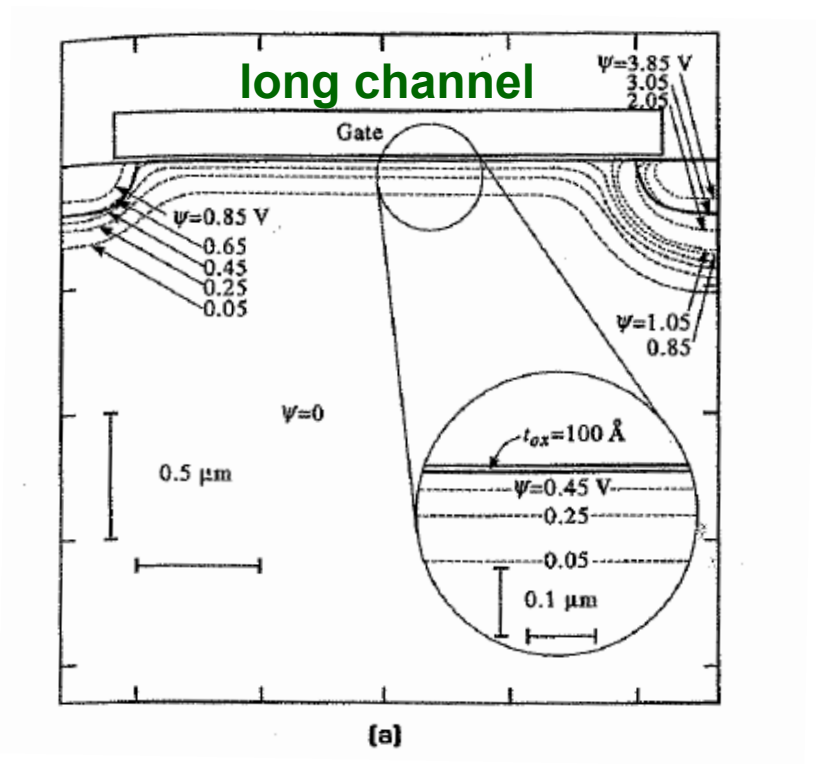


FIGURE 3.18. Simulated constant potential contours of (a) a long-channel and (b) a short-channel nMOSFET. The contours are labeled by the band bending with respect to the neutral p-type region. The solid lines indicate the location of the source and drain junctions (metallurgical). The drain is biased at 3.0 V. Both devices are biased at the same gate voltage slightly below the threshold.

Short Channel Effect

The effect of short channel becomes more pronounced as L is reduced further. As shown below, as the substrate doping increases, V_T increases but the V_T shift also becomes larger. The V_T shift becomes smaller as the junction depth r_j decreases, so that shallow junctions reduce the V_T dependence on L.

Channel doping dependence

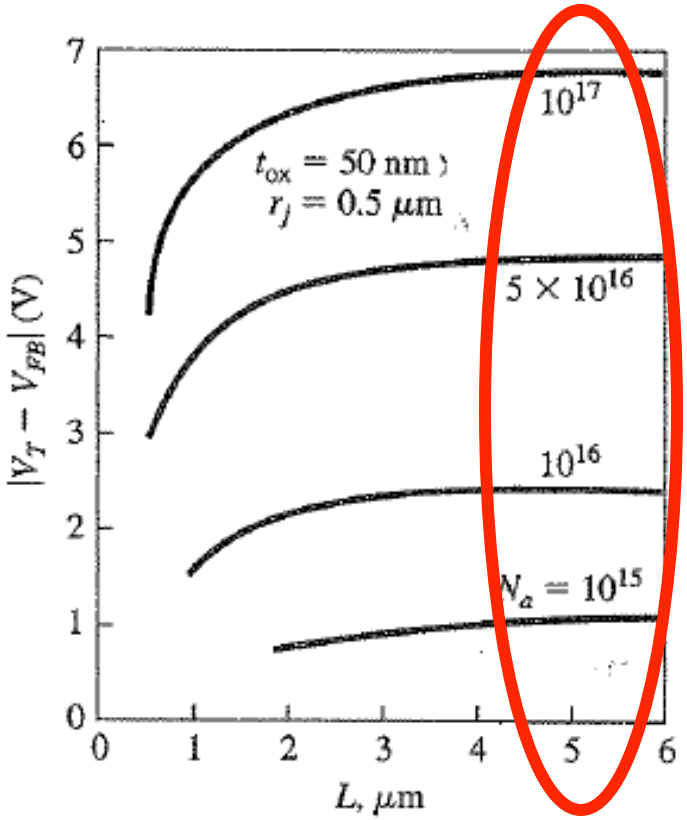


Figure 12.16 | Threshold voltage versus channel length for various substrate dopings. *(From Yau [26].)*

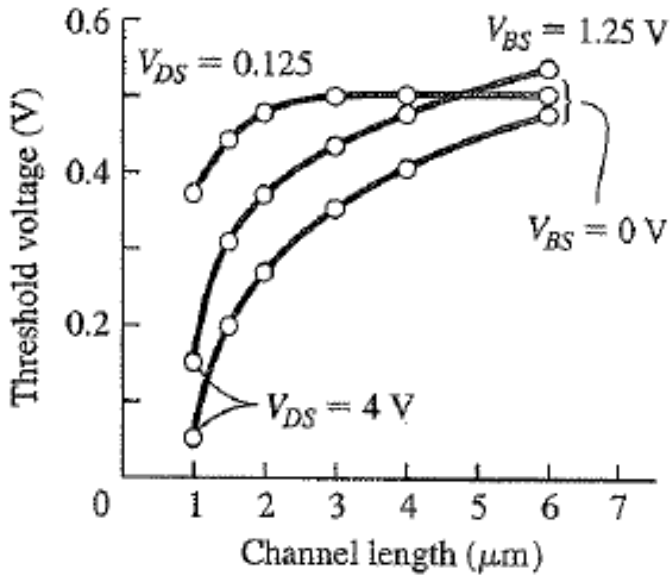


Figure 12.17 | Threshold voltage versus channel length for two values of drain-to-source and body-to-source voltage. *(From Yang [25].)*

Short Channel Effect Due to Drain Bias

So far we have assumed that the depletion region at source and drain where the same. If we now apply drain voltage, the space charge region at the drain widens, which makes L' smaller, and the amount of bulk charge controlled by the gate decreases even further. This effect makes the V_T a function of drain voltage. So as the drain voltage increases , the threshold voltage V_T of the MOSFET decreases.

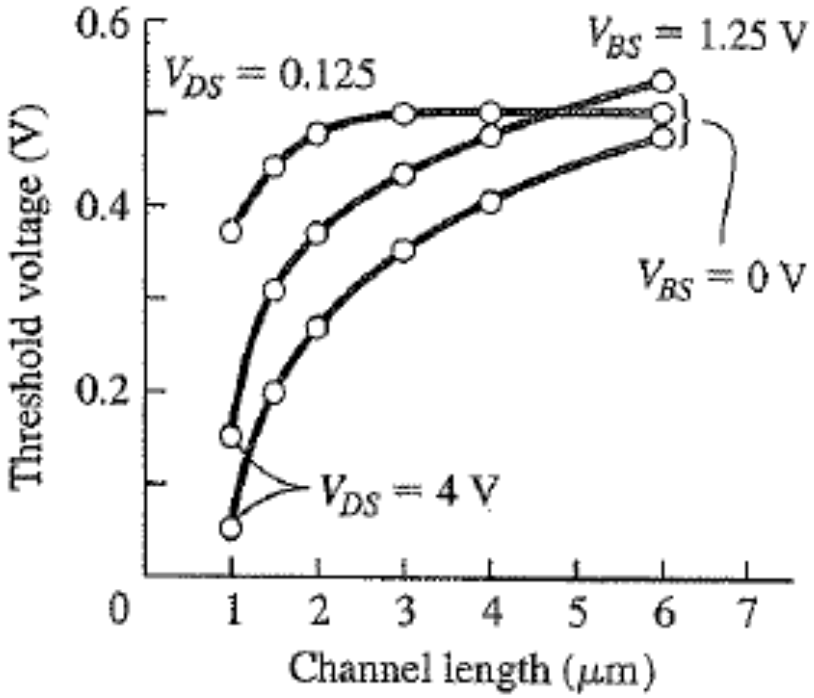


Figure 12.17 | Threshold voltage versus channel length for two values of drain-to-source and body-to-source voltage.

V_T dependence on V_D

Short Channel Effect Due to Drain Bias

The dependence of V_T as a function of drain bias (at short channel lenghts) is called drain induced barrier lowering or DIBL.

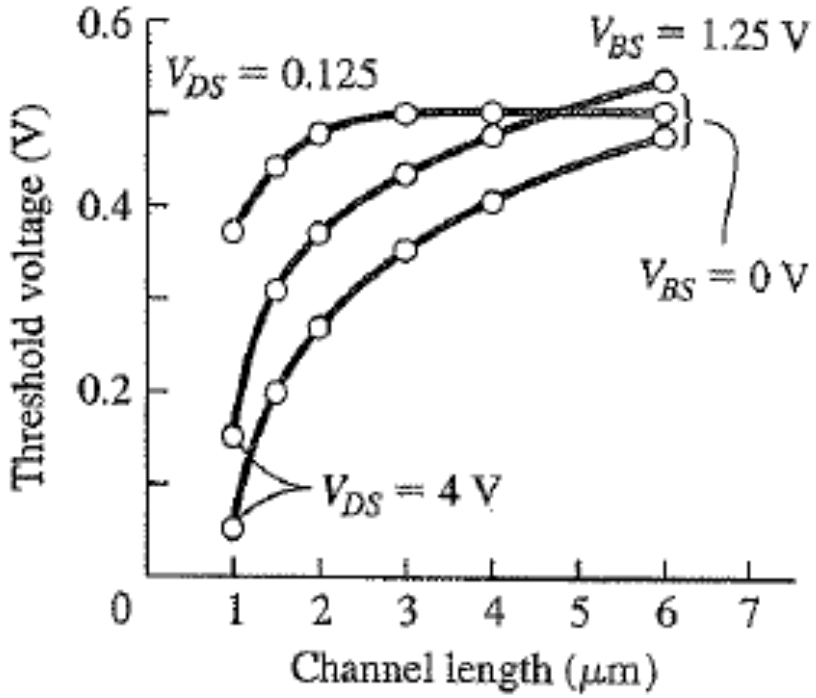


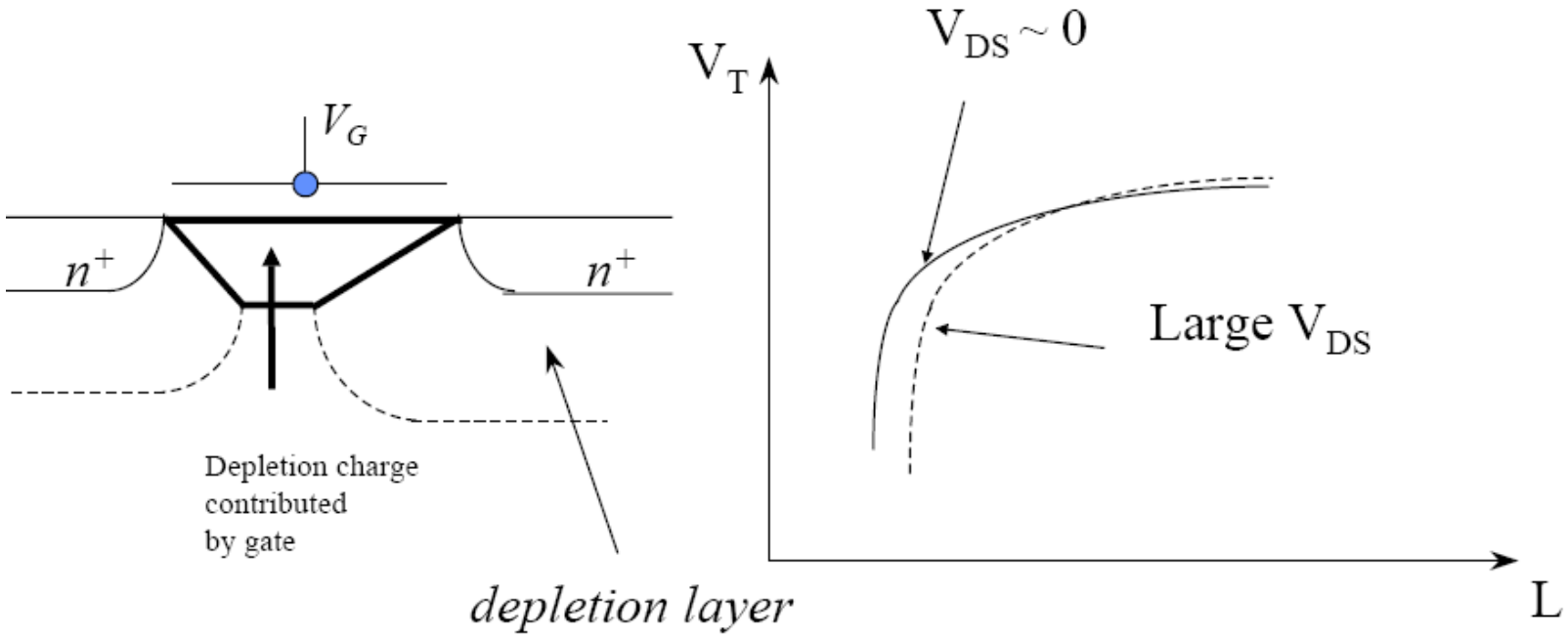
Figure 12.17 | Threshold voltage versus channel length for two values of drain-to-source and body-to-source voltage.

Drain-induced Barrier Lowering (DIBL)

When a high drain voltage is applied to a short-channel device, the barrier height is lowered even more, resulting in further decrease of the threshold voltage as shown in the figure below.

Effect of V_{DS} on V_T Lowering

Large $V_{DS} \Rightarrow$ Larger S/D depletion charge at the drain side
$\Rightarrow$ Smaller depletion region charge contributed by gate
$\Rightarrow$ V_T starts to decrease at larger L



Drain-induced Barrier Lowering (DIBL)

From the Figure below it can be observed that increased drain bias leads to a lower threshold voltage at short channel lengths and also the subthreshold slope increases.

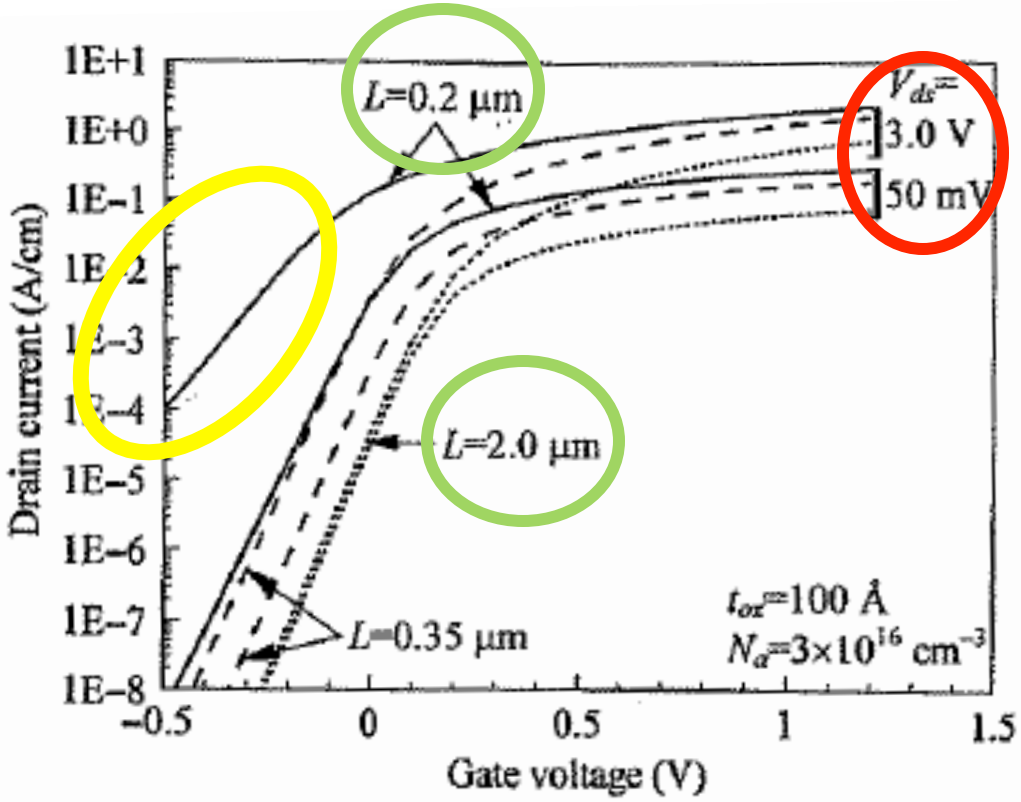


FIGURE 3.21. Subthreshold characteristics of long- and short-channel devices at low and high drain bias.

Drain-induced Barrier Lowering (DIBL)

The drain field reaches through the channel and reduces the barrier at the source side of the channel.

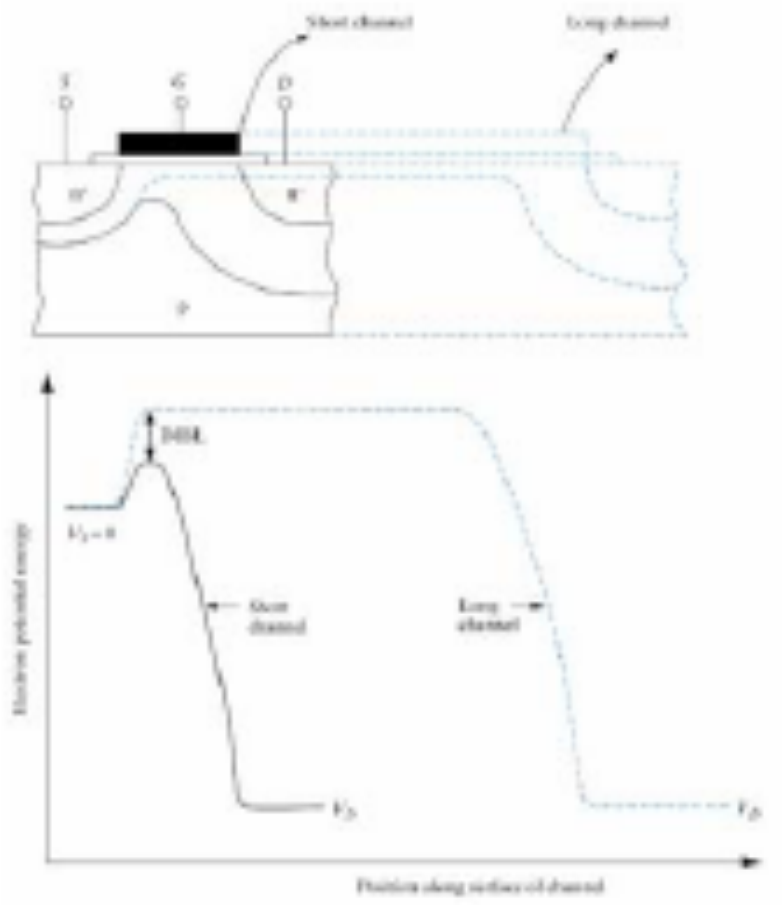


Figure 6—44
Drain-induced barrier lowering in MOSFETs. Cross-sections and potential distribution along the channel for a long channel and short channel MOSFET.

Drain-induced Barrier Lowering (DIBL)

The point of maximum barrier shifts toward the source end as shown below. This is referred to as drain-induced barrier lowering. It explains the experimentally observed increase of subthreshold current with drain voltage in short-channel MOSFETs. At very short channel lengths , the subthreshold slope starts to degrade as the surface potential is more controlled by the drain than by the gate electrode.

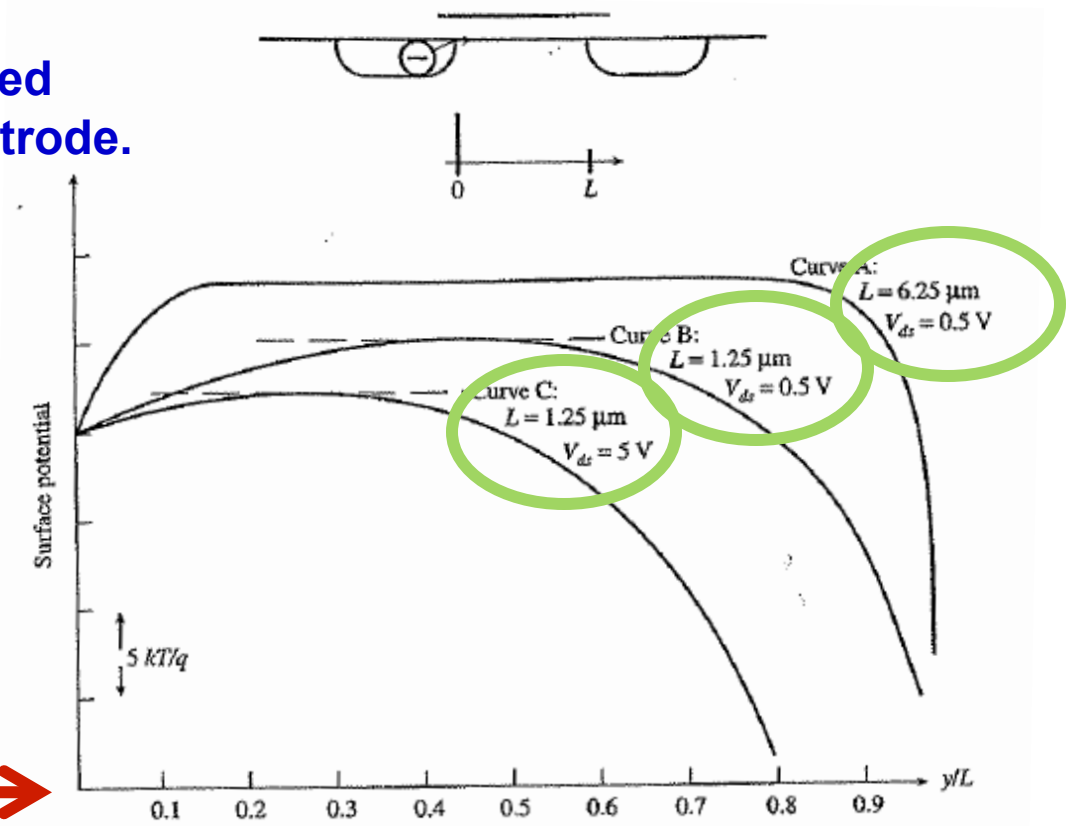


FIGURE 3.20. Surface potential versus lateral distance (normalized to the channel length L) from the source to the drain for (a) a long-channel MOSFET, (b) a short-channel MOSFET at low drain bias, and (c) a short-channel MOSFET at high drain bias. The gate voltage is the same for all three cases. (After Troutman, 1979.)

Please note that the horizontal scale is in the units of an actual channel length

Drain-induced Barrier Lowering (DIBL)

- Change in V_{T0}:
  - x_{dS}, x_{dD}: depth of depletion regions at S, D
  - x_j: junction depth

$$\Delta V_{T0} = \frac{1}{C_{ox}}\sqrt{2q\varepsilon_{Si}N_A|2\psi_B|} \times \frac{x_j}{2L}\left[\left(\sqrt{1+\frac{2x_{dS}}{x_j}}-1\right)+\left(\sqrt{1+\frac{2x_{dD}}{x_j}}-1\right)\right]$$

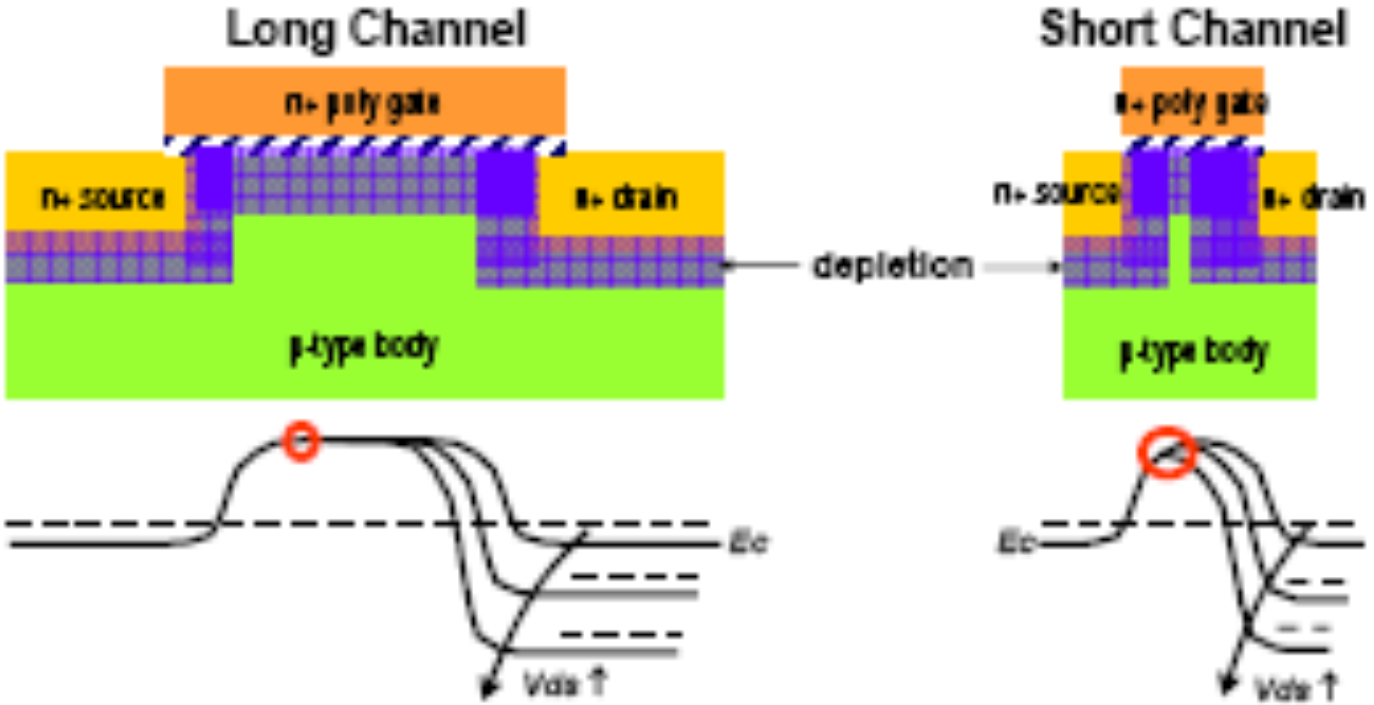
- ΔV_{T0} is proportional to (x_j/L)
  - For short channel lengths, ΔV_{T0} is large
  - For large channel lengths, term approaches 0

Drain-induced Barrier Lowering (DIBL)

- Drain-induced barrier lowering (DIBL)
  - Drain voltage V_{DS} causes change in threshold voltage
  - As V_{DS} is increased, threshold voltage decreases
- Cause: depletion region around drain
  - Depletion region depth around drain depends on drain voltage
  - As V_{DS} is increased, drain depletion region gets deeper and extends further into channel
  - For very large V_{DS}, source and drain depletion regions can meet → *punch-through*!
- Issue: results in uncertainty in circuit design

Drain-induced Barrier Lowering (DIBL)

Short Channel Effect: Drain Induced Barrier Lowering (DIBL)



- Increase in V_{DS} reduces V_t and increases V_t-roll-off: DIBL

Short Channel Effect - 3D View

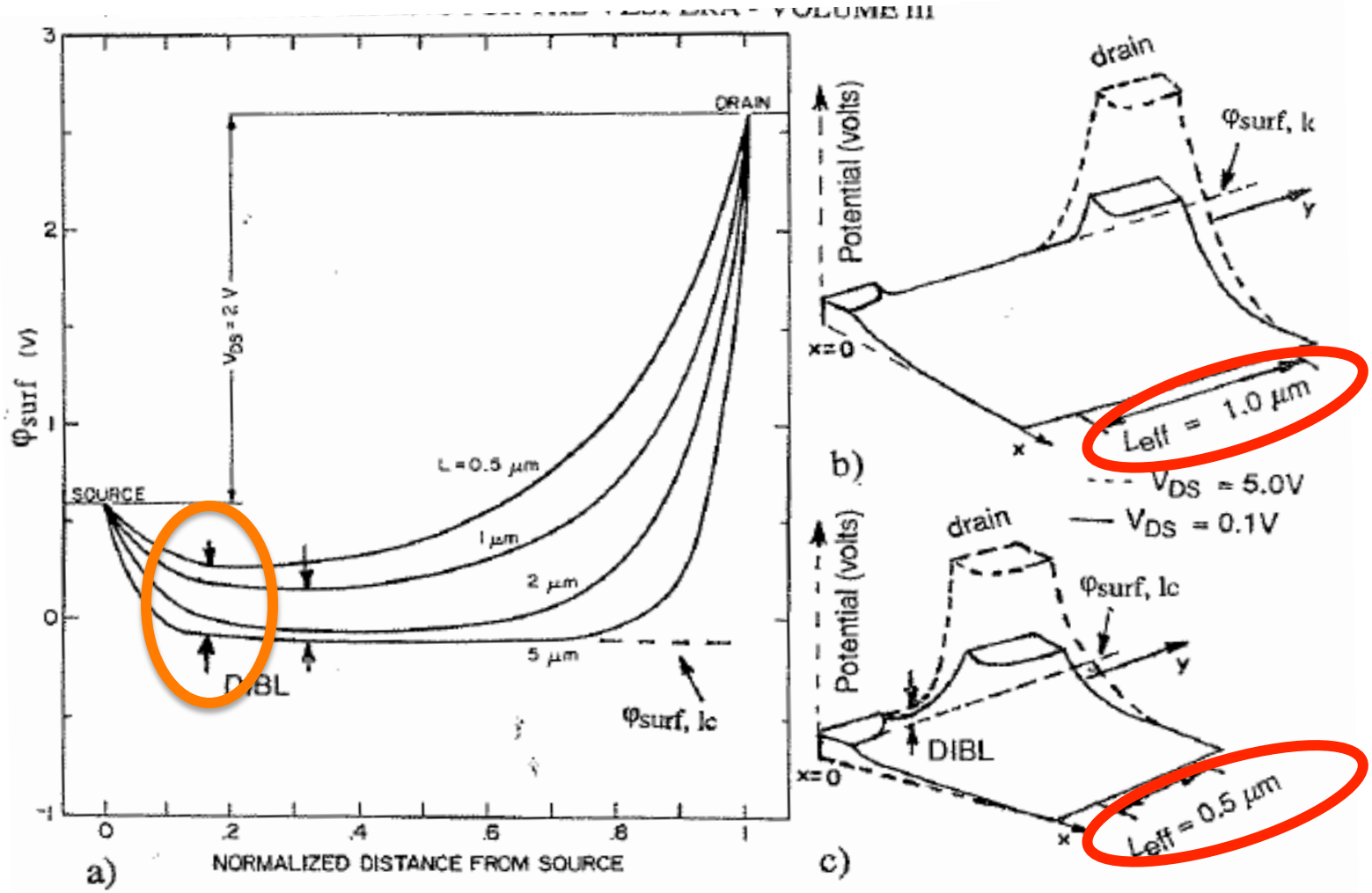
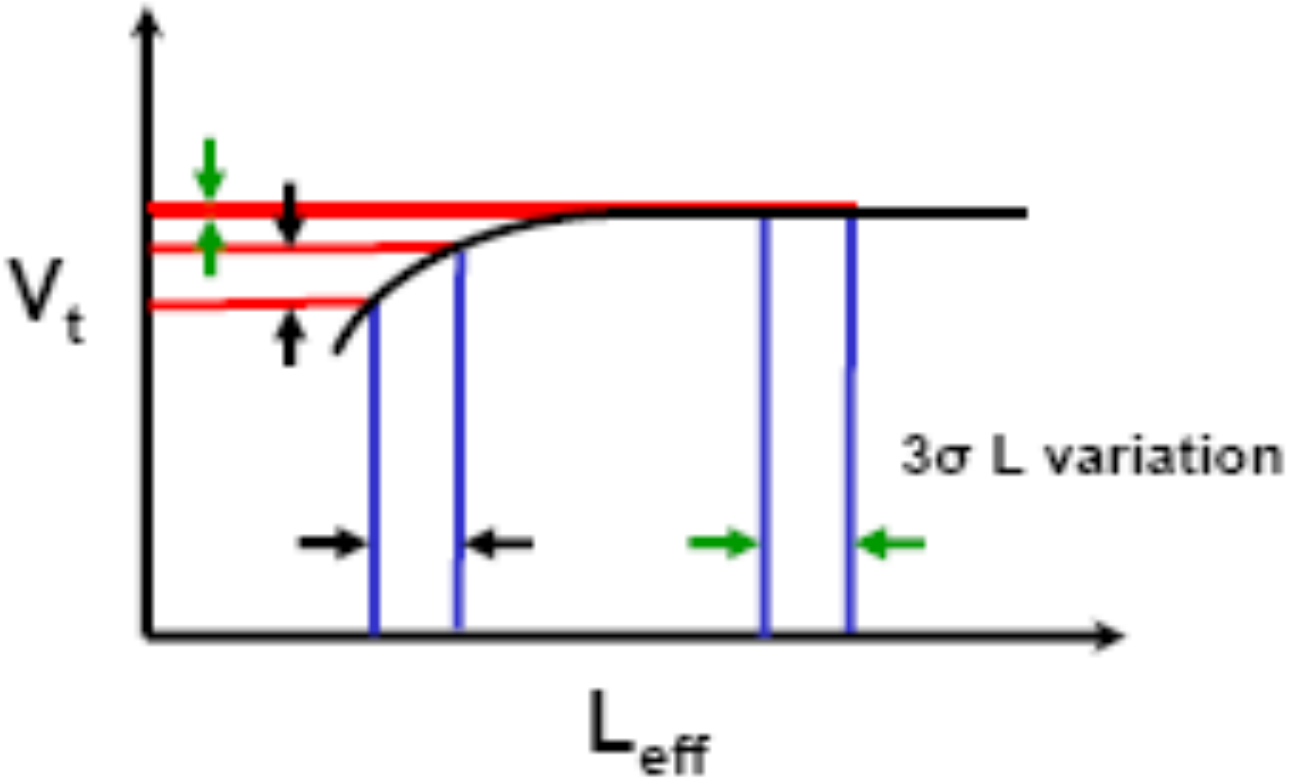


Fig. 5-3 Simulated values of the surface potential φ_{surf} along the channel for NMOSFETs with different channel lengths (note channel length is normalized). $N_A = 10^{15}$ cm^{-3}, t_{ox} = 500Å, $r_j = 0.33\mu$m, $V_{GS} = 0$V, $V_{DS} = 2.0$V, $V_{BS} = 0$V.[109] (© 1979 IEEE). (b & c) 2-D potential variation for NMOSFETs with (b) $L_{eff} = 1.0$ μm, and (c) $L_{eff} = 0.5$ μm (see also Fig. 5-5). Solid line, $V_{DS} = 0.1$V and dashed line, $V_{DS} = 5.0$V.

Short Channel Effect Implications

Short Channel Effect: V_t roll-off

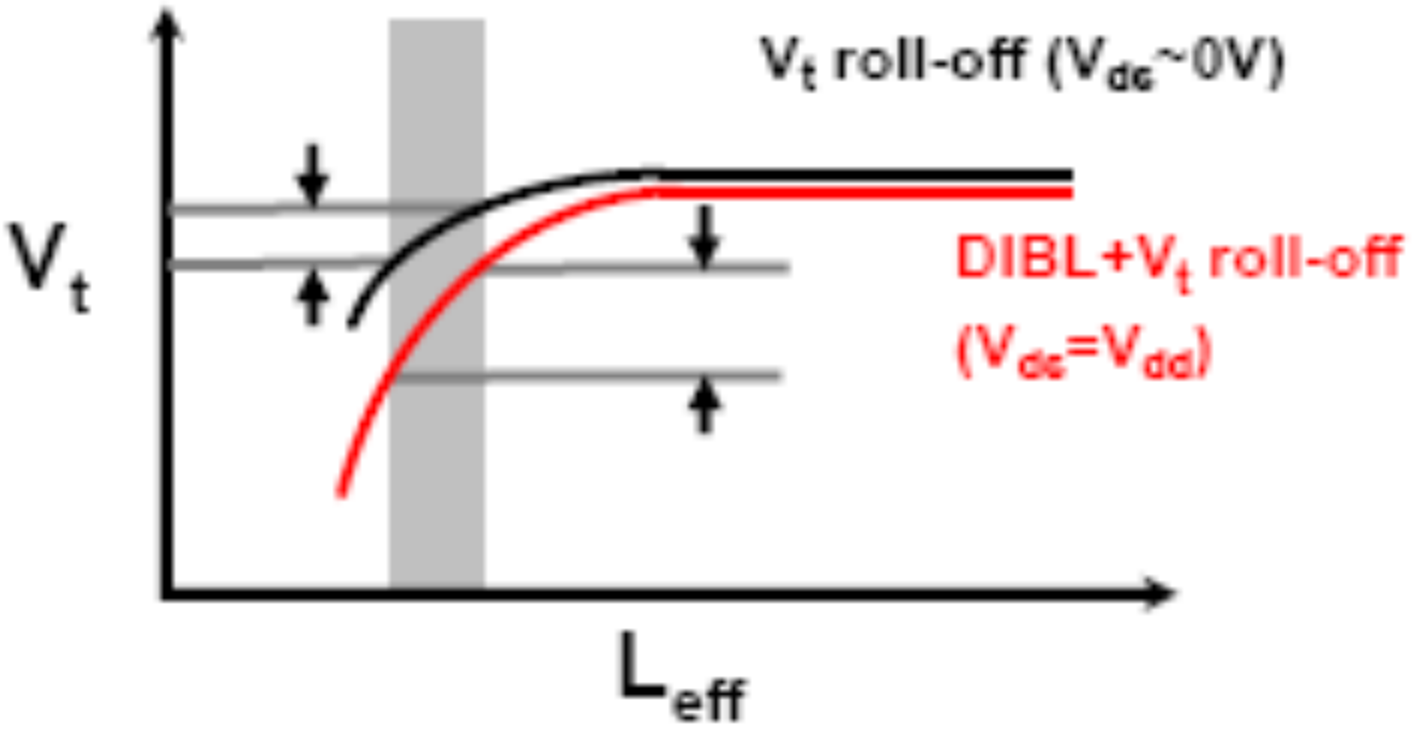


- 3σ V_t variation increases in short channel devices

The threshold voltage at short channel lengths can no longer be controlled.

Drain-induced Barrier Lowering (DIBL)

Short Channel Effect: Drain Induced Barrier Lowering (DIBL)



Uncertainty for Circuit Design !

$V_T(V_{BS})$ in Short-Channel Transistor

We have dealt before (MOS Capacitor Section) with substrate bias dependence on V_T in MOS capacitor.

$$\Delta V_T = \frac{\sqrt{2\varepsilon_S q N_A}}{C_{ox}}\left(\sqrt{2\psi_B + V_{BS}} - \sqrt{2\psi_B}\right)$$

In short-channel MOSFET, however, the effect of V_{bs} on V_T is not well modeled by this expression. For large V_{BS} V_T is less sensitive to V_{BS} than predicted by the above equation (see Figure)

$$V_T = V_{FB} + 2\psi_B + \gamma\sqrt{2\psi_B + V_{bs}}$$

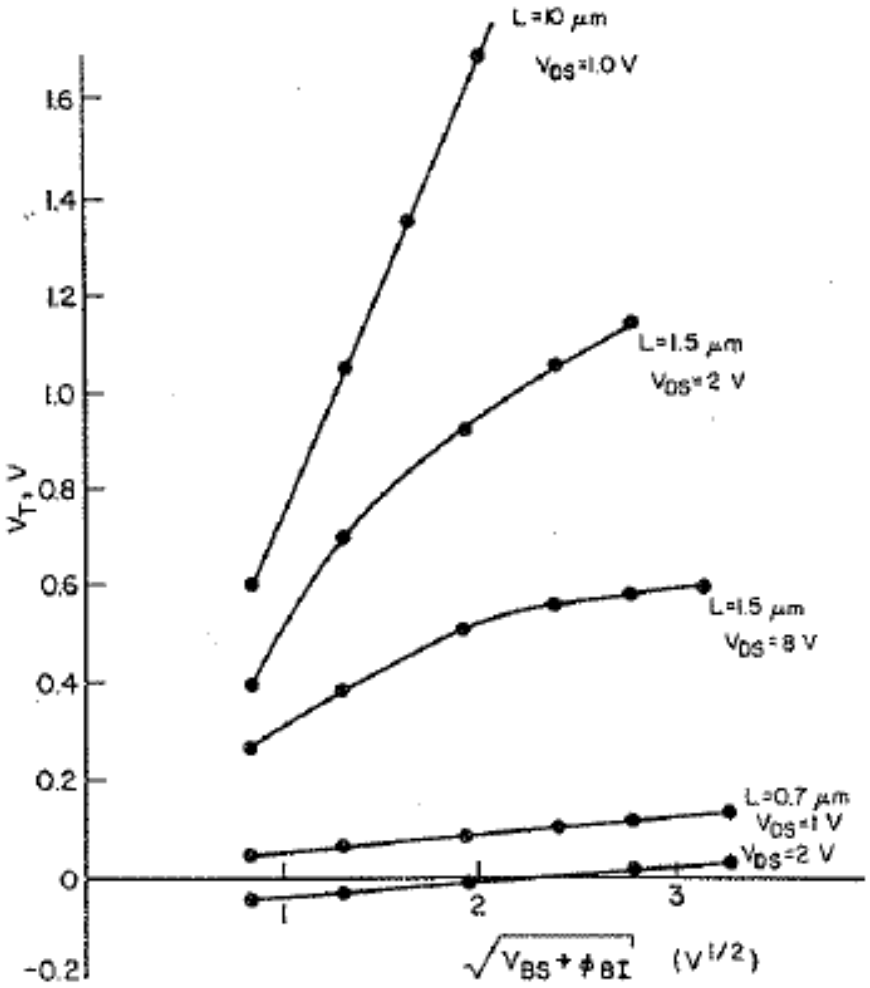


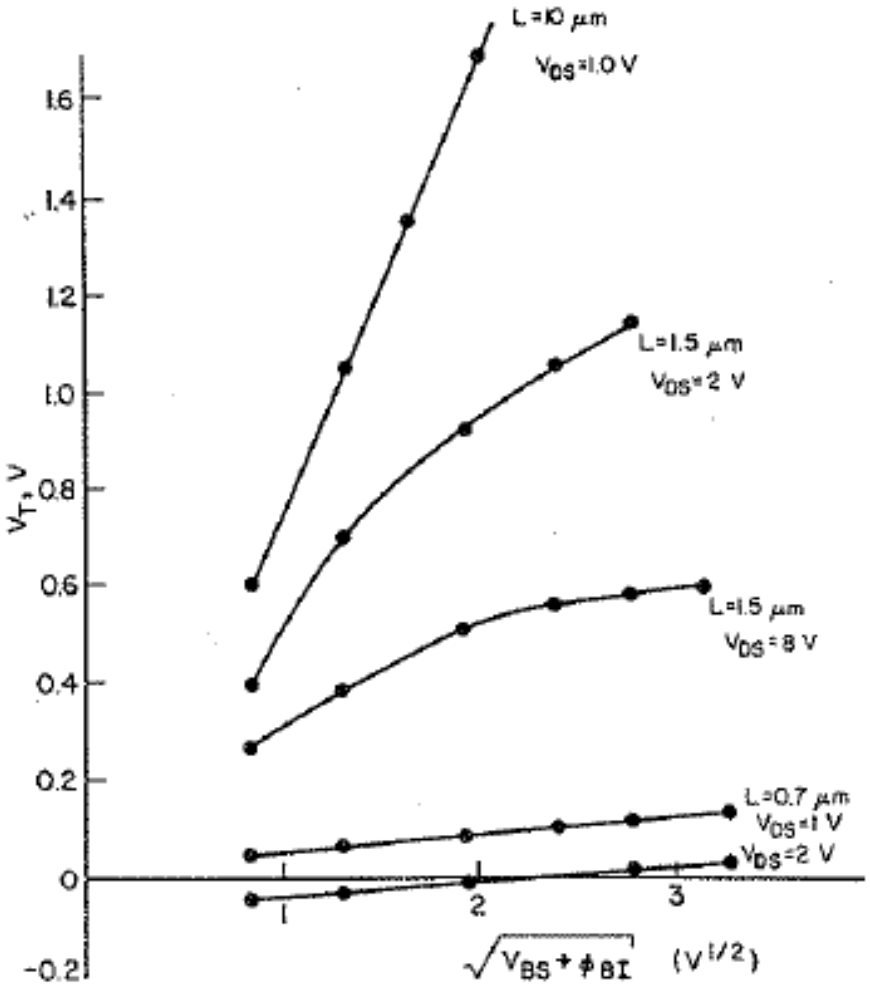
Fig. 5-12 Variation of V_T versus V_{BS} for three different channel lengths: $L = 10\ \mu m$ (long channel); $L = 1.5\ \mu m$ (short channel); $L = 0.7\ \mu m$ (punched through at $V_{BS} = 0V$). $N_A = 10^{15}$ cm^{-3}, $t_{ox} = 1000Å$; $r_j = 1\ \mu m$.[10] Reprinted with permission of *Solid-State Electronics*.

$V_T(V_{sub})$ in Short-Channel Transistor

It can be seen that for L=1.5 um and V_{ds}=8V, V_T becomes almost independent of V_{bs} for large V_{bs}. At L=0.7 μm V_T becomes independent for V_{bs} for all V_{bs}. Substrate tends to lose control over the channel region (just as does the gate itself) at shorter channel lengths.

The break in the slope of the L=1.5 μm curves occurs with punch-through of the depletion regions of the source and drain. This is because punch-through decouples the edge of the depletion region from the gate, thereby decoupling the channel from the substrate.

This effect can be described by using a smaller body effect coefficient γ.



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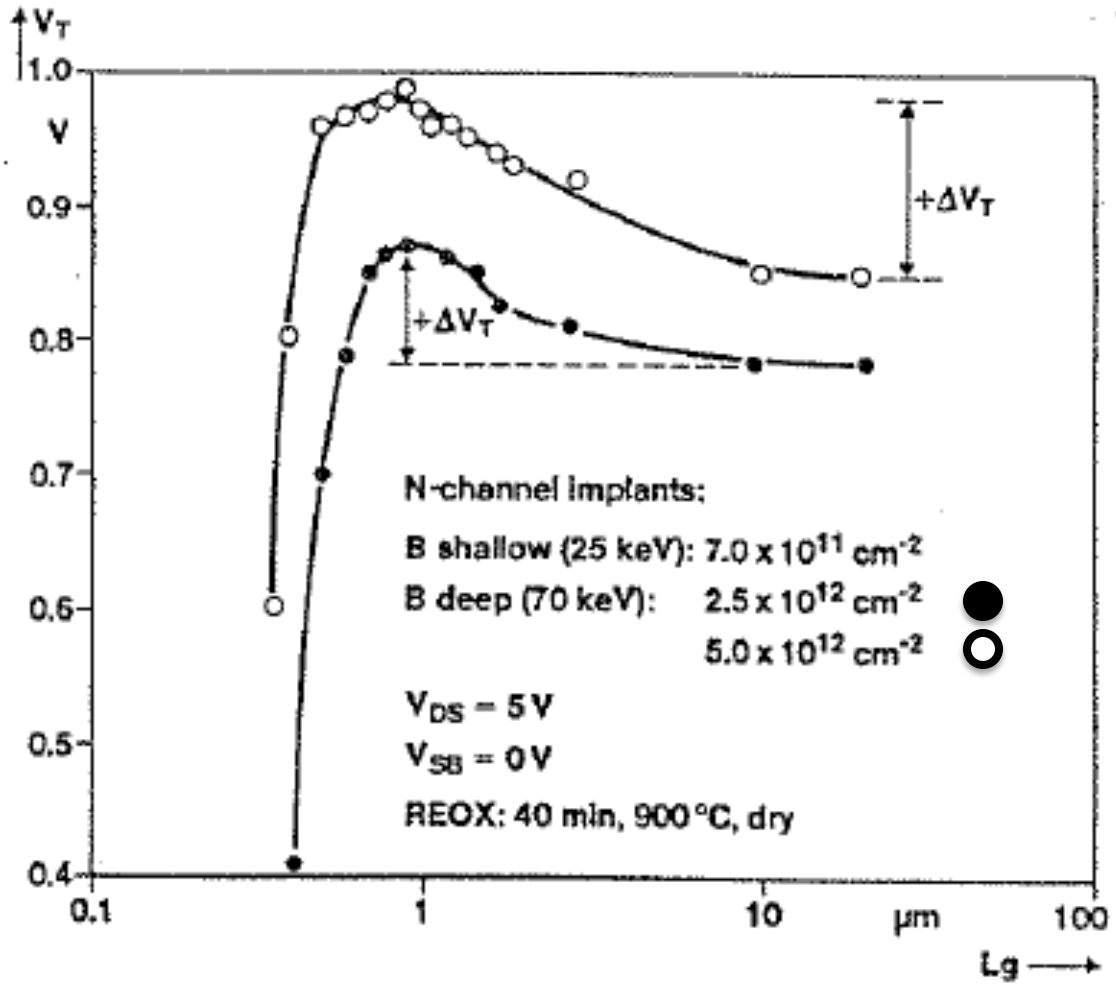
Reverse Short Channel Effect

In deep submicron technologies a new short channel effect has been observed: the Reverse Short Channel Effect shown below:

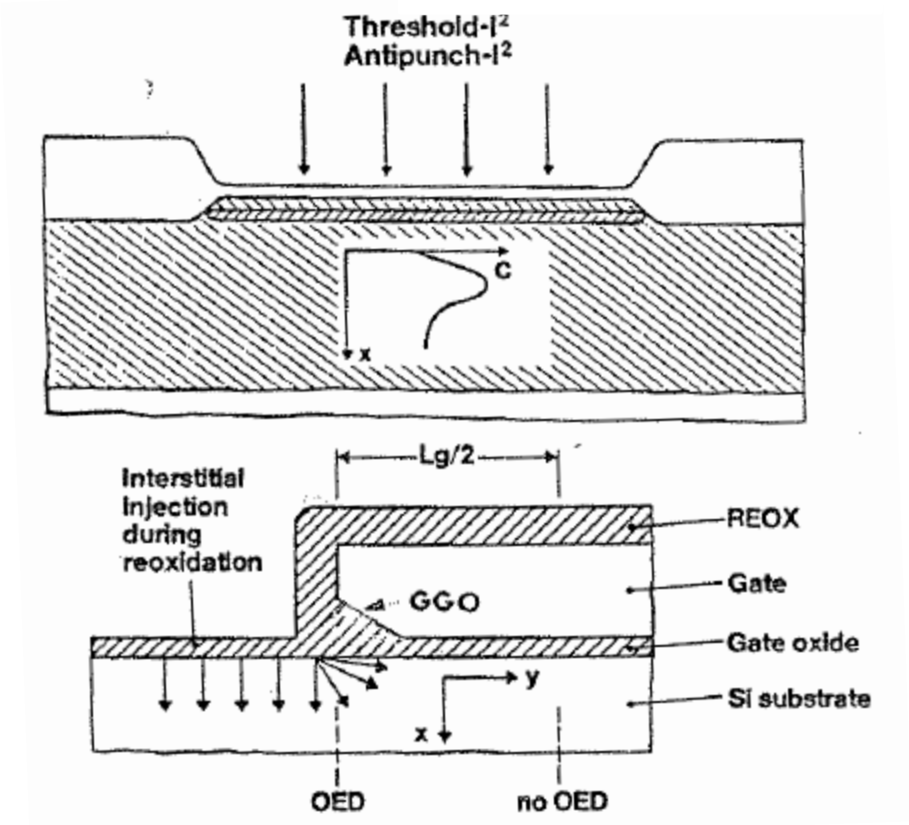


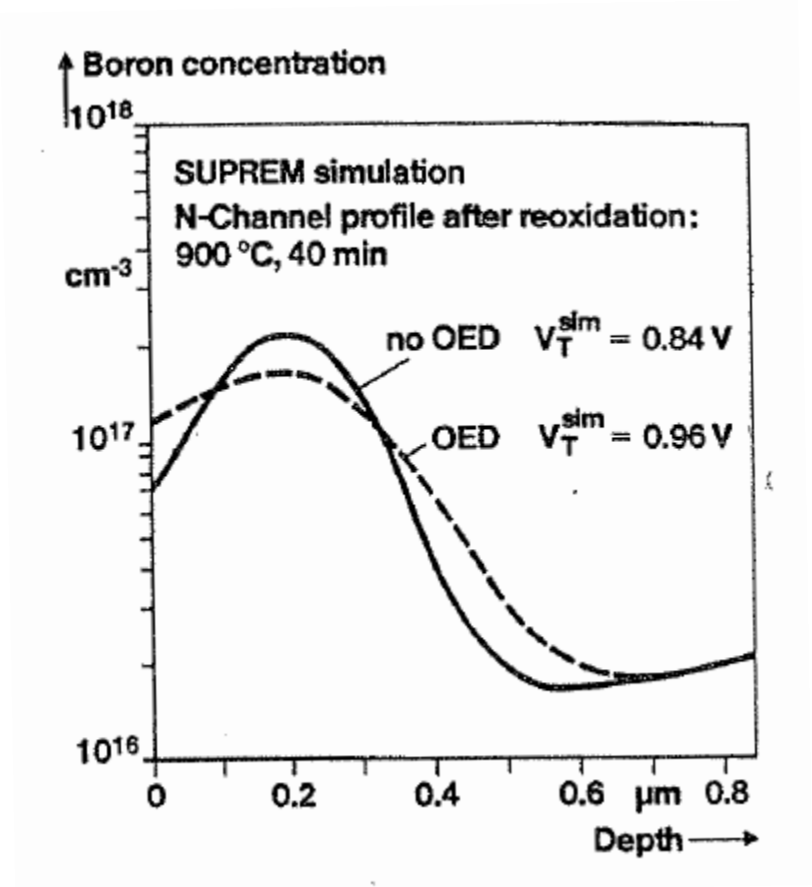
Experimental *n*-channel threshold voltage versus channel length.[92]

[92] M.Orlowski et al,” Submicron short channel effects due to gate reoxidation induced lateral interstitial diffusion”, IEDM 1987, p.632-635

Reverse Short Channel Effect

Reverse short channel effect depends on inhomogeneous channel doping redistribution. The inhomogenoeus dopant redistribution is driven by point defect injection from various sources. Point defects are the vehicles for dopant diffusion.





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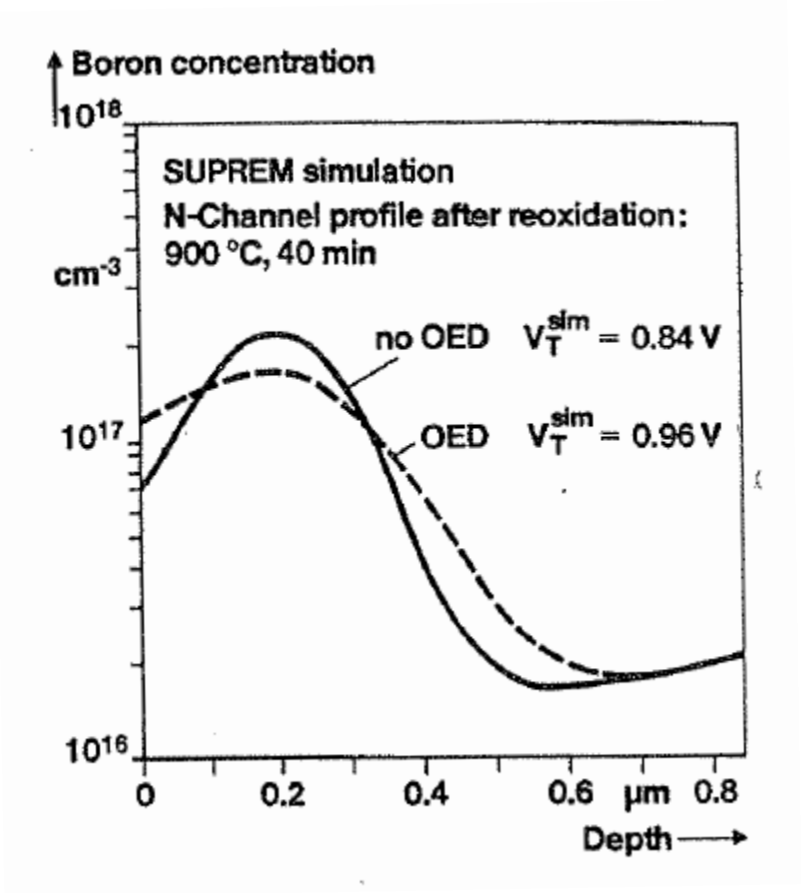
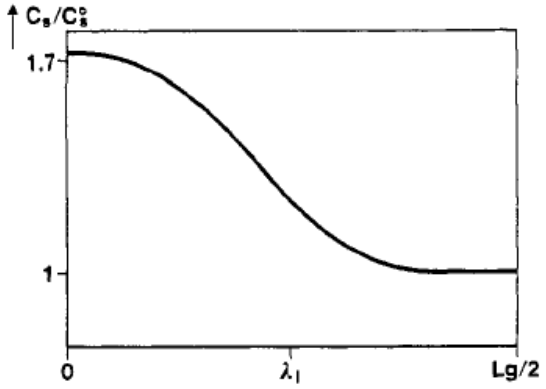
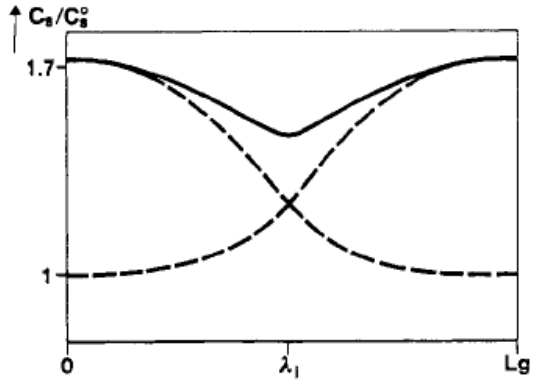




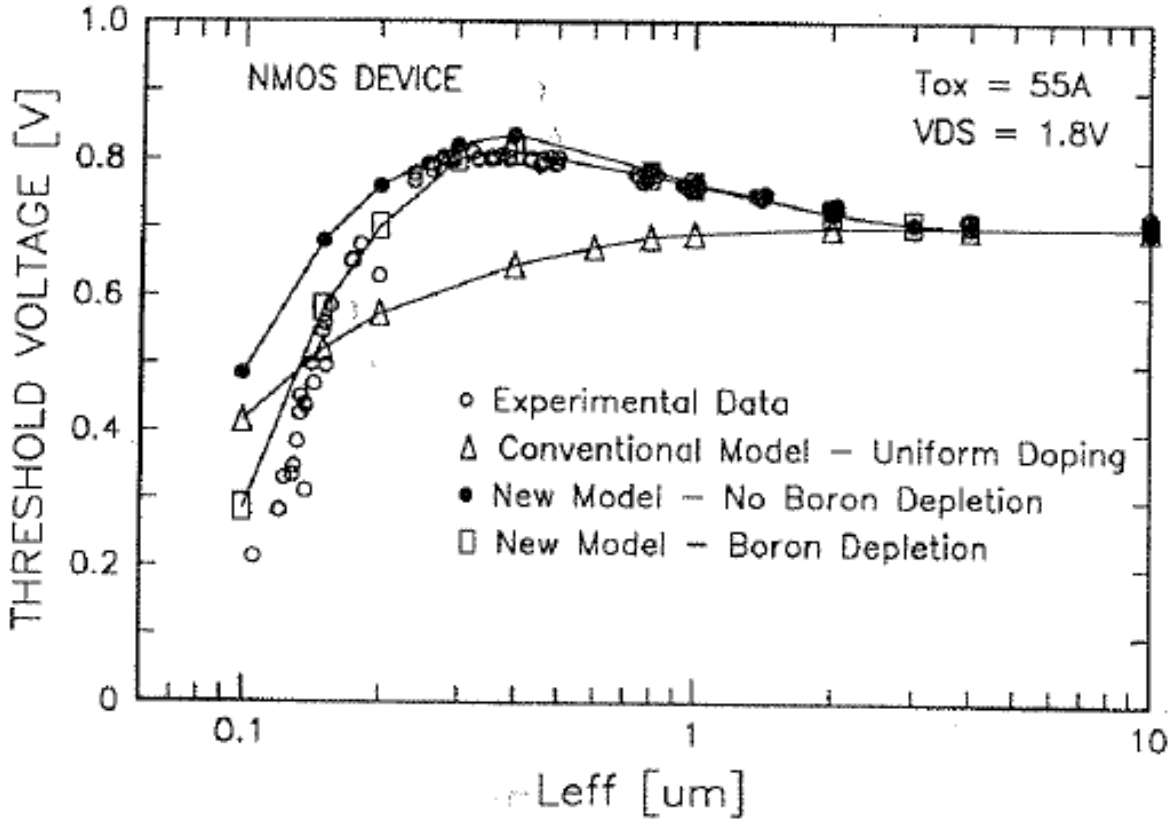
Short channel case: $Lg \lesssim 2 \times \lambda_i$



. 6 Schematic lateral channel surface concentration for a) long channel and b) short channel case.

[92] M.Orlowski et al,” Submicron short channel effects due to gate reoxidation induced lateral interstitial diffusion” , IEDM 1987, p.632-635

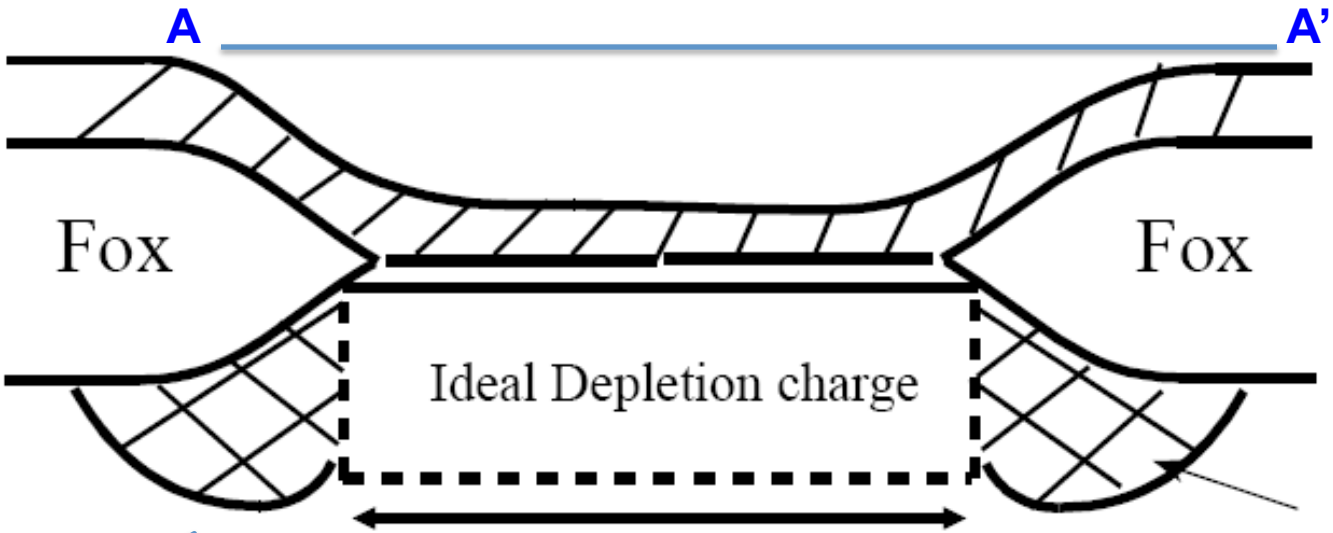
Reverse Short Channel Effect



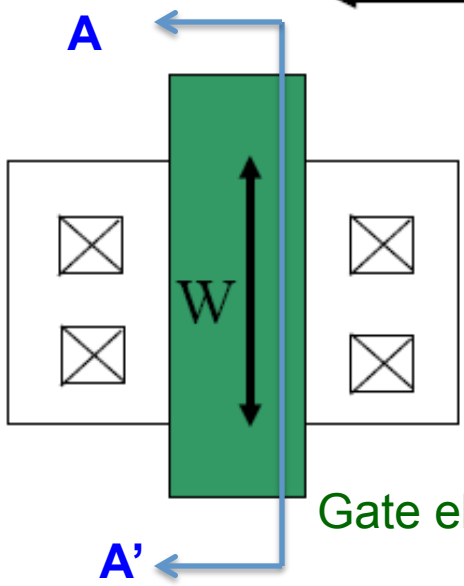
[92] M.Orlowski et al,” Submicron short channel effects due to gate reoxidation induced lateral interstitial diffusion”, IEDM 1987, p.632-635

Narrow Width Effects

Narrow Width Effect (related to W)



parasitic charge which has to be created by gate bias



$\therefore V_T$ is larger than ideal analysis.

Narrow Width Effects

In the short channel effect where a depletion region already exists at each pn junction requiring less voltage to be applied to invert channel. As demonstrated before, this leads to a *decrease* in V_T in short channel MOSFET.

However, at the ends of the channel perpendicular to the current flow, i.e. in the width dimension, no pn junction exists (along the width dimension). Hence, a gate bias that repels majority carriers must not only deplete carriers in the channel in the vertical direction, but also in the lateral direction beyond the thin gate oxide. Because the lateral depletion region width in this region extends beyond the gate, an effective bulk charge width larger than the actual width is apparently present.

If the width W is small, these side regions represent a large percentage of the depleted volume. Hence, larger V_{gs} must be applied to invert the channel than if these edge regions did not have to be depleted. This leads to an *increase* in V_T.

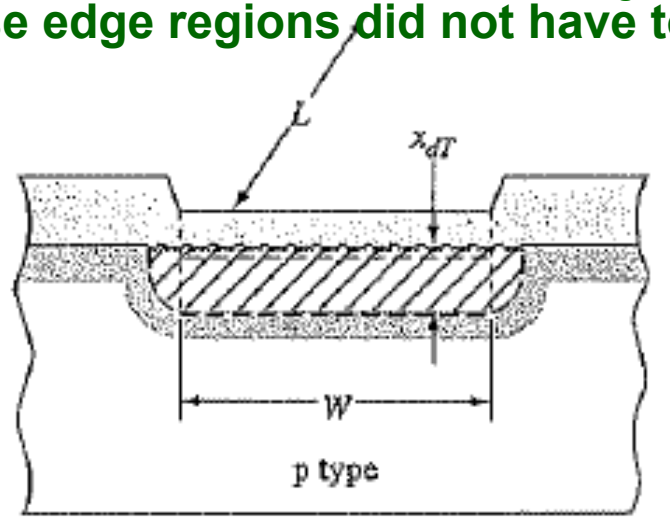


Figure 12.18 | Cross section of an n-channel MOSFET showing the depletion region along the width of the device.

Narrow Width Effects

Figure to the right shows cross section along the channel width of a MOSFET biased at inversion. The current is perpendicular to the channel width. We note that there is an additional space charge region at each end of the channel width. This additional charge is controlled by the gate voltage but was not included in the derivation of the ideal MOS capacitor. The expression for V_T has to be therefore modified to include this additional charge.

For the gate-controlled bulk charge we can write:

$$Q_B = Q_{Bo} + \Delta Q_B$$

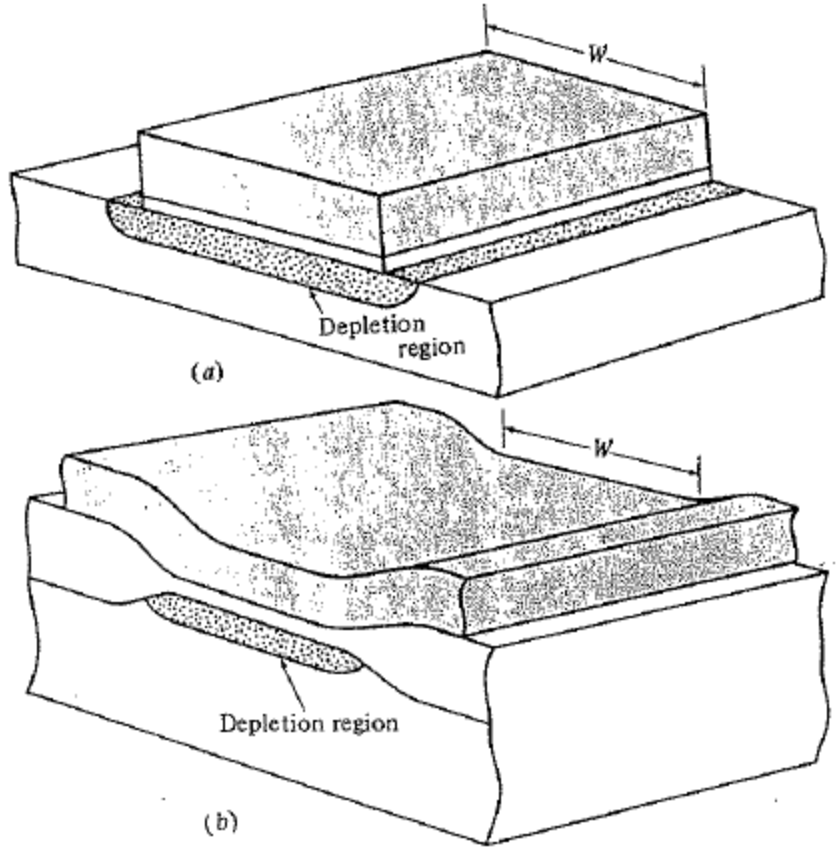


Fig. 5-13 Effect of fringing field on spreading the depletion region sideways. (a) In MOSFET with field oxide grown and then etched to expose the active region. (b) In MOSFET having a semirecessed LOCOS field oxide. From Y.P Tsividis, *Operation and Modeling of the MOS Transistor*, McGraw-Hill, New York, 1987, p. 192. Reprinted with permission.

$$Q_B = Q_{Bo} + \Delta Q_B$$

Narrow Width Effects

Where Q_B is the total bulk charge, Q_{Bo} is the ideal bulk charge, and ΔQ_B is the additional bulk charge at the ends of the channel width. For a uniformly doped p-type substrate at the inversion onset we have

$$\left|Q_{Bo}\right| = qN_A L \cdot x_{dT} \cdot W$$

$$\Delta Q_B = qN_A L \cdot x_{dT} \cdot (\xi \cdot x_{dT})$$

where we have replaced W by ξx_{dT}. Here ξ is a dimensionless fitting parameter that accounts for the lateral space charge width. Note that the lateral charge width may not be the same as the vertical width x_{dT}.

We may write now

$$\left|Q_B\right| = \left|Q_{B0}\right| + \left|\Delta Q_{B0}\right| = qN_A L x_{dT} \cdot W + qN_A L x_{dT} \cdot (\xi \cdot x_{dT})$$

$$= qN_A L x_{dT} \cdot W\left(1 + \frac{\xi \cdot x_{dT}}{W}\right)$$

Narrow Width Effects

The effect of the end space charge regions becomes significant as the width decreases and the distance ξx_{dT} becomes a significant fraction of the width W. The change of V_T due to the additional space charge is

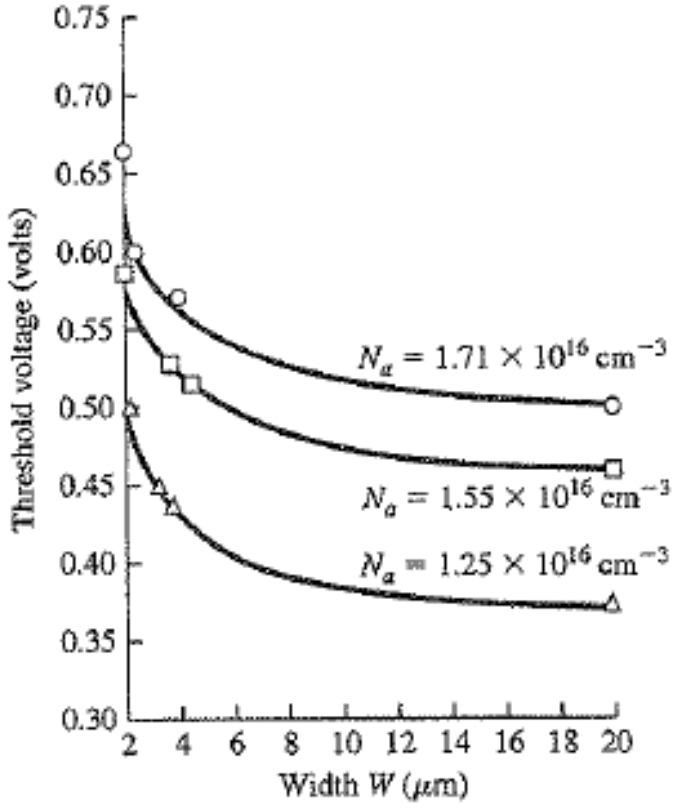


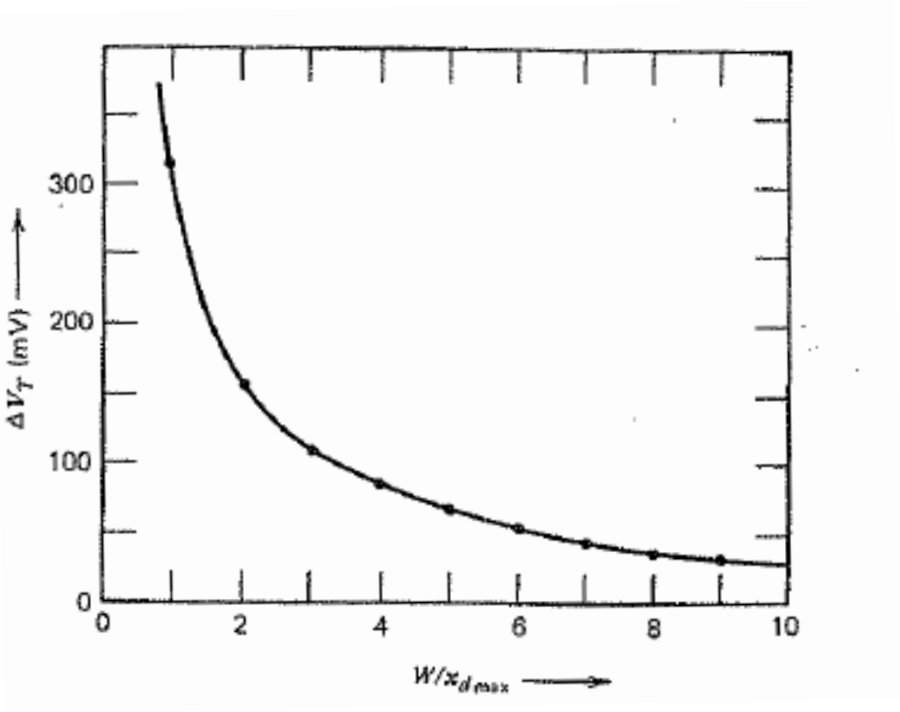
Figure 12.19 | Threshold voltage versus channel width (solid curves, theoretical; points, experimental).

$$\Delta V_T = \frac{qN_A x_{dT}}{C_{ox}} \cdot \left(\frac{\xi \cdot x_{dT}}{W} \right)$$

The V_T shift due to narrow width is in positive direction: as W becomes smaller, the V_T becomes larger.

Combination of the short L and narrow W requires 3D analysis (simulation).

Narrow Width Effects in terms of dimensionless variable x_{dT}/W

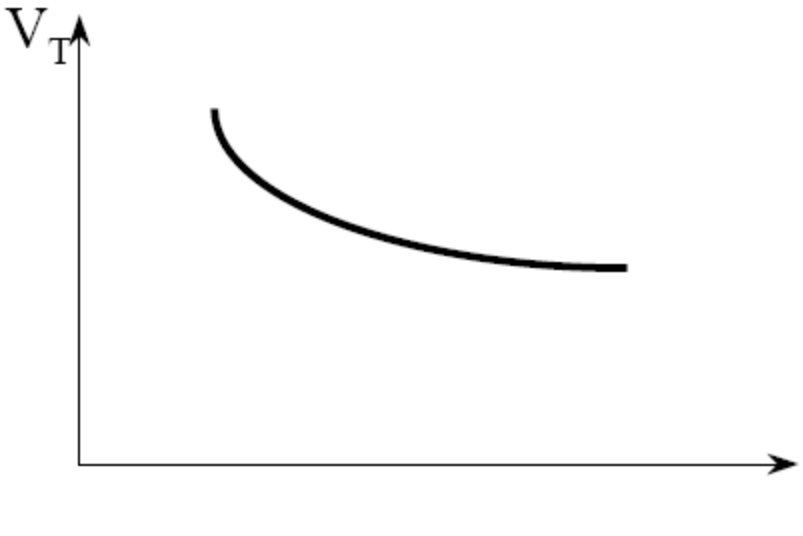


$$V_{T0}(\text{narrow channel}) = V_{T0} + \Delta V_{T0}$$

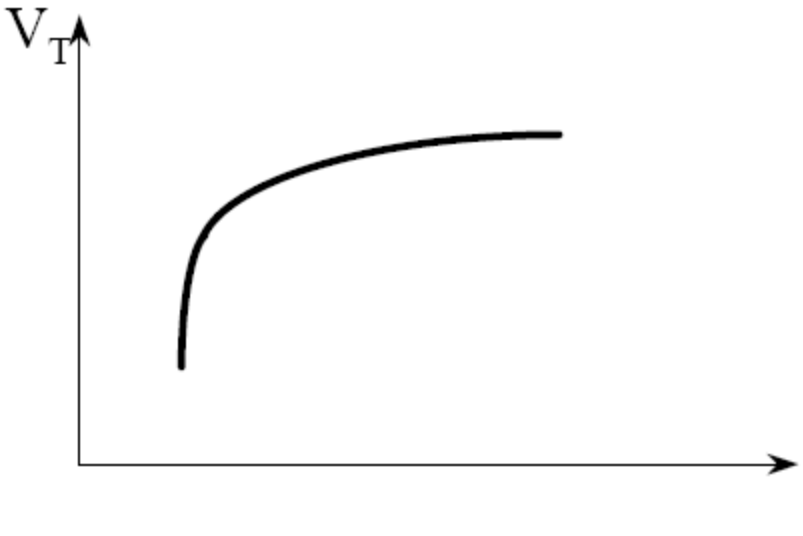
$$\Delta V_{T0} = \frac{1}{C_{ox}}\sqrt{2q\varepsilon_{Si}N_A|2\phi_F|} \bullet \frac{\xi x_{dT}}{W}$$

- ξ is empirical parameter: depends on shape of the fringe depletion region
- Change in V_{T0} proportional to $\frac{\xi x_{dT}}{W}$

Narrow Width and Short Channel Effects Juxtaposed



Narrow Width Effect

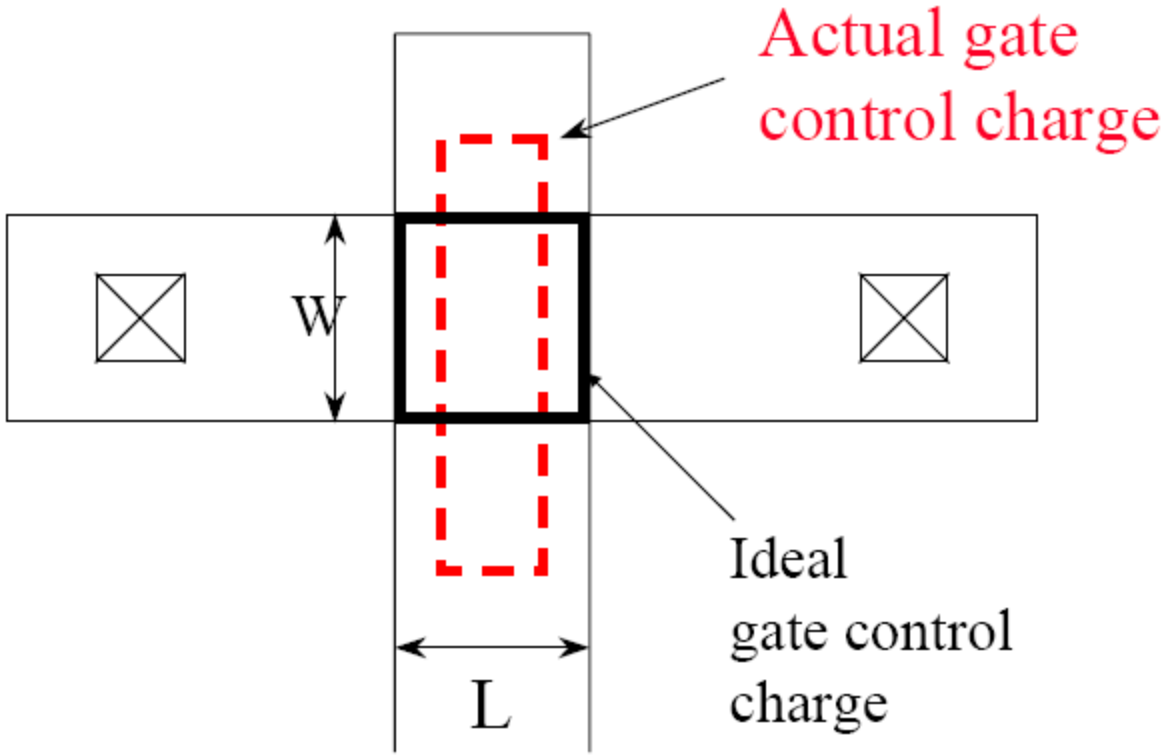


Short or

Narrow Channel Effect

Narrow Width and Short Channel Effects Juxtaposed

Small Geometry Effects Summary



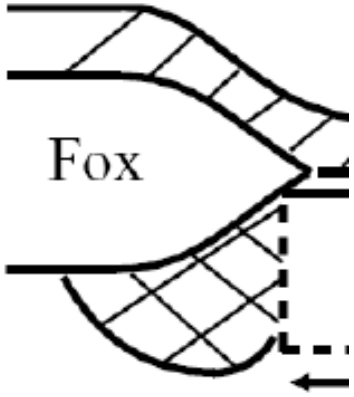
- Less charges in the length dimension
- More charges in the width direction

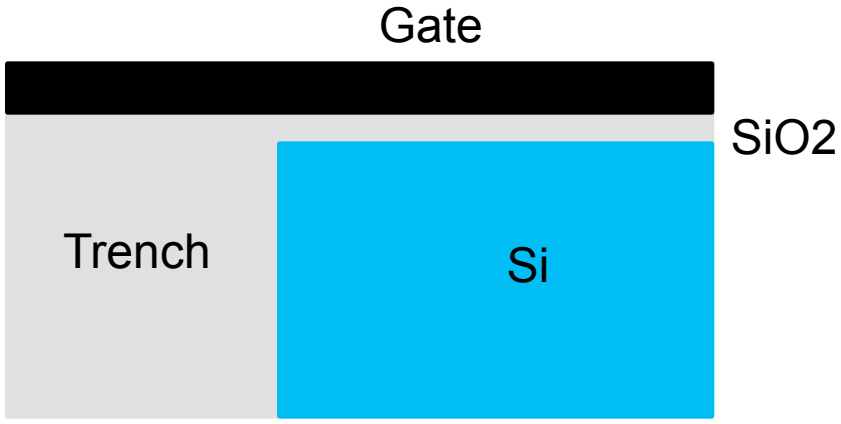
Inverse Narrow Width Effect

Because this particular type of width effect decreases the V_T, the effect is called inverse (not reverse as in the case of the channel effect) narrow-width effect. It occurs for transistors with trench isolation (or with fully recessed LOCOS isolation structures). Note that the width effect described before does not occur in trench isolation structures, since there is no semiconductor region beyond the edges of the gate in the width dimension, there is no region that is subject to depletion.

When the gate is biased, the field lines from the overlapping region are focused on the edge of the channel. Hence, at the edges of the channel, an inversion layer is formed at lower voltages than at the center. As a result, less bias overall must be applied to the gate to invert the channel across its full width.

LOCOS



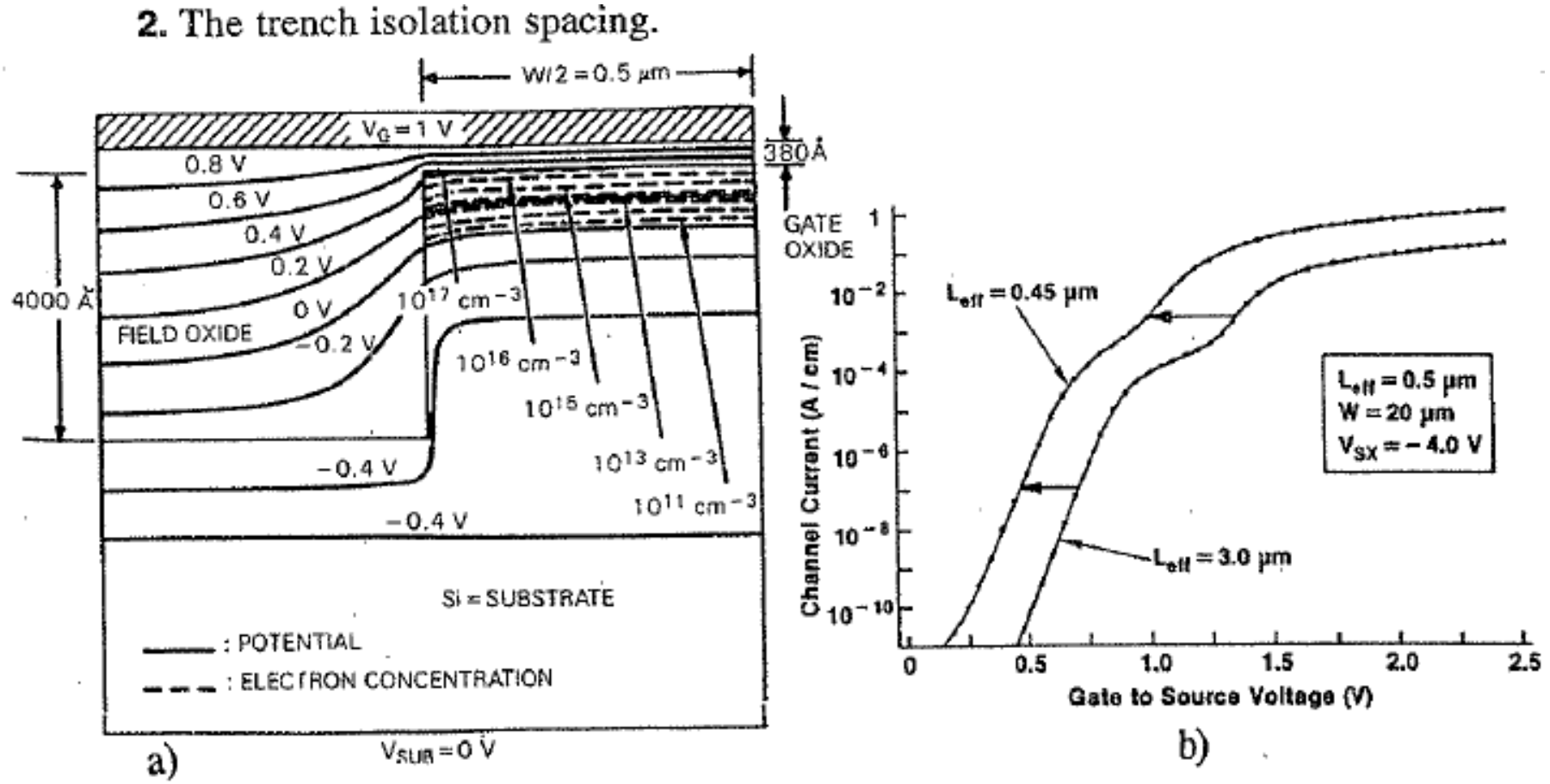


Comparison LOCOS and TRENCH isolation.

Inverse Narrow Width Effect

From another perspective, a corner parasitic MOSFET in parallel with the main device is being established. The parasitic device turns on at voltages lower that the main device, resulting in a "hump" in the drain current versus gate voltage curves.

Thus, the parasitic device increases the subthreshold leakage current of the active device.



Hot Carrier Effects

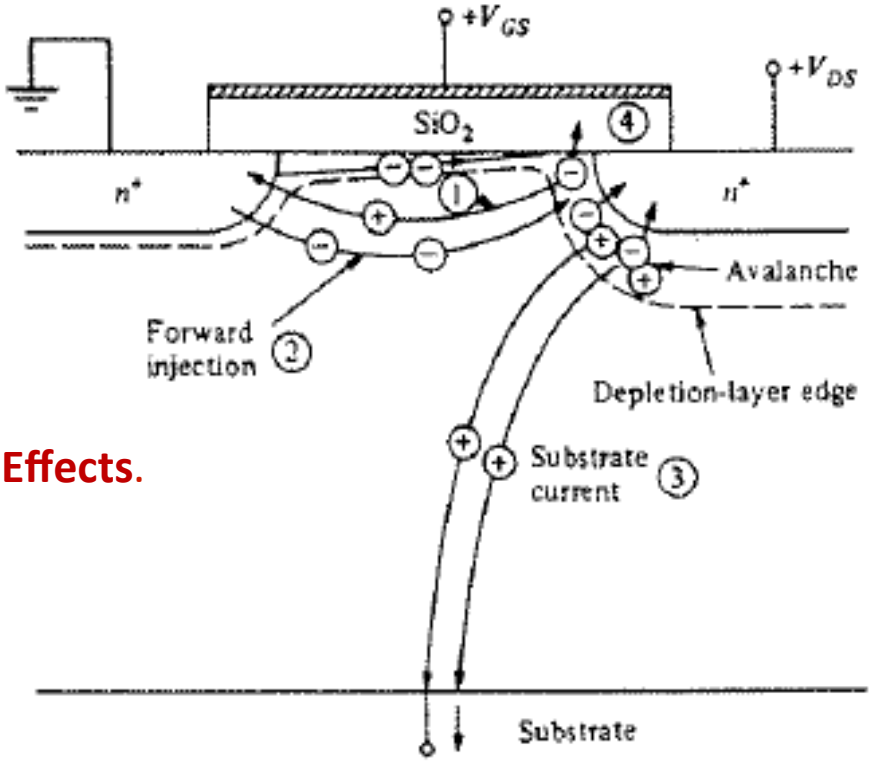
- As feature size decreases, at constant voltage bias electric field in channel region increases which leads to gain high kinetic energy by holes & electron (hot carriers) .

- High kinetic energy enables injection into the gate oxide and formation of interface states , which in turns causes degradation of circuit performance.

- Hot carriers are also the origin of substrate and gate currents.

What does "Hot" mean?
electron energy:
E=26 meV for T=300K

E=1 eV for T=1.2 10^4 K



- All these effects are called **Hot Carrier Effects**.

Hot Carrier Effects driven by high Electric Fields

$$E_{y\max} = (V_{ds} - V_{dssat})/l$$

Channel length
L dependence

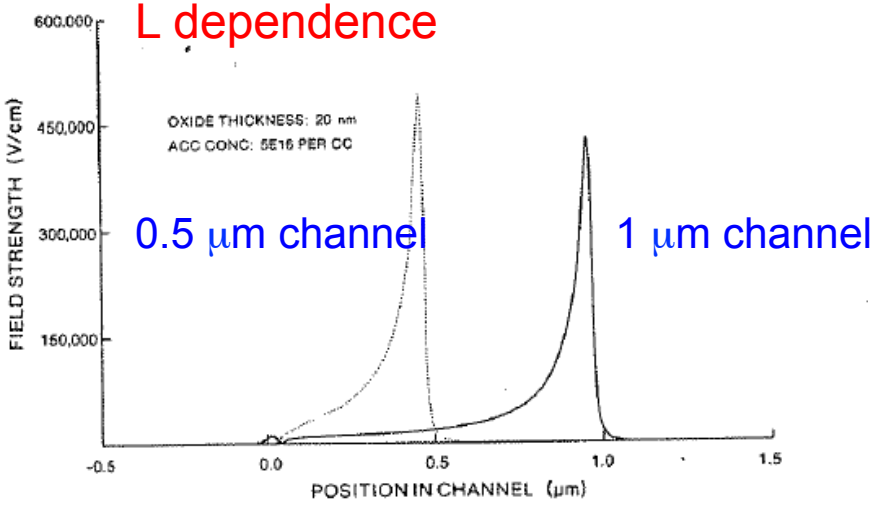


Fig. 9-2 $\mathcal{E}_y$ within an NMOSFET as a function of channel length for two devices with channel lengths of 1.0 μm and 0.5 μm, and the same value of t_{ox} = 20 nm.[146]

Oxide thickness
t_{ox} dependence

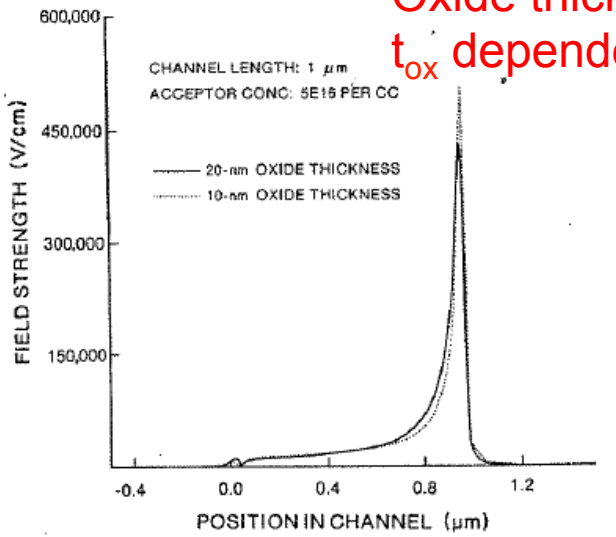


Fig. 9-3 $\mathcal{E}_y$ within an NMOSFET as a function of channel length and gate oxide thickness for two devices with a channel length (1.0 μm) and two values of t_{ox}, 10 and 20 nm.[146]

Empirical formulae for the width of the electrical field peak at the drain

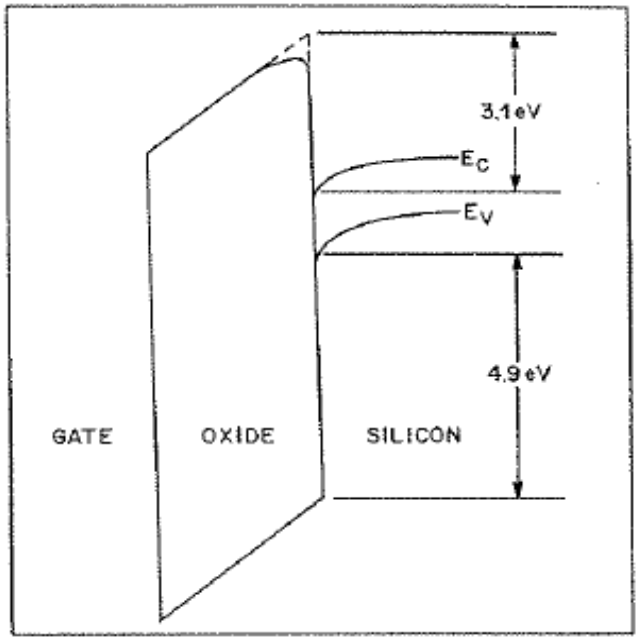
$$l = 0.22 \cdot t_{ox}^{1/3} r_j^{1/2} \quad for \quad t_{ox} \geq 15nm$$

r_j is the s/d junction depth

$$l = 1.7 \cdot 10^{-2} \cdot t_{ox}^{1/8} r_j^{1/3} L^{1/5} \quad for \quad t_{ox} < 15nm \ and \ L < 0.5\mu m$$

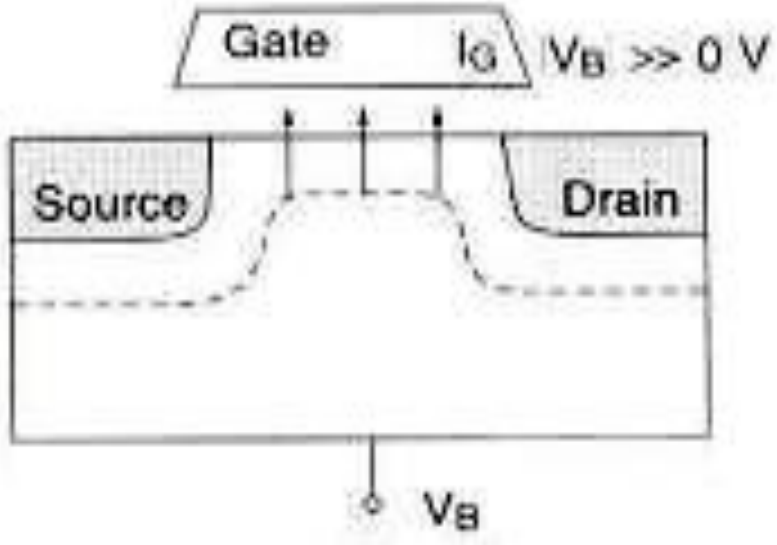
Different type of Hot carrier Injection

- Drain Avalanche Hot carrier (DAHC) Injection
- Channel Hot Electron (CHE) Injection
- Substrate Hot Electron (SHE) Injection
- Secondary generated hot electron (SGHE) injection



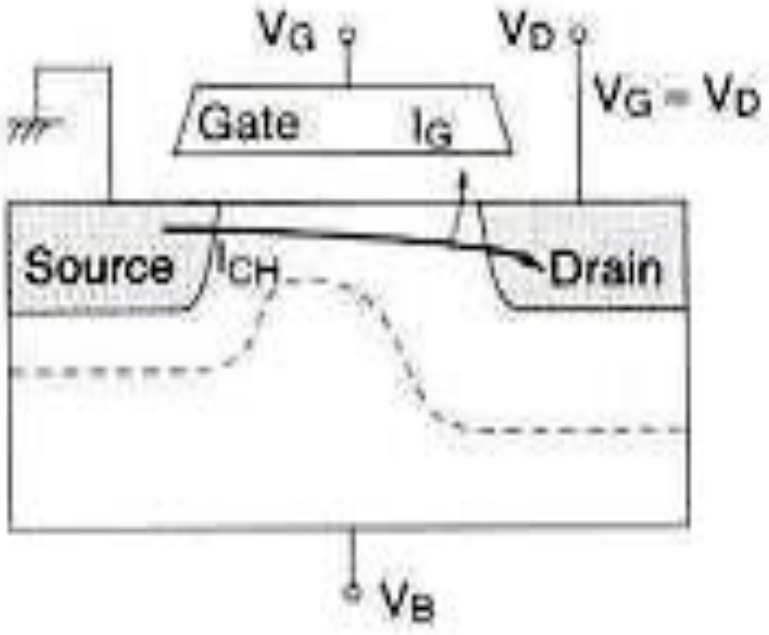
Substrate Hot Electron (SHE) Injection

- Occurs when the substrate back bias is very positive or very negative
- Carriers of one type in the substrate are driven by the substrate field toward the Si-SiO_2 interface.
- Gain high kinetic energy from and are injected to SiO_2.



Channel Hot Electron (CHE) Injection

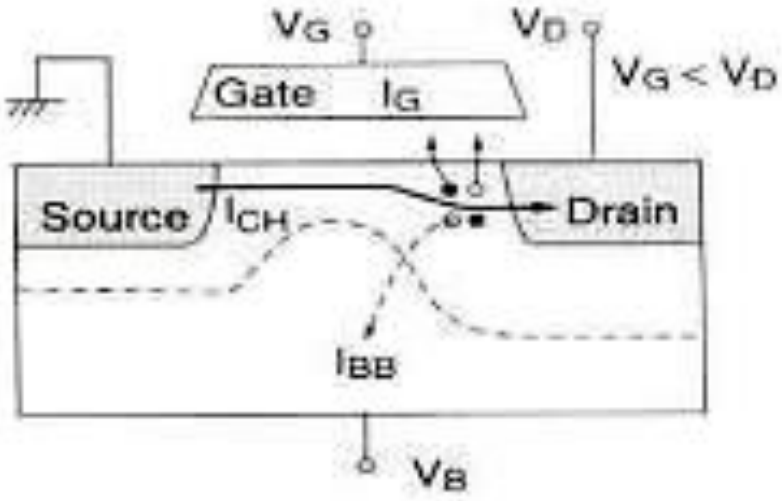
- When both $V_G = V_D$ higher than source voltage , some electrons are driven towards gate oxide



Drain Avalanche Hot carrier (DAHC) Injection

- When $V_D > V_G$, the acceleration of channel carrier causes Impact Ionization (avalanche).

- The generated electron – holes pair gain energy to break the barrier in Si-SiO_2 interface



Charge Generation inside SiO_2

- Negative charge generation
- Interface state (unsatisfied dangling bonds of Si) Q_i or D_{it} generation
- Positive charge generation

Hot Carriers

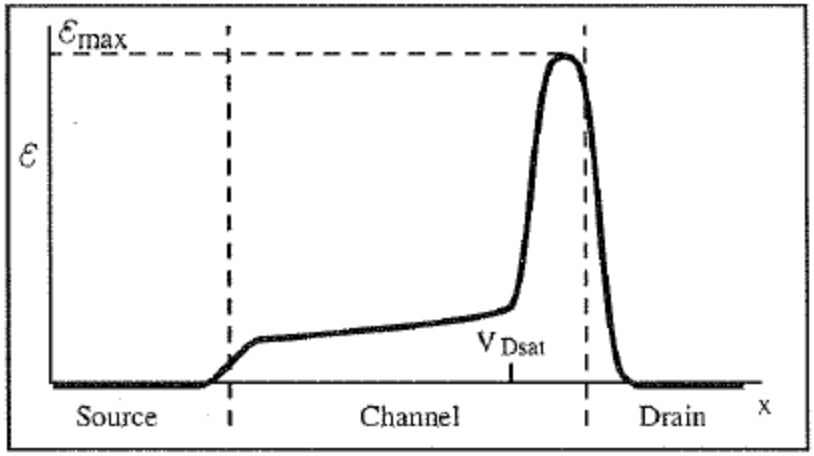


Figure 7.34: Lateral electric field, $\mathcal{E}$, at the surface of a MOSFET in saturation.[29]

In saturation regime electrons cross a very high lateral field region near the drain. They acquire high kinetic energy that they can cause impact ionization. Impact ionization leads to a high substrate current.

Highly energetic carriers create also permanent damage at the Si-SiO_2 interface and in the SiO_2. This damage alters the I-V characteristics of the MOSFET (degradation, reliability issue.
Some of the hot carriers may reach the gate and constitute gate current.

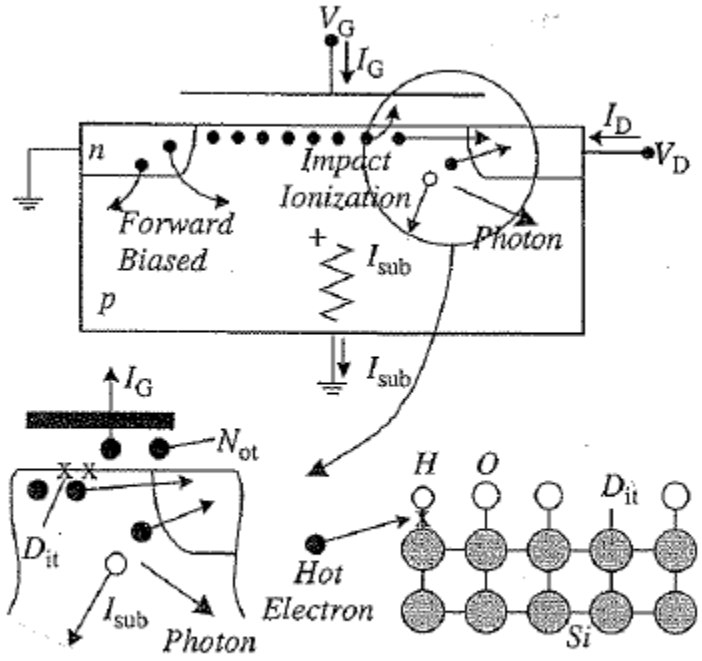


Fig. 12.8 Effect of hot electrons near the drain of MOSFETs.

Hot Carriers

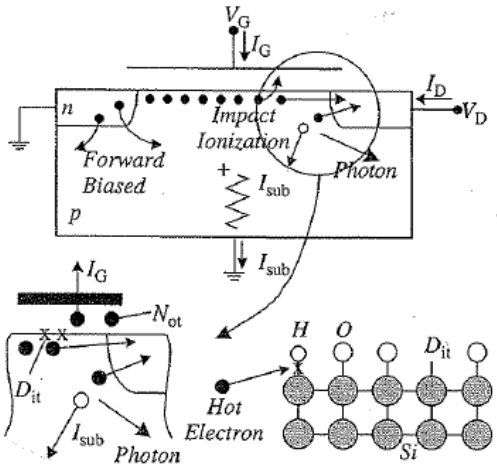


Fig. 12.8 Effect of hot electrons near the drain of MOSFE

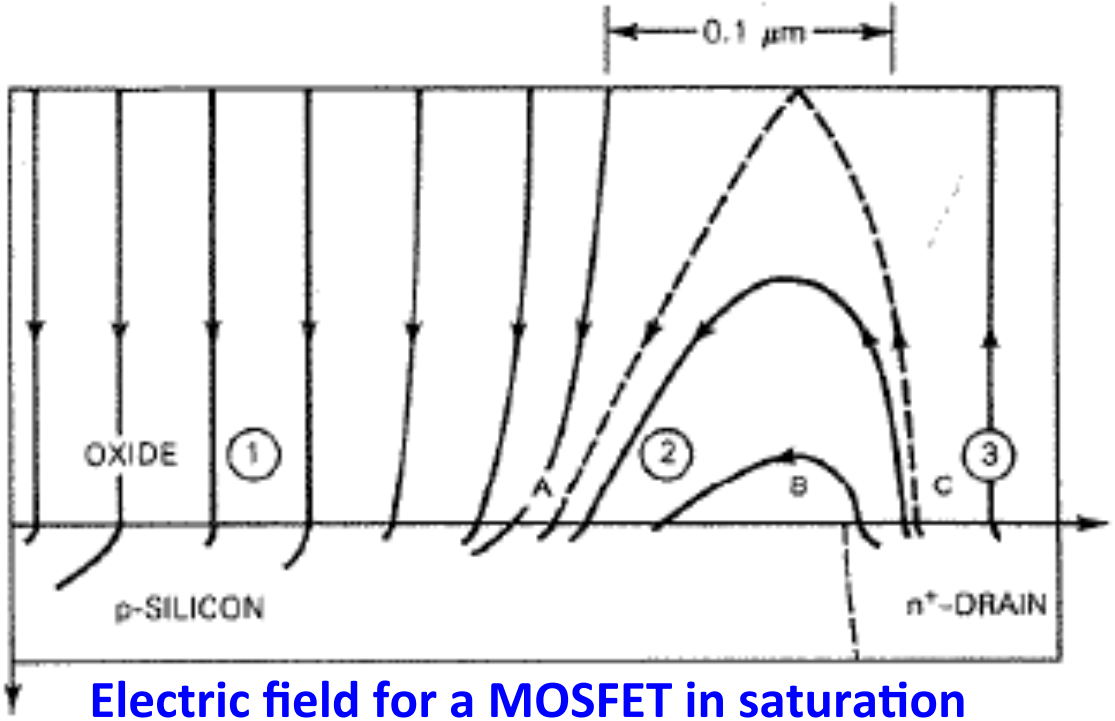
Electric field in the dielectric near the drain region determines the location of electron and hole injection into the oxide and into the gate.

Reversal of polarity of the vertical electric gate field :

Electrons are attracted by positive field

Hole are attracted by negative field

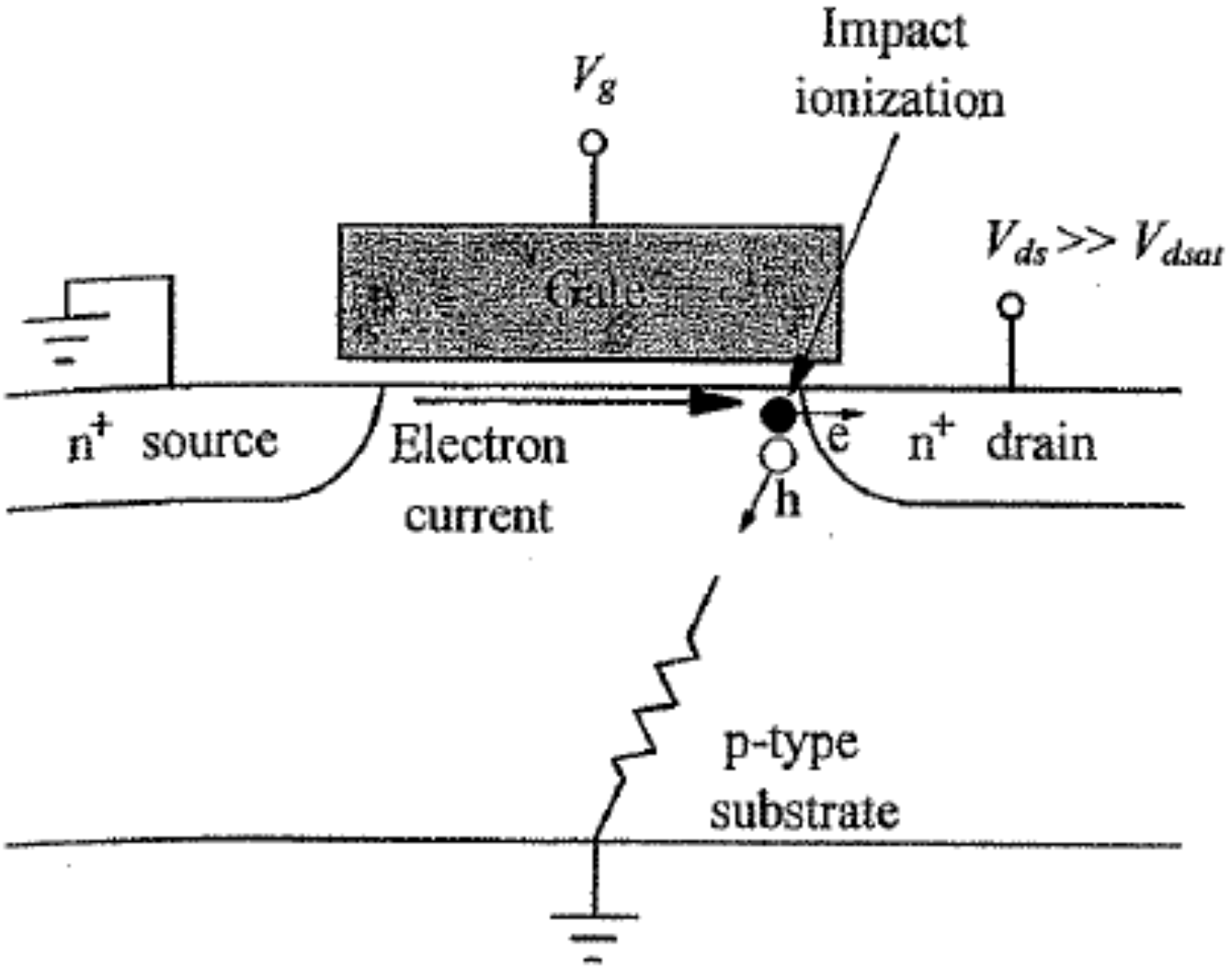
This determines the location of electron and hole injection



Electric field for a MOSFET in saturation

Figure 6.8 Two-dimensional electric field distribution near the drain of an *n*MOS. $V_d = 8$ V, $V_g = 7$ V, $V_B = -2.5$ V, $L_{eff} = 1.3$ μm and $t_{ox} = 400$ Å (Ref. 26, © 1984 IEEE).

Hot Electrons and Substrate Current



Hot Carriers and Substrate Current

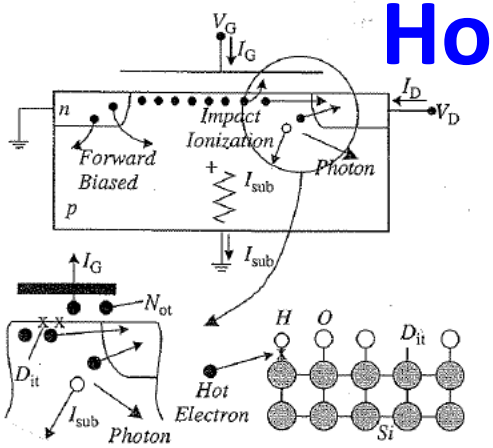
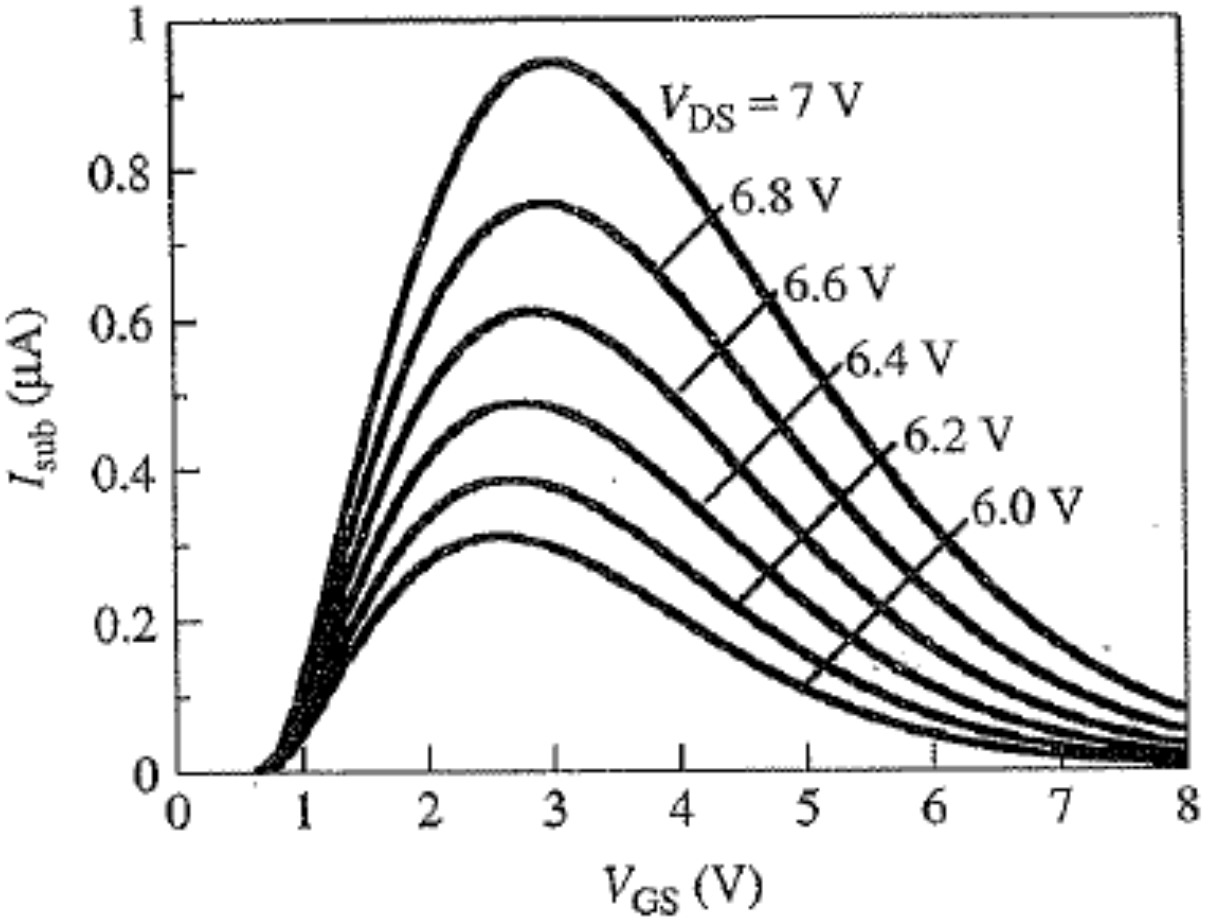


Fig. 12.8 Effect of hot electrons near the drain of MOSFETs.

The substrate current at a given drain bias, let say V_D=7V, increases first with the gate bias, because the current density increases. Note that the transistor operates in saturation regime and there is a high lateral field peak close to the drain where the impact ionization (II) is taking place. As the gate bias increases beyond the peak value the lateral electric field at the drain begins to decrease and consequently the impact ionization decreases as well.

For high impact ionization we need both a lot of carriers and a high electric field.



Substrate current dependence on drain and gate bias. Observe that the maximum of the substrate current takes place at about $V_{gs} \approx V_{ds}/3 - V_{ds}/2$.

Hot Carrier Effects

Hot carrier effects (including substrate current) are getting worse with scaling MOSFET to smaller dimensions because of increased local electric fields at the same voltages.

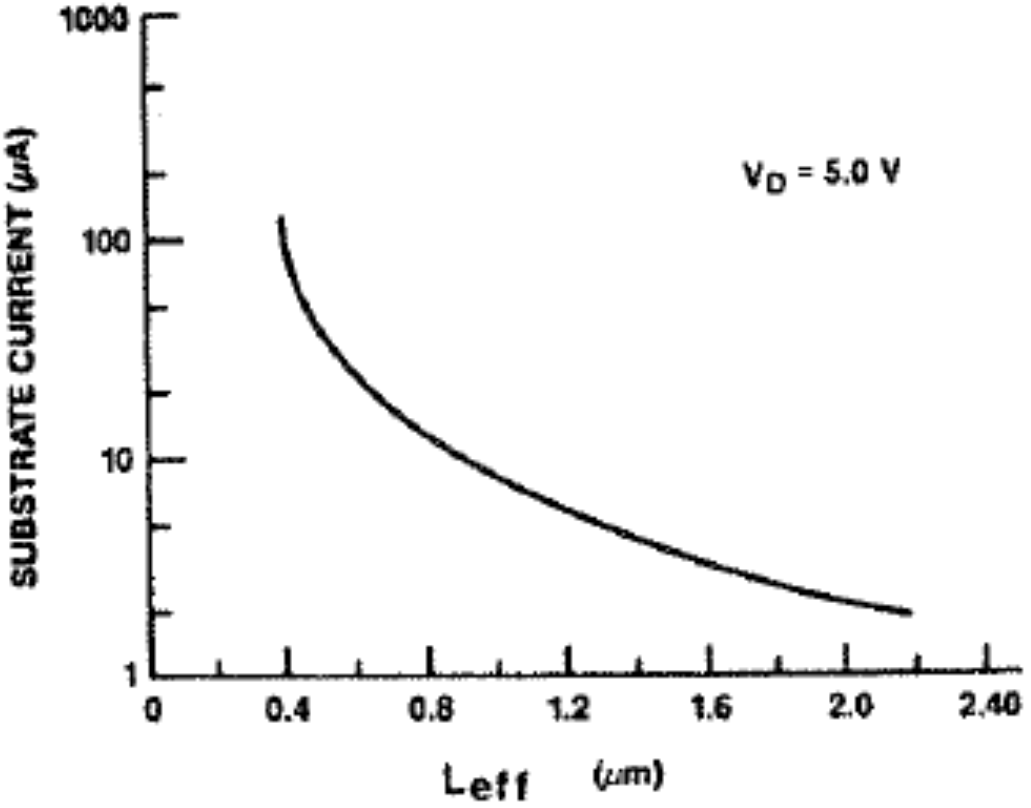
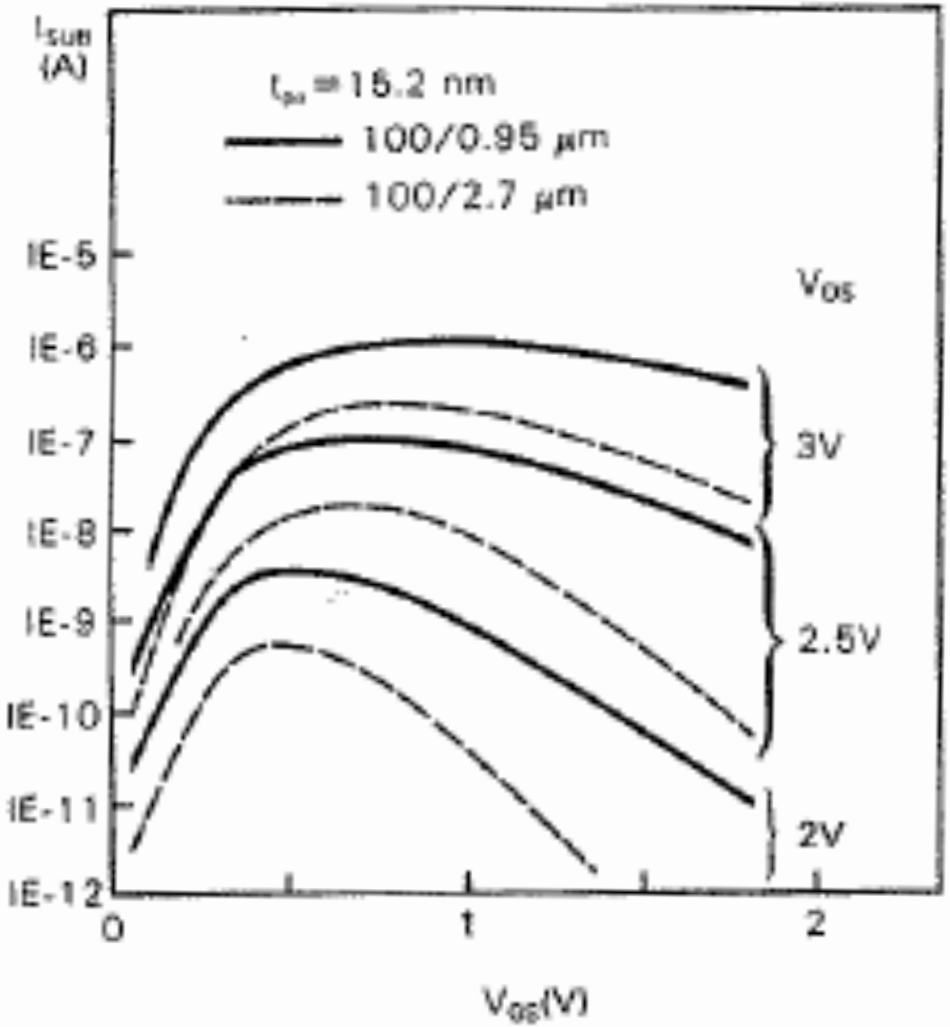


Fig. 9-4 The maximum substrate current due to impact ionization produced at a drain voltage of 5V vs. L_{eff} for MOSFETs with $t_{ox} = 250Å$.[6]

Hot Carriers and Substrate Current

Substrate current dependence on channel length: L=2.97 μm vs L=0.95 μm



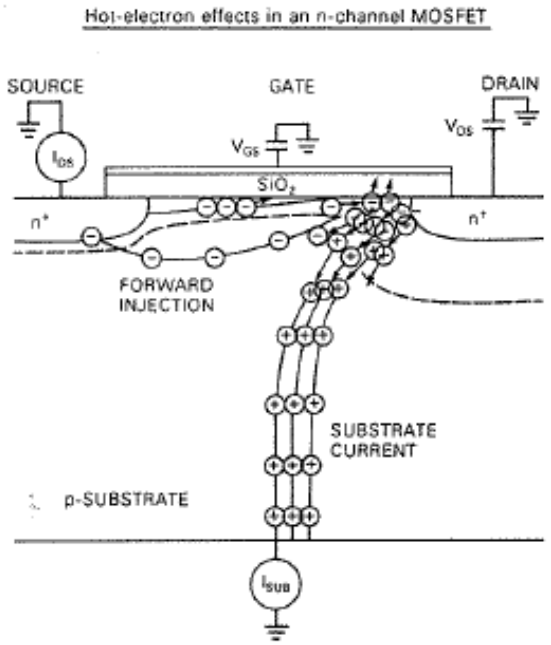
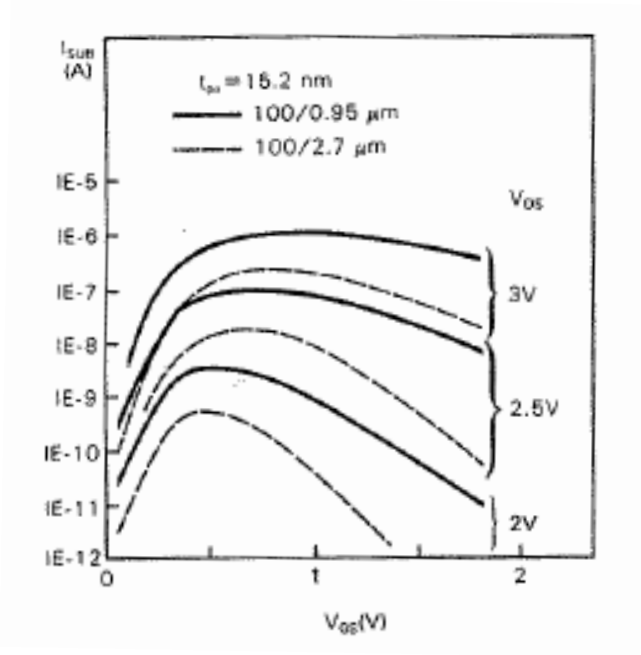


Figure 6.6 Schematic of hot-electron effects in an *n*-channel MOSFET.

Hot Carriers and Substrate Current and its Implications



Implications of excessive substrate current:

1) I_{sub} causes voltage drop in the resistive substrate on the order of 0.6V and forward biases the substrate-source junction. Electrons will then be injected from the source to the substrate. These electrons travel to drain and undergo impact ionization. A positive feedback loop is being established. It can lead to so called snapback breakdown.

2) The holes created in impact ionization travel back to the source and may undergo secondary impact ionization.

3) Latchup in CMOS circuits

Physics of the substrate current

$$I_{sub} \propto I_d$$

$$I_{sub} \propto \exp\left(-\frac{\Phi_i}{\lambda_e E_{y\max}}\right) = \exp\left(-\frac{\Phi_i}{kT_e}\right)$$

$$\rightarrow I_{sub} = C_1 I_d \exp\left(-\frac{\Phi_i}{\lambda_e E_{y\max}}\right)$$

$$E_{y\max} = (V_{ds} - V_{dssat})/l$$

$$l = 0.22 \cdot t_{ox}^{1/3} r_j^{1/2}$$

$$I_{sub} = C_1 I_d \exp\left(-\frac{0.22 \cdot t_{ox}^{1/3} r_j^{1/2} \Phi_i}{\lambda_e (V_{ds} - V_{dsat})}\right) = C_1 I_d \exp\left(-\frac{B_1}{(V_{ds} - V_{dsat})}\right)$$

Φ_i is the threshold energy for impact ionization, λ_e is the electron free mean path; so $\lambda_e E_{ymax}$ is the amount of energy gained by an electron before collision, and exp(- Φ_i / $\lambda_e E_{ymax}$) is the probability that an electron will cause impact ionization.

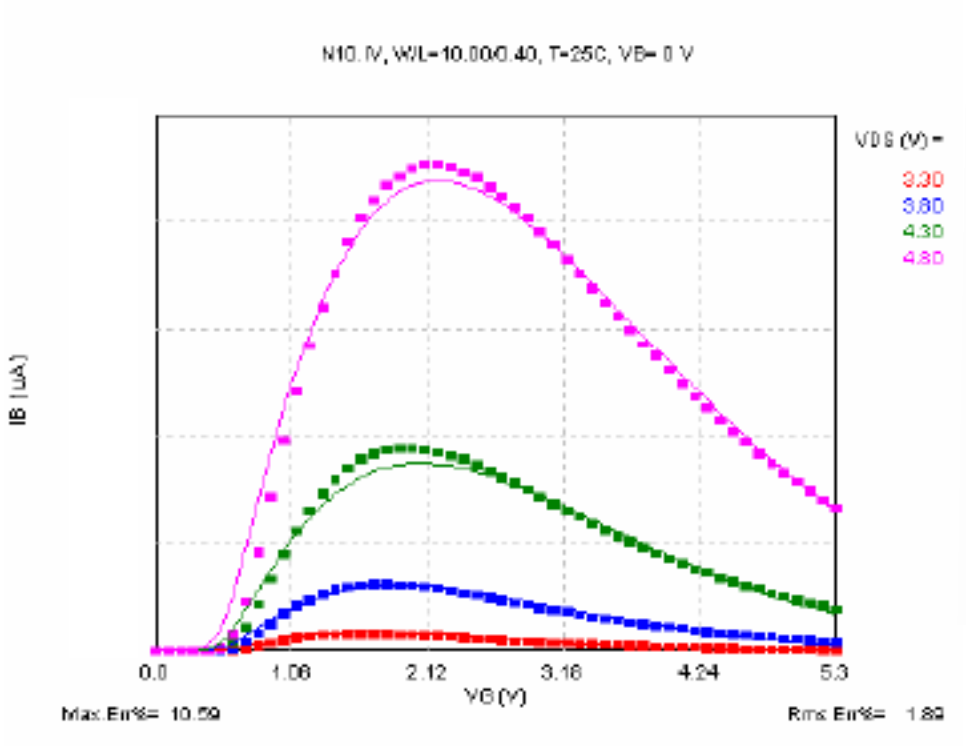
$\lambda_e E_{ymax}$ the kinetic energy of an electron, can be translated into electron temperature T_e. (Similarity to Arrhenius law)

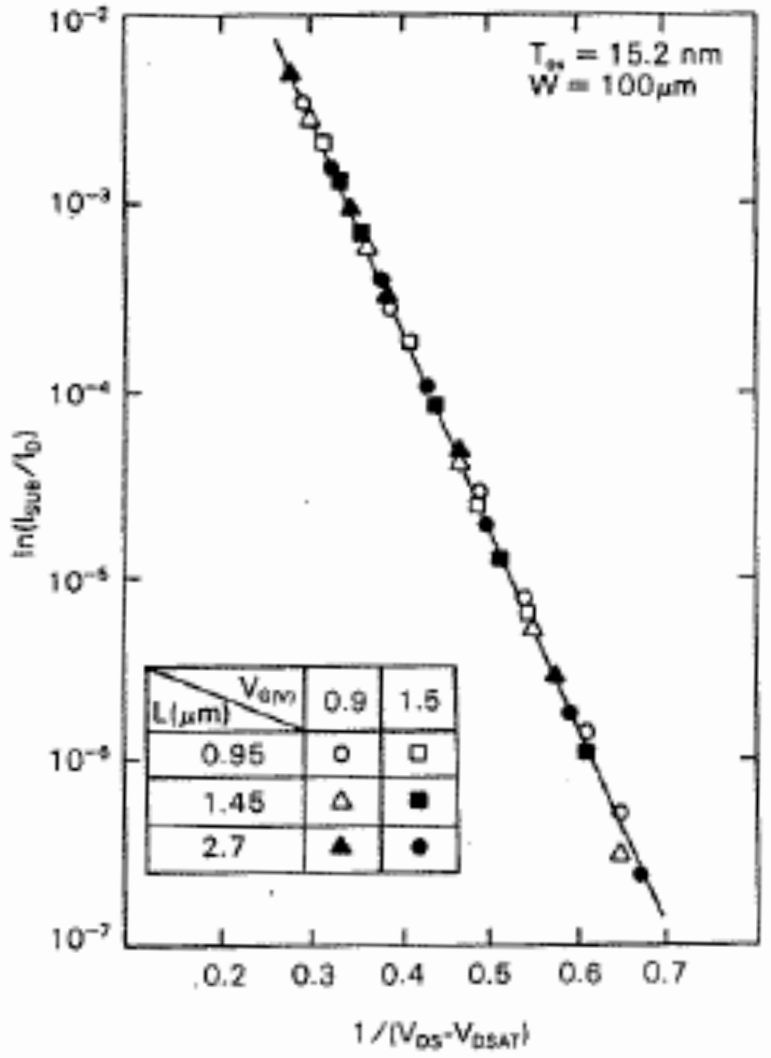
Hot Carriers and Substrate Current

Substrate current and device lifetime

Slightly modified equation

$$I_b = \frac{A_i}{B_i}(V_{ds} - V_{dsat}) I_d \exp\left(-\frac{B_i l_c}{V_{ds} - V_{dsat}}\right)$$

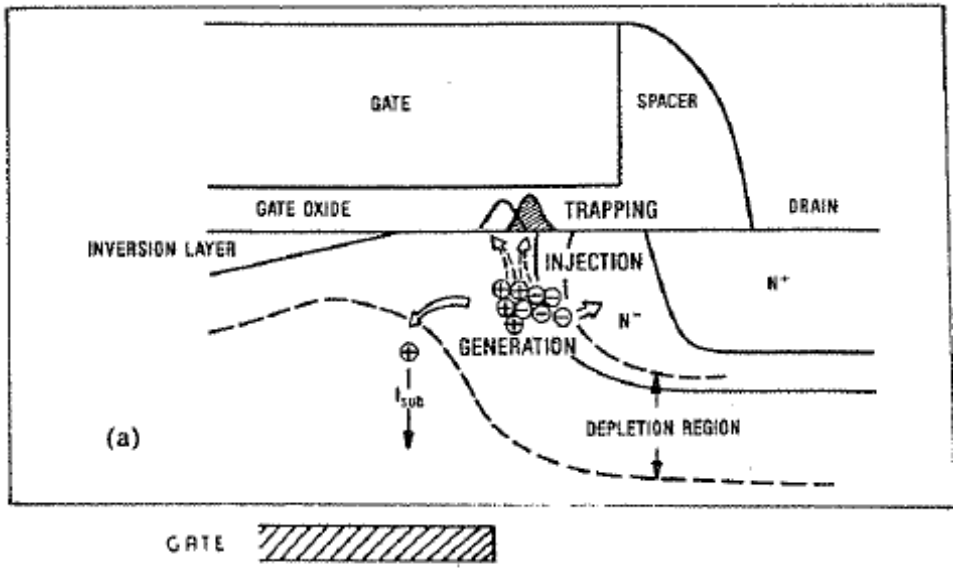




Universal nature of the curve gor all L and Vg

Degradation

Injection of electrons and holes into the oxide.



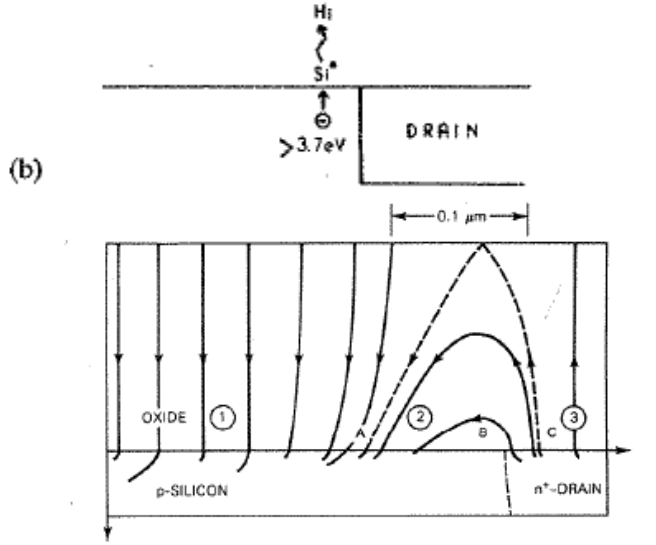


Figure 6.8 Two-dimensional electric field distribution near the drain of an *n*MOS. V_d = 8 V, V_g = 7 V, V_B = −2.5 V, L_{eff} = 1.3 μm and t_{ox} = 400 Å (Ref. 26, © 1984 IEEE).

Needed electron energy ~ 4eV:

Electron has to overcome Si-SiO_2 barrier 3.2eV

Has to break Si-H bond ~ 0.3 eV

Has to overcome repelling electric field 0.3 - 0.5 eV

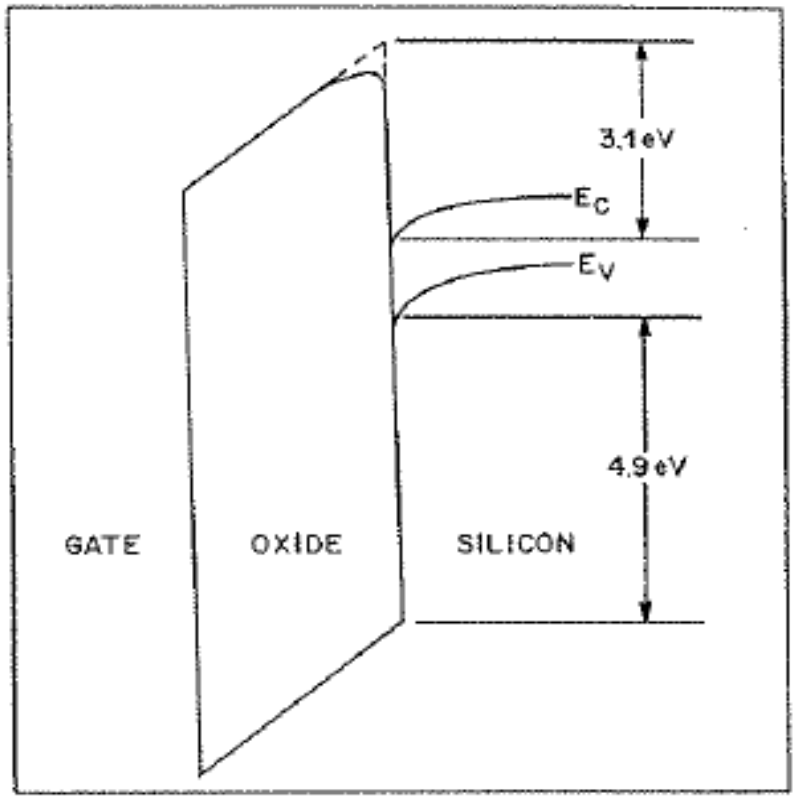
Situation for holes is more complicated:

Holes are not provided by the current but are generated during impact ionization; thus when created they are "cold". However, they accelerate in the local lateral field and acquire energy AND the vertical electric field is attractive for hole injection.

Hole has to overcome Si-SiO_2 barrier of 4.9V

Degradation (Exercise for ZrO_2)

Injection of electrons and holes into the oxide.



Needed electron energy ~ 4eV

Electron has to overcome Si-SiO_2 barrier 3.2eV

Has to break Si-H bond ~ 0.3 eV

Has to overcome repelling electric field 0.3 - 0.5 eV

Situation for holes is more complicated:

Holes are not provided by the current but are generated during impact ionization; thus: when created they are cold. However, they accelerate in the local lateral field and the vertical electric field are attractive for hole injection.

Hole has to overcome Si-SiO_2 barrier of 4.9V

Manifestation of Degradation

Characterization of degradation of a MOSFET transistor.

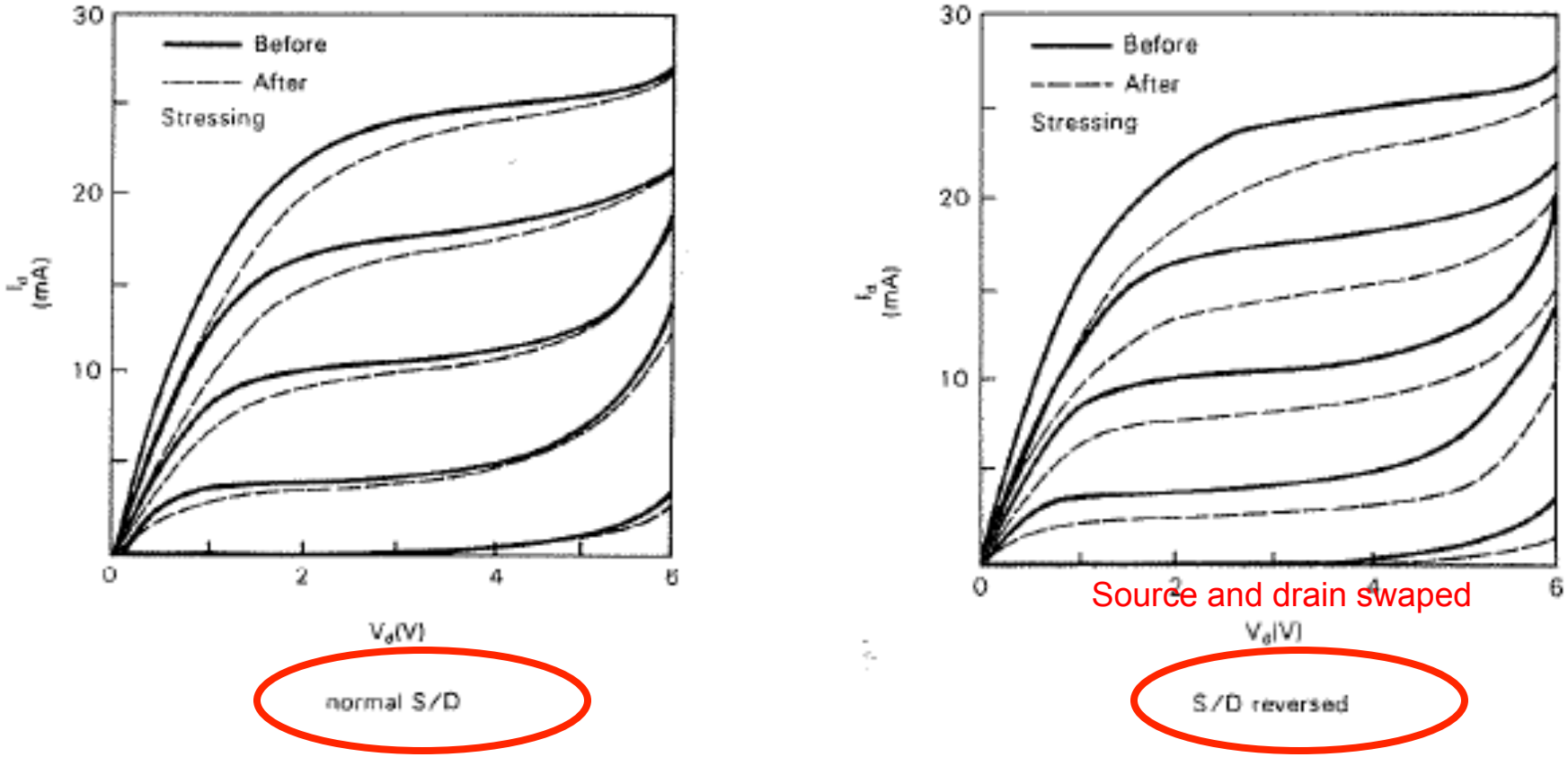


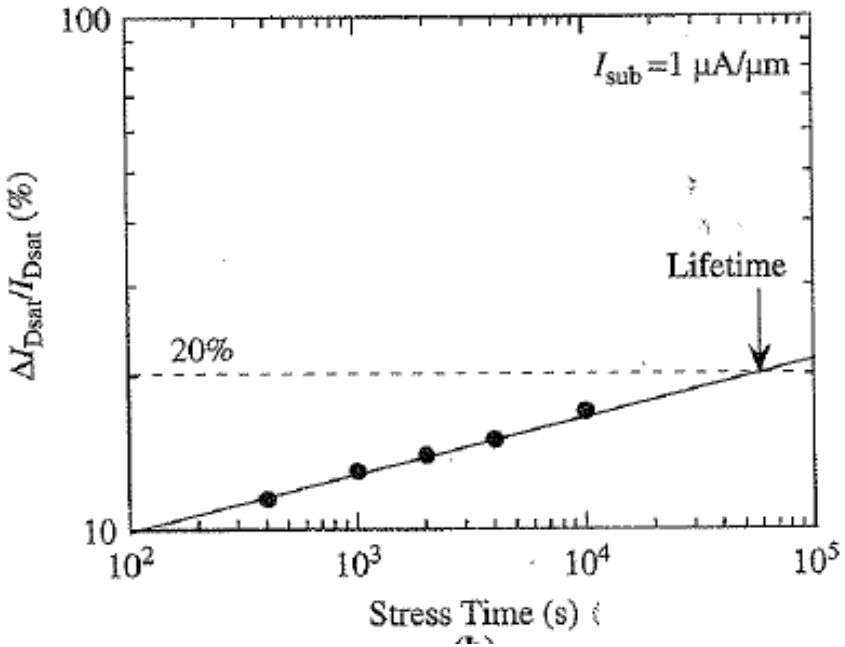
Figure 6.10 Degradation characteristics after stressing: (a) source/drain reversed during post-stress measurement; (b) source/drain unchanged during post-stress measurement (Ref. 29, © 1984 IEEE).

Hot Carriers

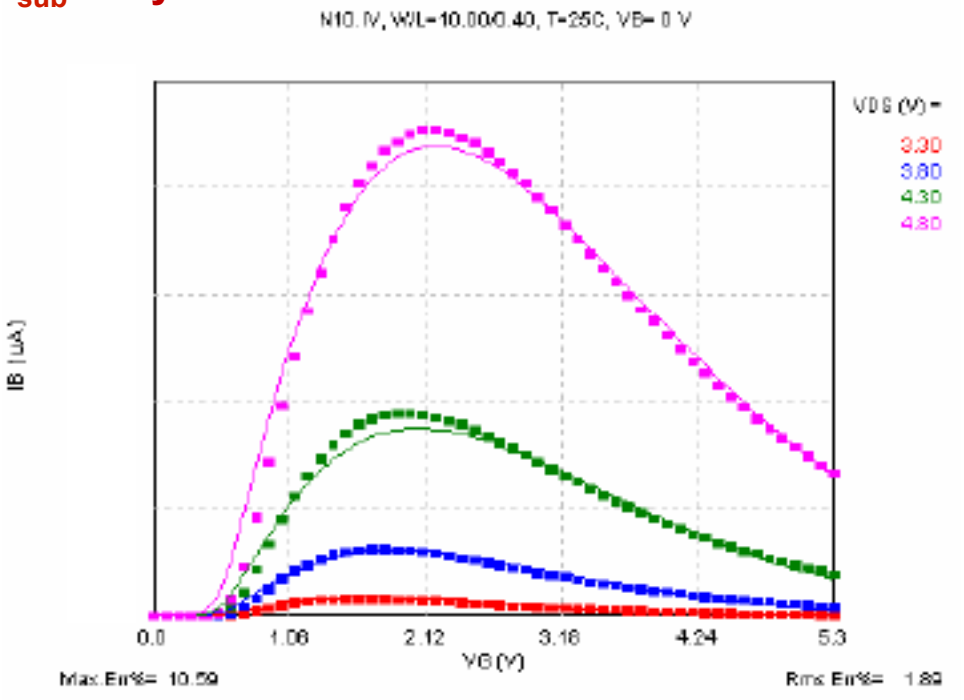
Substrate current and device lifetime

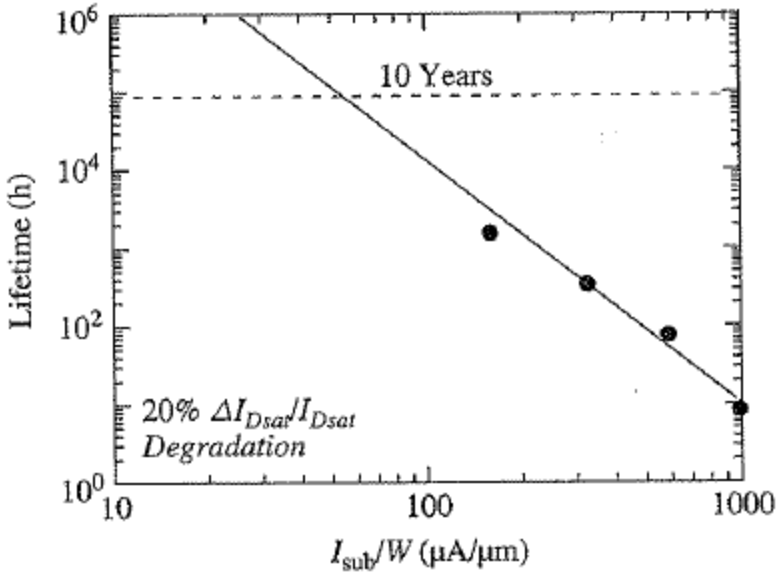
$$I_b = \frac{A_i}{B_i}(V_{ds} - V_{dsat}) I_d \exp\left(-\frac{B_i l_c}{V_{ds} - V_{dsat}}\right)$$

I_{sub} good indicator for degradation damage.
I_{sub} easy to measure



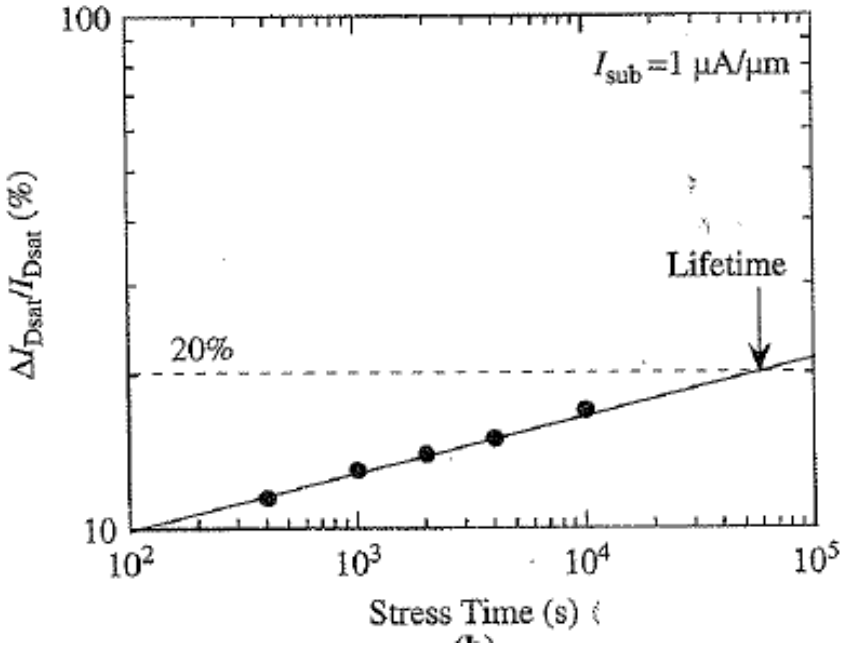
Bias at maximum substrate current



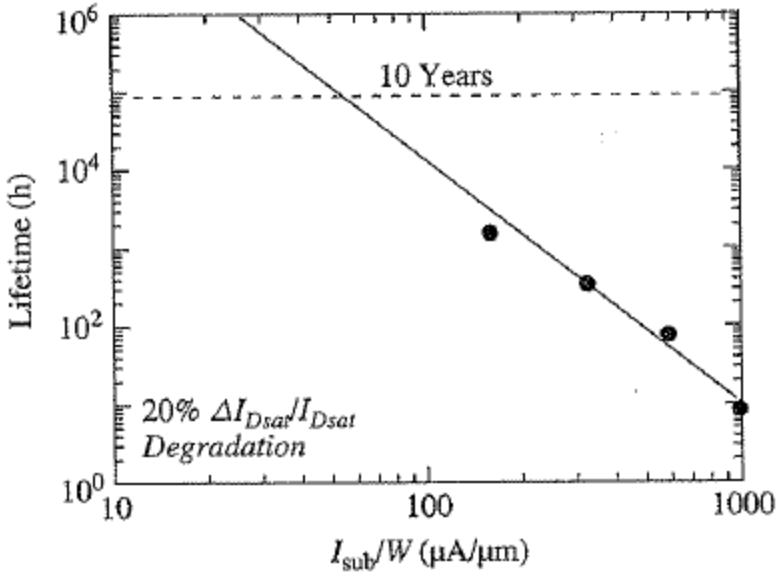


device lifetime determination:

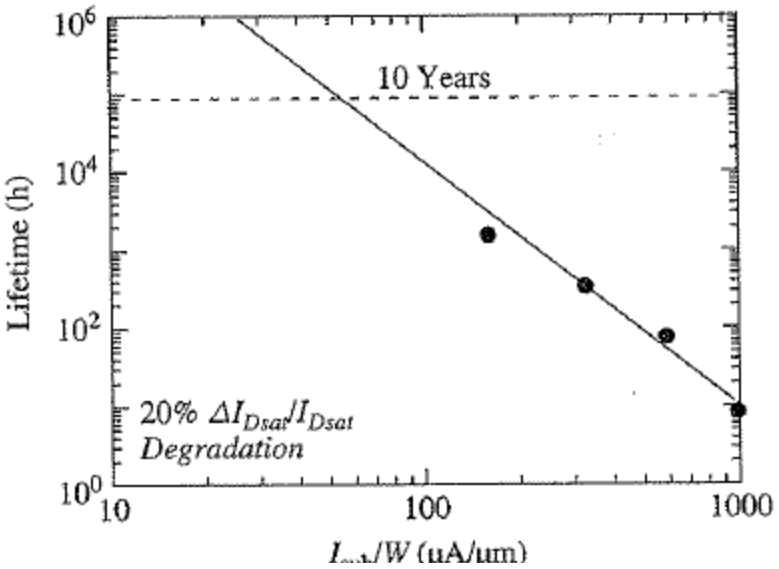
1) Monitor Id or Idsat as a function of stress time
2) Find expected time for a given change in current ΔI/I
3) Determine a good indicator for stress (here I_{sub})
4) Plot the life time as a function of the stress indicator (here I_{sub})
5) Your customer expects a product life time of 10 years
6) From your curves you can determine what is the average stress that the devices can tolerate without suffering a a specified degradation (here of ΔI/I=20%)



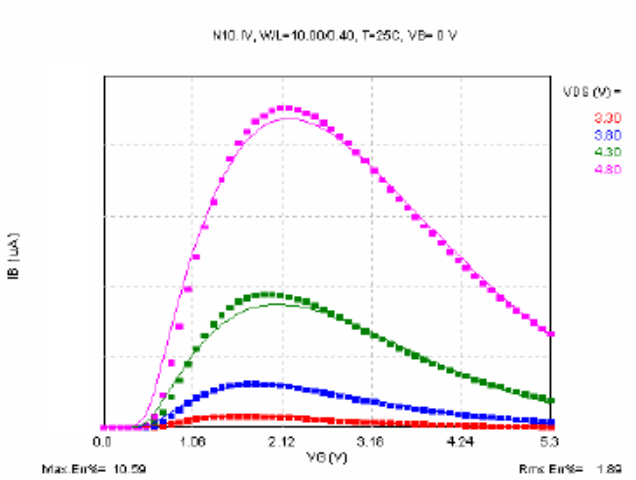
Bias at maximum substrate current



Substrate current and device lifetime



$$I_b = \frac{A_i}{B_i}(V_{ds} - V_{dsat}) I_d \exp\left(-\frac{B_i l_c}{V_{ds} - V_{dsat}}\right)$$



Hot carrier lifetime τ :

$$\tau = K \frac{(I_{sub} / I_d)^{-m}}{I_d}$$

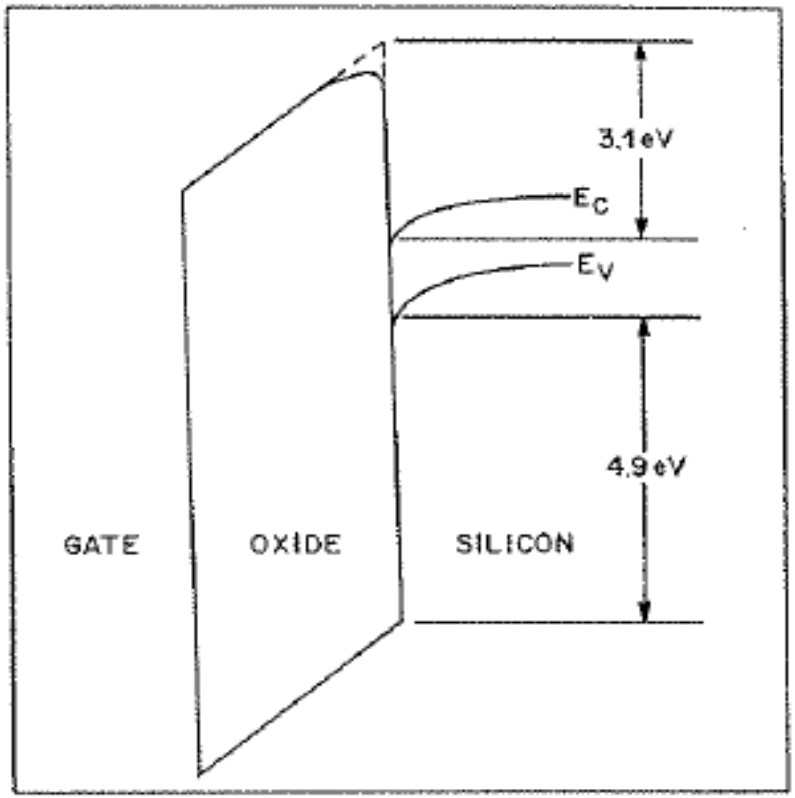
Or alternatively

$$\tau = K'(I_{sub} / I_d)^{-m}$$

Where m is approximately m=3
And K or K' are empirical constants.

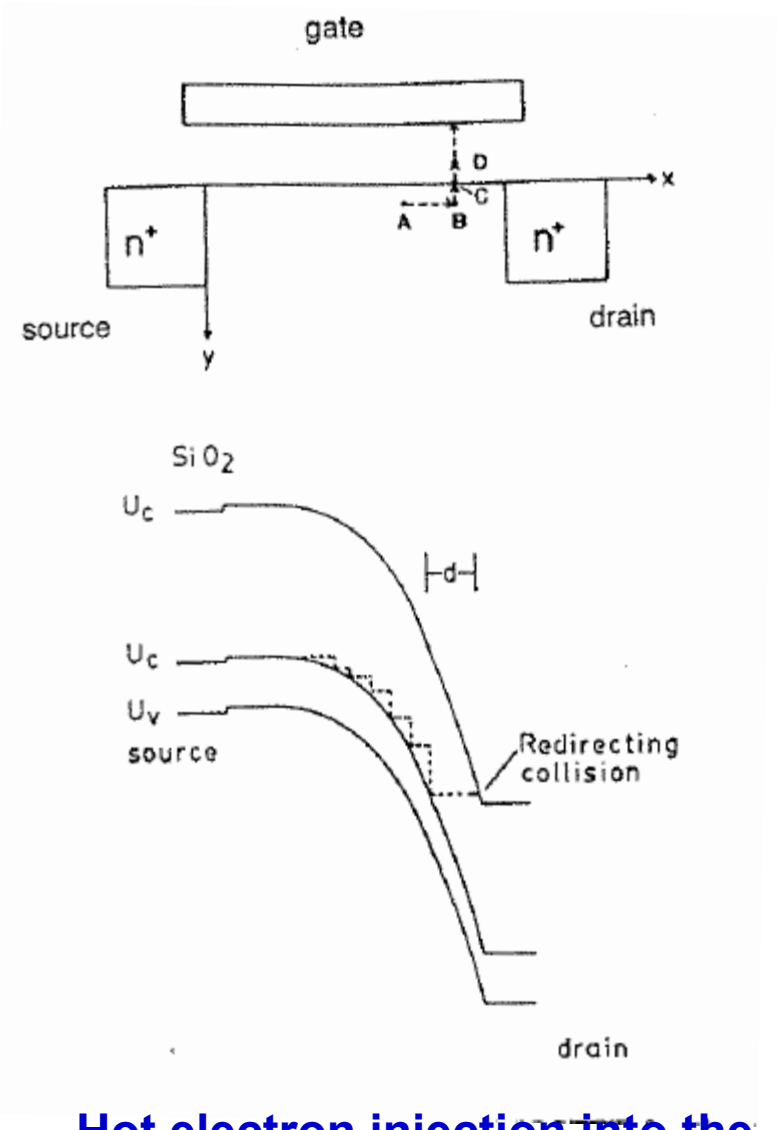
The equations were found to hold irrespective of the drain bias

Gate Current



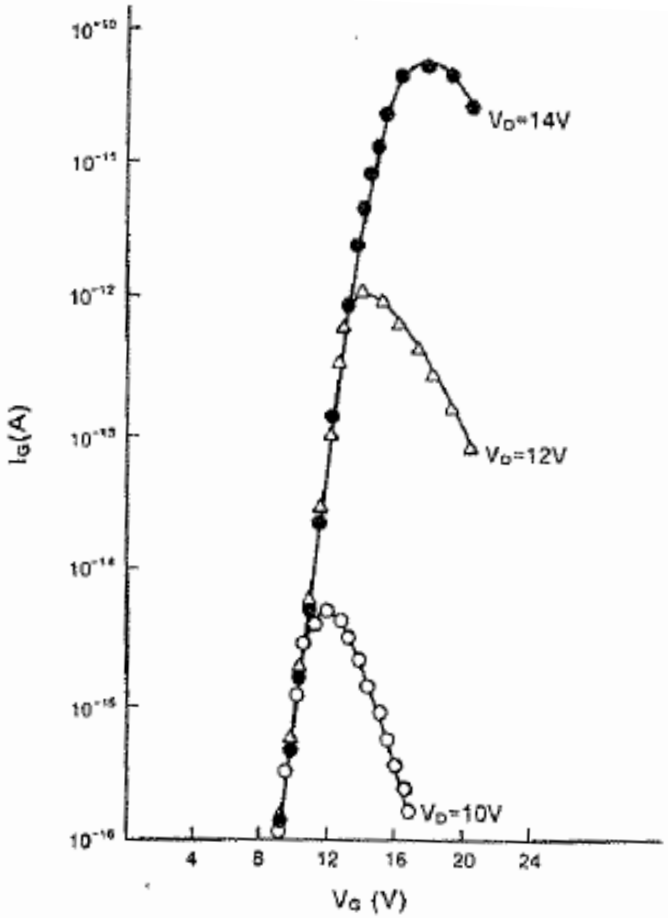
Barriers for electron and hole injection.

Channel hot electrons (CHE) are generally considered to be important, and channel hot hole injection is generally ignored.



Hot electron injection into the gate

Hot Electrons and Gate Current



Gate current due to channel hot electrons versus gate voltage, with V_{DS}

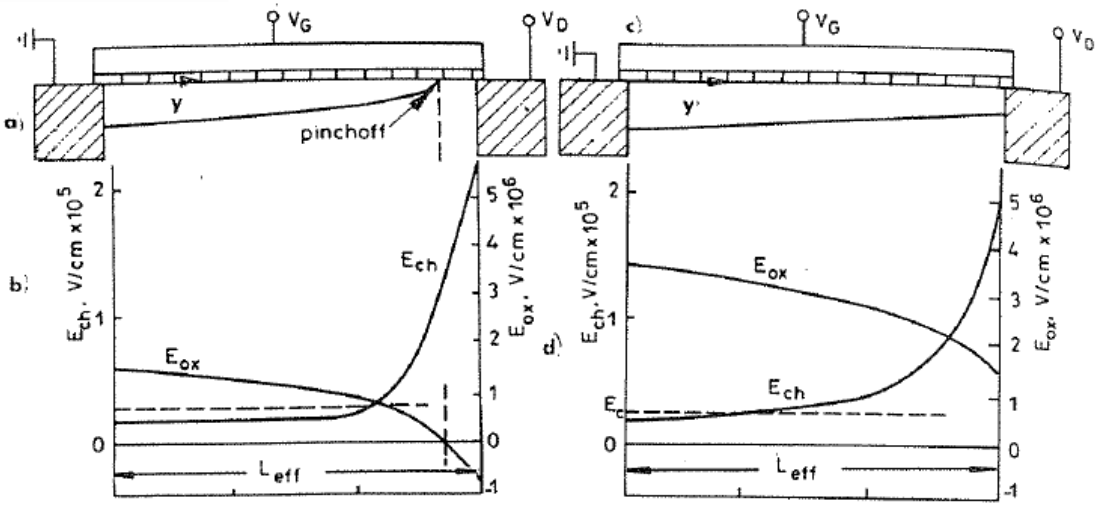
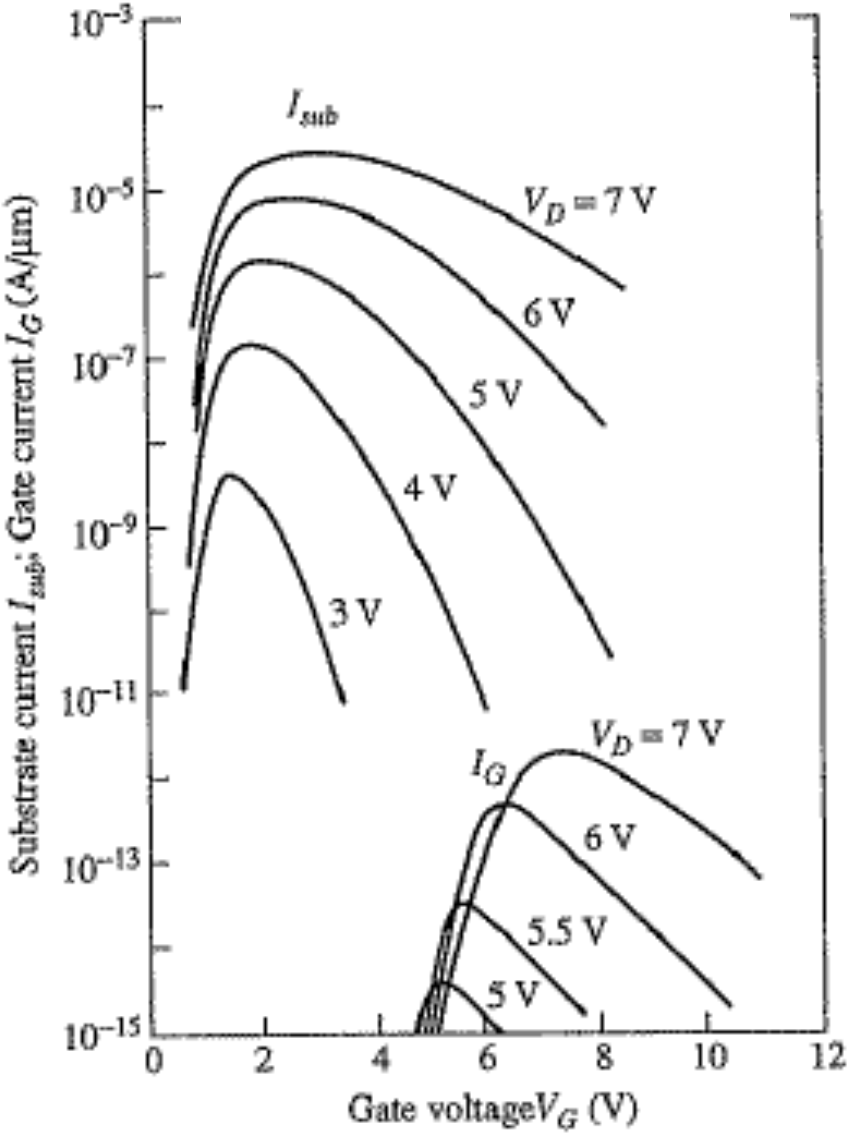


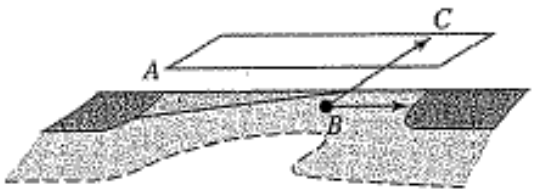
Fig. 7-8 (a) Cross section of MOS transistor operating in saturation. (b) The oxide and channel fields in the *y*-direction of the channel when the MOSFET is in saturation (i.e., $V_{GS}<V_{DS}$, here V_{GS} = 6V and V_{DS} = 8V). (c) Cross section of a MOS transistor operating in linear regime. (d) The oxide and channel fields in the *y*-direction of the channel when the MOSFET is in the linear regime (i.e., $V_{GS}>V_{DS}$, here V_{GS} = 15 V and V_{DS} = 8V).[119] (© IEEE 1991).

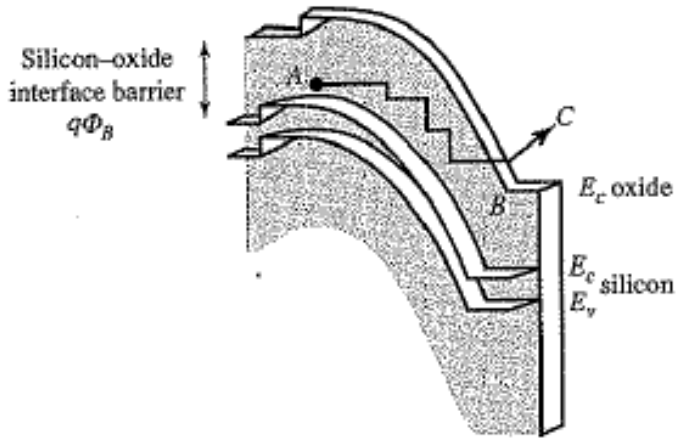
Initially, gate current increases with V_g due to increase in number of carriers. It peaks at about V_d=V_g; beyond this point $V_{gs}>V_{ds}$ the MOSFET is in linear region of operation and the electric field is rapidly reduced and few energetic electrons are produced.

Substrate and Gate Currents

$$I_G = I_D \int_0^L \exp\left(-\frac{\phi_B}{\mathscr{E}_y \lambda}\right) P(\mathscr{E}_{ox}) dy$$







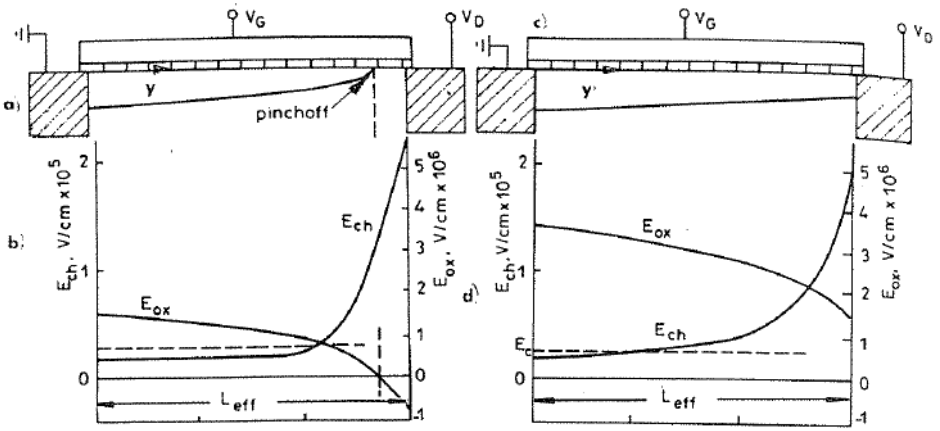


Fig. 7-8 (a) Cross section of MOS transistor operating in saturation. (b) The oxide and channel fields in the *y*-direction of the channel when the MOSFET is in saturation (i.e., $V_{GS}<V_{DS}$, here $V_{GS} = 6$V and $V_{DS} = 8$V). (c) Cross section of a MOS transistor operating in linear regime. (d) The oxide and channel fields in the *y*-direction of the channel when the MOSFET is in the linear regime (i.e., $V_{GS}>V_{DS}$, here $V_{GS} = 15$ V and $V_{DS} = 8$V).[119] (© IEEE 1991).

Modeling of the Gate Current

$$I_{gate} \propto I_d$$

$$I_{gate} \propto \exp\left(-\frac{\Phi_b}{\lambda_e E_{y\max}}\right) = \exp\left(-\frac{\Phi_b}{kT_e}\right)$$

$$I_{gate} = C_2(V_g, V_d) I_d \exp\left(-\frac{\Phi_b}{\lambda_e E_{y\max}}\right)$$

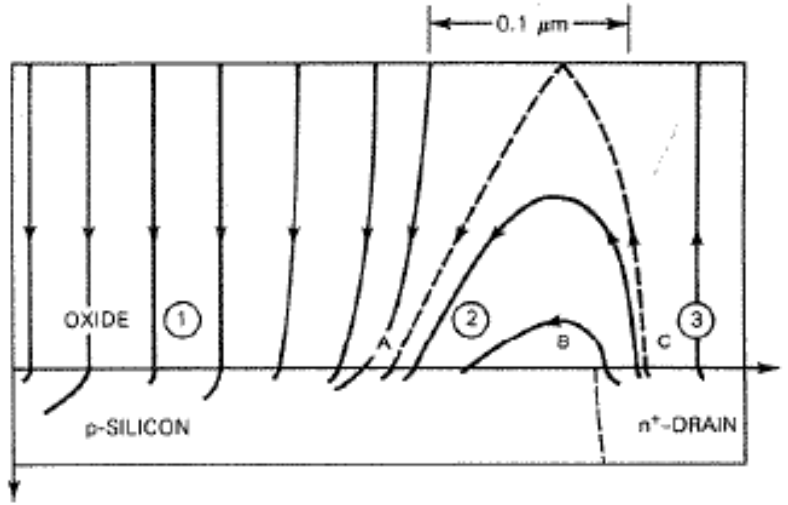


Figure 6.8 Two-dimensional electric field distribution near the drain of an *n*MOS. V_d = 8 V, V_g = 7 V, V_B = −2.5 V, L_{eff} = 1.3 μm and t_{ox} = 400 Å (Ref. 26, © 1984 IEEE).

Φ_b is the threshold energy Si-SiO_2 barrier, λ_e is the electron free mean path; so $\lambda_e E_{ymax}$ is the amount of energy gained by an electron before collision, and exp(- Φ_b / $\lambda_e E_{ymax}$) is the probability that an electron will overcome the Si/SiO2 barrier.

For V_g<V_d, C_2 decreases rapidly because the corresponding E_{ox} acts as a retarding field to prevent injected electrons from reaching the gate. For V_g>V_d $C_2 \approx 0.002$

Hot Carriers and Gate Current

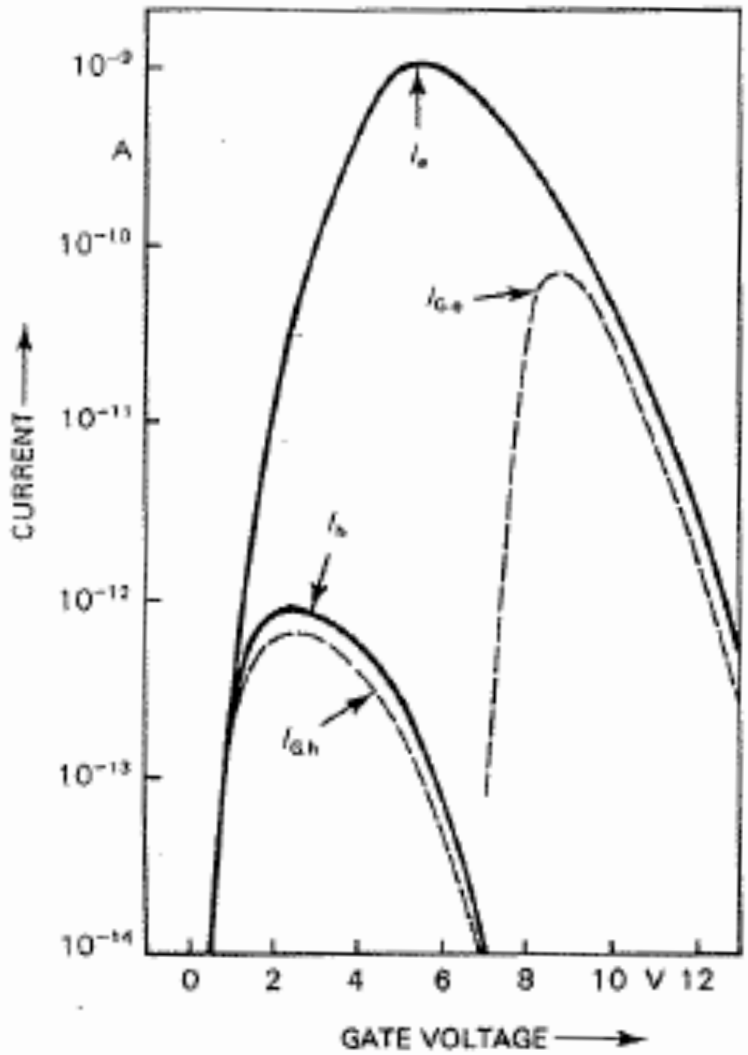


Figure 6.9 Calculated total emitted electron and hole current, I_e and I_h, as a function of gate voltage. $I_{G,e}$ is the electron gate current, and $I_{G,h}$ is the hole gate current. $V_d = 8$ V, $V_B = -2.5$ V, $W = 100$ μm, $L_{eff} = 1.8$ μm and $t_{ox} = 420$ Å (Ref. 26, © 1984 IEEE).

Only small fraction of the injected electrons reach gate. Especially at low gate bias, most injected electrons do not reach gate.

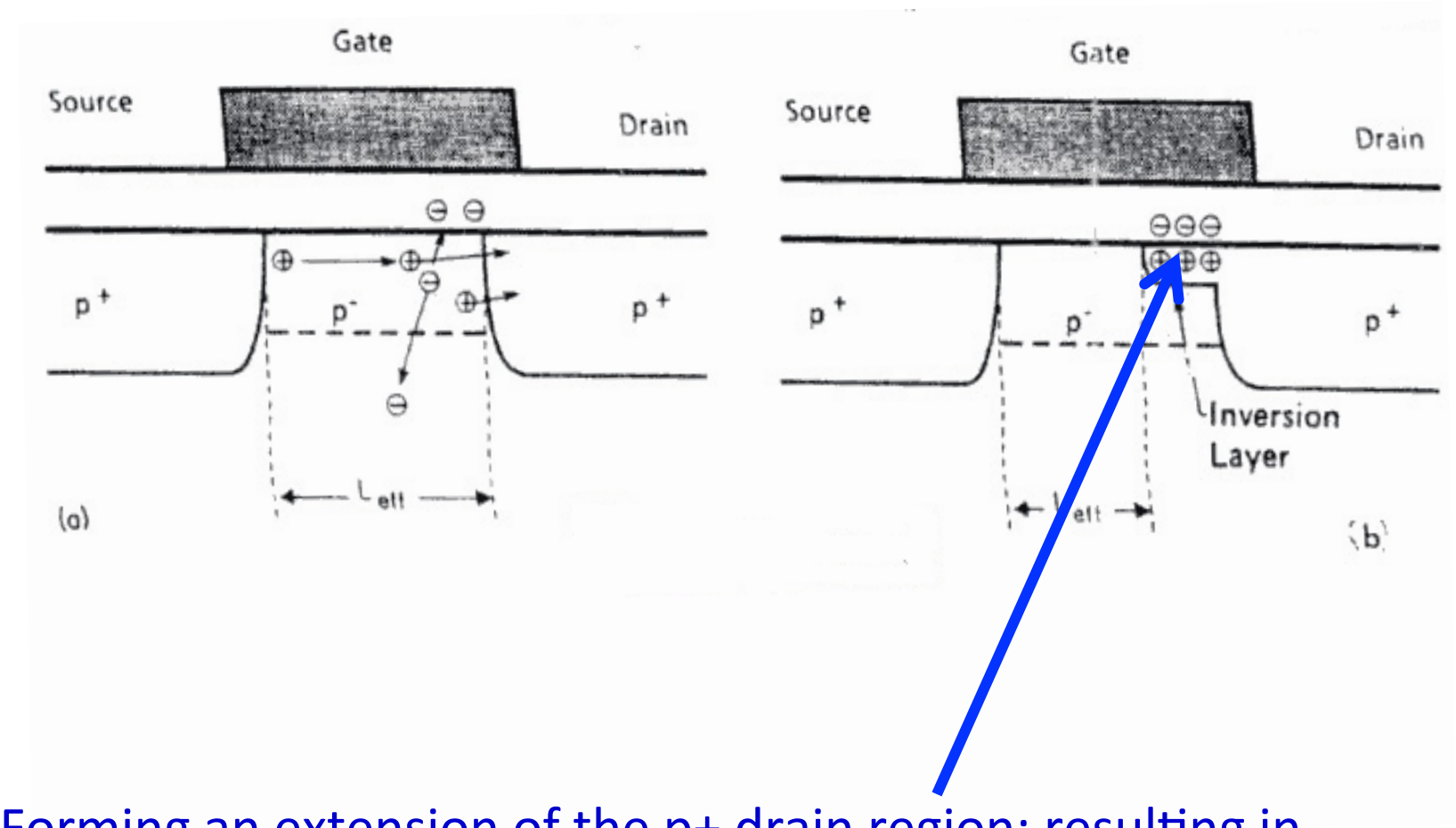
On the other hand, most hot holes, although at a much lower level, reach gate electrode when injecting into the oxide due to the attracting electric field in the oxide E_{ox} for $V_g<V_d$.

The injection efficiency for holes is lower than that of electrons because of the higher barrier (4.9 eV versus 3.1 eV for electrons).

The electron gate current is used for programming in non-volatile memory devices (floating gate devices).

Negative Charge Generation in PMOSFET

- Hot electron trapping results negative charge buildup in the oxide near the drain of a PMOSFET.



Forming an extension of the p+ drain region; resulting in channel length shortening

P-MOSFET Degradation

- Channel length Degradation
- Transconductance Degradation
- Threshold Shift degradation
- Shortening of L_{eff}

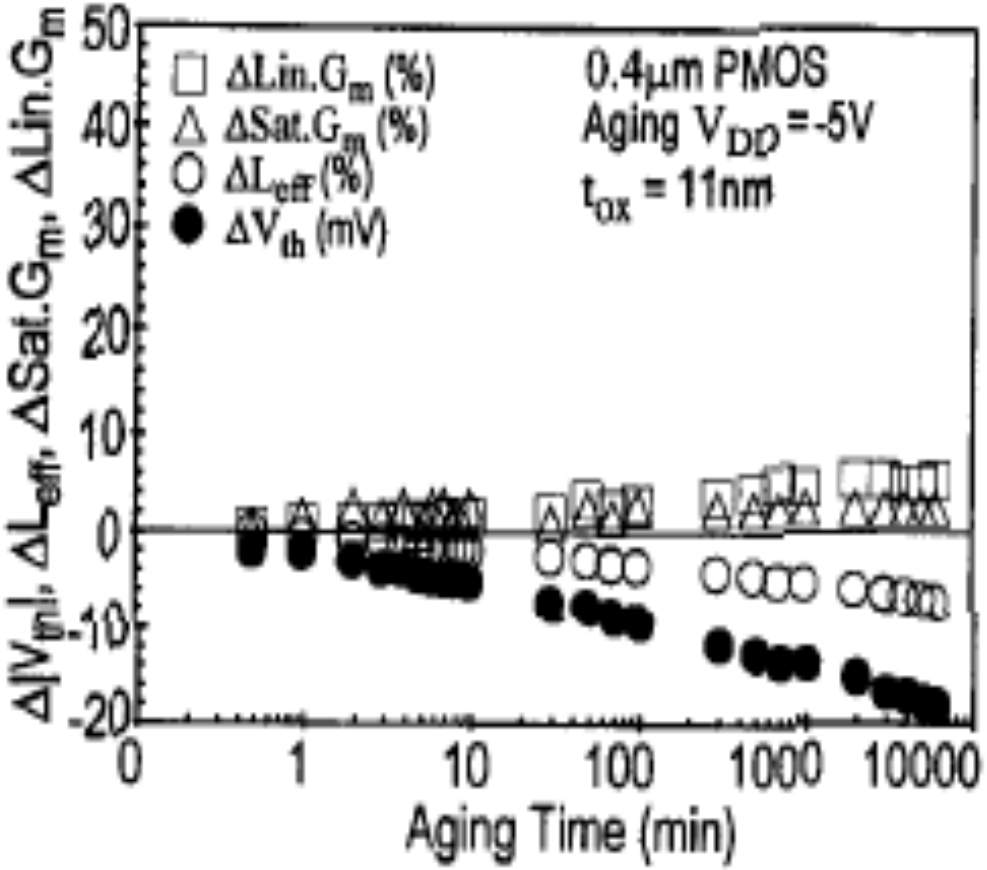


Fig.2 Hot carrier degradation of a 0.4μm PMOS. Both $|V_{th}|$ and L_{eff} decrease with the aging time. Saturation and linear G_m increase with time.

N-MOS Degradation

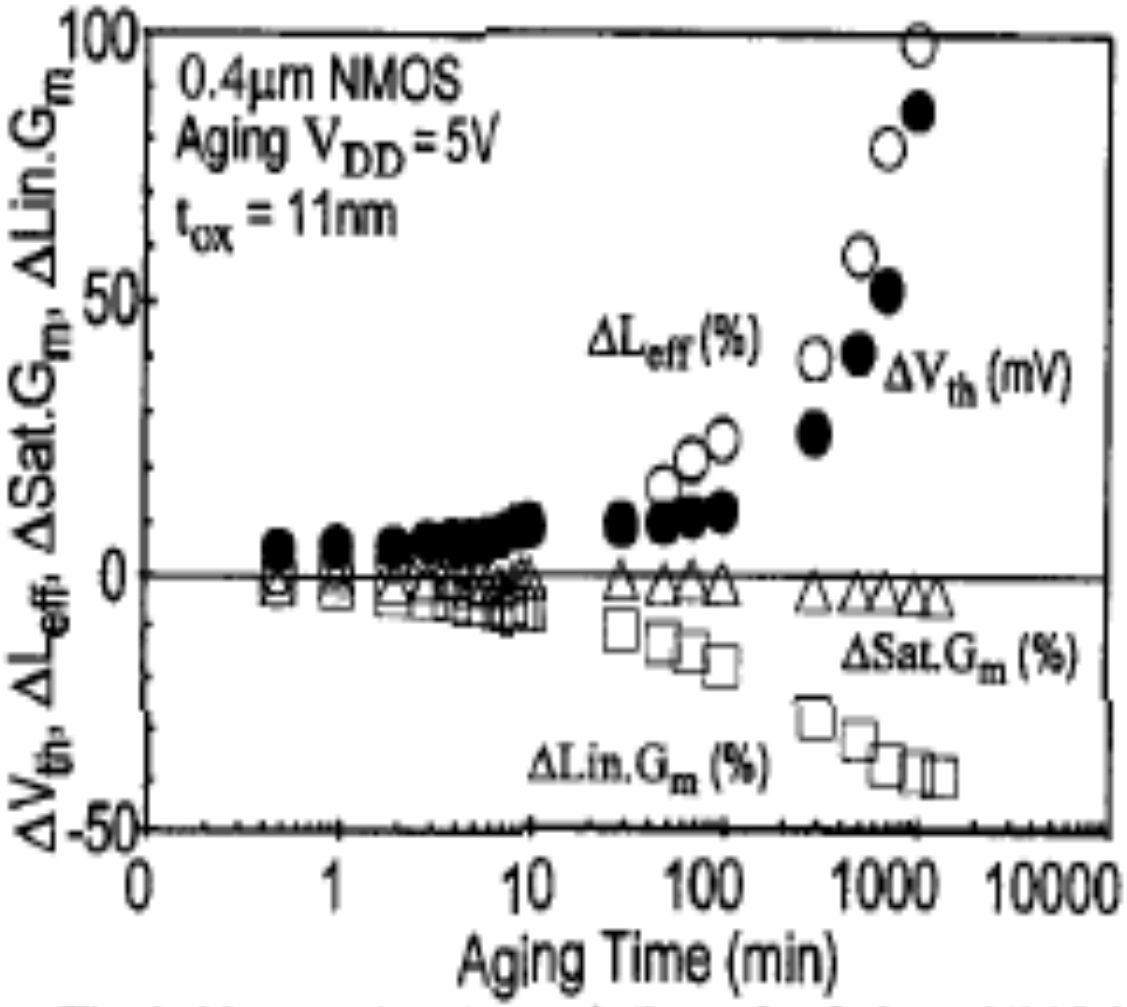


Fig.1 Hot carrier degradation of a 0.4μm NMOS. Both V_{th} and L_{eff} increase with the aging time. Saturation and linear G_m decrease with time.

- **Trapped electrons in the oxides result in the increase of V_T & L_{eff}**
- **… Opposite to PMOS**

Suppression of Hot Carrier Effect

(Device structure aspect)

- **Reduction of Hot-Carrier Generation**

❖ Reduce the high drain field

❖ Separate main current path away from maximum field .

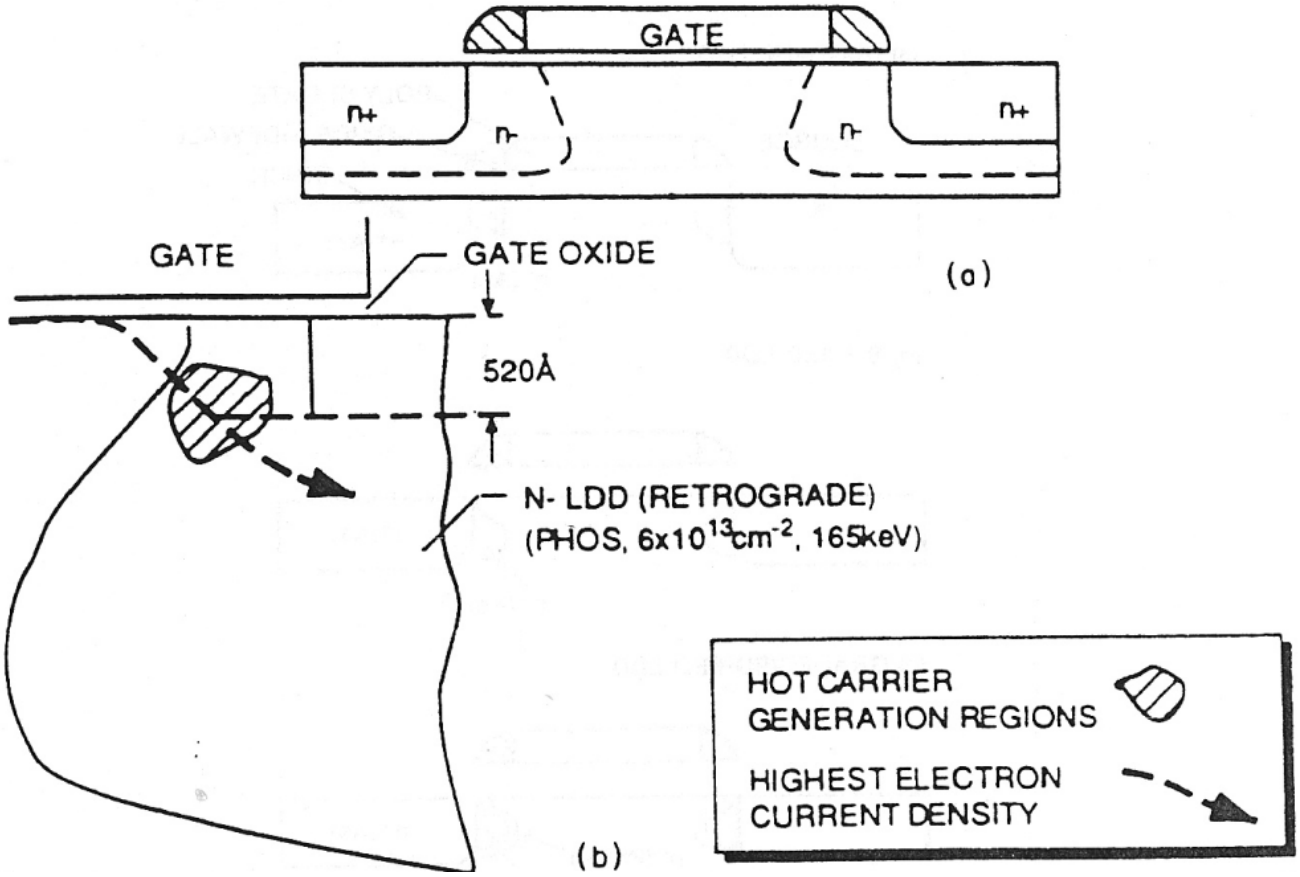
- **Reduction of Hot-Carrier Injection**

❖ Push impact ionization region deep into silicon.

❖ Position the injection point outside the gate

Suppression of Hot Carrier Effect

Separate main current path away from maximum field!



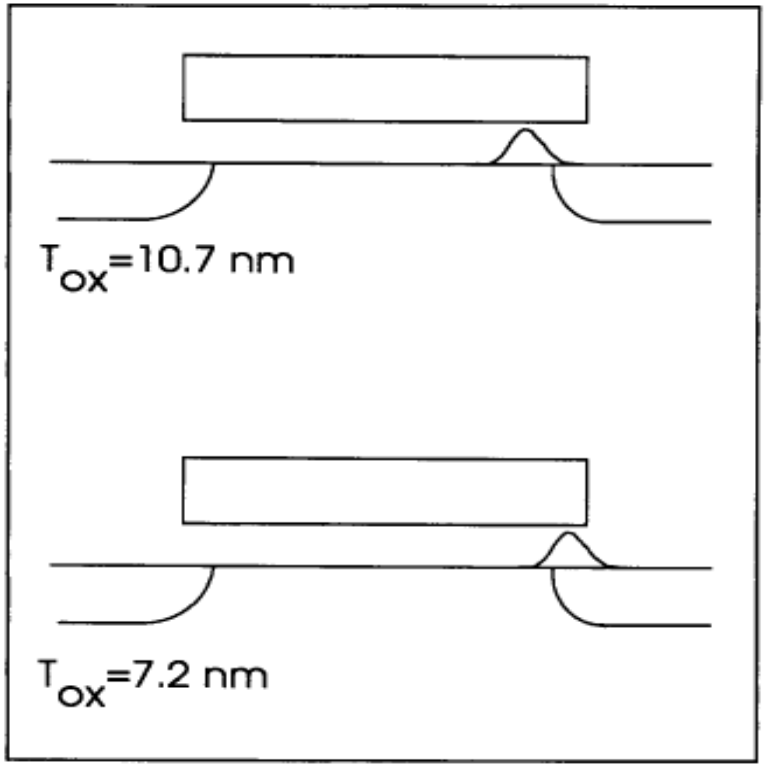
Debate whether I_{sub} is a good indicator for degradation for different technologies.

Hot Carrier Reduction Technique

- Gate Oxide thickness reduction (reduction of E_y)
- Lightly Doped MOSFET structure
- Double Diffused MOSFET structure
- Deuterium Post –Metal Annealing

Gate Oxide thickness reduction (reduction of lateral field and shift of the injection point)

- As the oxide thickness is reduced , the point of peak of electron injection moves further into the drain region , the damage region over the channel is reduced



High Electrical Peaks and LDD Drain

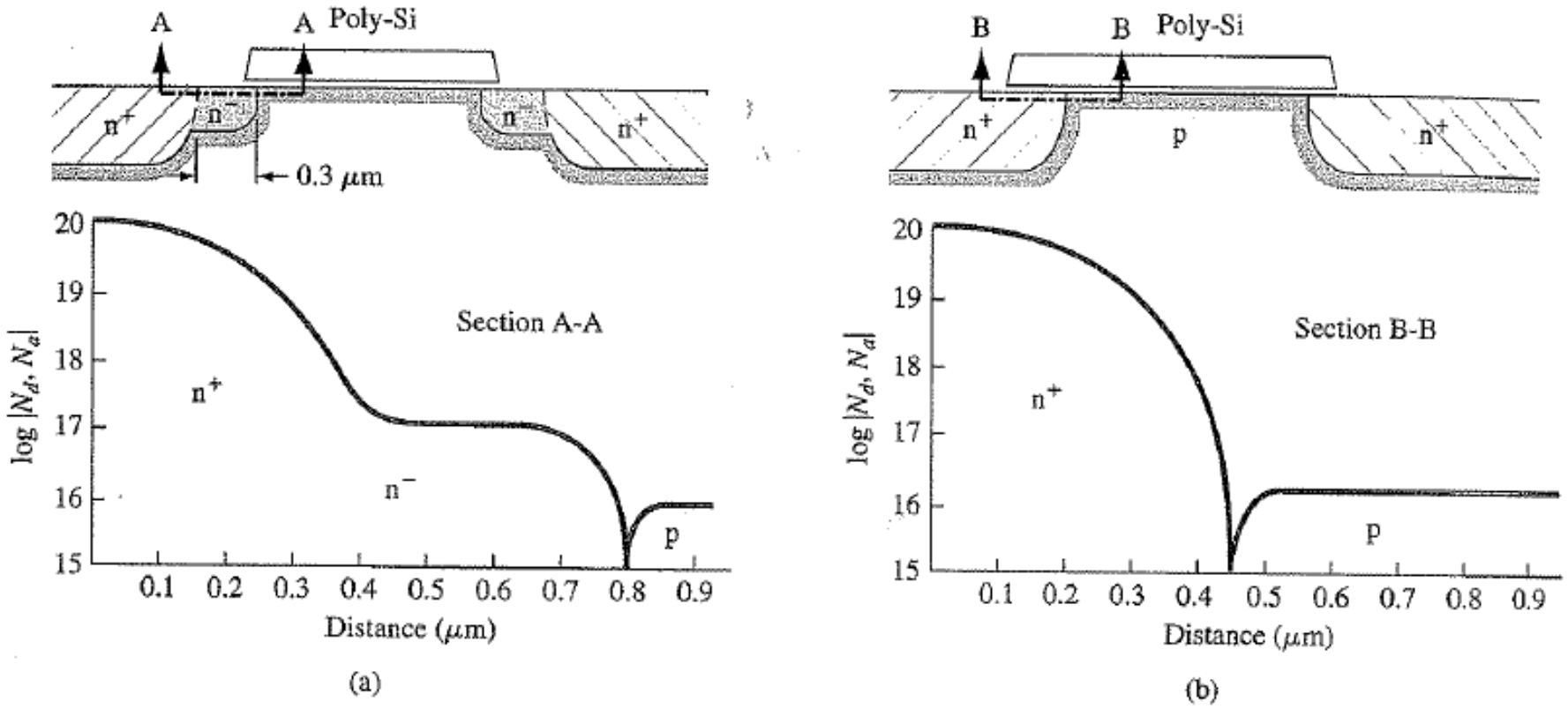
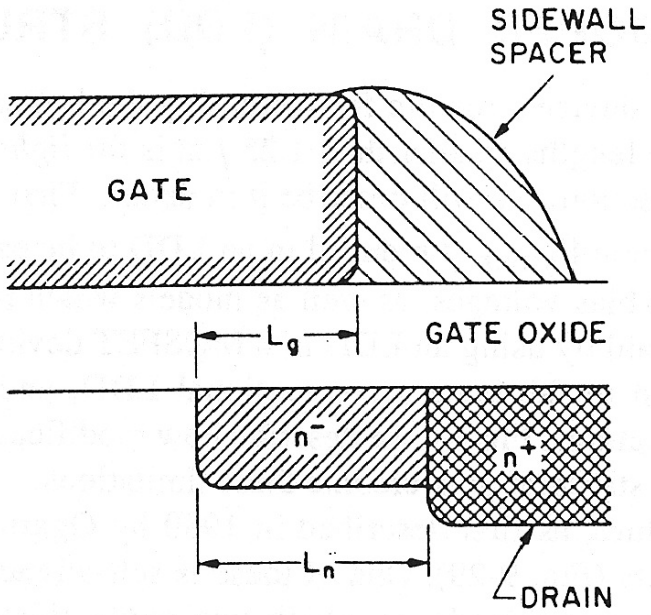


Figure 12.27 | (a) The lightly doped drain (LDD) structure. (b) Conventional structure.

High Electrical Peaks and LDD Drain



The price for LDD is a shorter channel length at the same gate length and increased possibility of punchthrough condition.

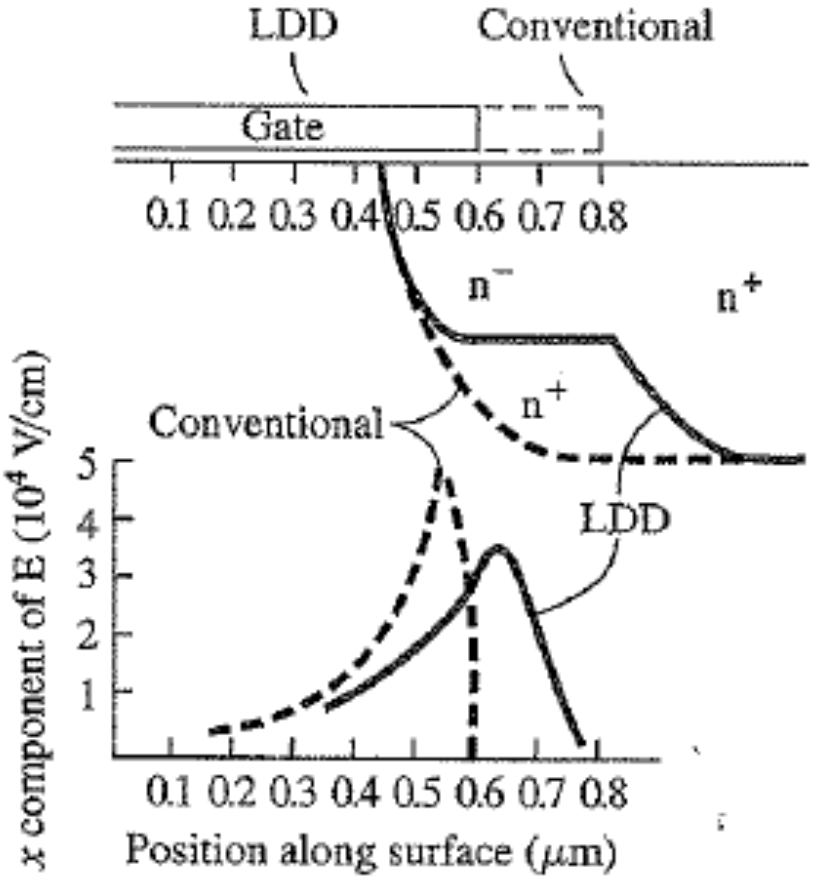


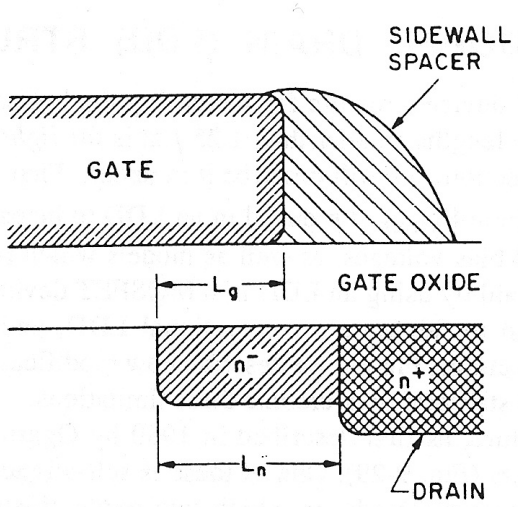
Figure 12.28 | Magnitude of the electric field at the Si–SiO_2 interface as a function of distance; $V_{DS} = 10$ V, $V_{SB} = 2$ V, $V_{GS} = V_T$.

High Electrical Peaks and LDD Drain

Modeling E_{ymax} in LDD MOSFETs

1. Simple model for estimating E_{ymax} in LDD MOSFETs

$$E_{ymax}\ (LDD) = (V_{DS}-V_{DSsat})/(0.22t_{ox}^{1/3}r_j^{1/3}+L_{n-})$$



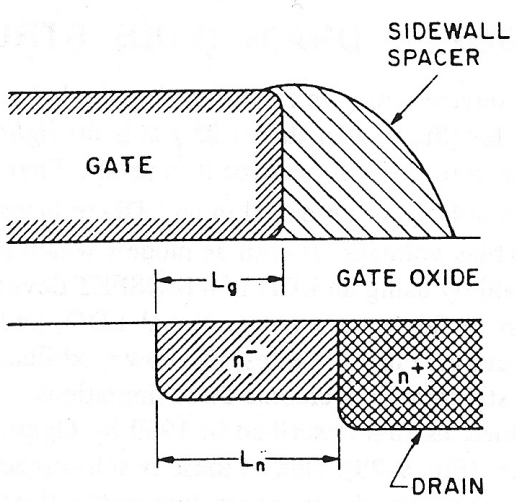
Tradeoff: With LDD we incurr a larger parasitic source/drain resistances which decrease the drain current.

$R_{n-} = L_{n-}/(Zq\mu_n N_D rj)$

Z: device width

μ_n: electron mobility in the n^- region

High Electrical Peaks and LDD Drain



Pros:

LDD → E_{ymax} ↓ → Hot-carrier↓

→ I_{sub} ↓ → hot-carrier reliability ↑

Cons:

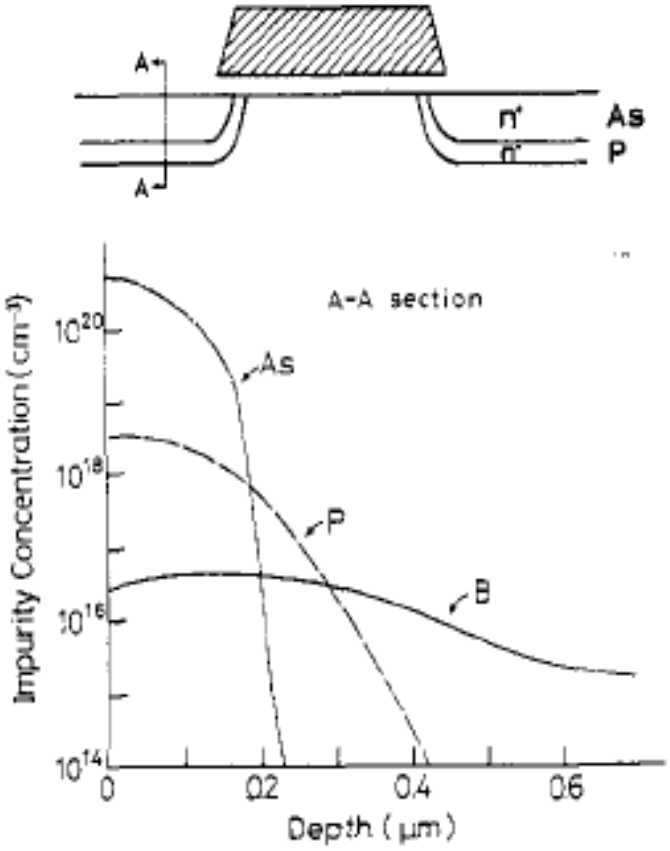
- LDD → I_d ↓
- Length scaling more difficult

- R_{n-} causes a 10~20% loss in both I_D and g_m compared to non-LDD devices.
- The drain R_{n-} and source R_{n-} act to decrease I_D in the linear region, while the source R_{n-} acts to decrease I_{Dsat}

- doping concentration of the n^- region ↑, L_{n-} length ↓ → R_{n-} ↓
- L_{n-} : neither too long, nor too short
- doping concentration of the n^- region : trade-off between performance and hot-carrier degradation

Double diffused MOSFET structure to mitigate hot carrier effects

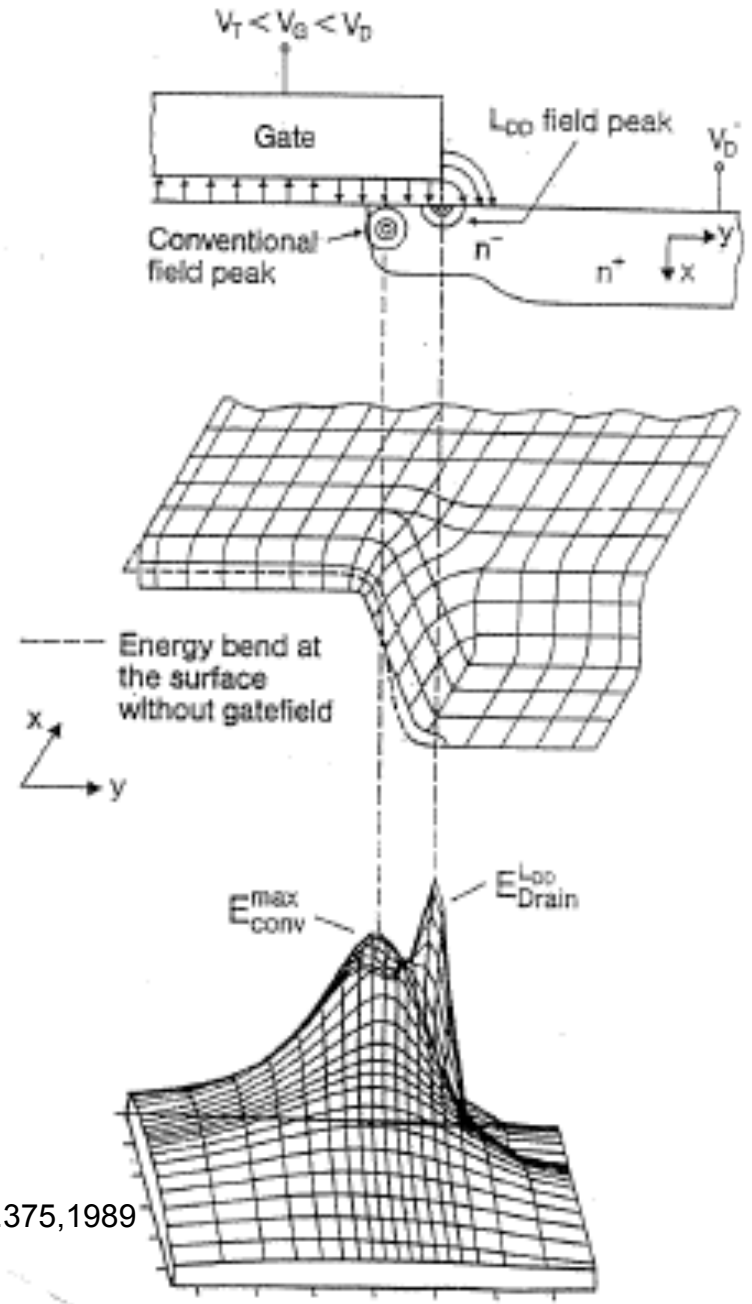
- Deeper n- phosphorous profile than N^+ As profile .
- The path of maximum current away from the position of the maximum field to reduce the impact ionization
- The disadvantage of double-diffused S/D regions over LDD regions is that one incurres a deeper junction depth running counter to scaling efforts



High electrical peaks and LDD Drain; secondary lateral field peaks

Origin of the LDD field peak:

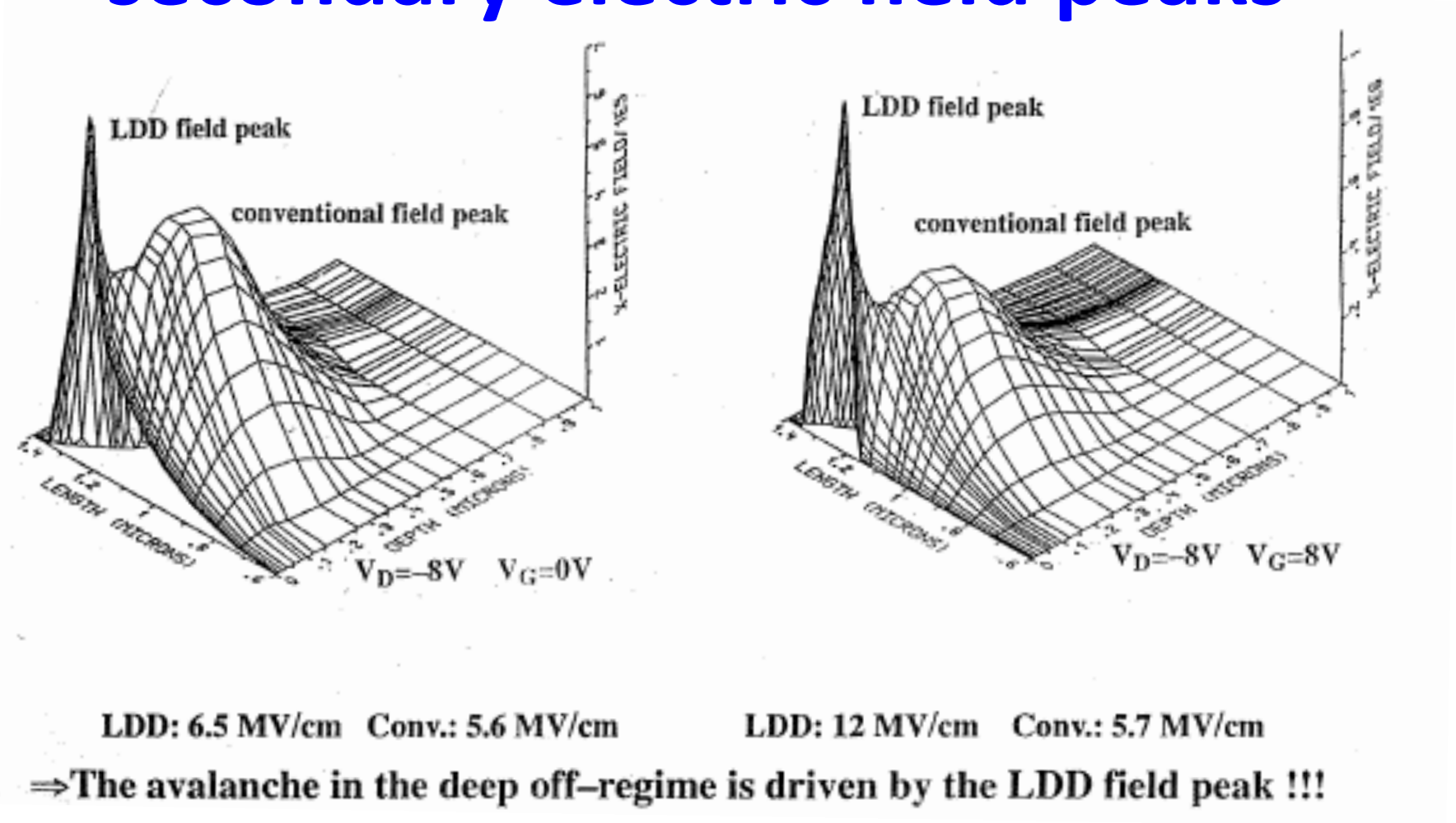
Lateral variation of the vertical electric field (gate oxide field) creates lateral field peak.



M.Orlowski et al, "Model for the Electric Fields in LDD MOSFET's - Part I: Field Peaks on the Source Side", IEEE TRANS.EL.. DEV. vol. 36(2) p.375,1989

M.Orlowski et al, "Model for the Electric Fields in LDD MOSFET's - Part II: Field Peaks on the Drain Side", IEEE TRANS.EL.. DEV. Vol. 36(2) p.382,1989

High Electrical Peaks and LDD Drain; secondary electric field peaks



LDD: 6.5 MV/cm Conv.: 5.6 MV/cm **LDD: 12 MV/cm Conv.: 5.7 MV/cm**

⇒The avalanche in the deep off–regime is driven by the LDD field peak !!!

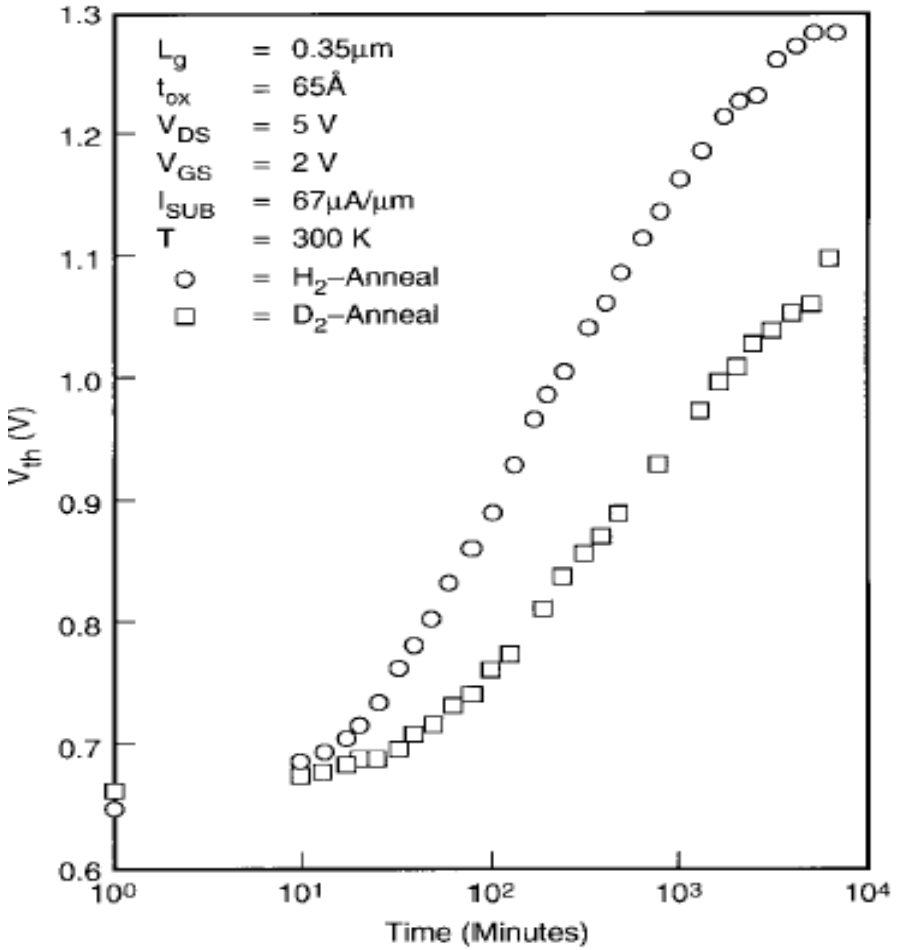
M.Orlowski et al, "Model for the Electric Fields in LDD MOSFET's - Part I: Field Peaks on the Source Side", IEEE TRANS.EL.. DEV. vol. 36(2) p.375 and p. 382,1989

Deuterium Post –Metal Annealing

Replace Si-H by Si-D bond

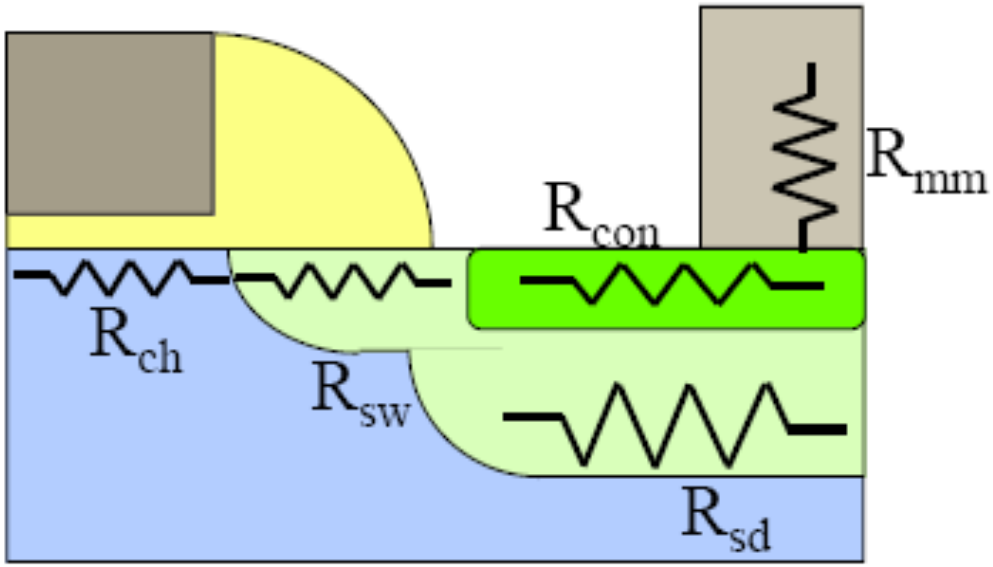
- Low temperature post metalization anneals in hydrogen ambient are critical in reducing Si-SiO_2 interface trap .
- Under Hot Carrier stress , bond to deuterium (^2H or D) are more difficult to break than bonds to protons

Evolution of V_{th} as function of stress time



Series Resistance in MOSFETs

Problems in Shallow Junction



- Many components of the transistor resistance
- Lot of effort spent to optimize each component

Accumulation/Spreading Resistance

The spreading of current lines causes additional voltage drop

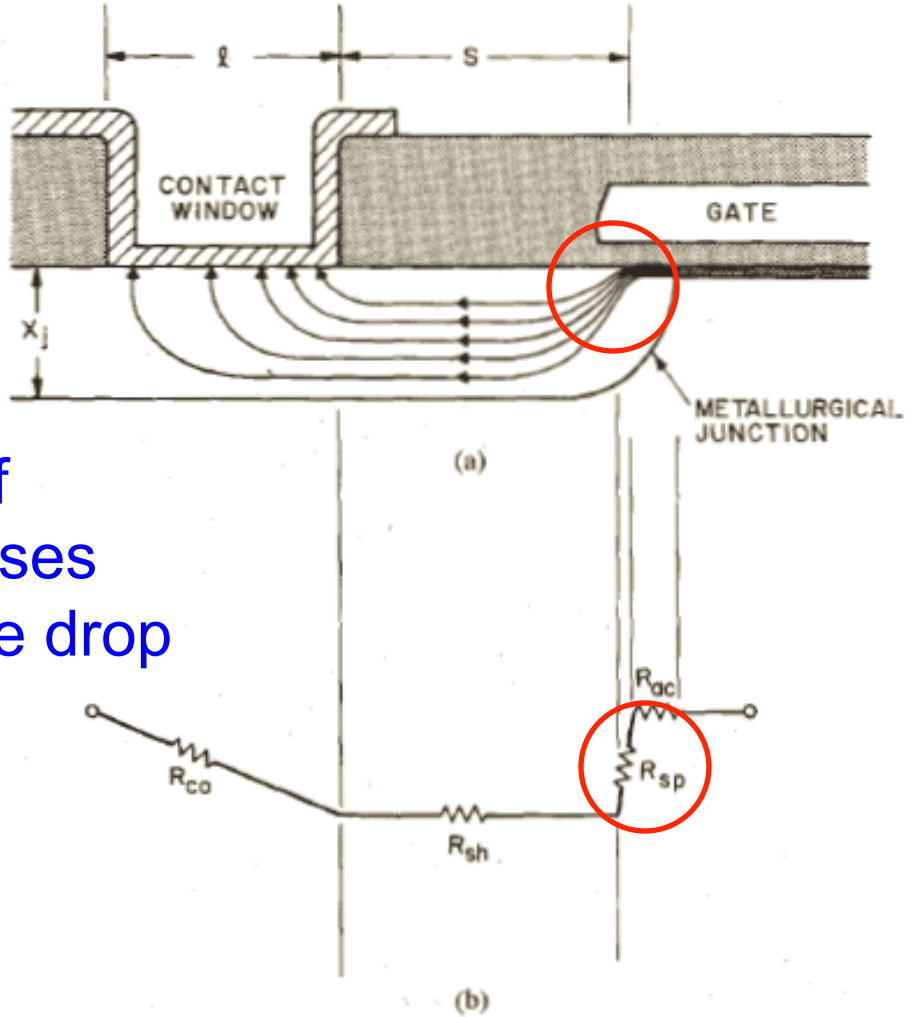
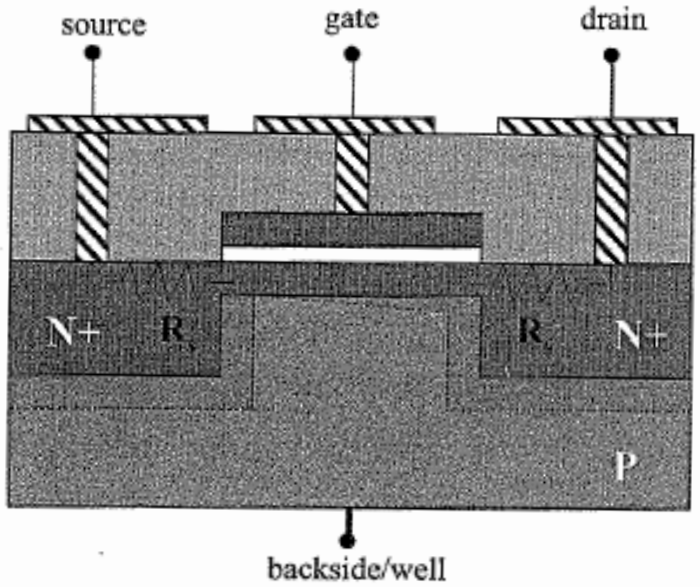
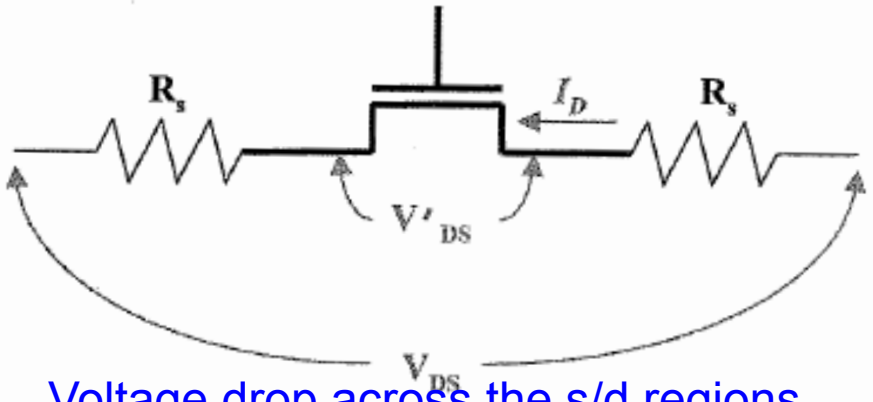


Fig. 1. Schematic diagrams for (a) current flow pattern in the source/drain region and (b) the associated resistance components.

Impact of Parasitic Resistance on MOSFET IV Characteristics





Voltage drop across the s/d regions reduces the voltage across the channel

$$V'_{DS} = V_{DS} - 2I_D R_s$$

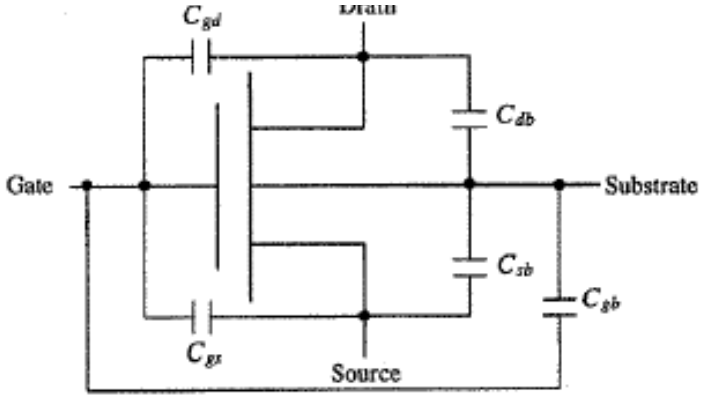
Thus the effective drain voltage is not The applied voltage V_{DS} but V'_{DS}.

$$I_D = \frac{Z\mu_{eff}C'_{OX}}{L}(V_{GS} - V_T)V'_{DS}$$

Resulting in:

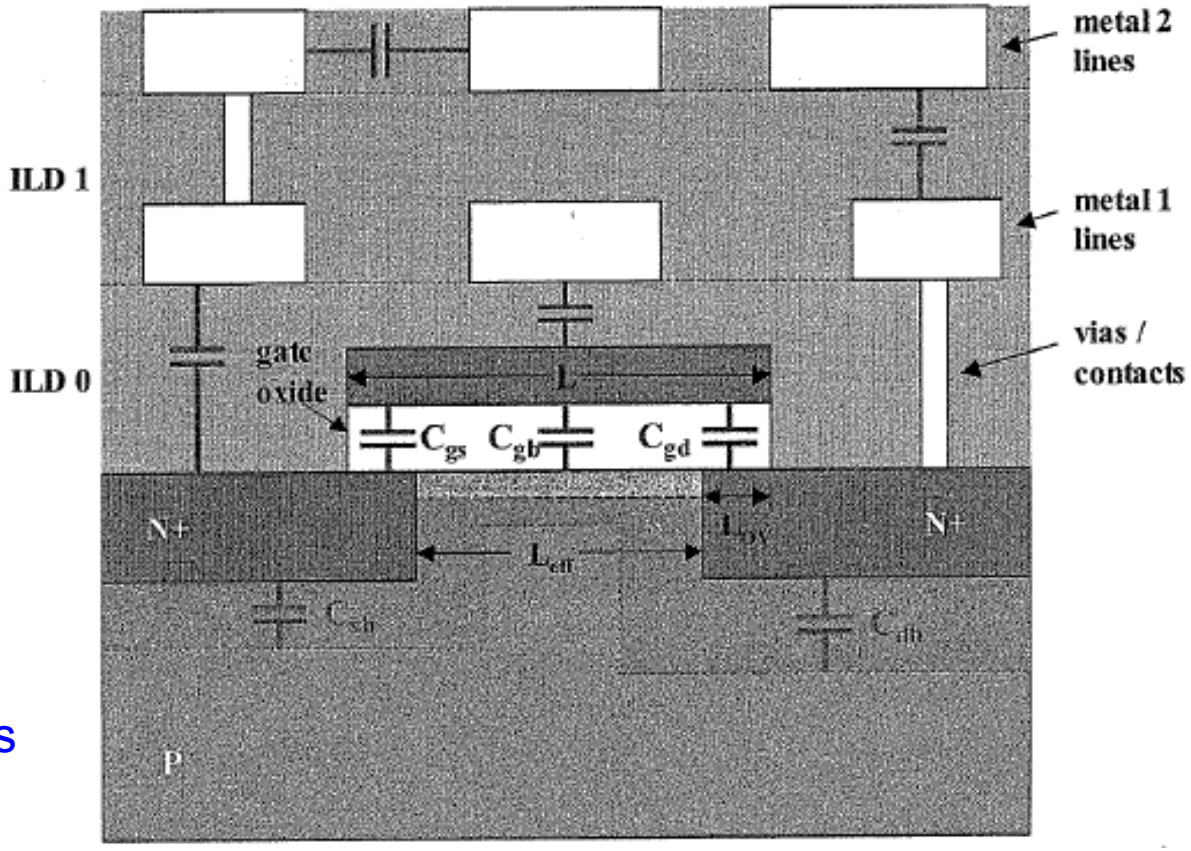
$$I_D = \frac{(Z/L)\mu_{eff}C'_{OX}}{1+\alpha_R(V_{GS}-V_T)}(V_{GS}-V_T)V_{DS} \qquad \text{where:} \quad \alpha_R = \frac{2\mu_{eff}C'_{OX}R_sZ}{L}$$

MOSFET Parasitic Capacitances

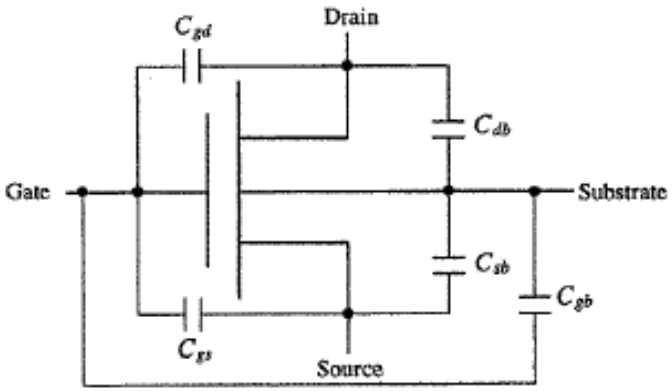


Capacitances are important for the switching speed of a MOSFET.

Every time V_G or $_{VD}$ are changed MOSFET capacitances have to be charged or discharged. Capacitances are not instantaneously charged and discharged; there will be always some time delay.
This should be minimized.



MOSFET Parasitic Capacitances: affect switching speed differently in different regimes



	Off (subthreshold)	Linear (triode)	Saturation
C_{gs}	C_{ov}	$\frac{1}{2}C_{ox}+C_{ov}$	$\frac{2}{3}C_{ox}+C_{ov}$
C_{gd}	C_{ov}	$\frac{1}{2}C_{ox}+C_{ov}$	C_{ov}
C_{gb}	C_{ox}	0	0
C_{sb}	C_j	C_j	C_j
C_{db}	C_j	C_j	C_j

MOS Capacitor:
- Inversion layer is electrically isolated from the outside world
- Inversion charge comes from R-G of minority carriers
- Capacitance depends on frequency

MOSFET:
- Inversion layer (channel) is electrically connected to source/drain
- Source is an ample supply of electrons at any practical frequency
- Charge fluctuates on either side of gate oxide (like parallel-plate)
- MOSFET gate capacitance is $\varepsilon_{ox}A/t_{ox}$ at any practical frequency

?

what about the MOS capacitor C-V frequency dependence?

where:

$$C_{ov} = \frac{\varepsilon_{ox}}{t_{ox}} ZL_{ov}$$ overlap (Miller) capacitance

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} ZL_{eff}$$ gate capacitance

$$C_j = \frac{\varepsilon_s A_j}{W}$$ PN junction capacitance

Scaling - Most Simple Model: Constant Field Scaling

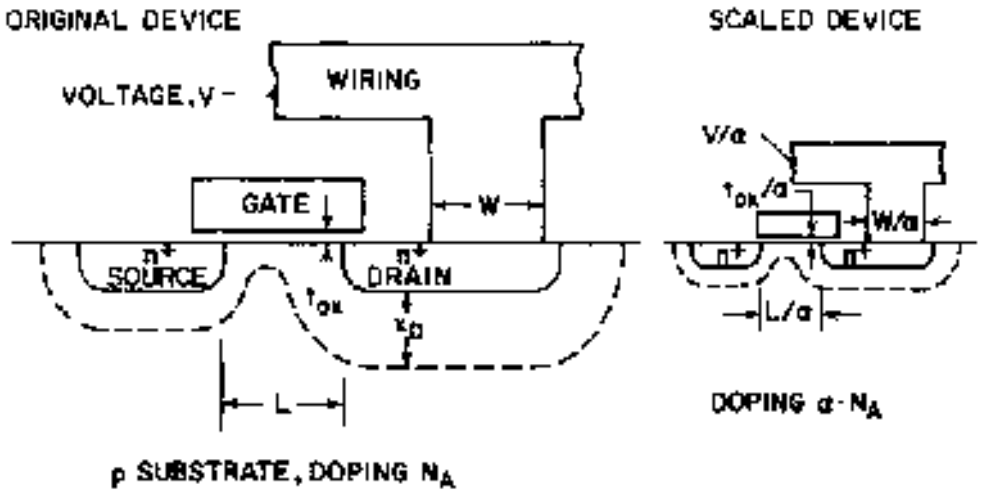


Fig. 1. Principles of constant-electric-field scaling for MOS transistors and integrated circuits.

$\mathcal{E} = V_{DD}/L$

after scaling becomes

$\mathcal{E} = (V_{DD}/\alpha)/(L/\alpha)$

…where $\alpha>1$

Table 1 Generalized Scaling Relationships

Physical Parameters	Constant-Electric Field Scaling Factor
Linear Dimensions	$1/\alpha$
Electric Field Intensity	1
Voltage (Potential)	$1/\alpha$
Impurity Concentration	α

Quantum Corrections to MOS Capacitor

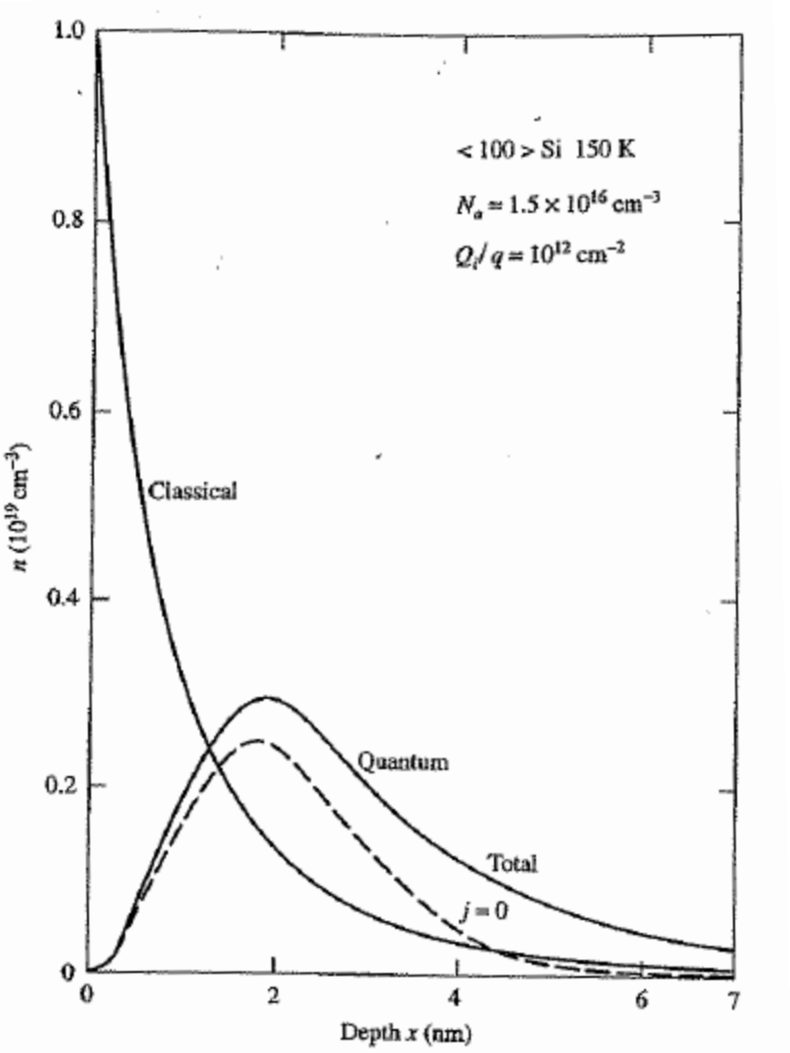
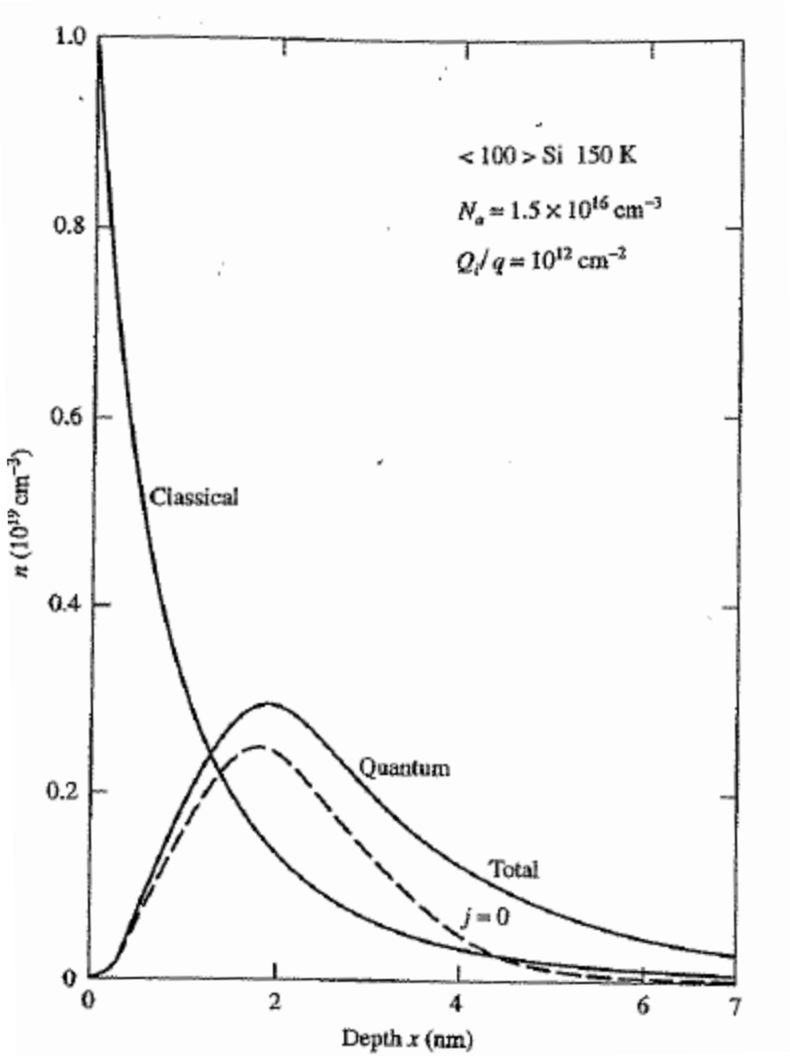


FIGURE 4.16. Classical and quantum-mechanical electron density versus depth for a ⟨100⟩ silicon inversion layer. The dashed curve shows the electron density distribution for the lowest subband. (After Stern, 1974.)



Important for the description of the surface scattering events in the channel (impact on mobility)

Quantum Corrections to MOS Capacitor

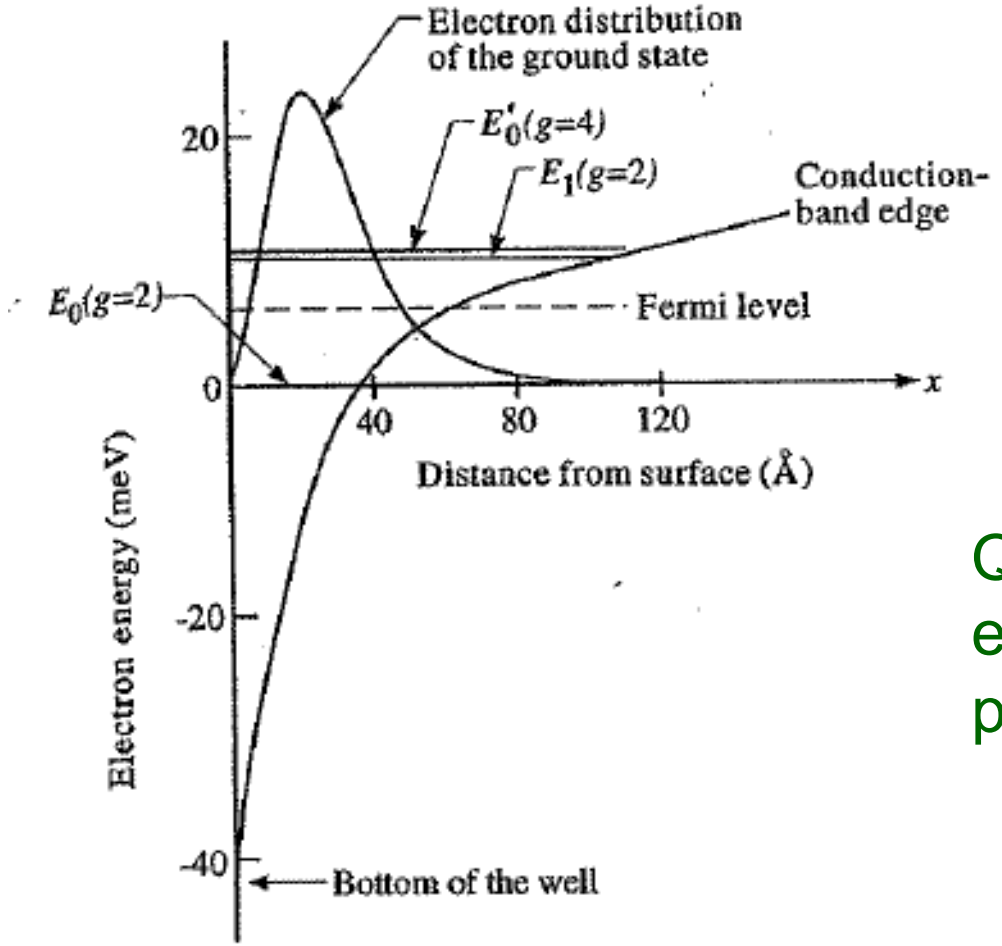


FIGURE 4.15. An example of quantum-mechanically calculated band bending and energy levels of inversion-layer electrons near the surface of an MOS device. The ground state is about 40 meV above the bottom of the conduction band at the surface. The dashed line indicates the Fermi level for 10^{12} electrons/cm^2 in the inversion layer. (After Stern and Howard, 1967.)

Quantum mechanics enters the MOSFET physics