MOS Capacitors

ECE 5205 Spring 2014

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MOS Capacitor

Contents

- ideal MOS Capacitor (accumulation, depletion, inversion)
- Threshold voltage for constant substrate doping
- C-V characteristics
- Real MOS Diode (work fct, built-in charge, flat band voltaged)
- Nonequilibrium analysis (substrate bias, body effect)
- non-uniform channel doping
- Gated diode

Threshold Adjust – Ion Implantation

- Make adjustments to device thresholds
  - Compensate for oxide trapped charge
  - Substrate doping may be fixed by other considerations
- **Shallow Implant** B or P at depth near semiconductor surface
- Forms "sheet" **(δ doping)** of ionized donors/acceptors (ideal distribution)
- Voltage shift due to charge sheet and gate capacitance
- Example: $5x10^{11}/cm^2$ B with 100 nm oxide

$$V = \frac{Q_{implant}}{C_i}$$

$$V = \frac{Q_{implant}}{C_i} = \frac{1.6x10^{-19} C/ion * 5x10^{11} ions/cm^2}{(3.9 * 8.85x10^{-14} F/cm^2 / 10^{-5} cm)} \approx 2Volts$$

Threshold Voltage for Non-uniform Channel Doping

Threshold can be adjusted by an additional channel dopant implant with realistic distribution as shown below.

The impurity profile in ion-implanted devices resemble a Gaussian distribution with maximum at a projected range R_p and with standard deviation ΔR_p, D_I is the ion does per unit area.

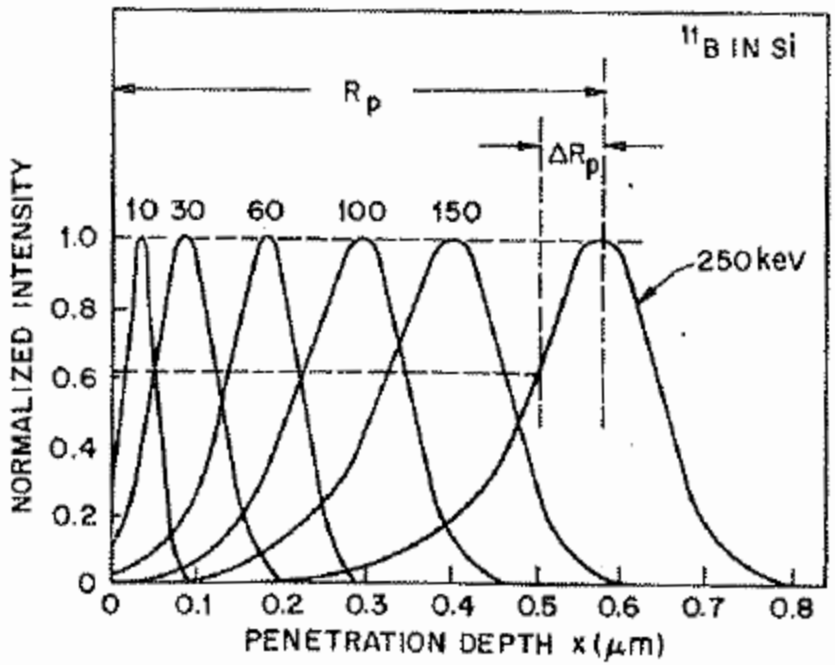


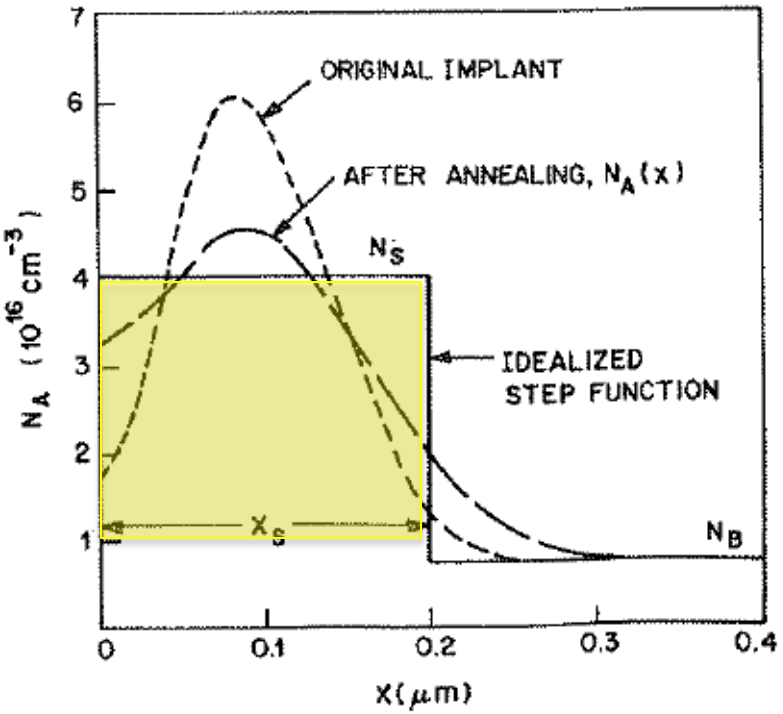
Fig. 21 Normalized range distribution of boron in silicon for different implantation energies. (After Wittmack, Maul, and Schulz, Ref. 34.)

$$N(x) = \frac{D_I}{\sqrt{2\pi}\,\Delta R_p} \exp\left[-\frac{(x - R_p)^2}{2(\Delta R_p)^2}\right]$$

Threshold Voltage for Non-uniform Channel Doping

To derive V_T due to ion implantation, we consider an idealized step-doping. The original implant is altered after thermal anneal and the annealed profile is approximated by the step function with depth x_s, such that

$$(N_s - N_B)x_s = \int_0^\infty [N_A(x) - N_B]dx = D_I$$



For the limiting case of a delta function on negative charge (ionized boron acceptors) localized at the Si/$Si0_2$ interface, the charge is equivalent to a reduction of the fixed oxide charge by an amount qD_I. Therefore:

$$V_T = V_{FB} + V_C + 2|\psi_B| + \frac{1}{C_{ox}}\sqrt{2\varepsilon_s qN_A(2|\psi_B| + V_{subs})} + \frac{qD_I}{C_{ox}}$$

$$\Delta V_T = V_T(D_I) - V_T(D_I = 0) = \frac{qD_I}{C_{ox}}$$

Threshold Voltage for Non-uniform Channel Doping

For a wide x_s (i.e. when $W_m < x_s$), the surface region can be considered a uniformely doped region with concentration N_s and we can use the standard definition by replacing N_b with N_s. (trivial case).

If $W_m > x_s$, the depletion layer width and the voltage drop across the oxide can be obtained from Poisson's equation with a high-low step doping profile:

$$W_m = \sqrt{\frac{2\varepsilon_s}{qN_B}[\psi_s + V_{subs} - \frac{qx_s^2}{2\varepsilon_s}(N_s - N_B)\}}^{1/2}$$

$$V_{ox} = \frac{q}{C_{ox}}\int_0^{Wm} N_A(x)\,dx =$$

$$= \frac{q}{C_{ox}}[N_B W_m + D_I]$$

$$V_T = V_{FB} + \psi_s + \frac{\sqrt{2\varepsilon_s qN_B}}{C_{ox}}(V_{subs} + \psi_s - \frac{qx_s}{2\varepsilon_s}D_I)^{1/2} + \frac{qD_I}{C_{ox}}$$

Recall from pn junction Lecture:

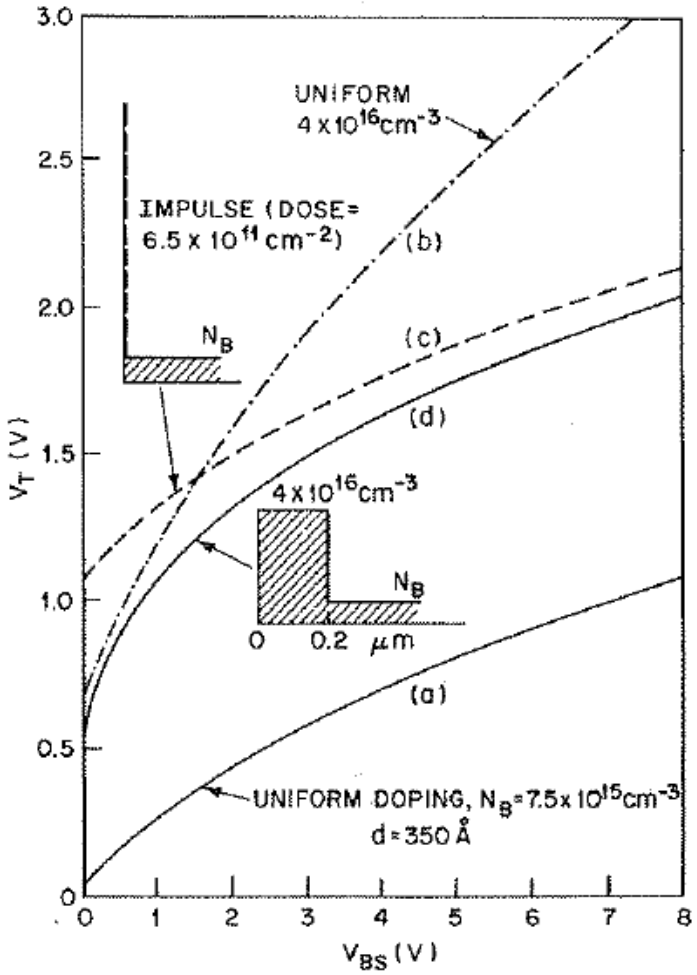
$$\psi(x) = \frac{eN_A}{2\varepsilon}(x_p + x)^2$$

The last equation indicates that when $(V_{BS}+\psi_s)$ becomes much larger than $qx_sD_I/2\varepsilon_s$, V_T for the step profiles approaches that for the delta-function profile at the interface.

$$V_T = V_{FB} + V_C + 2|\psi_B| + \frac{1}{C_{ox}}\sqrt{2\varepsilon_s qN_A(2|\psi_B| + V_{subs})} + \frac{qD_I}{C_{ox}}$$

Threshold Voltage for Non-uniform Channel Doping

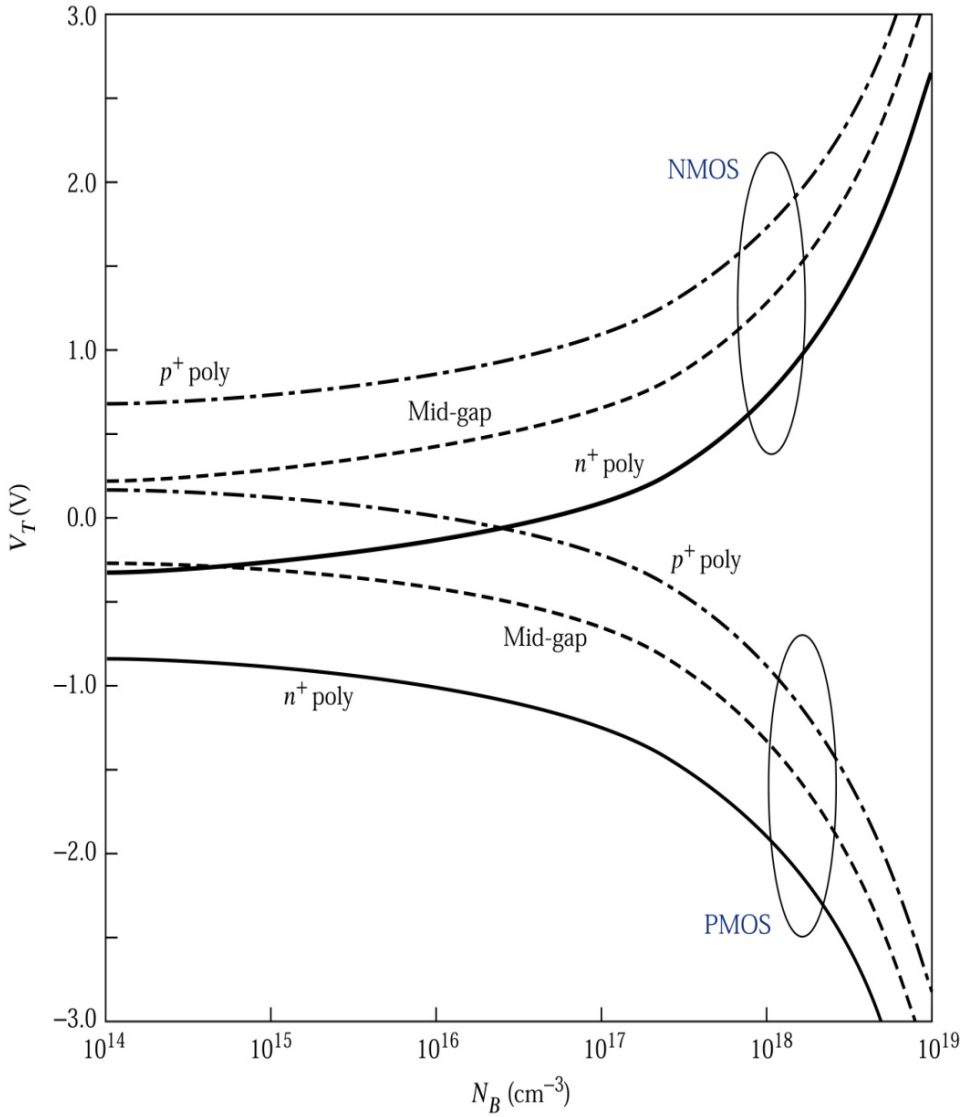
For a wide x_s (i.e. when $W_m < x_s$), the surface region can be considered a uniformely doped region with concentration N_s and we can use the standard definition by replacing N_a with N_s.



Generally, it is desirable to have low substrate sensitivity, i.e. weak dependence of V_T on V_{sub}, i.e. small γ.

The curves c) and d) show that a shallow channel implant with an appropriate dose can raise the V_T while maintaining a low substrate sensitivity.

threshold voltage control - summary



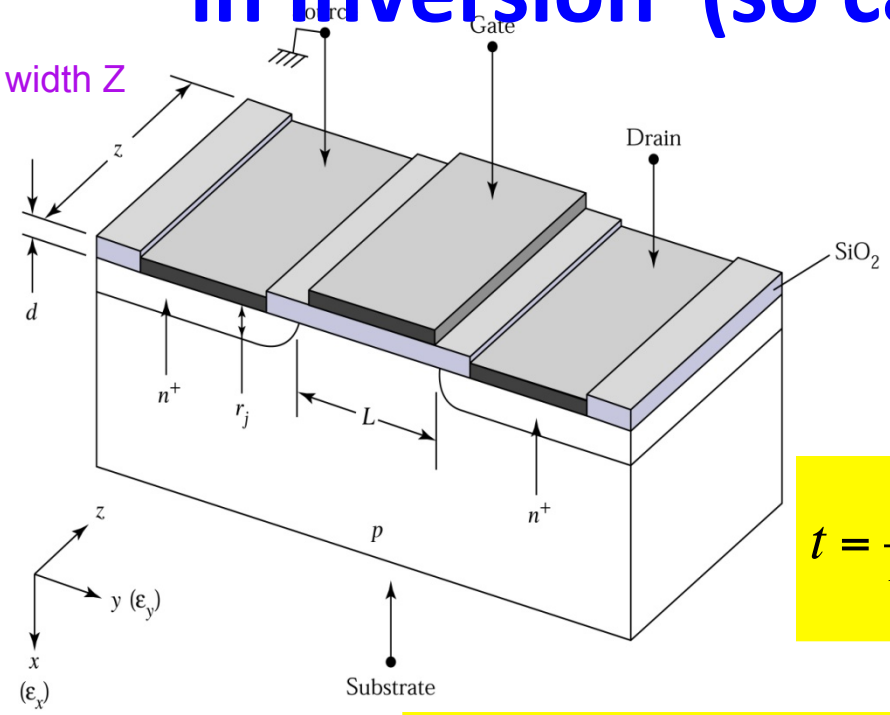
control of the threshold voltage:

$$V_{th} = V_{FB} + 2\psi_B + \frac{\sqrt{2\varepsilon_S q N_A (2\psi_B + V_{BS})}}{C_{ox}}$$

by:

- oxide thickness
- dielectric constant of oxide
- doping of the bulk
- doping of the polysilicon
- bulk-source voltage
- Work function of the gate electrode

First Simple Estimate of MOSFET Current in Inversion (so called linear regime)



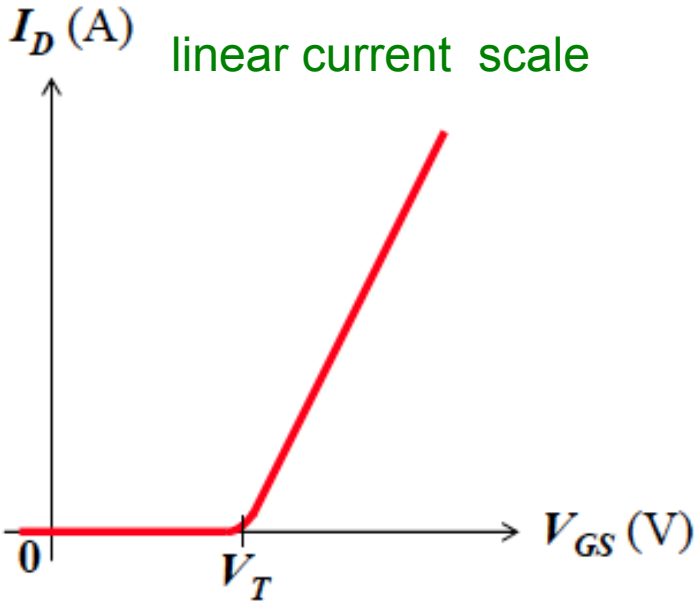
$$I_D = \frac{Q}{t}$$

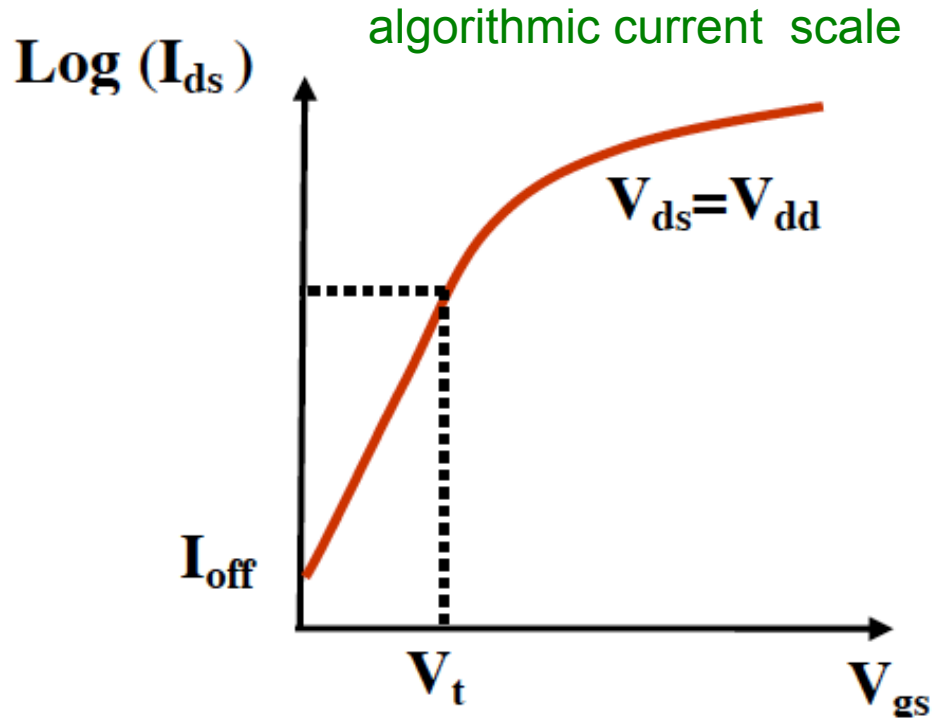
$$t = \frac{L}{v_d} = \frac{L}{E_{lat} \cdot \mu_{eff}} = \frac{L}{\mu_{eff}(V_D - V_S)/L} = \frac{L^2}{V_{DS} \cdot \mu_{eff}}$$

$$Q_n = C_{ox}^{tot} V = \frac{\varepsilon_{ox} A}{t_{ox}}(V_{GS} - V_T) = \frac{\varepsilon_{ox} ZL}{t_{ox}}(V_{GS} - V_T) = ZLC_{ox}(V_{GS} - V_T)$$

$$I_D = \frac{Z}{L}\mu_{eff} C_{ox}(V_{GS} - V_T) \cdot V_{DS}$$

MOSFET Current as a Function of the Gate Bias





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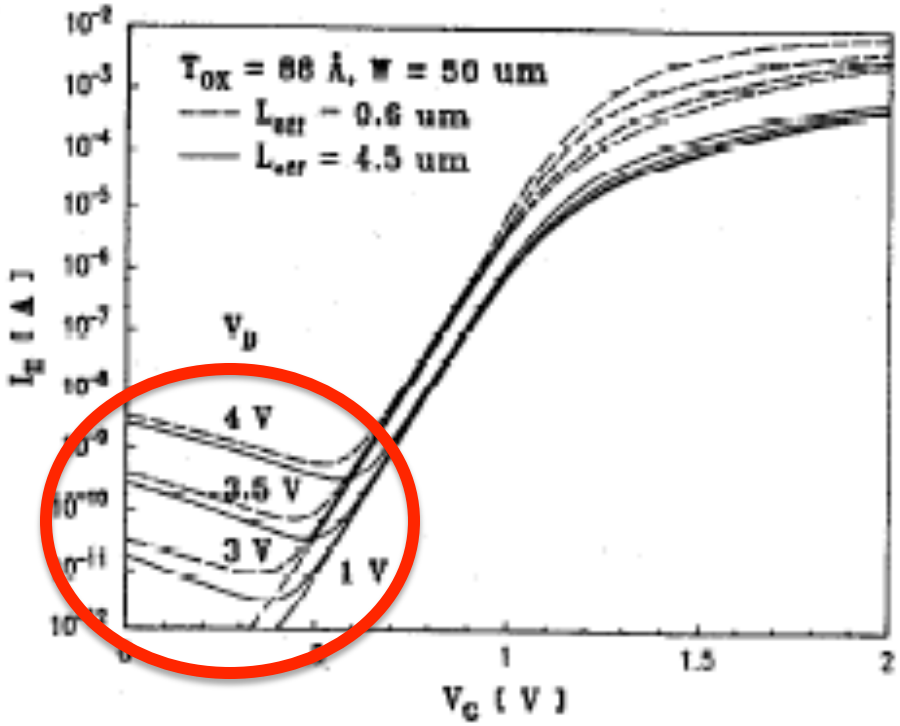
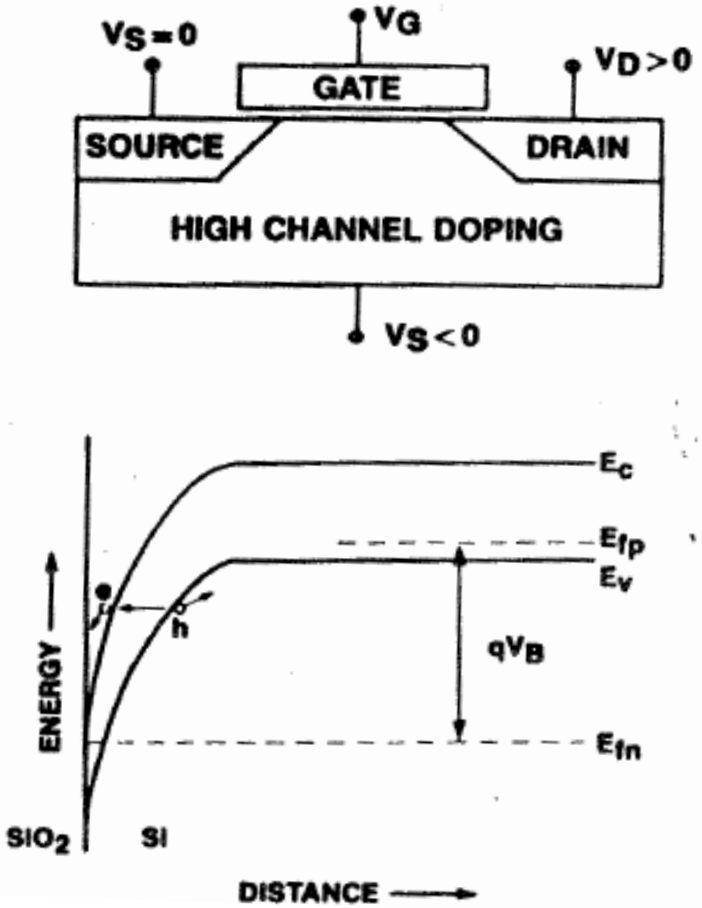
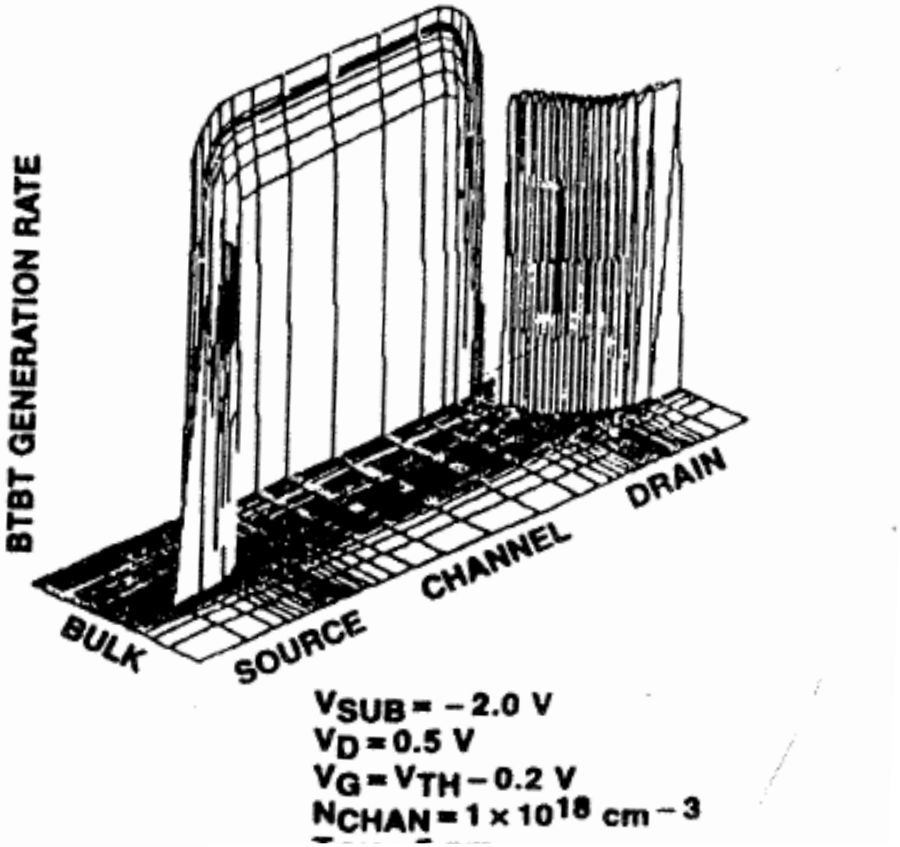
MOSFET Current as a Function of the Gate Bias: New Phenomenon observed in the new generation of transistors beginning of 1990's



Band-to-Band Tunneling in MOS-Diode V_{sub}<0

BTBT Origin of MOSFET Leakage Currents

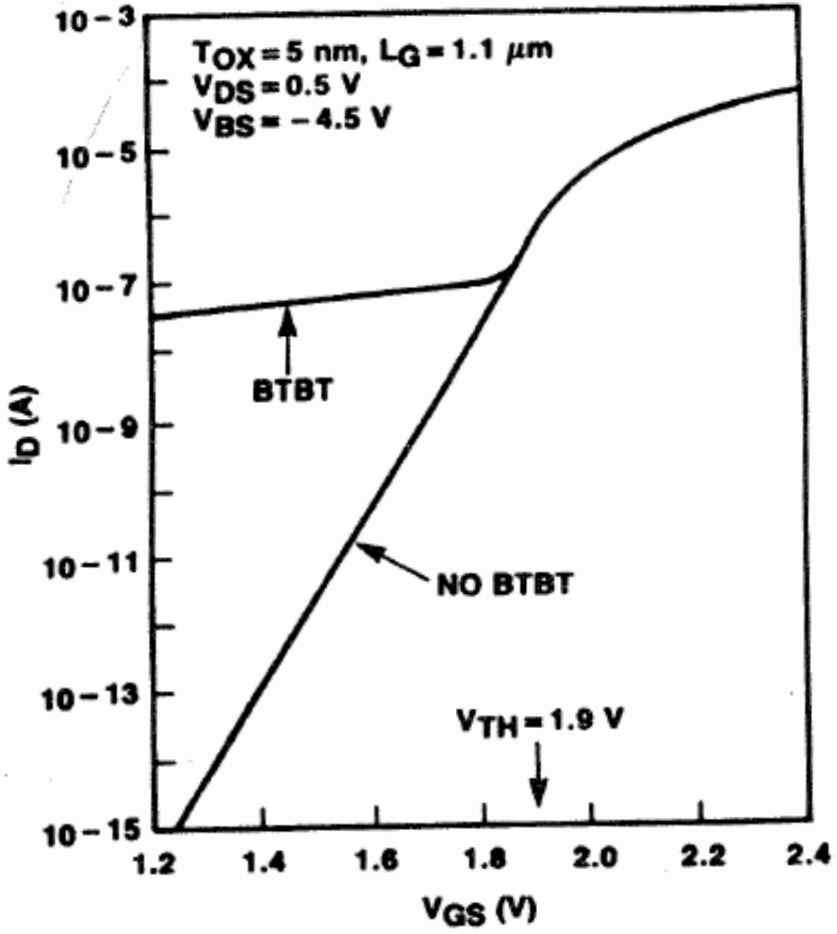




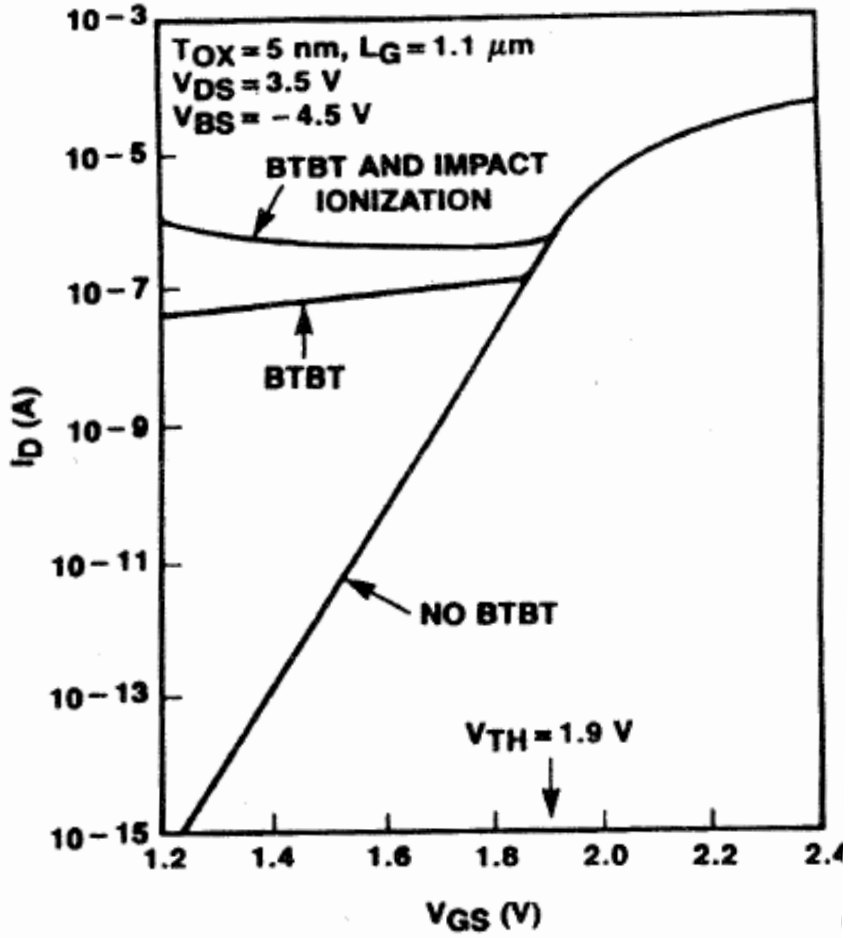
Orlowski et al "The Combined Effects of Band-to-Band Tunneling and Impact Ionization the Off Regime of an LDD MOSFET", Electron Device Letters (11), 1990, p.593

Band-to-Band Tunneling in MOS-Diode $V_{sub}<0$

Impact of BTBT and Impact Ionization Effects on MOSFET Leakage Currents



M. Orlowski et al, Electron, Device Letters (11), 1990, p.593



M.Orlowski et al, VLSI Technology Symposium 1990, p. 67

Band-to-Band Tunneling in MOS-Diode V_{sub}<0

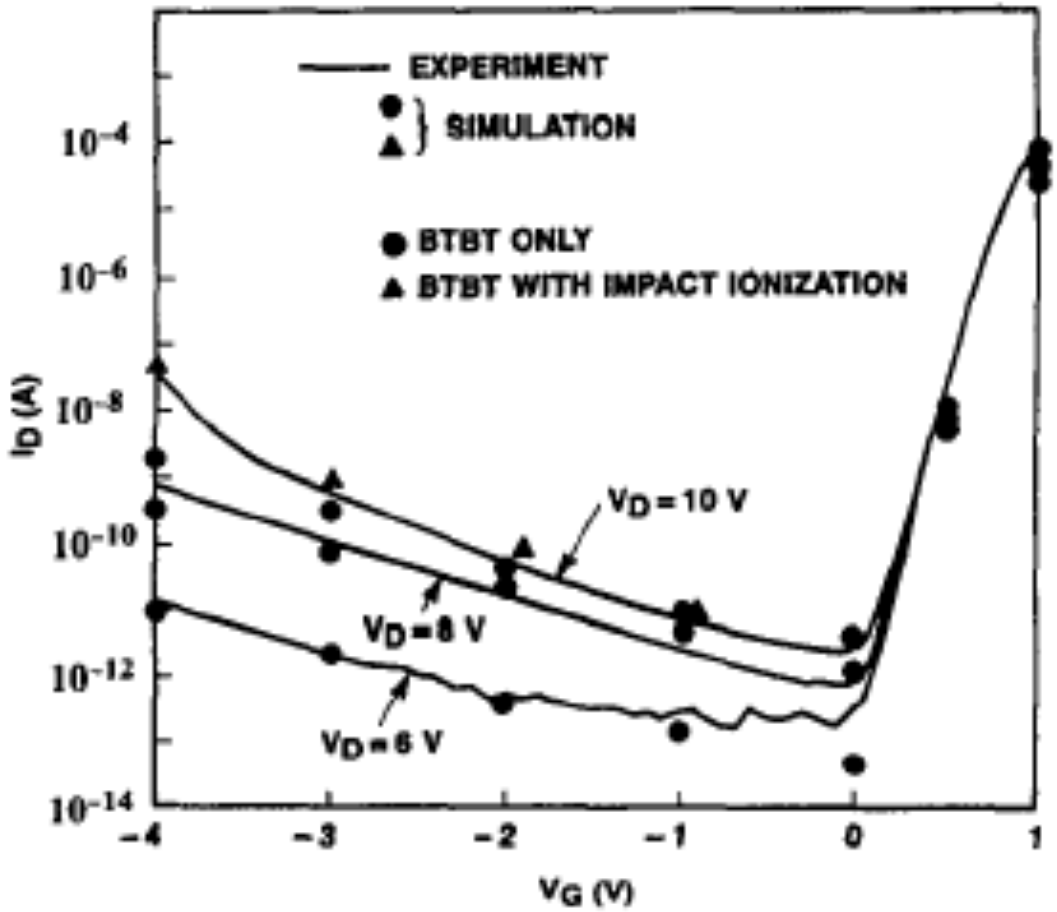
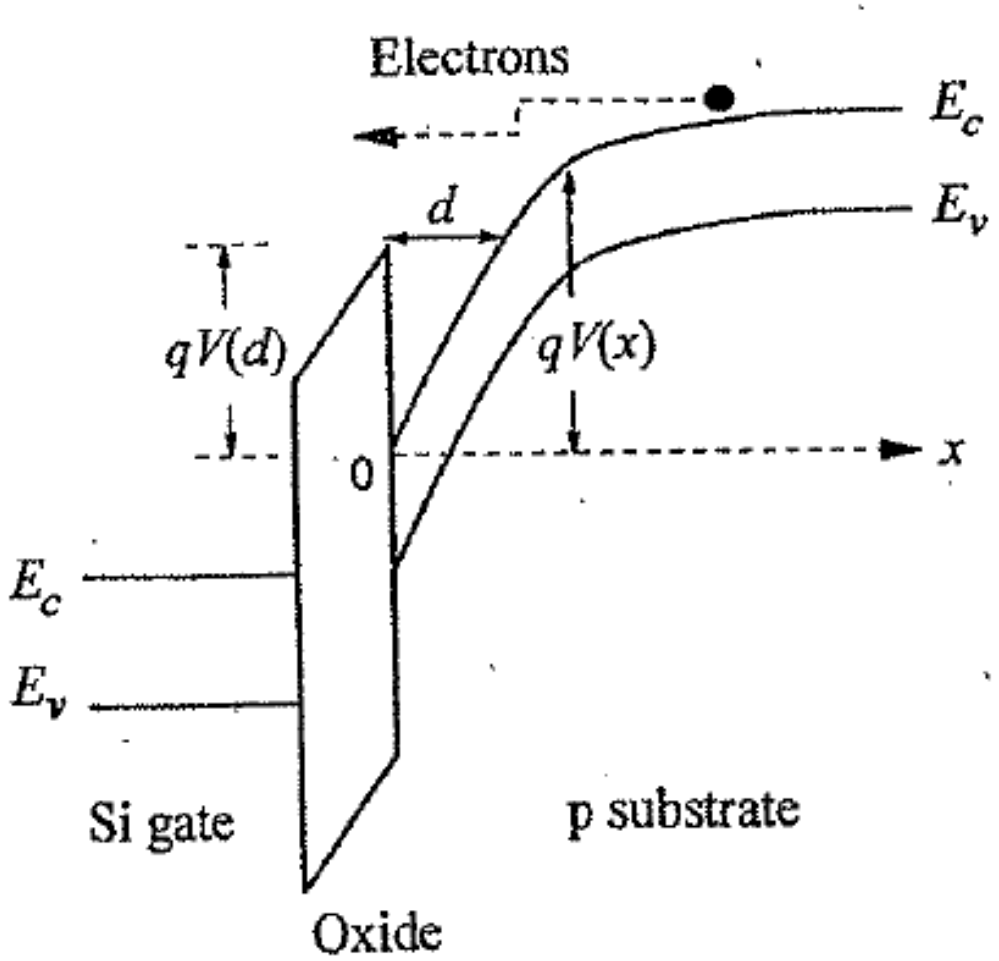


Fig. 1. Drain leakage current as a function of the gate and drain bias. Full dots denote simulation results invoking BTBT model only. Triangles denote simulation results invoking both BTBT and impact ionization models. For drain bias smaller than 10 V both simulation modes give very similar results.

Orlowski et al, Electron, Device Letters (11), 1990, p.593
M.Orlowski et al, VLSI Technology Symposium 1990, p. 67

Injection of "Hot" Electrons from Si into SiO_2 and gate electrode (I_g gate leakage current)



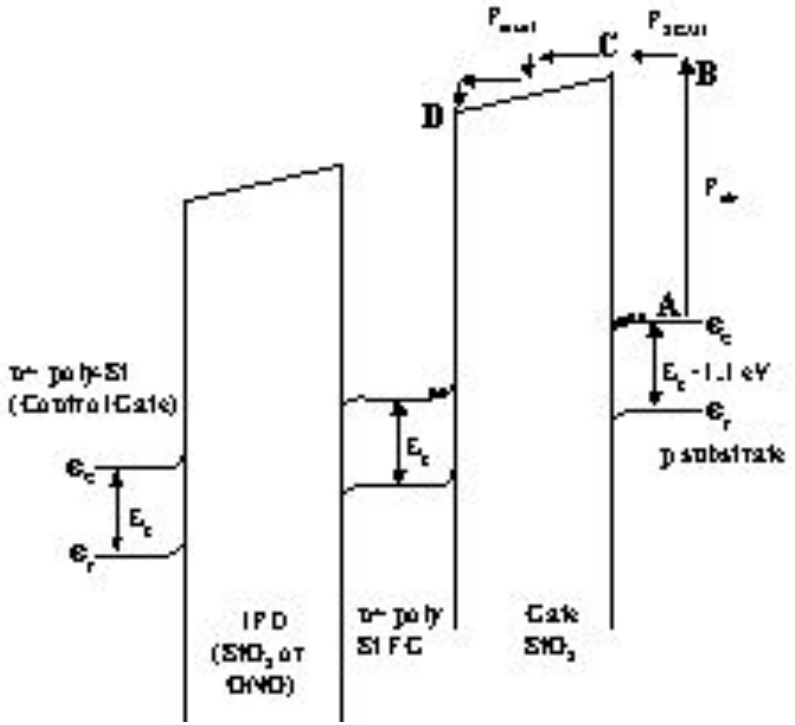
Lucky Electron Model

The lucky-electron approach of modeling the hot-electron distribution was originated by Shockley. Conceptually, the lucky-electron model can be described as follows. In order for hot-electrons to reach the gate, the hot-electrons must gain sufficient kinetic energy from the lateral channel field (E_{lat}) and have its momentum redirected towards the Si-SiO_2 interface in order to surmount the SiO_2 energy barrier . Figure below shows the concepts involved in the lucky-electron model. The three events involved in the lucky-electron model are:

A - B Event: A channel electron has to gain energy from the E_{lat} and become "hot". The hot-electron momentum has to be re-directed towards the Si-SiO_2 interface. The probability associated with this process is defined as the probability of an electron having enough normal momentum to surmount the Si-SiO_2 potential barrier height.

B - C Event: Once the hot-electron is re-directed, it must not suffer any energy robbing collisions. The probability associated with this event is P_{SEMI}. P_{SEMI} is defined as the probability of an electron traveling to the Si-SiO_2 interface without suffering any collisions.

C - D Event: While in transit from the Si-SiO_2 interface to the floating gate, the electron must not suffer any collisions in the oxide potential well. The probability associated with this event is P_{insul} and is defined as the probability of an electron suffering no collision in the oxide potential well.

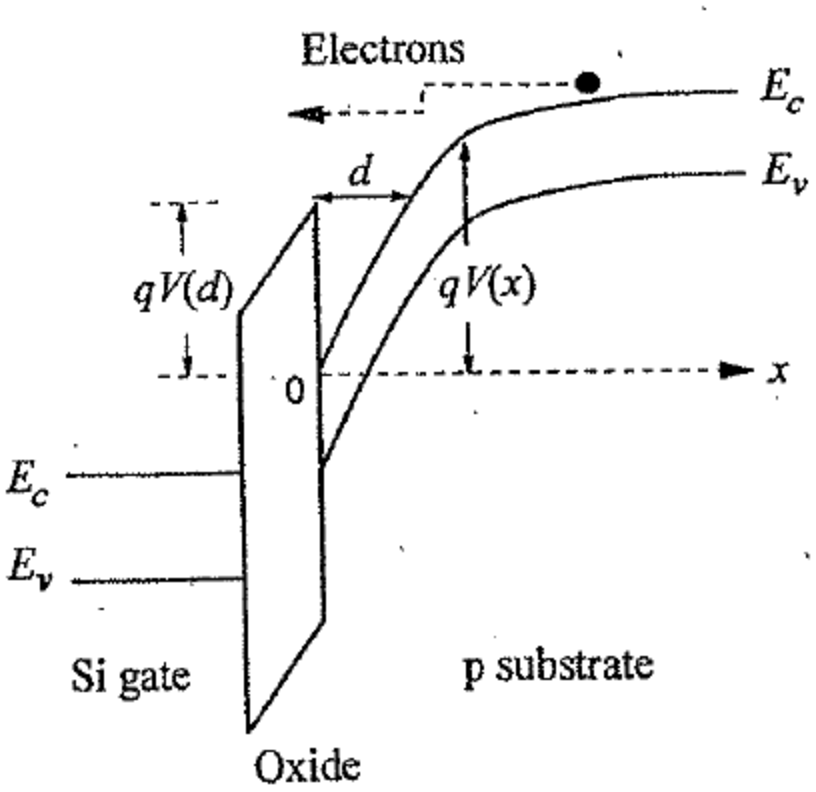


Since these three probabilities are statistically independent, the resultant probability is the product of the probability for each individual event. The gate current is given by

$$I_g = I_{ds} \int_0^{L_{eff}} P_{\Phi b} \cdot P_{semi} \cdot P_{ox} \frac{dx}{\lambda_r}$$

where,
λ_r = Momentum re-direction scattering mean free path (typically about 100A)
L_{eff} = Effective channel length of the transistor (cm)
I_{ds} = Drain-source current (A)
dx/λ_r redirection probability
The charge on the floating gate changes the threshold voltage (V_T) of the floating gate transistor by

Injection of Hot Electrons from Si into SiO_2 and gate electrode (I_g gate leakage current)



Si-SiO_2 barrier for electrons is 3.1 eV

How much is it for holes?

For holes ϕ_B is 4.8 eV .

$$I_g = C\left(\frac{\lambda E_m}{\phi_B}\right)^2 \exp\left(-\frac{\phi_B}{\lambda E_m}\right)$$

ϕ_B Si-SiO_2 barrier for electrons is 3.1 eV
E_m = peak lateral electric field at the oxide
λ electron free mean path

$$P = A\exp\left(-\frac{d}{\lambda}\right)$$

$$d = \phi_B / E_m$$

Probability that a hot electron at a distance d from the interface will be injected into the oxide.

"Lucky Electron" model

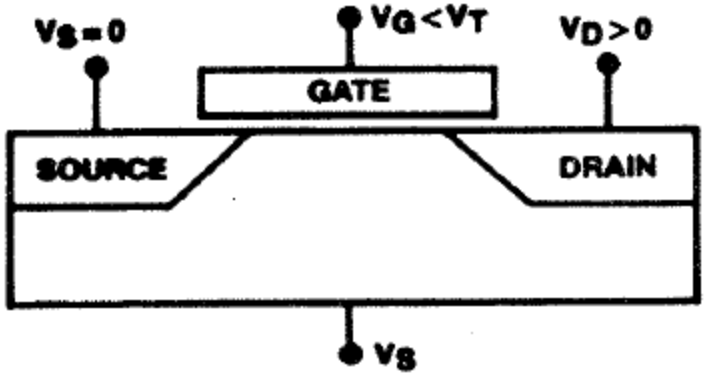
Gate Leakage Current I_g and the Injected Charge Q_{inj}

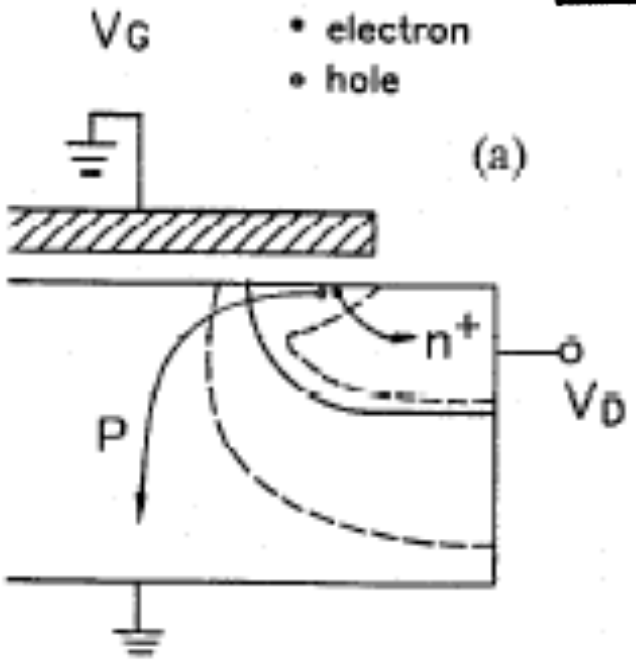
$$I_g = C\left(\frac{\lambda E_m}{\phi_B}\right)^2 \exp\left(-\frac{\phi_B}{\lambda E_m}\right)$$

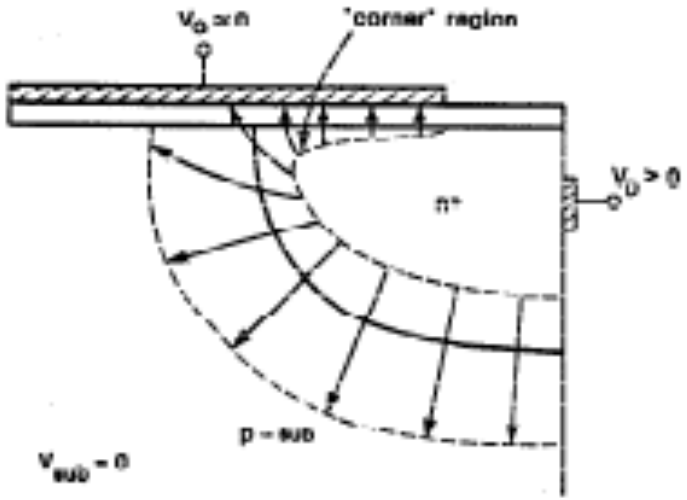
$$Q_{inj} = \int_0^{t_0} I_g(t)\,dt$$

Gated pn-Diode on the Drain Side

For small gate bias (zero or well below the threshold voltage) with substrate grounded and high drain bias a significant drain leakage can be observed. This leakage current is caused by band-to-band tunneling. The structure responsible for the effect is the gated diode structure.







Gated Diode

Since the gate is biased at negative voltage while a positive voltage is applied to the n+ region of the pn junction, a very high vertical silicon field appears in the gate-to-junction overlap region where the doping is sufficiently low. Because holes are drained away by the n^+-to-substrate field (the contact at the p-side of the junction), the n-type junction cannot be inverted and the device enters the deep-depletion mode. This implies that the energy band bending becomes larger than the energy gap, which allows valence electrons to directly tunnel to the conduction band of the n-type region. These electrons are swept to the drain contact due to the positive drain bias. On the other hand, the corresponding holes generated by BTBT are drawn to the substrate to form a large bulk current (typically a few hundred nano-amperes for a state-of-the-art memory cell).

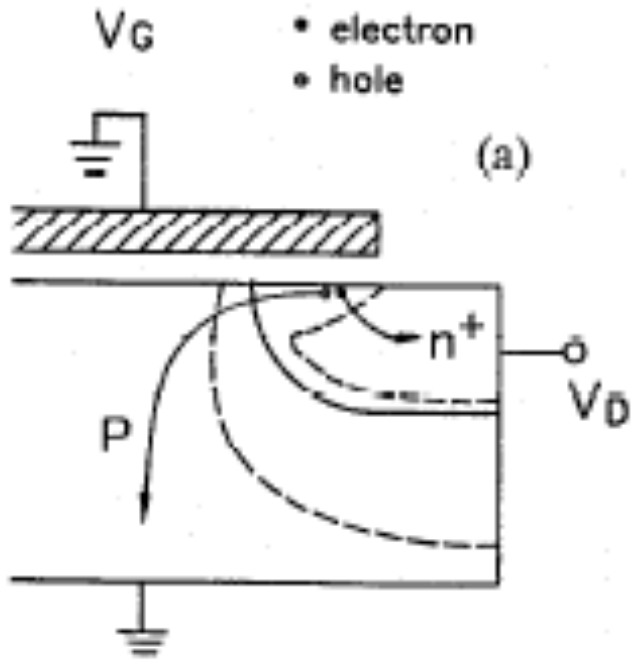
Looking ahead: If this mechanism is used in NVM memory cell for the erasure operation, this implies that the current to be supplied from the junction supply voltage can grow significantly large when erasing a large number of cells simultaneously. When using a large drain bias, this current has to be supplied from a charge pump, which creates limitations for the memory sector size. In addition, large substrate current can cause significant potential drops in the substrate of the memory array and increase the risk for forward biasing of other junctions.

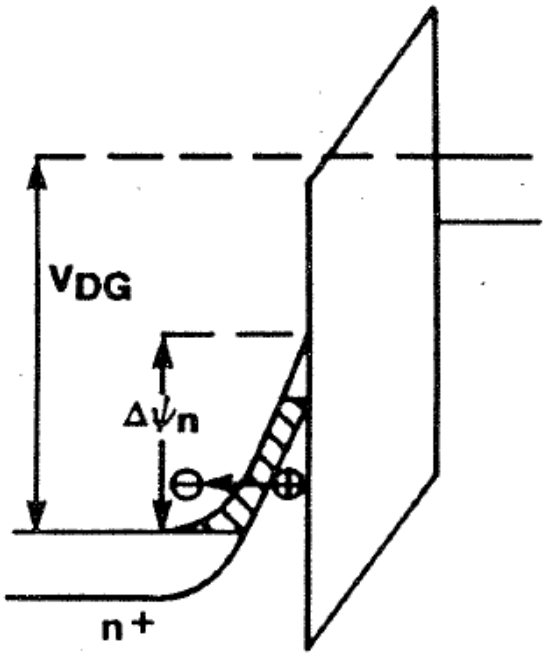
Moreover, some of the holes are heated by the junction field and are injected into the gate oxide, which is known to lead to severe reliability problems:

1) degradation of oxide,
2) lowering of endurance,
3)enhanced disturb effects

Gated Diode

The electric field can be very high in the drain region for V_D high and V_G=0. At the same time the quasi Fermi-levels are sufficiently separated by the reverse bias and the band bending exceeds the energy gap of the semiconductor. If the band bending is steep enough (high enough fields) band-to-band tunneling becomes appreciable.



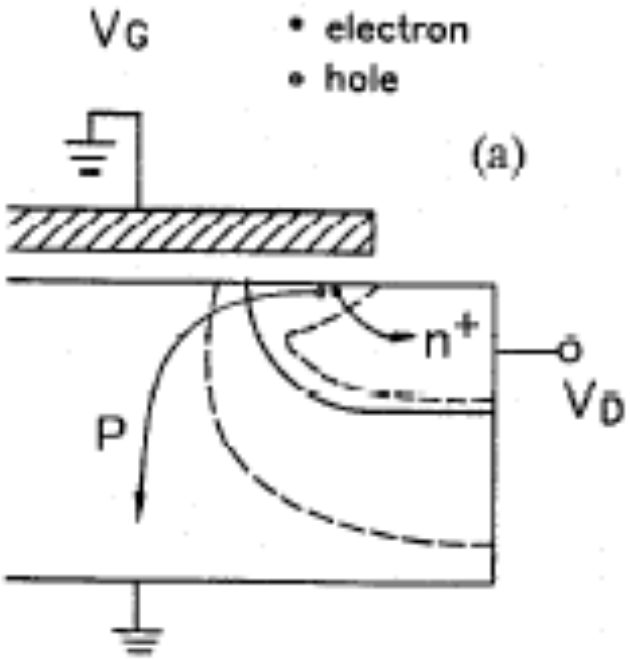


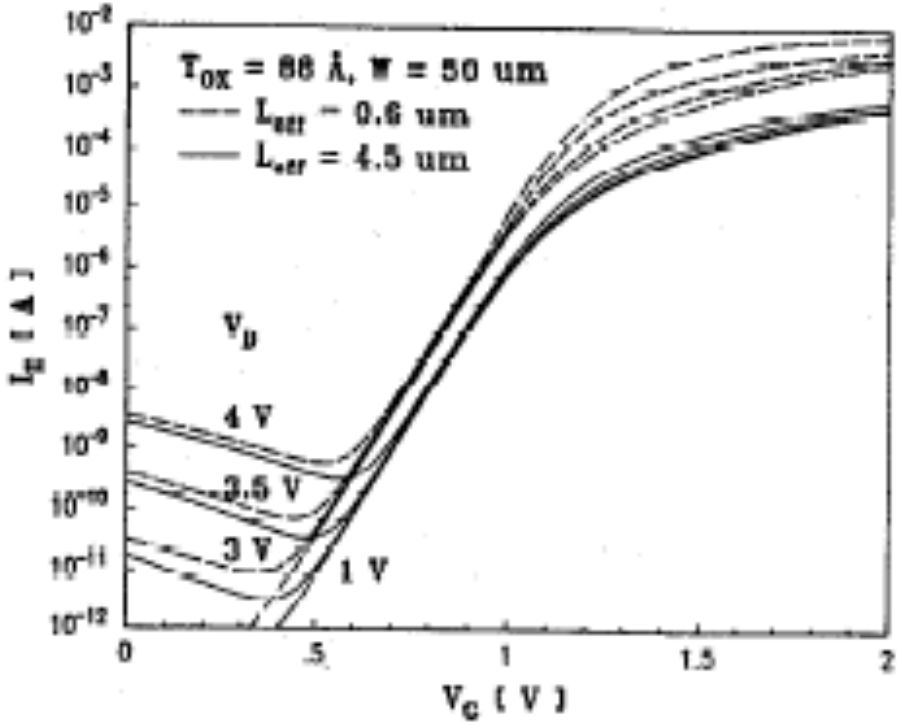
VERTICAL ENERGY BAND DIAGRAM IN THE GATE-DRAIN OVERLAP REGION

Gated Diode

The result is high substrate and high leakage current. At fixed drain voltage, the leakage current increases with decreasing gate bias.

$V_G=0<V_T$





Gated Diode

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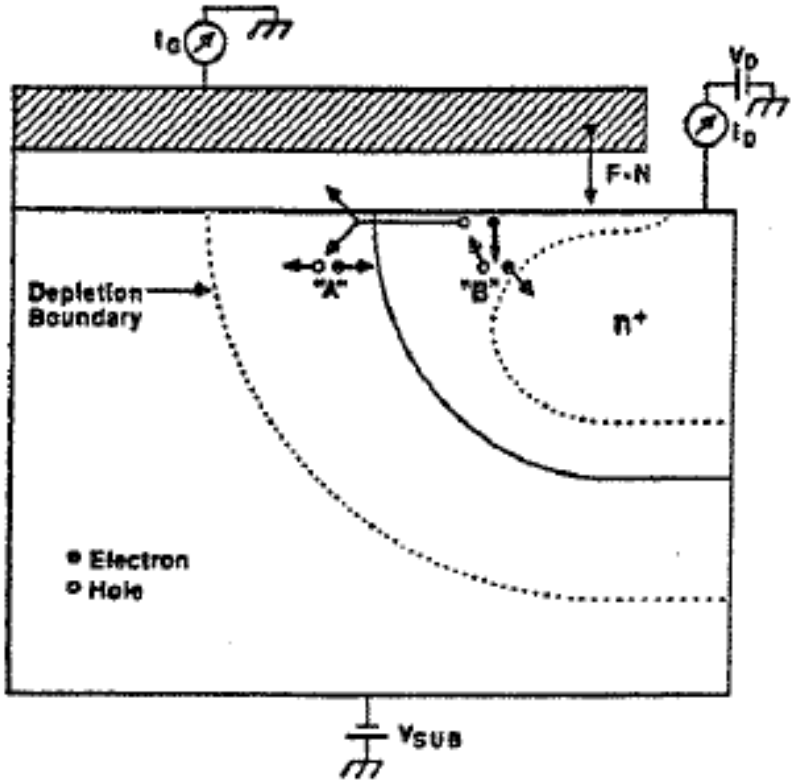
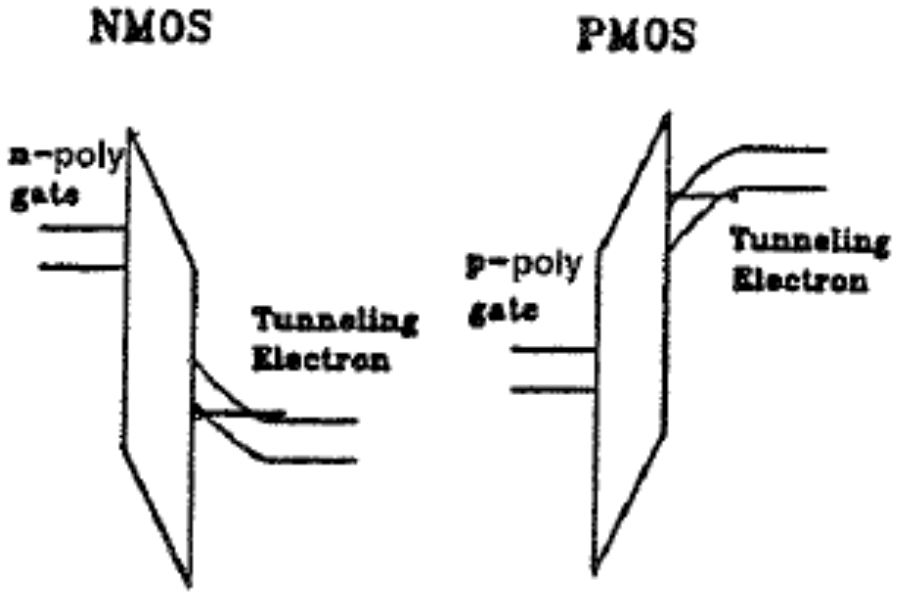
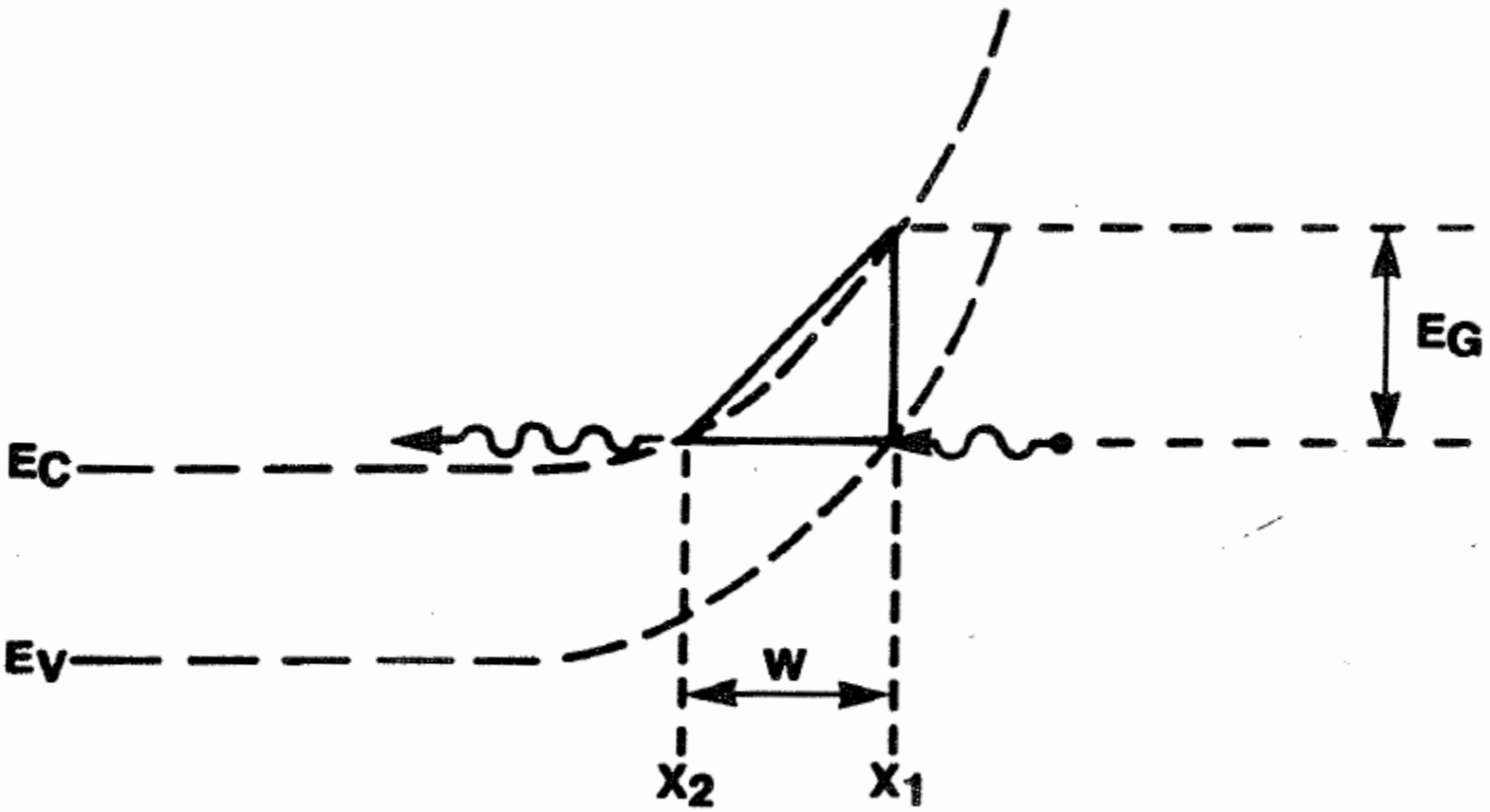




1-D APPROXIMATION

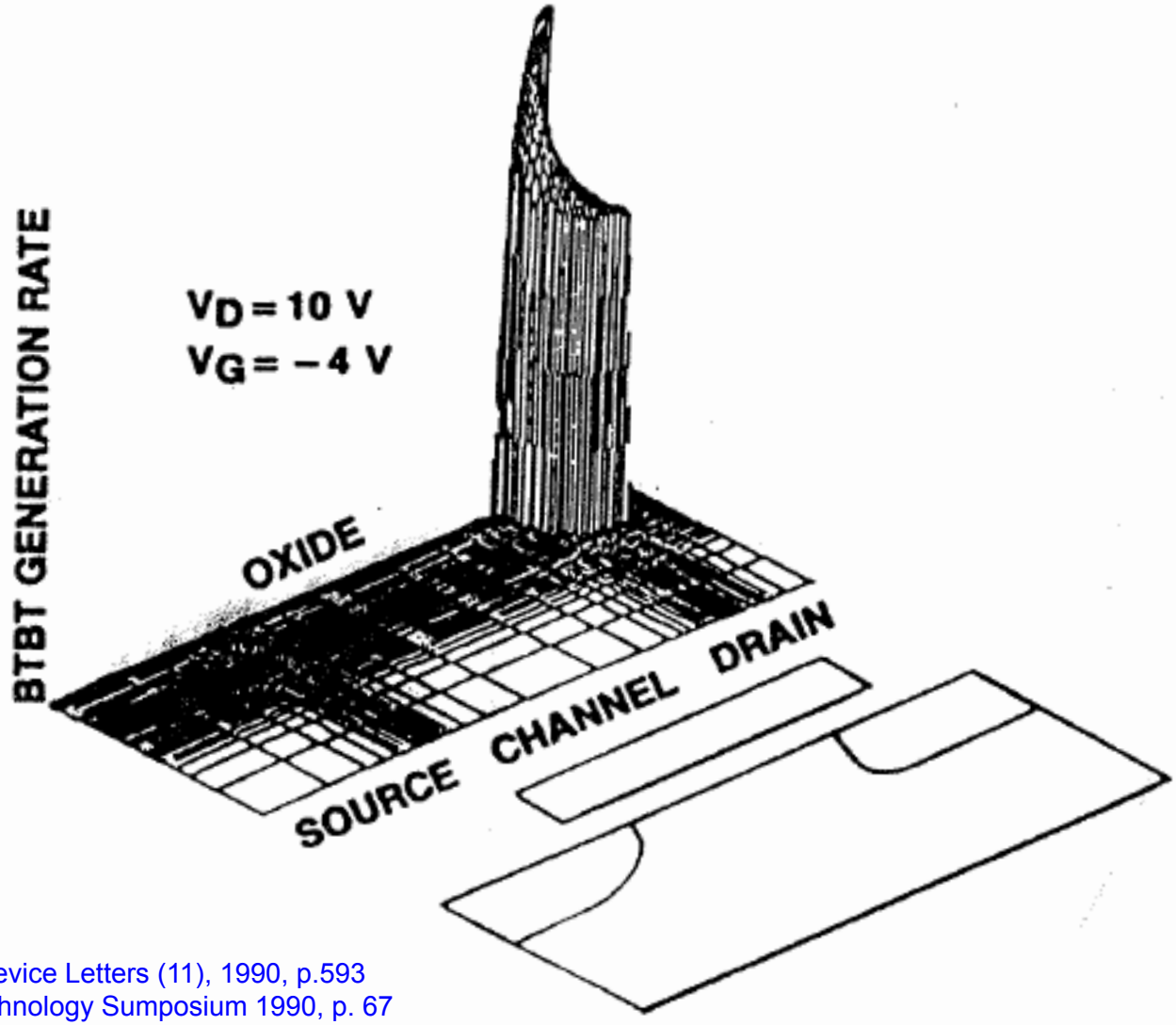


TUNNEL CURRENT $\sim E_S$ EXP $(-B/E_S)$

TUNNEL PROBABILITY $\sim |[\psi(X_2)]/[\psi(X_1)]|^2$

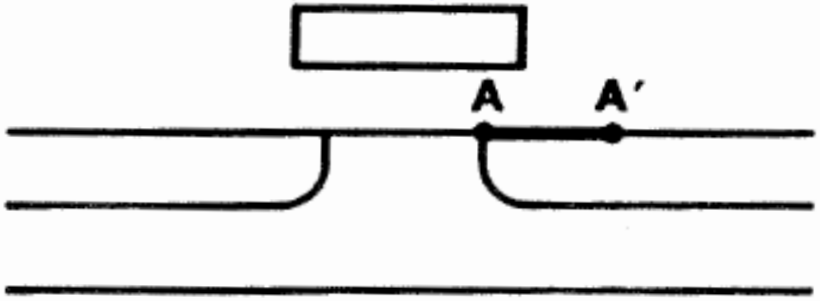
ψ QUANTUM MECHANICAL WAVE FUNCTION

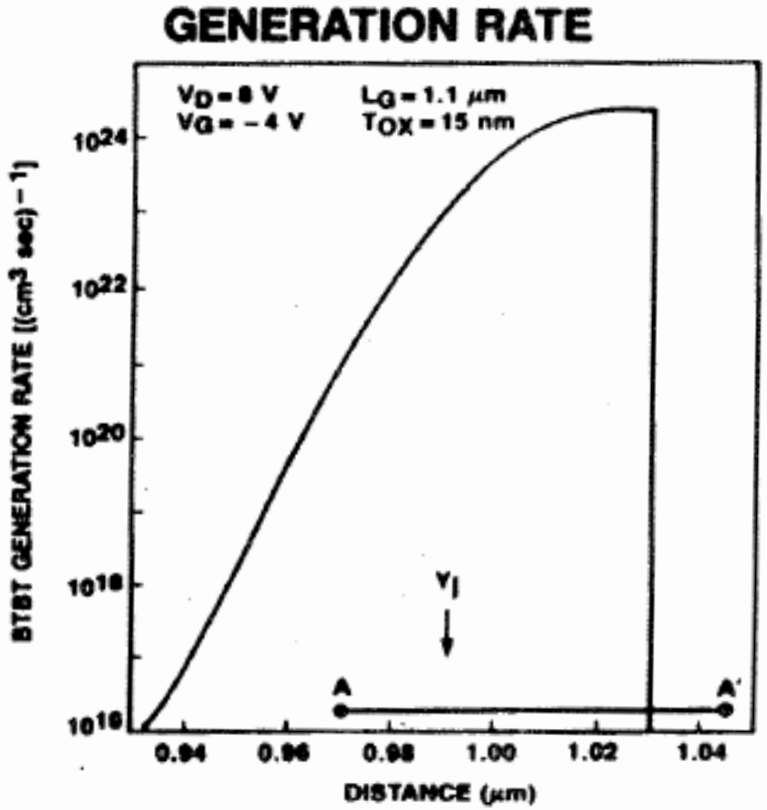
BTBT CARRIER GENERATION RATE DISTRIBUTION

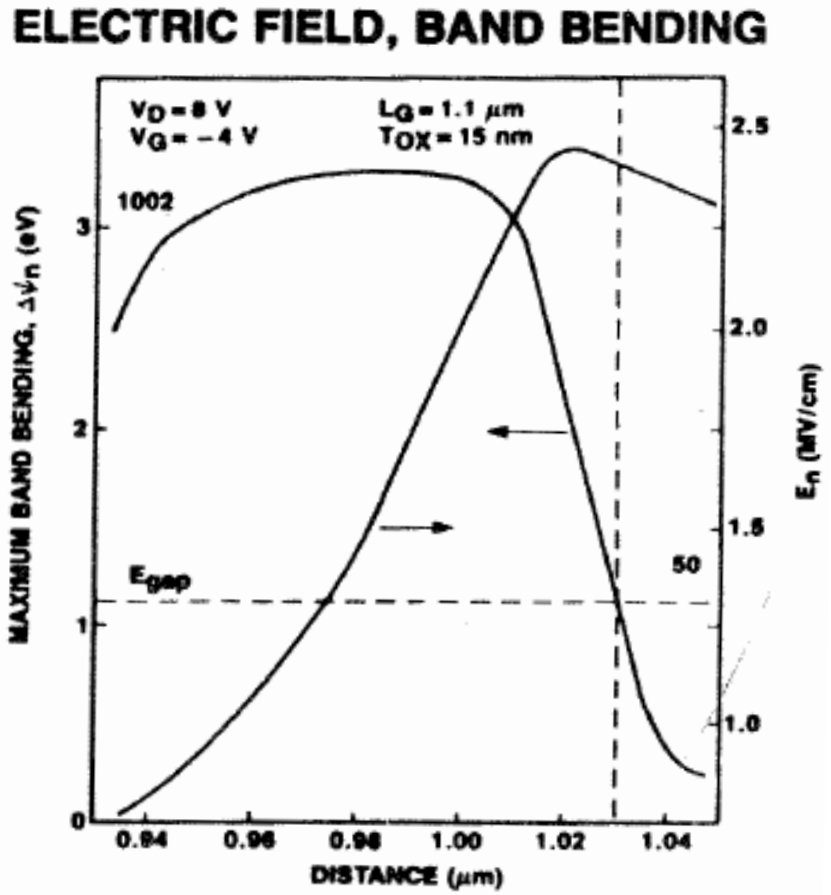


Orlowski et al, Electron, Device Letters (11), 1990, p.593
M.Orlowski et al, VLSI Technology Sumposium 1990, p. 67

Electric Field and Band Bending in Gated Diode BTBT Effect







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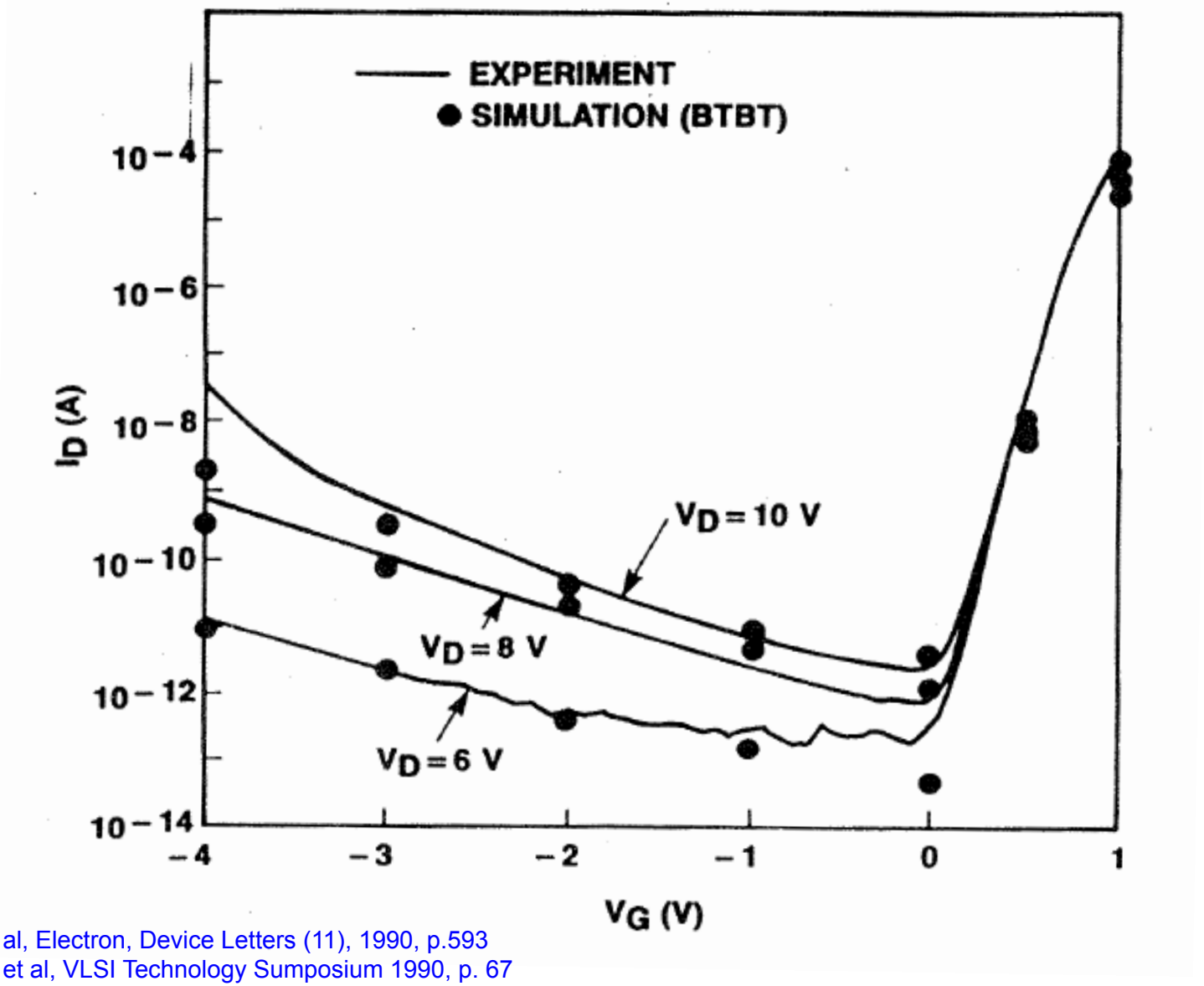
COMPARISON WITH EXPERIMENT



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Gate-Induced Drain Leakage (GIDL)

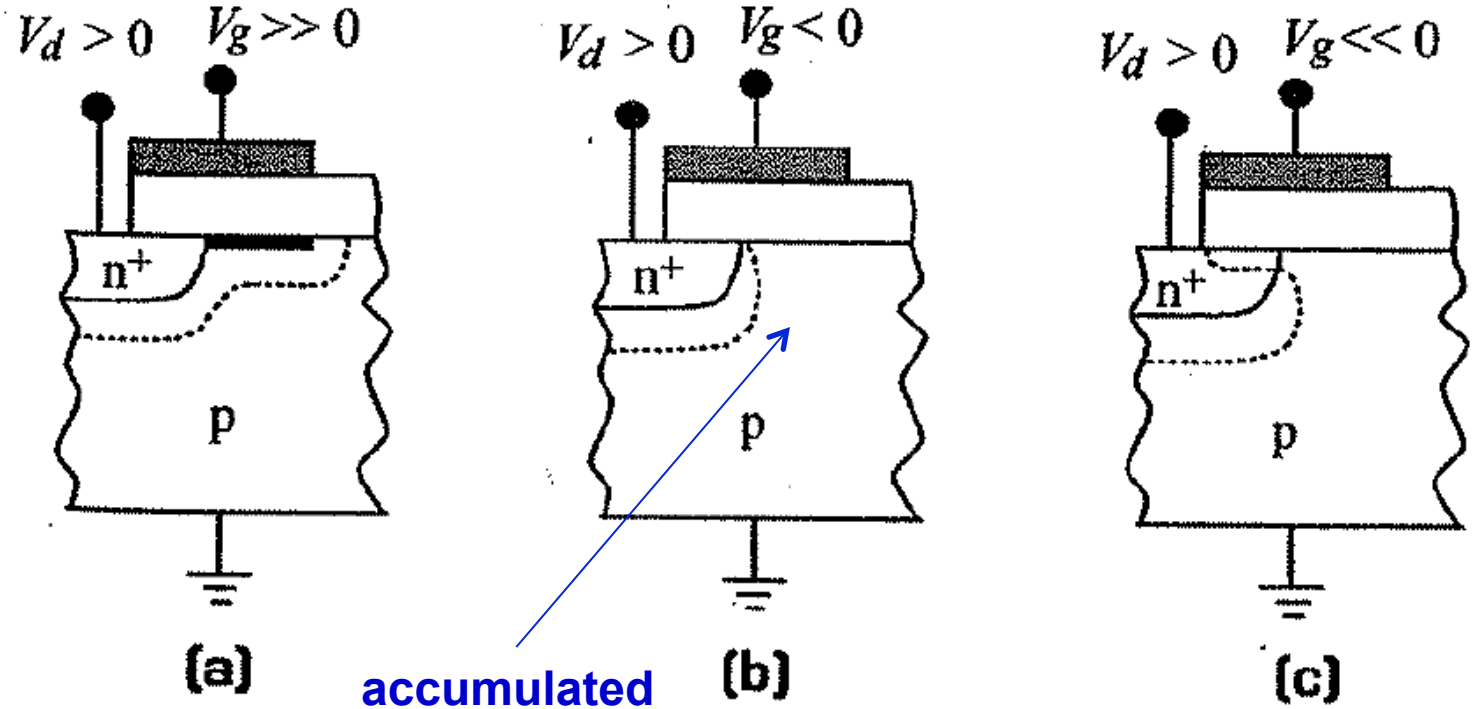
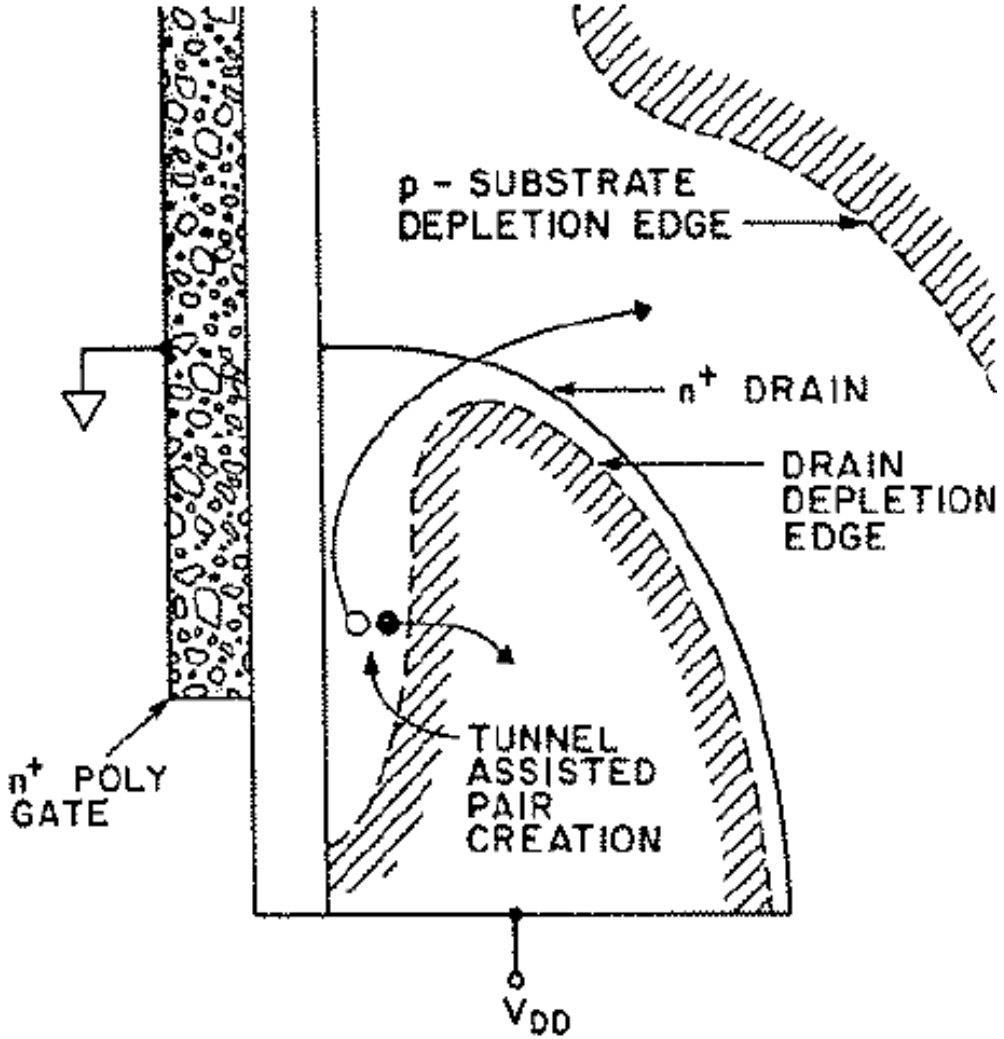


FIGURE 2.46. Schematics illustrating a gated n^+–p diode when the surface is (a) inverted and (b) accumulated, and (c) when the surface of the n^+ region is depleted or inverted. The dashed lines indicate the boundary of the depletion region.

GIDL is leakage current caused by BTBT tunneling in a gated n+p junction.

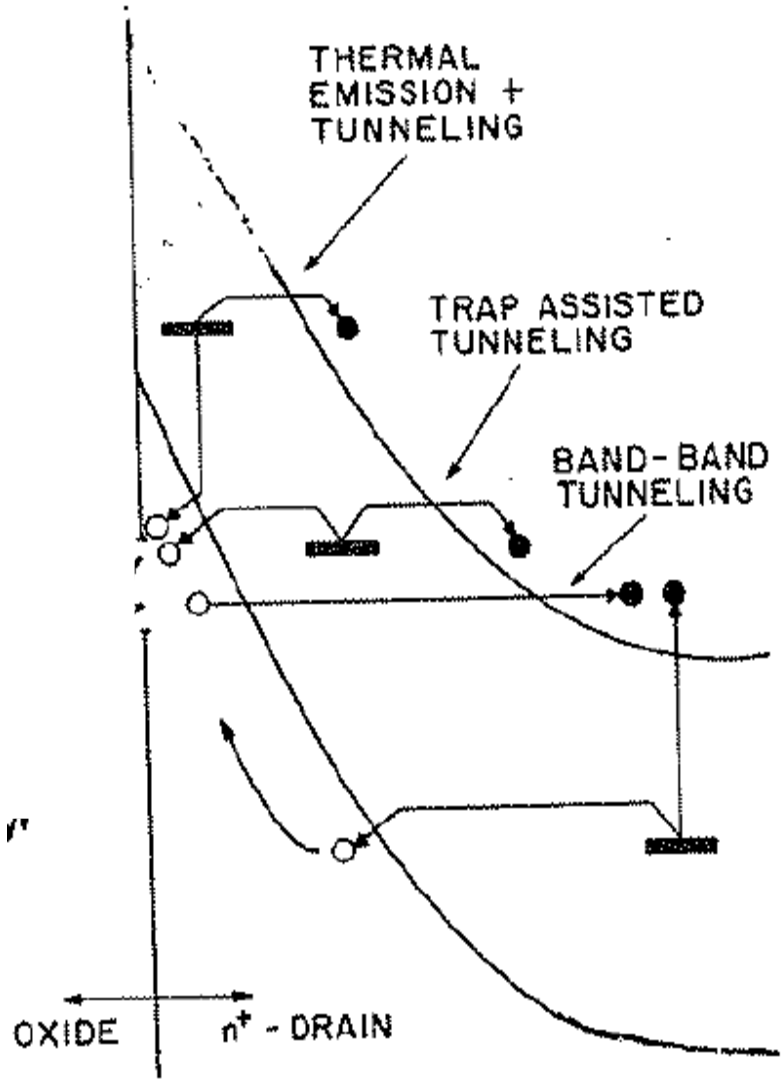
Gate-Induced Drain Leakage (GIDL)



Orlowski et al, Electron, Device Letters (11), 1990, p.593
M.Orlowski et al, VLSI Technology Symposium 1990, p. 67

The location of BTBT at a given V_g-V_d difference is determined by band bending in excess of the energy band gap E_G and high enough doping to make the width between E_c and E_v sufficiently small.

Gate-Induced Drain Leakage (GIDL)



GIDL can be enhanced by traps that exist in the forbidden energy gap of the semiconductor.

Remember that we consider this effect in the context of source and drain junctions. Because source and drain junction require very high implantation doses done usually by ion implantation, the source/drain regions suffer a lot of implant damage. This implant damage creates traps in the forbidden energy gap. As a result the BTBT is enhanced by so called trap assisted BTB tunneling.

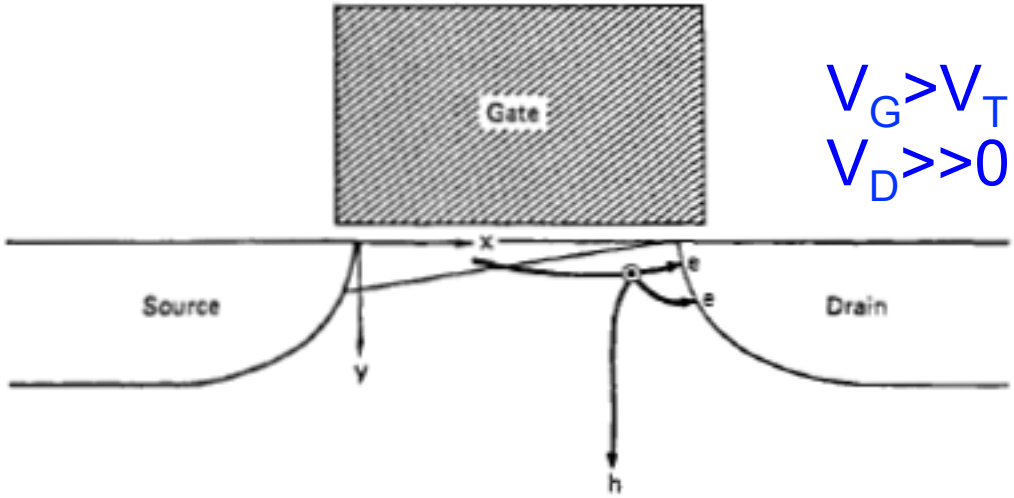
How to reduce GIDL?

- Increase tox to reduce oxide field; however larger tox results in higher V_T and in lower drain current.

- Reduce trap density by extra anneal or by avoiding implantation and use in-diffusion

- Increase concentration of n+ near the interface and make abrupt n^+p junction as this will reduce the depletion width and the tunneling volume.

Substrate Current in a MOSFET



$V_G > V_T$
$V_D >> 0$

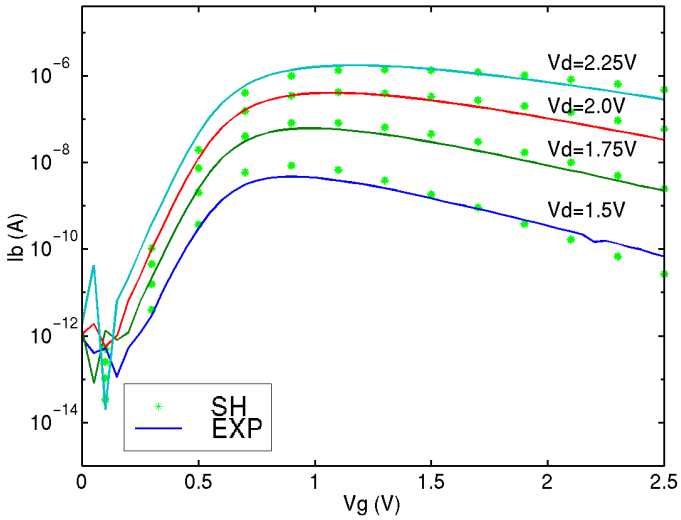
substrate current =
collected holes (for NMOSFET)
at the substrate contact

$$I_{sub} = C_1 I_D \exp\left(-\frac{\varphi_i}{\lambda q E_{\|}}\right)$$

φ_i *critical energy for impact ionization*

λ *mean free path*

Substrate current as a function of drain and gate voltages



Leakage Current due to BTBT and Impact Ionization

What happens to e-h pairs generated by BTBT in a MOSFET? The electrons are swept to the drain contact. Holes experience the high lateral fields at the drain and are accelerated towards the drain. They acquire high energy and can cause impact ionization (II) creating thus secondary e-h pairs. The electrons created in the secondary e-h pair generation are accelerated towards the drain and can cause tertiary impact ionization creating more e-h pairs. In a first order approximation we can assume that both mechanisms work in tandem.

Note that in a MOSFET geometry BTBT e-h are created by high vertical fields but avalanche is caused by high lateral fields.

Drain current in band-to-band tunneling and avalanche regime

$$I_{tot} = A_t E_\perp exp(-B_t E_\perp) \cdot \frac{1}{1 - \alpha_o exp(-\beta_o / E_\parallel)}$$

Band–To–Band Tunneling

Avalanche

Multiplication factor

Comment: Local Impact Ionization Model

Determination of impact ionization parameters α_o and β_o.

Multiplication factor $\dfrac{1}{1-\alpha_o exp(-\beta_o/E_{\|})}$

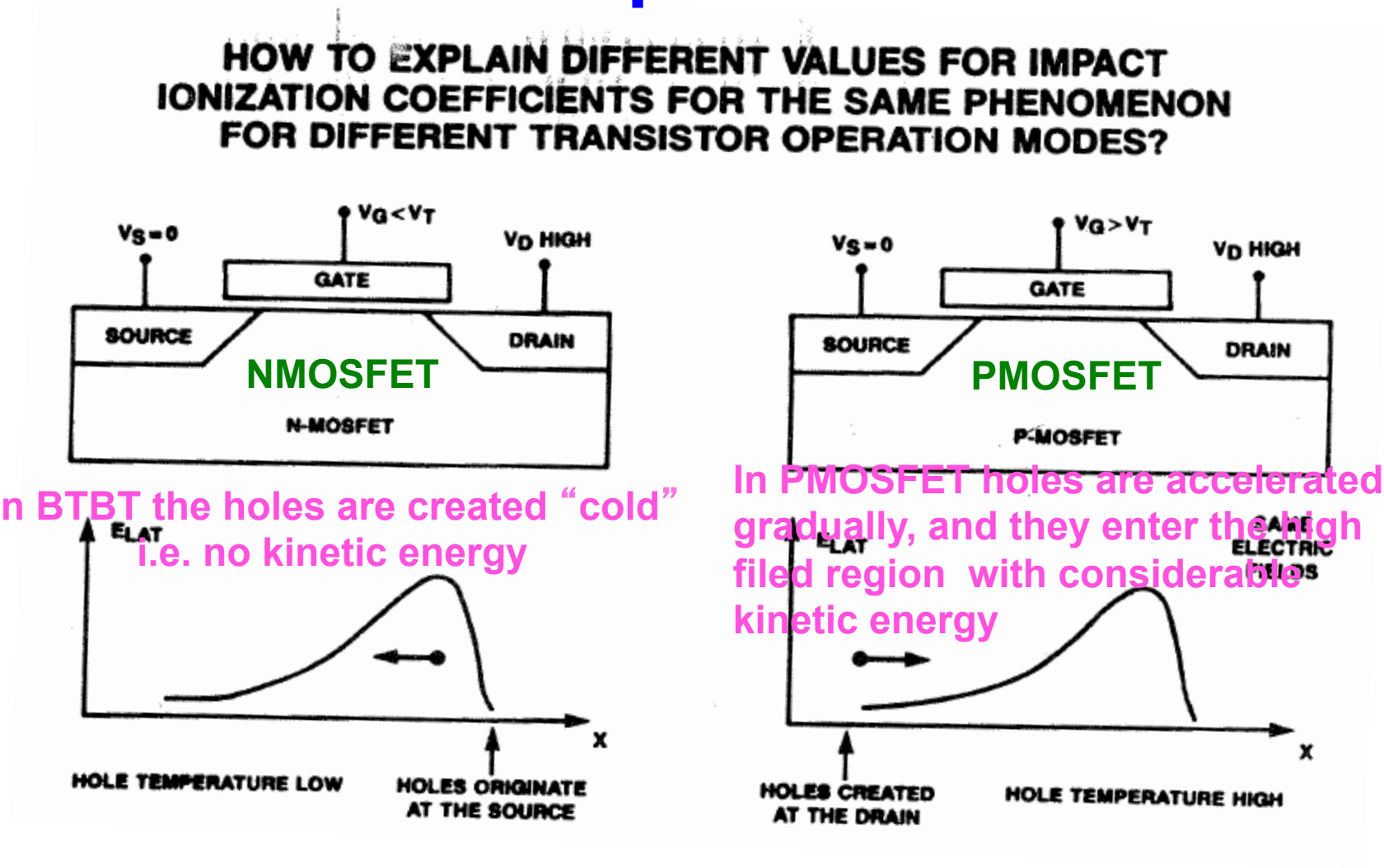
The parameters have been found to be different in a NMOSFET with BTBT as explained before and in PMOSFET in saturation to calculate the substrate current due to impact ionization.

Local impact ionization model assumes that the avalanche and impact ionization is determined only by the local electric field and does not depend on the hole prehistory, i.e. what is the hole's kinetic energy when it arrives at a position of a given electric field E(x).

The prehistory of the hole's kinetic energy, however, determines the actual kinetic energy of the hole at a position of a given electric field.

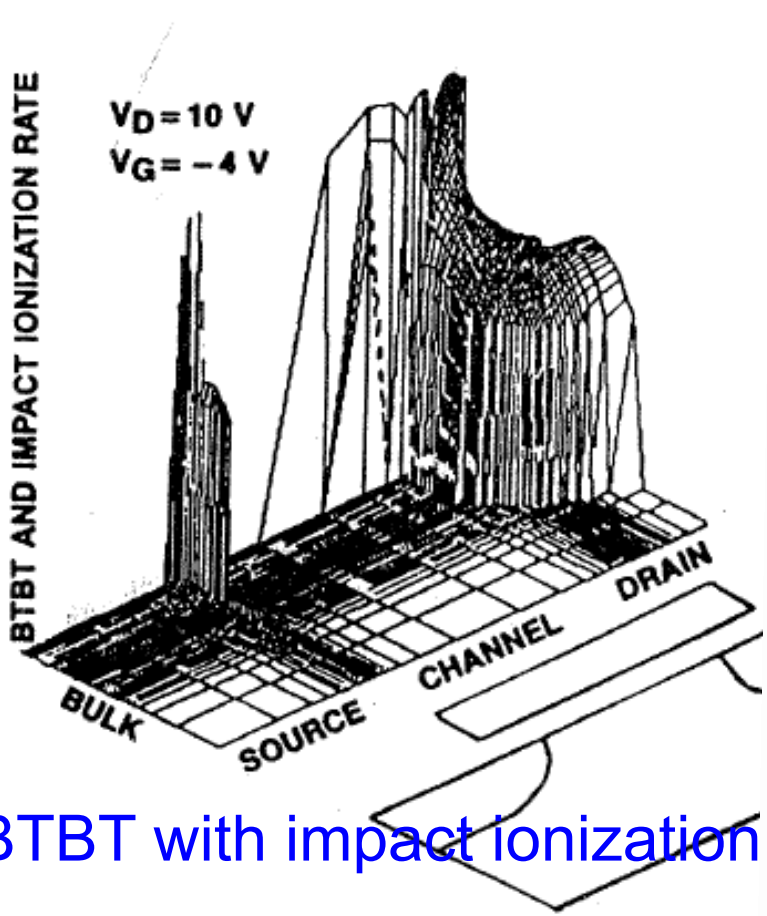
→ Nonlocal effects

Comment: Local Impact Ionization Model

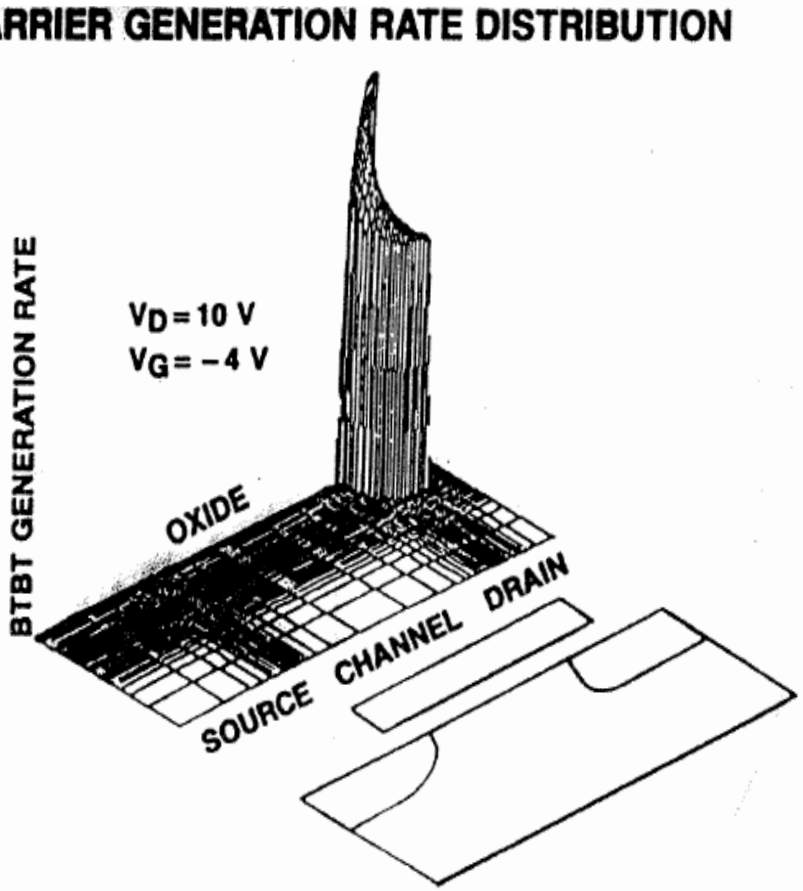


This experiment clearly shows that the **local** impact ionization model is inadequate to explain this differences → **nonlocal effects**

BTBT AND IMPACT IONIZATION



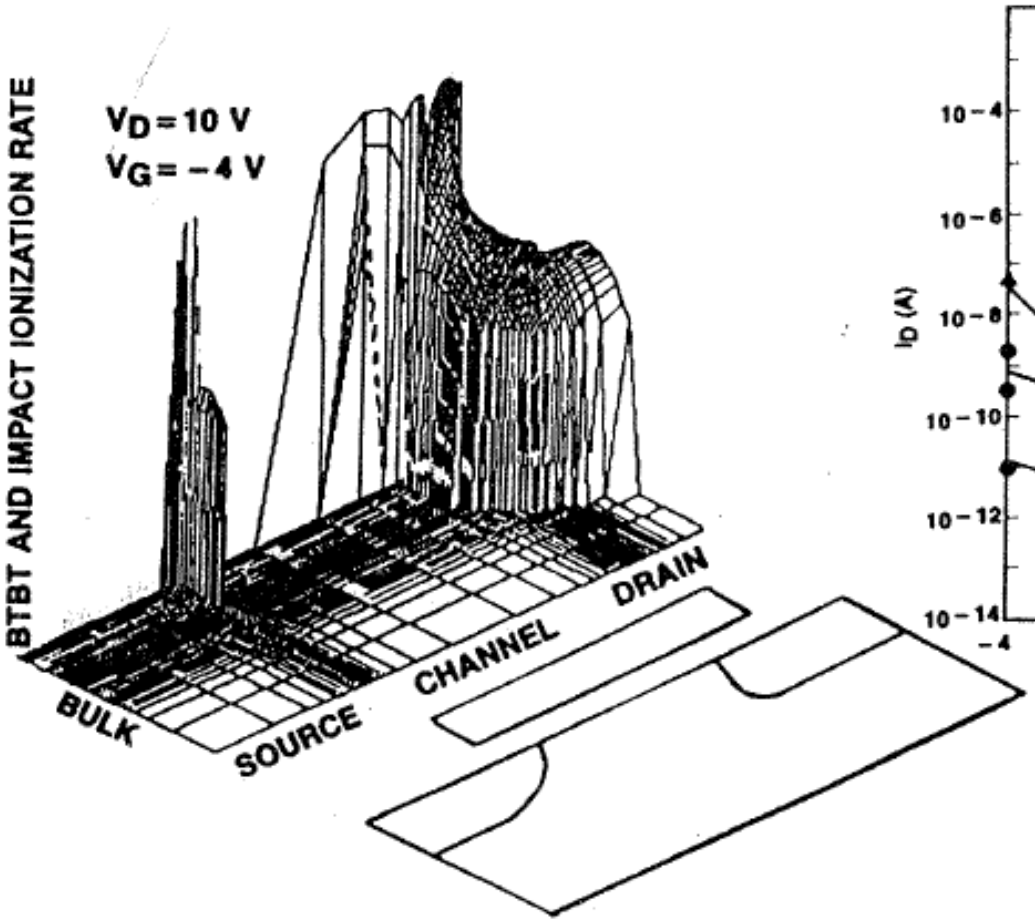
BTBT with impact ionization

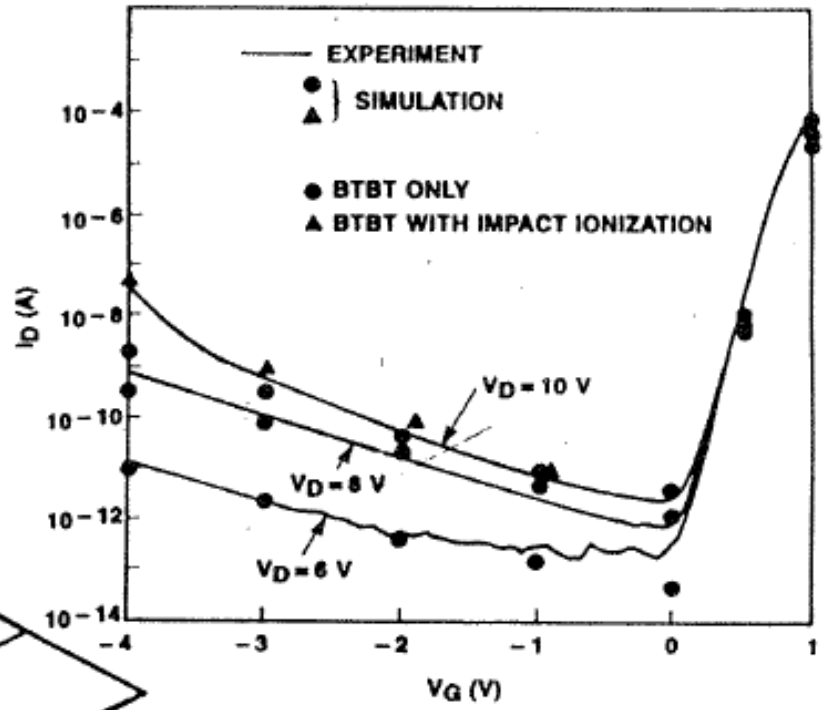


BTBT without impact ionization

Orlowski et al, Electron, Device Letters (11), 1990, p.593
M.Orlowski et al, VLSI Technology Sumposium 1990, p. 67

BTBT AND IMPACT IONIZATION





Temperature Dependence of the Band-to-Band Tunneling

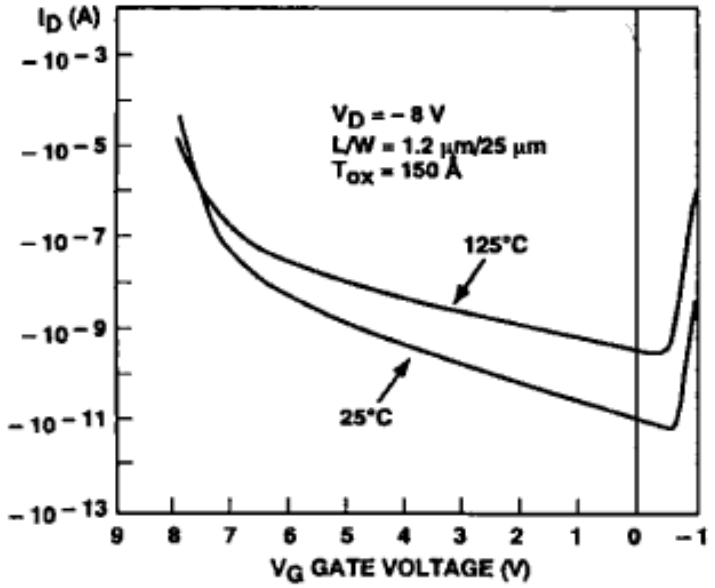


Fig.1 Experimental drain current of an PMOSFET in deep off−regime as a function of the gate bias for T=25 C and for 125 C.

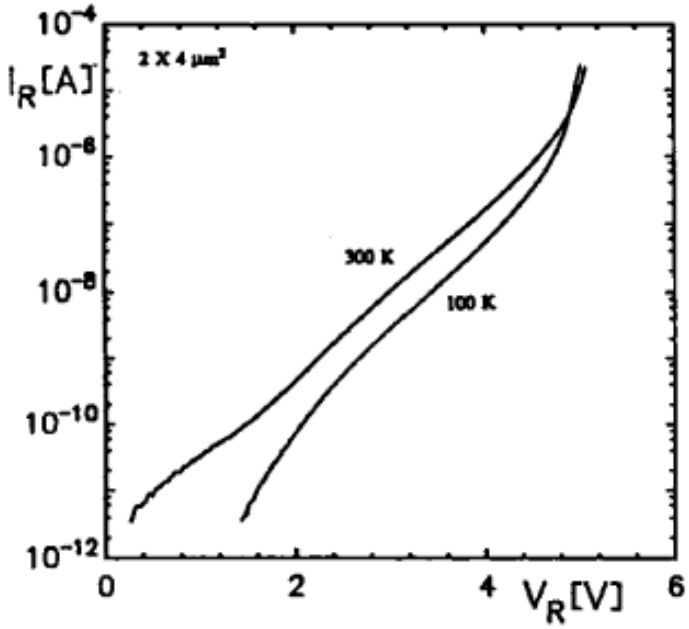


Fig.2 Reverse emitter−base current at 300 K and 100 K as a function of the reverse bias V_R.

MOSFET Experiment

Bipolar Experiment

Orlowski, M.; Shih Wei Sun; Burnett, D.
Temperature Cross-Over Effect of Carrier Avalanche Induced by Band-to-Band Tunneling in ULSI Devices
Solid State Device Research Conference, 1993. ESSDERC '93. p.385-388

Recall: BTBT Derivation in pn Diode Section

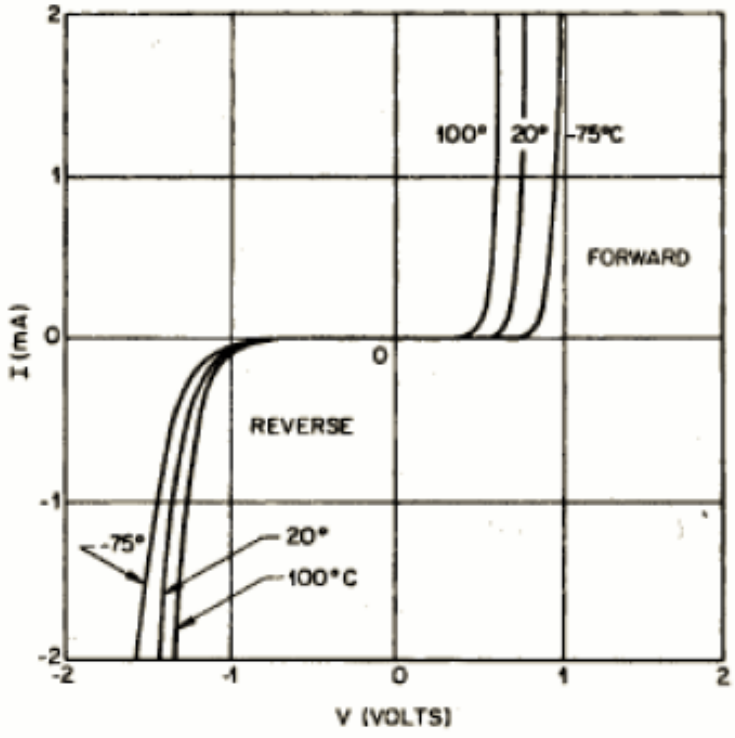
Temperature Effect on **Zener breakdown**

The tunneling current density can be expressed as :

$$J_T = \frac{\sqrt{2m^*}\, q^3 EV}{4\pi^2 \hbar^2 E_g^{1/2}} \exp\left(-\frac{4\sqrt{2m^* E_g^{3/2}}}{3\hbar E q}\right)$$

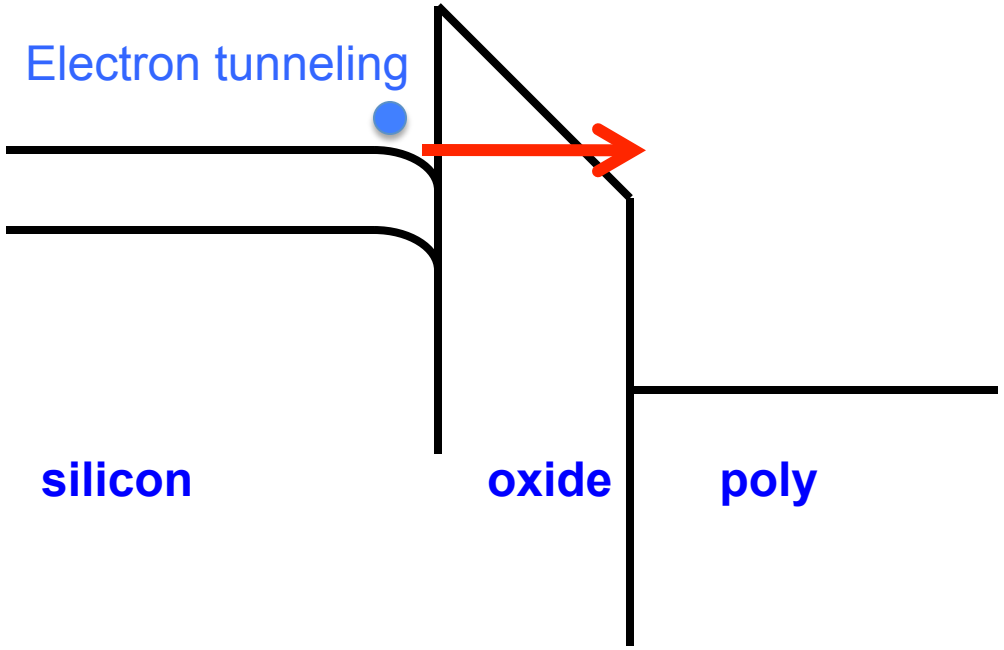
Where E is the electric field at the junction and V is the applied voltage

Since the energy bandgap Eg ***decreases*** with ***increasing*** temperature, the Zener breakdown voltage ***decreases*** with ***increasing*** temperature.



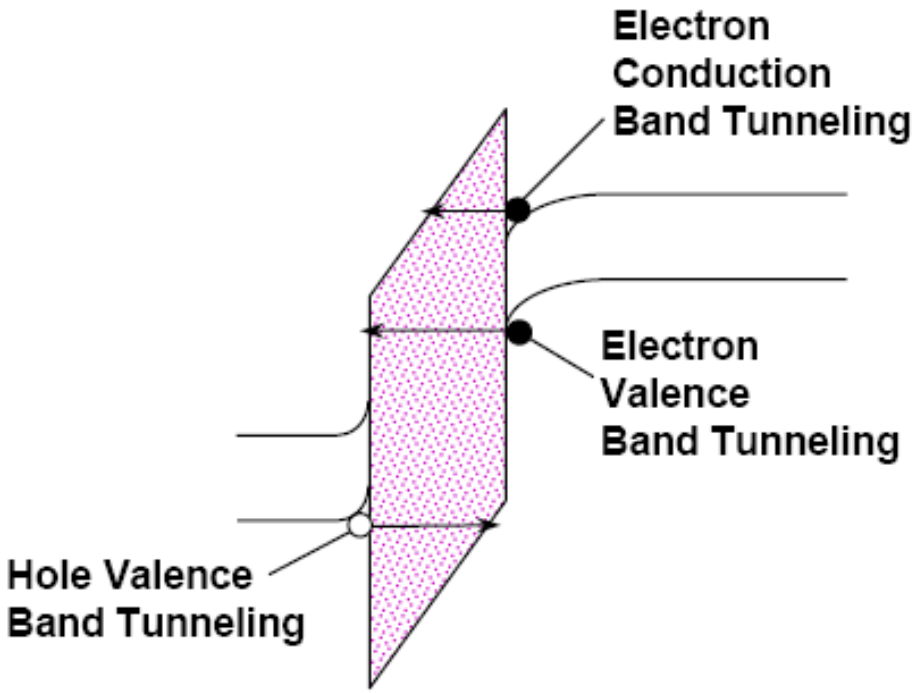
Fowler-Nordheim Tunneling

One important transport phenomenon through a dielectric layer between two electrodes is so-called Fowler-Nordheim (FN) injection, which is in fact a field-assisted electron tunneling. When a large voltage is applied across a polysilicon-SiO_2-silicon structure, its band structure has a shape as shown below. The electrons see a triangular barrier of which the width is dependent on the applied field. The height of the barrier is determined by the electrode material and the band structure of the dielectric (SiO_2).

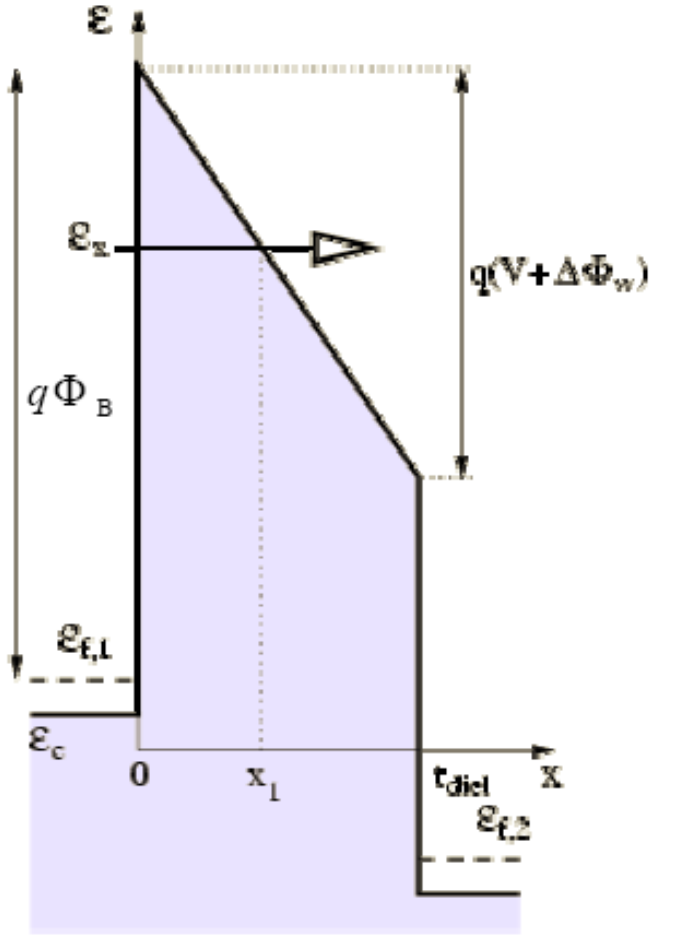


Fowler Nordheim Tunneling

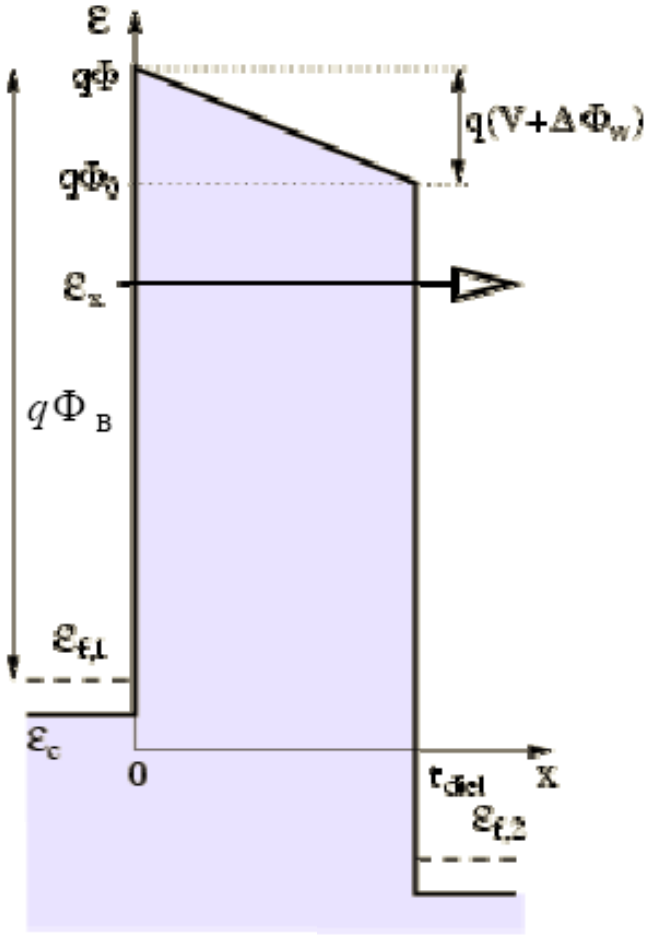
- Both electrons and holes can tunnel
- Electron conduction band tunneling most likely
- Hole tunneling less likely due to higher energy barrier



Distinguish:
FN and direct tunneling



FN tunneling



Direct tunneling

Q.M. Tunneling

Fowler-Nordheim, Direct, and Band-to-Band tunneling are the same quantum mechanical phenomenon, namely tunneling through a potential barrier.

In case of Fowler Nordheim and direct tunneling, the tunneling is through the potential barrier of an insulator;

In case of BTBT the tunneling is through the barrier in silicon of the forbidden energy between the conduction and valence band.

Because, in case of BTBT, where a valence band electron is tunneling to the conduction band, a hole is left behind, BTBT tunneling results in generation of electron-hole pairs. FN and direct tunneling do not generate carrier pairs.

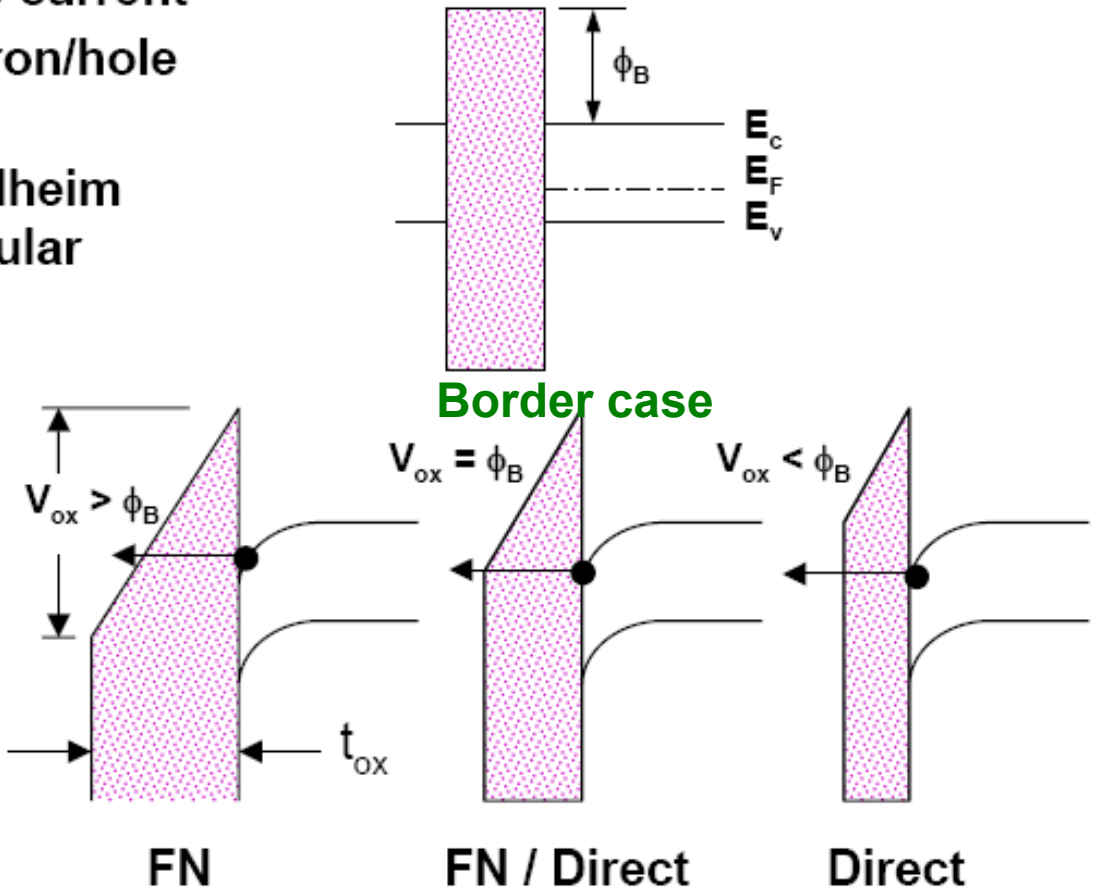
The potential barrier for both BTBT and for FN is a triangular one; the potential barrier for direct tunneling is trapezoidal.

All the three cases can be treated by the WKB quantum mechanical approximation that we exercised before for BTBT.

How to distinguish FN from direct tunneling: relation between ϕ_b and V_{ox}?

Gate Current

- High gate voltage $\Rightarrow$ gate current
- Gate current due to electron/hole tunneling
- For $V_{ox} > \phi_B$: Fowler-Nordheim tunneling (through triangular barrier)
  - Independent of oxide thickness
- For $V_{ox} < \phi_B$: direct tunneling (through entire oxide thickness)
  - Dependent on oxide thickness



current density for FN tunneling

- Fermi distribution replaced by step function (temperature 0K)
- WKB – approximation for transfer coefficient
- triangular shape of energy barrier
- the same work function of both electrode materials

the **Fowler-Nordheim formula** can be derived:

$$J\left(E_{\text{diel}}\right) = AE_{\text{diel}}^{2} \exp\left(-\frac{B}{E_{\text{diel}}}\right)$$

where

E_{diel} electric field in dielectric

A, B constants dependent on barrier configuration

current density for FN tunneling

for two conducting of semi-conducting electrodes separated by dielectric barrier the constants A and B are

$$A = \frac{q^3 m_{\text{eff}}}{8\pi m_{\text{diel}} h q \Phi_{\text{B}}} \qquad B = \frac{4\sqrt{2 m_{\text{diel}} (q\Phi_{\text{B}})^3}}{3\hbar q}$$

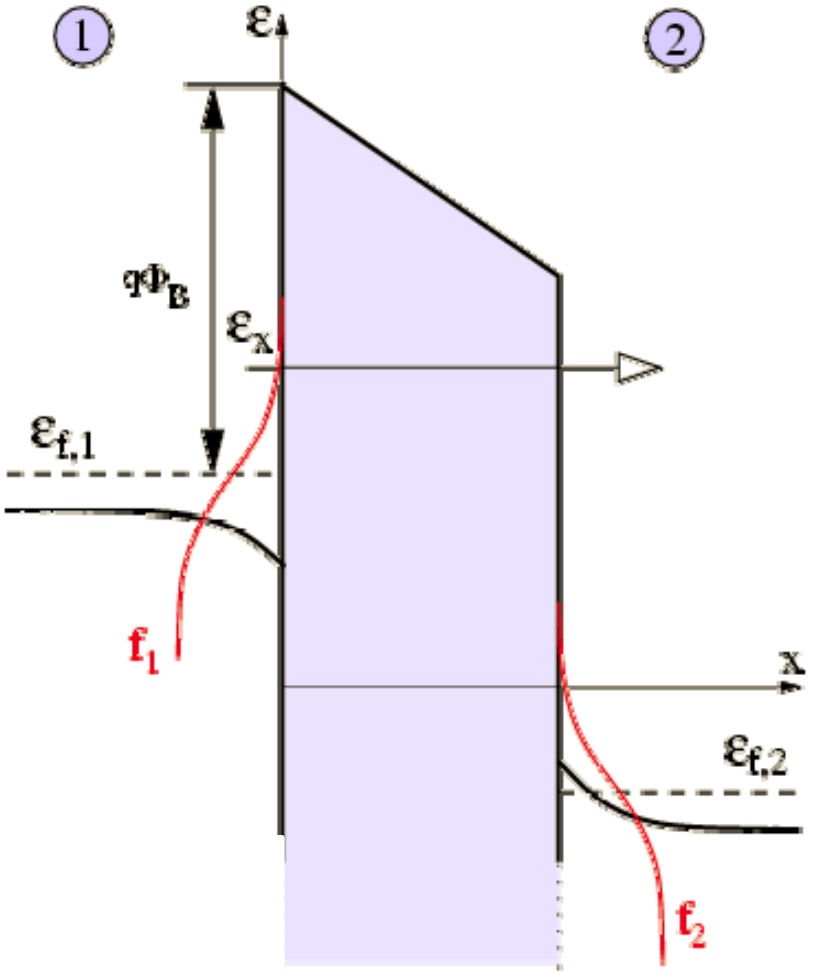
where

Φ_{B} height of the potential barrier measured from the Fermi level in the electrode to the conduction band in the dielectric

m_{eff} effective electron mass in electrode material

m_{diel} effective electron mass in the dielectric material

Tsu-Esaki formula



supply function

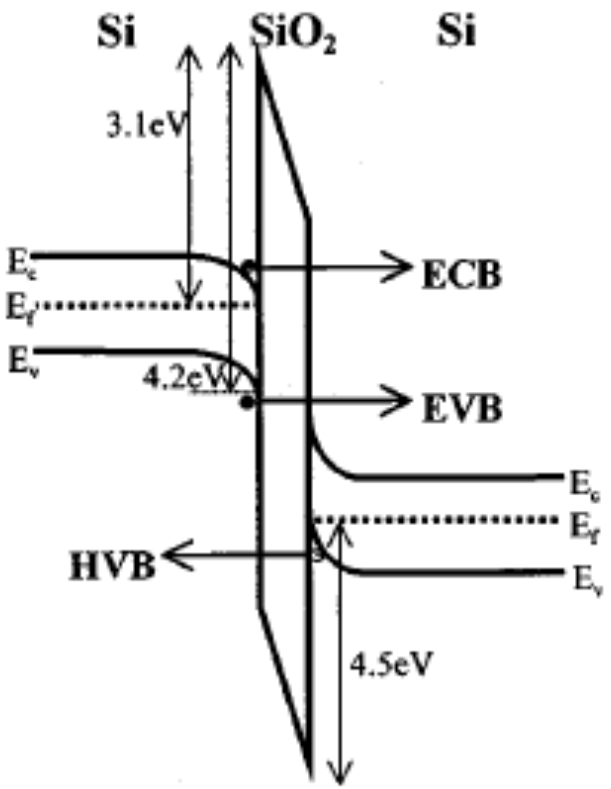
$$J = \frac{4\pi m_{\text{eff}} q}{h^3} \int_{E_{\min}}^{E_{\max}} T(E) N(E) dE$$

transfer coefficient

The calculation of current density requires not only the knowledge of the energy dependent **transfer coefficient**, but also the energy dependent electron probability (**supply function**).
In case of ECB the integration in the Tsu-Esaki formula is performed from the Fermi level of the electrode to the conduction level of the dielectric.

http://www.iue.tuwien.ac.at/phd/gehring/node36.html

DIRECT TUNNELING EQUATION



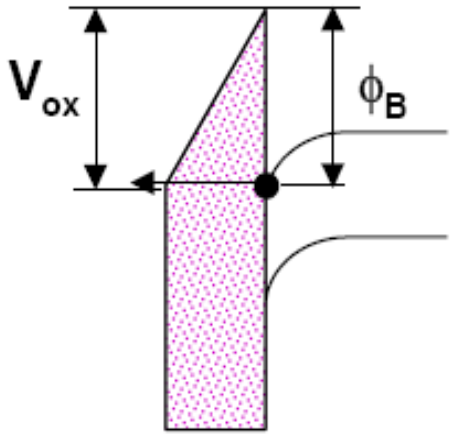
For large voltage difference between
gate electrode and silicon (larger than E_g);
then electron from conduction band and valence band tunnel through the oxide

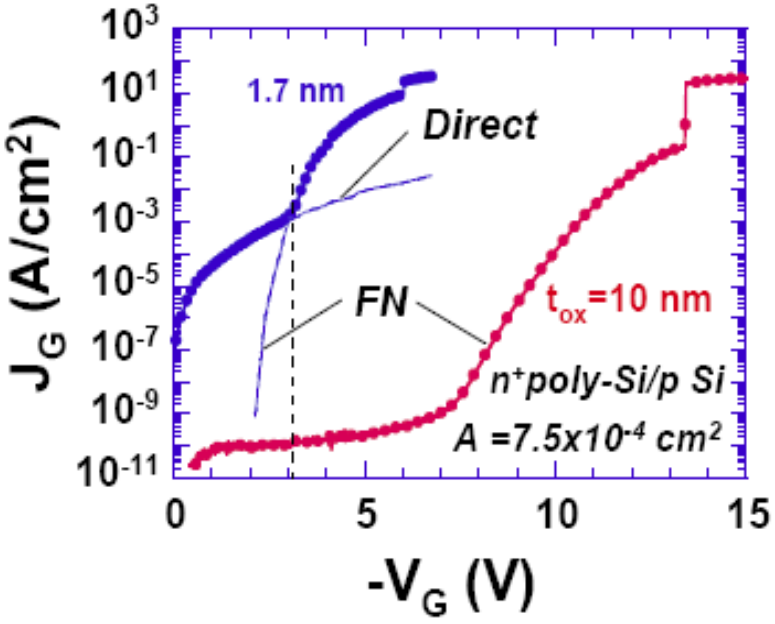
$$J = \sum_n N_n / \tau_n(E_n)$$

$$\frac{1}{\tau_n(E)} = \frac{T(E)}{\int_0^{tox} \sqrt{2m_n /[E_n - E_C(z)]}dz}$$

Fowler-Nordheim vs. Direct Tunneling

- $V_{ox} > \phi_B$: Fowler-Nordheim tunneling dominates
- $V_{ox} < \phi_B$: Direct tunneling dominates





For Si/SiO_2 system $V_{ox} < \phi_B = 3.2\ V \Rightarrow$ direct; $V_{ox} > \phi_B = 3.2\ V \Rightarrow$ F-N

Measured Fowler-Nordheim Currents Signature of FN Tunneling

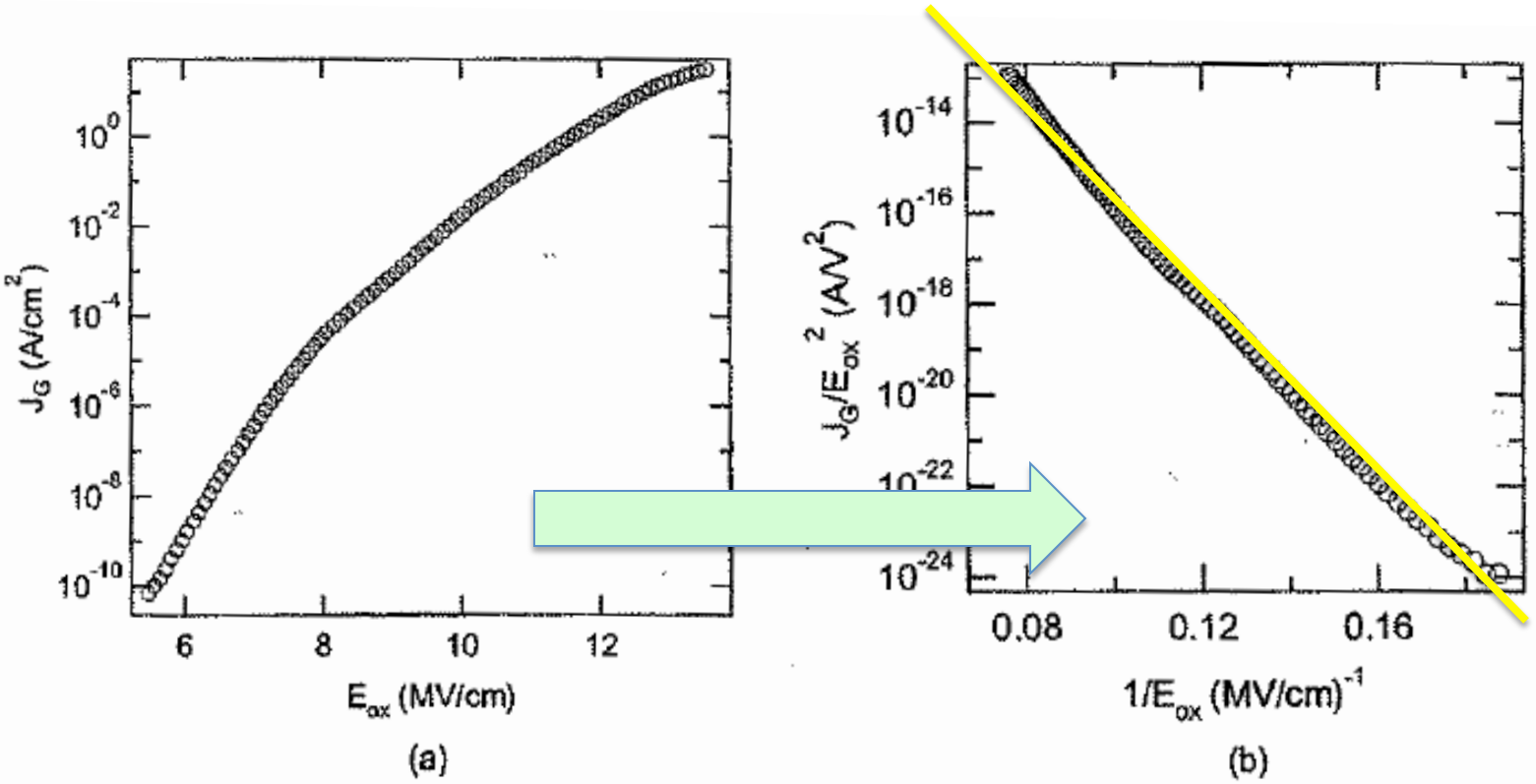


Figure 4.8. (a) Fowler–Nordheim tunneling current as a function of the applied field across the oxide. The current is exponentially dependent on the field. (*b*) Fowler–Nordheim plot: J/E^2 as a function of $1/E$, extracted from (*a*). A straight line is obtained.

Determination of the FN Tunneling Parameters

Fowler-Nordheim Tunneling

- The *FN* current density is

$$J_{FN} = A\varepsilon_{ox}^2 \exp\left(-\frac{B}{\varepsilon_{ox}}\right)$$

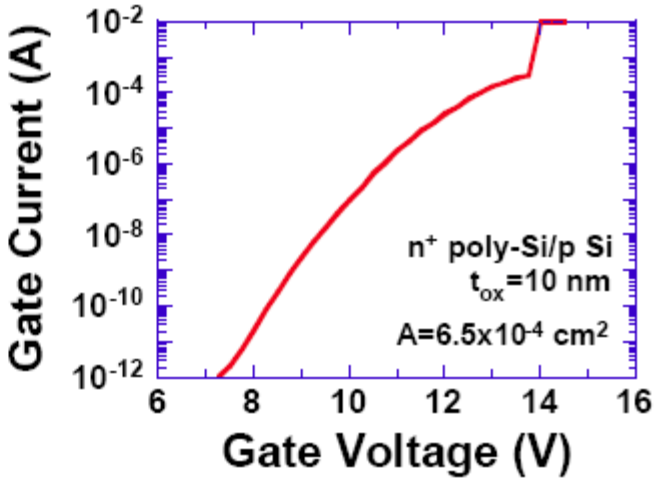
where

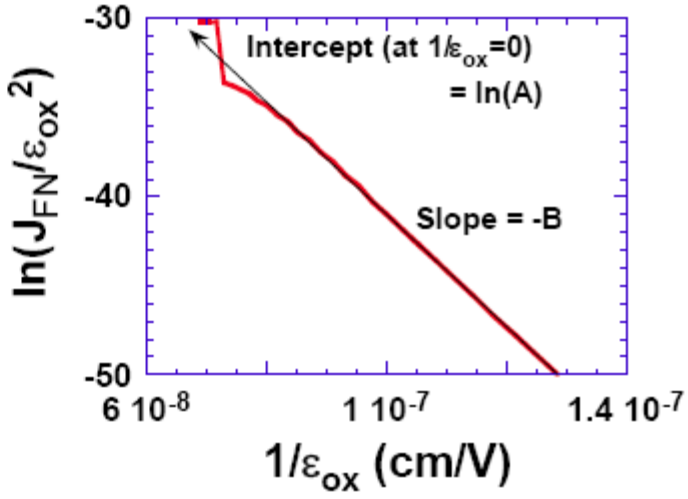
$$A = \frac{q^3 (m/m_{ox})}{8\pi h \phi_B} = 1.54x10^{-6} \frac{(m/m_{ox})}{\phi_B} \; [A/V^2]$$

$$B = \frac{4\sqrt{2m_{ox}\phi_B^3}}{3q\hbar} = 6.83x10^7 \sqrt{\frac{m}{m_{ox}}}\phi_B^3 \; [V/cm]$$

- *A* and *B* are determined

$$\ln\left(J_{FN}/\varepsilon_{ox}^2\right) = \ln(A) - B/\varepsilon_{ox}$$





$$E_{ox} = \frac{V_{appl} - V_{FB}}{t_{ox}}$$

V_{appl} *voltage applied across oxide*

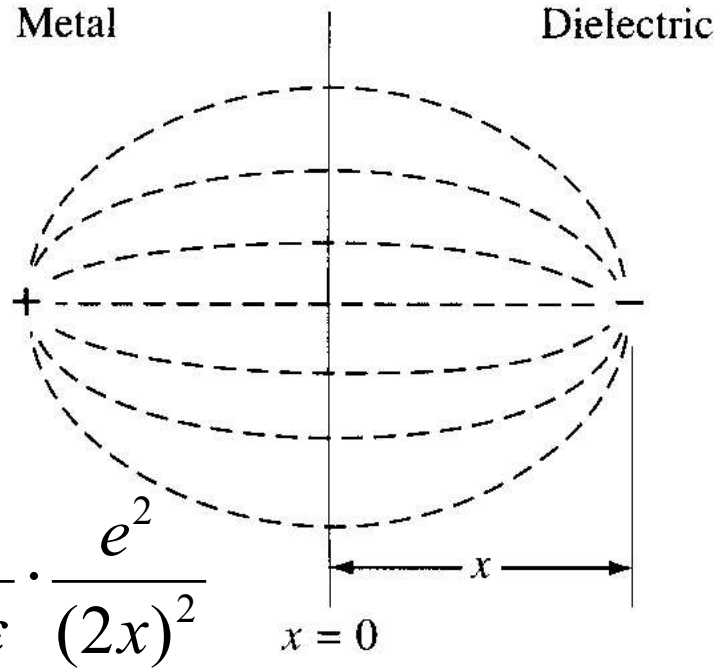
V_{FB} *flat band voltage*

Lowering of the Potential Barrier induced by Image-Force

also known as the 'Schottky effect'

The presence of a conductor distorts the radially symmetric Coulomb field of a point charge in front of it. The surface of the conductor is an equipotential surface, since no current flows parallel to it. i.e. the field lines must be perpendicular to the metal surface.
This requirement is reproduced by a mirror image of the original point charge which is equal size but of opposite sign (inside the metal so to speak).

As a consequence, there exists an attractive Coulomb potential between the real charge and its image induced in the conductor which lowers the total energy of the electron.



An electron in the depletion layer of a semiconductor at the distance x in front of the metal experiences an image force (Coulomb attraction) of

$$F(x) = -\frac{1}{4\pi\varepsilon} \cdot \frac{e^2}{(2x)^2}$$

The force on the electron due to the coulomb attraction with the image charge will be:

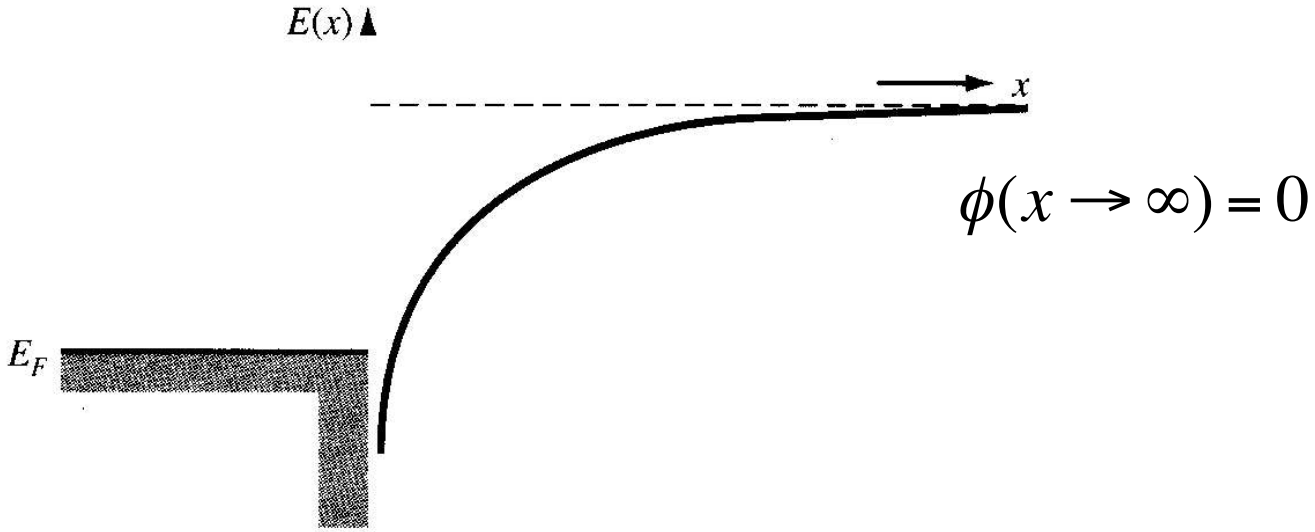
$$F = \frac{-e^2}{4\pi\epsilon_s(2x)^2} = -e\mathrm{E}$$

The potential can then be found as

$$-\phi(x) = +\int_x^\infty \mathrm{E}dx' = +\int_x^\infty \frac{e}{4\pi\epsilon_s \cdot 4(x')^2}dx' = \frac{-e}{16\pi\epsilon_s x}$$

where x' is the integration variable and where we have assumed that the potential is zero at x = ∞

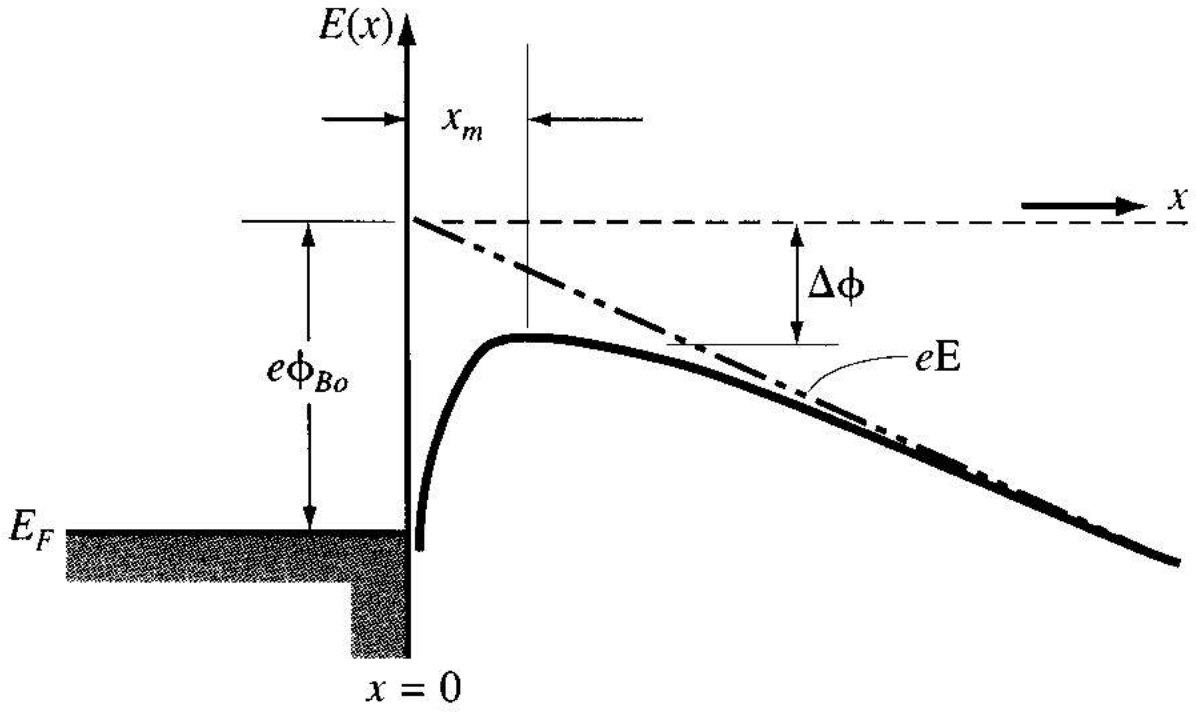
The potential energy of the electron is -eϕ(x); below is a plot of the potential energy assuming that no other electric field exists,



With an electric field in the dielectric, the potential is

$$-\phi(x) = \frac{-e}{16\pi\epsilon_s x} - \mathrm{E}x$$

Thus, the potential energy of the electron, including the effect of a constant electric field, becomes



The peak potential barrier is now lowered.
This is the image-force-induced lowering of the barrier.

(The same effect is at work in the Schottky diode.)

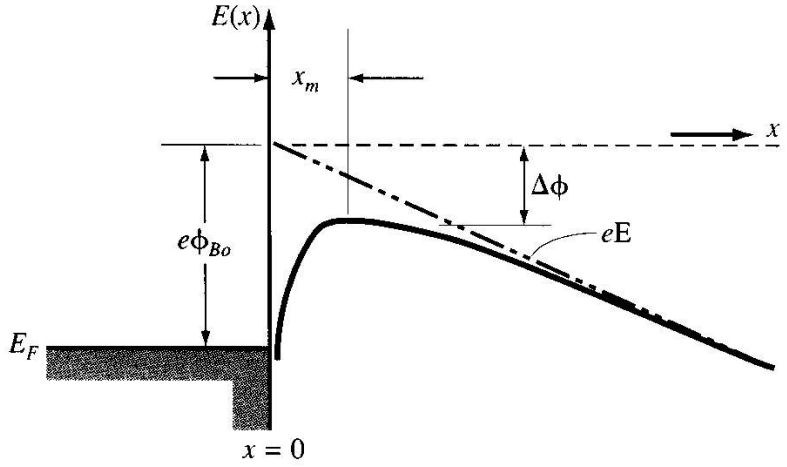
We can find the value of the Schottky barrier lowering, $\Delta\phi$, and the position of the maximum barrier, x_m, from the condition that

$$-\phi(x) = \frac{-e}{16\pi\epsilon_s x} - \mathrm{E}x$$

$$\frac{d(e\phi(x))}{dx} = 0$$

and we find that

$$x_m = \sqrt{\frac{e}{16\pi\epsilon_s \mathrm{E}}}$$



and

$$\Delta\phi = \sqrt{\frac{e\mathrm{E}}{4\pi\epsilon_s}}$$

x_m is typically 2-5 nm

Example (what are the orders of magnitude)

Calculate the barrier lowering and the position of the maximum barrier height where the electric field in the semiconductor (GaAs) is assumed to be E = 6.8 x 10^4 V/cm.
Using the above equations,

$$\Delta\phi = \sqrt{\frac{eE}{4\pi\epsilon_s}} = \sqrt{\frac{(1.6\times10^{-19})(6.8\times10^{+4})}{4\pi(13.1)(8.85\times10^{-14})}} = 0.0273 \text{ volt}$$

$$x_m = \sqrt{\frac{e}{16\pi\epsilon_s E}} = \sqrt{\frac{(1.6\times10^{-19})}{16\pi(13.1)(8.85\times10^{-14})(6.8\times10^{4})}}$$

which gives x_M = 2 x 10^{-7} cm = 20Å = 2 nm

This may seem a small value, but the barrier height and the barrier lowering will appear in exponential terms in the current-voltage relationship.

A small change in barrier height can have a significant effect on the current level in a in FN tunneling as it has in the Schottky barrier diode.

Corrections of FN due to image force

$$J = \alpha E_{inj}^2 \exp\left(\frac{-E_c}{E_{inj}}\right) \qquad \alpha = \frac{q^3}{8\pi h \phi_b}\frac{m}{m^*} \qquad E_c = \frac{4\sqrt{2m^*}\phi_b^{3/2}}{3\eta q}$$

where h = Planck's constant
ϕ_b = energy barrier at the injecting interface (3.2 eV for Si–SiO_2)
E_{inj} = electric field at the injecting interface
q = charge of a single electron (= 1.6×10^{-19} C)
m = free electron mass (= 9.1×10^{-31} kg)
m* = effective mass of an electron in the bandgap of SiO_2 (0.42 m according to [27])
$\eta = h/2\pi$

$$J = \alpha E_{inj}^2 \frac{1}{t^2(\Delta\phi_b)} f(T) \exp\left[\frac{-E_c}{E_{inj}} v(\Delta\phi_b)\right]$$

$$\Delta\phi_b = \frac{1}{\phi_b}\sqrt{\frac{q^3 E_{inj}}{4\pi\varepsilon_{ox}}} \qquad f(T) = \frac{\pi c k T}{\sin(\pi c k T)} \qquad c = \frac{2\sqrt{2m^*}t(\Delta\phi_b)}{hqE_{inj}}$$

Additional Effects Affecting Tunneling Currents through Oxides

Oxide polysilicon are called poly-oxides and show an interface covered with asperities due to the rough texture of the polysilicon surface. These asperities give rise to a local field enhancement at the interface and an enhanced tunneling of electrons. Average oxide fields of the order of 2MV/cm are sufficient to yield injection fields of the order of 10MV/cm.

This has a major practical advantage as large injection fields can be obtained at moderate voltages using relatively thick oxides grown on polysilicon.

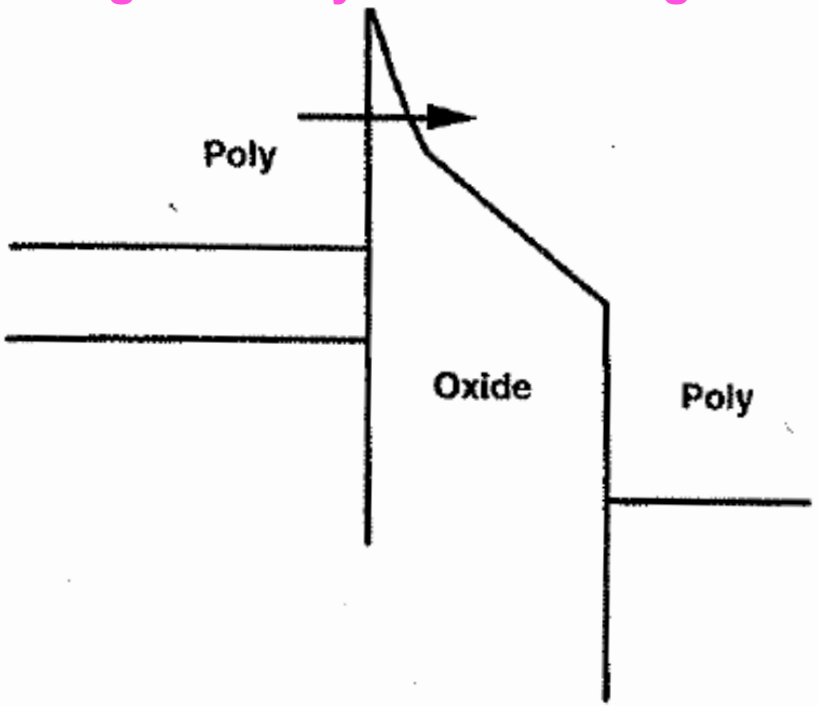
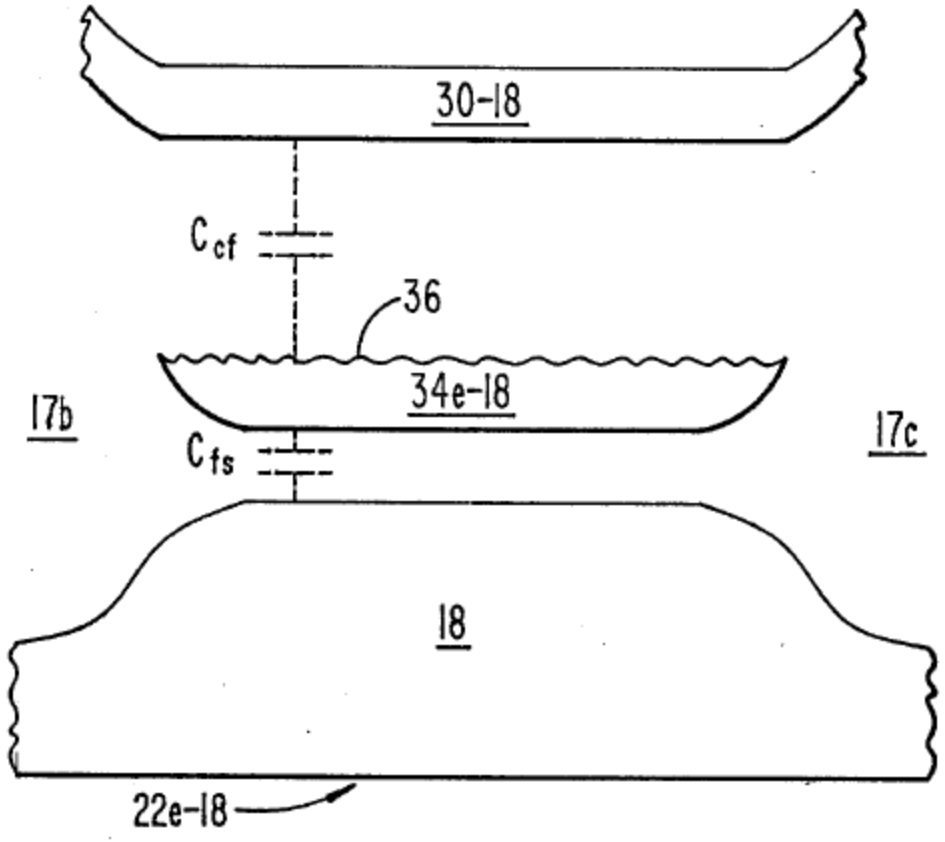


Figure 4.9. Energy band representation of Fowler–Nordheim tunneling through oxides thermally grown on polysilicon: The injection field is much higher than the average oxide field. The high injection field is due to local field enhancement at polysilicon–oxide interface asperities.

Asperities to enhance FN Tunneling



Stewart patent US 4,947,221 1990

Keep the C_{cf} capacitance small and nevertheless allow high FN tunneling currents!

Unassisted and Trap-assisted Direct Tunneling

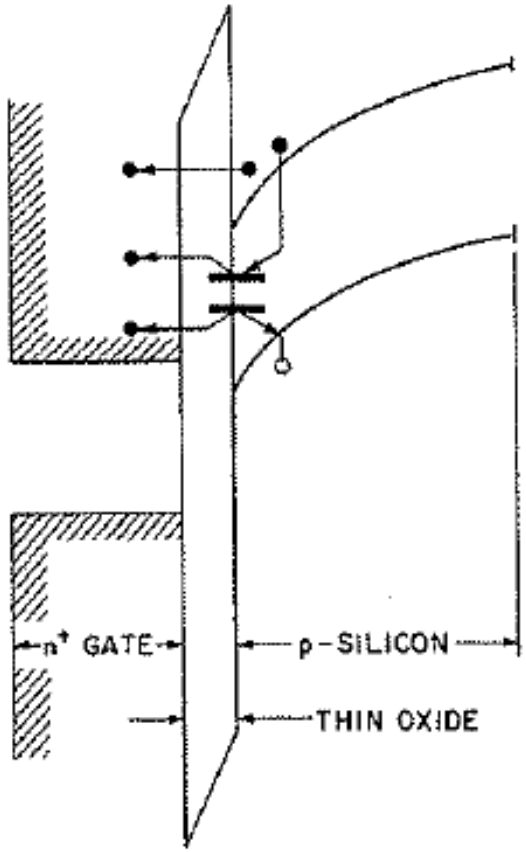


Fig. 7-12 Energy-band diagram for the phenomenon of direct tunneling through the gate oxide for thin oxides. Also shown are both unassisted tunneling and some possible interface-trap assisted leakage paths, with trap levels indicated by short, solid bars. From J.R. Brews,

Unassisted and Trap-assisted Direct Tunneling

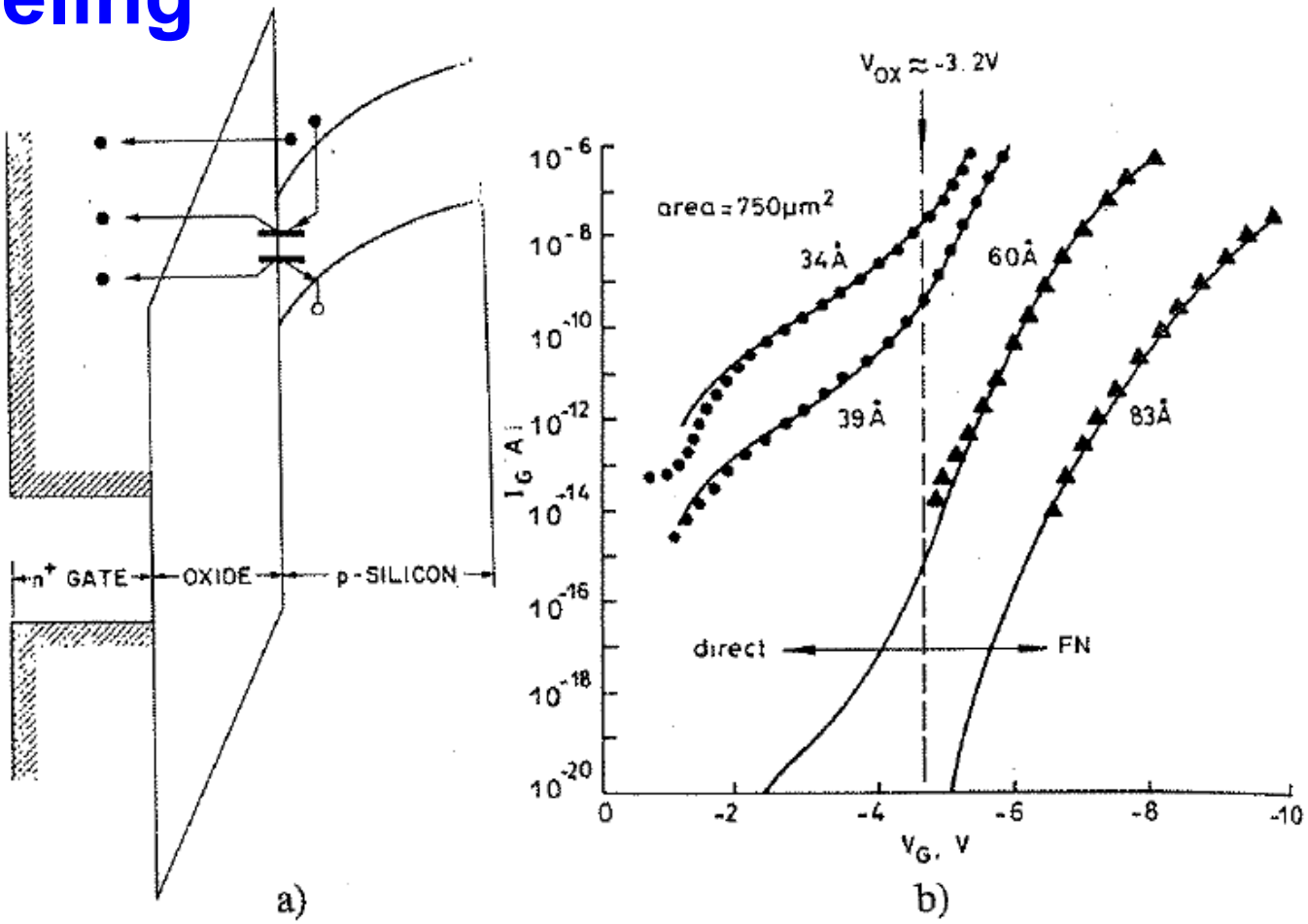
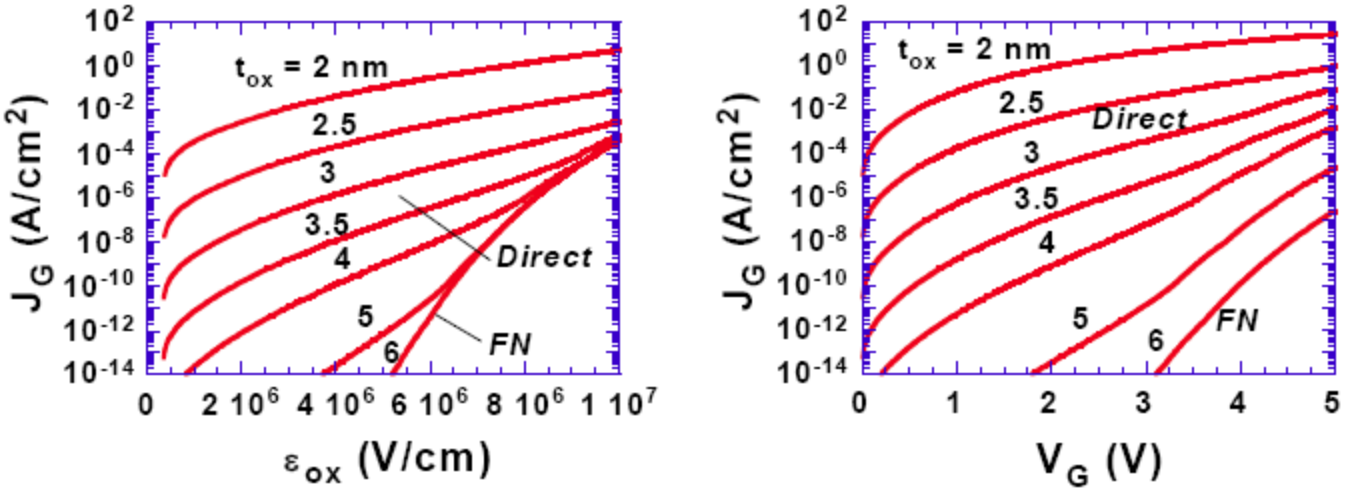


Fig. 7-11 (a) Energy-band diagram for the phenomenon of Fowler-Nordheim tunneling in the MOSFET gate oxide. Also shown are some possible interface-trap assisted leakage paths, with trap levels indicated by short, solid bars. From J.R. Brews, "The Submicron MOSFET," Chap. 3, in *High-Speed Semiconductor Devices*, Ed. Sze, p. 153. Copyright 1990, John

Direct Tunneling and limits to maintain inversion

- $J_{dir} > J_{FN}$ at low gate voltage ($V_{ox} < \phi_B$)

$$J_{dir} = \frac{A}{K_{ox}\varepsilon_o} C \exp\left[-\frac{B}{\varepsilon_{ox}}\left(1-\left(1-\frac{V_{ox}}{\phi_B}\right)^{3/2}\right)\right]$$



For oxide thicknesses smaller than 3 nm the direct tunneling current becomes large enough that it removes carriers faster than they can be supplied by the thermal generation. In such cases an inversion layer is kept from being formed in an MOS capacitor.

Summary FN and direct tunneling

$$J_{dir} = \frac{AV_G}{t_{ox}^2}\frac{kT}{q}C\exp\left(-\frac{B(1-(1-qV_{ox}/\Phi_B)^{1.5})}{\mathcal{E}_{ox}}\right) \qquad J_{FN} = A\mathcal{E}_{ox}^2\exp\left(-\frac{B}{\mathcal{E}_{ox}}\right)$$

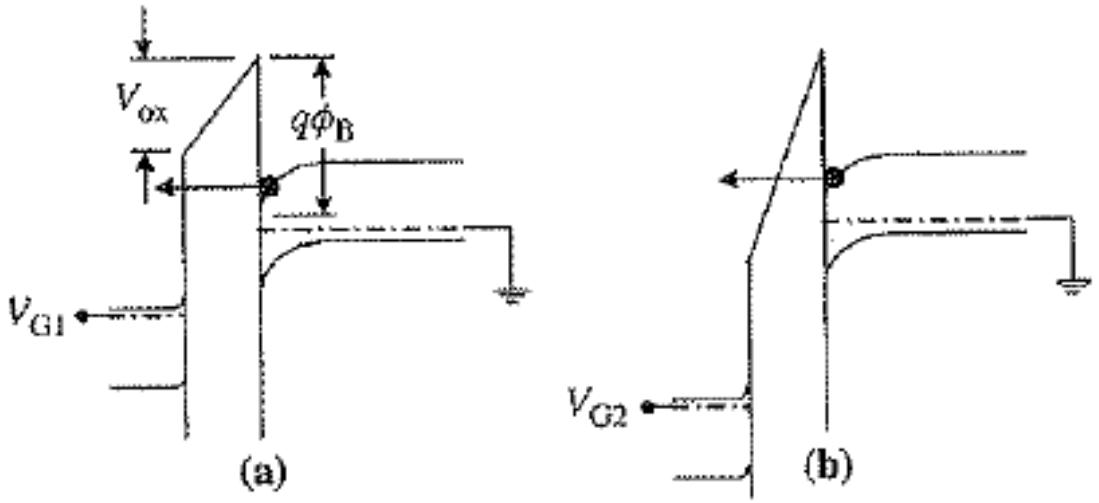


Fig. 12.10 MOS band diagrams for (a) $V_{ox} < q\phi_B$ (direct tunneling) and (b) $V_{ox} > q\phi_B$ (Fowler-Nordheim tunneling).

Tunneling Time (see pn junction section)

The tunneling time is not governed by the conventional (classical) transit time concept :

$$t = W/v$$

t=W/v, where W is the barrier width and v is the carrier velocity, but rather – one thinks – by the quantum transition probability per unit time which is proportional to

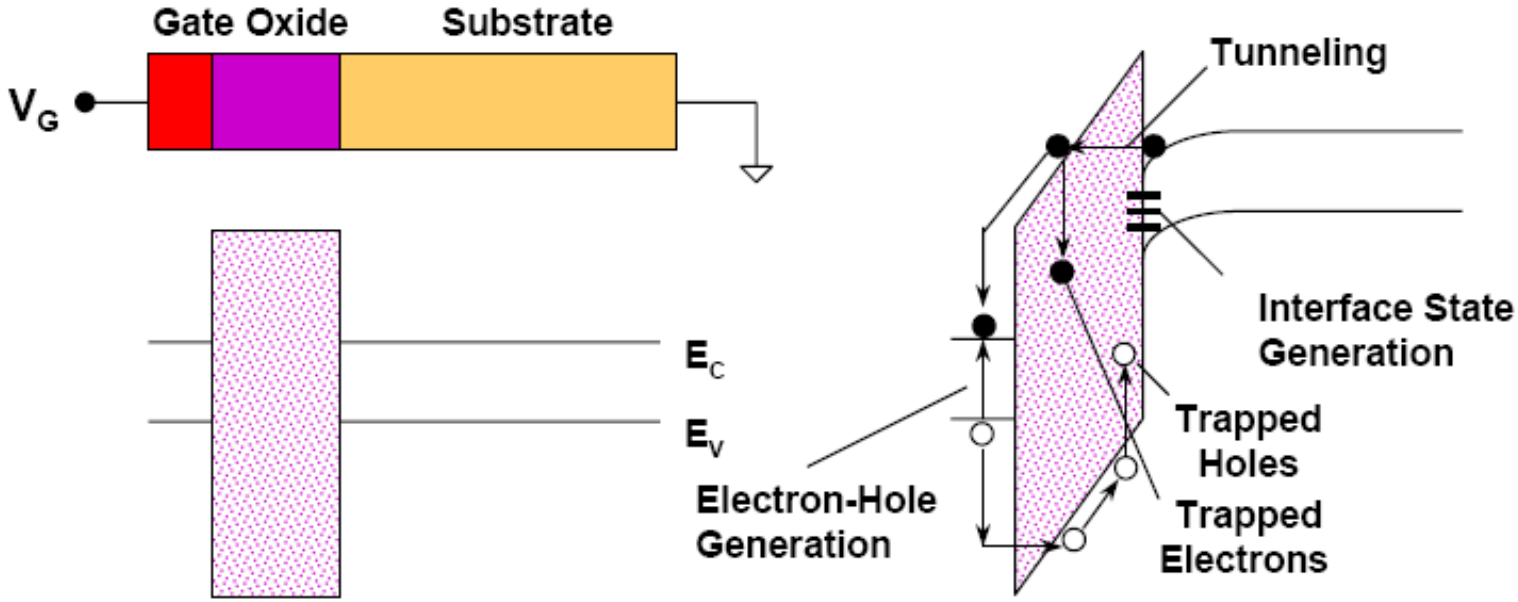
$$t \propto \exp(-2\bar{k}(0) \cdot W) \qquad p = mv = (h/2\pi)k$$

Where k(0) is the average value of momentum encountered in the tunneling path corresponding to an incident carrier with zero transverse momentum and energy equal to the Fermi energy. This tunneling time is very short permitting the use of tunnel devices at very high frequencies.

Oxide Integrity

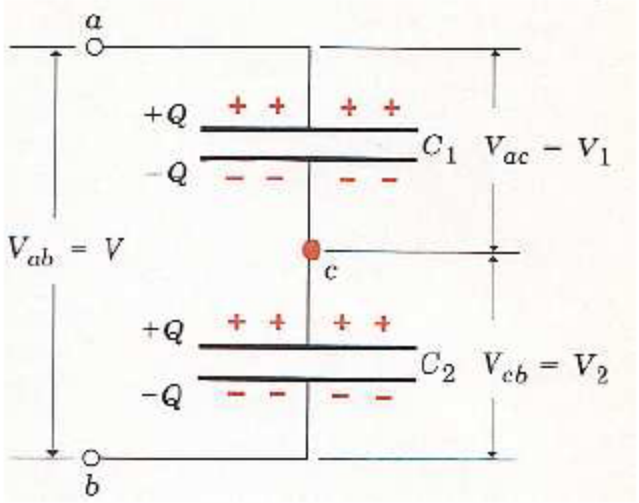
- Energetic electrons ⇒ hole/electron injection into the oxide
- Energetic holes ⇒ hole injection, hole trapping, interface state generation

⇒ *Threshold voltage shifts, transconductance degradation*



More about Capacitors

Capacitors in Series



$V_1 = Q/C_1,\ V_2 = Q/C_2$

$$V = V_1 + V_2 = Q\left(\frac{1}{C_1} + \frac{1}{C_2}\right)$$

$$\frac{1}{C_{eq}} = \frac{1}{C_1} + \frac{1}{C_2}$$

Equivalent Capacitance C_{eq}

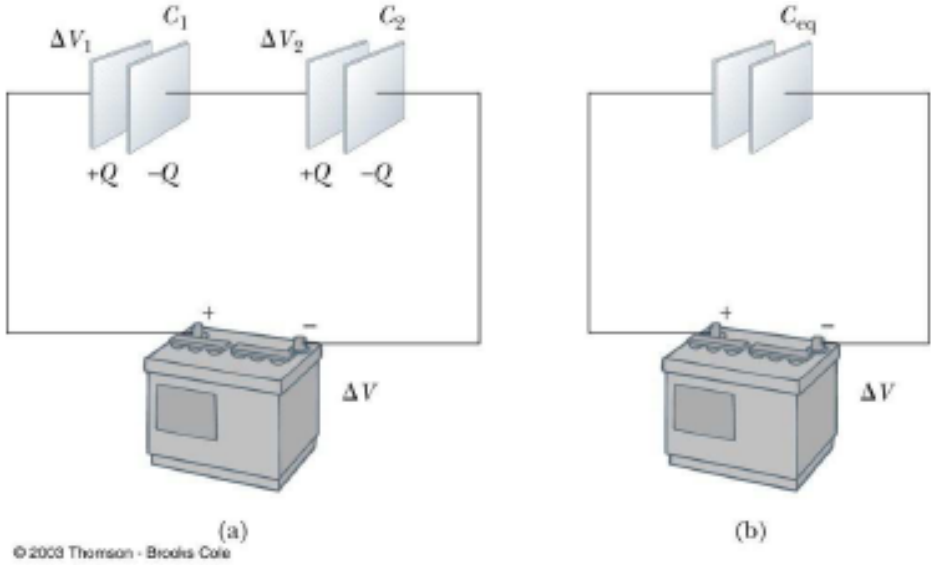
In a series connection the magnitude of charge on all plates is the same!

Capacitors in Series

$$V = V_1 + V_2$$

$$\frac{1}{C_{eq}} = \frac{1}{C_1} + \frac{1}{C_2}$$

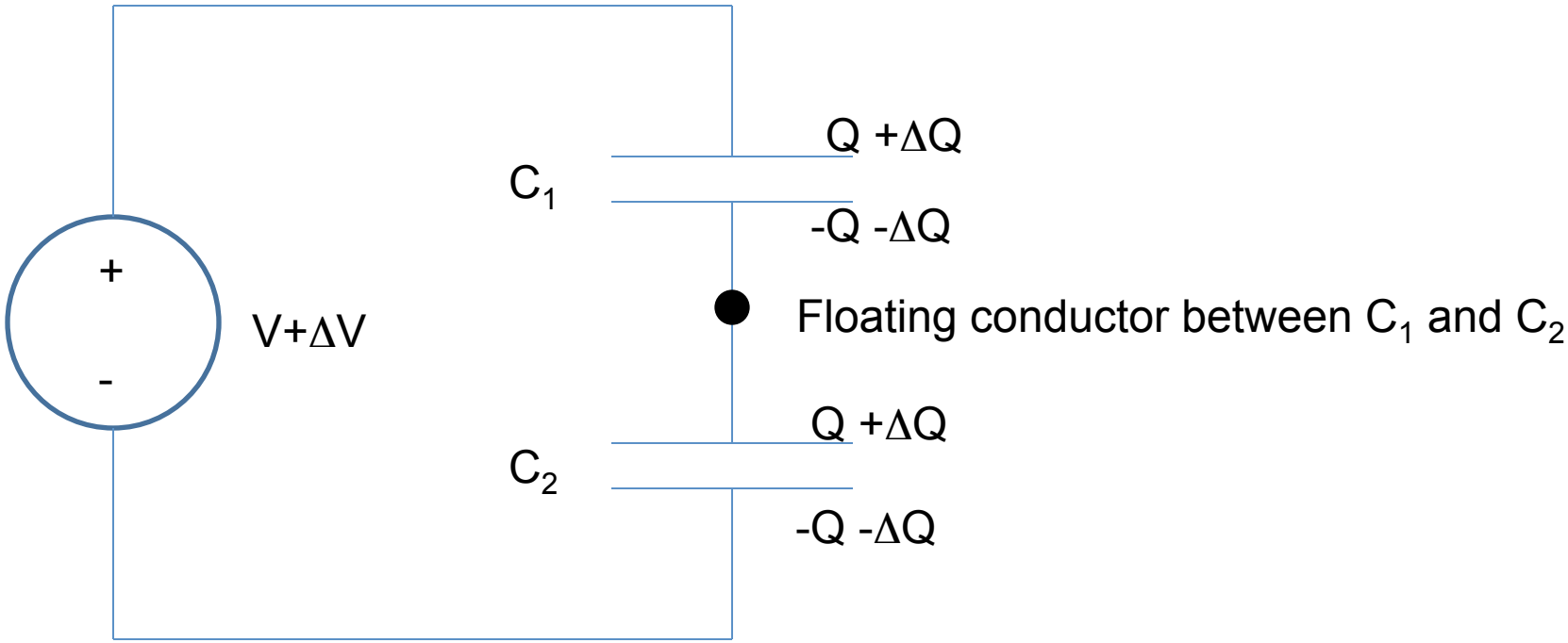
- An equivalent capacitor can be found that performs the same function as the series combination
- The potential differences add up to the battery voltage



The equivalent capacitance of a series combination is always less than any individual capacitor in the combination

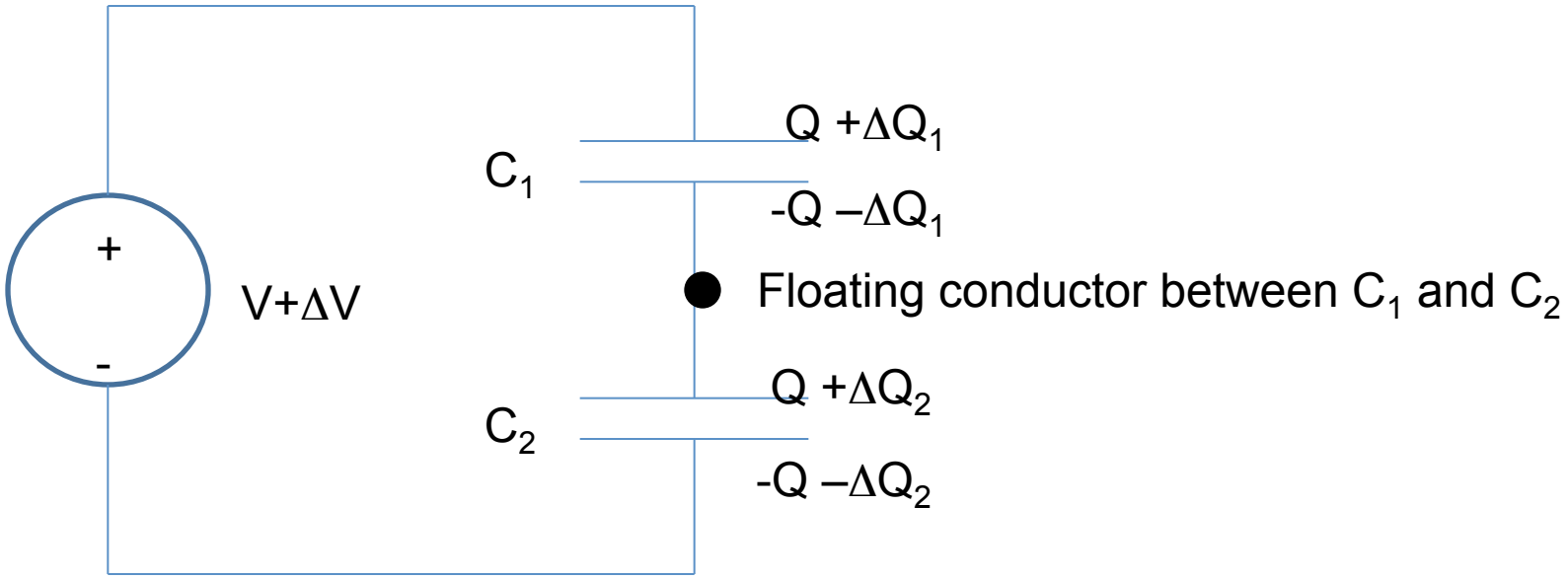
When two or more capacitors are connected to a power supply in series, the total capacitance between them reduces. They become less able to store charge.

Capacitive Voltage Divider



What is the potential of the floating conductor between the capacitors?

Capacitive Voltage Divider



No net charge can be introduced to the floating node, so

$$\Delta Q_1 = C_1 \Delta V_1$$
$$\Delta Q_2 = C_2 \Delta V_2$$

$$-\Delta Q_1 + \Delta Q_2 = 0$$
$$C_1 \Delta V_1 = C_2 \Delta V_2$$
$$\Delta V = \Delta V_1 + \Delta V_2$$

$$\Delta V_2 = \frac{C_1}{C_1 + C_2} \cdot \Delta V$$

Capacitive Voltage Divider

$$\Delta Q = C_1 \Delta V_1$$

$$\Delta Q = C_2 \Delta V_2$$

$$\Delta V = \Delta V_1 + \Delta V_2$$

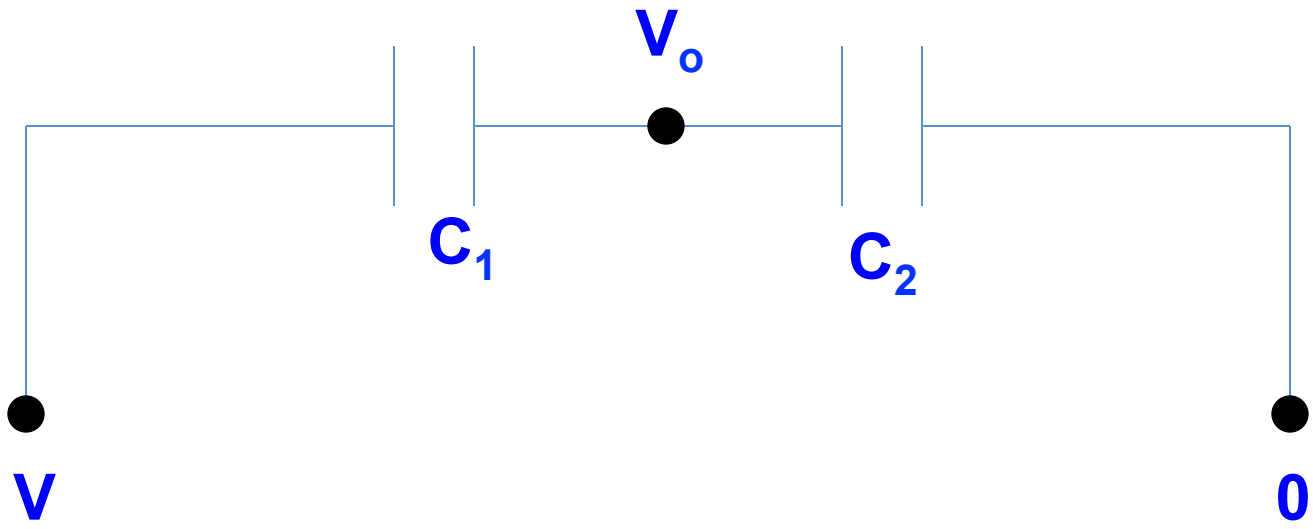
$$\Delta Q_1 - \Delta Q_2 = 0$$

$$C_1 \Delta V_1 = C_2 \Delta V_2$$

$$\Delta V = \Delta V_1 + \Delta V_2$$

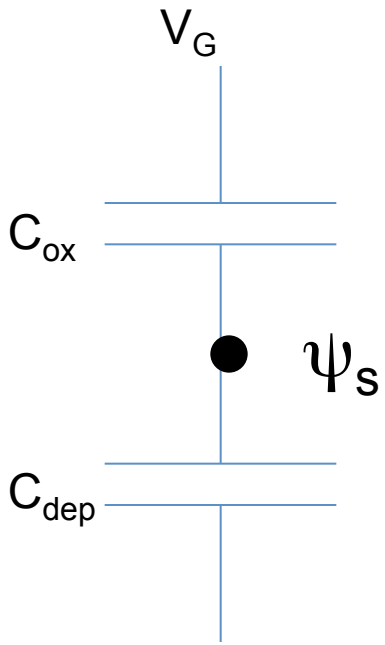
$$\Delta V_2 = \frac{C_1}{C_1 + C_2} \cdot \Delta V$$

Capacitive Voltage Divider – Circuit Model



$$V_o = \frac{C_1}{C_1 + C_2} \cdot (V - 0) = \frac{C_1}{C_1 + C_2} \cdot V =$$

Example MOS Capacitor (without biased source drains): inversion channel characterized by surface potential is a floating node



Capacitive Voltage Divider *Reactance formalism*

Two capacitors in series are commonly used as a capacitive voltage divider. The capacitors split the output voltage in proportion to their reactance (and inversely proportional to their capacitance).

What is the output voltage for the capacitive voltage divider?

Using reactance

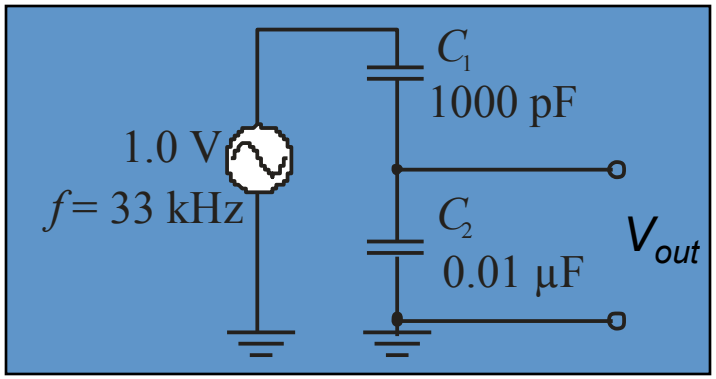
$$X_{C1} = \frac{1}{2\pi f C_1} = \frac{1}{2\pi(33\text{ kHz})(1000\text{ pF})} = 4.82\text{ k}\Omega$$

$$X_{C2} = \frac{1}{2\pi f C_2} = \frac{1}{2\pi(33\text{ kHz})(0.01\ \mu\text{F})} = 482\ \Omega$$

$$X_{C(tot)} = X_{C1} + X_{C2}$$

$$= 4.82\text{ k}\Omega + 482\ \Omega = 5.30\text{ k}\Omega$$

$$V_{out} = \left(\frac{X_{C2}}{X_{C(tot)}}\right)V_s = \left(\frac{482\ \Omega}{5.30\text{ k}\Omega}\right)1.0\text{ V} = 91\text{ mV}$$



The derivation with reactances is useful because it puts capacitive voltage divider on the same footing with the resistive voltage divider, even for dc applications.

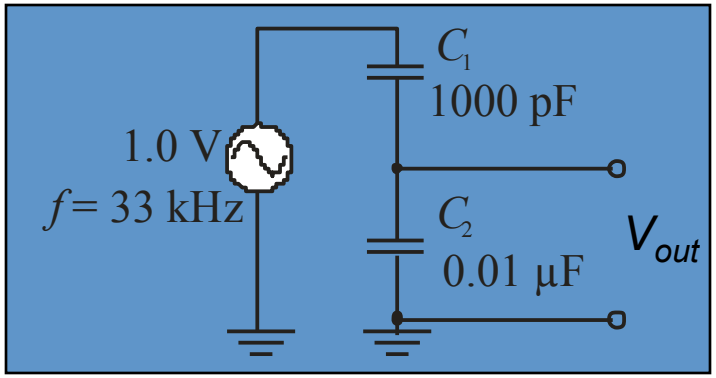
Capacitive Voltage Divider

Instead of using a ratio of reactances in the capacitor voltage divider equation, you can use a ratio of the total series capacitance to the output capacitance (multiplied by the input voltage). The result is the same. For the problem presented in the last slide

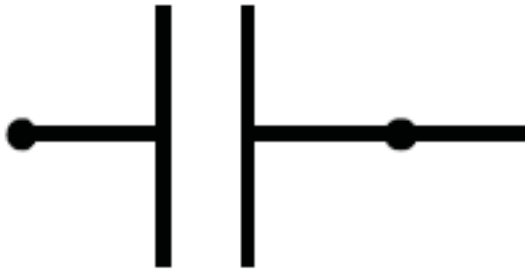
$$C_{(tot)} = \frac{C_1 C_2}{C_1 + C_2} = \frac{(1000\ \text{pF})(0.01\ \mu\text{F})}{1000\ \text{pF} + 0.01\ \mu\text{F}} = 909\ \text{pF}$$

$$V_{out} = \left(\frac{C_{(tot)}}{C_2}\right) V_s = \left(\frac{909\ \text{pF}}{0.01\ \mu\text{F}}\right) 1.0\ \text{V} = 91\ \text{mV}$$

$$V_{out} = \left(\frac{C_{(tot)}}{C_2}\right) V_s = \left(\frac{C_1}{C_1 + C_2}\right) V$$



Capacitance-Spring Analogy



$$V = \frac{1}{C}Q$$

Hooks law

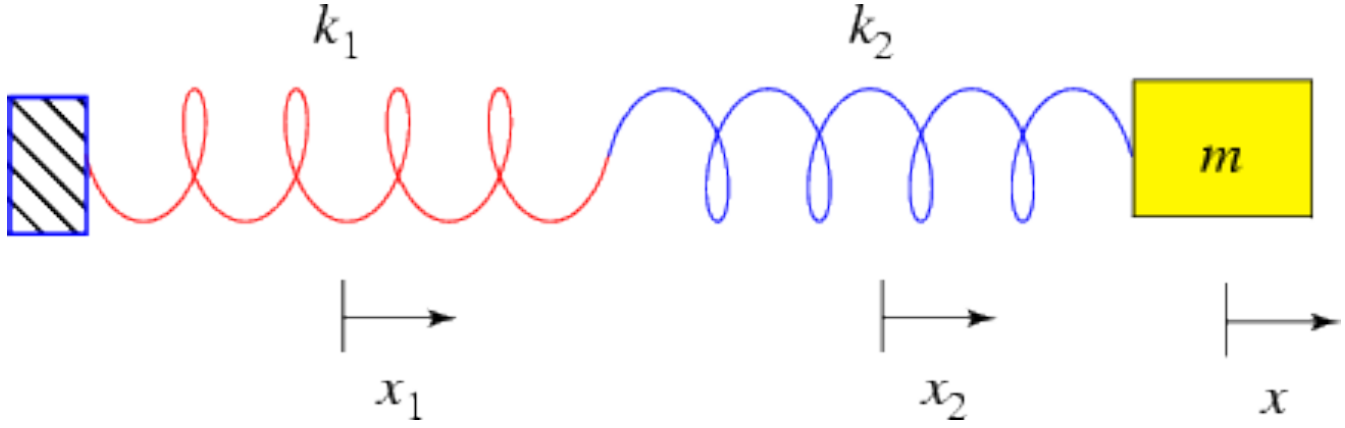
$$F = kx$$

k spring constant

The ability of a capacitor to store charge in response to the applied voltage is called "capacitance".

Capacitance-Spring Analogy

analogy of capacitances and springs in series

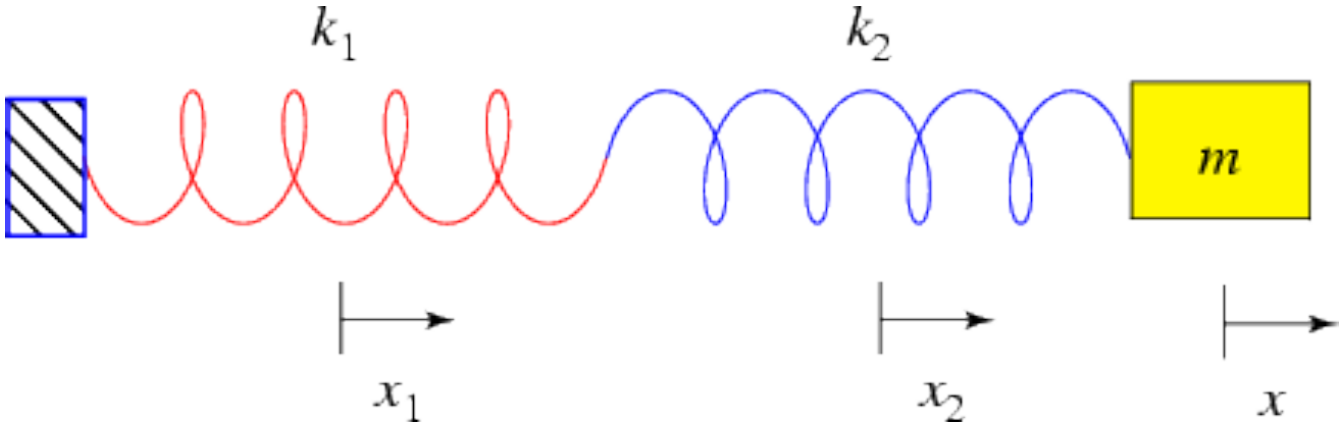


$$F = -k_1 x_1 = -k_2 x_2. \qquad x_1 = \frac{k_2}{k_1} x_2.$$

$$F = -k_{\text{eff}}(x_1 + x_2), \qquad k_2 x_2 = k_{\text{eff}} \left(\frac{k_2}{k_1} x_2 + x_2 \right).$$

$$k_2 = k_{\text{eff}} \left(\frac{k_2}{k_1} + 1 \right). \qquad k_{\text{eff}} = \left(\frac{1}{k_1} + \frac{1}{k_2} \right)^{-1},$$

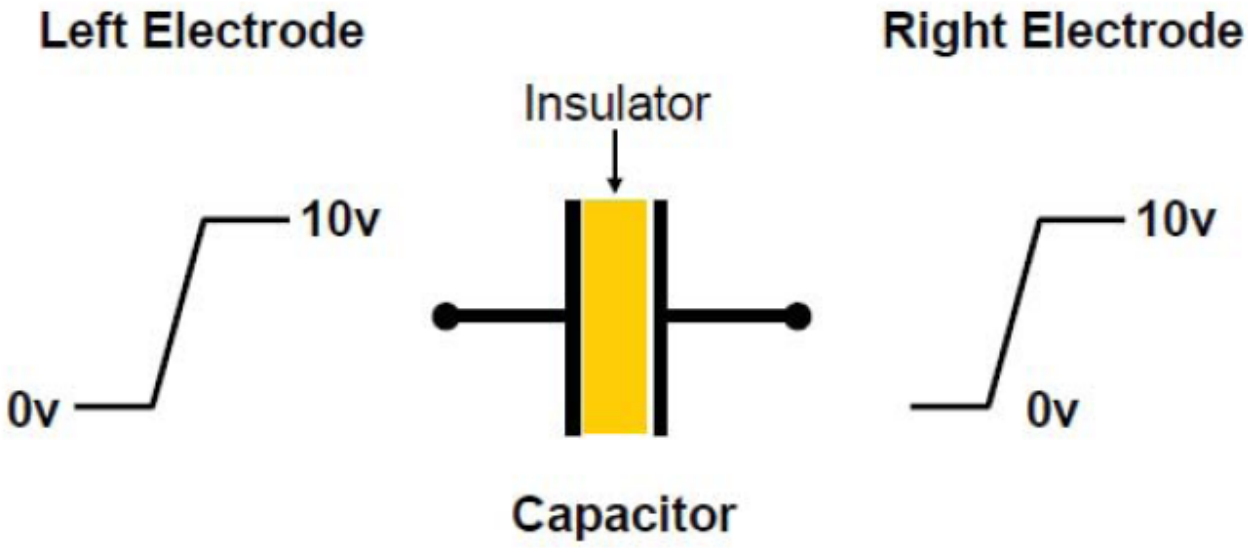
Capacitance-Spring Analogy



$$k_{eff} = \frac{k_1 k_2}{k_1 + k_2}$$

Two springs in series provide a more compliant (less stiff) effective spring constant than individual springs.

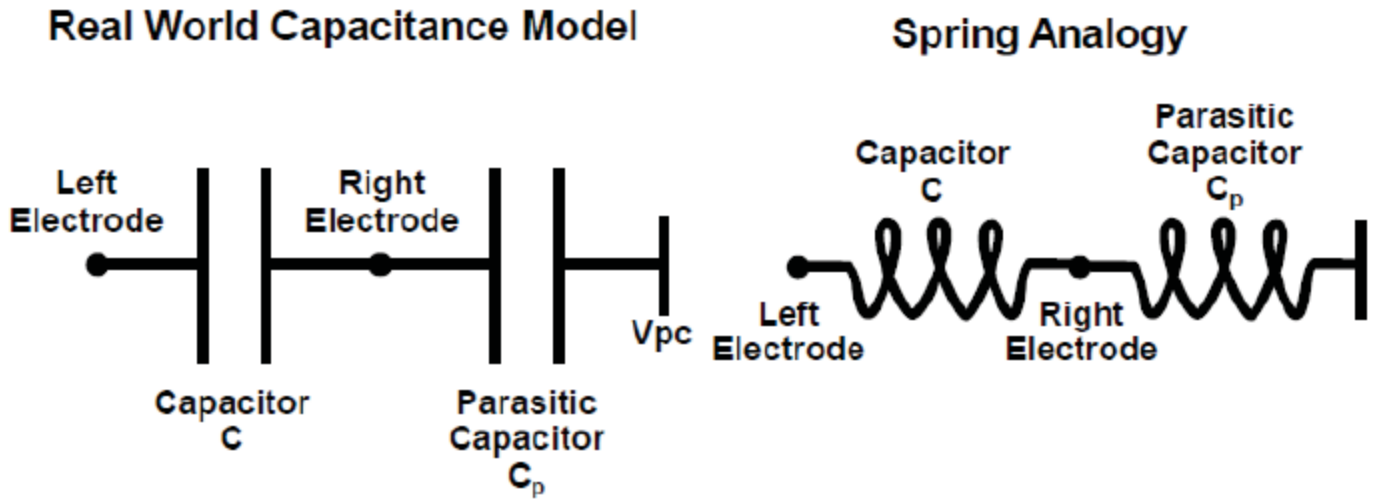
Capacitor with one right electrode floating



One interesting property of the capacitor is that it can be used to change the voltage of one side of the capacitor by just changing the voltage of the other side. Assume the right side electrode to be floating and to be initially at ground potential. If left side is increased from zero to 10V, the right side will be capacitively coupled to the same potential. Thus the right electrode will mirror the potential on the left side. An isolated capacitor will image this behavior perfectly and it is said to have the capacitive coupling ratio 1:1.

Using the spring analogy it is easy to visualize this situation: if the left side of the spring is not attached to anything ("floating"), then we would pull the whole spring by a certain distance and the spring would not extend and no energy would be stored.

Capacitor with parasitic capacitor in series

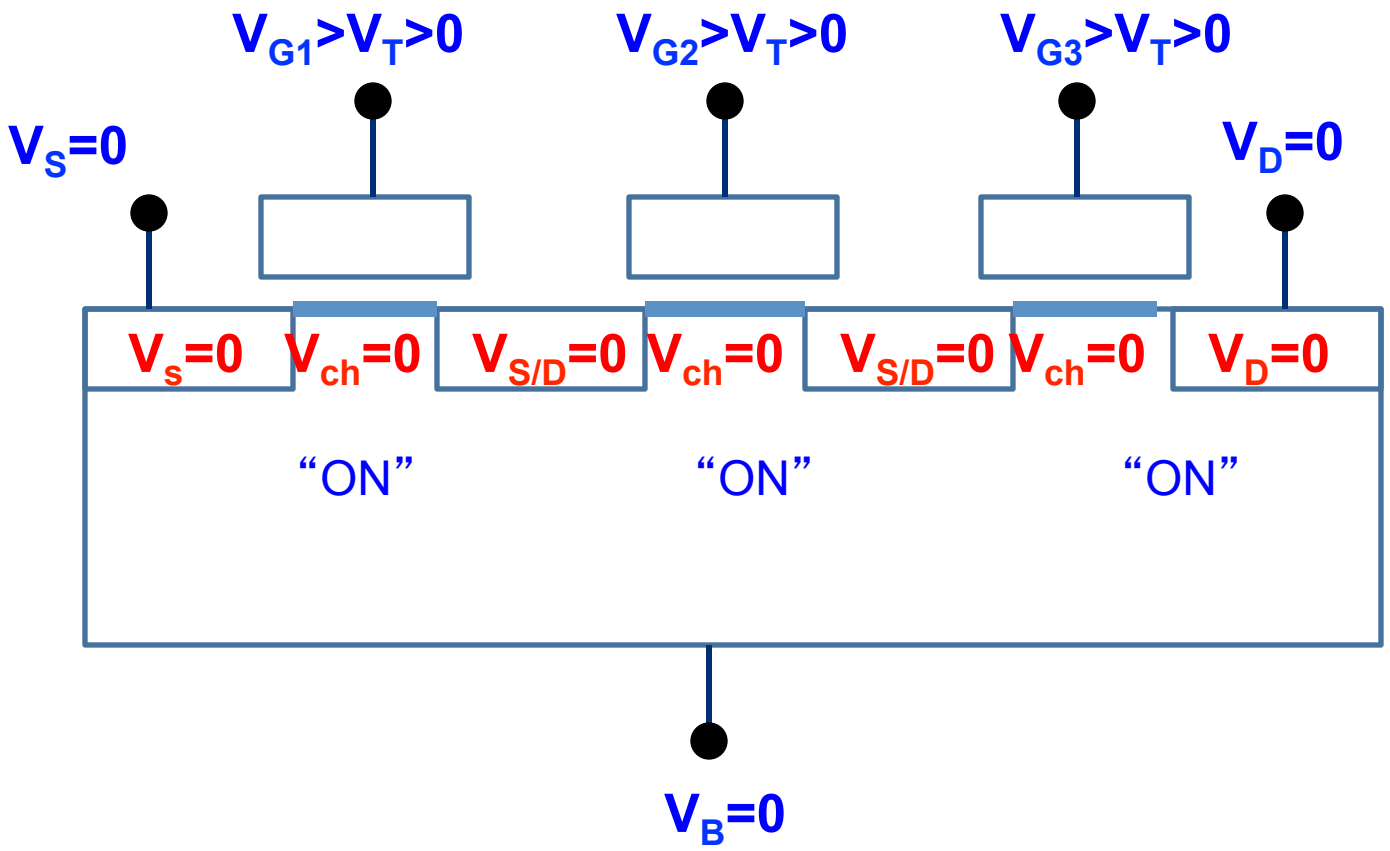


In practice, the ideal capacitive ratio of 1 will be compromised by a parasitic capacitance associated with the right electrode. The capacitive ratio of left electrode to the right electrode will be less than 1.

$$r = \frac{C}{C + C_p}$$

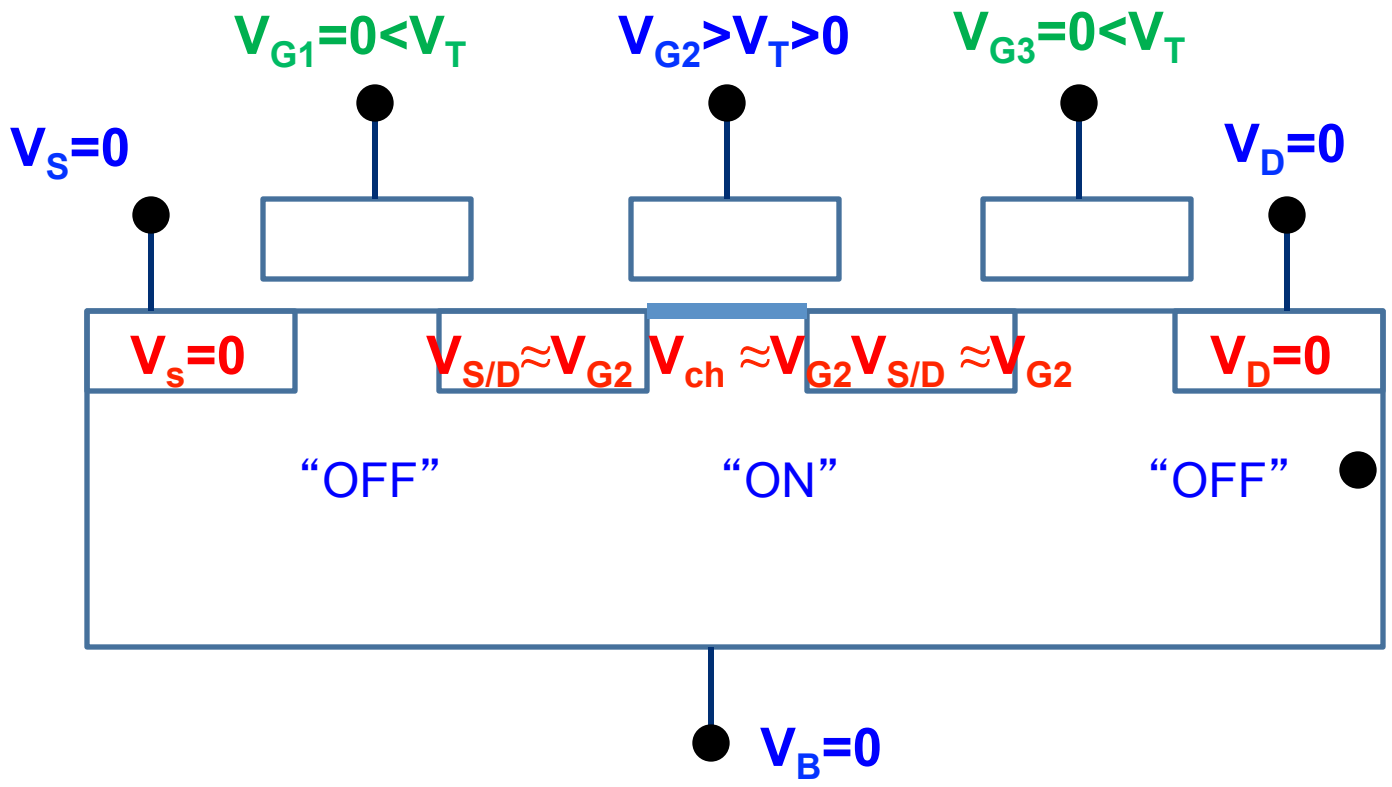
Two spring in series will be always less stiff than any of the springs alone.

Capacitive "Self-Boost" Effect



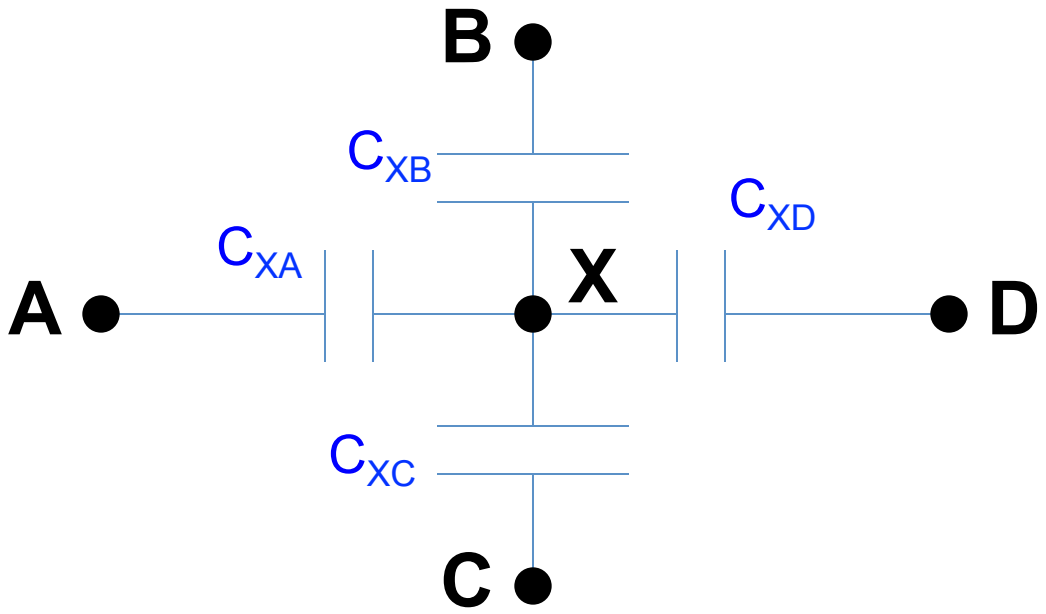
Initial situation: all transistors are conducting and thus all source/drain and channel regions are at ground potential (zero volt).

Capacitive "Self-Boost" Effect



The potential of source, drain and channel of the 2nd transistor has been boosted to a potential close to V_{G2}-V_T. S/D and channel of the central MOSFET form one plate and are floating.

General case:
coupling ratio and coupling coefficients



Obviously all the capacitances shown have a common floating electrode X

The total capacitance of the node X is the sum of the capacitances:

$$C_{xtot} = C_{XA} + C_{XB} + C_{XC} + C_{XD}$$

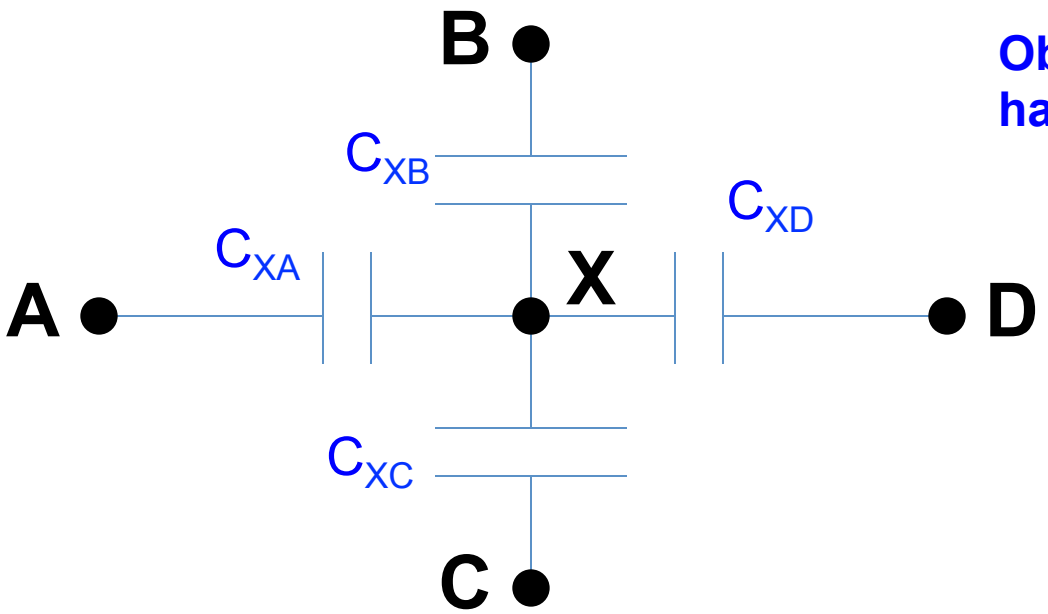
We define coupling coefficients as:

$$r_A = \frac{C_{XA}}{C_{Xtot}} \quad r_A = \frac{C_{XB}}{C_{Xtot}} \quad r_C = \frac{C_{XC}}{C_{Xtot}} \quad r_D = \frac{C_{XD}}{C_{Xtot}}$$

The voltage on the X node is therefore:

$$V_X = r_A V_A + r_B V_B + r_C V_C + r_D V_D$$

Coupling ratio and coupling coefficients



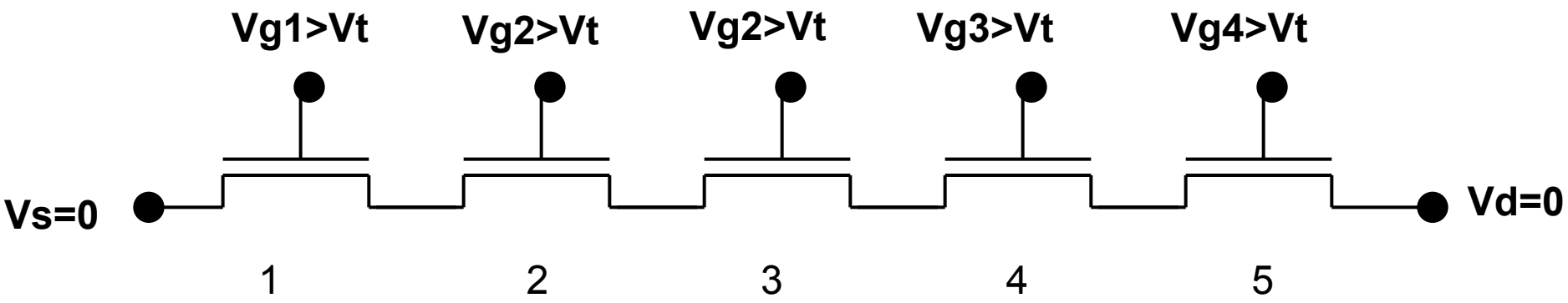
Obviously all the capacitances have a common floating electrode X

$$V_X = r_A V_A + r_B V_B + r_C V_C + r_D V_D$$

One can "drive" X node by the node D with the effectivity of r_D, or by the node A with effectivity r_A and so on.

Capacitive Self-Boost Effects

All transistors are identical and they are arranged in series (they share source/drain regions; their threshold voltage is V_T=1V; the substrate is grounded. The total capacitance of the gate electrode is $C_{tot}=C_{ox}+C_{gs}+C_{gd}+C_{par}$. Assume that $C_{par}=0.1C_{tot}$

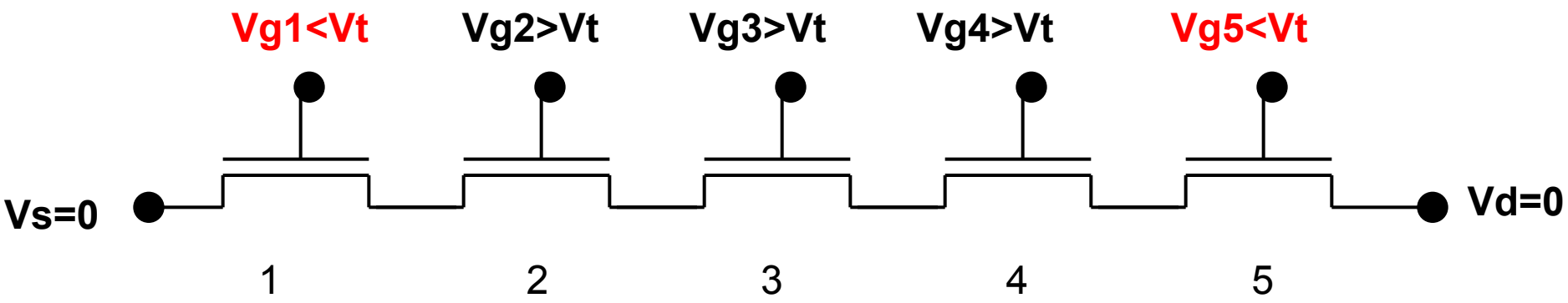


What are the channel potentials of isolated transistors 1,2,3,4? **0V**

What are the potentials of the shared source/drain regions? **0V**

Capacitive Self-Boost Effects

All transistors are identical and they are arranged in series (they share source/drain regions; their threshold voltage is V_T=1V; the substrate is grounded. The total capacitance of the gate electrode is $C_{tot}=C_{ox}+C_{gs}+C_{gd}+C_{par}$. Assume that $C_{par}=0.1C_{tot}$



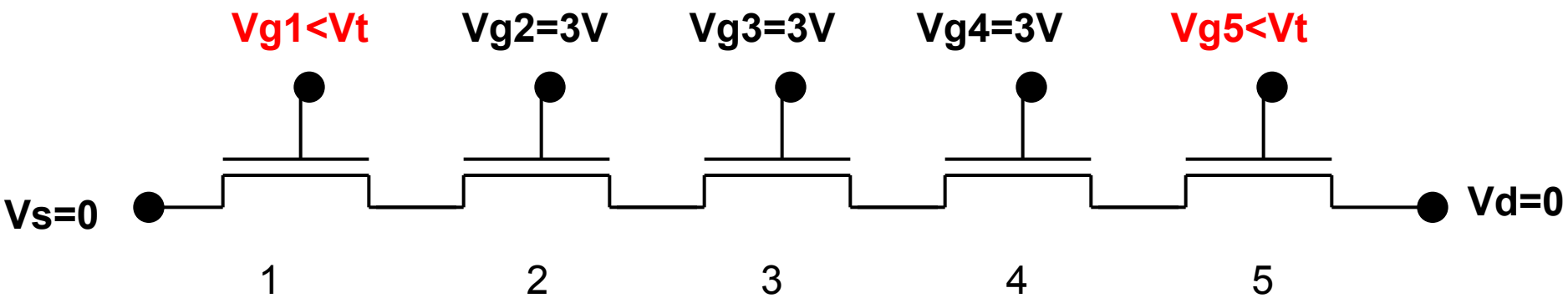
What are the channel potentials of isolated transistors 1,2,3,4?

What are the potentials of the shared source/drain regions?

0.9x[(Vg2-Vt)+(Vg3-Vt)+(Vg4-Vt)]/3

Capacitive Self-Boost Effects

All transistors are identical and they are arranged in series (they share source/drain regions; their threshold voltage is V_T=1V; the substrate is grounded. The total capacitance of the gate electrode is $C_{tot}=C_{ox}+C_{gs}+C_{gd}+C_{par}$. Assume that $C_{par}=0.1C_{tot}$



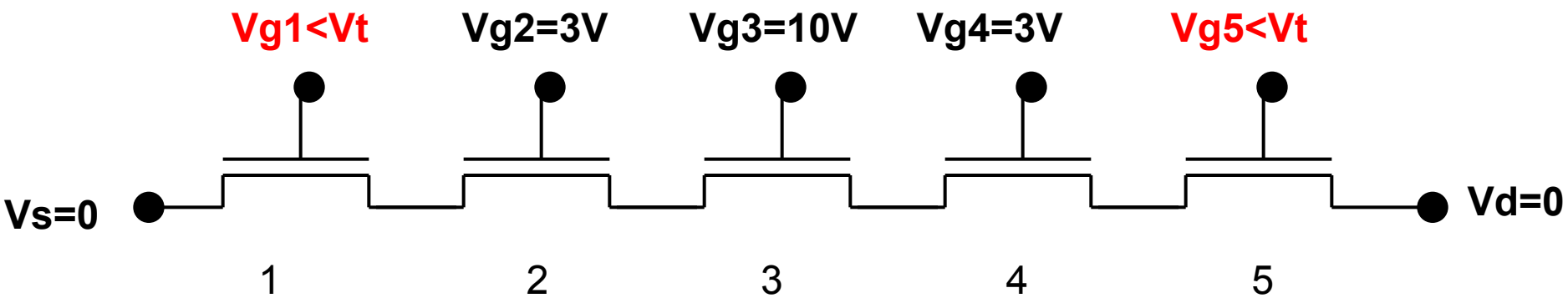
What are the channel potentials of isolated transistors 1,2,3,4?

What are the potentials of the shared source/drain regions?

$0.9x[(3-1)+(3-1)+(3-1)]/3 = 1.8V$

Capacitive Self-Boost Effects

All transistors are identical and they are arranged in series (they share source/drain regions; their threshold voltage is V_T=1V; the substrate is grounded. The total capacitance of the gate electrode is $C_{tot}=C_{ox}+C_{gs}+C_{gd}+C_{par}$. Assume that $C_{par}=0.1C_{tot}$



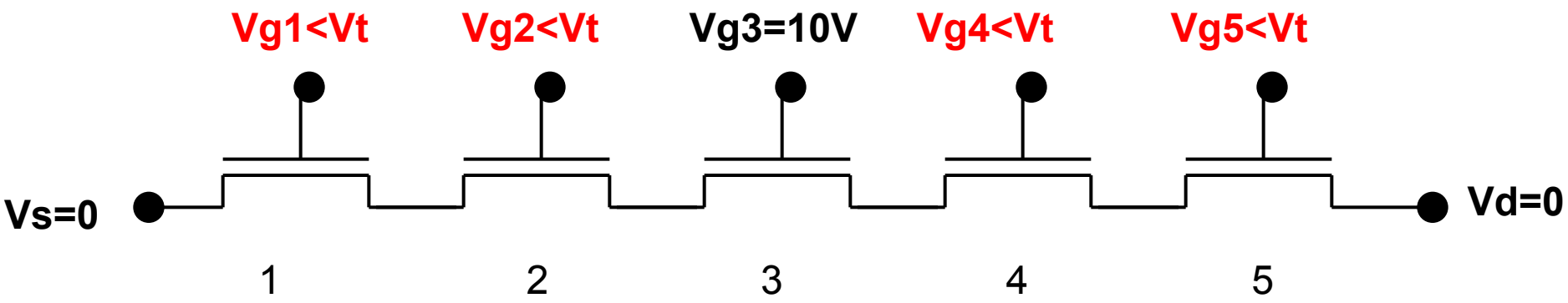
What are the channel potentials of isolated transistors 1,2,3,4?

What are the potentials of the shared source/drain regions?

0.9x[(3-1)+(10-1)+(3-1)]/3 = 3.9V

LOCAL SELF-BOOST EFFECT

All transistors are identical and they are arranged in series (they share source/ drain regions; their threshold voltage is V_T=1V; the substrate is grounded. The total capacitance of the gate electrode is $C_{tot}=C_{ox}+C_{gs}+C_{gd}+C_{par}$. Assume that $C_{par}=0.1C_{tot}$



What is the channel potential of transistor 3? **0.9x(10-1)= 8.1V**

What is the potential of the shared source/drain regions of transistor 3?

local self-boost effect