MOS Capacitors

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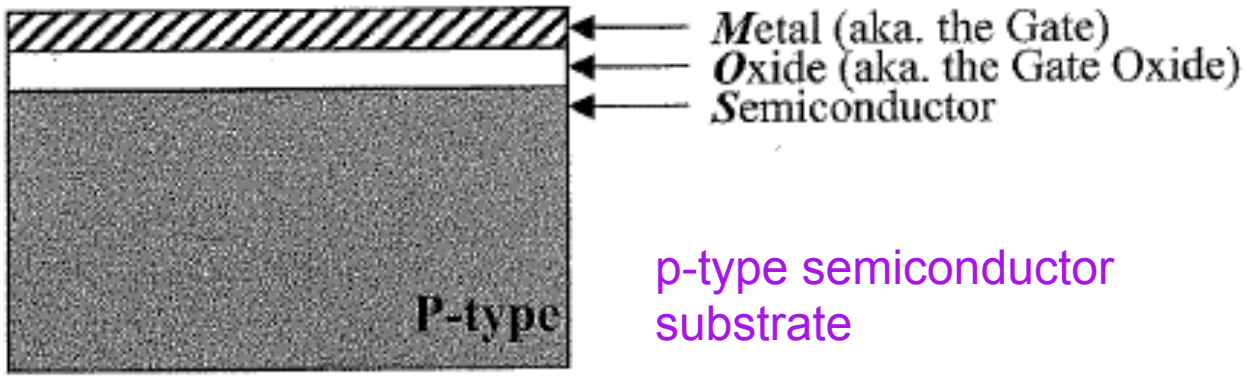
MOS Capacitor

Contents

- ideal MOS Capacitor (accumulation, depletion, inversion)
- Threshold voltage for constant substrate doping
- C-V characteristics
- Real MOS Diode (work fct, built-in charge, flat band voltaged)
- Nonequilibrium analysis (substrate bias, body effect)
- non-uniform channel doping
- Gated diode

MOS Capacitor (Ideal) - Equilibrium

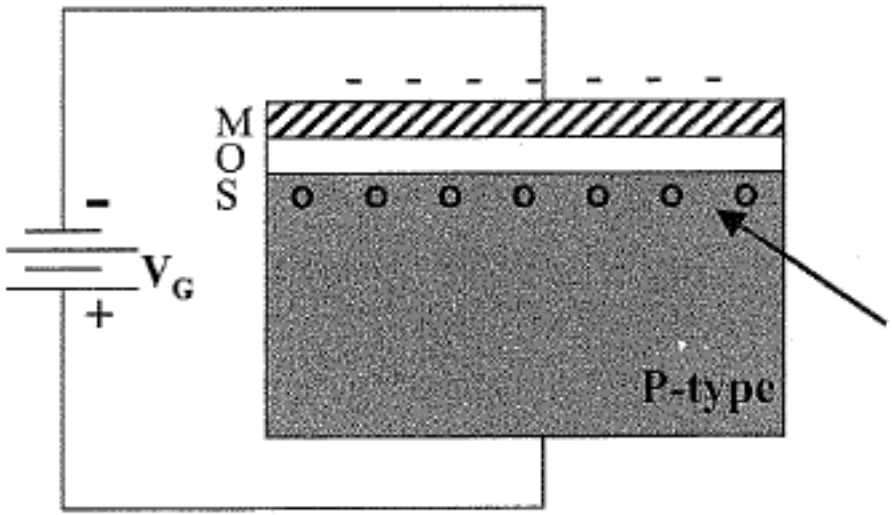


p-type semiconductor substrate

Three possible biasing regimes:

- Accumulation
- Depletion
- Inversion

MOS Capacitor - Accumulation



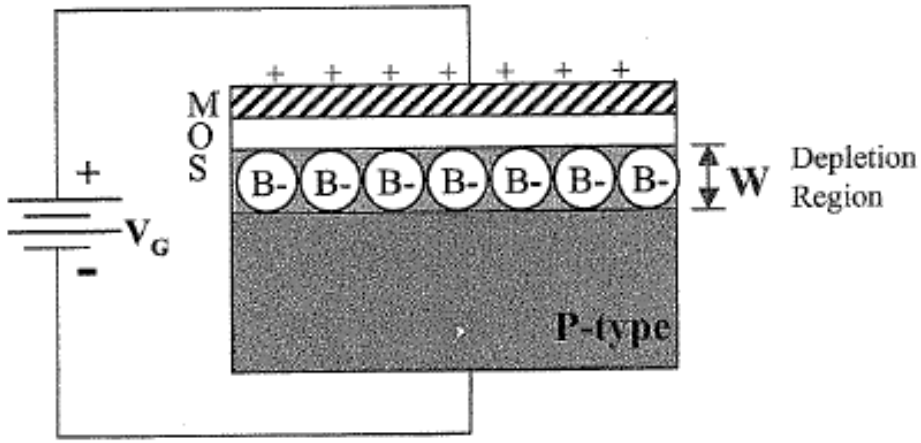
Holes accumulate underneath the oxide to balance the charge on the metal/gate - surface "looks" more P-type

$p_s > N_A$

p_s = hole concentration at semiconductor surface (cm^{-3})

MOS Capacitor - Depletion

$V_G < V_T$
Depletion



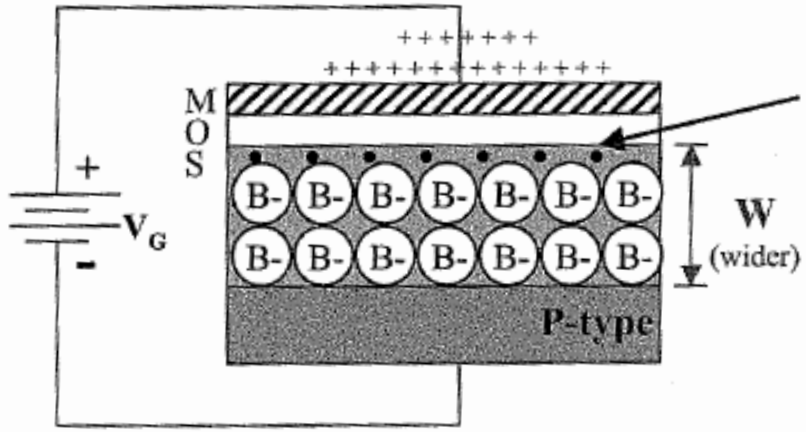
$Q_G = -Q_D$ Uncovered charge in the depletion region (Q_D) balances charge on gate (Q_G)

$Q_D = qAN_AW$ Charge in the depletion region (A = gate area)

As V_G increases $\rightarrow$ Q_G increases $\rightarrow$ W increases $\rightarrow$ Q_D increases $\rightarrow$ $Q_G = Q_D$

MOS Capacitor - Inversion

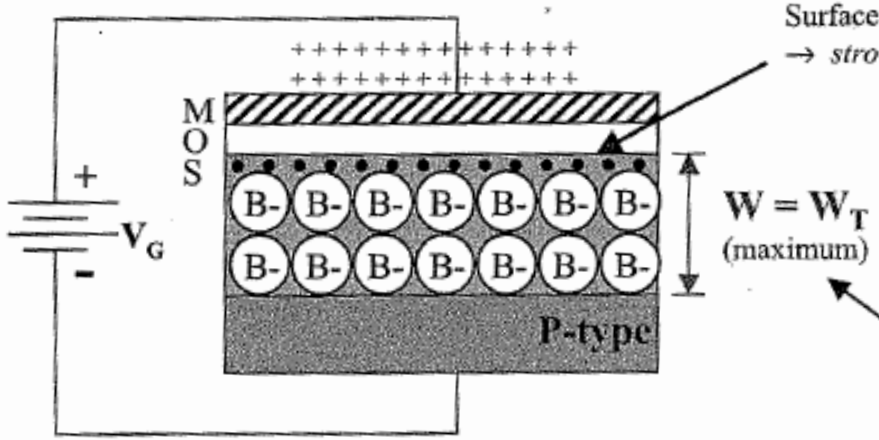
$V_G \rightarrow V_T$
Inversion



Electrons (minority carriers) pile up underneath the oxide → surface "looks" N-type → surface *inversion*

$$Q_G = - (Q_D + Q_n)$$

$V_G = V_T$
Strong Inversion (Threshold)

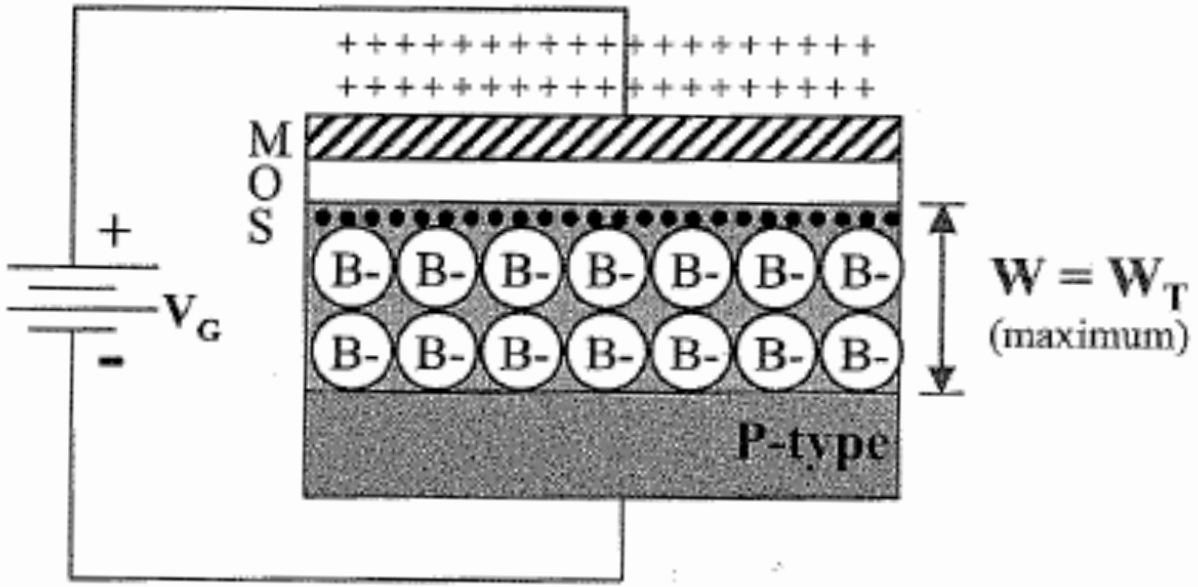


Surface looks as N-type as bulk is P-type → *strong* inversion → *threshold voltage*

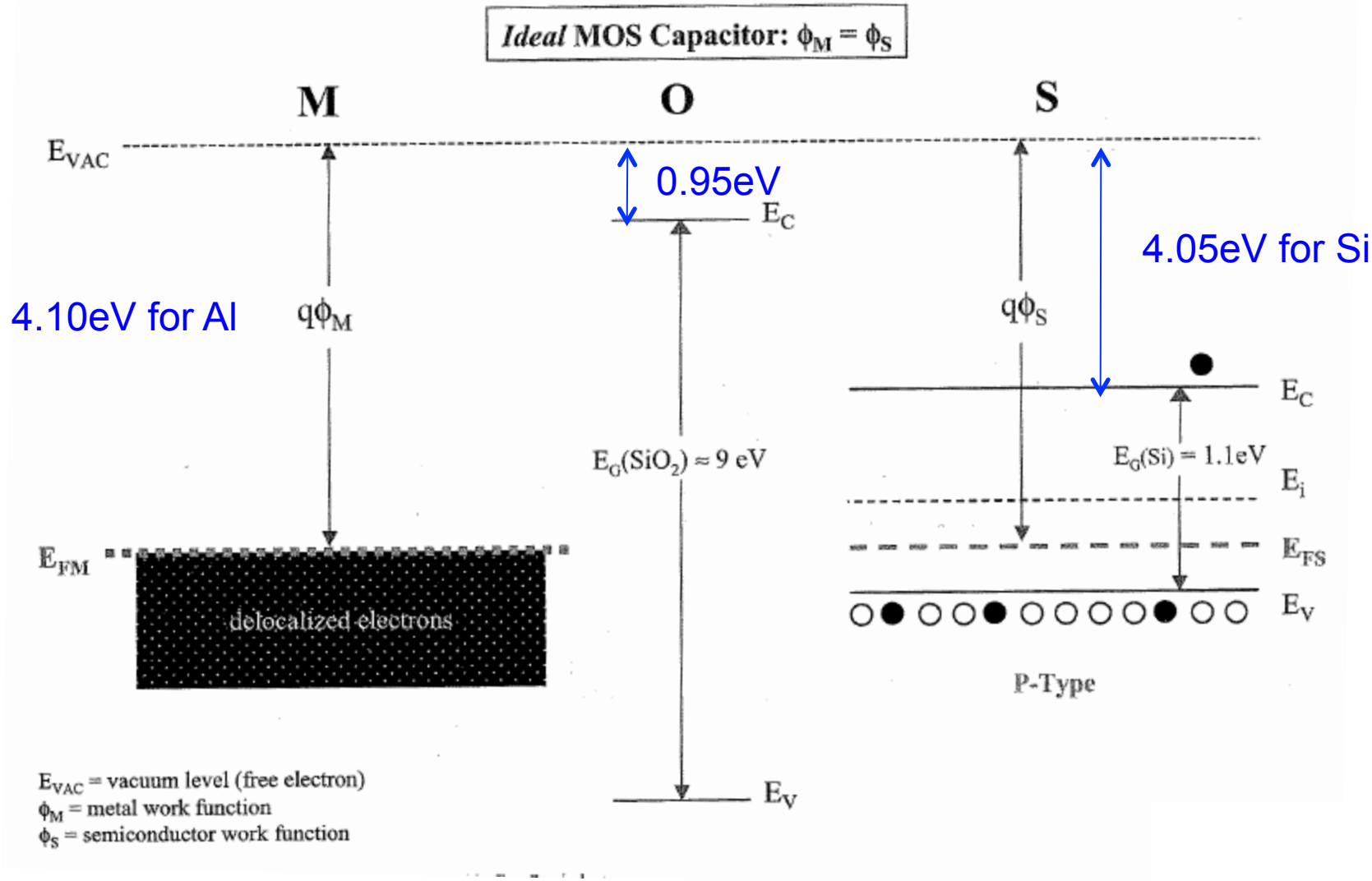
Depletion region reaches its maximum width (W_T) at threshold

MOS Capacitor - Inversion (cont.)

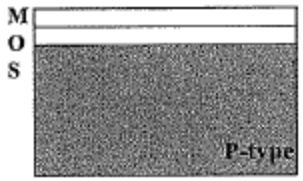
$V_G > V_T$
Beyond Threshold



MOS Capacitor (Ideal) - Band Diagram, Isolated Materials



MOS Capacitor (Ideal) - Band Diagram, Equilibrium



Ideal MOS Capacitor: $\phi_M = \phi_S$

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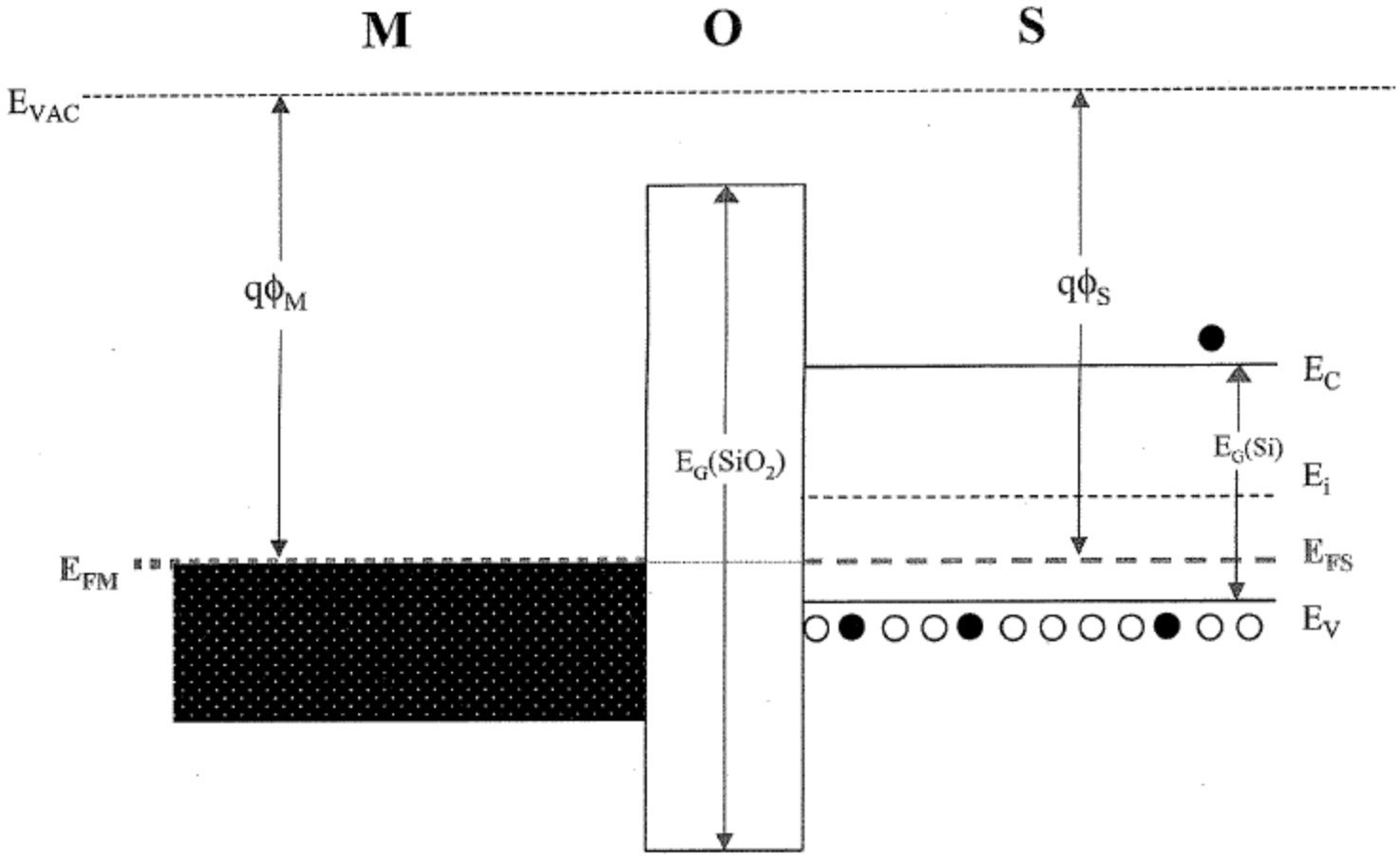
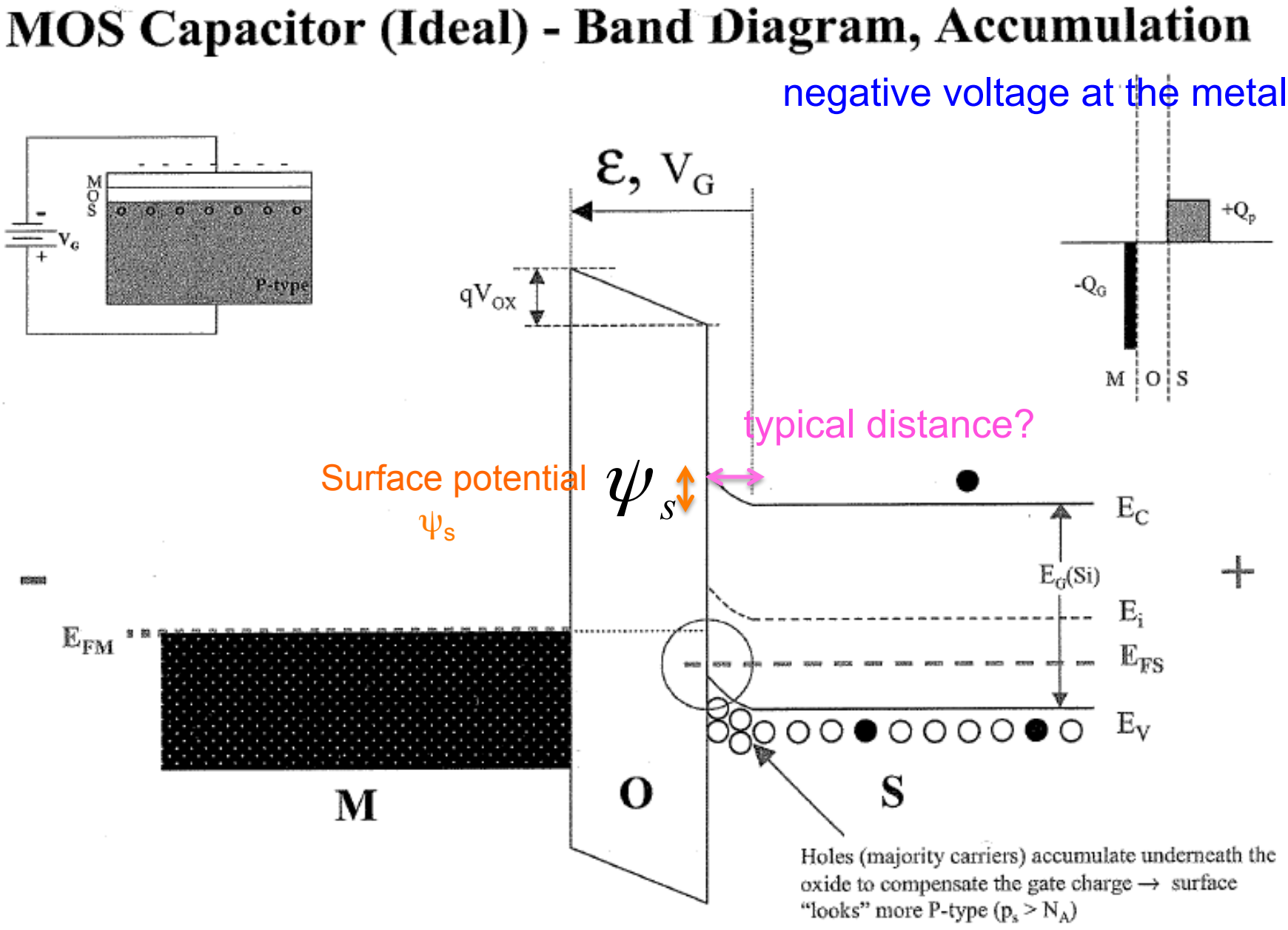
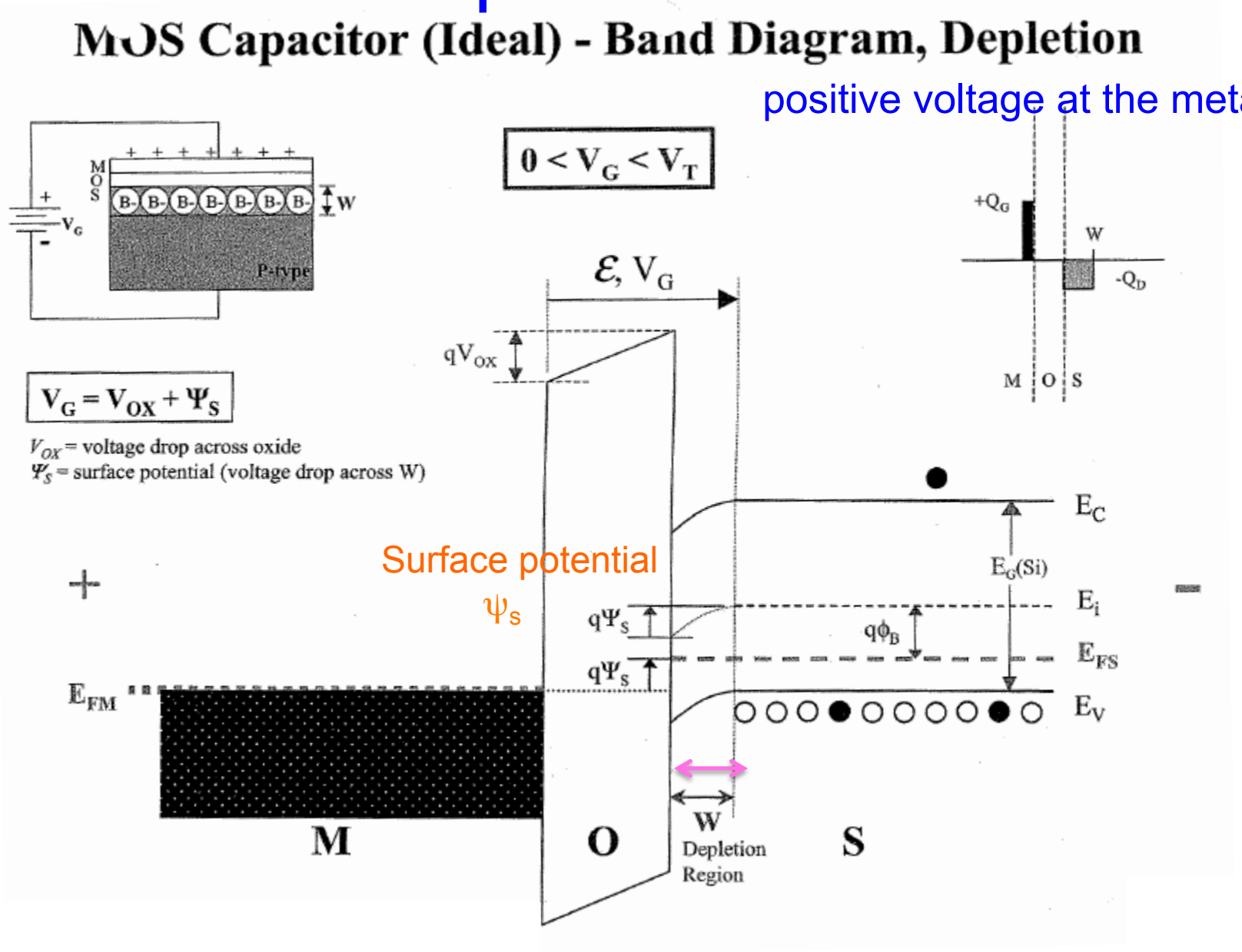


Ideal: metal work function = work function of the semiconductor

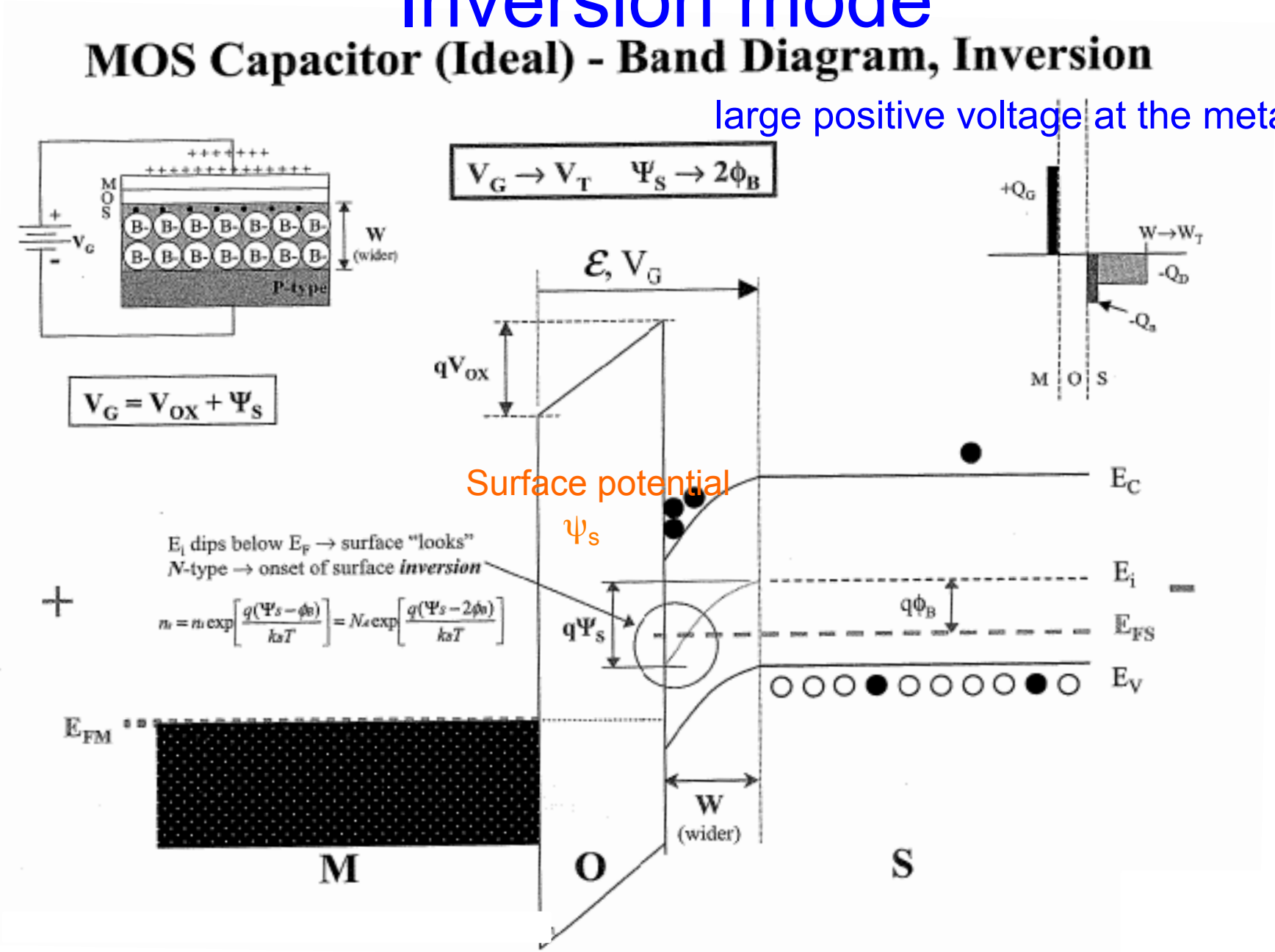
Accumulation mode



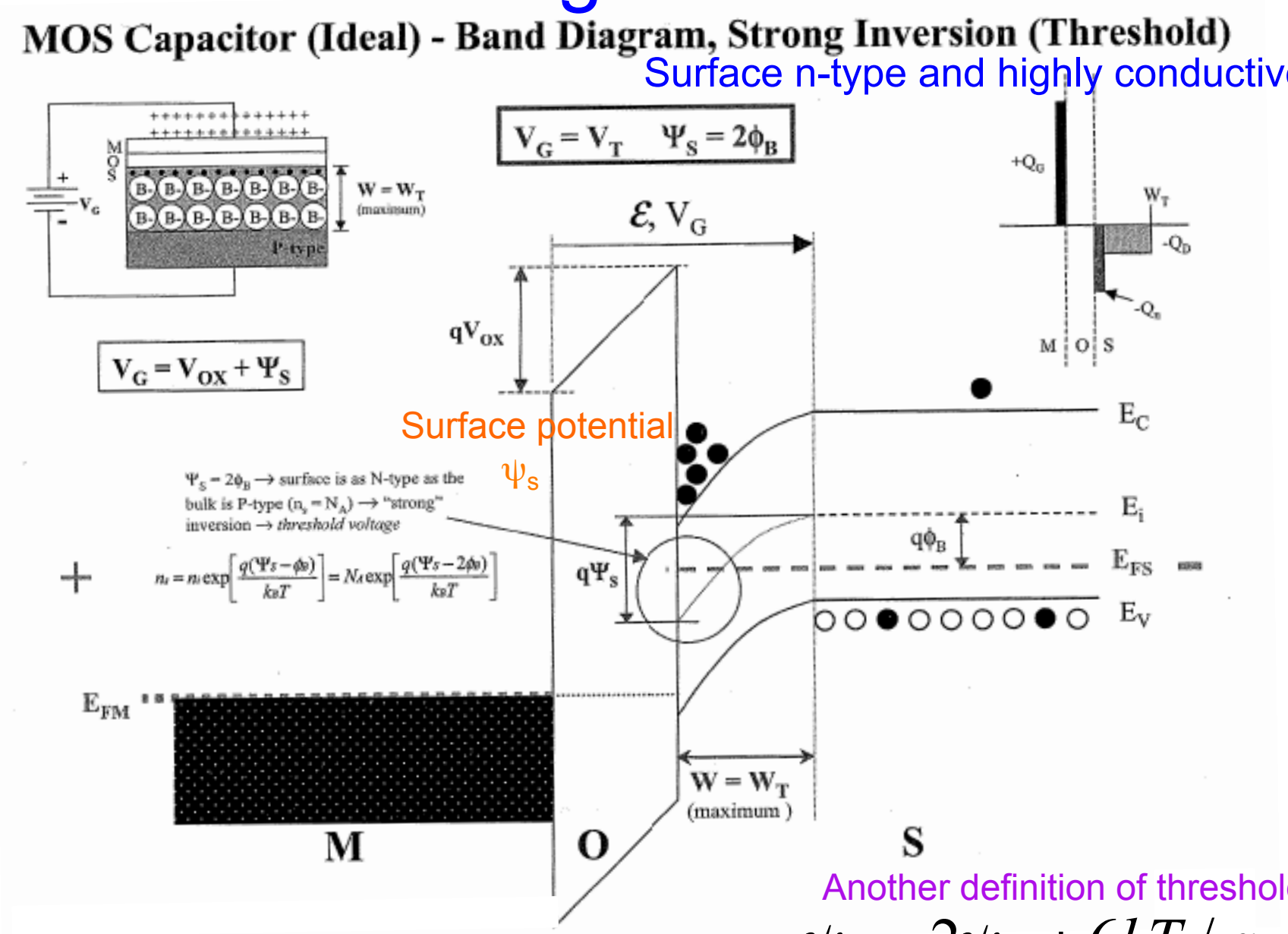
Depletion mode



Inversion mode



Strong Inversion mode

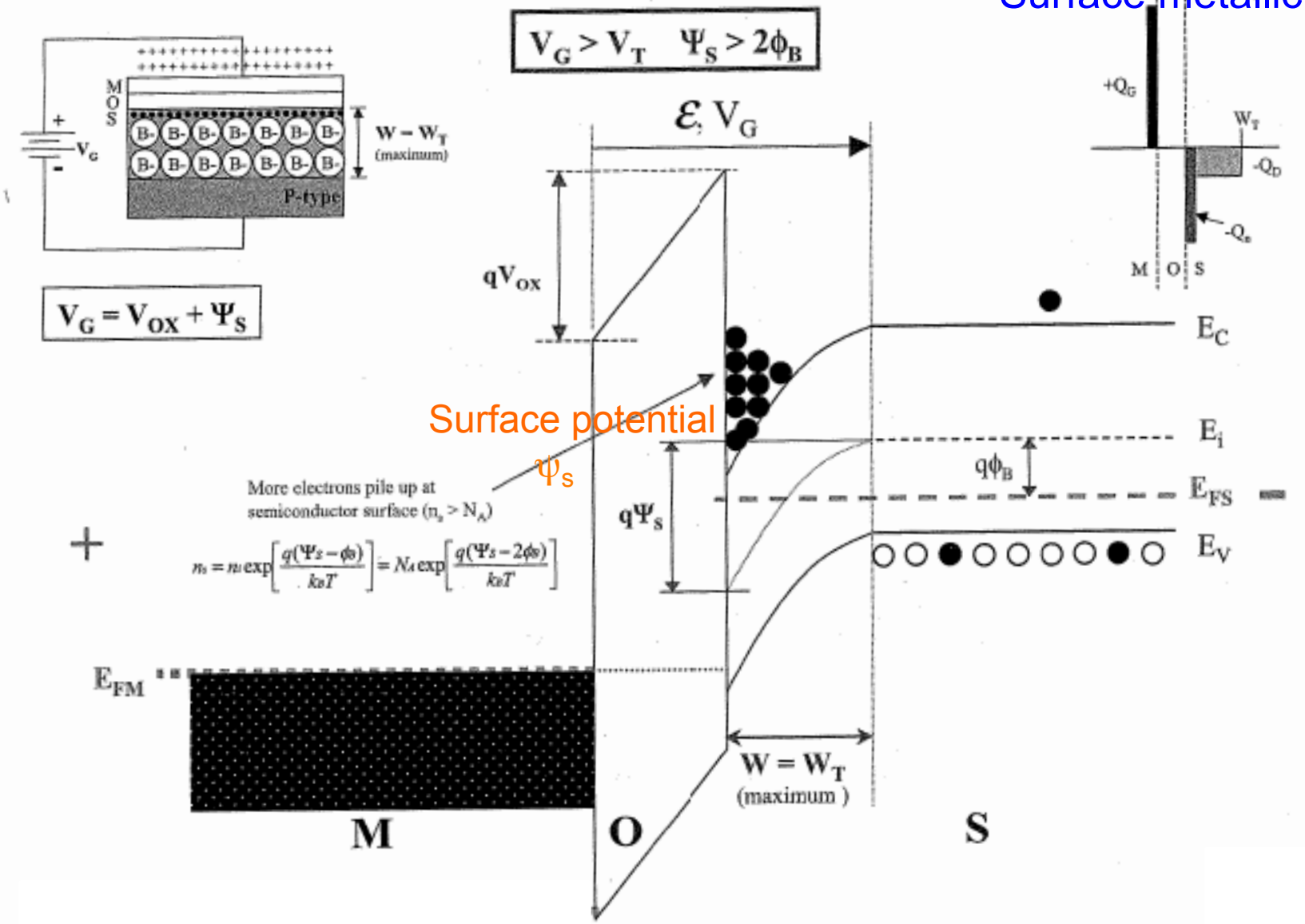


Another definition of threshold

$$\psi_s = 2\psi_B + 6kT/q$$

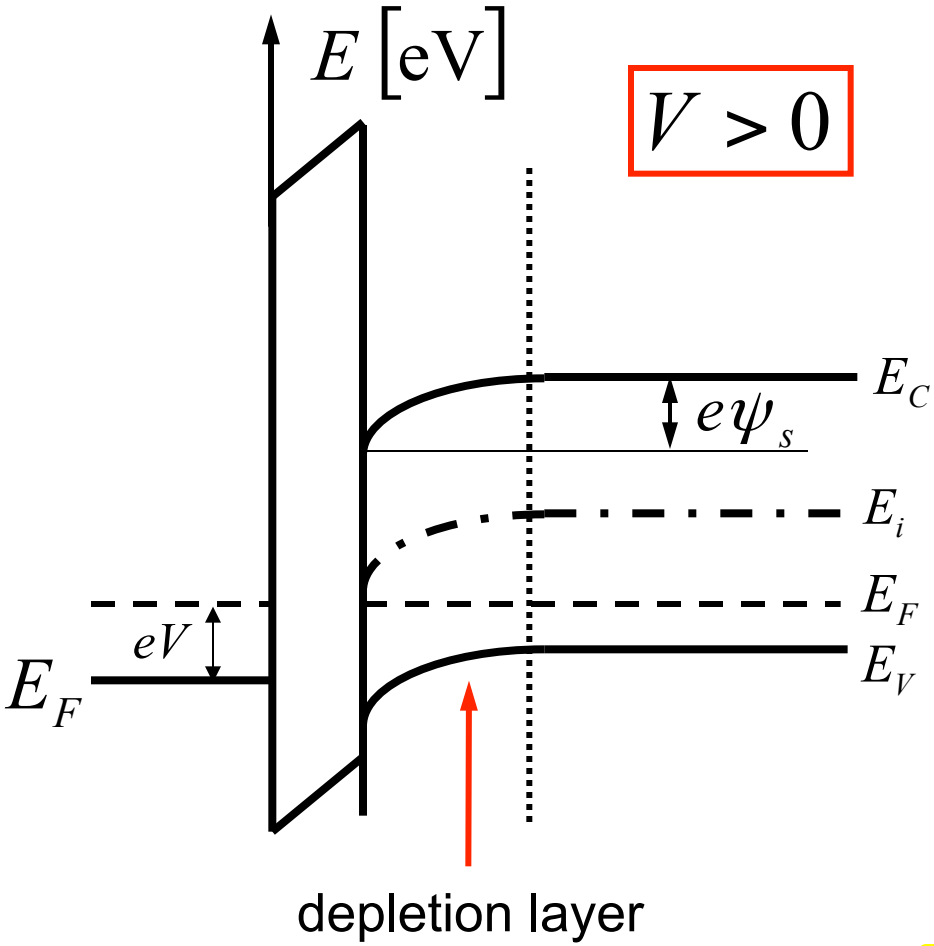
MOS Capacitor (Ideal) - Band Diagram, Beyond Threshold

Surface metallic

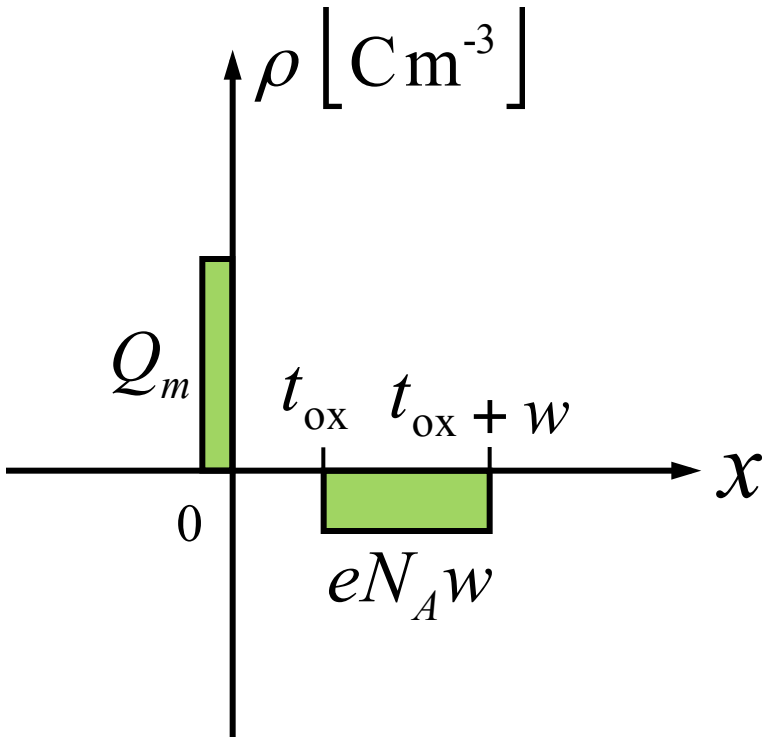


carrier depletion in ideal MOS diode

energy band diagram



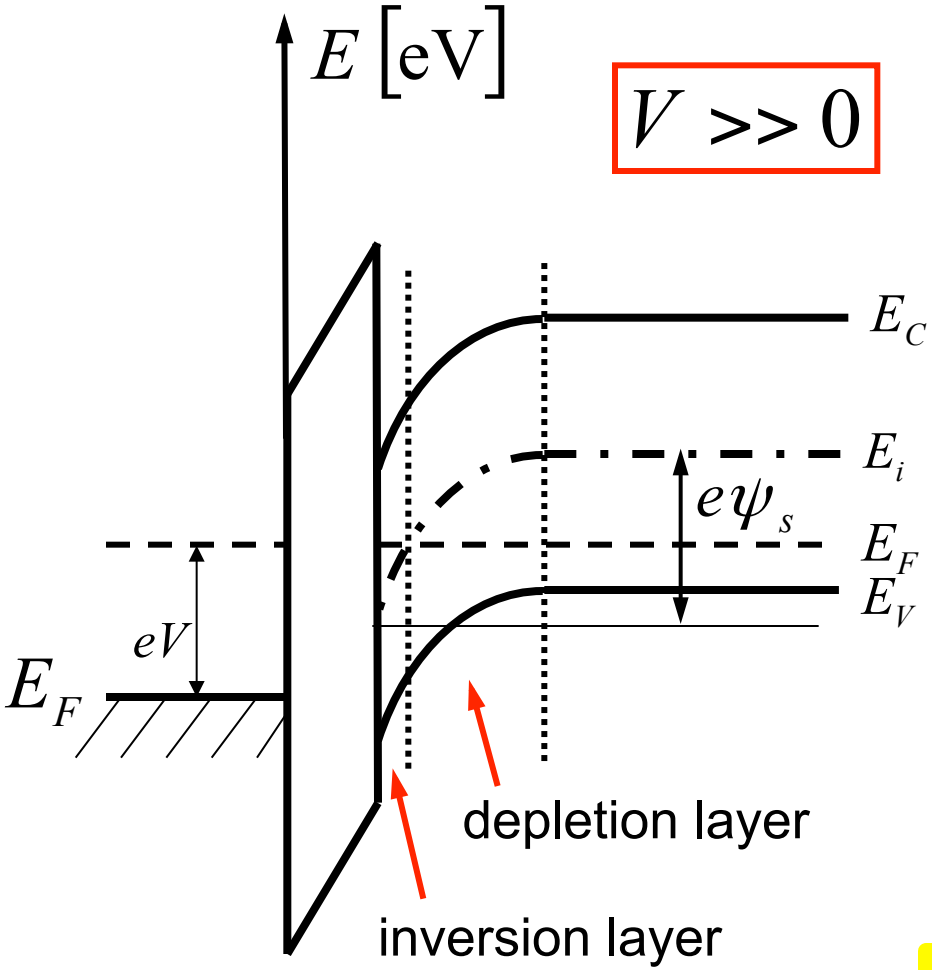
charge distribution



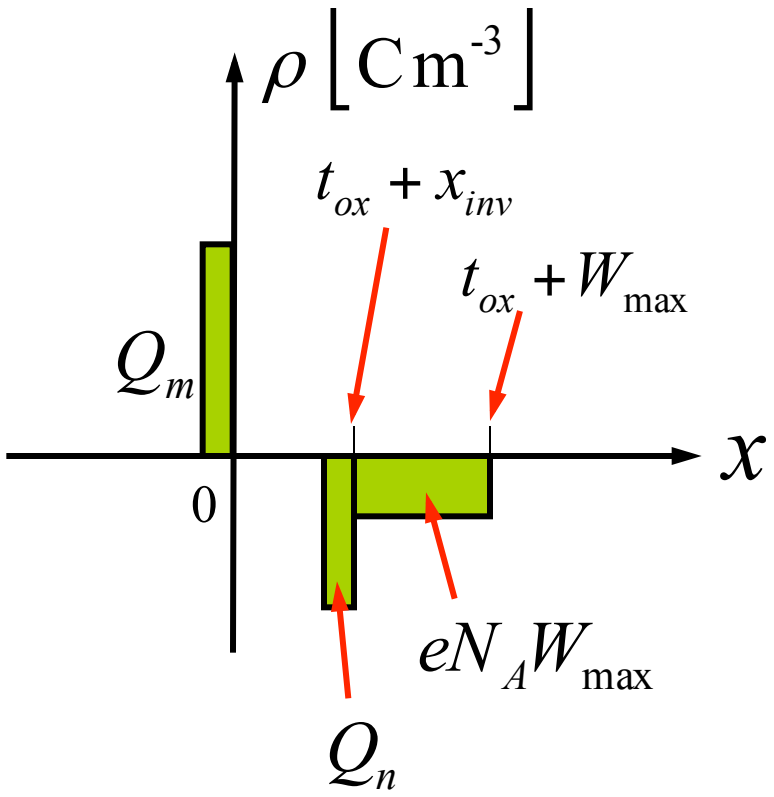
ψ_s Surface potential

Carrier inversion in ideal MOS diode

energy band diagram



charge distribution



ψ_s Surface potential

MOS Capacitor - Useful Equations

MOS capacitor voltage drops (ideal): $V_G = V_{OX} + \Psi_S$

These equations assume the MOS capacitor is in the extrinsic temperature region (e.g. around room temperature).

Depletion region width:

$$W = \sqrt{\frac{2\varepsilon_S}{qN_A}\Psi_S} \quad \text{P-type} \qquad W = \sqrt{\frac{2\varepsilon_S}{qN_D}\Psi_S} \quad \text{N-type}$$

Bulk potential:

$$\phi_B = \frac{E_i(bulk) - E_F}{q} = \frac{k_B T}{q}\ln\left(\frac{N_A}{n_i}\right) \quad \text{P-type}$$

$$\phi_B = \frac{E_i(bulk) - E_F}{q} = -\frac{k_B T}{q}\ln\left(\frac{N_D}{n_i}\right) \quad \text{N-type}$$

Definition of strong inversion (threshold): $\Psi_S = 2\phi_B$ (alternate definition: $\Psi_S = 2\phi_B + 6k_BT/q$)

Maximum depletion region width (occurs at threshold):

$$W_T = \sqrt{\frac{2\varepsilon_S}{qN_A}(2\phi_B)} \quad \text{P-type} \qquad W_T = \sqrt{\frac{2\varepsilon_S}{qN_D}(2\phi_B)} \quad \text{N-type}$$

Ideal MIS Structure

$$\varphi_{ms} \equiv \varphi_m - (\chi + E_g / 2q - \psi_B) = 0 \quad for \quad n-type$$

$$\varphi_{ms} \equiv \varphi_m - (\chi + E_g / 2q + \psi_B) = 0 \quad for \quad p-type$$

$$q\psi_B = E_i - E_F$$

Ψ_s given by substrate (uniform) doping

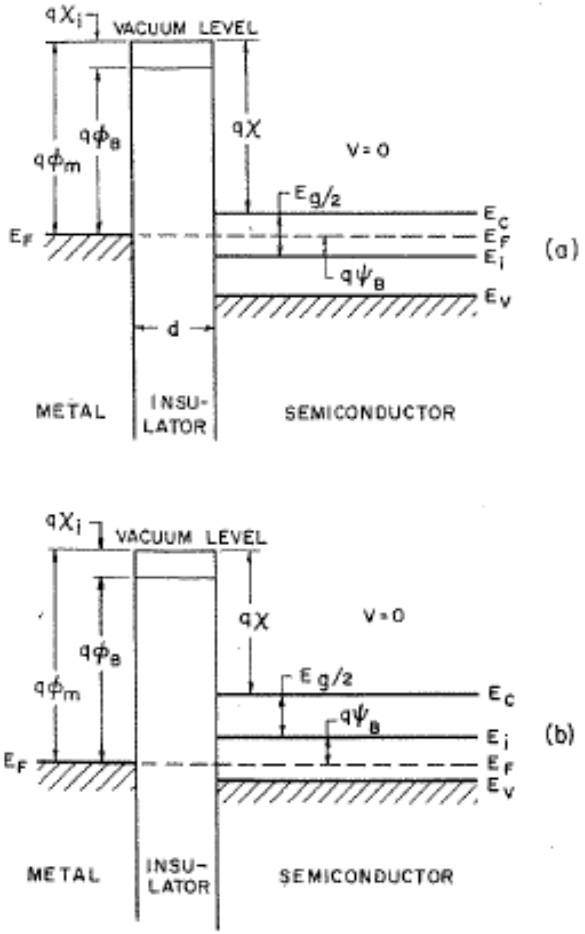


Fig. 2 Energy-band diagrams of ideal MIS diodes at V = 0. (a) n-type semiconductor. (b) p-type semiconductor.

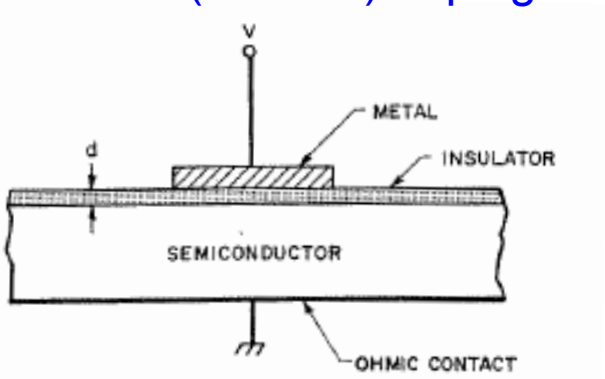


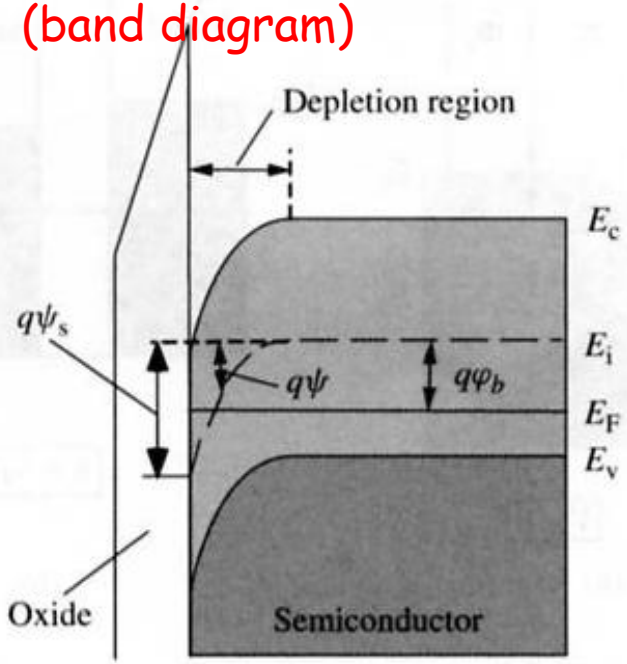
Fig. 1 Metal–insulator–semiconductor (MIS) diode.

•Surface potential Ψ_s determines the operation regimes.

$$\varphi_b = V_{th} \ln\left(\frac{N_a}{n_i}\right), \qquad (1.2)$$

Note: potential vs. energy
(voltage) (band diagram)

In band diagram:
positive potential
makes the band
energy level lower
at metal side.



$0 < \Psi_s < 2\varphi_b$
$\Rightarrow$ depletion and weak inversion
$\Psi_s = 2\varphi_b$
$\Rightarrow$ strong inversion
$\Psi_s < 0$
$\Rightarrow$ accumulation
$\Psi_s = 0$
$\Rightarrow$ flat band

Figure 1.4 Band diagram for MOS capacitor in weak inversion ($\varphi_b < \psi_s < 2\varphi_b$)

$$n_p = n_{po} \exp(q\psi/kT) = n_{po} \exp(\beta\psi)$$

$$p_p = p_{po} \exp(-q\psi/kT) = p_{po} \exp(-\beta\psi)$$

where n_{po} equilibrium minority carriers
where p_{po} equilibrium majority carriers
determined by the substrate doping

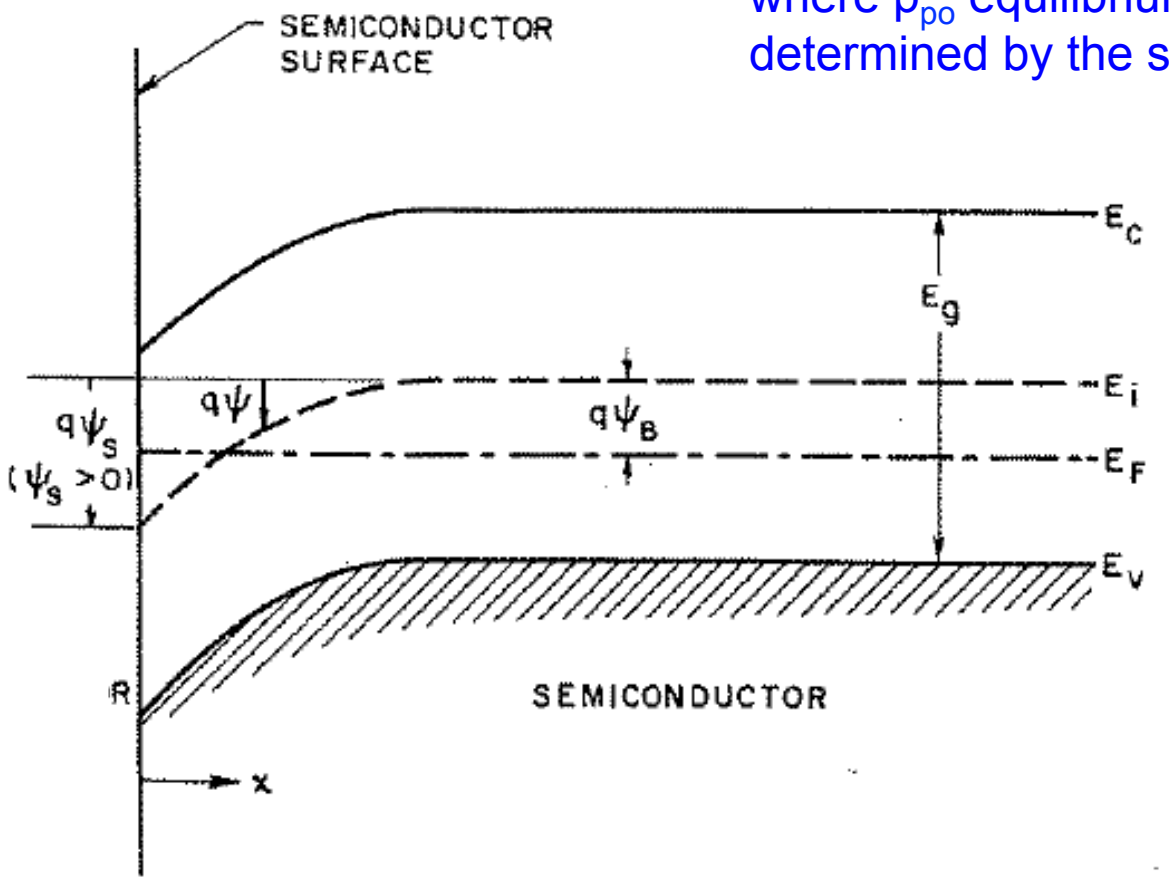


Fig. 4 Energy-band diagram at the surface of a *p*-type semiconductor. The potential ψ, defined as zero in the bulk, is measured with respect to the intrinsic Fermi level E_i. The surface potential ψ_s is positive as shown. (*a*) Accumulation occurs when $\psi_s < 0$. (*b*) Depletion occurs when $\psi_B > \psi_s > 0$. (*c*) Inversion occurs when $\psi_s > \psi_B$.

➢Potential Distribution: Poisson equation

At the surface:

$$p_s = N_a \exp(-\psi_s / V_{th})$$

$$n_s = \frac{n_i^2}{p_s} = n_{po} \exp(\psi_s / V_{th})$$

In the bulk :

$$p(x) = N_a \exp(-\psi(x)/V_{th})$$

$$n(x) = \frac{n_i^2}{p(x)} = n_{po} \exp(\psi(x)/V_{th})$$

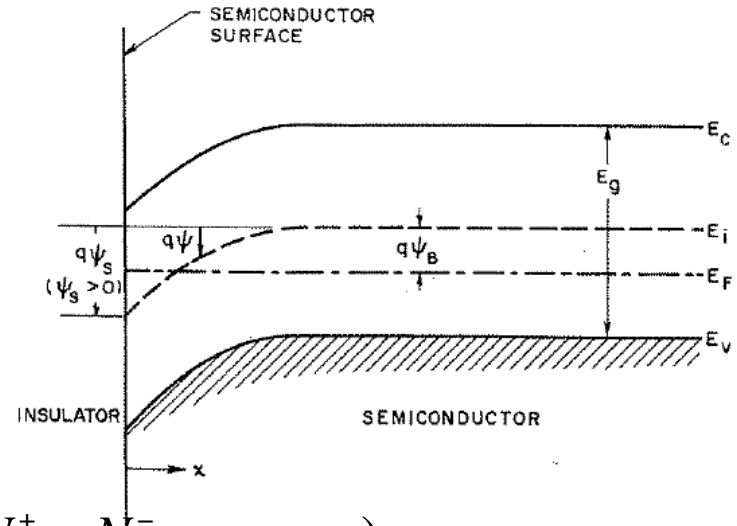
$\psi(x)$ also satisfies the Poisson's equation :

that is,

$$\frac{d^2\psi(x)}{dx^2} = -\frac{p(x) - n(x) - N_a^-}{\varepsilon_s}$$

where

$$\psi(\infty) = 0.$$



$$\beta = 1/kT = V_{th}$$

$$\frac{d^2\psi}{dx^2} = -\frac{\rho}{\varepsilon_s} = \frac{q(N_D^+ - N_A^- + p_p - n_p)}{\varepsilon_s}$$

Exact solution of Poisson equation for constant substrate doping

$$N_D^+ - N_A^- = n_{po} - p_{po}$$

$$p_p - n_p = p_{po}\exp(-\beta\psi) - n_{po}\exp(\beta\psi)$$

$$\frac{d^2\psi}{dx^2} = -\frac{q}{\varepsilon_s}[p_{po}(\exp(-\beta\psi) - 1) - n_{po}(\exp(\beta\psi) - 1)]$$

multiply both sides by 2dψ/dx

$$\int_0^{\partial\psi/\partial x}(\frac{\partial\psi}{\partial x})d(\frac{\partial\psi}{\partial x}) = -\frac{q}{\varepsilon_s}\int_0^{\psi}[p_{po}(\exp(-\beta\psi) - 1) - n_{po}(\exp(\beta\psi) - 1)]$$

$$E_s^2 = (\frac{2kT}{q})^2(\frac{qp_{po}\beta}{2\varepsilon_s})[(\exp(-\beta\psi_s) + \beta\psi_s - 1) + \frac{n_{po}}{p_{po}}(\exp(\beta\psi_s) - \beta\psi s - 1)]$$

Mathematical Addendum: Integration by substitution

$$2 \cdot \frac{d\psi}{dx} \cdot \frac{d^2\psi}{dx^2} = \frac{d}{dx}\left(\frac{d\psi}{dx}\right)^2$$

$$d\left(\frac{d\psi}{dx}\right)^2 = F(\psi) \cdot 2 \cdot \frac{d\psi}{dx}$$

$$\frac{d}{dx}\left(\frac{d\psi}{dx}\right)^2 = F(\psi) \cdot 2 \cdot d\psi$$

$$2 \cdot \frac{d\psi}{dx} d\left(\frac{d\psi}{dx}\right) = F(\psi) \cdot 2 \cdot d\psi$$

$$\frac{d\psi}{dx} d\left(\frac{d\psi}{dx}\right) = F(\psi) d\psi$$

$$\int_0^{d\psi/dx} \frac{d\psi}{dx} d\left(\frac{d\psi}{dx}\right) = \int_0^{\psi} F(\psi) d\psi$$

$$L_D = \sqrt{\frac{\varepsilon_s}{q p_{po} \beta}}$$

Debye length for holes (p-type substrate

$$F(\beta\psi, \frac{n_{po}}{p_{po}}) = [(\exp(-\beta\psi) + \beta\psi - 1) + \frac{n_{po}}{p_{po}}(\exp(\beta\psi) - \beta\psi - 1)]^{1/2}$$

$$for \quad \psi = \psi_s$$

Surface potential

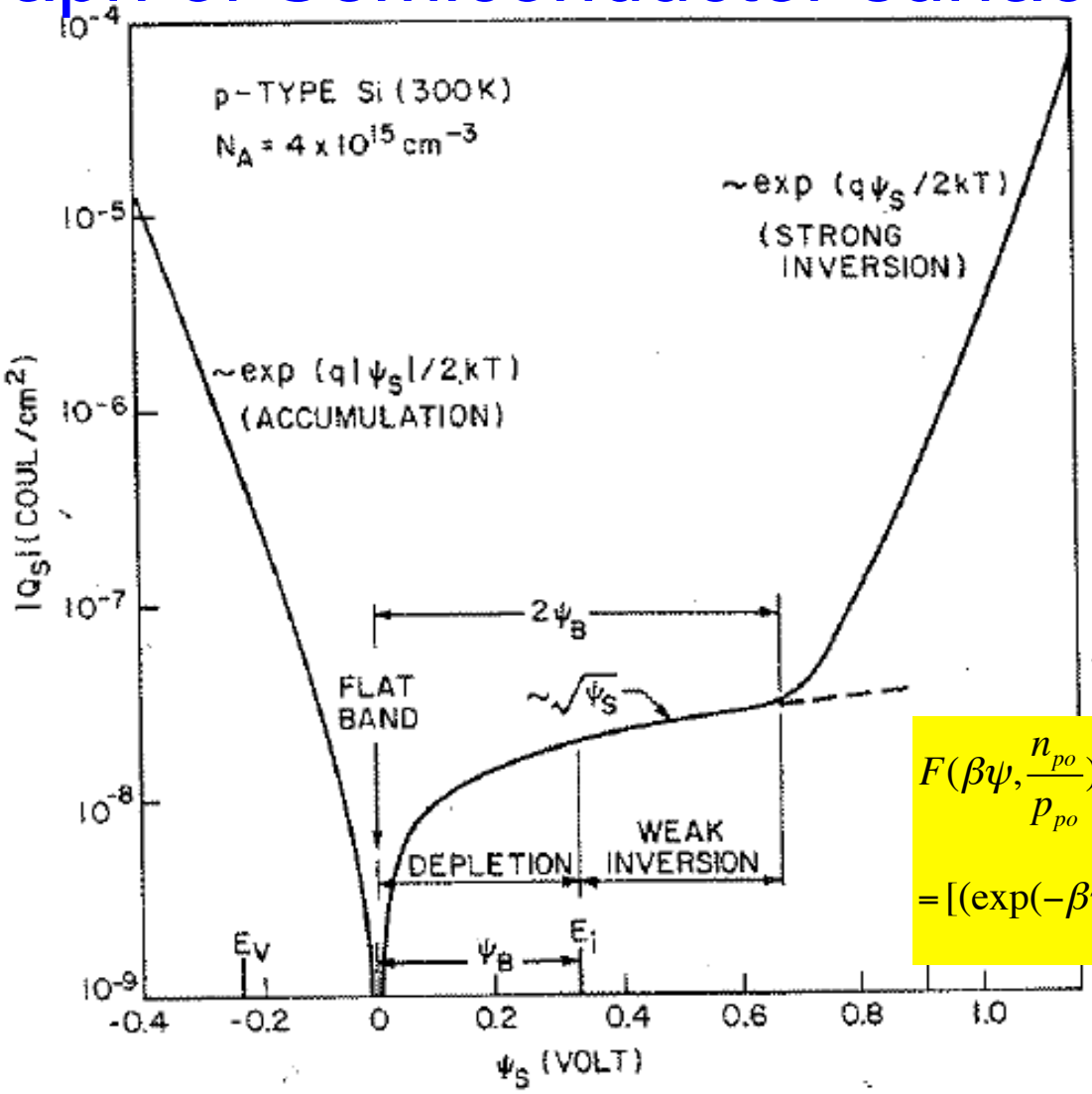
$$E_s = \pm \frac{\sqrt{2}}{\beta L_D} F(\beta\psi_s, \frac{n_{po}}{p_{po}})$$

Important equation; it relates the surface potential ψ_s to the surface field E_s.

$$Q_s = -\varepsilon_s E_s = \pm \frac{\varepsilon_s \sqrt{2}}{\beta L_D} F(\beta\psi_s, \frac{n_{po}}{p_{po}})$$

From the surface field E_s we can calculate the surface charge Q_s in the semiconductor.

Graph of Semiconductor surface charge Q_s.

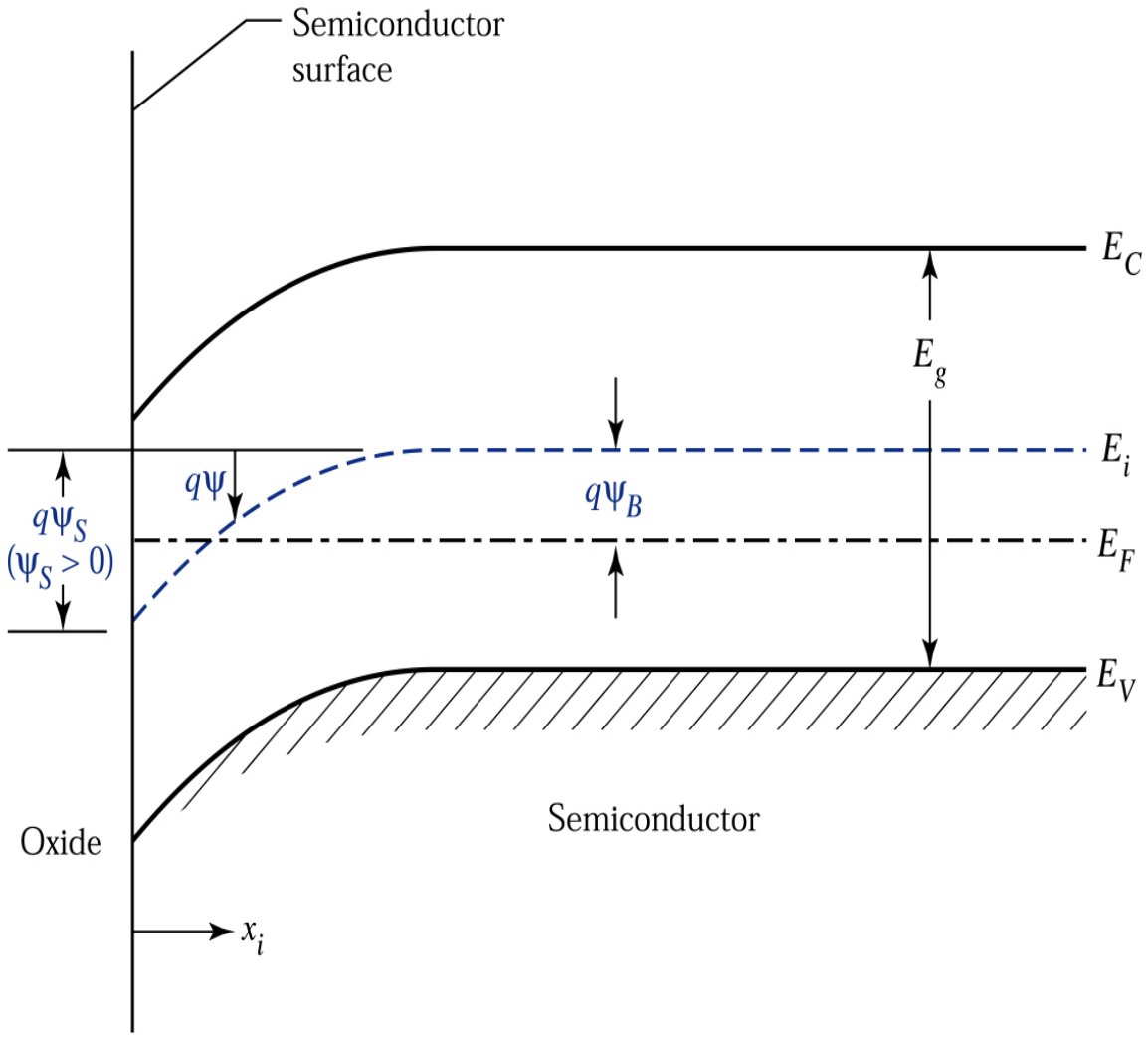


$$F(\beta\psi, \frac{n_{po}}{p_{po}}) =$$

$$= [(\exp(-\beta\psi) + \beta\psi - 1) + \frac{n_{po}}{p_{po}}(\exp(\beta\psi) - \beta\psi - 1)]^{1/2}$$

Fig. 5 Variation of space-charge density in the semiconductor as a function of the surface potential ψ_s for a *p*-type silicon with $N_A = 4 \times 10^{15}\ cm^{-3}$ at room temperature; ψ_B is the potential difference between the Fermi level and the intrinsic level of the bulk semiconductor. (After Garrett and Brattain, Ref. 13.)

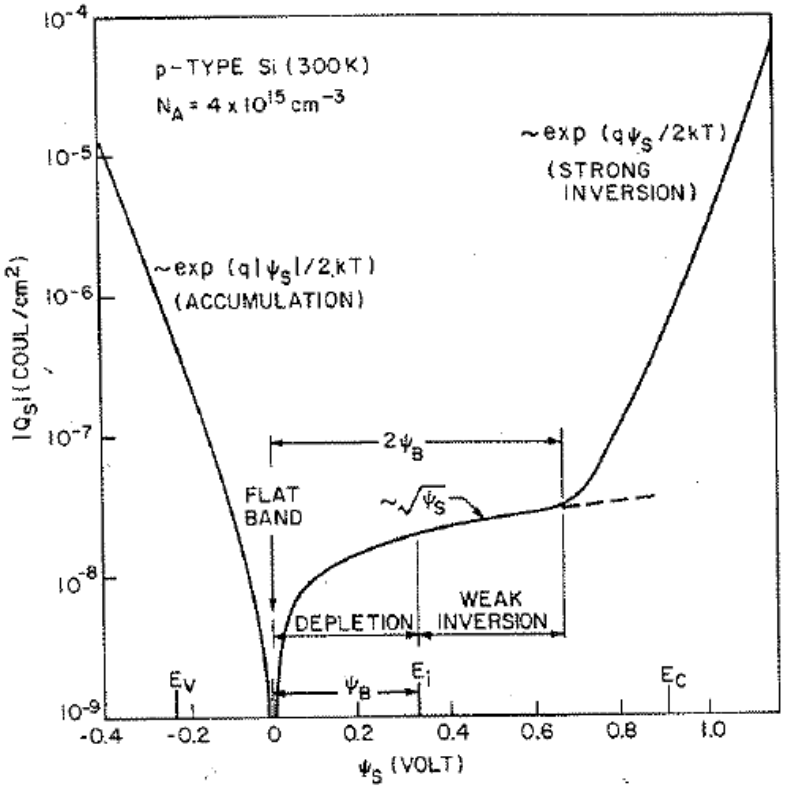
strong inversion condition



surface potential required for strong inversion is:

$$\psi_S(\text{inv}) \cong 2\psi_B = \frac{2kT}{e}\ln\left(\frac{N_A}{n_i}\right)$$

strong inversion is defined as conditions under which the potential E_{i} is as much below E_{F} as it is above E_{F} in the bulk



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$$\psi_s(inv) \cong 2\psi_B = \frac{2kT}{q}\ln\left(\frac{N_A}{n_i}\right)$$

Differential capacitance of the semiconductor layer

$$C_D \equiv \frac{\partial Q_s}{\partial \psi_s} = \frac{\varepsilon_s}{L_D\sqrt{2}} \frac{[1-(\exp(-\beta\psi_s) + \frac{n_{po}}{p_{po}}(\exp(\beta\psi_s)-1)]}{F(\beta\psi_s, \frac{n_{po}}{p_{po}})}$$

$flat-band$

$for \quad \psi_s = 0$

$$C_D(flat-band) = \varepsilon_s / L_D$$

another interpretation of Debye length

Summary of the analysisso far:

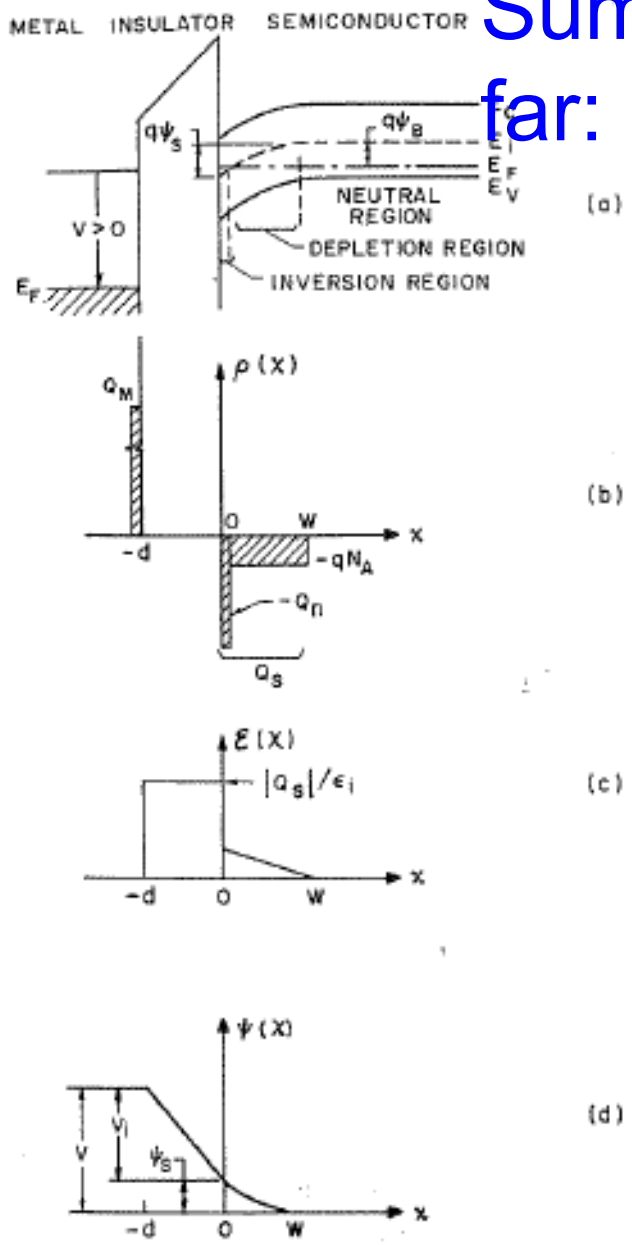


Fig. 6 (a) Band diagram of an ideal MIS diode. (b) Charge distribution under inversion condition. (c) Electric field distribution. (d) Potential distribution.

metal semiconductor

$$Q_M = Q_n + qN_A W = Q_s$$

electric field in dielectric — electric surface field in semiconductor

$$\varepsilon_i E_i = \varepsilon_s E_s$$

total applied voltage — voltage drop across dielectric + band bending in semiconductor

$$V = V_i + \psi_s$$

$$V_i = E_i \cdot d = \frac{|Q_s| \cdot d}{\varepsilon_i} \left(\equiv \frac{|Q_s|}{C_i}\right)$$

$$C_i = \frac{\varepsilon_i}{d}$$

Threshold Voltage

$$V = V_i + \psi_s$$

$$Q_M = Q_n + qN_A W = Q_s$$

$$\varepsilon_i E_i = \varepsilon_s E_s$$

$$V_i = E_i \cdot d = \frac{|Q_s| \cdot d}{\varepsilon_i} \left(\equiv \frac{|Q_s|}{C_i}\right)$$

$$V_G = \psi_s + \frac{|Q_s|}{C_i} = \psi_s + \frac{|Q_s(\psi_s)|}{C_i}$$

$$V_T \quad when \quad \psi_s = 2\psi_B$$

$$V_T = \frac{|Q_s(2\psi_B)|}{C_i} + 2\psi_B$$

Threshold Voltage defined as the voltage at which the band bending in semiconductor is equal to 2 ψ_B.

* As $V_G = V_T \rightarrow \Psi_s = 2\Psi_b$

Which V_T is called as the threshold voltage.

* The equivalent electric field at the interface becomes $E_s = -Q_s/\varepsilon_s = \sqrt{(4qN_a\Psi_B/\varepsilon_s)}$

Threshold Voltage for $V_{FB} \neq 0$

Since electric field flux continuity at the interface

$$\varepsilon_s E_s = \varepsilon_i E_i$$

Assume the insulator causes a voltage drop $E_i d_i$,

where d_i is the thickness of the dielectric layer;

$$\Rightarrow \quad (V_{GB} - E_i d_i - V_{FB}) = \Psi_s$$

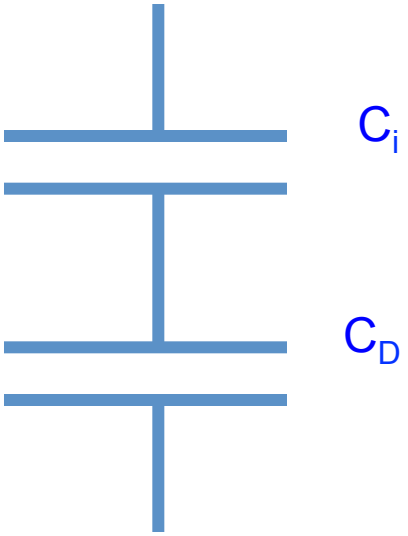
$$\Rightarrow \quad V_{GB} = V_{FB} + \Psi_s + (\varepsilon_s E_s)/C_{ox}$$

Where C_{ox} is the insulator capacitance per unit area and

$$Q_s = - \varepsilon_s E_s$$

Total capacitance of MOS diode

a series combination of the oxide capacitance and the semiconductor depletion-layer capacitance



$$C = \frac{C_i C_D}{(C_i + C_D)}$$

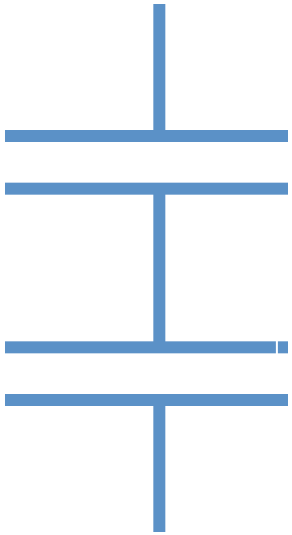
$$C_i = \frac{\varepsilon_0 \varepsilon_{ox}}{t_{ox}}$$

$$C_D = \frac{\varepsilon_0 \varepsilon_s}{W}$$

$$\psi_s = \frac{eN_A W^2}{2\varepsilon_0 \varepsilon_S}$$

$$\frac{C}{C_i} = \frac{1}{1 + \sqrt{\frac{2\varepsilon_0 \varepsilon_{ox}^2 \psi_s}{eN_A \varepsilon_s t_{ox}^2}}}$$

Total capacitance as a function of voltage



$$C = \frac{C_i C_D}{C_i + C_D}$$

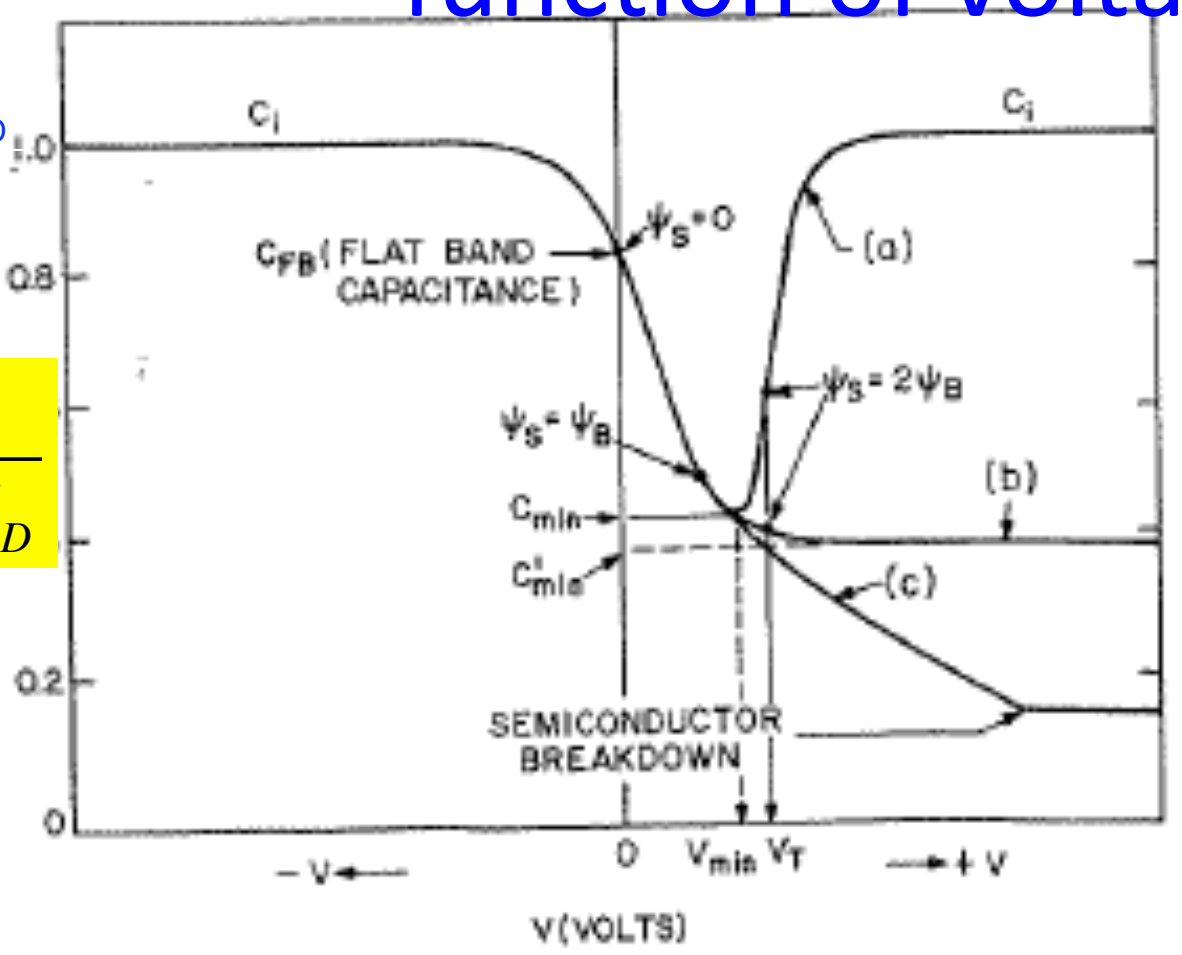


Fig. 7 MIS capacitance–voltage curves. (a) Low frequency. (b) High frequency. (c) Deep depletion. (After Grove et al., Ref. 16.)

$$C_{FB}(\psi_s = 0) = \frac{\varepsilon_i}{d + (\varepsilon_i / \varepsilon_s) L_D}$$

High frequency and deep depletion curves

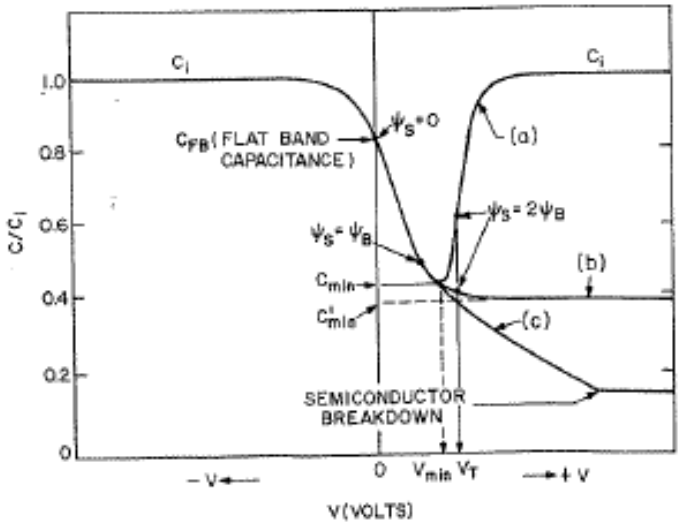


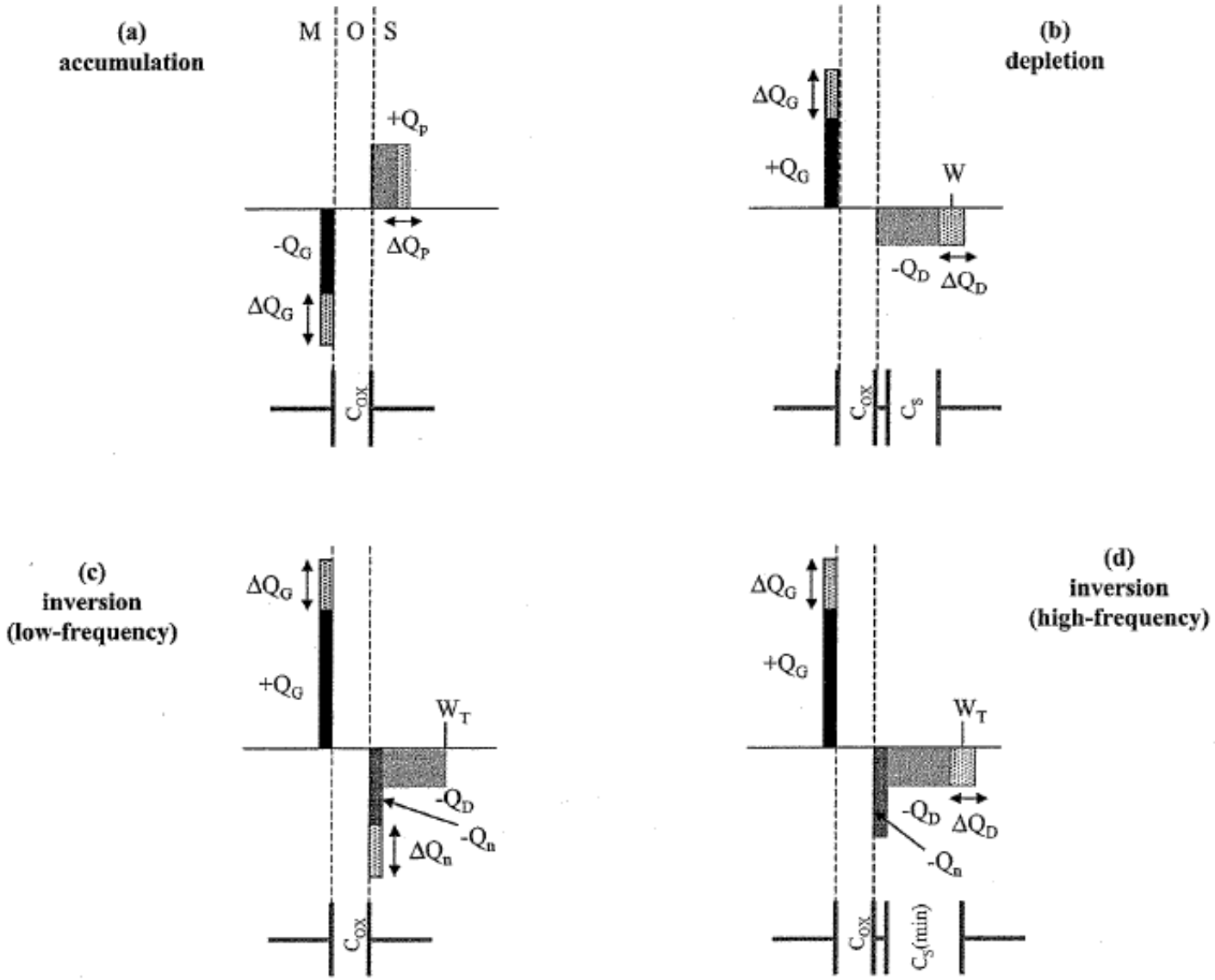
Fig. 7 MIS capacitance–voltage curves. (a) Low frequency. (b) High frequency. (c) Deep depletion. (After Grove et al., Ref. 16.)

Normal curve - increase of C past V_T depends on the electron ability to follow the applied signal. Happens only at low enough frequency (5-100 Hz) when recombination-generation rates can keep up with the signal variations.

At high frequency the recombination-generation rates are too slow to change the carriers.

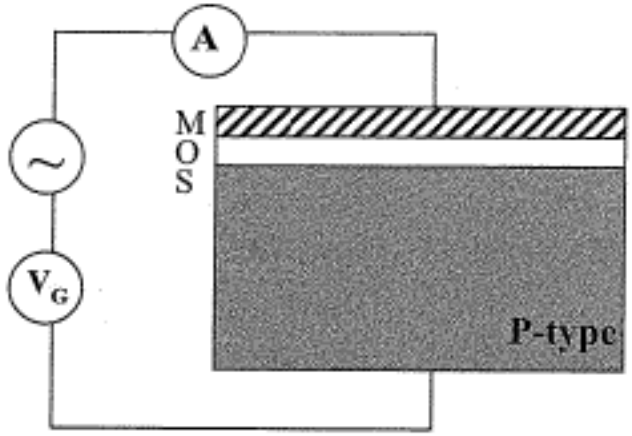
Deep depletion happens under pulse condition.
One applies a large voltage abruptly such that there is no enough time for the inversion channel to form due to the thermal generation.

MOS Capacitor - Qualitative Description of the C-V (cont.)

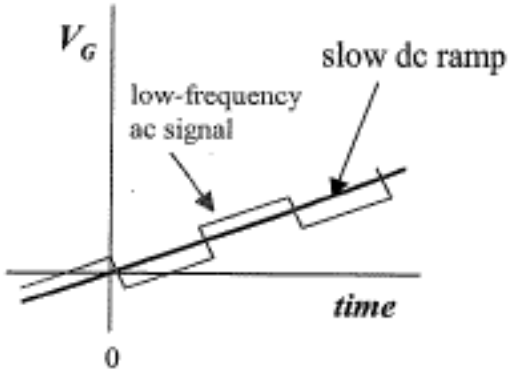


MOS Capacitor (Ideal) - AC Behavior & The C-V Curve

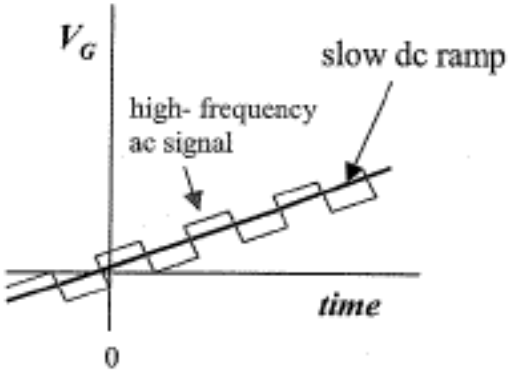
The C-V Test:



$$C = \frac{dQ}{dV}$$

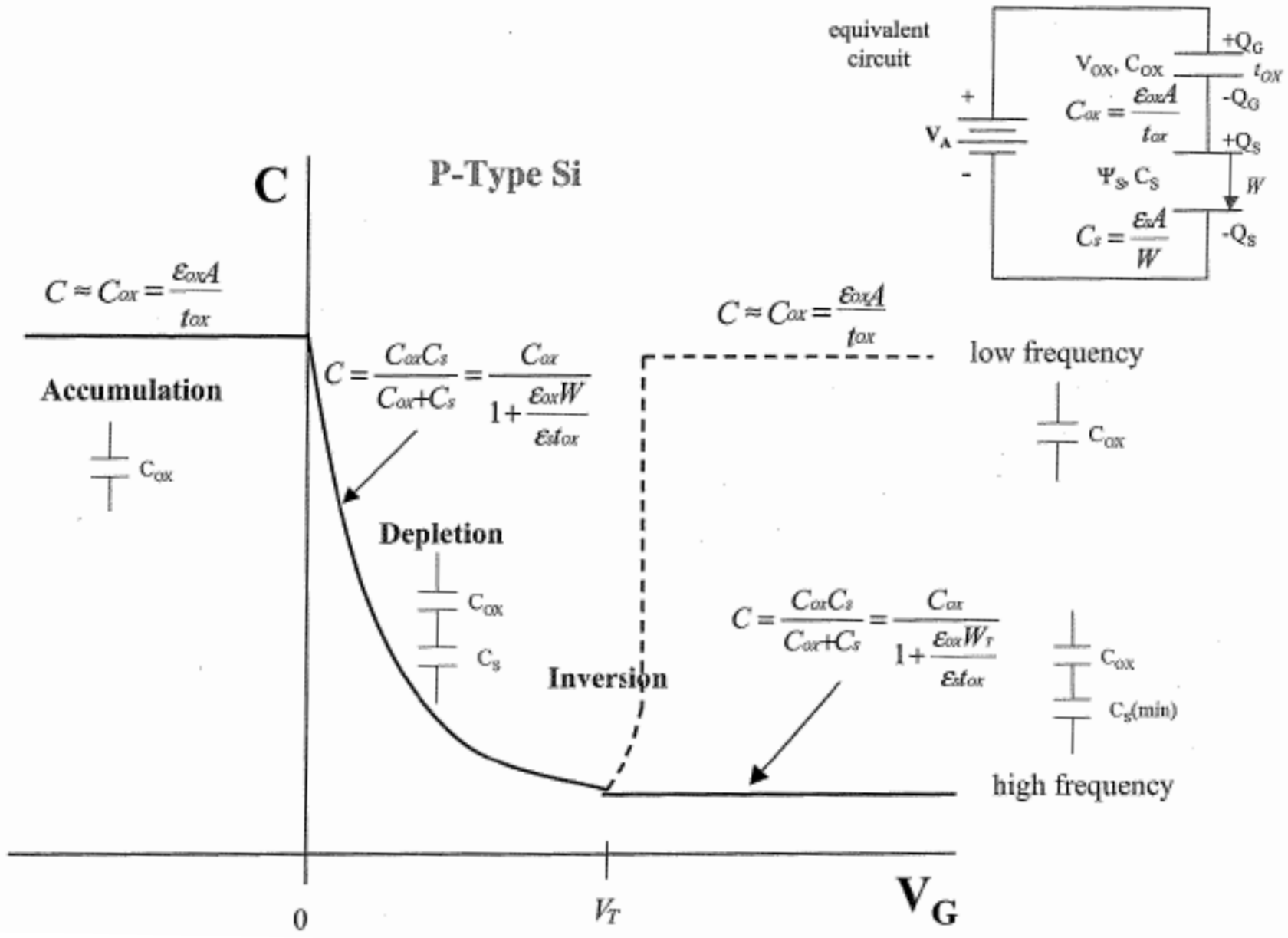


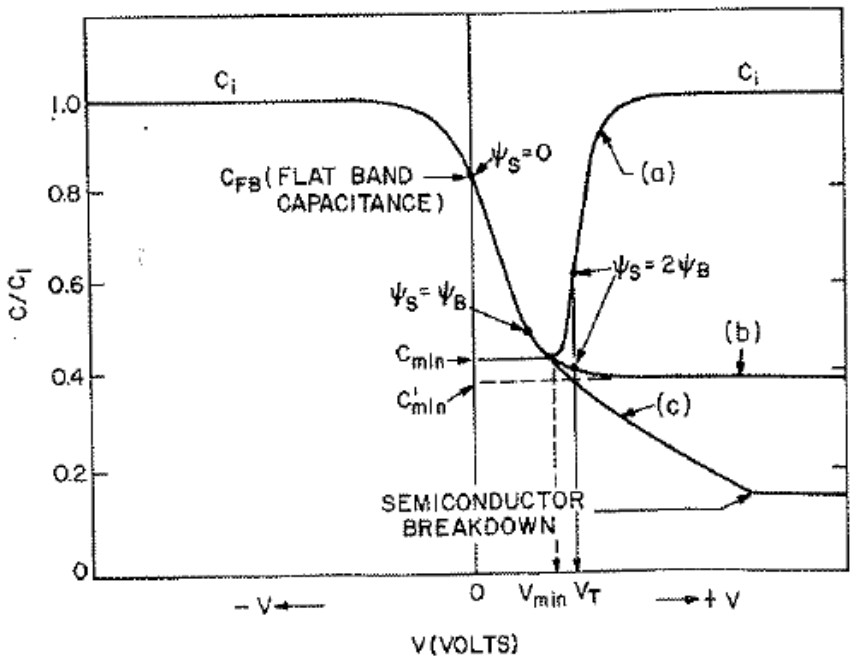
Low-Frequency Test



High-Frequency Test

MOS Capacitor (Ideal) - The C-V Characteristic





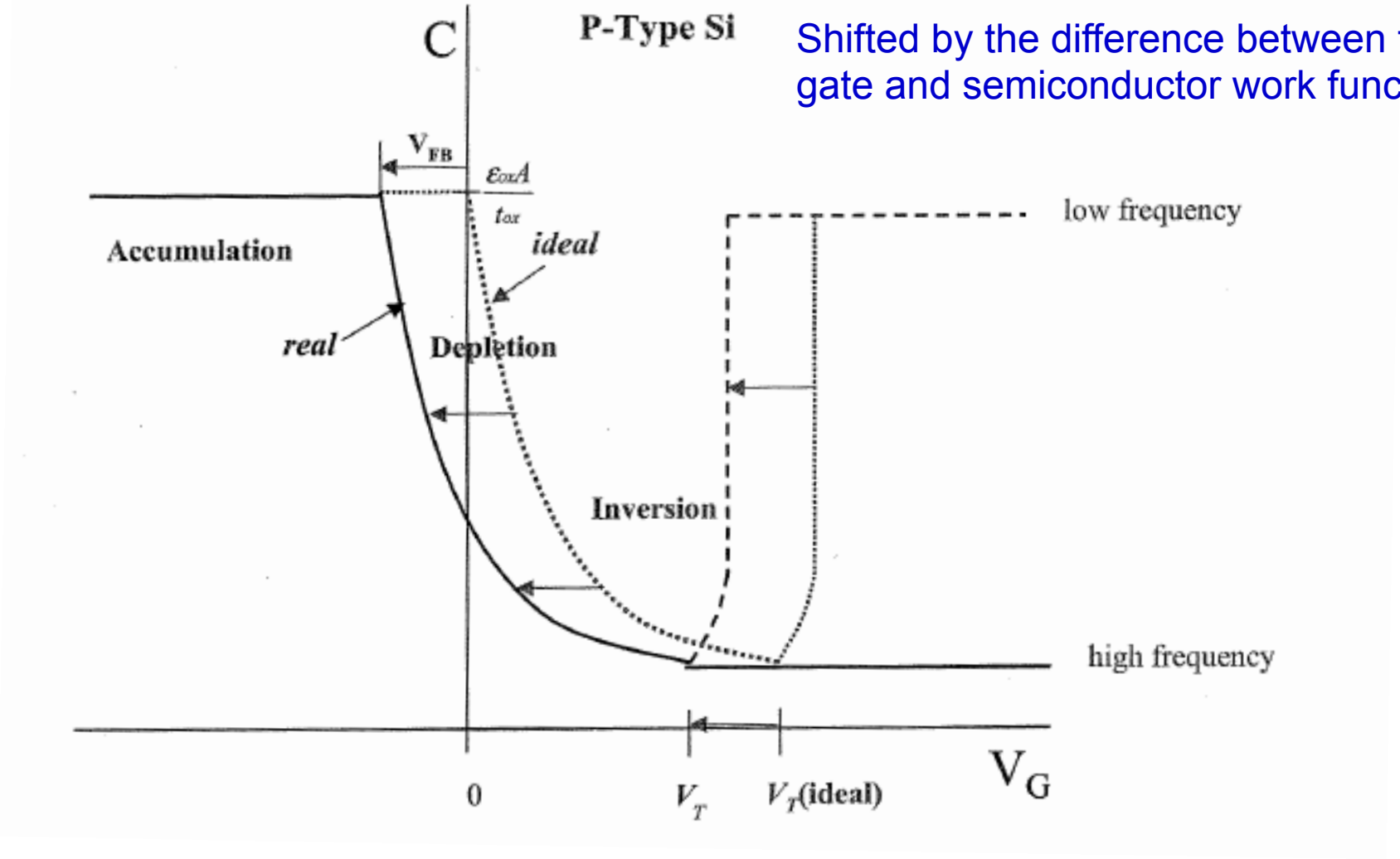
$$C'_{\min} = \frac{\varepsilon_i}{d + (\varepsilon_i / \varepsilon_s) W_{\max}}$$

$$C_{FB}(\psi_s = 0) = \frac{C_i \times C_D}{C_i \times C_D} = \frac{\dfrac{\varepsilon_i}{d} \times \dfrac{\varepsilon_d}{L_D}}{\dfrac{\varepsilon_i}{d} + \dfrac{\varepsilon_d}{L_D}} = \frac{\varepsilon_i}{d + (\varepsilon_i / \varepsilon_s) L_D}$$

$$W_{\max} = \sqrt{\frac{2\varepsilon_s \psi_s (inv)}{\varepsilon_s N_A}} = \sqrt{\frac{4kT\varepsilon_s \ln(N_A / n_i)}{q^2 N_A}}$$

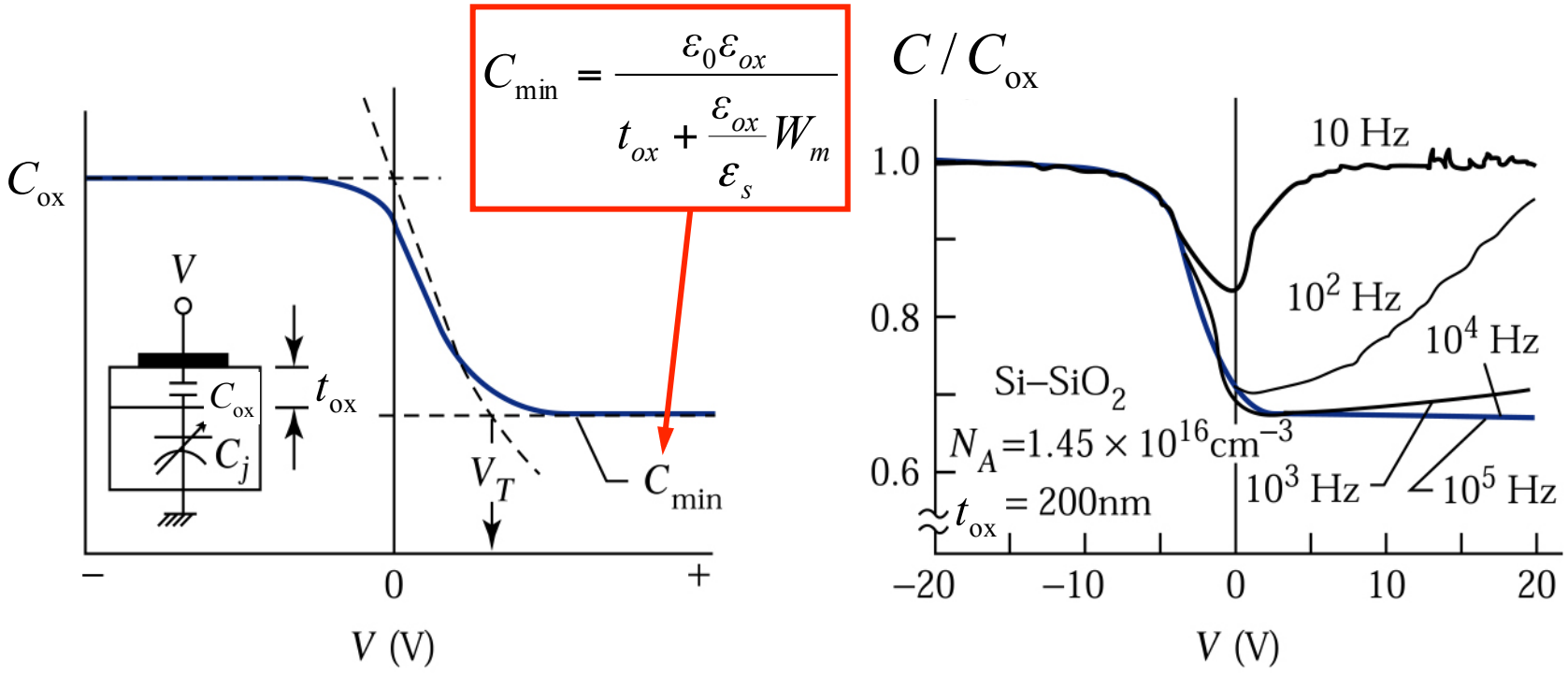
$$V_T(inv) = V_i + \psi_s = \frac{Q_s}{C_i} + 2\psi_B = \frac{\sqrt{4\varepsilon_s \psi_B N_A}}{C_i} + 2\psi_B$$

Real MOS Capacitor - C-V Characteristic Revisited



Shifted by the difference between the gate and semiconductor work functions

MOS diode capacitance realistic measurements



Possibility to determine the thermal generation rate of carriers in a semiconductor.

MOS diode capacitance - comment on deep depletion

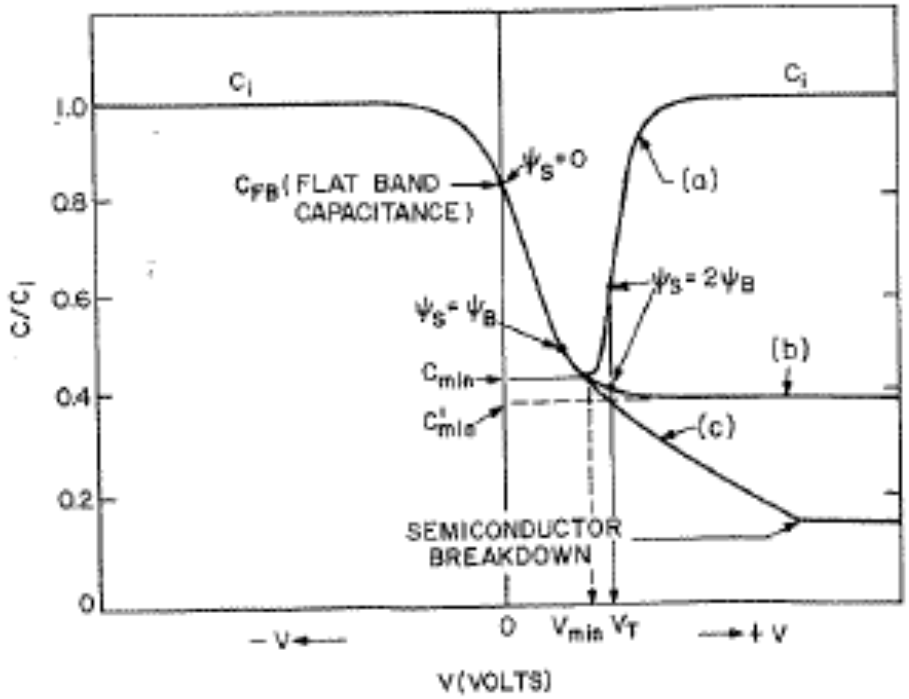


Fig. 7 MIS capacitance–voltage curves. (*a*) Low frequency. (*b*) High frequency. (*c*) Deep depletion. (After Grove et al., Ref. 16.)

When V_G and the small-signal measuring voltage vary at a faster rate that can be accommodated by G-R in the surface depletion region (see curve (c) in the Fig.7, the silicon goes into "deep depletion". Since inversion layer cannot form, the depletion region becomes wider than W_{max}. The generation of carriers increases as the depletion layer widens, and so the deep depletion curve is frequently observed to relax to the high frequency curve at higher biases.

threshold voltage

$$W_m \cong \sqrt{\frac{2\varepsilon_{ox}\varepsilon_S(2\psi_B)}{eN_A}} \qquad V = V_{\text{ox}} + \psi_s \qquad \psi_S(\text{inv}) \cong 2\psi_B$$

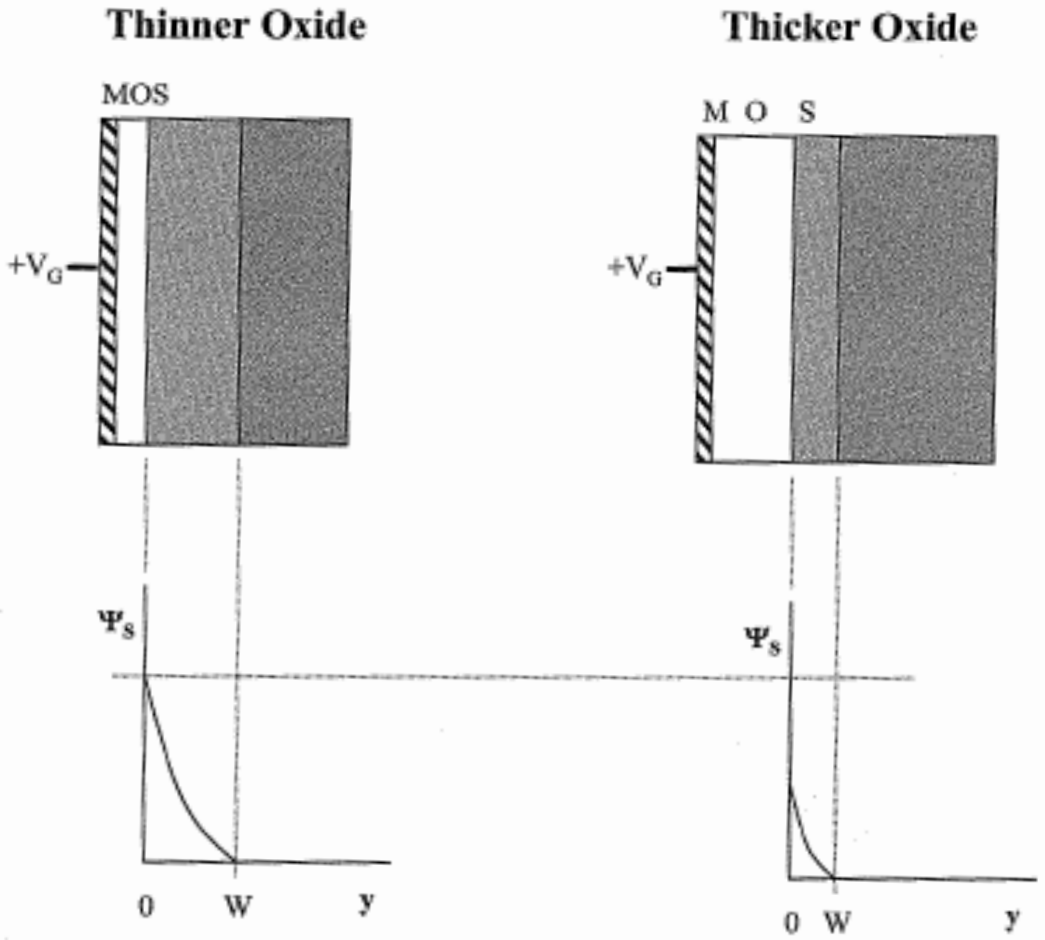
$$V_{th} = \frac{eN_A W_m}{C_{ox}} + \psi_S(\text{inv})$$

$$V_{th} \cong \frac{\sqrt{2\varepsilon_0\varepsilon_S eN_A(2\psi_B)}}{C_{ox}} + 2\psi_B$$

when strong inversion occurs, the width of the depletion region will not increase with a further increase in applied voltage – this condition takes place at the threshold voltage, when $\psi_S = \psi_S(\text{inv})$

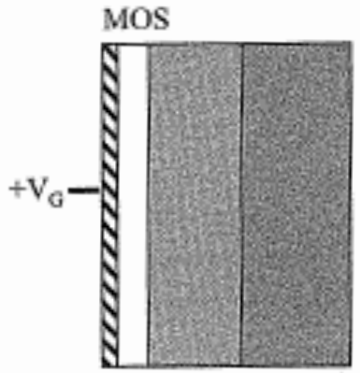
MOS Capacitor - Surface Potential & Gate Ox Thickness

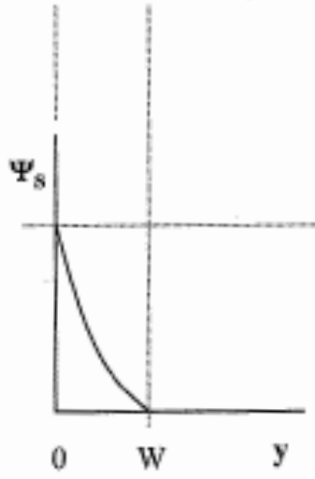
$$V_G = V_{OX} + \Psi_S$$



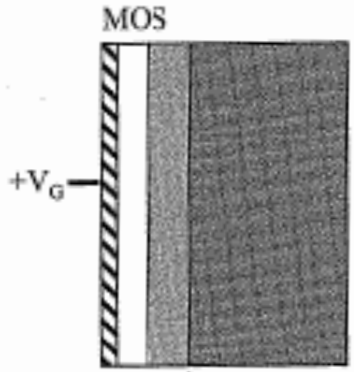
MOS Capacitor - Surface Potential & Doping

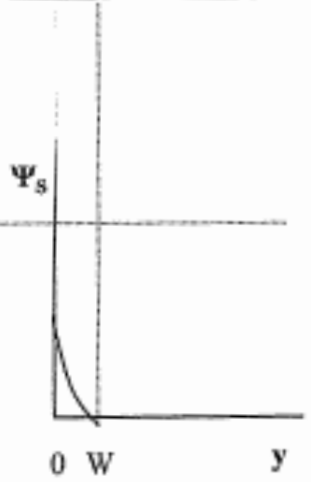
Lighter Doping





Heavier Doping





$$V_G = V_{ox} + \Psi_S$$

$$Q_G = -Q_D$$

$$Q_D = qAN_AW$$

MOS Capacitor (Ideal) - Threshold Voltage Calculation

Threshold Voltage

P-Type MOS Capacitor

$$V_T = 2|\phi_B| + \frac{\sqrt{2\varepsilon_S q N_A |2\phi_B|}}{C'_{OX}}$$

where $\phi_B = \frac{k_B T}{q} \ln\left(\frac{p}{n_i}\right)$

$p \approx N_A$ for extrinsic temperature region (e.g. room temp.)

$$C'_{OX} = \frac{\varepsilon_{OX}}{t_{OX}}$$ (gate capacitance per unit area)

N-Type MOS Capacitor

$$V_T = 2|\phi_B| - \frac{\sqrt{2\varepsilon_S q N_D |2\phi_B|}}{C'_{OX}}$$

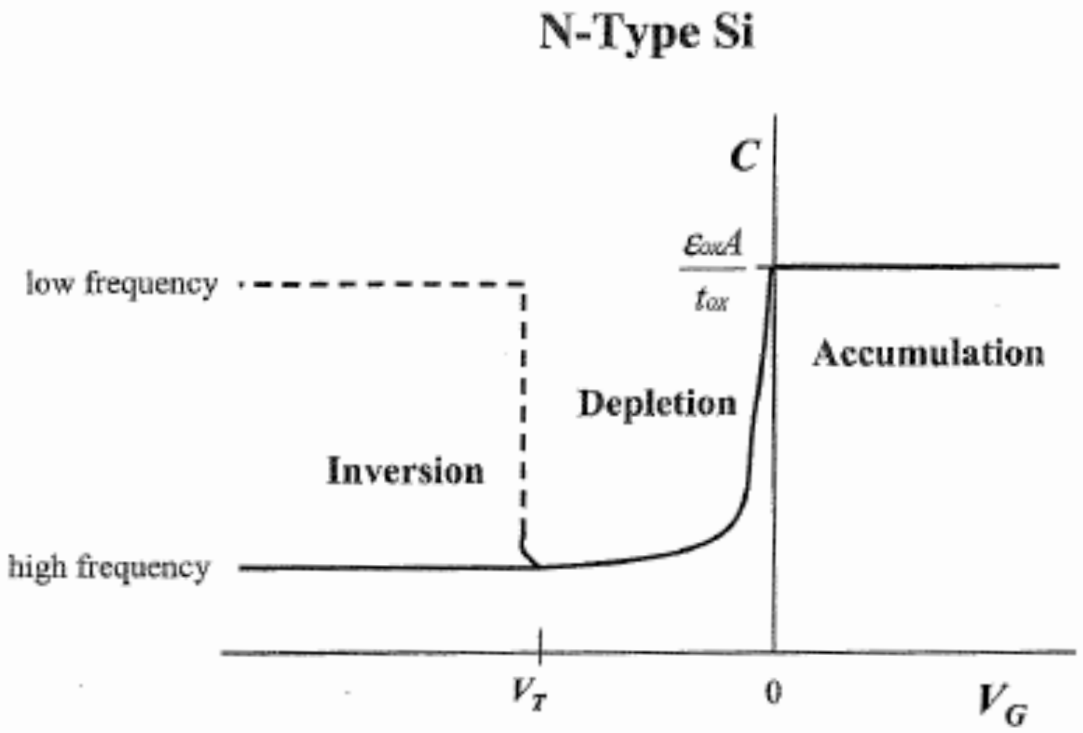
where $\phi_B = \frac{k_B T}{q} \ln\left(\frac{n}{n_i}\right)$

$n \approx N_D$ for extrinsic temperature region (e.g. room temp.)

$$C'_{OX} = \frac{\varepsilon_{OX}}{t_{OX}}$$ (gate capacitance per unit area)

The MOS capacitor for the n-type Si is analogous to p-type Si

MOS Capacitor - *N-Type* Si at a Glance (cont.)

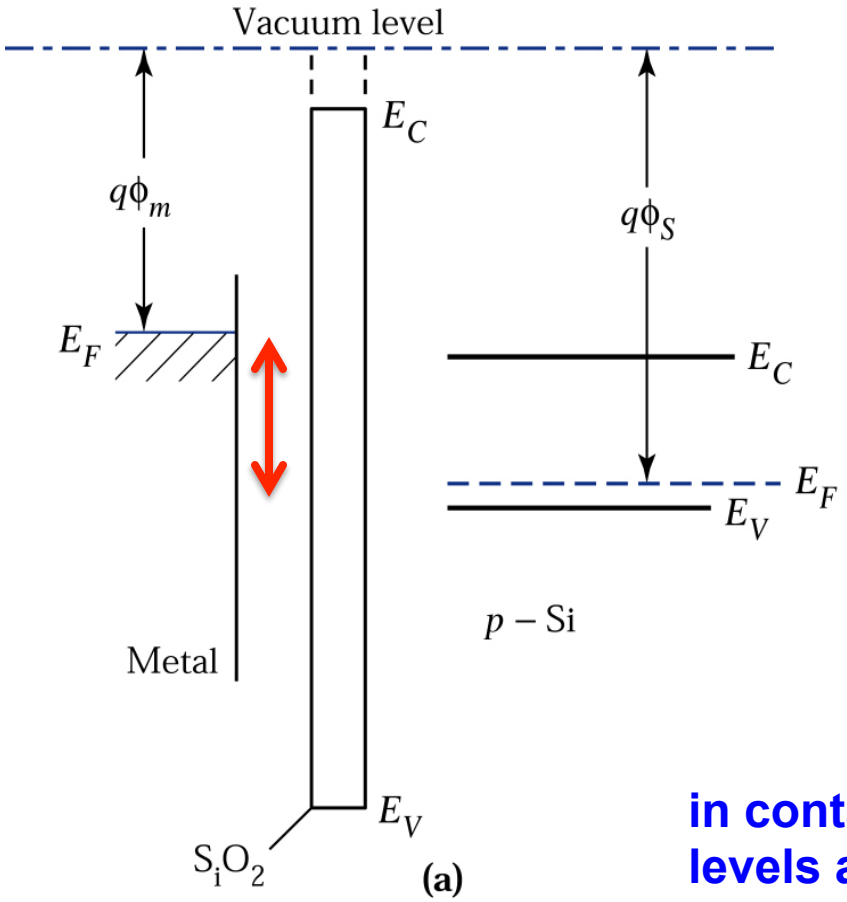


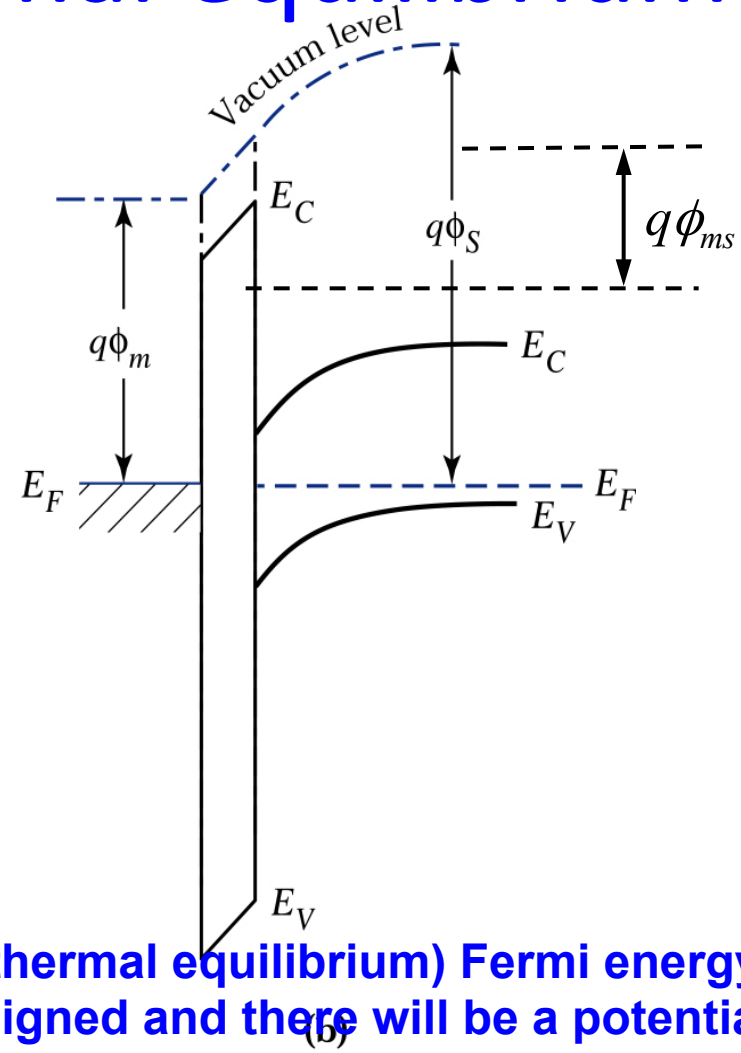
Real SiO_2-Si MOS diode

in real MOS diode:

- the work function difference is nonzero
- there exist build-in charges in the gate oxide

MOS diode in thermal equilibrium

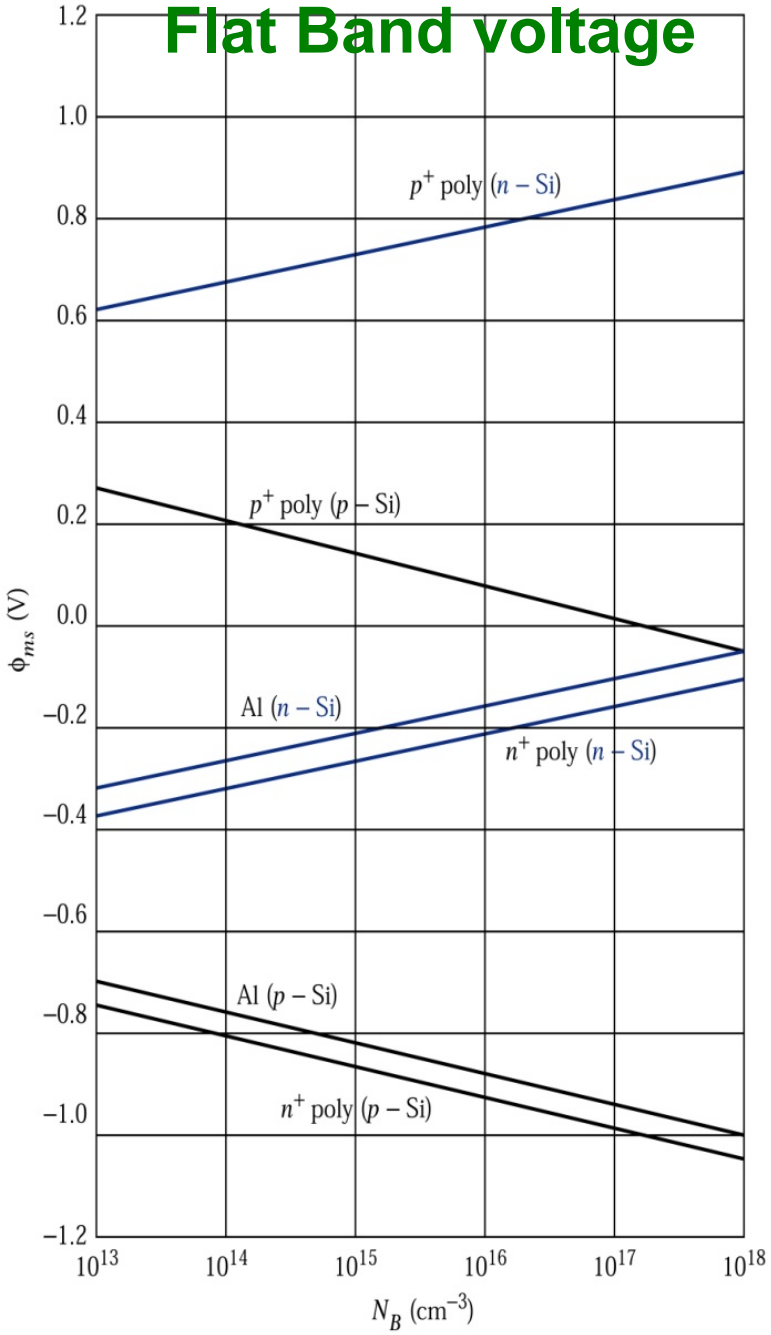




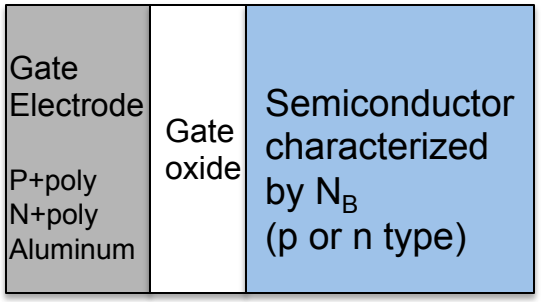
When separated

in contact (thermal equilibrium) Fermi energy levels are aligned and there will be a potential drop across dielectric and band bending in semiconductor; a certain voltage on the gate is needed to make the energy bending vanish
→ Flat Band Voltage

Flat Band voltage



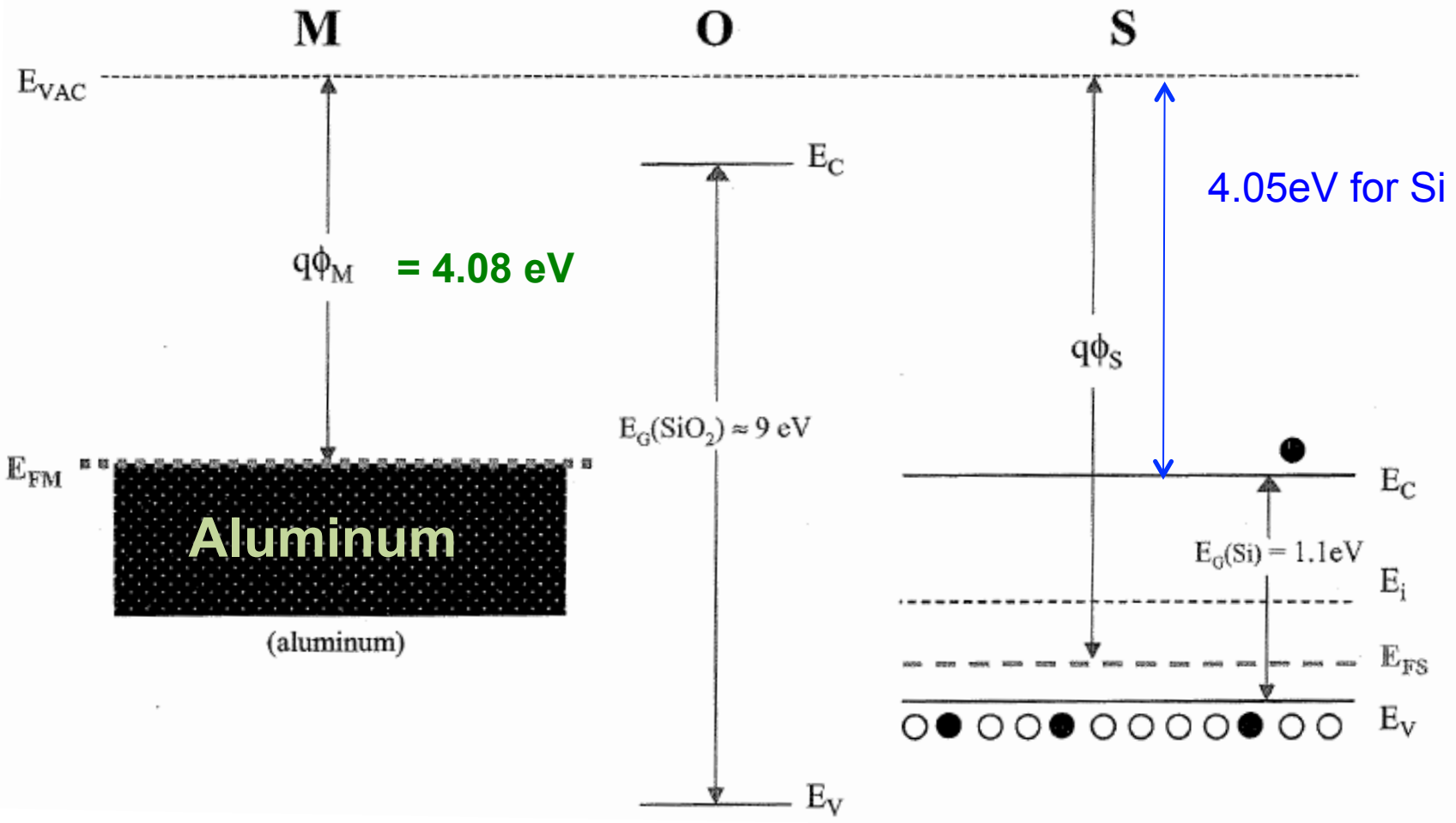
work function difference vs. impurity concentration for poly-silicon and Al gate



Combination of Al, p+ poly, n+ poly gate electrodes with n-type and p-type substrates

Real MOS Capacitor - Band Diagram, Isolated Materials

For a *real* (non-ideal) MOS capacitor, $\phi_M < \phi_S$



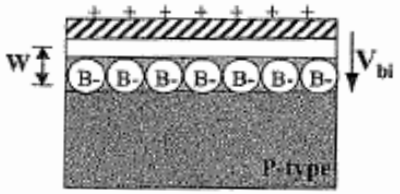
Gate electrode
work function engineering

Element	Work Function(eV)
Aluminum	4.08
Beryllium	5.0
Cadmium	4.07
Calcium	2.9
Carbon	4.81
Cesium	2.1
Cobalt	5.0
Copper	4.7
Gold	5.1
Iron	4.5
Lead	4.14
Magnesium	3.68
Mercury	4.5
Nickel	5.01
Niobium	4.3
Potassium	2.3
Platinum	6.35
Selenium	5.11
Silver	4.73
Sodium	2.28
Uranium	3.6
Zinc	4.3




Other gate materials TaN, TiSi, TaC, etc
Work function depends on stoichiometry
crystallinity, etc

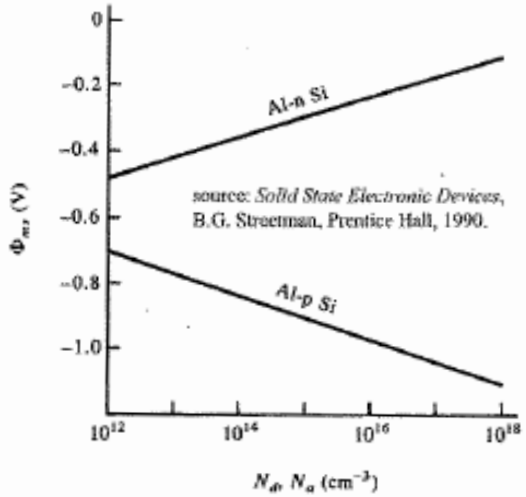
Real MOS Capacitor - Band Diagram, Equilibrium



equilibrium
(no applied voltage)

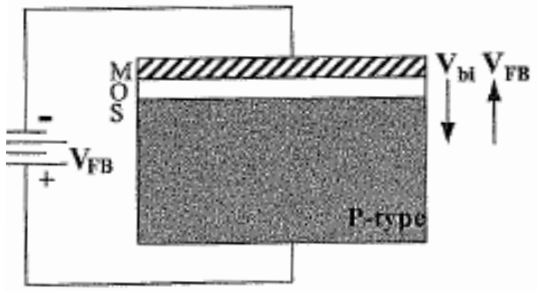
$\Phi_{MS} \equiv \phi_M - \phi_S$

$V_{bi} = -\Phi_{MS}$ (built-in voltage)



source: *Solid State Electronic Devices*, B.G. Streetman, Prentice Hall, 1990.

Real MOS Capacitor - Band Diagram, Flatband

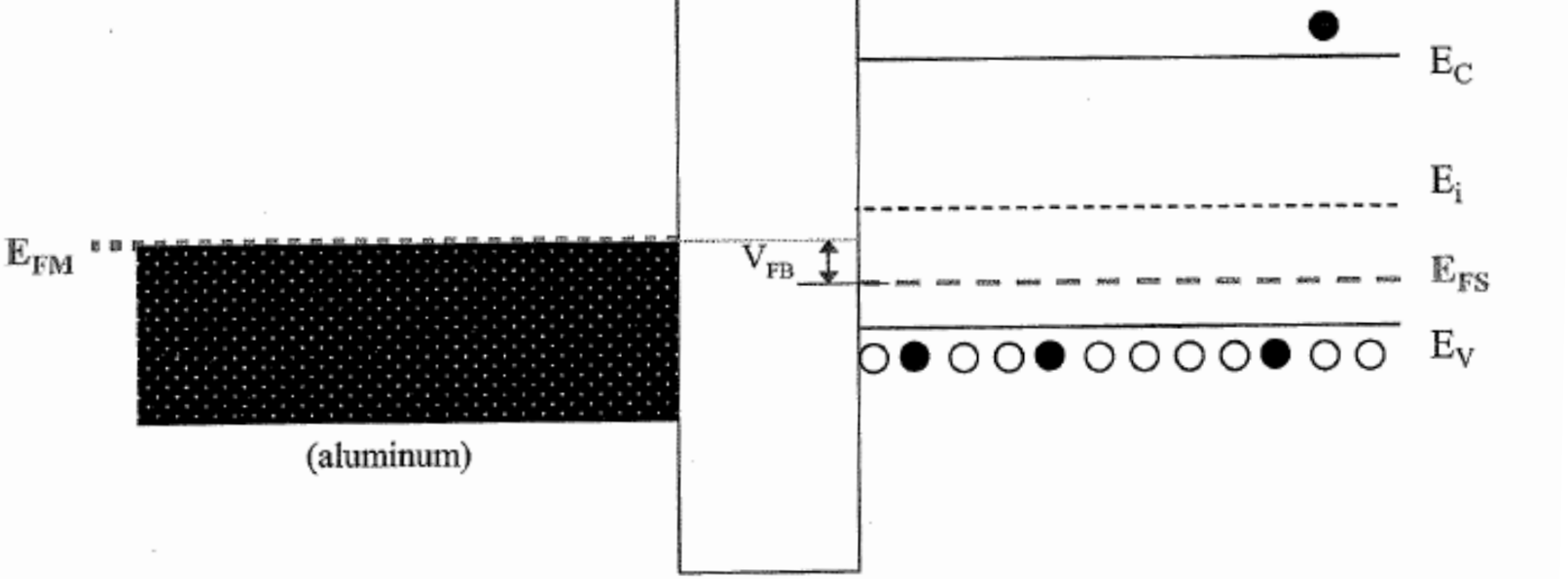


$$V_{FB} = -V_{bi} = \Phi_{MS}$$

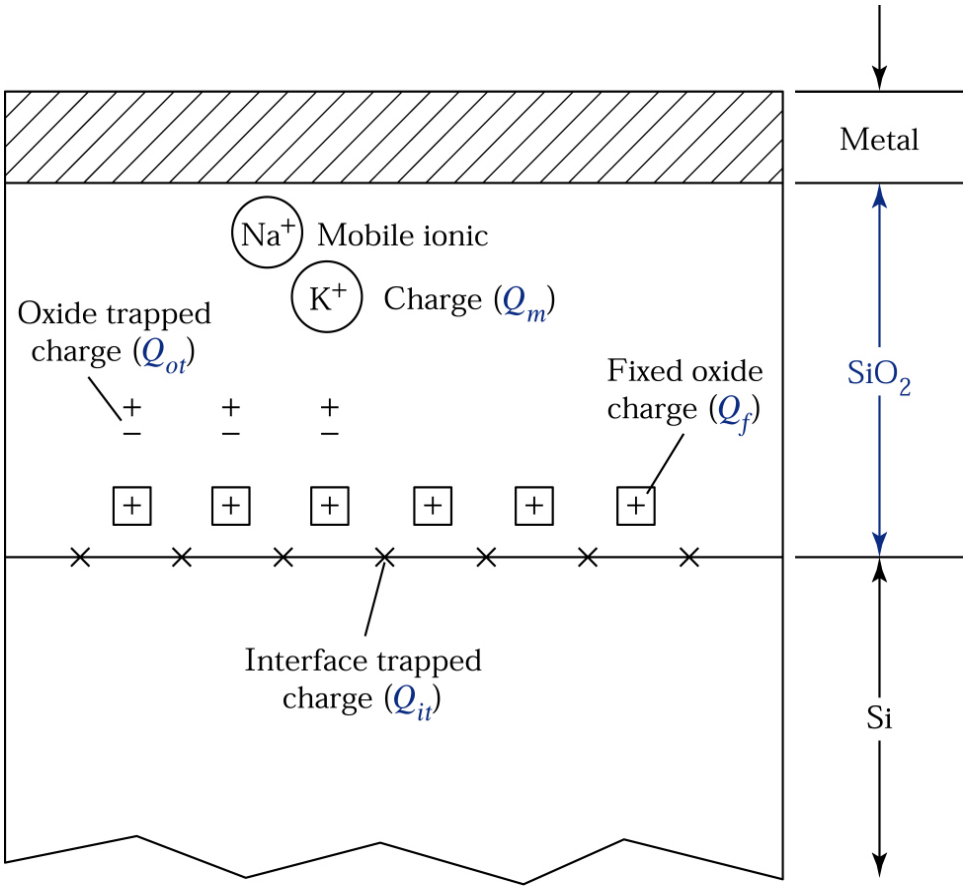
$$V_G = V_{OX} + \Psi_S + V_{FB}$$

V_{FB} = **Flatband Voltage**
for an *ideal* MOS Capacitor, $V_{FB} = 0$
for an Al gate on Si, $V_{FB} < 0$

Flat band condition



build-in charges: several kinds



$$\Delta V_{FB} = \frac{Q_{eff}}{C_i} = \frac{Q_{eff}}{C_{ox}}$$

$$Q_{eff} = \frac{1}{d}\int_0^d x\rho_{ox}(x)\,dx$$

If there is a non-negligible amount of oxide charge, the flatband voltage becomes:

$$V_{FB} = \Phi_{MS} - \frac{Q_i}{C_{ox}}$$

Flatband voltage w/ oxide charge included

Q_i = effective net oxide charge
C_{OX} = oxide capacitance = $\varepsilon_{OX}A/t_{OX}$
$\Phi_{MS} < 0$ for Al gate over Si

Parasitic charges: influence of Si orientation

Defect densities at the semiconductor surface for different crystal orientations

- 10^{10} cm^{-2} for <100>
- 10^{11} cm^{-2} for <111>

→ <100> is preferred for MOSFET production because of lower defect density

flat-band voltage of MOS diode

$$V_{FB} = \phi_{ms} - \frac{Q_{ox}}{C_{ox}}$$

with

$$Q_{ox} = Q_f + Q_m + Q_{ot} + Q_{it}$$

$$Q_{ot} \equiv \frac{1}{t_{ox}} \int_0^{t_{ox}} x \rho_{ot}(x) dx \qquad Q_m \equiv \frac{1}{t_{ox}} \int_0^{t_{ox}} x \rho_m(x) dx$$

Q_{ox} – all charges in the gate dielectric

Q_{it} - interface charges; often can be neglected, because it can be passivated by low temperature hydrogen annealing

Q_f - fixed charges

Q_{ot} - oxide trapped charges

Q_m - mobile charges

Non-ideal threshold voltage

n-channel in p-type bulk silicon

$$V_{th} = V_{FB} + 2|\psi_B| + \frac{\sqrt{2e\varepsilon_0\varepsilon_S N_A^{-}(2|\psi_B|)}}{C_{ox}}$$

p-channel in n-type bulk silicon

$$V_{th} = V_{FB} - 2|\psi_B| - \frac{\sqrt{2e\varepsilon_0\varepsilon_S N_D^{+}(2|\psi_B|)}}{C_{ox}}$$

All non-idealities are customarily absorbed in V_{FB}

Threshold voltage - Numerical Example

- MOS Capacitor with p-type substrate:

Gate is n^+ poly work function 4.1 eV , assume no parasitic oxide charges

$$t_{ox} = 20\text{nm} \quad N_a = 5\times10^{16}\,\text{cm}^{-3}$$

- Calculate flat-band voltage:

$$V_{FB} = -(\phi_{n^+} - \phi_p) = -(0.55 - (-0.4)) = -0.95\text{V}$$

- Calculate threshold voltage:

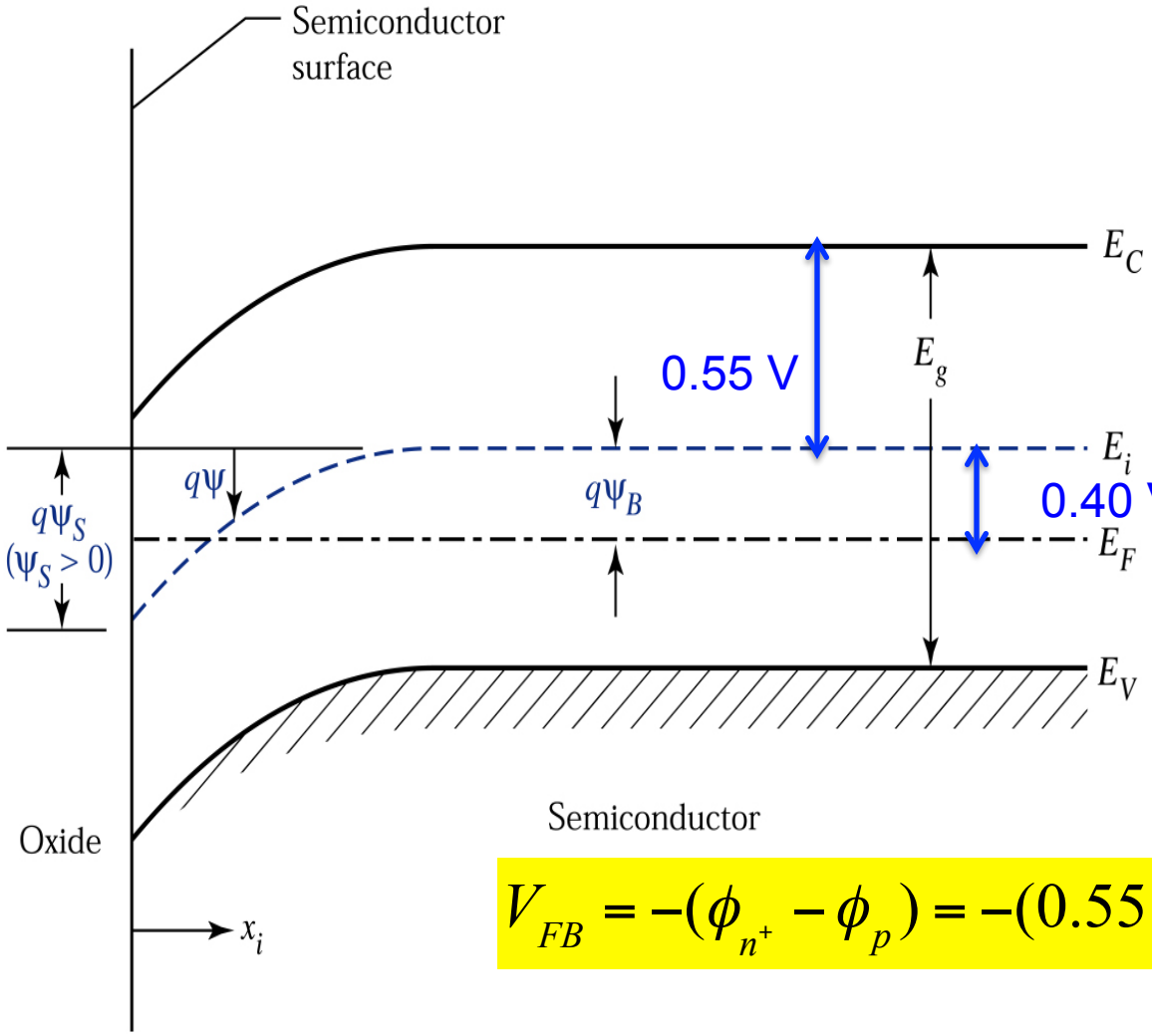
$$\psi_B = V_t \ln\left(\frac{N_A}{n_i}\right)$$

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{3.45\times10^{-13}\,\text{F/cm}}{2\times10^{-6}\text{cm}}$$

$$V_{Tn} = V_{FB} + 2\psi_B + \frac{1}{C_{ox}}\sqrt{2q\varepsilon_s N_a 2\psi_B}$$

$$V_{Tn} = -.95 - 2(-0.4) + \frac{\sqrt{2\times1.6\times10^{-19}\times1.04\times10^{-12}\times5\times10^{16}\times2\times0.4}}{C_{ox}} = 0.52\text{V}$$

flat-band voltage for n+ poly for $N_a = 5\times10^{16}\,\mathrm{cm}^{-3}$



0.40 V for $N_a = 5\times10^{16}\,\mathrm{cm}^{-3}$

$$V_{FB} = -(\phi_{n^+} - \phi_p) = -(0.55 - (-0.4)) = -0.95\mathrm{V}$$

MOS Capacitor – Threshold Voltage Revisited

Threshold Voltage

P-Type MOS Capacitor

$$V_T = V_{FB} + 2|\phi_B| + \frac{\sqrt{2\varepsilon_S q N_A |2\phi_B|}}{C'_{OX}}$$

($V_{FB} < 0$ for Al gate on Si → Increases P-type V_T in magnitude)

where $\phi_B = \frac{k_B T}{q} \ln\left(\frac{p}{n_i}\right)$

$p \approx N_A$ for extrinsic temperature region (e.g. room temp.)

$$C'_{OX} = \frac{\varepsilon_{OX}}{t_{OX}}$$ (gate capacitance per unit area)

N-Type MOS Capacitor

$$V_T = V_{FB} - 2|\phi_B| - \frac{\sqrt{2\varepsilon_S q N_D |2\phi_B|}}{C'_{OX}}$$

($V_{FB} < 0$ for Al gate on Si → Decreases N-type V_T in magnitude)

where $\phi_B = \frac{k_B T}{q} \ln\left(\frac{n}{n_i}\right)$

$n \approx N_D$ for extrinsic temperature region (e.g. room temp.)

$$C'_{OX} = \frac{\varepsilon_{OX}}{t_{OX}}$$ (gate capacitance per unit area)

Threshold Voltage vs. Substrate Doping (Oxide thickness)

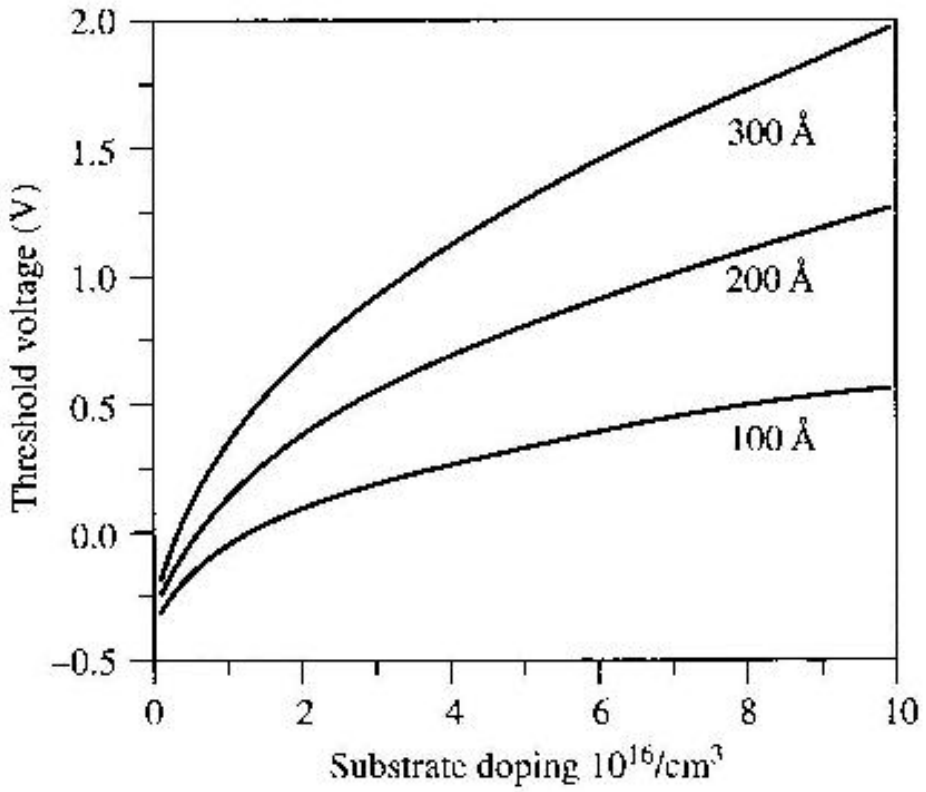
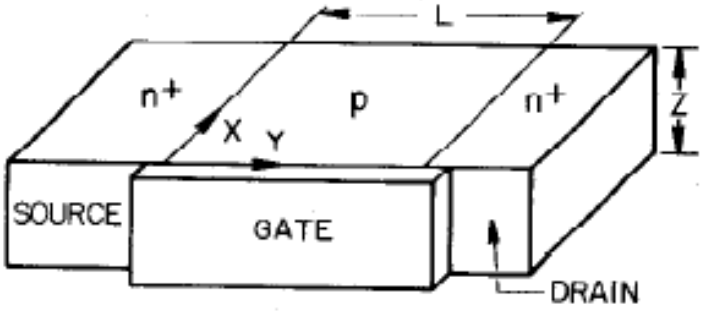
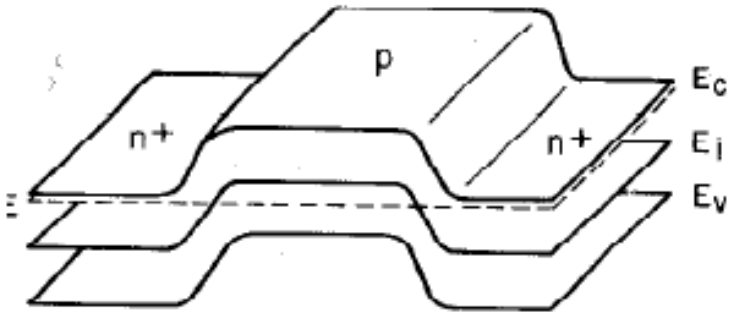


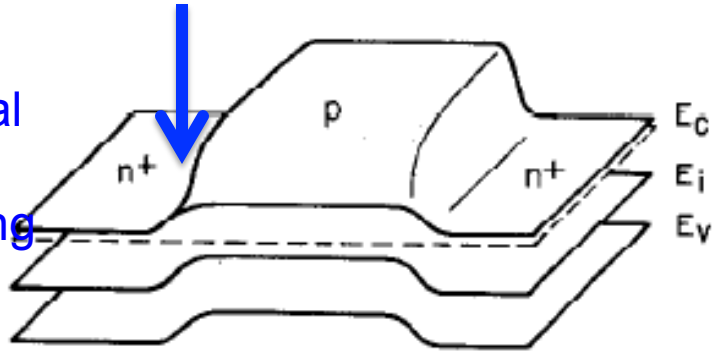
Figure 1.6 Dependence of MOS threshold voltage on the substrate doping level for different thicknesses of the dielectric layer. Parameters used in calculation: energy gap, 1.12 eV; effective density of states in the conduction band, $3.22 \times 10^{25}/m^3$; effective density of states in the valence band, $1.83 \times 10^{25}/m^3$; semiconductor permittivity, 1.05×10^{-10} F/m; insulator permittivity, 3.45×10^{-11} F/m; flat-band voltage, −1 V; temperature: 300 K. Reproduced from Lee K., Shur M., Fjeldly T. A., and Ytterdal T. (1993) *Semiconductor Device Modeling for VLSI*, Prentice Hall, Englewood Cliffs, NJ

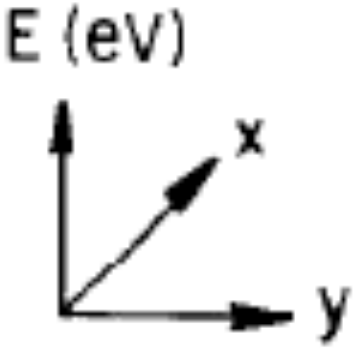
3D band diagram of a NMOS transitor





Vertical band bending

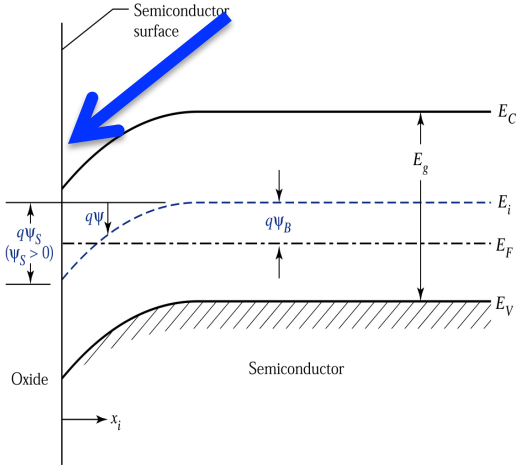




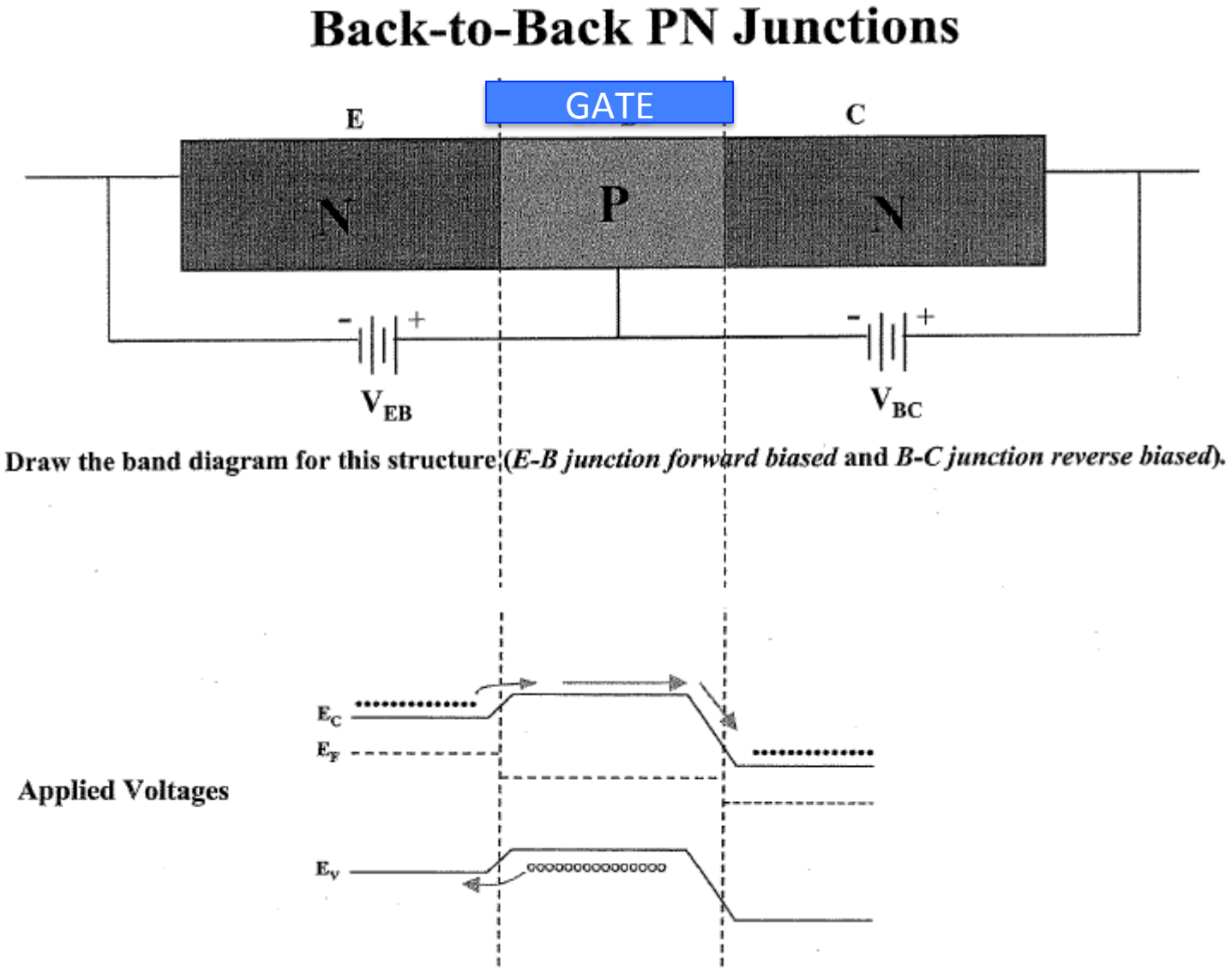
$V_G = V_D = 0$

Vertical band bending

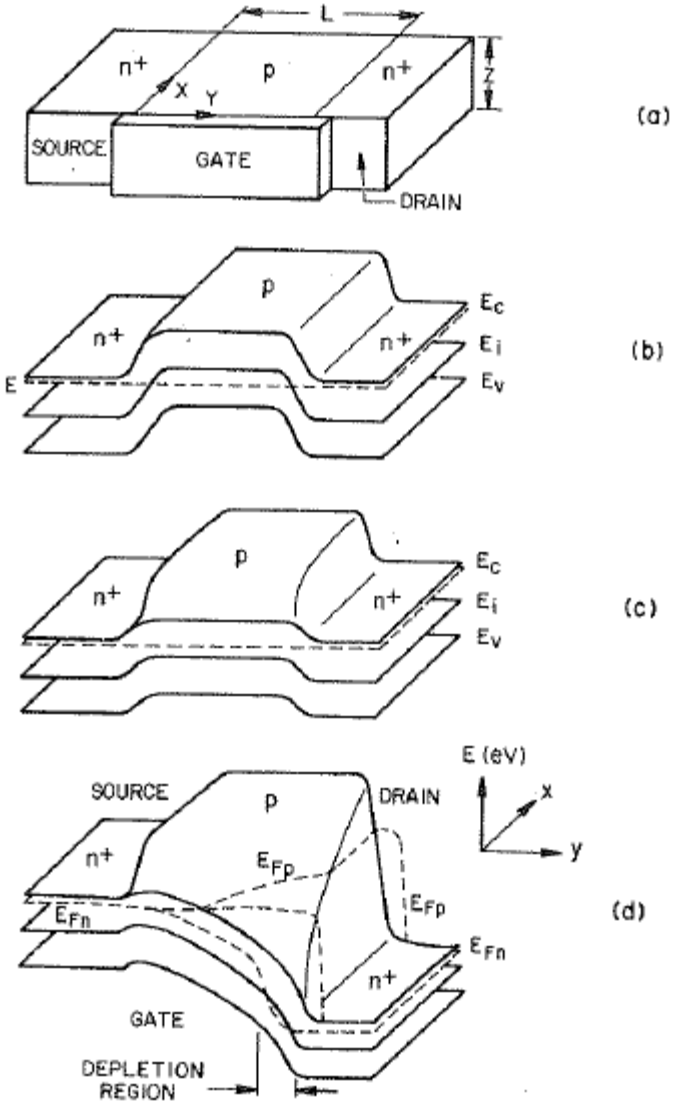
$V_G > 0$
$V_D = 0$



Weak inversion in the MOS capacitor enables conduction in the channel

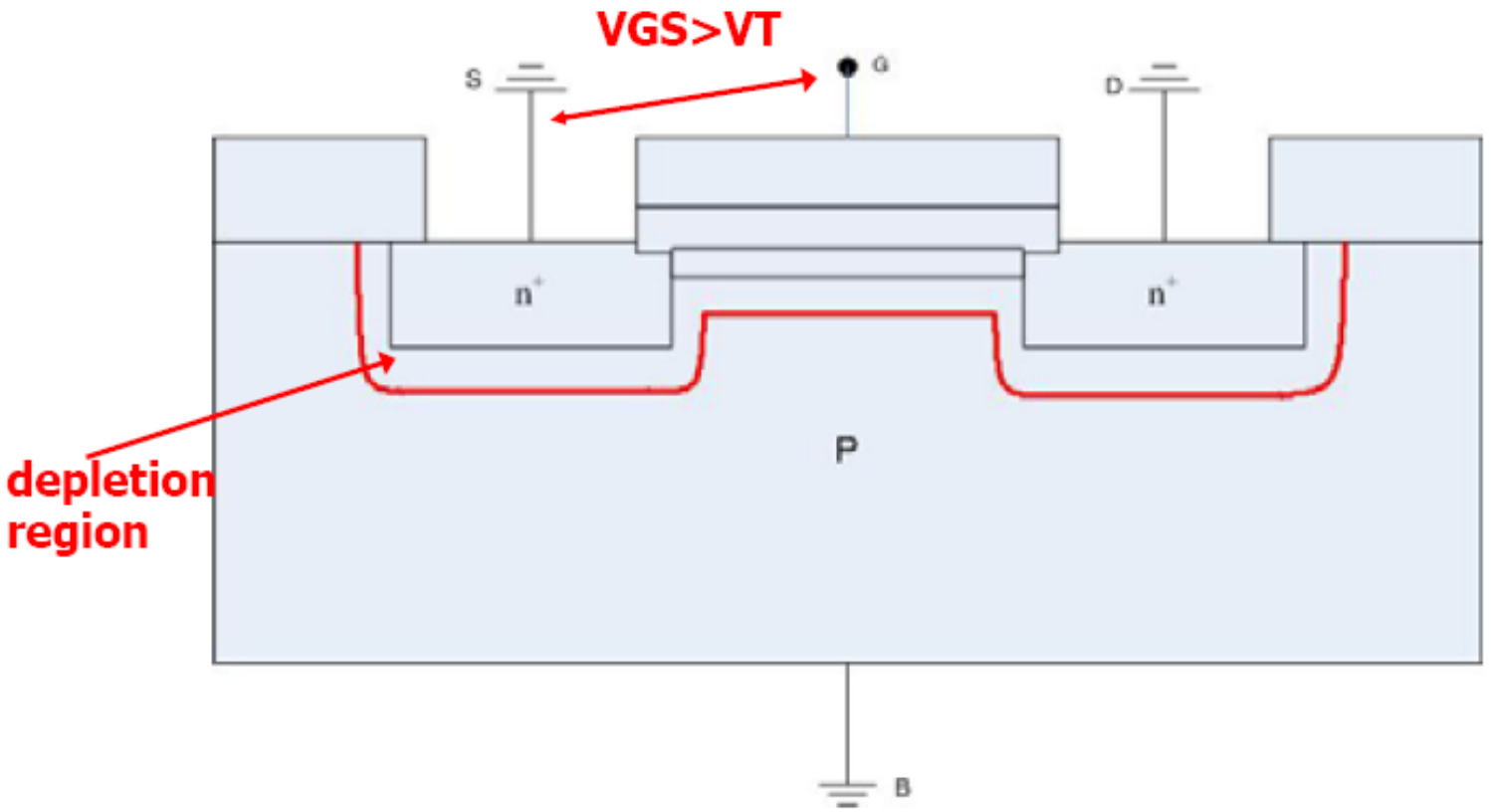


Applications of drain bias allows current flow from source to drain



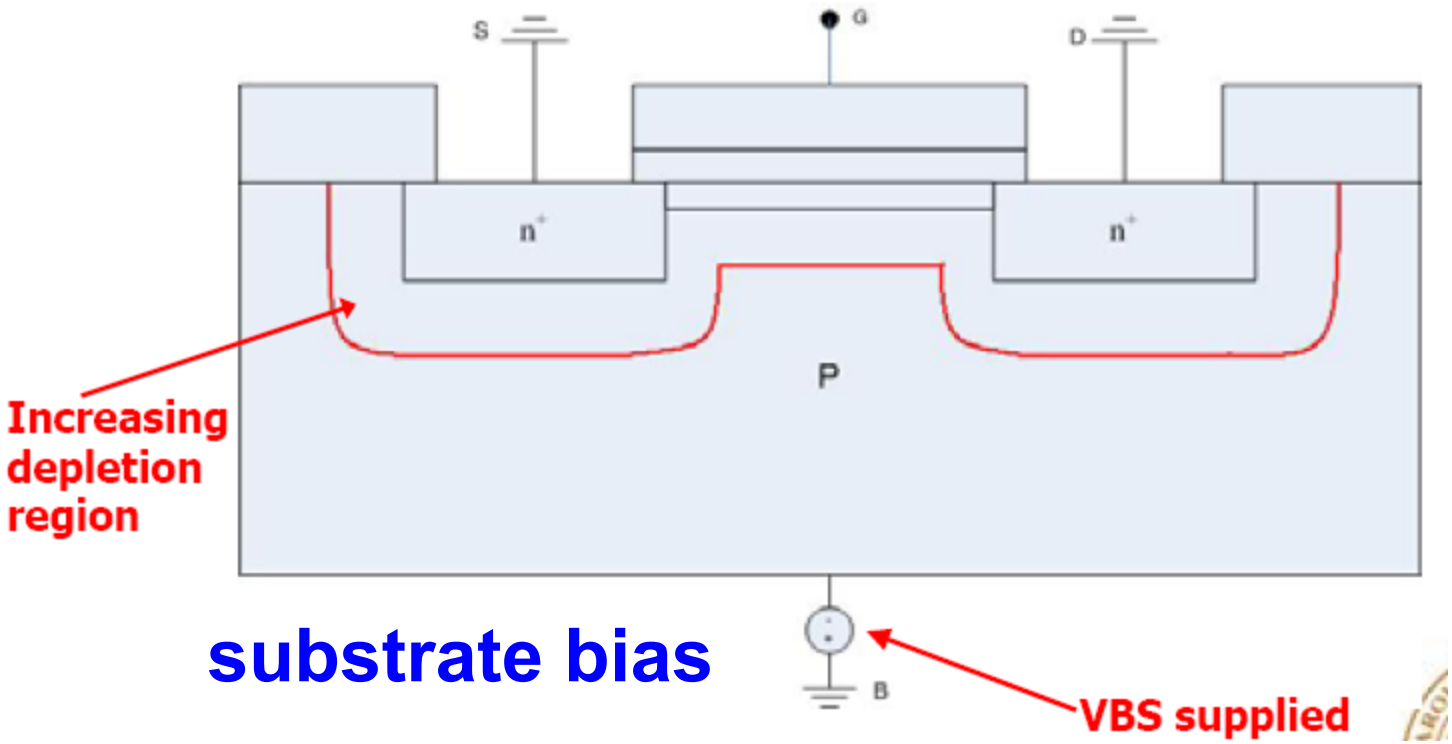
Energy bands on the drain side are pulled down

Impact of Substrate Bias on Threshold Voltage



Substrate bias Vsub =(V_{BS})≠ 0 → n+p junctions and MOS capacitor depletion zone widen

Substrate Bias Effect on Threshold Voltage

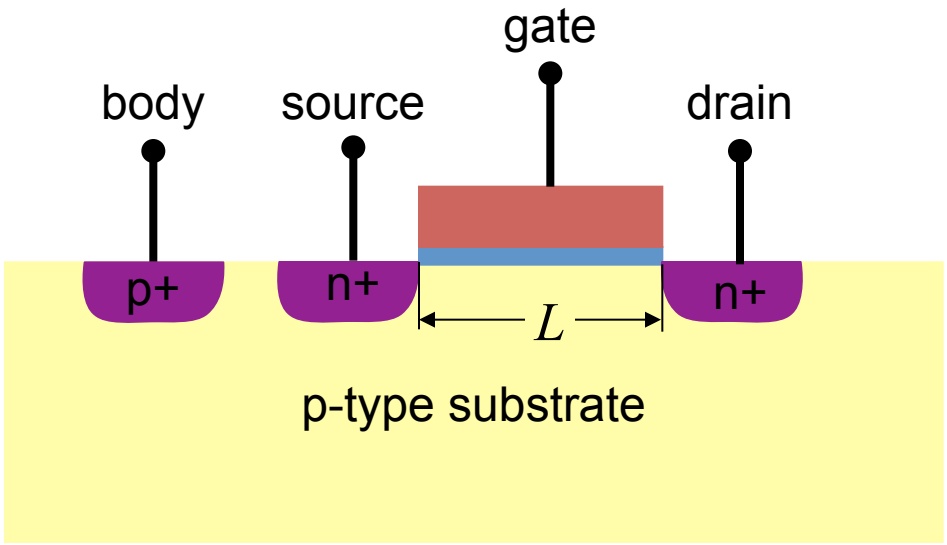


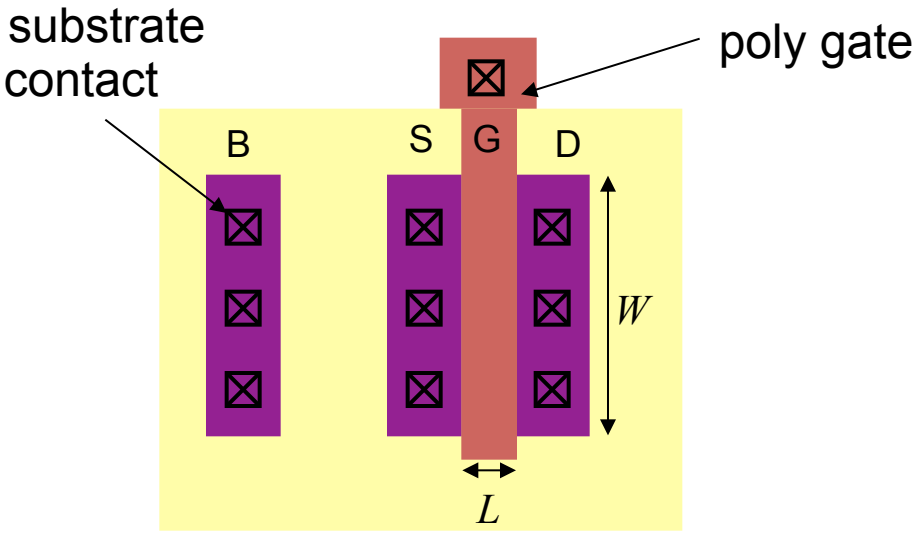
substrate bias

Balance of charges at the gate and in the substrate (depletion + inversion)

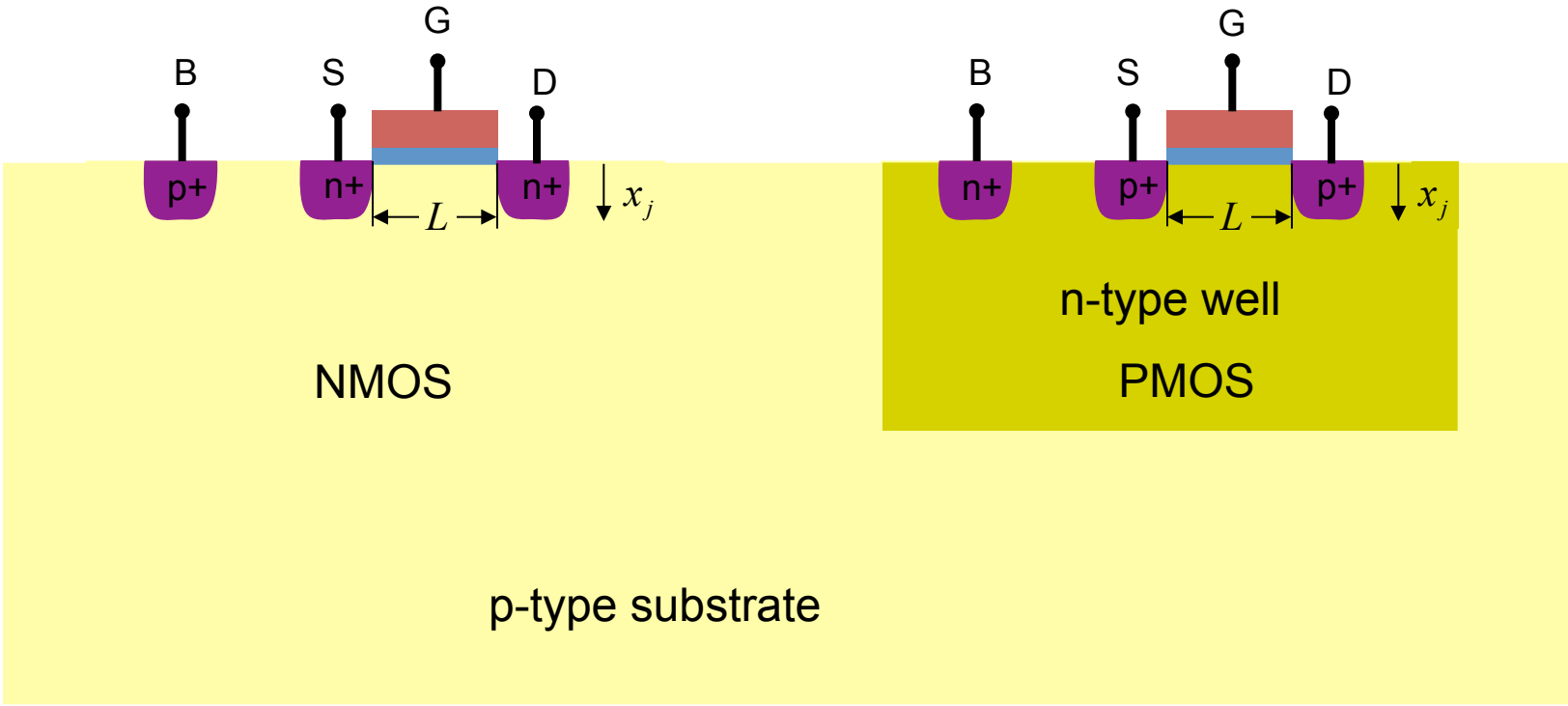
$$Q_g + Q_B + Q_n = 0$$

Implementation of the Substrate Bias Contact and MOSFET layout





NMOS and PMOS = CMOS



- Complementary MOS: Both P and N type devices
- Create a n-type body in a p-type substrate through compensation. This new region is called a "well".
- To isolate the PMOS from the NMOS, the well must be reverse biased (pn junction)

Impact of Substrate Bias on Threshold Voltage

$V_{BS} = 0$

At $V_g = V_t$ the depletion region under the gate supports $2\varphi_F$

$$Q_{B_0} = -\sqrt{2\varepsilon_0 \varepsilon_{si} q N_a (2\varphi_F)}$$

The depletion region extends and supports $2\varphi_F + |V_{BS}|$

$$Q_B = -\sqrt{2\varepsilon_0 \varepsilon_{si} q N_a (2\varphi_F + |V_{BS}|)}$$

Substrate Bias

Define the threshold voltage V_{t_0} at the zero bias $V_{BS} = 0$

$$V_{t_0} = \varphi_{ms} - \frac{Q_{ss}}{C_{ox}} - \frac{Q_{B_0}}{C_{ox}} + 2\varphi_F \qquad (1)$$

With V_{BS} applied

$$V_t = \varphi_{ms} - \frac{Q_{ss}}{C_{ox}} - \frac{Q_B}{C_{ox}} + 2\varphi_F \qquad (2)$$

(2) - (1)

Difference between VT with and without substrate bias

$$V_t = V_{t_0} + \frac{Q_{B_0} - Q_B}{C_{ox}}$$

$$V_t = V_{t_0} + \frac{1}{C_{ox}}\sqrt{2\varepsilon_0\varepsilon_{si}qN_a}\cdot\left(\sqrt{2\varphi_F + |V_{bs}|} - \sqrt{2\varphi_F}\right)$$

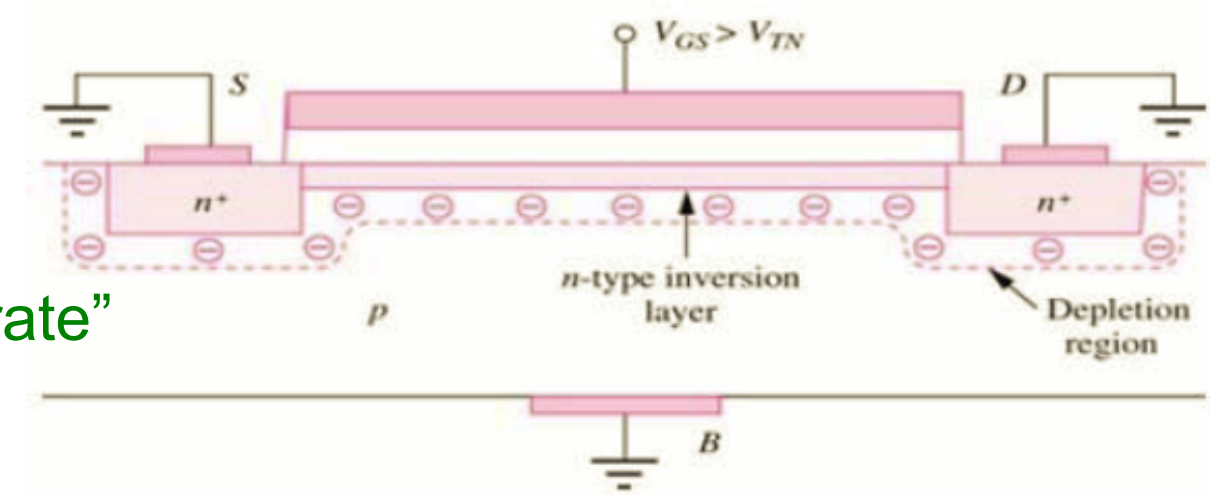
$$V_t = V_{t_0} + \gamma\cdot\left(\sqrt{2\varphi_F + |V_{bs}|} - \sqrt{2\varphi_F}\right)$$

γ – "body factor"

$$\gamma = \frac{\sqrt{2\varepsilon_0\varepsilon_{si}qN_a}}{C_{ox}}$$

The Role of Body - Body Effect

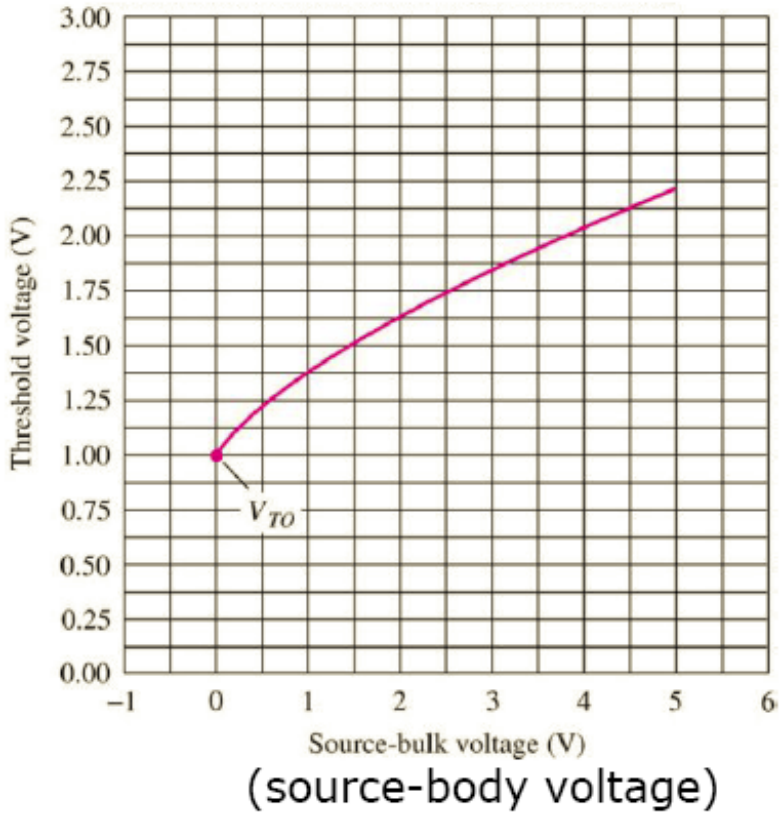
"body" = "substrate"



- Channel-body can be regarded as a *pn* junction
- If channel-body junction is reverse-biased,
  - Depletion layer beneath the gate oxide becomes wider
  - Since the amount of negative charges in the (channel + depletion) layer = amount of positive charges in the gate (Constant for a fixed gate-source voltage)
    → Channel depth is reduced
  - This is equivalent to an increase in the threshold voltage

Body Effect

or sensitivity of threshold voltage on substrate bias



- Non-zero v_{SB} changes threshold voltage:

$$V_{TN} = V_{TO} + \gamma\left(\sqrt{v_{SB} + 2\phi_F} - \sqrt{2\phi_F}\right)$$

where

V_{TO}= zero substrate bias for V_{TN} (V)

γ= body-effect parameter $(\sqrt{V})$

$2\Phi_F$= surface potential parameter (V)

$$\gamma = \frac{\sqrt{2\varepsilon_o \varepsilon_{Si} q N_a}}{C_{ox}}$$

It follows that the body voltage controls i_D.
This phenomenon is known as the **body effect**.

threshold adjustment by substrate bias numeric example

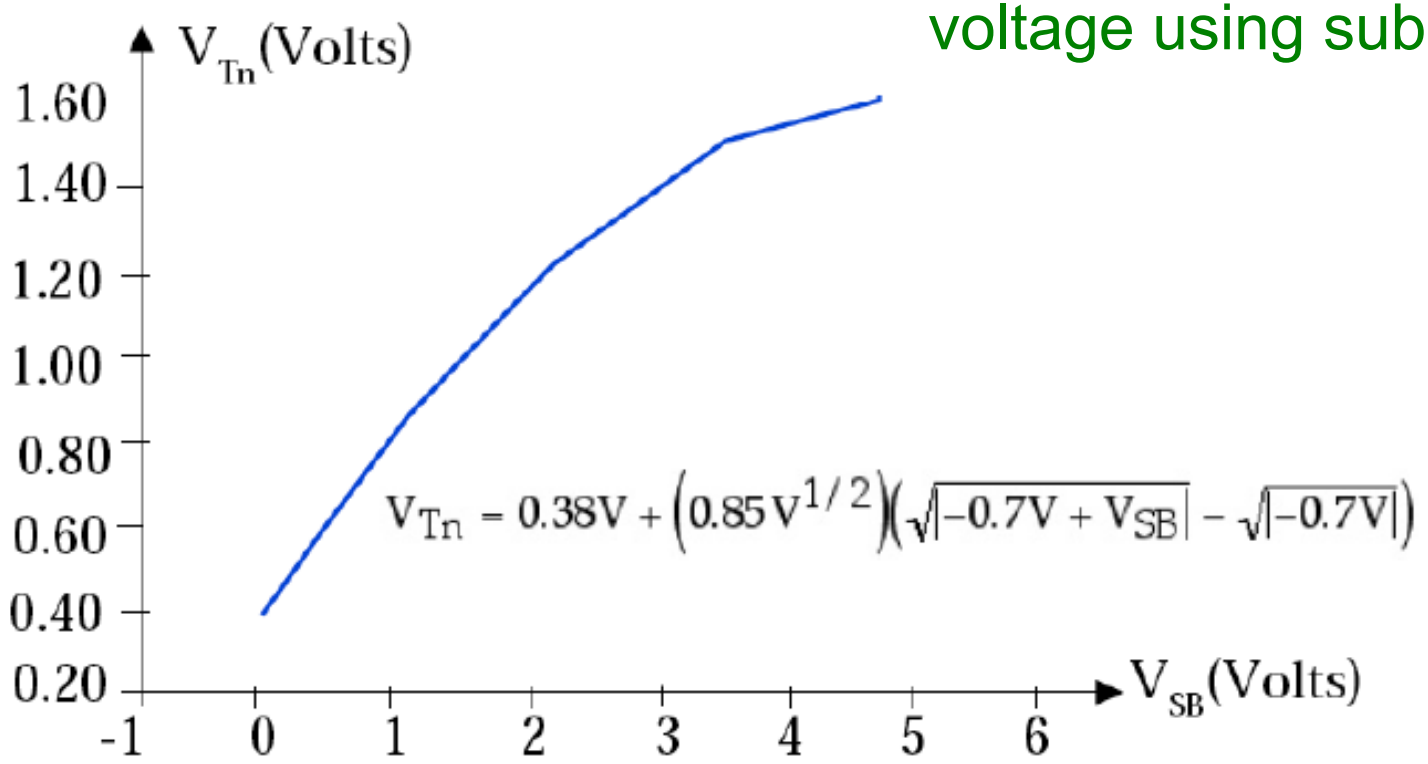
$$V_{Tn} = V_{T0n} + \gamma\left(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|}\right)$$

where

$$V_{T0n} = 0.38V$$

$$\gamma = 0.85\,V^{1/2}$$

Dynamic setting of threshold voltage using substrate bias



Non-equilibrium Analysis of the MOS Diode

Assume MOS diode is biased into the inversion mode, then a pn junction exists between the n surface and the p bulk.

If there is a nearby n^+-type diffused region that contacts the inverted surface and keeps it at a fixed potential, it is possible to apply bias to the pn junction. This corresponds to a non-equilibrium condition within the silicon. (Some current will flow between the n-surface and p-bulk. However, if the junction is reverse biased, the reverse current will be small.**)**

An energy band diagram for the case of bias applied to an inverted surface is characterized by quasi-Fermi levels, one for the p-region and one for the n-region. The two quasi-Fermi levels are separated by the applied reverse bias.

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Three biases
V_G, V_C, V_B

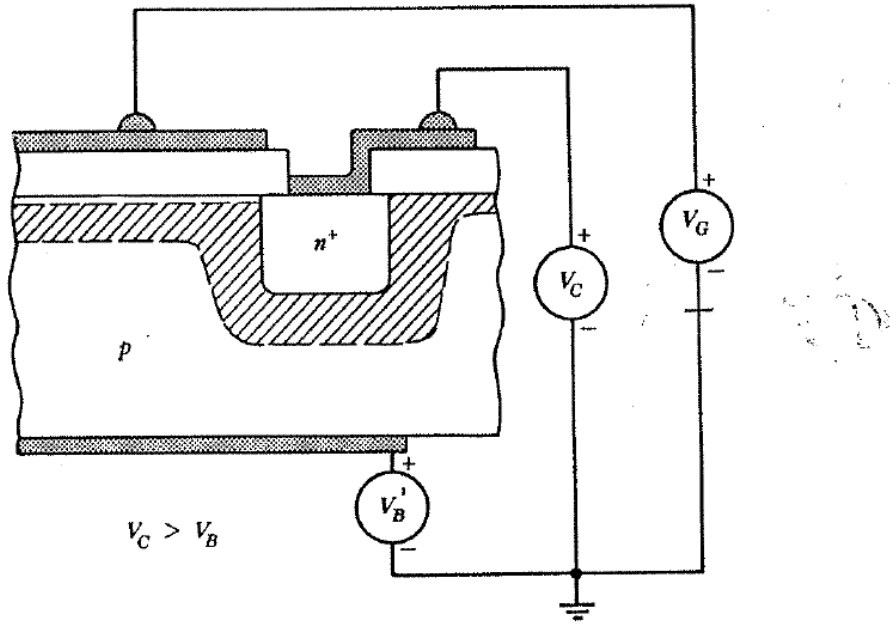
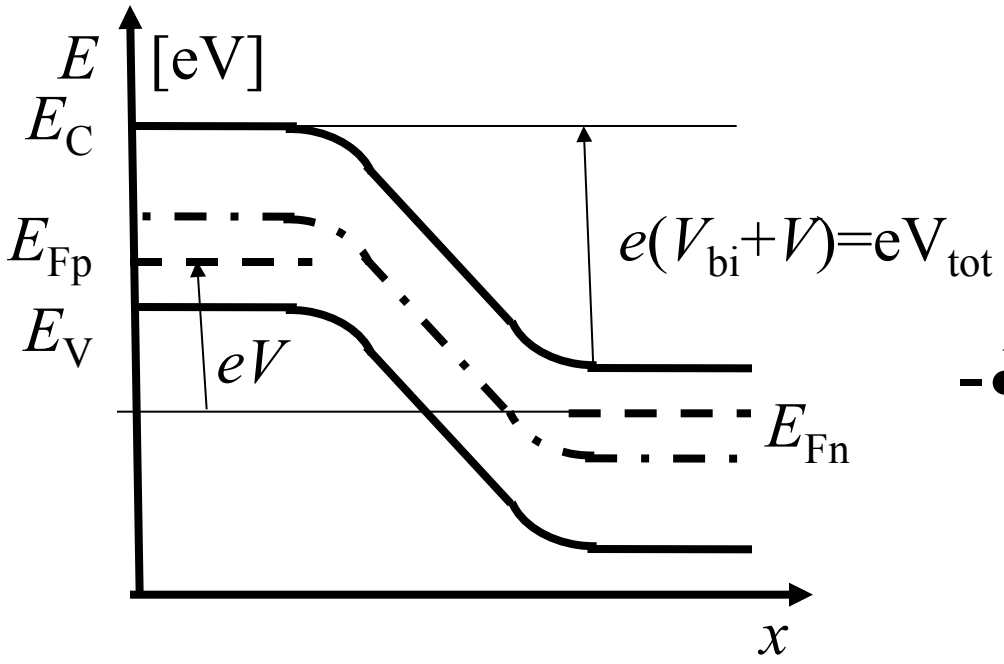


Figure 7.9 A diffused junction in the vicinity of an MOS capacitor can be used to bias the induced junction between the bulk of the silicon and an inversion layer formed at the oxide-silicon interface. The cross-hatching indicates the extent of the space-charge region in the depleted silicon.



Recall Reverse-biased pn Junction

$V < 0$

E_{Fp} and E_{Fn} are called the **quasi Fermi levels**. In non-equilibrium situation as above the quasi Fermi levels are separated by the reverse bias V.

Another example for quasi Fermi levels. For thermal equilibrium Fermi level is defined as follows:

$$n_o = n_i \exp\left(\frac{E_F - E_i}{kT}\right)$$

Now assume we have created excess carriers δn. We can now characterize the total electron population by a quasi Fermi level:

$$n_o + \delta n = n_i \exp\left(\frac{E_{Fn} - E_i}{kT}\right)$$

Non-equilibrium Analysis of the MOS Diode

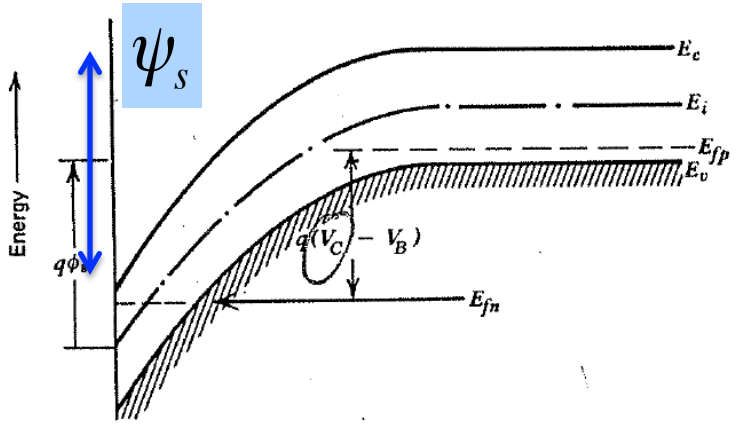


Figure 7.10 Energy-band diagram for an inverted surface on *p*-type silicon with a voltage $(V_C - V_B)$ applied between the inversion layer and the substrate.

A reverse bias between the induced surface n-region and the bulk increases the charge Q_d in the depletion layer. Since the negative charge induced by the reverse bias $V_G - V_B$ is shared between depletion and inversion layers, an increase of the charge in the depletion layer means that there is less charge available to form the inversion charge for a given gate voltage. In other words, more gate voltage has to be applied to induce the same number of electrons in the inversion layer when there is a reverse bias. With reverse bias present, the surface potential at the onset of strong inversion becomes

$$\psi_s = -2\psi_B + V_{sub}$$

rather than $$\psi_s = -2\psi_B$$

$$where \quad V_{sub} = V_C - V_B$$

Non-equilibrium Analysis of the MOS Diode

Consequently, the change of the surface potential between flat band and strong inversion is $2|\psi_B| + V_{sub}$ rather than $2|\psi_B|$ The corresponding maximum depletion layer width and the depletion-layer charge Q_d become

$$W_{\max} = (x_{d\max}) = \sqrt{\frac{2\varepsilon_s(2|\psi_B| + V_{sub})}{qN_A}}$$

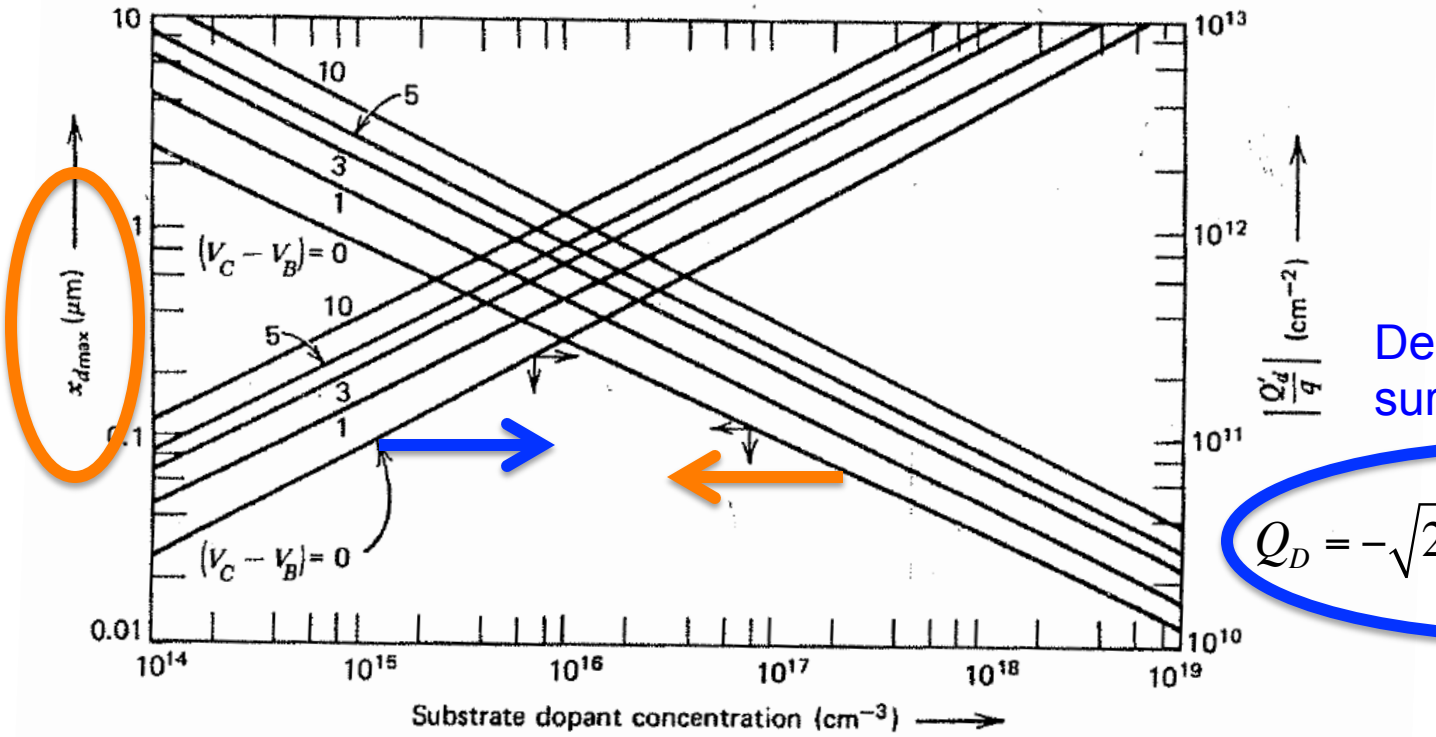
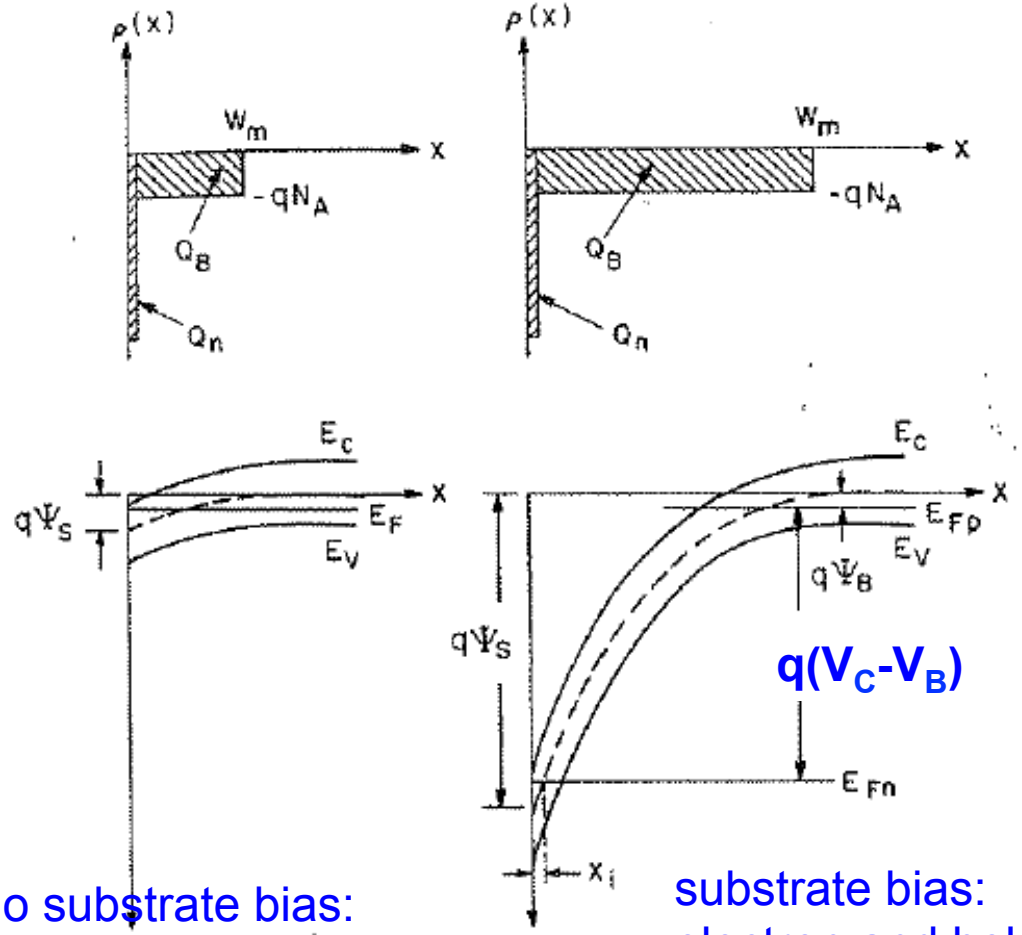


Figure 7.11 Maximum depletion-region width $x_{d\,max}$ and corresponding area density of charge in the depletion region Q'_d/q as functions of the substrate dopant concentration with the applied channel-to-substrate bias $(V_C - V_B)$ as a parameter. The curves are solutions to

Depletion charge surface density

$$Q_D = -\sqrt{2\varepsilon_s qN_A(2|\psi_B| + V_{sub})}$$

Non-equilibrium Analysis of the MOS Diode



$q(V_C-V_B)$

no substrate bias:
electron and hole
Fermi levels aligned

substrate bias:
electron and hole
Fermi levels are separated by V_{sub}

Fig. 5 Comparison of charge distribution and energy band variation of an inverted p region for (a) the equilibrium case and (*b*) the nonequilibrium case at the drain. (After Grove and Fitzgerald, Ref. 17.)

Non-equilibrium Analysis of the MOS Diode for Vc≠0

For the ideal diode (V_G-V_B)=V_{FB} corresponds to the condition of charge neutrality. Therefore (V_G-V_B)-V_{FB} is the effective voltage tending to charge the MOS capacitor. The charging voltage [(V_G-V_B)-V_{FB}] is the sum of a drop across the oxide V_{ox} and the drop in the silicon V_{si}.

$$V_G - V_B - V_{FB} = V_{ox} + \psi_s - \psi_B$$

$$E_{ox} = V_{ox} / d = [(V_G - V_B - V_{FB}) - (\psi_s - \psi_B)]$$

$$E_s = \frac{\varepsilon_{ox} E_{0x}}{\varepsilon_s}$$

$$\varepsilon_s E_s = C_{ox}[(V_G - V_B - V_{FB}) - (\psi_s - \psi_B)] = -Q_s$$

$$Gauss\ law \quad -\varepsilon_s E_s = Q_s = Q_n + Q_D$$

$$Q_n = -C_{ox}[(V_G - V_B - V_{FB}) - (\psi_s - \psi_B)] - Q_D$$

$$in\ strong\ inversion \quad \psi_s = -\psi_B + (V_c - V_b) = -\psi_B + V_{sub}$$

$$Q_n = -C_{ox}[(V_G - V_{FB} - V_c) - 2|\psi_B|] + \sqrt{2\varepsilon_s q N_A (2|\psi_B| + V_c - V_B)}$$

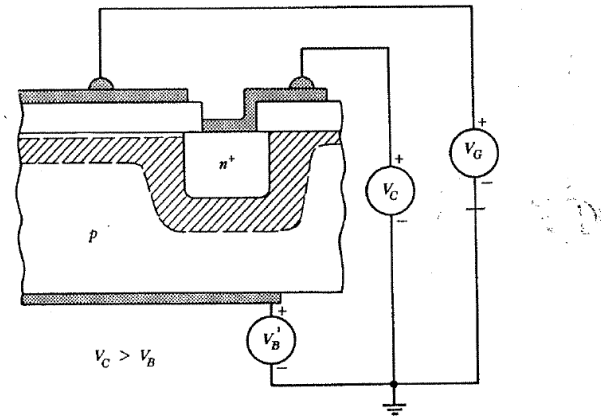


Figure 7.9 A diffused junction in the vicinity of an MOS capacitor can be used to bias the induced junction between the bulk of the silicon and an inversion layer formed at the oxide-silicon interface. The cross-hatching indicates the extent of the space-charge region in the depleted silicon.

Non-equilibrium Analysis of the MOS Diode

Threshold voltage is the gate voltage necessary to induce a conducting channel at the surface of the semiconductor and it can be defined as the gate votage that results when just Q_n=0. $[(V_G-V_B)-V_{FB}]$ is the sum of a drop across the oxide V_{ox} and the drop in the silicon V_{si}.
Solve equation Q_n for V_G and set $V_G=V_T$ when $\psi_s = -\psi_B + (V_c - V_B)$. At this condition the inversion charge Q_n will be just zero. The charge in Si is provided by the maximal depletion charge.

$$Q_n = -C_{ox}[(V_G - V_{FB} - V_c) - 2|\psi_B|] + \sqrt{2\varepsilon_s q N_A (2|\psi_B| + V_c - V_B)} = 0$$

$$V_T = V_{FB} + V_C + 2|\psi_B| + \frac{1}{C_{ox}}\sqrt{2\varepsilon_s q N_A (2|\psi_B| + V_c - V_B)}$$

Observations:

•The formula contains V_{FB} because a gate voltage equal to V_{FB} is necessary to bring the silicon to a charge neutral condition.

•Increasing channel voltage V_c increases the gate voltage necessary to induce a given charge at the surface 2abs(ψ_B) volts must be applied to cause the silicon bands to be bent to an inverted condition.

•The square-root term accounts for the uniform distribution of space charge in the depletion region. It is inversely proportional to the oxide capacitance. It increases with V_c-V_b and reflects the redistribution of charge Q_s from the inversion layer (Q_n) to the depletion layer Q_d.

Non-equilibrium Analysis of the MOS Diode using the body factor

Charge in the inversion layer

$$Q_n = -C_{ox}(V_G - V_T)$$

The body factor for MOS diode in non-equilibrium

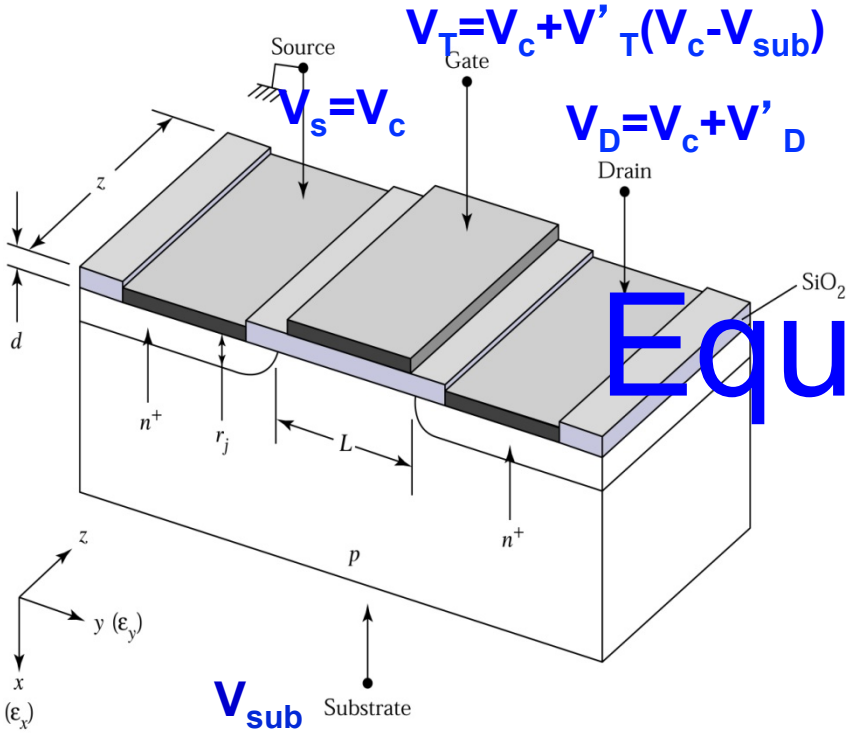
$$V_T = V_{FB} + V_C + 2|\psi_B| + \frac{1}{C_{ox}}\sqrt{2\varepsilon_s q N_A (2|\psi_B| + V_c - V_B)}$$

$$V_T = V_{FB} + V_C + 2|\psi_B| + \gamma\sqrt{(2|\psi_B| + V_c - V_B)}$$

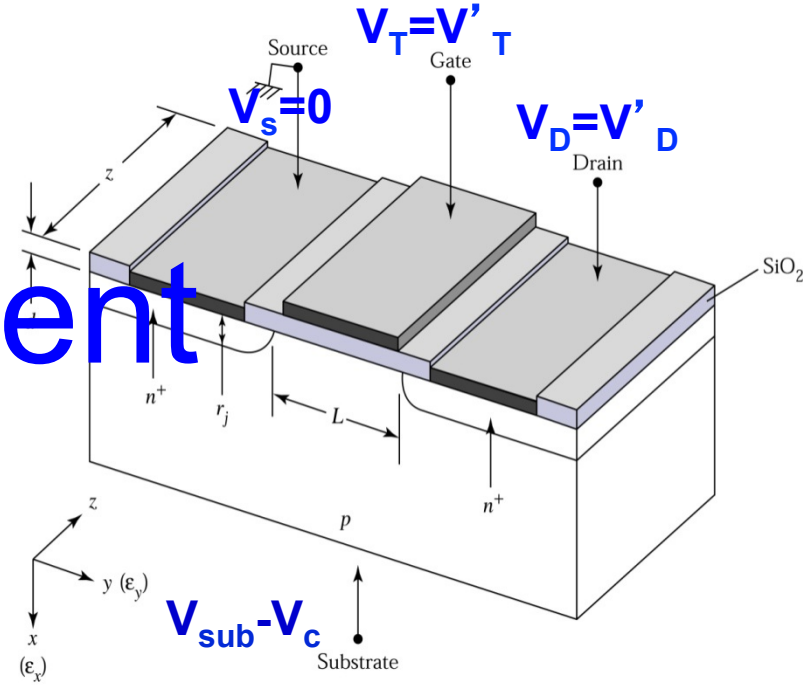
$$\gamma = \frac{1}{C_{ox}}\sqrt{2\varepsilon_s q N_A} \quad body\ \ factor$$

Significance of V_c or V_{ch}

V_c is the potential of the n^+ region connected to the inversion layer, when the inversion layer exists. Therefore in this case, Vc is called also the **channel potential** and sometimes denoted by V_{ch}. V_c or V_{ch} is a positive potential bias relative to the ground (in case of an NMOSFET).

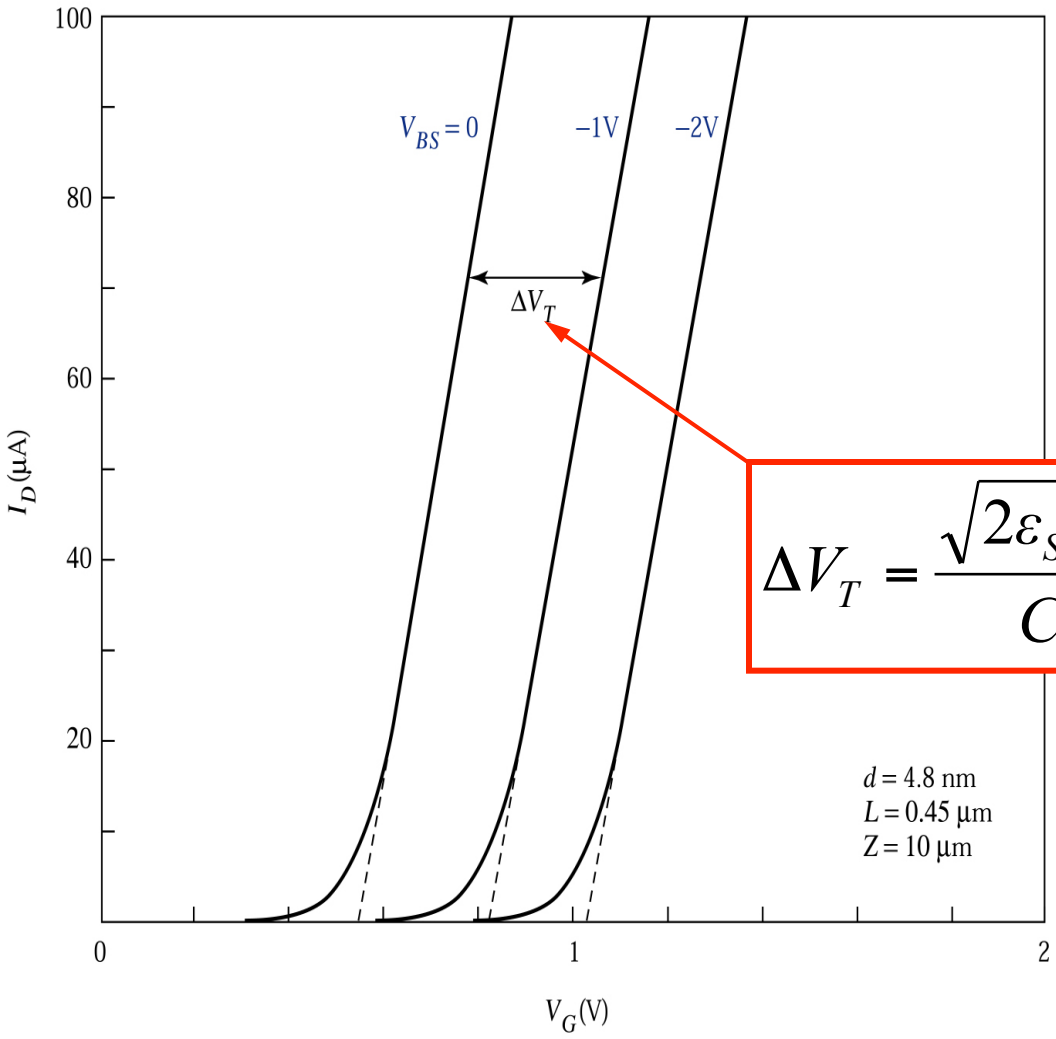


Equivalent to



In order to invert the channel the gate bias has to be at least V_c (the smaller potential bias of the two at the n+ regions) plus the intrinsic MOSFET threshold voltage.

Threshold adjustment by substrate bias



change of threshold voltage:

$$\Delta V_T = \frac{\sqrt{2\varepsilon_S q N_A}}{C_{ox}}\left(\sqrt{2\psi_B + V_{BS}} - \sqrt{2\psi_B}\right)$$

V_T with and without Substrate Bias

The threshold voltage :

$$V_T = V_{FB} + 2\varphi_b + \frac{\sqrt{4\varepsilon_s\, qN_a\, \varphi_b}}{C_{ox}}$$

The threshold voltage including body bias effect:

$$V_T = V_{FB} + 2\varphi_b + \frac{\sqrt{2\varepsilon_s\, qN_a\, (2\varphi_b - V_B)}}{C_{ox}}$$

For V_c=0