A 94-GHz Monolithic Front-End for Imaging Arrays in SiGe:C Technology

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***Abstract*— A monolithic downconverter for 94 GHz imaging arrays implemented in SiGe:C technology is presented. The downconverter consists of a three stage differential LNA with lumped matching networks and a polyphase subharmonic mixer. It yields 20 dB conversion gain at 94 GHz with an input 1-dB compression point of -31 dB and a current consumption of 45 mA at 3.3 V supply voltage. The total required die area of the complete downconverter (excluding pad frame) is 0.1 mm^2, making it particularly suitable as a front-end in multi-channel receiver systems.**

I. Introduction

An increased interest in millimeter-wave (mmWave) and THz imaging for security applications has recently created a demand for integrated receiver front-ends, which can be used in phased or focal-plane array configurations. For imaging arrays, the number of channels or pixels present in the system is a critical factor, since it determines the resolution, unless mechanical scanning is used. Hence, the die area and power consumption required by each receiver channel needs to be optimized.

A front-end architecture capable of meeting the requirements of a monolithic integrated receiver array is depicted in Fig. 1. The proposed subharmonic architecture has the advantage that the local oscillator (LO) signal can be generated and distributed at half the operating frequency. By use of differential circuit topology, balanced on- or off-chip antennas, such as folded dipole antennas, can be connected directly to the receiver input without the need for on-chip baluns. An advantage of the combined use of subharmonic mixing with differential architecture is that neither the LO fundamental nor its harmonics fall into the receive band. Provided that quadrature (I/Q) mixers are used, zero-IF or near zero-IF downconversion can thus be implemented without the DC-offset or blocking typically caused by LO self mixing.

A differential implementation of an LNA has been presented at 77 GHz [1]. As transmission line stubs were used in this paper for the interstage tuning a relatively large area was needed. However, it has been shown that spiral inductors can be used as a more compact alternative even at mmWave frequencies, with single-ended amplifier implementations available up to 140 GHz [2].

Subharmonic mixing has previously been demonstrated at 120 GHz in a SiGe:C process [3]. A polyphase concept with two mixer cores was used where the RF signal was

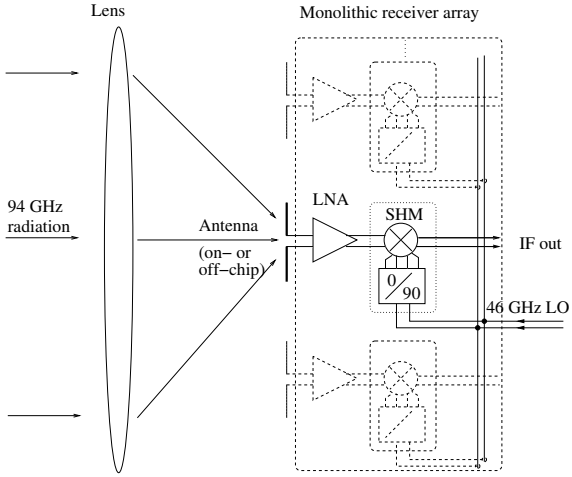

Fig. 1. Architecture of a subharmonic monolithic array receiver.

successively multiplied by an I and Q-component of the local oscillator signal. The die area, however, was 0.75 mm^2 without pads, primarily due to the area consumption of a 90-degree transmission line hybrid used to generate the necessary local oscillator phase shift for the two mixer cores. More compact solutions as described in this paper are based on conventional lumped RC polyphase networks and have previously been demonstrated primarily at lower frequencies, e.g. up to 60 GHz in [4], [5] and [6].

This paper presents a compact 94-GHz subharmonic front-end based on lumped passive elements and a fully differential circuit topology. Spiral inductors are used in the LNA matching networks and an area efficient RC-polyphase filter is used to provide the subharmonic mixer cores with the required LO signals. Through monolithic integration of the LNA and mixer, the total required die area for the downconverter is 0.1 mm^2, excluding pads.

II. Circuit Design

The downconverter subcircuits were designed and evaluated both as separate components, as well as, in their fully integrated configuration. In the following sections the details of the LNA, mixer, downconverter design, and integration are presented.

A. Differential 94-GHz amplifier

The amplifier core consists of three differential cascode amplifier stages as illustrated in Fig. 2. The cascode topology uses LC-interstage impedance matching and the transistors in the cascodes are biased at their peak f_T current density. Each

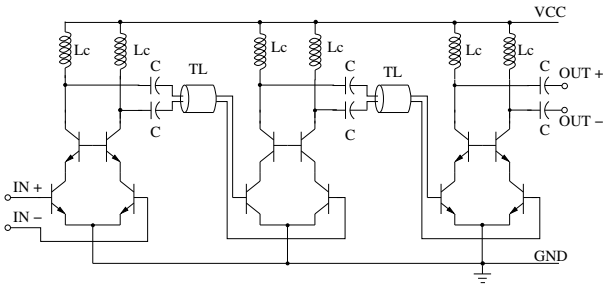

Fig. 2. Simplified schematic of the three-stage cascode LNA

cascode stage uses a lumped element spiral inductor (0.3 nH) and metal-insulator-metal (MIM) capactitor (6 fF) in a LC-tank to match their output impedance to the following stage. The spiral inductors are implemented as a square two-turn coil with the windings in adjacent metal layers. Interstage feedlines (TL) consisting of 55-μm long coupled microstrips with odd mode impedance of 100-Ω are used to cascade the stages of the amplifier.

The simulated gain of the three-stage amplifier is 21 dB, with an input 1-dB compression point of -23 dBm. The three-stage cascode amplifier draws 11 mA from a 3.3 V supply. To simplify design and testing, the biasing network uses separate current mirrors, which increases the total current consumption of the LNA to 28 mA. However, by the use of an optimized and shared biasing network, the total current consumption can be reduced to less than 15 mA.

B. Subharmonic Mixer

The subharmonic mixer, shown in Fig. 3 is based on two cascaded switching quads with the LO fed 90-degree out-of-phase through the help of a RC polyphase network. Multiplication of the RF signal with the in-phase (I) and quadrature component (Q) of the LO signal can mathematically be expressed as

$$\begin{aligned} IF_{out} &= RF(t)LO\left(\sin\left(\omega_{LO}t\right)\cos\left(\omega_{LO}t\right)\right) \\ &= RF(t)\frac{LO}{2}\left(\sin\left(2\omega_{LO}t\right)\right) \end{aligned} \quad (1)$$

which is identical to mixing of the RF signal with twice the LO frequency. Hence, this type of subharmonic mixing is not based on the use of higher order non-linearities in the devices. A broadband IF output bandwidth of up to 10 GHz was achieved using 200-Ω load resistors and a differential emitter follower buffer. The simulated conversion gain and 1-dB input compression point was 5 dB and -8 dBm, respectively. If desired, a higher conversion gain over a reduced IF bandwidth may be obtained by the use of larger collector load resistors or a tuned output network.

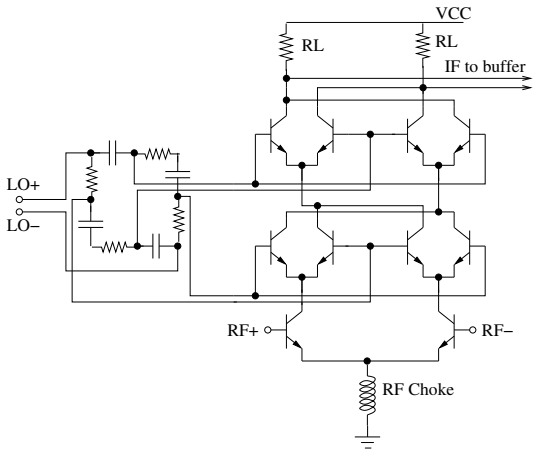

Fig. 3. Schematic of the subharmonic mixer and polyphase network. Biasing and the output buffer is excluded.

In the simulation, 8 dBm LO drive power is required for maximum conversion gain. Most of the LO power is consumed by the 50-Ω resistors in the polyphase network and a higher impedance network can be implemented in order to reduce the LO drive requirement.

The total current consumption of the mixer is 17 mA of which the majority is consumed by the common emitter IF output buffer. Less than 7 mA from a 3.3 V supply is required to power the mixer core.

C. Complete front-end and characterization setup

In the intended application, the differential front-end circuits are interfaced directly to a balanced (dipole) antenna, which can reside either on- or off-chip. Three test-sites with baluns at the RF and LO ports were designed as shown in Fig. 4 a-c) to facilitate characterization in a single ended wafer probing environment. The baluns were implemented as tuned transformers with windings in adjacent metal layers. Associated losses of the RF and LO baluns were extracted from back-to-back test structures.

III. Fabrication

The circuits were fabricated in the 0.25 μm SiGe:C BiCMOS technology (SG25H1) from IHP Microelectronics [7] featuring transistors with f_{max} of 220 GHz. The inductors and transmission lines where implemented in a five layer aluminum back-end.

Micrographs of the LNA, mixer, and downconverter test-sites are shown in Fig. 5, Fig. 6, and Fig. 7, respectively.

IV. Measured Results

A. LNA characterization

The meausured small-signal gain and the input return-loss of the LNA including the loss of auxiliary input and output test-baluns are shown in Fig. 8. The loss of the 94-GHz auxiliary test-baluns was extracted from back-to-back test structures and measured to be 4 dB each. Hence, the de-embedded gain of the LNA at 94 GHz is 15 dB. The detuning of the LNA gain peak

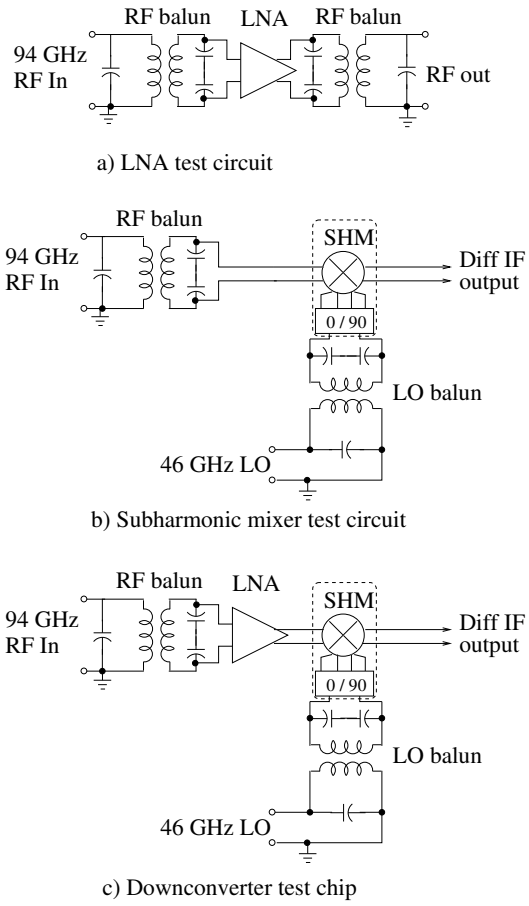

Fig. 4. Test sites designed to allow characterization of the LNA (a), the mixer (b), and the complete front-end (c). Baluns are included to facilitate testing in a single-ended environment.

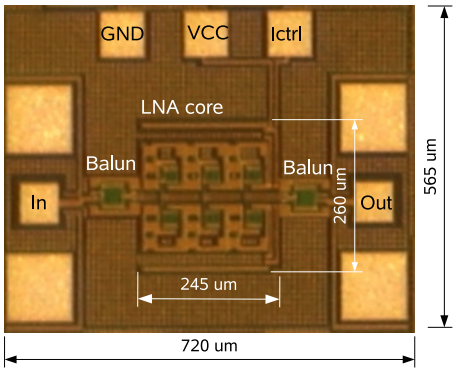

Fig. 5. LNA micrograph including auxiliary input and output test-balun transformers. The size of the LNA core is 245×260 μm^2.

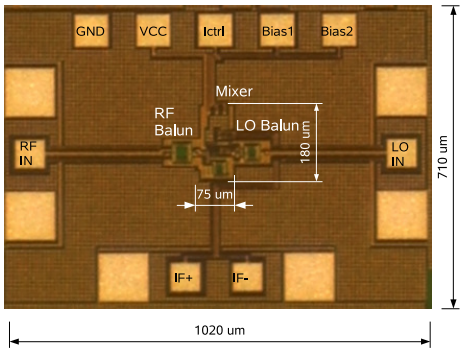

Fig. 6. Mixer micrograph with auxiliary RF and LO test-baluns at 94 GHz (left) and 46 GHz (right) next to the mixer core. The size of the Mixer core is 245×260 μm^2.

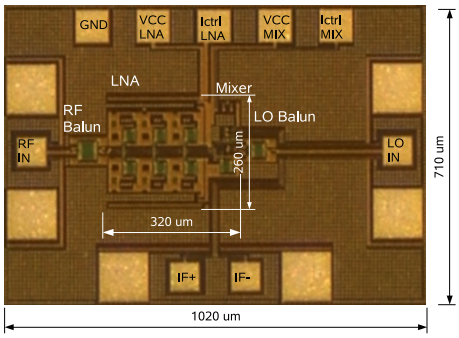

Fig. 7. Downconverter micrograph with auxiliary 94-GHz RF test-balun (left), LNA, mixer, and 46 GHz auxiliary LO test-balun (right). The size of the downconverter core is 320×260 μm^2.

from 94 GHz to 89 GHz is caused by modeling inaccuracies of the amplifier tank inductor in the initial design. The simulated noise figure is 11.3 dB excluding the losses in the baluns. No noise figure measurements were performed due to limitations in the measurement equipment.

B. Mixer characterization

The simulated and measured mixer conversion gain is shown in Fig. 9 versus the 46-GHz LO drive level at the input of the polyphase network. The measurement used a -25-dBm RF input signal at 94-GHz. The available power at the input to the polyphase network was estimated from the LO generator power, cable losses, and LO test-balun losses. Sufficient power was not available during the characterization to obtain maximum conversion gain, due to an 8-dB insertion loss in the cables and the auxiliary LO test-balun. Hence, the conversion gain was limited to 3 dB, which is in agreement with simulations for this LO drive level.

C. Downconverter characterization

The downconverter has been evaluated with the test circuit shown in Fig. 4 c). Fig. 10 shows the 2-GHz output power versus the 94-GHz input power. A small-signal conversion gain of 20 dB is obtained at 94 GHz, which corresponds to the measured 17-dB gain of the LNA and 3-dB conversion

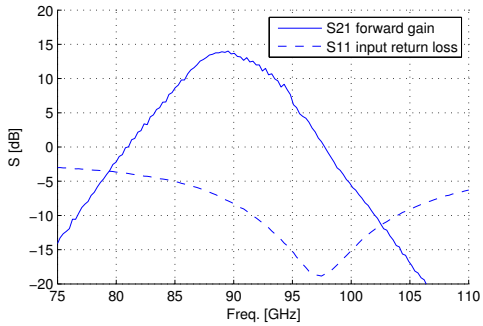

Fig. 8. Measured gain and input-return loss of the three stage differential LNA test chip including baluns (total insertion loss 4+4 = 8 dB at 94 GHz.

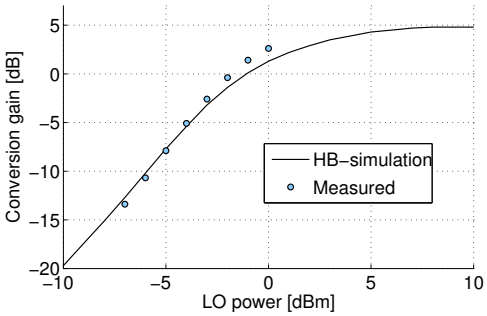

Fig. 9. Measured (circles) and harmonic balance (HB) simulation (line) mixer conversion gain as a function of LO power. RF input level - 25 dBm.

gain of the mixer. The 1-dB compression point is reached at an input level of -31 dBm.

The system noise figure was calculated from the mixer conversion gain G, and the quiescent input (N_0) and output (P_0) noise spectral densities as follows:

$$NF = P_0 - N_0 - G, \tag{2}$$

where N_0 is -174 dBm/Hz and P_0 = -137 dBm/Hz for a 2-GHz IF respectively. All noise spectral densities were measured with a spectrum analyzer. With a measured conversion gain of G = 20 dB, the single-side-band (SSB) system noise figure is 17 dB. The measured output noise level was however close to the noise floor of the available spectrum analyzer, which causes an overestimation of the system noise P_0. Based on the 11.3-dB simulated noise figure of the LNA the expected SSB cascaded system noise figure for a low IF system (where the mirror frequency falls within the LNA bandwidth) should be close to 15 dB, thus corresponding to a 12 dB DSB noise-figure in a superherodyne or zero-IF (with an additional quadrature mixer core) configuration.

V. Conclusion

A subharmonic monolithic downconverter with 20-dB conversion gain at 94 GHz has been implemented in SiGe:C process technology. Despite the use of a fully differential circuit architecture the area requirement of the complete downconverter (excluding pads) is only 0.1 μm, due to the use

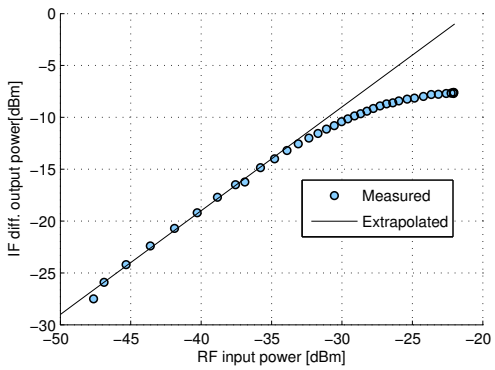

Fig. 10. Measured differential IF output signal as a function of the 94 GHz RF input power to the downconverter with an estimated 46-GHz LO level of 0 dBm at the input of the polyphase network.

of lumped components in the LNA tank and mixer polyphase networks. Future work include array receivers, as well as, extension of the design to a full quadrature (IQ) downconverter to take advantage of the wide IF bandwidth (dc-10 GHz) and the absence of LO-selfmixing problems in a wide-band zero-IF application such as a imaging system with high resolution ranging.

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