

# State of the Art in 60-GHz Integrated Circuits and Systems for Wireless Communications

*This paper discusses how broadband 60-GHz devices foreshadow the massively broadband future. The authors introduce relevant design and implementation concepts, and review emerging circuit, communication, and antenna developments.*

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**ABSTRACT** | This tutorial presents an overview of the technological advances in millimeter-wave (mm-wave) circuit components, antennas, and propagation that will soon allow 60-GHz transceivers to provide multigigabit per second (multi-Gb/s) wireless communication data transfers in the consumer marketplace. Our goal is to help engineers understand the convergence of communications, circuits, and antennas, as the emerging world of subterahertz and terahertz wireless communications will require understanding at the intersections of these areas. This paper covers trends and recent accomplishments in a wide range of circuits and systems topics that must be understood to create *massively broadband* wireless communication systems of the future. In this paper, we present some evolving applications of massively broadband wireless communications, and use tables and graphs to show research progress from the literature on various radio system components, including on-chip and in-package antennas, radio-frequency (RF) power amplifiers (PAs), low-noise amplifiers (LNAs), voltage-controlled oscillators (VCOs), mixers, and analog-to-digital converters (ADCs). We focus primarily on silicon-based technologies, as these provide the best means of implementing very low-cost, highly integrated 60-GHz mm-wave circuits. In addition, the paper illuminates character-

ization techniques that are required to competently design and fabricate mm-wave devices in silicon, and illustrates effects of the 60-GHz RF propagation channel for both in-building and outdoor use. The paper concludes with an overview of the standardization and commercialization efforts for 60-GHz multi-Gb/s devices, and presents a novel way to compare the data rate versus power efficiency for future broadband devices.

**KEYWORDS** | Analog-to-digital converters (ADCs); broadband communication; circuits and systems; CMOS integrated circuits; CMOS process; communication standards; IEEE standards; in-package antennas; integrated circuit modeling; low-noise amplifiers (LNAs); millimeter-wave (mm-wave) communication; millimeter-wave integrated circuits; millimeter-wave propagation; mixers; MOSFETs; on-chip antennas; power amplifiers (PAs); radio-frequency integrated circuits (RFICs); semiconductor waveguides; subterahertz wireless; transmission lines; voltage-controlled oscillators (VCOs); 60-GHz communication

## I. INTRODUCTION

Millimeter-wave (mm-wave) technology for the 60-GHz band is one of the most exciting opportunities for circuit, antenna, and communication system engineers over the next decade. 60 GHz is, in fact, the beginning of a trend of escalating carrier frequencies that will deliver unprecedented data rates, several tens of gigabits per second, allowing uncompressed high-definition media transfers, sensing and radar applications, and virtually instantaneous access to massive libraries of information. Consumer demand for these applications will result in millions of 60-GHz communication devices produced and sold by 2015 [1].

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Technological innovation is often spurred by federal authorities, such as the Federal Communications Commission (FCC), through the allocation of new radio spectrum bands that offer the promise of greater bandwidths and revolutionary products and applications. Indeed, today's global use of Wi-Fi and wireless local area networks (WLANs) was initially spurred by the FCC's 1985 allocation of the industrial, scientific, and medical (ISM) band, which permitted unlicensed spread-spectrum use of frequencies in the 900-MHz, 2.4-GHz, and 5.7-GHz bands [2]. At that time, communication devices at the 1–5-GHz carrier frequency bands were very expensive, and the market languished until two events happened concurrently: 1) semiconductor processes allowed high-speed, low-power wireless components to be made inexpensively and in large scale, and, 2) national spectrum regulators throughout the world agreed on common spectrum bands for global product adoption, creating a worldwide market. While memory sizes and computer clock speeds have increased by orders of magnitude over the past two decades since the FCC ISM ruling, wireless communication carrier frequencies have been bound between 800 MHz and 5.8 GHz. Today, we are at the dawn of a new age of massively broadband devices that operate at carrier frequencies of 60 GHz and above, and which handle multigigabits per second (multi-Gb/s) of data. Regulatory agencies have envisioned this opportunity for over a decade [3], [4].<sup>1</sup> As we describe subsequently, semiconductor technology appears ready to enable subterahertz wireless communications on a global scale. Just as cellular and Wi-Fi communications in the 1–5-GHz spectrum proliferated in the 2000s, today's trends indicate that wireless will soon enjoy an explosion in carrier frequencies and bandwidths, with revolutionary markets and applications for massively broadband devices.

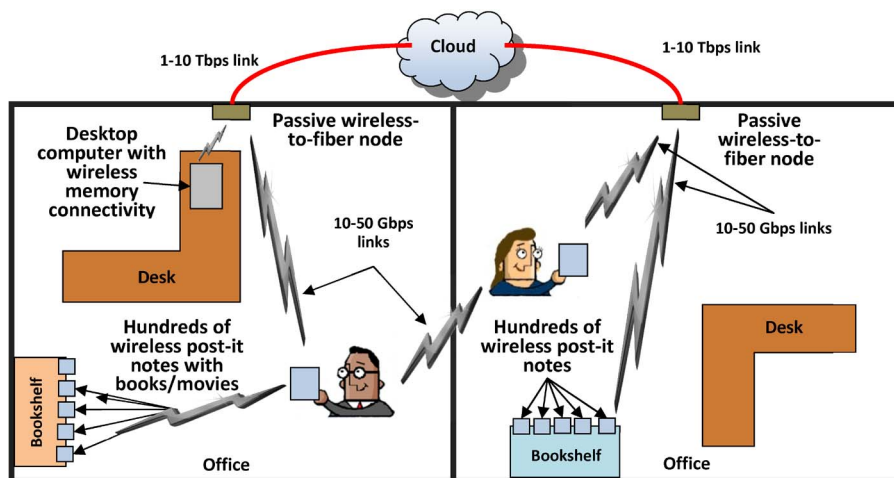
Shrinking transistor gate lengths that have enabled massive digital integration will soon make sub- and low-terahertz operation inexpensive for consumer applications, and widespread governmental agreement on spectrum allocation is likely in many bands given the properties of atmospheric absorption of electromagnetic waves, and the huge demand for bandwidth to portable end-user devices. There is already widespread agreement by federal agencies across the world on 60-GHz spectrum allocation, as several national regulatory agencies have agreed to use unlicensed spectrum at 60 GHz for wireless personal area networks (WPANs) [5], [6]. This trend is likely to continue to even greater carrier frequencies and bandwidths. When one considers the huge end-user data rates (e.g., 10–50 Mb/s) promised by nascent fourth generation (4G) cellular base station technology for a *single* mobile user, and the rapid

adoption of smartphones and Internet-ready mobile devices, it becomes clear why wireless carriers are eyeing subterahertz spectrum for rapidly deployable backhaul radios and base stations, which would facilitate more mobile bandwidth. International agreement on the 60-GHz band is the first of what is to be an exponential increase in carrier frequencies and bandwidths for wireless devices, as federal agencies across the world contemplate the allocation of more spectrum bands at frequencies above 100 GHz. At such high carrier frequencies, the bandwidths become enormous, up to tens of gigahertz, allowing massive data rates between portable devices, telecommunication infrastructure equipment, and the cloud.

Government agreement on spectrum allocation, along with early market success of portable reading and data access devices such as the Amazon Kindle and Apple iPad, portend a future where today's books and paper media, along with computer hard drives and magnetic media are replaced by the cloud or other large data repositories, and are wirelessly accessed by silicon-based electronic devices that are extremely inexpensive to fabricate. Fig. 1 illustrates a future office in the next decade, where massively broadband wireless connectivity replaces and transforms traditional paper media and magnetic data storage devices. The technical, business, and research implications of these trends toward 1) replacing paper and magnetic media and 2) ubiquitous wireless access to cloud-based data are enormous and pervasive. For example, today's wired Internet port will likely become a tetherless wireless-to-fiber connection. Book and content publishers may become web providers and purchasers of silicon chips or low-cost radio-frequency (RF) tags that contain various media content. Future researchers will have to develop entirely new strategies for circuit implementation, channel coding, data compression, interference mitigation, antenna beamforming, network addressing, and spectral usage to take advantage of massive available bandwidths, lower power requirements of devices, and the ever-present Internet. Recent inventions such as wirelessly enabled flash memory devices [7] and ultrawideband relays [201] are aimed at this future. Similarly, low-cost backhaul radio devices and massively broadband wireless relays may replace telephone poles and conventional repeaters in the telephone plant of the future. Internet data centers owned by large companies such as Google and Microsoft consume megawatts of power to cool and power entire warehouses of server computers [199]. The carbon footprint and power consumption of these data centers will be reduced as low-power wireless chip-to-chip communications replace cables, and permit novel cooling architectures and new flexibility in equipment configuration [200].

The atmospheric absorption properties of subterahertz radio spectrum offer opportunities for both long- and short-range multi-Gb/s wireless communications [8]. As shown in Fig. 2 (adapted from [4] and [8]), oxygen absorption allows stealth-like high-attenuation, short-range

<sup>1</sup>The authors acknowledge Michael Marcus for providing these references. Dr. Marcus worked for the FCC from 1988 to 1995 and proposed and directed deliberations for the ISM and 60-GHz unlicensed band policy.

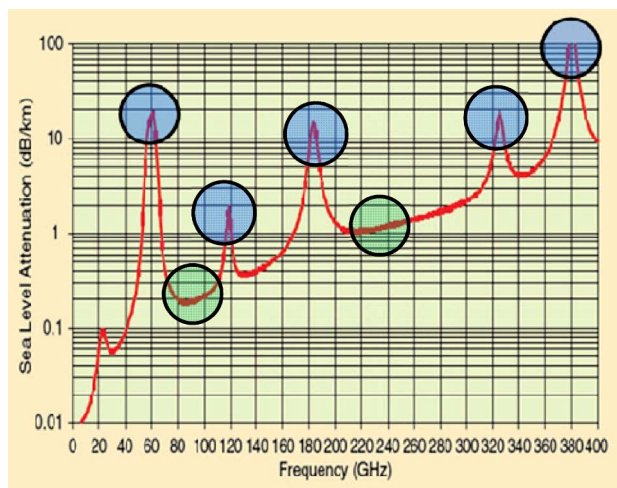


**Fig. 1.** Government allocation of high carrier frequencies and large bandwidths, along with advances in semiconductor technology, will create a future of portable and inexpensive mm-wave wireless devices that access the cloud and other large data repositories.

communications at 183, 325, and 380 GHz, making these ideal spectrum bands for densely packed electronic media that will characterize the future wireless office shown in Fig. 1. The dramatic attenuation at these frequency bands allows “whisper radio” communications, where weak signals do not propagate more than a few meters before

dropping below the thermal noise level. For communication across tens or hundreds of meters, atmospheric absorption, including rain and fog, can be the dominant physical factor for determining the correct cell size for wireless communications, with peaks in atmospheric absorption indicating those bands best used for dense, or “whisper” deployments of highest spectral frequency reuse, and low-attenuation bands being best suited for longer distance backhaul or cellular radio applications. In the future, Federal regulatory agencies around the world, having agreed upon 60 GHz as an international WPAN band, will likely approve bandwidths in excess of 10 GHz for several subterahertz bands and enable massively broadband WPAN communications and other scientific and medical applications, such as imaging. At lower attenuation bands of 77 and 240 GHz, cellular, backhaul, fiber-replacement, sensing, and vehicular radar will be viable. In addition to atmospheric and free-space attenuation, it is important to understand how wireless signals penetrate materials at these frequencies, and how the physical environment will affect propagation indoors and outdoors. We discuss RF propagation considerations in Section X.

This tutorial provides a comprehensive overview of system and circuits aspects vital to the development of mm-wave communication systems. We highlight key challenges that research and industrial communities are overcoming to create 60-GHz and future subterahertz wireless devices enabled by wireless spectrum policies and semiconductor technologies. Summaries of recent developments in 60-GHz mm-wave circuit design are provided to allow new researchers or communications and circuits practitioners to quickly assess the state of the art, and to find key works from which they can further their understanding. Section II provides an overview of the level of integration achieved for 60-GHz transmitters and



**Fig. 2.** (Modification of figure in [4] and [8].) The properties of atmospheric absorption of electromagnetic waves have resulted in widespread multigovernment agreement on spectrum allocation for short-range applications in the 60-GHz band. Agreement on allocation for short-range communications in the 120-, 183-, 325-, and 380-GHz bands (blue circles) is very likely. In coming years, the 77- and 240-GHz bands are likely candidates for widespread ISM allocations for longer range applications. When combined with highly directional antennas, attenuation for off-boresight links will be extreme at 380 GHz. See [www.mmWconcepts.com](http://www.mmWconcepts.com) for useful attenuation factors caused by rain, dust, and fog at mm-wave frequencies.

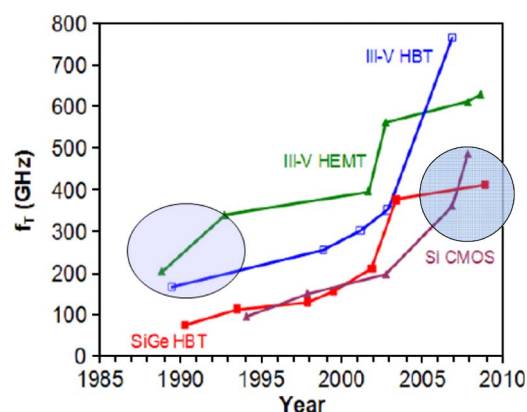
receivers. Section III discusses on-chip and in-package antennas for 60-GHz and other frequency bands, including 77-GHz vehicular radar, and also considers outdoor point-to-point antenna requirements. Sections IV–VII address circuit implementations and challenges of power amplifier (PA), low-noise amplifier (LNA), voltage-controlled oscillator (VCO), and mixer designs for 60-GHz communication systems. Section VIII discusses transmission lines and material parameter extraction as vital to the proper design and fabrication of mm-wave radio-frequency integrated circuits (RFICs). Section IX discusses high-speed analog-to-digital converters (ADCs) for 60-GHz systems. Section X describes the 60-GHz wireless channel. Section XI introduces various standards that are being developed for 60-GHz applications, including IEEE 802.15.3c, IEEE 802.11ad and the WiGig standard, WirelessHD, and ECMA 387. Conclusions are drawn in Section XII.

## II. HIGHLY INTEGRATED TRANSMITTERS AND RECEIVERS FOR 60 GHz

The mm-scale wavelength of 60 GHz (5 mm in free space, and smaller on semiconductors and substrates having permittivity greater than 1.0) allows unprecedented levels of integration of analog and microwave components such as transmission lines and disparate monolithic microwave integrated circuits (MMICs) onto a single chip or package. Several companies, including SiBEAM [9], LG, and Sony [10], have products under development that exhibit unprecedented analog integration. SiBEAM's products, which incorporate dozens of off-chip patch antennas and beam formers are complete systems-in-package [11] (including mixers, LNAs, PAs, and IF amplifiers). IBM recently developed prototypes of its 60-GHz superheterodyne transmitter and receiver codeveloped with MediaTek that include a 16-element antenna, phase shifters, and RF components on a single 6.08 mm × 6.2 mm chip for the receiver and 42 mm<sup>2</sup> for the transmitter [12]–[14].

The emergence of low-cost mm-wave devices has evolved through widespread research efforts throughout the world that began as early as the 1990s. In 1996, Niomiya *et al.* [15] utilized an InGaP/AlGaAs/GaAs high-electron mobility transistor (HEMT) process to create 15-GHz phase-locked loop (PLL), LNA, and mixer image rejector MMICs. Niomiya's pioneering ideas used expensive III-V semiconductor compounds that do not integrate easily with digital circuitry, thus their design was not a viable solution for extremely cheap, ubiquitous, and highly integrated consumer products. However, recent developments of silicon-based complementary metal–oxide–semiconductor (CMOS) processes (e.g., with transistor gate lengths below 180 nm) over the last decade now allow the implementation of these ideas for a broad consumer market.

In recent years, semiconductor manufacturers have successfully shrunk the gate length of transistors into deep



**Fig. 3.** Figure modified from [16]. In the past decade, smaller gate lengths have allowed the transit frequency  $f_T$  of silicon CMOS transistors to reach hundreds of gigahertz. The maximum frequency of operation  $f_{\max}$  is also of interest. Heterojunction bipolar transistor (HBT) III-V processes such as InP HBTs currently have  $f_{\max}$  values above 800 GHz [21]. Silicon currently has  $f_{\max}$  near 325 GHz for high-resistivity silicon-on-insulator (HR SOI) processes and near 300 GHz for CMOS and BiCMOS [a process in which both FET and bipolar junction transistors (BJTs) may be manufactured] processes [22].

submicrometer levels below 50 nm, allowing transit frequencies<sup>2</sup> of CMOS transistors to reach hundreds of gigahertz, much higher than the 60-GHz carrier frequency, thereby allowing analog microwave circuitry to be fabricated on the same circuit die and in the same semiconductor process as digital circuitry [16], [17]. Fig. 3 demonstrates how small transistor gate lengths allow high-frequency integrated circuits to be produced using low-cost silicon-based CMOS processes, rather than expensive GaAs or other III-V semiconductors. Remarkably, today's ability to integrate mm-wave analog circuits in the same process and die as high-speed digital circuitry is a by-product of Moore's Law, which has been predicting greater integration densities and computations per unit energy for digital circuitry rather than analog [17]. Fig. 3 indicates that analog components operating at hundreds of gigahertz in silicon CMOS may be commonplace beginning in 2012 (the generation lag of approximately two years of analog behind digital processes allows extra time needed to allow chip foundries to add specialized back-end-of-line (BEOL) features such as thick metal layers [17]). But there are challenges to using CMOS for mm-wave analog components, including increasingly lossy substrates with each new process generation due to higher substrate doping concentrations.

In 2002, Ohata *et al.* [18] of NEC presented transmitter and receiver circuits for use in the 60-GHz band in a III-V

<sup>2</sup>The transit frequency of a device is the frequency of unity current gain and is denoted as  $f_T$ . Another commonly referenced figure of merit is the maximum frequency of oscillation  $f_{\max}$ , which is the maximum frequency of unity power gain [20].



AlGaAs/InGaAs heterojunction field effect transistor (FET) process. They implemented a direct upconversion transmitter using separate MMICs including a 30-GHz oscillator, frequency doubler, amplitude shift keying (ASK) modulator, bandpass filter, and a PA. They also implemented a receiver out of separate MMICs including an LNA, demodulator, and postlimiting amplifier. While still not available at the time in low-cost CMOS, the work demonstrated a growing capability and interest in 60-GHz RF transceivers.

In 2004, Bosco *et al.* [19] of Applied Millimeter Wave Laboratory of Motorola Labs published results for a direct upconversion transmitter in custom and commercial MMICs in III-V processes. They demonstrated a 3.5-Gb/s link over a distance of 3 m with a bit error rate (BER) of  $10^{-8}$  using amplitude shift keying, ON-OFF keying (ASK/OOK) modulation, confirming the possibility of multi-Gb/s operation at 60 GHz. Their transmitter design incorporated a 15-GHz VCO,  $\times 4$  frequency multiplier, mixer, and a driver amplifier and medium power PA, an approach that has since been used by many researchers working in CMOS.

In 2004, Doan *et al.* [23] presented some of the earliest work in the use of CMOS for highly integrated 60-GHz systems. They demonstrated that adequate performance for 60-GHz operation in CMOS is not attained for all transceiver components if a technology node older than  $0.13\text{ }\mu\text{m}$ , such as  $0.18\text{ }\mu\text{m}$ , is used. They also demonstrated that optimal finger width for a multifinger 60-GHz transistor is approximately  $1\text{ }\mu\text{m}$ . Their results showed transmission lines would need to be extensively used in highly integrated mm-wave transmitters for 60-GHz applications due in part to their ability to clearly define current return paths, and also because on-chip mm-wave transmission lines are primarily characterized by their inductive quality factor instead of a capacitive quality factor. The result of Doan *et al.*'s [23] transmission line investigation also showed that coplanar waveguide transmission lines should be used instead of microstrip lines due to higher inductive quality factors.

In 2005, both Gunnarsson *et al.* [24] of Chalmers University of Technology and Ericsson of Sweden and Floyd *et al.* [25] of the IBM T.J. Watson Research Center presented 60-GHz designs. Gunnarsson *et al.* [24] used a  $0.15\text{-}\mu\text{m}$  pHEMT process to construct a  $5.0\text{ mm} \times 3.5\text{ mm}$  transmitter consisting of a balanced resistive mixer, IF balun, three-stage PA, and  $\times 8$  frequency multiplier local oscillator (LO) chain. They also implemented a  $5.7\text{ mm} \times 5.0\text{ mm}$  receiver that contained a three-stage LNA, image reject mixer, and an IF hybrid  $\times 8$  frequency multiplier chain. Gunnarsson *et al.*'s design represented an unprecedented level of integration for 60 GHz at the time. But higher levels of integration on chip, including the incorporation of digital baseband circuitry with analog circuitry still had not been done, as it required a silicon process such as CMOS.

In 2006, one of the first CMOS 60-GHz transmitter and receiver circuits was reported in the literature. Razavi [26] of the University of California at Los Angeles (UCLA) reported a quadrature downconverter in 130-nm CMOS that incorporated an LNA and active mixers in  $0.3\text{ mm} \times 0.4\text{ mm}$ . Alldred *et al.* [27] of the University of Toronto presented a differential downconverter in 90-nm CMOS that occupied only  $0.6\text{ mm} \times 0.48\text{ mm}$  and incorporated a two-stage LNA, double-balanced Gilbert-cell mixer, LO buffer, IF buffers, and baluns. This design had a power consumption of only 60 mW, and demonstrated the low-power potential of CMOS for 60-GHz applications. Earlier in 2005, an industry group led by Kenneth O contemplated the use of CMOS on-chip or in-package antennas for interchip (between chips) and intrachip (within a chip) communications of massively broadband data in the 10–20-GHz range [28]. These ideas were incorporated into a 60-GHz design in 2006. Reynolds *et al.* [29] of the IBM T. J. Watson Research Center demonstrated a 60-GHz transmitter and receiver in 130-nm BiCMOS that set a new benchmark for integration and incorporated an antenna in package. The transmitter successfully demonstrated a 630-Mb/s link over 10 m. Though it required nearly ten times the power of Alldred *et al.*'s design (500-mW receive and 800-mW transmit), Reynolds *et al.*'s implementation represented a very high level of integration on a  $3.4\text{ mm} \times 1.7\text{ mm}$  chip. Their design incorporated a three-stage LNA, PLL detector, low-pass filter, 8-band VCO,  $\div 32$  frequency divider, variable gain oscillator,  $\times 3$  frequency multiplier, and an IF mixer.

In 2007, Mitomo *et al.* [30] of Toshiba and Maruhashi *et al.* [31] of NEC reported 60-GHz receivers and transmitters that incorporated on-chip or in-package antennas. These designs foreshadow future systems on chip (SoC) in which many or all wired interconnects become wireless. Mitomo *et al.*'s [30] on-chip receiver design in 90-nm CMOS used only  $2.4\text{ mm} \times 1.1\text{ mm}$  excluding pads and included a one-stage LNA, downconversion mixer, and PLL synthesizer. The receiver required only 144 mW of power. Mitomo *et al.* did not measure the gain of their on-chip dipole antenna. Maruhashi *et al.* [31] reported separately packaged receiver and transceiver modules in AlGaAs/InGaAs over low-temperature co-fired ceramic (LTCC) substrate each of which occupied roughly 1–2 cm per side. The receiver incorporated a three-stage LNA downconverter and slot antenna, while the transmitter included a two-stage PA, upconverter, and slot antenna. Their use of LTCC allowed an antenna gain of 4 dBi. The high antenna gain using an LTCC substrate, when compared to typical gains for on-chip antennas over lossy CMOS substrates without compensating structures such as lenses, illustrates the difficulty of achieving high gains for antennas on CMOS.

In 2009, Dawn *et al.* [32] of the Georgia Institute of Technology presented two IF upconversion transmitters in 90-nm CMOS. The first used a single-ended transmitter

design intended for low-power applications and occupied  $1.4 \text{ mm} \times 1.5 \text{ mm}$ , while the second transmitter was a differential design for high-performance applications that occupied  $1.3 \text{ mm} \times 1.5 \text{ mm}$ . The single-ended transmitter contained a push–push VCO, LO amplifier, mixer, and three-stage PA. It had a gain of 8.6 dB, P1dB compression point of 1.5 dBm and consumed 76 mW. The high-performance differential transmitter included a cross-coupled VCO, Gilbert-cell mixer, marchand balun, and three-stage PA. It had a gain of 12.4 dB and a P1dB compression point of 4.1 dBm. In the same year, Parsa *et al.* [33] of UCLA also published a 90-nm CMOS near-complete transceiver that occupied  $0.19 \text{ mm}^2$  and consumed only 36 mW as a receiver and 78 mW as a transmitter. Their design was based on a new “half-RF” architecture that allowed a 30-GHz LO to be used to convert a baseband signal to 60 GHz.

The potential of 60-GHz links to achieve data rates as high as 6 Gb/s over distances of up to 2 m was demonstrated by Tomkins *et al.* of the University of Toronto in 2009 [34]. Tomkins *et al.* relied on a direct-conversion architecture that will likely become popular for inexpensive 60-GHz devices. Researchers and companies that use direct-conversion architectures will need to develop expertise and fabrication experience to understand the advantages and disadvantages over superheterodyne designs. Direct conversion eliminates the image frequency challenge of superheterodyne receivers and can be implemented in less area and more cheaply. However, it has the disadvantage of increased susceptibility to second-order harmonics, reduced isolation which can lead to self-jamming, and places more stringent requirements on RF filters used to reject adjacent channels [35]–[37]. As the LO frequency of a mm-wave system increases, the direct-conversion architecture will also face difficulty in attaining high quadrature accuracy (i.e., maintaining precise  $90^\circ$  phase shifts between quadrature components).

In May 2010, IBM and MediaTek demonstrated 60-GHz prototype transmitter and receiver chips in SiGe BiCMOS8HP each of which included a planar, 16-element antenna for use with the IEEE 802.15.3c standard [12]–[14]. The receiver chip achieved 72-dB gain, consumed 1.8 W from 2.7 V, and occupied an area of  $6.08 \text{ mm} \times 6.2 \text{ mm}$ . The transmitter chip achieved 40 dB of gain, occupied an area of  $44 \text{ mm}^2$ , and consumed 3.8–6.2 W. These chips demonstrate that 60-GHz products are on the verge of commercial viability.

Table 1 summarizes results achieved by the research community in 60-GHz radio design.

### A. Tradeoffs Between Simplicity and Performance

Subterahertz wireless will find applications both indoor and outdoor for short-range WPANs and longer range uses such as mm-wave backhaul between base stations. The maximum range envisioned for 60-GHz systems for WPANs is several meters, whereas outdoor systems will

likely be used for links up to 1 km. A more nuanced view of WPAN distinguishes two classes of devices that will occupy the 60-GHz WPAN product space. The first class is high-performance devices capable of operating in non-line-of-sight (NLOS) conditions such as around corners and past obstacles, and a range up to 10 m. The second class will be occupied by lower performance devices that only operate in line-of-sight (LOS) conditions with a range of a few meters (e.g., 3 m maximum), and will offer consumers a lower price entry point into the 60-GHz product space. Architecturally, the higher performance devices will be characterized by antenna arrays and more sophisticated baseband processors to implement beam-steering algorithms, while lower performance devices will contain fewer antennas (and thus offer lower directionality and gain) and simpler baseband processors that implement either simplified beam-steering algorithms or no beam-steering algorithms at all.

For example, in October 2010, Valdes-Garcia *et al.* [13] presented a 16-element beam-steering 60-GHz transmitter for use with the IEEE 802.15.3c standard. The complex multielement design was chosen to overcome challenges associated with the 60-GHz channel, including higher path loss compared to lower frequency systems (e.g., Wi-Fi) and more severe shadowing due to obstructions such as people walking around. Although the transmitter achieved a high gain of 40 dB, it required substantial area at  $44 \text{ mm}^2$ , substantial processing, and complex 1 : 16 power splitting to distribute a signal to all elements in the array. Work in [13] confirms that such hardware complexity is necessary to create radio links further than several meters as individual PAs cannot provide adequate output powers to attain the maximum power density of  $18 \text{ } \mu\text{W}/\text{m}^2$  as allowed by the FCC. Valdes-Garcia *et al.* [13] also show that highly complex systems, especially when implemented in CMOS or SiGe, should focus on antenna arrays, which necessitates beam steering, as opposed to on-chip power combining coupled with single low directivity antennas, which is a less efficient and more space intensive solution to attaining high range.

In 2007, Lee [38] provided an example of a contrasting low-complexity system that incorporated only a single antenna as opposed to the 16-element array used by [13]. This device was capable of 1.5-Gb/s transmissions up to 2 m, while Valdes-Garcia *et al.* [13] attained up to 5.3 Gb/s at a 4.5-m distance [14]. Compared to the  $44 \text{ mm}^2$  required by [13], this chip required only  $3 \text{ mm}^2$  of area and consumed only 25 mW of direct current (dc) power compared to 6.2 W required by [13].

When used for backhaul applications, 60-GHz and higher frequency mm-wave systems will need to consider outdoor obstructions such as foliage and weather, and antenna movements caused by wind and mechanical vibrations. The Doppler frequencies in outdoor channels will be much greater than for indoor WPAN applications, due to wind speeds, moving tree branches, and vehicular

**Table 1** The Level of Analog Integration for 60-GHz Devices Has Increased Dramatically Over the Past Decade

Reference, Year	TX	RX	Output Power	Gain	Noise Figure	IIP <sub>3</sub> , IP1dB, <sup>a</sup> etc	Bandwidth	Power Cons.	Size	Process
[31], 2000	X	X	PA: 12 dBm, Total TX: 10 dBm	PA: 12 dB, LNA: 18 dB, Complete RX: 10 dB	LNA: 5 dB	N/A	Complete TX/RX: 59 – 60 GHz	N/A	~ 2 x 1 cm <sup>2</sup>	Separate III-V MMICs on LTCC
[18], 2002	X	X	PA: 14 dBm, Total TX: >10.6 dBm	PA: 12 dB, LNA: 18 dB	N/A	N/A	LNA: 59 – 64 GHz, TX: 1.74 GHz	N/A	TX + RX: 82 mm x 53 x 7 mm <sup>2</sup>	Separate III-V MMICs
[19], 2004	X	X	10 dBm to antenna	LNA: 33 dB	Total TX: 6.5 dB	N/A	Total RX: 5 GHz	N/A	N/A	Separate III-V MMICs
[25], 2005	X	X	PA: 16.2 dBm, VCO: -8 dBm	LNA: 14.7 dB, RX w/o LNA: 18.6 dB,	LNA: 4.5 dB, RX w/o LNA: 14.8 dB	RX w/o LNA IP1dB: -17 dBm, LNA P1dB: -20 dBm	VCO: 65.8-67.9 GHz	LNA: 10.8 mW RX w/o LNA: 302 mW, PA: 270 mW	LNA: 0.9 x 0.6 mm <sup>2</sup> , RX w/o LNA: 1.9 x 1.65 mm <sup>2</sup> , PA: 2.1 x 0.8 mm <sup>2</sup>	Separate 0.12 $\mu$ m SiGe Bipolar MMICs
[24], 2005	X	X	Total TX: 3.7 $\pm$ 1.5 dBm	Total RX: 7.1 $\pm$ 1.5 dB, Total TX: 5.2 dB	Total RX: 10.5 dB	RX IIP <sub>3</sub> : -11 dBm, -19 IP1dB, TX: OP1dB: 0 dBm	TX: 54-61 GHz, RX: 59.5 – 64.5 GHz	Total TX: 820 mW, Total RX: 990 mW	Total RX: 5.7 x 5.0 mm <sup>2</sup> , Total TX: 5.0 x 3.5 mm <sup>2</sup>	Separate GaAs pHEMT MMICs
[26], 2006		X	N/A	RX: 28 dB Voltage Gain	Total RX: 12.5 dB	Total RX IP1dB: -22.5 dBm	57-64 GHz	Total RX: 9 mW	0.3 x 0.4 mm <sup>2</sup> excluding pads	Single 0.13 $\mu$ m CMOS chip
[27], 2006		X	N/A	Total RX: 16 dB	RX: <7 dB	Total RX P1dB: -21 dBm	58.5 – 60.5 GHz	60 mW	0.6 x 0.475 mm <sup>2</sup>	Single 90 nm CMOS chip
[47], 2006		X	N/A	LNA: 18 dB, Mixer: 10.8 dB, Total RX: 28 dB	LNA: 6.8 dB, Mixer: 14 dB (simulated)	Total RX OP1dB: -1.6 dBm	57-64 GHz	LNA: 66 mW, Mixer: 21 mW	0.8 mm <sup>2</sup>	Single SiGe:C BiCMOS chip
[29], 2006	X	X	Total TX: 15-17 dBm	RX: 38-40 dB, TX: 34-37 dB	Total RX: 6 dB	RX IIP <sub>3</sub> : -30 dBm, TX OP1dB: 10-12 dBm	55-64 GHz, 1.5 GHz VCO tuning	RX: 500 mW TX: 800 mW	Total RX: 3.4 x 1.7 mm <sup>2</sup> , Total TX: 4 x 1.6 mm <sup>2</sup>	Single 0.13 $\mu$ m SiGe BiCMOS chip
[30], 2007		X	N/A	LNA: 13.7 dB,	LNA: 7.8 dB (simulated)	N/A	VCO: 61.2 – 64.4 GHz, PLL: 1.7 GHz	LNA: 39 mW, Total RX: 144 mW	2.4 x 1.1 mm <sup>2</sup> without pads	Single 90 nm CMOS chip
[32], 2009	X		PA: 2.1 dBm, Total TX: 5.7 dBm	PA: 17 dB, Total TX: 8.6 dB	N/A	PA OP1dB: 2.1 dBm, Total TX OP1dB: 1.5 dBm	VCO: 48.5 – 55 GHz, Total TX: 57 – 65 GHz	PA: 44 mW, Total TX: 76 mW	1.4 x 1.5 mm <sup>2</sup>	Single 90 nm CMOS chip
[32], 2009	X		PA: 8.4 dBm, Total TX: 8.6 dBm	PA: 17 dB, Total TX: 12.4 dB	N/A	PA OP1dB: 8.4 dBm, Total TX OP1dB: 4.1 dBm	VCO: 53.4 – 55.7 GHz, Total TX: 57 – 65 GHz	PA: 54 mW, Total TX: 112 mW	1.3 x 1.5 mm <sup>2</sup>	Single 90 nm CMOS chip
[33], 2009	X	X	Total TX: -7.2 dBm	Total RX: 19.8 – 22 dB	Total RX: 5.7 – 7.1 dB	Total RX IP1dB: -27.5 dBm, Total TX OP1dB: -8.6 dBm	N/A	Total RX: 36 mW, Total TX: 78 mW	Total RX: 0.5 x .37 mm <sup>2</sup> active area, Total TX: 0.495 x 0.425 mm <sup>2</sup> active area	Single 90 nm CMOS chips (separate TX & RX)
[34], 2009	X	X	Total TX: -0.7 dBm	Total RX: 8.9 dB	Total RX: 5.8 dB	Total RX IP1dB: -22 dBm	Total TX: 50 – 66 GHz	Total TX + RX: 232 mW	Total TX+RX: 1.28 x 0.81 mm <sup>2</sup>	Single 65 nm CMOS chip (combined TX and RX)

<sup>a</sup> IIP<sub>3</sub> is the input referred third order compression point, and is the extrapolated input power at which the third order harmonic overtakes the first order harmonic in the output. IP<sub>1dB</sub> is the input referred 1 dB compression point, and is the input power at which the output power is 1 dB below expected output power based on extrapolation of output power with input power at low input powers.

traffic, thus requiring smaller data frame sizes and more frequent equalization and antenna beam-steering updates. The backhaul propagation environment at 60 GHz and above is not well understood today, but rain and fog will have a dramatic impact on the channel attenuation, as is clear when indoor 60-GHz measurements such as those conducted by Xu *et al.* [39] are compared to outdoor measurements in clear and adverse weather conditions [40], [41]. Work in [41] found that outdoor 60-GHz links can experience as much as 3.9 dB of attenuation due to rain over a link distance of less than 200 m. Measurements in

[40] show the need for improved understanding to combat deep fading in the outdoor channel, as mm-wave links can be interrupted or experience signal fades as deep as 46.7 dB due to antenna movement as slight as several centimeters. An advantage that backhaul and cellular systems will enjoy over short-range WPAN is that the radio fixture size will need to be large enough for pole or building mounting, and will have robust power supplies and room for circuitry that can support high-power transmitter amplifiers, sophisticated signal processing, and temperature control. The relatively large radio fixture will also

allow electrically large antenna apertures to be built onto the casing, thereby supporting extremely high gain, steerable planar antenna arrays in both horizontal and vertical directions.

Regardless of whether mm-wave communications systems are implemented indoors or outdoors, short range or long range, these new systems will use highly directional antennas to an extent never before seen in terrestrial communications. New protocols for finding and locking the antennas between desired transceivers are required, since highly directional antennas will appear “blind” to other transceivers when pointing in a single direction. Rapidly adjustable beamwidth antennas will be used to scan the many possible signal paths, before locking into a high beam mode to close the link for reliable high-speed communications.

### B. Link Budgets for Wireless Transceivers at 60 GHz

To determine the usability of RF transceivers, a link-budget analysis and measurement is required to ascertain acceptable communication distances. At short distances (millimeters or centimeters of separation), the linearity of the receiver dictates communications performance, whereas the noise figure of the receiver and transmitter dictates coverage range. Several researchers have presented measured or theoretical link budget data for the 60-GHz band, including [34], [39], [42]–[45], and [184]. The signal power  $P_{RX}$  at the input of a receiver, in dBm is given by [46]

$$P_{RX} = P_T - PL_d + G_T + G_R \quad (1)$$

where  $P_T$  is the transmitted power in dBm,  $PL_d$  is the path loss in decibels for the transmitter–receiver separation distance  $d$ ,  $G_T$  is the transmit antenna gain in decibels, and  $G_R$  is the receive antenna gain in decibels. The noise power in dBm at the input to a receiver is given by [46]

$$P_{noise} = 10 \log(kT_{syst}) + 10 \log(B) + NF_{RX} \quad (2)$$

where  $10 \log(kT_{syst})$  is equal to  $-174$  dBm/Hz for a system temperature of  $17^\circ\text{C}$ .  $NF_{RX}$  is the noise figure of the receiver in decibels, and  $B$  is the bandwidth of the signal in hertz. If we assume a 1-m link with 68 dB of free space path loss (through Friis free space formula at 60 GHz), using unity gain antennas, and a transmit power of 10 dBm, then the received power is given by

$$P_{RX} = 10 \text{ dBm} - 68 \text{ dB} + 0 + 0 = -58 \text{ dBm}.$$

Further, if we assume a receiver LNA noise figure of 6 dB, and an RF bandwidth of 1.25 GHz, then the noise

power at the receiver front end is given by

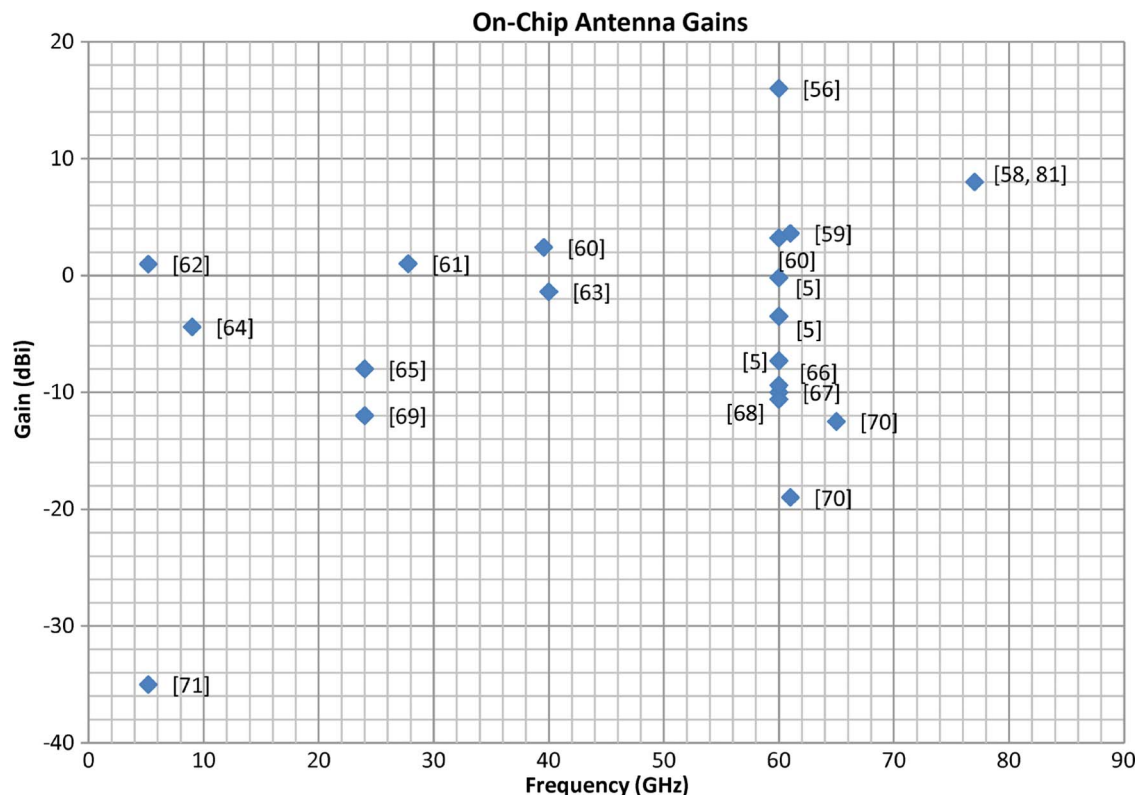
$$\begin{aligned} P_{noise} &= -174 \text{ dBm/Hz} + 10 \log(1.25 \text{ GHz}) + 6 \text{ dB} \\ &= -77 \text{ dBm}. \end{aligned}$$

This 1-m link would have a signal-to-noise ratio (SNR) of  $-58 \text{ dBm} - (-77 \text{ dBm}) = 19 \text{ dB}$  (ignoring implementation losses in the circuits). As discussed subsequently, the antenna and propagation characteristics greatly affect the link budget. It is important to note that SNRs of 10.7, 16.7, and 21.7 dB are needed for quadrature phase-shift keying (QPSK), 16-quadrature amplitude modulation (QAM), and 64-QAM transmissions, respectively, to obtain end-user BERs of  $10^{-11}$  after Reed–Solomon decoding [42]. We see that 1-m links can easily support multi-Gb/s for QPSK and 16-QAM modulation schemes using unity gain antennas. Even greater distances are achieved with phased array antennas. The recently publicized 60-GHz prototype receiver chip by IBM and MediaTek is claimed to have a gain of 72 dB and a noise figure of approximately 7.4 dB [12], [14]. This provides for reliable 60-GHz links at rates of 4 Gb/s over distances greater than 3 m using only 10 dBm of transmitted power. For outdoor backhaul and cellular applications, (1) can be modified to add the additional path loss due to atmospheric absorption fog, or rain. When considering the use of outdoor high gain antennas with 30–50 dB of gain, it is easily seen that coverage distances of over a kilometer are viable for multi-Gb/s data rates. Section X provides additional insights into propagation considerations for the link budget. For example, as shown in [41], millimeter-wave rain attenuation models may be used reliably for outdoor propagation scenarios, making outdoor cellular coverage predictions relatively simple.

### III. ON-CHIP ANTENNAS

The possibility of integrating and combining antennas directly on chip is one of the least explored areas for future subterahertz communication devices. While radiation losses are extremely large due to substrate absorption and conductive currents, the removal of all connections between RF circuits and the antenna offers substantial cost reduction and flexibility in circuit design for low-cost consumer electronics [5], [28]. Today’s conventional thinking hardly justifies on-chip antennas for low-power consumer devices due to high losses and low gains in the absence of compensating structures such as dielectric lenses. Indeed, typical on-chip antennas have only 10% efficiency and negative gain. However, if very high gain antenna structures can be designed and fabricated on chip in submillimeter sizes (e.g., by using frequency selective surfaces [48] or highly directional antennas such as Yagi or rhombic antennas [5]), then the benefits of extreme cost





**Fig. 4.** Reported results for on-chip antennas.

reduction and improved design flexibility may outweigh the use of more efficient off-chip antennas that require more expensive and complex manufacturing processes. As carrier frequencies and bandwidths move to the sub-terahertz regime, on-chip antennas may also be justified as a means of replacing metal interconnects between chips on a printed circuit board, since metal leads become unusable at vast bandwidths and carrier frequencies.<sup>3</sup> In addition to on-chip antennas, other promising interconnect mechanisms that will replace today's metal pins for massively broadband signals on subterahertz carriers include on-chip waveguides and through-silicon-via (TSV) waveguides [49]. Though we focus on on-chip antennas in this paper, a solution for replacing metal interconnects in today's chips must be discovered, as un-equalized metal interconnects are generally not operable past 20 GHz in passband bandwidth [50]. Successful implementation of on-chip antennas will be beneficial for a host of applications, including highly integrated transceiver design and spatial power combining for 60-GHz and

higher frequency mm-wave systems (e.g., see the recent work by Atesal *et al.* [51]).

On-chip antennas have been reported for a vast range of frequencies, from 0.9 GHz [54] to 77 GHz [55]. Fig. 4 and Table 2 give an overview of some of the results that have been reported in the literature.

The best on-chip antenna gains for single antennas have relied on the placement of dielectric lenses below or above the antenna (sometimes called a resonator). This technique has the effect of reducing energy lost to substrate modes [58], [60], [72]. Substrate modes allow waves of certain frequencies to propagate through the bulk silicon substrate, based on the chip's material properties and physical dimensions. A dielectric lens above the antenna reduces the difference in the dielectric constants above and below the antenna (without the lens above the antenna, the dielectric constant below the antenna is that of the silicon substrate, while that above is of air) [72], [73]. This lens has the effect of increasing the antenna's radiation intensity away from the substrate and reducing energy lost into the substrate. The lens above the antenna should be constructed of a material with a dielectric constant equal to or larger than that of the substrate that supports the antenna (e.g., a dielectric lens of silicon dioxide ( $\epsilon_r \approx 4$ ) above an antenna on doped silicon ( $\epsilon_r \approx 12$ ) will not substantially improve

<sup>3</sup>This is due to skin effect forcing more current to flow through the substrate with increasing frequency, in addition to the inverse proportionality of a metal's surface resistance to the penetration depth [52], [53]. As frequencies go to the terahertz range, massive bandwidths cannot be carried by typical metal leads.

Table 2 Summary of On-Chip Antennas From the Literature

Reference	Gain	Frequency	Type and Process
[71]	-35 dBi	5.2 GHz	Folded Dipole, 130 nm CMOS
[59]	3.6 dBi	61 GHz	Dipole, 150 nm pHEMT
[57]	8 dBi	77 GHz	Dipole over thin substrate with Dielectric Lens, 130 nm CMOS
[65]	-8 dBi	24 GHz	Dipole, 130 nm CMOS
[62]	0.96 dBi	5.2 GHz	Semi-Helical over High Resistivity Si CMOS substrate
[67]	-10 dBi	60 GHz	Yagi, 180 nm CMOS
[68]	-10.6 dBi	60 GHz	CP microstrip, 130 nm CMOS
[61]	1 dBi	27.78 GHz	Cylindrical Dielectric Resonator, IBM SigeHP5
[63]	-1.4 dBi	40 GHz	Wire Bond, SiGe CMOS
[64]	-4.4 dBi	9-10 GHz	Slot, 130 nm CMOS
[66]	-9.4 dBi	60 GHz	Triangular monopole, 130 nm CMOS
[69]	-12 dBi	24 GHz	Zigzag Dipole, 130 nm CMOS
[60]	2.4 dBi	39.56 GHz	Dipole with Dielectric Resonator
[60]	3.2 dBi	60 GHz	Rectangular Dielectric Resonator
[58]	8 dBi	77 GHz	Dipole + Si Lens, IBM 8HP 130 nm CMOS
[56]	16 dBi	60 GHz	Spiral Inductor Array, Silicon
[70]	-19 dBi	61 GHz	Inverted F, BEOL process <sup>b</sup>
[70]	-12.5 dBi	65 GHz	Quasi Yagi, BEOL process
[5]	-7.3 dBi <sup>c</sup>	60 GHz	Dipole
[5]	-3.5 dBi	60 GHz	Yagi
[5]	-0.2 dBi	60 GHz	Rhombic

<sup>b</sup>Back-end-of-line (BEOL) refers to the processing steps of chips in which metallization layers are added.

<sup>c</sup>These values are for simulated structures. Measurements will be released in an upcoming paper.

performance).<sup>4</sup> A dielectric lens below the chip releases and radiates the energy trapped as substrate modes in the silicon out the back of the chip [57], [58]. But these techniques have the disadvantage of being nonstandard in foundry production processes [64], and the dielectric lens above the chip substantially increases the form factor of the chip, as seen in [72] and [60]. Several ideas, such as the use of frequency selective screens and metamaterials as suggested by Ragan *et al.* [48], should also be investigated to reduce loss to silicon substrate modes. Another possibility being explored is the use of symmetric electromagnetic bandgap structures, as described by Llombart *et al.* [74].

A single dipole antenna is not adequate to meet robust link budget requirements for 60 GHz. For a worst case scenario over several meters with a deep signal fade, the combined gains of the transmitter and receiver antenna can reach as high as 71 dB for an acceptable link margin [44]. 60-GHz devices require the use of antenna arrays on chip or in package to meet link margin requirements. For example, IBM and MediaTek's recently released 60-GHz

prototype receiver chip incorporated 16 antennas and achieved a gain of 72 dB, illustrating the benefit of an antenna array [12], [14]. SiBEAM uses an outboard package containing 36 antennas [11]. Arrays offer the best means of attaining a tight antenna beam pattern with the most flexibility for steering the antenna and in creating a system design. The disadvantages of using arrays are the increase in area and power required for many antenna elements, and the added implementation of beam-steering protocols, although higher frequency bands will make on-chip arrays much smaller and thus easier to integrate. The area of an antenna array is determined by the area of each element and the element spacing. Table 3 summarizes sizes reported in the literature for on-chip antenna elements that may be considered in an array.

On-chip antennas on doped silicon substrates generally have low efficiencies of about 10% [5] for three reasons. First, the on-chip antenna "prefers" to radiate into the lossy chip substrate due to the higher dielectric constant of the substrate than that of air. Second, the substrate thickness approximates a resonant cavity that may have a resonant frequency near the mm-wave band of interest if substrate thinning is not used. This problem is exacerbated

<sup>4</sup>The lens above the antenna is not doped silicon so the propagation loss through it is low.

**Table 3** Dimensions of On-Chip Antennas Reported in the Literature

Reference	Antenna Type	Dimensions or Area
[71]	5.2 GHz Folded Dipole, -35 dBi	1.33 mm x 0.7 mm
[59]	61 GHz Modified Dipole, -36 dB TX Gain	0.9 mm <sup>2</sup>
[65]	24 GHz Dipole, -8 dBi	0.5 mm x 1.5 mm
[67]	60 GHz Yagi, -10 dBi	1.1 mm x 0.95 mm
[68]	CP microstrip, -10 to -7 dBi	1.4 mm x 1.4 mm
[61]	27.78 GHz DRA (Dielectric Resonator Antenna)	2 mm x 2.3 mm x 0.93 mm

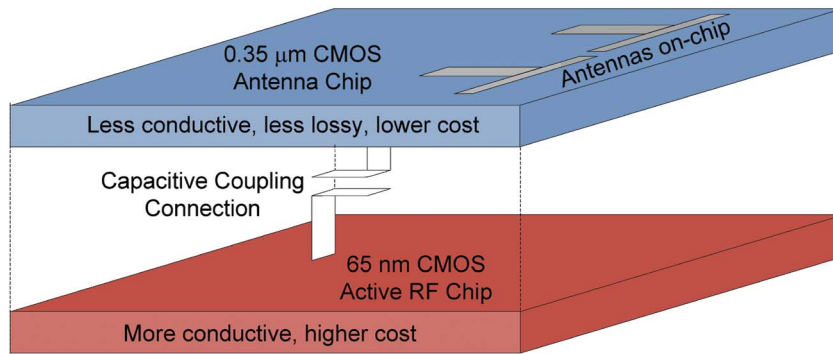
by the high effective loss tangent of the substrate, which results in wide resonant bandwidth of the chip substrate. Third, the high doping concentration of the substrate (especially in modern processes) which is used to avoid latch-up of digital components results in rapid attenuation of RF waves that enter the chip substrate. For this reason, other antenna implementations that are as close to the chip as possible while maintaining acceptable performance are of interest to the RFIC community. For example, *in-package antennas* place the antenna elements in the package surrounding the chip, and *stacked chips* with feed-through vias would allow an old, high resistivity technology process to house the antenna elements and simple ON-OFF switching diodes, while the RF electronics would be implemented on a more modern technology below the antennas, themselves. The low efficiencies of on-chip antennas also makes their characterization especially difficult. Most on-chip antennas are characterized on commercial probe-stations, where large pieces of metal can

result in multipath scattering and reflections that can badly degrade measurements of on-chip antenna patterns. Therefore, techniques to improve reliability and accuracy of on-chip antenna pattern measurements, such as those developed in [203], should be used and refined.

Although higher cost, in-package antennas can currently achieve much higher efficiencies than on-chip antennas due to their distance from the lossy chip substrate. Popular package technologies include Teflon ( $\epsilon_r = 2.2$ ), LTCC ( $\epsilon_r = 5.9\text{--}7.7$ ), fused silica ( $\epsilon_r = 3.8$ ), and liquid crystal polymer (LCP,  $\epsilon_r = 3.1$ ). In general, the best gain-bandwidth product will be obtained using materials with low dielectric constants [6]. There are a number of challenges to using in-package antennas as reported in 2010 by Kam et al. [75], including detuning of antennas due to the presence of packaging materials, difficulty in meeting mechanical and electrical reliability requirements, antenna interference from heat sinks, and possibly the high expense of packaging processes. LCP is currently viewed as

**Table 4** Summary of 60-GHz In-Package Antennas From the Literature

Reference	Gain	Efficiency	Frequency	Type & Process
[77]	11 dBi	94 % (estimated)	59 – 65 GHz	Slot antenna in cavity-down ceramic ball grid array LTCC
[75]	5 dBi/element	Not Reported	58.32 – 64.8 GHz	16 patch antennas in ball grid array
[78]	6 dBi	Not Reported	58.3 – 59.5 GHz	Yagi, LTCC Ball Grid Array
[79]	6 dBi	93 %	60.6 GHz – 62.9 GHz	Yagi, LTCC Cavity down ball grid array
[75]	~ 2 dBi/element	Not Reported	58.32 – 64.8 GHz	16 patch antenna in LCP surrounded by glass laminates
[80]	16.8 dBi package gain	Not Reported	57 – 64 GHz	4 x 4 circular polarized patch in LTCC with aperture coupling
[81]	7 dBi	Not Reported	56 – 67 GHz (for Broadside Radiation)	Patch antenna array on thin film micromachined substrate



**Fig. 5.** Advanced interconnect technology, such as capacitive coupling, allows much higher frequency operation than standard wire bond technology, and allows more flexible connections for better component integration. The science of coupling connections is well developed by [83]. Here, we suggest such a technique to interface an antenna chip fabricated on a mature, lower cost, less doped substrate with an active 60-GHz mm-wave RF chip.

a good low-cost method of implementing in-package antennas [75].

Both on-chip and in-package antennas will need to be very directive for long-range WPAN applications (for links up to 10 m in NLOS conditions). This will also be a characteristic of antennas used for outdoor mm-wave point-to-point applications such as mm-wave backhaul and future cellular systems. Millimeter-wave cellular and backhaul will also benefit from multiple-input-multiple output (MIMO) [76]. Table 4 summarizes literature results for 60-GHz packaged antennas. In-package antennas are more efficient and have higher gains than lower cost on-chip antennas.

Advanced packaging technologies provide the possibility of integrating antennas and other mm-wave components in more flexible ways than on a single chip. This depends on the type of interconnects used in the package. Popular interconnect technologies include flip chip connections [82], which facilitate stacked structures and coupling connections that can reach higher frequencies than standard wire bonds [83]. Coupling connections may come in many forms, and are designed using capacitive connections between different components in a package. This technique may be especially useful for integrating multiple chips into a single package. For example, an antenna may be fabricated on a mature, low-cost semiconductor process technology (e.g., 0.18- or 0.35- $\mu\text{m}$  CMOS) with lower substrate doping than the newest process technology. This may then be capacitively coupled to a more advanced process chip which contains active mm-wave components such as a 60-GHz PA. The antenna would benefit from the older technology's lower doping concentration and higher resistivity, which results in a less conductive, less lossy substrate than on a newer process technology. If an antenna array is used, simple low-speed active switches (e.g., diodes) could be integrated onto the antenna chip with phased passive feedlines to perform element tuning, phase shifting, and beam steering. This is illustrated in Fig. 5.

#### IV. POWER AMPLIFIERS

The RF PA stage used in 60-GHz transmitters is key to establishing the link budget and the power requirements (and hence battery life) of a device. The PA of a traditional wireless system is the most power hungry device. PAs for 60 GHz must be designed with adequate linearity for the specific modulation scheme used, while delivering adequate output power and efficiency for long battery life. These goals are made challenging by the low-voltage supplies of modern deep submicrometer CMOS, and the large dynamic ranges required for certain modulation schemes such as orthogonal frequency division multiplexing (OFDM).

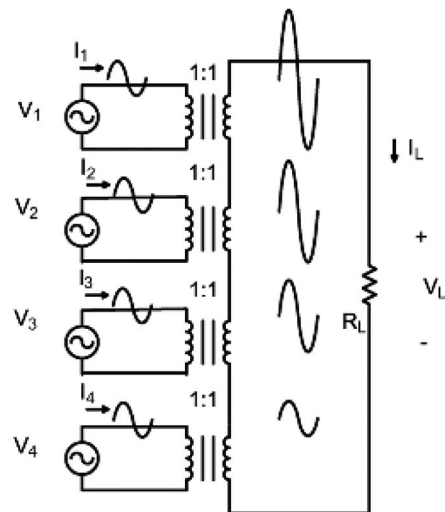
The large dynamic range of the output power required in certain M-ary modulation schemes such as OFDM complicates PA design as it requires highly linear operation. The amplifier spends a substantial portion of each cycle below saturation where the amplifier is less efficient (operating an amplifier below its saturation output power level is known as “backoff”) [85]. The linearity requirements are due in part to the peak-to-average power (PAPR) ratio of the particular modulation choice (see Table 15 in Section XI). Today's 60-GHz devices are considering both OFDM and single-carrier frequency domain equalization (SC-FDE) modulation and multiple access approaches. SC-FDE enjoys a smaller PAPR, implying that a less linear PA is required. There are many potential ways of improving the efficiency of linear or near-linear PAs, including the Doherty architecture [86], envelope tracking [87], [88], self-biasing [89] (which also can improve device lifetime), and power combining [88], [90]. Certain very inexpensive 60-GHz devices for low spectral efficiency applications may also achieve high PA efficiency by using a more efficient switching amplifier rather than a linear amplifier. The efficiency of mm-wave PAs is degraded by parasitic elements in active and passive components. Proper design of transmission line elements, discussed in Section VIII, will improve efficiencies of these designs.



The Doherty architecture improves efficiency by combining in parallel the outputs of a main large amplifier and a smaller auxiliary amplifier [86]. This design can also improve PA linearity [92]. For low input voltage levels the main amplifier operates near saturation (and hence with high efficiency) while the auxiliary amplifier is off. As the input voltage increases, the auxiliary amplifier turns on while the main amplifier continues to operate near saturation. The challenges associated with this design involve careful biasing and matching, including proper passive element design for power splitting and combining and designing the input impedances of the primary and secondary amplifiers. CMOS Doherty PAs at lower frequencies, in particular, have been difficult to integrate due to the long transmission lines required to correctly combine the outputs of the main and auxiliary amplifiers [86]. But this challenge is significantly reduced in the mm-wave region, where shorter wavelengths reduce the size of required transmission lines on a chip. Results for the Doherty architecture include [86] which shows a 14% power added efficiency (PAE)<sup>5</sup> at 2.4 GHz. The only reported Doherty implemented for use with 60 GHz achieved a 3% PAE [92]. Thus, substantial work remains to improve this design for mm-wave CMOS devices if it is to be used for purposes of improved efficiency as opposed to improved linearity.

The Doherty amplifier technique is an example of how transmission lines are used to provide appropriate impedances and matching circuitry to allow for power combining. In this instance, the transmission lines combine the outputs of two (or more) amplifiers. At mm-wave frequencies, approaches such as on-chip coupling transformers used by Liu *et al.* [90] at 2.4 GHz may also be used on chip for power combining. Fig. 6 demonstrates this technique, which uses multiple sub-PA stages that are coupled to provide in-phase power amplification [90]. The outputs of four sub-amplifiers are combined in-phase to deliver a large output power that is not limited by the voltage swing limitations of the smaller sub-amplifiers.

The Doherty technique and the technique presented by [90] are both examples of on-chip power combining. Off-chip power combining is also possible through correctly phased on-chip antennas. This technique was used as early as 1994 by Sanchez-Hernandez and Robertson [93] for 60-GHz Gunn Diode oscillators in mm-wave backhaul applications at 62.5/63.5 GHz. More recently in 2008, Emrick and Volakis [94] explored this technique with three antenna topologies including spiral, edge-bow tie, and half-circle printed antennas, each characterized individually and in an array to determine utility for power combining. For their metric of utility, Emrick and Volakis [94] showed that a power combining and in-phase transmission approach may be used to obtain a product of transmit power and transmitter and receiver antenna/

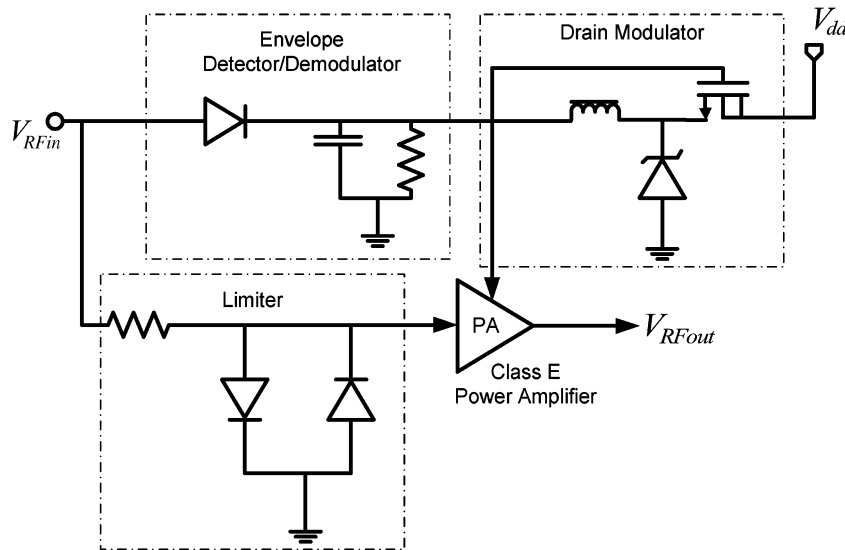


**Fig. 6.** This on-chip power combining approach is to ensure the amplifiers on the left are operated near saturation and to provide a large voltage swing on the output at the right [90].

antenna array gain (i.e.,  $P_t \times G_t \times G_r$ , or the numerator in Friis Free Space equation) of 60 dBm, which they cited as necessary for multi-Gb/s communications at 10-m distances. This study found that half-circular antennas were preferable and when a  $6 \times 6$  element array of these antennas each fed by an individual amplifier is used, the specified 60-dBm threshold is met. More recently, Valdes-Garcia *et al.* [13] of IBM and MediaTek used a form of spatial power combining for their implementation of a 16-element phased array transmitter for IEEE 802.15.3c. Atesal *et al.* [51] also recently used this technique for higher W-band frequencies (90–98 GHz) to perform spatial power combining for W-band PAs. On-chip power combining is difficult at 60-GHz and higher mm-wave frequencies due to the limited output powers of individual components and the low quality factors (Q) of on-chip passive components [51].

When deciding between on-chip power combining using transformers, and spatial power combining using active antenna arrays, the system requirements and solution must be carefully considered. For example, a spatial power combining approach must be able to overcome the challenges of on-chip antennas, including extremely lossy substrates and “preferential” antenna radiation into the substrate versus out to the surrounding environment. The method and location of phase shifter elements, either at baseband, LO, IF, or RF, and the tradeoffs associated with each must be considered also. If spatial power combining is possible in a way that overcomes the lossy substrate, e.g., using lower loss substrates such as SiGe, and if sufficient space is available for phase shifting without causing array grating lobes, then this method can be highly advantageous by avoiding losses associated with on-chip power combining structures [95]. In their implementation of a phased

<sup>5</sup>PAE =  $(P_{\text{RFout}} - P_{\text{RFin}})/P_{\text{dc}}$  [37] is a measure of how efficiently an amplifier converts dc power to RF power.



**Fig. 7. Envelope tracking for efficient amplifiers. The envelope demodulator and drain modulator work together to bias the amplifier such that it is most efficient [37].**

antenna array, Valdes-Garcia *et al.* [13] used RF-phase shifting and cited this method as requiring least area, lowest power, and fewest redundant components, and thus they deemed it advantageous over baseband, LO, or IF phase shifting. Buckwalter *et al.* [50] used a “power combining” antenna array for 60 GHz that used LO phase locking/shifting rather than RF phase shifting and found insufficient space was available to integrate all phase shifting components without generating grating lobes.

Envelope tracking [also known as “envelope elimination and restoration” (EER)] works by rapidly varying the power supply voltage in step with the input so the amplifier is kept near saturation. Intuitively, envelope tracking is beneficial for operation under backoff because it allows several nonlinear amplifiers to work in conjunction to achieve linear amplification [37] (nonlinear amplifiers are more efficient because they operate closer to saturation where current is conducted only a fraction of the time). If the EER device is not fully linear, then an additional linearization stage may be needed [37]. Results for envelope tracking at lower frequencies include 23% PAE at 16-dB backoff at 1.8 GHz by Choi *et al.* [87], who combined envelope tracking with a Doherty approach. This result should motivate further investigation of this technique for 60-GHz designs. Fig. 7 illustrates envelope tracking.

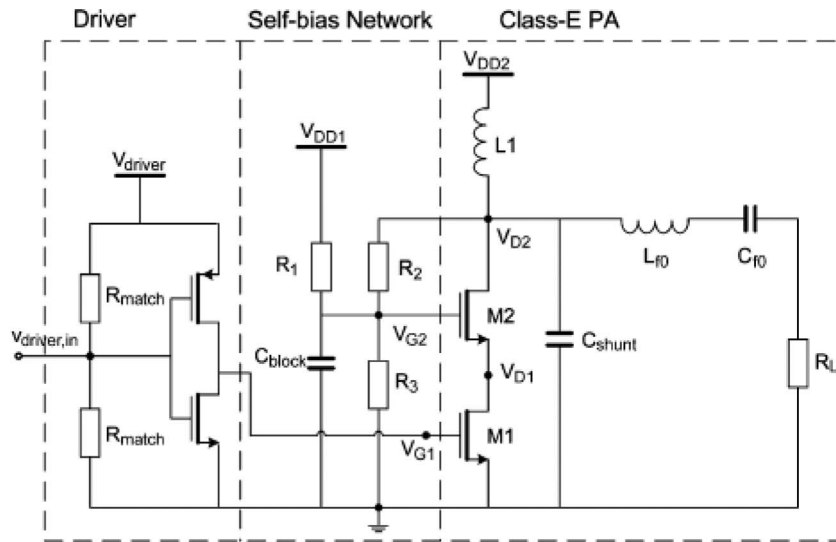
Self-biasing is attractive for designing high-efficiency PAs that require very high output powers (e.g., class-E PAs, in addition to linear amplifiers) [89]. The technique is similar to envelope tracking because it regulates the supply and bias [89]. Using passive devices, self-biasing regulates supply/bias voltages for optimal distribution of voltage swing across the different transistors in the PA [89]. In addition to high PAE, a properly designed self-biasing net-

work may make high output powers on the order of watts possible by reducing hot carrier effects that would otherwise degrade the device [96]. Results include 40% PAE at 16-dB backoff and 60% PAE at saturation reported by [89], who used a self-biasing technique at 2 GHz. At mm-wave frequencies, distributed inductive and capacitive components, such as transmission lines, would be required to create the passive devices for this technique. Fig. 8 illustrates the approach. This approach has proven to be very useful at lower RF frequencies, and merits more investigation at mm-wave frequencies of 60 GHz and above.

In addition to efficiency under linear operation, the gain, and output power achievable with a PA are key factors in the design of most 60-GHz devices. Achieving good gain and high output power becomes more challenging as CMOS scaling continues since output power is limited by the voltage supply of the device. Reduced supply voltage also limits the output voltage swing of the amplifier, putting an upper limit on gain. Novel topologies, including novel uses of transformers, may be useful in tackling these challenges [88], [98].

Table 5 summarizes some recent results in 60-GHz PA development reported in the literature. Table 6 contrasts these developments with low-power or high-efficiency PA designs for non-60-GHz applications.

Contrasting Tables 5 and 6 indicates that 60-GHz PAs are far less efficient than the most efficient designs at lower frequencies. This is due in part to operation closer to the maximum frequency of oscillation and the transit frequency of the technology node used to construct the device. But progress remains possible and improving the efficiency of 60-GHz PAs will be essential to consumer applications.



**Fig. 8.** Self-biasing as described and presented by Apostolidou et al. [89] for a 2-GHz PA. As shown here, it can be accomplished with a passive self-biasing network. This technique merits more investigation at mm-wave frequencies such as 60 GHz where high output powers are difficult to achieve.

## V. LOW-NOISE AMPLIFIERS

Performance of 60-GHz and subterahertz communication systems rely on low-noise figure and high gain and linearity at the receiver, as provided by RF LNAs [17]. LNA designs should be stable and must be designed to perform properly despite semiconductor process, voltage, and temperature variations. In the mm-wave region, good LNA performance becomes more difficult, due primarily to the need for more stages to achieve needed gain, and the greater variations in device parameters, due to manufacturing variations for deep submicrometer devices [17]. Proper biasing, e.g., proper current densities, can also reduce sensitivity to process, temperature, and voltage variations.

Table 7 summarizes examples of LNAs from the literature.

Fig. 9 shows a very generic LNA design for mm-wave circuits using inductors as would be found in a lower frequency design, e.g., at 1 GHz. The cascode design allows for good isolation between input and output stages, and allows for separate input and output matching [37]. Fig. 9 also shows “inductive degeneration” which uses inductors to simultaneously match for minimal noise figure and maximum gain. Various techniques have been explored for improving this design at mm-wave frequencies. One general and promising technique that would also be useful outside LNA design would be to carefully engineer current return paths to reduce the amount of current generated in the lossy substrate [106].

At mm-wave frequencies, it is often beneficial to implement the inductors in Fig. 9 using transmission lines instead of standard spiral inductors. The decision to use transmission lines or inductors should be made after con-

sidering the size, layout requirements, and electrical performance of each structure, and after conducting simulations of each approach using EM simulators such as High Frequency Structure Simulator (HFSS) for the chip environment [e.g., silicon or SiGe (silicon germanium) CMOS]. Transmission lines offer the advantages of faster design and well controlled current return paths at the expense of increased area [108], [109]. If transmission lines are used, then coplanar waveguide (CPW) transmission lines should be used instead of microstrip lines for highest inductive quality factor [23], and shields below the line (implemented as arrays of short strips below the line) may be added to improve the quality factor of the coplanar lines (Varonen et al. [110] show that shielded CPW lines can attain quality factors three times higher than nonshielded lines).

Inductors may offer space savings over transmission lines [111], [112], but do not offer the same routing flexibility as transmission lines. Die photographs of mm-wave chips with many transmission lines demonstrate this routing flexibility. When an inductor is used, it is advantageous to use spiral inductors rather than single-layer inductors and to use the smallest footprint possible for highest quality factor [112], [113]. When used in transformers, e.g., for input power matching, inductors should be implemented with stacked designs for best coupling [114].

## VI. 60-GHz VOLTAGE-CONTROLLED OSCILLATORS

The VCO is a fundamental building block of most wireless systems as it provides stable frequency sources, such as

**Table 5** Summary of Recent Developments in 60-GHz Power Amplifier Design

Reference	Topology	Gain and output Power <sup>d</sup> (measurement frequency)	PAE, Power Consumption, Supply Voltage
[97]	3 single ended CS (Common Source) class A <sup>e</sup> in 90 nm CMOS	5.2 dB gain, 9.3 dBm (61 GHz) saturated output power	7% PAE, 39.75 mW from 1.5 V
[25]	2-stage AB balanced CE (Common Emitter) in 0.12 $\mu$ m SiGe HBT	9 dB, 16 dBm (61.5 GHz) saturated output power	143 mW from 1.1 V
[99]	single-stage push-pull with microstrip and differential cascode in 0.13 $\mu$ m SiGe BiCMOS	18 dB, 13.1 dBm P1dB output 1dB compression point power, 20 dBm saturated output power	12.7% PAE, 248 mW from 4 V
[95]	cascaded 2-stage, CS to CS in 90 nm CMOS	9.8 dB, 6.7 dBm (56 GHz) P1dB output 1dB compression point power	20% PAE
[84]	transformer-coupled 3-stage cascade in 90 nm CMOS	15 dB, 12.2 dBm at 61 GHz saturated output power	84 mW from 1.2 V
[100]	2-stage transformer-coupled, cascode to CS, with differential-to-single ended conversion through transformer in 90 nm CMOS	5.6 dB, 12.3 dBm saturated output power	8.8% PAE, 1 V
[100]	3-stage transformer coupled, cascode to CS to CS in 90 nm CMOS	13.8 dB, 11.0 dBm saturated output power	14.6% PAE, 1 V supply
[101]	cascaded CS to CS in 65 nm CMOS	7.6 dB, 8.9 dBm output 1dB compression point power, 13 dBm saturated output power	PAE<11%, 64.8 mW from 0.9 V,
[92]	Doherty in 0.13 $\mu$ m CMOS	13.5 dB, 7.8 dBm saturated output power	3.0% PAE, 1.6 V
[102]	3-stage, cascode to CS to CS in 90 nm CMOS	17 dB, 5.1 dBm P1dB output compression point power, 8.4 dBm saturated output power	5.8% PAE, 54 mW

<sup>d</sup> Common measures of output power include Output/Input 3<sup>rd</sup> order intermodulation product intercept (OIP3 and IIP3), which indicate the extrapolated output/input power level at which the output power begins to be dominated by the third order harmonic for a two tone input. The saturated output power indicates the maximum output power for the device, and the input/output 1 dB compression point (IP1dB and OP1dB) indicates the input/output power level at which point the output power is 1 dB below the extrapolated output power for a small signal input.

<sup>e</sup> Class A indicates the amplifier is highly linear and operates as a current source over the entire period.



**Table 6** Lower Power or Power Efficient Power Amplifiers Below 60 GHz. Millimeter-Wave 60-GHz PAs May Never Be as Efficient Because Devices Are Operating Closer to Their Maximum Frequency of Operation

Reference	Topology	Gain and Output Power, Frequency	PAE, Power Consumption
[85]	load-shared driver amp and cascode PA, self-biased PA in 0.18 $\mu\text{m}$ CMOS	>30 dB, 32.2 dBm saturated output power, 1.8 GHz	35.6% PAE
[86]	cascode-cascade Doherty with CG (Common Gate) main, CS auxiliary in 0.18 $\mu\text{m}$ CMOS	12 dB, 21 dBm P1dB output compression point power, 2.4 GHz	14% PAE
[87]	envelope tracking in 2 $\mu\text{m}$ HBT and 0.13 $\mu\text{m}$ CMOS	24.62 dB, 24.22 dBm output power, for WiBro at 1.8 GHz (CMOS implementation)	23% PAE at 16 dB back-off, 38.6% PAE at 24.22 dBm output, 51% PAE at saturated output Power
[90]	pseudo-differential cascode with transformer class-AB <sup>f</sup> biasing in 0.13 $\mu\text{m}$ CMOS	10 dB, 24 dBm P1dB output compression point power 2.4 GHz	25% drain efficiency, 32% drain efficiency at Psat of 27dBm, 136.8 mW power consumption
[89]	class-E <sup>g</sup> RF cascode w/ self-bias network to class-E PA cascode in 65 nm CMOS	25 dB-30 dB, 30 dBm saturated output power 2 GHz	PAE of 60% at Pout of 30dBm, PAE of 40% at 16 dB back-off
[103]	CS gain stage to linearization stage to cascode power stage in 0.18 $\mu\text{m}$ CMOS	20 dB, 22 dBm saturated output power, 20.6 P1dB output compression point power, 2.4 GHz	34.6% PAE at 20.6dBm, 30% PAE at 22dBm

<sup>f</sup> Class-AB indicates the quiescent current (current flow when input is zero or very small) is a small fraction of the peak signal current.

<sup>g</sup> Class-E is a class of high efficiency switching amplifier [37].

LOs used in transmitters and receivers. VCOs for the unlicensed 60-GHz band must have very large absolute and relative tuning ranges, at about 15% (as high as 20% when process, temperature, and supply voltage variations are considered) of the operating carrier frequency, in order to cover the entire range of 57–67 GHz [115].

There are several broad classes of VCOs: LC-tank VCOs, which are the most pervasive for high-speed low-voltage applications, Colpitts VCOs, subharmonic or push-push VCOs, and distributed VCOs [17]. An LC-tank VCO relies on cross-coupled transistors to generate a negative resistance (necessary for oscillation) along with an LC circuit with tunable frequency of oscillation, as shown in

Fig. 10. One of the key advantages of an LC-tank VCO is the ability to generate a differential output [17]. Differential circuits, in general, are preferred over single-ended circuits in RF circuitry, since differential circuitry provides greater rejection of common-mode noise, better performance despite process–voltage–temperature (PVT) variations, and less susceptibility to cross talk and noise within a circuit layout.

The Colpitts VCO design is widely used and was demonstrated for 60 GHz as early as 2004 in a SiGe:C BiCMOS technology [116]. The Colpitts design is similar to the LC-tank design because the frequency is tuned through an LC tank, but it offers the advantage of requiring only a

Table 7 Examples From the Literature of LNAs

Reference	Gain	Noise-Figure	Topology	Linearity IIP3/P1dB	Power, Voltage	Process
[97]	14.6 dB	4.5 dB, simulated	2-stage cascode	-6.8 dBm at 58 GHz IIP3, -0.5 dBm at 58 GHz OP1dB	24 mW from 1.5 V	90 nm CMOS
[104]	20 dB from 51-57.5 GHz	8 dB from 50 – 57 GHz	3-stage cascode	-12 dBm at 56 GHz IIP3, -22 dBm, IP1dB	79 mW from 2.4 V	0.13 $\mu$ m CMOS
[26]	13 dB	4.6 dB simulated	2-stage CG to CS	N/A	N/A	0.13 $\mu$ m CMOS
[25]	14.7 dB at 61.5 GHz	4.5 dB at 61.5 GHz	2-stage single ended CB (Common Base) to degenerated cascode	-8.5 dBm IIP3, -20 dBm IP1dB	10.8 mW from 1.8 V	0.12 $\mu$ m SiGe BJT
[105]	15 dB	4.5 dB	unbalanced CB to degenerated cascode	-9 dBm IIP3, -20 dBm IP1dB	10.8 mW from 1.8 V	0.12 $\mu$ m SiGe BJT <sup>h</sup>
[106]	14.5 dB at 59 GHz	4.1 dB	cascode single stage	-2 dBm IIP3, +1.5 dBm OP1dB	8.1 mW from 1.8 V	0.12 $\mu$ m SiGe BiCMOS

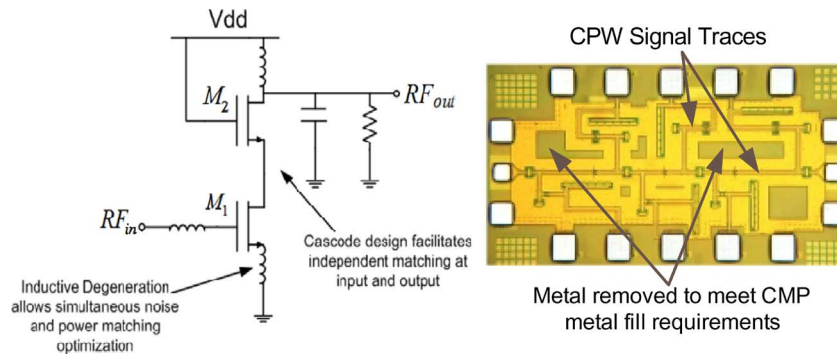
<sup>h</sup>Bipolar Junction Transistor

single transistor while the LC tank requires two [117]. The Colpitts design also offers low phase noise [37], but is more susceptible to low-Q inductors and capacitors than LC-tank VCOs [117].

Subharmonic VCOs allow active components to operate at only a fraction of the output frequency (e.g., transistors operate at 30 or 15 GHz for a 60-GHz VCO output), where they produce substantially more power than at the desired output frequency. This is in contrast with the Colpitts and LC-tank VCOs that require transistors to operate at the fundamental resonance frequency of the circuit, where transistor efficiencies are smaller. Push–push VCOs are a subclass of subharmonic VCOs, in which the second harmonic of the fundamental frequency of oscillation is extracted. Subharmonic VCOs at 60 GHz have been

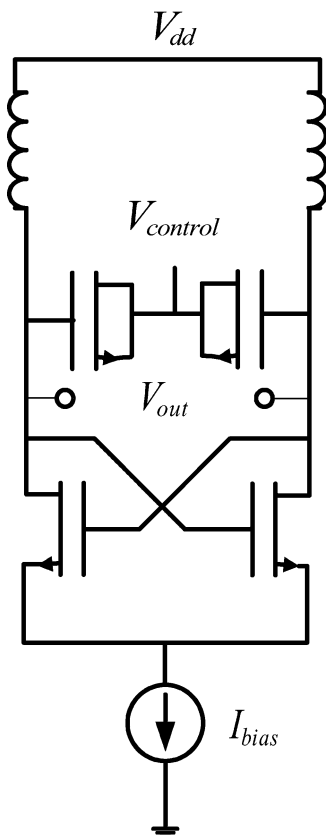
demonstrated in [118]–[120]. Conventional subharmonic designs have the disadvantage of only being capable of single-ended outputs [17], although a balun may be used to convert to a differential signal. Fig. 11 illustrates a push–push design (note location of output at source of coupled pair) that uses the second harmonic of a 30-GHz fundamental frequency to generate a 60-GHz output frequency.

Distributed-, ring-, or traveling-wave-based VCOs are based on a feedback design that generates the desired frequency along a transmission line [17], [119] or signal path. Miyazaki *et al.* [121] claim that ring-based VCOs generally require less power and are smaller than LC-tank VCOs. It is possible to achieve a tuning range of 0.1–65.8 GHz with a ring-based VCO [119]. A challenge usually faced by ring-based or distributed VCOs is lower maximum oscillation



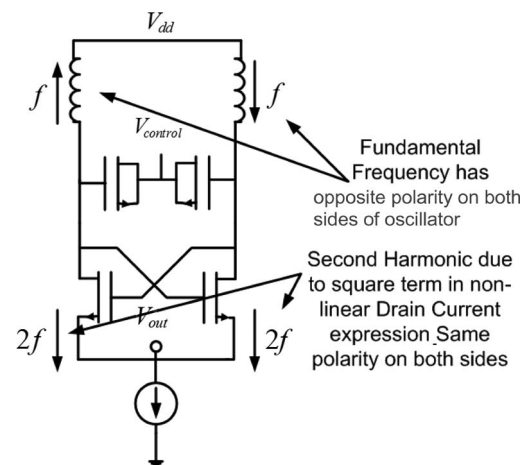
**Fig. 9.** A very typical LNA design. This figure indicates the importance of inductive elements for LNA design. Transmission lines are also used frequently as inductive components at mm-wave frequencies, as shown on the right from [107]. Transmission lines require more space than spiral inductors, but may be routed very flexibly, and may be easier to design for first-pass success.

frequency, which can be overcome using hybrid designs [119]. For example, Fig. 12 shows a ring-based subharmonic VCO [119] that converts a 20-GHz fundamental frequency to 60 GHz and offers a tuning range of 0.1–60 GHz. The success of this design indicates that hybrid and other innovative designs should be considered for 60-GHz and higher mm-wave and THz frequencies.

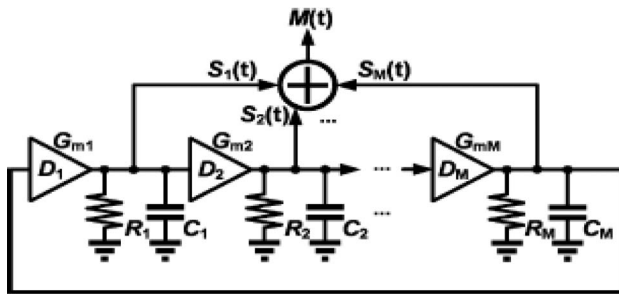


**Fig. 10.** A typical LC-tank voltage-controlled oscillator that generates a stable frequency source. This design is capable of a differential output.

In addition to subharmonic VCOs, it is possible to generate the needed LO frequency using frequency multiplication. For example, a 25-GHz VCO output frequency may be doubled to 50 GHz to serve as a useful LO frequency for a 60-GHz design. This is different from a subharmonic push-push design because frequency multiplication relies on an external frequency that is injected into the oscillator and then multiplied by the oscillator (while a subharmonic design generates a fundamental frequency and its harmonic within the same oscillator and outputs the harmonic frequency). This was the approach taken by Kishimoto *et al.* [122], who used the second harmonic of a 15-GHz source as an injection frequency into an oscillator. The oscillator then multiplied the input 30-GHz signal by 2 to obtain an output frequency of 60 GHz (and an overall multiplication factor of 4 for the originally generated 15-GHz signal). This approach may offer a low phase noise with small implementation area, but has the



**Fig. 11.** A typical push-push VCO design. The output is the second harmonic of the fundamental frequency and is taken at the source nodes of the transistors in the cross-coupled pair.



**Fig. 12.** A hybrid ring, triple-push VCO design [119]. This design has an extremely wide tuning range of 0.1–60 GHz.

disadvantage of requiring a large input injection power (e.g., the 30-GHz injection frequency in [122]). Kishimoto *et al.* [122] used a multiplication factor of 4, and a higher multiplication factor may be disadvantageous as it results in lower overall output power. Also, Kishimoto *et al.* [122] state that this technique has the disadvantage of high susceptibility to frequency shifts due to temperature variations.

Table 8 compares several VCO designs and implementations for 60 GHz. The table and discussion indicate a rich design space to explore when implementing a mm-wave VCO, and the advantages of each approach should be considered. Different approaches include fundamental 60-GHz oscillators such as the Colpitts for a single-ended 60-GHz signal, a cross-coupled pair for a 60-GHz differential output signal, and a subharmonic approach with frequency multiplication techniques.

## VII. 60 GHz MIXERS

Mixers may be active or passive. Operationally, active mixers modulate transconductance while passive mixers modulate a switch resistance [17]. Active mixers provide a conversion gain through transistors that serve as amplifying elements, while passive mixers use diodes or non-amplifying transistors as simple switches, resulting in a conversion loss. Passive mixers are easier to implement at subterahertz frequencies compared to active mixers [128], [129]. Passive mixers consume very little power, can achieve high linearity performance [128], and lower  $1/f$  noise and shot noise [129] than active designs.

Large LO power is difficult to achieve at 60 GHz, since transistors operate closer to the transit frequency and maximum frequency of oscillation in CMOS [17]. This greatly complicates mixer design (especially switch-based passive mixers, which often require higher LO power levels in order to switch firmly). Conversion gain falls off quickly and conversion loss rises quickly with reduced LO power [17]. Thus, 60-GHz mixer designs must consider lower LO power levels if passive mixers are used. Researchers must balance gain, linearity, and power consumption when selecting mixer and amplifier topologies.

Table 8 indicates that VCOs for the 60-GHz band typically provide output powers about  $-8$  to  $-20$  dBm. Table 9 summarizes recent mixer results.

It is also important to consider isolation between the different ports of the mixer. Mixers may be either single ended (the LO, IF, and RF frequencies appear at the output), single balanced (two of frequencies—RF, LO, or IF—appear at the output), or double balanced (only one of the frequencies—RF, LO, or IF—appear at the output). Low isolation results in increased distortion, self-jamming, and dc offset errors. Single-balanced and double-balanced designs offer better isolation at the cost of increased circuit area and complexity over single-ended mixer designs.

## VIII. TRANSMISSION LINES AND PARAMETER EXTRACTION FOR SUBTERAHERTZ CIRCUIT DESIGN

Transmission lines and other passive components such as spiral inductors dominate the area of most RF and mm-wave chips. Characterization of these structures is essential for successful 60-GHz design. It is quite common that major semiconductor manufacturers do not have a complete understanding of the material properties of their manufacturing processes at mm-wave frequencies, especially if their primary customers require digital, and not analog, circuits.

Transmission lines play many roles: they transport signals between structures, perform impedance matching, and are at times the best means of creating inductive or capacitive elements, especially when lumped components are impractical or too lossy to fabricate in the semiconductor process due to parasitic lead inductances or poorly defined current return paths [17].

The two primary forms of transmission lines used for 60-GHz structures include microstrip transmission lines and coplanar waveguide transmission lines [138]. Microstrip designs offer higher capacitive quality factors (defined as the ratio of electric energy stored to energy lost per cycle) than coplanar lines due to the placement of their ground shield above the substrate [138]. Coplanar designs offer higher inductive quality factors (defined as the ratio of magnetic energy stored to energy lost per cycle) than microstrip designs. The importance of inductive components (e.g., in Fig. 9) often makes coplanar transmission lines preferable to microstrip transmission lines [138], [139]. Fig. 13 illustrates microstrip and coplanar waveguide transmission lines. Emerging transmission line concepts include elevated coplanar waveguides, where the signal is elevated above the ground lines, possibly reducing insertion loss (e.g., signal line on a top metal layer, with ground lines in a lower metal layer) [140].

In addition to transmission lines, it is also possible to design hybrid on-chip couplers for mm-wave 60-GHz chips. In fact, most of the traditional microwave structures developed for lower frequencies such as those discussed by



**Table 8** A Comparison of VCOs That Operate in or Near the 60-GHz Band

Reference	Frequency Range	Topology & Process	Phase Noise	Output Power	Power Consumption, Voltage	FOM <sup>1</sup> , for highest Phase Noise
[105]	52-53.955 GHz, 3.68%	differential Colpitts in 0.12 $\mu\text{m}$ SiGe	-100 dBc/Hz at 1 MHz offset	-8 dBm	25 mW from 2.5 V	8.46, at 1 MHz offset
[105]	65.8-67.9 GHz, 3.14%	differential Colpitts in 0.12 $\mu\text{m}$ SiGe	-98 to -104 dBc/Hz at 1 MHz offset	-8 dBm	24 mW from 3.0 V	12.3 at 1 MHz offset
[118]	64-70 GHz, 8.95 %	fundamental 30 GHz push-push with output buffers in 0.13 $\mu\text{m}$ CMOS, single-ended output	-90.7 dBc/Hz at 1 MHz offset	-10 dBm	1.5 V and 1.0 V supply tested	Not Available
[124]	53.1-61.3 GHz, 14.3%	variable inductor LC-tank VCO in 90 nm CMOS, single-ended output	-118.75 dBc/Hz at 10 MHz offset	-6.6 dBm	8.7 mW from 0.7 V	-34.2 at 10 MHz offset
[125]	66.7-69.8 GHz, 4.5%	intrinsic tuning LC-tank VCO in 0.13 $\mu\text{m}$ CMOS, differential output	-98 dBc/Hz at 1 MHz offset, -115.2 dBc/Hz at 10 MHz offset	>-24.8 dBm	4.32 mW from 0.6 V	5.03 at 1 MHz offset, -32.15 at 10 MHz offset
[115]	55.5-61.5 GHz, 10.25%	cross-coupled pair with LC-tank (shielded slow-wave inductor, MOSCAP <sup>2</sup> varactors) in 0.13 $\mu\text{m}$ CMOS	>-90 dBc/Hz at 1 MHz offset	-15 dBm	3.9 mW from 1 V	11.253 at 1 MHz offset
[115]	59-65.8 GHz, 10.89%	cross-coupled pair with LC-tank (shielded slow-wave inductor, MOSCAP varactors) in 0.13 $\mu\text{m}$ CMOS	>-90 dBc/Hz at 1 MHz offset	-15 dBm	3.9 mW from 1 V	11.81 at 1 MHz offset
[119]	0.1-65.8 GHz, 199 %	ring-based triple push in 90 nm CMOS	-99.4 to -78 dBc/Hz at 1 MHz offset, -107.8 to -94.6 dBc/Hz at 10 MHz offset, measured up to 47.4 GHz	-27 to -7.5 dBm	1.2 to 26.4 mW from 1.2 V	26.57 at 1 MHz offset, -10.02 at 10 MHz offset
[126]	53.2-58.4 GHz, 9.31 %	inductive division LC-tank in 90 nm CMOS	-91 dBc/Hz at 1 MHz offset at 58.4GHz operating frequency	-14 dBm	8.1 mW from 0.7 V supply, 1.2 mW from 0.43 V supply	13.01 at 1 MHz offset
[127]	49-50.1 GHz, 2.2 %	LC-resonator with cross-coupled NMOS in 0.25 $\mu\text{m}$ CMOS	-99 dBc/Hz at 1 MHz offset	-11 dBm at 49.4 GHz	4 mW from 1.3 V	0.923 at 1 MHz offset
[120]	52-52.6 GHz, 1.15 %	push-push with thin film microstrip lines in 0.18 $\mu\text{m}$ CMOS	-97 dBc/Hz at 1MHz offset at 53 GHz	-16 dBm	27.3 mW from 2.1 V supply	11.73 at 1 MHz offset
[122]	62 – 62.76 GHz, 0.96 %	X4 frequency multiplication in 0.14 $\mu\text{m}$ AlGaAs/InGaAs HBT Process mounted in LTCC flip chip package	-94 dBc/Hz at 100 kHz offset for 2 dBm injection power	1 dBm	Not Reported	Not Available

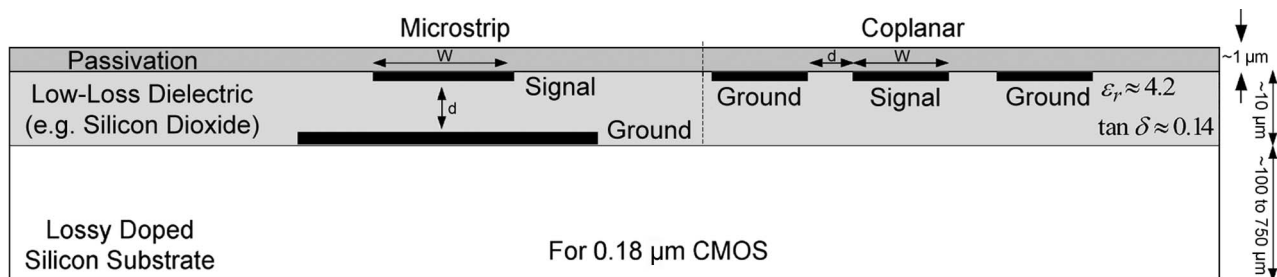
<sup>1</sup> Defined as  $\mathcal{L}\{f_o, \Delta f\} + 10 \log_{10} \left( \frac{\left( \frac{f_o}{\Delta f} \right)^2 P_{\text{consumed}}}{\text{mW}} \right)$  [123], where  $\mathcal{L}\{f_o, \Delta f\}$  is the phase noise at  $\Delta f$  from the center frequency  $f_o$ , and  $\frac{P_{\text{consumed}}}{\text{mW}}$  is the power consumed in mW. Better VCOs have lower FOM (Figure of Merit). This FOM indicates higher frequency VCOs are inherently more difficult to construct, as the FOM of a VCO becomes more positive (i.e. is worse) as  $f_o$  increases.

<sup>2</sup> Metal Oxide Semiconductor Capacitor

Table 9 Recent Results for 60-GHz Mixers

Reference	Topology and Type	Conversion Gain/Loss	Process	RF, IF Frequency	Tested LO Frequency and Power	RF-LO Isolation & Linearity <sup>k</sup>
[130]	Gilbert-cell upconversion double-balanced, active	>2 dB (Gain)	0.13 $\mu$ m CMOS	57 – 65 GHz RF, baseband IF	60 GHz at 0 dBm	-37 dB isolation, -5.6 dBm OP1dB
[131]	Gilbert-cell downconversion double-balanced, active	>2 dB (Gain)	0.13 $\mu$ m CMOS	57 – 64 GHz RF, baseband IF	60 GHz at 0 dBm	-36 dB isolation, -8 dBm IIP3
[132]	quadrature single-balanced single-gate, active	>-2 dB (Loss)	0.13 $\mu$ m CMOS	51-63 GHz RF, 2 GHz IF	58 GHz at 0 dBm	-15 dB isolation, -3.5 dBm IP1dB
[133]	unipolar subharmonic antiparallel diode pair, single ended, passive	-13.2 dB (Loss)	GaAs MSAG5 process	58.5-60.5 GHz RF, 1.5-2.5 GHz IF	14-14.5 GHz at 3-4 dBm	-17 dB isolation
[134]	4 <sup>th</sup> subharmonic antiparallel diode pair, single ended, passive	-17 dB (Loss)	GaAs on liquid-crystal Polymer	60 GHz RF, DC – 1.25 GHz IF	16 GHz at 8 dBm	-30 dB isolation, -2 dBm IIP3
[135]	2 <sup>nd</sup> sub-harmonic Gilbert cell, double-balanced, active	upconversion: -6 dB (Loss), downconversion: -7.5 dB (Loss)	0.13 $\mu$ m CMOS	35-65 GHz RF, baseband IF	20-32.5 GHz at 7-8 dBm	-45 dB isolation, -5 dBm IP1dB
[136]	push-pull dielectric resonator, double-balanced, passive	>-15 dB (Loss)	Fujitsu FHR02X K-band pHEMT	60-61.5 GHz RF, 1 GHz IF	self oscillating	isolation through integrated Yagi antenna
[137]	single-balanced Gilbert cell, active	>9 dB (Gain)	0.12 $\mu$ m SiGe BJT	57 – 64 GHz RF, 8.3-9.1 GHz IF	52 GHz at -3 dBm	-26 to -30 dB isolation, -7 dBm IP1dB (includes buffer)
[128]	single-ended resistive mixer, passive	-11.6 dB (Loss)	90 nm CMOS	57 – 63 GHz RF, 2 GHz IF	60 GHz at 4 dBm	6 dBm P1dB, 16.5 dBm IIP3
[129]	single-balanced resistive mixer, passive	-11.5 dB (Loss)	0.25 $\mu$ m pHEMT	57 – 67 GHz RF, 5.3 GHz IF	56 GHz at 8 dBm	34 dB isolation
[129]	single-balanced Image Reject mixer, passive	-13 to -16 dB (Loss)	0.25 $\mu$ m pHEMT	57 – 66 GHz RF, 5.3 GHz IF	57 GHz at 8 dBm	-36 dB isolation, -13 dBm OP1dB, 4 dBm IIP3

<sup>k</sup>Most authors report either P1dB or IIP3. The application determines which is most appropriate.



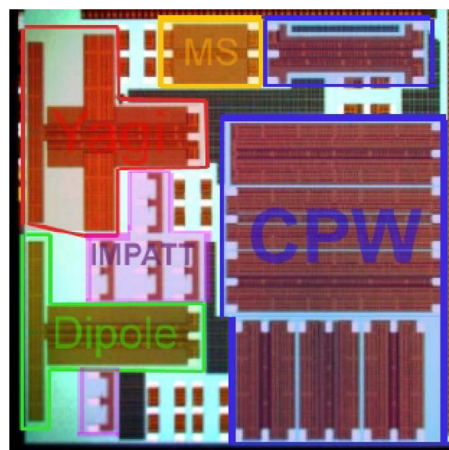
**Fig. 13.** Microstrip and coplanar waveguide structures. Parameters for the substrate are taken from [139].

Pozar in [53] may be implemented on chip at 60-GHz and higher mm-wave frequencies. For example, a  $180^\circ$  hybrid 4-port coupler traditionally designed on a printed circuit board can be used to create an on-chip mm-wave balun to convert a single-ended VCO output to a differential signal. In 2009, Lien *et al.* [141] presented a design and analysis of a  $180^\circ$  Marchand rat race hybrid in  $0.13\text{-}\mu\text{m}$  CMOS as a mm-wave balun. Their implementation achieved an insertion loss of 3–4 dB from 45 to 80 GHz on through ports, and isolation below  $-20$  dB from 47 to 72 GHz on isolated ports.

The primary challenge of passive component design is selecting the correct topology and dimensions for each component to avoid excessive losses. This requires accurate knowledge of the process material parameters at the operating frequency, including relative permittivity and loss tangent. This is difficult due to the differences among different fabrication technologies (e.g., the substrate doping concentration of CMOS substrates increases with each new technology node), and by the inability of foundries to supply these data for their processes at mm-wave frequencies. Researchers must extract these parameters and build a library of models using test structures before completing more complex designs.

A test structure chip containing passive components is an excellent tool for extracting material parameters. Such a chip for 60-GHz parameter extraction was fabricated at The University of Texas at Austin in  $0.18\text{-}\mu\text{m}$  CMOS, and is shown in Fig. 14 [139]. The test chip contained open and shorted coplanar transmission lines (CPW) of various lengths, a microstrip transmission line (MS), impact avalanche transit time (IMPATT) diodes, and Yagi and dipole antennas. Relative permittivity and loss tangent can be extracted from the structure by measuring the S-parameters of the transmission lines with a vector network analyzer (VNA). S-parameters can be extracted using a wafer probe station with correct probes for the type of transmission line used (e.g., ground-signal-ground probes for CPW transmission lines) and a VNA capable of operating at the desired frequency.

The coplanar waveguides on the chip shown in Fig. 14 were used to extract the effective material parameters of  $0.18\text{-}\mu\text{m}$  CMOS substrate at 60 GHz. The coplanar

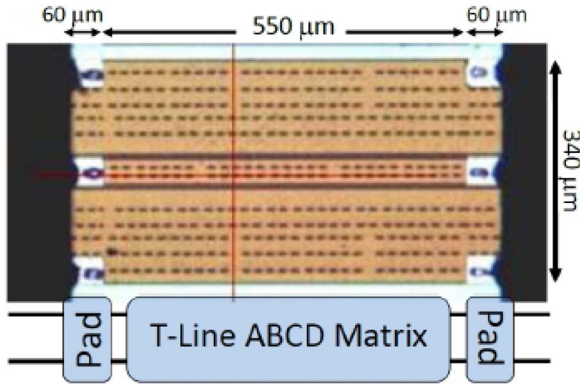


**Fig. 14.** A test structure chip created at The University of Texas at Austin for material parameter extraction for  $0.18\text{-}\mu\text{m}$  CMOS at 60 GHz, along with dipole and Yagi on-chip antennas [139].

waveguide transmission lines were modeled using ABCD matrices<sup>6</sup> cascaded between ground-signal-ground (GSG) probe pad ABCD matrices. The probe pad ABCD matrices were de-embedded by first measuring the ABCD parameters of isolated probe pads [139]. Researchers extracting material parameters or characterizing on-chip structures must include de-embedding structures on their chips, such as probe pads, which may be measured and characterized separately and apart from transmission lines or other circuitry. Fig. 15 illustrates the test transmission line, which includes probe pads whose effects must be de-embedded. The measured ABCD matrix of the transmission line was used to extract the characteristic impedance and propagation constant of the transmission line. These were then used with transmission line dimensions to determine the relative permittivity  $\epsilon_r$  and loss tangent  $\tan \delta$  of the substrate. For a popular  $0.18\text{-}\mu\text{m}$  CMOS process at 60 GHz, the

<sup>6</sup>ABCD parameters are equivalent to S-parameters for 2-port networks, but are advantageous because a cascaded structure can be modeled using multiplied ABCD matrices. Cascading rules for S-parameter matrices are more complex.





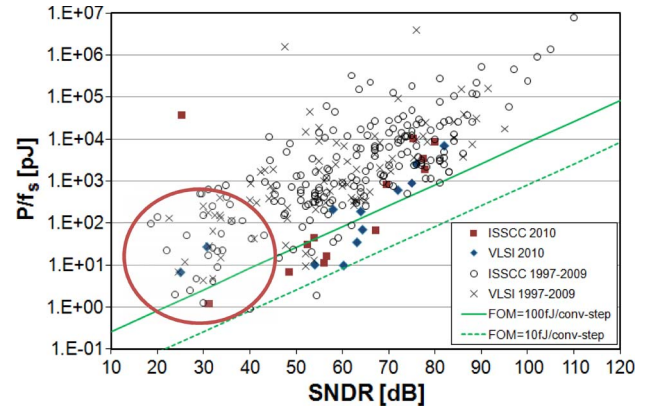
**Fig. 15.** On wafer measurements of a CPW transmission line were used to extract the material parameters of a 0.18-μm CMOS process [139].

effective relative permittivity and loss tangent were found to be approximately 4.2 and 0.14, respectively [139].

## IX. HIGH-SPEED ADCs

Massively broadband wireless communication systems must convert RF/analog wireless signals to the digital domain for proper storage and handling of the tremendous amount of transferred data. ADCs will be crucial in determining the achievable data rates for 60-GHz and subterahertz communication devices. A key challenge in ADC design is the power-bandwidth product which requires a designer to trade off high sampling rates with high resolution (e.g., number of bits). In any process technology, the designer's goal is to properly sample the massive information bandwidth while not consuming excessive power. Also, modern CMOS designs must achieve desired resolution with a low supply voltage to avoid damaging active components [142] to ensure low power operation. Kraemer [143] estimates an ADC will need at least 5 bits of resolution and an effective resolution bandwidth of 1 GHz to handle the data rates envisioned in the 60-GHz band. Work in [144] confirms that 5 bits of resolution, and perhaps even fewer bits, will be required for practical ADCs that also use analog equalization to mitigate multipath and other frequency selective effects of the radio channel and receiver front end.

For the most data-intensive applications of the 60-GHz band, such as the high-speed interface and high-definition audio and video streaming in the IEEE 802.15.3c standard, sampling rates as high as 2.5 Gs/s (giga-samples per second), with as many as 8 effective bits of resolution may be required [145]. SiGe BiCMOS and 65-nm standard CMOS ADCs have reached sampling speeds as high as 35–40 Gs/s [146]–[148], possibly allowing direct sampling of mm-wave frequencies, but these have required very high power. With non-CMOS, poorly integrable processes, it is also possible to attain sampling rates as high as 40 Gs/s



**Fig. 16.** Figure from [152]. Flash ADCs (which occupy the region circled in red) offer faster sampling rates than other topologies, but are only feasible up to 6 bits of resolution. For this reason they occupy the lower left portion of the curve [152].

[149]. Such ADCs will also suffer from very low dynamic range unless clock jitter can be made extremely low.<sup>7</sup> Also, nonstandard processes are not viable as inexpensive consumer electronics.

There are many architectures currently used in ADC design, of these, the requirement for high sampling rates makes flash ADCs an attractive option for 60 GHz. While fast, flash ADCs become impractical when more than 6 bits of resolution are required due to the large number of comparators required for higher resolutions—the comparator count grows exponentially with the number of bits [150]. Even if flash ADCs are not used, it is likely that a sub-block of any ADC will have a flash-based architecture, so it is important for designers to understand this topology [151]. Fig. 16 [152] is a plot of the energy/sampling rate provided by Prof. Murmann of Stanford University, in which flash ADCs occupy the lower left portion of the curve due to low resolutions. Flash ADC tradeoffs can be described according to [153]

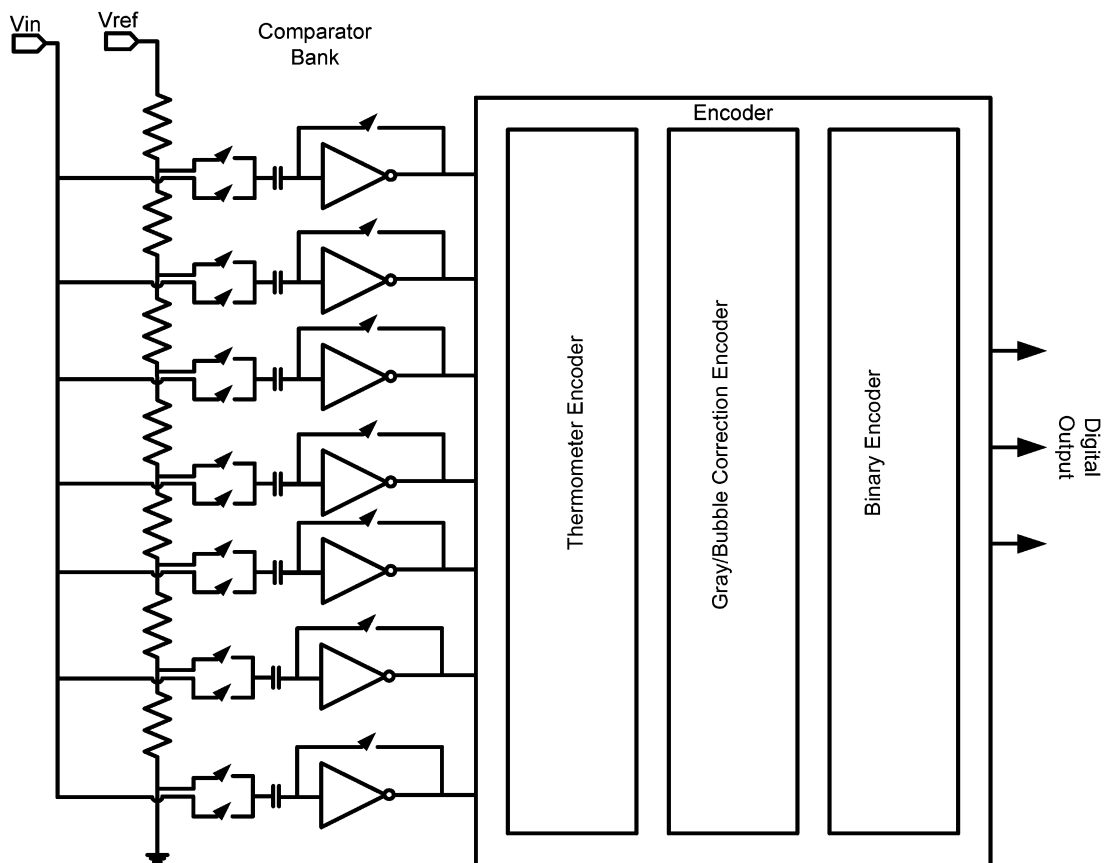
$$\text{Speed} \times \frac{\text{Accuracy}^2}{\text{Power}} \approx \frac{1}{C_{ox} A_{vt}^2} \quad (3)$$

where  $C_{ox}$  is the gate-oxide capacitance and  $A_{vt}$  is a technology-dependent factor that indicates the amount of threshold voltage mismatch between transistors on a die. From this equation we see that, for a given accuracy (number of bits), the speed (i.e., sampling rate) of the flash ADC directly trades with power consumption.

Equation (3) is useful for understanding several key trends affecting ADCs in mm-wave systems. Primarily, the

<sup>7</sup>The dynamic range (D.R.) of an ADC is limited by clock jitter, i.e., the difference in clocks distributed to different comparators in an ADC. As the input frequency increases, the impact of clock jitter increases also, limiting the dynamic range according to  $D.R. = -20 \log(\tau_{jitter} f_{in}) - 5.172 \text{ dB}$  [156].





**Fig. 17.** A basic flash architecture. Weste and Harris [155] offer an explanation of this design. The number of comparators grows as  $2^n - 1$  where  $n$  is the number of bits. This growth rate makes the input capacitance too high for high resolutions beyond 6 bits.

use of deep submicrometer processes result in faster operation, lower supply voltage, increased operation in weak or moderate inversion regimes, and increased mismatch between transistors [154]. The ADC implications of these trends are faster conversion rates, lower dynamic ranges and SNRs, increased use of designs that accommodate nonlinearity of small-signal operation in moderate or weak inversion, and increased use of low-voltage architectures [154].

Fig. 17 illustrates a basic flash architecture. The flash ADC uses a voltage ladder to generate a set of reference voltages that are compared to the input voltage using a set of comparators [155]. The design is fast because it does not require any feedback. Also, a flash ADC is mostly digital and does not require sub-digital-to-analog converters (DACs) that slow operation (other architectures require feedback from sub-digital-to-analog blocks within the ADC, requiring a slower analog portion). The key design issues with a flash ADC are the selection of input capacitance (which trades off accuracy and speed), the number of comparators to determine the number of bits of resolution, the type of encoder used, and the type of comparator used [155]. This architecture may require a complex

encoder since the output of the comparators is a thermometer (unary) code, which usually must be converted with bubble error correction to a standard binary code for processing. The large number of comparators in flash ADC can also severely load the circuits that precede it in the device [155].

The power consumption of flash ADCs directly trades with the required resolution. Authors commonly cite 6–8 bits of resolution as the limit for flash design, resulting in an effective limit on the achievable signal-to-noise-and-distortion power ratio (SNDR)<sup>8</sup> [151]. Power can also trade with accuracy [157] if error correction is incorporated into the ADC due to extra digital processing needed to implement various error correction schemes. Of the various bubble-error correction or suppression methods, Wallace-tree encoding is very popular as it can be implemented with a high-speed pipeline architecture. Generally, error correcting or extra encoding steps in the encoder will directly impact the achievable speed of the ADC [157].

<sup>8</sup>SNDR = signal power / (noise power plus distortion power) [158] is the signal-to-noise-and-distortion ratio, and is a measure of the dynamic range of the ADC.

There are several methods that can be used to reduce the power consumption of a flash ADC. These include modified flash architectures such as folding [155], or other topologies, for example, that minimize the number of active comparators that significantly determine the output.

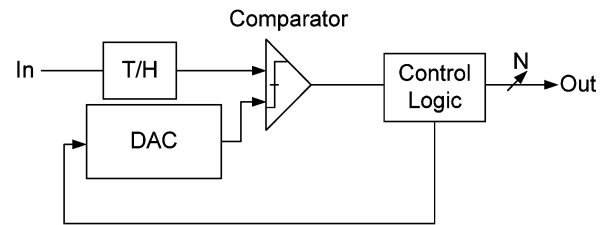
The process technology used to construct the ADC can have a tremendous impact on ADC design. The process directly impacts ADC design by setting the supply voltage, and low-voltage supplies of modern CMOS processes can make flash ADC design especially challenging [159]. The wide array of considerations involved in ADC design makes it one of the most challenging parts of designing a wireless device with integrated baseband components.

While flash ADCs may achieve high sampling rates required for mm-wave systems, they may dissipate too much power for certain applications. Recent results suggest that time-interleaved and successive approximation ADCs may be useful for mm-wave systems [202].

Time-interleaved ADCs are based on a turn-based sampling approach in which multiple ADCs successively take a sample of the input signal. The ADC output is produced from each sub-ADC in turn, thus allowing a slower sampling rate of  $f_s/M$  for each of the  $M$  sub-ADCs where  $f_s$  is the overall sampling rate. This is advantageous since slower sub-ADCs cooperate to create a high resolution and fast conversion rate ADC [147]. The challenges associated with time-interleaved ADCs are attaining low mismatch among the sub-ADC channels. Mismatch challenges include gain mismatch, bandwidth mismatch, and offset and clock phase mismatch (i.e., clock skew among different subchannels which results in spurious tones) [160]. In practice, the clock skew among subchannels limits the number of channels, and hence the achievable parallelism of this design is also limited [147]. A time-interleaved approach was used in 2010 by Cao *et al.* [160] based on subflash ADCs in 65-nm CMOS. The design achieved 10 Gs/s and dissipated 500 mW from a 1-V supply.

Successive approximation ADCs also merit consideration for mm-wave systems. The basic operation of a successive approximation ADC is illustrated in Fig. 18. A single output bit is determined at each iteration of the conversion loop, and the comparator output (either one or zero) is used to set the DAC output for each iteration. This topology was used for the sub-ADCs in 2008 by [161] in a time-interleaved design. Louwsma *et al.* [161] used an “over-ranging” technique in the design of the DAC. This approach reduces the DAC settling time and increases conversion speed. Their design also used look-ahead logic within the control logic of the successive approximation ADC, which enables limited prediction and reduces the time needed to set the output level of the DAC. The design achieved 1.35 Gs/s from a 1.8-V supply and dissipated 0.18 W.

Table 10 summarizes recent results in high-speed ADCs. The wide array of designs presented makes direct comparisons challenging. Designers should note that while flash ADCs may provide the fastest conversion rates, other



**Fig. 18. The basic operation of a successive-approximation ADC.** For an  $N$ -bit ADC, the conversion loop must be operated  $N$  times, as each iteration adds a single bit to the output. Each iteration is fast due to the small input capacitance presented by the single comparator compared to the  $2^N - 1$  comparators in a flash ADC architecture.

designs such as time-interleaving and successive approximation may result in lower dissipated power.

## X. SUBTERAHERTZ PROPAGATION

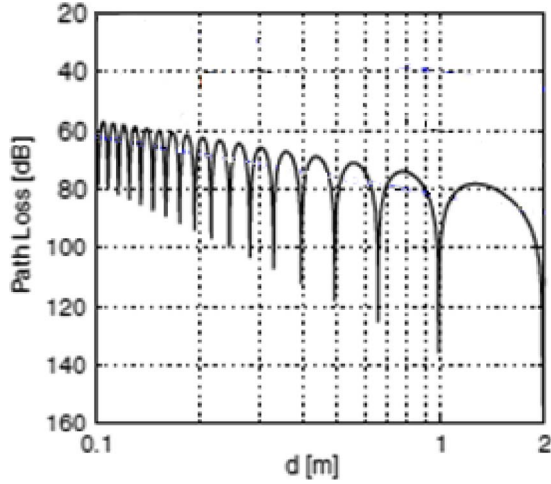
The radio propagation channel must be understood for proper design and deployment of wireless communication devices at 60 GHz and above. Both small-scale and large-scale propagation conditions must be properly characterized for a particular operating frequency band, and little is known at frequencies above 60 GHz. Large-scale propagation data describe the average loss in signal strength as a transmitter and a receiver become separated over large distances, up to tens or hundreds of meters, whereas small-scale propagation behavior happens over very small distances or time intervals (on the nanosecond or picosecond range, or over distances of a fraction of a wavelength) [46]. At 60 GHz and above, the wavelengths are so small that objects such as insects can appear as large obstructions or scatterers. Additionally, as shown in Fig. 19 [173], a simple two-ray propagation model consisting of a LOS and ground bounce component at a frequency of 300 GHz, the beginning of terahertz frequency regime, results in very deep nulls that occur repeatedly over a few centimeters of distance, something that has never been experienced in other frequency bands. Increased scattering and spatial frequency of severe reception nulls, even without movement in the channel, indicate dynamic range and adaptive antenna issues become more important at the subterahertz frequency range than in all previous wireless systems.

Large-scale propagation models are needed to estimate the SNR and interference levels as a function of separation distance between two devices. Small-scale models describe the channel over small fractions to several wavelengths of movement and are required to model the small-scale variations of multipath (e.g., multiple reflections of a signal off a wall or object). The small-scale spatial or temporal characteristics of the multipath channel is often characterized by the channel impulse response, which describes how a channel distorts an impulse of approximately infinite bandwidth sent from the transmitter to the receiver.

**Table 10** A Summary of High-Speed ADCs Reported in the Literature

Reference	Sampling Rate	Resolution <sup>1</sup> (ENOB)	Architecture and Process	Power and Voltage
[149]	1.333 Gsps	5 bit (4.5 ENOB)	2 stage pipelined flash in 180 nm CMOS	60 mW from 1.8 V
[159]	1.6 Gsps	6 bit (5.44 ENOB)	flash in 0.13 $\mu$ m CMOS	180 mW from 1.5 V
[162]	1.6 Gsps	8 bit (7.6 bit ENOB)	folding-Interpolating flash in 180 nm CMOS	936 mW from 1.8 V
[163]	5 Gsps	4 bit (3.65 ENOB)	flash with resistor ladder voltage Reference in 180 nm CMOS	70 mW from 1.8 V
[164]	1 Gsps (simulated)	7 bit (5.88 ENOB)	flash with x4 interpolator in 130 nm CMOS (simulation)	N/A
[165]	2 Gsps	6 bit (4.69 ENOB)	Single-analog-path flash ADC with ROM-based encoder in 180 nm CMOS	255 mW from 1.8 V
[157]	4 Gsps	4 bit (3.71 ENOB)	Single-channel flash with CML (Current Mode Logic) pipelining in 180 nm CMOS	43 mW from 1.8 V
[166]	600 MSs	5 bit (4 ENOB)	closed loop pipeline to 2-bit flash in 180 nm CMOS	70 mW
[167]	2 Gsps	8 bit (7.45 ENOB)	folding interpolating in SiGe	3.5 W from 3.3 V
[168]	800 Msps	6 bit (5.3 ENOB)	pipeline in 180 nm CMOS	105 mW from 1.8 V
[169]	2 Gsps	6 bit (5.689 ENOB)	Offset averaging network in 180 nm CMOS	310 mW from 1.8 V
[170]	1.356 Gsps	4 bit (3.35 ENOB)	fully differential flash with CMA (Current Mode Amplifier) and DSA (Dual Sense Amplifier) in 180 nm CMOS	68.4 mW from 1.8 V
[171]	200 Msps	6 bit (5.74 ENOB)	Flash with extra-comparators and comparator operation control in 0.35 $\mu$ m CMOS	17.05 mW from 3.3 V
[172]	2 Gsps	6 bit (5.68 ENOB)	Time-interleaving with triple-cross connection method in 180 nm CMOS	310 mW from 1.8 V
[160]	10 Gsps	6 bit (4.52 ENOB)	Time-interleaved with 4 sub-flash ADCs	500 mW from 1 V (includes PLL, programmable amplifier, and calibration components)
[161]	1.35 Gsps	10 bit (6.9 ENOB for single channel, 7.7 ENOB multi-channel)	16-channel Time-interleaved ADC with sub-successive approximation ADCs	0.18 W from 1.2 V and 1.6 V (two supply voltages)

<sup>1</sup> ENOB (Effective Number of Bits) is defined as  $\frac{SNDR - 1.76dB}{6.02dB}$ , and accounts for the fact that an ADC's resolution is lower than its "stated" resolution due to noise and distortion [158].



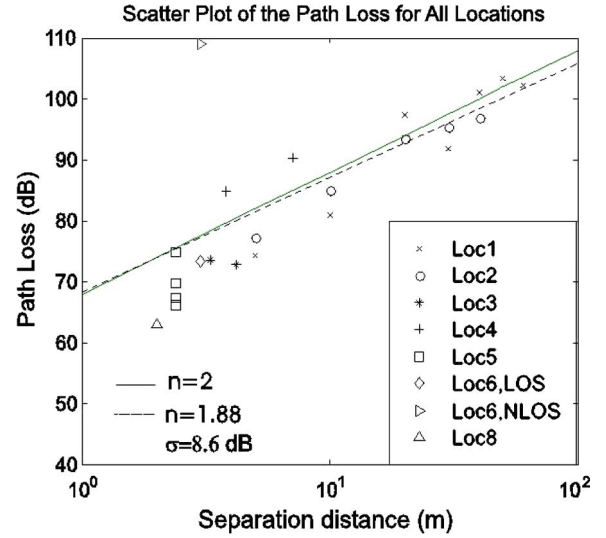
**Fig. 19.** From [173]. As carrier frequencies increase, the spatial separation between nulls in received signal strength decreases dramatically. This plot demonstrates this effect at 300 GHz. Although less severe at 60 GHz, it will be increasingly important that engineers understand this effect as 60-GHz designs will serve as models for subterahertz and terahertz devices.

Channel impulse responses are obtained with channel sounders, which excite the channel with an impulse (or a spread spectrum or swept frequency equivalent) that is 5–10 times the bandwidth of the passband of the channel of interest. While the impulse response is primarily used to determine small-scale channel behavior, large-scale characteristics may also be obtained from proper averaging of impulse responses obtained at various separation distances between the transmitter and the receiver [46].

Large-scale propagation statistics include the average path loss exponent and statistical variation from the average due to shadowing. The path loss exponent  $n$  indicates the average rate at which the received signal power decreases as a function of separation distance, where signal falls off as  $10n$  dB/decade of separation. The random variable  $X_\sigma$  accounts for log-normal shadowing and has a Gaussian distribution with random values in decibels and standard deviation  $\sigma$  dB and zero mean about the average distance-dependent path loss. A value of  $n = 2$  denotes free space propagation over distance, and a value of  $n = 4$  is common in severely attenuated propagation environments, and is the asymptotic path loss caused by a two-ray ground bounce propagation model [46]. Equation (4) summarizes large-scale channel modeling

$$PL(d) = PL(d_0) + 10n \log\left(\frac{d}{d_0}\right) + X_\sigma. \quad (4)$$

In (4),  $d_0$  is a reference distance, often taken at one meter for conventional cellular or Wi-Fi systems with cov-



**Fig. 20.** A typical path loss plot that illustrates large-scale propagation of 60 GHz at various locations [39].

erage distances of hundreds to thousands of meters. The value  $X_\sigma$  represents a Gaussian-distributed random variable with values in decibels (e.g., log-normal shadowing) to account for random shadowing caused by obstructions, antenna pointing errors, etc. The standard deviation of the shadowing has the value in  $\sigma$  dB. At 60 GHz and above, where antennas are small and the far-field region is only millimeters away from the antenna,  $d_0$  should be on the order of millimeters or centimeters for WPAN systems, and should be 1 m for a large aperture array in an outdoor backhaul system.<sup>9</sup> A large value of indicates a wide range of variation in the path loss due to many obstructions or scattering elements in the environment, causing the SNR on the communications link to vary widely. Fig. 20 illustrates the type of large-scale signal variations that can occur in typical office building environments at 60 GHz [39]. Table 11 summarizes the large-scale path loss exponents found by the research community for various channels. Work in [46] shows that simple ray tracing, when combined with statistical path loss models, provides extremely accurate site-specific propagation coverage models that can be used for practical system deployment. Such site-specific methods are likely to be even more accurate as carrier frequencies approach the THz regime.

The impulse response of a multipath channel characterizes how propagating signals are delayed by reflection and scattering in the channel. Small-scale spatial and temporal statistics collected from channel impulse responses include root mean square (RMS) delay spread, the mean-excess delay, the maximum excess delay, and angular

<sup>9</sup>The far-field, or Fraunhofer region, occurs at three wavelengths or  $2D^2/\lambda$  (where  $D$  is the largest dimension of the antenna radiating element and  $\lambda$  is the wavelength of the frequency of operation), whichever is longest.



**Table 11** Large-Scale Path Loss Models for 60-GHz Channels

Reference	Environment	Radius Considered	Path Loss Exponent	Path Loss Standard Deviation
[174]	office	0.5 m - 13 m	1.33	5.1 dB
[184]	university campus, indoor work environment	3.5 to 27.4 m	2.1	7.9 dB
[175]	laboratory	1.5 to 17 m	1.8	1.13 dB (Mean Square Error)
[176]	outdoors and indoors	4 m to ~14 m for path loss	4.4 indoor, 2 – 2.5 outdoors <sup>m</sup>	N/A
[39]	college campus building hallway	N/A	1.88 – 2 (lowest for hallway)	8.6 dB
[177]	corridor (52 m long), hall	N/A	Corridor: 1.64, LOS Hall: 2.17, NLOS Hall: 3.01	Corridor: 2.53 dB, LOS Hall: 0.88 dB, NLOS Hall: 1.55 dB

<sup>m</sup>The outdoor path loss usually follows a fourth power law for distances larger than the “break-point” defined as  $\frac{4h_t h_r}{\lambda}$  where  $h_t$  and  $h_r$  are the transmitter and receiver heights and  $\lambda$  is the wavelength [176]. Smulders et al. found that the break point is on the order of kilometers, indicating the fourth power law will not apply.

spread. At 60 GHz and above, where highly directional and steer-able antennas will be the norm, it becomes critical to understand propagation parameters such as path loss and RMS delay spread as a function of angle of arrival, so that proper adaptive antennas algorithms can be deployed to overcome shadowing and multipath [39], [178]. Equalizers will also be needed for multi-Gb/s data rate transmissions, depending on modulation methods employed, and understanding the extent and nature of multipath time dispersion (e.g., RMS delay spread) is critical to properly designing an equalizer algorithm. Because of the massive data rates used at 60 GHz and above, and the speed and power advantages of analog signal processing, equalizers will likely be implemented in analog at the RF or IF stages, rather than at digital baseband [144], [179]. While highly directional antennas may maximize the link budget while simultaneously minimizing the multipath delay spread by focusing on just one main signal path, the tradeoff between equalization and antenna beamwidth, and the speed of implementation for the beamwidth agility needed to find the “best” path (or diversity paths) will be critical for

practical implementations. Unfortunately, relatively little is known about subterahertz spatial channels, and researchers will need to understand these channels as spectrum allocations continue to become available at higher frequency bands. Today’s 60-GHz standards are including spatial coding approaches for antenna beam steering, variable beamwidth antennas, and protocols to find “blind” directional antennas, although this field is in infancy.

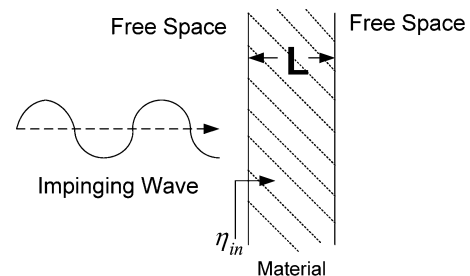
The RMS delay spread is a parameter that characterizes the propagation delays of a channel, and is useful in estimating if the channel will cause intersymbol interference without the use of an equalizer [46]. At 60 GHz, typical indoor RMS delay spread values are on the order of 10–20 ns [39], [184]. The mean excess delay describes the point in time of the impulse response of maximum multipath energy. The maximum excess delay indicates the largest delay between initial reception and the last measurable multipath component of particular amplitude. Table 12 gives values for these small-scale multipath parameters obtained for various channel environments. Other important parameters include the statistical varia-

Table 12 Small-Scale Statistics for 60 GHz

Reference	Environment	RMS Delay Spread	Mean Excess Delay	Maximum Excess Delay
[181]	conference room	narrow beam RX antennas: 1.05 ns, half-wave dipole RX antennas: 18.08 ns	N/A	N/A
[180]	university campus room	“omni” directional antennas: 22.7 ns, 60 degree directional antennas: 8.2 ns	N/A	>300 ns
[176]	large and small rooms, outdoor street level near buildings	small rooms: 15-45 ns, large indoor environments: 30-70 ns	50 ns	>300 ns
[182]	office building conference room	vertically polarized antennas: 11.02 ns, horizontally polarized antennas: 9.96 ns, circularly polarized antennas: 5.66 ns	N/A	120-140 ns
[183]	laboratory, classroom, corridor	laboratory: 6 ns (median) 14 ns (maximum), corridor: 3 ns (median) 13 ns (maximum), classroom: 13 ns (median), 35 ns (maximum)	N/A	200-300 ns

tion of multipath received power as a function of propagation time delay (e.g. a statistical model for the power delay profile), and the K-Factor. The power delay profile is useful in simulating impulse responses for novel environments [46]. The K-Factor describes the ratio of the LOS or most powerful multipath component relative to the sum of the powers of other multipath components arriving at the receiver, and has a direct impact on the quality of the eye diagram at the receiver [180], and can determine when an equalizer should be used [144].

There are three popular methods for measuring multipath channels. One method is to excite the channel with an RF pulse at the transmitter, and to use a high-speed oscilloscope at the receiver to capture the multipath echoes [46]. The second technique, called spread spectrum sliding correlator or correlative channel sounding [46], [143], simulates a pulse excitation of the channel. The receiver correlates all received signals with a predefined



**Fig. 21. The relative permittivity of materials is useful for understanding how wireless signals are attenuated by materials. Measurement campaigns such as those conducted by [184] are the most effective for determining how a material will attenuate a signal.**

**Table 13** Relative Permittivities of Various Materials at 60 GHz as found in [187]. These Values Correspond Roughly to Attenuations Measured by Anderson et al. [184]

Material	Relative Permittivity
Acrylic Glass at 60 GHz	2.5298 – j2.5298 [187]
Chipboard at 60 GHz	2.8556 – j0.1586 [187]
Concrete at 60 GHz	6.132 – j0.3014 [187]
Glass at 60 GHz	5.2839 – j0.2538 [187]
Plasterboard at 60 GHz	2.8096 – j0.0461 [187]
Wood at 60 GHz	1.5761 – j0.0962 [187]
Human Body at 60 GHz	13.2 – j10.4 [187]

widedband signal, such that multipath component arrivals result in a pulse at the system output. The third method is the swept frequency method, and usually requires a VNA with phase-locked cable between the transmitter and the receiver. A series of swept narrowband measurements are taken at different carrier frequencies to estimate the channel's frequency domain response. This is then transformed with an inverse Fourier transform to describe the channel's impulse response. While not practical for large transmitter-receiver separation distances used for Wi-Fi and cellular systems, the swept frequency method is easily implemented for short-range measurements at 60 GHz and above, using basic network analyzers and short cables. Today, all three methods are practically implemented using large pieces of test equipment. For meaningful research in practical WPAN environments of the future (e.g., behind stereo cabinets and book shelves, within vehicles, or for vehicle-to-vehicle environments), researchers will have to implement channel sounders in ultraportable, miniaturized packages, creating chips that implement the specialty functions of RF channel sounding.

An understanding of material penetration properties is also very useful for designing indoor communication systems. While extensive work is needed to fully characterize material penetration at 60 GHz and higher frequencies, knowledge of the complex permittivity of common materials is useful in estimating attenuation. At mm-wave frequencies and above, most objects are "large" compared to a wavelength, thus signal penetration is determined largely by the permittivity of the material. The reflection and transmission coefficients of an electromagnetic wave impinging normally on a material can usually be related to the relative permittivity of that material as shown in Fig. 21 (assuming no magnetic materials such as ferrites are present) [53]

$$\eta_{in} = \sqrt{\frac{\mu_0}{\epsilon_{material}}} \frac{(\sqrt{\epsilon_{material}} + \sqrt{\epsilon_0} \tanh(2\pi f \sqrt{\mu_0 \epsilon_{material}} L))}{\sqrt{\epsilon_{material}} (\sqrt{\epsilon_0} + \sqrt{\epsilon_{material}} \tanh(2\pi f \sqrt{\mu_0 \epsilon_{material}} L))} \quad (5)$$

$$\Gamma = \frac{\eta_{in} - \eta_0}{\eta_{in} + \eta_0}, \quad |T|^2 = 1 - |\Gamma|^2 \quad (6)$$

where  $\eta_{in}$  is the input impedance of the material,  $\epsilon_{material}$  is the complex permittivity of the material,  $\epsilon_0$  is the complex permittivity of free space,  $\mu_0$  is the complex permeability of free space,  $\Gamma$  is the reflection coefficient, and  $|T|^2$  is the square magnitude of the transmission coefficient, which indicates the percentage of power that penetrates the material. Table 13 gives the permittivities of several materials. This approach corroborates some of the attenuations measured by Anderson et al. [184].

The effects that building surfaces, passing cars, tree limbs, foliage, and weather have on subterahertz communications will need to be understood for proper outdoor wireless communications. Little is known about this field, but will be required for the development of standards and widespread wireless backhaul solutions. For example, work conducted by Kukshya et al. [41] indicated that rain severely impacts millimeter 38-GHz and 60-GHz signals over a link distance up to 500 m. Even short 60-GHz links of 160 m can experience attenuation of several decibels due to rain, and as high as 3.9 dB for a rain rate of 76.2 mm/h. Work in [185] considered 60-GHz propagation for outdoor intervehicle links and applied a very simple two-path propagation model to understand such phenomenon as intervehicle edge diffraction and frequency and time selectivity. As early as 1988, Bohlander et al. [186] studied the effects of adverse weather on higher frequency mm-wave systems at 116, 140, 173, and 230 GHz that may be used for backhaul or cellular links. They found and compared the effects of fog, rain, and snow, and showed rain was the most deleterious weather condition in its ability to disrupt mm-wave links. Although work by Kukshya et al. [41], Schafer [185], Bohlander et al. [186], and others has revealed much about outdoor mm-wave propagation, this line of research still remains in infancy due in part to the greater popularity of research for indoor, short-range (i.e., under 10 m) communication applications over the last decade. As circuitry, analog-to-digital, beam-pointing, and equalization capabilities are perfected for indoor applications, mm-wave communications will expand to include longer distance applications where research on outdoor propagation will become increasingly important.

**Table 14** Singh *et al.* [188] Reported This Table in 2009 to Compare the Major 60-GHz Standards That Are Under Development. An Asterisk (\*) Indicates Updates Since [188] Was Published

Name	Forum Type	Status	Maximum Data Rate (Gbps)		Applications
			OFDM	SC (Single Carrier)	
WirelessHD	Industry Consortium	Spec. 1.0, Jan 2008	4	—	Uncompressed HD video
ECMA-387	International Standard	Draft 1.0, Dec 2008	4.032	6.35	Bulk data transfer and HD streaming
802.15.3c (TG3c)	International Standard	Released October 2009*	5.7	5.2	Portable point-to-point file transfer and streaming
802.11ad (TGad)	International Standard	Target completion Dec 2012	>1		Rapid upload/download, wireless display, distribution of HDTV (High Definition TV)
WiGig	Industry Consortium	Released May 2010* [189]	7 Gbps* [189]		File transfers, wireless display and docking, and streaming high definition

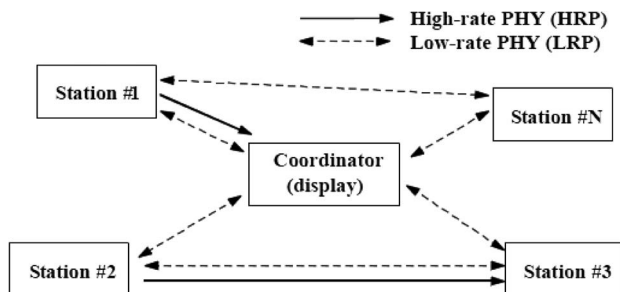
## XI. 60-GHz STANDARDS

There are many standardization and commercialization efforts currently underway by the engineering community for 60-GHz WPAN. Current technical standards activities include IEEE 802.15.3c, WirelessHD, IEEE 802.11ad, the WiGig standard, and ECMA 387. All of these standards target short range 60-GHz networks. In 2009, Singh *et al.* [188] reviewed each of these standards, as shown in Table 14. The commercialization efforts include the WirelessHD industry alliance which supports the WirelessHD standard, the WiGig industry alliance which supports both IEEE 802.11ad and the WiGig standard, and efforts by individual or smaller groups of companies, such as the recent alliance between IBM and MediaTek to deliver products based on the IEEE802.15.3c standard [12], [13], [188].

The first draft and overview of the WirelessHD standard was released in August 2009 [190], and an updated version was released in May 2010 [191] to accommodate data rates as high as 10–28 Gb/s. According to [190], the standard is intended to create wireless video area networks (WVANs) to stream uncompressed audio and 1080p video, deliver compressed audio/video data, provide advanced audio/video device control, and allow for NLOS operation with a high degree of privacy. Each WVAN makes use of a

central coordinating device to coordinate actions by member “station” devices. The coordinator is usually a sink device (i.e., a display), while the station devices are normally sink and source devices. The coordinator controls timing of station actions in the WVAN, tracks members of the WVAN, and supports the low-rate physical layer (PHY) in transmit and receive mode. A noncoordinator station device does not need to track members of the WVAN and may initiate stream connections. The standard utilizes two PHY modes in the WVAN. The high-rate PHY is intended for multi-Gb/s (up to tens of gigabits per second) throughput while the low-rate PHY is intended for multi-Mb/s throughput, both up to 10 m. Fig. 22 is from the WirelessHD specification overview and illustrates a WVAN [190]. Devices based on the WirelessHD standard were originally scheduled for release beginning in 2011 [192], but several products are currently being advertised, including WirelessHD adapters and WirelessHD equipped televisions (e.g., the WirelessHD Panasonic Viera Z1 Plasma TV). SiBEAM, a spin out company from University of California, Berkeley, is one of the standard’s strongest supporters, and has developed several chips that are in many of the first WirelessHD products [191]. Other strong supporters of WirelessHD include Intel, LG, MediaTek, and Panasonic.





**Fig. 22. Illustration of a WVAN Piconet for the WirelessHD standard [190].**

The IEEE 802.15.3c mm-wave standard is an amendment to the IEEE 802.15.3 standard and shares many similarities with the WirelessHD standard. It is a medium-access layer (MAC) and PHY layer specification targeted at WPANs, which are essentially identical to WVANs. The IEEE 802.15.3c standard supports data rates in excess of 5 Gb/s, beamforming to improve range, data aggregation schemes to improve MAC layer efficiency, and subpacket acknowledgement to reduce retransmission overhead [193]. The IEEE 802.15.3c standard uses three PHY modes: single-carrier (SC) mode for low power and complexity, high-speed interface mode using OFDM for low-latency bidirectional data transfer, and an audio/video mode for uncompressed HD audio and video streaming. IBM and MediaTek recently announced an agreement to deliver a 60-GHz chip in 2011 that uses the IEEE 802.15.3c standard [12]. To the authors' knowledge, no products are yet available that implement the IEEE 802.15.3c standard.

The WiGig alliance has worked closely with the IEEE 802.11ad technical group, and the WiGig standard closely mirrors the IEEE 802.11ad standard. There is speculation that the two groups will be merged into a single standard [1], [194]. IEEE 802.11ad is due for completion sometime in 2012. The standard is part of the emerging array of 4G cellular technologies, and is intended to support data rates on the order of 1 Gb/s at low velocities such as walking speeds [195]. The technical contents of IEEE 802.11ad and the WiGig standard resemble the Wi-Fi standard, but recast at 60 GHz, and include provisions for beam steering to mitigate path loss of 60-GHz propagation [196]. Many of IEEE 802.11ad's and the WiGig standard's top supporters are Wi-Fi chip manufacturers [1]. SiBEAM recently announced that its future 60-GHz products will support the WiGig or merged WiGig-IEEE 802.11ad standard [1], in addition to the WirelessHD standard. A Gartner survey of future wireless technologies rated the benefit of joining the WiGig alliance as "high" noting the technology should become important for "both domestic and business purposes" [194].

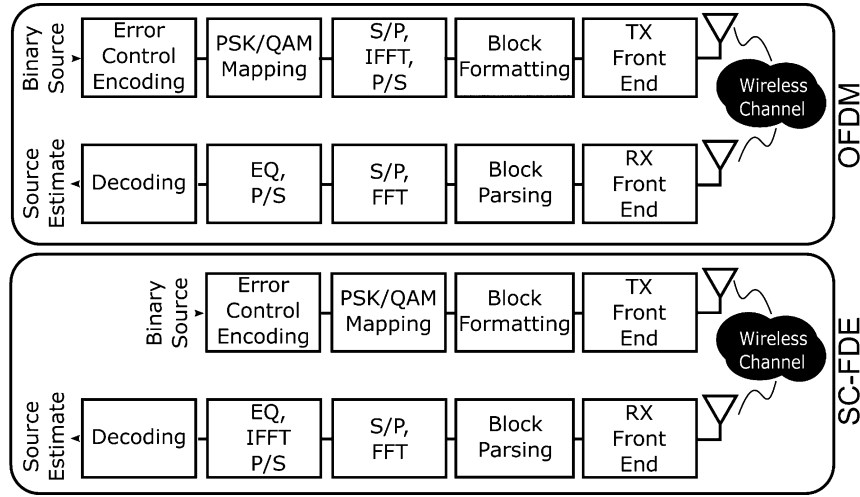
The ECMA 387 standard is intended to facilitate bulk and streaming data transfer for three device types: high-end

video/audio streaming devices for operation over a distance up to 10 m with LOS or NLOS links (type A device), economical data/video devices for LOS operation up to 3 m (type B device), and very inexpensive data-only devices for LOS operation over a 1-m range (type C device). The standard defines four frequency channels each with a bandwidth of 2.16 GHz and a symbol rate of 1.78 Gs/s [197] to support bit rates up to 10 Gb/s. If higher data rates are required, the standard supports channel combining or bonding. The standard provides the framework for high-definition media interface protocol adaptation layer (HDMI PALs) in which a 60-GHz wireless device may operate as an intermediate network node between source and sink.

Currently, the large number of 60-GHz standards could present a major problem for device interoperability which increases consumer confusion and limits device ubiquity. For example, there is no widespread agreement on the best modulation scheme for 60-GHz devices. This is illustrated in the IEEE 802.15.3c standard, which features both SC-FDE and OFDM [6]. SC-FDE reduces the number of steps dedicated to Fourier transforms compared to OFDM, which results in lower phase noise sensitivity and reduces the need for PAs to operate in "backoff" (i.e., unsaturated low-efficiency output power levels). However, OFDM provides better overall performance in highly frequency selective channels [6]. One primary reason for different modulation schemes represented by OFDM and SC-FDE in IEEE 802.15.3c is that simple short range (i.e., 1 m) direct LOS mm-wave radios have very different hardware design requirements than radios intended for longer range (i.e., up to 10 m to 1 km) LOS/NLOS operation. Fig. 23 from [6] illustrates the differences between OFDM and SC-FDE. Table 15 explains the differences between single carrier, OFDM, and SC-FDE [198].

While 60-GHz technology is not yet characterized sufficiently to give a comprehensive comparison in terms of power consumption and data rate versus range for different standards, it is possible to make comparisons based on a several simple principles. For example, it is of interest to estimate the ratio of the consumed power  $P_{\text{consumed}}$  to the data rate of a 60-GHz radio.

We now derive a quality metric that can be used to compare the data rate per consumed power for any wireless RF device. The units of this quality metric are bits-per-second-per-Watt (B/S/W). Consider a homodyne transmitter that is composed of a baseband processor, mixer, oscillator, power amplifier, and antenna. The transmitter accepts baseband signals from the baseband processor into its mixer's IF port, and any baseband signal is mixed up directly to the carrier frequency at the mixer's RF port and sent through a power amplifier and antenna. Signals are radiated out to a receiver from the antenna. A local oscillator provides an LO signal at the RF carrier frequency that is used by the mixer to convert the baseband signal up to the carrier frequency. Homodyne transmitters (also known as direct conversion



**Fig. 23.** From [6]. OFDM and SC-FDE are two modulation schemes in the IEEE 802.15.3c standard. In practice, the wide array of optional modes for 60-GHz devices may create problems for device interoperability.

transmitters) are very popular for millimeter-wave 60-GHz radios, as discussed in Section II (e.g. see reference [34]), and may be implemented in less area and more cheaply than a heterodyne architecture while avoiding image frequency problems associated with heterodyne implementations. Our goal is to determine the data rate per power using this transmitter paired with a lossless receiver. We now determine a mathematical expression, equation (32), that may be used to compare the data rate per power of different standards (e.g. IEEE 802.15.3c) and circuits. The expression may also be used to optimize such parameters as the signal-to-noise-ratio and channel bandwidth to achieve the best possible data rate per power for a given scenario, involving any transmitter-receiver separation distance. The expression allows engineers to explore the tradeoffs, in terms of data rate per power, of different circuit implementations of any radio standard, including 60-GHz standards such as IEEE 802.15.3c or the WiGig standard.

The efficiency of the power amplifier (PA) may be written as

$$\eta_{PA} = \frac{P_{RF}^{PA}}{P_{RF}^{PA} + P_{NON-RF}^{PA}} \quad (7)$$

where  $P_{RF}^{PA}$  is the RF (radio frequency) signal power at the output of the PA, and  $P_{NON-RF}^{PA}$  is the portion of the dc power consumed by the PA but not radiated usefully. It is important to understand that the total dc power used by the power amplifier is equal to  $P_{RF}^{PA} + P_{NON-RF}^{PA}$ .  $P_{NON-RF}^{PA}$  may be written using

$$P_{NON-RF}^{PA} = P_{RF}^{PA} \left( \frac{1}{\eta_{PA}} - 1 \right). \quad (8)$$

**Table 15** From [198]. The Differences Between Various Modulations Proposed for 60-GHz Applications

Modulation	Advantages	Disadvantages
Constant Envelope	Low PAPR; operates with simpler RF components	Low spectral efficiency; hard to equalize
SC-FDE	Requires lower precision ADCs; lower PAPR; can operate with little or no coding	IFFT/FFT both at receiver (asymmetry); cannot capture frequency diversity as well
OFDM	Best spectral efficiency; offers best potential for interference handling	Requires linear PA, backoff; requires robust FEC; sensitive to phase noise

In (8), if the efficiency of the power amplifier were 100%, then all of the dc power used by the power amplifier would transfer to usefully radiated RF power.

Similarly we may write the efficiency of the mixer,  $\eta_{\text{MIX}}$ , according to

$$\eta_{\text{MIX}} = \frac{P_{\text{RF}}^{\text{MIX}}}{P_{\text{RF}}^{\text{MIX}} + P_{\text{NON-RF}}^{\text{MIX}}} \quad (9)$$

where  $P_{\text{NON-RF}}^{\text{MIX}}$  is the power used or wasted by the mixer that is not part of the mixer's RF output power and  $P_{\text{RF}}^{\text{MIX}}$  is the useful output RF power. The mixer could be either active or passive. If the mixer is passive, then there is no dc power consumed by the mixer. But, the mixer will still waste or use power that does not contribute to the RF output power. If the mixer is active, then it will use some dc power, only a portion of which will be transformed into usefully radiated RF power. If  $P_{\text{NON-RF}}^{\text{MIX}}$  were zero, then the mixer would have a 100% efficiency. We may find the non-RF power wasted or used by the mixer using

$$P_{\text{NON-RF}}^{\text{MIX}} = P_{\text{RF}}^{\text{MIX}} \left( \frac{1}{\eta_{\text{MIX}}} - 1 \right). \quad (10)$$

For the transmit antenna, just as for a passive mixer, there is generally no dc power. But, the antenna will dissipate power that is not radiated usefully. We may therefore write the efficiency of the antenna as

$$\eta_{\text{ANT}} = \frac{P_{\text{RF}}^{\text{ANT}}}{P_{\text{RF}}^{\text{ANT}} + P_{\text{LOSS}}^{\text{ANT}}} \quad (11)$$

where  $\eta_{\text{ANT}}$  is the efficiency of the transmit antenna,  $P_{\text{RF}}^{\text{ANT}}$  is the RF power that is usefully radiated by the transmit antenna, and  $P_{\text{LOSS}}^{\text{ANT}}$  is all the power that is dissipated by the antenna but not radiated. If  $P_{\text{LOSS}}^{\text{ANT}}$  were zero, then the antenna would have an efficiency of 100% and would radiate all its input power. We may find  $P_{\text{LOSS}}^{\text{ANT}}$  using

$$P_{\text{LOSS}}^{\text{ANT}} = P_{\text{RF}}^{\text{ANT}} \left( \frac{1}{\eta_{\text{ANT}}} - 1 \right). \quad (12)$$

The efficiency of the entire radio, denoted as  $\eta_{\text{radio}}$ , may be written as

$$\eta_{\text{radio}} = \frac{P_{\text{RF}}^{\text{RADIO}}}{P_{\text{RF}}^{\text{RADIO}} + P_{\text{NON-RF}}^{\text{PA}} + P_{\text{NON-RF}}^{\text{MIX}} + P_{\text{LOSS}}^{\text{ANT}} + P_{\text{BB}} + P_{\text{OSC}}} \quad (13)$$

where  $P_{\text{RF}}^{\text{RADIO}}$  is the RF output power of the entire homodyne transmit radio,  $P_{\text{BB}}$  is the power used by the baseband components, and  $P_{\text{OSC}}$  is the power used by the oscillator. Equation (13) states that the efficiency of the transmit radio would be 100% if the mixer, power amplifier, and antenna wasted zero power, and if zero power were required for the baseband components and oscillator.  $P_{\text{RF}}^{\text{RADIO}}$  may be written as

$$P_{\text{RF}}^{\text{RADIO}} = P_{\text{IN}}^{\text{MIX}} G^{\text{MIX}} G^{\text{PA}} G^{\text{ANT}} \quad (14)$$

where  $G^{\text{MIX}}$  is the mixer's conversion gain (or loss),  $G^{\text{PA}}$  is the gain of the power amplifier, and  $G^{\text{ANT}}$  is the gain of the antenna.  $P_{\text{IN}}^{\text{MIX}}$  is the input signal power to the mixer from the baseband components. Similarly, we may write  $P_{\text{RF}}^{\text{ANT}}$ ,  $P_{\text{RF}}^{\text{PA}}$ , and  $P_{\text{RF}}^{\text{MIX}}$ , the output RF powers of the antenna, power amplifier, and mixer, respectively, as

$$P_{\text{RF}}^{\text{ANT}} = P_{\text{RF}}^{\text{RADIO}} \quad (15)$$

$$P_{\text{RF}}^{\text{PA}} = P_{\text{IN}}^{\text{MIX}} G^{\text{MIX}} G^{\text{PA}} = \frac{P_{\text{RF}}^{\text{RADIO}}}{G^{\text{ANT}}} \quad (16)$$

$$P_{\text{RF}}^{\text{MIX}} = P_{\text{IN}}^{\text{MIX}} G^{\text{MIX}} = \frac{P_{\text{RF}}^{\text{RADIO}}}{G^{\text{ANT}} G^{\text{PA}}} \quad (17)$$

where  $P_{\text{RF}}^{\text{ANT}}$  is the RF output power of the transmit antenna,  $P_{\text{RF}}^{\text{PA}}$  is the RF output power of the PA, and  $P_{\text{RF}}^{\text{MIX}}$  is the RF output power of the mixer. From (8), (10), (12), and (15)–(17), we may write

$$P_{\text{LOSS}}^{\text{ANT}} = P_{\text{RF}}^{\text{RADIO}} \left( \frac{1}{\eta_{\text{ANT}}} - 1 \right) \quad (18)$$

$$P_{\text{NON-RF}}^{\text{PA}} = \frac{P_{\text{RF}}^{\text{RADIO}}}{G^{\text{ANT}}} \left( \frac{1}{\eta_{\text{PA}}} - 1 \right) \quad (19)$$

$$P_{\text{NON-RF}}^{\text{MIX}} = \frac{P_{\text{RF}}^{\text{RADIO}}}{G^{\text{ANT}} G^{\text{PA}}} \left( \frac{1}{\eta_{\text{MIX}}} - 1 \right) \quad (20)$$

Therefore, we may re-write the efficiency of the radio in (13) as (21), shown at the bottom of the next page.

To verify (21), consider the case in which the radio wasted no power for baseband processing or the oscillator, and in which the antenna, mixer, and power amplifier were all 100% efficient. In this case, the efficiency of the radio, as given by (21) is 100%. Also, note that the efficiency of the antenna,  $\eta_{\text{ANT}}$ , the efficiency of the power amplifier,  $\eta_{\text{PA}}$ , and the efficiency of the mixer,  $\eta_{\text{MIX}}$ , are all less than or equal to unity so that the computed efficiency of the radio can never be negative.

The denominator of equation (21) represents the total consumed power of the radio, including the total radiated

power and power that is not radiated to the receiver. We shall denote this power as

$$p_{\text{consumed}}^{\text{RADIO}} = p_{\text{RF}}^{\text{RADIO}} \left( 1 + \left( \frac{1}{\eta_{\text{ANT}}} - 1 \right) + \frac{1}{G_{\text{ANT}}} \left( \frac{1}{\eta_{\text{PA}}} - 1 \right) + \frac{1}{G_{\text{ANT}} G_{\text{PA}}} \left( \frac{1}{\eta_{\text{MIX}}} - 1 \right) \right) + p^{\text{BB}} + p^{\text{OSC}}. \quad (22)$$

Now, for a given signaling scheme the total data rate may be found by (23) using the spectral efficiency of the signaling scheme used and the channel bandwidth

$$R = \eta_{\text{sig}} B \quad (23)$$

where  $\eta_{\text{sig}}$  is the spectral efficiency of the signaling scheme (in Bits/s/Hz),  $B$  is the channel bandwidth (in Hz) and  $R$  is the data rate (in Bits/s).

Consider a receiver that is a distance,  $D$ , from the transmitter. We may estimate the received power as

$$p_{\text{RX}}^{\text{RECEIVED}} = p_{\text{RF}}^{\text{RADIO}} \times PL \times G_{\text{TX}} \times G_{\text{RX}} \quad (24)$$

where  $p_{\text{RF}}^{\text{RADIO}}$  is given by (14),  $PL$  is the path loss between the transmitter and receiver,  $G_{\text{RX}}$  is the gain of the receiver, and  $G_{\text{TX}}$  is the gain of the transmitter. Note that the symbol “ $\times$ ” has been used in (24) to represent multiplication and is present for visual clarity. The total gain of the transmitter,  $G_{\text{TX}}$ , is given by

$$G_{\text{TX}} = G^{\text{MIX}} G^{\text{PA}} G^{\text{ANT}}. \quad (25)$$

The pathloss,  $PL$ , may be estimated using Friis free-space formula

$$PL = \left( \frac{\lambda}{4\pi D} \right)^2 = \left( \frac{c}{4\pi f_{\text{osc}} D} \right)^2 \quad (26)$$

where  $\lambda$  is the wavelength of the carrier frequency (in meters),  $D$  is the separation between the transmitter and receiver (in meters), and  $f_{\text{osc}}$  is the carrier frequency (in Hz), which is also the output frequency of the oscillator. We arrived at (26) by using the fact

$$c = \lambda f_{\text{osc}} \quad (27)$$

where  $c$  is the speed of light in free space (approximately 3e8 m/s).

For a given modulation scheme, there is a minimum signal-to-noise power ratio required at the receiver to ensure an acceptable bit-error-rate. We denote this minimum signal-to-noise ratio as  $\text{SNR}_{\text{MIN}}$ . The total noise power  $p_{\text{RX}}^{\text{NOISE}}$  available at the receiver may be found according to

$$p_{\text{RX}}^{\text{NOISE}} = KTB_{\text{RX}} \quad (28)$$

where  $K$  is Boltzman’s constant (1.38e-23 J/K),  $T$  is the receiver temperature (in degrees Kelvin), and  $F_{\text{RX}}$  is the noise factor of the receiver. We may use  $\text{SNR}_{\text{min}}$  and the noise power at the receiver in (28) to find the minimum received power to ensure an acceptable bit-error-rate

$$p_{\text{RX,min}}^{\text{RECEIVED}} = \text{SNR}_{\text{min}} KTB_{\text{RX}}. \quad (29)$$

We may then use (29) and (24) to find the minimum transmitted power from the transmitter radio to ensure an acceptable bit-error-rate

$$p_{\text{RF,min}}^{\text{RADIO}} = \frac{p_{\text{RX,min}}^{\text{RECEIVED}}}{PL \times G_{\text{TX}} \times G_{\text{RX}}} = \frac{\text{SNR}_{\text{min}} KTB_{\text{RX}} (4\pi f_{\text{osc}} D)^2}{c^2 \times G_{\text{TX}} \times G_{\text{RX}}}. \quad (30)$$

Assume the radio radiates exactly the minimum required power to achieve an acceptable bit-error-rate,

$$\eta_{\text{radio}} = \frac{p_{\text{RF}}^{\text{RADIO}}}{p_{\text{RF}}^{\text{RADIO}} \left( 1 + \left( \frac{1}{\eta_{\text{ANT}}} - 1 \right) + \frac{1}{G_{\text{ANT}}} \left( \frac{1}{\eta_{\text{PA}}} - 1 \right) + \frac{1}{G_{\text{ANT}} G_{\text{PA}}} \left( \frac{1}{\eta_{\text{MIX}}} - 1 \right) \right) + p^{\text{BB}} + p^{\text{OSC}}} \quad (21)$$



as given by (30). We may then use (30) in (22) to find the minimum total power consumed by the transmitter to ensure an acceptable bit-error-rate

$$p_{\text{consumed}}^{\text{RADIO}} = \frac{\text{SNR}_{\min} K T B F_{\text{RX}} (4\pi f_{\text{osc}} D)^2}{c^2 \times G_{\text{TX}} \times G_{\text{RX}}} \times \left( 1 + \left( \frac{1}{\eta_{\text{ANT}}} - 1 \right) + \frac{1}{G_{\text{ANT}}} \left( \frac{1}{\eta_{\text{PA}}} - 1 \right) + \frac{1}{(G_{\text{ANT}} G_{\text{PA}})} \left( \frac{1}{\eta_{\text{MIX}}} - 1 \right) \right) + p^{\text{BB}} + p^{\text{OSC}}. \quad (31)$$

Taking the ratio of (23)–(31), we find that the bit rate per power, in Bits/s/W, is given by (32), shown at the bottom of the page.

This is a general result that can be applied to many different cases. The parameters of (32) can be optimized to maximize the data rate per power and also allow one to determine the impact of each component in an integrated circuit implementation. Equation (32) allows engineers to explore the tradeoffs between different circuit implementations of standards, and to compare different standards in terms of data rate per power. By correctly applying the parameters for a given situation (e.g. for the efficiencies of the various components in the transmitter), an engineer can use (32) to determine how best to maximize data rate per power. This is important, especially as the industry strives for higher data rates with longer battery life. For example, consider the case in which the baseband processor and the oscillator both require a very small amount of power. In this case, we can let  $p^{\text{BB}} + p^{\text{OSC}}$  approach zero to find (33), shown at the bottom of the page.

We see from (33) that for a transmitter with very little power dedicated to baseband processing or the oscillator, the data-rate per consumed power is approximately independent of bandwidth. Equation (33) indicates the efficiency of the antenna is more important than the efficiency of the power amplifier or mixer, since the impact of the mixer and power amplifier efficiencies are reduced by the gain of the antenna. Similarly, the gain of the power amplifier reduces the impact of mixer efficiency. This indicates that a poor-efficiency component will have the worst impact if it appears *after* the signal has been significantly amplified.

Consider the case in which the baseband processor power dominates the power of the RF chain, e.g. for a media-processing device used in a short-range peer-to-peer application. In this case, we may estimate the bit rate per power by using (32) and allowing the first term in the denominator to approach zero (as we assume it is much less than the second term)

$$\frac{R}{p_{\text{consumed}}^{\text{RADIO}}} = \frac{\eta_{\text{sig}} B}{(p^{\text{BB}} + p^{\text{OSC}})} \quad (34)$$

In this case, data rate per consumed power improves linearly with bandwidth and spectral efficiency. Furthermore, for a given minimum signal to noise ratio, there is an upper bound on the spectral efficiency,  $\eta_{\text{sig}}$ , according to Shannon's law:

$$\eta_{\text{sig}} \leq \log_2(1 + \text{SNR}) \quad (35)$$

where SNR is the actual signal to noise ratio at the receiver. SNR may in general be greater than  $\text{SNR}_{\min}$ . Let us replace  $\text{SNR}_{\min}$  in (32) with the actual signal to noise ratio at the receiver, SNR. In (29), this simply assumes that the received power is greater than the minimum received

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$$\frac{R}{p_{\text{consumed}}^{\text{RADIO}}} = \frac{\eta_{\text{sig}} B \times c^2 \times G_{\text{TX}} \times G_{\text{RX}}}{\text{SNR}_{\min} K T B F_{\text{RX}} (4\pi f_{\text{osc}} D)^2 \left( 1 + \left( \frac{1}{\eta_{\text{ANT}}} - 1 \right) + \frac{1}{G_{\text{ANT}}} \left( \frac{1}{\eta_{\text{PA}}} - 1 \right) + \frac{1}{G_{\text{ANT}} G_{\text{PA}}} \left( \frac{1}{\eta_{\text{MIX}}} - 1 \right) \right) + (p^{\text{BB}} + p^{\text{OSC}}) \times c^2 \times G_{\text{TX}} \times G_{\text{RX}}} \quad (32)$$


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$$\frac{R}{p_{\text{consumed}}^{\text{RADIO}}} = \frac{\eta_{\text{sig}} \times c^2 \times G_{\text{TX}} \times G_{\text{RX}}}{\text{SNR}_{\min} K T B F_{\text{RX}} (4\pi f_{\text{osc}} D)^2 \left( 1 + \left( \frac{1}{\eta_{\text{ANT}}} - 1 \right) + \frac{1}{G_{\text{ANT}}} \left( \frac{1}{\eta_{\text{PA}}} - 1 \right) + \frac{1}{G_{\text{ANT}} G_{\text{PA}}} \left( \frac{1}{\eta_{\text{MIX}}} - 1 \right) \right)} \quad (33)$$

**Table 16** Companies Supporting, Involved, or With Access to Each of the Developing 60-GHz Standards

WiGig (IEEE802.11ad/VHT and WiGig standards)	WirelessHD	ECMA 387 (ECMA Members)
Agilent Technologies AMD Atheros Communications Beam Networks Broadcom Corporation Dell, Inc. Intel Corporation LG Electronics Inc. Marvell International LTD. MediaTek Inc. Microsoft Corporation NEC Corporation Nokia Corporation NVIDIA NXP Panasonic Corporation Realtek Ralink Technology Corp. Samsung Electronics SK Telecom STMicroelectronics Tensormcom, Inc. Texas Instruments Toshiba TMC Wilocity	Abocom Agilent ALPS Electronics (USA), Inc Anritsu Azurewave Technologies Beam Networks Best Buy, Inc. Broadcom Corporation ClearSpeed Technologies D&M Holdings Eastech Electronics ETRI Korea Funai Electric Co., Ltd Gefen Hitachi Intel Corporation LG Electronics LG Innotek MediaTek NXP Semiconductor NEC Corporation Onkyo Panasonic Corporation Quantum Data Rohde & Schwarz Royal Philips Electronics Samsung Seiko Epson Sharp Electronics SiBEAM, Inc. Silicon Image, Inc Sony Corporation ST Microelectronics TDK Corporation Tektronix Toshiba Corporation Yamaha Corporation Zoran	AMD Google Hewlett Packard Hitachi IBM Intel Microsoft Philips Samsung Sony Toshiba Yahoo Apple (Associate) NEC (Associate) Panasonic (Associate)

power needed to ensure an adequate bit-error-rate. We may use (35) in (32) to find (36), shown at the bottom of the page.

Equation (36) is useful for determining an upper bound on the data rate per power for a given SNR. We may also use (36) to determine an optimum SNR to

$$\begin{aligned}
& \frac{R}{p_{\text{consumed}}^{\text{RADIO}}} \\
& \leq \frac{\log_2(1 + \text{SNR})B \times c^2 \times G_{\text{TX}} \times G_{\text{RX}}}{\text{SNR} \times KTB_{\text{RX}}(4\pi f_{\text{osc}}D)^2 \left(1 + \left(\frac{1}{\eta_{\text{ANT}}} - 1\right) + \frac{1}{G_{\text{ANT}}} \left(\frac{1}{\eta_{\text{PA}}} - 1\right) + \frac{1}{G_{\text{ANT}}G_{\text{PA}}} \left(\frac{1}{\eta_{\text{MIX}}} - 1\right)\right) + (p^{\text{BB}} + p^{\text{OSC}}) \times c^2 \times G_{\text{TX}} \times G_{\text{RX}}}
\end{aligned} \tag{36}$$

$$D_{\text{SNR}} \left[ \frac{\log_2(1 + \text{SNR}) B \times c^2 \times G_{\text{TX}} \times G_{\text{RX}}}{\text{SNR} \times K T B F_{\text{RX}} (4\pi f_{\text{osc}} D)^2 \left( 1 + \left( \frac{1}{\eta_{\text{ANT}}} - 1 \right) + \frac{1}{G_{\text{ANT}}} \left( \frac{1}{\eta_{\text{PA}}} - 1 \right) + \frac{1}{G_{\text{ANT}} G_{\text{PA}}} \left( \frac{1}{\eta_{\text{MIX}}} - 1 \right) \right) + (P^{\text{BB}} + P^{\text{OSC}}) \times c^2 \times G_{\text{TX}} \times G_{\text{RX}} \right]} \right] = 0 \quad (37)$$

achieve the best possible data rate per power for the given transmitter and receiver parameters. For example, we may differentiate (36) with respect to the actual SNR and set the result to zero to find an optimum SNR in terms of data rate per power in (37), shown on top of the page.

While (37) does not have a closed form solution due to the  $\log$  dependence, the result may be found numerically for a given set of parameters. This is useful for determining the difference between the actual SNR and the optimum SNR in terms of data rate per power, and may be used to set signaling rates in a device based on channel conditions. A similar procedure may be used with (32) to determine the optimum bandwidth to optimize data rate per power for a given spectral efficiency. Also, using (32), we may compare different standards and radio implementations in terms of their respective bit rates per power.

Millimeter-wave 60-GHz wireless technology will enter the consumer marketplace in a major way over the next few years, and will usher in a new era of wireless communications that enables multi-Gb/s data transfers. Major companies have developed prototype 60-GHz devices based on one of the developing 60-GHz standards: WirelessHD, IEEE 802.15.3c, ECMA 387, IEEE 802.11.ad, and the WiGig standard [1], [12], [192]. Large industry consortia, including WiGig and WirelessHD are actively and aggressively marketing 60-GHz devices as the best means to deliver high-definition content wirelessly over short distances. Table 16 summarizes the companies supporting or involved in ECMA 387, IEEE 802.15.3c, and IEEE 802.11ad and the WiGig standard.

## XII. CONCLUSION

60-GHz wireless communications technology may be the world's first massively broadband mm-wave communications technology. The data rates and bandwidths available at 60 GHz are staggering—this is readily seen by summing the bandwidths of all commercial wireless systems ever built to date, including every television broadcast channel, AM/FM radio station, Wi-Fi, cellular, satellite, and WiMAX band, and then noting that the total spectrum occupancy of all these services combined still represents only a fraction of the total bandwidth available at 60 GHz. The 60-GHz movement has already received tremendous industry interest and support, and

this will encourage federal regulators to allocate large frequency bands at even higher frequencies. Today's early progress at 60 GHz will build the foundations for many future systems at higher mm-wave and subterahertz bands. The availability of such massive bandwidths and subterahertz carrier frequencies will require communications engineers to rethink wireless approaches while learning how to fabricate devices in silicon, and circuit and antenna designers will need to become more aware of communication requirements.

Since the release of 60-GHz spectrum by the FCC and other governmental bodies, tremendous progress has been made toward the realization of highly integrated 60-GHz radios for inexpensive and potentially ubiquitous consumer adoption. Progress in the areas of on-chip antennas, PAs, LNAs, VCOs, mixers, ADCs, and mm-wave channel characterization will result in widespread commercial 60-GHz products as early as 2012. Progress is needed in antenna integration, lower power components, improved baseband and beamforming processing, and in creating more targeted and streamlined standards to bring 60-GHz and future mm-wave wireless devices to consumers. This paper has offered a comprehensive view of how massively broadband devices will transform access to content, and has provided a tutorial of many crucial concepts needed to design and implement subterahertz communications devices of the future, including circuit design, on-chip and in-package antennas, 60 GHz and subterahertz communication concepts, and propagation. We also derived a mathematical formulation of the ratio of the data rate to consumed power for an arbitrary radio system using any modulation or signaling scheme. The analysis allows engineers to compare power versus data rate tradeoffs for all future massively broadband wireless communication circuits and systems, for 60 GHz and above. For example, the mathematical expression that results from the analysis may be applied to future communication technologies such as short-range peer-to-peer applications at 120, 183, 325, or 380 GHz, or longer range applications at 77 and 240 GHz. As devices become more sophisticated and users rely on their devices for more functionality, it will be crucial to optimize the efficiency of devices in terms of data rate per consumed power. Doing so will provide users with the best possible data rates for the longest possible battery life. Over the next decade, the advances in mm-wave CMOS technology and movement to higher carrier frequencies will greatly impact the way people consume media and how wireless networks and systems are designed and deployed. ■

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