Subharmonic 220- and 320-GHz SiGe HBT Receiver Front-Ends

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***Abstract*—Monolithically integrated 220- and 320-GHz receiver front-ends manufactured in an engineering version of an $f_T/f_{\max} = 280/435$-GHz SiGe technology are presented. Subharmonic mixing is provided by a Gilbert cell with stacked switching quads fed by quadrature 110/160-GHz local oscillator (LO) signals. The 220-GHz version of the front-end is equipped with an integrated LNA with a measured 15-dB gain and 28-GHz bandwidth. This front-end yields a conversion gain of 16 dB, an 18-dB single-sideband (SSB) noise figure (NF), and a 30-GHz bandwidth when pumped with a 0-dBm 110-GHz LO signal. The 320-GHz version of the front-end omits the low-noise amplifier and features an integrated $\times 9$ LO multiplier chain to facilitate operation and characterization. A conversion gain of -14 dB and a 36-dB SSB NF is obtained over the 313-to-328-GHz frequency range. The presented circuits demonstrate that a fully integrated receiver front-end can be implemented up to submillimeter-wave frequencies in an SiGe HBT technology.**

***Index Terms*—Heterojunction bipolar transistors (HBTs), millimeter-wave receivers, monolithic microwave integrated circuit (MMIC) frequency converters, silicon.**

I. Introduction

MILLIMETER-WAVE systems are used in an increasing number of commercial, defense, and security-related applications, such as high-speed wireless communication and millimeter-wave imaging. Although most of the present systems operate below 100 GHz, the use of the 220–320-GHz WR-03 waveguide band would offer increased communication bandwidth and improved imaging resolution in such systems. This band has recently become more accessible with the availability of low-cost monolithically integrated sources in CMOS [1] and SiGe heterojunction bipolar transistor (HBT) [2] technologies. Receiver front-ends with excellent performance can be implemented in this frequency range using Schottky-diode mixers in waveguide technology, with below 10 dB of conversion loss and noise figure (NF) at 330 GHz reported in [3]. However, array implementations of receivers based on discrete diodes and waveguide technology remain space consuming and costly. Hence, monolithically integrated receiver front-ends are typically needed in millimeter-wave system designs driven by low-cost requirements or a need for a large number of parallel channels [4].

In III–V technologies, integrated receivers incorporating low-noise amplifiers (LNAs), mixers, and optional local-oscillator (LO) multipliers have been demonstrated at 220 GHz [5], [6]. Improved SiGe-HBT process technologies with a present $f_{\max}$ of 500 GHz [7] do, however, allow similar circuits to be implemented in silicon BiCMOS technology, thus benefiting from the higher degree of integration, smaller die size, and lower cost in large quantities. Conventional super-heterodyne and zero-IF receivers and receiver front-ends based on SiGe HBTs have been demonstrated at 160 GHz in [8] and [9], as well as at 170 GHz in [10]. The fundamental down-conversion mixers used in these receivers do, however, require higher LO-drive power with increased frequency due to the input *RC*-time constants of the switching transistors. Since the on-chip generation of a high-power LO signal is difficult and power consuming at high millimeter-wave frequencies, it becomes increasingly difficult to obtain the saturated switching of the mixing devices needed for efficient low-noise downconversion.

Harmonic-mixer-based receiver front-ends allow the LO to be generated at a lower frequency than the input RF signal and have been successfully demonstrated up to a frequency of 825 GHz [11] in SiGe-HBT technology. However, such mixers tend to suffer from a relatively low conversion gain and high NF due to an inefficient mixing process, which relies on generation of the required LO harmonics by the nonlinearities of the transistor itself. As an alternative, a subharmonic downconversion architecture, where the LO is provided at half the RF frequency, can be implemented with a two-stage mixing process. A modified Gilbert cell with two stacked mixer cores [12] driven with quadrature LO signals is commonly used as a subharmonic down-converter in bipolar technologies [13]. This combination of two cascaded fundamental-frequency mixers for a two-stage downconversion process does not suffer from the same conversion-gain and noise limitations as harmonic mixers based on higher order nonlinearities. Millimeter-wave implementations of such downconversion mixers include a 94-GHz receiver front-end [14], a 122-GHz mixer [15] and receiver [16], as well as a 220-GHz receiver front-end [17].

In this paper, we elaborate on the design and results of a 220-GHz LNA/mixer receiver front-end, originally presented in [17], which has been manufactured in an $f_T/f_{\max} = 280/435$ GHz SiGe-HBT technology. Additionally, a 320-GHz implementation of this mixer with an integrated LO frequency multiplier chain is presented. These

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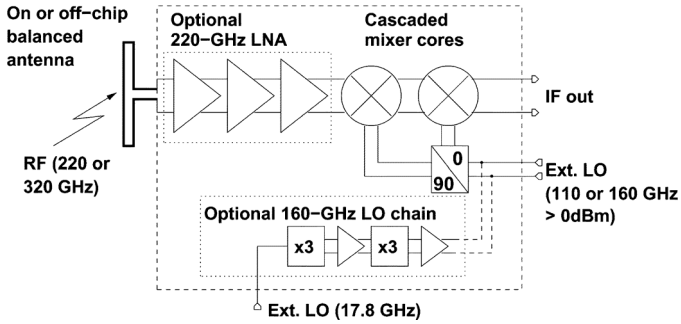

Fig. 1. Block diagram of the monolithically integrated subharmonic receiver front-end. The three-stage 220-GHz LNA is followed by two cascaded mixer cores pumped by quadrature LO signals in order to obtain subharmonic mixing. The LO signal is either provided from an external source, or in the case of the 320-GHz receiver, an on-chip frequency multiplier chain.

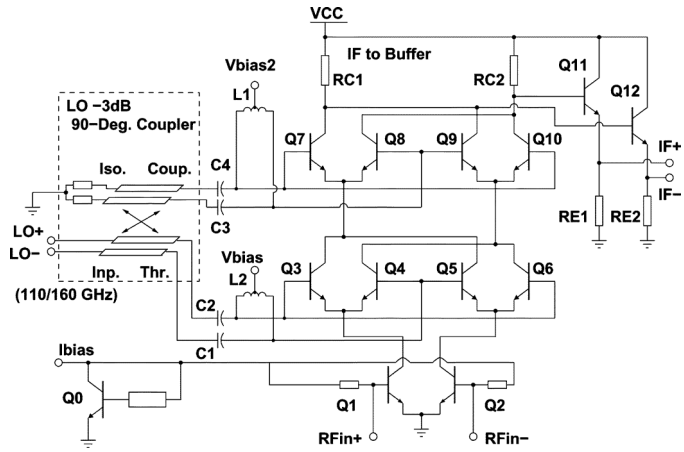

Fig. 2. Schematic diagram of the subharmonic Gilbert-cell mixer. Two stacked mixer quads driven with quadrature LO signals provide subharmonic mixing.

circuits demonstrate that receivers based on a conventional low-frequency subharmonic downconversion architecture can be successfully implemented up to submillimeter-wave frequencies. Section II describes the circuit design of the subharmonic 220- and 320-GHz mixer, as well as the three-stage differential 220-GHz LNA. In Section III, details about the manufacturing and layout of the circuits are provided. The characterization setup and results are presented in Sections IV and V, respectively, whereas conclusions are given in Section VI.

II. Circuit Design

A modular architecture has been implemented for the monolithically integrated 220/320-GHz subharmonic receiver front-end, as shown in Fig. 1. The input of the front end is differential and can be directly interfaced with balanced on-chip antennas such as folded-dipole radiators. For single-ended characterization in a wafer-probing environment, a version of the circuit with an on-chip Marchand balun is used at the RF port. A three-stage differential LNA is integrated in the 220-GHz version of the circuit to boost the conversion gain and reduce the cascaded system NF of the front end. This LNA is absent in the 320-GHz version of the circuit due to the low available gain of the HBT devices at this frequency.

The subharmonic differential 110/160-GHz LO signal is provided externally through an integrated Marchand balun. In the case of the 320-GHz version, the LO is provided by an integrated $\times 9$ 160-GHz frequency multiplier chain, similar to the driver circuit used for the 320-GHz frequency doubler in [2].

A. Subharmonic 220/320-GHz Mixer

The subharmonic mixer is based on a three-level multiplier, implemented by a modified Gilbert-cell equipped with stacked switching quads [12]. As suggested in [13], subharmonic mixing can be obtained by feeding the RF input signal to the first port and driving the two remaining ports with the in-phase and quadrature components of the LO signal according to the trigonometric identity

$$V_{\rm out} = A \times V_{\rm RF}(t)\cos(\omega_{\rm LO}t)\sin(\omega_{\rm LO}t) \quad (1)$$

$$= \frac{A}{2} \times V_{\rm RF}(t)\sin(2\omega_{\rm LO}t). \quad (2)$$

In Fig. 2, a schematic diagram of the subharmonic mixer is presented. The core of the mixer consists of the two mixing quads (Q3–Q10), equipped with minimum size transistors ($A_E = 0.12 \times 0.96\ \mu\text{m}^2$) each biased at half f_T current $I_C = 1.2$ mA. This selection of device size and bias point was made to obtain saturated switching of the quads with a <5-dBm LO signal. Inductive shunt compensation of the capacitive LO-input impedance of each quad is performed by the 65-pH differential inductors L1/L2. These inductors provide a broadband reduction of the simulated LO return loss of each quad to <10 dB in a 100-Ω system. They also provide a dc-bias path from the bases of the quads to the bias nodes $V_{\rm bias} = 1.9$ V and $V_{\rm bias2} = 3$ V. The 30-fF metal–insulator–metal (MIM) coupling capacitors C1–C4 provide dc isolation of the quad bias from the LO input.

The input and output coupling to the mixer core is implemented using a conventional transconductance input stage Q1/Q2 and resistive collector loads RC1/RC2, respectively. Devices with an emitter size ($A_E = 2 \times 0.12 \times 0.96\ \mu\text{m}^2$) are used for Q1/Q2, biased at 2.4 mA through reuse of the quad quiescent current. This selection yields 8-dB input return loss of the mixer at 220 GHz in an 100-Ω system without further matching components present. The collector loads RC1/RC2 have been selected to 200 Ω through optimization in order to maximize the conversion gain at low (<10-GHz) IF frequencies and to allow a 3.6-V supply voltage with sufficient voltage headroom for the collectors of the Q7–Q10 devices. The differential IF signal available at the collectors of Q7–Q10 is provided to the $A_E = 4 \times 0.12 \times 0.96\ \mu\text{m}^2$ large emitter–followers Q11/Q12. This yields a wideband IF output capable of dc to 10-GHz operation.

In contrast to the implementations described in [13], [14], and [16], the quadrature LO components are generated by a differential 90° −3-dB transmission-line coupler instead of a lumped *RC* polyphase network. A low-loss quadrature coupler can provide close to 3-dB insertion loss for each of the quadrature LO outputs, whereas the insertion loss of an *RC*-polyphase network is usually significantly higher. The implementation of an *RC* polyphase network at frequencies above 100 GHz is also challenging due to the high and often poorly modeled parasitics of

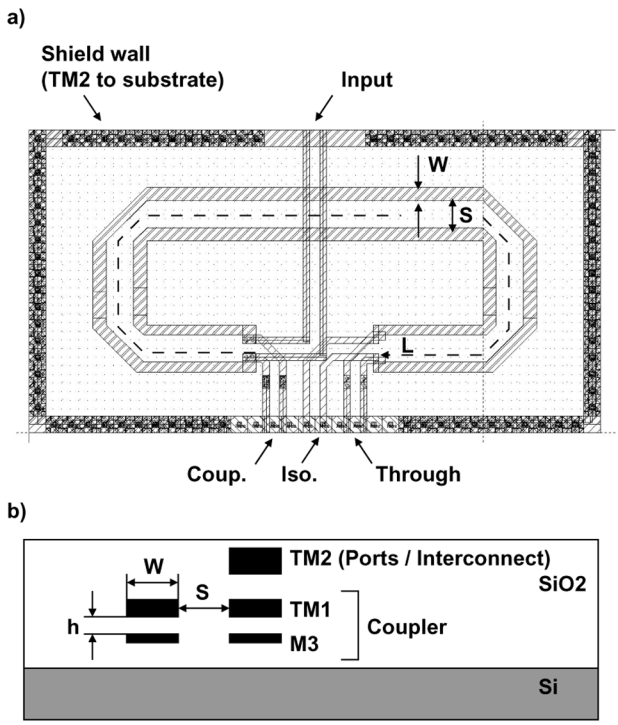

Fig. 3. (a) Layout and (b) cross section of the −3-dB 90° differential transmission line coupler used for LO quadrature generation.

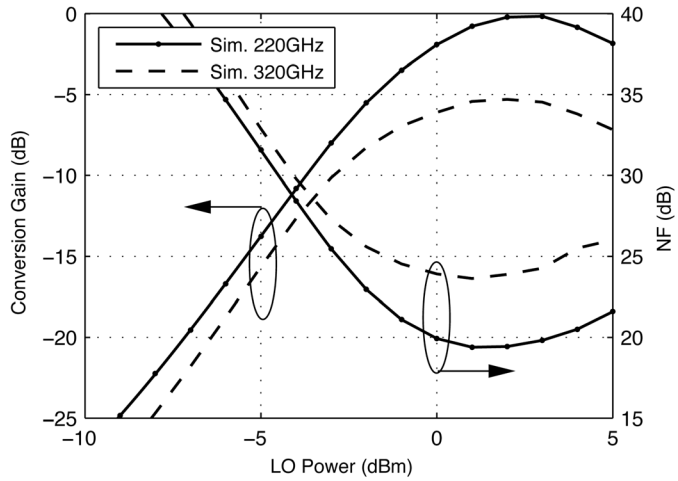

Fig. 4. Simulated conversion gain and DSB NF of the 220-GHz (solid line) and 320-GHz (dashed line) mixers.

the passives and interconnects. Compared to the branch-line hybrid used in a similar design in [15], the 90° coupler offers larger bandwidth and requires less area.

The coupler is implemented as two coupled quarter-wave long coplanar striplines (CPSs) in adjacent metal layers of the back-end metallization, as shown in Fig. 3. To obtain sufficient coupling between the transmission lines for 3-dB coupling, the broadside hybrid coupler uses a combination of the closely spaced thin M3 and thick TM1 metal layers, separated by a $h = 0.9$ μm oxide layer, instead of the thicker, but further spaced TM1/TM2 layers. The coupled lines are implemented as two parallel strips with $W = 4$ μm width and $S = 8$ μm spacing. In order to reduce the required silicon area, the coupler has been folded into a C-shape with mitered corners. The total length L corresponds to a quarter of a guided wavelength and is 260 μm for the 110-GHz version in the 220-GHz mixer and 180 μm in the 160-GHz coupler used in the 320-GHz case. With the selected dimensions, a 75-Ω impedance is obtained for the coupler ports, which provides an acceptable matching to the 100-Ω system impedance used in the rest of the circuit. The isolated port is terminated to ground with two 37.5-Ω resistors to absorb any power reflected by the LO inputs of the two mixer quads. A shield wall with via connections from the top metal layer (TM2) to substrate contacts surrounds the coupler and minimizes coupling to adjacent passives and transmission lines. Within these shield walls, filling of metal dummies is suppressed, in order to prevent parasitic loading of the coupler.

A full-wave 3-D electromagnetic (EM) (HFSS) simulation of the 110-GHz 90° coupler has been performed over the 80–140-GHz frequency range. The simulation results show a maximum 5-dB insertion loss (2-dB excess loss), a 1-dB amplitude imbalance, and a maximum of 7° of phase error. Similarly, the 160-GHz coupler provides 4.2-dB insertion loss, an amplitude error less than 1 dB, and a maximum 3° phase error over the simulated 140–220-GHz frequency range.

The simulated conversion gain and double-sideband (DSB) NFs of the 220- and 320-GHz mixers are plotted in Fig. 4 for a power sweep of the 110/160-GHz LO signals. The 220-GHz version of the mixer provide 0 dB of conversion gain with a 3-dBm LO signal. At this LO-power level, a DSB NF of 20 dB is obtained. The 320-GHz version of the mixer shares the same component values as the 220-GHz version, except for the differently designed coupler, with no further re-optimization. Hence, the low transconductance of the input devices Q1/Q2 when operated above the 280-GHz transit frequency, as well as the larger loss of the switching quads at this frequency, mainly explain the drop of the conversion gain to −5 dB. Furthermore, the simulated DSB NF increases to 24 dB with this reduced conversion gain.

The mixer is powered from a 3.6-V supply in order to provide sufficient voltage headroom for three stacked transistors. At this bias level, the current consumption of the mixer is 18 mA, which is dominated by the IF-output emitter followers.

B. 220-GHz LNA

Fig. 5 presents the schematic diagram of the three-stage differential LNA, which consists of three cascaded differential cascode stages. Since only preliminary device models of the HBTs extracted from 40-GHz measurements were available at the time of the design, a single LNA stage with 100-Ω nominal input and output impedance was designed. This stage is optimized to produce positive gain at 220 GHz in the presence of device parameter variations inherent to an engineering version of the device technology. To obtain sufficient gain in the receiver application, this stage was then replicated to form a three-stage differential amplifier.

Each stage is equipped with four $A_E = 3\times(0.12\times0.96)$ μm^2 large devices Q1–Q4 arranged in a differential cascode configuration. This device size was chosen to obtain an optimum noise

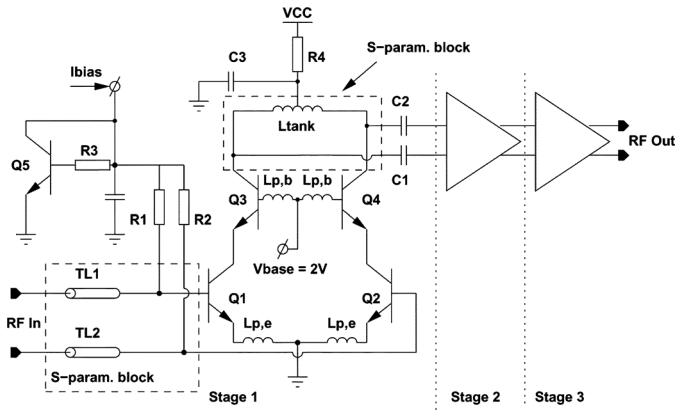

Fig. 5. LNA schematic showing the first stage of the 220-GHz differential three-stage LNA. The second and third stages are of identical design and tuning as the first stage. The circuit elements inside the dashed boxes were modeled by 3-D EM simulation and included as S-parameter blocks in the simulation.

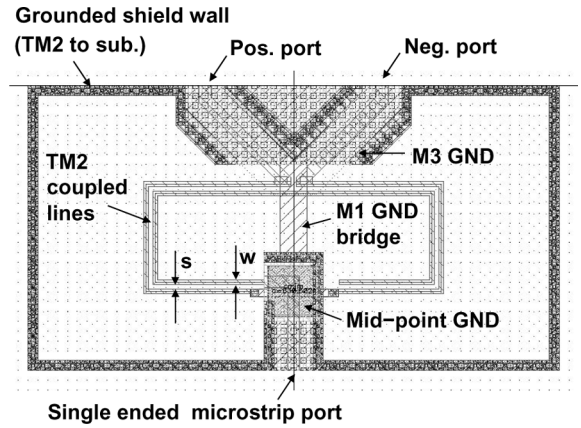

Fig. 6. Layout of the 220-GHz Marchand balun implemented in the TM2 top metal layer of the back-end. The 110- and 320-GHz baluns share the same design, but are stretched to accommodate a $\lambda_g/2$ long transmission line at the respective frequency.

match to a $2 \times 50\ \Omega$ differential source impedance without additional matching components. It simultaneously yields an acceptable input return loss of 10 dB with the post-layout parasitics included. The HBTs are biased at an $I_C = 5.4$ mA collector current, which is close to the f_T current of this device. This current was optimized to minimize the cascaded NF of the three-stage amplifier, which requires sufficient gain of each stage in addition to low-noise operation.

The output matching network of each amplifier stage consists of a conventional LC tank equipped with a single-turn differential inductor $L_{\rm tank}$ and the 14-fF series MIM capacitors C1/C2. A $24 \times 21\ \mu{\rm m}^2$ large rectangular loop with a 2-μm-wide conductor in the top TM2 metallization is used to implement the inductor. However, the 20-μm-long interconnects between the edge of the inductor and the collector nodes provide a significant part of the total inductance. Hence, full-wave EM-simulation (HFSS) results of the complete inductor and interconnect layout were included as an S-parameter block in the simulation during the design phase. Similarly, the transmission lines and interconnects at the input of the stage were modeled with an S-parameter block obtained by EM simulation of the layout. Additional parasitics in the form of the wiring inductances $L_{p,b} = 6$ pH at the critical base connection between the cascode transistors Q3/Q4 and emitter inductances $L_{p,e} = 6$ pH were also added to the post-layout simulation.

The supply voltage VCC is provided to each amplifier stage through the filter network R4/C3. These low-pass filters minimize the risk of spurious common-mode oscillations caused by coupling between the stages through the shared power supply connection. Due to the voltage drop in these filters, the VCC is selected to 3.6 V, which yields a total current consumption of 42 mA for the three-stage amplifier.

The full three-stage LNA was simulated using the available preliminary device models of the optimized HBTs. A simulated gain and NF of 14 and 13 dB were obtained in an 100-Ω system, respectively, together with an input return loss of 9.5 dB.

C. Test Benches and Circuit Break-Outs

In the targeted imaging application, the receiver front-end is intended to be used together with an on-chip differential antenna, such as a folded dipole radiator. However, since the implemented circuits were to be characterized by wafer probing, on-chip Marchand baluns were integrated at the RF and LO inputs.

The Marchand baluns are implemented with a two-wire balanced transmission line in the top (TM2) thick aluminum metallization with 2-μm conductor width w and conductor spacing s, as shown in Fig. 6. The transmission line is arranged in a rectangular loop and its length corresponds a half guided wavelength at the design frequency, with 360- and 260-μm length used at 220 and 320 GHz, respectively. The capacitance of the ground–signal–ground (GSG) pad is compensated with a shunt inductance obtained by a short grounded transmission-line stub, as described in [18]. The simulated insertion loss of the pad and balun combination is 2 dB at 220 GHz, whereas the insertion loss of the 320-GHz balun/pad combination was extracted from back-to-back characterization and found to be 4 dB.

An overview of the manufactured circuit breakouts is presented in Fig. 7. In addition to the 220-GHz down-conversion front-end, a breakout of the standalone three-stage LNA has been implemented. The 320-GHz front-end does not include an LNA since the low available gain of the current technology at this frequency make an LNA implementation impractical. Since commonly available laboratory equipment cannot provide the required $>$0-dBm 160-GHz LO drive required by the 320-GHz version of the mixer, the 160-GHz frequency multiplier chain described in [2] has been integrated with this breakout.

III. Technology and Manufacturing

The down-conversion front-end has been manufactured in an HBT-only engineering version of a 0.25-μm BiCMOS technology. For circuit fabrication, the process offers polysilicon and silicide resistors. The back-end manufacturing corresponds to the process flow and design rules of the SG25H1 [19] technology with five aluminum metal layers, including a 1-fF/$\mu{\rm m}^2$ MIM capacitor. The basic flow of the SiGe HBT module was presented first in [20] and was later implemented in IHP's 0.13-μm BiCMOS technology [21]. Starting from the HBT performance level of this technology, the peak values of $f_T/f_{\rm max}$ were improved from 240 GHz/330 GHz to 250 GHz/380 GHz in the course of a first development cycle. The corresponding

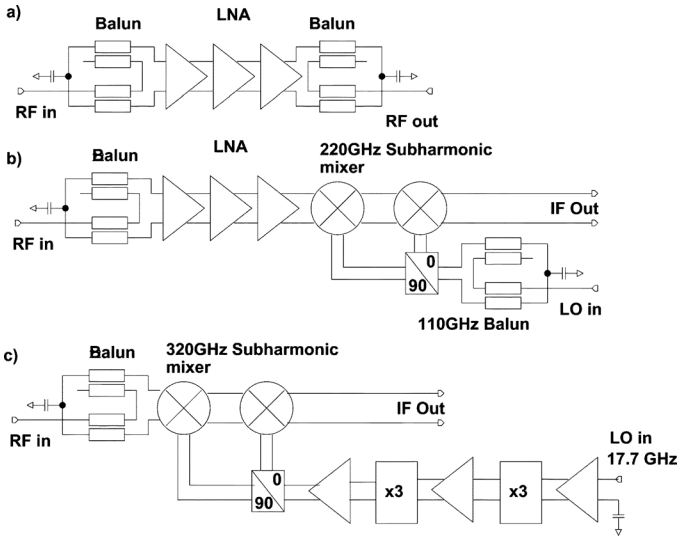

Fig. 7. (a) Breakout of the differential 220-GHz LNA with Marchand input and output baluns for wafer probing. (b) Integrated 220-GHz downconverter with baluns for the 220-GHz RF and 110-GHz LO inputs. (c) 320-GHz with input balun and integrated × 9 LO frequency multiplier chain.

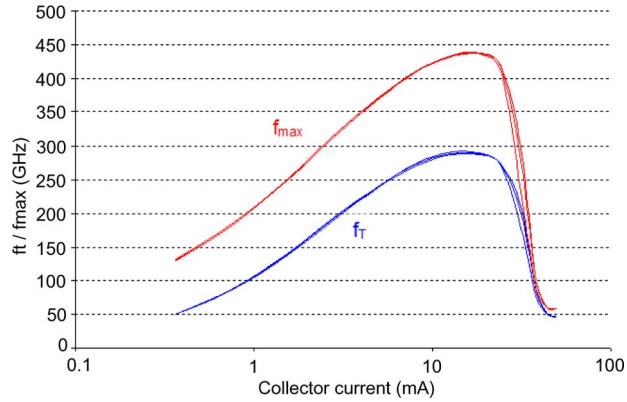

Fig. 8. f_T and $f_{\max}$ versus I_C of HBTs with eight emitters in parallel ($A_{E,\text{eff}} = 8 \times (0.12 \times 0.96)\ \mu\text{m}^2$) measured on three dies. OPEN and SHORT de-embedded small-signal current gain h_{21} and unilateral gain U versus frequency were used for extrapolation of f_T and $f_{\max}$ at 40 GHz with −20 dB per frequency decade. Measurements were performed on an E8364A (50 GHz).

high-speed capabilities of the up-graded technology were tested in runs for circuit fabrication [2], [9]. Additional progress of the high-speed performance was achieved in a second development cycle. A further reduced thermal budget, lateral device scaling (minimum emitter width was scaled from 160 to 120 nm), as well as a modified collector and emitter formation resulted in a performance enhancement to peak $f_T/f_{\max}$ values of 280 GHz/435 GHz. An optimized version of this HBT technology with even higher $f_T/f_{\max}$ values of 300 GHz/500 GHz was presented elsewhere [7].

The transistors of the second development cycle achieve a current gain of approximately 700 at $V_{\text{BE}} = 0.7$ V and demonstrate an open-base collector–emitter breakdown-voltage BV_{CEO} of 1.7 V. Open and short de-embedded small-signal current-gain h_{21} and unilateral gain U were used for the extrapolation of f_T and $f_{\max}$ from 40 GHz with −20 dB per frequency decade. Peak $f_T/f_{\max}$ values of approximately 280 GHz/435 GHz are demonstrated in Fig. 8.

The micrograph of the manufactured $1.1 \times 0.6\text{-mm}^2$ large front-end chip is shown in Fig. 9. The largest part of the die is occupied by the pad frame and the RF/LO input baluns, while the downconverter core only requires an area of $0.5 \times 0.2\ \text{mm}^2$. The transmission lines, baluns, and inductors are all implemented in the 3-μm-thick top metal TM2 aluminum layer.

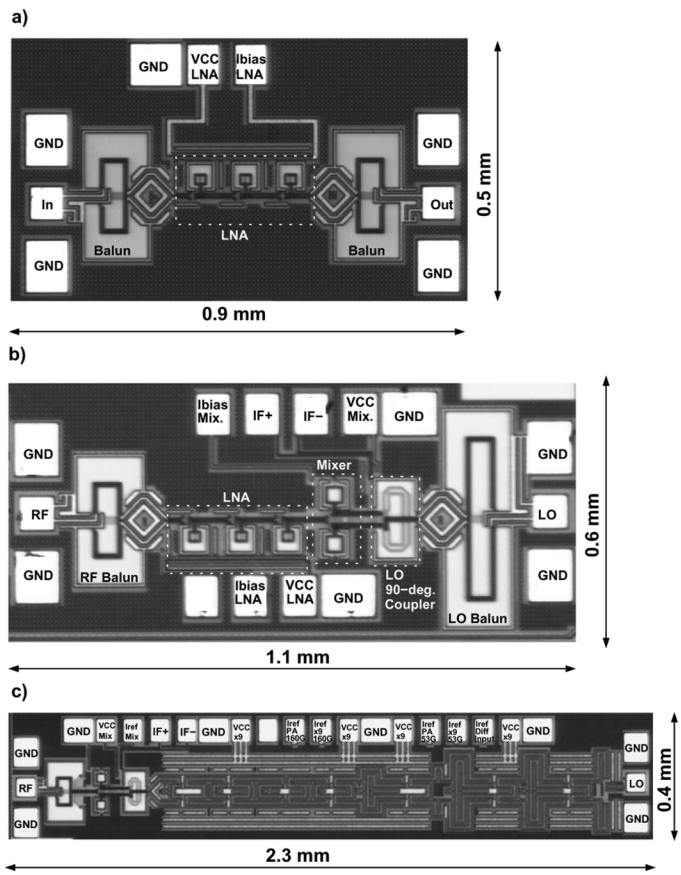

Fig. 9. Micrographs of the: (a) breakout of the 220-GHz three-stage LNA, (b) 220-GHz downconverter, and (c) 320-GHz downconverter with integrated × 9 LO multiplier chain.

IV. Characterization Setup

Fig. 10 presents the measurement setup used for the characterization of the conversion gain and noise of the integrated 220- and 320-GHz receiver front-ends. The RF input power from a sub-millimeter-wave multiplier was calibrated at the wafer-probe waveguide interface using an Erickson calorimeter. This calibration was performed in 1-GHz frequency steps over the 190–240- and 315–330-GHz frequency ranges, and yielded a measured average input power of −28 dBm. Due to the low power levels involved, simultaneous monitoring of the input power during device-under-test (DUT) characterization using a directional coupler and the power meter was not practical with the available coupler.

The insertion loss of the WR03 wafer probe was obtained by measuring the return loss at the waveguide interface while probing an open, short, and load impedance provided by a calibration substrate. From the corresponding return-loss values measured at the waveguide interface, an insertion loss of 3 dB was calculated for the wafer probe.

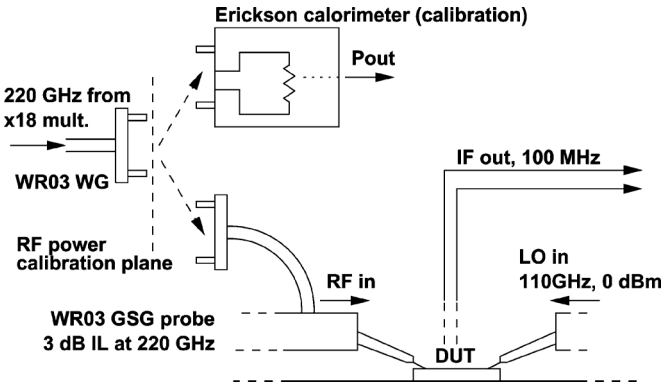

Fig. 10. Integrated downconverter conversion-gain measurement setup.

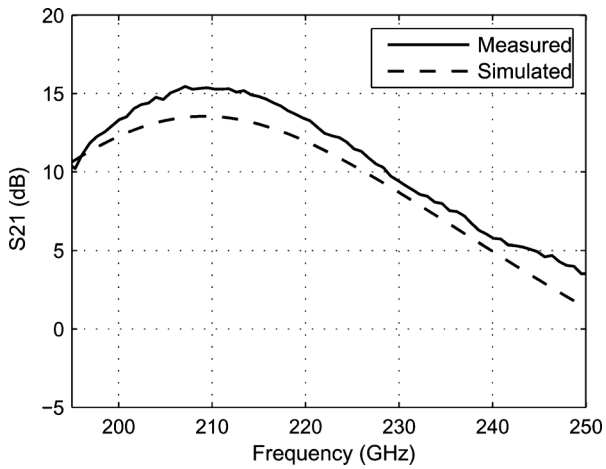

Fig. 11. Measured (solid line) and simulated (dashed line) gain of the three-stage differential LNA including pads and input and output baluns.

The 110-GHz LO drive to the mixer is provided by a synthesizer-driven $\times 6$ frequency multiplier feeding the integrated mixer through a coaxial W-band probe. An LO drive power of 0 dBm is obtained at the pads of the DUT. For the 320-GHz version of the receiver, a 17.7-GHz 3-dBm signal is provided to the integrated $\times$ 9 LO frequency multiplier chain through a wafer probe.

An external balun was used to combine the 100-MHz differential IF outputs to a single-ended signal. The 100-MHz IF frequency and surrounding noise floor was monitored with a spectrum analyzer. Since no WR03 noise source was available, the single-sideband (SSB) NFs of the characterized receiver front-ends has been calculated from the measured conversion gain and output noise floor with the input port terminated with a matched load. Hence, an input $N_{0,\mathrm{in}} = -174$-dBm/Hz thermal noise floor can be assumed, and the noise factor F calculated from the IF noise floor $N_{0,\mathrm{out}}$ and conversion gain G using the direct method as

$$F = \frac{\dfrac{S_{\mathrm{in}}}{N_{0,\mathrm{in}}}}{\dfrac{S_{\mathrm{out}}}{N_{0,\mathrm{out}}}} = \frac{N_{0,\mathrm{out}}}{GN_{0,\mathrm{in}}}. \tag{3}$$

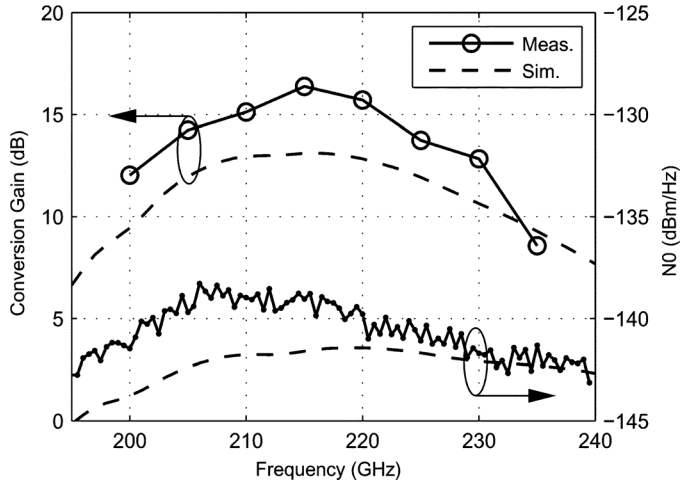

Fig. 12. Measured and simulated conversion gain and output noise floor including the 2-dB losses of the on-chip auxiliary balun in front of the LNA.

The 220-GHz LNA S-parameters were measured with a network analyzer equipped with WR-03 frequency-extender modules and waveguide wafer probes. Short-open-load-thru (SOLT) calibration was performed using a millimeter-wave calibration substrate.

V. Results

A. Three-Stage 220-GHz LNA Breakout

Fig. 11 presents the measured and simulated gain of the three-stage LNA breakout, with the calibration planes at the input and output pads. Hence, the results include a total of $2 + 2$ dB nonde-embedded losses from the baluns and pads at the input and output. The simulated results include extracted post-layout parasitics not included in the initial design. These parasitics, as well as the influence of the pad compensation, move the gain peak closer to 210 GHz than the intended 220-GHz center frequency. Relatively good agreement between measured and simulated gain is obtained over the complete 195–250-GHz frequency range. The 2-dB higher gain in the measurement compared to the simulation at the 210-GHz peak gain frequency can be partly explained by the fact that the preliminary device models used in the simulations do not fully capture the improved device performance of the measured silicon.

B. LNA-Integrated 220-GHz Front-End

In Fig. 12, the measured conversion gain and noise floor of the integrated receiver front-end is presented. At the targeted 220-GHz operating frequency, a 16-dB conversion gain and a -140-dBm/Hz output noise floor is obtained. It can be noted that the level of the noise floor follows the conversion gain and the gain of the LNA. This shows that the output noise of the full downconverter is dominated by the down-converted noise from the LNA and that the LNA has sufficient gain to overcome the simulated 20-dB NF of the subharmonic mixer.

According to (3), the measured conversion gain and output IF noise floor corresponds to a 18-dB SSB NF or a 15-dB DSB NF

TABLE I
COMPARISON OF MONOLITHICALLY INTEGRATED RECEIVERS ABOVE 150 GHz

Technology [μm]	Integration Level [circuit blocks]	BW[1]/Freq. [GHz]	LO Input [GHz]	Conv. Gain [dB]	NF [dB]	Reference
III/V-based						
0.1-μm mHEMT	Ant., LNA, Mixer	208-224	109	2	8.4	[5]
0.1-μm mHEMT	Ant., LNA, Mixer, LO-Chain	212-224	55	3.5	7.4	[6]
Silicon-based						
0.13-μm SiGe HBT	LNA, Mixer, VCO	160-175	Int. VCO	-5	21	[10]
0.13-μm SiGe HBT	LNA, IQ-Mixer, LO-Chain	158-165	18	25 / 27[2]	11 / 9[2]	[9]
0.13-μm SiGe HBT	LNA, Mixer	155-161	160	27 / 29[2]	9.5 / 7.5[2]	[8]
0.13-μm SiGe HBT	LNA, Mixer	202-230	110	16 / 18[2]	18[4] / 16[2,4]	This Work
0.13-μm SiGe HBT	Mixer, LO-Chain	315-328	17.7	-14/ -10[3]	36[4] / 32[3,4]	This Work

[1]3-dB bandwidth.
[2]Excluding the 2-dB auxiliary input balun and pad losses.
[3]Excluding the 4-dB auxiliary input balun and pad losses.
[4]Estimated SSB NF from conv. gain and output noise.

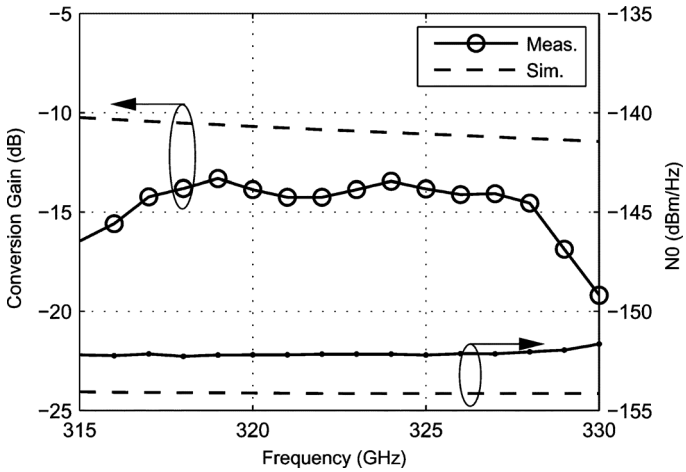

Fig. 13. Measured and simulated conversion gain and output noise floor including the 4-dB losses of the on-chip auxiliary balun in front of the mixer.

at 220 GHz since the 100-MHz IF frequency means that both of the sidebands are present within the LNA bandwidth. The measured NF is in good agreement with the simulated 13-dB NF of the LNA and the estimated 2-dB losses of the auxiliary on-chip RF balun and impedance-compensated pad.

The measured current consumption is 20 mA for the mixer and 40 mA for the LNA from a 3.6-V supply.

C. 320-GHz Front-End With Integrated × 9 LO Chain

Fig. 13 presents the measured conversion gain and the output IF noise floor of the 320-GHz front-end with an integrated LO chain. As in the case of the 220-GHz downconverter, the 4-dB losses of the 320-GHz input pad and balun have not been de-embedded from the results. Due to a stability issue with the integrated frequency multiplier chain, the measurement was performed with supply voltage and current to the multiplier increased to 5 V/600 mA on-chip instead of the nominal 4 V/300 mA. Hence, the 160-GHz LO-drive power is expected to be lower than than the 10-dBm output level previously reported in [2] for optimum biasing of this chain. The supply to the subharmonic mixer remained at 3.6 V with a nominal current consumption of 20 mA. The measured −14-dB conversion gain at the 320-GHz operating frequency correspond to −10-dB conversion gain at the mixer input terminals and shows reasonable agreement with the simulated gain of −10/−6 dB (with/without balun). The lower conversion gain in the measurement can be explained by a nonoptimized LO-drive level from the de-biased integrated multiplier chain, as well as layout parasitics not captured by the simulation. Outside of the 317–328-GHz frequency range, the output power of the LO multiplier sharply drops, thereby leading to a corresponding drop in the conversion gain.

The measured noise floor of −152 dBm/Hz is 3 dB higher than the simulated noise level of −154 dBm/Hz. However, it should be noted that the measured noise floor is close to the −157-dBm/Hz floor of the spectrum analyzer, thus causing an overestimation of the output noise. The relatively high conversion loss causes the output noise to be dominated by noise generated at the 100-MHz IF frequency rather than down-converted high-frequency noise. Hence, the noise floor remains relatively constant over the bandwidth. The measured conversion gain and noise floor provide an estimated SSB NF [see (3)] of 36/32 dB (with/without input pad and balun) at 320 GHz.

VI. CONCLUSION

Subharmonic 220- and 320-GHz receiver front-ends have been demonstrated in an engineering version of an SiGe-HBT technology. The use of a subharmonic mixer facilitates the generation of the LO-drive signal and can also to help simplify the LO distribution in a multichannel array configuration. The 220-GHz receiver front-end consists of an LNA and subharmonic mixer. As shown in Table I, the demonstrated 16-dB conversion gain demonstrated with this circuit is higher than the gain obtained with a similar circuit in a III–V technology. The comparatively high NF of 15 dB (DSB) is partly caused by the use of an integrated RF balun at the receiver input. An 18-dB conversion gain and 13-dB NF should be obtainable in the intended configuration with a differential input signal from an on-chip antenna. The 320-GHz version of the front-end demonstrates that the operational frequency range of this mixer can extend into the sub-millimeter-wave frequency range although the absence of a suitable LNA leads to a significantly increased NF. The use of a further optimized device technology and circuit design is also expected to yield a reduced NF and improved conversion gain.

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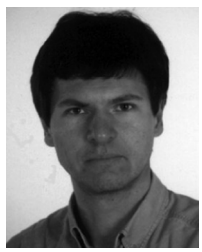

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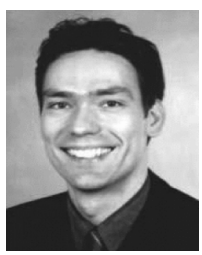

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