A Low-Power BiCMOS 4-Element Phased Array Receiver for 76–84 GHz Radars and Communication Systems

Sang Young Kim, *Student Member, IEEE*, and Gabriel M. Rebeiz, *Fellow, IEEE*

***Abstract*—This paper presents a 76–84 GHz low-power 4-element phased array receiver built using a 0.13 μm BiCMOS process. The power consumption is reduced by using a single-ended design and alternating the amplifiers and phase shifter cells to result in a low noise figure at a low power consumption. A variable gain amplifier and an 11° trim bit are used to correct for the rms gain and phase errors at different operating frequencies. The phased array consumes 32 mW per channel and results in a gain of 10–19 dB at 76–84 GHz, a noise figure of 10.5 $\pm$0.5 dB at 80 GHz and an rms gain and phase error $<$0.8 dB and $<$7.2°, respectively, up to 81 GHz, and $<$1.1 dB and 10.4° up to 84 GHz. The phased array also shows a channel to channel coupling of <-30 dB up to 84 GHz. To our knowledge, this work presents state-of-the-art on-chip performance at W-band frequencies.**

***Index Terms*—Millimeter-wave integrated circuits, phase shifters, phased arrays, silicon germanium.**

I. Introduction

MILLIMETER-WAVE automotive radar chips, both at 77 GHz (mostly FMCW systems) and at 79–81 GHz (pulse based systems), were recently demonstrated using SiGe and CMOS technologies [1]–[11]. The SiGe implementations were particularly successful due to their low phase noise performance and their operation at temperatures as high as 125 °C which is required in automotive applications. There are two radar platforms for automotive applications: 1) long-range radars for cruise control (1–200 m) implemented at 76–77 GHz and with 200–1000 MHz bandwidth, and 2) short-range radars (0.5–40 m) implemented at 79–81 GHz using <1 ns radar pulses for blind-spot detection, lane change, and collision avoidance applications. Both applications require that the antenna beam be scanned in space, and this can be done using switched focal plane systems [12]–[14], digital beamforming [15], [16], or phased arrays [17], [18]. The phased arrays for the long-range radars are particularly challenging since an 8 cm aperture can be replaced by 8–24 antennas (the number of channels depends on the scanning angle and the number of transmit channels [15], [19]), and therefore, it is advantageous to reduce the power consumption per phased-array element.

The 81–86 GHz band is also used in high-data rate point-to-point communication systems with complex modulation [20]–[23]. In this case, the band can be used entirely in one shot, or can be subdivided into two different band (81–84 GHz, 83–86 GHz, etc.). These systems are currently based on reflector antennas, but phased arrays are proposed to solve the costly alignment issue between two reflector antennas located on towers. In this case, the SiGe phased array must be proceeded by a low noise InP amplifier (one per channel) since the system noise figure (NF) must have a very low NF ($<$4 dB) for long distance communications.

Silicon-based phased arrays have been demonstrated at millimeter-wave frequencies using All-RF, LO and IF beamforming architectures [17], [18], [24]–[28]. This work is based on the All-RF approach which eliminates the I/Q mixers on each element and the LO distribution network. The RF beamforming architecture can be scaled to a large number of elements (16–32) as shown by UCSD, Intel, IBM and Mediatek at 45–65 GHz [18], [24]–[26]. A single-element chip and a 4-element chip are presented capable of operation at 76–77 GHz, 79–81 GHz, and 81–84 GHz with low power consumption and wide instantaneous bandwidth.

The phased-array receiver design is single-ended and consumes less power than a differential implementation, but on the other hand, it is sensitive to the grounding inductance when packaged with off-chip antennas. One way to solve this problem is to use on-chip antennas as shown in [29] for a 3×3 wafer-scale power amplifier array. In this case, the antenna and the amplifier/phase-shifter share the same ground and there is no ground transition between the chip and the antennas. Another way is to migrate the design presented in this paper to a differential circuit which is robust to ground inductance transitions as shown in [24].

II. Design

A. Architecture

The 4-element phased-array architecture is shown in Fig. 1. The design is based on an amplifier/phase-shifter cell/amplifier approach [30], and the outputs of the 4-element array are added together using a two-stage Wilkinson coupler. Wilkinson couplers are passive devices with high linearity and low loss

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The authors are with the Department of Electrical and Computer Engineering, University of California at San Diego, La Jolla, CA 92093 USA (e-mail: sangykim@ucsd.edu; rebeiz@ece.ucsd.edu).

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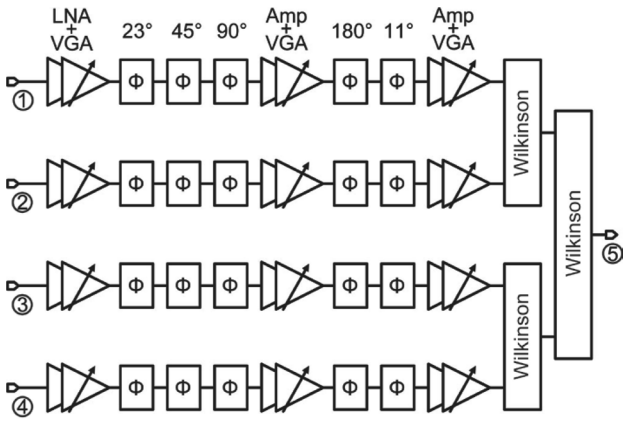

Fig. 1. W-band 4-element phased-array architecture.

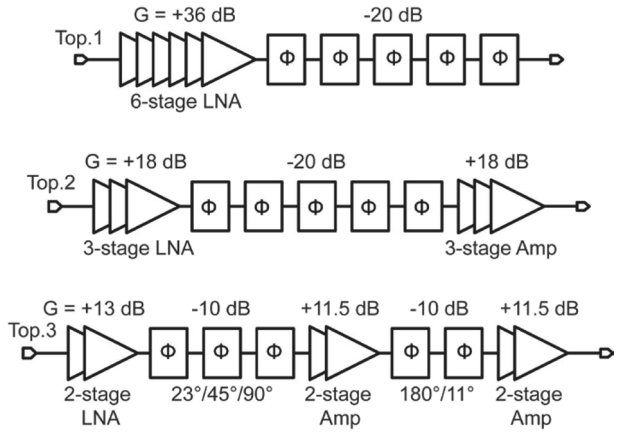

Fig. 2. Comparison of three different architectures, at 80 GHz.

[31], and are ideal at mm-wave frequencies due to their relatively small size and low loss [32], [33]. The amplifiers are implemented using 0.13 μm SiGe transistors with a $f_T/f_{\max}$ of 200/220 GHz, and the phase shifters are based on switched-LC networks implemented using 0.13 μm CMOS transistors (available in the IBM 8 HP process) [34]. The phase shifters show in high linearity (IIP3 of $\sim$23 dBm) and zero power consumption, but have a simulated loss of 17–20 dB for a 5-bit design due to the channel resistance and parasitic capacitance of the 0.13 μm CMOS transistors [33], [35], [36].

Fig. 2 and Table I compare three different topologies for the phased-array element: Topology 1 is based on a traditional design with an LNA in front followed by a 5-bit phase shifter, topology 2 divides the amplifier into two units, one at the input and one at the output of the phase shifter, and topology 3 distributes the amplifiers and phase shifters throughout the chain. The design is done for an input $P_{1\mathrm{dB}}$ of -26 dBm and a gain of 16 dB at 81 GHz. Topology 1 results in the lowest NF but with the highest power consumption due to the 36 dB amplifier gain required to overcome the 20 dB phase shifter loss. This results in an $P_{1\mathrm{dB}}$ of $+10$ dBm at the output of the LNA and high power consumption. Also, due to the potential of substrate coupling, it is not advisable to design 36 dB gain amplifiers in single-ended systems [37]. Topology 2 results in the highest NF, and this is not acceptable. It is seen that topology 3 results in a NF of 11.4 dB and with a power consumption of only 32 mW per channel, roughly quarter of topology 1.

TABLE I
COMPARISON OF THREE DIFFERENT TOPOLOGIES

	Gain (dB)	NF (dB)	IP1dB (dBm)	Power Cons. (mW)
Topology 1	16	8.4	-26	120
Topology 2	16	12.5	-26	32
Topology 3	16	11.0	-26	32

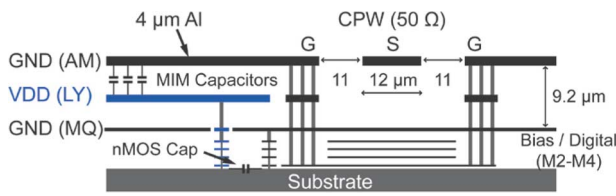

Fig. 3. IBM 8 HP metal stack-up with a presentative 50 Ω CPW line.

B. Amplifiers

The 4-element phased array is built using the IBM 8 HP process with seven metal layers and a 4-μm-thick top layer (AM) (Fig. 3). The coplanar-waveguide (CPW) transmission lines are built using the AM and MQ layers with a 9.2 μm thick interlayer dielectric, and have a simulated loss of 0.75 dB/mm at 80 GHz for a 50 Ω line. Fig. 4 presents the simulated $f_{\max}$ and f_T for a 5×0.12 μm common-emitter transistor given by the IBM model (reference to M1) and including the full electromagnetic (EM) simulation up to AM layer. It is seen that the EM-simulated f_T and $f_{\max}$ are lower than the values obtained using the IBM model. This has significant effect on the gain and NF of mm-wave amplifiers and is therefore essential for accurate circuit design.

A two-stage cascode-based LNA with a center frequency of 81 GHz is used with conjugate inter-stage matching for maximum gain (Fig. 5(a)). The second stage is gain controlled using 2-bit current steering (0/$-$0.2/$-$2.3/$-$4.0 dB relative gain). Resistors are placed in shunt with the load inductors in order to widen the 3 dB bandwidth to 19 GHz at the expense of 0.5 dB in additional noise. The inductors are designed using microstrip lines between AM and M1, with a width of 6 μm and Q of 18 at 81 GHz, and are EM modeled by Sonnet [38]. C1 (40 fF) is built using custom capacitors between M3 and M4 with a simulated Q of 40 at 81 GHz. The current bias is done at 0.6 mA/μm to result in the lowest noise figure and is less than the optimal bias current for highest gain as given by the IBM design manual [34]. A simulated gain and noise figure of 9.9–12.2 dB and 8.2–8.8 dB, respectively, are obtained at 76–85 GHz for a total bias current of 6 mA. The amplifier results in a wide impedance match (S_{11}, $S_{22}<-10$ dB at 72–100 GHz, 74–91 GHz respectively) and a $P_{1\mathrm{dB}}$ of -21 dBm. The other variable-gain amplifiers are identical to the two-stage LNA.

An essential design tool at millimeter-wave frequencies is the global analysis and optimization of the two-stage cascode amplifier (Fig. 5(b)). In the layout around the transistors, the ground

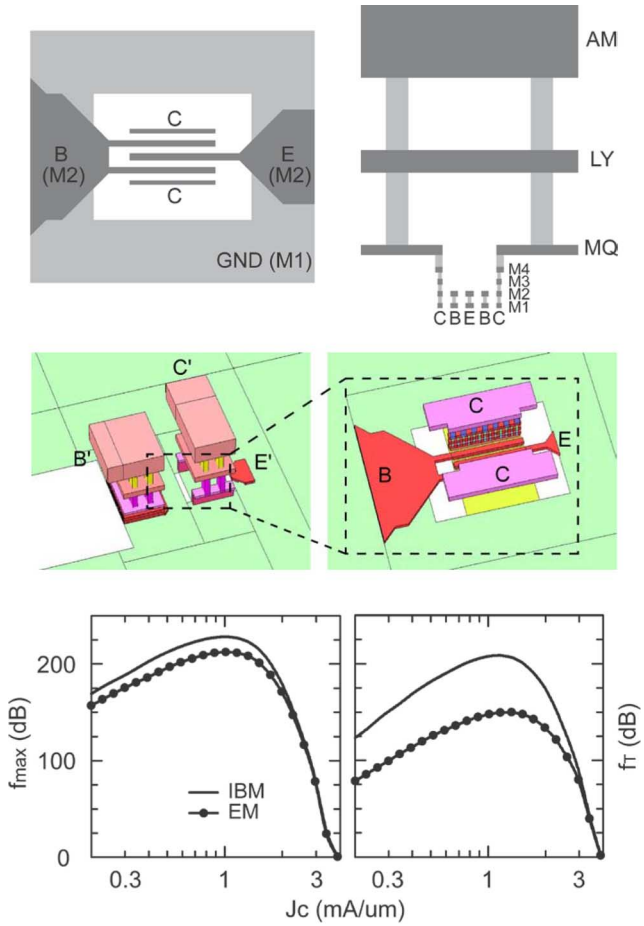

Fig. 4. Simulated $f_{\max}$ and f_T without and with EM simulation (transistor size $= 5\ \mu\text{m} \times 0.12\ \mu\text{m}$.

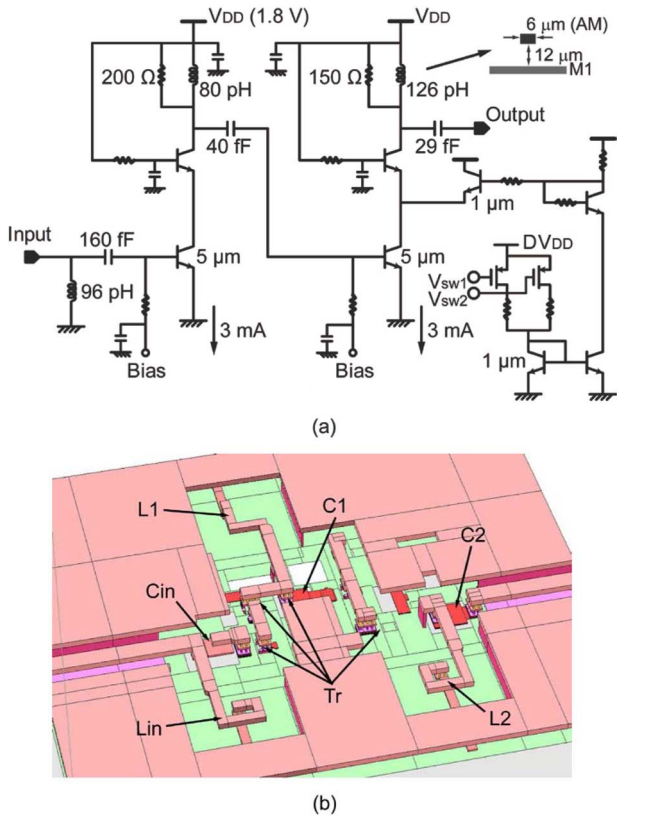

Fig. 5. (a) Schematic and (b) layout of the two-stage W-band cascode amplifier with gain control.

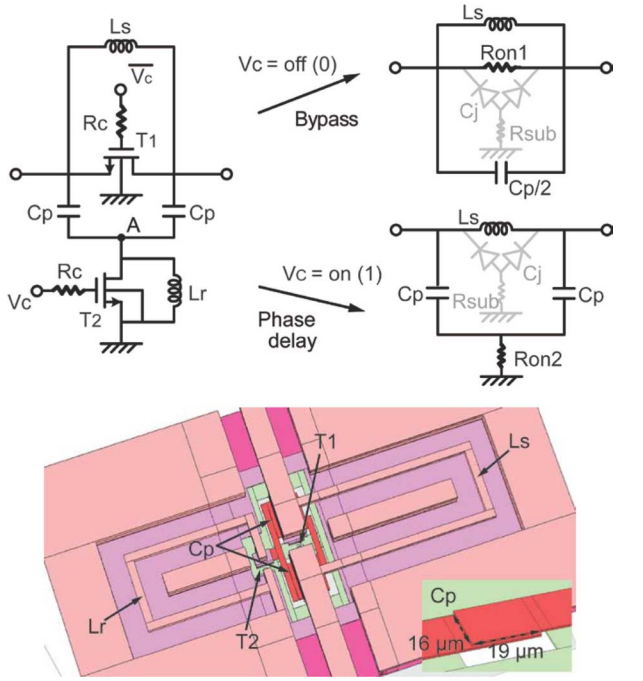

Fig. 6. Design of switched-delay CMOS phase shifters.

plane is dropped from MQ to M1 to result in a low emitter inductance, and the inductors are based on microstrip-lines using AM and M1 layers. The entire circuit is modeled using Sonnet with internal ports for the base-emitter-collector nodes, and the ports are attached to the IBM transistor models in the Cadence. This takes into account the full-wave electromagnetic effects of the vias around the transistors and any coupling between the inductors in the amplifier. The Sonnet simulation takes 4 hours to analyze the cascode amplifier from 0.1 to 200 GHz on a modern desktop station (Fig. 5(b)). The global modeling and optimization technique, while time intensive, results in excellent comparison between simulations and measurements (see Section III).

C. Phase Shifter Design

The design of the phase shifter is based on switched 50 Ω low-pass networks for the 11°, 22.5°, 45°, and 90° bits, and the 180° bit is built using two 90° bits under the same control voltage (Fig. 6) [35]. In the bypass-state, T1 is ON and T2 is OFF, Lr resonates with the off-state capacitance of T2, creates an open-circuit at node A, and port 1 is connected to port 2 using T1. In the phase-delay state, T1 is OFF and T2 is ON, T2 connects point A to ground, and port 1 is connected to port 2 using the low-pass network Cp-Ls-Cp. The phase delay is determined by the choice of Cp and Ls, and is linear with frequency within a ±10% frequency range.

The transistors (T1, T2) must be chosen to result in relatively low insertion loss when the transistors are ON, but on the other hand, the 0.13 μm CMOS technology results in a large substrate

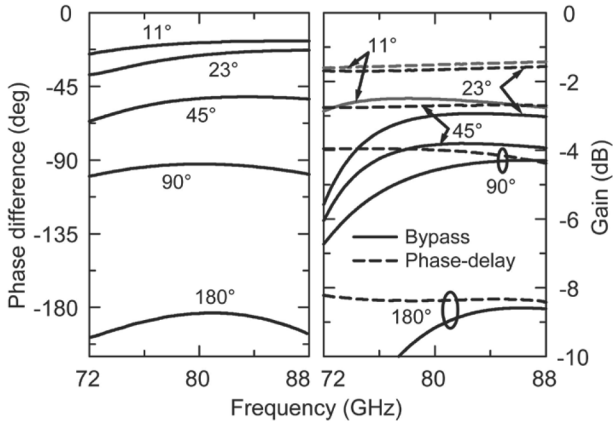

Fig. 7. Simulated switched-delay CMOS phase shifter cells.

TABLE II
PHASE SHIFTER COMPONENT VALUES

	11°	22°	45°	90°	180°
T1/T2 (μm)	7/4	7/4	14/4	14/10	14/10
Ls (pH)	65	70	80	74	74
Cp (fF)	12	12	17	41	41
Lr (pH)	117	107	92	62	62
Bypass loss (dB)	2.5	2.9	3.8	4.4	8.7
Delay loss (dB)	1.4	1.6	2.7	4.0	8.3

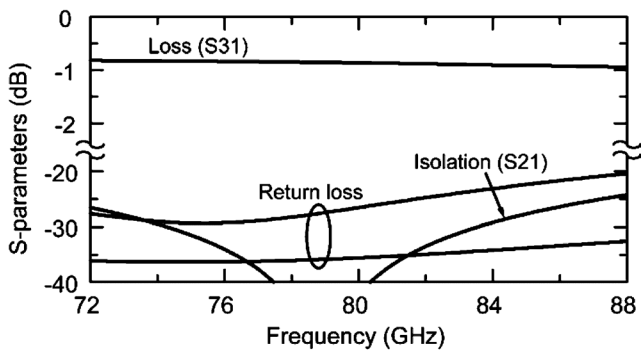

Fig. 8. Simulated S-parameters of a single-stage Wilkinson coupler.

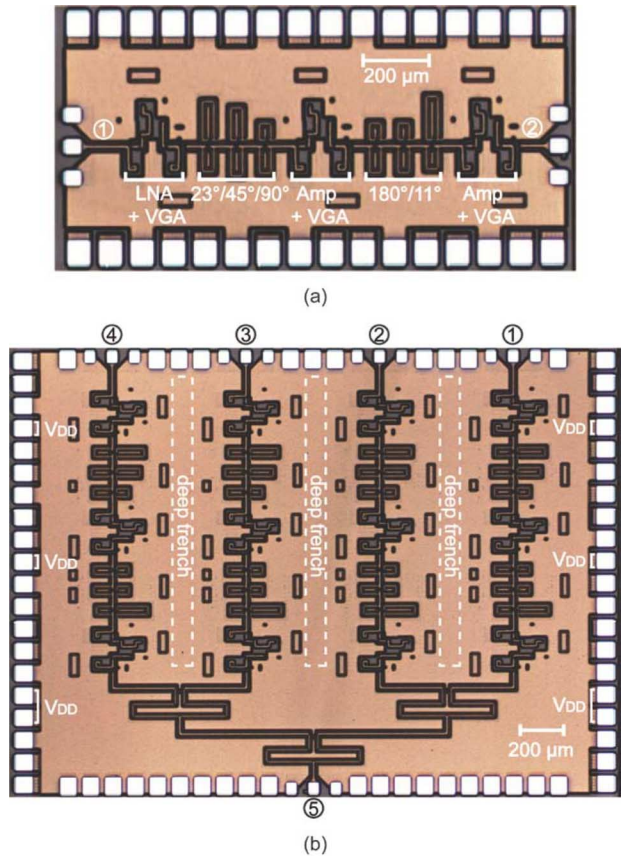

Fig. 9. Photograph of (a) single channel (1.6×0.8 mm^2) and (b) 4-element phased arrays (2.0×2.7 mm^2).

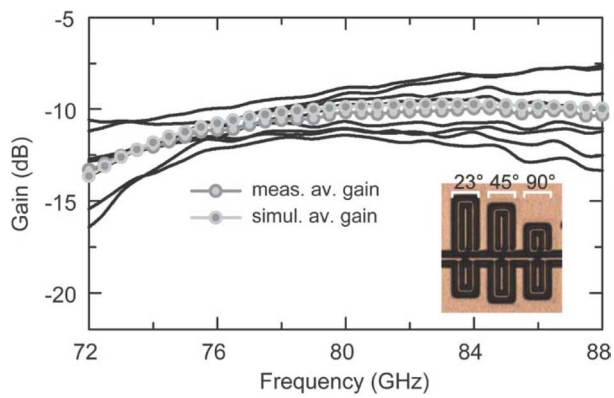

Fig. 10. Measured and simulated gain of the $23°/45°/90°$ phase shifter cell.

capacitance which contributes to high insertion loss at 77–85 GHz even when the transistors are off. T1 and T2 are therefore chosen to result in similar insertion loss in the bypass and phase-delay states (see Table II). Fig. 7 presents the simulated gain and phase response of the individual phase shifter cells. The 90° bit is challenging due to the large Cp-Ls-Cp values used, and results in an insertion loss of 4.0–4.2 dB (8.2–8.5 dB for the 180° bit) and an S_{11} (or S_{22}) <-11.5 dB from 75–85 GHz in the phase-delay state. In order to alleviate the effect of the S_{11} mismatch, the 90° and the 180° cells are placed next to the central amplifier which is a well-matched 50 Ω impedance block. The inductors are designed using Sonnet and based on high-impedance transmission-lines ($Zo=$ 70.7 Ω, 2 dB/mm, $Q = 13$ at 80 GHz), and global EM simulation is performed (see Fig. 6 for the Sonnet EM model). Also, the $22°/45°/90°$ and the $180°/11°$ bits are simulated together in Sonnet and Cadence in order to ensure low electromagnetic coupling between the individual bits and a wideband impedance match.

This phase shifter topology results in gain variation over the 16 states due to the loss and impedance variation between the two states of each cell, and the cascade of non-ideal 50 Ω blocks (especially the 45° and 90° cells). Simulations indicate a gain of -17 to -20 dB over the 32 states at 81 GHz. The variable gain amplifiers are therefore essential to compensate for this effect and to result in a low rms gain error.

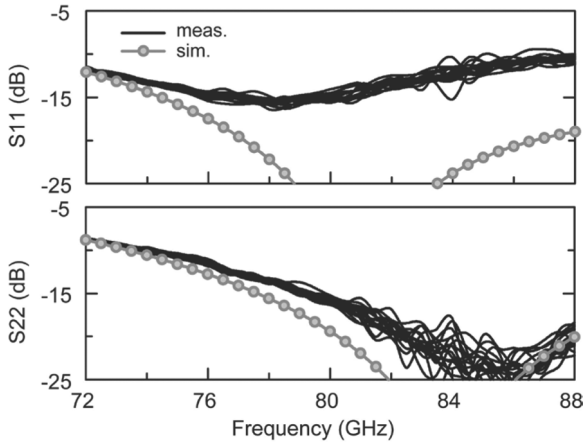

Fig. 11. Measured S_{11} and S_{22} for 16 phase states.

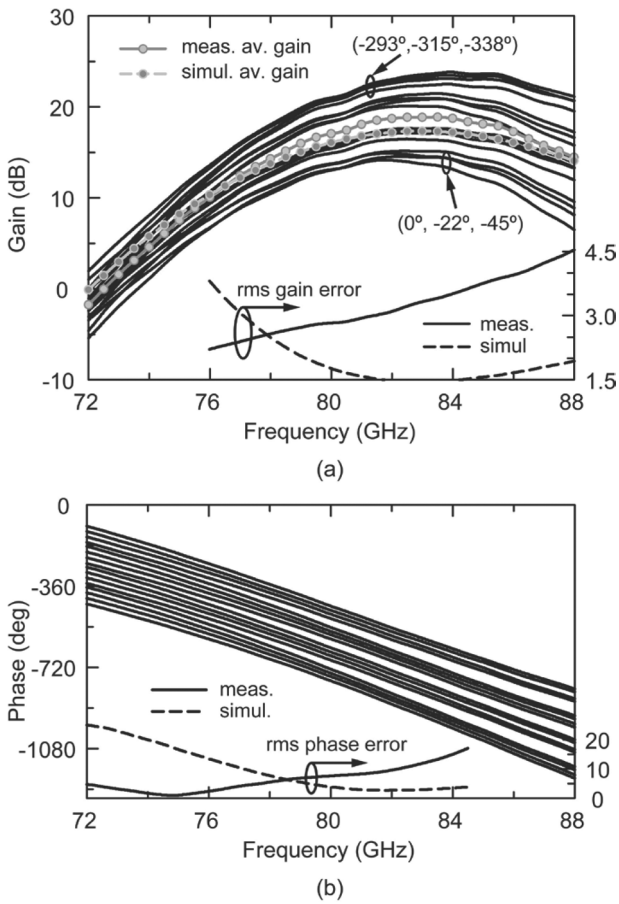

Fig. 12. Measured (a) gain and (b) phase response versus 16 phase states.

D. Two-Stage Wilkinson Combiner

The 50 Ω Wilkinson combiners are designed using two $\lambda/4$ sections of 70.7 Ω CPW lines ($Q = 13$ at 80 GHz) and result in an insertion loss of 0.9 dB and $S_{11}/S_{22}/S_{33} < -20$ dB at 72–88 GHz (Fig. 8). The isolation between the two ports, S_{23}, is >25 dB at 72–88 GHz. The Wilkinson combiner is wideband and has no effect on the channel S-parameters except for an additional 0.9 dB loss per stage. Again, the 4:1 Wilkinson combiner is electromagnetically modeled in Sonnet and its S-parameter block is used in Cadence.

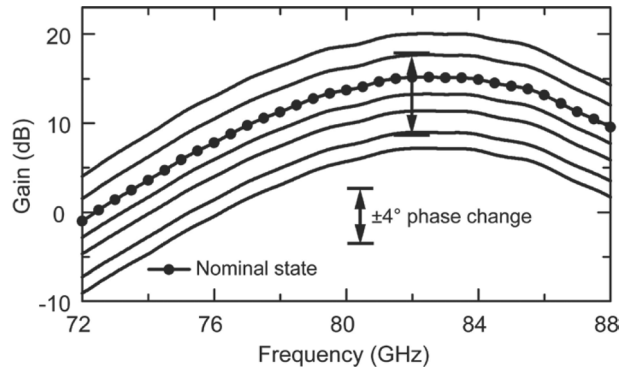

Fig. 13. Measured VGA operation at the (1,1,1,1) state.

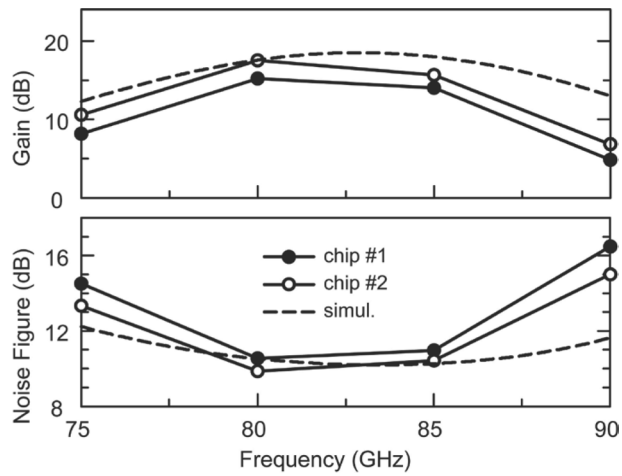

Fig. 14. Measured gain and noise figure using a hot/cold technique. Gain is set at the nominal state (see text).

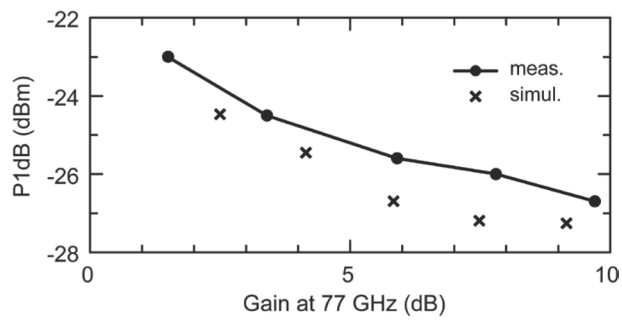

Fig. 15. Measured input $P_{1\mathrm{dB}}$ versus gain setting at 77 GHz.

E. Phased Array Simulations

The simulated average gain of a single channel is 16.1 dB at 80 GHz for the 16 phase states, with a corresponding noise figure of 11.1±0.6 dB, an input $P_{1\mathrm{dB}}$ of −27 dBm, and a power consumption of 32 mW (1.8 V, 18 mA). The simulated S_{11} and S_{22} are <-10 dB from 73 GHz to >90 GHz. The gain can be controlled by 9.5 dB in 1.6 dB steps. An important design aspect is that the channel phase does not change by more than ±4° over a large gain-control range. This allows the variable gain amplifiers to correct for the gain change versus phase state without adding additional phase errors. The 4-element array results in a similar performance as a single channel but with an additional 2.4 dB loss at 81 GHz: 1.8 dB loss due to two Wilkinson couplers and 0.6 dB for the added transmission lines.

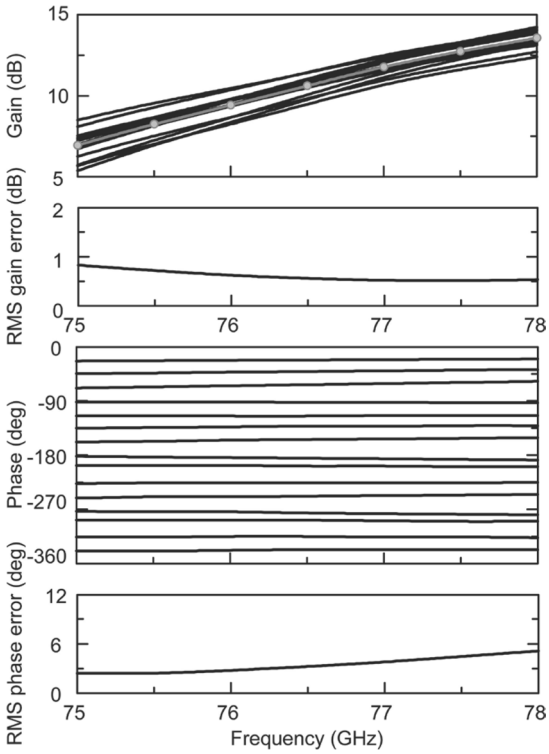

Fig. 16. Gain, phase, and RMS error after calibration at 76.5 GHz.

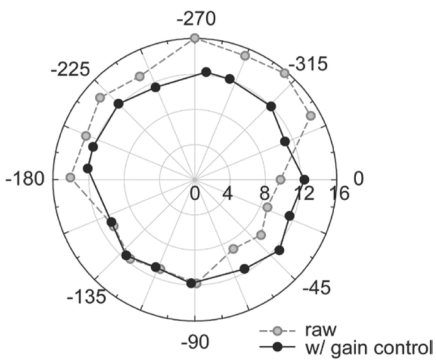

Fig. 17. Gain and phase correction on a vector chart at 76.5 GHz.

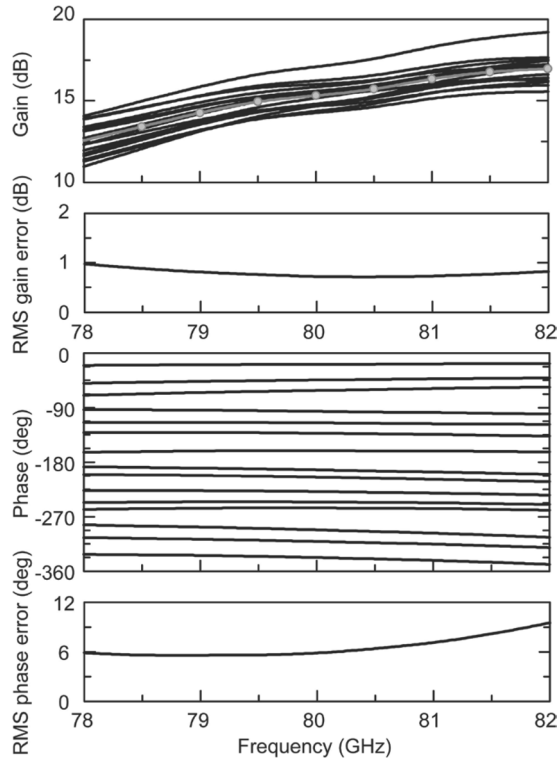

Fig. 18. Gain, phase, and RMS error after calibration at 80 GHz.

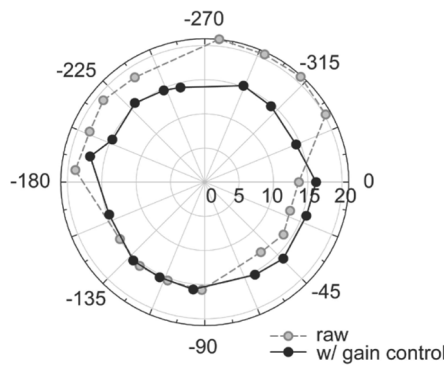

Fig. 19. Gain and phase correction on a vector chart at 80 GHz.

Since this is a single-ended design, the phased array channels are placed 600 μm from each other, and the area between the channels is filled with Vcc decoupling capacitors (23 pF per channel) and with metal walls which connect the AM metal layer to the substrate. The input GSG (CPW) pad transition is designed using Sonnet and includes a short high-impedance tapered section to match the pad capacitance at 70–90 GHz, and results in $S_{11} \leq -20$ dB and $S_{21} \leq -0.2$ dB at 75–85 GHz.

III. Measurements

Fig. 9 presents microphotographs of a single-channel chip and a 4-element chip. All measurements are done on-wafer using an Agilent E8361 A Vector Network Analyzer with extenders to 110 GHz. A probe-tip calibration is first done using the Cascade 138–357 calibration substrate [39], and the measurements include the GSG pad transition loss. Several chips were measured and resulted in similar measurements.

Fig. 10 presents the measured gain response of a stand-alone test chip with $23^\circ/45^\circ/90^\circ$ phase shifters. The measured average gain agrees well with simulations, but has larger variation versus phase states at $>$82 GHz than predicted by simulations. It shows good matching between the simulated and measured average gain of the phase shifters.

Figs. 11 and 12 present the measured S-parameters of a stand-alone single channel for 16 phase states and the bias conditions are $V_{\rm DD} = 1.8$ V and a current of 18.3 mA/channel. A wideband input and output matching is achieved with a rms gain and phase error of 2.2–3.5 dB and $\leq 15^\circ$, respectively, at 76–84 GHz. Comparison with simulations indicates excellent match with S_{11}, S_{22} and the average S_{21}, but again with a higher rms gain and phase error. This is attributed to the phase shifter cells which showed higher loss than simulations due to inadequate 0.13 μm transistor models at 75–85 GHz. The measurement also shows 13 dB of gain control with $\leq \pm 4^\circ$ phase

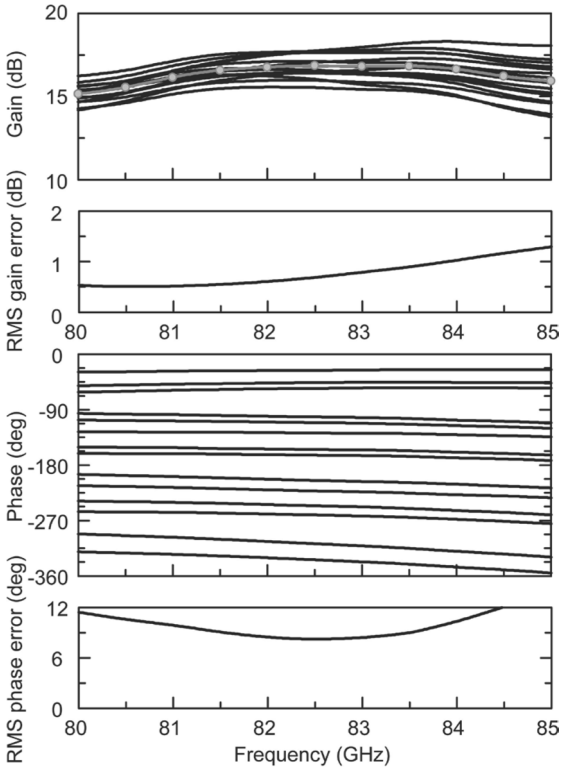

Fig. 20. Gain, phase, and RMS error after calibration at 82.5 GHz.

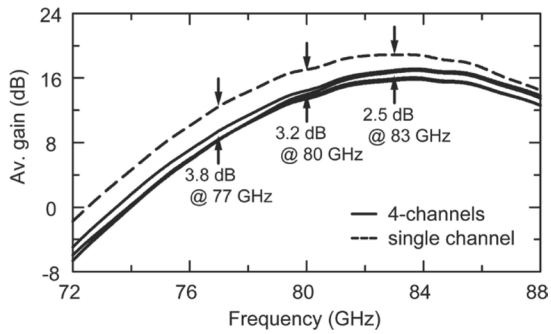

Fig. 21. Measured average gain of 4-channel phased array chip and single channel chip.

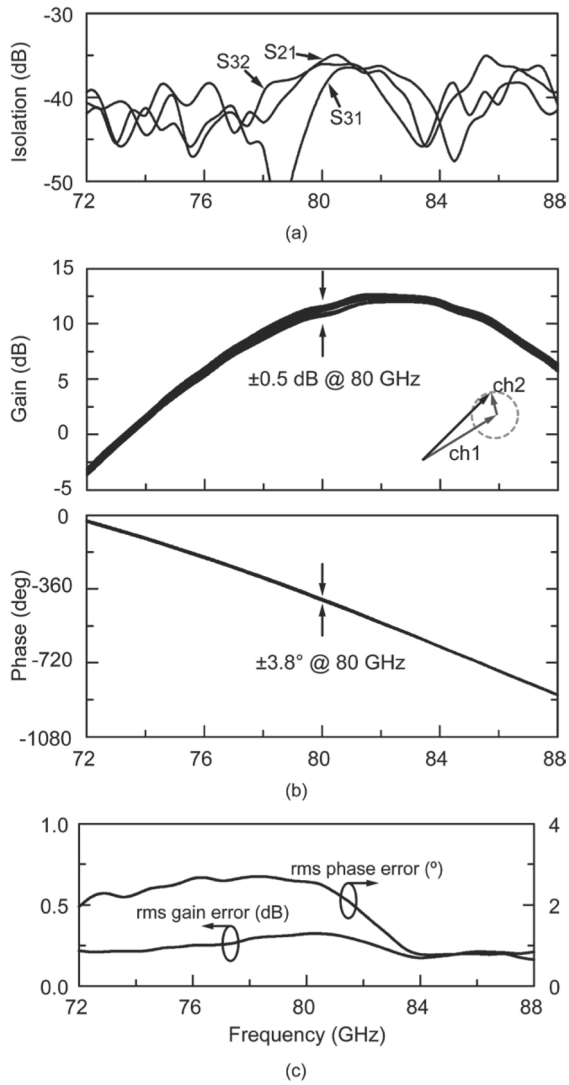

Fig. 22. (a) Measured S-parameters coupling between the channels, (b) the effect of channel 2 phase change on channel 1, and (c) rms gain and phase error in channel 1 due to the phase change in channel 2.

change over a 10 dB control range (Fig. 13). The nominal state in Fig. 13 is the gain-state setting which is used for all measurements (S-parameters in Figs. 11 and 12).

The measured NF and input $P_{1\mathrm{dB}}$ were also done on the single channel chip and are shown in Figs. 14 and 15. The NF measurements are done at the nominal gain state so as to yield the average NF seen by the phased array channels when the gain control is used. The measured average NF is 10.5 dB at 80 GHz which agrees well with simulations (11.1 ± 0.6 dB at 80 GHz for all phase states). The measured input $P_{1\mathrm{dB}}$ is -26.7 to -23.0 dBm at 77–80 GHz depending on the gain setting and also agrees well with simulations.

The rms gain error can be substantially reduced using the variable gain amplifiers, and the rms phase error can also be corrected using the 11° phase bit as a trim bit. Figs. 16 and 17 present the achieved performance at 76–77 GHz (gain control only), 79–81 GHz (gain control and 11° phase trim), and 81–84 GHz (gain control and 11° phase trim). In Fig. 17, the small phase change between the raw data and the gain control data is due to the variable gain amplifier. The simulated NF under low rms gain and phase states is within ±0.5 dB of the nominal-state values shown in Fig. 14. The phased array can be used in the automotive bands with instantaneous bandwidth of 500 MHz (76.5 GHz) and 2 GHz (79–81 GHz), and is also usable in the 81–84 GHz band.

The 4-element chip consumes 74 mA ($V_{\mathrm{DD}} = 1.8$ V) and results in virtually identical performance to the single element chip except for an additional 2.5–3.8 dB loss at 76–84 GHz due to the Wilkinson network (Fig. 21). Note that each channel in the 4-element array results in near identical gain versus frequency, which is typical of SiGe-based circuits and a symmetrical passive combiner [33].

The measured coupling between the different channels is done using S-parameters first (Fig. 22(a)), and then by changing the phase of channels 2, 3, 4 and monitoring the S-parameters on channel 1 (Fig. 22(b)) [37], [40]. In this case, channels 2, 3, 4

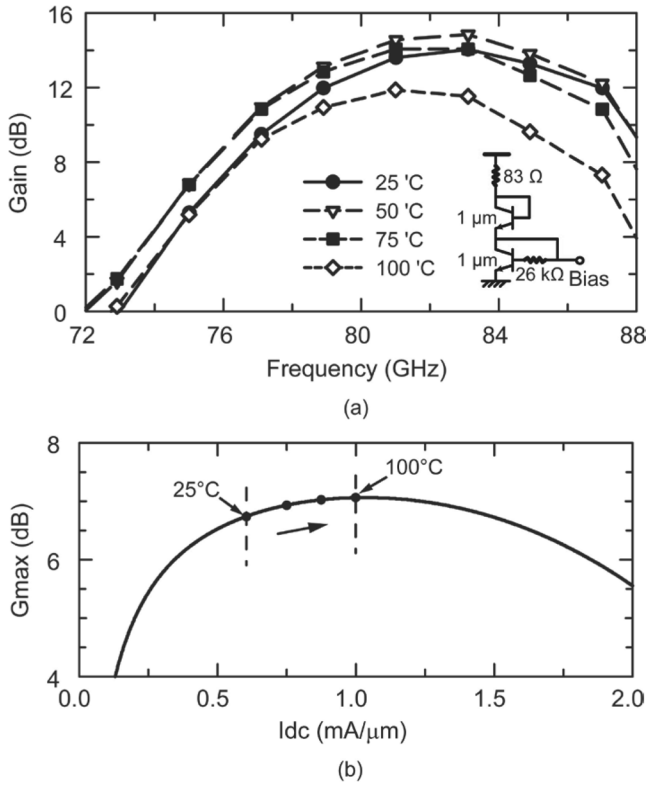

Fig. 23. (a) Measured gain of a single channel at different temperatures. (b) Channel current consumption and bias condition versus temperature.

TABLE III
CURRENT CONSUMPTION VS TEMPERATURE

Temp (°C)	25	50	75	100
Current (mA)	18.5	22.4	26.1	29.3

TABLE IV
SUMMARY OF PHASED ARRAY PERFORMANCE

Technology	0.13 µm SiGe BiCMOS (IBM 8HP)
Frequency band	76-84 GHz
Supply voltage	1.8 V (analog), 1.5 V (digital)
Current consumption	18.0 mA / channel
Chip area	5.4 mm² (2.0 x 2.7 mm²)
Input return loss	-10 dB @ 70-88 GHz
Output return loss	-10 dB @ 74-88 GHz
Power gain (avg.)	10.1 - 18.9 dB @ 76-84 GHz
Phase resolution	4-bit
Gain error (rms)	< 0.6 dB @ 76-77 GHz < 0.8 dB @ 79-81 GHz < 1.1 dB @ 81-84 GHz
Phase error (rms)	< 3.9° @ 76-77 GHz < 7.2° @ 79-81 GHz < 10.4° @ 81-84 GHz
NF	10.5 ± 0.5 dB @ 80 GHz

are left open-circuited which results in a worse-case condition for testing. The on-chip coupling is very low, estimated to be <-30 dB between channels 1 and 2 using the vector addition method. The effect of channel 3 and 4 on channel 1 are negligible ($<\pm 0.1$ dB, $<\pm 1^\circ$).

Fig. 23 presents the measured gain versus temperature at nominal settings. The gain is constant up to 75 °C and then drops by 3 dB at 100 °C. This is achieved by a simple biasing network which employs a diode in the current reference path and results in an increased bias current versus temperature. As stated above, the amplifiers are biased at 0.60 mA/μm so as to result in a low NF, and the increase in the bias current results in a near constant gain versus temperature. The phase performance versus temperature remains essentially unchanged as shown by simulations and as demonstrated in similar circuits at 30–40 GHz [33]. The chip performance is summarized in Table IV.

IV. CONCLUSION

A 76–84 GHz 4-element phased array receiver was demonstrated in a 0.13 μm BiCMOS process. The rms gain and phase error were mostly due to inaccuracies in the transistor switch model, but can be corrected using a VGA and an 11° trim bit. Also, the phase shifter loss is high due to the use of the 0.13 μm CMOS technology. The results indicate that this topology can be applied at 60–120 GHz using advanced CMOS nodes (65 nm, 45 nm). The single-ended design can be extended to a differential topology which is less sensitive to ground inductance and packaging effects.

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REFERENCES

[1] H. P. Forstner, H. Knapp, H. Jäger, E. Kolmhofer, J. Platz, F. Starzer, M. Treml, A. Schinko, G. Birschkus, J. Bock, K. Aufinger, R. Lachner, T. Meister, H. Schafer, D. Lukashevich, S. Boguth, A. Fischer, F. Reininger, L. Maurer, J. Minichshofer, and D. Steinbuch, "A 77 GHz 4-channel automotive radar transceiver in SiGe," in *IEEE Radio Frequency IC Symp. Dig.*, Jun. 2008, pp. 233–236.

[2] C. Wagner, H. P. Forstner, G. Haider, A. Stelzer, and H. Jäger, "A 79-GHz radar transceiver with switchable TX and LO feedthrough in a Silicon-Germanium technology," in *IEEE BCTM Dig.*, Oct. 2008, pp. 105–108.

[3] S. Trotta, B. Dehlink, A. Ghazinour, D. Morgan, and J. John, "A 77 GHz 3.3 V 4-channel transceiver in SiGe BiCMOS technology," in *IEEE BCTM Dig.*, Oct. 2009, pp. 186–189.

[4] S. Trotta, B. Dehlink, R. Reuter, Y. Yin, J. John, J. Kirchgessner, D. Morgan, P. Welch, J. J. Lin, B. Knappenberger, I. To, and M. Huang, "A multi-channel Rx for 76.5 GHz automotive radar applications with 55 dB IF channel-to-channel isolation," in *Proc. IEEE EuMIC*, Sep. 2009, pp. 192–195.

[5] S. Trotta, H. Knapp, D. Dibra, K. Aufinger, T. F. Meister, J. Bock, W. Simburger, and A. L. Scholtz, "A 79 GHz SiGe-bipolar spread-spectrum TX for automotive radar," in *IEEE ISSCC Dig.*, Feb. 2007, pp. 430, 613.

[6] T. Mitomo, N. Ono, Y. Yoshiara, O. Watanabe, and I. Seto, "A 77 GHz 90 nm CMOS transceiver for FMCW radar applications," *IEEE J. Solid-State Circuits*, vol. 45, no. 4, pp. 928–937, Apr. 2010.

[7] Y. Kawano, T. Suzuki, M. Sato, T. Hirose, and K. Joshin, "A 77 GHz transceiver in 90 nm CMOS," in *IEEE ISSCC Dig.*, Feb. 2009, pp. 310–312.

[8] S. T. Nicolson, K. H. K. Yau, S. Pruvost, V. Danelon, P. Chevalier, P. Garcia, A. Chantre, B. Sautreuil, and S. P. Voinigescu, "A low-voltage SiGe BiCMOS 77-GHz automotive radar chipset," *IEEE Trans. Microw. Theory Tech.*, vol. 56, no. 5, pp. 1092–1104, May 2008.

[9] S. T. Nicolson, P. Chevalier, B. Sautreuil, and S. P. Voinigescu, "Single-chip W-band SiGe HBT transceivers and receivers for Doppler radar and millimeter-wave imaging," *IEEE J. Solid-State Circuits*, vol. 43, no. 10, pp. 2206–2217, Oct. 2008.

[10] V. Jain, F. Tzeng, L. Zhou, and P. Heydari, "A single-chip dual-band 22–29-GHz/77–81-GHz BiCMOS transceiver for automotive radars," *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 3469–3485, Dec. 2009.
[11] J. Lee, Y. Li, M. Hung, and S. Huang, "A fully-integrated 77-GHz FMCW radar transceiver in 65-nm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2746–2756, Dec. 2010.
[12] J. Hasch, U. Wostradowski, S. Gaier, and T. Hansen, "77 GHz radar transceiver with dual integrated antenna elements," in *Proc. IEEE German Microwave Conf.*, Mar. 2010, pp. 280–283.
[13] B. Schoenlinner, X. Wu, J. P. Ebling, G. V. Eleftheriades, and G. M. Rebeiz, "Wide-scan spherical-lens antennas for automotive radars," *IEEE Trans. Microw. Theory Tech.*, vol. 50, no. 9, pp. 2166–2175, Sep. 2002.
[14] I. Gresham, N. Jain, T. Budka, A. Alexanian, N. Kinayman, B. Ziegner, S. Brown, and P. Staecker, "A compact manufacturable 76–77-GHz radar module for commercial ACC applications," *IEEE Trans. Microw. Theory Tech.*, vol. 49, no. 1, pp. 44–58, Jan. 2001.
[15] Y. Asano, S. Ohshima, T. Harada, M. Ogawa, and K. Nishikawa, "Proposal of millimeter-wave holographic radar with antenna switching," in *IEEE MTT-S Int. Symp. Dig.*, May 2001, pp. 1111–1114.
[16] R. Feger, C. Wagner, S. Schuster, S. Scheiblhofer, H. Jager, and A. Stelzer, "A 77-GHz FMCW MIMO radar based on an SiGe single-chip transceiver," *IEEE Trans. Microw. Theory Tech.*, vol. 57, no. 5, pp. 1020–1035, May 2009.
[17] A. Babakhani, X. Guan, A. Komijani, A. Natarajan, and A. Hajimiri, "A 77-GHz phased-array transceiver with on-chip antennas in silicon: Receiver and antennas," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2795–2806, Dec. 2006.
[18] K. Koh, J. W. May, and G. M. Rebeiz, "A millimeter-wave (40–45 GHz) SiGe BiCMOS 16-element phased-array transmitter," *IEEE J. Solid-State Circuits*, vol. 44, no. 5, pp. 1498–1509, May 2009.
[19] C. A. Balanis, *Antenna Theory: Analysis and Design*, 3rd ed. New York: Wiley-Interscience, 2005.
[20] D. Lockie and D. Peck, "High-data-rate millimeter-wave radios," *IEEE Microw. Mag.*, vol. 10, no. 5, pp. 75–83, Aug. 2009.
[21] J. Wells, "Faster than fiber: The future of multi-G/s wireless," *IEEE Microw. Mag.*, vol. 10, no. 3, pp. 104–112, May 2009.
[22] T. Kosugi, A. Hirata, T. Nagatsuma, and Y. Kado, "MM-wave long-range wireless systems," *IEEE Microw. Mag.*, vol. 10, no. 2, pp. 68–76, Apr. 2009.
[23] I. Sarkas, S. T. Nicolson, A. Tomkins, E. Laskin, P. Chevalier, B. Sautreuil, and S. P. Voinigescu, "An 18-Gb/s, direct QPSK modulation SiGe BiCMOS transceiver for last mile links in the 70–80 GHz band," *IEEE J. Solid-State Circuits*, vol. 45, no. 10, pp. 1968–1980, Oct. 2010.
[24] A. Valdes-Garcia, S. T. Nicolson, J. Lai, A. Natarajan, P. Chen, S. K. Reynolds, J. C. Zhan, D. Kam, D. Liu, and B. Floyd, "A fully integrated 16-element phased-array transmitter in SiGe BiCMOS for 60-GHz communications," *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2757–2773, Dec. 2010.
[25] S. K. Reynolds, A. S. Natarajan, M. Tsai, S. Nicolson, J. C. Zhan, L. Duixian, D. G. Kam, O. Huang, A. Valdes-Garcia, and B. A. Floyd, "A 16-element phased-array receiver IC for 60-GHz communications in SiGe BiCMOS," in *IEEE Radio Frequency IC Symp. Dig.*, May 2010, pp. 461–464.
[26] E. Cohen, C. Jakobson, S. Ravid, and D. Ritter, "A thirty two element phased-array transceiver at 60 GHz with RF-IF conversion block in 90 nm flip chip CMOS process," in *IEEE Radio Frequency IC Symp. Dig.*, May 2010, pp. 457–460.
[27] K. Kim, K. Ahn, T. Lim, H. Park, and J. Yu, "A 60 GHz wideband phased-array LNA with short-stub passive vector generator," *IEEE Microw. Wireless Compon. Lett.*, vol. 20, no. 11, pp. 628–630, Nov. 2010.
[28] S. Kishimoto, N. Orihashi, Y. Hamada, M. Ito, and K. Maruhashi, "A 60-GHz band CMOS phased array transmitter utilizing compact baseband phase shifters," in *IEEE Radio Frequency IC Symp. Dig.*, Jun. 2009, pp. 215–218.
[29] Y. Atesal, B. Cetinoneri, M. Chang, R. Alhalabi, and G. M. Rebeiz, "Millimeter-wave wafer-scale silicon BiCMOS power amplifiers using free-space power combining," *IEEE Trans. Microw. Theory Tech.*, vol. 59, no. 4, pp. 645–655, Apr. 2011.
[30] D. Shin and G. M. Rebeiz, "Low-power low-noise 0.13 μm CMOS X-band phased array receivers," in *IEEE MTT-S Int. Symp. Dig.*, May 2010, pp. 956–959.
[31] D. M. Pozar, *Microwave Engineering*, 3rd ed. New York: Wiley, 2004.
[32] K. Koh and G. M. Rebeiz, "A Q-band four-element phased-array front-end receiver with integrated Wilkinson power combiners in 0.18-μm SiGe BiCMOS technology," *IEEE Trans. Microw. Theory Tech.*, vol. 56, no. 9, pp. 2046–2053, Sep. 2008.
[33] D. W. Kang, J. G. Kim, B. W. Min, and G. M. Rebeiz, "Single and 4-element Ka-band transmit/receive phased-array silicon RFICs with 5-bit amplitude and phase control," *IEEE Trans. Microw. Theory Tech.*, vol. 57, no. 12, pp. 3534–3543, Dec. 2009.
[34] *BiCMOS-8HP Model Reference Guide*, IBM Microelectronics Division, Compact Model Development LZVV Dept., 2007.
[35] B. Min and G. M. Rebeiz, "Ka-band low-loss and high-isolation switch design in 0.13-μm CMOS," *IEEE Trans. Microw. Theory Tech.*, vol. 56, no. 6, pp. 1364–1371, Jun. 2008.
[36] S. Y. Kim and G. M. Rebeiz, "A 4-bit passive phase shifter for automotive radar applications in 0.13 μm CMOS," in *Proc. IEEE CSICS*, Oct. 2009, pp. 1–4.
[37] T. Yu and G. M. Rebeiz, "A 22–24 GHz 4-element CMOS phased array with on-chip coupling characterization," *IEEE J. Solid-State Circuits*, vol. 43, no. 9, pp. 2134–2143, Sep. 2008.
[38] *Sonnet*. Sonnet Software Inc., Syracuse, NY.
[39] *Cascade Impedance Standard Substrate*. Cascade Microtech [Online]. Available: http://www.cmicro.com
[40] K. Koh and G. M. Rebeiz, "An X- and Ku-band 8-element phased-array receiver in 0.18-μm SiGe BiCMOS technology," *IEEE J. Solid-State Circuits*, vol. 43, no. 6, pp. 1360–1371, Jun. 2008.

Sang Young Kim (S'05) received the B.S. degree in electrical engineering from Seoul National University (SNU), Seoul, Korea, in 2003, the M.S. degree in electrical engineering from the University of Southern California (USC), Los Angeles, in 2005. He is currently working toward the Ph.D. degree in electrical engineering at the University of California at San Diego (UCSD), La Jolla. His doctoral study is on RF and millimeter-wave integrated circuits and phased arrays in silicon technologies.

Gabriel M. Rebeiz (F'97) received the Ph.D. degree from the California Institute of Technology, Pasadena.

He is a Professor of electrical and computer engineering at the University of California at San Diego (UCSD). Prior to this appointment, he was at the University of Michigan from 1988 to 2004. He contributed to planar mm-wave and THz antennas and imaging arrays from 1988 to 1996, and his group has optimized the dielectric-lens antennas, which is the most widely used antenna at mm-wave and THz frequencies. Prof. Rebeiz' group also developed 6–18 GHz and 40–50 GHz 8-and 16-element phased arrays on a single silicon chip, and the first mm-wave silicon passive imager chip at 85–105 GHz. His group also demonstrated high-Q RF MEMS tunable filters at 1–6 GHz (Q>200) and the new angular-based RF MEMS capacitive and metal-contact switches. As a consultant, he helped develop the USM/ViaSat 24 GHz single-chip SiGe automotive radar, phased arrays operating at X, Ku-band, and W-band for defense and commercial applications, the RFMD RF MEMS switch and the Agilent RF MEMS switch. He is the Director of the UCSD/DARPA Center on RF MEMS Reliability and Design Fundamentals. He is the author of the book *RF MEMS: Theory, Design and Technology* (Wiley, 2003).

Prof. Rebeiz is an IEEE Fellow, an NSF Presidential Young Investigator, an URSI Koga Gold Medal Recipient, and the IEEE MTT 2003 Distinguished Young Engineer. He is the recipient of the IEEE MTT 2000 Microwave Prize, the IEEE MTT 2010 Distinguished Educator Award and the IEEE AP 2011 John D. Kraus Award. He also received the 1998 Eta-Kappa-Nu Professor of the Year Award and the 1998 Amoco Teaching Award given to the best undergraduate teacher at the University of Michigan, and the 2008 Teacher of the Year Award at the Jacobs School of Engineering, UCSD. His students have won a total of 19 best paper awards at IEEE MTT, RFIC and AP-S conferences. He has been an Associate Editor of IEEE MTT, and a Distinguished Lecturer for IEEE MTT and IEEE AP. He has graduated 42 Ph.D. students, and currently leads a group of 20 Ph.D. students and two Post-Doctoral Fellows in the area of mm-wave RFIC, microwaves circuits, RF MEMS, planar mm-wave antennas and terahertz systems.