A 70–100 GHz Direct-Conversion Transmitter and Receiver Phased Array Chipset Demonstrating 10 Gb/s Wireless Link

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***Abstract*—A transmitter and receiver phased array chipset is demonstrated in the range between 70 and 100 GHz using a 0.18 µm SiGe BiCMOS process with f_T/f_{MAX} of 240/270 GHz. Each chip comprises four phased array elements with distributed calibration memory and calibrated direct up- and down-conversion mixer chain. Each receive channel has a conversion gain of 33 dB and noise figure of < 7 dB from 75–95 GHz. Each transmit channel has a flat saturated output power of > 5 dBm between 70 and 100 GHz. Both transmitter and receiver arrays operate from 1.5 V and 2.5 V power supplies and consume 1 W each. Using a die-on-PCB prototype with integrated antennas, a wireless link operating at 10 Gb/s (using 16-QAM) or 8.75 Gb/s (using 32-QAM) is demonstrated at a distance of 1-meter with a carrier frequency of 88 GHz.**

***Index Terms*—Die-on-PCB, direct-conversion, down-converter, E-band, integrated antenna, MMIC, multi-gigabit wireless link, phase amplitude calibration, phased array, QAM constellation, SiGe BiCMOS, transmitter receiver array, up-converter, W-band.**

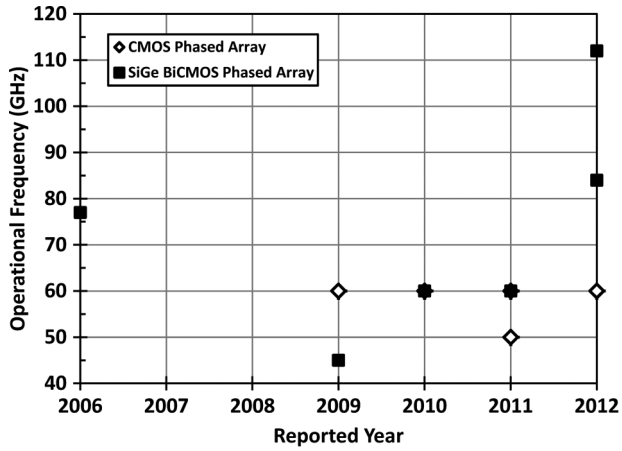

Fig. 1. Survey of state-of-the art Silicon V- and W-band phased arrays intended for short-reach, cellular backhaul and last mile applications.

I. Introduction

THANKS to the introduction of high-performance SiGe BiCMOS and nano-scale CMOS technologies, Silicon has made its foray into mm-wave applications. In the mm-wave wireless domain, two applications have received significant research efforts: i) last mile, high-data-rate, point-to-point wireless links for backhaul cellular applications operating in the E-band, ii) short-reach, multi-gigabit radios operating around 60 GHz for uncompressed video streaming and wireless serial link replacement [1]–[18]. Both applications enjoy a wide, unrestricted allocated bandwidth (71–76 GHz, 81–86 GHz and 92–95 GHz in the case of E-band and 57–66 GHz for 60 GHz radios) allowing multi-gigabit wireless links to be realized. Furthermore, Silicon-based receivers and transmitters have been demonstrated operating up to D-band and the high integration density has enabled fully integrated multi-channel phased arrays to be realized [1]–[4], [6], [7], [10]–[16], [18]. Fig. 1 shows an operational-frequency scatterplot of mm-wave transceivers and arrays reported in recent years.

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In this paper, we present receiver and transmitter arrays designed for steerable-beam and highly spectral efficient data links in both E- and W-band. The arrays were designed to span the complete frequency range in the newly released commercial bands at 71–76, 81–86 and 92–95 GHz with low noise figure and good output power. Additionally, accurate I/Q-calibration and good linearity enables the use of higher order modulation format such as QAM for higher aggregated data throughput. Furthermore, we present an inexpensive die-on-PCB and antenna-on-PCB prototype for multi-gigabit wireless link demonstration.

This paper is organized as follows. Section II presents the transmitter and receiver phased array architecture and design with detailed block diagrams and schematics of critical components. Section III discusses the chipset fabrication details as well as the design and implementation of the antenna-on-PCB and die-on-PCB prototype. Section IV presents all wafer probe measurements and wireless link demonstration. Concluding remarks are made in Section V.

II. Transmitter and Receiver Phased Array Architecture and Design

The block diagrams of the 4-element receiver and transmitter phased arrays are shown in Fig. 2. Each integrated circuit consists of either I/Q direct up- or down-conversion chain with IF variable gain amplifiers (VGAs) and LO frequency doubler. Each array element employs 4-bit phase shifters with the addition of low noise amplifiers (LNAs) or power amplifiers (PAs)

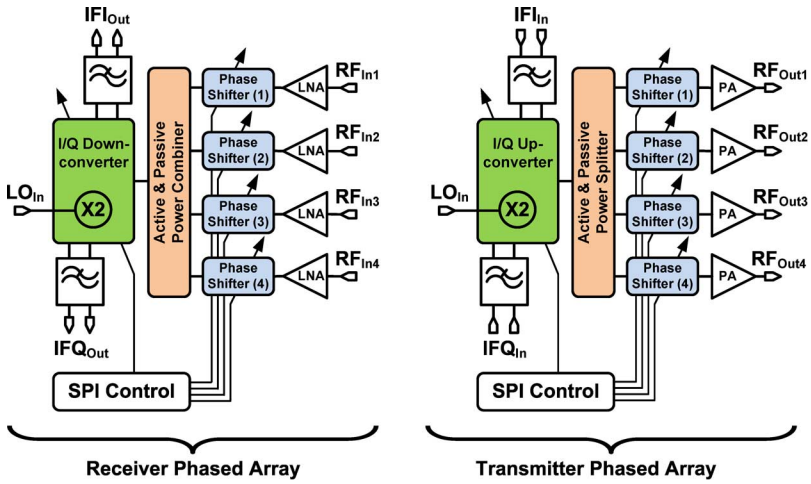

Fig. 2. Simplified block diagram of the implemented 4-element phased array receiver (left) and transmitter (right) chipset. Each integrated circuit is equipped with a global SPI interface for settings and calibration.

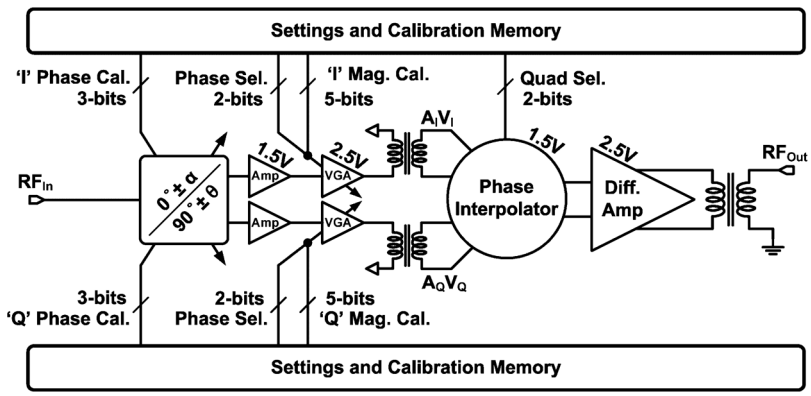

Fig. 3. Block diagram of the implemented 4-bit W-band phase shifter. Each phase shifter is equipped with an internal settings and calibration memory which can be accessed through the global SPI interface.

for the receiver and transmitter array respectively. Active and passive signal dividers are used to distribute signals from the phase shifters to the frequency conversion blocks. Various RF and LO stages are stagger-tuned between 75 GHz–100 GHz to increase the overall system bandwidth. All calibration settings, phase shifter control and biasing circuitry are configured through a global Serial Peripheral Interface (SPI) link. Detailed circuit schematics, simulations and operation of all major phased array blocks are presented in the following sections.

A. W-Band 4-Bit Phase Shifter

The schematic diagram of the W-band 4-bit phase shifter is shown in Fig. 3. The phase shifter uses vector summation to synthesize any phase between 0° to 360°. A quadrature splitter generates in-phase and quadrature components which can be described as a function of the input signal ($\mathrm{RF_{In}}$),

$$\begin{cases} \boldsymbol{V_I} = \frac{\mathrm{RF_{In}}}{\sqrt{2}} \\ \boldsymbol{V_Q} = \mathrm{j}\frac{\mathrm{RF_{In}}}{\sqrt{2}} \end{cases} \tag{1}$$

Each signal ($\mathrm{V_I}$ and $\mathrm{V_Q}$) is then applied to independent VGAs whose outputs are summed using a linear phase interpolator. The resulting output vector ($\mathrm{RF_{Out}}$) can be mathematically described as a function of the VGA gains $\mathrm{A_I}$ and $\mathrm{A_Q}$,

$$\boldsymbol{RF_{Out}} = A_I \boldsymbol{V_I} + A_Q \boldsymbol{V_Q} = A_I \frac{\boldsymbol{RF_{In}}}{\sqrt{2}} + \boldsymbol{j} A_Q \frac{\boldsymbol{RF_{In}}}{\sqrt{2}} \tag{2}$$

Assuming that the normalized VGA gains ($\mathrm{A_I}$ and $\mathrm{A_Q}$) can take any value between $\{-1, 1\}$, the phase and magnitude components of the output signal can be derived through vector algebra [9],

$$|\boldsymbol{RF_{Out}}| = \frac{|\boldsymbol{RF_{In}}|}{\sqrt{2}} \sqrt{|A_I| + |A_Q|} \tag{3}$$

$$\angle \boldsymbol{RF_{Out}} = \angle \boldsymbol{RF_{In}} + \begin{cases} 0° + \tan^{-1}\left(\frac{A_Q}{A_I}\right), A_I \geq 0, A_Q \geq 0 \\ 180° - \tan^{-1}\left(\frac{A_Q}{A_I}\right), A_I < 0, A_Q \geq 0 \\ 180° + \tan^{-1}\left(\frac{A_Q}{A_I}\right), A_I < 0, A_Q < 0 \\ 360° - \tan^{-1}\left(\frac{A_Q}{A_I}\right), A_I \geq 0, A_Q < 0 \end{cases} \tag{4}$$

1) Transformer-Based Quadrature Hybrid: The quadrature hybrid is based on the lumped implementation of coupled lines which was first introduced in [19]. At any desired frequency,

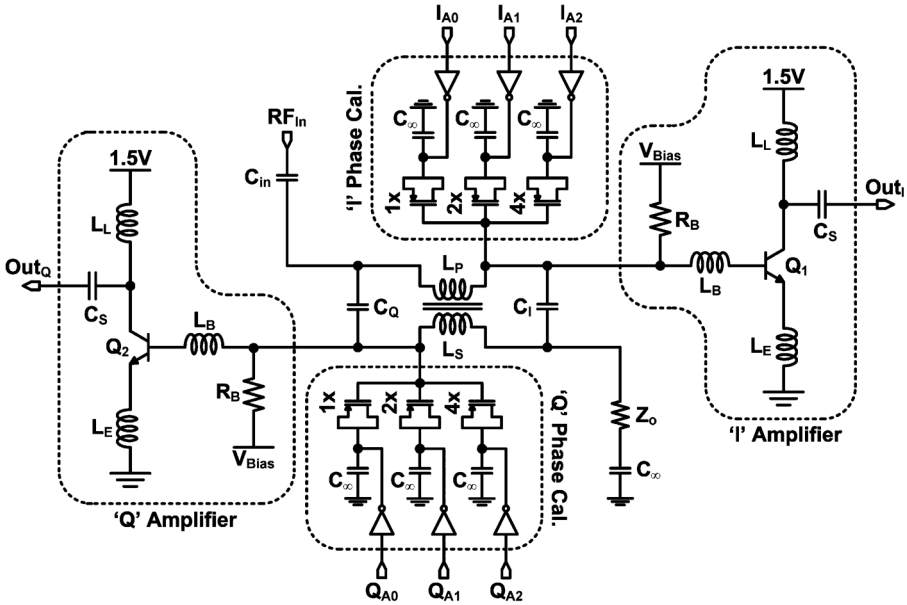

Fig. 4. Schematic of the transformer-based quadrature hybrid and I/Q amplifiers. The addition of varactor banks to the transformer structure enables digital quadrature phase calibration across the W-band.

simultaneous amplitude balance and quadrature outputs are achieved by selecting the values of mutual inductance, coupling capacitance and coil inductances as described in [19]. However, depending on the back-end-of-line technology (BEOL), implementing a transformer with the required coupling factor and coil inductance may not be possible. Furthermore, acceptable performance of passive implementation of a quadrature hybrid is limited to a relatively narrow frequency range. Therefore, calibration of the quadrature hybrid is essential to enable its use in broadband phase shifters. Fig. 4 shows the schematic of our quadrature hybrid with the addition of varactor banks which can be used for phase calibration. The varactors are implemented using thin-oxide 0.18 μm AMOS devices. These binary-weighted AMOS varactors provide 3-bits ($\mathrm{I_{A0-2}}$ and $\mathrm{Q_{A0-2}}$) of minor phase adjustment on each of the 'I' and 'Q' outputs for a total of 16 calibration phase settings. Fig. 5 shows the simulated phase and magnitude balance of the quadrature hybrid as a function of the digital varactor settings. These varactor banks enable quadrature phase generation over a much broader frequency range compared to a traditional hybrid with fixed capacitance values. Furthermore, varactor settings have a weak impact on the amplitude balance. Therefore amplitude calibration can be performed independently from phase calibration.

Fig. 4 also shows the schematic of the 'I' and 'Q' amplifiers. These common-emitter amplifiers operate from 1.5 V and compensate for the losses introduced by the passive hybrid. Furthermore, they isolate the sensitive hybrid output nodes from impedance variations of the subsequent VGA stages.

2) Variable Gain Amplifiers (VGAs): The 'I' and 'Q' VGAs, whose schematics are reproduced in Fig. 6, consist of single-ended bipolar cascode amplifiers ($\mathrm{Q_{1-3}}$ and $\mathrm{Q_{8-10}}$) with transformer loads for single-ended to differential conversion. The collector of transistors $\mathrm{Q_3}$ and $\mathrm{Q_{10}}$, which would normally be tied to the power supply, are connected to a dummy inductor $\mathrm{L_D}$. The purpose of this dummy load is to emulate the transformer's primary coil inductance ($\mathrm{L_P}$). This approach minimizes impedance variations of the cascode node at various gain settings.

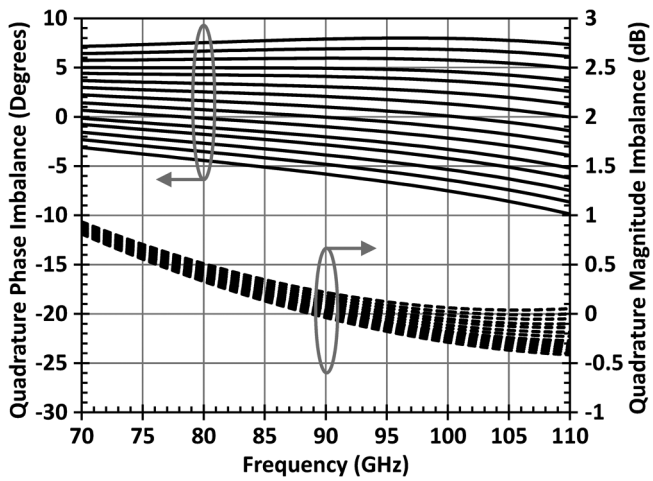

Fig. 5. Simulated phase and magnitude balance of the transformer-based quadrature hybrid as a function of digital varactor settings. A total of $\pm 8^\circ$ of phase adjustment (solid lines) can be achieved with minimal impact on magnitude balance (dashed lines).

The VGA gain is set by adjusting the relative currents between the cascode transistors $\mathrm{Q_{2-3}}$ and $\mathrm{Q_{9-10}}$ through the use of digitally controlled 7-bit pre-distortion blocks. In this design the VGAs accomplish three functions: i) perform amplitude calibration of the preceding quadrature hybrid, ii) act as the transconductance for the phase interpolator stage and iii) enable partial phase selection for the overall phase shifter. The first five least significant bits ($\mathrm{I_{B0-4}}$ and $\mathrm{Q_{B0-4}}$) compensate for the quadrature hybrid amplitude imbalance between the 'I' and 'Q' paths as well as the arctangent nonlinearity described in (4). The remaining two most significant bits ($\mathrm{I_{B5-6}}$ and $\mathrm{Q_{B5-6}}$) are used for phase selection within each quadrant.

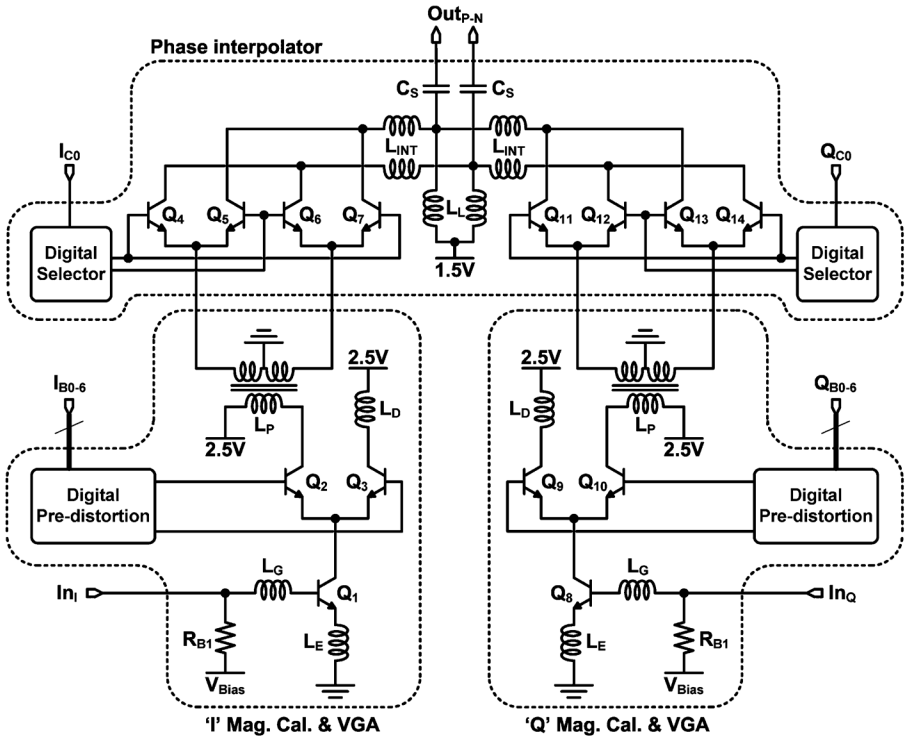

Fig. 6. Schematic of the I/Q VGAs and phase interpolator implemented in the phase shifters. Transformers are used at the interface of the single-ended VGAs and the differential phase interpolator which operates from 1.5 V.

3) Phase Interpolator: The schematic of the transformer coupled phase interpolator is also shown in Fig. 6. It consists of two identical half circuits operating from 1.5 V. Their outputs are summed passively using $\mathrm{L_{INT}}$ and $\mathrm{L_L}$. The resulting differential output $(\mathrm{Out_{P-N}})$ is the weighted sum of the signals $\mathrm{In_I}$ and $\mathrm{In_Q}$. The digital selector bits ($\mathrm{I_{C0}}$ and $\mathrm{Q_{C0}}$) are used to select the desired output phase quadrant. After calibration, the digital settings of the phase interpolator in conjunction with the VGAs enable 4-bits of phase shifting in 22.5° steps as described by equation (5), shown at the bottom of the page. Each phase shifter is equipped with on-chip memory where calibration, phase and bias settings are stored. This distributed memory allows for independent calibration of each array element through the global SPI interface. The calibration process may be applied at multiple frequencies within the W-band and the corresponding calibration bits can be loaded according to the desired frequency range of operation. This is particularly beneficial to implement systems which will serve in multiple channels in the W-band spectrum.

B. RF Signal Distribution

To overcome losses associated with purely passive signal distribution, the RF path of each phased array is implemented with a combination of active and passive signal distribution. The overall response of the signal distribution is designed to offer a few dB of gain within the frequency band of interest. To reduce power consumption and chip size, single-ended RF signal distribution networks are implemented.

1) Receiver Power Combiner: Fig. 7 (top) shows the schematic of the receiver RF signal distribution. A pair of Wilkinson power combiners is used to combine the RF signal from the four phased array elements. The resulting two signals are then applied to an active power combiner. It consists of two common-emitter amplifiers ($\mathrm{Q_1}$ and $\mathrm{Q_2}$) whose outputs are summed and applied to a common-base amplifier $(\mathrm{Q_3})$. The output collector of the common-base amplifier simultaneously drives two transformers which perform single-ended to differential conversion before the I/Q down-conversion mixer.

2) Transmitter Power Splitter: Fig. 7 (bottom) shows the schematic of the transmitter RF signal distribution. The differential output of the I/Q up-conversion mixer is converted to single ended by a balun $(\mathrm{X_1})$ before being applied to the RF signal distribution. The active power splitter consists of a bipolar cascode amplifier $(\mathrm{Q_1})$ whose common-base transistor has been divided into two transistors of the same size ($\mathrm{Q_{2–3}}$).

$$\angle \boldsymbol{RF_{Out}} = \angle \boldsymbol{RF_{In}} + \begin{cases} 11.25^\circ + 22.5^\circ(I_{B0} + 2I_{B1}), Q_{B5-6} = \overline{I_{B5-6}}, I_{C0} = 0, Q_{C0} = 0 \\ 168.75^\circ - 22.5^\circ(I_{B0} + 2I_{B1}), Q_{B5-6} = \overline{I_{B5-6}}, I_{C0} = 1, Q_{C0} = 0 \\ 191.25^\circ + 22.5^\circ(I_{B0} + 2I_{B1}), Q_{B5-6} = \overline{I_{B5-6}}, I_{C0} = 1, Q_{C0} = 1 \\ 348.75^\circ - 22.5^\circ(I_{B0} + 2I_{B1}), Q_{B5-6} = \overline{I_{B5-6}}, I_{C0} = 0, Q_{C0} = 1 \end{cases} \quad (5)$$

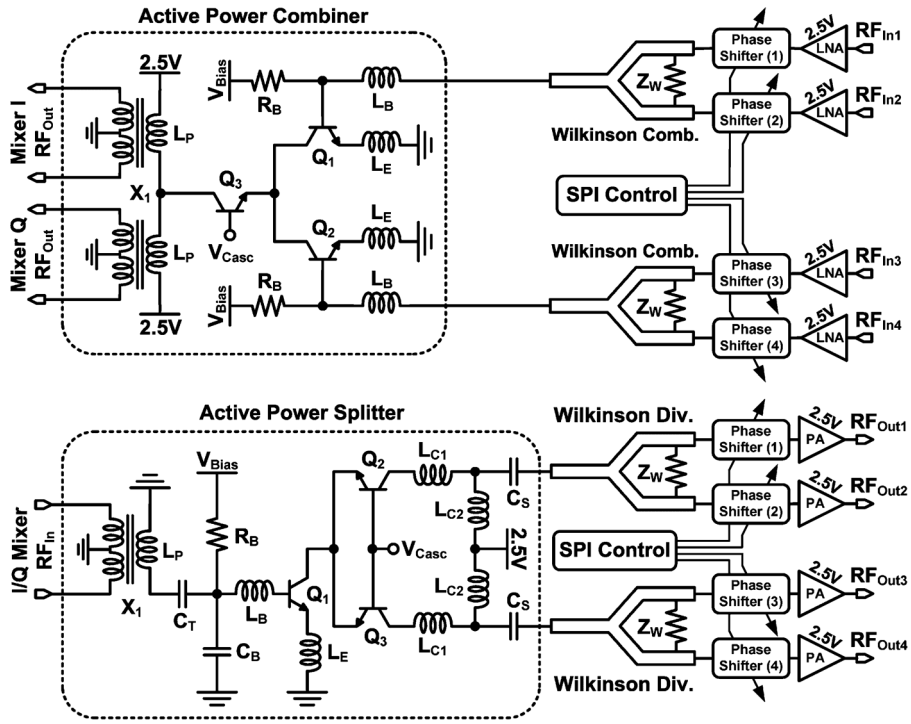

Fig. 7. Schematic of the active and passive power combiner (top) and power splitter (bottom) used in the phased array chipset. Transformers are used at the interface between the differential mixers to the single-ended signal distribution networks.

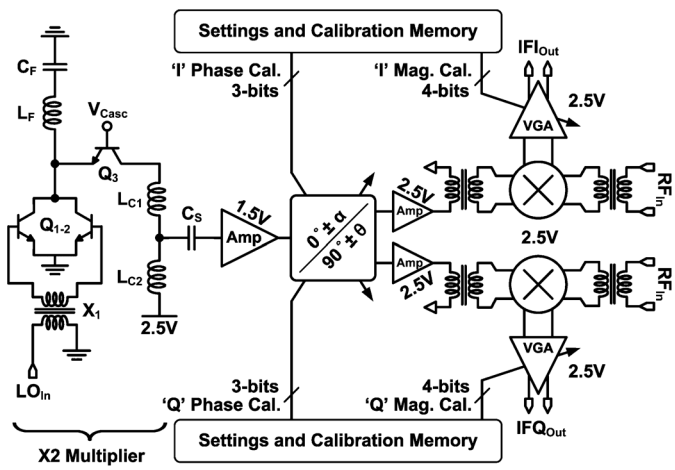

Fig. 8. Schematic of the LO doubler and I/Q direct down-conversion mixer. The LO doubler employs a notch filter (C_F and L_F) for improved fundamental tone rejection.

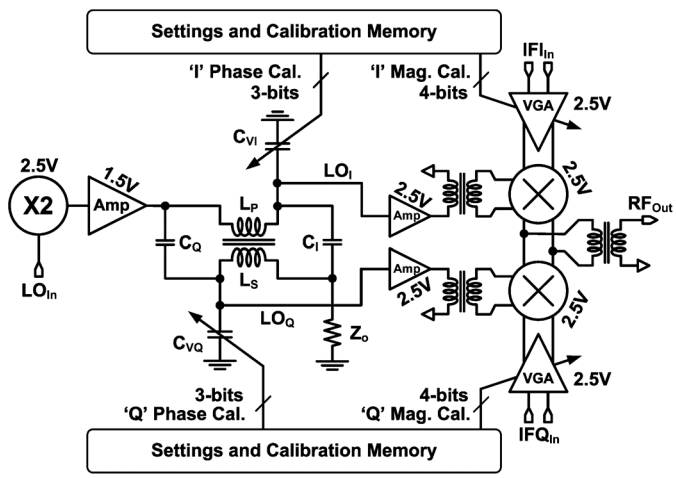

Fig. 9. Schematic of the transformer-based quadrature hybrid and I/Q direct up-conversion mixer. The quadrature hybrid employs varactor banks for I/Q calibration at the desired LO frequency.

The resulting two outputs then drive two identical Wilkinson dividers which directly connect to the phase shifter elements.

C. I/Q Frequency Converters

The schematic and block diagram of various elements of the I/Q frequency converters are shown in Fig. 8 and Fig. 9. Both the up- and down-conversion blocks are equipped with a frequency doubler, LO amplifier chain, transformer based quadrature hybrid, I/Q mixers and IF variables gain amplifiers.

1) W-Band Frequency Doubler: The schematic of the frequency doubler is shown in Fig. 8. The half-rate input LO signal is converted to differential signals via a transformer (X_1) whose outputs drive transistors Q_{1-2}. The second harmonic is collected and amplified by the common-base transistor Q_3 while the fundamental tone is further attenuated by the LC band-stop filter C_F and L_F. This allows efficient doubling of the frequency while attaining high fundamental rejection over a wide bandwidth. The output of the frequency doubler is amplified by a 1.5 V common-emitter amplifier before being applied to the quadrature hybrid.

The single-ended LO output of the common-emitter amplifier is processed by a quadrature hybrid with phase calibration capability (Fig. 9). The quadrature outputs (LO_I and LO_Q) are applied to a pair of high-gain amplifiers operating in limiting

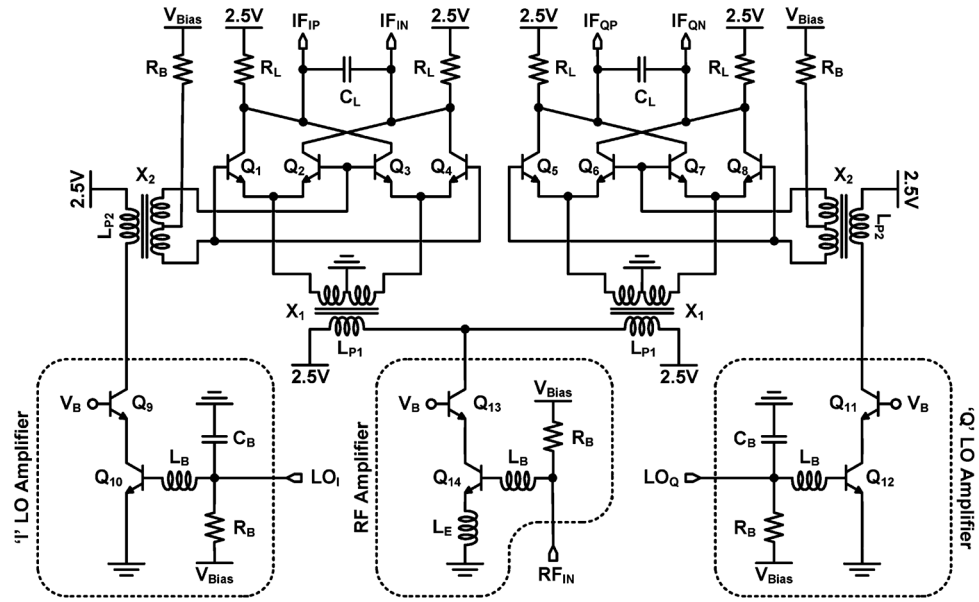

Fig. 10. Schematic of the I/Q down-conversion mixer, RF and LO amplifiers. The mixer uses transformers at both the RF and LO interfaces for single-ended to differential conversion.

mode. This combination reduces the impact of quadrature hybrid amplitude imbalance.

2) I/Q Down-Conversion Mixer: Fig. 10 shows the schematic of the I/Q down-conversion mixer. Transformers X_1 and X_2 are used at the interfaces to the double-balanced mixer (Q_{1-8}) to convert the single-ended RF and LO signal to differential. The RF cascode amplifier (Q_{13-14}) acts as the transconductance of the mixer and employs heavy inductive degeneration for improved linearity and impedance matching. This combination allows the mixer to operate from 2.5 V. Unlike the RF amplifier, the 'I' and 'Q' LO amplifiers operate in limiting mode and instead use series inductance $(\mathrm{L_B})$ and shunt capacitance $(\mathrm{C_B})$ to achieve impedance matching. The mixer output employs a single-pole low-pass filter ($\mathrm{R_L}$ and $\mathrm{C_L}$) to limit the output bandwidth to below 8 GHz.

3) I/Q Up-Conversion Mixer: The schematic of the BiCMOS I/Q up-conversion mixer is shown in Fig. 11. Similar to the down-converter, the LO amplifiers interface with the mixer through a pair of transformers (X_1). The mixer IF inputs comprise 0.18 μm nMOS transistors which are biased at high current density $(J = 0.3\ \mathrm{mA}/\mu\mathrm{m})$. This biasing approach offers a combination of high-linearity and bandwidth on the IF path [20]. Furthermore, the mixer uses no tail current sources in order to operate from a single 2.5 V supply [21]. The differential mixer output signal from transistors (Q_{1-8}) is converted to single-ended using balun X_2 before being applied to the RF signal distribution network.

4) Low Noise Amplifier (LNA) and Power Amplifier (PA): The schematics of the implemented LNA and PA are shown in Fig. 12. The LNA comprises a single-stage cascode amplifier (Q_{1-2}). The input pad capacitance (approximately 12 fF) is absorbed into the matching capacitor $\mathrm{C_B}$. The output matching uses a split inductor load $(\mathrm{L_{C1-2}})$ with the series capacitor $\mathrm{C_m}$.

The power amplifier (Fig. 12) performs differential to single-ended conversion and output signal matching through the use an output transformer and series matching capacitor $\mathrm{C_m}$. Common-mode inductive and resistive degeneration has also been added to the differential cascode circuit to improve its common-mode rejection ratio.

5) IF Variable Gain Amplifiers: Fig. 13 shows the schematic of the differential IF variable gain amplifier. The core of the amplifier comprises a common-emitter stage (Q_{1-2}) with digitally selectable resistive degeneration $(\mathrm{R_{E0-3}})$ for gain control. Each of the four control bits drives an nMOS transistor which operates as a switch (Q_{5-8}). Both the transmitter and receiver IF amplifiers offer 6 dB of digital gain control with 0.35 dB steps. This fine gain control can be used to compensate for I/Q amplitude imbalance and to improve image rejection.

III. Fabrication and Antenna-on-PCB Design

The transmitter and receiver arrays have been implemented in the TowerJazz 0.18 μm SBC18H3 SiGe BiCMOS process. The process offers 0.18 μm CMOS transistors, HBT bipolar devices with f_T/f_{MAX} of 240/270 GHz, thin film capacitors, resistors and 6 layers of Aluminum metallization. All passive elements were modeled using EMX from Integrand Software [22].

The die photos of the chipset are shown in Fig. 14. The die area of both the transmitter and receiver array is 1.7 mm × 2 mm including pads. Various test structures including that of the phase shifter, frequency multiplier and RF distribution network have also been fabricated for the purpose of characterization. To demonstrate the capability of the chipset in wireless link, a die-on-PCB prototype with integrated antennas has been assembled.

A. Die- and Antenna-on-PCB Design

Since the implemented phased array chipset is capable of operating in a wide frequency range extending over almost the entire W-band, it is desirable to have an antenna array that has broad bandwidth without sacrificing much of gain or efficiency.

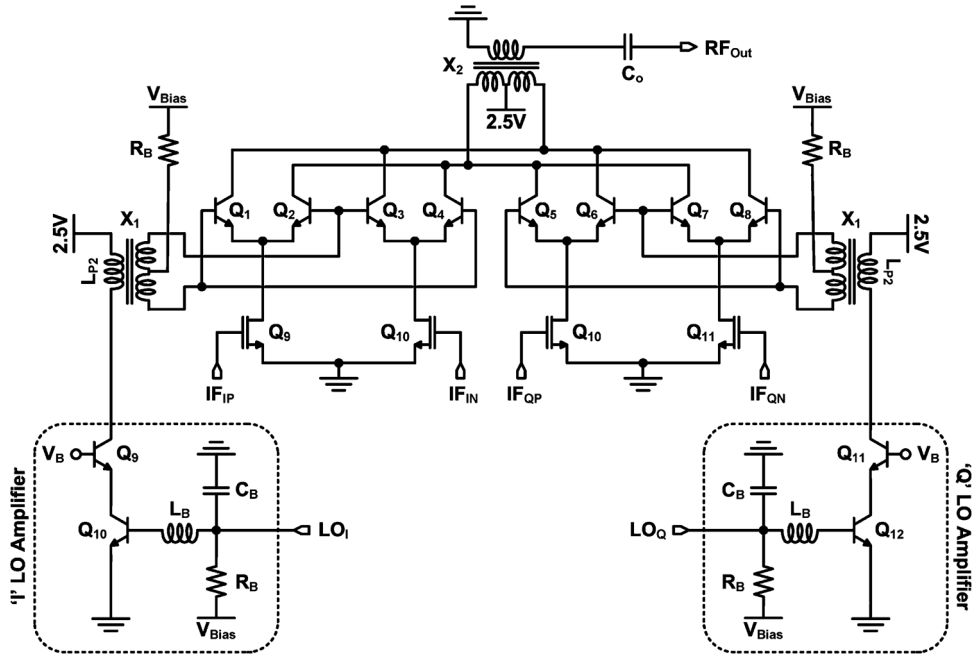

Fig. 11. Schematic of the I/Q up-conversion mixer and LO amplifiers. The BiCMOS mixer uses 0.18 μm nMOS transistors at the IF input ports for improved linearity.

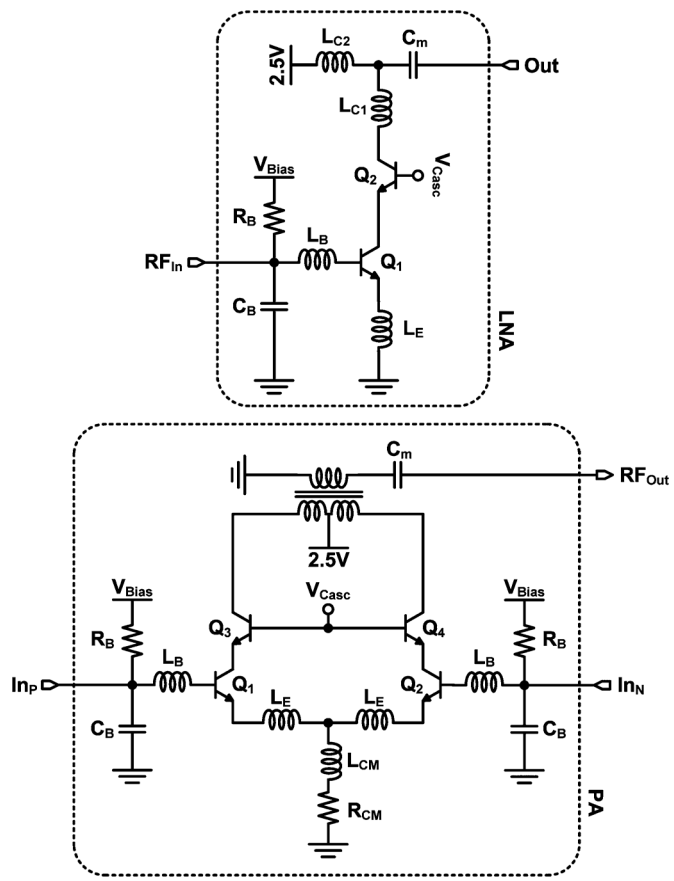

Fig. 12. Schematic of the LNA with split inductor output matching (top) and differential to single-ended PA using an output balun (bottom).

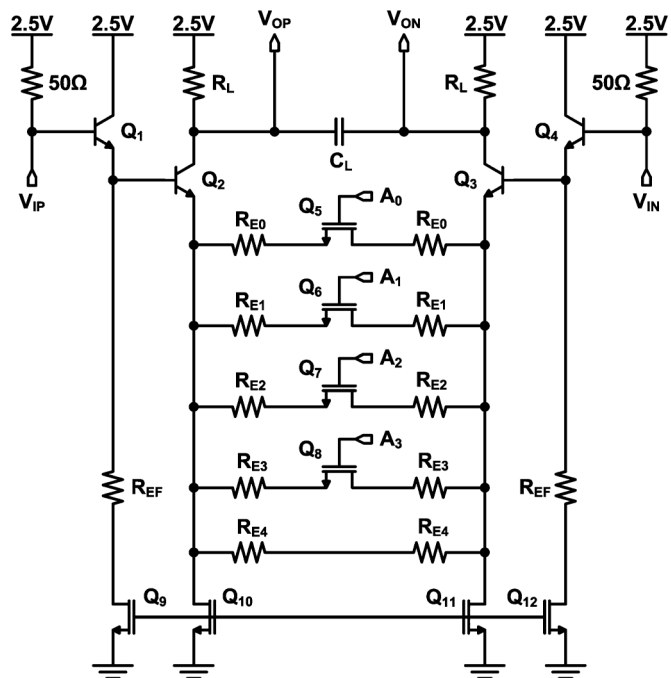

Fig. 13. Schematic of the IF variable gain amplifier. Each IF amplifier offers 6 dB of digital gain control with 0.35 dB steps.

The antenna array shown in Fig. 15 is designed to achieve the wide bandwidth while maintaining good gain and efficiency. While the proposed antenna and array can be realized in conventional microwave substrate such as quartz, we have chosen a high-speed PCB Megtron-6 [23] substrate for array fabrication to further advance the knowledge and techniques of millimeter-wave antenna integration. The usage of such substrate material in this frequency band is a novel attempt to the authors' best knowledge. Such PCB fabrication process would enable the

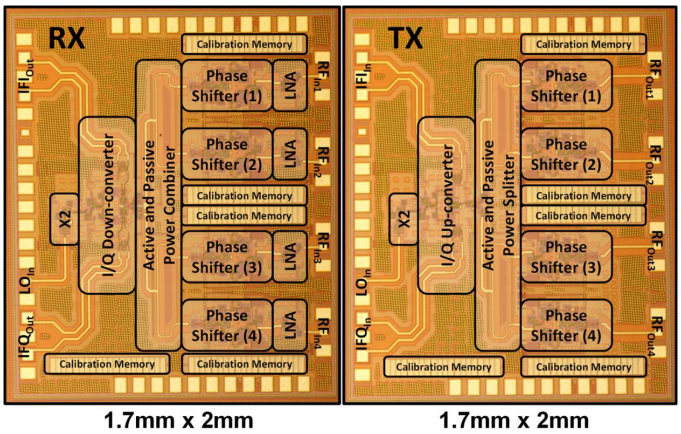

Fig. 14. Die photograph of the receiver phased array (left) and transmitter phased array (right). Both chips occupy an area of 1.7 mm × 2 mm including pads.

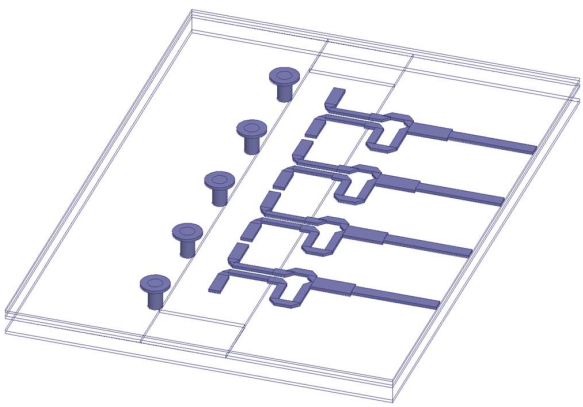

Fig. 15. A 3-dimensional view of the implemented phased array antenna. The antennas are implemented using the top metal layer of the printed circuit board.

integration of antennas into the rest of the control circuit and achieve simplification of overall module fabrication.

The proposed antenna element is a dipole antenna fed by microstrip line with transition to coplanar stripline (CPS). In this regards, the antenna configuration resembles a previously reported quasi-Yagi antenna [24]. The dipole antenna is backed by the conductor ground plane that acts as a quarter-wave reflector. The antenna's radiating elements are fed by a uni-planar balun which eliminates the need for the RF signal vias. The entire antenna array (including all elements and quarter-wave reflector) is implemented in a single substrate fabrication process as opposed to multiple fabrication and integration steps which may be required for typical antenna super-strate approach [8]. The stripline with ground vias (shown north of dipole driver elements) suppress the endfire propagation and direct the antenna to form broadside radiation with a simulated gain of 6-dB. Such broadside radiation is desirable as it enables antenna operation in low profile implementation. The proposed single fabrication approach can be extended to add director elements to form Yagi antennas in broadside radiation to achieve even higher directivity. The relatively complicated feeding network including balun (balanced to unbalanced transformer) is integrated to interface with the single-ended outputs from the phased array elements.

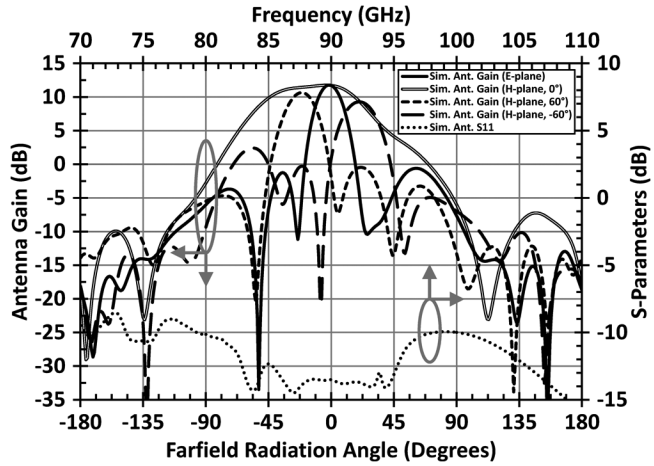

Fig. 16. Simulated antenna default radiation pattern and return loss. The PCB-integrated antenna array achieves broadband operation with 12 dB of maximum gain.

Fig. 16 shows the simulated return loss of the proposed antenna which achieves broadband operation of 19-GHz corresponding to 21-% bandwidth for $S_{11}<-10$ dB. Fig. 16 also shows the simulated default radiation pattern of the antenna array and the scanned beams at two different scan angles. The progressively linear phase offsets of 60° and −60° are added to the excitation source of antenna elements. The computed radiation pattern shows that the antenna gain peak is found at 20° and −20° respectively. The detail characteristics of the antenna array including measured radiation patterns is not in the scope of this paper and will be reported in a future publication.

IV. Measurement Results

Both the transmitter and receiver phased arrays operate from 1.5 V and 2.5 V power supplies and consume 1 W of total power. All high frequency measurements have been performed on wafer and on a single phased array element. All phased array simulation are performed using the Agilent GoldenGate suite [25] and show good agreement with the measured results.

A. Phase Shifter Measurements

A circuit breakout is used to measure the performance of the phase shifter. Fig. 17 shows the simulated and measured S-parameters. The phase shifter has a measured 3 dB bandwidth of approximately 20 GHz and a maximum gain of 19 dB.

The phase and magnitude error of the phase shifter is shown in Fig. 18. The phase shifter has been calibrated at 90 GHz and the total magnitude error at the calibration frequency is approximately ±1 dB (0.57 dB rms) and remains better than ±1.5 dB within the W-band. Similarly, a very low phase error is also observed at the calibration frequency. The phase error is better than $\pm 0.5^\circ$ (0.27° rms) at 90 GHz and remains better than $\pm 5^\circ$ between 82 GHz to 105 GHz. Furthermore, the phase shifter can achieve similarly low rms phase and magnitude errors at any selected calibration frequency within its 3 dB bandwidth.

B. I/Q Phased Array Receiver Measurements

The receiver down-conversion gain has been measured for each array element individually and is shown in Fig. 19. Each

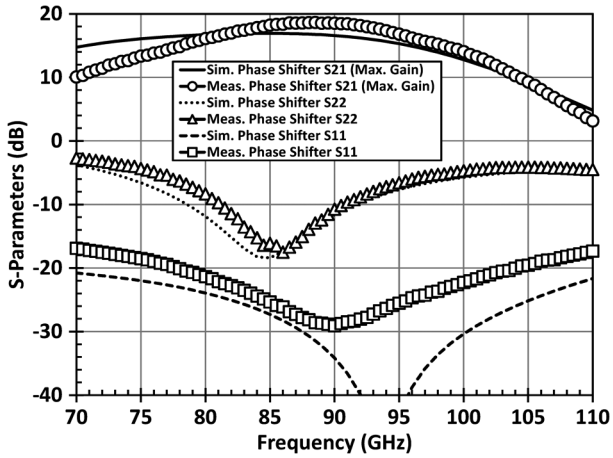

Fig. 17. Simulated and measured phase shifter S-parameters. The phase shifter has a measured 3 dB bandwidth of 19 GHz and maximum gain of 19 dB.

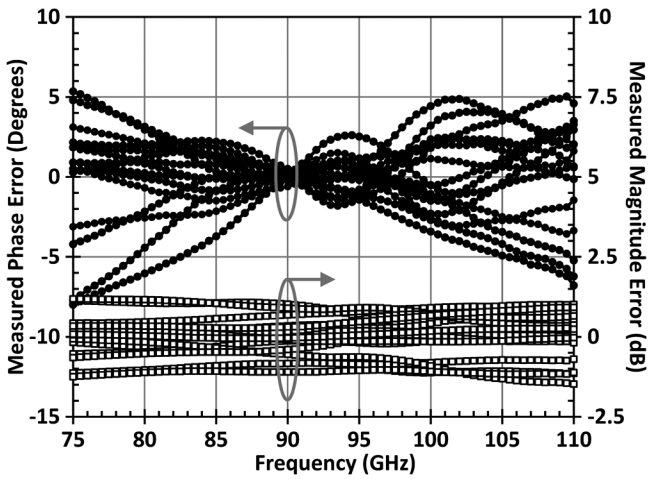

Fig. 18. Measured phase shifter phase and magnitude error after calibration at 90 GHz.

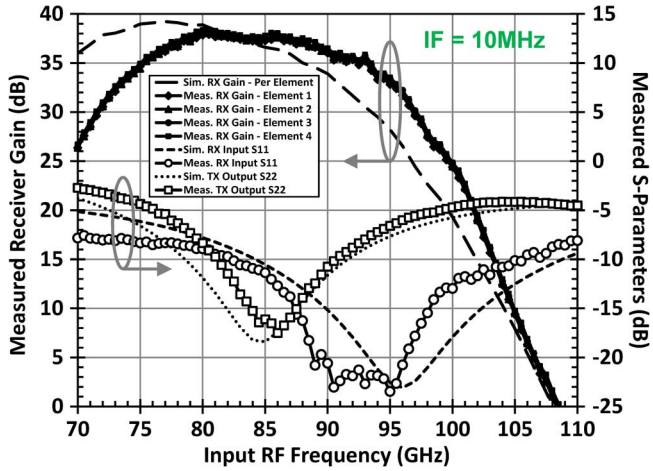

Fig. 19. Simulated and measured receiver gain, LNA input return loss and PA output return loss versus frequency for each array element at a fixed IF frequency of 10 MHz.

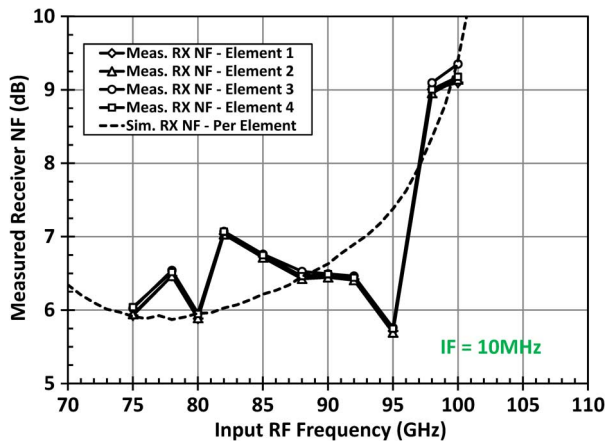

Fig. 20. Simulated and measured receiver NF versus input RF frequency of each array element at a fixed IF frequency of 10 MHz. The measured noise figure is better than 7 dB between 75 GHz to 95 GHz.

receiver element achieves a bandwidth of about 20 GHz and a maximum conversion gain of 37 dB. Under default settings, the gain variation between the four elements is better than 0.5 dB. The measured IF bandwidth and gain control is approximately 8 GHz and 6 dB respectively.

The measured total down-conversion noise-figure (Fig. 20) of a receiver element is 6.5 dB at 90 GHz and remains below 7 dB between 75 GHz to 95 GHz. The input matching is better than −10 dB between 82 GHz to 105 GHz for each element to the 50-ohm source. The input compression point of the receiver elements is better than −35 dBm between 70 GHz to 102 GHz (Fig. 21).

Fig. 22 shows the phase and amplitude error of a receiver element versus the input RF frequency. The phase and amplitude imbalance remain better than $\pm 2^{\circ}$ and ± 0.5 dB between 81.5 GHz and 100.5 GHz respectively.

C. I/Q Phased Array Transmitter Measurements

The I/Q transmitter produces a maximum saturated output power of 8.5 dBm per element and higher than 5 dBm between 70 GHz to 100 GHz (Fig. 21). The image and LO rejection of the transmitter are shown in Fig. 22. With calibration, the image signal at 90 GHz can be suppressed to below 40 dB. The LO rejection is achieved by applying a small differential DC signal to each of the IF input terminals.

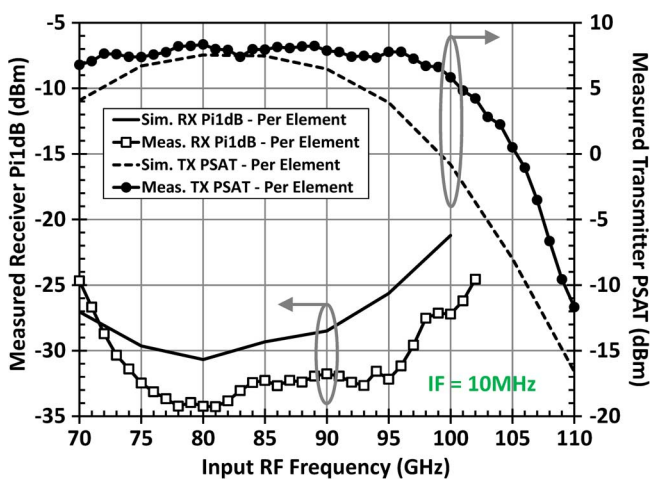

Fig. 21. Simulated and measured receiver input compression point (Pi1dB) and transmitter saturated output power (PSAT) per element.

TABLE I
COMPARISON OF THE REPORTED STATE-OF-THE-ART SILICON TRANSCEIVERS AND PHASED ARRAYS

	This Work	[10,12]	[16]	[15]	[5]
Frequency (GHz)	**70-100**	51-65	76-84	57-62	55-65
# of Elements	**4**	16	16	4	1
Function	**TX/RX**	TX/RX	RX	TX/RX	TX/RX
Conversion	**Direct I/Q**	Sliding IF I/Q	Direct I/Q	No	Direct
Phase Shifting	**Active RF**	Passive RF	Active RF	Passive RF	No
Bandwidth (GHz)	**20**	13	10	5	10
Gain Per Element (dB)	**> 25**	58	> 28	25	> 10
PSAT Per Element (dBm)	**> 6**	10	N/A	7	2.4
NF Per Element (dB)	**< 7**	7.6	< 13.5	< 10	< 6
Calibration	**Yes**	Yes	Yes	No	No
Constellation	**16QAM - 32QAM**	16QAM	FMCW	N/A	BPSK
Integration Level	**Die-on-PCB Antenna-on-PCB Beam former I/Q direct conv. IQ calibration Digital interface**	Organic BGA Beam former Freq. conv. Synthesizer IQ calibration Digital Interface	Beam former I/Q direct conv. I/Q calibration Self-test Digital interface	Antenna-in-pak. Beam former	Direct conv.
Antenna Substrate	**Megron-6**	LTCC	N/A	LTCC	N/A (Horn)
Wireless TX/RX	**Yes/Yes**	Yes/Yes	No	No/No	Yes/Yes
Wireless Data Rate (Gb/s)	**10**	5.3	N/A	N/A	6
Power / Channel (W)	**0.5 (TX + RX)**	0.35 (TX + RX)	0.075 (RX)	0.145 (TX + RX)	0.374 (TX + RX)
Area (mm^2)	**1.7 x 2**	6.5 x 6.75	5.5 x 5.8	2 x 2	1.28 x 0.81
Process (f_T / f_{MAX})	**BiCMOS 0.18µm 240/270G**	BiCMOS 0.12µm 200GHz	BiCMOS 0.12µm 200 GHz	65nm CMOS N/A	65nm CMOS N/A

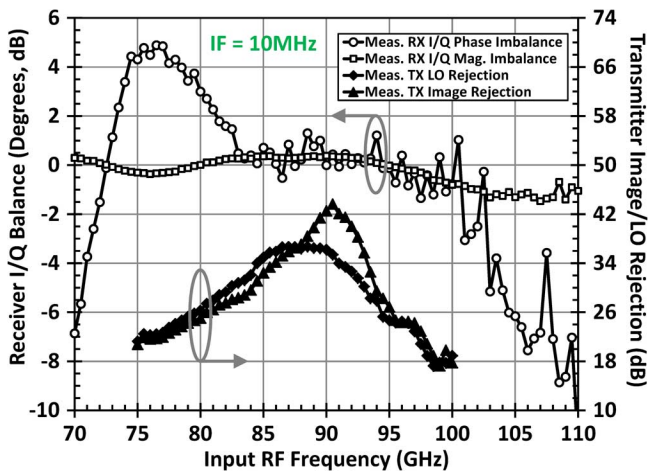

Fig. 22. Measured receiver phase/magnitude error and transmitter image/LO rejection after calibration at 90 GHz.

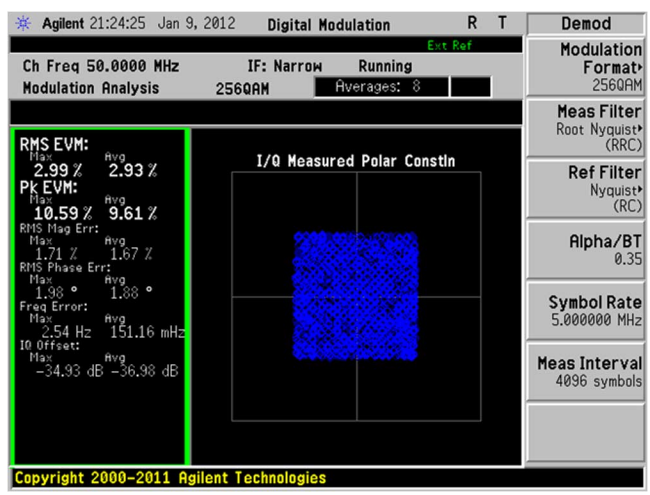

Fig. 23. Measured transmitted 256-QAM constellation at 90 GHz carrier frequency. Output power is 0 dBm per channel.

A transmitted 256-QAM constellation with 3% EVM is shown in Fig. 23. Demodulation symbol rate is limited by the instrument to 5 MS/s. The total transmitted output power is 0 dBm per channel which corresponds to an 8 dBm backoff from the saturated output power.

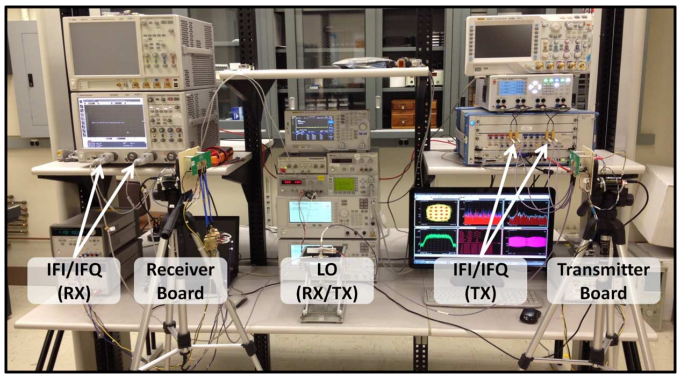

Fig. 24. Photograph of the established wireless link setup. The transmitter and receiver PCBs are mounted on tripods which are spaced 1-meter apart.

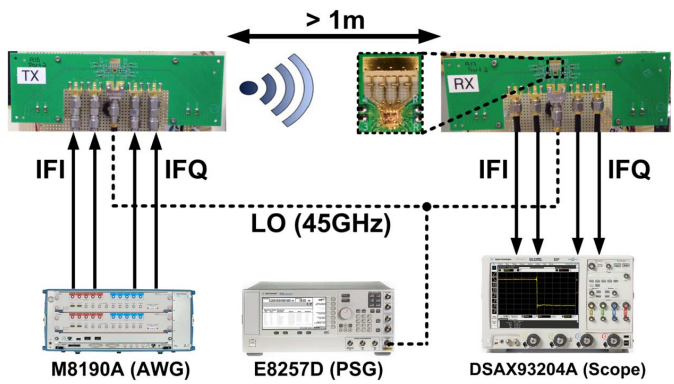

Fig. 25. Simplified block diagram of the wireless link measurement setup. The arbitrary waveform generator (AWG) and the oscilloscope are controlled from a PC running Agilent VSA software suite.

D. Wireless Link Demonstration

Fig. 24 shows a photograph of the wireless link setup. The transmitter and receiver PCBs are mounted on tripods which are spaced 1-meter apart. Both phased arrays interface with a computer through USB-SPI converters for programming calibration and bias settings. The transmitter baseband data is provided by an Agilent M8190A arbitrary waveform generator which interfaces directly with the transmitter PCB. The received baseband signal is digitized by an Agilent DSA93204A oscilloscope and analyzed by Agilent VSA software which performs constellation analysis. An Agilent E8257D signal generator provides the half-rate LO signal to both PCBs. The simplified block diagram of the wireless link is shown in Fig. 25.

At a distance of 1-meter, a 2.5 GBaud/s 16-QAM or 1.75 GBaud/s 32-QAM link can be established with a measured EVM of 8.1% and 6.6% respectively. The measured SNR in both cases is approximately 20 dB. Lower data rates are also achievable at longer distances. The measured spectrum, constellation and performance parameters are shown in Fig. 26.

V. Conclusions

In this paper we demonstrated a 4-channel receiver and transmitter array with integrated direct-conversion mixers. Our solution covers a wide frequency range (70–95 GHz) with low receiver noise (<7 dB), good transmit output power (>5 dBm)

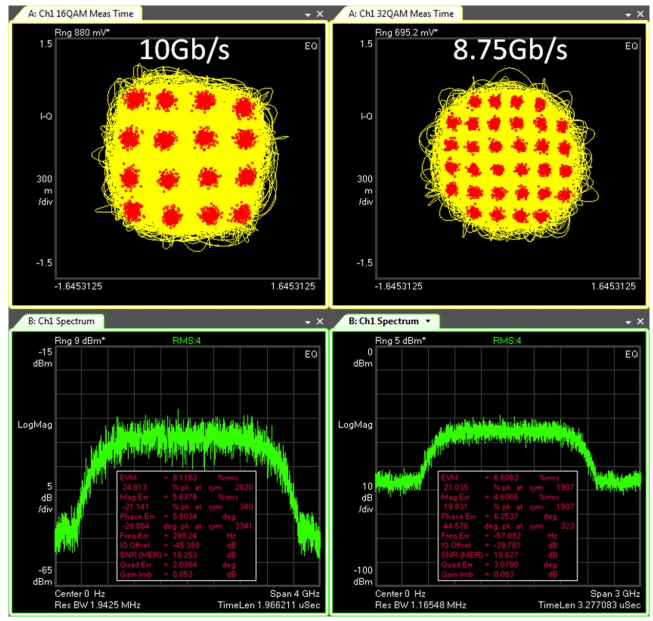

Fig. 26. Measured constellation and spectrum of the complete wireless link operating using an 88 GHz carrier. At a distance of 1-meter, a 2.5 GBaud/s 16-QAM (left) or 1.75 GBaud/s 32-QAM (right) link can be established with a measured EVM of 8.1% and 6.6% respectively.

from each element. Active accurate calibration for both array phase and amplitude settings enable mitigation of I/Q amplitude and phase mismatch in the direct-conversion architecture. This calibration can be performed at any of the frequencies within the 70–100 GHz band. By employing a chip- and antenna-on-PCB design, a 10 Gb/s wireless link is demonstrated at a distance of 1 meter with an 88 GHz carrier. This work is compared with existing state-of-the art mm-wave arrays and transceivers in Table I.

Acknowledgment

The authors would like to acknowledge Dr. Joseph Weiner for his aid in designing the phased array PCBs and CAD support, Dr. Ut-Va Koc for digital synthesis, Dr. Ian Rippke from Agilent for his expertise with the GoldenGate simulator, and Dr. Jeffrey Sian Chong Lee for his support during the wireless transmission experiments.

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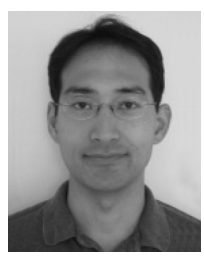

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