Design of UWB Cascode SiGe BiCMOS LNA with Current Reuse

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Abstract —**A Cascode SiGe BiCMOS low-noise amplifier (LNA) is presented for ultra-wideband (UWB) application. The emitter degenerative inductive technique is employed to achieve input impedance matching and optimize the noise performance. The output impedance matching is achieved by resistance-inductor shunt feedback. The current reuse topology is adopted to achieve high gain with low power consumption. Based on TSMC 0.35μm SiGe BiCMOS process, the topology and chip layout of the proposed LNA have been designed, its area is 0.62×0.64 mm^2. The simulation results of the LNA demonstrate that in the range of UWB, the noise figure is 2.6~4.1 dB, the gain is 19.3~20.8 dB, gain flatness is ±0.75 dB, linearity is -4~-7dBm, the input and output match well, the LNA is unconditionally stable in the whole band.**

I. INTRODUCTION

In the recent few years, for the demand of high data-rate wireless communications, the standard of Ultra-Wideband (UWB) was set up and authorized the unlicensed 7.5 GHz band (3.1-10.6GHz) by Federal Communications Commission (FCC) in 2002. UWB receivers have some advantages of strong anti-interference, high transmission rate, wide frequency bandwidth, and low cost [1]. As the first stage of UWB receivers, UWB low noise amplifier (LNA) performance has an important influence on whole receiver system. UWB LNA should have low noise figure, high gain, good gain flatness, impedance matching, good linearity in order to suppress interference between adjacent channel [2], and absolute stability in the whole band.

SiGe HBT is gradually applied in RF circuit design for some advantages such as large output impedance, large gain, good frequency characteristics, good compatibility with Si and CMOS process. In this paper, the emitter degeneration inductive technique is adopted to achieve input impedance matching. the noise performance of LNA is analyzed. In order to achieve high gain performance with low power consumption, the LNA with current reuse topology is proposed. The topology and chip layout of the proposed UWB LNA have been designed base on TSMC 0.35μm SiGe BiCMOS process. It achieves high power gain and superior noise performance with low power consumption.

II. THEORY AND TOPOLOGY OF PROPOSED LNA

A. Impedance matching and noise analysis

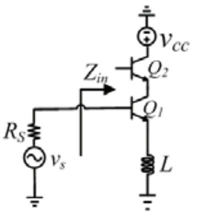

Figure 1.Cascode amplifier with emitter degenerative inductive

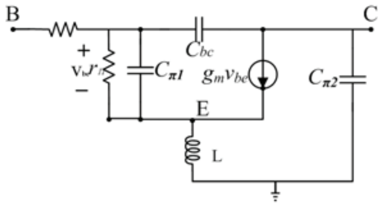

Figure2 small signal equivalent circuit

The Cascode amplifier is used as the input stage of the LNA with the advantages of high reverse isolation and good frequency characteristic. Since the LNA is the first component of the receiver, in order to reduce the distortion caused by signal reflection, the input impedance must be matched to the source impedance (50 ohm). The emitter degenerative inductive technique is used to achieve UWB input impedance matching for Cascode amplifier. The topology and small signal equivalent circuit is shown in Fig. 1 and Fig. 2, respectively. Input impedance Z_{IN} of the amplifier is given as follows:

$$Z_{in} = r_b + \frac{1}{jwC_\pi} + jwL + \frac{L \cdot g_m}{C_\pi} \quad (1)$$

The input impedance matching can be achieved by adjusting the inductive value and the bias current of the circuit. In order to achieve the impedance matching, the transistor with four base fingers and 10μm emitter length is chose as the common emitter transistor of cascode amplifier, the value of inductor L is 0.3 nH.

According to the Friis noise figure equation of cascade amplifier [3], when the gain of the first stage is high enough in the LNA, the total *NF* of the LNA is mainly dominated by the first stage. Therefore, it is assumed that the overall noise figure is mainly due to the first stage in the following analysis. The common base stage in the Cascode amplifier with emitter degenerative inductive technique has a current gain close to unity and adds some noise to the LNA. This noise from the common-base transistor is very small at the output compared with the noise from the common-emitter stage. Thus, for simplification of calculation, the common base part is omitted.

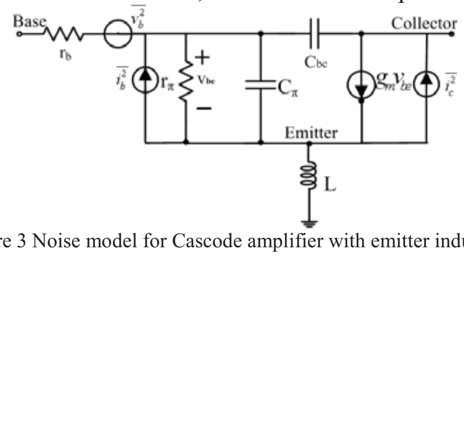

Figure 3 Noise model for Cascode amplifier with emitter inductive

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The noise model for cascode amplifier with emitter degenerative inductive is shown in Fig. 3. The noise sources are expressed as:

$$\overline{v_b^2} = 4kTr_b\Delta f$$
$$\overline{i_b^2} = 2qI_B\Delta f \qquad (2)$$
$$\overline{i_c^2} = 2qI_C\Delta f$$

where r_b is the base series resistance, k is Boltzmann's constant, q is the electron charge, T is absolute temperature in degrees Kelvin, Δf is frequency bandwidth of interest. The noise parameters (equivalent noise resistance R_n, the optimum noise impedance Z_{OPT}, the minimum noise figure NF_{min}) of the cascode amplifier are derived as follows:

$$R_n = R_b + \frac{1}{2}\left(\frac{g_m}{\beta} + g_m\frac{w^2}{w_T^2}\right)w^2L_e^2 + \frac{1}{2g_m} - \frac{w}{w_T}wL_e$$

$$Z_{OPT} = \frac{1}{g_m/\beta + g_m\, w^2/w_T^2}\sqrt{2\left(g_m/\beta + g_m\, w^2/w_T^2\right)R_b + \frac{1}{\beta}} \qquad (3)$$

$$+ j\left(\frac{w}{\left(g_m/\beta + g_m\, w^2/w_T^2\right)w_T} - wL_e\right)$$

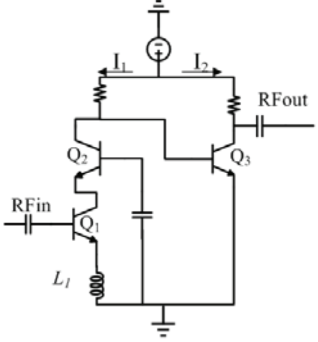
$$NF_{\min} = 1 + 2\sqrt{\left(g_m/\beta + g_m\bullet w^2/w_T^2\right) + \frac{1}{\beta}}$$

The NF is calculated as:

$$NF = NF_{\min} + \frac{2\left(g_m/\beta + g_m\, w^2/w_T^2\right)}{R_S}\left|Z_{OPT} - Z_S\right|^2 \qquad (4)$$

where, $g_m = qI_C/kT$, β is the current gain, $w_T = g_m/(C_\pi + C_{bc})$. The size and bias current of the transistor have been set to achieve the input impedance matching, According to the Eq. (3), the emitter inductor decreases the optimum noise impedance without affects the minimum noise figure. Therefore the noise figure is reduced from Eq. (3). According to the analysis, the input impedance can be matched and the noise figure can also be reduced by the emitter degenerative inductive technique.

B. Current reuse



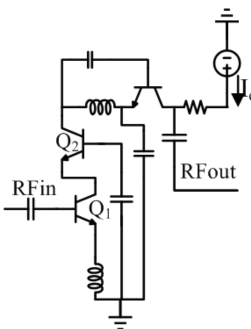


Figure 4 Cascade amplifier Figure 5 Current reuse amplifier

As shown in Fig. 4, the cascade amplifier is generally used to achieve high gain, but the gain is improved at the expense of increasing power dissipation. In order to achieve high gain without increasing the power dissipation, a new circuit topology with current reuse is proposed, which is shown in Fig. 5. The current reuse topology is composed of two stages amplifiers, which reduces current consumption through the reuse of the bias current in the DC path. The input stage of the LNA is the Cascode amplifier. Common base stage of which reduces the miller effect and improves isolation from output return signal. After the signal is amplified by the Cascode input stage, the series inductor L_2 provides a high impedance path to block the signal, the capacitor C_2 decouple the AC interaction between the first and second stage over the frequencies of interest, therefore the signal can once again be amplified by the second stage of current reuse amplifier. As shown in Fig. 4 and Fig. 5, the total DC power consumption of cascade amplifier and current reuse amplifier are obtained respectively as follows:

$$P_{cascade} = V_{cc1} \times (I_1 + I_2) \qquad (5)$$
$$P_{current-reuse} = V_{cc2} \times I_c$$

According to the Eq. (5), when the input impedance of cascade amplifier and current reuse amplifier are all matched well with the same input stage, I_1 should be equal to I_c. Consequently, the DC power consumption of the current-reuse amplifier is the half of the cascade amplifier.

Since the current gain from the emitter to collector of common base transistor Q_2 is nearly unity, the effective transconductance of the cascode amplifier is equal to the transconductance of Q_1[3]. So the effective transconductances of cascade amplifier and current reuse amplifier are obtained as

$$G_{cascade} = G_{current-reuse} \approx g_{m,Q_1} \times g_{m,Q_3} \qquad (6)$$

When the $V_{cc1}=V_{cc2}$, $I_1=I_2=I_C$, we can know that the current reuse amplifier reduce the power consumption with high power gain.

C. Topology and layout of proposed LNA

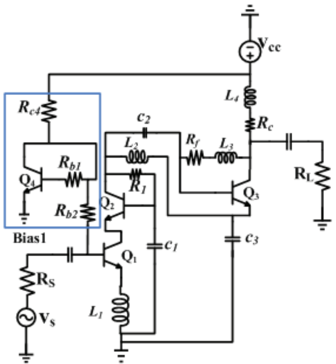


Figure 6 Topology of the proposed UWB LNA

Based on TSMC 0.35μm SiGe BiCMOS process, the topology and chip layout of the proposed UWB LNA with current reuse have been designed, and are shown in Fig. 6 and Fig. 7. The input impedance matching is achieved by emitter inductor L_1, and output impedance matching is achieved by R_f-L_3 shunt feedback. Resistance R_f and R_1 are used for self-biasing for Q_3 and Q_2. Q_4 and Q_1 constitute mirror current sources Bias1 to provide stable bias current for transistors Q_1. Inductor L_2 and capacitor C_2 are used for the current reuse structure. The chip layout of the UWB LNA is shown in Fig. 7. The total area is $0.62 \times 0.64\ mm^2$.

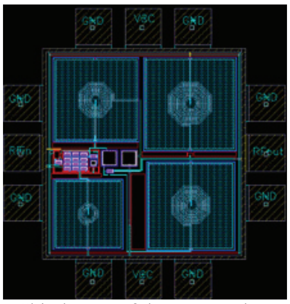


Figure 7 Chip layout of the proposed UWB LNA

III. VERIFICTION AND RESULTS ANALYSIS

Based on TSMC 0.35μm SiGe BiCMOS process, the proposed LNA is simulated by using the Spectre of Cadence Design Systems Inc and the current reuse technology is verified.

Fig. 8 depicts the S_{21} of the proposed UWB LNA with current reuse structure from 3.1 to 10.6 GHz. The proposed LNA with current reuse also have high gain S_{21} compared with the cascade LNA, the peak of S_{21} is 20.8 at 8.6GHz. The gain S_{21} and gain flatness are 19.3~20.8dB and ±0.75dB from 3.1 to 10.6 GHz. The result demonstrates that the current reuse can indeed achieve high UWB S_{21} characteristics. That verifies the validity of the proposed current reuse. The proposed LNA has good noise performance, the noise figure is 2.6~4.1 dB from Fig. 8

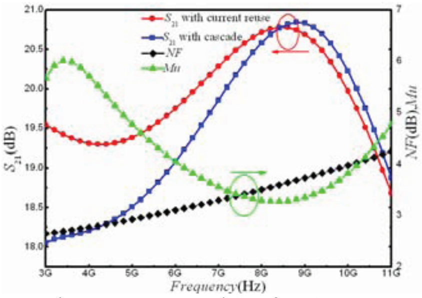


Figure 8 *NF*, *Mu*, and S_{21} of LNA

In RF circuit design, input return loss S_{11} and output return loss S_{22} are all less than -10 dB. Fig. 9 depicts the S_{11}, S_{22}, reverse isolation S_{12} from 3.1 to 10.6 GHz. S_{11} and S_{22} are all lower than -10 dB while S_{12} is lower than -42 dB up to 11 GHz. This LNA has good impedance matching and reverse isolation in the whole band.

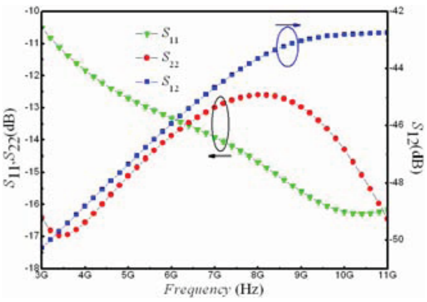


Figure 9 S_{11}, S_{22}, S_{12} of LNA

In RF circuit, when the stable factor *Mu* of the LNA is larger than 1 the LNA is absolute stability. Fig. 8 shows the *Mu* of LNA from 3.1 to 10.6 GHz. The stable factor is larger than 3, the LNA is absolute stability from 3.1 to 10.6 GHz. As shown in Fig. 10, the IIP_3 (input 3rd order intercept point) of the LNA is -4 dBm at 6GHz, when a two tone test is performed with 10MHz spacing. IIP_3 of this proposed LNA is -4~-7 dBm in the whole band from Fig. 11. Therefore this proposed LNA have good linearity.

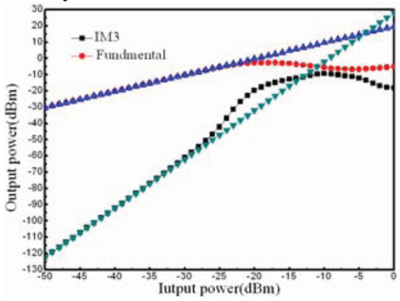


Figure10 IIP_3 of LNA at 6GHz

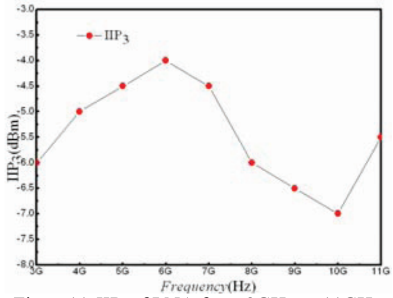


Figure11 IIP_3 of LNA from 3GHz to 11GHz

IV. CONCLUSION

An UWB SiGe LNA employing current reuse has been proposed. By utilizing emitter degenerative inductive technology, input impedance matching and noise optimization are achieved. The current reuse technology is applied to achieve high gain with low power consumption. The topology and chip layout were designed. The results demonstrate that the proposed LNA has high gain, good gain flatness, NF and linearity over the whole UWB band, meets the requirement of UWB receivers.

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