Impact of High Frequency Correlated Noise on SiGe HBT Low Noise Amplifier Design

Pei Shen[1,2], Guofu Niu[1], Ziyan Xu[1] and Wanrong Zhang[2]

[1]Electrical and Computer Engineering Department, Auburn University, Auburn, AL 36849, USA
[2] Beijing University of Technology, Beijing, 100124, China

***Abstract* — This paper investigates the impact of high frequency noise correlation on SiGe HBT LNA design. With correlation, simultaneous noise and impedance match is found to continue to hold approximately. However, a larger size and hence a higher biasing current are required for noise matching. The actual noise figure (*NF*) of LNAs designed without considering noise correlation is also investigated. Further investigation shows that a size considerably smaller than noise matching size is more preferable, as it produces high gain, high linearity and *NF* only slightly higher noise figure at much smaller power consumption.**

***Index Terms* — Cascode LNA, high frequency noise correlation, emitter length, noise figure.**

I. Introduction

Noise figure of a RF system is to a large extent determined by the noise figure of the low noise amplifier (LNA), which in turn depends on circuit design as well as noise sources in the transistors used. At present, two kinds of noise sources are included in SiGe HBT design kits used by RFIC designers: 1) thermal noise of terminal resistances, and 2) noise in the terminal base and collector currents. The later is described with a simplified model that assumes both base and collector current noises are shot like and uncorrelated with each other:

$$S_{i_b i_b^*} = 2qI_B, \tag{1}$$

$$S_{i_c i_c^*} = 2qI_C, \tag{2}$$

$$S_{i_c, i_b^*} = 0, \tag{3}$$

which is often referred to as the SPICE noise model, as it is used in SPICE like simulators.

At RF, various noise physics mechanisms come into play, primarily causing a frequency dependent correlation between base and collector current noises. For a modern SiGe HBT process, we have shown previously that the collector-base junction space charge region noise transport contributes significantly to noise correlation [1], and developed a new physics-based large signal noise model, together with a Verilog-A implementation.

The purpose of this work is to investigate the impact of noise correlation on LNA design. We will first examine its impact on simultaneous noise and input impedance matching in emitter inductor degenerated LNAs, a desired coincidence that was previously derived using the SPICE noise model [2]. We will show that simultaneous matching continues to hold approximately, but a larger transistor and higher power consumption are required in presence of noise correlation. We further evaluate the "real" noise figure of LNAs designed using the SPICE noise models, and found them to be fairly comparable to the real noise figure of LNAs designed using the new model. Transistor size optimization is then investigated.

II. Technology and Compact Model

The HBTs used are from IBM's 5PAE SiGe HBT BiCMOS technology. The design kit uses the HICUM model for HBTs. The new noise model of [1] is used. The noise equations are implemented in a form compatible with a Verilog-A implementation of HICUM. Details of the model and Verilog-A implementation can be found in [1]. The collector-base junction transit time parameter was extracted by fitting measured noise parameters. Other compact model parameters were extracted by fitting dc I-V curves and y-parameters.

Fig. 1 shows the modeled and measured noise parameters versus current density (J_C) at V_{CE}=3.3 V and f=5 GHz, including the minimum noise figure (NF_{min}), noise resistance (R_n), real and imaginary part of noise matching source impedance (R_{opt} and X_{opt}). The SiGe HBT used has an emitter area of 0.8 ×20×3 μm^2, a peak f_T of 36 GHz and a peak f_{max} of 65 GHz. Noise measurements were made using a commercial system. Noises of the probing pads and interconnects from the pads to HBT terminals are de-embedded with open-short method. The new noise model produces much more accurate noise parameters than the SPICE noise model. Observe that the noise matching source resistance R_{opt} from measurement and new model are higher than from the SPICE model. Consequently, at a given current density J_C (or V_{BE}), for noise matching through transistor sizing, one needs to use a larger size than given by the SPICE model, as detailed below.

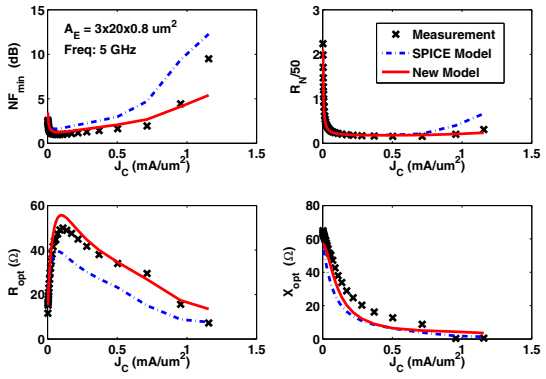

Fig. 1. Modeled and measured noise parameters versus J_C at 5GHz.

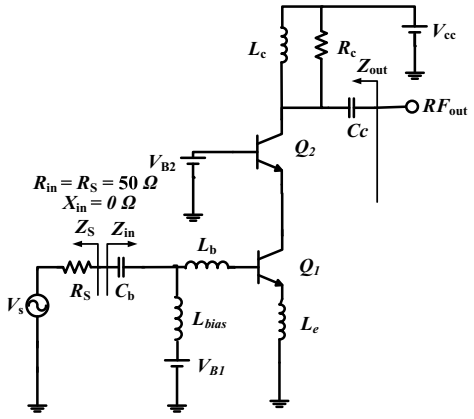

Fig. 2. Schematic of the SiGe HBT cascode LNA used.

III. Simultaneous Noise and Impedance Matching

An important RF property of bipolar transistor derived in [2] is that simultaneous noise and input impedance match can be achieved through transistor sizing and the use of two inductors placed at the emitter and base. At a given J_C, real part of noise matching is achieved by adjusting transistor size such that R_{opt}=50 Ω. An emitter inductor L_e provides an input resistance R_{in}=50 Ω. A base inductor L_b cancels out the input reactance and at the same time transforms the source noise matching reactance of the LNA to 0 Ω.

This important property that highly simplifies RF LNA design, however, was derived using the SPICE noise model that does not consider the frequency dependent correlation, together with additional approximations. A logical question is how frequency dependent correlation affects simultaneous noise and (input) impedance matching.

To address this question, we design LNAs using both SPICE and new noise models as follows. At a given J_C:

1. Choose emitter length L_E so that R_{opt}=50 Ω.
2. Optimize emitter and base inductors L_e and L_b for input impedance match.

As no optimization or consideration is given for reactance noise matching, the closeness of the resulting LNA noise matching reactance X_{opt} to 0 Ω can be used as an indicator of the closeness of source noise matching and input impedance matching. The process is then repeated for different J_C. The sweep is also useful in adding another dimension to design optimization. The simulator used is Agilent ADS, which supports Verilog-A compact model and optimization. A cascode topology shown in Fig. 2 is chosen for its better reverse isolation and excellent frequency stability [3]. C_b is for DC blocking, and L_{bias} is for AC blocking. Here we choose to use the same size for Q_1 and Q_2. Size adjustment is made by changing emitter length (L_E). We also optimize L_c and C_c for output impedance matching. R_c is fixed during optimization but can be optimized as well.

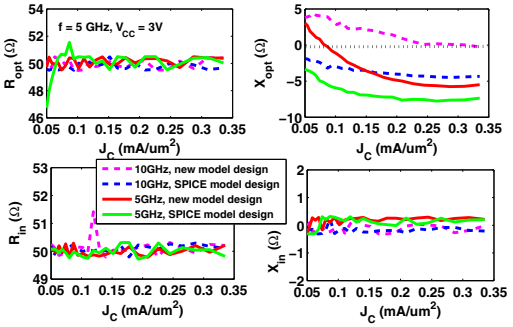

Fig. 3. Real and imaginary part of noise matching source impedance and input impedance for SPICE model and new model designed LNAs versus J_C at 5 GHz and 10 GHz.

Fig. 3 shows the noise matching source impedance and input impedance of designs using both noise models versus J_C at 5 GHz and 10 GHz. For both models, input impedance is matched within the used optimization tolerance. Real part noise matching is achieved using the size calculated from R_{opt} per emitter length, without optimization. With noise correlation, noise matching and impedance matching turned out to be even closer, as $X_{opt,LNA}$ is closer to 0 Ω. The closeness is better at higher frequency than at lower frequency.

IV. LNA Performance

A. SPICE vs New Model Designs

Fig. 4 shows the emitter length (L_E) and I_C of LNAs designed using the SPICE model and new model versus J_C at 5GHz. Note that a new design is made at each J_C. For the J_C, a larger emitter length is required for source resistance noise match, i.e. R_{opt} = 50 Ω, in all the new noise model LNA designs. This directly translates into a *higher* I_C and thus higher power consumption at simultaneous noise and

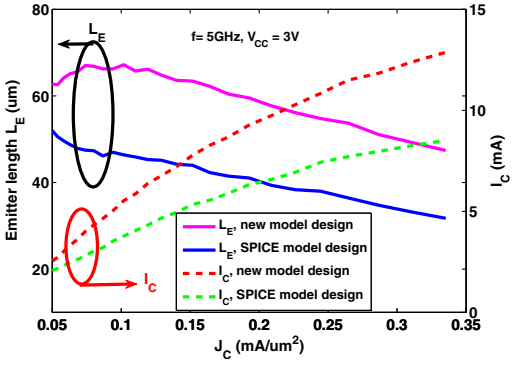

Fig. 4. Emitter length (L_E) for R_{opt}=50Ω and I_C versus J_C at 5 GHz.

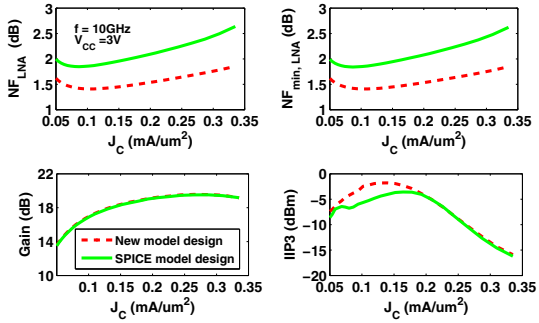

Fig. 5. NF_{LNA}, $NF_{min,LNA}$, gain and IIP3 of SPICE model and new noise model designed LNAs versus J_C at 5GHz.

input impedance matching.

The root cause of this can be found from transistor R_{opt} difference between two models. As was shown in Fig. 1, for the same transistor size, the new model R_{opt} is higher than SPICE model R_{opt}. Compared to measurements and the new model, the SPICE noise model underestimates R_{opt}, and consequently requires a smaller emitter length for adjusting R_{opt} to 50 Ω. At the same J_C, this means a higher I_C in the new model LNA designs. However, as we will show below, one does not need exact noise matching (sizing) and can use smaller sizes to save power with just a slight increase of LNA noise figure.

Fig. 5 shows NF_{LNA}, $NF_{min,LNA}$, gain and IIP3 of versus J_C at 5GHz. For designs made using both models, NF_{LNA} is nearly identical to $NF_{min,LNA}$. Given that noise matching is done for both model designs, NF_{LNA} follows NF_{min}, which is higher for the SPICE model, as we expect from transistor level modeling shown earlier in Fig. 1.

Gain is approximately the same for designs using both models. IIP3, however, is better for the new model designs for $J_C < 0.2$ mA/μm^2.

B. Real Performance of SPICE Model Designs

Given the fact that designers have been using the inaccurate but nevertheless de facto industry "standard" SPICE noise model to produce working SiGe HBT LNAs, we logically would like to know what the actual performance of the SPICE noise model designed LNAs would be. To find out the answer, we re-simulated the SPICE model designed LNAs using our new noise model. The new model simulated performance can be viewed as the "real" performance of the SPICE model designed LNAs.

Fig. 6 compares the simulated "real" noise performance of designs made using both noise models. First, "real" NF_{LNA} of SPICE model designs is lower than its designed noise figure, i.e. SPICE model simulated noise figure. Second, perhaps surprisingly, the "real" noise figure of the SPICE model designs is fairly close to the noise figure of the new model designs, despite the clear inaccuracy of the SPICE noise model used in the design. Gain and linearity are similar.

Practically speaking, the SPICE model designed LNAs show fairly comparable performance at a smaller I_C, which originates from the smaller (and inaccurate) transistor R_{opt} modeling.

To understand why the "real" noise figure of SPICE model designs is close to that of the new model designs despite inaccuracy of the SPICE noise model, we rewrite the noise factor F expression as follows:

$$F = F_{min} + \frac{G_n}{R_S}\left|Z_S - Z_{opt,LNA}\right|^2 \quad (4)$$

$$= F_{min} + \frac{G_n}{R_S}\left(\left|R_S - R_{opt,LNA}\right|^2 + \left|X_S - X_{opt,LNA}\right|^2\right), \quad (5)$$

where G_n is the noise conductance, and other symbols have their usual meanings. $NF = 10\log_{10}F$.

Fig. 7 compares the "real" (meaning simulated using the new model) $\triangle R$, $\triangle X$, $\triangle F$ and noise conductance (G_n) for both SPICE model and new model LNA designs. Inaccuracy of the SPICE noise model causes deviation from noise matching, which is primarily reflected by a larger $\triangle R$. $\triangle X$, on the other hand, is about the same for both type of designs. However, the noise conductance G_n remains small enough such that the resulting ΔF is small compared to F_{min}. As a result, NF_{LNA} is still dominated by $NF_{min,LNA}$. The "real" noise figure is thus only slightly higher in SPICE model designed LNAs.

One should also notice that ΔX is on the order of a few Ω. Therefore, transistor sizing for R_{opt}=50 Ω does not need to be better than say 6 Ω.

C. Size Optimization

We have seen that even a 20 Ω deviation of R_{opt} from R_s=50 Ω caused less than 0.1 dB increase of noise figure. Power saving, however, is appreciable compared to sizing the transistor for R_{opt}=50 Ω. This observation is in a way

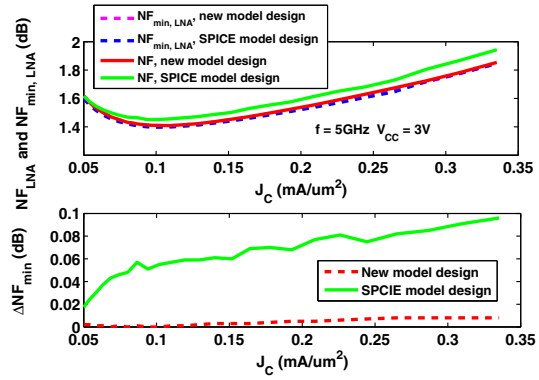

Fig. 6. Comparison of the simulated "real" noise performances of SPICE model and and new model designed LNAs versus J_C at 5GHz.

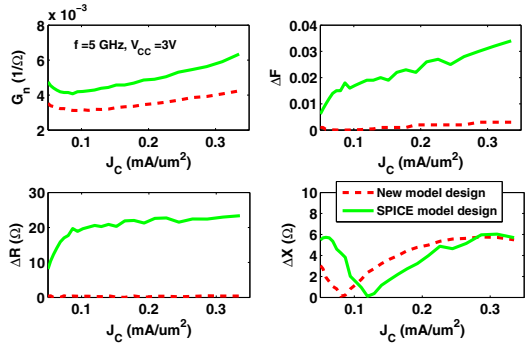

Fig. 7. Comparison of the "real" $\triangle R$, $\triangle X$, $\triangle F$ and noise conductance (G_n) for SPICE model and new model designed LNAs versus J_C at 5GHz.

consistent with recent report of intentional use of transistor sizes with $R_{opt} > 50\Omega$ for power saving and linearity enhancement, e.g. in [4].

To examine size optimization, for a given J_C, we vary transistor emitter length, and repeat LNA design for each emitter length. Results are shown in Fig. 8 for J_C=0.178 mA/μm^2. The emitter lengths corresponding to R_{opt}=50 Ω are 41.46 μm and 61.42 μm, for the SPICE and new noise models, respectively. The I_C's are 5.9 and 8.7 mA, for the SPICE and new noise models, respectively. $X_{opt,LNA}$ is fairly close to 0 Ω for most part, even though the exact 0 Ω occurs at 28.46 μm, far away from 61.42 μm required for R_{opt}=50 Ω.

Gain is nearly constant above 25 μm. IIP3 shows a peak of 0.2 dBm around 40 μm. Overall, an emitter length around 30 μm, much smaller than required for R_{opt} matching (61.42 μm), is a good tradeoff that provides high gain, high linearity, low power consumption and low noise figure.

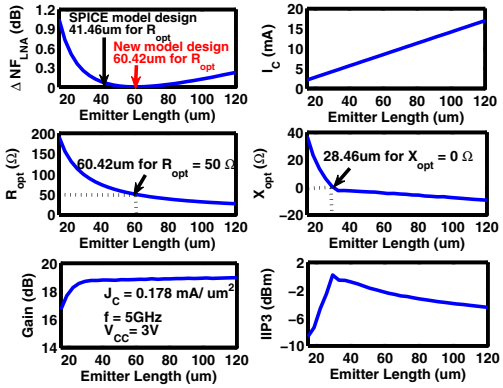

Fig. 8. $\triangle NF_{LNA}$, I_C, $R_{opt,LNA}$ $X_{opt,LNA}$, gain and IIP3 versus J_C for designs using new noise model versus emitter length at J_C=0.178 mA/μm^2 and 5GHz.

V. Conclusion

We have examined the impact of high frequency noise correlation on LNA design and performance. LNA design and simulation using a Verilog-A based new compact noise model shows that simultaneous noise and input impedance matching continues to hold in presence of high frequency noise correlation. Noise matching, however, requires a considerably larger transistor and power consumption. The actual noise figure and other performance of SPICE model designed LNAs are found to be overall comparable to that of the new model designed LNAs. The small noise conductance G_n allows significant deviation from noise matching size for power saving and linearity enhancement.

References

[1] Z. Yu, G. Niu, and M. M. Ramana, "Compact modeling of collector base junction space charge region transmit time effect on noise in SiGe HBTs," in *Dig. of SiRF*, 2010, pp. 180–183.

[2] S. P. Voinigescu, M. C. Maliepaard, J. L. Showell, G. E. Babcock, D. Marchesan, M. Schroter, P. Schvan, and D. L. Harame, "A scalable high-frequency noise model for bipolar transistors with application to optimal transistor sizing for low-noise amplifier design," *IEEE Solid State Circuits*, vol. 32, pp. 1430–1439, 1997.

[3] D. K. Shaeffer and T. H. Lee, "A 1.5-v 1.5ghz CMOS low noise amplifier," *IEEE Solid State Circuits*, vol. 32, pp. 745–759, 1997.

[4] B. Kang, J. Yu, H. Shin, S. Ko, W. Ko, S. Yang, W. Choo, and B. Park, "Design and Anylysis of a Cascode Bipolar Low-Noise Amplifier With Capacitive Shunt Feedback Under Power-Constraint," *IEEE Trans. Microw. Theory Tech.*, vol. 59, pp. 1539–1551, 2011.