A SiGe:C BiCMOS LNA for 60GHz band applications

R. R. Severino[1], T. Taris[1], Y. Deval[1], D. Belot[2], J. B. Begueret[1]

[1]IMS Laboratory, University of Bordeaux, 33405 Talence, France
[2]ST Microelectronics, site Minatec, 38016 Grenoble, France

***Abstract* — A new differential LNA dedicated to 60GHz band has been implemented in a 130nm BiCMOS technology intended for millimeter-waves (mm-Waves) applications. Focusing on the circuit implementation which is a critical design step in mm-Waves range, this work proposes a systematic modeling of layout parasitic elements leading to almost perfectly fit measurement and simulation results. The two stage cascode LNA achieves a 21.14dB maximum peak of power gain at 61.5GHz. Measured 1dB compression point is -21.2dBm, whereas the minimum simulated noise figure is 4.3dB at 60GHz. Power consumption is 10.2mW for the circuit core. This building block is also presented as a specific example of a complete design flow for mm-Waves applications.**

***Index Terms* — millimeter-waves (mm-Waves), low noise amplifier (LNA), Bipolar/BiCMOS integrated circuit, 60GHz, BiCMOS9MW, load pull.**

I. Introduction

First examples of Low Noise Amplifiers (LNAs) intended for mm-Waves 60GHz applications such as WPANs and gigabit/s data rate communications have been demonstrated during the last few years, both in Bipolar and CMOS newest technology nodes. [1]-[3]

When designing at mm-Waves frequencies, special care must be taken for both active and passive devices modeling. Indeed, any portion of metal path can be considered as a distributed passive device that alters the circuit behavior. The higher is the operating frequency, the stronger is the impact of such parasitic contributions. Unfortunately, current design kits do not furnish with proper models and extraction tools. So, designers have to develop their own models by means of electromagnetic simulations, increasing the complexity of the design flows. This feature of silicon high frequency design makes circuit implementation intricate. The aim of this work is to setup a more reliable design flow of mm-Waves building blocks based on a systematic modeling of active, passive and interconnection parasitic elements.

Hereafter a new LNA is proposed, realized in BiCMOS9MW technology from STMicroelectronics.

After shortly resuming the main features of BiCMOS9MW technology, the new LNA schematic is described in section III. A detailed mm-Waves design flow is developed, suggesting the proper way to overcome all the aforementioned difficulties related to devices and parasitic elements characterization. Moreover, it will be then demonstrated that transmission lines (T-Lines) can be used for modeling all devices interconnections in post layout simulations. RF Pads can be modeled as well. Finally, measurement results are compared with simulations in section IV.

II. 130nm BiCMOS Technology

A. Active devices

130nm BiCMOS9MW technology from STMicroelectronics offers a high speed self aligned SiGe:C HBT with 230/280GHz f_T/f_{max} and 1.6V BV_{CE0}. As reported in Fig. 1, 5µm×0.27µm NPN transistor achieves 2.8dB NF_{min} and 226GHz f_{Tmax} for a 0.8mA/µm² and a 4.4mA/µm² current density respectively. These active device features help transistor sizing in the LNA design.

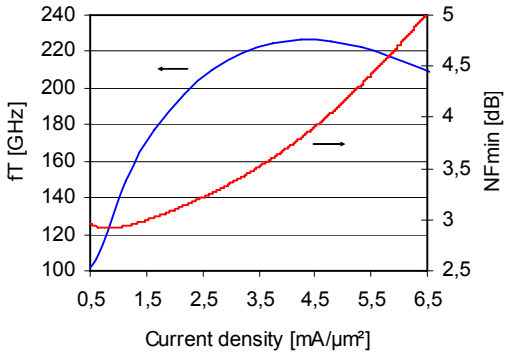

Fig. 1. $f_{T}max$ and NFmin versus current density in a 5µm×0.27µm npnvhs transistor.

B. Passive devices

130nm BiCMOS9MW is a dedicated millimeter waves back-end based on BiCMOS9 process. As depicted in Fig. 2, they differ from the 3 last Cu and oxide levels, which are set ticker in BiCMOS9MW. The quality of passive devices is improved since the attenuation constant of a 50Ω microstrip transmission line becomes close to that of above-IC BCB realizations, a roughly 0.5dB/mm at 80GHz.

Concerning design facilities, T-Lines with customized BEOL are provided, together with scalable models intended for mm-Waves applications.

MIM capacitors implemented with the two last metal levels perform a 2fF/µm² capacitance.

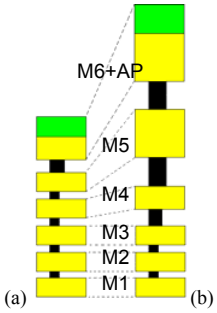

Fig. 2. Metal level backend comparison between BiCMOS9 (a) and BiCMOS9MW (b) technologies.

III. Two Stage Cascode Differential LNA Design

A. Theoretical design

Fig. 3 depicts the schematic of the 60GHz differential LNA dedicated to WLAN applications that has been implemented in the aforementioned 130nm BiCMOS9MW technology. Cascode stages have been here selected to increase reverse isolation and stability. The first stage, (Q1, Q2), performs both 50Ω input impedance and noise matching. The second stage, (Q3, Q4), improves voltage gain and provides 50Ω output matching.

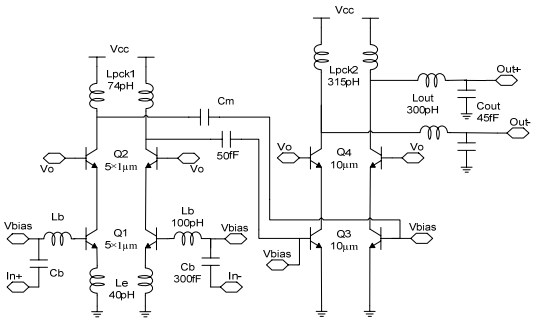

Fig. 3. Schematic of a two cascode stages LNA.

Both transistors in the first stage are implemented with five emitters of 1µm length and are biased with 3mA. Second stages transistors are sized as single 10µm emitters biased with 5.5mA.

Since the NF of a two stage amplifier depends on both stages NF and on first stage power gain, the first stage transistors (Q1, Q2) are sized on a tradeoff between minimum NF and maximum f_T optimization, enhancing the contribution of the first stage to the overall power gain and providing the optimization of the NF, according to Friis equation. Also the second stage transistors (Q3, Q4) are biased at almost the same value of current density (~2mA/µm²) in order to reduce their contribution to NF and to provide sufficient gain. The number of emitters in Q1 is set to achieve noise matching, whereas inductive degeneration (Lb, Le) achieves 50Ω input matching. Lpck1 is tuned to optimize available gain (Ga) at the operating frequency, when Cm and Q3 are connected. Lpck2 in combination with output network completes 50Ω output matching. The output network consists of a 300pH series T-Line and a 45fF shunt capacitor. With V_{CC} set to 1.2V, the DC power consumption for the LNA core is 10.2mW.

This amplifier has been realized using T-Lines for inductors implementation. The models of T-Lines provided by the Design Kit have been demonstrated to be extremely accurate at mm-Waves frequencies, whereas precise models are not provided for lumped inductors. A photo of the chip is shown in Figure 4.

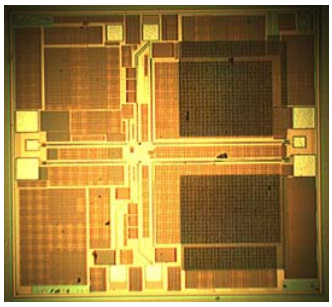

Fig. 4. LNA chip photo. Dimensions are 1254µm × 1185µm.

B. Considerations for design implementation

At the concerned frequencies, the effects of layout parasitic elements cannot be neglected, otherwise a strong frequency down-shift will occur between simulation and measurement results. In particular, three kinds of parasitic effects can be observed and are resumed as follows:

1) Parasitic capacitances at transistor level, between base, emitter, collector terminals and between these

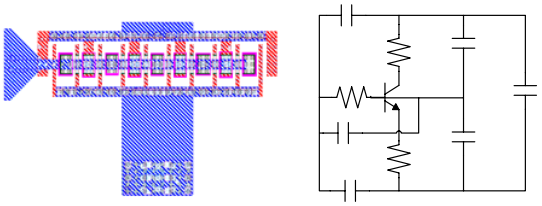

Fig. 5. Input transistor (Q1) layout with 5×1µm emitters and its equivalent model with RC parasitic elements.

terminals and the substrate. In order to take these elements into account, transistor layouts must be simulated by means of a capacitor extraction tool, such as Quickcap. A transistor model including RC parasitic elements is reported in Fig. 5. The effect of parasitic resistances due to transistor routing can be neglected.

2) none of the interconnections existing in layout, between the different circuit devices, can be considered as a short circuit contact and all of them must be modeled as distributed elements. Layout interconnections can be modeled as T-Lines of corresponding metal levels and geometries. An example, concerning the connection between two lumped resistors, is reported in Fig. 6.

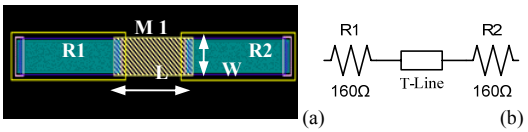

Fig. 6. Interconnection between two resistors (a) modeled as a T-line (b). All interconnections must be modeled and included in simulations.

3) MIM capacitors terminations as well as RF Pads must be considered as AluCap/Metal6 T-Lines and modeled consequently. An example, relative to a 3pF capacitor, is depicted in Fig. 7.

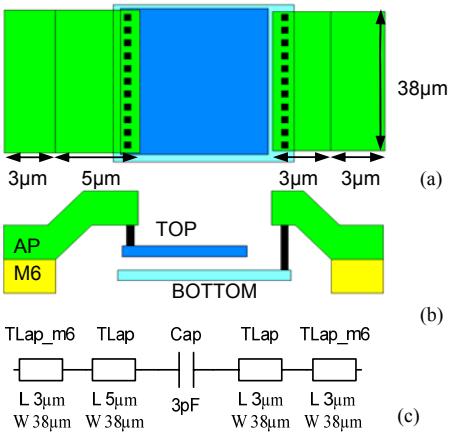

Fig. 7. 3pF MIM capacitor area (a), section (b), and its equivalent model (c). Capacitor terminals are represented as T-Lines.

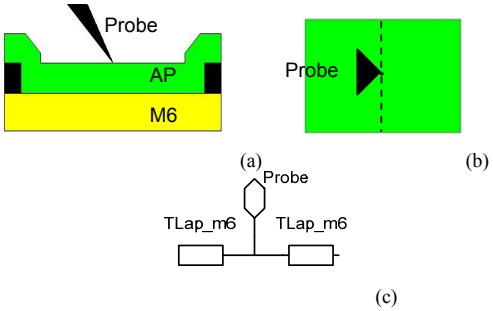

Fig. 8. RF Pad section (a), area (b), and its equivalent model (c). Pads are modeled as two T-Lines, one on each side of the test probe.

RF pads are divided into two parts following an ideal line across the centre, where the test probe is located, as shown in Fig. 8. Then, a T-line models the connection between the probe and the circuit, whereas an open T-line represents the outer side of the Pad. DC pads contribution can be neglected if enough DC decoupling is provided.

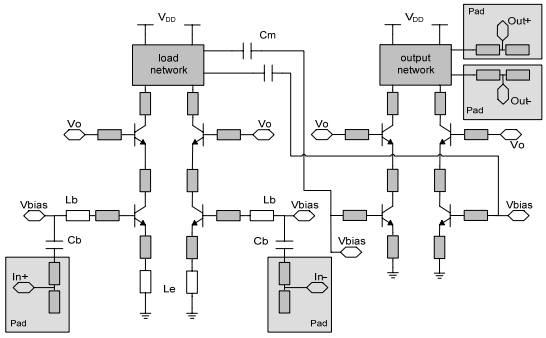

Fig. 9. New schematic of LNA with parasitic extracted models of transistors, capacitors, interconnections and RF Pads.

Taking into account the parasitic extracted models of devices, the schematic of the two stage cascode LNA, presented in Fig. 3, is modified according to Fig. 9.

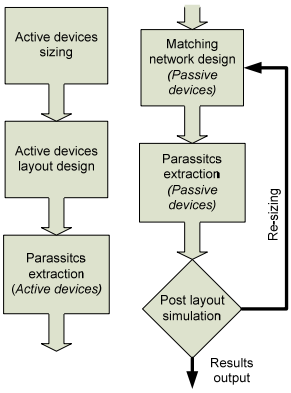

Fig. 10. Design flow for mm-Waves building blocks.

Whereas schematic and layout design are traditionally considered as two separate and consequent steps, at mm-Waves frequencies, accounting for parasitic effects leads to an embedded design flow. As a first step, schematic and layout of core devices, that is transistors, must be defined. Then parasitic extraction at transistor level is executed and the results are back annotated on the schematic. Next, matching network of passive devices such as T-Lines, capacitors and eventually lumped inductors can be designed and modeled according to the aforementioned rules. As consequences of corrections for devices interconnections, matching networks elements must be resized, following the design flow of Fig. 10. It is worth noting that the number of resizing loops is dramatically reduced as the design flow runs over the new schematic of Fig. 9.

IV. Measurement Results

Since no differential GSG probes are nowadays available in the mm-Waves range, the LNA has been characterized with single-ended measurements. To do so, one side of the differential structure of Fig. 4 is terminated on 50Ω on chip resistances. Post layout simulation and measurement results are depicted in Fig. 11.

In good agreement with post layout simulations, the power gain exhibits a maximum of 21.14dB at 61.5GHz. S11 parameter plot shows a good input impedance matching over a large bandwidth (less than -6dB between 44GHz and 110GHz) and reaches its optimum (-12.9dB) at 69GHz. The peak of S11 rising at 59GHz is due to input transistor parasitic elements (Q1). Even if its extent has been slightly underestimated by simulations, this phenomenon does not affect the performances of the amplifier.

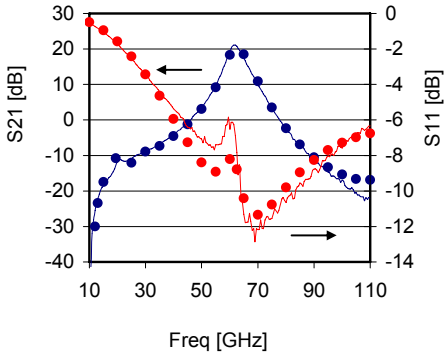

Fig. 11. Measured (line) and simulated (dot) Input Matching (S11) and Power Gain (S21).

Moreover, it can be definitely removed if a more accurate routing of input devices is accomplished. The simulated Noise Figure is shown in Fig. 12. Its minimum value is 4.3dB at 60GHz. Noise Figure measurement will be performed as soon as measurement tools will be available. The 1dB compression point has been measured by means of a load-pull test bench. At 61.5GHz it features -21.2dBm of input power. Measured reverse isolation is higher than 30dB up to 110GHz.

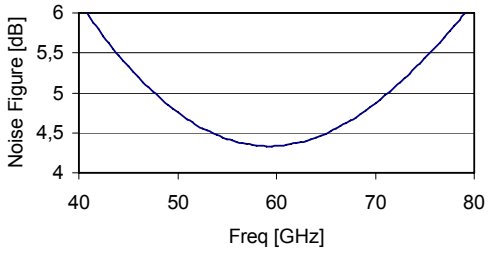

Fig. 12. Simulated Noise Figure.

As shown in Figures 11 and 13, simulations results are very close to measured data, both in small and large signal analysis. That is a proof of the correctness of the design method described in section III and its accuracy in millimeter-Waves context.

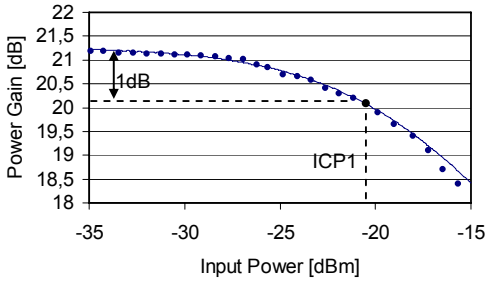

Fig. 13. Measured (line) and simulated (dot) 1dB Compression point at -21.2dBm of Input Power.

VII. Conclusion

After resuming the main features of the BiCMOS9MW technology from STMicroelectronics, a complete and effective design flow for mm-Waves applications has been defined. The efficacy of the design flow has been demonstrated by applying it to a two-stage cascode LNA design. Power gain has a 21.14dB peak at 61.5GHz and S11 is lower than -6dB between 44GHz and 110GHz. The core power consumption is 10.2mW and the minimum simulated noise figure is 4.3dB at 60GHz. Input power at 1dB compression point is -21.2dBm.

Acknowledgement

The authors wish to acknowledge STMicroelectronics for technology support and the Aquitaine Region for its financial support on the NANOCOM measurement platform.

References

[1] T. Yao, M. Q. Gordon, K. K. Tang, K. H. Yau, M. Yang, P. Schvan, and S. P. Voinigescu, "Algorithmic Design of CMOS LNAs and PAs for 60-GHz Radio," *IEEE Journal of Solid-State Circuits,* vol. 42, no. 5, pp. 1044-1057, May 2007.

[2] Y. Sun, J. Borngräber, F. Herzel, and W. Winkler, "A Fully Integrated 60 GHz LNA in SiGe:C BiCMOS Technology," *IEEE Bipolar / BiCMOS Circuits and Technology Meeting (BCTM2005),* pp. 14-17, October 2005.

[3] E. Cohen, S. Ravid, and D. Ritter, "An ultra low power LNA with 15dB gain and 4.4db NF in 90nm CMOS process for 60 GHz phase array radio," *IEEE RFIC Symposium,* pp. 14-17, June 2008.